6	1800 BAUD
7	2400 BAUD

MAINDEC-08-DHMPA-A-D

PDP-8/E EXTENDED MEM
PARITY TEST

ABSTRACT

THE PDP-8/E EXTENDED MEMORY PARITY CHECKERBOARD DIAGNOSTIC IS DESIGNED TO DETECT PARITY FAILURES ON HALF-SELECTED LINES UNDER WORST CASE NOISE CONDITIONS. THE WORST CASE PATTERN PROVIDED WILL GENERATE WORST CASE NOISE CONDITIONS IN ALL PDP-8/E PARITY STACKS. ALSO, THE PARITY ERROR INTERRUPT AND THE PARITY DATA DECODING CIRCUITS ARE CHECKED FOR PROPER OPERATION. THIS PROGRAM WILL TEST SYSTEMS EQUIPPED WITH PARITY AND FROM 8K TO 32K WORDS OF CORE MEMORY. AUTOMATIC PROGRAM RELOCATION IS PROVIDED FOR ERROR IDENTIFICATION, AND THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PROGRAM BY VARIOUS SR SETTINGS.

REQUIREMENTS

A PDP-8/E COMPUTER EQUIPPED WITH MEMORY PARITY AND AT LEAST 8K OF CORE MEMORY.

STORAGE - THIS PROGRAM OCCUPIES CORE LOCATION 0000 - 5177 AND 6400 - 6630 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE SR TO THE INSTRUCTION FIELD AND DATA FIELD OF THE STACK WHICH CONTAINS THE PROGRAM.
PRESS KEY EXTD ADDR LOAD.
SET THE SR EQUAL TO 0200.
PRESS KEYS ADDR LOAD, CLEAR, AND CONT. A SETUP SR MESSAGE WILL BE PRINTED.
SET THE SR FOR DESIRED OPERATION.
PRESS KEY CONT.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH	0 (DOWN)	1 (UP)
SR00	CONTINUE AFTER ERROR	HALT AFTER ERROR
SR01	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
SR02	NORMAL	TTY BELL ON ERROR
SR03	RELOCATE PROGRAM	INHIBIT PROGRAM RELOCATION
SR04	NORMAL	CHANGE STACK LIMITS
SR05	NORMAL	HALT AFTER CURRENT TEST
SR06-08	STARTING STACK LIMIT (0-7)	
SR09-11	ENDING STACK LIMIT (0-7)	

MAINDEC-08-DHLSA-A

LS8E LINE PRINTER TEST