IDENTIFICATION

Product Code: Maindec 08-D4AØ - D

Product Name: PDP-8, 8/I Memory Parity Checkerboard

Date Created: May 14, 1968

Maintainer: Diagnostics Group

1. Abstract

The PDP-8, 8I Memory Parity Checkerboard diagnostics tests the parity bit plane for core failure on half-selected lines under worst case conditions. Its use is intended for basic 4K memory systems.

2. Requirements

2.1 Equipment

A standard PDP-8 or 8/I equipped with a parity memory stack and associated parity control logic.

2.2 Storage

There are two versions of this Maindec. The Low End program occupies locations 0005 to 0146 octal, and tests memory from 147 to 7700 octal.

The High End program occupies locations 7430 to 7571 octal, and tests memory from 100 to 7400 octal.

2.3 Preliminary Programs

The RIM loader must be in locations 7756 to 7776 octal.

3. Loading Procedure

3.1 Method

Load the program with the RIM loader.

a. Turn off the teletype reader.
b. Set the SWITCH REGISTER to 7756.
c. Press LOAD ADDRESS, and then START.
d. Place the program tape in the reader and turn on the reader.
e. When the program has been loaded, stop the computer, turn off the reader, and remove the tape.

4. Starting Procedure

4.1 Starting Addresses

0005 Low End Checkerboard
7430 High End Checkerboard

4.2 Control Switch Settings

One of the four possible patterns that can be written in memory is obtainable by each of the following SR settings:

0100 (This setting is used for the standard PDP-8 core unit.)

0101 (This setting is used for the standard PDP-8/I core unit.)

0000 (These are for special core units from other suppliers.)
0001

4.3 Operator Action

With the program in memory, set the SWITCH REGISTER to the starting address, 0005 for Low End or 7430 for High End.

Press LOAD ADDRESS.

Set the SWITCH REGISTER to one of the four settings given in section 4.2 to obtain the correct pattern. For most PDP-8's this will be 0100. For most PDP-8/I's, the setting will be 0101.

Press START.

The program will run until and error is detected, or stopped by the operator.

5. Operating Procedure

5.1 Operational Switch Settings

See section 4.2.

5.2 Subroutine Abstracts

The PDP-8 uses even parity (the 13 bit word always contains an even number of binary ones). The PDP-8/I uses odd parity (the 13 bit word always contains an odd number of binary ones).

The checkerboard patterns are written into the parity bit plane by writing a word containing an odd or even number of bits (a word of all Ø's is considered as even), into the memory stack. With the PDP-8/I, for example, a one is written into the parity plane by writing a word of all Ø's. To write a Ø, a word equal to 0001 octal is written. The inverse is applied for a PDP-8.

After a pattern is written, error checking begins by reading a location and issuing an SNPE IOT (6101). If no skip occurs the program assumes a parity error is present. If a skip occurs, the contents are complemented, written back into the same location, and rechecked for parity error.

The original contents are returned to the location, and the next sequential location is then checked.

After all of memory is tested, the program then writes the complement of the pattern and proceeds to check as before.

5.3 Operator Action

See section 4.3.

6. Errors

An error halt will result anytime that the SNPE IOT does not skip.

6.1 Error Halts and Description

Two halts are provided for each error, and are described below. Two addresses are given for each halt; the first is for the Low End Test, and the second for the High End Test.

C(MA)	Tag	Description
0121 7544	E1	A memory parity error. The AC displays the contents of the location last read when the parity error occurred.
0124 7547	E1A	The AC displays the address read when the parity error occurred.

6.2 Error Recovery

Tag	Operator Action
E1	Press CONTINUE to reach the next halt.
E1A	Press CONTINUE to clear the parity error, and resume testing with the next sequential memory location.

7. Restrictions

7.1 Starting Restrictions

None

7.2 Operating Restrictions

All diagnostics, including Basic Memory Checkerboard, for a basic PDP-8 or 8/I must have been previously run without error.

8. Miscellaneous

8.1 Execution Time

The time to write and test any pattern and its complement is approximately three (3) seconds.

9. Program Description

The resultant checkerboard patterns written into the parity bit plane are the same as those generated by the Basic Memory Checkerboard test. For a detailed description, including diagrams of the patterns, refer to the Basic Memory Checkerboard write-up (Maindec-08-D1J0-D).

10. Listing

```
                        /PDP8-8/I PARITY CHECKERBOARD (LOW)

                        /
0001                    *1              /LOW END TEST
                        /
6101                    SMP=6101
6104                    CMP=6104
                        /
0001  5001              JMP .
0002  0002              0002
0003  0003              0003
0004  0000              0
0005  7121              CLL CML IAC
0006  3142              DCA COM
0007  6104              CMP
0010  1145              TAD JMP1
0011  3045              DCA STD-2

0012  7604    STX,      LAS
0013  1144              TAD MUD
0014  3137              DCA PAT
0015  1144              TAD MUD
0016  3141              DCA SA

0017  2142    STB,      ISZ COM
0020  1142              TAD COM
0021  0134              AND DOT         /2
0022  7640              SZA CLA
0023  1133              TAD NOT         /10
0024  1130              TAD HOT
0025  3034              DCA Y           /COMPLEMENT THE PATTERN

0026  1132    STC,      TAD POT         /100
0027  1141              TAD SA          /TEST FOR FINAL ADDRESS
0030  7650              SNA CLA
0031  5010              JMP SVX-2
0032  1137              TAD PAT
0033  0131              AND ROT         /200

0034  0000    Y,        0
0035  1133              TAD NOT         /Y LINE PRESETS X LINE
0036  1130              TAD HOT         /TO SNA OR SZA
0037  3042              DCA X
0040  1137              TAD PAT
0041  0134              AND DOT         /2

0042  0000    X,        0
0043  7001              IAC
0044  7420              SNL
0045  5056              JMP DOALL
0046  3541              DCA I SA                /STORE PATTERN AND RECOMPLEMENT

0047  2141    STD,      ISZ SA          /WORD WHEN CHECKING
```

```
0051  1141          TAD SA
0052  0135          AND BOT         /77
0053  7650          SNA CLA
0054  5026          JMP STC
0055  5040          JMP X-2
```

```
                        /
                        /READ AND COMPLEMENT 15 TIMES BEFORE TEST.
                        /
0056  3143   DUALL,    DCA WRD          /SAVE DATA
0057  1136             TAD M17
0060  3140             DCA LOOP         /LOOP COUNTER
0061  1144             TAD MOD          /END OF PROGRAM+1
0062  3141             DCA SA           /ADDRESS COUNTER
0063  1541   LALL,     TAD I SA         /READ
0064  1131             TAD ROT          /COMPLEMENT
0065  3541             DCA I SA         /WRITE BACK
0066  1132             TAD POT          /64 DECIMAL
0067  1141             TAD SA
0070  7650             SNA CLA          /ADDRESS=7700 IF NO SKIP
0071  5074             JMP .+3
0072  2141             ISZ SA           /INCREMENT ADDRESS
0073  5063             JMP LALL         /LOOP

0074  2140             ISZ LOOP         /15 TIMES WHEN SKIP
0075  5061             JMP LALL-2       /LOOP
0076  1146             TAD JMP2         /JMP2=JMP CCK
0077  3045             DCA STD-2
0100  1144             TAD MOD
0101  3141             DCA SA
0102  1143             TAD WRD
```

```
0123  3143          CCK,    DCA WRD         /CHECK PATTERN
0124  1541                  TAD I SA
0125  6121                  SMP             /SKIP ON NO PARITY ERROR
0126  5120                  JMP CC3         /ERROR
0127  1131                  TAD ROT         /COMPLEMENT PARITY BIT
0110  3541                  DCA I SA                /COMPLEMENT THE WORD
0111  1541                  TAD I SA                /IN CORE
0112  6121                  SMP             /SKIP ON NO PARITY ERROR
0113  5120                  JMP CC3
0114  7200                  CLA

0115  1143          CC2,    TAD WRD
0116  7100                  CLL
0117  5046                  JMP STD-1

0120  1541          CC3,    TAD I SA                /ERROR: AC CONTAINS INCORRECT WORD.
0121  7402          E1,     HLT
0122  7200                  CLA
0123  1141                  TAD SA          /AC CONTAINS ADDRESS OF
0124  7402          E1A,    HLT             /REGISTER IN ERROR
0125  7300                  CLA CLL
0126  6104                  CMP             /CLEAR ERROR

0127  5115          CC4,    JMP CC2

0130  7640          HOT,    7640            /CONSTANTS
0131  0200          ROT,    200
0132  0100          POT,    100
0133  0010          NOT,    10
0134  0002          DOT,    2
0135  0077          BOT,    77
0136  7760          M17,    7760

0137  0000          PAT,    0               /VARIABLES
0140  0000          LOOP,   0
0141  0020          SA,     20
0142  0000          COM,    0
0143  0000          WRD,    0
0144  0147          MUD,    .+3
0145  5356          JMP1,   JMP DUALL
0146  5103          JMP2,   JMP CCK

$
```

THERE ARE [illegible] ERRORS

SYMBOL TABLE

BOT	0135
CCK	0143
CC2	0115
CC3	0120
CC4	0127
CMP	0174
COM	0142
DOALL	0256
DOT	0134
E1	0121
E1A	0124
HOT	0130
JMP1	0145
JMP2	0146
LALL	0263
LOOP	0140
MUD	0144
M17	0136
NOT	0133
PAT	0137
POT	0132
ROT	0131
SA	0141
SMP	0171
STR	0217
STC	0226
STD	0247
STX	0212
WRD	0143
X	0242
Y	0234

SYMBOL TABLE

STX	0012
STB	0017
STC	0026
Y	0034
X	0042
STD	0047
DOALL	0056
LALL	0063
CCK	0073
CC2	0115
CC3	0120
E1	0121
E1A	0124
CC4	0127
HOT	0130
ROT	0131
POT	0132
NOT	0133
DOT	0134
BOT	0135
M17	0136
PAT	0137
LOOP	0140
SA	0141
COM	0142
WRD	0143
MUD	0144
JMP1	0145
JMP2	0146
SMP	6101
CMP	6104

```
                        /PDP-8 PARITY CHECKERBOARD (HIGH)
                        /MAINDEC 802:   PDP-8 CHECKERBOARD
                        /
      0001              *1
0001  5001                       JMP .
0002  0002                       0002
0003  0003                       0003
                        /
      7430              *7430
                        /
      6101              SMP=6101
      6104              CMP=6104
                        /
7430  7121                       CLL CML IAC       /HIGH END TEST
7431  3363                       DCA COM
7432  6104                       CMP
7433  1370                       TAD JMP1
7434  3270                       DCA STD-2

7435  7604              STX,     LAS
7436  1353                       TAD K100
7437  3364                       DCA PAT
7440  1353                       TAD K100
7441  3365                       DCA SA

7442  2363              STR,     ISZ COM
7443  1363                       TAD COM
7444  0361                       AND DOT           /2
7445  7640                       SZA CLA
7446  1360                       TAD NOT           /10
7447  1357                       TAD HOT
7450  3257                       DCA Y             /COMPLEMENT THE PATTERN

7451  1356              STC,     TAD SOT           /400
7452  1365                       TAD SA            /TEST FORFINAL ADDRESS
7453  7650                       SNA CLA
7454  5233                       JMP STX-2
7455  1364                       TAD PAT
7456  0355                       AND ROT           /200

7457  0000              Y,       0
7460  1360                       TAD NOT           /10-Y LINE PRESETS
7461  1357                       TAD HOT           /X LINE TO SNA OR SZA
7462  3265                       DCA X
7463  1364                       TAD PAT
7464  0361                       AND DOT           /2

7465  0000              X,       0
7466  7001                       IAC
7467  7420                       SNL
7470  5301                       JMP DOALL
7471  3765                       DCA I SA                  /STORE PATTERN AND THE COMPLEMENT
```

```
7472  2365          STD,    ISZ SA          /WORD WHEN CHECKING
7473  2364                  ISZ PAT
7474  1365                  TAD SA
7475  0354                  AND BOT         /77
7476  7650                  SNA CLA
7477  5251                  JMP STC
7500  5263                  JMP X-2
```

```
                        /
                        /READ AND COMPLEMENT 15 TIMES BEFORE TEST.
                        /
7501  3356  DOALL,  DCA WRD          /SAVE DATA
7502  1362          TAD M17
7503  3367          DCA LOOP                /LOOP COUNTER
7504  1353          TAD K100
7505  3365          DCA SA            /ADDRESS COUNTER
7506  1765  LALL,   TAD I SA                 /READ
7507  1355          TAD ROT
7510  3765          DCA I SA                /WRITE BACK
7511  1356          TAD SOT           /400
7512  1365          TAD SA
7513  7650          SNA CLA           /ADDRESS=7700 IF NO SKIP
7514  5317          JMP .+3
7515  2365          ISZ SA            /INCREMENT ADDRESS
7516  5306          JMP LALL                /LOOP
                        /
7517  2367          ISZ LOOP                /15 TIMES WHEN SKIP
7520  5304          JMP LALL-2        /LOOP
7521  1371          TAD JMP2                /JMP2=JMP CCK
7522  3270          DCA STD-2
7523  1353          TAD K100
7524  3365          DCA SA
7525  1366          TAD WRD
                        /
7526  3366  CCK,    DCA WRD           /CHECK PATTERN
7527  1765          TAD I SA
7530  6101          SMP                     /SKIP ON NO PARITY ERROR
7531  5343          JMP CC3           /ERROR
7532  1355          TAD ROT           /COMPLEMENT PARITY BIT
7533  3765          DCA I SA                /COMPLEMENT THE WORD
7534  1765          TAD I SA                /IN CORE
7535  6101          SMP               /SKIP ON NO PARITY ERROR
7536  5343          JMP CC3           /ERROR
7537  7200          CLA
7540  1366  CC2,    TAD WRD
7541  7100          CLL
7542  5271          JMP STD-1
7543  1765  CC3,    TAD I SA
7544  7402  E1,     HLT               /ERROR:AC CONTAINS
7545  7200          CLA               /INFORMATION IN ERROR
7546  1365          TAD SA
7547  7402  E1A,    HLT               /AC CONTAINS ADDRESS OF
7550  7300          CLA CLL           /REGISTER IN ERROR
7551  6104          CMP               /CLEAR ERROR
7552  5347  CC4,    JMP CC2
```

```
7553  0100          K100,   100
7554  0077          BOT,    77
7555  0200          ROT,    200
7556  0400          SOT,    400
7557  7640          HOT,    7640
7560  0010          NOT,    10
7561  0002          DOT,    2
7562  7760          M17,    7760
7563  0000          COM,    0               /VARIABLES
7564  0000          PAT,    0
7565  0000          SA,     0
7566  0000          WRD,    0
7567  0000          LOOP,   0
7570  5301          JMP1,   JMP DOALL
7571  5326          JMP2,   JMP CCK
                    $
```

THERE ARE NO ERRORS

SYMBOL TABLE

BOT	7554
CCK	7526
CC2	7540
CC3	7543
CC4	7552
CMP	6104
COM	7563
DOALL	7501
DOT	7561
E1	7544
E1A	7547
HOT	7557
JMP1	7570
JMP2	7571
K100	7553
LALL	7506
LOOP	7567
M17	7562
NOT	7560
PAT	7564
ROT	7555
SA	7565
SMP	6101
SOT	7556
STB	7442
STC	7451
STD	7472
STX	7435
WRD	7566
X	7465
Y	7457

SYMBOL TABLE

SMP	6171
CMP	6174
STX	7435
STB	7442
STC	7451
Y	7457
X	7465
STD	7472
DOALL	7501
LALL	7506
CCK	7526
CC2	7540
CC3	7543
E1	7544
E1A	7547
CC4	7552
K100	7553
BOT	7554
ROT	7555
SOT	7556
HOT	7557
NOT	7560
DOT	7561
M17	7562
COM	7563
PAT	7564
SA	7565
WRD	7566
LOOP	7567
JMP1	7570
JMP2	7571