IDENTIFICATION

PRODUCT CODE:

MAINDEC-08-D1AA-D

PRODUCT NAME:

PDP-8 Memory Power On/Off Test

DATE CREATED:

December 2, 1965

MAINTAINER:

Diagnostic Group

AUTHOR:

R. Green M. Horovitz

PREVIOUS CODE:

MAINDEC 829



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1. ABSTRACT

This program is a Memory Data Validity Test to be used after a simulated power failure.

2. REQUIREMENTS

Storage

Memory locations 00208--76778

Subprogram and/or Subroutines

High RIM

High Binary Loader

Equipment

PDP-8 Processor, keyboard reader, and Teleprinter

3. <u>USAGE</u>

3.1 Loading

Normal binary tape loading procedures are to be used with this program.

3.2 Start up and/or Entry

Load address 0020 and press START.

The program should then halt at 0043g.

Load address 0001 and press START.

The program should now loop between 0044g and 0065g.

3.3 Errors in Usage

Errors detected by the program cause the program to halt at memory address 0056_8 . The contents of memory addresses 0011_8 and 0012_8 indicate the addresses of the data that failed to check-sum. Memory addresses 0007_8 and 0010_8 contain the data words that failed to check-sum.

Lower Address = $(0011_8) = 100_8 - 3677_8$

Upper Address = $(0012_8) = 3700_8 - 7677_8$

Lower Error Word = (0007_8) = 2525_8

Upper Error Word = (0010_8) 52528

3.4 Error Recovery

Press CONTINUE to test for other error words in memory.

Reload address 00208 to restart the entire program.

4. DESCRIPTION

4.1 Discussion

This program tests memory for bit drop out and pick up after a simulated power failure has occurred.

By starting the program at memory address 0020g, data words consisting of 2525g are written into memory locations 0100g--3677g, and the data words consisting of 5252g are written into memory locations 3700g--7677g after which the program halts at memory address 0043g. Load address 0001 and restart the program; the program will 2's add the contents of memory location 0100g with 3700g. If the result equals 7777g, the program will 2's add the contents of memory locations 0101g with 3701g, etc. until the memory addresses of 3677g and 7677g are tested. The program stays in the 2's add compare loop until an error occurs. Concurrently cycle the power to the PDP-8 off and on. After the power has been reapplied to the PDP-8, load address 0001g and press START. If an error occurred during the power cycling, the program halts at location 0056g. The program may be restarted at memory address 0001g as many times as desired.

4.2 Examples and/or Applications

A HALT occurs at memory address 00568.

Address $0007_8 = 2505_8$ (Data Word) Address $0010_8 = 5252$ (Data Word) Address $0011_8 = 0101$ (Address Word) Address $0012_8 = 3701$ (Address Word)

Bit 7 was dropped at memory address 01018.

5. EXECUTION TIME

1 msec/loop

16. PROGRAM LISTING

/MFMORY POWER ON OFF TEST

*0020

	0020	4022	START,	JMS	SETUP		/START	INITIAL
	0021	5031	JMP	WRKON				
	0022	0000	SETUP,	Ø				
	0023	7200	CFV			•		
;	0024	1002	TAD	KAA77		٠,٠		L
	0025	3011	DCA	11				f
	0026	1003	TAD	K3677				
	0027	3012	DCA	12				
	0030	5422	JMP	T SETUP	•			

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```
U 1131
       1005 URKAN,
                         TAN UPPEG
9032
       3411
                  DCA 1 11
3033
      1006
                  TAM LIDREG
6034
       7412
                  00/ 1/12
                  TAF 11
1935
       1911
MUZA
       7040
                  CWA
4037
       1003
                  TAT. # 3677
MAMA
       7040
                  MM A
0041
       7644
                  C| 1 844
      5031
SVEN
                  July 1 3KDF
MMAB
            STEND,
      7492
                           HLT
                                             ITURN POWER OFF AND IN
0044
      4022
             COMPAK,
                           JMS SETUP
      7200
9945
                  CLA
                  TAN 1 11
141466
       1411
                                             /11=UPPER ADDRESS 100-3700
91447
       7 MM 7
                  DCV HPPFR
MURM
      1412
                  TAT 1 12
                                             /12=LOWER ADDRESS 37M1-7760
                  DOY I INEE
9051
       3010
GUE 2
       1007
                  TAN HERER
                  TAC LOWER
WW83
       1010
1313C4
                  CHA
       7/14/4
4055
                  541
       7440
MUE 6
       7402 F1, HL1
                        /ERROR , NO COMPARE
111157
                  TA" 11
       1011
NAGN
       7949
                  44.7
9961
       1003
                  T4" 13677
3445
       79140
                  CMA
       744 PA
CAND
                  SZA
MM64
       5045
                  JHP COMPAR+1
                  JAP CULPAR
ИИ65
      5044
             # 01 2 M W
图例例例
      1044
                 ሲሀ አነላ
      540%
មាល (1
                  J4 - 1 C
                                    /START AFTER PIWER UP
             ⊁Й 77,
11/AP2
      4077
                           7.177
             K3677,
14003
       3677
                           マらフフ
9(4)44
       7700 K7700,
                           7700
0005
      2525 HPARE.
                           2525
u w c y
       5252
             LOMFG,
                           5252
             HPPER,
ዘИИИ7
       NODE
                           Ø
                                    /ERROR WORD (2525)
             I OWER,
11/1/11/11
       1000
                           Ø:
                                    /ERROR WORD (5252)
COMPAR
         M044
F 1
         0056
K0077
         SNNN
K3K77
         0003
Kフフロバ
         00014
LUHEG
         MAMA
10kmk
         9019
```

MAINDEC-08-DIAA-D

SETUP	いのとろ
START	0020
STEND	0043
UPPER	0007
UPREG	0005
WRKON	0031
COMPAR	@ @ 4 4
F1	ØØ56
K0077	8005
K3677	0003
K7700	Ø Ø Ø 4
1 ORFG	MOMA
IOWER	0010
SFTUP	0022
START	MØ2Ø
STEND	0043
UPPFK	9997
UPREG	0005
WRKON	0031

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