lab8/e
user's handbook

digital equipment corporation

DEC-LB-HRZA-D

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user's handbook

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CONTENTS

ILLUSTRATIONS

TABLES

FOREWORD

The LAB-8/E User's Handbook is intended to familiarize the user with the LAB-8/E Laboratory System, which contains the newest, low cost PDP-8/E Computer.

A separate chapter of this handbook is devoted to the use of each of the following PDP-8/E options:

a. Front Panels
b. Analog-to-Digital Converter
c. Point-Plot Display Control
d. Real-Time Clock
e. Buffered Digital I/O

It is beyond the scope of this manual to cover the use of the PDP-8/E or the other options mentioned.

REFERENCE DOCUMENTS

The following reference documents are available from Digital Equipment Corporation:

LAB-8/E Maintenance Manual DEC-LB-HXZA-D
PDP-8/E Small Computer Handbook
PDP-8/E Maintenance Manual DEC-8E-HRIB-D
VR14 Display Maintenance Manual
DEC-IZ-HRZA-D
Introduction to Programming
Programming Languages

1

SYSTEM INTRODUCTION

LAB-8/E SYSTEM

The LAB-8/E (see Figure 1-1) is a PDP-8/E computer with numerous options designed to provide the scientific and engineering communities with a low-cost, modular, easy-to-use laboratory instrument computer. The basic system comprises:

a. A PDP-8/E General-Purpose, 12-bit Digital Computer with basic 4096 word memory and 1.2 μs cycle time.
b. A Teletype® Model 33 ASR 10-bit Input/Output device with paper-tape reader and punch.
c. A laboratory mounting panel with precision power supply for use with LAB-8/E peripherals.
d. A 10-bit Analog-to-Digital Converter with sample and hold circuitry and optional multiplexer.
e. A 10-bit Point-Plot Display Control for the graphic display of data on an oscilloscope.
f. A Real-Time Clock with five programmable ranges from 1 μs per count to 10 ms per count, plus three Schmitt triggers.

More advanced LAB-8/E Systems make use of standard PDP-8/E options. The options most commonly used with the LAB-8/E are:

a. Extra core memory
b. High-speed paper-tape reader and punch
c. VR14 large-screen display oscilloscope
d. An 8-channel analog multiplexer (expandable to 16 channels)
e. VM03 mounting hardware and cable for Tektronix Model 602 Oscilloscope

Figure 1-1 LAB-8/E System

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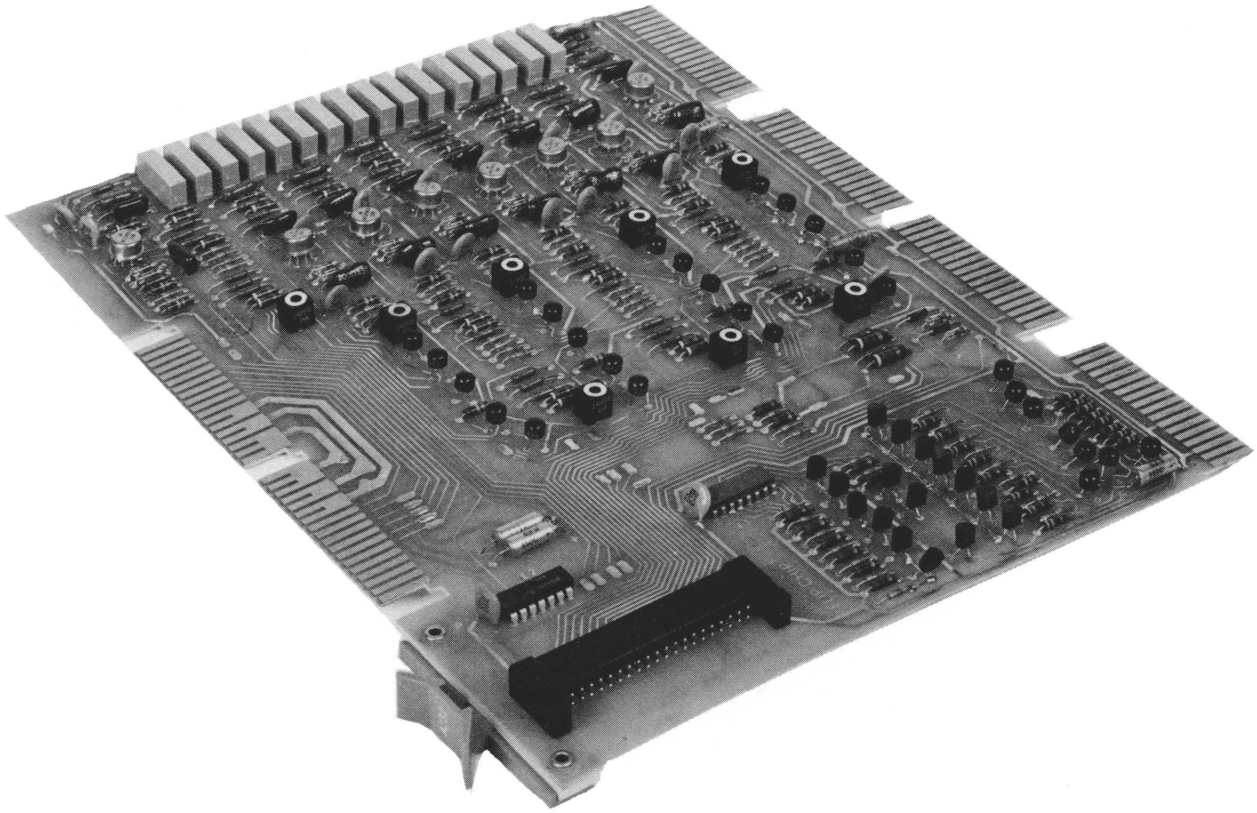
2

ANALOG INPUT PANELS



Analog Multiplexer (AM8-E)

ANALOG PANELS

DESCRIPTION

Four front panels are available with the LAB-8/E. The AM8-ED and AM8-EC analog panels are available with the AD8-E AM8-E options. A DK8-EF panel is available for the Real-Time Clock option, and a DR8-EB panel is available for the Buffered Digital I/O option (see Figure 2-1).

The AM8-ED panel furnishes the user with two DB-25S receptacles, which provide inputs for a maximum configuration, 16-channel system. In addition, the AM8-ED panel is supplied with an AD8-ES option, where a single input is wired to channel 0 of the panel. Field expansion with AM8-EA options (2 maximum) can utilize the AM8-ED panel for signal inputs. Two DB-25P connectors (DEC Part No. 12-05886) are also supplied to connect with the Analog Panel.

The AM8-EC analog panel is similar to the AM8-ED panel; however, parameter potentiometers are supplied for channels 0 through 3. These variable potentiometers have ±1.3 Vdc applied to them, and they can

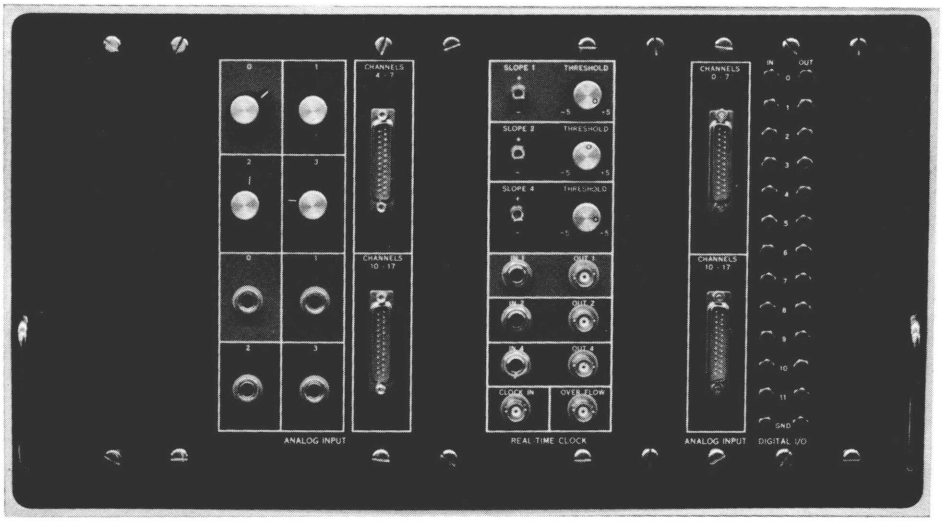


Figure 2-1 Analog Input Panel

be used to vary thresholds, to move pointers across display tubes, to edit text, and to perform other functions.

The ± 1 Vdc Inputs to these four channels can be removed from the potentiometers by installing a 3-conductor 1/4-in. telephone plug in the telephone jack on the selected channel. Four telephone jacks are supplied with each AM8-EC panel.

The DK8-EF Real-Time Clock panel assembly is used to connect the Schmitt triggers and external clock inputs to the Real-Time Clock. There are + and -slope switches that enable each Schmitt trigger channel to select the direction of the slope of the input. A potentiometer associated with each channel adjusts the trigger amplitude. Inputs to the Schmitt trigger channels can be supplied by 3-conductor 1/4-in. telephone jacks one for each channel and BNC connectors for all inputs. BNC connectors and telephone jacks are supplied with the panel.

ANALOG PANEL PIN CONNECTIONS

The pin connections for each optional analog panel are presented in Table 2-1.

Table 2-1
Pin Connections

Channel	Input	AM8-ED	AM8-EC
0	+	Pin 1	Phone Plug
	-	2	Phone Plug
	Gnd	3	Phone Plug
1	+	4	Phone Plug
	-	5	Phone Plug
	Gnd	6	Phone Plug
2	+	7	Phone Plug
	-	8	Phone Plug
	Gnd	9	Phone Plug
3	+	10	Phone Plug
	-	11	Phone Plug
	Gnd	12	Phone Plug
4	+	14	1
	-	15	2
	Gnd	16	3
5	-	18	5
	Gnd	19	6
6	+	20	7
	-	21	8
	Gnd	22	9
7	+	23	10
	-	24	11
	Gnd	25	12

Channels 10 through 17 on each panel are identical to the wiring of channels 0 through 7 on the AM8-ED panel, except that channel 0 corresponds to channel 10 1 to 11, etc.

The DR8-EB panel has 2 module connectors for 12 digital inputs and 12 digital outputs. This panel is used to connect the DR8E Buffered Digital I/O modules with various outside devices. Two M904 Modules are provided with this panel that enable the user to connect his cables. One diagnostic jumper cable to connect Input and Output connectors is provided for troubleshooting and running I/O diagnostic tests.

DR8-EB Panel Assembly Connections

The DR8-EB Buffered Digital I/O panel connections are shown in Table 2-2. The M904 Module is used to connect to the front panel block.

Table 2-2
DR8-EB Panel Connections

Bit No.	Input Pin
0	B1
1	D2
2	D1
3	E2
4	E1
5	H2
6	H1
7	K2
8	J1
9	M2
10	L1
11	P2

Ground connected to A1 N1 F1 K1 N1 R1 T1 C2 F2 J2 L2 N2 R2 U2.

DK8-EF Panel Assembly Connections

The DK8-EF Real-Time Clock Input Connections are shown in Table 2-3.

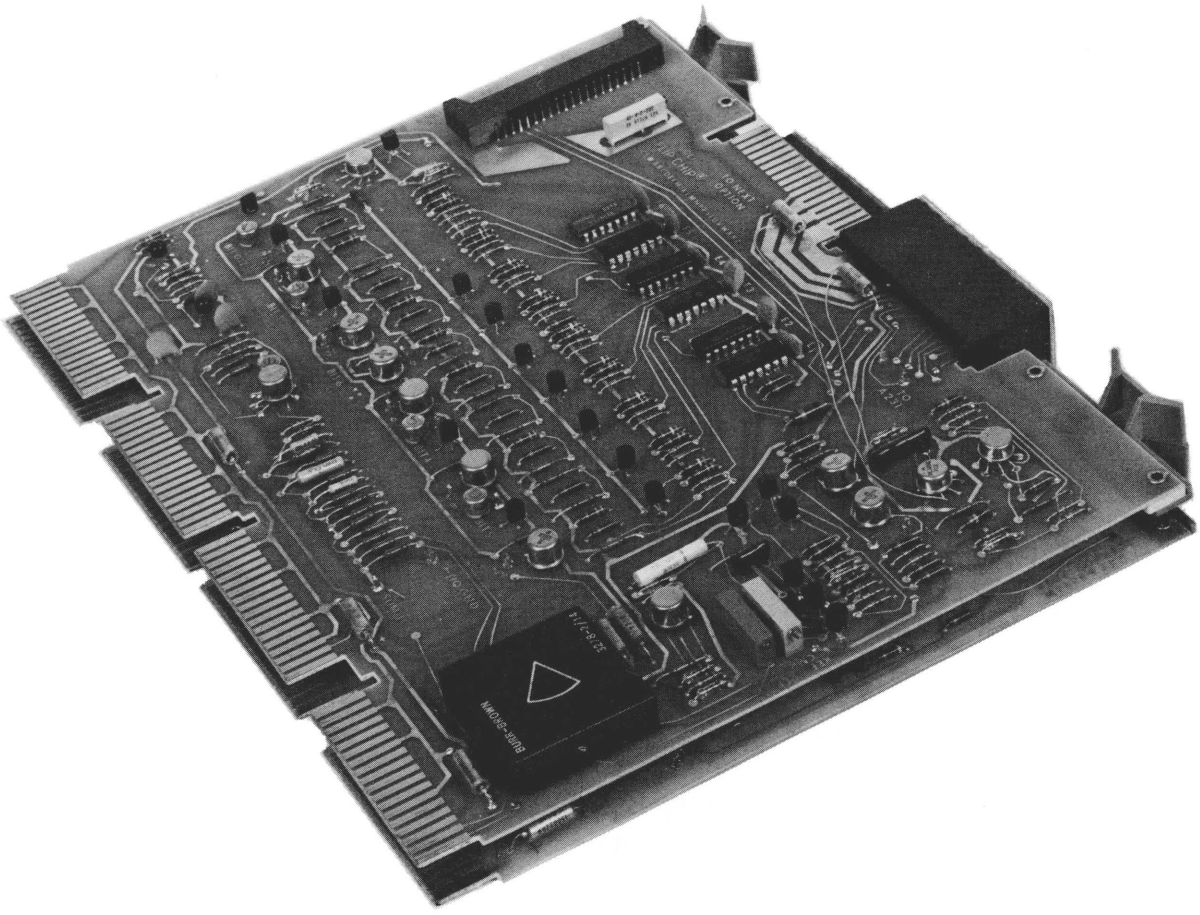
Table 2-3
DK8-EF Panel Connections

Cable or Channel No.	Channel No.	Pin No.	Signal
Cable No.1	1	F	+
		C	Gnd
		D	-
	2	L	+
		J	-
		H	Gnd
	4	R	+
		N	-
		M	Gnd
Cable No. 2		T	+6.2V
		U	Gnd
		X	-6.2V
		SS	Gnd
		RR	Ext. Clock In
		PP	Gnd
		NN	Overflow
		V	Schmitt common
		AA	Gnd
Cable No. 3		FF	Ch1(L)
		DD	ST1
		CC	Gnd
		JJ	Ch2(L)
		BB	ST2
		EE	Gnd
		LL	CH4(L)
		Z	ST4
		HH	Gnd
BNC 1			ST1 (out)
BNC 2			ST2 (out)
BNC 3			ST4 (out)
BNC 4			Overflow
BNC 5			Ext. Clock In
J1	1		IN 1
J2	2		IN 2
J3	4		IN 4

BNC connector shield tied to Schmitt common.

3

ANALOG-TO-DIGITAL CONVERTER SYSTEM



Analog-to-Digital Converter (AD8-E)

A/D CONVERTER

GENERAL DESCRIPTION

The LAB-8/E Analog-to-Digital Converter System enables the user to sample analog data at specified rates and to store the equivalent digital value in the memory of the PDP-8/E for subsequent processing. Sample and hold circuitry in the converter ensures an accurate conversion of even the fastest changing signals by holding the voltage at the input constant until the conversion process is complete.

When used with two 8-channel multiplexer and expander boards, the analog-to-digital converter can select up to 16 analog channels for sampling (refer to Figure 3-1). Connectors on a panel mounted on the front of the LAB-8/E laboratory mounting panel provide the inputs to the

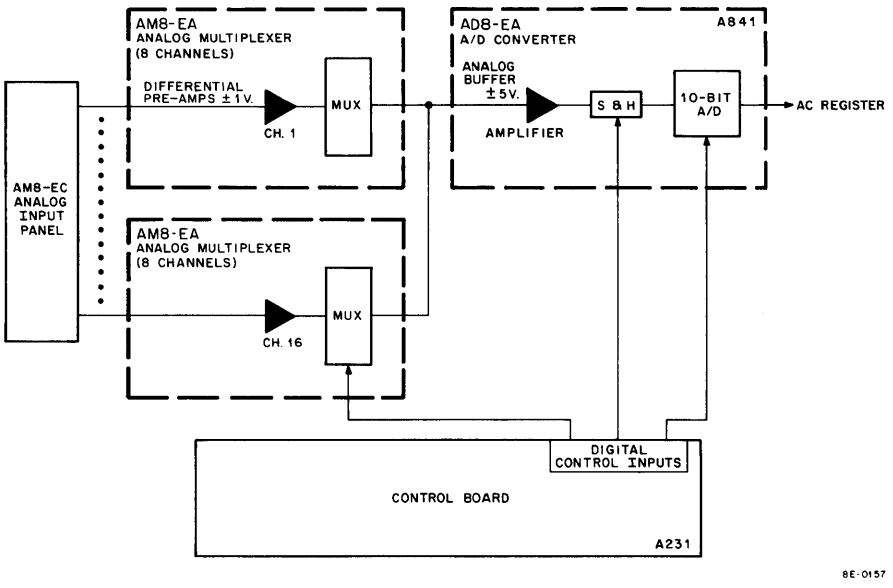


Figure 3-1 A/D Converter and Multiplexer---Simplified Block Diagram

LAB-8/E Analog-to-Digital Converter System. When only the AD8-EA Analog-to-Digital Converter is used, the input is differential and in the range of ±5V. With the AM8-EA multiplexer, the input range is ±1V differential, which is amplified to ±5V for input to the Analog-to-Digital Converter.

Four continuously variable parameter knobs are also available with the multiplexer. These knobs control the position of potentiometers, which tap a voltage from a standard power supply and feed that voltage to the converter system. These variable knobs are useful to programmers for establishing parameters, setting threshold levels, or moving parts of the display. The output of each of these potentiometers is physically connected to a multiplexer channel; knob 0 connects to channel 0 knob 1 to channel 1, etc. To prevent monopolizing the multiplexer channels in the event that they are required for external use, a phone jack is associated with each parameter knob. When used externally, the corresponding potentiometer output is disabled and the multiplexer input is available at one common connector input.

AD8-EA ANALOG-TO-DIGITAL CONVERTER

The AD8-EA is a 10-bit successive-approximation converter with sample and hold circuits, conversion circuits, an input buffer, and control logic contained on two PDP-8/E modules (A231 and A841). The converter can be used singularly with one channel input having an input range of ±5V, or it can be used with the AM8-EA multiplexer boards (A232) to perform conversions for up to 16 channels having full-scale inputs of ±1V. Analog inputs are connected to the module by H851 Edge connectors from the multiplexer or by a shielded twisted pair from an external device.

Operation of the AD8-EA Converter

The operation of the AD8-EA converter is controlled by IOT instructions. A conversion is initiated by an ADST instruction or from the DK8-ES Real-Time Clock. An input starts the conversion and clears the A/D Done Flag. When the conversion is complete, the converter sets its A/D Done Flag. This flag is sensed by an ADSK instruction, and if set, it causes the next instruction to be skipped; thus, the 10-bit digital word can be transferred to AC2-11 by an ADRB instruction. Because the 10-bit word is in 2's complement form, AC00 and AC01 copy AC02 (sign-extended format). In other words, a negative voltage results in a negative signed number. The converter contains an INTERRUPT ENABLE flip-flop that is controlled by program instructions. When this flip-flop is enabled, the converter can generate interrupt requests to the program interrupt facility on completion of a conversion.

The converter also contains circuits for detection of timing errors. A timing error is defined as the receipt of a conversion request, attempting to read the AD Buffer, or an attempt to change the multiplexer channel while a conversion is in progress. If one of these conditions occurs, the Timing Error Flag is set. The Timing Error Flag is sensed by an ADSE instruction and cleared by an ADCL or ADST instruction.

AD8-EA Specifications

Input Voltage Range:	± 5V
Input Impedance:	Differential + input greater than 10 MΩ negative input (with jumper) greater than 10 kΩ. Common mode rejection at least 35 dB at 60 Hz (common mode voltage less than 5V to ground)
Output Format:	Parallel: 10 bits right-justified and sign extended 2's complement
Resolution:	.1%(1 bit in 1024)
Temperature Stability:	± .1%FS/C°
Accuracy:	.1%
Repeatability:	99.7%repeatable (3 standard deviations on a normal distribution function)
Conversion Rate:	50 kHz maximum

AM8-EA 8-CHANNEL ANALOG MULTIPLEXER

The AM8-EA is an 8-channel multiplexer designed to expand the capability of the AD8-EA A/D Converter. The multiplexer accepts bipolar analog inputs having a full-scale range of ±1V and converts these inputs into a full-scale ±5V output supplied to the AD8-EA Converter.

Operation of the AM8-EA 8-Channel Analog Multiplexer

The AM8-EA consists of multiplexer switches and scaling amplifiers for eight analog channels. The AM8-EA can be expanded up to 16 channels in 8-channel groups by adding an additional AM8-EA 8-channel Multiplexer Expander Module. Multiplexer operation is controlled by the AD8-EA. Programmed instructions and the associated multiplexer control provide the capabilities for random or sequential selection of a multiplexer channel and for reading the active channel address to the computer. Two programmable address modes are provided: auto-increment or non-auto-increment. The AD8-EA is set to the non-auto-increment mode when the ADCL command is given.

In the auto-increment mode, channel addresses are incremented automatically at the completion of a conversion by an A/D Done output from the converter. The computer specifies the first channel requested by the user by issuing an ADLM instruction, then issues A/D converter instructions to start an A/D conversion. On completion, the A/D Done Flag increments the multiplexer channel address for the next sample. This process continues until the AUTO MODE flip-flop is reset. Incrementing beyond channel 17_8 causes an automatic reset to channel 0.

AM8-EA Specifications

Input Voltage:	Bipolar ±1V
Input Impedance:	Non-inverting input is 70 kΩ ±2% in parallel with 300 pF. Inverting input is 35 kΩ ±2% in parallel with 300 pF
Output:	Bipolar ±5V full scale
Common Mode Rejection:	Greater than 25 dB, 35 dB (typical)
Overload Protection:	±67V from fault line (indefinitely)
Overload Recovery Time:	8 μs
Frequency Response:	Flat from 0 to 30 kHz, -3 dB at 60 kHz
Leakage Current:	Negligible at 70Ω impedance
Long Term Stability (one hour):	Not more than 0.1% for ±30C° change

PROGRAMMING

Eight instructions are used to program the A/D Converter and Multiplexer. Each instruction is completed in 1.2 μs. The instructions are as follows (see Figure 3-2 for word format):

CLEAR ALL (ADCL)
Octal Code: 6530
Operation: Clears the A/D Done Flag and Timing Error Flags to ready the converter for another conversion. This instruction also clears the MUX and Enable Register.

LOAD MULTIPLEXER (ADLM)
Octal Code: 6531
Operation: Load Multiplexer Register with contents of AC8-11 and clear AC.

START CONVERSION (ADST)
Octal Code: 6532
Operation: Clear A/D Done and Timing Error Flags and start A/D Converter. Channel to be converted is determined by MUX Register.

READ A/D BUFFER (ADRB)
Octal Code: 6533
Operation: Clear A/D Done Flag and load the contents of the A/D Buffer into AC0-11.

SKIP ON A/D DONE (ADSK)
Octal Code: 6534
Operation: Skip the next instruction if A/D Done = 1. Do not clear flag.

SKIP ON TIMING ERROR (ADSE)
Octal Code: 6535
Operation: Skip the next instruction if Timing Error Flag = 1. Do not clear flag.

LOAD ENABLE REGISTER (ADLE)
Octal Code: 6536
Operation: Load Enable Register with contents of AC2-5 and clear AC Register.

READ STATUS REGISTER (ADRS)
Octal Code: 6537
Operation: Read A/D Status Enable Register and MUX Register contents into AC0-11.

The Status Enable and Multiplexer bits indicate the following conditions:

Status Register 0— A/D Done Flag Status (Done = 1)

1—Timing Error Flag Status (Error = 1)

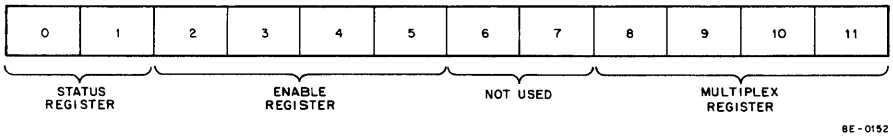


Figure 3-2 Status, Enable, and Multiplexer Register Word Format

Enable Register

2—Enable Interrupt on A/D Done = 1

3—Enable Interrupt on Timing Error = 1 (Note 1)

4—Enable External (e.g., clock) A/D start

5—Auto-Increment Mode (Note 2)

Multiplex Register

8—11—Indicates current channel ($0\text{-}17_8$) to be sampled by A/D.

NOTE

1. **The Timing Error Flag indicates that either an ADRB, ADLM, ADST, or external A/D start was attempted while a conversion was in progress. ADLM or ADRB will cause an erroneous result to appear in the A/D buffer, while external A/D start or ADST will be ignored.**

2. **When this bit is set, the occurrence of A/D Done = 1 will increment the Multiplex Register by 1. Incrementing past channel 17_8 will cause the MUX Register to reset to channel 0.**

Programming Examples

Normal Mode — To program the analog-to-digital converter (ADC), the program must issue a start command; loop on the Done Flag until the conversion process is complete and the Done Flag is set to a 1; then read the value of the converter's buffer into the PDP-8/E accumulator. The program is as follows:

```
ADST    /CLEAR ADC DONE FLAG AND START CONVERSION
ADSK    /SKIP THE NEXT INSTRUCTION WHEN DONE
JMP-1   /JUMP BACK ONE INSTRUCTION
ADRB    /READ THE ADC BUFFER INTO THE AC
```

If the ADC has been enabled to accept start pulses from an external device (such as a clock), then a timing error could occur. To check for this possibility, the following code should be added after the ADRB command:

```
.
.
.
ADSE            /SKIP THE NEXT INSTRUCTION ON ERROR
SKP             /UNCONDITIONAL SKIP
JMS ERROR       /GO TO ERROR ROUTINE
.
.
.
```

When the ADC is equipped with the multiplexer option, the channel to be sampled is selected prior to starting the conversion process using the ADLM command. For example, a simple program to continuously read the value of one of the parameter knobs and display the digital value in the PDP-8/E accumulator is as follows:

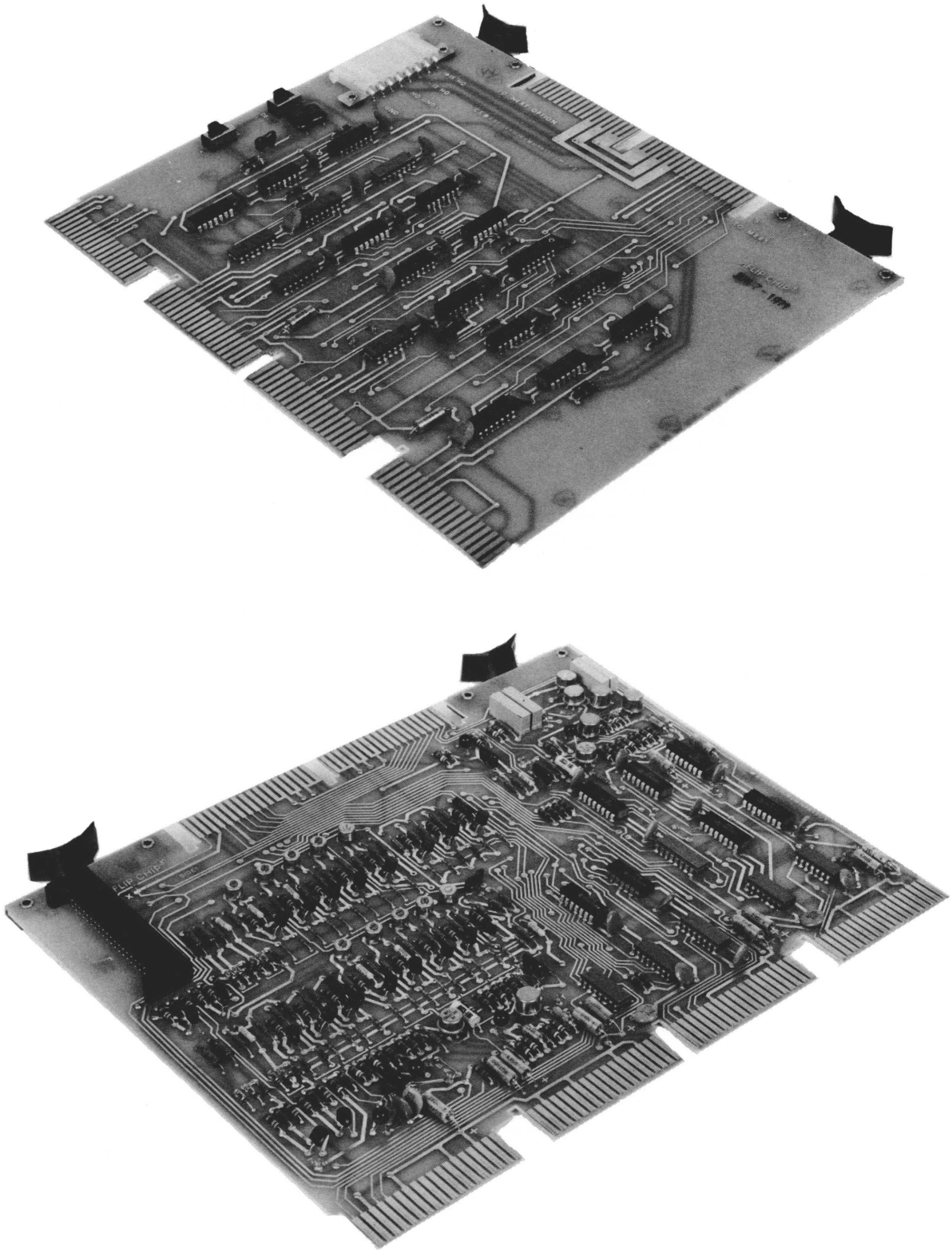
```
START, CLA      /CLEAR THE PDP-8/E ACCUMULATOR
TAD CHN         /GET THE CHANNEL # (0-3 FOR KNOBS)
ADLM            /LOAD MULTIPLEXER FROM AC
AGAIN, ADST     /START
ADSK            /SKIP WHEN FINISHED
JMP.-1          /
ADRB            /READ ADC VALUE
JMP AGAIN
```

Clock Mode — In this special mode, samples are taken at regular intervals as defined by the clock rate. A conversion is initiated with every clock overflow. The following example takes 1000_{10} samples at the specified clock rate and stores them in memory.

```
          .
          .
          .
INITIALIZE CLOCK AND ADC ENABLE REGISTER
          .
          .
          .
START, CLA
          TAD NUMBER        /-1000#
          DCA COUNTER       /STORE IN COUNTER
          TAD ADDRESS       /ADDRESS OF A/D CONVERSION STORAGE AREA
          DCA POINTER       /POINTER IS AN AUTO-INDEX REGISTER
ADLOOP, ADSK                /WAIT FOR CONVERSION DONE
          JMP-1
          ADRB              /READ CONVERSION
          DCA I POINTER     /STORE IT AWAY
          ISZ COUNTER       /HAVE THE REQUIRED # OF SAMPLES BEEN TAKEN
          JMP ADLOOP        /NO: GET ANOTHER
          .
          .
          .
NUMBER,       -1750#        /# OF SAMPLES (1000# IN THIS CASE)
COUNTER,      0
ADDRESS,      n-1           /BEGINNING OF TABLE-1
POINTER,      0
```

4

DISPLAY SYSTEM



Point-Plot Display Control (VC8-E)

VC8-E DISPLAY CONTROL

GENERAL DESCRIPTION

The VC8-E Display control can control a Tektronix 602 or VR14 Display in the form of a 1024_{10} by 1024_{10} dot array. Under program control, a bright spot can be momentarily produced at any point in this array. A series of these intensified dots can be programmed to produce graphic output.

VC8-E POINT-PLOT DISPLAY CONTROL

The VC8-E consists of a two-axis, digital-to-analog converter and intensifying circuit (Module M885) that provide deflection and intensity signals. The output of the D/A converters is -5V to +5V in steps of ≈10 mV per step. The signals from the VC8-E are applied to the input amplifier circuitry of such display units as the Tektronix Model 602 or the type VR14 Oscilloscope. The control circuit for the VC8-E is located on a PDP-8/E module (M869). Both modules plug into the OMNIBUS ™

The basic VC8-E system consists of the following circuitry:

a. OMNIBUS interface, IOT decoding, skip, clear AC, and interrupt control.

b. X-axis buffer, D/A converter, summing amplifier, and bipolar line driver.

c. Y-axis buffer, D/A converter, summing amplifier, and bipolar line driver.

d. Z-axis control, which consists of provisions for the intensity signal necessary for the Tektronix Model 602 Oscilloscope, and intensity and channel select signals necessary for the VR14 oscilloscope.

The VC8-E interfaces with the Tektronix Model 602 or the VR14 through two different connector assemblies.

Note the relationship between the signed octal numbers shown below and their corresponding 2's complement form.

Signed Values (used in programming example)	2's Complement (10 Bit)	(12 Bit)
+777	0777	0777
.	.	.
.	.	.
.	.	.
+1	0001	1
0	0000	0
-1	1777	7777
.	.	.
.	.	.
.	.	.
-777	1001	7001

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OPERATION OF THE DISPLAY SYSTEM

The VC8-E is a two-axis (X and Y), digital-to-analog converter and intensifying circuit (Z-axis) that provides defection and intensity information to the display oscilloscope. In Figure 4-1, the position of the oscilloscope beam will be determined by the contents of the X-and Y-buffer registers. Coordinate (0.0) is located in the center of the screen. Coordinate data (see Figure 4-2) is transferred to the X-and Y-axis from bits 2 through 11 of the PDP-8/E accumulator. This data must be in the range $\pm 0777_8$.

the oscilloscope (provided by the user) in the H945 LAB-8/E Mounting Cabinet. A modification kit for the oscilloscope and a BC01L-10 cable are provided to properly interface the Model 602 oscilloscope to the VC8-E. Cable lengths other than 10 ft are available at extra cost.

Display Times

The display times of instructions that include intensification depend on the type of oscilloscope used.

VR14:	21 μs
Tektronix Model 602:	6 μs

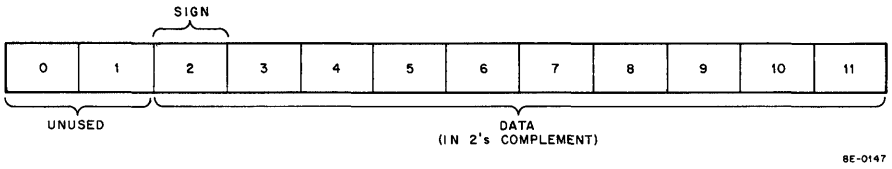


Figure 4-1 X or Y Buffer

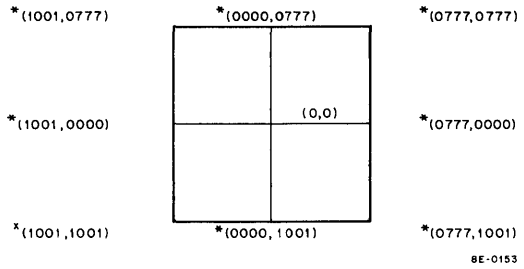


Figure 4-2 Operation of the Point-Plot Display System

NOTE

Octal 1000 is a point on the oscilloscope below 1001; however, it is undefined in 2's complement arithmetic.

Type VR14 Oscilloscope Display

The VR14 is a compact solid-state CRT display with self-contained power supplies and a viewing area of 6-3/4 in. by 9 in. The VR14 can plot 1500 random points and up to 75 in. of vector with no flicker. A maximum deflection step in any direction requires only 21 μs. Interface with the VC8-E is through connector assembly BC01K-10 (10 ft) BC01K-25 (25 ft), or BC01K-50 (50 ft). The standard length is 10 ft.

VM03 Mounting Hardware

The VM03 Mounting Hardware kit for the Tektronix Model 602 Oscilloscope provides brackets for inserting

These times are necessary for the electron gun to reach the specified position before intensification can take place. A switch is provided on the M869 Module to select the proper interval. The switch is marked DELAY, with settings L for long and S for short.

Specifications

Z-Axis (intensity pulse) — The Z-axis polarity is controlled by a switch in the M869 Module. The pulse will be either positive or negative, depending on the setting. For the Tektronix 602, the switch must be in the positive position; for the VR14, the switch must be in the negative position.

Pulse Width:	1 μs
Pulse Size:	+4V to -2V
Rise Time:	100 ns
Fall Time:	200 ns

NOTE

Provisions have been made for controlling a Tektronix Model RM503 Oscilloscope. However, the settling time for this unit is somewhat longer than the VR14 settling time (21 μs). A software time delay before intensification must be provided by the user for proper operation. A jumper wire must be removed on the M885 Module, and another wire must be installed on two split lugs. This modification will create a +4V to -10V intensity pulse. With adjustments of the Z-axis intensity on the RM503, the oscilloscope functions properly.

Digital-to-Analog Converter Specifications

Output Voltage:	+5.12V to -5.12V ±.01V
Resolution:	10 mV ± 2.5 mV
Slewing Speed:	<2.5 V/μs
Drive Capability:	Capable of driving loads greater than 1 kΩ (min) in parallel with 5000 pF; i.e., 100 ft, 50 pF/ft cable.

Offset and gain adjustments provide a 10%decrease in range and step sizes, and a variation of ±.5V from ground.

PROGRAMMING

To output data on the oscilloscope display use the instructions defined as follows (refer to Figure 4-3 for Display Enable/Status Register):

Clear All Logic (DILC)
Octal Code: 6050
Operation: Clears, enables, flags and delays.

Clear Done Flag (DICD)
Octal Code: 6051
Operation: Clears Done Flag.

Skip On Done Flag (DISD)
Octal Code: 6052
Operation: Skip if Done Flag (1). Do not clear Done Flag.

Load X-Register (DILX)
Octal Code: 6053
Operation: Clear Done Flag; load X-Register, wait for settle. Set Done Flag. Do not clear AC.

Load Y-Register (DILY)
Octal Code: 6054
Operation: Clear Done Flag; load Y-Register, wait for settle. Set Done Flag. Do not clear AC.

Intensify (DIXY)
Octal Code: 6055
Operation: Clear Done Flag; intensify; set Done Flag.

Load Enable (DILE)
Octal Code: 6056
Operation: Transfers contents of AC to Enable Register as defined below. Clears AC.

Read Enable/Status Register (DIRE)
Octal Code: 6057
Operation: Transfer the contents of the Display Enable/Status Register to the AC as defined below:

The Done Flag (bit 0) can be read using a DIRE (transfer enable to AC) command; however, the Done Flag may not be set under program control using the DILE (load enable, clear AC) command.

The channel number selects the VR14 display channel. Bit 10 = 0, channel 0; bit 10 = 1, channel 1.

Both channel number and interrupt can be loaded from and read into the AC using the DILE and DIRE commands, respectively.

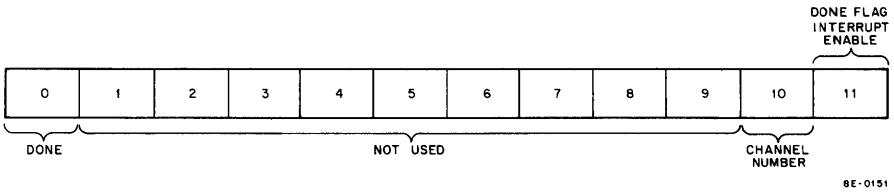


Figure 4-3 Display Enable/Status Register

Programming Examples

The VC8-E Display Control is extremely fast; thus, many display oscilloscopes cannot position their beam before an intensify command is performed. For this reason, a Done Flag has been incorporated into the control and should be used whenever random points are plotted sequentially.

The Tektronix 602 requires only 6 μs to display clear information on the oscilloscope. In applications where the program overhead time is of sufficient length to consume 5 cycles of processor time, there is no need to wait for display Done Flag indications. This time saving factor is indicated by the following example:

```
.
.
.
CLA
TAD X          /GET X-COORDINATE
DILX           /LOAD X-REGISTER
CLA
TAD Y          /GET Y-COORDINATE
DILY           /LOAD Y-REGISTER
TAD TABLE 1 )
DCA X       }
TAD TABLE 2 }  CYCLE TIME TO BE USED
DCA Y       )
DIX Y           INTENSIFY POINT
```

When using the VC8-E with slower oscilloscopes, such as the VR14, or if there is some doubt concerning the program overhead time, the following code should be inserted prior to an intensify instruction and after the load sequence:

```
.
.
.
DISD     /SKIP ON DISPLAY DONE FLAG
JMP.-1
.
.
.
```

The following example displays a dot on the screen; the coordinates are set by the position of parameter knobs 0 and 1 of the ADC:

```
START, CLA              /SET AC=Ø
       JMS SAMPLE       /POSITION OF KNOB Ø
       DILX   /LOAD     /LOAD
       CLA IAC          /SET AC=1
       JMS SAMPLE       /POSITION OF KNOB 1
       DILY             /LOAD
       DISD             /SKIP ON DISPLAY DONE FLAG
       JMP-1
       DIXY             /INTENSIFY
       JUMP START
SAMPLE,      Ø
       ADLM             /LOAD MULTIPLEXER
       ADST             /START CONVERSION
       ADSK             /WAIT
       JMP.-1
       ADRB             /READ
       JMPI   SAMPLE
```

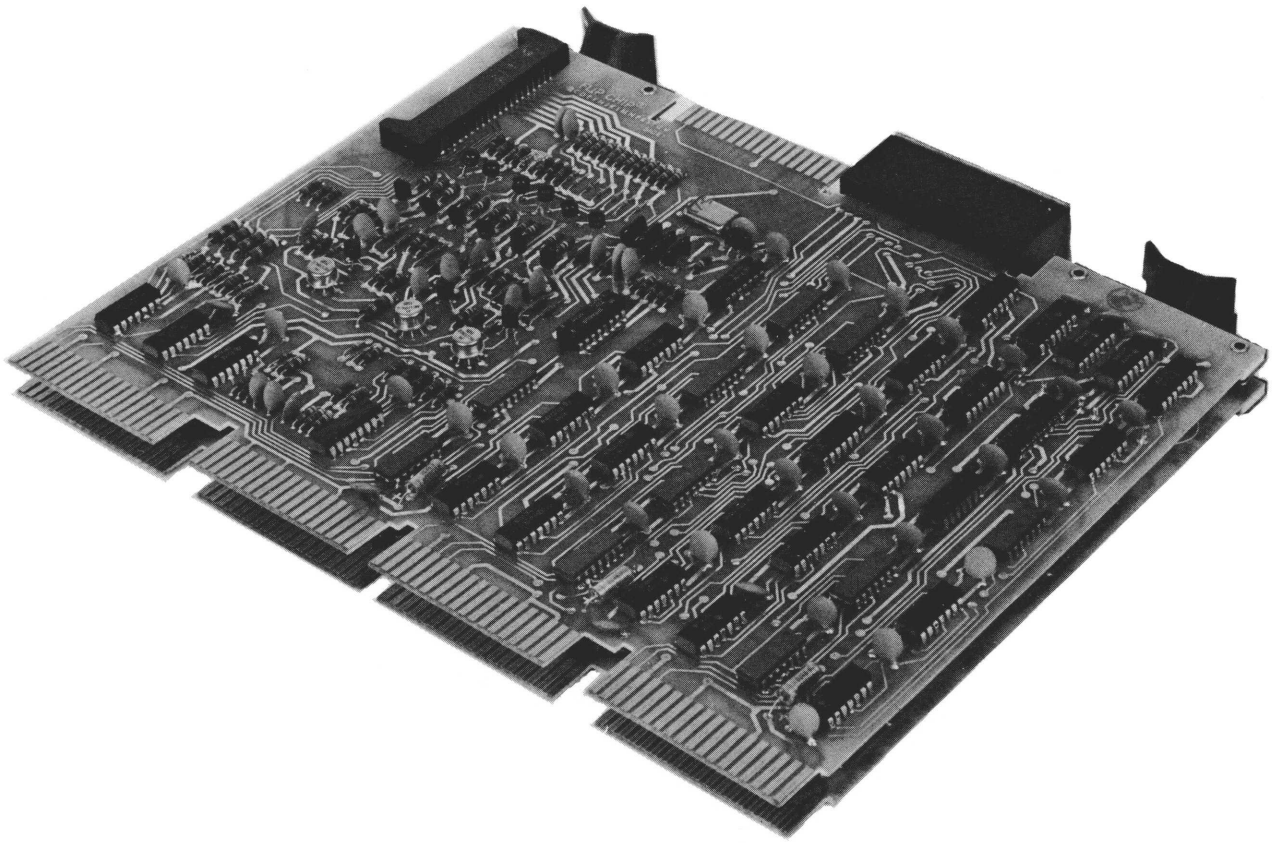
The kaleidoscope program for the VC8-E vividly shows the versatility of the VC8-E Display System. The pictures on the screen are varied by manipulating switch register bits 9, 10, and 11.

```
/KALEIDOSCOPE PROGRAM

START, TAD        Y        /GET Y
       JMS        SCALE    /SCALE IT
       CMA                 /2's COMPLEMENT
       TAD X               /CONFUSE WITH X
       DCA X
       TAD X
       DILX                /LOAD X
       JMS        SCALE    /SCALE
       TAD Y               /CONFUSE WITH Y
       DILY                /LOAD Y
       DISD
       JMP.-1
       DIXY                /INTENSIFY
       DCA Y
       JMP        START    /DO AGAIN
SCALE, Ø
       DCA        TEM      /TEMP STORE
       OSR                 /READ SWITCHES
       CIA                 /NEGATE
       DCA        C        /STORE
       TAD        TEM      /GET VALUE TO CHANGE
CHANGE, CLL
       SPA
       CML
       RAR
       ISZ        C
       JMP        CHANGE
       JMP I      SCALE
       X,2222
       Y,1111
```

5

REAL-TIME CLOCK



Real-Time Programmable Clock (DK8-E)

DK8-ES REAL-TIME CLOCK

GENERAL DESCRIPTION

The LAB-8/E DK8-ES Real-Time Clock option offers the PDP-8/E user a method of accurately measuring and counting intervals or events in a number of ways. The real-time clock can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide program interrupts at programmable intervals. Some of these operations can be performed concurrently.

OPERATION OF THE DK8-ES REAL-TIME CLOCK

Logically, the DK8-ES contains the features described in the following paragraphs.

Clock Counter Register

The Clock Counter Register (see Figure 5-1) is one of the four registers in the DK8-ES that are accessible to the program. Each generated pulse causes the clock counter to be incremented by 1. The clock counter increments 7777_8 and then overflows on the next pulse, causing the Overflow Flag to be set to 1. The program detects the Overflow Flag; the flag is also sensed by a program interrupt, a skip instruction, and/or a read status instruction. The contents of the clock counter at any given point can be determined by an instruction that puts the contents of the clock counter into the AC via the Buffer-Preset Register. The contents of the Clock Counter Register can also be set by the user via the Buffer-Preset Register and the Clock Control Register.

Buffer-Preset Register

The 12-bit Buffer-Preset Register is the link between the processor, accumulator (AC), and the clock counter (see Figure 5-2). The Buffer-Preset Register is used to read the contents of the Clock Counter Register into the AC; it is also used to buffer the current count in the clock counter when this value is to be saved. The Buffer-Preset Register is then made available to the program by an instruction that reads the contents of the Buffer-Preset Register into the AC. This register is also used to hold the number to be transferred into the clock counter

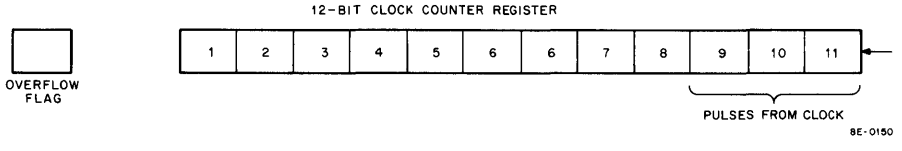


Figure 5-1 12-Bit Clock Counter Register

each time the counter overflows. This number is then loaded into the Buffer-Preset Register from the AC. This procedure allows the counter to be reset to some desired starting value each time the counter overflows; thus, the program has a highly flexible control over the apparent clock frequency.

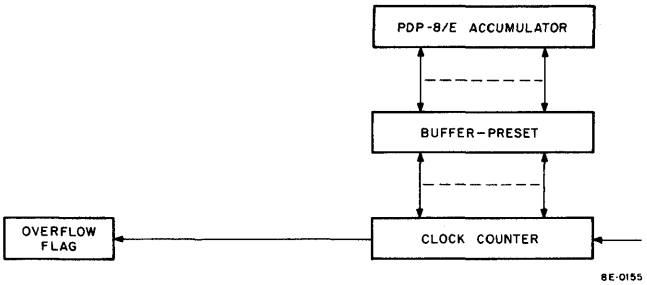


Figure 5-2 Operation of Buffer-Preset Register

Clock Enable Register

The Clock Enable Register (see Figure 5-3) is the 12-bit register that enables the operation of the entire clock option.

This Clock Enable Register controls the rate of the time base and the mode of counting and selectively enables each of the three input channels and the interrupt line. Other bits in the 12-bit register determine interrupt and enable conditions. The Clock Enable Register is loaded from the PDP-8/E accumulator under program control. The conditions enabled for any channel determine the action that must be taken to detect an event.

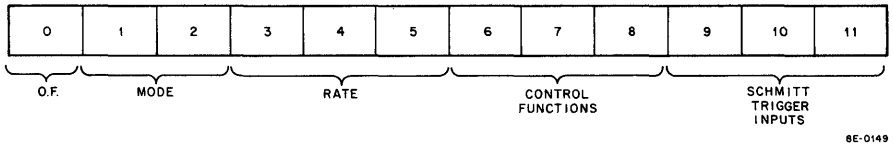


Figure 5-3 Clock Enable Register Word Format

Mode Selection — Bits 1 and 2 of the Clock Enable Register can be considered the Mode Control Register; this register is used to determine the method by which the clock operates.

AC Bit	Function
0	Enables clock overflow to set corresponding bit in the Status Register.
00	Free Run -the counter is incremented at the specified rate.

AC Bit	Function
00	Counting goes from 0 to 7777_8, overflows, and then starts counting from 0 again. Overflow, therefore, occurs every 4096_{10} counts (or every 4096 · counting rate cycles). The overflow flag remains set until cleared by programming. 000 → 7777 → OVERFLOW
01	Present Time -as in mode 00, the counter is incremented at the specified rate. Each time overflow occurs, however, the contents of the Buffer-Preset Register are transferred automatically to the counter, which then continues counting up from that value. The Buffer-Preset Register is usually set to the negative (2's complement) value of the number of counts desired before overflow. In this mode, the user has not only determined the rate of counting but also the number of counts before overflow, thus allowing him two dimensions in selecting the time intervals between overflow (see Figure 5-4). In this mode, as in mode 00, the overflow remains set until cleared by the program.

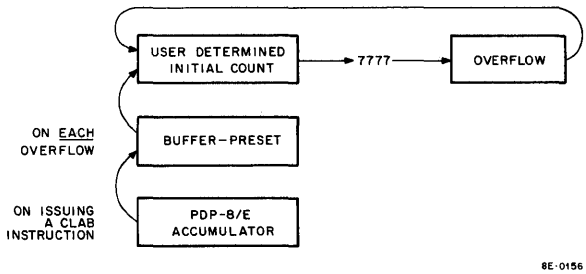
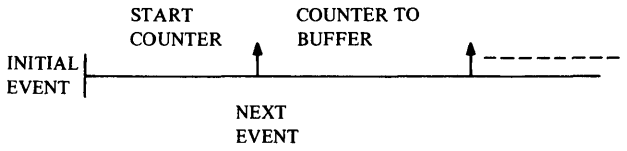


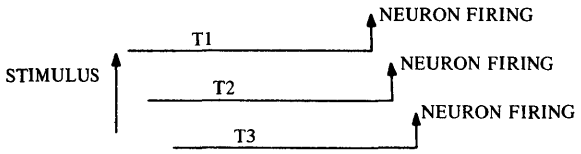
Figure 5-4 Partial Diagram Showing Major Components of Real-Time Clock

10 Time Base from Initial Event -as modes 00 and 01, the clock counter is incremented at the specified rate, but on each occurrance of an input event on a selected input channel (Schmitt trigger), the contents of the clock counter are automatically transferred to the Buffer-Preset Register, and the counter continues to count.



This mode is useful for determining the total elapsed time between some initial event (e.g., a stimulus) and subsequent events that might be caused by the initial event (e.g., muscle reaction). In using mode 10, the Clock Status Register is used in conjunction with the Clock Enable Register to detect the occurance of the input events. Each time such an event is recognized, the contents of the Buffer-Preset Register can be picked up by the program and stored away, or processed as the user wishes.

A Post Stimulus Histogram (PST) can be generated as follows: 0 a stimulus can be issued to a subject, and the clock started. Then, the elapsed time to succeeding neuron firings (i.e., input events) can be determined by saving the time counts that are transferred from the counter to the Buffer-Preset Register on each firing.



11 Time Base between Two Events -as in modes 00, 01, and 10, the clock counter is incremented at the specified rate.

On each occurrence of an input event on a selected input channel (Schmitt trigger), the contents of the clock counter are automatically transferred to the Buffer-Preset Register. This procedure is identical to mode 10 thus far. However, mode 10 and mode 11 differ as follows: in mode 10, the clock counter continues to count after the transfer, regardless of which of the three enabled input channels the event occurred on. In mode 11, the clock counter is cleared after being transferred to the Buffer-Preset Register; counting then continues from 0 at the specified rate (refer to Table 5-1).

AC Bit	Function
6	Enable external start (of AD8-E).
7	Inhibits the clock from counting when set to a 1. Bit 7 is cleared by firing any enabled Schmitt trigger.
8	Causes an interrupt request when any bits in the Status Register are set to a 1.

Table 5-1
Rate Selection

Contents of Bits 3-5	Octal Value	Interval Between Pulses (seconds)	Frequency
000	0	Stop	0
001	1	---	External Input
010	2	10	100 Hz
011	3	10	1 kHz
100	4	10	10 kHz
101	5	10	100 kHz
110	6	10	1 kHz
111	7	Stop	0

AC Bit	Function
9, 10, & 11	Enabled the firing of Schmitt triggers 1, 2, or 4 to set corresponding bits in the Status Register. Schmitt trigger 4 Schmitt trigger 2 Schmitt trigger 1

NOTE

The program interrupt facility must be enabled by issuing an ION (6001) before an actual program interrupt can occur. If an ION has been issued, enabling interrupt on an input channel or on overflow still causes the Clock Flag to be set to 1; however, the program will JUMP to a subroutine at 0. The Clock Flag can be checked, like any other device flag, with a Skip on Flag = 1 instruction CLSK.

Any or all of the Schmitt triggers can be enabled to set the Clock Status Registers, and depending on other bits set in the Enable Register, an interrupt or a transfer of clock counter information to the Buffer-Preset Register may occur.

Schmitt Triggers

Access to the Schmitt triggers is gained through the Input Control Panel, which is mounted on the Laboratory Mounting Panel. The Input Control Panel has three groups of outlined boxes, each designated Schmitt triggers and each with an identical set of controls. Each box represents one input channel to which an external signal may be connected. Within each box, there is a phone jack (Differential Input) marked input, and a BNC marked output; also within each box, there is a switch marked slope, and a control knob marked threshold. The input jacks have the following specifications:

Input Threshold:	Variable between ±5V
Source:	Positive, Negative, or Line Voltage
Input Type:	Differential
Input Resistance:	50 k
Minimum Duration Input Pulse:	2 μs
Maximum Permissible Input Voltage	±50V
Hysteresis:	0.3V
Common Mode Rejection:	35 dB
Propagation:	600 ns
Output Voltage:	0 to +5V (falling edge denotes firing and resets on recrossing the threshold voltage).

NOTE

A Schmitt trigger need not be enabled to make use of its signal conditioning properties. An analog signal can be used to drive the external clock input by connecting the analog signal to the Schmitt trigger input, and then connecting the output to the external clock input.

The Schmitt trigger firing (see Figure 5-5) is governed by setting the source and threshold controls. A voltage between +5V and -5V is coarsely selected by setting the threshold knob to the far right for +5V, far left for -5V, or at some point in between. The slope, either positive-going or negative-going, is then chosen by setting the slope switch to either + or -. At this point, each time the external signal crosses the preset voltage in the indicated direction, the Schmitt trigger fires, causing a pulse to be generated. This pulse is referred to as an event.

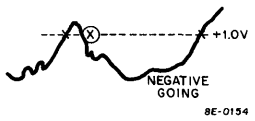


Figure 5-5 Schmitt Trigger Definition

Other Enable bit functions are discussed in the next section on clock programming.

If threshold was set to +1V and slope to +, then the asterisks indicate a pulse generated, whereas the X does not. Even though the threshold was crossed, the second condition of slope was not satisfied; thus, a pulse was not produced.

Clock Status Register

The Clock Status Register (see Figure 5-6) contains events 1, 2, 4, and the overflow bit.

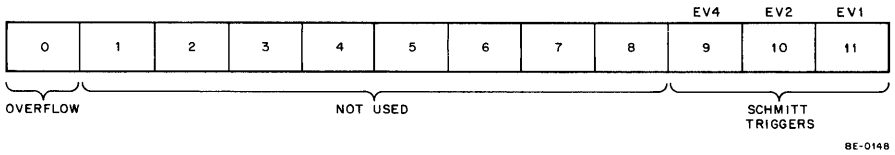


Figure 5-6 Clock Status Register

PROGRAMMING

The following IOT instructions control the DK8-ES Real-Time Clock:

Clear Clock Enable Register per AC (CLZE)
Octal Code: 6130
Operation: Clears the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

Skip on Clock Interrupt (CLSK)
Octal Code: 6131
Operation: Causes the next instruction to be skipped if an interrupt condition exists.

a. An enabled Schmitt trigger has fired.

b. The clock counter has overflowed.

Set Clock Enable Register per AC (CLOE)
Octal Code: 6132
Operation: Sets the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

AC to Clock Buffer-Preset (CLAB)
Octal Code: 6133
Operation: Causes the contents of the AC to be transferred into the Clock Buffer-Preset; then causes the contents of the Clock Buffer-Preset to be transferred into the clock counter. The AC is not changed.

Load Clock Enable Register (CLEN)
Octal Code: 6134
Operation: Causes the contents of the Clock Enable Register to be transferred into the AC.

Clock Status to AC (CLSA)
Octal Code: 6135
Operation: Interrogates the Clock Input and Overflow Status flip-flops. The clock status information is inclusively ORed into the AC, then all status bits are cleared. This procedure ensures that only one occurrence of an event will be transferred to the program.

The status condition is established as follows:

AC Bit	Status Condition
0	Overflow
9	Event 4
10	Event 2
11	Event 1

Clock Buffer to AC (CLBA)
Octal Code: 6136
Operation: Clears the AC, then transfers the contents of the Clock Buffer into the AC.

Clock Counter to AC (CLCA)
Octal Code: 6137
Operation: Clears the AC, transfers the contents of the clock counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC.

NOTE

The clock counter can be read while it is counting. Gating in the clock control section prevents data from being strobed out of the counter before a specified time following a clock pulse. This time, approximately 300 ns, allows the data to be settled in the counter.

This feature allows the counter to be read any number of times without introducing timing errors in counting; it allows the counter to read the amount of time between intervals, and it also eliminates false counts that are the result of reading the counter as one or more bits are in transition from one state to another.

Programming Examples

```
          *1
          JMP I 2
          SERVC              /POINTER TO INTERRUPT SERVICE ROUTINE

          *200
START,    CLA CLL
          DCA HIGH           /ZERO HIGH ORDER WORD
          TAD ENABLE
          CLOE               /LOAD ENABLE REGISTER
          CMA                /CLEAR UNUSED BIT
          CLZE
          ION                /AND TURN ON INTERRUPT
                             MAIN PROGRAM

           .
           .
           .
           .
SERVC,    CLSK               /WAS INTERRUPT CAUSED BY CLOCK FLAG?
          JMP RETURN         /NO
          CLSA               /READ STATUS, IGNORE FLAG AND CLEAR IT
          SPA CLA            /WAS STATUS REGISTER NEGATIVE?
          ISZ HIGH           /YES, INCREMENT THE HIGH ORDER WORD
          JMP RETURN         /AND RETURN IF HIGH DID NOT OVERFLOW
          JMP SOMEWHERE      /AFTER 4096*4096 COUNTS, DO SOMETHING
RETURN,   ION
          JMP I 0

ENABLE,   4210               /OVERFLOW, + MODE 00 + 100 HZ RATE +
                             /INTERRUPT ENABLE
HIGH,     0
```

Example Subroutine#1 — This example illustrates how the DK8-ES Real-Time Clock can be used as a double-precision (24-bit) free-running clock, using the clock counter as the low-order 12 bits and a memory location as the high-order 12 bits. Because all the registers of the clock have been set to 0 initially by the clear key, it is necessary that the program only zero the high-order words, set the Enable Register, and turn on the interrupt. After 4096 counts, the clock counter overflows, signalling an interrupt. The service routine simply increments the high-order word, then returns to the main program.

With this program, time can be kept during program execution. With the clock set to its fastest rate (1 μs per tick), this double-precision counter can mark time for just over 16 seconds; with the clock set to its slowest rate, it can mark time for over 100 days.

A simple routine can be written to interrogate elapsed time by using the CLCA (Clock Counter to AC) command.

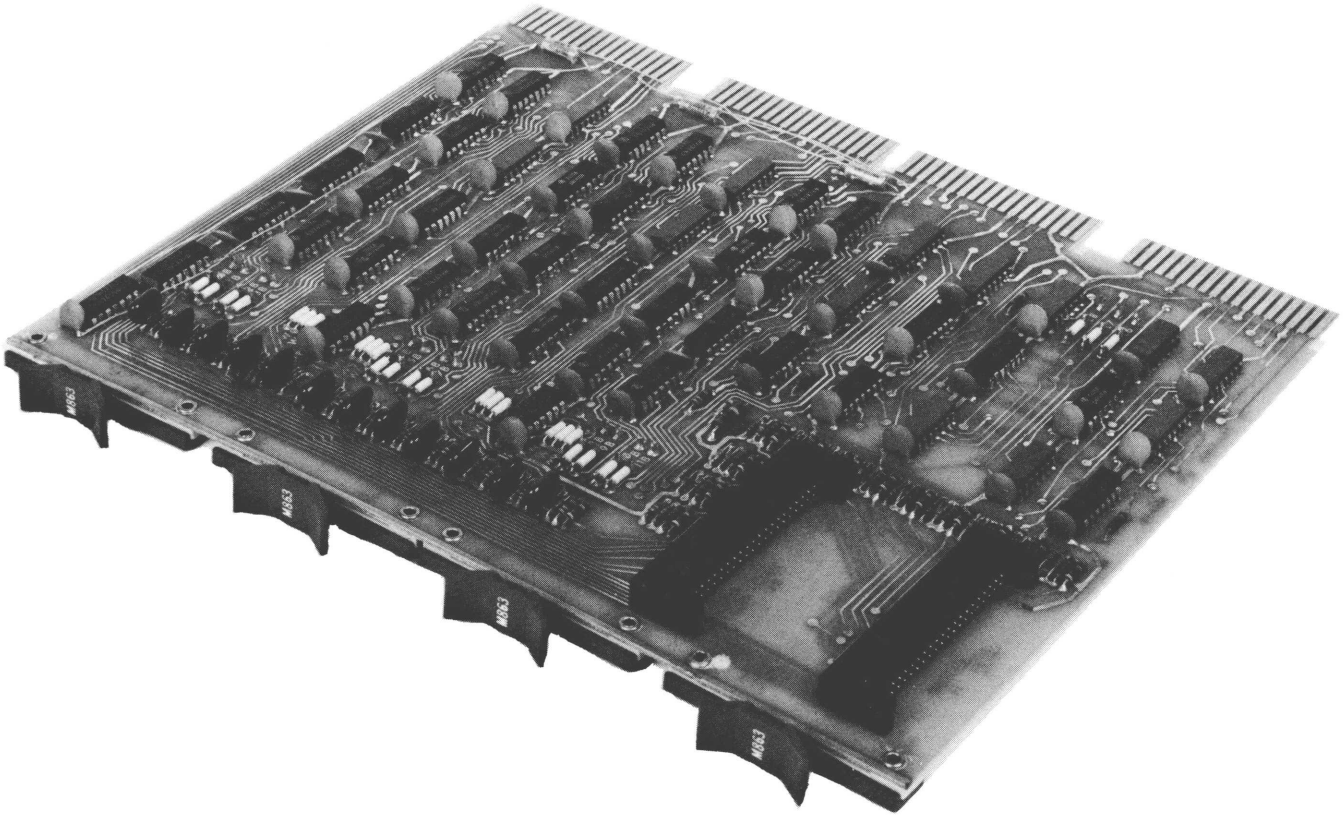
Example Subroutine #2 — The DK8-ES can also easily be programmed to function as an alarm clock, counting off a period of time, giving an alarm, automatically resetting itself, and continuing. The alarm could be used to ring a bell, as indicated in the example; however, a more practical use might be to start an analog-to-digital converter to take a number of samples from an external source.

In this example, the bell will ring every second:

```
START,    CLA
           TAD COUNTER       /SET COUNTER TO -1000 DECIMAL
           CLAB
           CLA
           TAD ENABLE        /SET ENABLE REGISTER
           CLOE
AGAIN,    CLSK               /CLOCK SKIP?
           JMP.-1
           CLSA
                             /YES, READ STATUS AND CLEAR IT
           CLA
           TAD BELL          /RING BELL
           TLS
           TSF
           JMP.-1
           JMP AGAIN
COUNTER,  -1750
ENABLE,   OVERFLOW + MODE 01 + 1 MS # 5300
BELL,     207
```

6

BUFFERED DIGITAL I/O



Buffered Digital IO (DR8-E)

DR8-EA 12-CHANNEL BUFFERED DIGITAL I/O

GENERAL DESCRIPTION

The DR8-EA 12-Channel Buffered Digital I/O (see Figure 6-1) can be used to control 12 discrete digital switching circuits (externally located) and can also be used to accept 12 discrete inputs from external sources. The unit consists of IOT control logic, a 12-bit input buffer, a 12 bit output buffer, and 3 multiplexer ICs that control the flow of data for input and output operations. All circuits are transistor-to-transistor (TTL) logic and are mounted on a single PDP-8/E module that plugs into the OMNIBUS. Standard TTL outputs are connected to the external load via two H854 connectors on the module. Inputs from external sources are also connected to the DR8-EA, using H854 connectors.

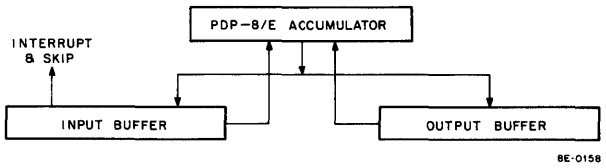


Figure 6-1 12-Channel Buffered Digital I/O -Block Diagram

A maximum of eight DR8-EA options can be used. Each device selector code is determined by the user through various jumpers. Device codes 50 to 57 are legal; however, the DR8-EA normally comes with device code 50 installed.

The DR8-EA is contained entirely on one 8-½ in. Quad-type board (M863). The module can be used in the PDP-8/E OMNIBUS, BE8 expanded OMNIBUS, or BA8 expander.

Output Transfers

Data outputs are updated under program control. Standard output drivers have a TTL 30-unit load capability. For an output function, the computer issues a DBR0, DBS0, or DBC0 instruction. For DBS0 instructions, only logical 1s in the AC are loaded into the output register; AC bits containing logical 0s do not affect output register bits. For DBC0 instructions, logical 1s in the AC result in logical 0s in corresponding bits of the output register. For DBR0 instructions, the contents of the output register are transferred into the AC register.

Input Transfers

Data inputs must be TTL compatible, have negative transition to 0.8V or less for a logical 1, and have a pulse duration of greater than 50 ns. Pulse rise and fall time should be less than 150 ns for maximum noise immunity. In one mode of operation, the input register bits, after being set by the data inputs, remain set until read by a DBRI instruction and cleared by a DBCI instruction. In the second mode of operation, the input can be placed directly through gating on the bus and remains as long as the input remains. The DBRI instruction is also used to

read the input data. When this IOT is issued, the contents of the input register are gated to the AC via the OMNIBUS. A DBCI instruction, used with DBRI instruction, enables inputs that occurred too late to be read by the next DBRI instruction, provided that the frequency of input data is greater than the time elapsed between the issuing of the DBRI instruction and the DBCI instruction. Correct usage of this feature results in " zero dead time " for events. Any of the input lines can cause an interrupt if the proper jumpers are selected. The interrupt facility can be enabled by the DBEI instruction and disabled by the DBDI instruction.

SPECIFICATIONS

Input Format:	Parallel, 12 bits
Input Levels:	TTL-compatible levels. Input lines are clamped at +5V for positive input protection.
Input Connections and Pulse Width:	Inputs to Inverter buffers are normally held high by resistors. A negative transition of 0.8V or less will cause the input to become a logical 1. Optional inputs bypass the flip-flop for direct interrogation of input line status.
Output Format:	Parallel, 12 bits
Output Levels:	TTL-compatible levels capable of driving 30 unit loads. Output lines are protected from short circuits to ground.
Environmental:	0° C to 55° C 10% to 90% relative humidity (non-condensing)
Power Requirements:	+5.0V, 2.25A (worst case)

Jumper Descriptions

The following chart will enable the user to change the IOT device code by changing the jumper across the specified split lug.

Device Selector	Jumper
50 (normal conf)	6H 7H 8H
51	6H 7H 8L
52	6H 7L 8H
53	6H 7L 8L
54	6L 7H 8H
55	6L 7H 8L
56	6L 7L 8H
57	6L 7L 8L

The normal configuration will be factory installed with device selector code 50. The input will have Jumper A (edge triggered flip-flop) installed at the factory. To change to level Enables, use jumper B. The A and B lugs are on all 12 bits. Jumpers will also be provided to isolate the inputs from the interrupt and skip circuitry.

PROGRAMMING

The following instructions are used for DR8-EA operation. The X refers to a jumper selectable code; however, the DR8-EA normally comes with code 50 installed.

Disable Interrupt (DBDI)
Octal Code: 65X0
Operation: Disable all interrupts that are caused by logical 1 on input.

Enable Interrupts (DBEI)
Octal Code: 65X1
Operation: Set Interrupt Enable Flip-Flop. This tests the In Flag and causes the Interrupt Request if In Flag equals 1.

Skip on Flag (DBSK)
Octal Code: 65X2
Operation: Tests the In Flag. If the flag is a 1, the next sequential memory location is skipped.

Clear Selective Input Register (DBCI)
Octal Code: 65X3
Operation: Ones in the AC clear the respective bits in the Input Register.

Transfer Input to the AC (DBRI)
Octal Code: 65X4
Operation: Transfers the complete 12-bit Input Register to the AC.

Clear Selective Output Register (DBCO)
Octal Code: 65X5
Operation: Ones in the AC clear the respective bits in the Output Register.

Set Selective Output Register (DBSO)
Octal Code: 65X6
Operation: Ones in the AC set the respective bits in the Output Register.

Transfer Output to AC (DBRO)
Octal Code: 65X7
Operation: Transfer the complete 12-bit Output Register to the AC.

Programming Examples

Example 1: Assume that 10 bits of digital information are to be transferred to the PDP-8/E. When the data is ready, the occurrence of one of two possible pulses defines this information.

Solution: Define input bits 2-11 as data and remove the interrupt jumpers. Define input bit 0 as process one; this causes an interrupt. Define input bit 1 as process two, and this also causes an interrupt. Define output 0 as the data accepted pulse.

```
SET UP, CLA, CLL    /CLEAR THE AC AND THE LINK
        CMA         /ALL ONES THE AC
        DBCI        /CLEAR THE INPUT REGISTER
        DBCO        /CLEAR THE OUTPUT REGISTER
        DBEI        /ENABLE THE INTERRUPTS IN DR8-EA
        ION         /TURN ON INTERRUPTS
        JMP PROGRAM /JUMP TO PROGRAM THAT WAITS FOR DATA
```

When an interrupt occurs, the program goes to the location specified and jumps to the interrupt handling routine.

```
    DBSK        /SKIP ON AN INPUT FLAG
    SKP         /SKIP TO NEXT IN CHAIN
    JMP INPUT   /GO TO DATA PROCESSING ROUTINE
```

Data processing routine will define and accept the data.

```
INPUT,  CLA, CLL    /CLEAR THE AC AND LINK
        DBRI        /TRANSFER TO AC
        DBCI        /CLEAR THE BITS THAT WERE SET
        DCA TEMP    /STORE
        DBDI        /DISABLE INTERRUPT
        TAD 4000    /BIT 0 #1
        DBSO        /CREATE START OF PULSE
        DBCO        /END THE PULSE (1.2 US PULSE)
        CLA, CLL    /CLEAR AC # LINK
        TAD TEMP    /ADD IT TO THE AC
        SMA         /CHECK FOR BIT 0 #1
        JMP P2      /JUMP TO PROCESS TWO
        JMP P1      /JUMP TO PROCESS ONE


          THE DATA IS THEN IN PROCESS

P2,     CLA
        TAD TEMP    /ADD TOTAL REGISTER
        AND K1777   /MASK FOR DATA
        DCA DATA    /STORE IT
```

Example 2: Twelve random events may occur at any time; the object of this exercise is to control their corresponding output functions.

Solution: Define the same corresponding input and output bits; i.e., bit 0 input event — bit 0 output function.

```
SET UP, CLA, CLL    /CLEAR THE AC AND THE LINK
        CMA         /ALL ONES IN THE AC
        DBCI        /CLEAR THE INPUT REGISTER
        DBCO        /CLEAR THE OUTPUT REGISTER
        DBSK        /SKIP ON A FLAG
        JMP .-1     /GO BACK

INPUT,  CLA, CLL    /CLEARS THE AC AND LINK
        DBRI        /GET THE INFORMATION (TO AC)
        DBSO        /SET CORRESPONDING OUTPUT BIT
        DBCO        /CLEAR CORRESPONDING OUTPUT BIT

        (AN OUTPUT PULSE HAS BEEN CREATED.)

        DBCI        /CLEAR INPUT BIT
        JMP PROGRAM /DO SOMETHING WITH DATA
        .
        .
        .
        CONTINUE (DETECT OTHER EVENT)
```

INTERFACE

The DR8-EA interfaces to the PDP-8/E OMNIBUS by plugging directly into the bus. Two edge connectors on the M863 Module provide the interface to the outside world. Signals leaving the board (12 bits parallel) are high (+3V) for a logical false and ground (0V) for a logical true. Each output line has approximately 20 mA of drive (high level) and 20 mA of sink (low level). Output levels remain fixed except when changed by the processor.

Signals entering from the outside world must be in TTL format. The input represents approximately two unit loads. When jumpered for " edge detection ", a negative-going edge (3V to 0V) is sensed. The signal must remain low (0V) for at least 50 ns. When sensing for an external level (jumpered to bypass the flip-flop), ground (0V) represents a logical true, and a high (+3V) represents a logical false. With all bits jumpered in this manner, the option represents a 12-bit parallel input register rather than an event decoder.

An optional method for interfacing to the DR8-EA is as follows: two BC08J-X cables are provided. Each cable (ribbon-type) is terminated by a Berg-type connector on one end (for interfacing to the DR8-EA module) and a standard DEC Flip-Chip on the other. One cable is used for the input and the other for output.

Cable Descriptions

The 7008418 cable is used to jumper the input to the output for diagnostic purposes. The cable is part of the

DR8-EA option. If the user desires interface cables, the BC08J cables can be purchased. The BC08J cable includes the 1210073-0 Berg connector, a cable, and the M953 Module.

PIN CONNECTIONS

J2 — Input	J1 — Output
D — Bit 0	D — Bit 0
F — Bit 1	F — Bit 1
J — Bit 2	J — Bit 2
L — Bit 3	L — Bit 3
N — Bit 4	N — Bit 4
R — Bit 5	R — Bit 5
T — Bit 6	T — Bit 6
V — Bit 7	V — Bit 7
Z — Bit 9	Z — Bit 9
BB — Bit 10	BB — Bit 10
DD — Bit 11	DD — Bit 11

The input and output pins corresponding to the AC bits enabled on the M863 Module (DR8-EA) are as follows:

Input and Output End Pins (BC08J)	Grounds
Bit 0 — B1	A1 C2
Bit 1 — D2	C1 F2
Bit 2 — D1	F1 J2
Bit 3 — E2	K1 L2
Bit 4 — E1	N1 N2
Bit 5 — H2	R1 R2
Bit 6 — H1	T1 U2
Bit 7 — K2	
Bit 8 — J1	
Bit 9 — M2	
Bit 10 — L1	
Bit 11 — P2	

7

LABORATORY MOUNTING PANEL

H945 MOUNTING PANEL

The laboratory mounting panel is designed for compact, versatile packaging of modular accessory equipment for laboratory environments. The panel is a 19-in. rack-mounted unit with H945 Mounting Panel frame and housing that accepts plug-in type modules or module panels. Modules can be single-width, double-width, or other multiples of single-width, and may contain a printed circuit card mounted on the vertical dimensions. Controls and input/output connectors for peripheral equipment are mounted on the module front panel. Modules or module panels are attached to the panel frame, using one fastener at the top and bottom of the module panel.

The following options are available:

H945	Housing (rack-mountable chassis) for mounting laboratory peripherals, including space for mounting 11 panel units; 5 single-panel units; 3 double-panel units, and a single 1-1/2 panel, unit filler panel.
H945-BA	115V Table-Top version with super cover.
H945-BB	230V Table-Top version with super cover.
H945-CA	115V Rack-Mounted version
H945-CB	230V Rack-Mounted version
AM8-EC	Analog input Panel —16-channel A/D panel used for AM8-EA multiplexer inputs. Panel contains four 3-conductor phone jacks, four 10-turn vernier controls, and two connectors. Panel requires three single-panel unit widths.
AM8-ED	Simple analog input Panel — 16-channel A D panel used for AM8-EA multiplexer inputs. Panel contains two connectors and requires a single-panel unit width.
VM03	Tektronix Model 602 Oscilloscope Mounting Hardware
VR14	115 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-A	230 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-B	100 Vac CRT Display with mounting hardware for Rack-Mounted version.
VR14-C	115 Vac CRT Display with mounting hardware for Table-Top version.
VR14-D	230 Vac CRT Display with mounting hardware for Table-Top version.
VR14-E	100 Vac CRT Display with mounting hardware for Table-Top version.
DK8-EF	Real-Time Clock Input Panel — 3 external Schmitt trigger inputs, 3 outputs, external clock in, and external overflow.
DR8-EC	Digital I/O Panel — 12-bit output and 12-bit input, including two M904 Modules.

digital equipment corporation