DEC-8I-HODA-D

KB8/I
GENERAL INPUT/OUTPUT INTERFACE OPTION DESCRIPTION

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INTRODUCTION

The KB8/I General Input/Output Interface Option provides an interface between a positive bus PDP-8/I and any I/O device. All data transfers, both to and from the PDP-8/I, can be controlled by the I/O device via the KB8/I. The KB8/I operates in two basic modes: receive and transmit; they are designated as follows:

a. KB8/I-A - Receiver
b. KB8/I-B - Transmitter

The KB8/I-A and KB8/I-B variations can be used separately or together in the same PDP-8/I mainframe. This manual discusses each mode as a separate function.

SPECIFICATIONS

The KB8/I-A consists of one M107 IOT Decoder, one M738 Receiver module, and one 15-ft I/O cable (BC08A-15).

The KB8/I consists of one M737 Transmitter/IOT Decoder and one 15-ft cable (BC08A-15). Table 1 lists the power requirements.

Table 1
Power Requirement Specifications*

Module	Voltage	Current (max.)
M107	+5V	245 mA
M737	+5V	300 mA
M738	+5V	370 mA

*Power is supplied by the PDP-8/I mainframe.

Environmental Specifications

Temperature: 32°F to 130°F (0°C to 54°C)
Relative Humidity: 10% to 95%, non-condensing

Data Format

The data format consists of 12 parallel data bits transferred between the PDP-8/I and an external device.

Voltage levels for the KB8/I are 0V for a logical 0V and +3V for a logical 1V, providing direct TTL logic interfacing and the appropriate diode clamp protection.

PROGRAMMING DESCRIPTION

The KB8/I utilizes device selection codes 36 and 37 for programmed IOT instructions. Device selection code 36 is used by the KB8/I-B Transmitter for the two IOT instructions. Device selection code 37 is used by the KB8/I-A Receiver for the seven IOT instructions.

The KB8/I-A Receiver uses the following instructions:

Skip on Receive Flag 1 (SKA)

Octal Code: 6371
Event Time: 1
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: When Receive Flag 1 is set, skip the next instruction.
Symbol: Does RF1 = 1? If yes, AC + 1 → AC

Skip on Receive Flag 2 (SKB)

Octal Code: 6372
Event Time: 2
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: When Receive Flag 2 is set, skip the next instruction.
Symbol: Does RF2 = 1? If yes, AC≠1 → AC

Clear Accumulator (ACCL)

Octal Code: 6373
Event Time: 1, 2
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Each of 12 accumulator bits is cleared to binary 0.
Symbol: 0 → AC0-11

Strobe Data and Set Receive Flag 1 (STB, SFA)

Octal Code: 6374
Event Time: 3
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Strobe data onto accumulator bus and set Receive Flag 1 (jam transfer).
Symbol: Data → AC0-11
1 → RF1

Clear Receive Flag 1 (CFA)

Octal Code: 6375
Event Time: 1, 3
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Receive Flag 1 is cleared to binary 0.
Symbol: 0 → RF1

Strobe Data and Set Receive Flag 2 (SDN, SFB)

Octal Code: 6376
Event Time: 2, 3
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Strobe data from external device into counter/buffer and set Receive Flag 2 (jam transfer).
Symbol: Data → CB
1 → RF2

Stop Clock and Clear Receive Flag 2 (SCK, CFB)

Octal Code: 6377
Event Time: 1, 2, 3
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Stop data modification by resetting clock flip-flop and clear Receive Flag 2 to binary 0.
Symbol: 0 → Clock FF
0 → RF2

The KB8/I-B Transmitter uses the following instructions:

Skip on Transmit Flag 1 (STFA)

Octal Code: 6361
Event Time: 1
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: When Transmit Flag 1 is set, skip the next instruction.
Symbol: Does TF1 = 1? If yes, AC + 1 → AC

Load Output Bus and Clear Transmit Flag 1 (LBD, CTFA)

Octal Code: 6362
Event Time: 2
Indicators: IOT, FETCH, PAUSE
Execution Time: 4.25 μs
Operation: Load accumulator bits 0 through 11 into buffer register and clear Transmit Flag 1.
Symbol: AC0-11 → BR
0 → TF1

Use of the KB8/I-A Receiver is illustrated in the following programming example:

```
START   CLA
          .
          .
        SDN,SFB   /Strobe data in from
                  /device and set RF2
        SKB       /Skip on RF2
        JMP .-1   /Jump back one instruction
        CFB       /Clear RF2
        STB,SFA   /Transfer data to the ac-
                  /cumulator bus and set
                  /RF1
        SKA       /Skip on RF1
        JMP .-1   /Jump back one instruction
        CFA       /Clear RF1
        JMP       /Jump to start
```

Use of the KB8/I-B Transmitter is illustrated in the following programming example:

```
BEGIN   CLA
        TAD
          .
          .
        LDB,CTFA  /Transfer data to the
                  /external device and
                  /clear TF1
        STFA      /Skip on TF1
        JMP .-1   /Jump back one instruction
        JMP       /Jump to begin
```

OPERATION

KB8/I-A Receiver (see Figure 1)

The KB8/I-A Receiver receives 12 bits of data in parallel from the external device and loads them, upon application of the load pulse, into the counter/buffer. The data presented to the bus driver from the counter/buffer is sent (when strobe pulse is used) to the PDP-8/I accumulator as 12 parallel data bits.

The external device can increment the data by first enabling the clock in the M738 and then sending one clock pulse per increment to the counter/buffer. The modified data is then sent to the accumulator. Refer to Engineering Drawing D-BS-KB8I-0-01 to supplement the following discussions.

IOT Decoder Circuit

Each program instruction stored in core memory is read into the PDP-8/I memory buffer register (MB) for execution. When the computer recognizes a KB8/I-A IOT instruction (637X), it generates a select code based on the 37_8 configuration of bits MB03 through MB08. Module M107 of the KB8/I-A accepts this select code and produces a SELECT enabling signal (D7,8).* The computer also enables its IOP generator to produce IOP pulses as determined by bits MB09 through MB11. These IOP pulses, together with bits MB09 through MB11 (C7), are ANDed into the decoder network (C7) with the SELECT enabling signal to produce the seven IOT pulses required by the KB8/I-A.

The outputs of the decoder are designated by two numbers separated by a hyphen. The number before the hyphen indicates the octal value of bits MB09 through MB11. This number corresponds to the least significant digit of the octal codes for the seven KB8/I-A instructions. The number after the hyphen indicates the IOP pulse (1, 2, or 4) at which the IOT occurs. These numerical designations are used elsewhere on the logic diagram to indicate inputs to other circuits. An example is the designation IOT 1-1, which indicates a true signal resulting

*The alphanumeric designation refers to the coordinate locations of signals and circuits on DEC Drawing D-BS-KB8I-0-01.

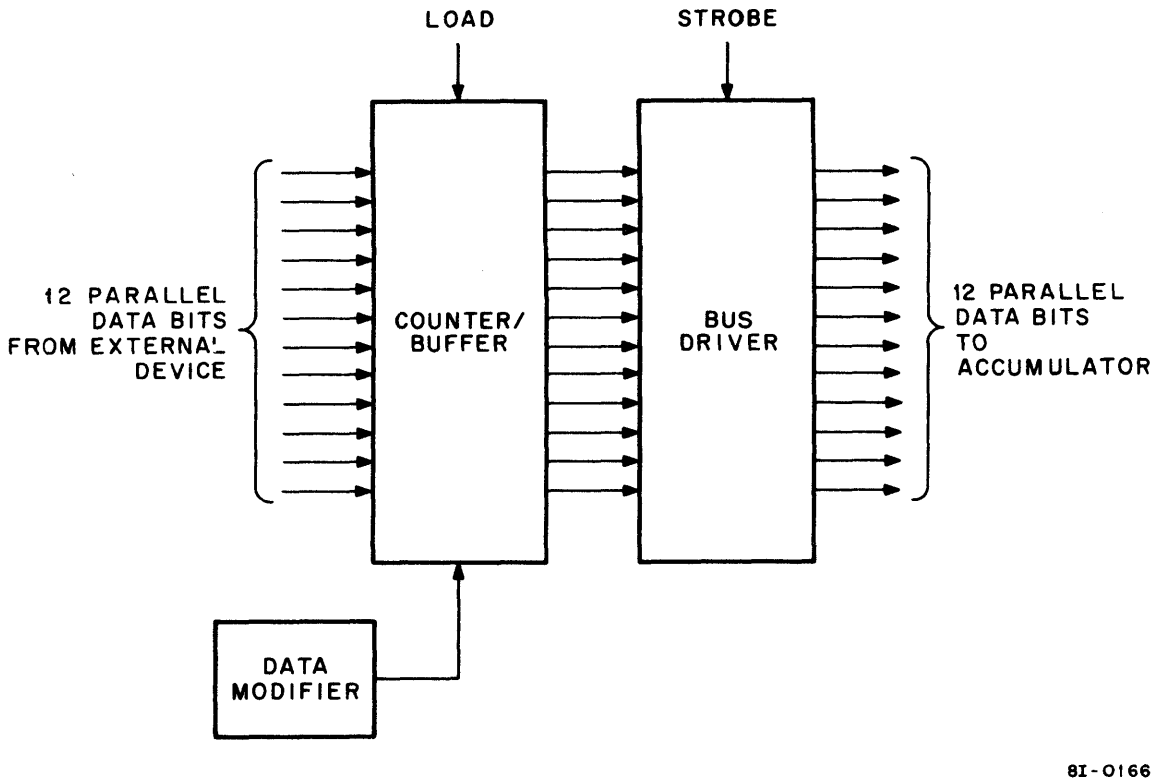

Figure 1 KB8/I-A Receiver

from the decoding of a 6371 SKIP ON RECEIVE FLAG 1 instruction and IOP1. For more information on IOT and device selection, refer to the input/output section of the DEC Small Computer Handbook.

Clear Accumulator

The accumulator (AC) must be cleared to all zeros before data transfer. Otherwise, the resulting word in the AC will be the inclusive OR of the previous word in the AC and the current word being transferred. To accomplish the clearing, the KB8/I-A provides signal I/O BUS IN AC CLR (D1) to the computer I/O bus. This signal is generated whenever IOT 3-2 is issued (D3).

Receiver Circuit

Initially, the I/O device generates signal CLR CNTR/BUFF, which clears all flip-flops in the counter/buffer (B3). To be true, this signal must be at 0V for a minimum of 3 μs. IOT 6-4 (B3) is then issued and jam-transfers the data from the device into the counter/buffer. At this point, if the data is to be incremented, the external device initiates a 0V start clock pulse (B7) which clears the clock flip-flop (B5).

The 0-side output (high) of the clock flip-flop is gated with a device-generated, positive-going clock pulse (B7) to provide a shift pulse (one shift pulse per clock pulse). The shift pulse is gated into the counter/buffer for the amount of incrementation desired. If overflow

from the counter/buffer occurs, +3V signal OVERFLOW (B3) is sent back to notify the external device. When the data has been sufficiently incremented, an IOT 7-4 instruction is issued (A6), which sets the clock flip-flop, thereby inhibiting further shift pulses.

With the data modification complete, IOT 4-4 (C2) is issued, initiating a strobe pulse to the bus driver (B2), which, in turn, transfers the contents of the counter/buffer to the PDP-8/I accumulator. If incrementing of the data is not desired, IOT 4-4 is issued immediately and the data is transferred directly into the accumulator.

Interrupt Request and Skip Circuits

A program interrupt request can be generated by the set side of either REC'V FLAG 1 (C4) or REC'V FLAG 2 (C3) flip-flop. The command to skip the next instruction can be generated by the combination of the set side output of either the REC'V FLAG 1 or REC'V FLAG 2 flip-flop and a programmed IOT instruction.

IOT 4-4 is issued when data from the external device is ready to be strobed into the computer. In addition, IOT 4-4 sets the REC'V FLAG 1 flip-flop. The set output of this flip-flop is applied to both a NOR gate (D3) and to one input of a two-input NAND gate (D3). The 0V output of the NOR gate is designated I/O BUS IN INT and initiates a program interrupt request to the PDP-8/I. When the 0V IOT 1-1 is issued, it is amplified (D4) to 3V and applied to the other input of the NAND gate. This input, together with the set output of REC'V FLAG 1, qualifies the NAND gate and generates the output signal I/O BUS IN SKIP (D1), which, in turn, instructs the computer to skip the next instruction. (IOT 1-1 effectively samples the state of REC'V FLAG 1 output.)

The REC'V FLAG 2 flip-flop initiates an interrupt request and a skip command in much the same manner as REC'V FLAG 1. However, REC'V FLAG 2 flip-flop is set by a device-generated signal designated SET FLAG 2 (C3). The set output is applied to the same NOR gate (D3) as REC'V FLAG 1 and generates the interrupt signal I/O BUS IN INT. The set output is also applied to one input of a two-input NAND gate (C2). When the 0V IOT 2-2 is issued, it is amplified to 3V (C3) and applied to the other input of the NAND gate. With both inputs high, the NAND gate is enabled, producing the signal I/O BUS IN SKIP.

INITIALIZE

When the system is first turned on, the PDP-8/I generates a 3V INITIALIZE signal, which is inverted and gated to the reset inputs of REC'V FLAG 1, REC'V FLAG 2 and clock flip-flops.

KB8/IB Transmitter (see Figure 2)

In the KB8/I-B Transmitter portion, 12 parallel data bits are received from the PDP-8/I accumulator and, upon application of the select level enable pulse, are loaded into the buffer register. When input/output pulse 2 (IOP2) is received, data stored in the buffer register is strobed into the output buffer and presented to the external device as 12 parallel data bits. Refer to Engineering Drawing D-BS-KB8I-0-02 for the following discussion.

Transmitter Logic Operation

The external device generates a set signal (C5) which sets the XMIT FLAG 1 flip-flop (C5), indicating that the device is ready to accept data from the PDP-8/I. If a program interrupt request to the computer is required, the set output of the XMIT FLAG 1 flip-flop and the device-generated signal PI ENABLE (C4) are ANDed together (C3). The output of the AND

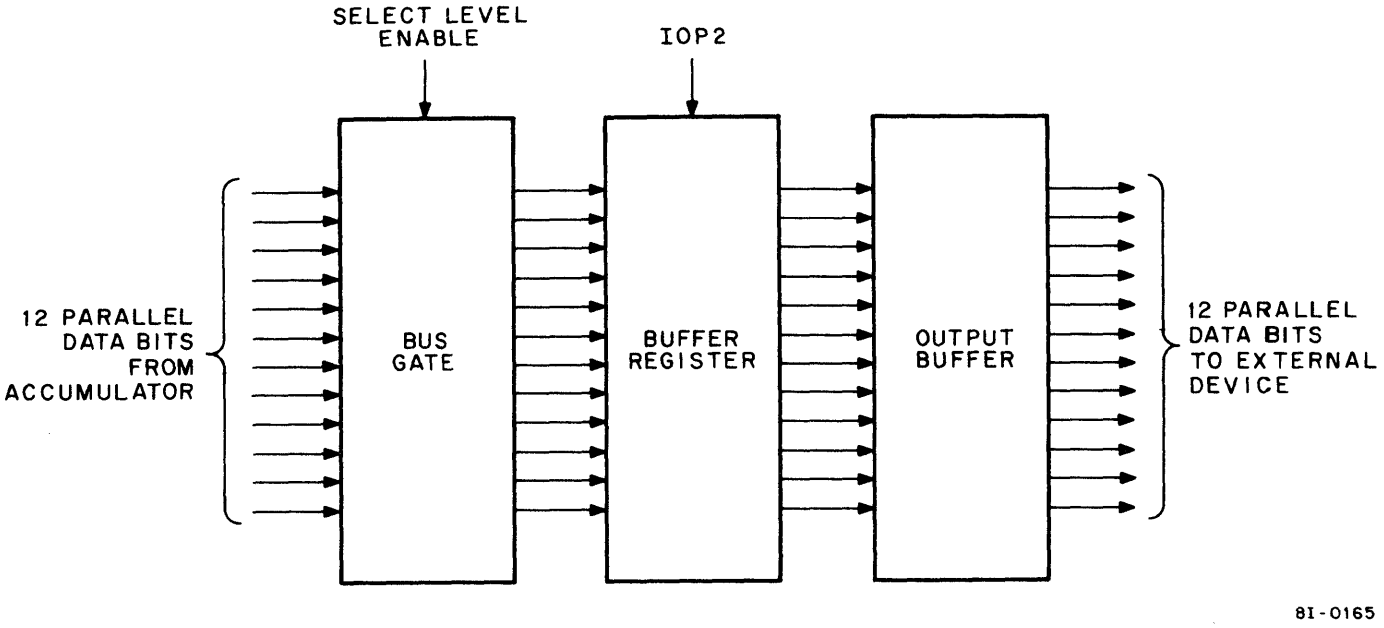

Figure 2 KB8/I-B Transmitter

gate is inverted to 0V to produce the signal I/O BUS IN INT (C2). The FLAG 1 signal (C4) is at 0V for the length of time that the flag is set, and allows the external device to monitor the status of XMIT FLAG 1 flip-flop.

For data to be transmitted via the KB8/I-B, the computer supplies a device select code of 36_8 by means of memory buffer bits MB03 through MB08. The KB8/I-B decodes bits MB03 through MB08 (D6) and, when it recognizes the 36_8 configuration, generates a multipurpose select level signal (output of OR gate, D5). This select level enables the bus gate (B6), allowing the 12 data bits in the accumulator to be loaded into the buffer register (B5). A command to skip the next instruction can be generated by the ANDing (D3) of the select level, IOP1, and the set output of XMIT FLAG 1 flip-flop. The output of the AND gate is inverted to 0V (D2) to produce the signal I/O BUS IN SKP.

When IOP2 is decoded, the resulting signal is gated (C6) with the select level, both to reset the XMIT FLAG 1 flip-flop and to transfer the data stored in the buffer register to the output buffer (B4). The data is then immediately applied to the external device. Provision is also made for the select level to be generated by an externally supplied signal instead of a programmed IOT instruction. The device initiates the signal EXT ENABLE, which is inverted to 3V (C6) and applied to the OR gate (D5) that produces the select level.

INTERFACE

The three module cards which comprise the KB8/I option are mounted within the PDP-8/I mainframe. These cards are connected to the external device by two BC08A-15 cables, one for receive and one for transmit. Each cable is

15 ft long. On either end of each cable is an M903 connector module which terminates the cable. Engineering Drawing D-UA-BC08A-0-0 details the BC08A-15 cable and its associated M903 modules.

MAINTENANCE

Maintenance procedures for the KB8/I Option are defined in diagnostic program MAINDEC-8I-D8GA.

DRAWINGS

D-BS-KB8/I-0-01	Receiver
D-BS-KB8/I-0-02	Transmitter
D-BS-KB8/I-0-03	Acceptance Procedure
D-BS-KB8/I-0-04	Engineering Specification
D-UA-BC08A-0-0	Cabling