Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-8
Data Communications Equipment

DCO8A

Serial Line Multiplexer

DEC-8I-H80A-D

DCO8A
SERIAL LINE MULTIPLEXER

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CHAPTER 1

INTRODUCTION AND DESCRIPTION

1.1 SCOPE OF MANUAL

This manual describes the DC08 Data Communications equipment in general. It contains specific information for both the DL8I Data Line Interface and the DC08A Serial Line Multiplexer. Line interface hardware options are listed in this chapter; however, detailed information for each hardware option is a separate addendum to this manual.

1.2 EQUIPMENT APPLICATION

The DC08 Data Communications equipment can interface as many as 128 serial, asynchronous, full-duplex communication lines to a PDP-8/I Computer. The DC08 equipment can be connected to a variety of lines with different baud rates; for example, communication can be with local or remote terminals, over telegraph, or any other low-speed data line. Communication can be simplex, duplex, or half-duplex (up to four different speeds), depending on the system configuration and the line options in use. In this manual, a data line is considered to be a full-duplex asynchronous line. A complete data communications system, including the PDP-8/I and the DC08, can be connected to a remote large-scale computer using a high-speed data link between computers. The DC08 and PDP-8/I then converse with the individual data lines on a real-time (low-speed) basis and provide concentrated high-speed data to the larger computer. In this application, the DC08 becomes a part of what is termed the 680I Data Communications System. The line interface options listed in Table 1-1 are used to connect the DC08 equipment to the different types of communication lines.

1.3 EQUIPMENT DESCRIPTION

The DC08 equipment usually connects the PDP-8/I Computer and one or more line interface options through use of the DL8I and the DC08A (see Figure 1-1). The PDP-8/I and two specific line interface options are shown for reference only. At least one line sampling clock is required by the DC08 system. The choice of clock frequency depends on the application; therefore, the line sampling clock is shown separately and becomes an option. One clock is supplied with the system, and unless otherwise specified, it is 110 baud. Each clock operates at five times the baud rate of the lines it is used to sample. Up to four clocks can be used to sample four different data rates under program control.

Table 1-1
Line Interface Options

DC08B Local Terminal Connector Panel
DC08C Telegraph Line Adapter Panel
DC08D Telegraph Line Terminator Panel
DC08EB Telegraph Line Current Adjustment Panel
DC08F EIA Modem Interface
DC08FE Extension to DC08F for 32 lines
DC08FF Extension to DC08FE for 32 lines
DC08FX Extension to DC08F for line status control
DC08H Automatic Calling Unit
DC08Y Line Sampling Clock

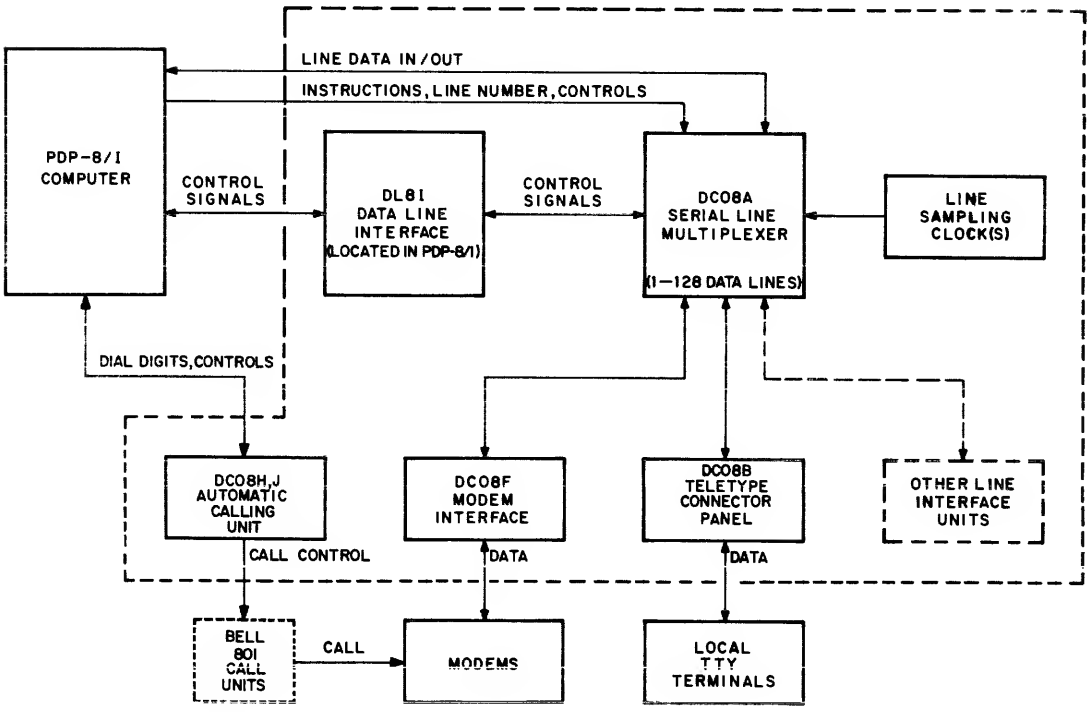


Figure 1-1 Basic Block Diagram

1.3.1 DL8I Data Line Interface

The DL8I is the control interface between the PDP-8/I and the DC08A. It is physically located in the PDP-8/I processor and is connected to the DC08A by cable.

The DL8I responds to the three special IOT instructions that are added to the PDP-8/I. On receipt of one of these special instructions, the DL8I takes control of the PDP-8/I program for the time required to transfer data to or from the communication lines via the DC08A. The DL8I also maintains a control signal interface with the DC08A.

1.3.2 DC08A Serial Line Multiplexer

The DC08A is mounted in a separate equipment cabinet located adjacent to the PDP-8/I (with DL8I). The required data line interfaces and line sampling clocks are mounted in the same cabinet as the DC08A, or in adjacent cabinets.

The DC08A is essentially an automatically controlled, dual-purpose switch that:

a. Connects any selected data line to a single line input to the computer for data transfers into the PDP-8/I.

b. Connects the single line output of the computer to any selected data line for data transfers out of the PDP-8/I.

NOTE

The DC08 equipment employs bit multiplexing (as opposed to character or message multiplexing). Using bit multiplexing, only one bit position of a data character can be transferred (in or out) each time the selected line is serviced. The line data rates are very low compared to the computer cycle rate; thus, it is possible to service all data lines in a relatively small percentage of available computer time.

1.4 SYSTEM OPERATION

The DC08 Data Communications equipment operates in response to the special IOT instructions associated with teletype information transfer. These special instructions are as follows:

a. TTO (TT out) - This instruction acts on the AC register and on the selected output line. The instruction is executed during one computer fetch (F) cycle to shift the AC contents one position to the right and transfer the rightmost bit (AC11) through the DC08A to the output line.

b. TTINCR (TT increment) - This instruction is usually microprogrammed with the TTO instruction to increment the line selection register (LSR). Incrementing the LSR causes selection of the next consecutive output line number (after the TTO action) and increases software efficiency.

c. TTI (TT in) - This instruction is used to transfer the line state from an input line to the computer. It is the most complex of the TT instructions because it involves three locations in core memory and can cause two additional cycles to follow the F cycle. The memory locations are used to store the line status word (LSW) and the character assembly word (CAW) for each input data line. The additional cycles are used to examine the LSW (S cycle) and load the CAW (C cycle) with line data at the proper time.

1.4.1 TTO (and TTINCR) Instruction Implementation

Serial data is transferred from the PDP-8/I to the data lines, using the TTO (6404) instruction. This can be done in two ways:

a. randomly, in which case the line sequence must be individually specified and software loaded into the LSR using conventional IOT instructions

b. sequentially, using combined TTO and TTINCR (6405) instructions, which increments the LSR after each output and effects a stepping action.

1.4.2 TTI Instruction Implementation

Serial data is assembled into the PDP-8/I from the data lines using the TTI (6402) instruction in a service series. The system performs the service series, scanning every line during each clock interrupt. Interrupts occur at five times the baud rate. A section of a typical service series is shown below in Figure 1-2, with details shown in Figures 1-3 and 1-4.

NOTE

CAW is initialized to 2000 for 8-bit characters and to 0200 for 5-bit characters.

```
0674    6402    TTI             /LINE 47(8)
0675    0470    LSW
0676    0200    CAW
0677    4511    JMS I ASSMBL
0700    6402    TTI             /LINE 10(8)
0701    0100    LSW
0702    2000    CAW
0703    4511    JMS I ASSMBL
0704    6402    TTI             /LINE 60(8)
```

```
0705    0600    LSW
0706    2000    CAW
0707    4511    JMS I ASSMBL
0710    6402    TTI             /LINE 11(8)
0711    0110    LSW
0712    0200    CAW
0713    4511    JMS I ASSMBL
0714    6402    TTI             /LINE 61(8)
0715    0610    LSW
0716    2000    CAW
0717    4511    JMS I ASSMBL
0720    6402    TTI             /LINE 12(8)
0721    0120    LSW
0722    0200    CAW
0723    4511    JMS I ASSMBL
0724    6402    TTI             /LINE 62(8)
0725    0620    LSW
0726    0200    CAW
0727    4511    JMS I ASSMBL
```

Figure 1-2 Typical Service Series

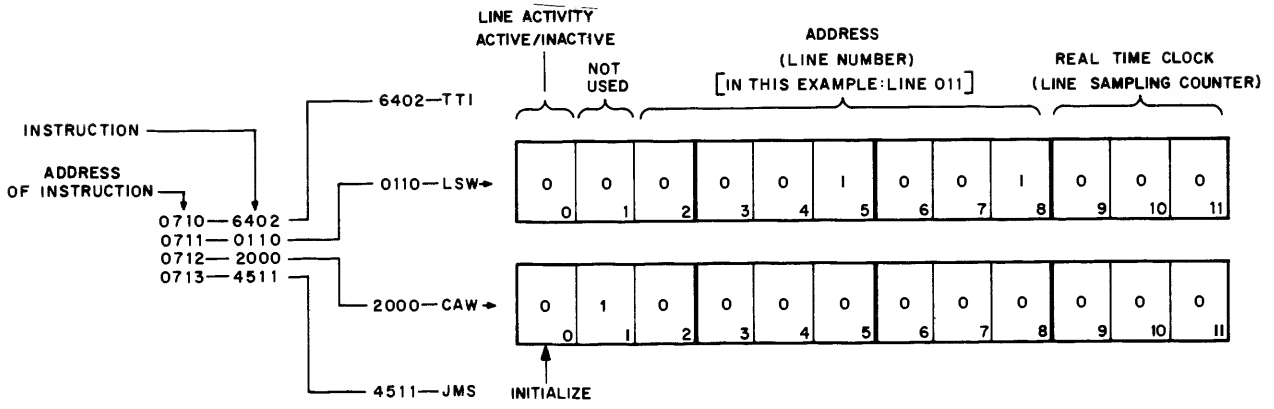


Figure 1-3 Line Servicing Group of Instructions

08-0055

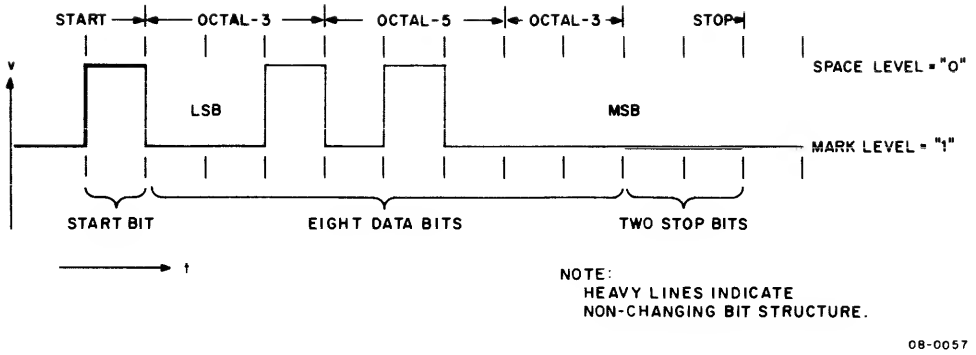


Figure 1-4 Typical Teletypewriter Character (353_8)

The service series consists of a string of line servicing instruction groups (TTI block), with one group of two instructions for each line. The servicing group shown in Figure 1-3 does not consist of four instructions as expected. The TTI command uses three memory locations, the actual TTI instruction and the two locations following it. The two locations following, used for line status and character assembly purposes, are called the line status word (LSW) and the character assembly word (CAW), respectively. The instruction following the three TTI storage locations is usually a JMS (jump to subroutine). The subroutine can be used for limited data processing and storage and is usually entered only after the CAW is complete and $R \neq 0$.

The structure of the LSW is shown in the upper portion of Figure 1-3. Bit 0 is used to indicate the activity status of the particular line. Bit 0 is a 0 if the line was inactive during the last sampling; bit 0 is a 1 if the line was active during the last sampling. Bit 1 is not used. Bits 2 through 8 contain the line number (in octal) of the line being serviced. Bits 9, 10, and 11 are used as a real-time counter to approximate the center of the bit to be sampled, thereby increasing the amount of telegraph distortion which can be tolerated over what could be tolerated with early or late sampling. Sampling takes place after the real-time clock, which is incremented on each service series after the start bit has been detected, reaches a count of two. The data is actually sampled between 40 and 60 percent after its starting point (where 50 percent is the theoretical center of the bit).

Clock interrupts (and consequently complete service series) are occurring at five times the line data rate.

Data seldom appears at exactly the same instant as the clock interrupt. The actual position (software) of the particular service group in the service series also affects sampling time.

After the data is sampled, the real-time counter continues counting clock interrupts to a count of four and is reset to zero for the next data bit. This series continues until a complete character has been assembled in the CAW. When the real-time clock count equals two and a complete character has been loaded into the CAW, all steps have been performed except the JMS. When the character is assembled, the hardware causes a JMS to be performed to store the character and re-initialize the CAW. If, however, hardware register R, software

controlled, is at zero because the programmed number of storage subroutines have already been performed, the JMS is skipped until one of the next four service series. Then the character is stored and the CAW is re-initialized. Therefore, a TTI service group always requires at least two machine cycles (TTI and LSW); at times, three machine cycles (TTI, LSW, and CAW); and sometimes the service subroutines plus the storage subroutine.

1.4.3 Conventional IOT Instructions

Table 1-2 lists the conventional IOT instructions used to program the DC08 equipment. These IOT instructions are similar to those used in programming the 680 Data Communication System. The basic difference is that load IOT's do not clear the AC.

Table 1-2
IOT Instruction Codes and Functions

IOT	Code	Function
TTI	6402	Inputs data to MB0. Requires 2 or 3 machine cycles depending on line activity and real time clock count. Fetch (F) cycle and status (S) cycle are always performed. S-cycle summarization: . MEM 2-8 → LSR . LH → HS . LINE → MB0 if MEM0 = 0 or HS = 1 . MEM + 1 → MB if MEM0 = 1 and MEM 9 = 0 and HS = 0 . MEM0 - 8 → MB0 - 8 and 0 → MB9-11 if MEM0 = 1 and MEM9 = 1 and HS = 0 . +2 → PC if MB9 - 11 $\neq$ 2 . 1 → C if MB9 - 11 = 2 (enter C cycle) C-cycle summarization: . LINE → MB0 and MEM $\overset{SR}{\rightarrow}$ MB if HS = 0 . MEM → MB if HS = 1 . +1 → PC if MB11 = 0 or if MB11 = 1 and R = 0 . 1 → LH if MB11 = 1 and R = 0 . MEM $\overset{SR}{\rightarrow}$ AC and LINE → AC0 if MB11 = 1 and HS = 0 and R $\neq$ 0 . MEM → AC if MB11 = 1 and HS = 1 and R $\neq$ 0 . 0 → LH if MB11 = 1 and R $\neq$ 0
TTO	6404	Outputs data from AC11 (buffered), summarized as: . 0 → L . AC11 → LINE output flip-flop . L → AC0 . AC SHIFT RIGHT
T1 OFF	6422	Clears clock 1 enable flip-flop; inhibits clock 1 flag flip-flop.
T2 OFF	6432	Clears clock 2 enable flip-flop; inhibits clock 2 flag flip-flop.
T3 OFF	6442	Clears clock 3 enable flip-flop; inhibits clock 3 flag flip-flop.
T4 OFF	6452	Clears clock 4 enable flip-flop; inhibits clock 4 flag flip-flop.

Table 1-2 (Cont)
IOT Instruction Codes and Functions

IOT	Code	Function
T1 SKIP	6421	Causes program to skip next instruction if clock 1 flag is set.
T2 SKIP	6431	Causes program to skip next instruction if clock 2 flag is set.
T3 SKIP	6441	Causes program to skip next instruction if clock 3 flag is set.
T4 SKIP	6451	Causes program to skip next instruction if clock 4 flag is set.
Line Selection Register (LSR) Control Instructions		
TT INCR	6401	Increments the LSR by 1. Can be microprogrammed to occur following TTO by code 6404
TTCL	6411	Clears the LSR
TTLL	6412	ORs AC5-11 into LSR
TTSL	6413	Clears the LSR and loads AC5-11 into the LSR. Microprogram of TTCL and TTLL.
TTRL	6414	ORs content of LSR into AC5-11. AC must be zero for true transfer.
R-Register (Load Distribution Counter) Control Instructions		
TTR INCR	6461	Increments the R-register by 1.
TT RR	6464	ORs content of R-register into AC7-11. AC must be zero for true transfer.
Clock Control Instructions		
T1 ON	6424	Sets clock 1 enable flip-flop; clears clock 1 flag flip-flop
T2 ON	6434	Sets clock 2 enable flip-flop; clears clock 2 flag flip-flop
T3 ON	6444	Sets clock 3 enable flip-flop; clears clock 3 flag flip-flop
T4 ON	6454	Sets clock 4 enable flip-flop; clears clock 4 flag flip-flop

1.5 LINE INTERFACE OPTIONS

The purpose of the following paragraphs is to introduce the various line interface options. Technical details of each line interface option, as well as comprehensive functional descriptions, are contained in the addenda to this manual. Terminals (both local and remote), telegraph, and dataphone lines may be interfaced using the line interface options described below.

1.5.1 DC08B Local Terminal Connector Panel

The DC08B Local Terminal Connector Panel can connect as many as 48 local lines or data sets (data only) to the DC08A. A local line is limited to approximately 1500 ft of cable. Up to three DC08B Local Terminal Connector Panels can be connected to a DC08A. However, only 128 of the available 144 lines can be used.

1.5.2 DC08C Telegraph Line Adapter Panel

The DC08C can connect as many as 32 telegraph lines to the DC08A. Four DC08C Telegraph Line Adapter Panels can be used with the DC08A.

1.5.3 DC08D Telegraph Line Terminator Panel

The DC08D provides demarcation point (terminal block) for interfacing between DEC equipment and 32 telegraph lines.

1.5.4 DC08EB Telegraph Line Current Adjustment and Meter Panel

The DC08EB provides rheostats and meters to adjust and monitor line current for transmit/receive on each of 32 lines.

1.5.5 DC08F Modem Interface Control

The DC08F can be used to interface and control as many as 64 Bell System 103A, 103E, 103F, or the equivalent, data sets to the DC08A. Line control is provided by one DC08G module and cable set for every two data lines. A DC08G consists of a M753 module and two BC01B-25 data set connector cables to connect two data sets (modems).

1.5.6 DC08FE Channel Extension

The DC08FE is used to extend DC08F by an additional 32 data lines.

1.5.7 DC08FF Channel Extension

The DC08FF is used to extend DC08FE by an additional 32 data lines.

1.5.8 DC08FX Control Extension

The DC08FX provides DC08F with the capability of reading the carrier status of all lines at any time. The DC08FX is a wiring option in the DC08F hardware.

1.5.9 DC08H Automatic Calling Unit

The DC08H provides automatic callup interface for up to 10 data lines on a per-line basis, using DC08J module and cable sets connected to Bell System Type 801 automatic calling units, or equivalent.

CHAPTER 2
INSTALLATION

2.1 DL8I DATA LINE INTERFACE INSTALLATION

All PDP-8/I Computers are wired to accept the 13 modules that form the DL8I Data Line Interface. No additional cables or power distribution lines are required.

2.1.1 Module Location

Module Utilization drawing D-MU-8I-0-17 (Sheet 1) shows the rack location of the 13 DL8I modules. Five modules are mounted in locations C07 through C11, and the remainder are mounted in locations D04 through D11.

2.1.2 Special Wiring (Field Installation Only)

All PDP-8/I Computers contain factory-installed jumpers that must be removed when options are installed in the field. Temporary Jumper drawing A-SP-8I-0-23 (Sheet 2) lists 20 jumpers that must be removed on installation of the 13 DL8I modules.

2.1.3 Power Requirements

The DL8I modules are supplied by the PDP-8/I power supply with no additional power supply needed.

2.1.4 Interface Cabling

A special cable connects location D04 in the PDP-8/I rack to location A09 in the DC08A rack and provides the interface between the DL8I and the DC08A. The cable type is W011. Connector pin signal names and origins are listed in Table 2-1.

NOTE

Two signals, TT INST and LINE MUX(0), are on I/O bus lines.

Table 2-1
PDP-8I to DL8I Connector Pin Designations

Pins	Signal	Origin	Transmit Module	Receive Module
D2	B LINE HOLD	DL8/I	M661	M101
E2	B TP3	DL8/I	M660	M113
H2	B MEM LSR	DL8/I	M660	M751
K2	B C(0)	DL8/I	M661	M101
M2	STLR	DL8/I	M661	M101
P2	B DC INST	DL8/I	M660	M101
T2	$\overline{\text{LHS(I)}}$	DC08A	M750	M516
V2	$\overline{\text{BR=0}}$	DC08A	M623	M516

2.2 SERIAL LINE MULTIPLEXER DC08A INSTALLATION

The DC08A, the required power supply, and the associated line interface units are mounted in a standard DEC Type CAB-8/I-A Cabinet. Cabinet location must be no further than 6 ft from the PDP-8/I.

2.2.1 Module Location

Module Utilization drawing DC08-A-6 (Sheets 1 and 2) shows the rack location of the DC08A modules. The total number of M901 Cable Connector modules and M750 Line I/O Control modules depends on the number of communication lines in service.

2.2.2 Power Requirements

Power is supplied by H710 Power Supplies mounted on the rear cabinet door.

+5V : 1.5A (1H710)

Power required on a per line basis is 60 mA/line. Thus, the number of H710 Power Supplies required is:

1 H710 for up to 48 lines
2 H710s for 49 to 128 lines

2.2.3 Interface Cabling

For interface cabling to the DL8I, refer to Paragraph 2.1.4. The standard interface cabling to the PDP-8/I is listed in Table 2-2. All cables are Type W011.

Table 2-2
DC08A to PDP-8/I Interface Cabling

BAC Cables (W011)	Location in DC08A
BAC (0-8)	A1
BAC (9-11), BIOP (1-4), BTS3, BTS1, B INITIALIZE	B1
BMB (0-5)	A3
BMB (6-11)	B3
AC BUS (0-8)	A5
AC BUS (9-11), SKIP	
INT-RQST BUS, AC CLEAR	B5
RUN (0), BTTINST, LINEMUX (0)	

Two additional W011-Type cables are required for transfer of signals MEM to MEM 11. Pin locations are listed in Table 2-3. The transmit module is G020 or G021 in the PDP-8/I, and the receive module is M751 in the DC08A.

Table 2-3
Memory Signal Transfer Cable Pin Locations

Pins	Signals	Pins	Signals
D2	MEM P	D2	MEM 8
E2	MEM 0	E2	MEM 9
H2	MEM 1	H2	MEM 10
K2	MEM 2	K2	MEM 11
M2	MEM 3		
P2	MEM 4		
S2	MEM 5		
T2	MEM 6		
V2	MEM 7		

The interface between DC08A and any of the options (DC08B, DC08C, DC08F) consists of two signals for each communication channel - DLInn (data input from line nn) and DLOnn (data output to line nn).

The transmit module for DLOnn and the receive module for DLInn is an M750. The signals are shown in Table 2-4.

Table 2-4
Transmit and Receive Signal Pin Designations

Signal	Pins	Signal	Pins
DLI0	C1	DLI4	M1
DLO0	D1	DLO4	N1
DLI1	E1	DLI5	P1
DLO1	F1	DLO5	R1
DLI2	H1	DLI6	S1
DLO2	J1	DLO6	T1
DLI3	K1	DLI7	U1
DLO3	L1	DLO7	V1

Location A29

Connectors Used: M901
Lines: DLI8 and DLO8 to DLI15 and DLO15 on same pins, but side 2.

Lines	Location	Lines	Location
0-15	A29	64-79	B29
16-31	A30	80-95	B30
32-47	A31	96-111	B31
48-63	A32	112-127	B32

The DC08B local terminal connector is interfaced to DC08A for 48 lines via three cables with M901 connectors. Each cable carries 32 signals (DLI and DLO for each line) and serves 16 lines. The cables are:

	Cables	
	DC08B	DC08A
First DC08B	A09	A29
	A20	A30
	A31	A31
Second DC08B	A09	A32
	A20	B29
	A31	B30
Third DC08B	A09	B31
	A20	B32
	A31	--

The polarity definitions for data signal transfer between the line interface units and the M750 modules in the DC08A are:

Mark = Low = Ground = 0V

Space = High = +3V

For these polarities the M750 modules must be jumpered as follows:

Output:	E2 to U2 and R2 to T2
Filtered input:	M2 to D2, A1 to J1, H1 to C1, N2 to V1, U1 to K1 and L2 to E1
Direct input:	M2 to J1, H1 to C1, N2 to K1 and L2 to E1

CHAPTER 3

OPERATION

Operating procedures for the DC08 Data Communications System requires the addition of character assembly subroutines in the PDP-8/I repertoire. Either 8-bit or 5-bit subroutines (or both) can be used, depending on the system configuration. Both subroutines listed below can be obtained from the Program Library, Digital Equipment Corporation, Maynard, Massachusetts.

Appendix A	DEC-8I-F8VA-D, DC08 8-Bit Character Assembly Subroutine
Appendix B	DEC-8I-F5VA-D, DC08 5-Bit Character Assembly Subroutine

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

Theory of operation for the DC08 Data Communications System is divided into three parts:

a. functional description of the DC08, with flow diagrams to illustrate the method of data transfer during TTO, TTINCR, and TTI instructions.

b. detailed description of the DL8I logic, with reference to both simplified logic and flow diagrams.

c. detailed description of the DC08A logic, with reference to both simplified logic and flow diagrams.

Reference is also made to the DL8I and DC08A logic schematics. Continue to refer to the flow diagram, Figure 4-1, as each function is described.

4.2 FUNCTIONAL DESCRIPTION

The DC08 adds two major cycles to the PDP-8/I, STATUS (S) and CHARACTER (C), as well as a modified FETCH (F) cycle, each of which is described in appropriate sequence. Each cycle is subdivided into time states. The hardware implementation of each cycle is described in subsequent paragraphs.

4.2.1 Fetch Cycle (F) (see Figure 4-1)

The F cycle is common to all TTINCR, TTI and TTO instructions (6401, 6402, and 6404). During this cycle, instruction decoding takes place, and the TTO or TTINCR instructions are performed. Portions of the TTI instruction are performed during the S and C cycles that follow.

4.2.1.1 Time State 1 (F-TS 1) - During F-TS 1, the content of the memory address register (MA) is incremented and transferred into the program counter register (PC). This is part of a conventional F cycle and is not under control of the DL8I. Instruction decoding has not yet taken place.

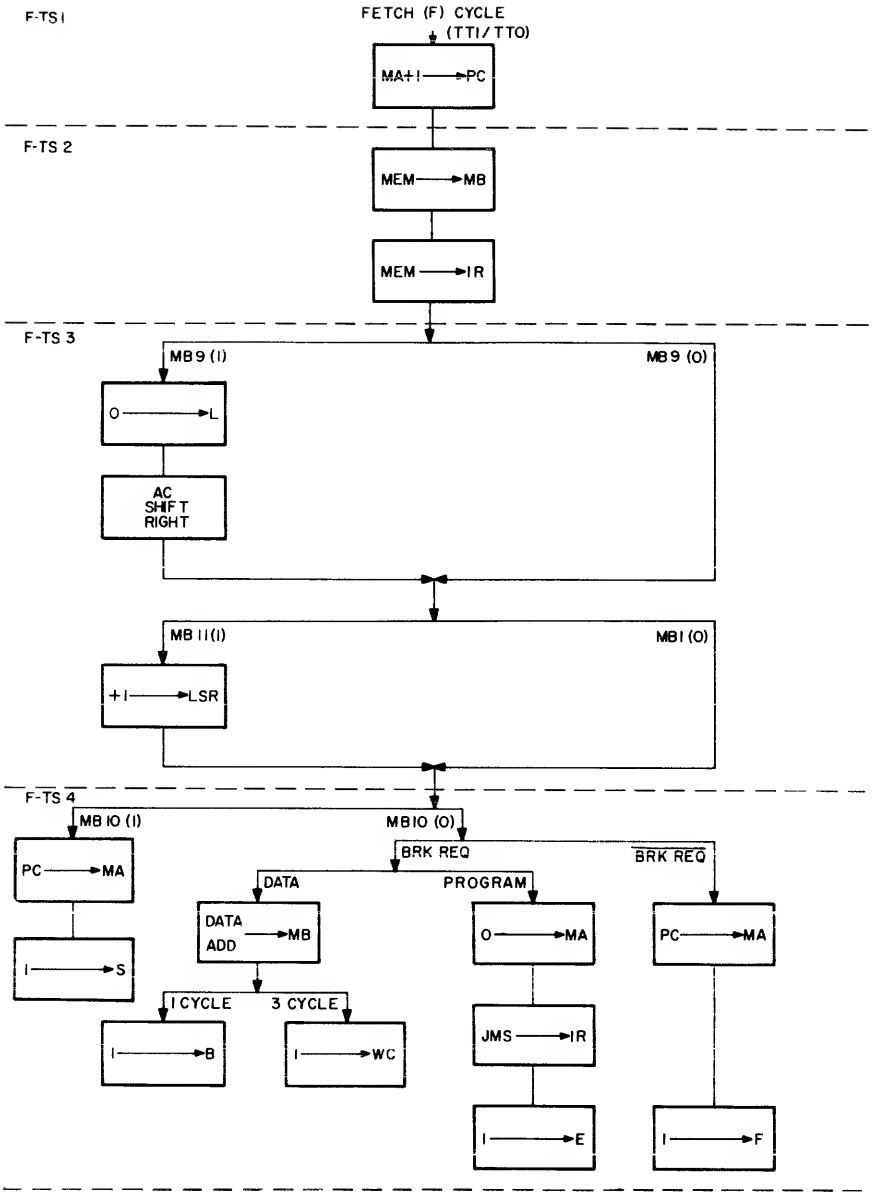


Figure 4-1 DL8I Flow Diagram (Sheet 1)

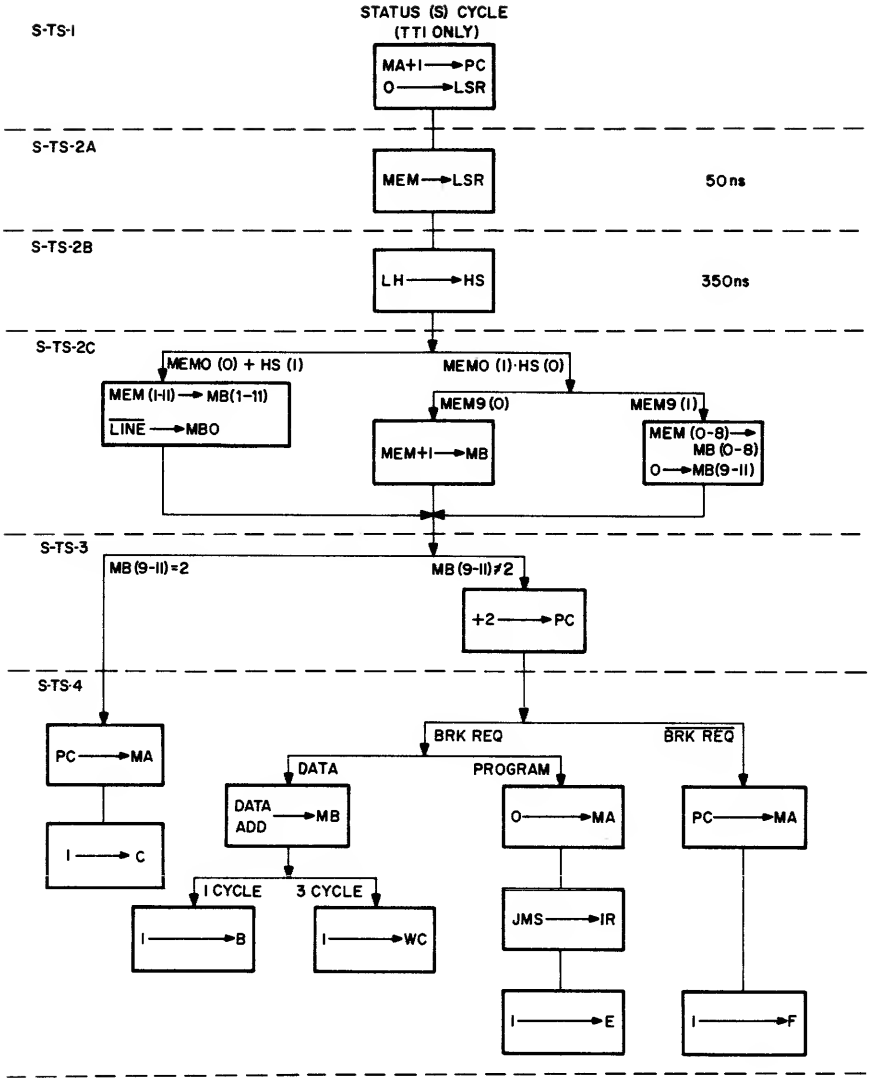


Figure 4-1 DL8I Flow Diagram (Sheet 2)

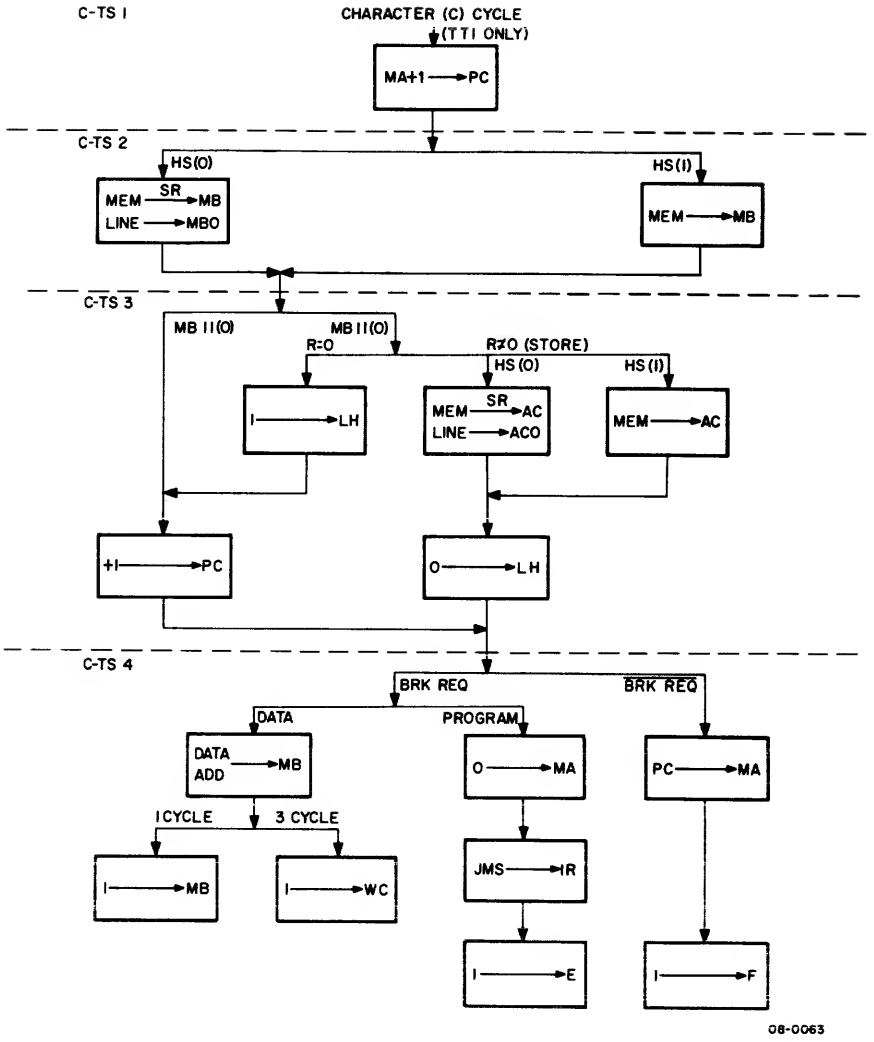


Figure 4-1 DL8I Flow Diagram (Sheet 3)

Table 4-1
PDP-8/I - DL8I - DC08A Interface Signal Reference Table

Signal Name (mnemonic)	Origin	Destination	Origin Dwg. No. & (Sheet)	Location on Dwg	Dest. Dwg No. & (Sheet)	Location on Dwg
B LINE HOLD	DL8I	DC08A	DL8I-0-2	C1	DC08-A-2(2)	C3
B C(0)	DL8I	DC08A	DL8I-0-2	C1	DC08-A-2(2)	B3
B STLR	DL8I	DC08A	DL8I-0-2	B1	DC08-A-2(2)	B3
B TP3	DL8I	DC08A	DL8I-0-2	C8	DC08-A-2(2)	B3
B MEM → LSR	DL8I	DC08A	DL8I-0-2	B8	DC08-A-2(2)	B3
B DC INST	DL8I	DC08A	DL8I-0-2	B8	DC08-A-2(2)	B3
LHS(1)	DC08A	DL8I	DC08-A-2(2)	B3	DL8I-0-2	B8
B R=Q	DC08A	DL8I	DC08-A-2(2)	B3	DL8I-0-2	B8
AC00-AC11 BUS	DC08A	PDP-8/I	DC08-A-2(2)	B,C,D6	8I-0-10	B1-B8
I/O SKIP	DC08A	PDP-8/I	DC08-A-2(2)	B6	8I-0-10	B3
INT RQST	DC08A	PDP-8/I	DC08-A-2(2)	B6	8I-0-10	B3
AC CLEAR BUS	DC08A	PDP-8/I	DC08-A-2(2)	B6	8I-0-10	B2
B RUN(0)	DC08A	PDP-8/I	DC08-A-2(2)	B6	8I-0-10	C2
LINE MUX(0)	DC08A	PDP-8/I	DC08-A-2(2)	A6	8I-0-10	B1
DATA IN 0-127	DC08A	PDP-8/I	DC08-A-1 (1,2)	Total	8I-0-10	B3-B8
B TT INST	PDP-8/I	DC08A	8I-0-10	C1	DC08-A-2(2)	B6
DATA OUT 0-127	PDP-8/I	DC08A	8I-0-10	B3-B8	DC08-A-1(1,2)	Total
B AC00-B AC11	PDP-8/I	DC08A	8I-0-10	D3-D8	DC08-A-2(1)	B,C,D7
B MB00-B MB11	PDP-8/I	DC08A	8I-0-10	C1-C8	DC08-A-2(1)	A,B,C,D4
MEM00-MEM07 & P	PDP-8/I	DC08A	8I-0-14	C4-C8	DC08-A-2(2)	C,D5
MEM08-MEM11	PDP-8/I	DC08A	8I-0-14	C1-C3	DC08-A-2(2)	D3
B IOP 1,2,4	PDP-8/I	DC08A	8I-0-10	D2,D3	DC08-A-2(1)	B7
B TS3	PDP-8/I	DC08A	8I-0-10	D2	DC08-A-2(1)	B7
B TS1	PDP-8/I	DC08A	8I-0-10	D1	DC08-A-2(1)	A7
B INITIALIZE	PDP-8/I	DC08A	8I-0-10	D1	DC08-A-2(1)	A7
MEM → LSR	PDP-8/I	DL8I	8I-0-2(2)	C5	DL8I-0-2	B8
LH → HS	PDP-8/I	DL8I	8I-0-2(2)	C4	DL8I-0-2	C1
LINE(0)	PDP-8/I	DL8I	8I-0-10	C1	DL8I-0-2	C2
MEM DONE	PDP-8/I	DL8I	8I-0-13	D1	DL8I-0-2	B1
MEM 0	PDP-8/I	DL8I	8I-0-14	C7	DL8I-0-2	B5

Table 4-1 (Cont)
PDP-8/I - DL8I - DC08A Interface Signal Reference Table

Signal Name (mnemonic)	Origin	Destination	Origin Dwg. No. & (Sheet)	Location on Dwg	Dest. Dwg No. & (Sheet)	Location on Dwg
S(1)	DL8I	PDP-8/I	DL8I-0-2	D7	8I-0-2 8I-0-13	C6 D3
S(0)	DL8I	PDP-8/I	DL8I-0-2	D8	8I-0-2 8I-0-13	C6 D3
$\overline{\text{TT SET}}$	DL8I	PDP-8/I	DL8I-0-2	D6	8I-0-3	B2
$\overline{\text{TT SET}}$	DL8I	PDP-8/I	DL8I-0-2	D6	8I-0-4	A7
$\overline{\text{TT CARRY INSERT}}$	DL8I	PDP-8/I	DL8I-0-2	B7	8I-0-4	B7
$\overline{\text{TT CARRY INSERT}}$	DL8I	PDP-8/I	DL8I-0-2	B7	8I-0-5	B3
$\overline{\text{TT CARRY INSERT}}$	DL8I	PDP-8/I	DL8I-0-2	B7	8I-0-5	D3
$\overline{\text{STORE}}$	DL8I	PDP-8/I	DL8I-0-2	B2	8I-0-4	D7
$\overline{\text{TT I/O ENABLE}}$	DL8I	PDP-8/I	DL8I-0-2	B2	8I-0-4	B6
TT CARRY INSERT	DL8I	PDP-8/I	DL8I-0-2	B3	8I-0-6	C5
$\overline{\text{MEM INH 9-11}}$	DL8I	PDP-8/I	DL8I-0-2	C4	8I-0-4	C6
TT L DISABLE	DL8I	PDP-8/I	DL8I-0-2	D3	8I-0-4	A3
$\overline{\text{C NO SHIFT}}$	DL8I	PDP-8/I	DL8I-0-2	A4	8I-0-5	D3
$\overline{\text{TT SHIFT ENABLE}}$	DL8I	PDP-8/I	DL8I-0-2	B6	8I-0-5	C2
TT SHIFT ENABLE	DL8I	PDP-8/I	DL8I-0-2	B6	8I-0-8	A8
$\overline{\text{TT INCREMENT}}$	DL8I	PDP-8/I	DL8I-0-2	D5	8I-0-5	A7
$\overline{\text{TT RIGHT SHIFT ENABLE}}$	DL8I	PDP-8/I	DL8I-0-2	D5	8I-0-5	D5
$\overline{\text{TT CYCLE}}$	DL8I	PDP-8/I	DL8I-0-2	D3	8I-0-5	A5
$\overline{\text{TT AC LOAD}}$	DL8I	PDP-8/I	DL8I-0-2	C2	8I-0-6	D7
$\overline{\text{TT INST}}$	DL8I	PDP-8/I	DL8I-0-2	D4	8I-0-2(1)	B3
$\overline{\text{TT INST}}$	DL8I	PDP-8/I	DL8I-0-2	D4	8I-0-8	A8,C8
$\overline{\text{TT INST}}$	DL8I	PDP-8/I	DL8I-0-2	D4	8I-0-10	B1
TT DATA	DL8I	PDP-8/I	DL8I-0-2	D2	8I-0-8	A8
$\overline{\text{TT LINE SHIFT}}$	DL8I	PDP-8/I	DL8I-0-2	C5	8I-0-9(1-4)	C8
TT CARRY INSERT S	DL8I	PDP-8/I	DL8I-0-2	B7	8I-0-9(4)	A5

4.2.1.2 Time State 2 (F-TS 2) - During F-TS 2, the content of the selected memory location is transferred into memory buffer (MB) register. MB bits 0, 1, and 2 are then transferred into the instruction register (IR). As in F-TS 1, this is part of a conventional F cycle and is not under control of the DL8I. Instruction decoding has not yet taken place.

4.2.1.3 Time State 3 (F-TS 3) (see Figure 4-2) - During TS 3, the contents of the instruction register are decoded. An octal 6 in the instruction register indicates an IOT instruction. This is normally a 4.25 μs slow-cycle instruction. However, when the DL8I decodes on octal 4 in MB 3 through MB 5 and an octal 0 in MB 6 through MB 8, it inhibits the $\overline{\text{SLOW CYCLE}}$ signal, and disables the conventional IOT timing train. At this point, the DL8I controls the PDP-8/I.

NOTE

The above sequence is not shown in Figure 4-1 because it takes place almost entirely under PDP-8/I control, not DL8I control. If the above conditions did not exist, i.e., 640X in MB (X can be 0 to 7), this F cycle would be changed to a conventional IOT F cycle. Therefore, all succeeding discussion presumes that 640X, or TT instruction, is in MB.

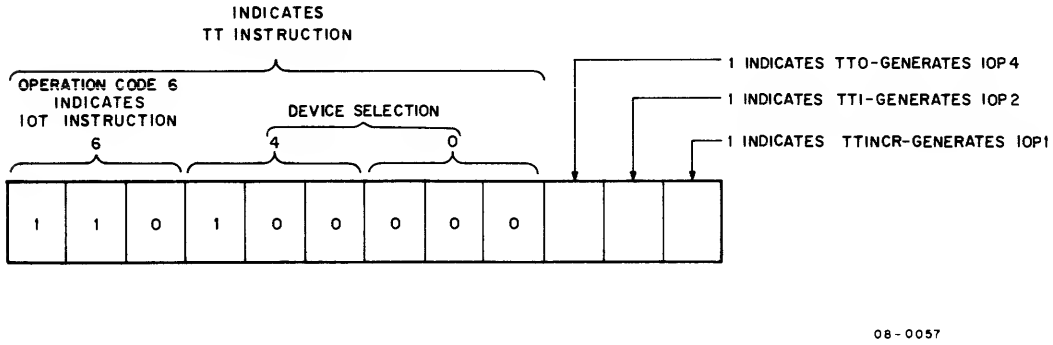


Figure 4-2 Format of TT Instruction Words in MB

During F-TS 3, the contents of MB 9 and MB 11 are decoded. If MB 9 is a 1, indicating a TTO instruction, a 0 is set into the link (L), and the content of the accumulator (AC) is shifted once to the right with 0 shifted into AC0. If MB 9 is a 0, indicating either a TTI or TTINCR instruction, the above sequence is bypassed. One bit of line data is shifted out of AC11 during a TTO instruction.

MB 11 is decoded. If MB 11 is a 1, indicating a TTINCR instruction, the line status register (LSR) is incremented. If MB 11 is a 0, indicating either a TTI or a TTO without microprogrammed TTINCR instruction, the LSR incrementation sequence is bypassed.

4.2.1.4 Time State 4 (F-TS 4) - During F-TS 4, MB 10 is decoded. If MB 10 is a 1, indicating a TTI instruction, the content of the PC register is shifted into MA, and the S flip-flop is set, thereby enabling the S cycle at the end of F-TS 4, for TP4. If MB 10 is a 0, indicating a TTI or a TTINCR instruction (or both microprogrammed), and if there is no break request, the contents of the PC register are transferred into MA, and the F flip-flop is again set; this enables another F cycle at the following TS 1. If a break is called for, the PDP-8/I determines the type of break and processes it accordingly.

4.2.2 Status Cycle (S) (see Figures 4-1 and 4-3)

The S cycle is the second phase of a TTI instruction. It utilizes the line status word (LSW) located in the memory location immediately following the TTI instruction. During the S cycle, the servicing of a particular line for input is started. The line number is indicated by bits 2 through 8 of the LSW (see Figure 4-3). Bit 0 indicates the status by association of the selected line, and bits 9 through 11 are used as a real-time clock to count the number of samples up to 2 (0---1---2) before entering the CHARACTER (C) cycle, when the data bit is sampled and the character is assembled. If the count does not equal 2, the next F cycle is entered. The clock counts up to a count of 4.

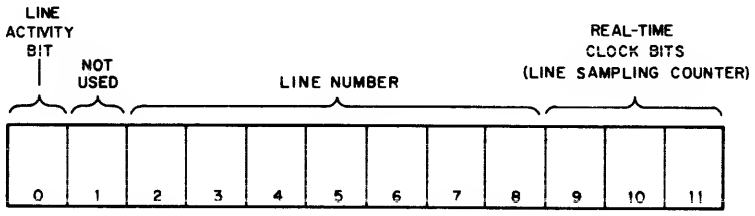


Figure 4-3 Format of Line Status Word (LSW)

4.2.2.1 Time State 1 (S-TS 1) - During S-TS 1, the content of MA is incremented and transferred into the PC register. The LSR is then cleared to allow insertion of the new LSW.

4.2.2.2 Time State 2 (S-TS 2) - S-TS 2 is subdivided into three substates, S-TS 2A, 2B and 2C. During the first substate (S-TS 2A), the appropriate bits of the LSW are transferred into the LSR in the DC08A by MEM→LSR pulse. During S-TS 2B the status of the line hold (LH) flip-flop, associated with the selected line, is transferred into the hold sync (HS) flip-flop (LH → HS). When the HS flip-flop is set, the character assembly word (CAW) contains a complete character which has not yet been processed because the program allows only a certain number of characters to be processed on each service cycle (see Paragraph 4.4.5.2).

During substate S-TS 2C, bit 0 of the LSW is decoded with the HS flip-flop as follows:

a. MEM 0 (0) + HS (1)

If bit 0 of the LSW equals zero (indicating that the line was not active during the last service cycle) or the HS flip-flop is set (indicating a completed but as yet unstored character in the CAW), then bits 1 through 11 of the LSW are transferred into bits 1 through 11 of the MB register. The complement of the signal on the input line is transferred into bit 0 of the MB (a 0 sets the activity bit). A conventional start bit is a zero; therefore, its complement is a one. All of the above is done to indicate a newly active line and also to bypass the real-time clock after a character has been assembled but not stored.

b. MEM 0 (1) · HS (0)

If bit 0 of the LSW equals one (indicating that the line was active during at least the last service cycle) and the HS flip-flop is reset (indicating that there is neither a completed character nor a stored completed character yet in the CAW), then the following takes place: if bit 9 of the LSW equals zero, indicating that the real-time clock has not yet reached a count of 4, the content of the LSW is incremented and transferred into the MB register. This, in effect, is adding one to the value of the real-time clock. If, however, bit 9 of the LSW equals one, indicating the real-time clock has reached a count of 5, then bits 0 through 8 of the LSW are transferred into bits 0 through 8 of the MB register, and a zero is transferred into bits 9, 10, and 11 of the MB register, resetting the real-time clock to zero.

4.2.2.3 Time State 3 (S-TS 3) - During S-TS 3, the value of bits 9 through 11 of MB are examined. If this value is equal to 2, indicating the time is correct to sample the line, S-TS 4 is entered. This leads to the CHARACTER (C) cycle. If, however, the value is not equal to 2, the program counter is incremented twice, and TS 4 is entered. The program counter is incremented twice to skip the next two instructions (i.e., skip the C cycle and the following instruction).

4.2.2.4 Time State 4 (S-TS 4)

a. MB (9-11) = 2

When TS 4 is entered along this route, the content of the PC register is transferred to the MA register. Then, the CHARACTER (C) flip-flop is set, enabling the C cycle during the next TS 1.

b. MB (9-11) $\neq$ 2

When S-TS 4 is entered along this route, the PDP-8/I Computer checks for data breaks. If there is no break request, the count of the PC register is transferred into the MA register, and the F flip-flop is set, thereby enabling another F cycle at the following TS 1. If a break is called for, the PDP-8/I program determines the type of break and processes it accordingly.

4.2.3 Character Cycle (see Figure 4-1)

The C cycle is the last cycle of the TTI instruction. Associated with the C cycle is a character assembly word (CAW). The software initializes one of the leftmost bit positions of the CAW (the actual position depends on character length). Received line data bits are shifted in from the left, one bit at a time, until the character is complete. Completion is determined by the appearance of the initialization bit at position 11 of the CAW. Between C cycles, the CAW is returned to memory for storage.

4.2.3.1 Time State 1 (C-TS 1) - During C-TS 1, the content of the MA register is incremented and transferred into the PC register.

4.2.3.2 Time State 2 (C-TS 2) - During C-TS 2, the status of the line HS flip-flop is examined. If HS = 0, indicating that the CAW does not contain a character completed during the last pass, the CAW is shifted one place to the right and transferred to the MB register, and the content of the incoming line is strobed into bit 0 of the MB. If the HS = 1, indicating the selected CAW contains a fully assembled but unstored character, C-TS 3 is entered.

4.2.3.3 Time State 3 (C-TS 3) - During C-TS 3, decisions are made about processing of the completed CAW.

a. MB 11 = 0

If the MB register bit 11 is a 0, the PC register is incremented, resulting in the program skipping the following instruction (usually JMS which leads to the store subroutine). MB 11 (0) implies that the character in the CAW is not yet complete.

b. MB 11 = 1

If MB register bit 11 is a 1, a completed CAW is being processed and is either in the MB register or the memory sense buffer (if it has been completed and not processed, or if it has been completed during C-TS 2). The state of the line HS flip-flop indicates which of these conditions exists. A second decision is made by examining the count in the R register.

c. R = 0

This indicates that the program does not have enough time left during the current service cycle to process the completed character; as a result, the LH flip-flop associated with the particular line is set to 1, the PC register is incremented to skip the succeeding JMS (go to store subroutine) instruction, and C-TS 4 is entered.

d. $R \neq 0$

This indicates that the completed characters can be processed (i.e., the program has enough time to go to through the character storage subroutine).

One final decision remains; if the character was completed during the previous service cycle (indicated by HS = 1), the CAW is transferred to the accumulator, and the line hold flip-flop is reset. If, however, the character was completed during the present C-TS 2 (indicated by HS = 0), the CAW is shifted right and transferred to the accumulator, and the LH flip-flop is reset. The right-shift, in the one case, and the direct transfer, in the other case, ensure that both characters have the same right justification. When this action is complete, C-TS 4 is entered.

4.2.3.4 Time State 4 (C-TS 4) - When C-TS 4 is entered, the PDP-8/I first checks for data breaks. If there is no break request, the count of the PC register is transferred into the MA register, and the F flip-flop is set, thereby enabling another F cycle at the following TS 1. If a break is necessary, the PDP-8/I decides the type of break and processes it accordingly.

4.3 DL8I DETAILED LOGIC DESCRIPTION

4.3.1 General

Detailed description of the DL8I logic is limited to the development of the control signals required by the flow diagram (refer to Paragraph 4.2). Only those areas of the flow diagram relating to DC08 operation are described. Subdivision is according to major cycles and time states within major cycles. Identification of logic elements is accomplished by using the module location code followed by the output pin number. This scheme allows common reference to both simplified logic diagrams and logic schematic DL8I-0-2. For instance, signal TTL DISABLE is generated by gate D09-S2, shown on the simplified logic diagram (see Figure 4-4) and on logic schematic DL8I-0-2 at coordinates D3. D09 is the specific module rack location; S2 is the specific pin number of the module in location D09. Continue to refer to the DL8I flow diagram, Figure 4-1, as each function is described.

4.3.2 Fetch (F) Cycle

Time states F-TS 1 and F-TS 2 are functions relating to the PDP-8/I program only. The DL8I is affected starting with F-TS 3.

4.3.2.1 Time State F-TS 3 - (see Figures 4-4 and D-BS-DL8I-0-2)

a. 640X Decoding

During TS 3, three special TT instructions, TTI (6402), TTO (6404), and TTINCR (6401), are decoded. Signal IOT is a decoded octal 6 in MB 0, MB 1, and MB 2 on D-BS-8I-0-3. TT INST is used to disable the normal IOT timing chain and inhibit a slow cycle, as shown on D-BS-8I-0-2 (Sheet 1). $\overline{\text{TT INST}}$ also causes the LINE → MB 0 transfer.

b. Link Disable

Gate D09-S2 generates TTL DISABLE which in turn disables the link by inhibiting signal L ENABLE (D-BS-8I-0-4). During all three time states, gate D09-S2 is enabled as follows:

(1) During the F cycle, TT INST is low, thereby enabling the gate.

(2) During the S cycle, the S flip-flop is set; therefore, S (0) is low, enabling the gate.

(3) During the C cycle, the C flip-flop is set; therefore, C (0) is low, enabling the gate.

NOTE

All subsequent DC08 discussion assumes that the link is disabled by TT INST.

c. MB 9 Decoding

MB 9 is decoded by gate C11-N1 which is enabled only when MB 9 (1) is high at F-TS 3, thereby generating $\overline{\text{TT I/O ENABLE}}$, which causes I/O ENABLE (D-BS-8I-0-4) and then AC ENABLE to allow AC loading or right shift.

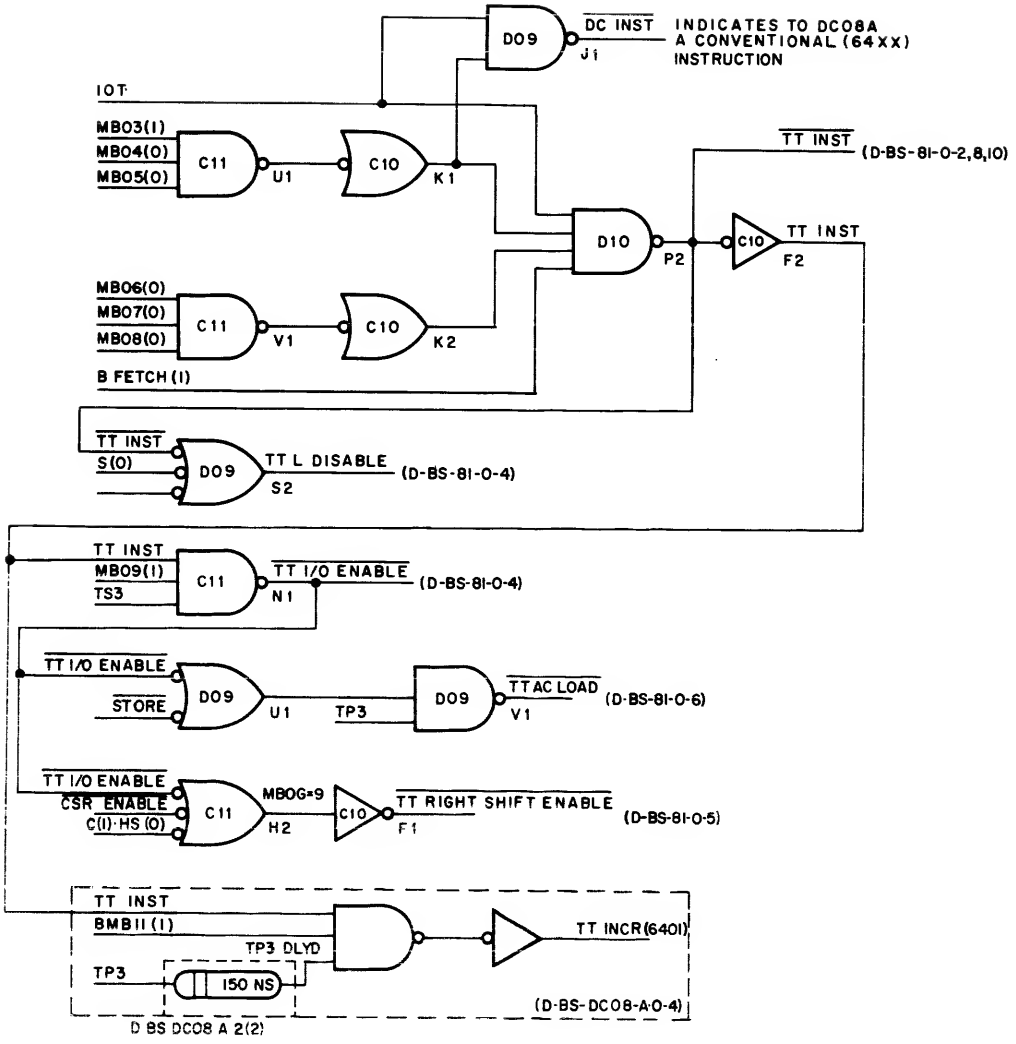


Figure 4-4 Simplified Logic Diagram, F State, TS 3

d. Right Shift

$\overline{\text{TT I/O ENABLE}}$ (used only for a TTO instruction) and TT RIGHT SHIFT ENABLE (D-BS-8I-0-5) set the PDP-8/I major register gating network for an accumulator internal right shift. The shift occurs at TP 3 when gate D09-V1 generates TTAC LOAD. In the case of a TTO instruction, the F flip-flop for the selected line (D-BS-DC08-A-1) is loaded with data at the beginning of F-TS 3. In the case of TTINCR, the incrementing of LSR occurs at TP 3 delayed (150 ns). Thus, for microprogrammed TTO and TTINCR (6405), TTI occurs before TTINCR.

e. MB 11 Decoding

MB 11 = 1 is decoded by a gate in the DC08A to produce TTINCR 150 ns after TP 3; TTINCR increments the LSR by one count to select the next successive line.

4.3.2.2 Time State F-TS 4 (see Figure 4-5)

a. TTINCR, TTI, TTO Decoding

MB 10 is decoded by gate D10-E1 which is enabled by MB 10 = 1 and TTINST. The output at gate D10-E1 is S SET, which sets the status (S) flip-flop at TP4.

b. TT SET

The $\overline{\text{S SET}}$ output is inverted to become TT SET. TT SET causes PC → MA transfer and disables normal return to the F Cycle (D-BS-8I-0-3).

c. The status (S) cycle is entered next.

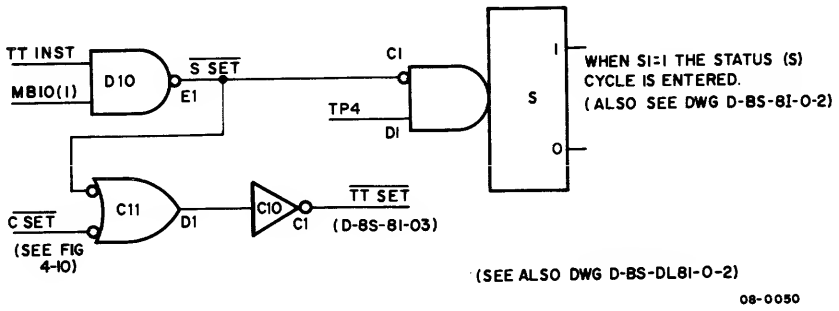


Figure 4-5 Simplified Logic Diagram, F-TS 4

4.3.3 Status (S) Cycle

During the S cycle, the line status word (LSW) is examined to determine if a character cycle is to be entered.

4.3.3.1 Time State S-TS 1 (see Figure 4-6)

NOTE

Time state S-TS 1 is applicable to the character cycle. Thus, the functions of Figure 4-6 apply to both S-TS 1 and C-TS 1 (except for STLR).

a. TTL DISABLE

Gate D-09-S2 is activated by S = 0 to produce TTL DISABLE.

b. TT CYCLE

TTL DISABLE activates gate C10-N1 to generate TT CYCLE. This signal increments the MA register by generating PC INCREMENT at TS1 (D-BS-8I-0-3) and, at TP 1, causes MA → PC transfer.

c. STLR

STLR is generated by S = 1 after MEM DONE ends to clear the line status register (LSR). $\overline{\text{MEM DONE}}$ prevents a premature STLR pulse at the end of a memory cycle (D-BS-DL8I-0-2).

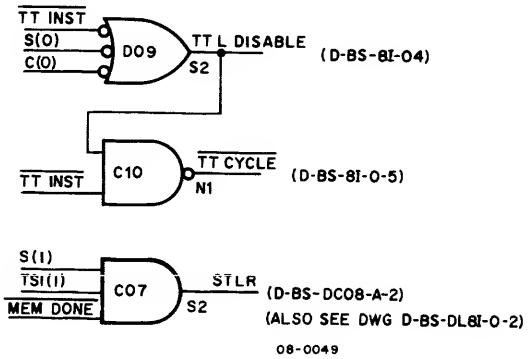


Figure 4-6 Simplified Logic Diagram, S and C States, S-TS 1 and C-TS 1

4.3.3.2 Time State S-TS 2 - S-TS 2 is subdivided into three substates called S-TS 2A, 2B, and 2C.

a. S-TS 2A (see Figure 4-7)

$\overline{\text{MEM} \rightarrow \text{LSR}}$ - Signal S = 1 at TP 1 activates gates in the PDP-8/I (D-BS-8I-0-13) to generate the $\overline{\text{MEM LSR}}$ transfer pulse. The contents of MEM 2 through MEM 8 (the LSW) are strobed through the input gating circuits to the line selection register (LSR) in the DC08A.

b. S-TS 2B (see Figure 4-7)

LH → HS - The state of the line hold (LH) flip-flop of the selected line is transferred to the hold status (HS) flip-flop in the DL8I approximately 400 ns after the status transfer. The output of HS is used to initiate decoding of the LSW.

c. S-TS 2C (see Figure 4-8)

(1) $\overline{\text{TT LINE SHIFT}}$ - This signal is generated in gate C11-M2 by the presence of MEM0 = 0 or HS = 1. The signal causes the MEM 1-11 → MB 1-11 transfer in the PDP-8/I (D-BS-8I-0-9) and gates the line value into MB 0 (LINE → MB 0). This is the new data bit from the selected line. $\overline{\text{TT LINE SHIFT}}$ completes one path through S-TS 2. When activity is established, MEM 0 = 1 and no further line shift is made in successive passes.

(2) $\overline{\text{MEM INH 9-11}}$ - the alternative path through time state S-TS 2C occurs for the term MEM0 (1) · HS (0) from inverter C09-F1. Gates C09-K2 and D10-L1 detect the value of MEM 9. If MEM 9 is active, gate D09-N1 and inverter C09-N1 produce an output that satisfies gate C09-K2. The resulting $\overline{\text{MEM INH 9-11}}$ output of C09-K2 allows transfer of only MEM 1-8 and sets all zeroes in MB 9-11 (D-BS-8I-0-4). MB 9-11 is the real-time clock which, in this case, is set at zero count.

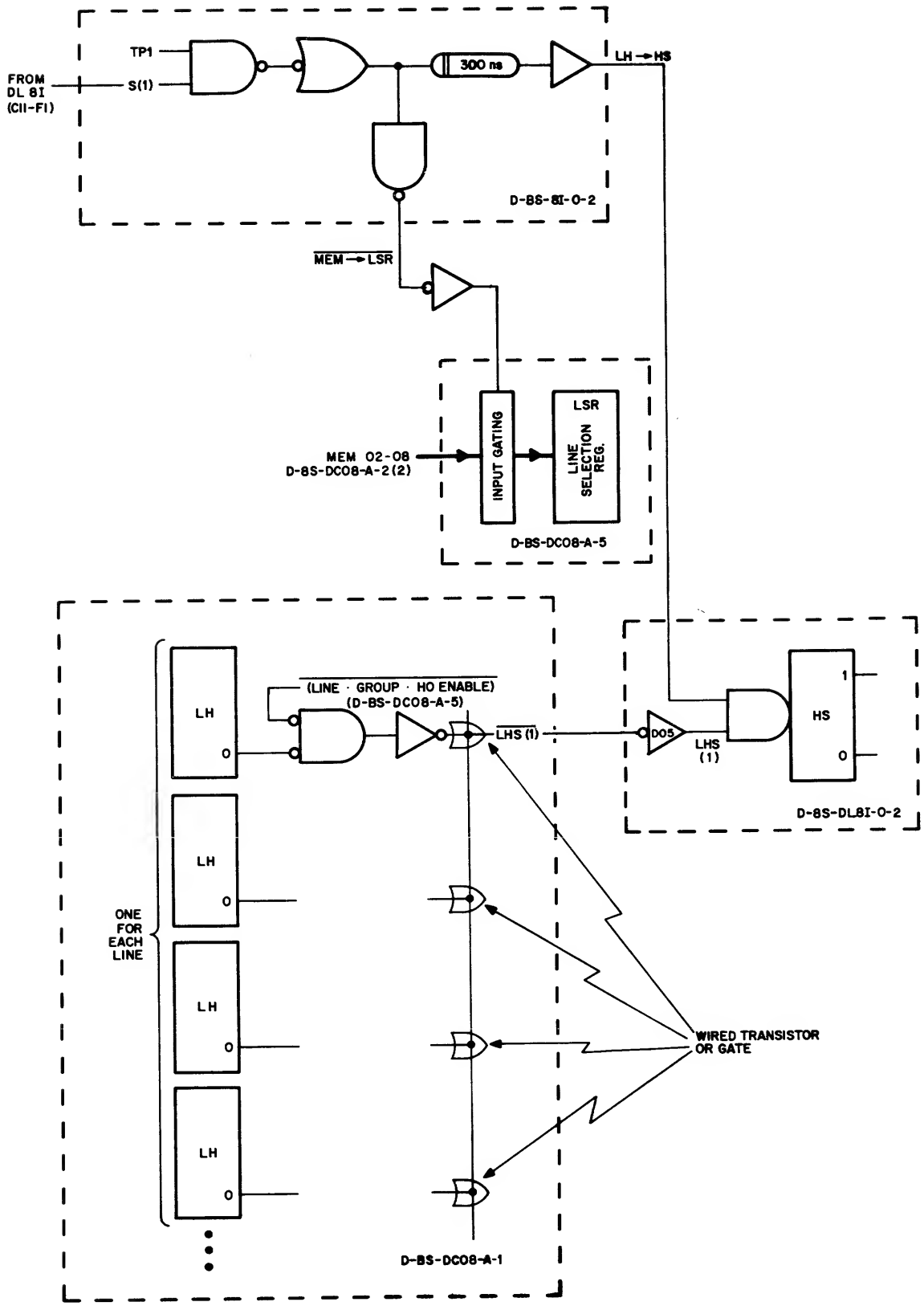


Figure 4-7 Simplified Logic Diagram S-TS 2A and 2B

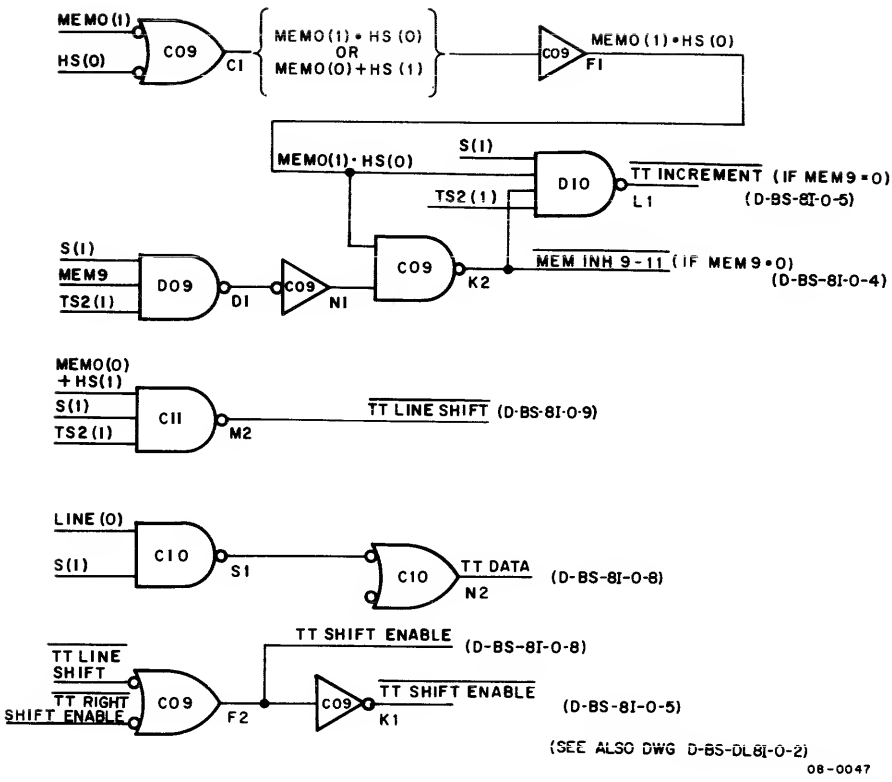


Figure 4-8 Simplified Logic Diagram, S State, TS 2C

4.3.3.3 Time State S-TS 3 (see Figure 4-9) - Time state S-TS 3 is used to examine the count of the real-time clock to determine if the character (C) cycle is to be entered.

a. $\overline{\text{C SET}}$

Gate D 10-J2 generates $\overline{\text{C SET}}$ when MB 10 = 1 and MB 11 = 0 are coincident (real-time-clock count equals two). $\overline{\text{C SET}}$ indicates that the clock count of the LSW is to the count at which the line data should be sampled. This allows an immediate passage to time state S-TS 4.

b. $\overline{\text{TT CARRY INSERT S}}$

If the real-time clock count does not equal two, gate C11-S2 is enabled, and the $\overline{\text{TT CARRY INSERT S}}$ signals are generated as shown. These signals cause the PC to be incremented by two counts (D-BS-8I-0-9, Sheet 4), and the next two instructions are skipped.

4.3.3.4 Time State S-TS 4 (see Figure 4-10) - During time state S-TS 4, the signals are generated to enable entry into the character (C) cycle or return to the next fetch (F) cycle.

a. $\overline{\text{TT SET}}$

The $\overline{\text{C SET}}$ output of gate D10-J2 also activates gate C11-D1 and enables the input to the C flip-flop. Gate C11-D1 and inverter C10-C1 develop $\overline{\text{TT SET}}$ in the same manner as described in Paragraph 4.3.2.2.b. $\overline{\text{TT SET}}$ disables normal return to the fetch cycle. At TP 4, the C flip-flop is set and the character cycle is entered.

b. If $\overline{\text{C SET}}$ does not occur during S-TS 3, $\overline{\text{TT SET}}$ and its results are inhibited. The PC + 2 count is entered in MA (PC → MA), and the next fetch (F) cycle is entered.

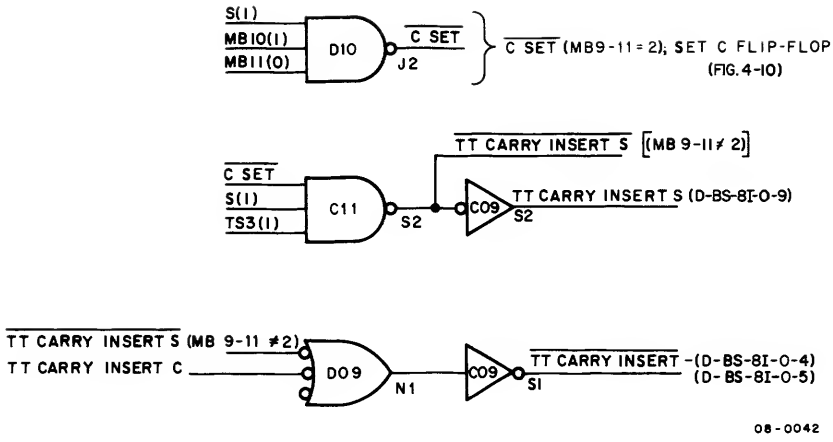


Figure 4-9 Simplified Logic Diagram, (S-TS 3)

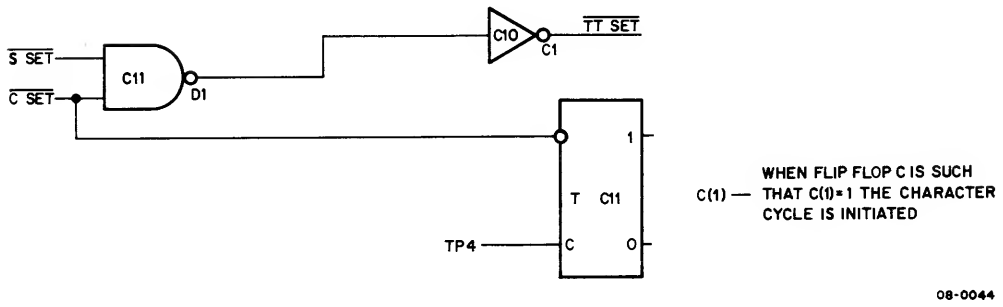


Figure 4-10 Simplified Logic Diagram, S State TS 4 (S-TS 4)

4.3.4 Character (C) Cycle

Time state C-TS 1 is the same as described for S-TS 1, Paragraph 4.3.3, except that STLR is not generated for the C cycle.

4.3.4.1 Time State C-TS 2 (see Figure 4-11 and Drawing D-BS-8I-0-5)

a. HS = 0 Decoding

If HS = 0 (HS flip-flop cleared) during C-TS 2, gates C11-J1, C11-H2 and C09-F2 combine to generate the signals required to right-shift the MEM register and effect a MEM → MB transfer. This action drops bit 11 and vacates the bit 0 position. Inverter C10-V2 and gates C10-S2 and C10-N2 load the line data bit into MB 0. Thus, MB contains the incoming character data including the most recent data bit.

b. HS = 1 Decoding

If HS = 1 (HS flip-flop is set) during C-TS 2, the right-shift of MEM is inhibited, and a simple MEM → MB transfer is done.

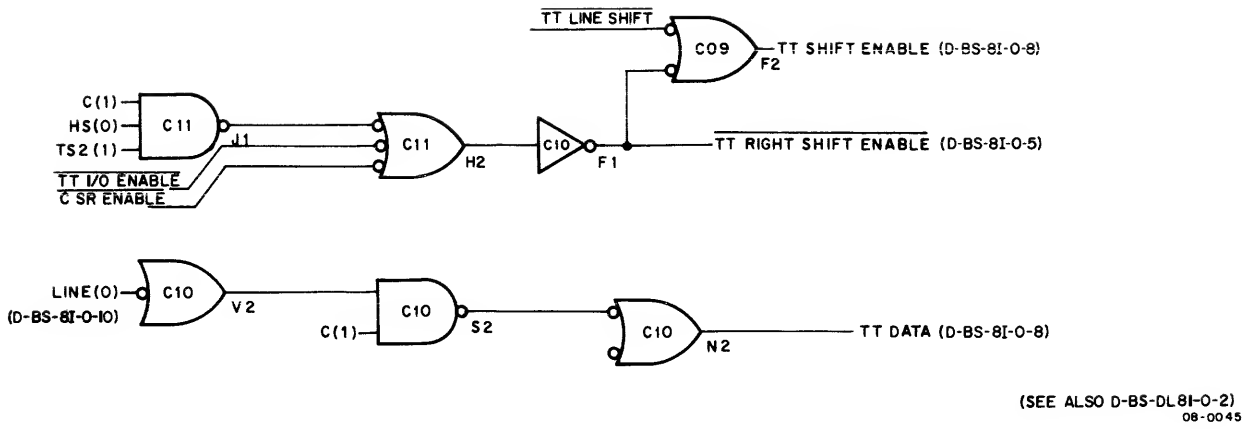


Figure 4-11 Simplified Logic Diagram, C State, TS 2 (C-TS 2)

4.3.4.2 Time State C-TS 3 (see Figure 4-12) - During C-TS 3, the CAW is examined to determine if a complete character is contained in the MB register. If a complete character is present, the R register is checked to determine if the character can be processed.

a. MB 11 = 0

If character assembly is incomplete (MB 11 = 0), gates D09-H2 and D09-N1 are activated, and the TT CARRY INSERT signals are generated. This results in incrementation of the PC (+1 → PC) and advancement to time state C-TS 4 (D-BS-8I-0-4,5,6).

b. MB 11 = 1

If character assembly is complete, MB 11 = 1 enables gates D10-S1 and D10-V2, one of which is activated depending on the state of the R register as follows:

(1) R = 0 generates $\overline{\text{LINE HOLD}}$, which sets the LH flip-flop for the particular line in the DC08A, and processing must wait. In this case, the PC is incremented and C-TS 3 is ended.

(2) R ≠ 0 generates $\overline{\text{STORE}}$. $\overline{\text{STORE}}$ generates TT AC LOAD (D-BS-DL8I-0-2) and MEM ENABLE (D-BS-8I-0-4). TT AC LOAD causes MEM → AC transfer (D-BS-8I-0-6). The condition of flip-flop HS determines if a right-shift of MEM is done prior to the transfer. STORE also generates $\overline{\text{C NO SHIFT}}$ and $\overline{\text{C SR ENABLE}}$. $\overline{\text{C NO SHIFT}}$ causes NO SHIFT signal for straight MEM → AC (D-BS-8I-0-5). $\overline{\text{C SR ENABLE}}$ causes $\overline{\text{TT SHIFT ENABLE}}$ which inhibits NO SHIFT to allow a right shift in MEM and also allows the transfer of line status to MB 0.

4.3.4.3 Time State C-TS 4 - Time state C-TS 4 is the same as time state S-TS 4, Paragraph 4.3.3.4, except that the next fetch (F) cycle is always enabled.

4.4 DC08A DETAILED LOGIC DESCRIPTION

4.4.1 General

Logic description of the DC08A Serial Line Multiplexer consists of a brief examination of the DC08A block diagram, followed by a description of the four groups of DC08A circuits. During the descriptive paragraphs, keep in mind that there is always one line control circuit (1/2 M750) for each data line, up to a total of 128 individual such circuits (or 64 M750 modules).

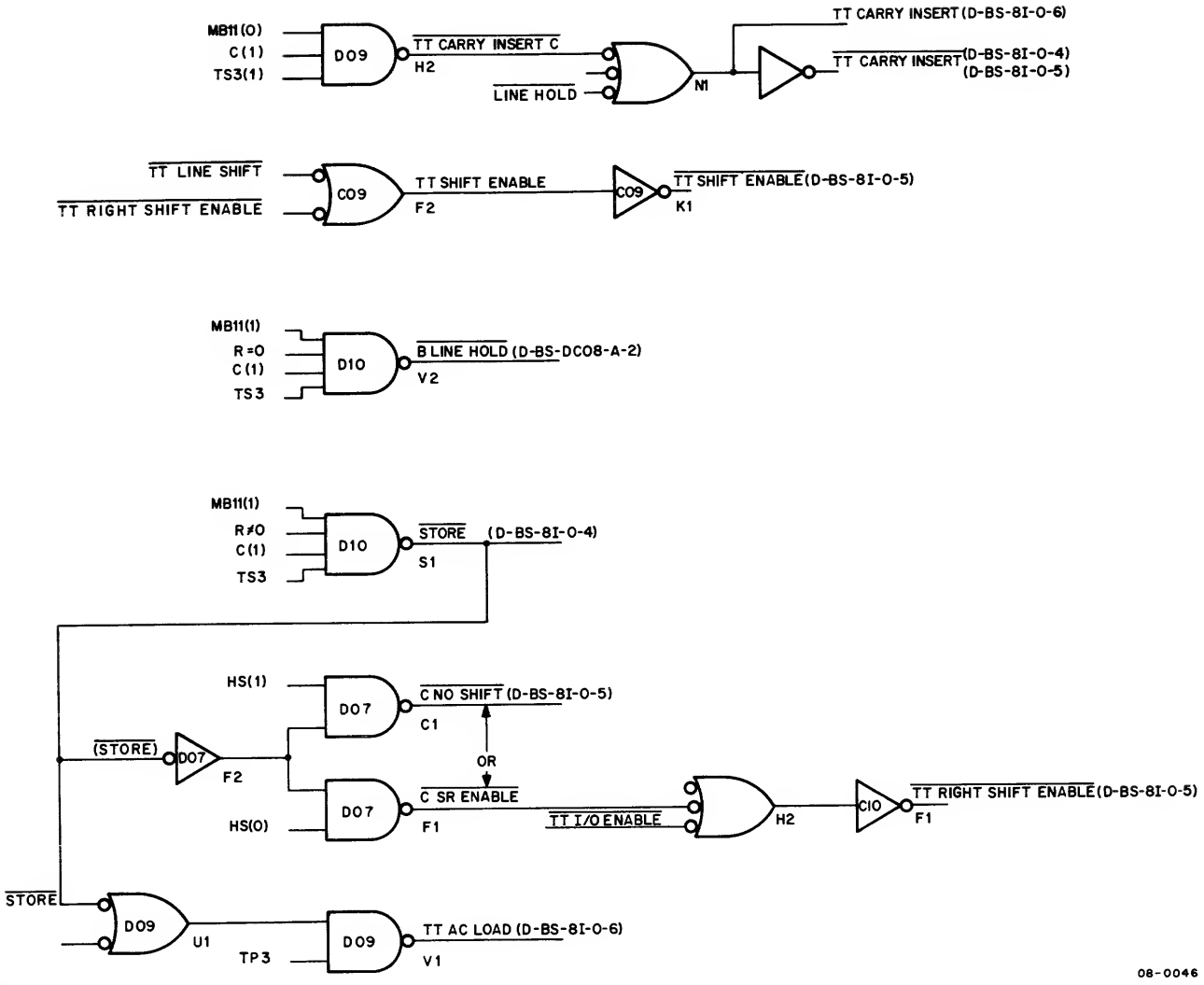


Figure 4-12 Simplified Logic Diagram, C State, TS 3

4.4.2 Block Diagram Description (see Figure 4-13)

The DC08A consists of four functional circuit groups:

a. Line register and control
b. Clock skip and interrupt
c. Instruction decoder
d. Line control (one for each line); the line control has three types of inputs and outputs:
   (1) Multiplexed inputs and outputs
   (2) Line select inputs
   (3) Individual data line inputs and outputs

The multiplexed inputs and outputs appear at each line control, but only one line control is selected at any given time by the line register (LINE SELECT). Therefore, at any given time, only one line control is being used. Individual DATA OUT and DATA IN lines appear at the line side of each line control module. Thus, the major function of the DC08A is to connect the selected line to the PDP-8/I. The M751 line register and control module (D-BS-DC08-A-5) decode the PDP-8/I line number outputs and generate a LINE SELECT grouping of signals comprising:

a. $\overline{H0}$ for lines from 0 - 63
   H0 for lines from 64 - 127.
b. GROUP is broken down as follows:

   0 - 7 and 64 - 71
   8 - 15 and 72 - 79
   16 - 23 and 80 - 87
   24 - 31 and 88 - 95
   32 - 39 and 96 - 103
   40 - 47 and 104 - 111
   48 - 55 and 112 - 119
   56 - 63 and 120 - 127

c. LINE n where n varies from 0 - 7

These signals, called LINE SELECT, can address up to 128 lines. The instruction decoder consists of a decoding matrix that interprets all TT instructions for internal use. The clock skip and interrupt circuits provide a maximum of four different clock interrupt rates (one (110-baud) is included in the basic DC08A; the other three are optional).

4.4.3 Line Control Module M750 (Figure 4-14 and D-BS-DC08-A-1)

The line control circuits interface each data line to the DC08. There is one line control circuit for each line, and two on each M750 module. Because the PDP-8/I operates several orders of magnitude faster than any of the

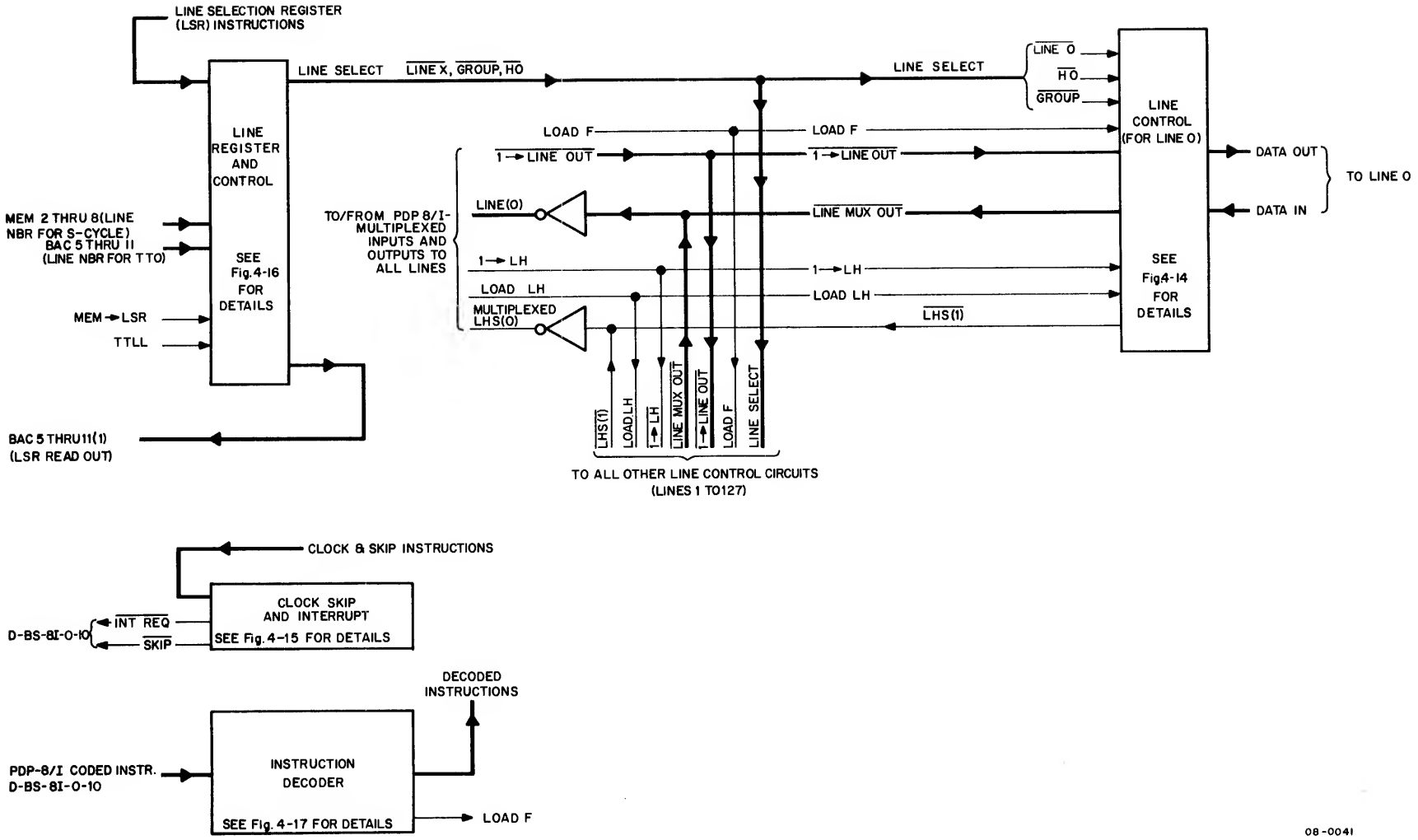


Figure 4-13 DC08A Simplified Block Diagram

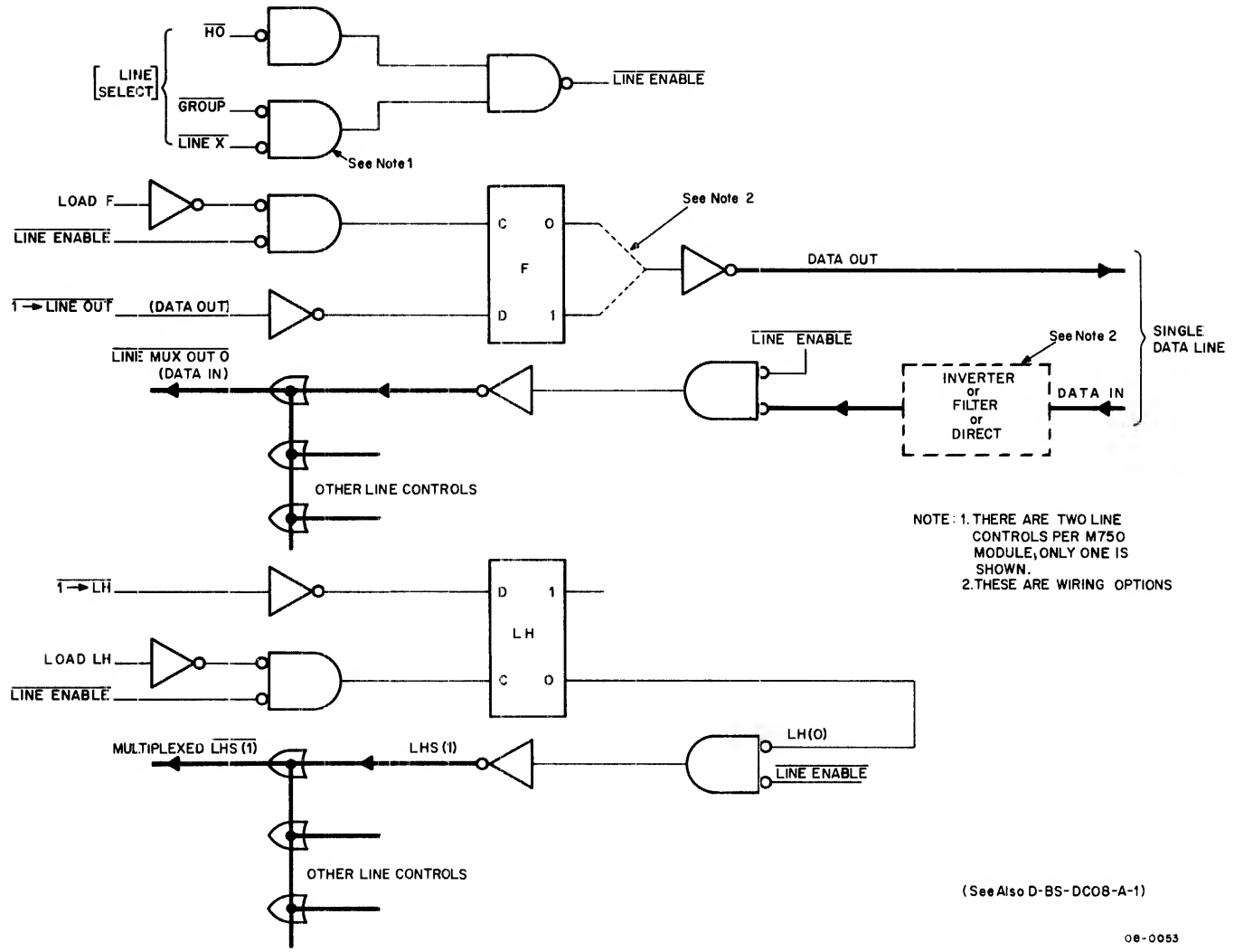


Figure 4-14 Line Control Logic Diagram

data lines that it is coupled to, it is necessary to store output data; the F flip-flop provides short-term output data storage. Input data, however, is sampled from the line in real-time. The LH flip-flop provides short-term line history, as described in DL8I flow diagram theory.

4.4.3.1 Line Selection - Gates 3 and 4 combine the LINE SELECT signals to form an internal $\overline{\text{LINE ENABLE}}$ signal. $\overline{\text{LINE ENABLE}}$ enables the F and LH flip-flops and the data input gate.

4.4.3.2 F Flip-Flop - The F flip-flop provides short-term storage of output data when set by 1 → LINE OUT with LOAD F and LINE ENABLE. The output of the F flip-flop is routed through an inverter to the data line as DATA OUT.

4.4.3.3 Data Input - Input data from the data line is either inverted, filtered, or wired directly to gate 5. When gate 5 is enabled by the LINE SELECT signals, the value of the data line, appropriately processed, appears on $\overline{\text{LINE MUX OUT}}$ and is subsequently sampled in real-time by the PDP-8/I.

4.4.3.4 LH Flip-Flop - The LH flip-flop provides a short-term history of the line being serviced. The LH flip-flop is set if a character has been completely assembled, but has not been processed. The LH flip-flop is set to the state: (1 → LH) by (LOAD LH). The zero output of LH is routed through gate 8 to $\overline{\text{MULTIPLEXED LHS(1) OUT}}$.

4.4.4 Clock Skip and Interrupt Circuits (see Figure 4-15 and Drawing D-BS-DC08-A-3)

Up to four clocks of different frequencies can be included in the DC08A. The frequency of each clock should be five times the baud rate of the sampled data; therefore, five clock interrupts will occur during the sampling of each bit of data. Each clock is free running, but normally disabled by the clock flag flip-flop input gate. A TTX ON instruction sets the enable flip-flop, clears the clock flag flip-flop, and enables the clock flag flip-flop input gate. The first positive clock transition sets the clock flag flip-flop, generating a clock n flag (where n is the clock number), which is combined with the other clock flags to generate $\overline{\text{INT}}$. $\overline{\text{INT}}$ is coupled through a bus driver to become $\overline{\text{INT RQST}}$. The program detects the interrupt request and attempts to determine which clock has caused the interrupt. This is accomplished by generating skip instructions. When a skip is generated for the appropriate clock flag, its gate is enabled, generating $\overline{\text{SKIP}}$ at gate A 16-B1. $\overline{\text{SKIP}}$ informs the PDP-8/I that it has determined the clock causing the interrupt. For example, TTI ON (6424) clears the Clock Flag flip-flop and enables its input gate. The next positive transition sets the Clock 1 Flag flip-flop, generating CLOCK 1 FLAG(1). CLOCK 1 FLAG(1) is combined with the other clock flags to generate $\overline{\text{INT}}$. Assuming T4 SKIP (6451) is generated first, no $\overline{\text{SKIP}}$ signal is generated. The same logic holds true for T3 SKIP (6441) and T2 SKIP (6431). When T1 SKIP (6421) is generated, however, a gate combines T1 SKIP and CLOCK 1 FLAG (1) to generate $\overline{\text{SKIP}}$.

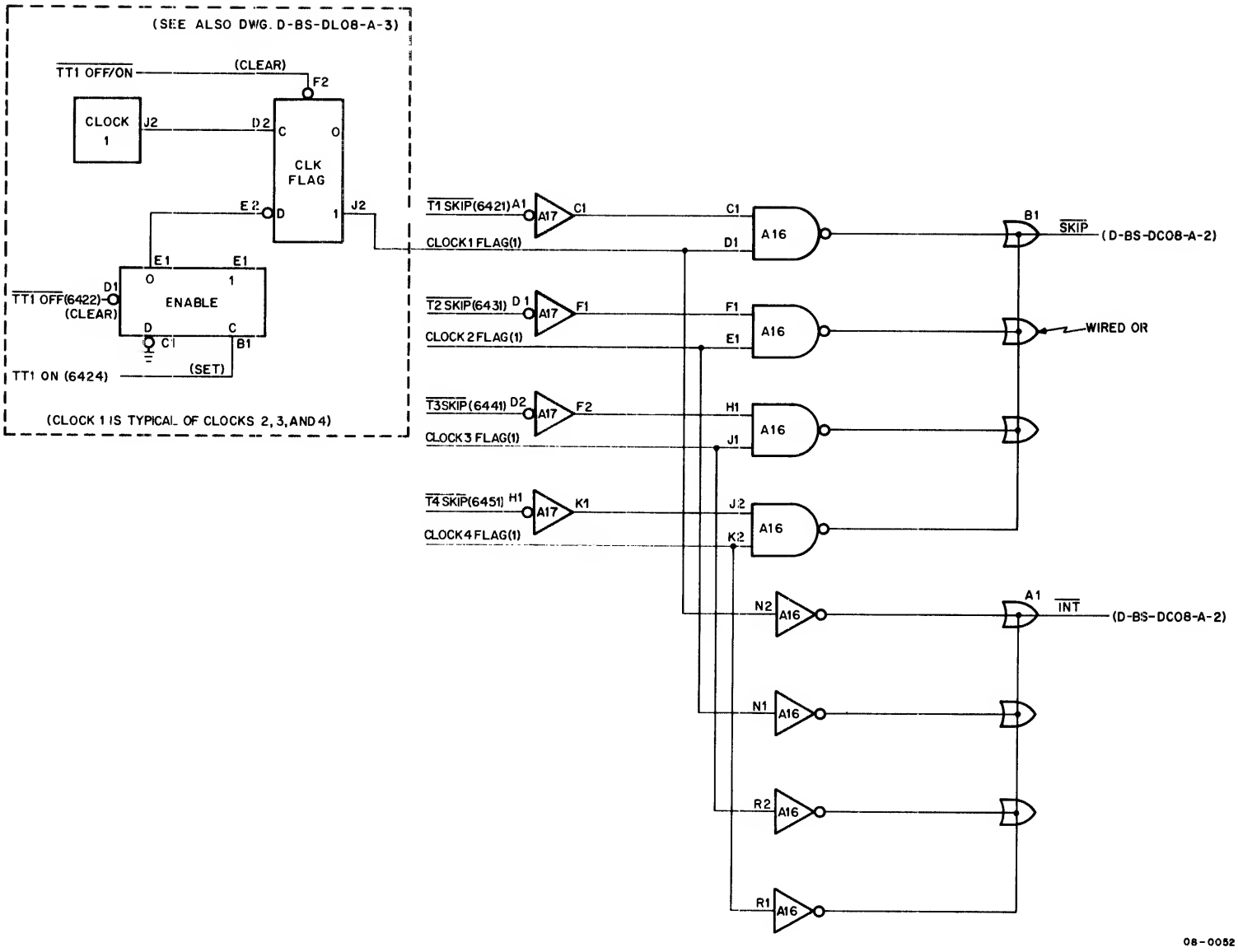


Figure 4-15 Clock, Skip and Interrupt Logic Diagram

Skip instructions are usually sequenced from 1 to 4. Similarly, clock 1 is usually the highest frequency clock, and clock 4 the lowest, with the others in sequence. Therefore, the higher frequency data lines are given priority over the slower ones.

4.4.5 Line Register and Control Theory (see Figure 4-16 and Drawing D-BS-DC08-A-5)

a. The seven-stage line register with its associated decoder.
b. The five-stage R register with its associated decoder.
c. Output gates.

4.4.5.1 Line Register LR - The seven-stage line register LR (L1, L2, L4, L8, L16, L32 and L64) can be loaded with either the contents of MEM 2 through MEM 8, or BAC 5 through BAC 11. MEM → LSR enables the series of input gates designated as BA 1, setting the LR to the value of MEM 2 through MEM 8. This is done during the status (S) cycle of the TTI instructions after STLR clears the LSR during S-TS 1 (see Figure 4-6). TTLL (6412) enables the series of input gates designated as BE 1, ORing the LR with the value of BAC 5 through BAC 11. This is done during a TTO instruction. The LR can be incremented by TTINCR (6401) (or cleared by TTCL (6411) or by STLR during S-TS 1), both of which are ORed in the instruction decoder. The outputs of the LR are decoded and form the LINE SELECT group of signals, allowing selection of any one of 128 line control circuits. The contents of LR can also be ORed into accumulator positions AC5 through AC11 by IOT instruction TTRL (6414).

4.4.5.2 R Register - The number of assembled data characters that can be processed during a service cycle is generally programmed to be from 20 to 40 percent of the total number of data lines in use. The software enters the two's complement of this value into the load distribution counter (R register) at the beginning of a service cycle. Then, each time a character is processed, a count of one is effectively added to the value remaining in the R register by TTR INCR. When the content of the register reaches zero, no further character processing can take place until the next service cycle is entered with $R \neq 0$. The R register (R1, R2, R4, R8 and R16) is loaded with the contents of BAC 7 through BAC 11 by IOT instruction TTLR (6472).

As each input data character is processed by a JMS, the program issues IOT instruction TTR INCR (6461). The R register is incremented by one count. The program can then issue IOT instruction TTRR (6464) to read the R-register count into accumulator positions AC 7 through AC 11. TTR INCR and TTRR can be microprogrammed as IOT instruction 6465. The R register can be cleared by IOT instruction TTCR (6471).

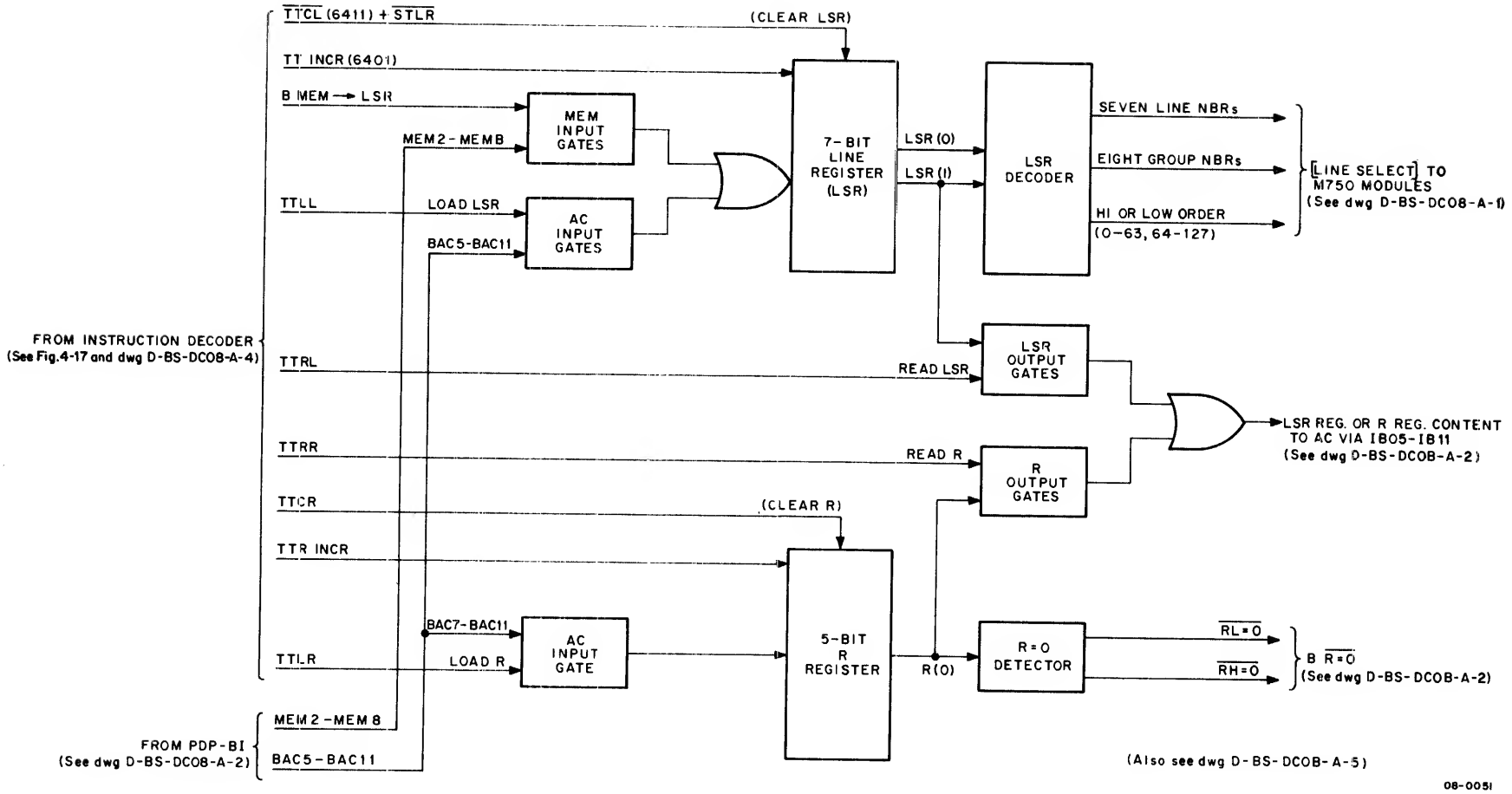


Figure 4-16 Line Register and R Register, Block Diagram

4.4.5.3 Output Gates - The output gates allow either the contents of the LR or the R register to be gated to the accumulator. TTRL (6414) ORs the contents of the line register to AC 5 through AC 11; TTRR (6464) ORs the contents of the R register to AC 7 through AC 11.

4.4.6 Instruction Decoder (see Figure 4-17 and Drawing D-BS-DC08-A-4)

The instruction decoder circuits decode all IOT instructions issued by the program except TTI (6402), TTO (6404), and TT INCR (6401). TTI and TTO are not decoded in the DC08A. TT INCR is described in Paragraph 4.4.7. Coded IOTs are applied to binary decoder gates that produce outputs of octal 1 through 7. These seven signals are applied to three decoder timing gates (1, 2, and 4).

The decoder gates are simultaneously enabled by $\overline{\text{DC INST}}$ during the IOT cycle and individually enabled by IOP1, IOP2, and IOP4. The relative timing of the IOP pulses is shown in Figure 4-17.

The decoded instruction is formed in three steps. The first two digits (64) are assumed with $\overline{\text{DC INST}}$, because the 6400 series is reserved for data communications. The third digit (1 through 7) is the discrete output of the binary decoder gates. The fourth bit is determined by which decoder timing gate is enabled by an IOP. The program controls the issuance of IOPs and can issue any combination of IOP1, IOP2, and IOP4 for the purpose of microprogramming IOT instructions. Thus, 64 is implied by $\overline{\text{DC INST}}$, and the last two digits of each instruction are a combination of the binary decoder output and the programmed timing pulses. For example, to load the R register, instruction TTLR (6472) is required. The program issues an IOT code of 64XX, which results in $\overline{\text{DC INST}}$ and BMB06, 07, 08 for a binary 7. IOP1 is skipped, and then IOP2 enables decoder timing gate 2 to produce 6472 (TTLR). If the programmer desires to increment the R register with TTR INCR (6461) and then read the R register contents back into the AC with TTRR (6464), a microprogram can be implemented as follows:

a. The IOT results in $\overline{\text{DC INST}}$, and the program issues BMB06, 07, $\overline{08}$ for a binary 6.

b. IOP1 enables decoder timing gate 1 to produce 6461 (TTR INCR), IOP2 is skipped, and then IOP4 enables decoder timing gate 4 to produce 6464 (TTRR).

Thus, two instructions are decoded during the same IOT cycle. Each pair of clock control instructions (TT1 ON and TT1 OFF, etc) is applied to an OR function such that when either clock instruction is issued, the OR function produces an output. For instance, when either $\overline{\text{TT1 OFF}}$ (6422) or TT1 ON (6424) is issued, $\overline{\text{TT1 OFF/ON}}$ results for the same duration as the instruction.

4.4.7 Line Control Gating Circuits (see Figure 4-18 and Drawing D-BS-DC08-A-4)

The line control gating circuits both develop and amplify the signals that condition the M750 modules. The control signals are applied to all M750 modules (in either low or high order) in parallel. The output of the

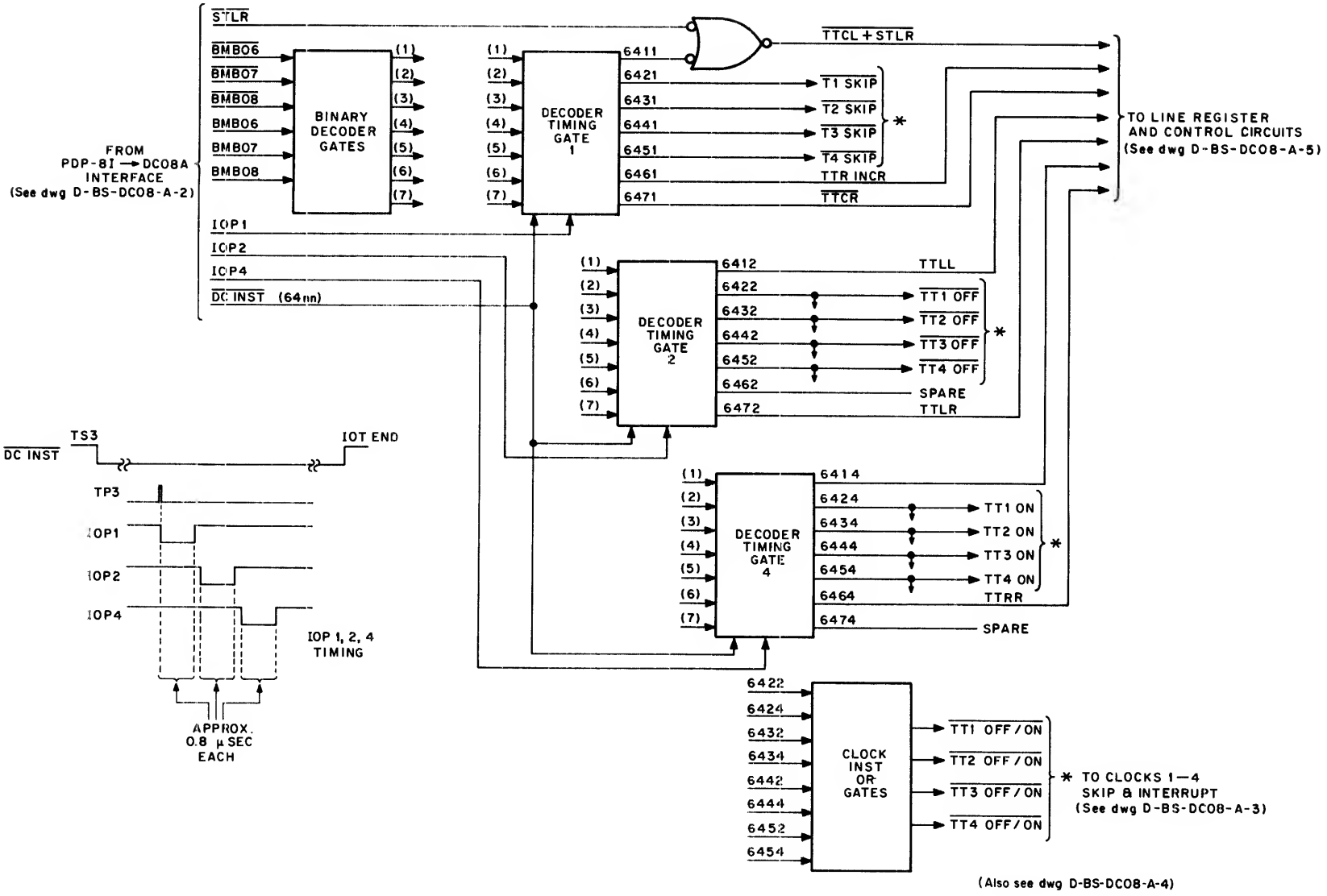


Figure 4-17 IOT Instruction Decoder, Block Diagram

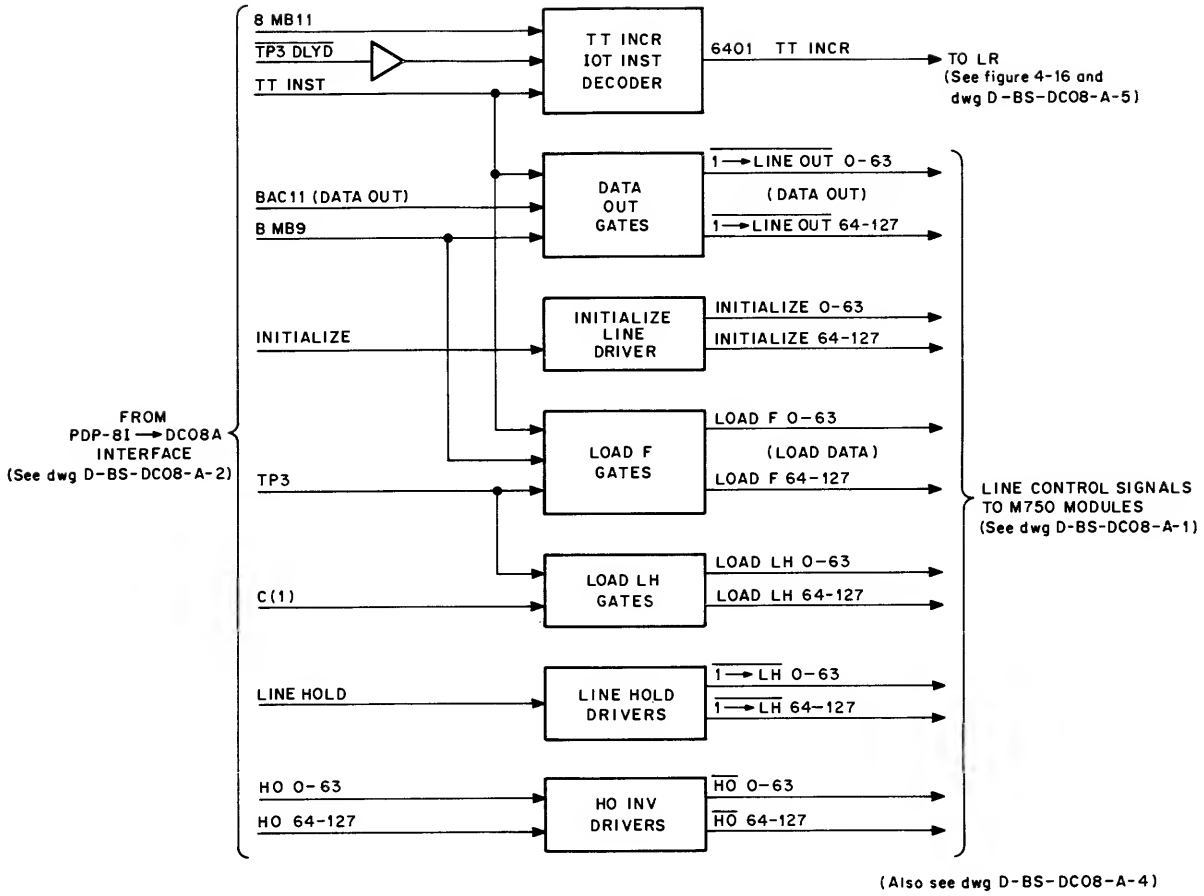


Figure 4-18 Line Control Gating Circuits, Block Diagram

line register (LR) determines which M750 module responds to the control signal. Thus, the line control gating circuit produces the control signals, and the LR output determines which M750 module is affected. The gating circuits operate as follows:

a. When outputting data to a line, TT INST enables the data out gates and the load F gates. BMB9 also enables both sets of gates. The output data on BAC 11 is applied to the M750 modules as $\overline{\text{T} \rightarrow \text{LINE OUT}}$. At TP3 the load F gates apply LOAD F to the M750 modules, and the data is set into the F flip-flop of the selected line.

b. INITIALIZE is coupled through line drivers to all M750 modules.

c. The combination of LINE HOLD and C(1) signals sets the value of the signal $\overline{\text{T} \rightarrow \text{LH}}$ flip-flop of the selected M750 module.

d. The HO 0-63 and HO 64-127 signals are outputs of the highest order flip-flop in line register (LR). These signals simply determine which half of the 128 lines are affected by all other line control gating signals.

The uppermost gate shown in Figure 4-18 generates the TT INCR (6401) instruction, the description of which was omitted in Paragraph 4.4.6 because it occurs during TT INST. If BMB 11 is a one during TS 3 of the fetch (F) cycle, TT INCR (6401) increments line register LR at TP 3 DLYD of TS 3.

CHAPTER 5

MAINTENANCE

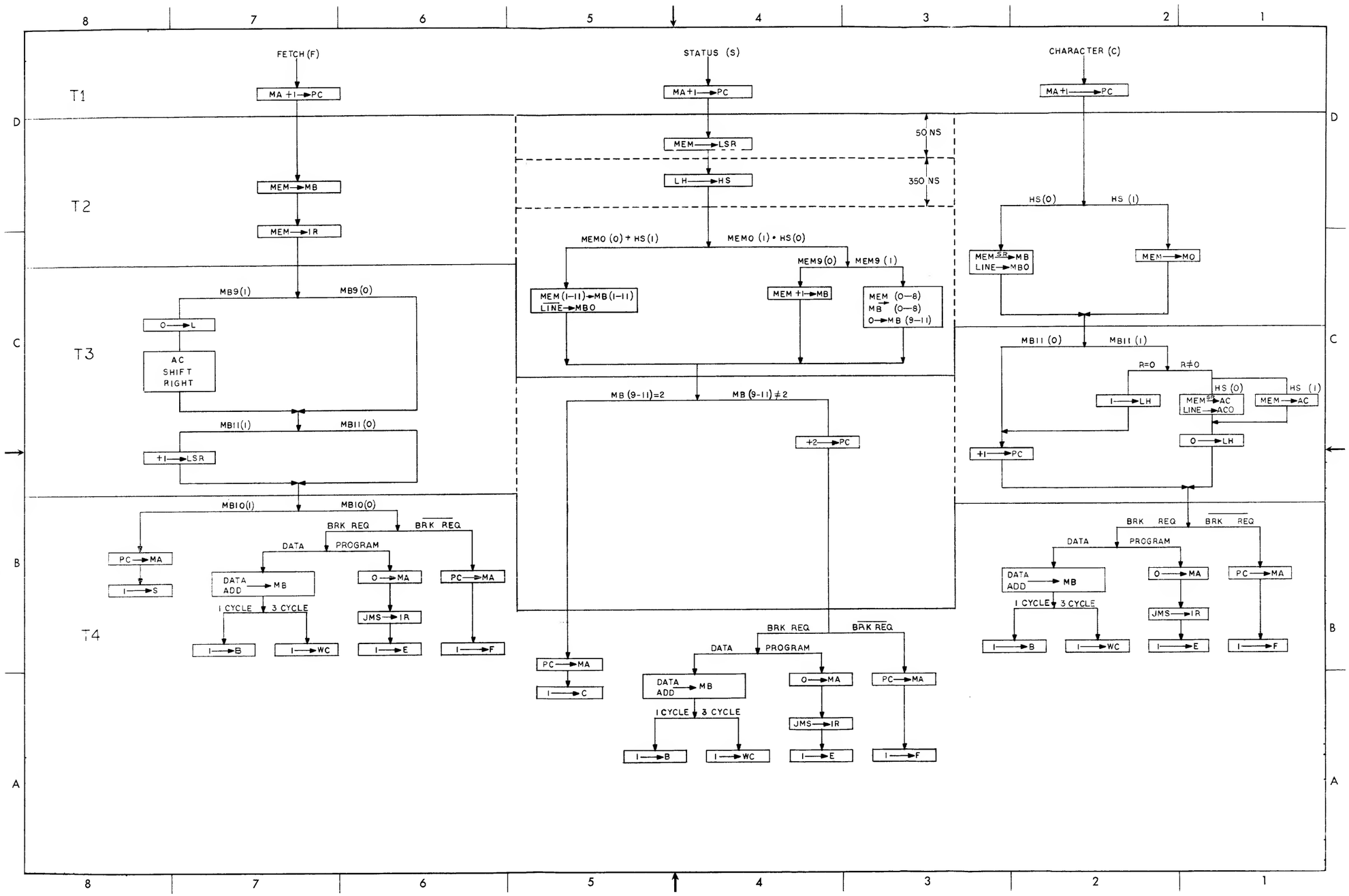
Maintenance of the DC08 Data Communications System is limited to the use of both off-and on-line diagnostic programs. Test modules are supplied with the system for use with the off-line diagnostic program. Each G724 Test Module simulates 16 input/output lines. The test modules are inserted in DC08A locations A29 through A32 and B29 through B32 in place of the operational cables. Up to eight test modules can be used, depending on the number of operational input/output lines. The diagnostic programs listed below can be obtained from the Program Library, Digital Equipment Corporation, Maynard, Massachusetts.

Appendix C Maindec 8I-D8AA - DC08T1, DC08 Off-Line IOT and Data Test

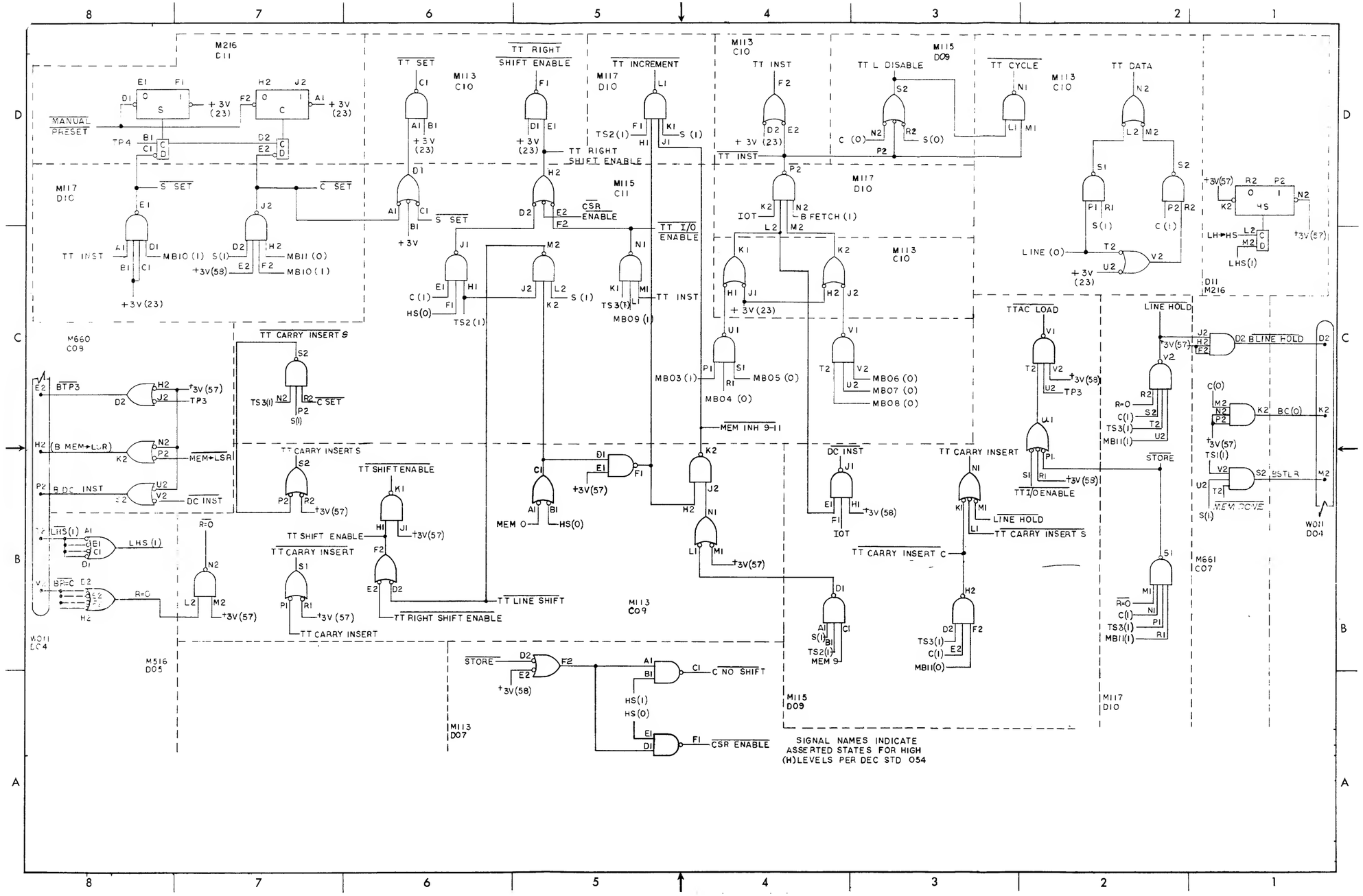
Appendix D Maindec 8I-D8BA - DC08T2, DC08 On-Line Data Exercise

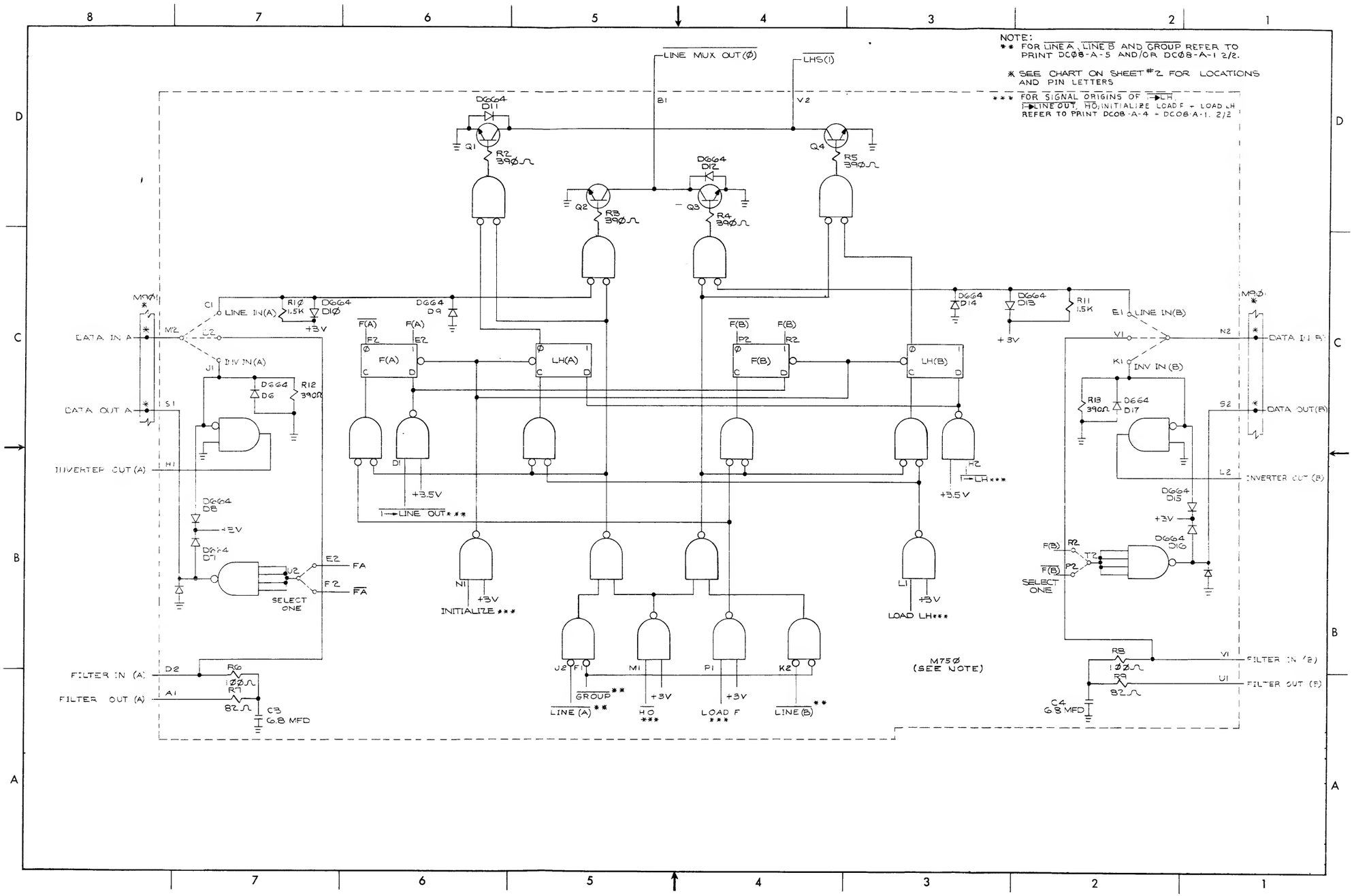
CHAPTER 6
DIAGRAMS

This chapter contains all pertinent equipment diagrams for the DL8I and the DC08A. Drawings for all DC08 options are included in the particular addendum devoted to each option. The following drawings are contained in this chapter.



D-FD-DL8I-0-1 Flow Diagram


M216 D11
MANUAL PRESET
TP4
S SET
C SET
M117 D10
TT INST
MB10 (1)
S(1)
MB11 (0)
MB10 (1)
+3V(58)
+3V (23)
M113 C10
TT SET
TT RIGHT SHIFT ENABLE
TT INCREMENT
M117 D10
TS2(1)
S (1)
TT RIGHT SHIFT ENABLE
M115 C11
CSR ENABLE
TT I/O ENABLE
C(1)
HS(0)
TS2(1)
TS3(1)
MB09 (1)
TT INST
M113 C10
TT INST
TT L DISABLE
C (0)
S(0)
TT CYCLE
M113 C10
TT DATA
LINE (0)
C(1)
LH→HS
LHS(1)
D11 M216
M660 C09
TT CARRY INSERT S
TS3(1)
S(1)
BTP3
TP3
B MEM→LUR
MEM→LSR
B DC INST
DC INST
TT CARRY INSERT S
TT SHIFT ENABLE
TT CARRY INSERT
TT RIGHT SHIFT ENABLE
TT LINE SHIFT
M113 C09
MB03 (1)
MB05 (0)
MB04 (0)
MB06 (0)
MB07 (0)
MB08 (0)
MEM INH 9-11
MEM 0
HS(0)
+3V(57)
M117 D10
IOT
B FETCH (1)
TTAC LOAD
TP3
LINE HOLD
BLINE HOLD
BC(0)
BSTLR
MEM MOVE
STORE
TT I/O ENABLE
LINE HOLD
TT CARRY INSERT S
TT CARRY INSERT C
DC INST
IOT
MEM 9
M661 C07
WD11 DO4
WD11 DC4
M516 D05
M113 D07
STORE
C NO SHIFT
CSR ENABLE
M115 D09
M117 D10
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054



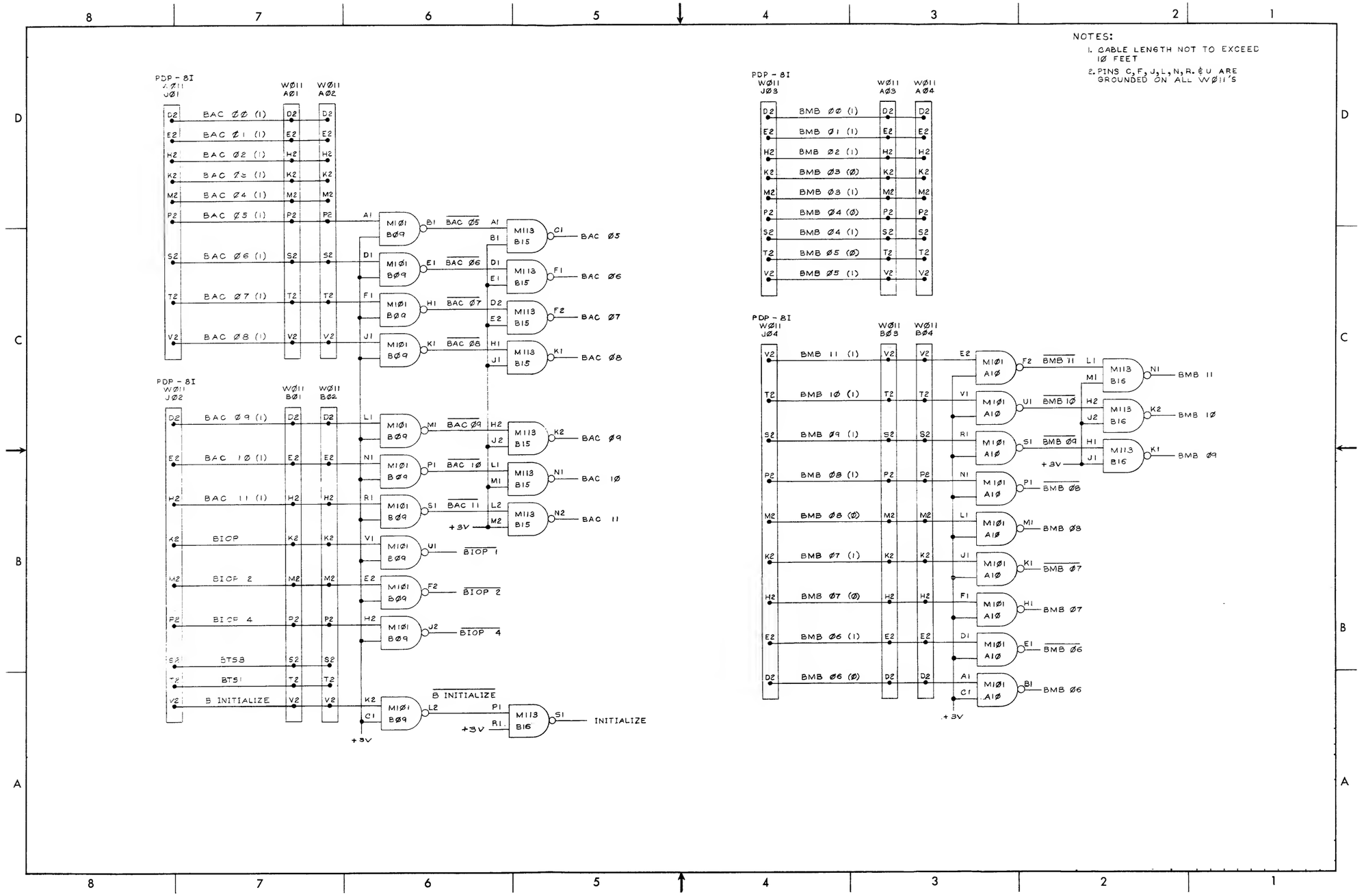
D-BS-DC08-A-1 Line I/O Control 0-127 (Sheet 1)

M750 MODULE LOCATION		
LINES (OCTAL)	LINES (DECIMAL)	LOCATION
0-1	0-1	C01
2-3	2-3	C02
4-5	4-5	C03
6-7	6-7	C04
10-11	8-9	C05
12-13	10-11	C06
14-15	12-13	C07
16-17	14-15	C08
20-21	16-17	C09
22-23	18-19	C10
24-25	20-21	C11
26-27	22-23	C12
30-31	24-25	C13
32-33	26-27	C14
34-35	28-29	C15
36-37	30-31	C16
40-41	32-33	C17
42-43	34-35	C18
44-45	36-37	C19
46-47	38-39	C20
50-51	40-41	C21
52-53	42-43	C22
54-55	44-45	C23
56-57	46-47	C24
60-61	48-49	C25
62-63	50-51	C26
64-65	52-53	C27
66-67	54-55	C28
70-71	56-57	C29
72-73	58-59	C30
74-75	60-61	C31
76-77	62-63	C32
100-101	64-65	D01
102-103	66-67	D02
104-105	68-69	D03
106-107	70-71	D04
110-111	72-73	D05
112-113	74-75	D06
114-115	76-77	D07
116-117	78-79	D08
120-121	80-81	D09
122-123	82-83	D10
124-125	84-85	D11
126-127	86-87	D12
130-131	88-89	D13
132-133	90-91	D14
134-135	92-93	D15
136-137	94-95	D16
140-141	96-97	D17
142-143	98-99	D18
144-145	100-101	D19
146-147	102-103	D20
150-151	104-105	D21
152-153	106-107	D22
154-155	108-109	D23
156-157	110-111	D24
160-161	112-113	D25
162-163	114-115	D26
164-165	116-117	D27
166-167	118-119	D28
170-171	120-121	D29
172-173	122-123	D30
174-175	124-125	D31
176-177	126-127	D32

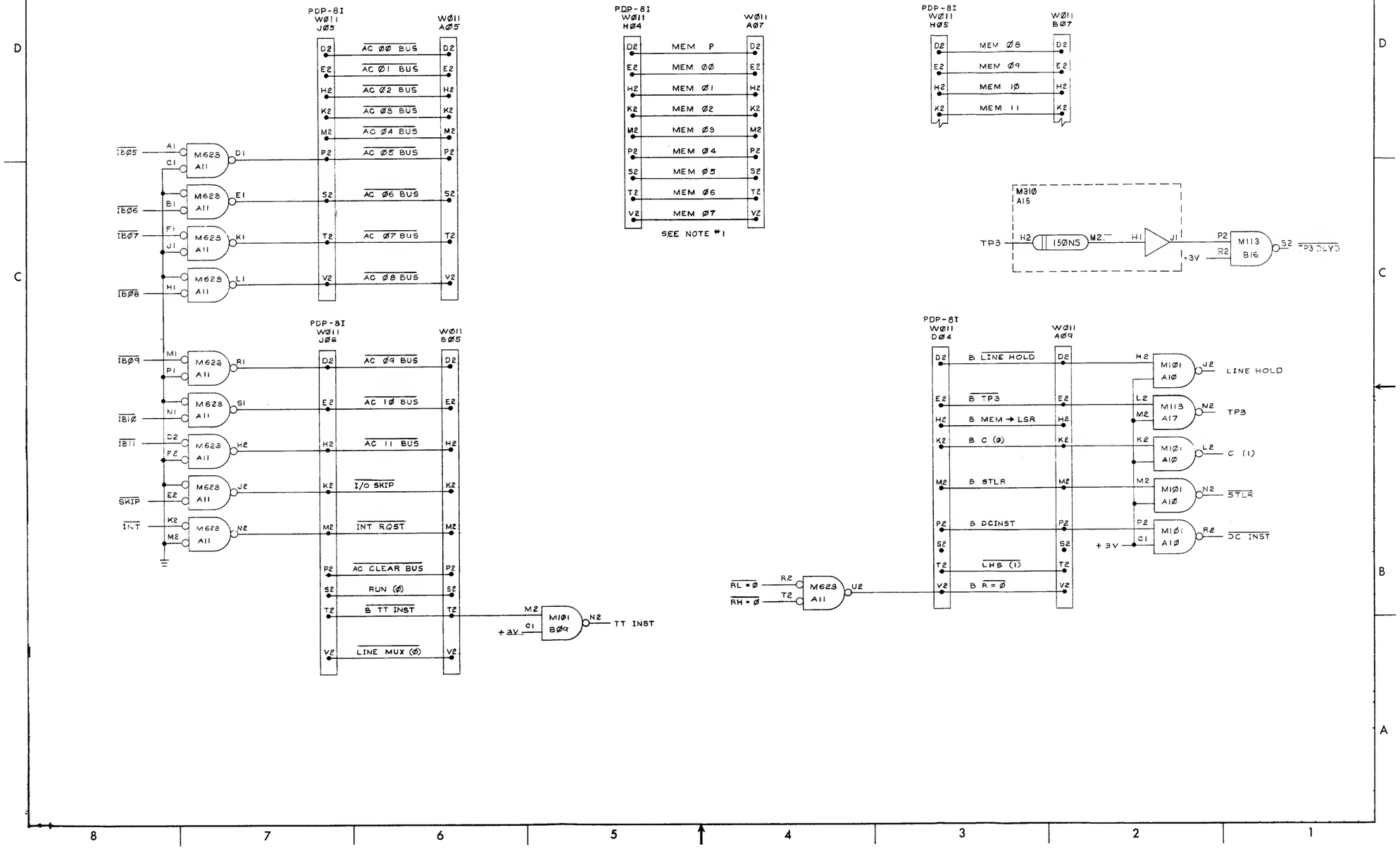
M901 CONNECTOR LOCATIONS & DESTINATIONS											
SIGNAL NAME	LOCATION	PIN LETTER	SIGNAL NAME	LOCATION	PIN LETTER	SIGNAL NAME	LOCATION	PIN LETTER	SIGNAL NAME	LOCATION	PIN LETTER
DATA IN 00	A29	C1	DATA IN 32	A31	C1	DATA IN 64	B29	C1	DATA IN 96	B31	C1
OUT 00		D1	OUT 32		D1	OUT 64		D1	OUT 96		D1
IN 01		E1	IN 33		E1	IN 65		E1	IN 97		E1
OUT 01		H1	OUT 33		H1	OUT 65		H1	OUT 97		H1
IN 02		J1	IN 34		J1	IN 66		J1	IN 98		J1
OUT 02		K1	OUT 34		K1	OUT 66		K1	OUT 98		K1
IN 03		L1	IN 35		L1	IN 67		L1	IN 99		L1
OUT 03		M1	OUT 35		M1	OUT 67		M1	OUT 99		M1
IN 04		N1	IN 36		N1	IN 68		N1	IN 100		N1
OUT 04		P1	OUT 36		P1	OUT 68		P1	OUT 100		P1
IN 05		R1	IN 37		R1	IN 69		R1	IN 101		R1
OUT 05		S1	OUT 37		S1	OUT 69		S1	OUT 101		S1
IN 06		T1	IN 38		T1	IN 70		T1	IN 102		T1
OUT 06		U1	OUT 38		U1	OUT 70		U1	OUT 102		U1
IN 07		V1	IN 39		V1	IN 71		V1	IN 103		V1
OUT 07		C2	OUT 39		C2	OUT 71		C2	OUT 103		C2
IN 08		D2	IN 40		D2	IN 72		D2	IN 104		D2
OUT 08		E2	OUT 40		E2	OUT 72		E2	OUT 104		E2
IN 09		H2	IN 41		H2	IN 73		H2	IN 105		H2
OUT 09		J2	OUT 41		J2	OUT 73		J2	OUT 105		J2
IN 10		K2	IN 42		K2	IN 74		K2	IN 106		K2
OUT 10		L2	OUT 42		L2	OUT 74		L2	OUT 106		L2
IN 11		M2	IN 43		M2	IN 75		M2	IN 107		M2
OUT 11		N2	OUT 43		N2	OUT 75		N2	OUT 107		N2
IN 12		P2	IN 44		P2	IN 76		P2	IN 108		P2
OUT 12		R2	OUT 44		R2	OUT 76		R2	OUT 108		R2
IN 13		S2	IN 45		S2	IN 77		S2	IN 109		S2
OUT 13		T2	OUT 45		T2	OUT 77		T2	OUT 109		T2
IN 14		U2	IN 46		U2	IN 78		U2	IN 110		U2
OUT 14		V2	OUT 46		V2	OUT 78		V2	OUT 110		V2
IN 15		C3	IN 47		C3	IN 79		C3	IN 111		C3
OUT 15	A29	D3	OUT 47	A31	D3	OUT 79	B29	D3	OUT 111	B31	D3
IN 16	A30	E3	IN 48	A32	E3	IN 80	B30	E3	IN 112	B32	E3
OUT 16		H3	OUT 48		H3	OUT 80		H3	OUT 112		H3
IN 17		J3	IN 49		J3	IN 81		J3	IN 113		J3
OUT 17		K3	OUT 49		K3	OUT 81		K3	OUT 113		K3
IN 18		L3	IN 50		L3	IN 82		L3	IN 114		L3
OUT 18		M3	OUT 50		M3	OUT 82		M3	OUT 114		M3
IN 19		N3	IN 51		N3	IN 83		N3	IN 115		N3
OUT 19		P3	OUT 51		P3	OUT 83		P3	OUT 115		P3
IN 20		R3	IN 52		R3	IN 84		R3	IN 116		R3
OUT 20		S3	OUT 52		S3	OUT 84		S3	OUT 116		S3
IN 21		T3	IN 53		T3	IN 85		T3	IN 117		T3
OUT 21		U3	OUT 53		U3	OUT 85		U3	OUT 117		U3
IN 22		V3	IN 54		V3	IN 86		V3	IN 118		V3
OUT 22		C4	OUT 54		C4	OUT 86		C4	OUT 118		C4
IN 23		D4	IN 55		D4	IN 87		D4	IN 119		D4
OUT 23		E4	OUT 55		E4	OUT 87		E4	OUT 119		E4
IN 24		H4	IN 56		H4	IN 88		H4	IN 120		H4
OUT 24		J4	OUT 56		J4	OUT 88		J4	OUT 120		J4
IN 25		K4	IN 57		K4	IN 89		K4	IN 121		K4
OUT 25		L4	OUT 57		L4	OUT 89		L4	OUT 121		L4
IN 26		M4	IN 58		M4	IN 90		M4	IN 122		M4
OUT 26		N4	OUT 58		N4	OUT 90		N4	OUT 122		N4
IN 27		P4	IN 59		P4	IN 91		P4	IN 123		P4
OUT 27		R4	OUT 59		R4	OUT 91		R4	OUT 123		R4
IN 28		S4	IN 60		S4	IN 92		S4	IN 124		S4
OUT 28		T4	OUT 60		T4	OUT 92		T4	OUT 124		T4
IN 29		U4	IN 61		U4	IN 93		U4	IN 125		U4
OUT 29		V4	OUT 61		V4	OUT 93		V4	OUT 125		V4
IN 30		C5	IN 62		C5	IN 94		C5	IN 126		C5
OUT 30		D5	OUT 62		D5	OUT 94		D5	OUT 126		D5
IN 31		U2	IN 63		U2	IN 95		U2	IN 127		U2
DATA OUT 31	A30	V2	DATA OUT 63	A32	V2	DATA OUT 95	B30	V2	DATA OUT 127	B32	V2

NOTES:

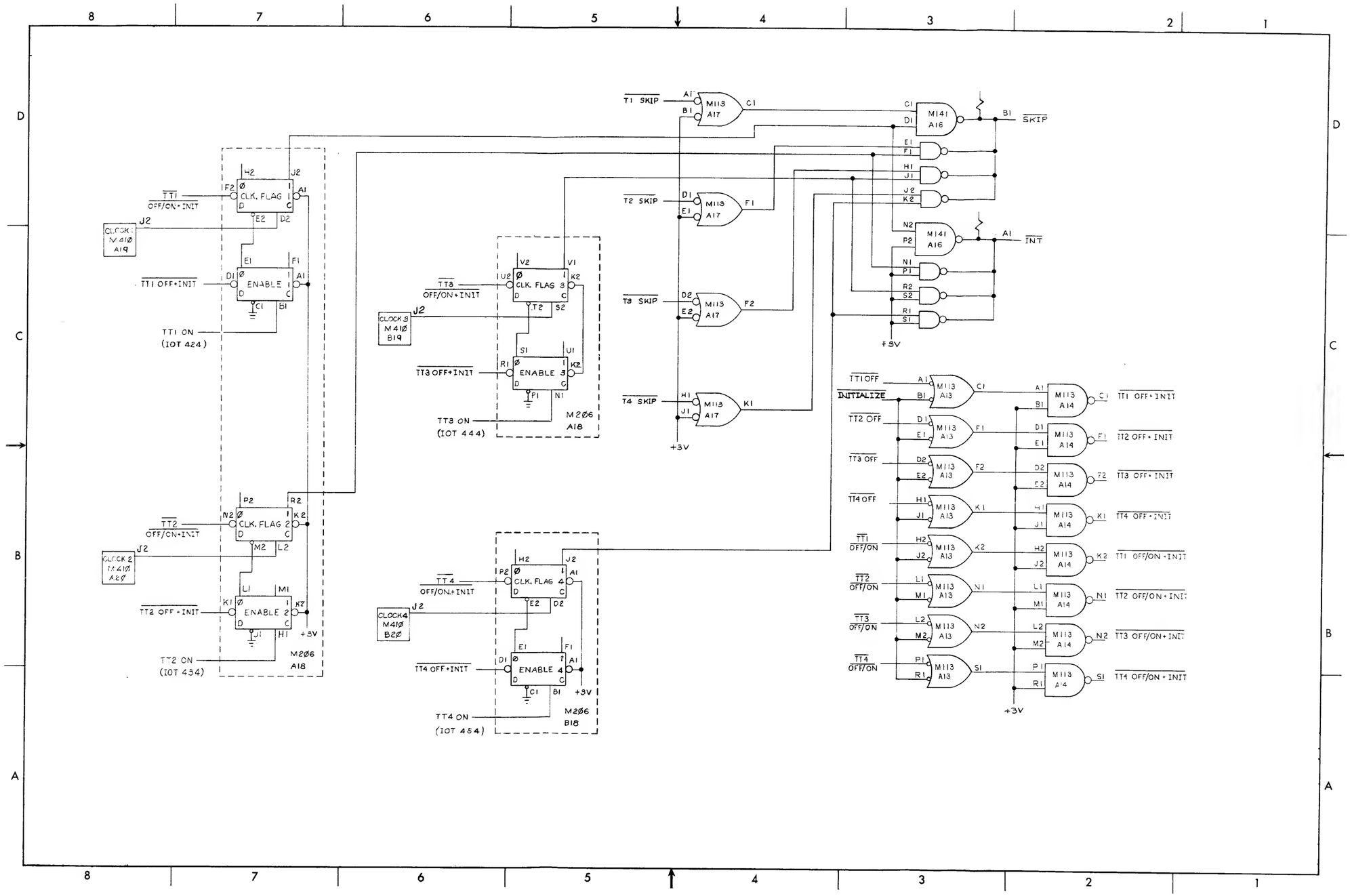
1. IN REFERENCE TO MODULE LOCATIONS (M750) THE DIAGNOSTICS REFER TO LINES IN OCTAL. CONVERSION IS PROVIDED TO EASE UNDERSTANDING OF PRINTS WHICH REFER TO LINES IN DECIMAL



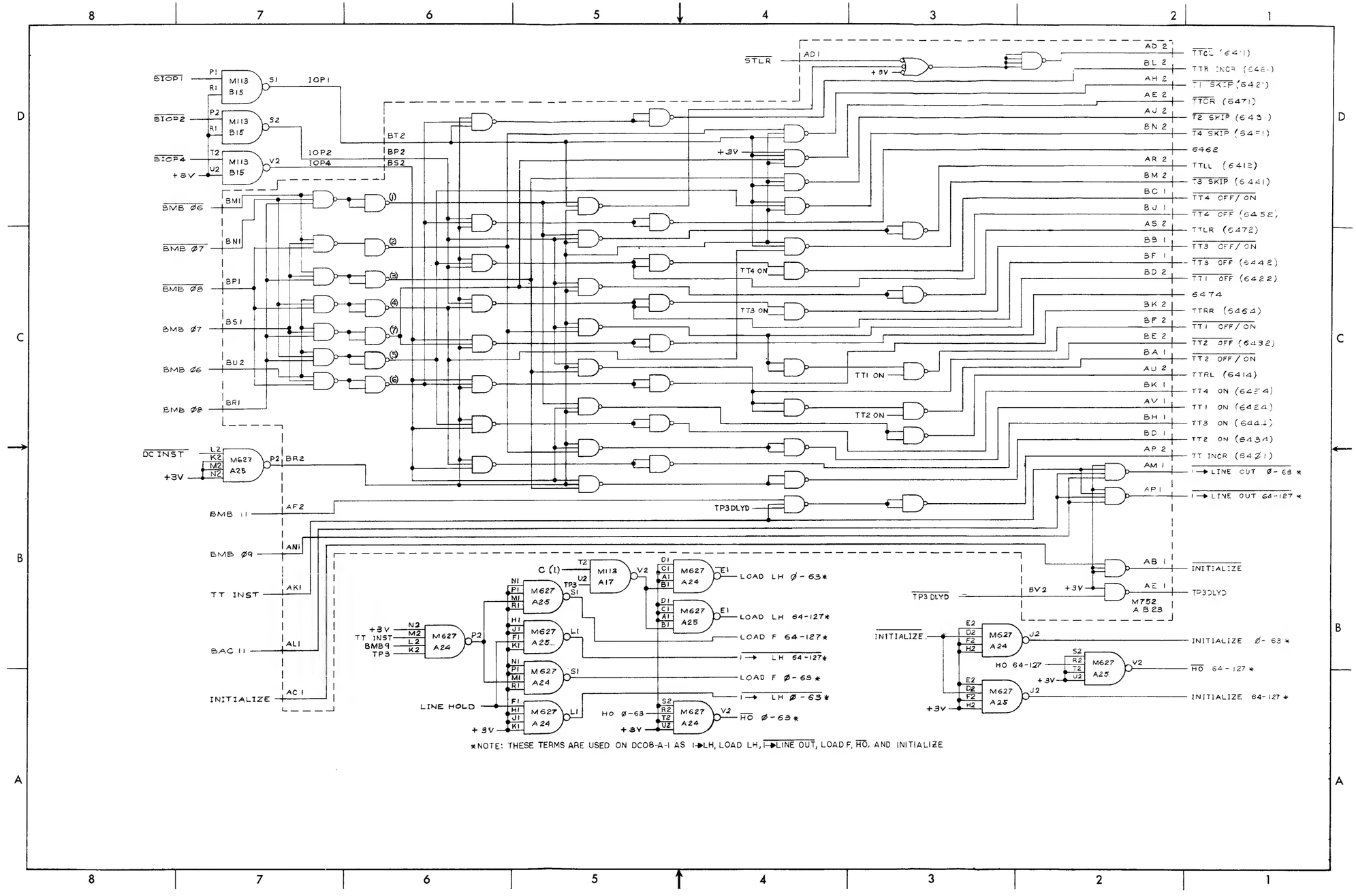
D-BS-DC08-A-2 PDP-8I DC08A Interface (Sheet 1)



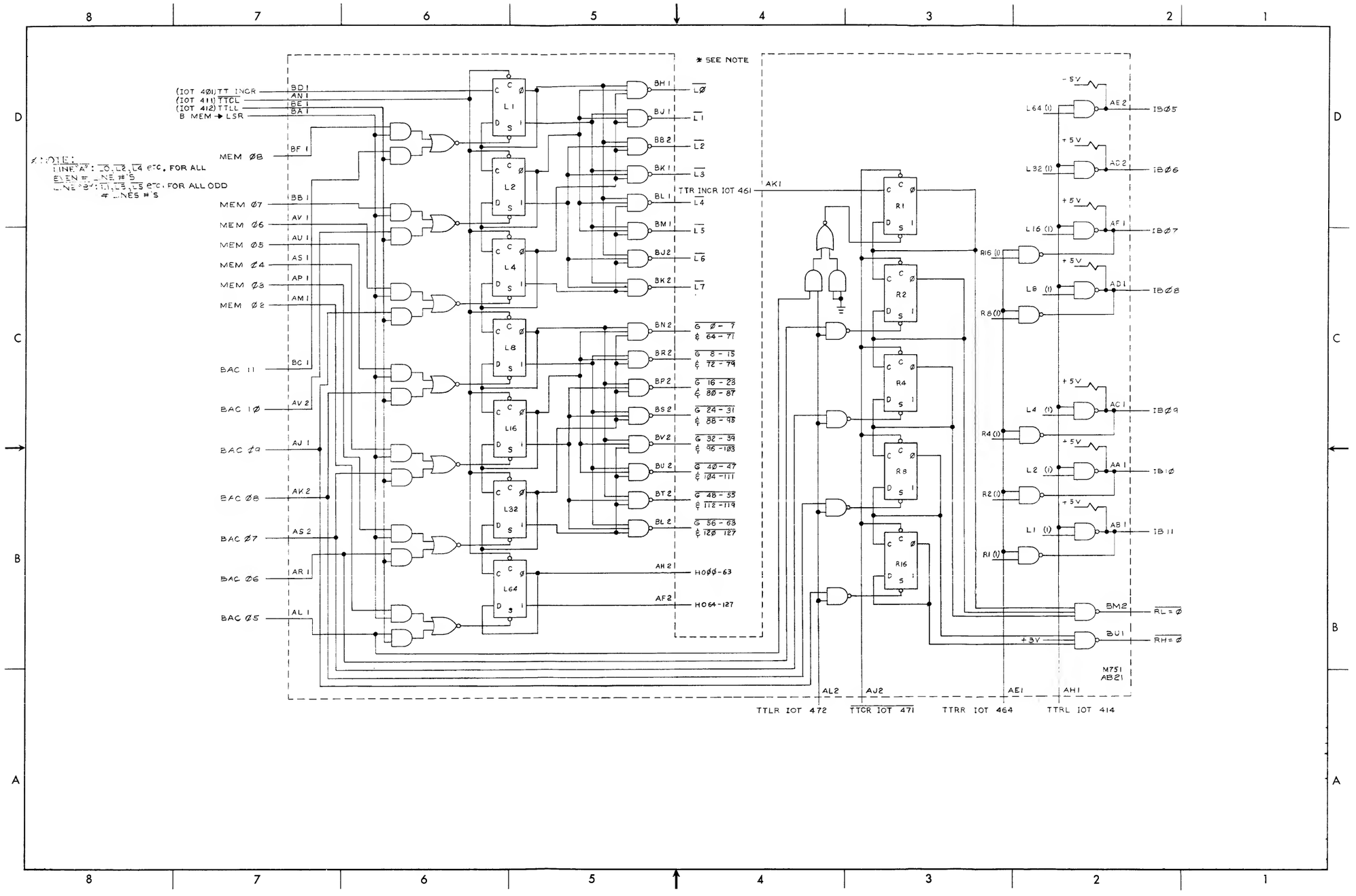
D-BS-DC08-A-2 PDP-8I DC08A Interface (Sheet 2)



D-BS-DC08-A-3 Clocks 1-4 Skip and Interrupt

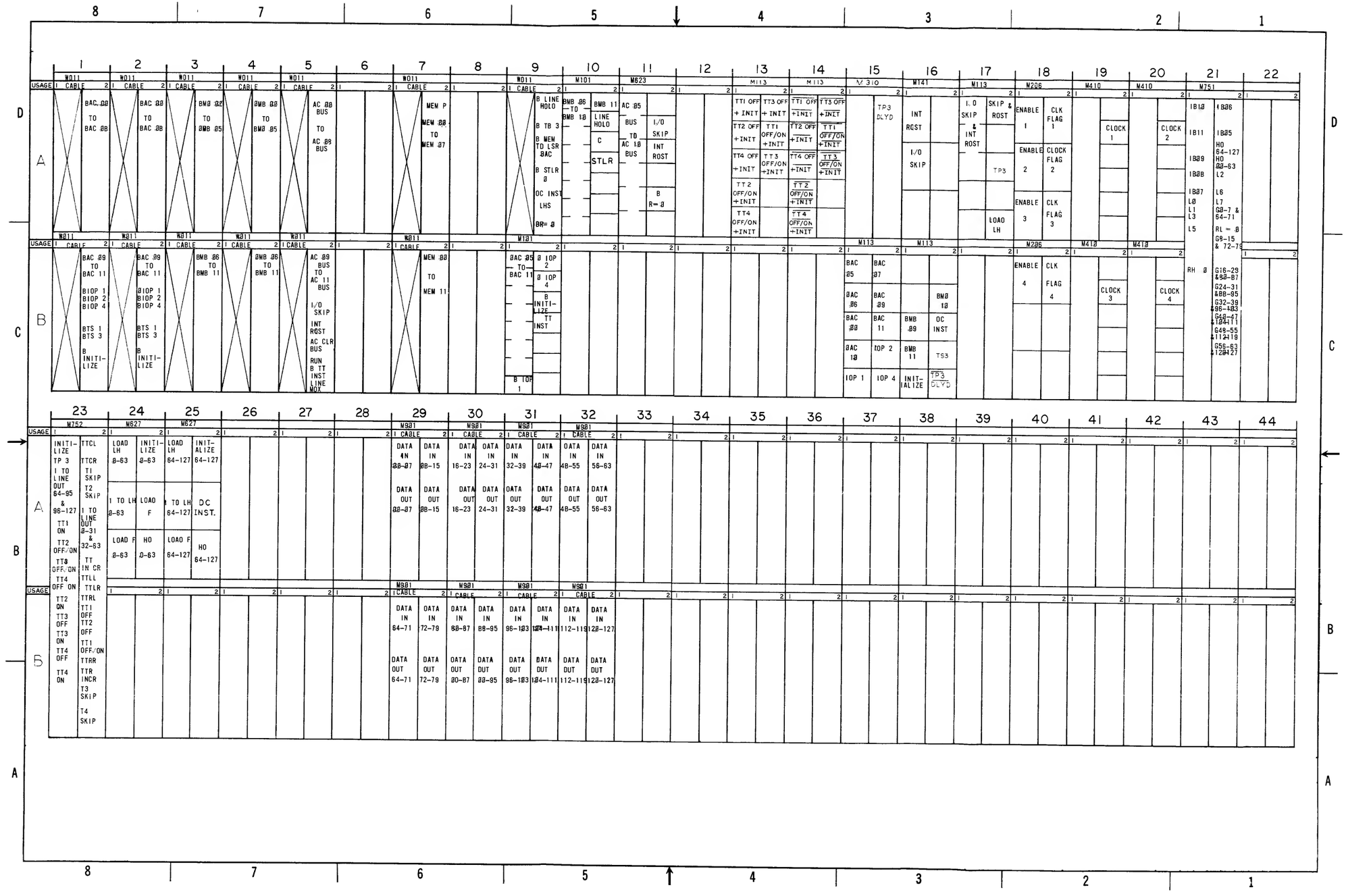


*NOTE: THESE TERMS ARE USED ON DC08-A-1 AS I→LH, LOAD LH, I→LINE OUT, LOAD F, HO, AND INITIALIZE

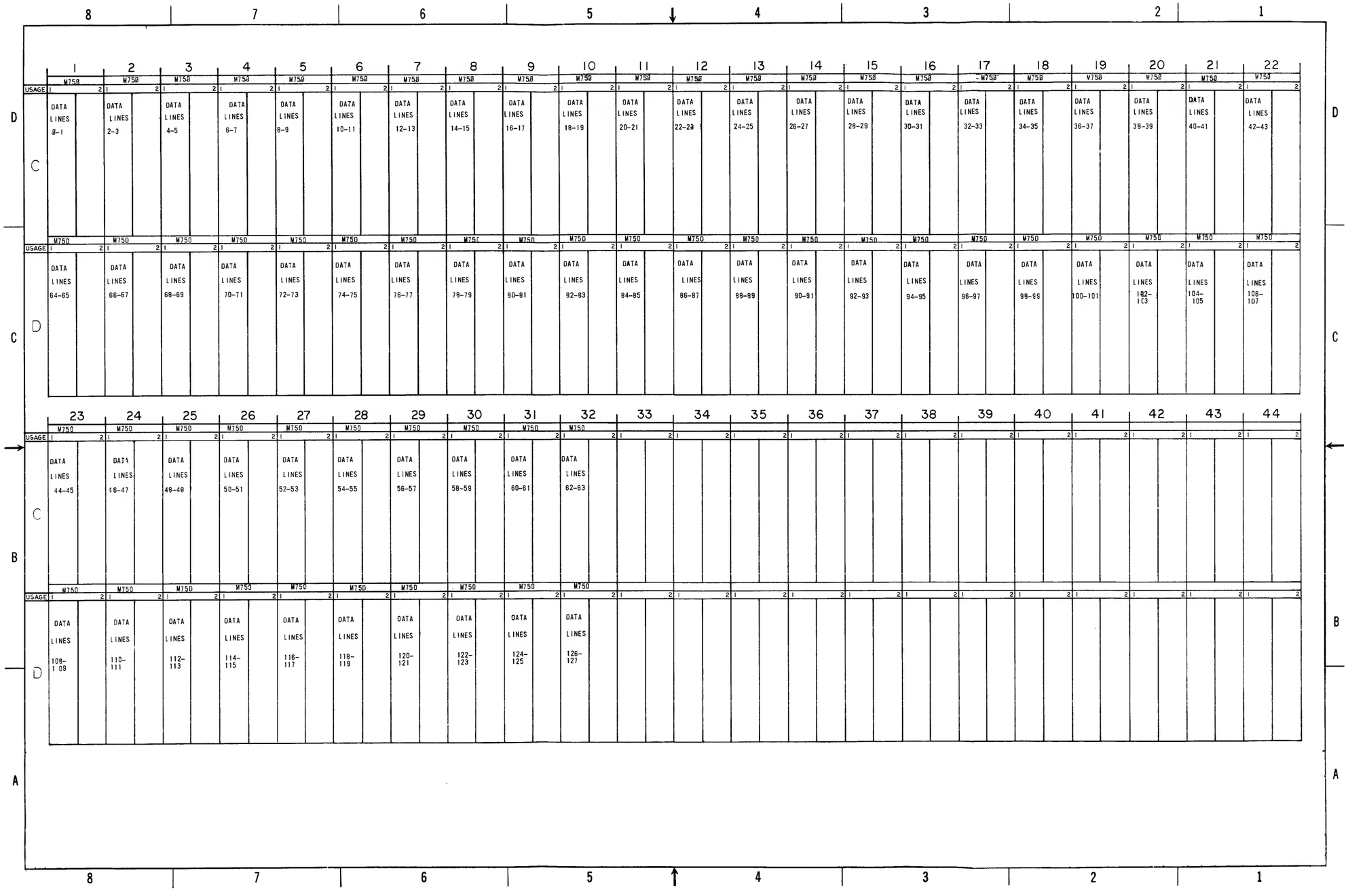


NOTE:
LINE A'S: $\overline{L0}$, $\overline{L2}$, $\overline{L4}$ etc. FOR ALL EVEN # LINE #'S
LINE B'S: $\overline{L1}$, $\overline{L3}$, $\overline{L5}$ etc. FOR ALL ODD # LINES #'S

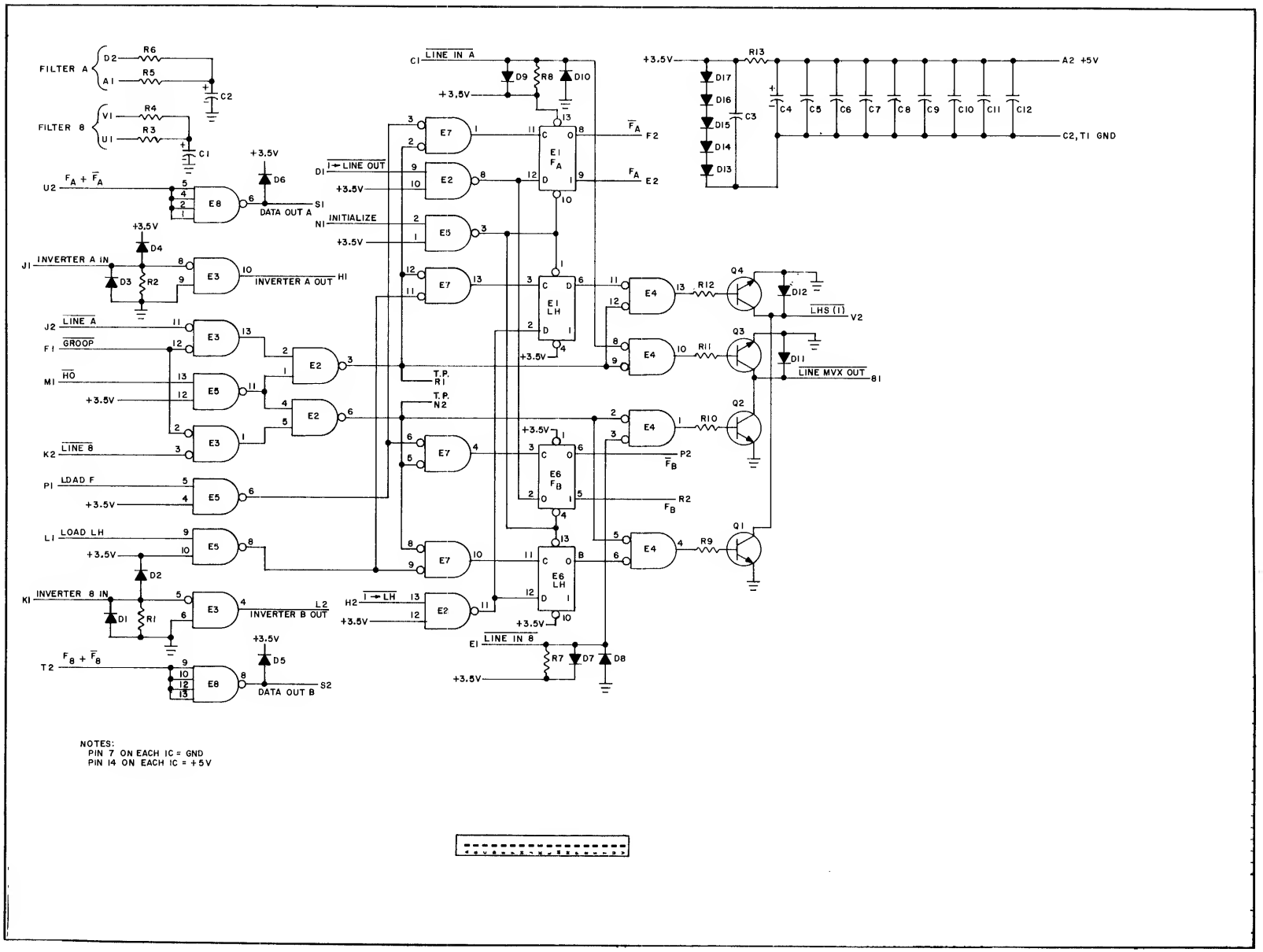
D-BS-DC08-A-5 Line Register and Control

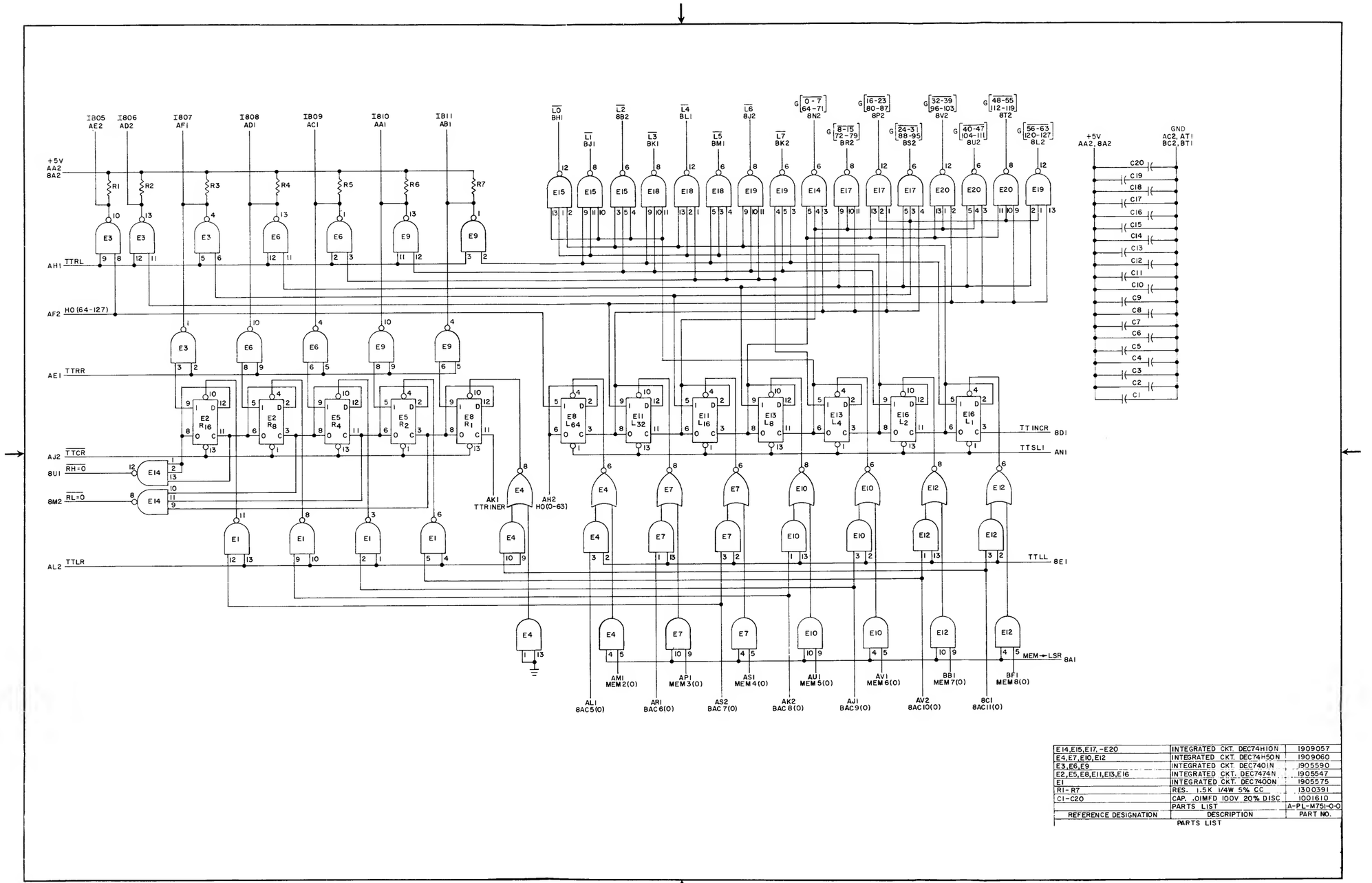


D-MU-DC08-A-6 Module Utilization (Sheet 1)



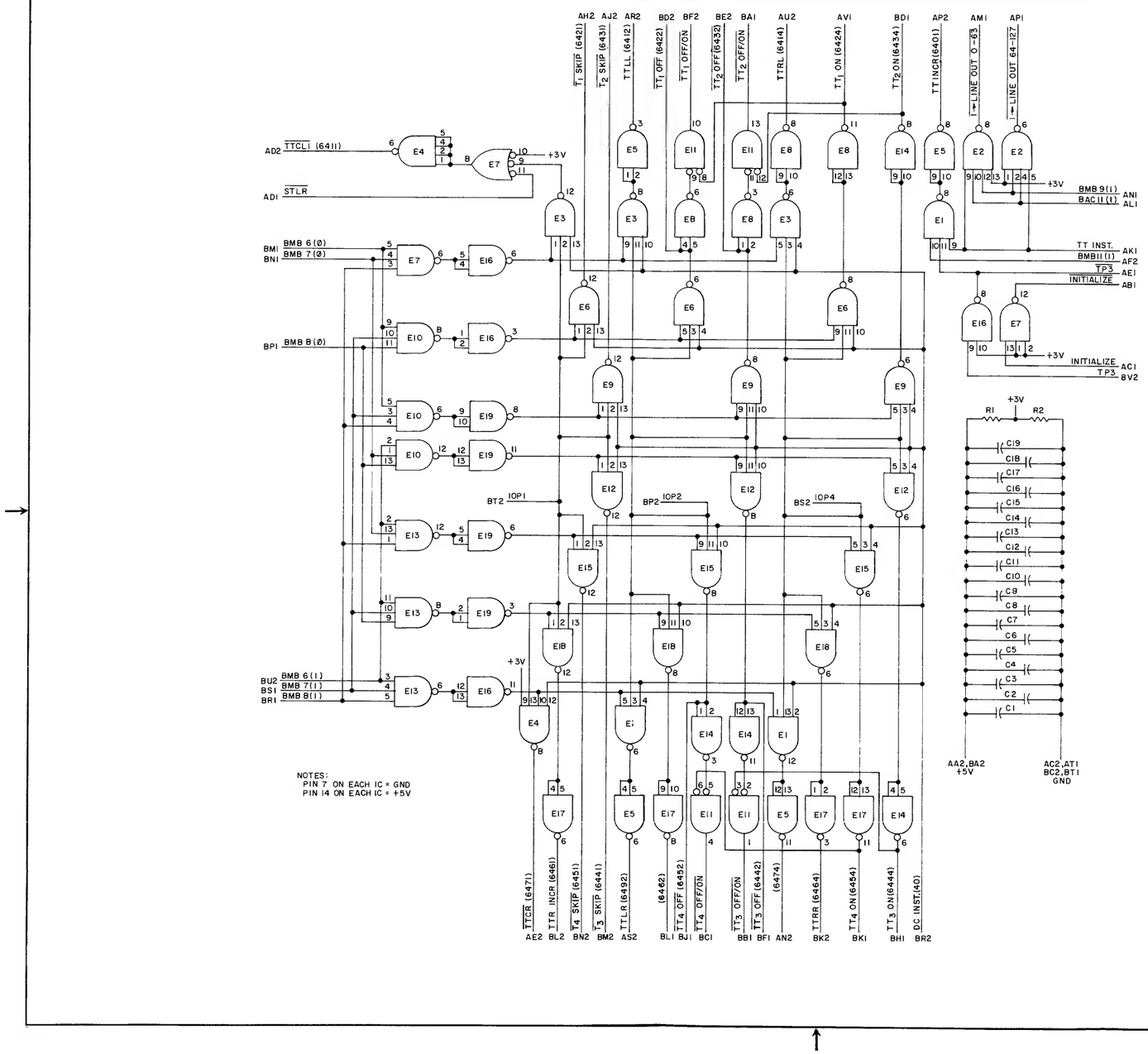
D-MU-DC08-A-6 Module Utilization (Sheet 2)


FILTER A
D2
A1
R6
R5
C2
FILTER B
V1
U1
R4
R3
C1
+3.5V
D6
U2
$F_A + \overline{F}_A$
E8
DATA OUT A
S1
D4
J1
INVERTER A IN
D3
R2
E3
INVERTER A OUT
H1
J2
LINE A
F1
GROOP
M1
H0
+3.5V
K2
LINE B
P1
LDAD F
L1
LOAD LH
D2
K1
INVERTER B IN
D1
R1
INVERTER B OUT
L2
T2
$F_B + \overline{F}_B$
D5
DATA OUT B
S2
E7
E2
E5
E1 F_A
E1 LH
E6 F_B
E6 LH
D1 LINE OUT
N1 INITIALIZE
H2 1→LH
T.P. R1
T.P. N2
C1 LINE IN A
D9
R8
D10
E1 LINE IN B
R7
D7
D8
$\overline{F}_A$ F2
F_A E2
$\overline{F}_B$ P2
F_B R2
E4
Q4
Q3
Q2
Q1
R12
R11
R10
R9
D12
D11
LHS (1) V2
LINE MVX OUT B1
+3.5V
R13
D17
D16
D15
D14
D13
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
A2 +5V
C2, T1 GND
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M751-0-0
C1-C20	CAP. .01MFD 100V 20% DISC	1001610
R1-R7	RES. 1.5K 1/4W 5% CC	1300391
E1	INTEGRATED CKT. DEC7400N	1905575
E2,E5,E8,E11,E13,E16	INTEGRATED CKT. DEC7474N	1905547
E3,E6,E9	INTEGRATED CKT. DEC7401N	1905590
E4,E7,E10,E12	INTEGRATED CKT. DEC74H50N	1909060
E14,E15,E17,-E20	INTEGRATED CKT. DEC74H10N	1909057

PARTS LIST



E11	INTEGRATED CKT. DEC7402N	1909004
E5,E8,E14,E16,E17,E19	INTEGRATED CKT. DEC7400N	1905575
E2	INTEGRATED CKT. DEC74H40N	1905586
E4	INTEGRATED CKT. DEC7440N	1905579
E1,E3,E6,E7,E9,E10,E12,E13,E15,E18	INTEGRATED CKT. DEC7410N	1905576
R2	RES. 750 1/4W 5% CC	1301401
R1	RES. 330 1/4W 5% CC	1300295
C1 - C19	CAP. .01 MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M752-0-0

REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

Digital Equipment Corporation
Maynard, Massachusetts

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