

PDP-8
Maintenance Manual

DM01

Data Multiplexer

PDP-8
DM01
DATA MULTIPLEXER
MAINTENANCE MANUAL

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CONTENTS

<u>Chapter</u>		<u>Page</u>
1	INTRODUCTION.....	1-1
2	SCOPE.....	2-1
3	OPERATION.....	3-1
3.1	General.....	3-1
3.2	Logic Operation.....	3-1
3.2.1	Multiplexer Control (BS-D-DM01-0-2).....	3-1
3.2.2	Level Production from Multiplexer Control (BS-D-DM01-0-11)	3-3
3.2.3	Data Address Line Selector (BS-D-DM01-0-4)	3-4
3.2.4	Data Bits Line Selector (BS-D-DM01-0-3).....	3-4
4	INTERFACE.....	4-1
5	POWER SUPPLY	5-1
6	MAINTENANCE	6-1
6.1	Preventive Maintenance	6-1
6.1.1	Power Supply Checks.....	6-1
6.2	Corrective Maintenance	6-1
7	INSTALLATION.....	7-1
7.1	Mounting.....	7-1
7.2	Environmental Conditions	7-1
7.3	Power Requirements	7-1
8	SCHEMATICS	8-1
8.1	Semiconductor Substitution.....	8-1

TABLES

<u>Table</u>		
6-1	Type 728 Power Supply Output Checks (Drawing CS-B-728).....	6-1
8-1	Semiconductor Substitution.....	8-1

ILLUSTRATIONS

<u>Figure</u>		
1-1	DM01 General Block Diagram	1-1
3-1	DM01 Data Break Signals	3-2
3-2	PDP-8 - DM01 Timing Diagram	3-3

CONTENTS (continued)

<u>Figure</u>		<u>Page</u>
8-1	Power Supply (CS-B-728)	8-2
8-2	Diode Gate (CS-B-B141)	8-2
8-3	Diode Cluster (RS-B-R002)	8-3
8-4	Dual Flip-Flop (RS-B-R202)	8-3
8-5	Inverter (CS-B-S107).....	8-4
8-6	Diode Gate (CS-B-S111)	8-4
8-7	DC Carry Chain (RS-B-S181)	8-5
8-8	Dual Flip-Flop (CS-B-S202).....	8-5
8-9	Clamped Loads (CS-B-W005)	8-6
8-10	Signal Cable Connector (RS-B-W021)	8-6
8-11	Pulse Amplifier (CS-B-W640).....	8-7
8-12	Utilization Module List (UML-D-DM01-0-8)	8-9
8-13	Multiplexer Control (BS-D-DM01-0-2)	8-11
8-14	Level Production from Multiplexer Control (BS-D-DM01-0-11)	8-13
8-15	Data Address Line Selector (BS-D-DM01-0-4)	8-15
8-16	Data Bits Line Selector (BS-D-DM01-0-3).....	8-17
8-17	DM01 Interconnecting Cable Diagram (IC-DM01-0-13)	8-19
8-18	I/O Connectors (BS-D-DM01-0-6)	8-21
8-19	Data Multiplexer Connectors (BS-D-DM01-0-5).....	8-23

CHAPTER 1

INTRODUCTION

This manual covers the maintenance of the data multiplexer, designated as Type DM01, now in production at the Digital Equipment Corporation of Maynard, Massachusetts.

The DM01 is essentially a switching device for use between the PDP-8[®] and a maximum of seven peripheral or I/O devices, as shown in figure 1-1. The peripheral devices include high-speed magnetic tape systems, high-speed drum memories, and CRT display systems containing memory elements, all of which use the PDP-8 data break facility.

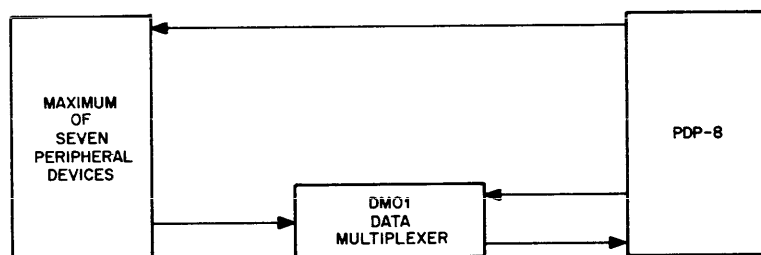


Figure 1-1 DM01 General Block Diagram

[®] PDP is the registered trademark of the Programmed Data Processor manufactured by Digital Equipment Corporation of Maynard, Massachusetts.

CHAPTER 2

SCOPE

This manual provides complete maintenance data on the logic circuitry of the Data Multiplexer Type DM01. It details information on logical operation, interface characteristics and connections, and installation and mounting.

Uses of the levels and pulses produced by the peripheral devices and the PDP-8 are not covered in this manual. For further information on such signals, reference to the PDP-8 User's Handbook F-85 and instruction manuals of the specific peripheral devices is advised.

CHAPTER 3

OPERATION

3.1 GENERAL

The Data Multiplexer Type DM01, as noted, acts as a switch between the PDP-8 and a maximum of seven high-speed peripheral devices which use the data break facility.

Whenever a device using the data break facility requests a break, the device produces a number of signals. As figure 3-1 shows, only the signals from the selected peripheral device pass through the DM01 into the PDP-8.

3.2 LOGIC OPERATION

The following paragraphs describe the logic operation of the DM01 Data Multiplexer as it relates to the PDP-8 and the peripheral devices connected to it. (Each major heading references directly to an engineering drawing found in chapter 8 of this manual.)

3.2.1 Multiplexer Control (BS-D-DM01-0-2)

Figure 8-13 illustrates the logic control circuitry of the DM01 Data Multiplexer. Upon receipt of PDP-8 timing pulses and a BRK REQ (break request) level from the peripheral device requesting the data break, this control logic produces MPX, B ENABLE, and BRK REQ levels and ADD ACC (address accepted) pulse.

For ease in explanation, it is assumed the peripheral device producing the BRK REQ 1 level is requesting service. Similar operations occur when other peripheral devices request data breaks.

The timing diagram in figure 3-2 is used in conjunction with the multiplexer control description.

During the PDP-8 turn-on period, or whenever the operator presses the START key, POWER CLEAR pulses (-3v, 100-nsec pulses at a 10-kHz rate) clear the BREAK IN PROGRESS (figure 8-4), and the B ENABLE, and MPX flip-flops (figure 8-8). These pulses are accepted, and their function implemented, without the need for device selection through addressing.

All BRK REQ levels enter the DM01 through the R002 diode network (figure 8-3) at location B22 and S111 diode gate (figure 8-6) at B23. This circuitry is shown in the upper right corner of the drawing.

The ground BRK REQ 1 level is applied to terminal L of the above modules. The remaining input terminals are at -3v.

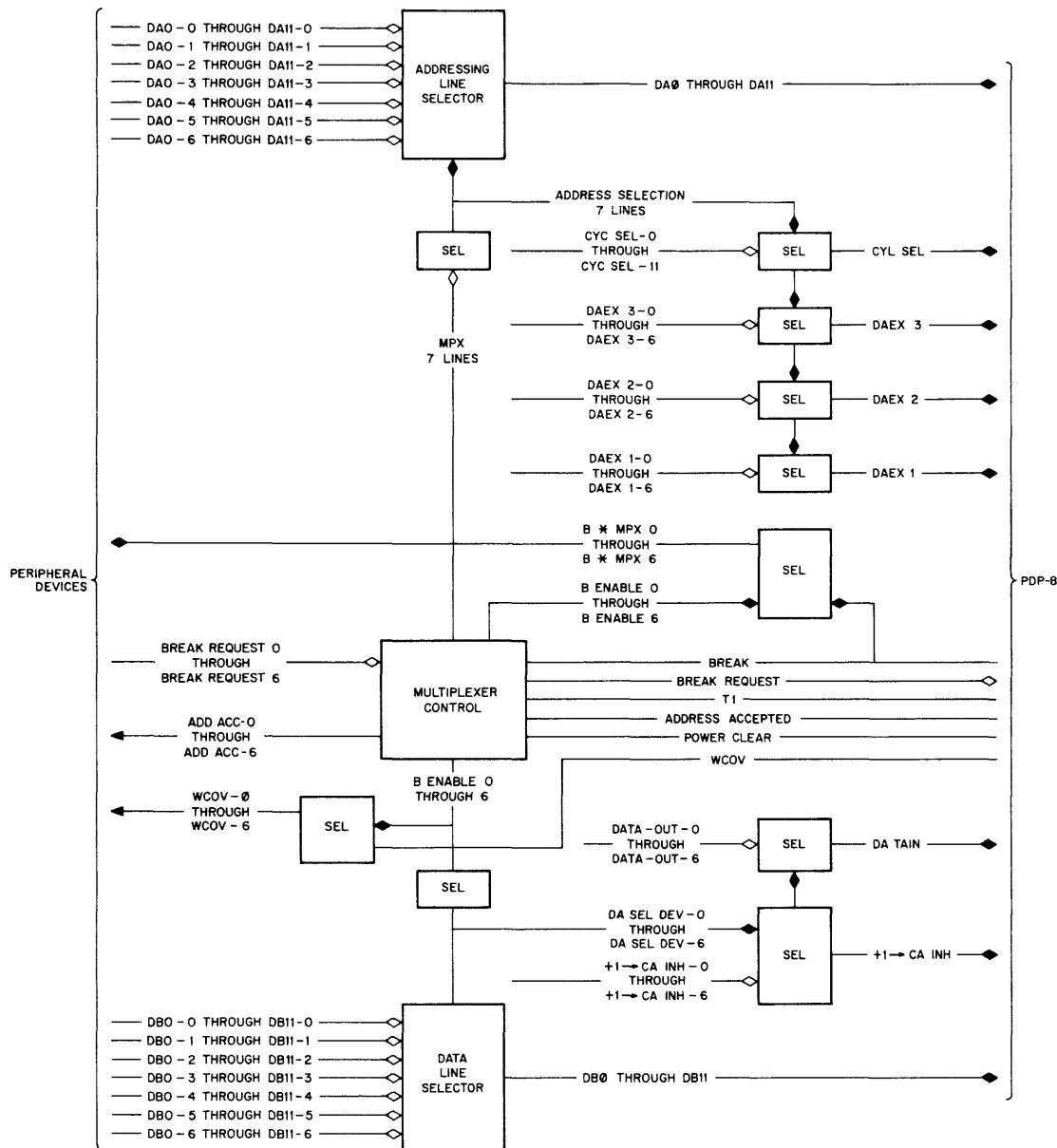


Figure 3-1 DM01 Data Break Signals

The -3v output of the S111 diode gate is inverted by the S107 module (figure 8-5) at location B32. The resulting BRK REQUEST ground level goes to the PDP-8 major state generator to signal the computer that a data transfer is to take place.

BRK REQ 1 is also applied to terminal E of the W005 clamped load (figure 8-9) at location B9 and shown across the middle of the drawing. The level enables the DCD gate associated with the set terminal of the MPX-1 flip-flop. The corresponding gate of the remaining MPX flip-flops is inhibited.

A PDP-8 T1 timing pulse sets the MPX-1 flip-flop, enabling the DCD gate connected to the set terminal of the B ENABLE 1 flip-flop. The ground level from the 1 side of the MPX-1 is applied to terminal F of the S181 dc carry chain (figure 8-7) at B12 and shown across the lower portion on the drawing. Through this operation, all MPX flip-flops that are less significant (to the right of) than MPX-1 are held in the 0 state. Because of this function, the peripheral device producing BRK REQ 1 is given priority over the less significant peripherals.

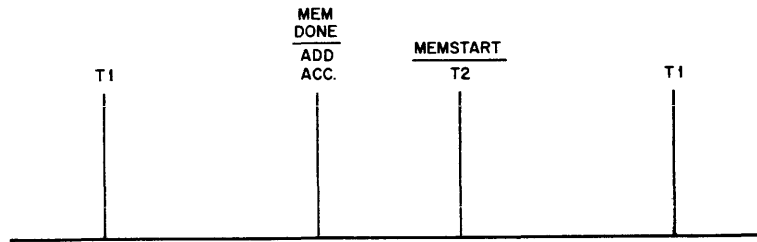


Figure 3-2 PDP-8 - DM01 Timing Diagram

A -3v level is present at K of the S111 module at B30 and also shown across the lower part of the drawing. When an ADDRESS ACCEPTED pulse arrives from the PDP-8, B ENABLE 1 is set and a -3v ADD ACC-1 pulse is generated.

The levels and pulses produced by multiplexer control are used by other circuits of the DM01, as covered in the following sections.

3.2.2 Level Production from Multiplexer Control (BS-D-DM01-0-11)

The logic circuitry of figure 8-14 uses the output levels of the MPX and B ENABLE flip-flops to produce levels and pulses for use by both the DM01 and the peripheral devices.

The logic element on the left side of the drawing consists of seven, 2-input, diode gate-inverter-clamped load networks. The S111 diode gates at locations B6, B8, and B23 have paired inputs which form AND gates. One terminal of each gate is common, and is at -3v whenever a break is in progress.

Proceeding with the example, a -3v level from the set B ENABLE 1 flip-flop provides the level necessary to give the desired -3v B · MPX 1 level from the W005 clamped load at B9.

The gated driver, made up of the S111 diode gates at A16, A17, and A18 and the W640 pulse converters (figure 8-11) at B29, A14, and A15 produce a -3v WCOV (word count overflow) pulse when suitable inputs are present. Because a -3v B ENABLE level is present, a -3v WCOV-1 pulse is produced when a -3v WCOV pulse arrives. The B · MPX 1 level and WCOV-1 pulse go to peripheral device 1.

The two paralleled inverters on the right side of the drawing produce levels that are used by DM01 selector networks. A -3v DB SEL DEV 1 level, which is used by the selector networks shown in figure 8-16 and discussed in section 3.2.4, is generated by applying a ground level from the B ENABLE 1 flip-flop to terminal H of the S107 diode gate at A12. The output is at terminal F at B4.

DA SBL DEV 1 is used by the logic circuitry of figures 8-15 and 8-16, and is explained in section 3.2.3. The level is produced by inverting the MPX-1 ground level present at terminal H of the S107 inverter at B5. The output is present at F, location A13.

3.2.3 Data Address Line Selector (BS-D-DM01-0-4)

The circuitry shown across the top of figure 8-15 serves to permit the 12-bit address from the peripheral device requesting the break to enter the PDP-8 memory address register. This is accomplished through a logical AND operation.

The terminals labeled E, H, K, M, P, S, and U of the B141 Module (figure 8-2) at location C1 receive the levels designated DA SEL DEV 0 through DA SEL DEV 6, respectively. The most significant data address bit from the peripheral devices is applied to terminals F, J, L, N, R, T, and V of module C1; the least significant is applied to module C12.

Continuing with the example, a -3v DA SEL DEV 1 level, applied to terminal H, provides one level needed by the AND gate. The data address bits, designated DA0-1 through DA11-1, are applied to the remaining terminal of the gate.

The output levels, DA0 through DA11, which go to the PDP-8 memory address register, appear at the S107 inverter output at locations B7 and B15.

The logic circuitry across the lower part of the drawing functions in a similar manner. DA SEL DEV 1 enables the same terminal of each B141 Module.

A CYC SEL-1 level from peripheral device 1 is logically ANDed with DA SEL DEV 1 in the diode gate at C13. The output CYC SEL level, available at terminal R of the inverter at B15, goes to the PDP-8 major state generator.

The B141 diode gates at locations C14, C15, and C16 permit the extended memory address bits from peripheral device 1 to enter the PDP-8. The output levels, designated DAEX 1, DAEX 2, and DAEX 3, are available at the S107 inverter terminals F and D at B25 and T at B15, respectively.

3.2.4 Data Bits Line Selector (BS-D-DM01-0-3)

Data bits from the selected peripheral device reach the PDP-8 memory buffer register through the logic circuitry, made up of the B141 diode gates at locations C17 through C28, and illustrated across the top of figure 8-16.

This circuitry operates in the same manner as that used for data addressing; namely, DB SEL DEV 1 provides one level required by the gate string, and the data bits from peripheral device 1, designated DB0-1 through DB11-1, provide the remaining levels.

The 12-bit output, comprised of the bits labeled DB0 through DB11, are found at the S107 inverter outputs at locations B25 and B26.

An INCREMENT CA INHIBIT (+1 \longrightarrow CA INH) level, which is used during 3-cycle breaks, is produced by ANDing the DB SEL DEV 1 and +1 \longrightarrow CA INH levels.

Similarly, a DATA IN level, which specifies the data transfer direction, is produced by ANDing DA SEL DEV 1 with DATA OUT.

These two levels are terminated at pins N and R, respectively, of the S107 diode gate at location B32.

CHAPTER 4

INTERFACE

All interface connections to the DM01 are made at assigned module receptacle connectors at the back of the multiplexer. The interfacing between the PDP-8, DM01, and the peripheral devices is shown in the following figures:

Figure 8-17	DM01 Interconnecting Cable Diagram (IC-DM01-0-13)
Figure 8-18	I/O Connectors (BS-D-DM01-0-6)
Figure 8-19	Data Multiplexer Connectors (BS-D-DM01-0-5)

CHAPTER 5

POWER SUPPLY

ADEC Type 728 Power Supply (table 8-1) generates the voltage levels (+10 and -15 vdc) required for operation of the multiplexer.

Chapter 8 contains the schematic of this power supply and chapter 6, the output check data. The DEC System Modules Catalog (C-100) provides detailed information on the operational characteristics of the supply.

CHAPTER 6

MAINTENANCE

6.1 PREVENTIVE MAINTENANCE

The general preventive maintenance procedures provided in the PDP-8 Maintenance Manual (F-87) apply to the multiplexer control logic.

6.1.1 Power Supply Checks

Table 6-1 shows the output voltage checks needed for the Type 728 Power Supply used in this equipment. Perform the power supply checks described in table 6-1. Use a multimeter to make the output voltage measurements with the normal load connected, and an oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10v and -15v supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, consider the power supply defective and initiate troubleshooting procedures.

TABLE 6-1 TYPE 728 POWER SUPPLY OUTPUT CHECKS
(Drawing CS-B-728)

Measurement Terminals at Power Supply Output	Nominal Output (vdc)	Acceptable Output Range (v)	Maximum Output Current (a)	Maximum Peak-to-Peak Output Ripple (v)
Red (+) to Yellow (-)	+10	+9.5 to +11.0	7	0.7
Yellow (+) to Blue (-)	-15v	-14.5 to -16.0	8	0.7

6.2 CORRECTIVE MAINTENANCE

The simplicity of the system and the logic description provided in this document permit the use of standard troubleshooting techniques for isolating the trouble quickly and efficiently. For economical maintenance under most conditions, replace the inoperative module with one from spares and return the defective module to DEC for repair or replacement.

CHAPTER 7

INSTALLATION

7.1 MOUNTING

The DM01 Data Multiplexer is 10-1/2 inches high, and is designed for mounting in a standard 19-inch-wide rack.

7.2 ENVIRONMENTAL CONDITIONS

No special environmental conditions are required for proper operation of the DM01. Ambient temperature may vary between 32° and 130° F (0° and 55° C).

7.3 POWER REQUIREMENTS

The DM01 obtains its primary power from a Type 728 Power Supply.

CHAPTER 8

SCHEMATICS

The following pages contain schematics of all modules used in the DM01 Data Multiplexer.

8.1 SEMICONDUCTOR SUBSTITUTION

Standard EIA components specified in table 8-1 can replace the majority of DEC semiconductors used in modules of the data multiplexer and shown in the schematic section of this publication. Exact replacement is recommended for semiconductors not listed.

TABLE 8-1 SEMICONDUCTOR SUBSTITUTION

DEC	EIA
D662	1N645
D664	1N3606
DEC3009A	2N3009
2N3605	same
DEC3639	2N3639
DEC3639-1	2N3639

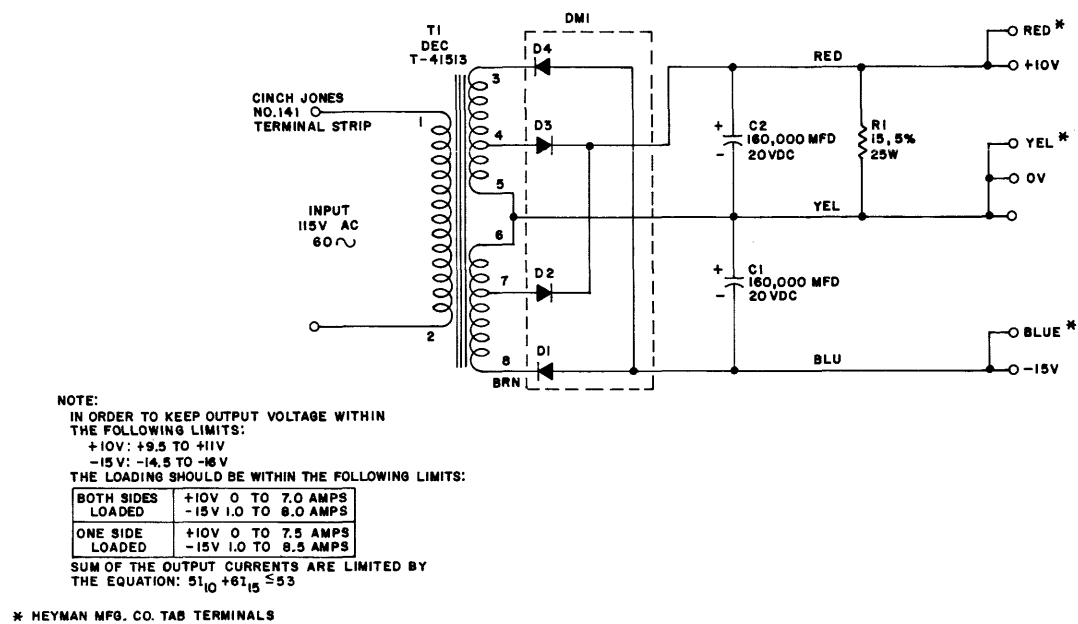


Figure 8-1 Power Supply (CS-B-728)

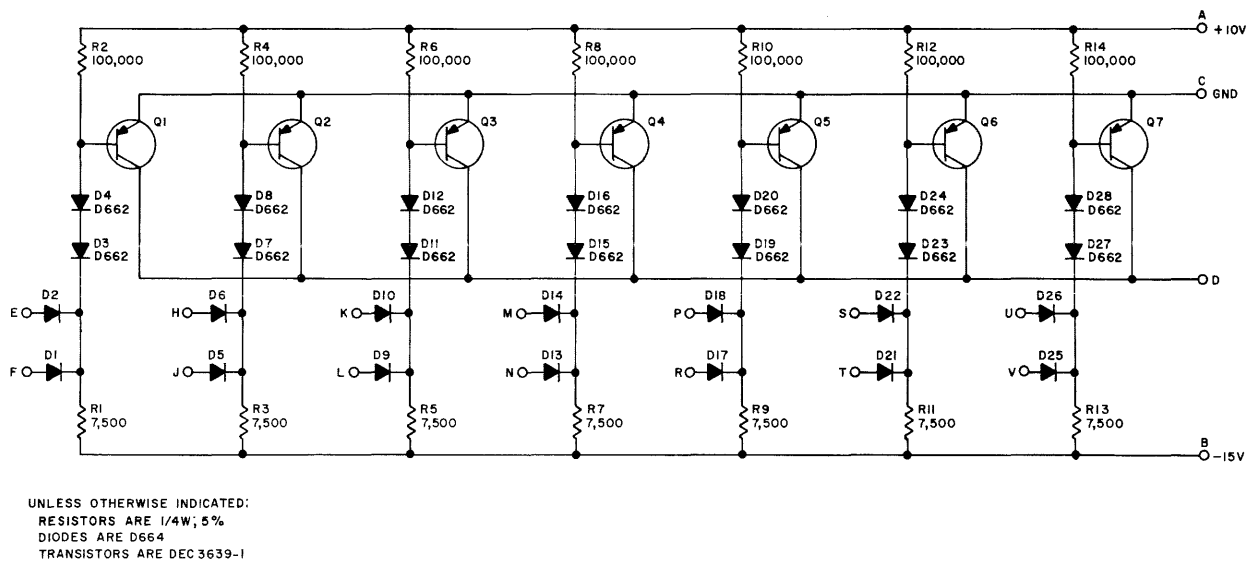


Figure 8-2 Diode Gate (CS-B-B141)

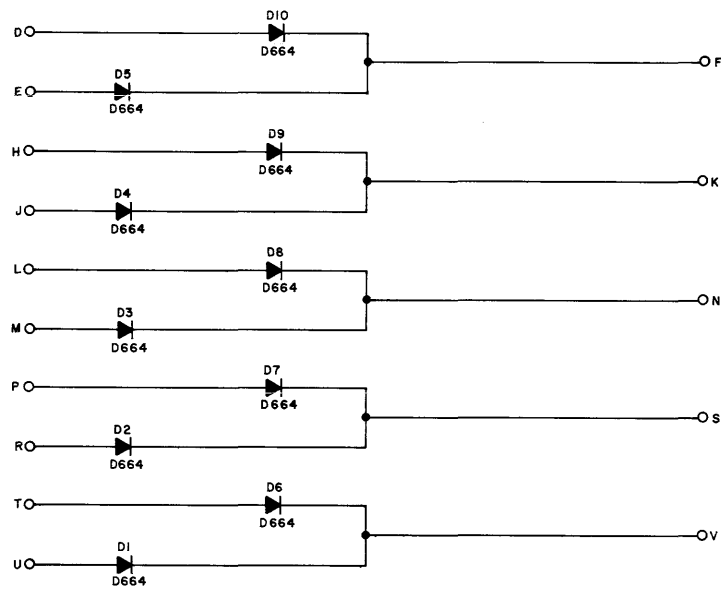


Figure 8-3 Diode Cluster (RS-B-R002)

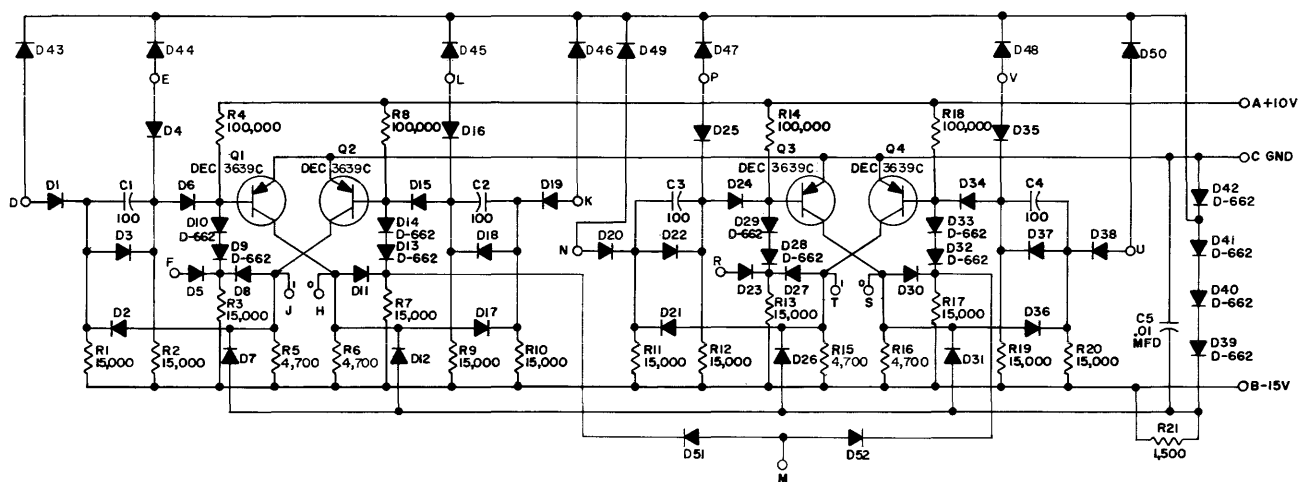


Figure 8-4 Dual Flip-Flop (RS-B-R202)

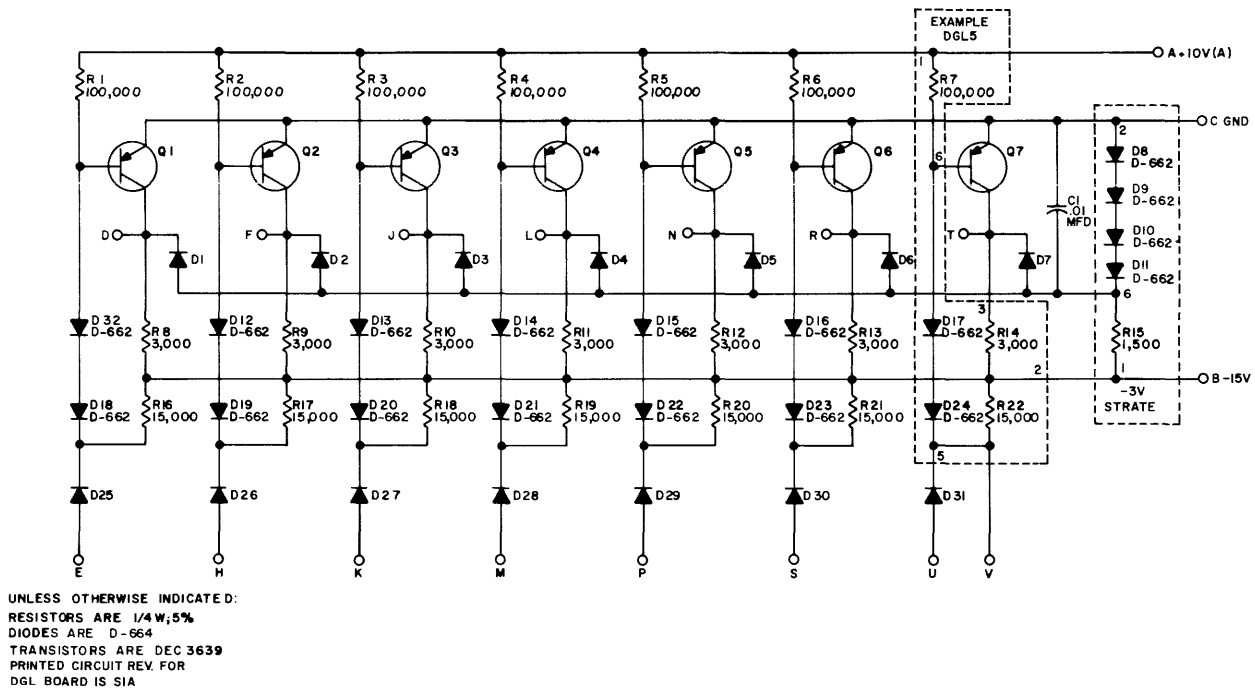


Figure 8-5 Inverter (CS-B-S107)

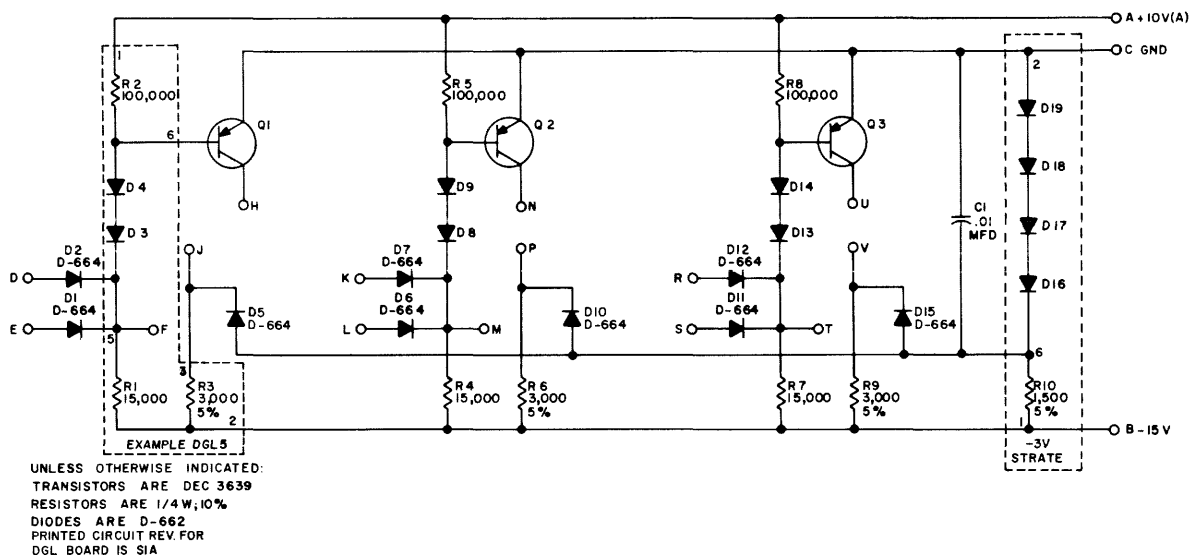


Figure 8-6 Diode Gate (CS-B-S111)

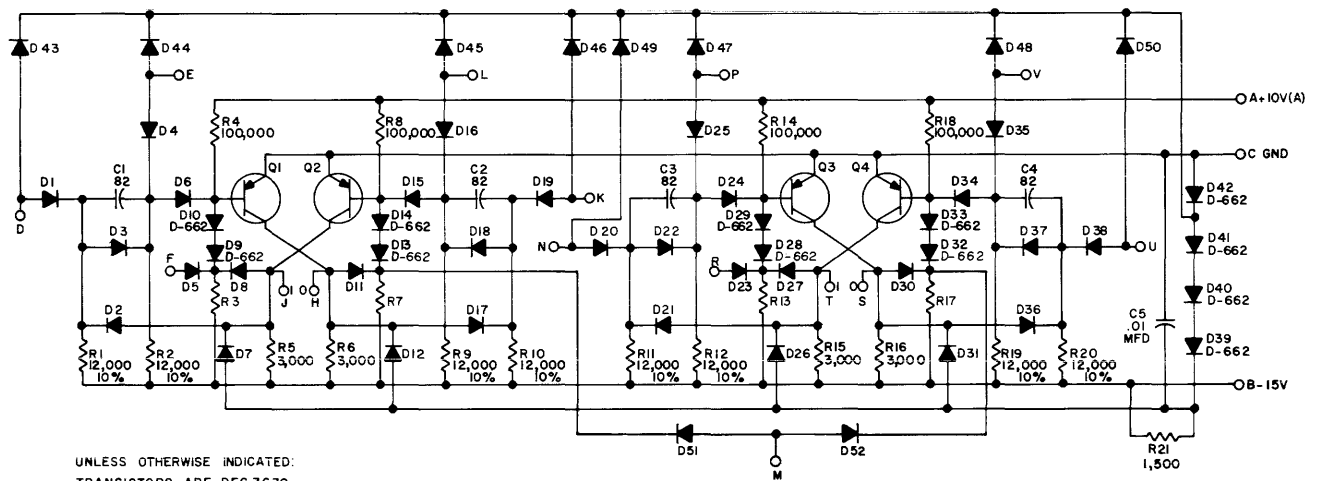


Figure 8-7 DC Carry Chain (RS-B-S181)

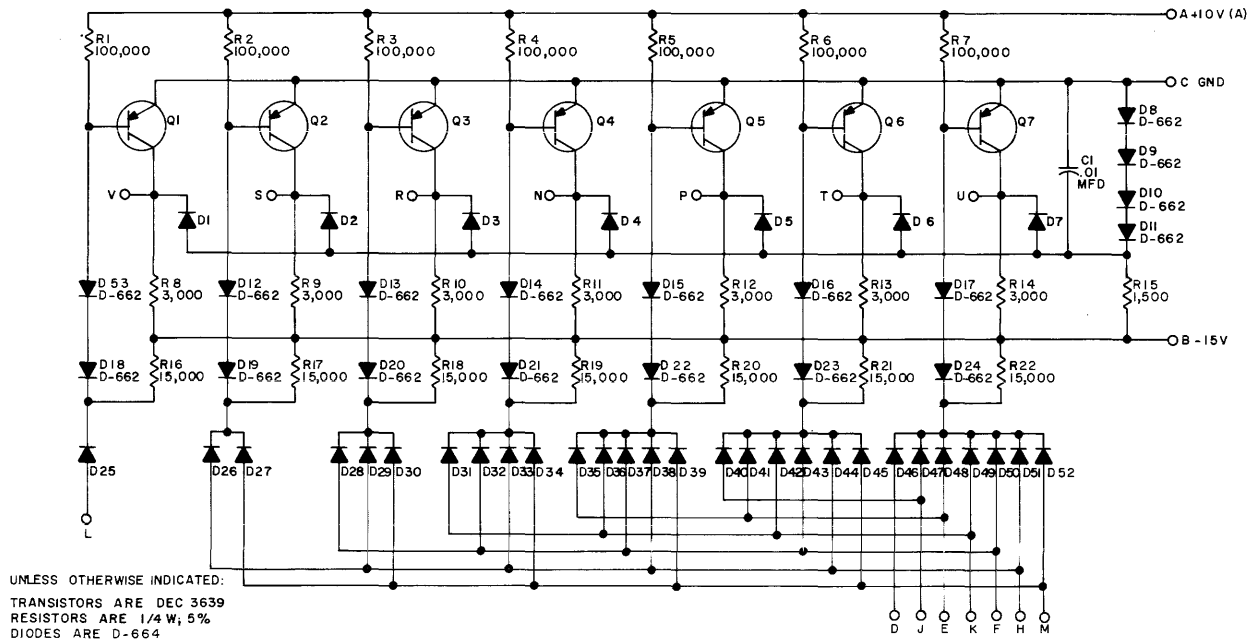


Figure 8-8 Dual Flip-Flop (CS-B-S202)

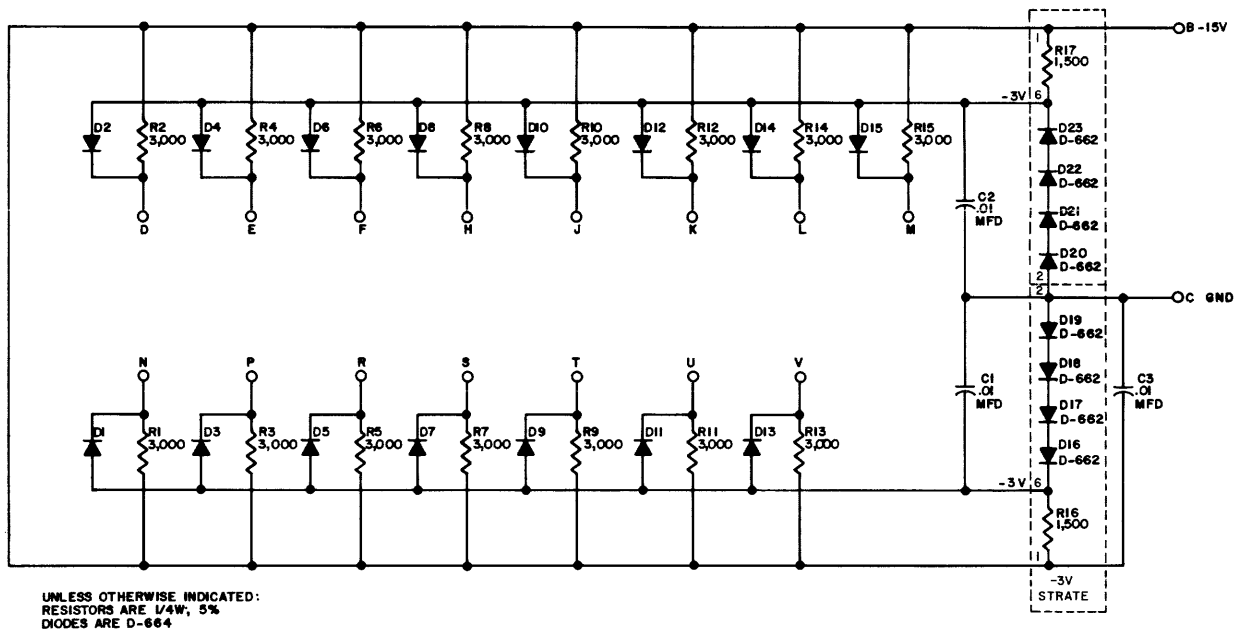


Figure 8-9 Clamped Loads (CS-B-W005)

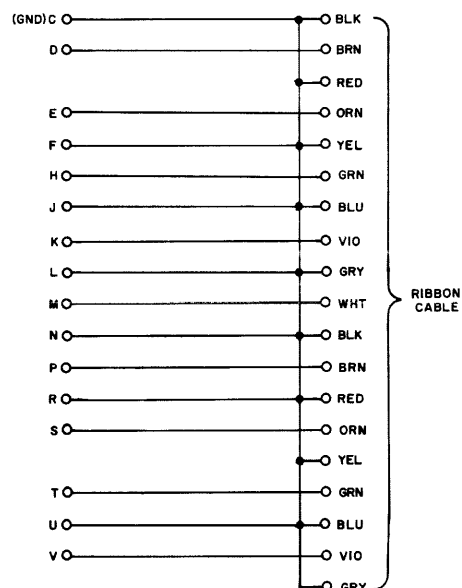


Figure 8-10 Signal Cable Connector (RS-B-W021)

Figure 8-11 Pulse Amplifier (CS-B-W640)

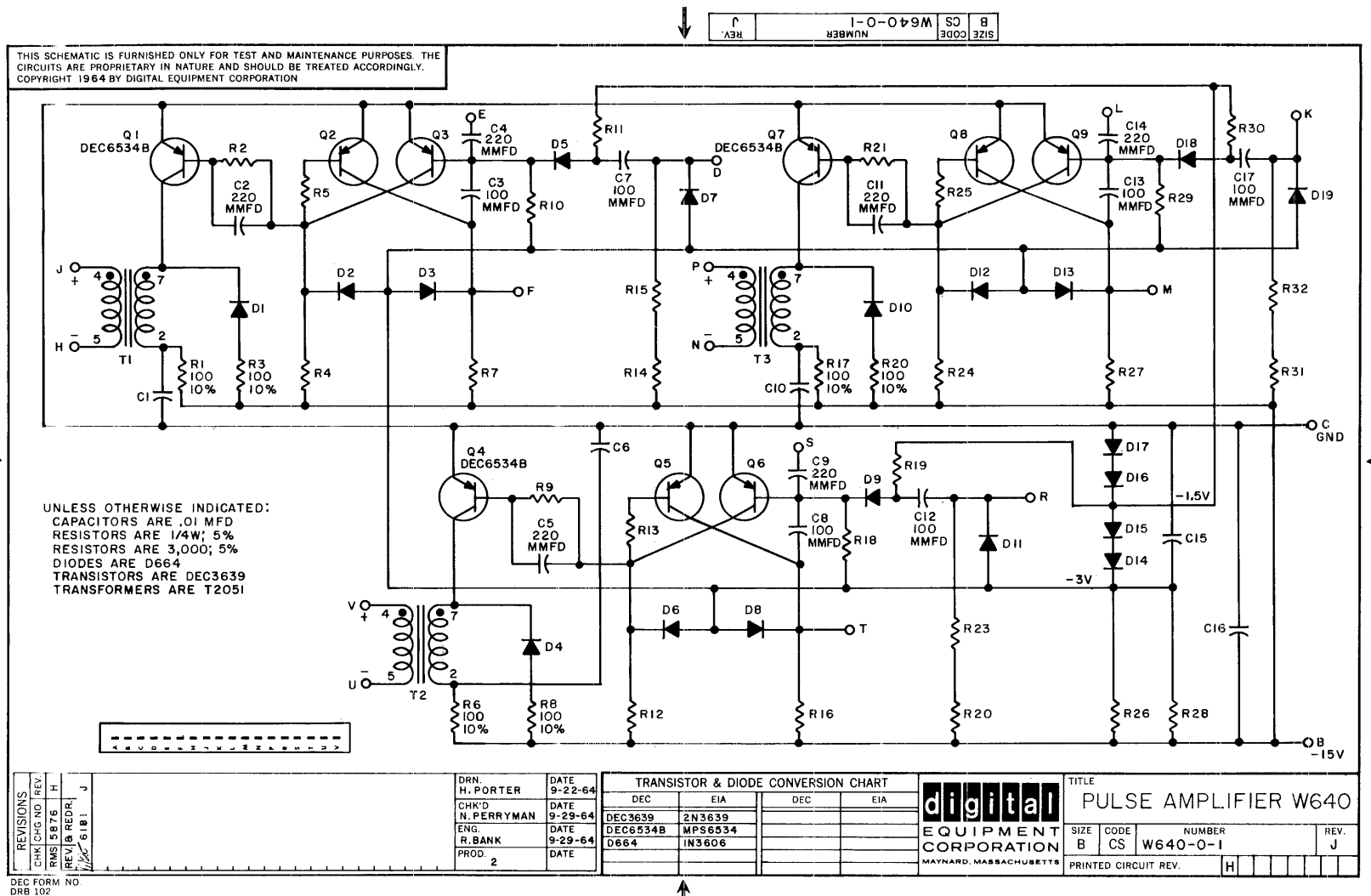


Figure 8-12 Utilization Module List (UML-D-DM01-0-8)

A

B

C

D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
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BAC 0-8	BAC 0-11 IOP 1 IOP 2 IOP 4 T1 PWR CLR	BMB 0-5	BMB 6-11	IM 0-8	IM 9-11 SKIP INT RUM(1) AC CLEAR	DA 0-8	DA 9-11 BRK REQ DATA OUT BREAK(1) ADD, ACC INC MB	DB 0-8	CYC SEL +1→CA INH WCOV	DB 0-11 DF 0(1) DF 1(1) DF 2(1) ADD EXT 1-3	DB SEL DEV 1 DB SEL DEV 2 DB SEL DEV 3 DB SEL DEV 4 DB SEL DEV 5 DB SEL DEV 6	DA SEL DEV 1 DA SEL DEV 2 DA SEL DEV 3 DA SEL DEV 4 DA SEL DEV 5 DA SEL DEV 6	WCOV -2	WCOV -5	WCOV -8	WCOV -3	WCOV -5	BREAK IN PROGRESS				DA(0-8) 5	DA(9-11) 5	DB(0-8) 5	DB(9-11) 5	DF 0(1) DF 1(1) DF 2(1)	BRK REQ 5 DATA OUT 5 B MPX 5 ADD ACC 5 INC MB	CYC SEL-5 +1→CA INH -5 WCOV-5	DAEX (1-3) 5	BRK REQ 6 DATA OUT 6 B MPX 6 ADD ACC 6 INC MB	CYC SEL-6 +1→CA INH -6 WCOV-6	DAEX (1-3) 6																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
MPX 0	SET ENABLE 0-6	DB SEL DEV 2 DB SEL DEV 1	0	8	MPX 0	DA 0	8	MPX 3	DA 1	8	MPX 3	DA 2	8	MPX 4	DA 3	8	MPX 5	DA 4	8	MPX 6	DA 5	8	MPX 7	DA 6	8	MPX 8	DA 7	8	MPX 9	DA 8	8	MPX 10	DA 9	8	MPX 11	DA 10	8	MPX 12	DA 11	8	MPX 13	DA 12	8	MPX 14	DA 13	8	MPX 15	DA 14	8	MPX 16	DA 15	8	MPX 17	DA 16	8	MPX 18	DA 17	8	MPX 19	DA 18	8	MPX 20	DA 19	8	MPX 21	DA 20	8	MPX 22	DA 21	8	MPX 23	DA 22	8	MPX 24	DA 23	8	MPX 25	DA 24	8	MPX 26	DA 25	8	MPX 27	DA 26	8	MPX 28	DA 27	8	MPX 29	DA 28	8	MPX 30	DA 29	8	MPX 31	DA 30	8	MPX 32	DA 31	8	MPX 33	DA 32	8	MPX 34	DA 33	8	MPX 35	DA 34	8	MPX 36	DA 35	8	MPX 37	DA 36	8	MPX 38	DA 37	8	MPX 39	DA 38	8	MPX 40	DA 39	8	MPX 41	DA 40	8	MPX 42	DA 41	8	MPX 43	DA 42	8	MPX 44	DA 43	8	MPX 45	DA 44	8	MPX 46	DA 45	8	MPX 47	DA 46	8	MPX 48	DA 47	8	MPX 49	DA 48	8	MPX 50	DA 49	8	MPX 51	DA 50	8	MPX 52	DA 51	8	MPX 53	DA 52	8	MPX 54	DA 53	8	MPX 55	DA 54	8	MPX 56	DA 55	8	MPX 57	DA 56	8	MPX 58	DA 57	8	MPX 59	DA 58	8	MPX 60	DA 59	8	MPX 61	DA 60	8	MPX 62	DA 61	8	MPX 63	DA 62	8	MPX 64	DA 63	8	MPX 65	DA 64	8	MPX 66	DA 65	8	MPX 67	DA 66	8	MPX 68	DA 67	8	MPX 69	DA 68	8	MPX 70	DA 69	8	MPX 71	DA 70	8	MPX 72	DA 71	8	MPX 73	DA 72	8	MPX 74	DA 73	8	MPX 75	DA 74	8	MPX 76	DA 75	8	MPX 77	DA 76	8	MPX 78	DA 77	8	MPX 79	DA 78	8	MPX 80	DA 79	8	MPX 81	DA 80	8	MPX 82	DA 81	8	MPX 83	DA 82	8	MPX 84	DA 83	8	MPX 85	DA 84	8	MPX 86	DA 85	8	MPX 87	DA 86	8	MPX 88	DA 87	8	MPX 89	DA 88	8	MPX 90	DA 89	8	MPX 91	DA 90	8	MPX 92	DA 91	8	MPX 93	DA 92	8	MPX 94	DA 93	8	MPX 95	DA 94	8	MPX 96	DA 95	8	MPX 97	DA 96	8	MPX 98	DA 97	8	MPX 99	DA 98	8	MPX 100	DA 99	8	MPX 101	DA 100	8	MPX 102	DA 101	8	MPX 103	DA 102	8	MPX 104	DA 103	8	MPX 105	DA 104	8	MPX 106	DA 105	8	MPX 107	DA 106	8	MPX 108	DA 107	8	MPX 109	DA 108	8	MPX 110	DA 109	8	MPX 111	DA 110	8	MPX 112	DA 111	8	MPX 113	DA 112	8	MPX 114	DA 113	8	MPX 115	DA 114	8	MPX 116	DA 115	8	MPX 117	DA 116	8	MPX 118	DA 117	8	MPX 119	DA 118	8	MPX 120	DA 119	8	MPX 121	DA 120	8	MPX 122	DA 121	8	MPX 123	DA 122	8	MPX 124	DA 123	8	MPX 125	DA 124	8	MPX 126	DA 125	8	MPX 127	DA 126	8	MPX 128	DA 127	8	MPX 129	DA 128	8	MPX 130	DA 129	8	MPX 131	DA 130	8	MPX 132	DA 131	8	MPX 133	DA 132	8	MPX 134	DA 133	8	MPX 135	DA 134	8	MPX 136	DA 135	8	MPX 137	DA 136	8	MPX 138	DA 137	8	MPX 139	DA 138	8	MPX 140	DA 139	8	MPX 141	DA 140	8	MPX 142	DA 141	8	MPX 143	DA 142	8	MPX 144	DA 143	8	MPX 145	DA 144	8	MPX 146	DA 145	8	MPX 147	DA 146	8	MPX 148	DA 147	8	MPX 149	DA 148	8	MPX 150	DA 149	8	MPX 151	DA 150	8	MPX 152	DA 151	8	MPX 153	DA 152	8	MPX 154	DA 153	8	MPX 155	DA 154	8	MPX 156	DA 155	8	MPX 157	DA 156	8	MPX 158	DA 157	8	MPX 159	DA 158	8	MPX 160	DA 159	8	MPX 161	DA 160	8	MPX 162	DA 161	8	MPX 163	DA 162	8	MPX 164	DA 163	8	MPX 165	DA 164	8	MPX 166	DA 165	8	MPX 167	DA 166	8	MPX 168	DA 167	8	MPX 169	DA 168	8	MPX 170	DA 169	8	MPX 171	DA 170	8	MPX 172	DA 171	8	MPX 173	DA 172	8	MPX 174	DA 173	8	MPX 175	DA 174	8	MPX 176	DA 175	8	MPX 177	DA 176	8	MPX 178	DA 177	8	MPX 179	DA 178	8	MPX 180	DA 179	8	MPX 181	DA 180	8	MPX 182	DA 181	8	MPX 183	DA 182	8	MPX 184	DA 183	8	MPX 185	DA 184	8	MPX 186	DA 185	8	MPX 187	DA 186	8	MPX 188	DA 187	8	MPX 189	DA 188	8	MPX 190	DA 189	8	MPX 191	DA 190	8	MPX 192	DA 191	8	MPX 193	DA 192	8	MPX 194	DA 193	8	MPX 195	DA 194	8	MPX 196	DA 195	8	MPX 197	DA 196	8	MPX 198	DA 197	8	MPX 199	DA 198	8	MPX 200	DA 199	8	MPX 201	DA 200	8	MPX 202	DA 201	8	MPX 203	DA 202	8	MPX 204	DA 203	8	MPX 205	DA 204	8	MPX 206	DA 205	8	MPX 207	DA 206	8	MPX 208	DA 207	8	MPX 209	DA 208	8	MPX 210	DA 209	8	MPX 211	DA 210	8	MPX 212	DA 211	8	MPX 213	DA 212	8	MPX 214	DA 213	8	MPX 215	DA 214	8	MPX 216	DA 215	8	MPX 217	DA 216	8	MPX 218	DA 217	8	MPX 219	DA 218	8	MPX 220	DA 219	8	MPX 221	DA 220	8	MPX 222	DA 221	8	MPX 223	DA 222	8	MPX 224	DA 223	8	MPX 225	DA 224	8	MPX 226	DA 225	8	MPX 227	DA 226	8	MPX 228	DA 227	8	MPX 229	DA 228	8	MPX 230	DA 229	8	MPX 231	DA 230	8	MPX 232	DA 231	8	MPX 233	DA 232	8	MPX 234	DA 233	8	MPX 235	DA 234	8	MPX 236	DA 235	8	MPX 237	DA 236	8	MPX 238	DA 237	8	MPX 239	DA 238	8	MPX 240	DA 239	8	MPX 241	DA 240	8	MPX 242	DA 241	8	MPX 243	DA 242	8	MPX 244	DA 243	8	MPX 245	DA 244	8	MPX 246	DA 245	8	MPX 247	DA 246	8	MPX 248	DA 247	8	MPX 249	DA 248	8	MPX 250	DA 249	8	MPX 251	DA 250	8	MPX 252	DA 251	8	MPX 253	DA 252	8	MPX 254	DA 253	8	MPX 255	DA 254	8	MPX 256	DA 255	8	MPX 257	DA 256	8	MPX 258	DA 257	8	MPX 259	DA 258	8	MPX 260	DA 259	8	MPX 261	DA 260	8	MPX 262	DA 261	8	MPX 263	DA 262	8	MPX 264	DA 263	8	MPX 265	DA 264	8	MPX 266	DA 265	8	MPX 267	DA 266	8	MPX 268	DA 267	8	MPX 269	DA 268	8	MPX 270	DA 269	8	MPX 271	DA 270	8	MPX 272	DA 271	8	MPX 273	DA 272	8	MPX 274	DA 273	8	MPX 275	DA 274	8	MPX 276	DA 275	8	MPX 277	DA 276	8	MPX 278	DA 277	8	MPX 279	DA 278	8	MPX 280	DA 279	8	MPX 281	DA 280	8	MPX 282	DA 281	8	MPX 283	DA 282	8	MPX 284	DA 283	8	MPX 285	DA 284	8	MPX 286	DA 285	8	MPX 287	DA 286	8	MPX 288	DA 287	8	MPX 289	DA 288	8	MPX 290	DA 289	8	MPX 291	DA 290	8	MPX 292	DA 291	8	MPX 293	DA 292	8	MPX 294	DA 293	8	MPX 295	DA 294	8	MPX 296	DA 295	8	MPX 297	DA 296	8	MPX 298	DA 297	8	MPX 299	DA 298	8	MPX 300	DA 299	8	MPX 301	DA 300	8	MPX 302	DA 301	8	MPX 303	DA 302	8	MPX 304	DA 303	8	MPX 305	DA 304	8	MPX 306	DA 305	8	MPX 307	DA 306	8	MPX 308	DA 307	8	MPX 309	DA 308	8	MPX 310	DA 309	8	MPX 311	DA 310	8	MPX 312	DA 311	8	MPX 313	DA 312	8	MPX 314	DA 313	8	MPX 315	DA 314	8	MPX 316	DA 315	8	MPX 317	DA 316	8	MPX 318	DA 317	8	MPX 319	DA 318	8	MPX 320	DA 319	8	MPX 321	DA 320	8	MPX 322	DA 321	8	MPX 323	DA 322	8	MPX 324	DA 323	8	MPX 325	DA 324	8	MPX 326	DA 325	8	MPX 327	DA 326	8	MPX 328	DA 327	8	MPX 329	DA 328	8	MPX 330	DA 329	8	MPX 331	DA 330	8	MPX 332	DA 331	8	MPX 333	DA 332	8	MPX 334	DA 333	8	MPX 335	DA 334	8	MPX 336	DA 335	8	MPX 337	DA 336	8	MPX 338	DA 337	8	MPX 339	DA 338	8	MPX 340	DA 339	8	MPX 341	DA 340	8	MPX 342	DA 341	8	MPX 343	DA 342	8	MPX 344	DA 343	8	MPX 345	DA 344	8	MPX 346	DA 345	8	MPX 347	DA 346	8	MPX 348	DA 347	8	MPX 349	DA 348	8	MPX 350	DA 349	8	MPX 351	DA 350	8	MPX 352	DA 351	8	MPX 353	DA 352	8	MPX 354	DA 353	8	MPX 355	DA 354	8	MPX 356	DA 355	8	MPX 357	DA 356	8	MPX 358	DA 357	8	MPX 359	DA 358	8	MPX 360	DA 359	8	MPX 361	DA 360	8	MPX 362	DA 361	8	MPX 363	DA 362	8	MPX 364	DA 363	8	MPX 365	DA 364	8	MPX 366	DA 365	8	MPX 367	DA 366	8	MPX 368	DA 367	8	MPX 369	DA 368	8	MPX 370	DA 369	8	MPX 371	DA 370	8	MPX 372	DA 371	8	MPX 373	DA 372	8	MPX 374	DA 373	8	MPX 375	DA 374	8	MPX 376	DA 375	8	MPX 377	DA 376	8	MPX 378	DA 377	8	MPX 379	DA 378	8	MPX 380	DA 379	8	MPX 381	DA 380	8	MPX 382	DA 381	8	MPX 383	DA 382	8	MPX 384	DA 383	8	MPX 385	DA 384	8	MPX 386	DA 385	8	MPX 387	DA 386	8	MPX 388	DA 387	8	MPX 389	DA 388	8	MPX 390	DA 389	8	MPX 391	DA 390	8	MPX 392	DA 391	8	MPX 393	DA 392	8	MPX 394	DA 393	8	MPX 395	DA 394	8	MPX 396	DA 395	8	MPX 397	DA 396	8	MPX 398	DA 397	8	MPX 399	DA 398	8	MPX 400	DA 399	8	MPX 401	DA 400	8	MPX 402	DA 401	8	MPX 403	DA 402	8	MPX 404	DA 403	8	MPX 405	DA 404	8	MPX 406	DA 405	8	MPX 407	DA 406	8	MPX 408	DA 407	8	MPX 409	DA 408	8	MPX 410	DA 409	8	MPX 411	DA 410	8	MPX 412	DA 411	8	MPX 413

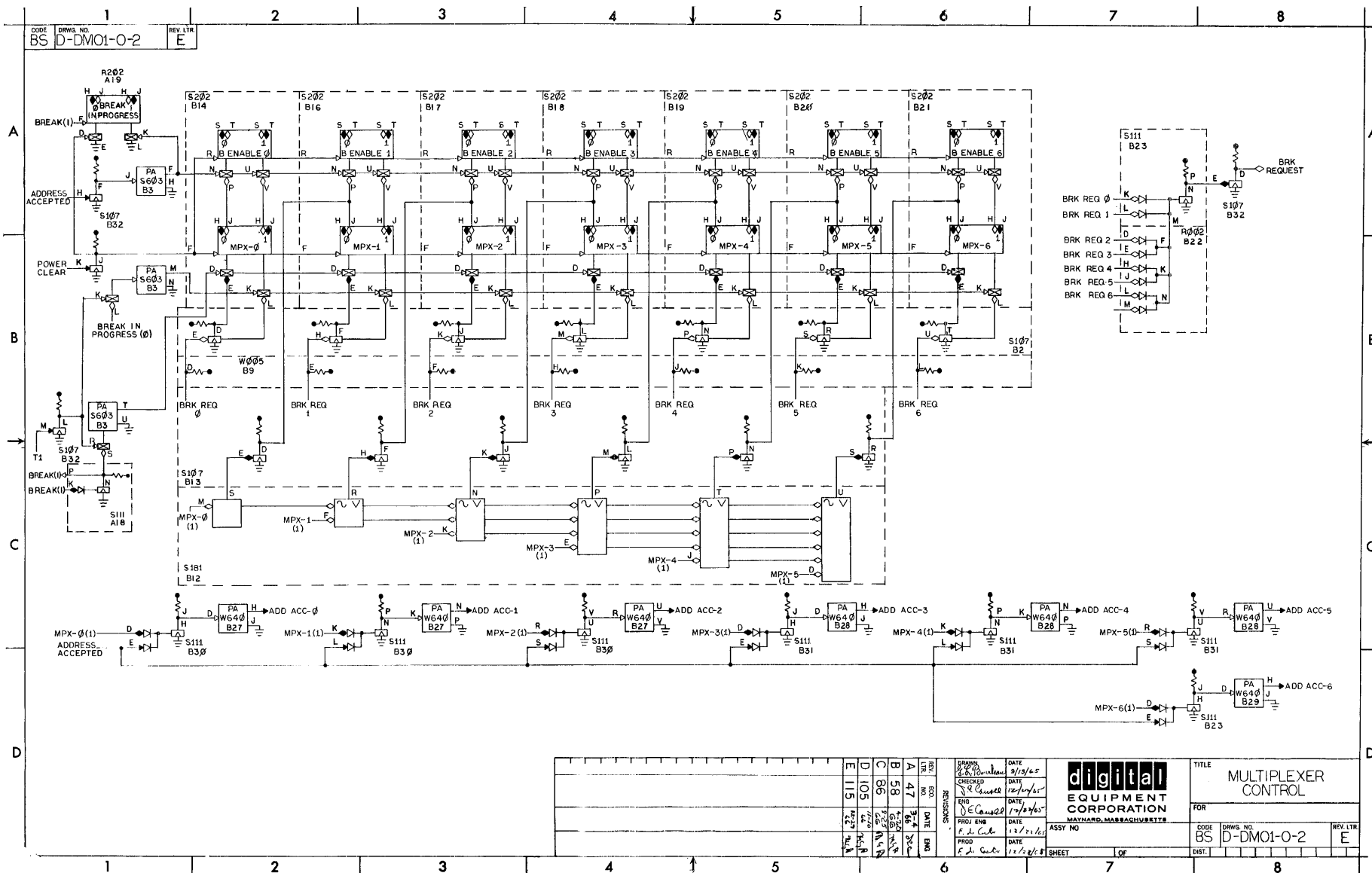


Figure 8-14 Level Production from Multiplexer Control (BS-D-DM01-0-11)

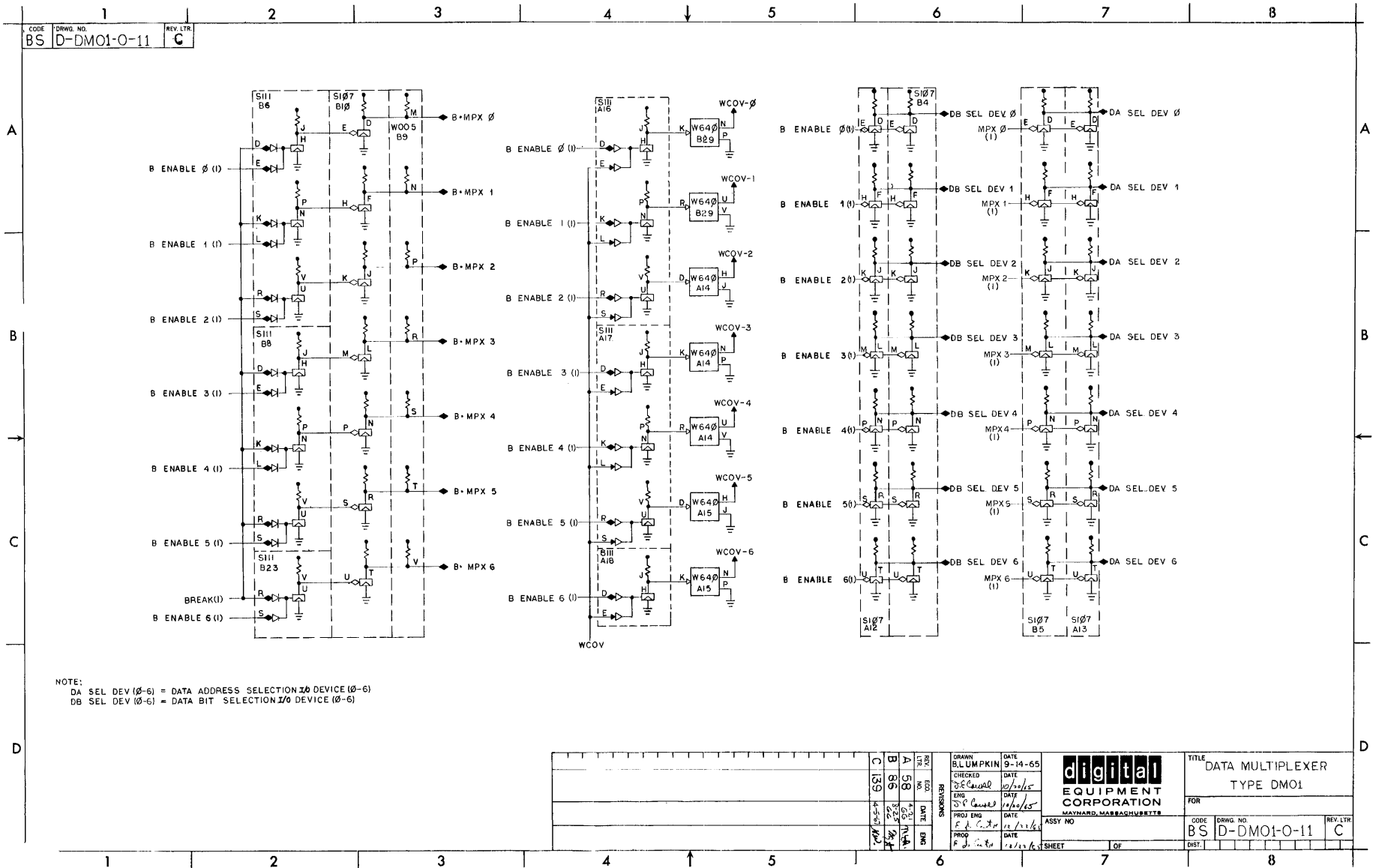


Figure 8-15 Data Address Line Selector (BS-D-DM01-0-4)
8-15

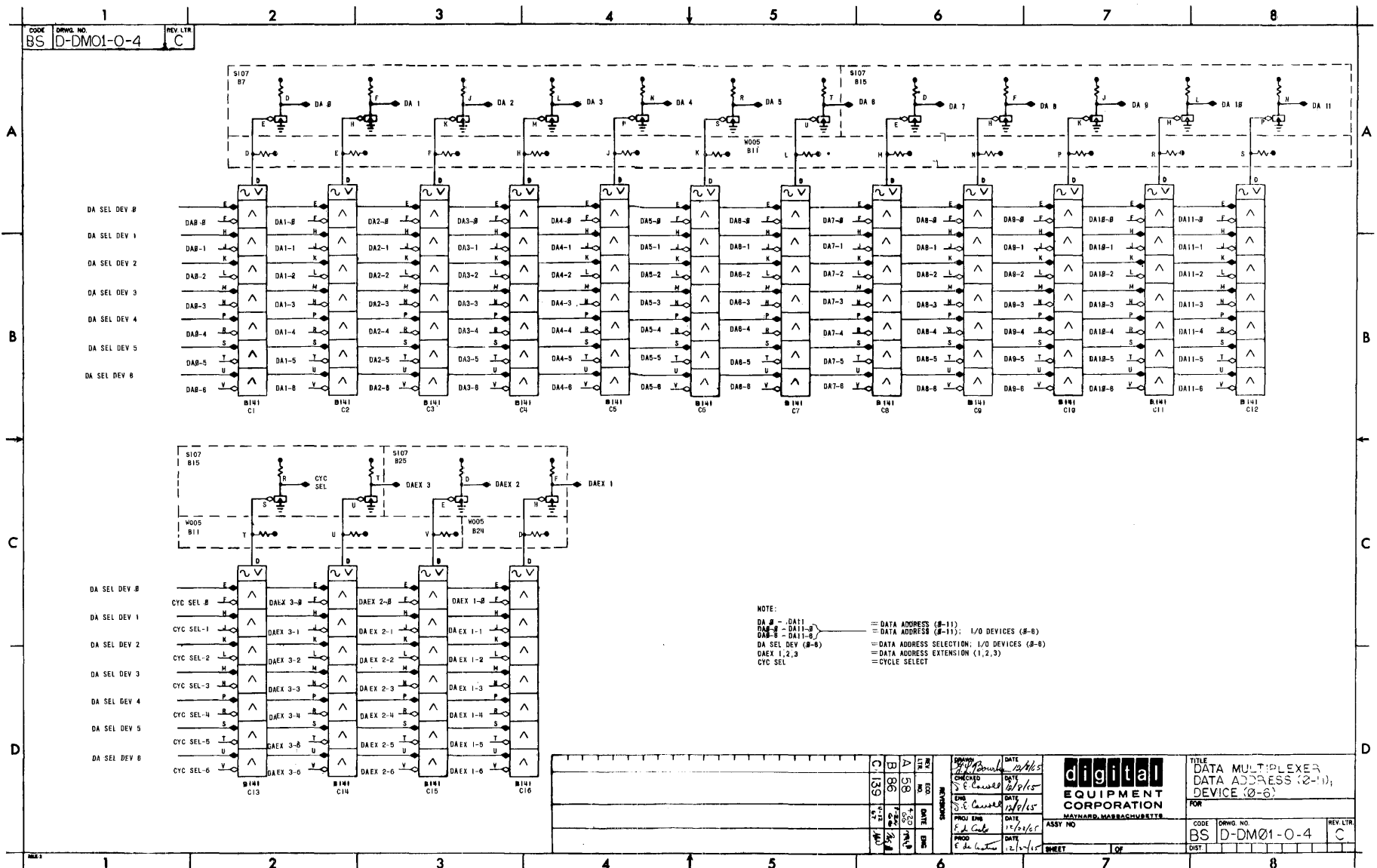
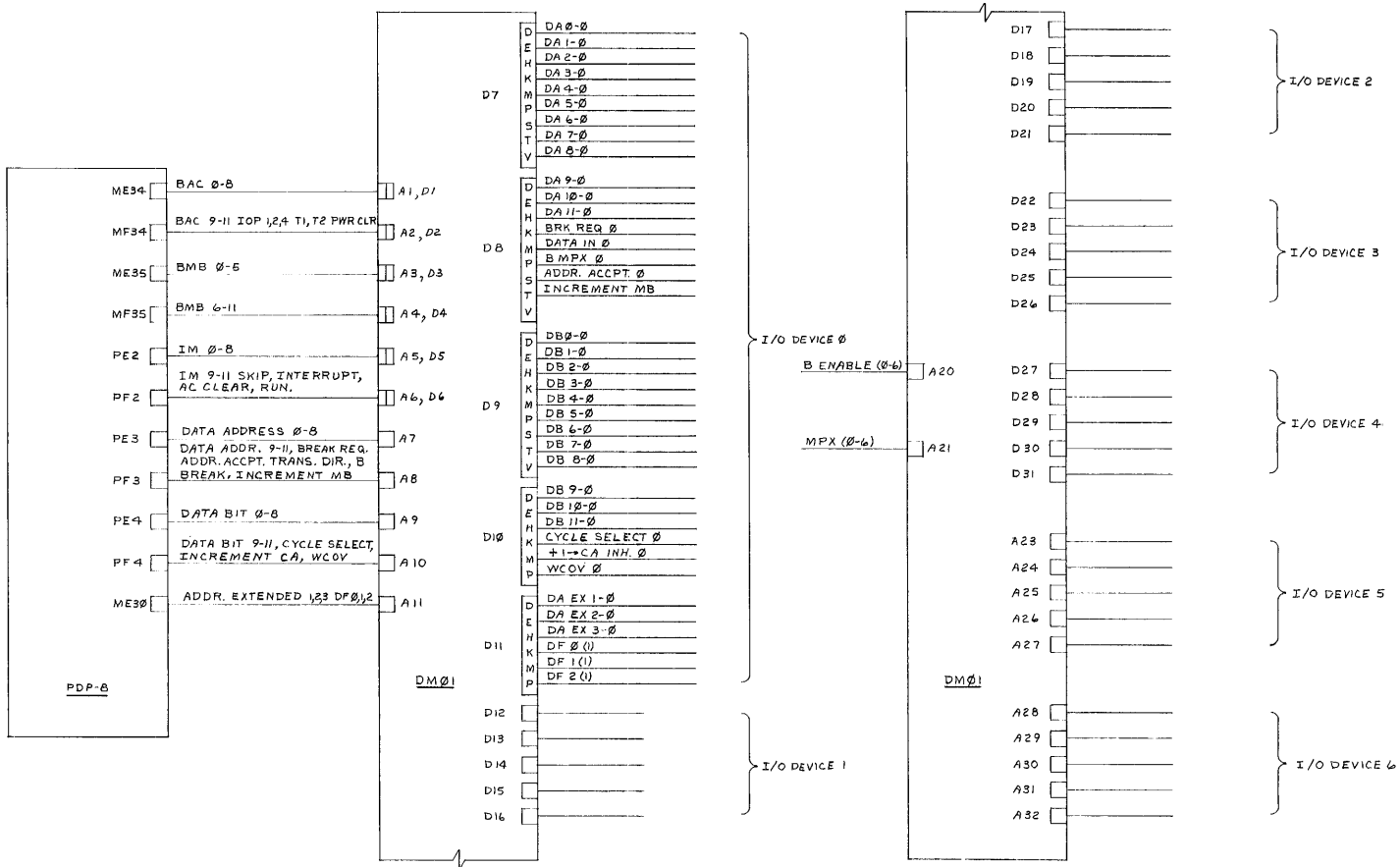
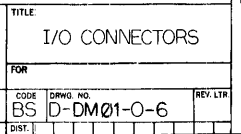


Figure 8-17 DM01 Interconnecting Cable Diagram (IC-DM01-0-13)





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