INSTRUCTION MANUAL

SERIAL DRUM SYSTEM
TYPE RM08

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-08-I5AA-D

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TYPE RM08
INSTRUCTION MANUAL

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CHAPTER 1
INTRODUCTION

This manual describes the operation of and provides maintenance information on the Digital Equipment Corporation Type RM08 Serial Drum System.

1.1 PURPOSE

The Type RM08 Serial Drum System is used in conjunction with the Programmed Data Processor-8 (PDP-8) as an auxiliary data storage device. Information in the PDP-8 can be stored in the RM08 drum and retrieved in sectors of 16 computer words. Sectors are automatically transferred between the PDP-8 core memory and the drum after program initialization. Transfer of each word is interleaved with the running computer program under control of the PDP-8 data break facilities. A word is transferred in parallel (12 bits at a time) and is read from or written onto the surface of the rotating drum in serial fashion (one bit at a time).

Words within the drum system consist of 12 information bits and a parity bit. Parity bits are generated internally when writing, and are checked when reading. The drum system has 64 tracks - each track holds 64 sectors of 16 13-bit words. The storage capability can be expanded to 256 tracks (262,144 words).

1.2 PHYSICAL DESCRIPTION

The Type RM08 Serial Drum System is contained in a DEC computer cabinet 23-1/2 in. wide, 27-1/16 in. deep, and 69-1/8 in. high. All indicators are located on a panel at the front of the machine.

A coordinate system is used to locate racks, modules, cable connectors and terminals. Each 5-1/4 in. position on the front of the cabinet is assigned a capital letter beginning with A at the top, as indicated in Figure 1-1. Modules are numbered from 1 through 25 from left to right in a rack, as viewed from the wiring side (front). Connectors are numbered from 1 through 6 from left to right, as viewed from the front of the machine. Blank-module and connector locations are not numbered, and terminals on a module connector are designated by capital letters from top to bottom. For example, D09E is the fourth location from the top (D), the ninth module from the left (09), and the fifth terminal from the top of the module. Engineering drawing D-RM08-0-6 (Chapter 7) shows the module types used in racks 1C, 1D, and 1E.

Table 1-1 lists the specifications for the Type RM08 Serial Drum System.

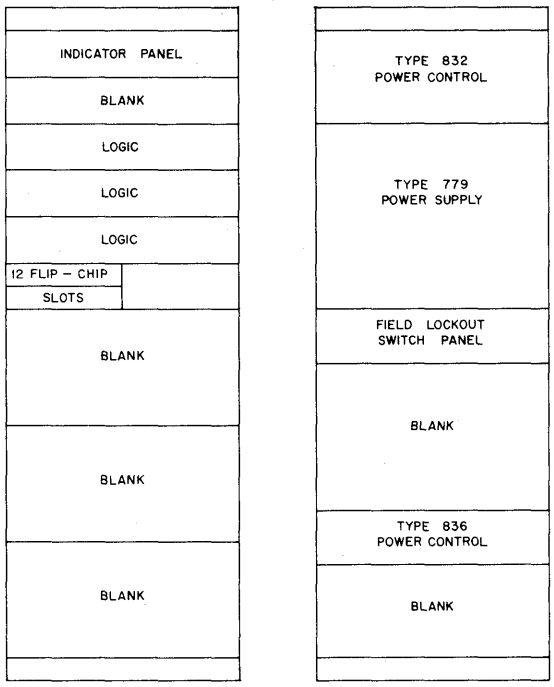


Figure 1-1 Component Location-RM08

Table 1-1
Specifications

Dimensions:

23-1/2 in. wide
27-1/16 in. deep
69-1/8 in. high

Service Clearances:

8-3/4 in. front
14-7/8 in. rear

Weight:

500 lb.

Power Requirements:

115V, 60 c/s, single phase	240V, 50 c/s, single phase
8A starting current	4A starting current
5A running current	2.5A running current

Power Control Point:

Local or remote (computer)

Signal Cables:

11 10-ft, 9-conductor coaxial cables with W021 connectors

Table 1-1 (continued)
Specifications

Ambient Temperature:

60°F to 100°F

Initial Starting Delay:

5 min.

Drum Motor:

115V or 245V, single phase, 2 pole, induction, capacitor start and run

Write Current:

120 mA

Drum Speed:

3600 rpm (60 c/s)
3000 rpm (50 c/s)

Word Transfer Time:

15.6 μs (3600 rpm)
19.5 μs (3000 rpm)

Sector Transfer Cycle:

250 μs (3600 rpm)
313 μs (3000 rpm)

Access Time:

8.65 ms (17.3 ms max at 3600 rpm)
10.3 ms (20.5 ms max at 3000 rpm)

1.3 ABBREVIATIONS

The following abbreviations are used in text throughout this manual and on the engineering drawings of Chapter 7.

Abbreviation	Definition	Abbreviation	Definition
AC	Accumulator in computer	DDC	Drum data channel in serial drum
ACT	Active	DE	Data error
AMP	Amplifier	DF and DFB	Drum final buffer in serial drum
COND	Condition	DS	Device selector in serial drum
CLR	Clear	DSA	Drum sector address
DCL	Drum core location counter in serial drum	DTA	Drum track address
DCT	Drum control element in serial drum	INT	Interrupt control in computer

Abbreviation	Definition	Abbreviation	Definition
IOT	Input/Output transfer	PE	Parity error
MA and MAR	Memory address register in computer	PG	Pulse generator
		RQ	Request flip-flop
MB	Memory buffer register in computer	R PARITY	Read/write parity flip-flop in serial drum
PA	Pulse amplifier	SC	Sector counter in serial drum
PAR	Parity	SA	Sector address
DSB CONTROL	Drum serial buffer control (-3V source)	TRA	Transfer

1.4 ASSOCIATED PUBLICATIONS

The following documents are pertinent to the RM08 Serial Drum Systems.

PDP-8 Users Handbook,
PDP-8 Maintenance Manual,
Systems Modules Catalog, C-100
FLIP-CHIP Modules Catalog, C-105

CHAPTER 2
PRINCIPLES OF OPERATION

2.1 FUNCTIONAL DESCRIPTION

The major functional areas of the Type RM08 Serial Drum System are illustrated in Figure 2-1 and are described in the following paragraphs. Detailed engineering diagrams for the serial drum logic are contained in Chapter 7. The references in text are to the engineering drawing numbers. Complete information transfer flow is illustrated in Dwg. No. D-RM08-0-23.

2.1.1 Device Selector

During the execution of an IOT instruction, the device selector receives MB bits 3 through 8 and the IOP1, IOP2, and IOP4 pulses from the computer. The internal structure of the device selector, which consists of three Type 4605 modules, permits it to generate the IOT pulses which control the drum circuits during an IOT instruction. The device selector is shown in the lower right-hand corner of Dwg. No. D-RM08-0-4.

2.1.2 Drum Core Location Counter (DCL)

The drum core location counter (Dwg. No. D-RM08-0-5) is a 15-bit register which addresses the next core location to or from which the next word is to be transferred. Prior to transfer of the initial word in a block, the address of the first word is set into the DCL under program control from the computer accumulator. As each word is transferred, the DCL is incremented by one.

2.1.3 Drum Track (DTA) and Sector Address (DSA) Registers

The DTA and DSA registers (Dwg. No. D-RM08-0-5) comprise a 14-bit register (8 tracks and 6 sectors) which addresses the drum track and sector which is currently transferring data. Upon completion of a successful last sector transfer (error flag is 0), these registers are incremented by one.

2.1.4 Drum Field and Sector Number Registers

The drum field register is a 2-bit register which holds the drum field. The sector number register is a 6-bit register specifying the number of sectors to be transferred. The contents of these registers can only be changed by an IOT. The drum field register is a 2-bit register which specifies one of four drum fields (64K words per field) to which the data will be transferred. These registers are shown in (Dwg. No. D-RM08-0-3).

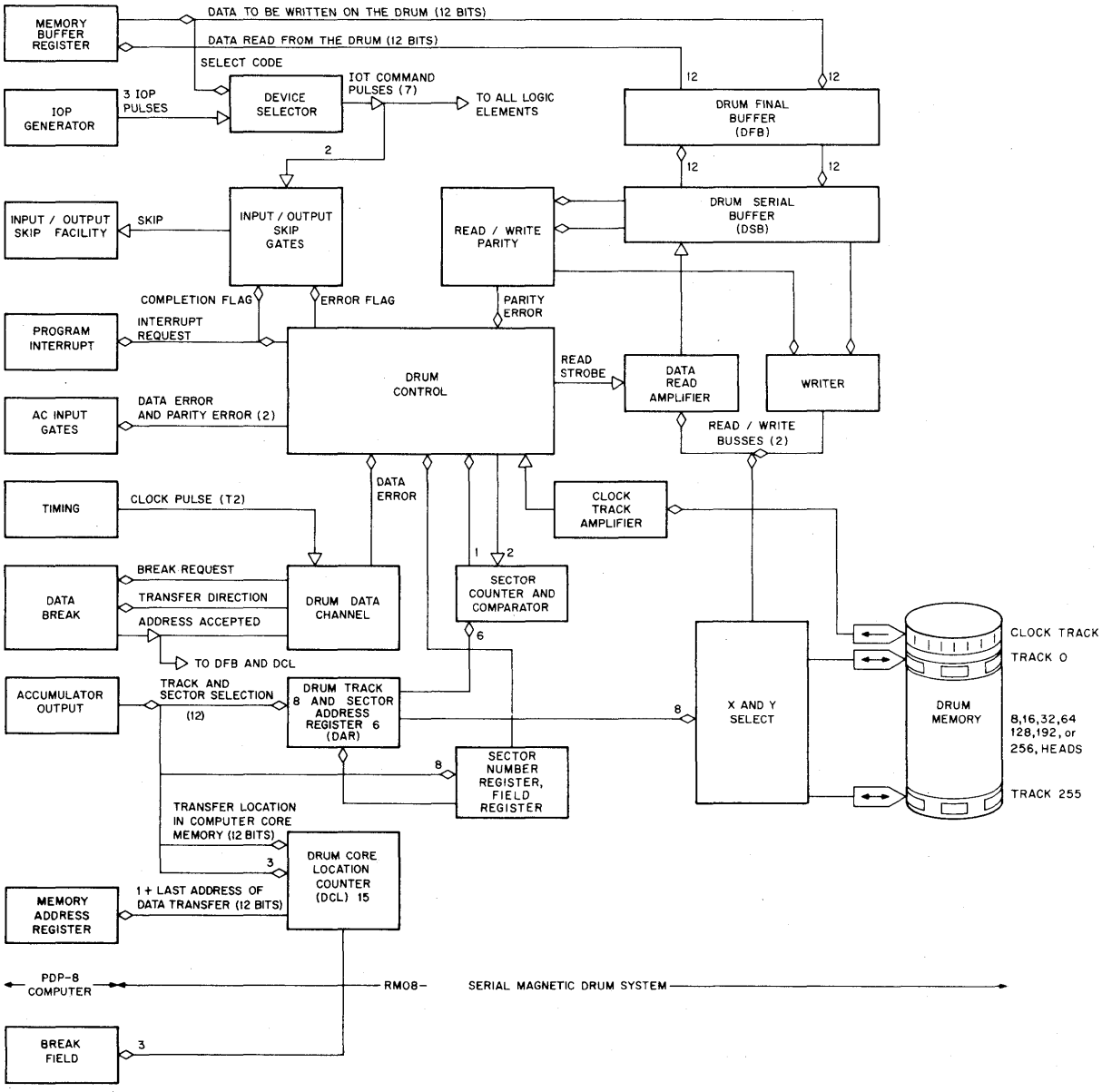


Figure 2-1 Type RM08 Functional Diagram

2.1.5 Sector Number Counter

The sector number counter (Dwg. No. D-RM08-0-21) is a 7-bit counter which contains the 2s complement of the sector number register. The number of sectors transferred is counted, and any overflow produces a flag interrupt condition. The sector counter is a 6-bit counter which is incremented automatically after each sector of clock information.

2.1.6 Drum Final Buffer (DFB)

The drum final buffer (Dwg. No. E-RM08-0-3) is a 12-bit register under control of the data break facility which is a buffer between the memory buffer register and the drum serial buffer. During write-in, the DFB holds the next word to be written. During read-out, the DFB stores the word read from the drum until it is transferred to the PDP-8.

2.1.7 Drum Serial Buffer (DSB)

The drum serial buffer (Dwg. No. E-RM08-0-3) is a 14-bit register which contains a data word and two control bits. This register serves as a serial-to-parallel converter during read-out, and as a parallel-to-serial converter during write-in. Information is read from the drum into the DSB in serial fashion and is transferred into the DFB in parallel. During write-in, a word is transferred in parallel from the DFB to the DSB and written serially around the drum.

2.1.8 Drum Head Selection

Selection of a drum head is performed in the drum X and Y select circuits (Dwg. No. E-RM08-0-2) and in the diode matrix within the drum housing. The 16 FIELD LOCKOUT switches, when closed, inhibit the X0 and X1 selection modules to prevent writing on certain tracks which may contain data the programmer wishes to preserve. Each switch inhibits writing on four tracks (4096_{10} words).

2.1.9 Drum Control

The basic timing pulses for the machine are generated in the DCT from pulses received from the clock track amplifier. The DCT also contains a 4-stage device consisting of four negative diode gates. Each state of this device corresponds with and initiates one of the machine control states: idle (IDLE), transfer (TRA), active (ACT), or transfer done (COMP FLAG). This logic is shown on Dwg. No. D-RM08-0-4).

2.1.10 Read-Write Parity

As each bit of a word is written on the drum surface, the R PARITY flip-flop counts the number of binary 1's and produces a 13th bit to provide odd parity. When data is read from the drum, this flip-flop again counts the 1's and sets the parity error (PE) flip-flop if an even number is detected in any word. The condition of the PE flip-flop is indicated in the DCT as one of the two possible causes of an error condition. These circuits are shown in area C4 of Dwg. No. E-RM08-0-3.

2.2 RECORDING AND PLAYBACK TECHNIQUE

The recording and playback technique employed in the Type RM08 Serial Drum System is NRZ (non-return-to-zero) phase modulation. This technique records binary 1's and 0's by controlling the direction of flux change on the drum surface. For example, a flux change in one direction represents a 1, and a flux change in the opposite direction represents a 0.

To clarify this point, consider the timing diagram Figure 2-2 and the simplified logic diagram Figure 2-3. As shown on these drawings, a positive voltage swing (identified by the arrow) from the write flip-flop produces a flux change to write a 1, and a negative voltage swing produces a flux change to write a 0. The read/write circuits are synchronized so that recording occurs on the phase A time pulse. The write flip-flop must be in a state so that the phase A pulse can complement the flip-flop to write the specified bit. The phase B pulse shifts the bit to be written into the last bit of the data register, the DSB0 flip-flop. The delayed phase B pulse senses the DSB0 bit to put the write flip-flop in the proper state so that the next phase A pulse complements the write flip-flop to write the bit specified by DSB0.

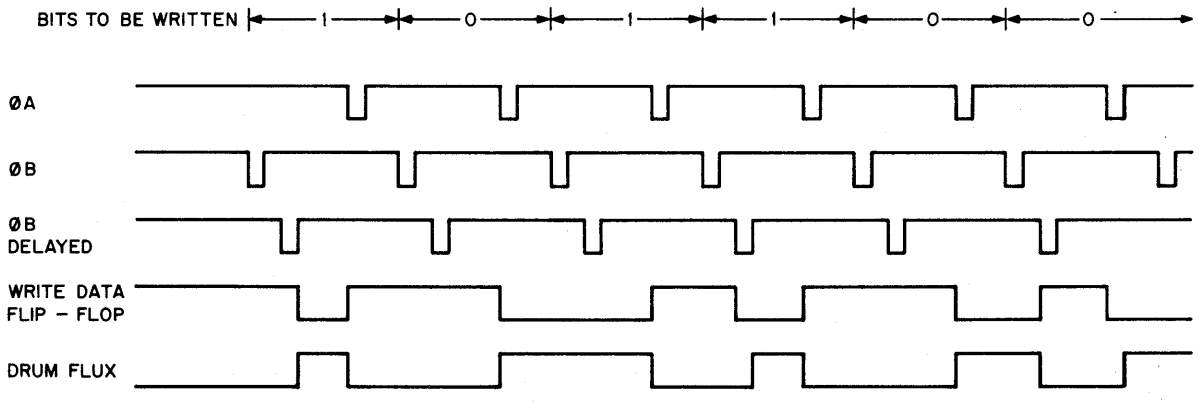


Figure 2-2 Simplified Timing - NRZ Writing

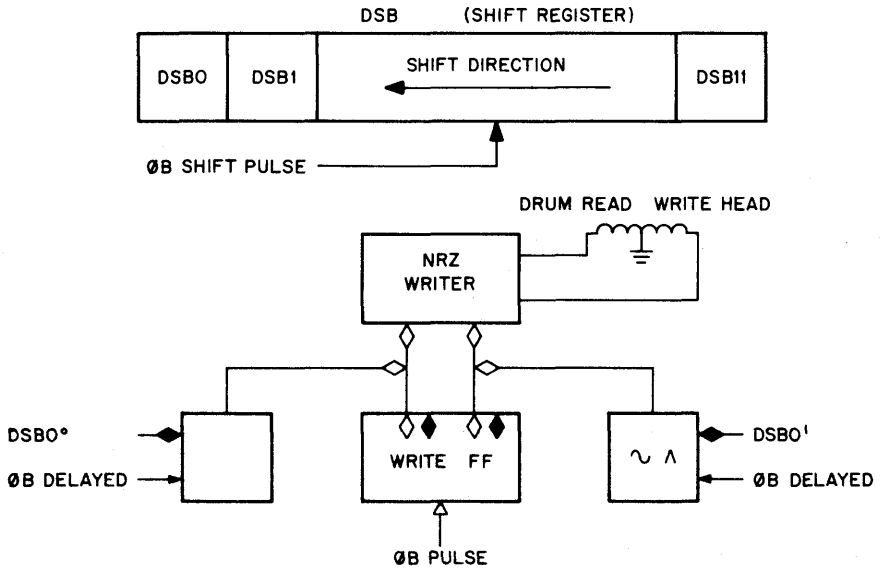


Figure 2-3 Simplified Logic of Writing Circuits

Obviously, when the state of write flip-flop is switched by the delayed phase B pulse, it causes a flux change on the drum surface. This flux change is not sensed, however, as a binary 1 bit because the drum is sensed during playback (reading) for a flux change only at phase A time. Detailed information on the principle of NRZ recording using phase modulation is shown on Figure 2-4.

2.3 DRUM FORMAT

Data from the computer is written on drum tracks that circumscribe the drum cylinder as shown in Figure 2-5. The RM08 has 256 tracks; each data track contains 64 sectors and each sector contains 16 13-bit words (0 through 17 octal). The 13-bit word consists of 12 data bits and a parity bit.

The words within any particular sector are stored consecutively on the track. The first 16 words on the track are for sector 0; the next 16 words for sector 1, etc., as shown in Figure 2-5. The last 16 words on the drum track are words 0 through 17 for sector 77_8. There are 13 clock pulses per word throughout the drum track. The drum also contains a clock pulse track. The clock pulse track supplies clock pulses to the drum control logic at 1.2 μs (60 c/s) intervals to synchronize writing and reading of the drum. There is a 10 μs gap between sectors within each track and a 300 μs gap to separate the beginning and end of each track. A 300 μs gap, where no clock pulses exist, separates the beginning and end of each track.

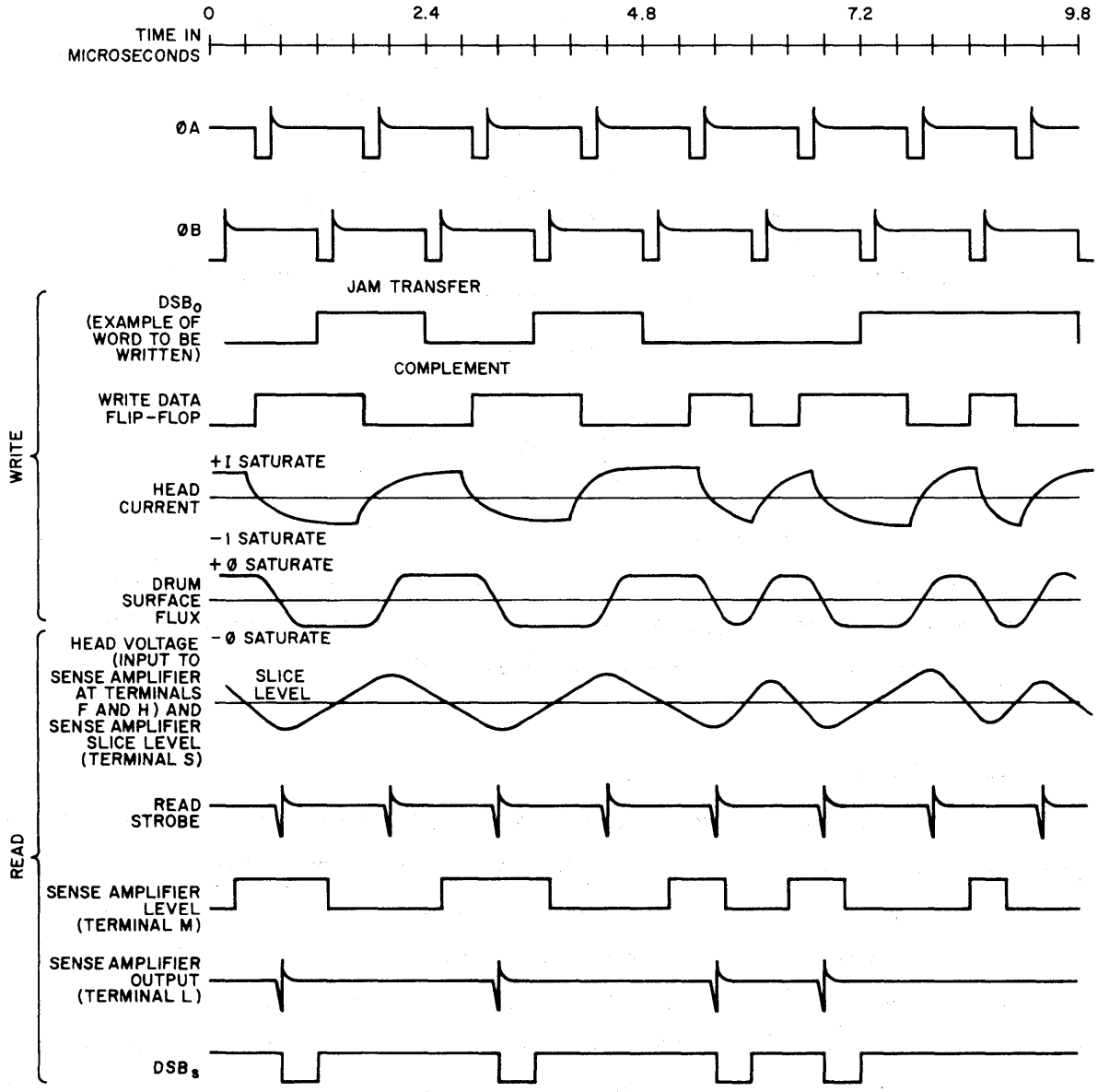
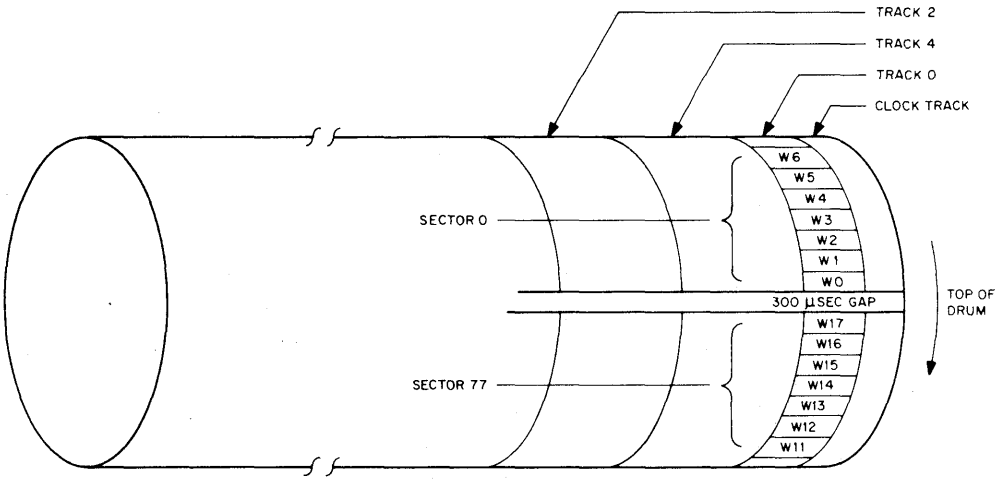


Figure 2-4 Typical Recording and Playback Timing



WORD 0 SECTOR 1	10 μ SEC GAP	WORD 17 SECTOR 0	WORD 2 SECTOR 0	WORD 1 SECTOR 0	WORD 0 SECTOR 0	300 μ SEC GAP	WORD 17 SECTOR 77	WORD 16 SECTOR 77	WORD 0 SECTOR 77	10 μ SEC GAP	WORD 17 SECTOR 76

Figure 2-5 Drum Format

Figure 2-6 shows a closer view of the word format in a sector. The words shown are the first word of the track, word 0 of sector 0 and word 1 of sector 0. The first clock pulse (index pulse) following the 300 μs gap does not write a bit; it alerts the drum control circuits of the beginning of timing pulses. The next 12 drum clock pulses write the 12 data bits of the word. After 12 bits are written, an odd parity bit is written; i.e., if the 12 bits contain an even number of 1's, a parity bit of 1 is written to generate off parity. To separate sectors, a 10-μs gap exists after the 16th word of each sector and preceding the first word of the succeeding sector.

2.4 DRUM WRITE CYCLE

As a quick reference source, Table 2-1, Analysis of Instructions for the Write Cycle, is located at the end of this chapter.

In general, the DRCW instruction (see Table 5-1) initiates a drum write cycle in the drum control logic. IOT instruction 6624 must be given initially before DRCW in order to select the proper core memory field, drum field and number of sectors to be transferred. This instruction may be given once if the core memory field, drum field and block size remain the same. The DRCW command normalizes certain control flip-flops in the drum control logic, sets the read/write flip-flop to the write state,

sets the drum 4-state device to idle, sets the data in/out signal to notify the computer data break facility that the transfer direction is out of the computer, loads the DCL from the accumulator, and sets the break request flip-flop to initiate a data break.

NOTE

The drum control logic incorporates a 4-state device to signify drum control status. The four states are IDLE, TRA, ACT, and COMP FLAG. Only one state at a time is entered and, during a normal transfer, the states advance in sequence. Entry into any state disables all other states. The IDLE state indicates that the drum has not been activated by the program or it is waiting for a 200-μs delay to set the TRA state. The TRA state indicates that the drum control is set up to transfer data, but the beginning of the drum track has not been encountered. The ACT state is entered at the beginning of the track to transfer data. The FLAG stage indicates the completion of a sector transfer.

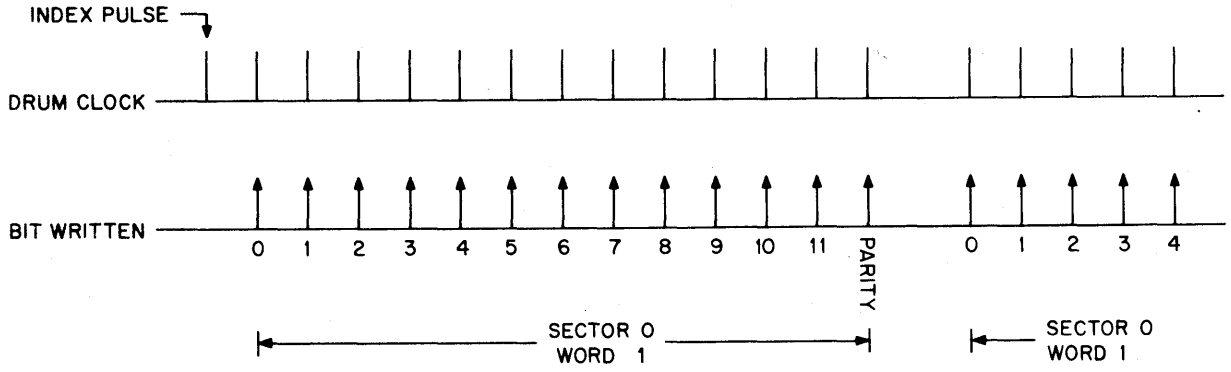


Figure 2-6 Word Format

The break request signal, generated by the break request flip-flop, initiates a computer data break cycle. During the data break cycle, the DFB is loaded from the memory location specified by the DCL and the contents of the DCL are incremented so that the next data break cycle addresses the next higher memory location. The drum control circuits now wait for the execution of the DRTS command (see Table 5-1).

The DRTS command loads the drum track and sector address from the accumulator into the DTA and DSA registers. The DRTS command also loads the 1s SNC from the SNR ← 1s complement of SNR. The DTA address register selects the specified track for the ensuing write cycle, and the DSA selects one sector of the track. The DFB register contents are transferred into the DSB register. The DRTS command also initiates a 200 μs delay to permit the track selection circuits to set up.

After the 200 μs delay, the TRA (transfer) state is set. The SYNC is incremented by 1 to produce the 2s complement of SNR. The first clock pulse of the selected sector (first clock pulse after the gap on the drum) sets the 4-state device to ACT (active). If the sector counter is equal to the sector address (SC = DSA), writing begins immediately. The ACT signal enables the drum clock pulses to generate the shift pulses and the write pulses (phase-A pulses). The first word to be written is shifted into the DSB by the shift pulses. After a data bit is shifted into the most significant bit of the DSB (DSB0), the phase-A pulse complements the write data flip-flop.

With the NRZ writer enabled, the data bit in DSB0 is written on the drum. The control pulses continue shifting the contents of the DSB and writing the DSB0 contents until the 12 data bits and the parity bit are written. After the 13 bits are written, the DSB is again loaded from the DFB and the circuits are set up to write another word, and the break request is sent to the computer to reload the DFB with the next word to be written. Writing continues in this manner until all 16 words of a sector are written. The end of the sector (beginning of the 10-μs gap) sets the drum 4-state device to FLAG if SCOV is a one or sets the 4-state device to TRA if SCOV is a zero. If TRA is set then the next 16-word sector will be written, if Flag is set then it indicates the completion of the data transfer.

2.4.1 Write One Sector-Detailed Description

The 6624 instruction loads the core memory bank, drum field, and puts 01_8 into SNR. The DRCW command (Table 5-1) that is executed by the computer starts the write cycle. The octal code of this IOT instruction is 6605. The execution of 6605 generates IOP1, IOP2, and IOP4 pulses in the computer. (Refer to the PDP-8 Users Handbook or the PDP-8 Maintenance Manual for the explanation of the IOT instruction.) Memory buffer bits 3 through 8 and the IOP pulses are applied to the 4605 Device Selector as shown on Dwg. No. D-RM08-0-4, coordinates C7. (Hereafter, drawing references will show only the last digit of the drawing and the coordinate, e.g., 4C7.) The internal gating structure of the 4605 circuit permits the IOT 6605 instruction to generate IOT 6601 and 6604 pulses (see Table 2-1). Note that the IOT 6601 pulse sets the 4-state device to IDLE (4A5). The 4-state device can be in only one state at a time because the feedback from the current state disables the other three states.

After the DRCW execution, the DCL register contains the memory address of the first word to be written on the drum. The DRCW has set the break request flip-flop; therefore, the computer executes a data break cycle (Table 2-1) to load the DFB from the memory location specified by the DCL register. The contents of the DCL register are incremented so that it addresses the next higher memory location. (Information on the computer data break cycle can be found in the PDP-8 Maintenance Manual.)

The control circuits now wait for the computer to execute the DRTS instruction. The DRTS instruction, 6615, applied MB bits 3 through 8 and the IOP pulses to the device selector (4C7) to generate the IOT 6611 and 6614 pulses. These pulses perform the operations outlined in Table 2-1. In brief, they load the DTA and DSA registers from the accumulator, load the ONE's complement of SNR ⟶ SNC, transfer the contents of the DFB into DSB, and trigger the 200-μs delay which sets the TRA state (4B5/6) and +1 to SNC.

The DSB is loaded with the word to be written, and assuming that the 200-μs delay (4B5), which permits the track selection circuits to set up, is completed, the 4-state device is set to TRA. Note that no phase-A (ΦA) or phase-B (ΦB) pulses are generated since ACT = 0 (1E11, 4C3). Therefore, the DSB is not shifted and no writing occurs.

The TAKE WORD signal (generated during DRTS) is enabled and sets the break request (RQ) flip-flop. This break generates the second word into the DFB. The DFB is transferred to the DSB. At this point, word zero is in the DSB and word ONE is in the DFB.

The index pulse at the beginning of the desired sector generates the START pulse which sets the 4-state device to the ACT state if SC = SA. The drum clock pulses are shaped by PG 1410 (4C2) the output of which triggers the (BLOCK 3.4-μs) and DATA (12-μs) integrating single shots. As long as there are clock pulses, the BLOCK and DATA multivibrators are held in the ONE state. However, in the absence of drum clock pulses, as during the 10-μs gap, the ZERO state is enforced for BLOCK, and during the 300-μs gap the ZERO state is enforced in both BLOCK and DATA. When SC = SA and SNCOV is a zero, the TRA is set, then the BLOCK going to a ONE will set ACT.

If the first four bits of the word to be written are 0011, as shown in Figure 2-7, the ACT signal (3D1) generates the 0B + ACT pulse. This pulse enables the WRITE DATA circuits (3D2) to put the WRITE DATA flip-flop into the proper state to write the designated DSB0 bit at phase A pulse time. The ACT signal gating ΦA (1E11R, 4C3) does not permit the index pulse to generate a phase-A pulse. The second drum clock pulse generates the phase A pulse, and it complements the WRITE DATA flip-flop. The WRITE DATA flip-flop output is coupled to the NRZ Writer Module, Type 4529 to write the designated bit. The ensuing phase-B pulse generates the shift pulse (3B1) to shift the DSB. The phase-B pulse, which was delayed to permit rise time of DSB0, generates the 0B + ACT pulse which again establishes the proper state of the WRITE DATA flip-flop. The next phase-A pulse writes the second bit specified by the DSB0 flip-flop.

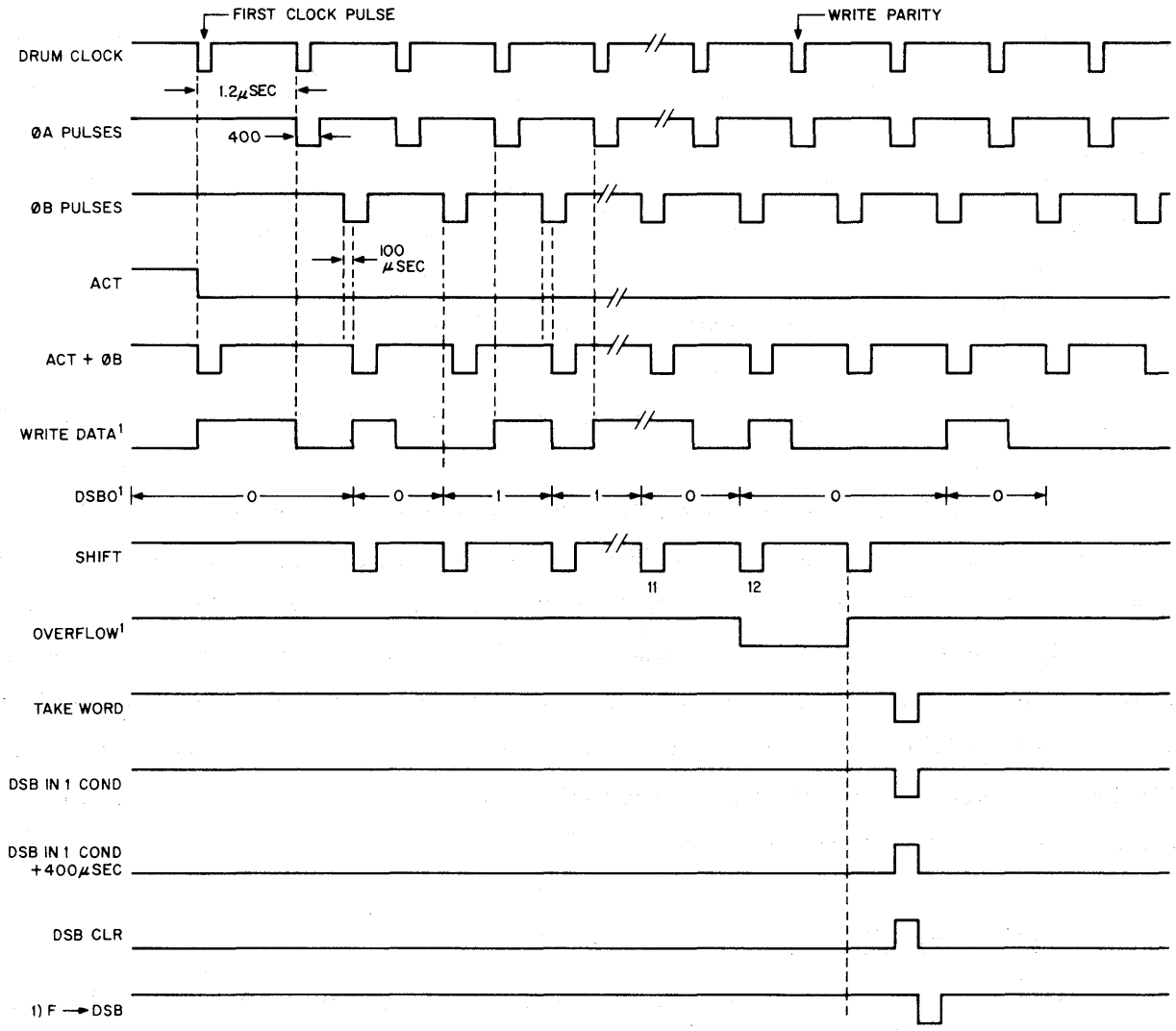


Figure 2-7 Write Cycle Timing

After 11 shifts of the DSB register, DSB2 through DSB11 contain all 0's because the DSBS flip-flop, which is continually reset by the shift pulses, shifts 0's into the DSB. Note that DF⟶DSB pulse initially sets DSBS; this insures at least 1 bit in DSB2 through DSB11 during the 11 shifts when a word is wirtten in the event that the DSB was originally all 0's. The 12th shift pulse sets the OVERFLOW flip-flop (3C4) since DSB2 through DSB11 are all 0's. The OVERFLOW signal enables the R PARITY flip-flop to write the parity bit. The shift pulses complement the R PARITY flip-flop for each 1 bit that is written. Since the R PARITY flip-flop is initially set, an odd number of 1's leaves the R PARITY flip-flop in the reset state. In this case, the R PARITY^0 signal (1D10-M, 3D2) causes the WRITE DATA flip-flop to reset so that the phase-A pulse writes a 0 parity bit to generate odd parity.

Writing continues until all 16 words of the address sector are written. The drum clock pulse that writes the parity bit of the 16th word of sector 77_8 is the last drum clock pulse before the 10 μs gap. The BLOCK one-shot multivibrator (3C1) reverts to the ZERO state 3.4 μs after the last drum clock pulse. This signal BLOCK 0-3B6) sets the 4-state device to the FLAG state if SNCOV is a 1 or to a TRA state if SNCOV is a 0.

After the FLAG state is set, the actions that follow depend on the computer. If the computer is programmed to write only one sector, the DRSC instruction (octal code 6622) generates the IOP 6622 pulse to sense the FLAG state (1E10M, 4A7). When the FLAG state is 1, the I/O SKIP causes the computer to skip the next instruction and exit from the DRSC loop. The DRSE (code 6621) may then sense the drum control for errors. This is accomplished by the DRSE instruction which generates the IOT 6621 pulses to sense the $PE^0 \cdot DE^0$ state (4A8). If no errors occur, the I/O SKIP signal causes the computer to skip the next instruction and exit from the drum routine. If an error occurs, the program will not skip the next instruction which contains a JMP to an error check routine.

2.5 DRUM READ CYCLE

As a quick reference source, Table 2-2, Analysis of Instruction for the Read Cycle, is located at the end of this chapter.

The 6624 IOT is given first. The DRCR instruction loads the DCL from the accumulator, normalizes control flip-flops in preparation for the read cycle, sets the 4-state device to IDLE, sets the DATA IN/OUT signal to DATA IN, and sets the READ/WRITE flip-flop to read. The program execute the DRTS instruction to load the DTA, DSA registers from the accumulator, SNR to SNC (ONE's complement) and after a 200-μs delay plus 1 to SNC and sets the TRA state. If SC = SA then the next index pulse sets the ACT state which enables the drum control circuits to read the drum. Data read from the addressed drum track is strobed into the least significant bit of the DSB register, (DSBS) and the contents of the DSB are shifted. After 12 shifts, the DSB contains the word read from the drum; then parity is checked. If a parity error occurs, the parity error flip-flop is set to indicate the error. The DSB contents

are transferred to the DFB and the break request signal is sent to the computer. The computer enters a data break cycle to transfer the DFB contents into the memory location specified by the DCL register. The DCL contents are then incremented. Transfer continues in this manner until all 16 words of the addressed sector are read. After the last word of the sector is encountered, BLOCK is reset to a ZERO to signify the completion of the sector transfer.

2.5.1 Read One Sector - Detailed Description

The 6624 IOT is given first. The DRCR instruction (octal code 6603) applies the MB bits 3 through 8 and the IOP pulses to the device selector to generate the IOT 6601 and 6602 pulses. Table 2-2 shows the detailed signal flow of the DRCR instruction. In brief, the DRCR instruction sets the IDLE state, clears the READ/WRITE flip-flop, and loads the DCL from the accumulator. The READ/WRITE flip-flop remains clear to signify the READ state. The READ signal causes the DATA IN signal (4B7) to be -3V to signify a DATA IN direction to the data break circuits in the computer.

The DRTS instruction is then executed to load the DTA and DSA registers with the drum track and sector address of the forthcoming read cycle (loads the ONE's complement SNR to SNC). As shown in Table 2-2, the DRTS instruction prepares the control circuits to read the first word. Note that a 1 is inserted into DSB11 (by DSB INI COND + 400 ns) (3C8) and the DSB register is cleared. After 12 shifts, the 1 that was inserted into DSB11 is in DSBF (3B2). Therefore when DSBF is a ONE, it indicates that one word has been read from the drum. The Read Cycle Timing Diagram, Figure 2-8, illustrates this condition.

After TRA is set, the control circuits wait for the index pulse and SC = SA. The index pulse sets the BLOCK one-shot multivibrator (4C1) to START which in turns sets the 4-state device to ACT (4A6). The ACT signal (4C2) enables the drum clock pulses to produce phase A (ΦA), READ STROBE, and phase B (ΦB) pulses. As the drum rotates, the flux changes induce signals into the read heads. The addressed drum read head output is applied to the Type 1537 Sense Amplifier. The READ STROBE, which occurs 0.25 µs after the phase A pulse, senses the sense amplifier (3C6) and produces a DATA READ pulse when a 1 is read from the drum; no pulse is produced when a 0 is read from the drum. The DATA READ pulse sets the DSBS flip-flop (3C8), and the shift pulse shifts the 1 from the DSBS into DSB11, as it shifts the DSB register.

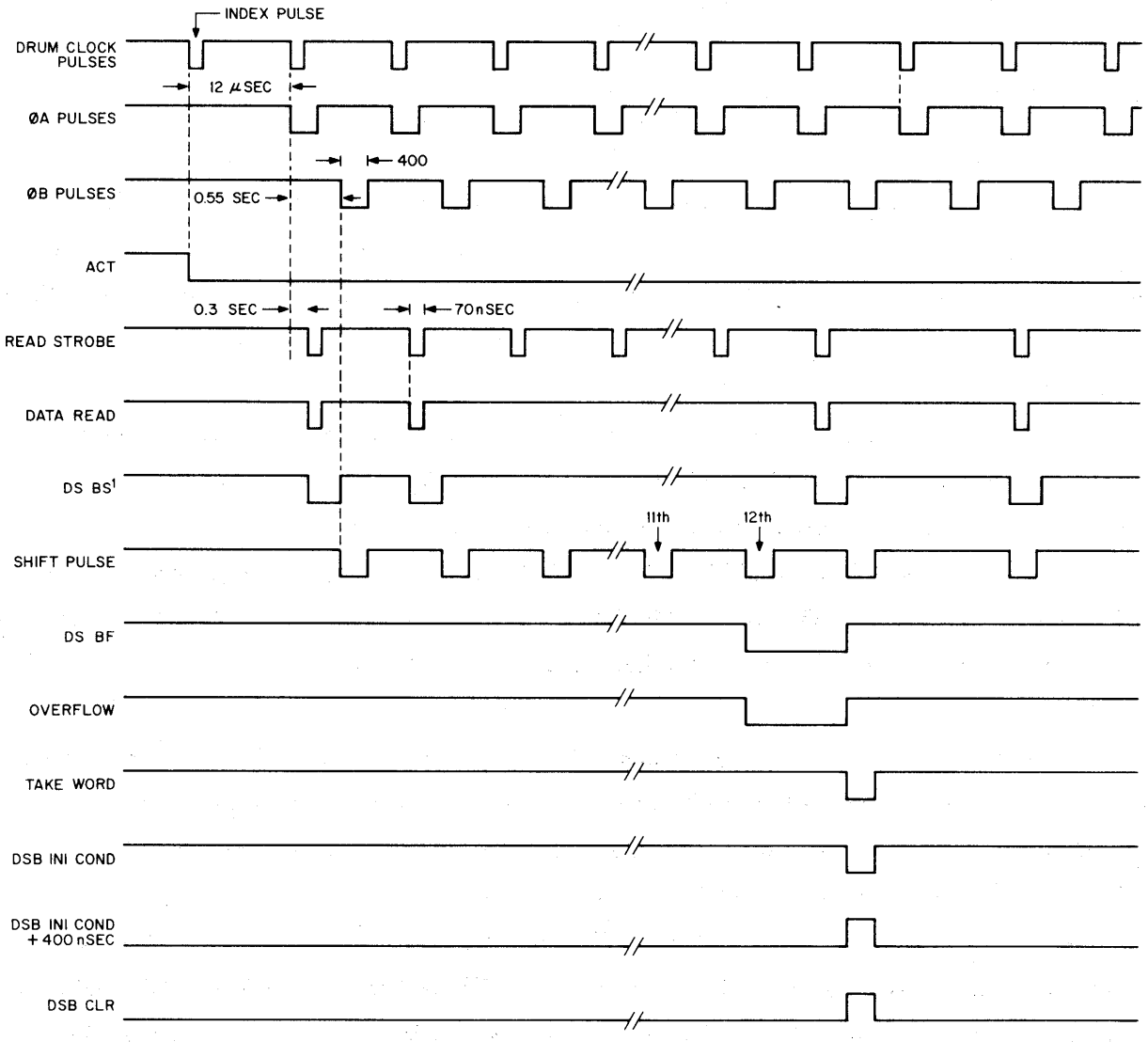


Figure 2-8 Read Cycle Timing

The shift pulse also resets the DSBS flip-flop. If the data bit read from the drum is 0, the DSBS flip-flop remains reset and the shift pulse shifts a 0 into the DSB11 flip-flop. Data transfers continue in this manner until the original 1 bit that was in DSBS is shifted into DSBF. As the 1 is shifted into the DSBF flip-flop, the DSBF1 signal sets the OVERFLOW flip-flop (3C4). The 12 bits read from the drum are in the DSB register. The next phase-B pulse, enabled by READ and OVERFLOW, generates TAKE WORD and DSB INI COND (3C2, 3C3). The DSB INI COND signal checks parity (explained later) and prepares the circuits to read the next word from the drum. The TAKE WORD (3B2) transfers the DSB contents into the DFB and sets the RQ flip-flop (4A2). The next phase-B pulse resets the OVERFLOW flip-flop.

When the RQ flip-flop is set, the word read from the drum is in the DFB. The RQ signal initiates a computer data break cycle to transfer the DFB contents into the memory location specified by the DCL (refer to Table 2-2).

Data transfer continues in this manner until all words of the addressed sector have been read. As the 10-μs gap is encountered, clock pulses cease to occur and the BLOCK multivibrator reverts to the ZERO state. This signal sets the TRA state if SCNOV is 0 and sets flag state if SCNOV is 1. With the flag state set, the program senses the flag state to exit from the read routine. If TRA was set then the next sector will be transferred.

2.5.2 Parity Check

As a word is read from the drum, the DATA READ pulse complements the R PARITY flip-flop (3C4). The R PARITY is initially set. The DATA READ pulse occurs only when a 1 is read from the drum. Since odd parity is generated during the write cycle, the R PARITY flip-flop should be in a reset state after the 12-bit word plus the parity bit are read from the drum. If not, the DSB INI COND pulse sets the PE flip-flop to indicate a parity error.

2.6 PARITY ERROR/DATA ERROR DETECT

A parity error (PE), described previously, occurs when a word is incorrectly read-out of the drum. A data error (DE) is generated when the computer does not answer a break request before another break request is made. The break request signal sets the ER SYNC flip-flop (4A3). The T2D pulse, which occurs during a data break resets the ER SYNC flip-flop. If a data break does not occur, this flip-flop remains set. The next RQ signal is enabled by ER SYNC to set the data error flip-flop.

The DRCF (clear flag) instruction generates the IOT 6611 pulse that resets the DE flip-flop (4A3), DTA (5B1), PE (3C5), and sets IDLE (4A5). Instruction DREF loads the condition of PE and DE into accumulator bits 0 and 1, respectively, to permit programmed evaluation of an error flag. Instruction DREF also generates the IOT 6612 pulse, which clears the AC (0 ⟶ AC, 4C5) and generates a

delayed 6612D (400 ns) pulse which transfers DE to AC1 (4A4) PE to AC0 (3D5) and the contents of the sector counter to the accumulator $SC_{0 \longrightarrow 5} \longrightarrow AC_{7 \longrightarrow 11}$. The state of the PE and DE flip-flops is sensed by instruction DRSE and causes a program skip if no error occurs. This condition of PE(1) + DE(1) will set SNCOV to terminate a transfer.

In the ON position, the MAINTENANCE ON/OFF switch (4D2) applies $PE^0 \cdot DE^0$ to the gate (1D9F, 4C3) which enables the phase A, phase B, and READ STROBE pulses. Detection of a data error or a parity error inhibits the clock signals so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error. In the OFF position the equipment functions normally and data errors or parity error can be detected via the error flag at the end of a sector transfer. The maintenance SW ON will only operate if the instruction for clearing the error flag is not regenerated and transfer restarted.

2.7 DRUM TRACK SELECTION CIRCUITS

The drum track selection circuits are shown in Dwg. No. E-RM08-0-2. DTA bits 4 through 7 are applied to the Y-selection circuits, and DTA bits 0 through 3 are applied to the X-selection circuits. The addressed X-selection circuit applies the read and write buses to a set of drum read/write heads. The addressed Y-selection circuits provide a single return path for the group of read/write heads addressed by the X selection circuits. Hence the DTA selects a single drum read/write head by the coincidence of the X- and Y-selection lines. For example, when the DTA is clear (DTA = 000000000), the Y0 line and the X0 line select the read/write head that is labeled '$0\text{-}77_8$". The "$0\text{-}77_8$" refers to the 64 sectors written by that read/write head. Similarly, all other read/write heads are labeled with their track and sector address.

FIELD LOCKOUT switches are provided so that data can be retained on certain fields to be available for reading only. There are 16 FIELD LOCKOUT switches (Figure 4-1). Each switch prevents writing on four drum tracks. Switch 0 inhibits tracks 0 through 3; switch 1 inhibits tracks 4 through 7; and, consequently, switch 15 inhibits tracks 74 through 77. The lockout is accomplished as follows.

The DTA4 and DTA5 bits are applied to four decoders (5D5). Each decoder output LO_0 through LO_3 is a logic 1 when the bit contents of DTA4 and DTA5 are 00 through 11, respectively. The WRITE signal is also an input to the decoders. The LO_0 through LO_3 signals are applied to the FIELD LOCKOUT switches as shown in (3D1, 2D2, 2D3). When switch 1 is closed, LO_0 applies a negative potential to the X0 selection to prevent writing on the addressed track 0. Similarly, the other seven switches lock out their associated tracks.

2.8 MECHANICAL DESCRIPTION OF DRUM

The full complement of magnetic heads is mounted on the drum in a series of blocks, with a line of eight heads in each block, and the gaps coplanar at one surface, as shown in the simplified mechanical diagram, (Figure 2-9). The flat surface serves as the pad or slider of a hydrodynamic bearing, using the boundary layer of air clinging to the rotating drum as a lubricating or self-pressurizing medium. A single thin strip of spring steel connects each magnetic head/bearing pad to the drum frame. The spring steel reed serves as a combined motion pivot, loading spring, and mounting cantilever. The action of this simple mechanical system for placing the magnetic head pad in close proximity to the drum surface when the drum is at operating speed is illustrated in Figure 2-10.

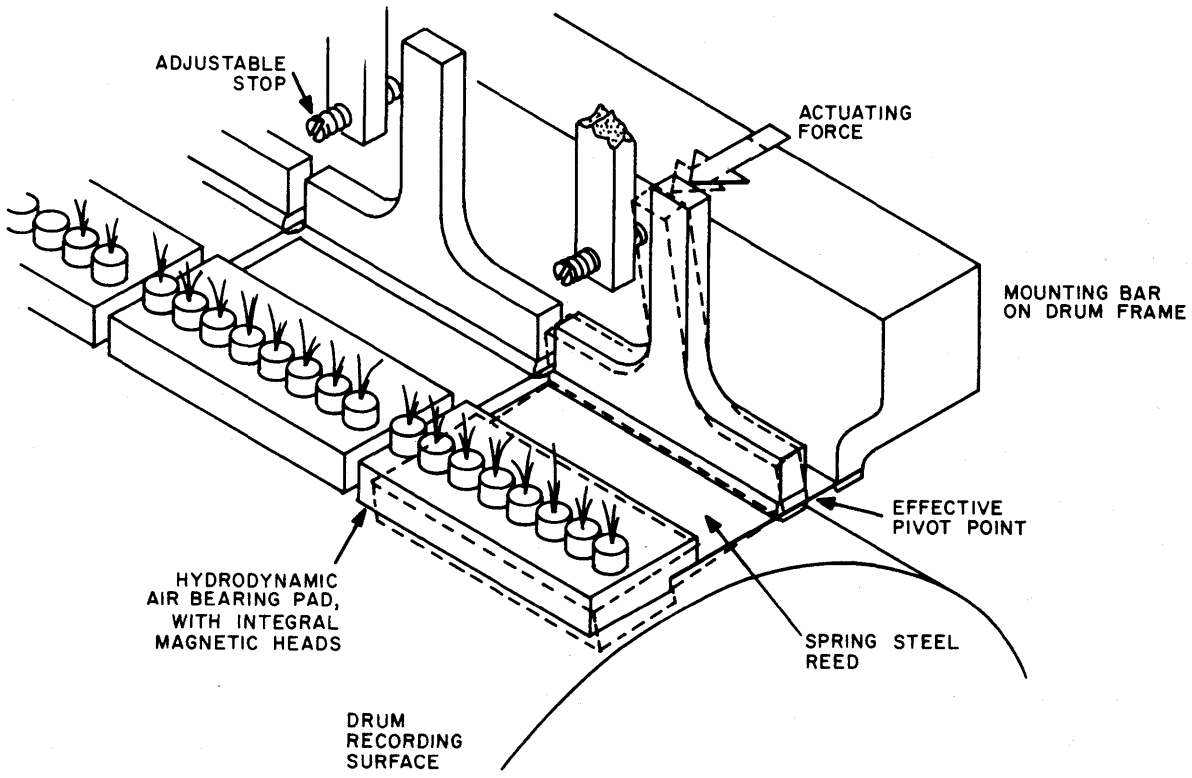


Figure 2-9 Drum Head Mounting

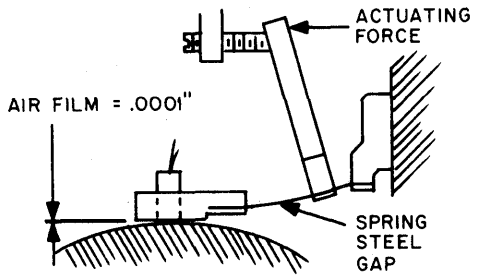


Figure 2-10 Operating Position of the Head Pad

The mechanical actuator moves the head into close proximity of the drum surface when the drum is up to speed. As the drum comes to speed, a centrifugal switch, mounted on the motor end, closes and sets a time delay relay (red cap). The relay energizes in 1.5 min and sets another time delay relay (yellow cap) which supplies actuating power to the linear motor actuator for 6s. After the linear motor pulls in the heads, a holding coil, which is energized from rectified ac, holds in the heads. The 1.5-min delay permits the drum to reach full speed prior to actuation. The 6-s interval should not be exceeded because the linear motor has a very short duty cycle and can burn out if left energized. A circuit breaker that is thermally actuated by the linear motor current provides further protection for the motor.

Normal shut down of drum power on any power failure will instantly raise the heads. Motor burnout, although not anticipated, results in speed loss so that the centrifugal switch opens and raises the heads.

A fuse mount, located under the right-hand front corner of the cabinet, contains a switch that can be used to actuate the heads. The drum centrifugal switch must be closed to operate this switch.

If holding coil fails to hold at the end of the pull-in cycle, the manual switch must be opened and closed to restart the cycle.

2.9 POWER SUPPLY AND DISTRIBUTION (RM08 DRUM SYSTEM)

The 120 Vac for the RM08 Serial Drum is supplied by a 120-Vac outlet. The ac is applied to the Type 832 Power Control in the RM08 Drum System (refer to Dwg. No. D-RM08-0-12). Relay contacts in the RM08 Drum 836 Power Control connect terminal 1 to 2 when the relay is energized. The relay is energized by -15V from the PDP-8 power supply (Dwg. No. PW-D-RM08-0-12 and RS-836). With the circuit breaker on and the REMOTE/LOCAL switch in the REMOTE position, ac power is supplied to relay contacts K1 and K2 when the -15V from the PDP-8 computer energizes the relay in the 836 Power Control. In the LOCAL position, ac power is applied to the K1 and K2 relays when the circuit

breaker is on. The K2 contacts enable the fast-on delayed-off ac power. The K1 contacts apply ac to the time delay relay K3 which enables the delayed-on fast-off ac power.

The fast-on delayed-off ac power is applied to the blower fan, drum motor, and the +10V and -15V power supply in the Type 779 Power Supply. The delayed-on fast-off ac power is applied to the dual 15-V power supply in the Type 779 Power Supply only, (refer to Dwg. No. D-RM08-0-). The red terminal of the 779 Power Supply is grounded, and the yellow terminal remains unconnected. This provides -30V at the green terminal which is used in the NRZ writer, read sense amplifier, and the X- and Y-selection modules.

When power is initially applied to the RM08 Drum System, a DDC CLEAR pulse is generated to normalize control flip-flops in the drum control circuits. This is accomplished by the Type 4401 module (Dwg. No. D-RM08-0-) supplying DDC CLEAR pulses to the system. An RC network delays the -15V to terminal V of the 4401 module; shortly after the application of power, terminal V is sufficiently negative to inhibit the clock pulses, and the drum can function normally.

Tables 2-1 and 2-2 show the analysis of instructions for the write and read cycle, respectively. These tables provide a reference to detailed signal flow during a write or read cycle.

Table 2-1
Analysis of Instructions for Write Cycle

Instruction, Operation, or Signal	Function
DRCW (6605)	Generates IOT 6601 and 6604 pulses (4C7).
IOT 6601 pulse	(Via 1E11W, (4B1) Clears, RQ, READ/ WRITE, ER SYNC, DE, and via 1C11V (4A4) sets IDLE.
	Generates DDC CLEAR (4B4) which clears OVERFLOW, R PARITY, WRITE DATA, PAR ERROR (3C4, 3C5).
IOT 6604 pulse	Transfers AC to DCL (5B1)
	Clears AC (4C5)
	Sets RQ, WRITE, and ER SYNC (4A2, 4A3).
DATA BREAK CYCLE	DCL to MA signal resets RQ and generates DRA (4B1)
	DRA increments the DCL contents (DCL14-1C6, 5C6) and clears DFB (3A2)
	T2A pulse from computer (4B2) resets ER SYNC and generates T2D
	T2D transfers MB to DFB (3A).

Table 2-1 (continued)
Analysis of Instructions for Write Cycle

Instruction, Operation, or Signal	Function
DRTS (6615)	Generates IOT 6611 and 6614 pulses (4C7).
IOT 6611 pulse	Clears DTA and DSA
	Clears PAR ERROR (3C5)
	Clears DE (1C09-4B3).
IOT 6614 pulse	Transfers AC to DTA and SA (5C1)
	Clears AC (4C5)
	Generates TAKE WORD (3C2)
	SNR ⟶ SNC
	Triggers 200-μs delay (4B5) that sets TRA +1 to SNC.
TAKE WORD	Set RQ (4B2)
	Generates DSB INI COND (3C3).
DSB INI COND	Clears DSBF (3B2) and DSBS (3C8)
	Generates DFB ⟶ DSB (3C3) which sets DSBS (3C8), and transfers DFB and DSB (3C3).
	Generates DSB INI COND + 400 ns which sets R PARITY.
ΦA pulse	Complements WRITE DATA (3C5)
	Generates ΦB pulse (4C5).
ΦB pulse	Resets OVERFLOW if OVERFLOW = 1 (3C4)
	Generates SHIFT pulse if OVERFLOW = 0 (3B1)
	(Delayed) generates 0B+ACT pulse (3D2).
DRSC (6622)	Generates IOT 6622 pulse which senses the flag state (4A7).
IOT 6624 pulse	Loads AC_{10}, AC_{11} into DFR (21B2), loads AC_0 through AC_5 into SN register.
	Loads AC_6 through AC_8 into DCLO-2 (5A1).
IOT 6612	0 ⟶ AC
	Generates 6612D
	6612D loads PE ⟶ AC_0, DE ⟶ AC_1, $SC_{0 \longrightarrow 5}$ ⟶ AC_{7-11}.

Table 2-2
Analysis of Instruction for Read Cycle

Instruction, Operation, or Signal	Function
DRCR (6603)	Generates IOT 6601 and 6602 pulses (4C7).
IOT 6601 pulse	(Via 1E11W, (4B1) Clears RQ, READ/WRITE, ER SYNC, DE and via 1C11V (4A4) sets IDLE
	Generates DDC CLEAR (4B4) which clears OVERFLOW, R PARITY, PAR ERROR, WRITE DATA (3C4, 3C5).
IOT 6602 pulse	Clears DFB
	Transfers AC to DCL
	Clears AC.
DRTS (6615)	Generates IOT 6611 and 6614 pulses (4C7).
IOT 6611 pulse	Clears DTA and DSA
	Clears PAR ERROR (3C5).
	Clears DE (1C09-4B3).
IOT 6614 pulse	Transfers AC to DTA and SA (5C1)
	Clears AC (4C5)
	Generates DSB INI COND (3C3)
	SNR ⟶ SNC
	After 200 μs sets TRA, and +1 to SNC
DSB INI COND	Clears DSB (3C8) and DSBF (3B2)
	Sets PAR ERROR if READ · ACT · R PARITY[1] = (3C5)
	Clears DSBS (3C8)
	Generates DSB INI COND + 400 ns which sets R PARITY (3C4) and DSB11 (3B8).
ΦA pulse	Generates READ STROBE (4C)
	Generates ΦB pulse (4C8).
ΦB pulse	Generates SHIFT PULSE if OVERFLOW = 0 (3B1)
	Resets OVERFLOW (3C4) if OVFLO(1)
	Generates TAKE WORD when OVERFLOW = 1 (3C1, 3C2).

Table 2-2 (continued)
Analysis of Instruction for Read Cycle

Instruction, Operation, or Signal	Function
TAKE WORD	Generates DSB INI COND (3C3)
	Transfers DSB to DFB during READ (3B2)
	Set RQ (4B2).
DATA BREAK CYCLE	DCL to MA signal resets RQ and generates DRA (4B1)
	DRA increments DCL contents (DCL14-1C6, 5C6)
	T2A pulse from computer (4B2) resets ER SYNC and generates T2D, T2D clears DFB (3A1).
	T2 generates DFB ⟶ MB (internal to PDP-8)
DRSC (6622)	Generates IOT 6622 pulse which senses FLAG (4A7).
DRFS (6624)	Generates IOT 6624 pulse (4C8).
IOT 6624 pulse	Loads AC_{10}, AC_{11} into DFR (21B2), loads AC_0 through AC_5 into SN register
	Loads AC_6 through AC_8 into DCL 0-2 (5A1).
IOT 6612	Same as write cycle.

CHAPTER 3
INTERFACE

All logic signals which pass between the computer and the serial drum are standard DEC levels or standard DEC pulses. A standard DEC level is either ground (0.0V to -0.3V) or nominal -3V. Standard DEC pulses are nominal 2.5V in amplitude (2.3V to 3.0V) and are 0.4 μs in duration (500 kc modules). Positive pulses are referenced to ground (0.0V to +2.5V) and negative pulses are referenced to ground.

Standard DEC ground potential signals are symbolized by an open diamond (—◇) and standard DEC negative signals by a solid diamond (—◆). Standard DEC positive pulses are also represented by an open diamond, and negative pulses by a solid diamond.

The input and output signals of the RM08 pass through connectors (1F2, 1F3, etc.). The connectors, and associated input and output signals are contained on the logic drawings (refer to Chapter 7). Refer to the PDP-8 Maintenance Manual for interface information in and out of this unit.

CHAPTER 4
INSTALLATION AND OPERATION

4.1 SITE REQUIREMENTS

The installation site must provide floor space at least 24 in. wide and 28 in. deep to accommodate the serial drum. At least 9 in. must be provided in front of the cabinet and 15 in. at the back to allow opening of the doors for maintenance.

Power to the RM08 is supplied from a 115 Vac output. Current drawn from the power source is 8.0A starting surge and 5.0A running.

The ambient operating temperature recommended is from 70° to 85°F.

4.2 CONTROLS AND INDICATORS

Manual control of the serial drum is accomplished through switches on the switch panel (Figure 4-1). Table 4-1 lists the switches and provides a brief description of their functions.

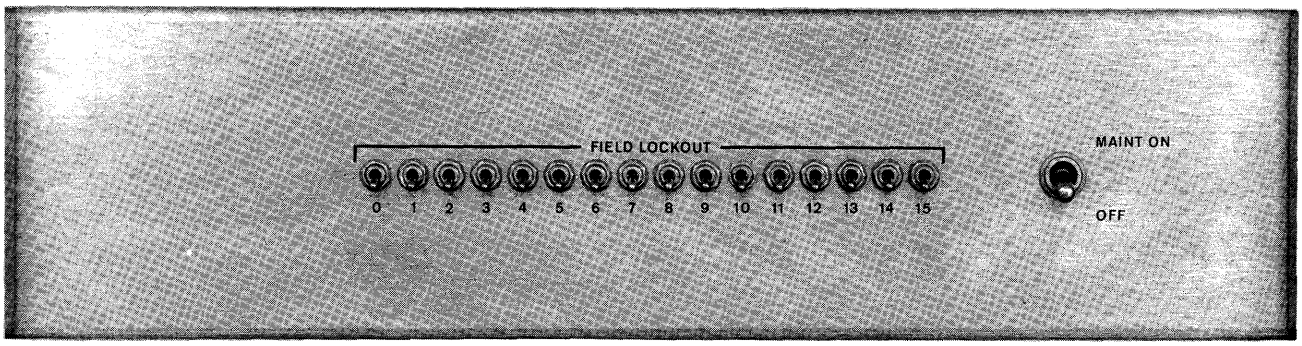


Figure 4-1 Field Lockout Switch Panel

Table 4-1
Controls, Indicators, and Switches for RM08 Serial Drum

Control, Indicator, Switch	Function
MAINT ON/OFF (Field Lockout panel)	Allows maintenance personnel to select the normal or stop-on-error mode of operation. In the OFF position the equipment functions normally and data errors or parity errors can be detected only by the error flag at the end of a sector transfer. In the ON position detection of data error or parity error by the machine inhibits generation of clock signals (ΦA, Read Strobe, and ΦB) so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error.
LOCAL/REMOTE (832 Power Control)	In the REMOTE position, the PDP-8 computer controls the application of power to the serial drum. In the LOCAL position, power is supplied to the serial drum. In both LOCAL and REMOTE positions, the circuit breaker must be on before power is applied to the serial drum. In the OFF position power is turned off from the serial drum.
ON/OFF (832 Power Control)	Applies ac power to the serial drum. The ac power is supplied from the computer; therefore, power must be turned on at the computer before this switch is effective.
FIELD LOCKOUT (16 Switches Field Lockout panel)	Each switch can control the inhibiting of a group of 4 consecutive tracks (4096 words) during writing so that the information stored on those tracks cannot be accidentally destroyed.

4.3 INDICATOR PANEL

The indicator panel lamps (Figure 4-2) provide visual indication of the machine status and register contents. The functions denoted by these lamps are shown in Table 4-2.

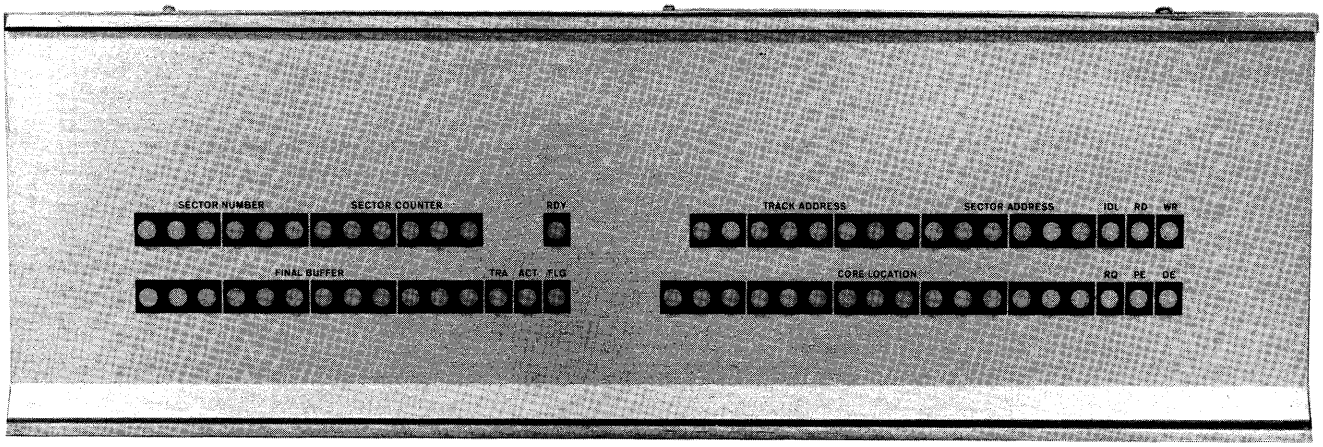


Figure 4-2 Indicator Panel

Table 4-2
Indicator Panel Lamps

Indicator	Function
SECTOR NUMBER (6)	Light to indicate 1's in the sector number register.
SECTOR COUNTER (6)	Light to indicate 1's in the sector counter.
FINAL BUFFER (12)	Light to indicate 1's in the drum final buffer.
TRACK ADDRESS (8)	Light to indicate 1's in the drum track address register.
SECTOR ADDRESS (6)	Light to indicate 1's in the drum sector address register.
CORE LOCATION (15)	Light to indicate 1's in the drum core location counter.
RDY	Lights to indicate that the drum is up to speed and ready for transfers.
TRA	Lights to indicate receipt of IOT pulse. It also indicates that the machine has been taken out of IDLE state and is waiting for clock pulses to be read from the drum. This indicator assures that the drum is in the correct position before initiating a transfer.
ACT	Lights to indicate that the machine has been taken out of the TRA (transfer) state and is actively engaged in a data transfer.
FLG	Lights to indicate that a sector transfer has been completed and the machine has been taken out of the active state. The machine remains in this state until the flag is cleared when the machine is set to either the IDLE or the TRA state.
IDL	Lights to indicate that the drum is in the IDLE state.
RD/WR	Light to indicate that the machine is in either the read or write mode.
RQ	Lights to indicate that a data request signal has been sent to the computer to request a data break to transfer a word.

Table 4-2 (cont)
Indicator Panel Lamps

Indicator	Function
PE	Lights to indicate that the machine has detected a parity error after read-in from drum to core. If the MAINT ON/OFF switch is OFF when a parity error occurs, the drum error flag is set to 1; if the switch is ON, the IDLE state is set and the transfer terminated.
DE	Lights to indicate that the machine has detected a data error, because the data request signal from the drum was not answered before another request was given.

CHAPTER 5
PROGRAMMING

5.1 INSTRUCTIONS

The operation of the RM08 Serial Drum is controlled by the IOT instructions listed in Table 5-1.

Table 5-1
Type RM08 Serial Drum Instructions

Octal Code	Mnemonic Symbol	Operation
6603	DRCR	Load the drum core location counter with the core memory location information in the accumulator. Prepare to read a number of sectors of information from the drum into the specified core location.* Clears the AC on completion.
6605	DRCW	Load the drum core location counter with the core memory location information in the accumulator. Prepare to write a number of sectors of information into the drum from the specified core location.* Clears the AC.
6611	DRCF	Clear completion flag and error flag.
6612	DRES	Load the condition of the parity error and data timing error flip-flops of the drum control into accumulator bits 0 and 1, respectively, to allow programmed evaluation of an error flag. Load the condition of the drum sector counter into the accumulator bits 6 ⟶ 11, for program evaluation of the drum address. First, clears the AC then loads.
6615	DRTS	Loads the drum address register with the track and sector address held in the accumulator. Load the contents of the drum field and sector number register into the drum track register (DTA_0, DTA_1) and sector number counter, respectively. Clear the completion and error flags, and begin a transfer (reading or writing).* Clears the AC.
6621	DRSE	Skip the next instruction if the error flag is a 0 (no error).
6622	DRSC	Skip next instruction if the completion flag is a 1 (sector transfer is complete).

*The sector, track, and core memory address are suitably incremented and allow transfer of the next sequential sector without respecifying addresses up to 64 sectors.

Table 5-1 (continued)
Type RM08 Serial Drum Instructions

Octal Code	Mnemonic Symbol	Operation
6624	DRFS	Load the drum field register with the contents of the accumulator bits 10 and 11 (AC^0_{10}, AC^0_{11} = Field 0). Load the sector number register with the contents of the accumulator, bits 0 through 5, to specify the number of sectors to be transferred (1 to 100_8).** Load the three most significant bits of the drum core location register (DCL_{0-2}) with the contents of the AC bits 6, 7, 8, to specify the core memory block to be used during the drum transfer. If the DRFS is not given before each DRTS instruction, the drum will transfer the field and sector number left in the drum field and sector number register. If memory blocks are changed (4K), then 6624 must be given before 6605 in order to break to the correct extended memory block.

**100_8 = 00

5.2 DRUM FORMAT AND PROGRAM TIMING

Chapter 2 explained the drum format and showed diagrams of the drum format and word format. A sector transfer begins when the continuously rotating drum reaches the index mark 1.2 μs before the beginning of the data in a selected track and sector.

Because the selection of the track read-write head requires 200 μs of stabiliaztion time for continuous transferring, a new track must be specified during the first 200 μs of the 300-μs interval. During transfer, if a data timing or parity error occurs, the track and sector address are not advanced and operations stop at the conclusion of the sector transfer. This feature allows the program to sense for error conditions and to locate the track and sector where transmission fails.

The drum completion flag is set to 1 upon completion of a transfer, causing a program interrupt. The flag is cleared either by a clear flag (DRCF) or automatically when one of two transfer instructions (DRTS, DRCN) is given.

The error flag, which should be checked at the completion of each transfer, indicates either of the following conditions.

a. A parity error has been detected after reading from drum to core.

b. The data break request signal from the drum was not answered within the required 16-μs period. This condition can occur if other devices with higher priority are connected to the data break

facility. Thus, in reading from the drum the data work stored in core memory is incorrect; in writing on the drum, the next word has not been received from the computer.

5.3 PROGRAMMING SUBROUTINES

The following program examples indicate the operation of the drum system in single and multiple sector transfers.

Subroutine to Transfer (Read) One Sector

```
(1)             CLA             /Calling sequence
(2)             TAD ADDR        /Initial core memory address
(3)             JMS READ
(4)             1000            /10 sectors, memory field 0, drum field
(5)             0               /Track and sector address
(6)     READ    0
(7)             DRCR            /DRCW to write
(8)             TAD I READ      /Load AC with sector count (AC0-5)
                                /Memory field (AC6-8), drum field (AC9-11)
(9)             DRFS            /Load sector counter (any value up to 77),
                                Load memory field register, and load drum
                                field register
(10)            ISZ READ
(11)            CLA
(12)            TAD I READ      /Load AC with track and sector address
(13)            DRTS            /Load serial drum DTA and start transfer
(14)            DRSC            /Done?
(15)            JMP .-1         /No
(16)            DRSE            /Errors?
(17)            JMP ERR         /Jump to error check routine
(18)            ISZ READ
(19)            JMP I READ      /Return
```

The first instruction (CLA) clears the accumulator so that the core memory starting address of the data block to be transferred can be loaded into the accumulator by the second instruction (TAD ADDR). The third instruction is a jump to subroutine at address READ. In executing this instruction the contents of the program counter (which now contains the address of the fourth memory location) are stored in the sixth memory location (designated READ), the contents of the accumulator are unchanged, and program control advances to the seventh memory location. The DRCR instruction is executed to transfer the initial

core memory address from the accumulator into the drum core location counter and to establish the read status in the drum. The next instruction TADs indirectly from the READ location. At this time the READ location contains the 12-bit address of location four, which was deposited here as the contents of the program counter during the execution of the third instruction. Therefore, the TAD instruction loads the accumulator with sector number, drum field, and core field. The DRFS instruction loads the drum with the sector number, drum field, and core field. The ISZ READ again increments location READ and then loads it into the AC. This TAD loads the track and sector address. The DRTS instruction transfers the track and sector information contained in the accumulator into the DTA and DSA registers, clears both drum flags, and initiates transfer. The DRSC instruction senses the drum completion flag and increments the contents of the program counter if the flag is a 1, thus indicating that the transfer is not complete. The program advances to instruction 15 which is a jump back to location 14 to check the flag again. When the flag indicates that the transfer has been completed, the program advances to the instruction 16 which is the DRSE instruction. The DRSE instruction senses the error flag and skips the next instruction if no error has been detected. If an error has been detected, the error flag is 1 and the program advances to the next instruction to transfer program control to the error check routine. Finding no drum error, the program advances to the ISZ READ instruction. The next-to-last instruction is the ISZ at address READ. The READ location contains the address of the track and sector address (location 4). The ISZ instruction increments the contents of READ so that it contains the address of the RETURN to the main program. Therefore, the JMP I READ instruction returns program control to the main program.

5.4 FIELD LOCKOUT SWITCHES

The FIELD LOCKOUT switches (Figure 4-1) permit data to be retained on certain tracks where it is available for reading only. Turning a LOCKOUT SWITCH to the ON position inhibits writing on its associated track addresses. The octal address inhibited by each switch are shown below.

Switch	Address	Switch	Address
0	0000-377	8	4000-4377
1	0400-777	9	4400-4777
2	1000-1377	10	5000-5377
3	1400-1777	11	5400-5777
4	2000-2377	12	6000-6377
5	2400-2777	13	6400-6777
6	2000-3377	14	7000-7377
		15	7400-7777

CHAPTER 6
MAINTENANCE

Maintenance of the Type RM08 Serial Drum consists of a test and maintenance program MAINDEC-08-D5AA-D, procedures repeated periodically as preventive maintenance, and tasks performed after equipment malfunction as corrective maintenance. Maintenance activities require use of the equipment (or equivalent) listed in Table 6-1, and standard hand tools, cleansers, test cables, and probes.

Table 6-1
Maintenance Equipment

Equipment	Manufacturer	Model
Multimeter	Triplett/Simpson	630-NA/260
Oscilloscope	Tektronix	540 Series
Variable Power Supply	DEC	734
System Module Extender*	DEC	1954
System Module Puller*	DEC	1960
Diagnostic Program	DEC	Digital-5-55-M

*One supplied with the equipment

If it is necessary to remove modules, use the Type 1960 System Module Puller. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the panel. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling.

To gain access to adjustment controls on the module, or to points for signal tracing, remove the module, and insert a Type 1954 System Module Extender into the proper module slot in the panel, and then reinsert the module into the extender.

6.1 PREVENTIVE MAINTENANCE

Perform preventive maintenance tasks prior to initial operation of the equipment and periodically during its operating life. Perform these tasks in accordance with a reasonable schedule to discover progressive deterioration, to correct minor damage, and thus forestall future failure. Compile a log book to record data found during the performance of preventive maintenance to indicate the rate of circuit operating deterioration and provide information to determine when components should be replaced.

Preventive maintenance tasks consist of mechanical checks such as cleaning and visual inspections, checks of specific circuit elements such as the power supply, clock timing, sense amplifiers, and magnetic heads, and marginal checks to aggravate borderline conditions or intermittent failures so that they can be detected and corrected. All preventive maintenance tasks should be performed every six months or 1,000 equipment operating hours, whichever occurs first.

6.1.1 Mechanical Checks

To assure good mechanical operation of the equipment, perform the following steps and the indicated corrective action for any substandard conditions that may be found:

a. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and its housing which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-Kote (procured from Research Products Corporation, Madison, Wisc.).

c. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

d. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue enamel number 3277-1S65.

e. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security.

f. For mechanical security, inspect switches, knobs, jacks, connectors, transformers, fan, capacitors, and lamp assemblies.

g. Inspect modules for proper seating in the racks.

h. Inspect power supply capacitors for leaks, bulges, or discoloration.

6.1.2 Power Supply Checks

Check the output voltage and ripple content of the Type 779 Power Supply. Check the +10V output between the yellow (-) and orange (+) connectors to assure that it is between 9.5V and 11.0V with less than 800 mV ripple. Check the -15V and the +15V outputs (green to yellow and red to yellow, respectively) to assure that they are between 14.5V and 16.0V with less than 400 mV ripple.

These supplies are not adjustable; thus if the output voltage or ripple content is not within the tolerance specified, the supply is defective.

6.1.3 Timing Checks

Using the oscilloscope and referring to Dwg. No. D-RM08-0-4, check the timing of the Type 4303 Integrating Single Shots at location 1C4, 1C13 and the Type 1304 Delay at location 1C15. If necessary, adjust the timing of these modules by turning the potentiometer screw which is accessible through a hole in the handle.

Check the single-shot by observing the 1 output at 1C4W while triggering the oscilloscope on 1C4K. During each revolution of the drum, the single-shot is triggered every 1.2 μs for approximately 17 ms during data reading and receives no pulses during the 300-μs gap. The output at terminal 1C4W should be at ground level during the gap, drop to -3V at the first triggering pulse, and remain at -3V for 3.4 μs after the last triggering pulse is received before reverting to ground potential. The output at 1C13W should be at 0V for 7 μs during the 10-μs gaps between the 64 sectors and at 0V for 300 μs during the large 300 μs gap. Any other time it should be at ground.

Check the timing of the delay module by observing the negative read strobe pulse at terminal 1C15E while triggering the oscilloscope on the ΦA pulse at 1C14J. Read strobe pulses should follow ΦA pulses by approximately 0.25 μs. Observe the read strobe pulses and the amplified output of a magnetic read head by connecting the second input of the dual-trace oscilloscope to terminal 1E25S. It is important that the read strobe pulses occur at the negative peak of the sinusoidal read signal. Measurements should be made using several different heads, and the read strobe pulse should be adjusted for an average of the measurements to eliminate large differences in peak playback time.

6.1.4 Drum Sense Amplifier Checks

The Type 1537 Drum Sense Amplifier modules at locations 1C1 (clock track) and 1E25 (data track) are checked for proper slice or threshold level at terminal S. This measurement can be made with the oscilloscope by measuring the amount by which the base line shifts above ground when the signal is connected to the input. The clock track sense amplifier slice level should be +100 mV. The data track sense amplifier slice level should be +150 mV. Adjustment of the slice level can be achieved by turning the potentiometer screw which is accessible through a hole in the module handle.

6.1.5 Drum Head Mounting Adjustments

Adjustment of the magnetic heads is provided by the stop screw for each pad of heads and its actuating arm, as shown in Figure 6-1. With this stop screw properly positioned, the actuating arm moves the pad to a position where the reed is slightly bent and the pad is tangent to the drum surface at the line of head gap. These adjustments are made at the factory and under normal circumstances should not have to be changed, at least no more than minor adjustment. Should adjustment be necessary, however, proceed in the following manner.

a. Connect an oscilloscope to 1E25S to observe the preamplifier output for the drum head in question.

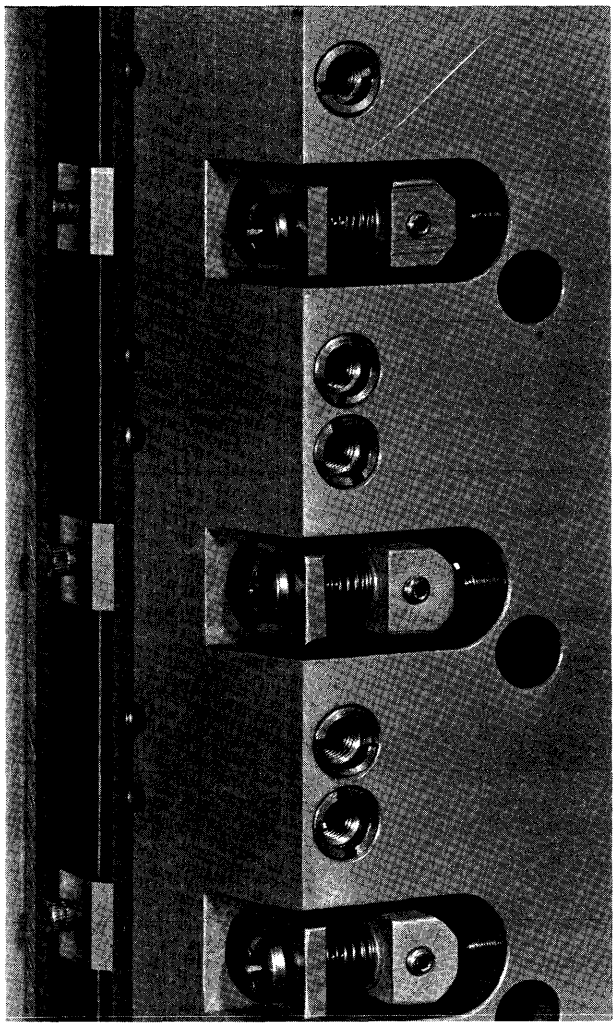


Figure 6-1 Stop Screw Position

b. Set the DTA to address the drum head in question. Drawing No. BS-E-RM08-0-2 shows the bar and pad location and the octal address of each drum head.

c. Set the drum control status to read.

d. Using a 5/64 hexagonal for socket heads, adjust the stop screws until a maximum output is noted on the oscilloscope as shown in Figure 6-2. The adjustment screw is located on the right-hand side of each bar as one views the drum as shown in Figure 6-1.

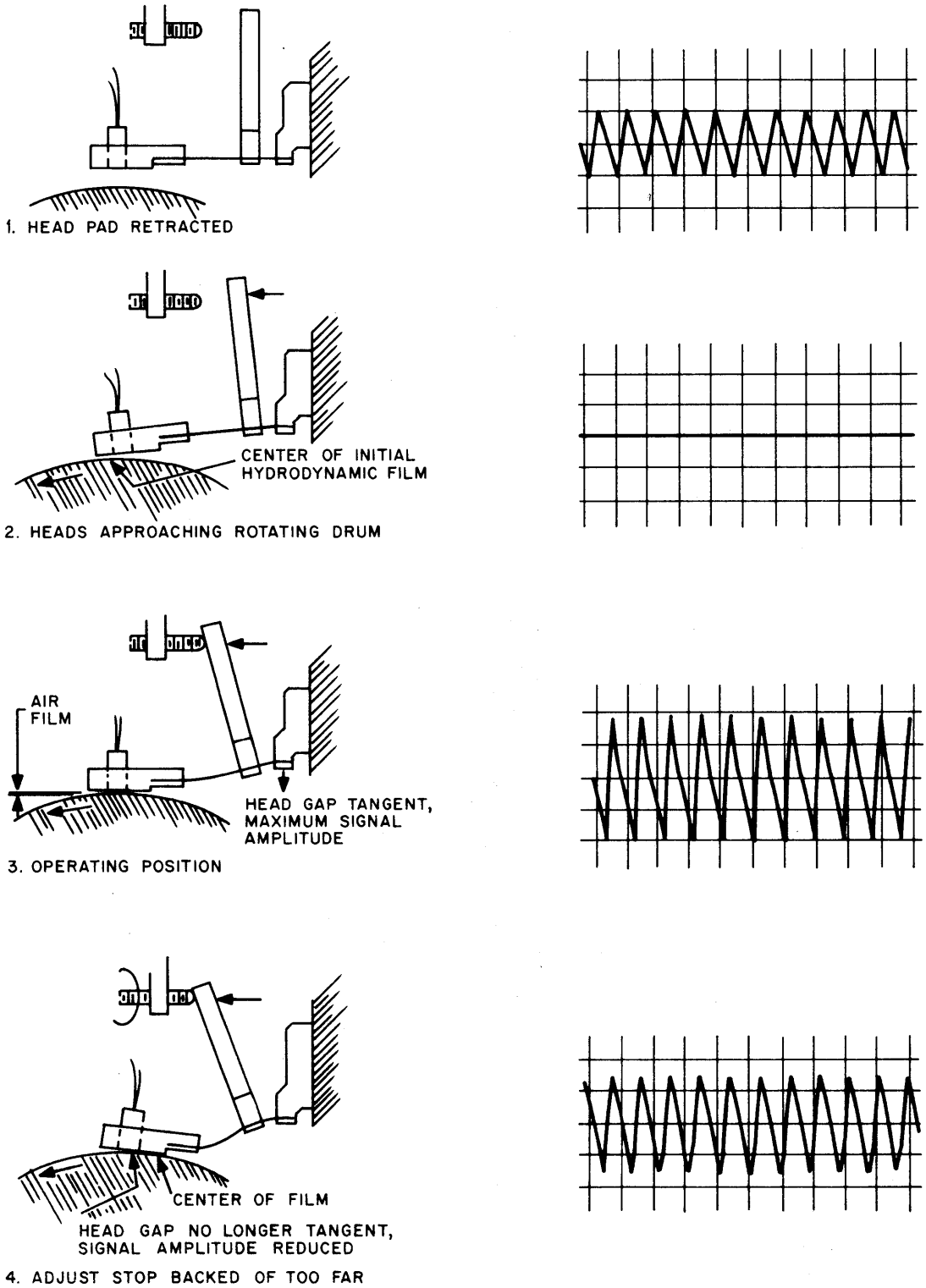


Figure 6-2 Operating Positions of Head Pad

CAUTION

If head adjustment is attempted with diode boards in place, make sure that the adjustment wrench is placed and/or insultated to prevent shorting connections or components to ground.

The best method of making this check is to run a program in which the patterns of all 0s, all 1s, or alternate 1s and 0s are written on the selected track, then read the data and monitor the output of the selected track. If data on the selected track is to be retained, it should be read into core memory before proceeding with this adjustment. Rewrite the selected track and read the recorded signal after every adjustment.

6.1.6 Pad Leveling Adjustment

The amplitude of head playback signals among the eight heads in each pad is set as uniformly as possible by using the pad leveling screws which are accessible at the outer surface of each bar, approximately adjacent to the upper and lower edges of each pad. This may be checked on head number 0 (sectors 0-77) and 7 (sectors 0-77) (top and bottom heads) with secondary reference to heads 2 and 7. Clockwise rotation of a pad leveling screw tends to increase signal amplitude at that end of the pad. Continuously write and read the selected heads always alternating between the two.

6.1.7 Marginal Checks

Marginal checks are performed to aggravate borderline conditions within the logic to reveal observable faults. Therefore, these conditions can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. The checks are performed by operating the equipment logic circuits from an external, adjustable power source, such as the DEC Type 734 Variable Power Supply.

Raising the bias voltage above +10V is equivalent to lowering the amount of base drive on a particular transistor. This in turn simulates a lower gain driving transistor, thus raising the bias voltage tends to indicate low gain transistors. Lowering the bias voltage below +10V simulates a condition where the voltage drop across the previous driving transistor (V_{CE}) has increased. This tends to indicate high V_{CE} drop (leakage) transistors or low gain driving transistors. The -15V supply margins are not checked in the serial drum because to raise or lower the -15V does not affect the majority of control logic, since it is the collector load voltage and is usually clamped to -3V. The +10V margin should be about ±5V.*

*The 1537 Sense Amplifier, 1C1 and 1E25, has only ±2V margins on +10V(B).

By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement. Marginal checks of the +10 (A) supply (top switch at the left of the rack) to rack E varies the slice level on the drum sense amplifier modules and therefore is a valuable tool in verifying the capability of the machine to read and write on the drum surface. Normally increasing the +10 (A) supply by three or four volts also increases the slice level and causes bits to be dropped out. Decreasing the +10 (A) source by three or four volts usually lowers the slice level and causes bits to be picked up.

Marginal check terminals are provided on color-coded connectors which are connected in common to all racks, so that an external power supply can be attached to any connector to marginal check all racks. The color coding of these connectors from top to bottom is as follows:

Green: +10 Vdc marginal-check supply

Red: +10 Vdc internal supply

Black: ground

Blue: -15 Vdc internal supply

Yellow: -15 Vdc marginal-check supply

Three single-pole single-throw switches at the end of each rack of logic allow selection of either the normal internal power supply or the external marginal-check power supply for distribution to the logic. The top switch selects the +10V supply routed to terminal A of all modules in that rack. In the down position the fixed internal +10V supply connected to the red terminal is supplied to the modules, and in the up position the marginal-check voltage supplied to the green terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10V level to terminal B of all modules. The bottom switch selects the -15V supply to be routed to terminal C of all modules. In the down position, the fixed -15V output of the internal power supply, received at the blue terminal, is supplied to the modules; while in the up position, the marginal-check voltage, connected to the yellow terminal, is supplied to terminal C of all modules.

To perform marginal checks, use the following procedure.

a. Connect the external marginal-check power supply to the colored connector on any rack between the green (+) and the black (ground) terminal.

b. Energize the marginal-check power supply and adjust the outputs to supply the nominal +10 Vdc.

c. Set the top switch on the rack to be checked to the up position.

d. Start equipment operation in a repetitive pattern or in a routine which fully utilizes the circuits in the rack to be tested. The diagnostic drum program, MAINDEC-08-D5AA-D, obtainable from the Digital Program Library should be used unless a user has developed a special maintenance program.

e. Lower the +10V marginal-check power supply until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced.

f. Start equipment operation, then decrease the +10V marginal-check supply until normal operation is interrupted. At this point record the marginal-check voltage. Transistors can again be located and replaced.

g. Stop operation and return the top switch to the down position.

h. Repeat steps b through g for the center switch on the logic rack that is being checked.

i. Repeat steps b through h for each rack of logic to be checked.

j. Deenergize and/or disconnect the external marginal-check power supply.

6.2 CORRECTIVE MAINTENANCE

No special test equipment nor tools are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the system logic. Persons responsible for maintenance should become thoroughly familiar with the system concept and the operation of specific circuits as described in Chapter 2; program techniques, described in Chapter 5; the engineering drawings, presented in Chapter 7; and the location of mechanical and electrical components.

Diagnosis and remedial action for a fault condition is performed in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the system.

b. System troubleshooting to locate the fault to within a module through the use of diagnostic programming, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of the malfunction.

e. Validation tests to assure that the fault has been corrected.

f. Log entry to record pertinent data.

6.2.1 System Troubleshooting

Do not attempt to troubleshoot the drum system without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that the serial drum is actually at fault before continuing corrective maintenance procedures. Faults in equipment transmitting or receiving information or improper connections

of the system frequently give indications very similar to those caused by drum malfunction. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been determined to be within the RM08 Serial Drum, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test should be employed to locate the source of the fault.

6.2.1.1 Diagnostic Program - Refer to program number MAINDEC-08-05AA-D from the Digital Program Library.

6.2.1.2 Signal Tracing - If the fault has been located within a functional logic element, program the equipment to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace a signal flow through the suspect logic element. Oscilloscope sweep may be synchronized by control signals or clock pulses available at individual module terminals. Trace the signal from the output back to its origin.

6.2.1.3 Aggravation Tests - Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive test cycle. Often, wiping the handle of a screwdriver across the back of a suspected row of modules is a useful technique. By repeatedly starting the equipment and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

6.2.2 Circuit Troubleshooting

Where downtime must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare of each module type (Table 6-2) which can be inserted when system troubleshooting procedures have located the fault to a particular component.

Bench troubleshooting procedures can be performed to correct the defective components. Where downtime is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules within the equipment. This practice involves module removal by means of a Type 1960 System Module Puller, insertion of a Type 1954 System Module Extender into the logic rack, insertion of the suspect module in the module extender, and osiclloscope signal tracing of the module with the equipment energized and operating.

Table 6-2
Spare Module List

Module No.	Name
1213	Flip-Flop
1304	Delay (One Shot)
1410	Pulse Generator
1537	Drum Sense Amplifier
4102	Inverter
4106	Inverter
4112-47	Negative Diode NOR
4113	Negative Diode NOR
4114-74	Negative Diode NOR
4115-17	Positive Diode NOR
4127	Capacitor-Diode Gate
4141-R	Negative AND-NOR Gates
4215-X	Complementing Flip-Flops
4216	Shift Register
4217	Complementing Flip-Flops
4220-377	Buffer Register
4222-77	Counter Flip-Flops
4225	Counter Flip-Flops
4301	Delay (One Shot)
4303	Integrating Single Shot
4401	Variable Clock
4529	Drum Writer
4530	Drum X Select
4531	Drum Y Select
4604	Pulse Amplifier
4605	Pulse Amplifier
4606	Pulse Amplifier
6102-145	Inverter
6106-17	Inverter

Table 6-2 (cont.)
Spare Module List

Module No.	Name
6110	Negative Diode NOR
6113	Positive Diode NOR
6115-12	Positive Diode NOR
R107	Inverter

Static and dynamic circuit troubleshooting procedures may be performed at a bench. Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

a. Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

b. Do not attempt to measure resistance of any clock head. The voltage applied to the test probes is sufficient to erase information from the drum surface.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistance of transistors. Most catastrophic failures are due to short circuits between the collector and the emitter or due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse directions. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back.

In this analogy PNP transistors are considered to have both cathodes connected together to form the base and both the emitter and collector assume the function of an anode. In NPN transistors, the base is assumed to be a common-anode connection and both the emitter and collector are assumed to be the cathode. Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. More reliable indication of diode or transistor malfunction is obtained through the use of one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by an intermittent connection, can be detected by connecting a 1.5V flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 756 Power Supply can be used to energize a system module. These supplies provide both the +10 Vdc and -15 Vdc operating supplies for the module as well as ground and -3V sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by logic level by means of eyelets provided on a Jones plug on the power cable. Type 911 Patch Cords may be used to make these connections on the Jones plug. In this manner logic operations and voltage measurements can be made. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

6.2.3 Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placement of excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the special precautions that follow should be taken.

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6V soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals.

6.2.4 Head Pad Replacement

This replacement should be performed only by qualified personnel. To replace the head pads, the tools that are listed below are required.

a. Surface plate (at least 3 ft by 2 ft)

b. Two 2-inch machinists' parallels

c. Aligning pin, VRC (Vermont Research Corp.) part no. 59P7

d. Steel Scale, 1/32-inch calibrations

e. Height comparator with 0.000, 050 inch calibration (or finer), with less than 5 gram contact pressure. The "Electroprobe" manufactured by Federal Products, Providence, R.I., is suggested.

f. Adjustable height gage, 3- to 4-in. micrometer caliper

Replacement of the head pad must be done with the head mounting bar removed from the drum. This is done by removing the four socket head cap screws at the ends of the bar, disconnecting the matrix wiring, and setting the head mounting bar on the two parallels on the surface plate. Place the bar with the bearing surface of the pads upward and the stop adjusting screws accessible at the edge of the surface plate.

Remove the head pad by removing screws at the pad and those holding the leads with a strain relief and the associated connector. Insert the new pad, bending the leads gently. Replace all screws. Check polarization of connector locating pins (which also serve as mounting screws) to ensure proper mating with the other half. Before tightening head pad mounting screws, insert the aligning pin through the corresponding hole in the bar and up into the aligning hole in the loose pad.

Insert aligning pin into the pad carefully, making sure that no leads are caught at the pin hole. With the pin in place, scale the distance from each end of the pad to the reed mount and adjust the parallel within 1/64 inch. Tighten pad mounting screws and recheck parallelism. Remove the aligning pin and proceed to height adjustment.

Using housing flat-to-drum dimensions and the required drop allowance, measure the thickness of the bar and parallels in use and calculate the height setting for the height gage as follows.

Housing-to-Drum Dimension – Drop Allowance = Required Bar-to-Head Dimension

Required Bar-to-Head Pad Dimension + Parallel Thickness + Bar Thickness = Height Gate Setting

Set the height gate to size using the micrometer caliper; then use the height gage to set the comparator to zero or center range. Rotate the actuator link and allow the head pad to move into actuated position. Using a hexagonal wrench in the corresponding stop screw, lower the pad being adjusted until the height comparator reads approximately zero at the center of the pad. Check elevation of the entire pad. Using the two differential pad leveling screws between the read mount and bar, and the stop screw for overall elevation, set the pad level within 0.0001 in. (leading to the trailing edge) and 0.0002 in. (end to end).

Replace the bar on the drum housing. Replace all matrix boards and wiring. Monitor the output signal from the replaced head pad (as described previously for head pad adjustment) while letting this pad approach the recording surface for the first time. As the stop screw is moved out, allowing the actuator to move the pad into "flying position," compare output levels on heads 1 and 8 (top and bottom) in the pad. Balance these levels with ±10% with the differential screw adjustment at partial output levels; then move the stop screw out father until the "peaking" process (described under Head Adjustment) is complete.

6.2.5 Validation Test

Following the replacement of any electrical component of the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustments of timing or signal levels caused by the replacement. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor was replaced in the proper supply, the ripple check for that power supply should be repeated as specified under Power Supply Checks. If repairs or replacements are made in an area which is not checked during preventive maintenance, the diagnostic program should be run or an appropriate operational test should be devised. For example, if a flip-flop is repaired or replaced, the register or control function performed by the flip-flop should be checked in entirety by manually setting and clearing, by programmed exercise of the function, or by repeating the diagnostic program.

6.2.6 Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

CHAPTER 7
ENGINEERING DRAWINGS

This chapter contains reduced copies of the DEC engineering prints on the Type RM08 Serial Drum. Only those drawings are included which are essential and are not available in the referenced documents that are pertinent to this system are included.

7.1 DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information separated by hyphens. For example, drawing number BS-D-RM08-0-4 includes the information that follows.

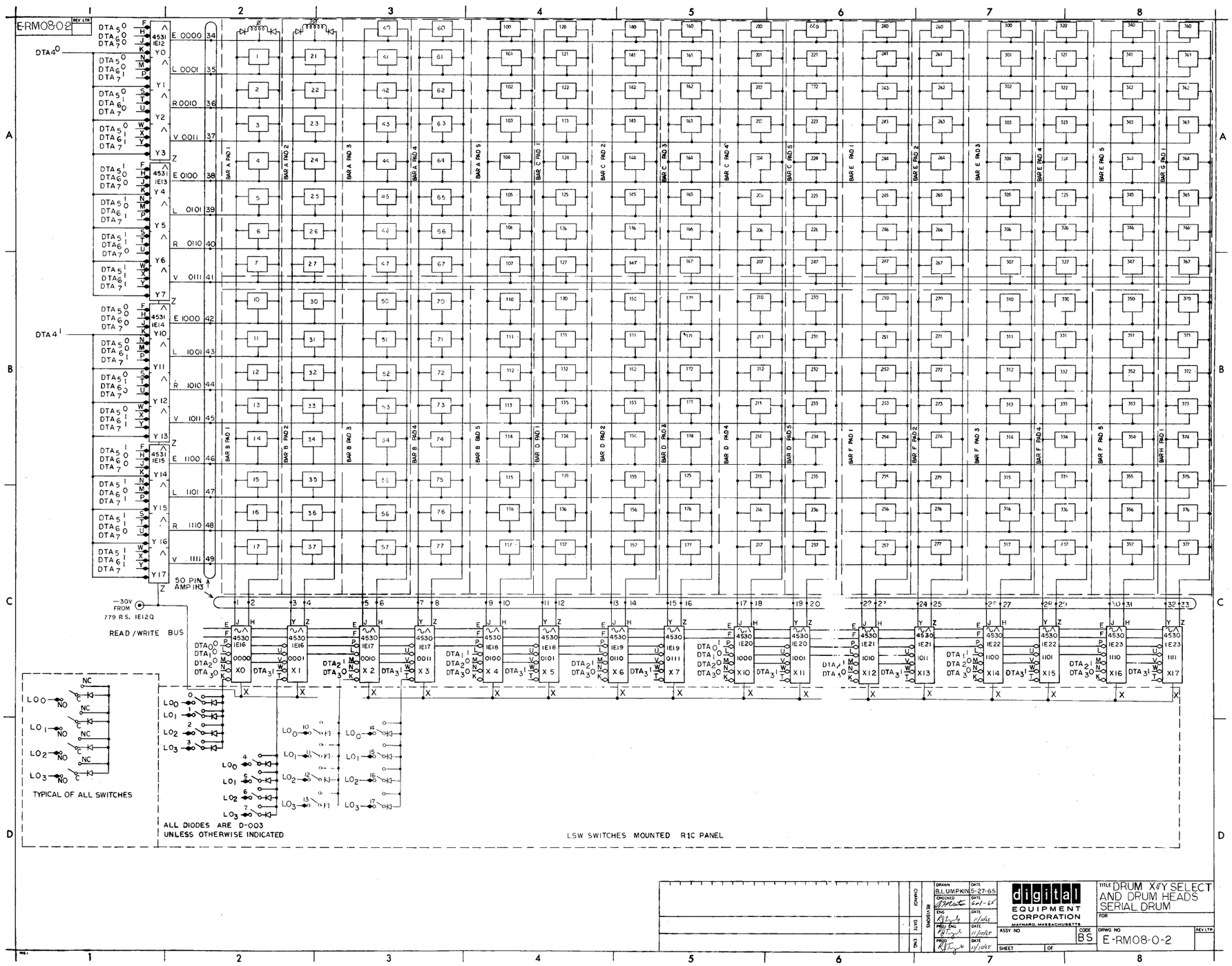
BS - type of drawing
D - original drawing size
RM08 - equipment type
0 - manufacturing series of the equipment
4 - drawing number within the series

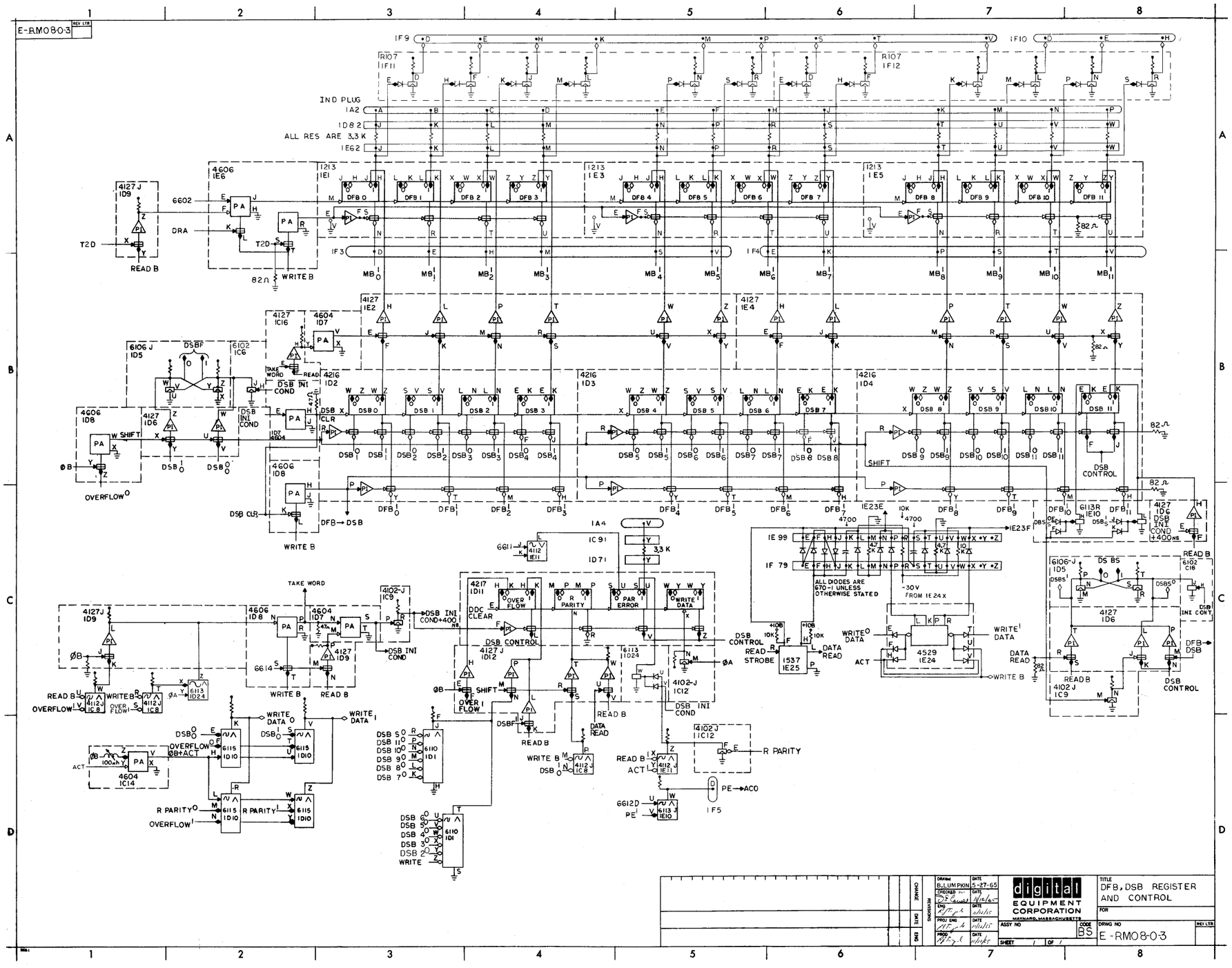
The drawing types are listed below:

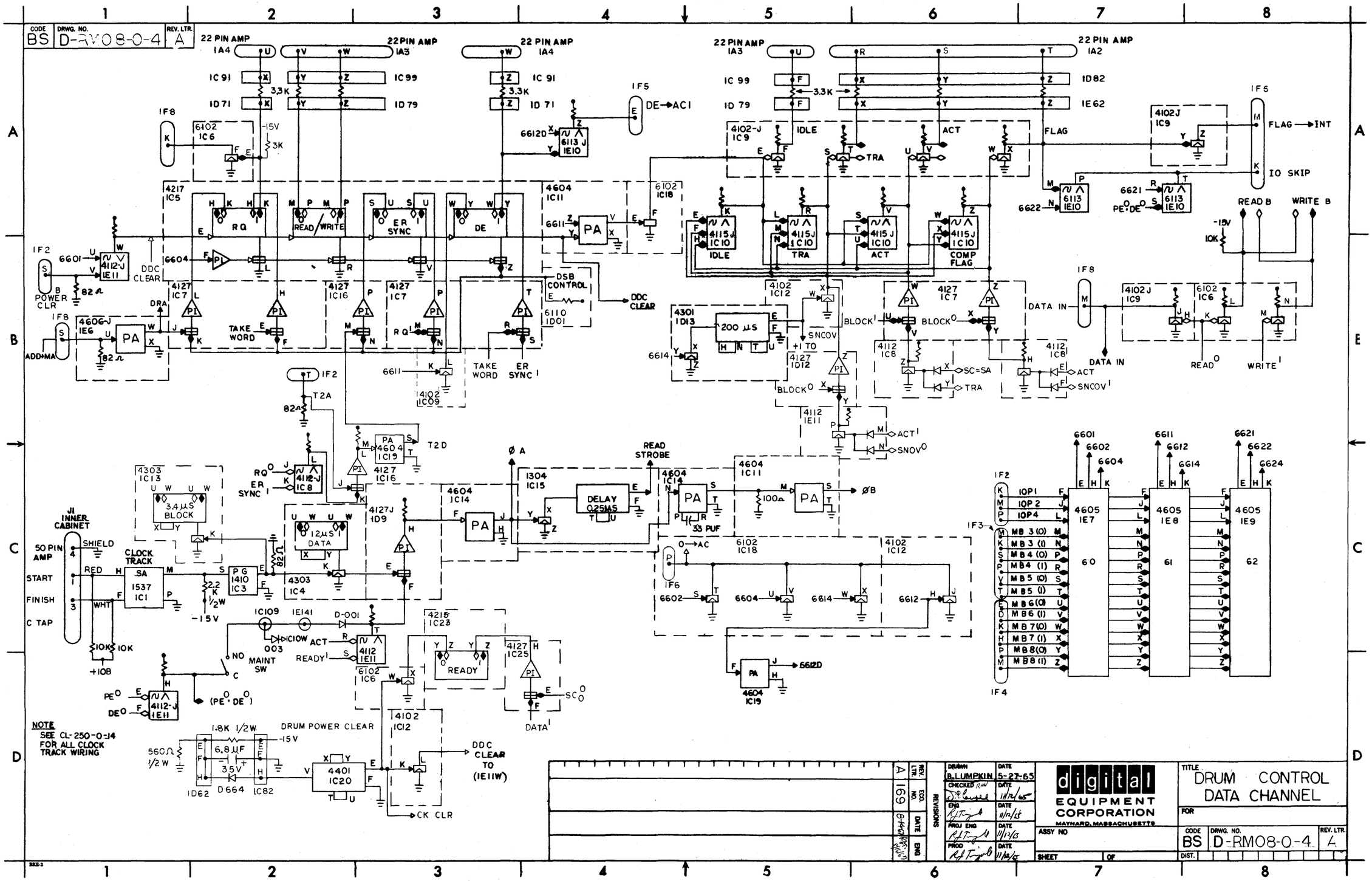
BS, block schematic or logic diagram
CD, cable diagram
CL, cable list
CS, circuit schematic diagram
FD, flow diagram
ID, interconnection diagram
MA, mechanical assembly diagram
ML, module location diagram
PW, power wiring diagram
RS, replacement schematic diagram
SD, system diagram
TD, timing diagram
TFD, timing and flow diagram
TSL, terminal strip location diagram
UML, utilization module list
WD, wiring diagram
WL, wiring list
WS, wiring sheet

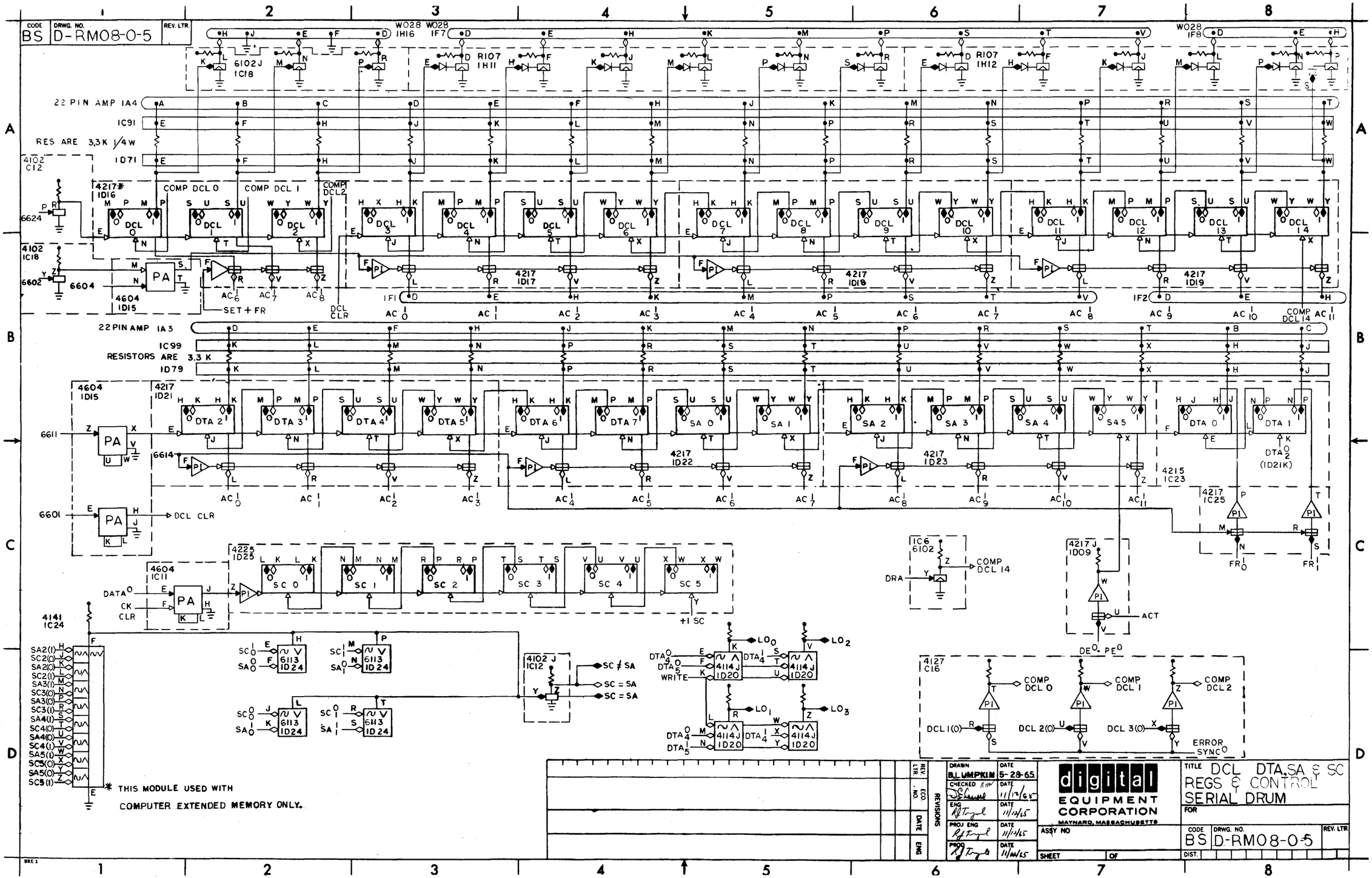
7.2 CIRCUIT SYMBOLS

The block schematics of DEC equipment are multipurpose drawings that combine signal flow, logical function, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block, or semi-block form, with special symbols that define the circuit operation. These symbols are defined in the FLIP CHIP Modules Catalog and the Systems Module Catalog.


E-RM0802
REV LTR
DTA4 0
DTA4 1
4531 1E12
4531 1E13
4531 1E14
4531 1E15
E 0000 34
L 0001 35
R 0010 36
V 0011 37
E 0100 38
L 0101 39
R 0110 40
V 0111 41
E 1000 42
L 1001 43
R 1010 44
V 1011 45
E 1100 46
L 1101 47
R 1110 48
V 1111 49
50 PIN AMP 1H3
-30V FROM 779 R.S. 1E12Q
READ/WRITE BUS
4530 1E16
4530 1E17
4530 1E18
4530 1E19
4530 1E20
4530 1E21
4530 1E22
4530 1E23
0000 X0
0001 X1
0010 X2
0011 X3
0100 X4
0101 X5
0110 X6
0111 X7
1000 X10
1001 X11
1010 X12
1011 X13
1100 X14
1101 X15
1110 X16
1111 X17
BAR A PAD 1
BAR A PAD 2
BAR A PAD 3
BAR A PAD 4
BAR A PAD 5
BAR B PAD 1
BAR B PAD 2
BAR B PAD 3
BAR B PAD 4
BAR B PAD 5
BAR C PAD 1
BAR C PAD 2
BAR C PAD 3
BAR C PAD 4
BAR C PAD 5
BAR D PAD 1
BAR D PAD 2
BAR D PAD 3
BAR D PAD 4
BAR D PAD 5
BAR E PAD 1
BAR E PAD 2
BAR E PAD 3
BAR E PAD 4
BAR E PAD 5
BAR F PAD 1
BAR F PAD 2
BAR F PAD 3
BAR F PAD 4
BAR F PAD 5
BAR G PAD 1
BAR H PAD 1
NC
NO
C
TYPICAL OF ALL SWITCHES
ALL DIODES ARE D-003
UNLESS OTHERWISE INDICATED
LSW SWITCHES MOUNTED R1C PANEL
DRAWN BL LUMPKIN 5-27-65
CHECKED
ENG
PROJ ENG
PROG
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DRUM X&Y SELECT AND DRUM HEADS SERIAL DRUM
FOR
ASSY NO
CODE BS
DRWG NO E-RM08-0-2
REV LTR
SHEET
OF


E-RM080-3
IND PLUG
ALL RES ARE 3.3 K
READ B
WRITE B
OVERFLOW
SHIFT
DSB CONTROL
DSB INI COND
DSB CLR
DFB→DSB
TAKE WORD
DSB INI COND+400
DDC CLEAR
OVER FLOW
PARITY
PAR ERROR
WRITE DATA
DATA READ
R PARITY
PE→ACO
ALL DIODES ARE 670-1 UNLESS OTHERWISE STATED
-30V FROM 1E24X
DFB→DSB
DSB INI CONT
DS BS
DFB→DSB
DRAWN B.LUMPKIN 5-27-65
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE DFB, DSB REGISTER AND CONTROL
CODE BS
DRWG NO E-RM08-0-3
SHEET 1 OF 1


CODE BS
DRWG. NO. D-RM08-0-4
REV. LTR. A
22 PIN AMP
1A4
1A3
1A2
IC 91
IC 99
ID 71
ID 79
ID 82
IE 62
3.3K
DE→AC1
FLAG
FLAG→INT
IO SKIP
READ B
WRITE B
DATA IN
READ
WRITE
IDLE
TRA
ACT
COMP FLAG
RQ
READ/WRITE
ER SYNC
DE
DDC CLEAR
DSB CONTROL
POWER CLR
ADD+MA
TAKE WORD
ER SYNC
200 µS
SNCOV
BLOCK
SC=SA
ACT
SNCOV
READ STROBE
DELAY 0.25µS
33 PUF
100Ω
ØA
ØB
3.4µS BLOCK
12µS DATA
J1 INNER CABINET
50 PIN AMP
SHIELD
START
FINISH
C TAP
CLOCK TRACK
SA 1537 IC1
PG 1410 IC3
MAINT SW
READY
DATA
DRUM POWER CLEAR
DDC CLEAR TO (IE11W)
CK CLR
NOTE
SEE CL-250-0-14 FOR ALL CLOCK TRACK WIRING
4605 IE7
4605 IE8
4605 IE9
60
61
62
IF2
IF3
IF4
IF5
IF6
IF8
A 169
REVISIONS
DRAWN B.LUMPKIN DATE 5-27-65
CHECKED
ENG
PROJ ENG
PROD
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
ASSY NO
SHEET OF
TITLE DRUM CONTROL DATA CHANNEL
FOR
CODE BS
DRWG. NO. D-RM08-0-4
REV. LTR. A
DIST.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REV. LTR.
22 PIN AMP 1A4
IC91
RES ARE 3.3K 1/4W
1D71
4102 C12
4217* 1D16
COMP DCL 0
COMP DCL 1
COMP DCL2
6624
4102 1C18
6602
6604
4604 1D15
PA
SET + FR
DCL CLR
AC 6
AC 7
AC 8
4217 1D17
4217 1D18
4217 1D19
IF1
IF2
AC 0
AC 1
AC 2
AC 3
AC 4
AC 5
AC 6
AC 7
AC 8
AC 9
AC 10
COMP AC 11
COMP DCL 14
22 PIN AMP 1A3
IC99
RESISTORS ARE 3.3 K
1D79
4604 1D15
4217 1D21
DTA 2
DTA 3
DTA 4
DTA 5
DTA 6
DTA 7
SA 0
SA 1
SA 2
SA 3
SA 4
SA5
DTA 0
DTA 1
DTA 0 2 (1D21K)
6611
6614
4217 1D22
4217 1D23
4215 1C23
4217 1C25
6601
DCL CLR
4604 1C11
DATA 0
CK
CLR
4225 1D25
SC 0
SC 1
SC 2
SC 3
SC 4
SC 5
+1 SC
4141 1C24
SA2(1)
SC2(0)
SA2(0)
SC2(1)
SA3(1)
SC3(0)
SA3(0)
SC3(1)
SA4(1)
SC4(0)
SA4(0)
SC4(1)
SA5(1)
SC5(0)
SA5(0)
SC5(1)
6113 1D24
4102 J 1C12
SC ≠ SA
SC = SA
SC = SA
LO0
LO2
LO1
LO3
DTA 0 4
DTA 0 5
WRITE
4114 J 1D20
IC6 6102
DRA
COMP DCL 14
4217 J 1D09
ACT
DE0 PE0
4127 C16
COMP DCL 0
COMP DCL 1
COMP DCL 2
DCL 1(0)
DCL 2(0)
DCL 3(0)
ERROR SYNC0
FR0
FR1
* THIS MODULE USED WITH COMPUTER EXTENDED MEMORY ONLY.
DRAWN B.L.UMPKIN 5-28-65
CHECKED 11/17/65
ENG 11/17/65
PROJ ENG 11/17/65
PROG 11/17/65
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DCL DTA, SA & SC REGS & CONTROL SERIAL DRUM
FOR
ASSY NO
CODE BS DRWG. NO. D-RM08-0-5 REV. LTR.
SHEET OF
DIST.
REVISIONS REV. LTR. ECO. NO. DATE ENG

CODE: UML | DRWG. NO.: D-RM08-0-6 | REV. LTR.:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	1537	W505 4912	1410	4303	4217	6102-145	4127	4112-677	4182-477	4115-17	4604	4102	4303	4604	1304	4127-67	4604	6102-161	4604	4401	4220-377	4222-77	4215+X	4141-R	4127
A	CLOCK READER	OPTION LOW VOLTAGE DETECTOR	TIME CHAIN	DONE START	RQ	RQB	I→RQ	I→FLAG	IDLE	IDLE	0→SEC CTR	PAR ERROR	BLOCK	ØA	READ STROBE	DSB→DFB	0→SNC	SET IDLE	6612D	DRUM POWER CLEAR	FIELD REG	SNCOV	DTA0	COMPUTER SC=SA	I→READY
						0-DSBF			DATA IN			0→AC 6612				T2D		0→DSBS			FIELD REG	SNC0			+1→SNC
					R/W	READ ◆	0→REQ	0→ERROR SYNC	0→PE			PWR CLR						DCL0B			SN 0	SNC1	DTA1		I→DTA0
						WRITE ◆	I→ERROR SYNC	COMP R PARITY	0→DSBS	TRA	ØB	COMP WD		TIME CHAIN		0→ERROR SYNC	SET	DCL1B	T2D		SN 1	SNC2			I→DTA1
1C						SC SYNC			DSB IN COND + 1US			0→DCL 0, 2						DCL2B			SN 2	SNC3	SC SYNC		SC SYNC
					ERR SYNC	SC SYNC	I→DATA ERROR	WRITE OVERFLOW	TRA	ACT		+1 SNC				DCL0		0→AC 6602			SN 3				
						SC SYNC	I-START	READ TW	ACT		DDC CLEAR	SC SYNC				DCL1	SPARE	6604 0→AC	INC SN		SN 4	SNC4			SC SYNC
B					DATA ERROR	0→READY			FLAG	FLAG		I→TRA		ØB + ACT ÷		DCL2		6614 0→AC					READY		
						+I→DCL	I-FLAG	I→ACT	FLAG TO INTERRUPT			SC=SA ◇						6602 AC→DCL			SN 5	SNC5			SC SYNC
	6110	4216	4216	4216	6106-17	4127	4604	4606	4127-53	6115-12	4217	4127-02	4301	6113	4604	4217 *	4217	4217	4127	4114-74	4217	4217	4217	6113-01	4225
	DETECT OVERFLOW CONDITION	DSB_3	DSB_7	DSB_{11}	OPTION VOLTAGE DETECTION	I→DSB_{11}	DSB CLEAR	DFB→DSB	TIME CHAIN	WRITE $DATA^0$	OVER FLOW	0→OVERFLOW	DELAY 6614	SC→AC_{11}	CLR DCL	NOT USED	DCL 3	DCL 7	DCL 11	LO 0	DTA 2	DTA 6	SA 2	SC=SA	
					0 SNCOV	0-DSB_S			READ TW					SC→AC_{10}										SC=SA	SC_0
		DSB_2	DSB_6	DSB_{10}	DSB_S^0	0-DSB_S	DSB INI COND	TAKE WORD	6614 + READ		R PARITY	I-OVERFLOW		SC→AC_9	AC→DCL	DCL 0	DCL 4	DCL 8	DCL 12	LO 1	DTA 3	DTA 7	SA 3	SC=SA	SC_1
1D					DSB_S^1	READER TO DSB_S			SPARE			COMP R PARITY		SC→AC_8		DCL 1	DCL 5	DCL 9	DCL 13	LO 2	DTA 4	SA 0	SA 4	SC=SA	SC_2
					DSB_F^0	0→DSB_F			+1 ÷ SA	WRITE $DATA^0$	PAR ERROR	COMP R PARITY		SC→AC_7										PAR ERROR	SC_3
		NOT USED	DSB_4	DSB_8			DSB→DFB	SHIFT							CLR DTA	DCL 2	DCL 6	DCL 10	DCL 14	LO 3	DTA 5	SA 1	SA 5		SC_4
					DSB_F^1	I-DSB_F			0→DSB		WRITE DATA	I→TRA		SC→AC_6										TAKEWORD	SC_5
	1213	4127	1213	4127	1213	4606	4605	4605	4605	6113-01	4112-47	4531	4531	4531	4531	4530	4530	4530	4530	4530	4530	4530	4530	4529	1537
	DFB_0	I-DFB_0	DFB_4	I-DFB_6	DFB_8	0-DFB	10T 6601 10T 6602 6604	10T 6611 6614	10T 6621 6622 6624	DSB_{11}^0	PE AND DE	Y0	Y4	Y10	Y14	X0	X2	X4	X6	X10	X12	X14	X16	DATA WRITE	DATA READER
		I-DFB_1		I-DFB_7						DSB_{11}^1	0→PE														
	DFB_1	I-DFB_2	DFB_5	I-DFB_8	DFB_9	MB-DFB				FLAG TO IO SKIP	I→TRA	Y1	Y5	Y11	Y15										
1E	DFB_2	I-DFB_3	DFB_6	I-DFB_9	DFB_{10}					GOOD TRANSFER TO IO SKIP	ACT READY	Y2	Y6	Y12	Y16	X1	X3	X5	X7	X11	X13	X15	X17		
		I-DFB_4		I-DFB_{10}						PE TO AC	FORM CLEAR DDC														
	DFB_3	I-DFB_5	DFB_7	I-DFB_{11}	DFB_{11}	DRA				DE TO AC	I-PE	Y3	Y7	Y13	Y17										

NOTE:
* THESE MODULES USED ONLY WITH EXTENDED MEMORY SYSTEMS.

REVISIONS: REV. LTR. | ECO. NO. | DATE | ENG

DRAWN	B. LUMPKIN	DATE 5-12-65
CHECKED	J. E. Lowell	DATE 11/12/65
ENG	R. J. Fryd	DATE 11/12/65
PROJ ENG	R. J. Fryd	DATE 11/12/65
PROD	R. J. Fryd	DATE 11/12/65

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

ASSY NO

SHEET 1 OF 2

TITLE: UTILIZATION MODULE LIST

FOR

CODE: UML | DRWG. NO.: D-RM08-0-6 | REV. LTR.:

DIST.

BKE-2

CODE	DRWG. NO.	REV. LTR.
UML	D-RM08-0-6	

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IF	W021	W021	W021	W021	W021	W021	W028	W028	W021	W021	R107	R107																				
	BAC Ø-8	BAC 9-11 IOP B PWR CLR B T1 B T2A	BMB Ø-5	BMB 6-11	AC Ø-8	AC 9-11 0 AC INT.RQ. SKIP	DATA ADDR Ø-8 DCL 3 TO DCL 11 BUF	DATA ADDR 9-11 DCL 12 TO DCL 14 BUF TRANSFER DIRECTION BREAK REQ. ADDR ACCEPTED	DFB 0 TO DFB 8 BUF	DFB 9-11	DFB 0 BUF DFB 1 BUF DFB 2 BUF DFB 3 BUF DFB 4 BUF DFB 5 BUF	DFB 6 BUF DFB 7 BUF DFB 8 BUF DFB 9 BUF DFB 10 BUF DFB 11 BUF																				
	(ME 34)	(MF 34)	(ME 34)	(MF 35)	(PE 2)	(PF 2)	(PE 3)	(PF 3)	(PE 4)	(PF 4)																						
IH	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	R107	R107				W028																
	BAC Ø-8	BAC 9-11 IOP B PWR CLR B T1 B T2A	BMB Ø-5	BMB 6-11	AC Ø-8	AC 9-11 0 AC INT. RQ. SKIP	DATA ADDR Ø-8 DCL 3 TO DCL 11 BUF	DATA ADDR 9-11 DCL 12 TO DCL 14 BUF TRANSFER DIRECTION BREAK REQ ADDR ACCEPTED	DFB 0 TO DFB 8 BUF	DFB 9-11	DCL 3 BUF DCL 4 BUF DCL 5 BUF DCL 6 BUF DCL 7 BUF DCL 8 BUF	DCL 9 BUF DCL 10 BUF DCL 11 BUF DCL 12 BUF DCL 13 BUF DCL 14 BUF				DCL 0 TO DCL 2 BUF																
	(ME 34)	(MF 34)	(ME 35)	(MF 35)	(PE 2)	(PF 2)	(PE 3)	(PF 3)	(PE 4)	(PF 4)																						

REV. LTR.	ECO. NO.	DATE	ENG

REVISIONS

DRAWN	Maureen Marion	DATE 7/27/65
CHECKED	J. F. Carroll	DATE 11/12/65
ENG	R J Tyrol	DATE 11/12/65
PROJ ENG	R J Tyrol	DATE 11/12/65
PROD	R J Tyrol	DATE 11/12/65

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ASSY NO

SHEET 2 OF 2

TITLE UTILIZATION MODULE LIST

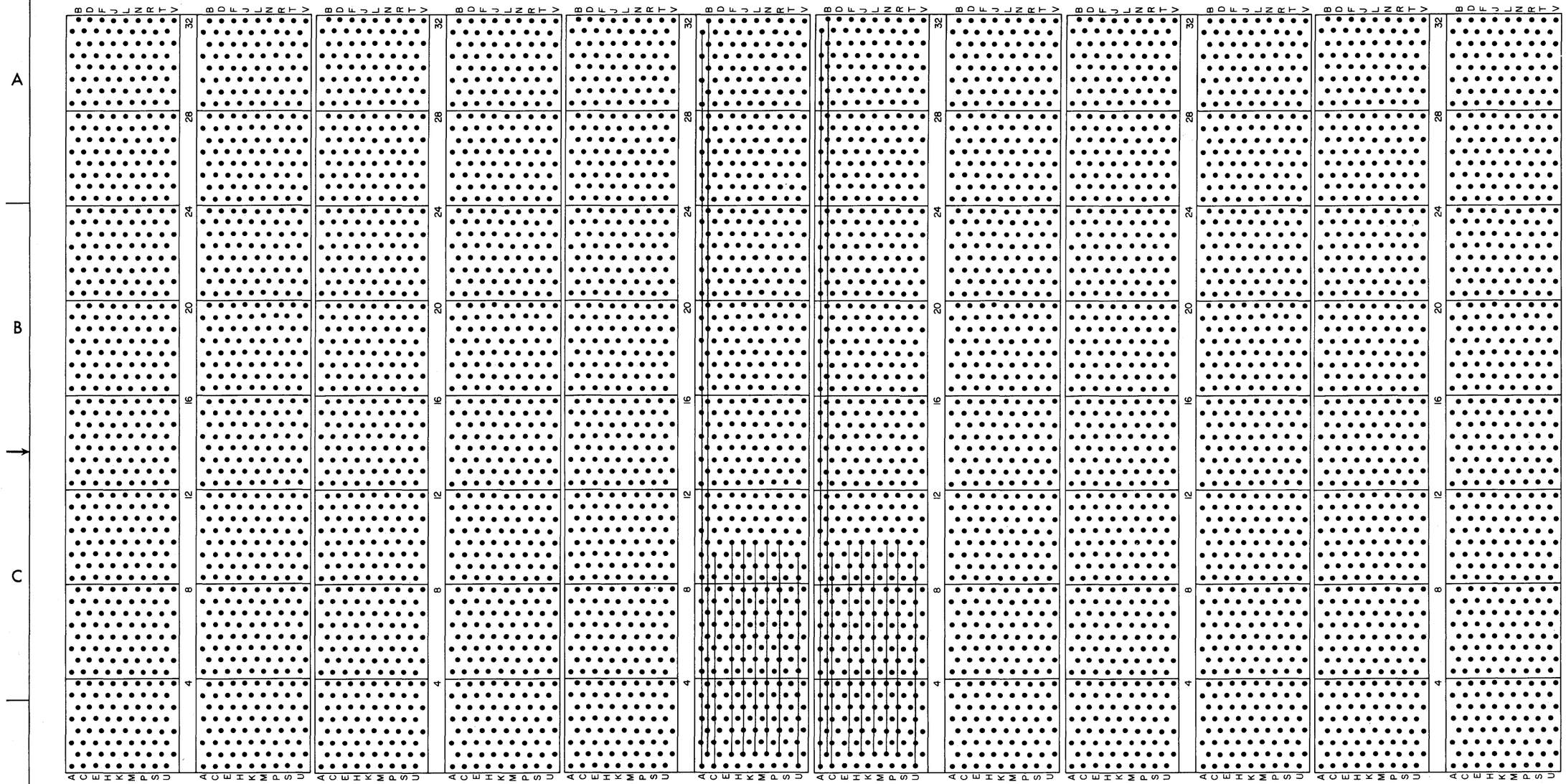
FOR

CODE	DRWG. NO.	REV. LTR.
UML	D-RM08-0-6	

DIST.

BKE-2

CODE	DRWG. NO.	REV. LTR.
WD	D-RM08-0-10	.



REV. LTR.	ECO NO.	DATE	ENG
REVISIONS			

DRAWN	B.LUMPKIN	DATE 5-12-65
CHECKED		DATE 6-1-65
ENG		DATE 11/10/65
PROJ. ENG		DATE 11/10/65
PROD		DATE 11/10/65

digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ASSY NO

SHEET 1 OF 1

TITLE
SERIAL DRUM
BUSS SCHEDULE

FOR

CODE	DRWG. NO.	REV. LTR.
WD	D-RM08-0-10	

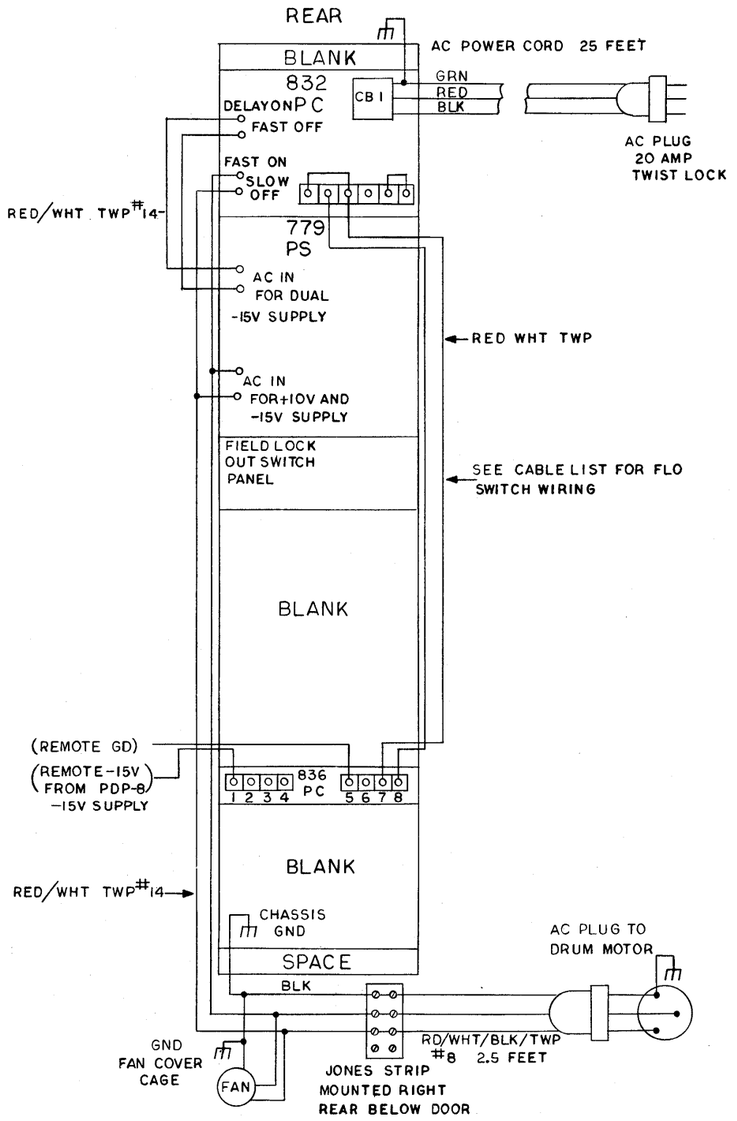
DIST.

BKE-2

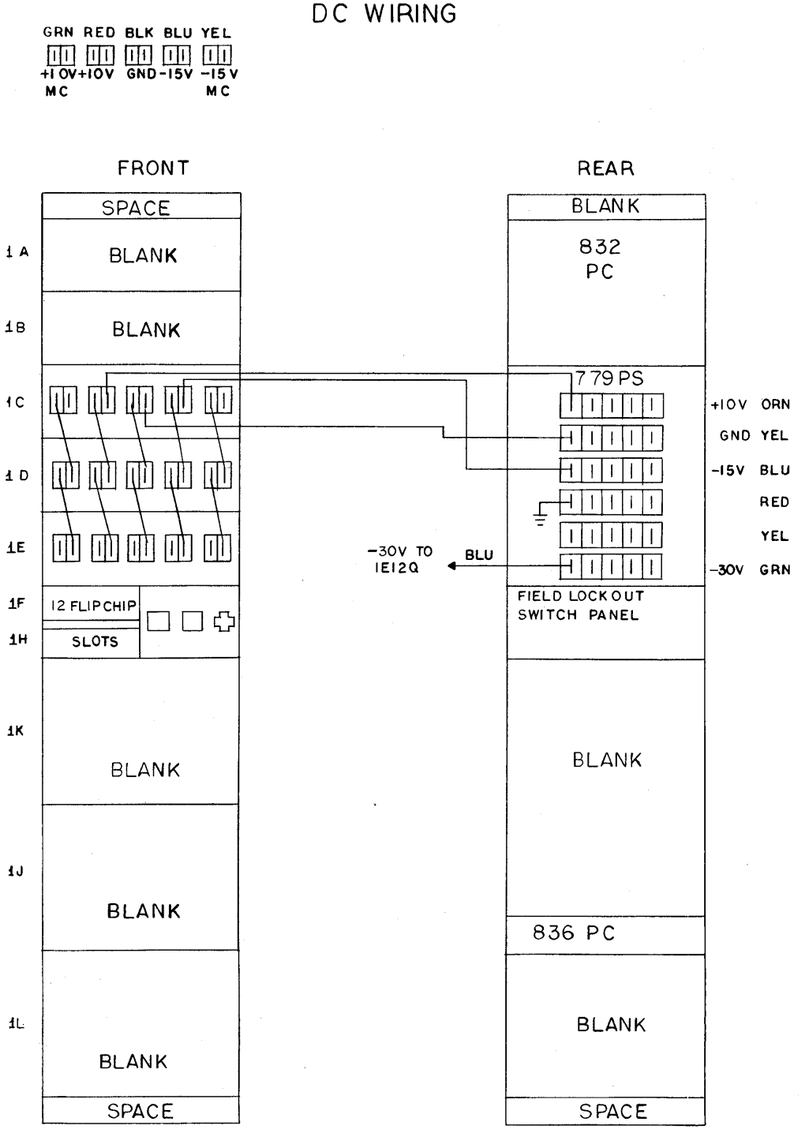
CODE	DRWG. NO.	REV. LTR.
PW	D-RM08-0-12	

AC WIRING

VIEW FACING REAR DOOR



DC WIRING



REVISIONS	REV. LTR.	ECO. NO.	DATE	ENG

DRAWN	B.LUMPKIN	5-11-65
CHECKED		6-1-65
ENG		11/12/65
PROJ ENG		11/12/65
PROD		11/12/65

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ASSY NO

SHEET OF

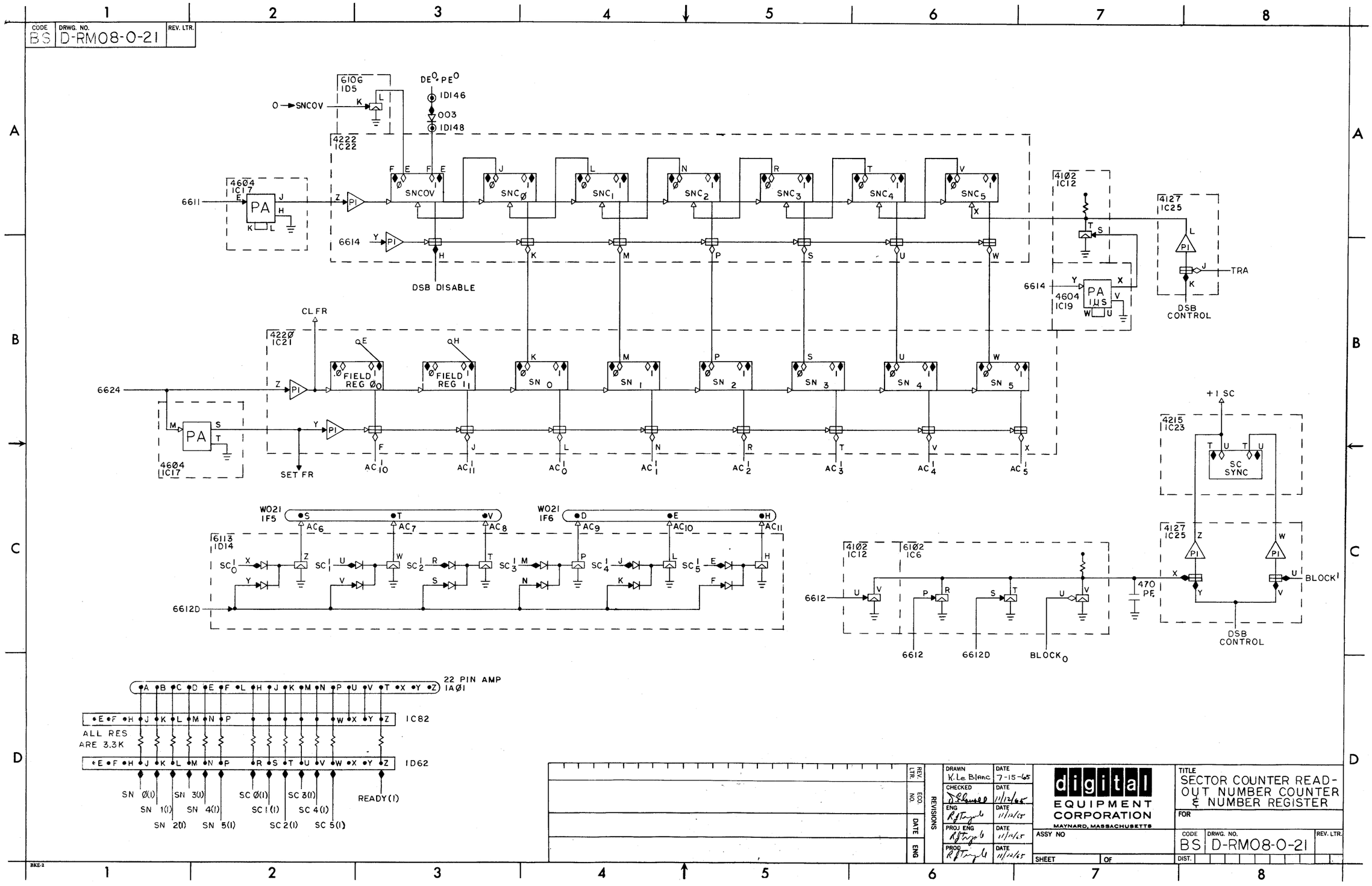
TITLE SERIAL DRUM
POWER WIRING

FOR

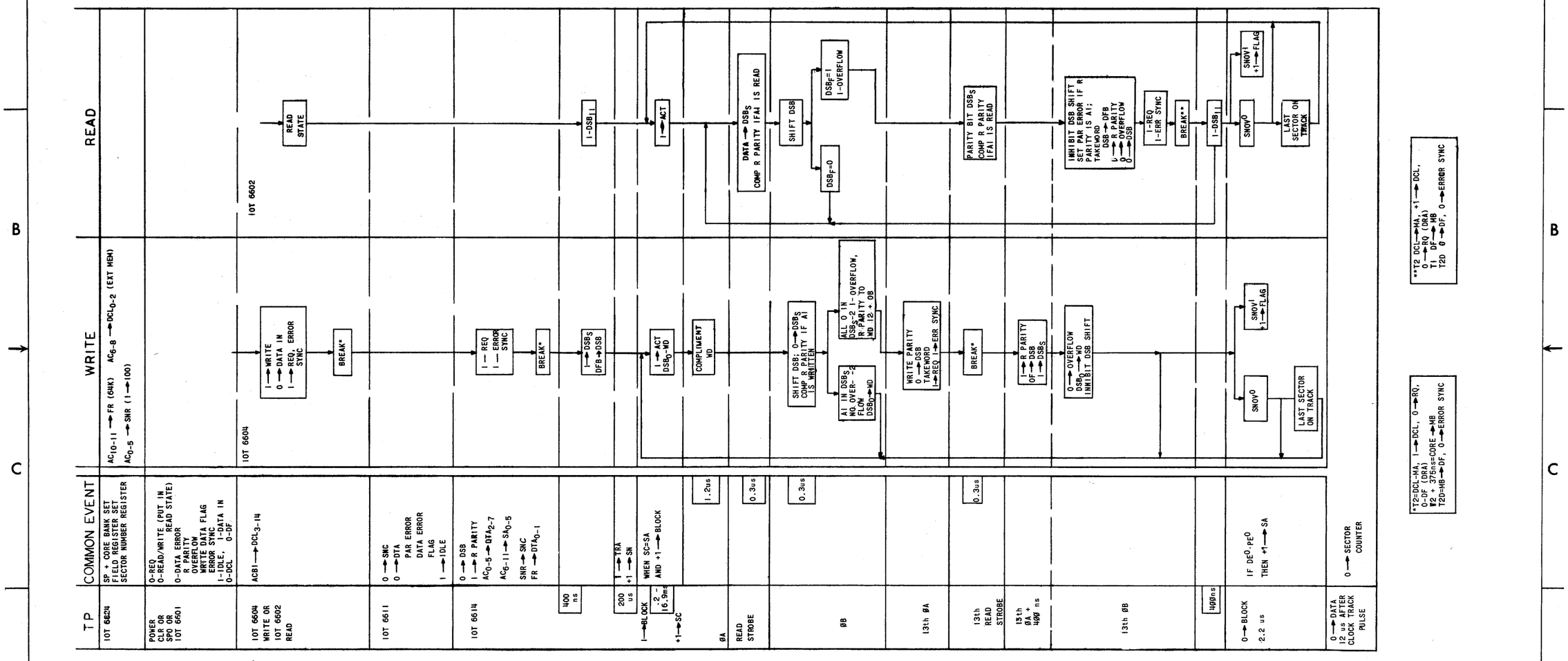
CODE	DRWG. NO.	REV. LTR.
PW	D-RM08-0-12	

DIST.

BKS-2


CODE BS
DRWG. NO. D-RM08-0-21
REV. LTR.
6106 1D5
0 → SNCOV
DE0 PE0
1D146
003
1D148
4222 1C22
4604 1C17
6611
PA
SNCOV
SNC0
SNC1
SNC2
SNC3
SNC4
SNC5
6614
DSB DISABLE
4102 1C12
4127 1C25
TRA
DSB CONTROL
4604 1C19
1μS
CL FR
4220 1C21
6624
FIELD REG 0
FIELD REG 1
SN 0
SN 1
SN 2
SN 3
SN 4
SN 5
SET FR
AC10
AC11
AC0
AC1
AC2
AC3
AC4
AC5
+1 SC
4215 1C23
SC SYNC
W021 1F5
W021 1F6
AC6
AC7
AC8
AC9
AC10
AC11
6113 1D14
SC0
SC1
SC2
SC3
SC4
SC5
6612D
4102 1C12
6102 1C6
6612
470 PF
BLOCK0
BLOCK1
DSB CONTROL
22 PIN AMP 1A01
1C82
1D62
ALL RES ARE 3.3K
SN 0(1)
SN 1(1)
SN 2(1)
SN 3(1)
SN 4(1)
SN 5(1)
SC 0(1)
SC 1(1)
SC 2(1)
SC 3(1)
SC 4(1)
SC 5(1)
READY(1)
REV. LTR.
ECO. NO.
DATE
ENG
REVISIONS
DRAWN K. Le Blanc DATE 7-15-65
CHECKED DATE 11/12/65
ENG DATE 11/12/65
PROJ ENG DATE 11/12/65
PROD DATE 11/12/65
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
ASSY NO
SHEET OF
TITLE SECTOR COUNTER READ-OUT NUMBER COUNTER & NUMBER REGISTER
FOR
CODE BS
DRWG. NO. D-RM08-0-21
REV. LTR.
DIST.
BKE-2

CODE FD | DRWG. NO. D-RM08-0-23 | REV. LTR.



NOTE:
IOT 6624 NEED ONLY BE GIVEN INITIALLY AND THEREAFTER ONLY WHEN THE NUMBER OF SECTORS, DRUM FIELD, OR MEMORY BANK NEED TO BE CHANGED.

REVISIONS	TRL REV.	ECO NO.	DATE	ENG

DRAWN E.FANCY	DATE 7-27-65	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHECKED	DATE	
ENG	DATE 11/12/65	
PROJ ENG	DATE 11/16/65	
PROD	DATE 11/16/65	

ASSY NO
SHEET OF

TITLE FLOW DIAGRAM
FOR
CODE FD | DRWG. NO. D-RM08-0-23 | REV. LTR.
DIST.

BKE-2

JACK [X] PLUG [ ]

FEMALE [X] MALE [ ]

LOCATION, LENGTH, ROUTE

1J3 OF PLUG PANEL

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED } TWP	1E16J	1	X0	RED } TWP	1E22J	26	X14
GRN }	H	2	X0	GRN }	H	27	X14
RED } TWP	Y	3	X1	RED } TWP	Y	28	X15
GRN }	1E16Z	4	X1	GRN	1E22Z	29	X15
RED } TWP	1E17J	5	X2	RED } TWP	1E23J	30	X16
GRN }	H	6	X2	GRN }	H	31	X16
RED } TWP	Y	7	X3	RED } TWP	Y	32	X17
GRN }	1E17Z	8	X3	GRN }	1E23Z	33	X17
RED } TWP	1E18J	9	X4	BLK	1E12E	34	Y0
GRN }	H	10	X4		L	35	Y1
RED } TWP	Y	11	X5		R	36	Y2
GRN }	1E18Z	12	X5		1E12V	37	Y3
RED } TWP	1E19J	13	X6		1E13E	38	Y4
GRN }	H	14	X7		L	39	Y5
RED } TWP	Y	15	X7		R	40	Y6
GRN }	1E19Z	16	X7		1E13V	41	Y7
RED } TWP	1E20J	17	X10		1E14E	42	Y10
GRN }	H	18	X10		L	43	Y11
RED } TWP	Y	19	X11		r	44	Y12
GRN }	1E20Z	20	X11		1E14V	45	Y13
		21			1E15E	46	Y14
RED } TWP	1E21J	22	X12		L	47	Y15
GRN }	H	23	X12		R	48	Y16
RED } TWP	Y	24	X13		1E15V	49	Y17
GRN }	1E21Z	25	X13	BLK	GND	50	GND

REV. LTR.	ECO. NO.	DATE	ENG.

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

50 PIN AMPHENOL

TITLE
SERIAL DRUM RM08
R/W HEAD SELECT
DRUM SIDE

DRAWN M. Mariano 5/13/65

FOR

CHECKED

ENG.

PROD.

CODE CL | DRWG. NO. A-RM08-0-15 | REV.

SHEET 1 OF 1

DIST.

JACK ☐ PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE [X]	J1 ON DRUM TO LOGIC

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED	1C1H	1	START	RED	1C1H	26	START
BLACK		2	CT CLOCK	BLACK		27	CT CLOCK
GREEN	F	3	FIN. #1	GREEN	F	28	FIN. #7
SHIELD	GND	4	GND	SHIELD	GND	29	GND
RED	H	5	START	RED	H	30	START
BLACK		6	CT CLOCK	BLACK		31	CT CLOCK
GREEN	F	7	FIN. #2	GREEN	F	32	FIN. #8
SHIELD	GND	8	GND	SHIELD	1C1GND	33	GND
RED	H	9	START			34	
BLACK		10	CT CLOCK	NOTE		35	
GREEN	F	11	FIN. #3	TAPER PIN	CONNECTION	36	
SHIELD	GND	12	GND	AT PLUG END. USE TRIPLE		37	
RED	H	13	START	CONDUCTOR SHIELDED WIRE		38	
BLACK		14	CT. CLOCK	EXAMINING ALL OUTPUTS		39	
GREEN	F	15	FIN. #4	AND INITIALLY USE HEAD		40	
SHIELD	1C1GND	16	GND	WITH HIGHEST OUTPUT.		41	
		17		JUMPER IN OTHERS AS		42	
RED	1C1H	18	START	NEEDED. PLUG END MUST		43	
BLACK		19	CT CLOCK	NOT BE CONNECTED WHILE		44	
GREEN	F	20	FIN. #5	WIRING LOGIC END.		45	
SHIELD	GND	21	GND			46	
RED	H	22	START			47	
BLACK		23	CT CLOCK			48	
GREEN	F	24	FIN. #6			49	
SHIELD	1C1GND	25	GND			50	

REV. LTR.	ECO. NO.	DATE	ENG.

digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

50 PIN AMPHENOL

TITLE: SERIAL DRUM RM08
CLOCK RACK PLUG

DRAWN: M. Mariano 5/13/65
CHECKED:
ENG.:
PROD.:

FOR:

CODE	DRWG. NO.	REV.
CL	A-RM08-0-16	

SHEET 1 OF 1

DIST.:

JACK ☐ PLUG [X]

FEMALE ☐ MALE [X]

LOCATION, LENGTH, ROUTE

J3 PLUG PANEL TO J2 DRUM CABLE 16" INSIDE DIMENSION

COLOR	PIN MALE	PIN MALE	NAME	COLOR	PIN	PIN	NAME
RED } TWP	1	1	X0	RED } TWP	26	26	X14
GRN }	2	2	X0	GRN }	27	27	X14
RED } TWP	3	3	X1	RED } TWP	28	28	X15
GRN }	4	4	X1	GRN }	29	29	X15
RED } TWP	5	5	X2	RED } TWP	30	30	X16
GRN }	6	6	X2	GRN }	31	31	X16
RED } TWP	7	7	X3	RED } TWP	32	32	X17
GRN }	8	8	X3	GRN }	33	33	X17
RED } TWP	9	9	X4	BLK	34	34	Y0
GRN }	10	10	X4	↑	35	35	Y1
RED } TWP	11	11	X5	↑	36	36	Y2
GRN }	12	12	X5	↑	37	37	Y3
RED } TWP	13	13	X6	↑	38	38	Y4
GRN }	14	14	X6	↑	39	39	Y5
RED } TWP	15	15	X7	↑	40	40	Y6
GRN }	16	16	X7	↑	41	41	Y7
RED } TWP	17	17	X10	↑	42	42	Y10
GRN }	18	18	Y10	↑	43	43	Y11
RED } TWP	19	19	X11	↑	44	44	Y12
GRN }	20	20	X11	↑	45	45	Y13
WHT	21	21	SPARE	↑	46	46	Y14
RED } TWP	22	22	X12	↑	47	47	Y15
GRN }	23	23	X12	↑	48	48	Y16
RED } TWP	24	24	X13	↓	49	49	Y17
GRN }	25	25	X13	BLK	50	50	GND

REV. LTR.	ECO. NO.	DATE	ENG.

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

50 PIN AMPHENOL

TITLE: SERIAL DRUM RM08 SELECTION CABLE

DRAWN: M. Mariano 5/13/65

CHECKED

ENG.

PROD.

FOR

CODE: CL | DRWG. NO.: A-RM08-0-17 | REV.:

SHEET 1 OF 1

DIST.

COLOR	NAME	PIN	PIN	REMARKS
BLUE	PE^0-DE^0	1E11H	MAINT SW COMMON	
BLUE	PE^0-DE^0	1C09Q	MAINT SW NORM OPEN	
WHITE	LO^0	1D20K	SW 0 NORM OPEN	
WHITE	LO^1	1D20R	SW 1 NORM OPEN	
WHITE	LO^2	1D20V	SW 2 NORM OPEN	
WHITE	LO3	1D20Z	SW 3 NORM OPEN	
RED	LOF0	NORM CLOSED BUS SW 0,SW 1,SW2,SW3		
RED	LOF1	NORM CLOSED BUS SW4,SW5,SW6,SW7		
RED	LOF2	NORM CLOSED BUS SW 8 ,SW 9 ,SW10,SW11		
RED	LOF3	NORM CLOSED BUS SW12, SW13,SW14,SW15		
WHITE	LO0	NORM OPEN BUS SW 0-SW4-SW8-SW12		
WHITE	LO1	NORM OPEN BUS SW1-SW5-SW9-SW13		
WHITE	LO2	NORM OPEN BUS SW2-SW6-SW10-SW14		
WHITE	LO3	NORM OPEN BUS SW3-SW7-SW11-SW15		
NOTE:	D003 DIODES WILL	BE MOUNTED ONALL	SWITCHES, BAR END TO COMMON,	
	OTHER END TO NORM CLOSE POSITION.			
	LOF2	1E17K	SW11/NC	
	LOF3	1E17T	SW15/NC	
	LOF0	1E16K	SW3/NC	
	LOF1	1E16T	SW7/NC	
NOTE:	REFERENCE BS-E-250-0-6.			

REV. LTR.	ECO. NO.	DATE	ENG.
A	107	12/1/66	RJT

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DRAWN M. Mariano 5/13/65
CHECKED
ENG.
PROD.

GENERAL WIRING SHEET

TITLE FIELD LOCKOUT PANEL WIRING SERIAL DRUM RM08

CODE	DRWG. NO.	REV.
WS	A-RM08-0-18	A

SHEET 1 OF 1
DIST.

JACK [ ]	PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE [X]	MALE [ ]	1AØ4

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	1C91E	A	DCL 0	
W/BRN (Z)	F	B	1	
W/RED (R)	H	C	2	
W/ORN (O)	J	D	3	
W/YEL (Y)	K	E	4	
W/GRN (N)	L	F	5	
W/BLU (B)	M	H	6	
W/VIO (V)	N	J	7	
W/GRY (G)	P	K	8	
WHT (W)		L		
W/BLK (X)	1C91R	M	DCL 9	
W/BRN (Z)	S	N	10	
W/RED (R)	T	P	11	
W/ORN (O)	U	R	12	
W/YEL (Y)	V	S	13	
W/GRN (N)	W	T	14	
W/BLU (B)	1C91X	U	RQ	
W/VIO (V)	1C91Y	V	PAR ERR	
W/GRY (G)	1C91Z	W	DE	
WHT (W)		X		
		Y		
		Z		

DRAWN Maureen Mariano 8/5/65

CHECKED [signature] 11/12/65

ENG [signature] 11/12/65

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

22 PIN AMPHENOL

TITLE
DRUM CORE LOCATION
INDICATOR CABLE

APP'V

ECO. NO.
REV. LTR.

DWG NO A-RM08-0-24

REV. LTR.

SHEET OF

CODE CL

JACK ☐ PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE [X] MALE ☐	1AØ1

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	1C82J	A	SN 0	
W/BRN (Z)	K	B	1	
W/RED (R)	L	C	2	
W/ORN (O)	M	D	3	
W/YEL (Y)	N	E	4	
W/GRN (N)	P	F	5	
W/BLU (B)	R	H	SC Ø	
W/VIO (V)	S	J	SC 1	
W/GRY (G)	T	K	SC 2	
WHT (W)		L		
W/BLK (X)	1C82U	M	SC 3	
W/BRN (Z)	V	N	4	
W/RED (R)	W	P	5	
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)	1C82Z	T	READY 1	
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

DRAWN Maureen Mariano 8/5/65

CHECKED [illegible] 11/2/65

ENG [illegible] 11/2/65

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

APP'V

ECO. NO. REV. LTR.

22 PIN AMPHENOL

TITLE
DRUM SECTOR COUNTER
INDICATOR CABLE

DWG NO A-RM08-0-25

REV. LTR.

SHEET OF

CODE CL

JACK [ ]	PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE [X]	MALE [ ]	1AØ2

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	1D82J	A	DFB 0	
W/BRN (Z)	K	B	1	
W/RED (R)	L	C	2	
W/ORN (O)	M	D	3	
W/YEL (Y)	N	E	4	
W/GRN (N)	P	F	5	
W/BLU (B)	R	H	6	
W/VIO (V)	S	J	7	
W/GRY (G)	T	K	8	
WHT (W)		L		
W/BLK (X)	1D82U	M	DFB 9	
W/BRN (Z)	V	N	10	
W/RED (R)	W	P	11	
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

DRAWN Maureen Mariano 8/5/65

CHECKED [illegible] 11/12/65

ENG [illegible] 11/12/65

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

22 PIN AMPHENOL

TITLE
DRUM FINAL BUFFER
INDICATOR CABLE

APP'V

ECO. NO.
REV. LTR.

DWG NO A-RM08-0-26

REV. LTR.

SHEET OF

CODE CL

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☒ MALE ☐	1AØ3

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)		A		
W/BRN (Z)	1C99H	B	DTA 0	
W/RED (R)	1C99T	C	DTA 1	
W/ORN (O)	1C99K	D	DTA 2	
W/YEL (Y)	1C99E	E	DTA 3	
W/GRN (N)	1C99M	F	DTA 4	
W/BLU (B)	1C99N	H	DTA 5	
W/VIO (V)	1C99P	J	DTA 6	
W/GRY (G)	1C99R	K	DTA 7	
WHT (W)		L		
W/BLK (X)	1C99S	M	SA Ø	
W/BRN (Z)	1C99T	N	SA 1	
W/RED (R)	1C99U	P	SA 2	
W/ORN (O)	1C99V	R	SA 3	
W/YEL (Y)	1C99W	S	SA 4	
W/GRN (N)	1C99X	T	SA 5	
W/BLU (B)	1C99F	U	IDLE	
W/VIO (V)	1C99Y	V	READ	
W/GRY (G)	1C99Z	W	WRITE	
WHT (W)		X		
		Y	-15V	
		Z	GND	

DRAWN Maureen Mariano 8/5/65

CHECKED

ENG

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

22 PIN AMPHENOL

TITLE
DRUM TRACK ADDRESS
INDICATOR CABLE

APP'V

ECO. NO. REV. LTR.

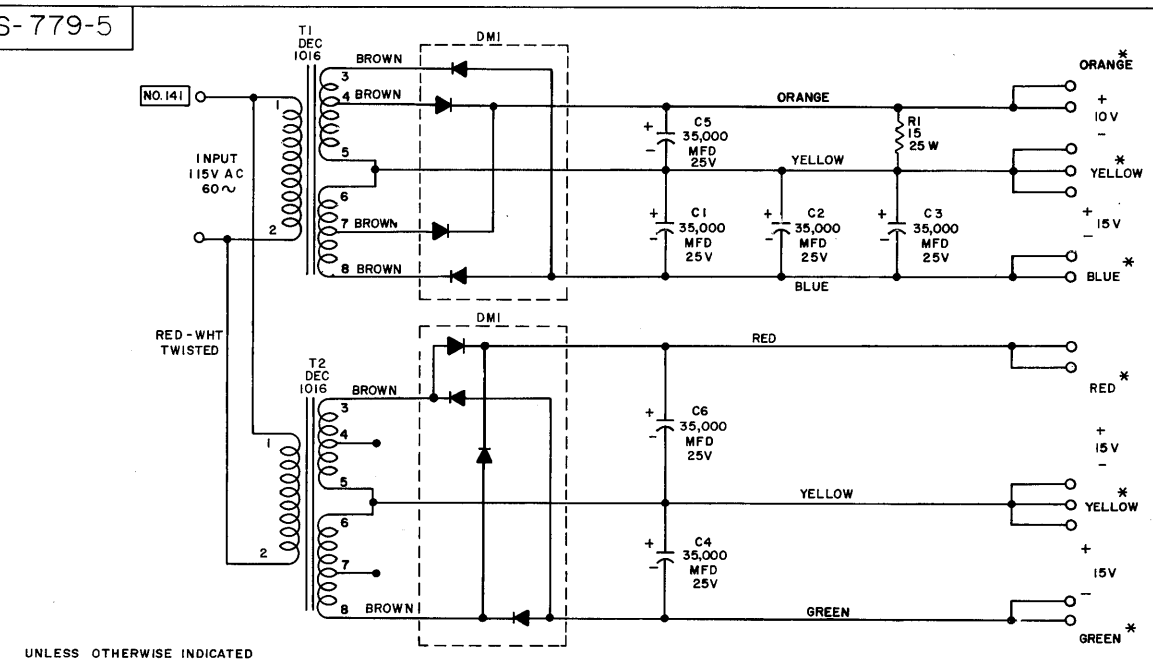
DWG NO A-RM08-0-27

REV. LTR.

SHEET OF

CODE CL

CS-779-5



UNLESS OTHERWISE INDICATED
* HEYMAN MFG CO TAB - TERMINAL IN PLASTIC BUSHING
CINCH JONES TERMINAL STRIP

CHANGE	CH NO	APP	EXPER	DRAWN	digital EQUIPMENT CORPORATION MAYNARD·MASSACHUSETTS	CS-779-5
	5098-3		PRODUCTION	J.S. CARO 2-13-63		
	4925-4			CHECKED		
	4018-3		OTHER	ENGINEER	POWER SUPPLY 779	
	3482-2					
	3246-1					

SIZE	CODE	NUMBER	REV
B	CS	836-0-2	B

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
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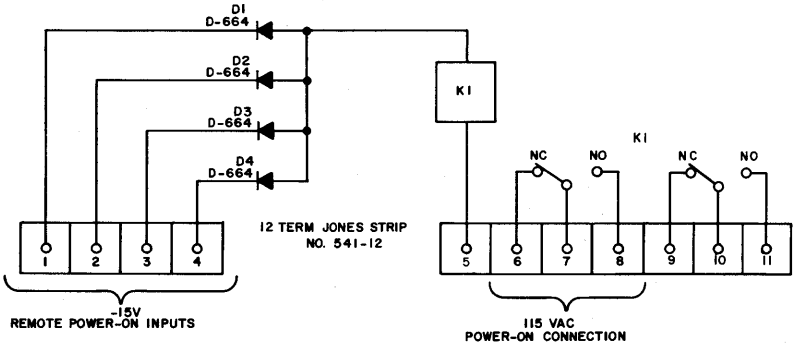


NOTES:
K1 MAGNICRAFT RELAY; CAT. NO. 66CSX-7 WITH DUST COVER.

REVISIONS			
CHK	CHG NO	REV	
DAW	4376	1	
REV	& REDR	B	
	5448		

DRN.	H PORTER	DATE 10-7-64
CHK'D	N PERRYMAN	DATE 10-15-64
ENG.	L WHITE	DATE 10-15-64
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N3606		

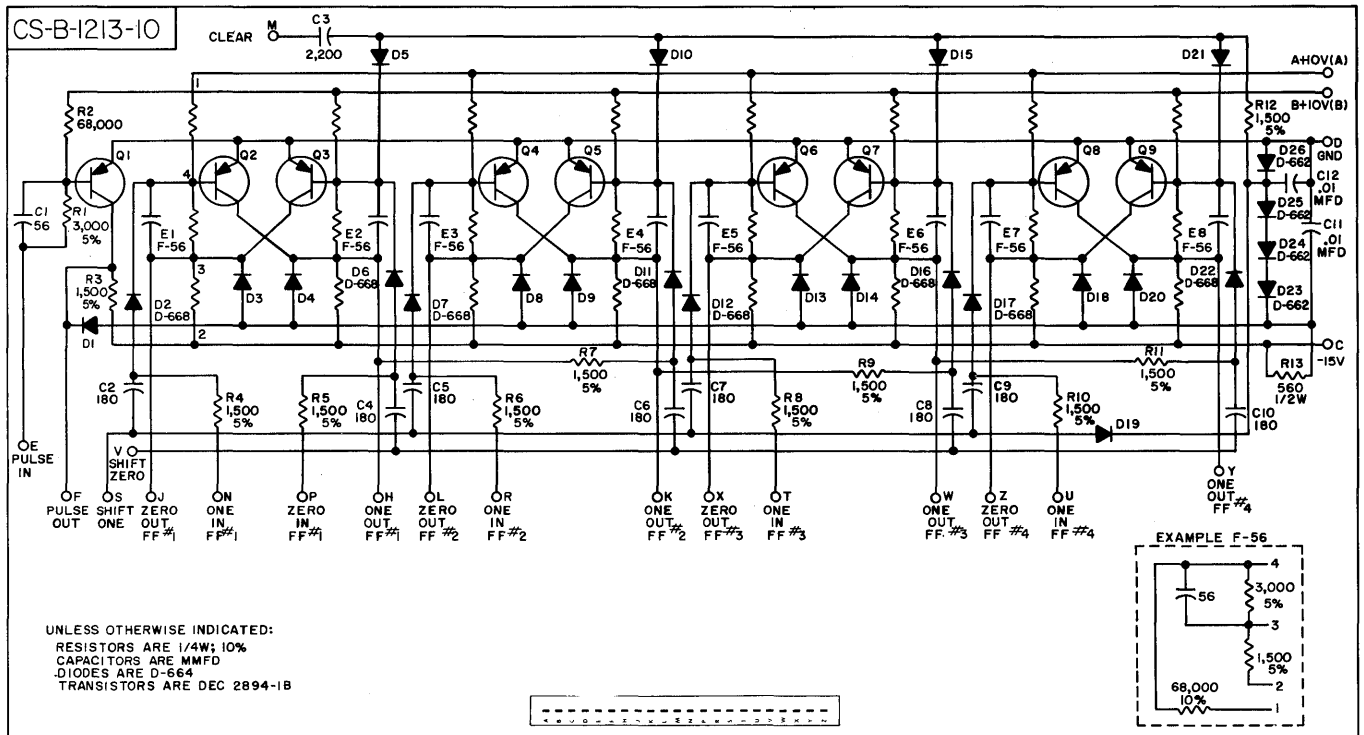
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE DC REMOTE POWER CONTROL 836

SIZE	CODE	NUMBER	REV
B	CS	836-0-2	B

PRINTED CIRCUIT REV.

DEC FORM NO. DRB 102



REVISIONS																
5710-10	4144-9 REDRAWN AND REVISED	3239-8 D.A.W. 3/63 REVISED AND REDRAWN	2963-7 R.L.B. 10-62	2841-6 R.L.B. 9-62	2374-5 R.L.B. 10-61	2293-4 R.L.B. 9-61	1873-3 R.L.B. 12-14-62	1581-2 R.L.B.	1538-1 R.L.B.	ECO. NO.	ENG.	REVISIONS	DRAFTSMAN A. OUELLETTE DATE 8-18-64	CHECKER A.V. DATE 3-25-63	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	CODE CS	DWG. NO. B-1213	REV. 10
													ENGINEER R L BEST DATE	PRODUCTION DATE	TITLE QUADRUPLE FLIP-FLOP 1213			

SIZE	CODE	NUMBER	REV.
B	CS	1304-0-1	AB

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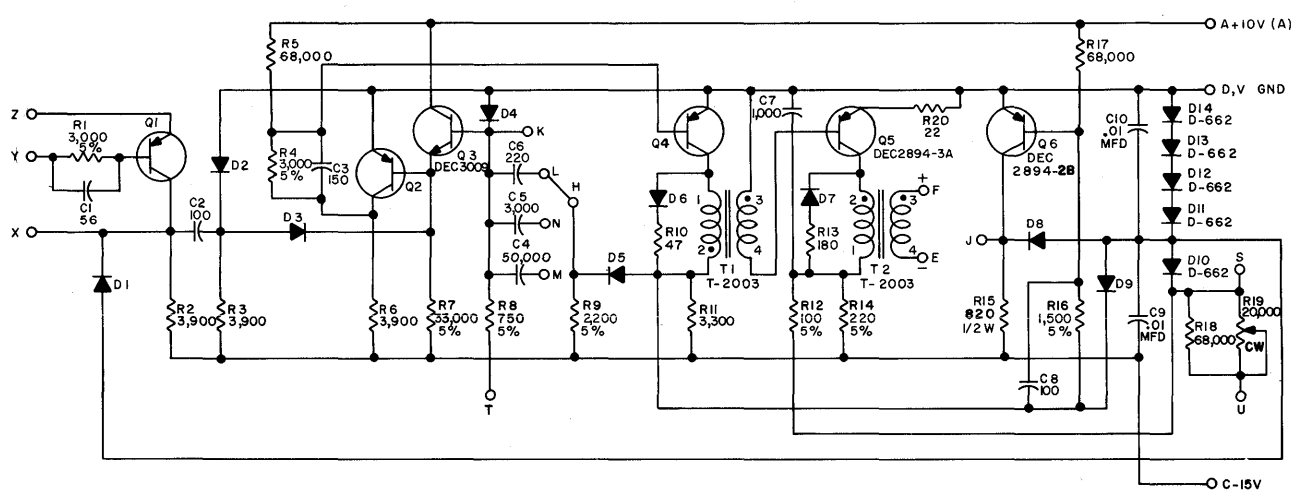


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 2894-1B
CAPACITORS ARE MMFD
RESISTORS ARE 1/4W, 10%
DIODES ARE D-664
R19 IS A #275P

REVISIONS																
CHK	CHG NO.	REV.														
RLB	4689	20														
REV.	& REDR.	Z														
	5894	AA														
	6258	AB														

DRN. I. HAHN	DATE 3-28-63	TRANSISTOR & DIODE CONVERSION CHART	
CHK'D A.VARTANIAN	DATE 3-28-63	DEC	EIA
ENG. D.A.WHITE	DATE 3-28-63	DEC2894-1B	NONE
PROD.	DATE	DEC2894-2B	NONE
		DEC2894-3A	NONE
		DEC3009	2N3009
		D662	1N645
		D664	1N3606

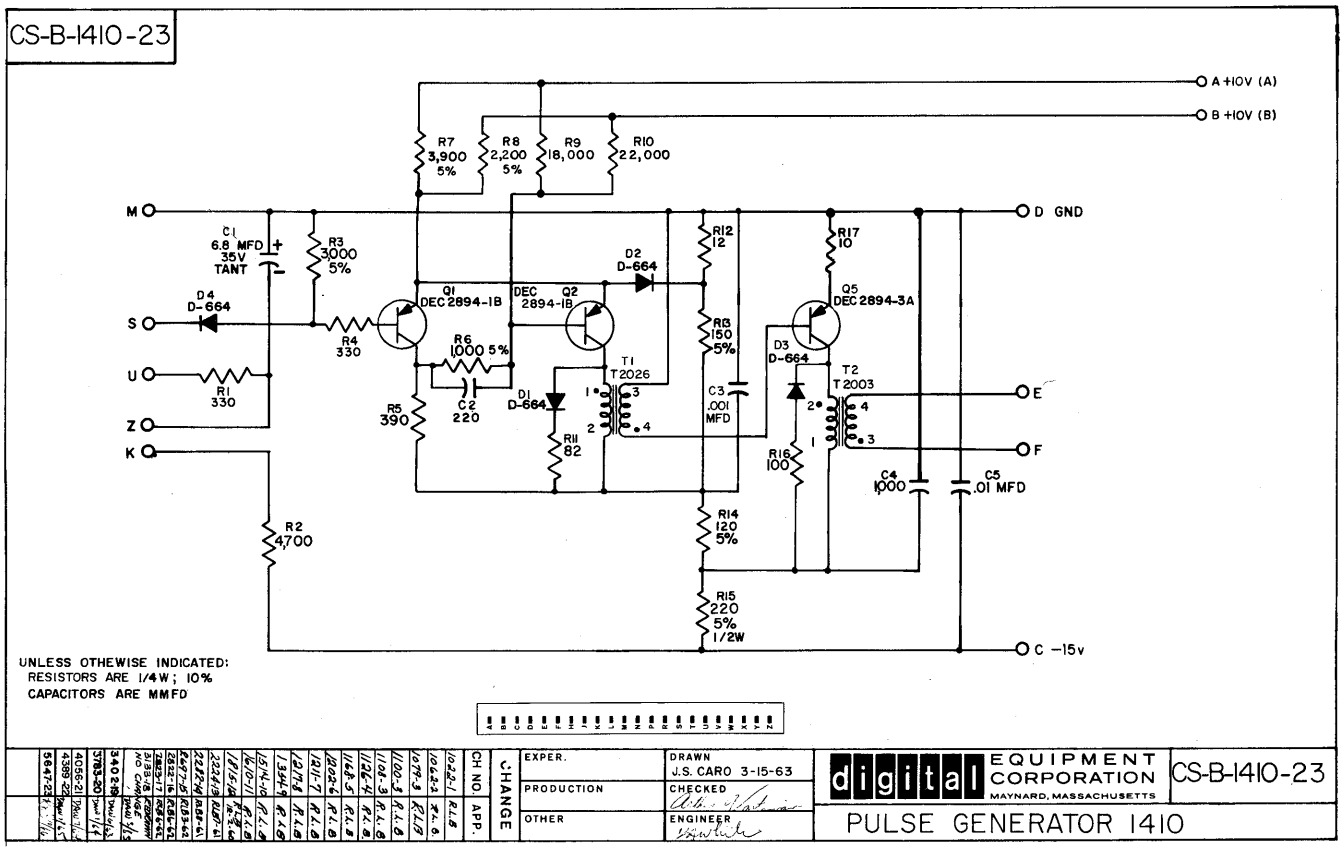
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

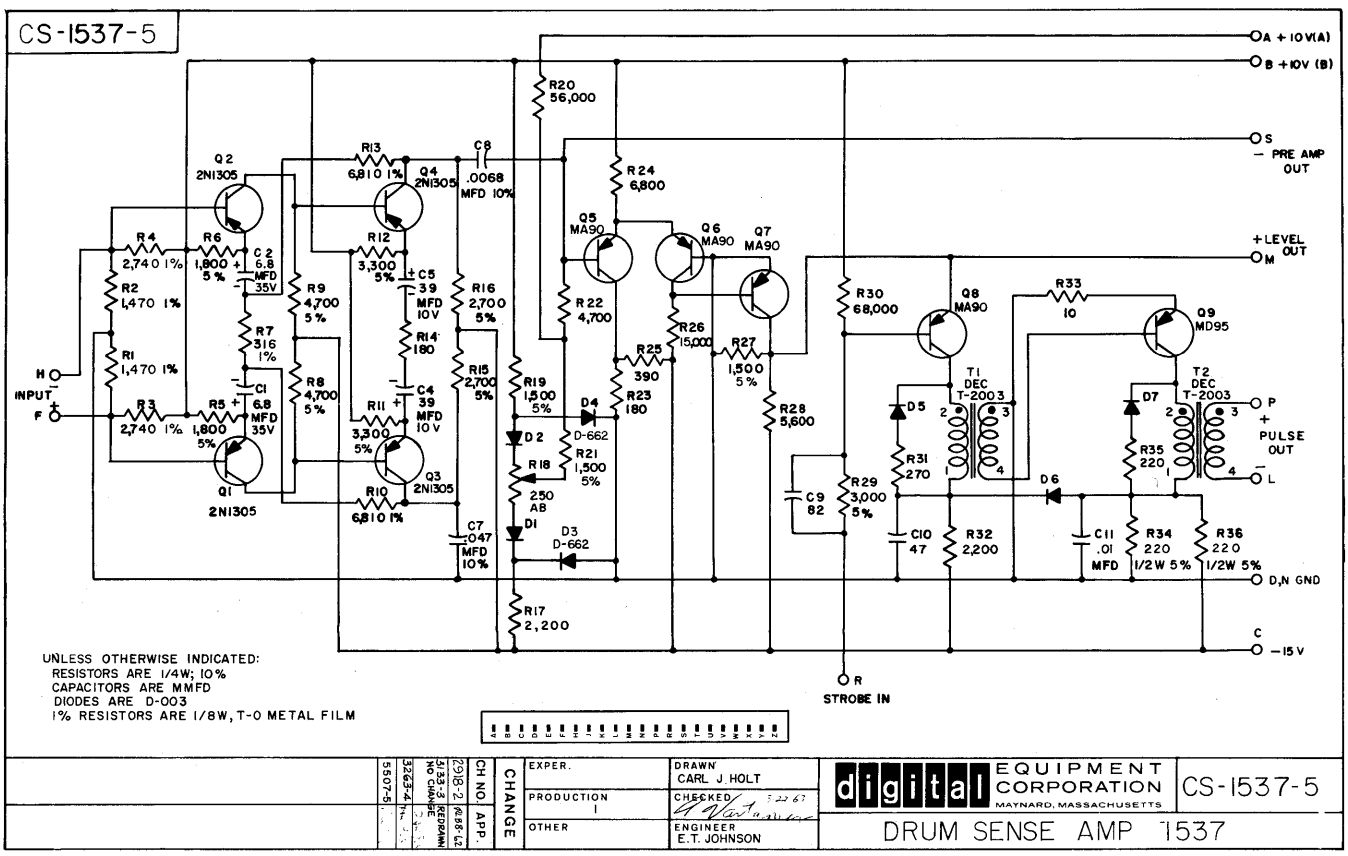
TITLE DELAY 1304

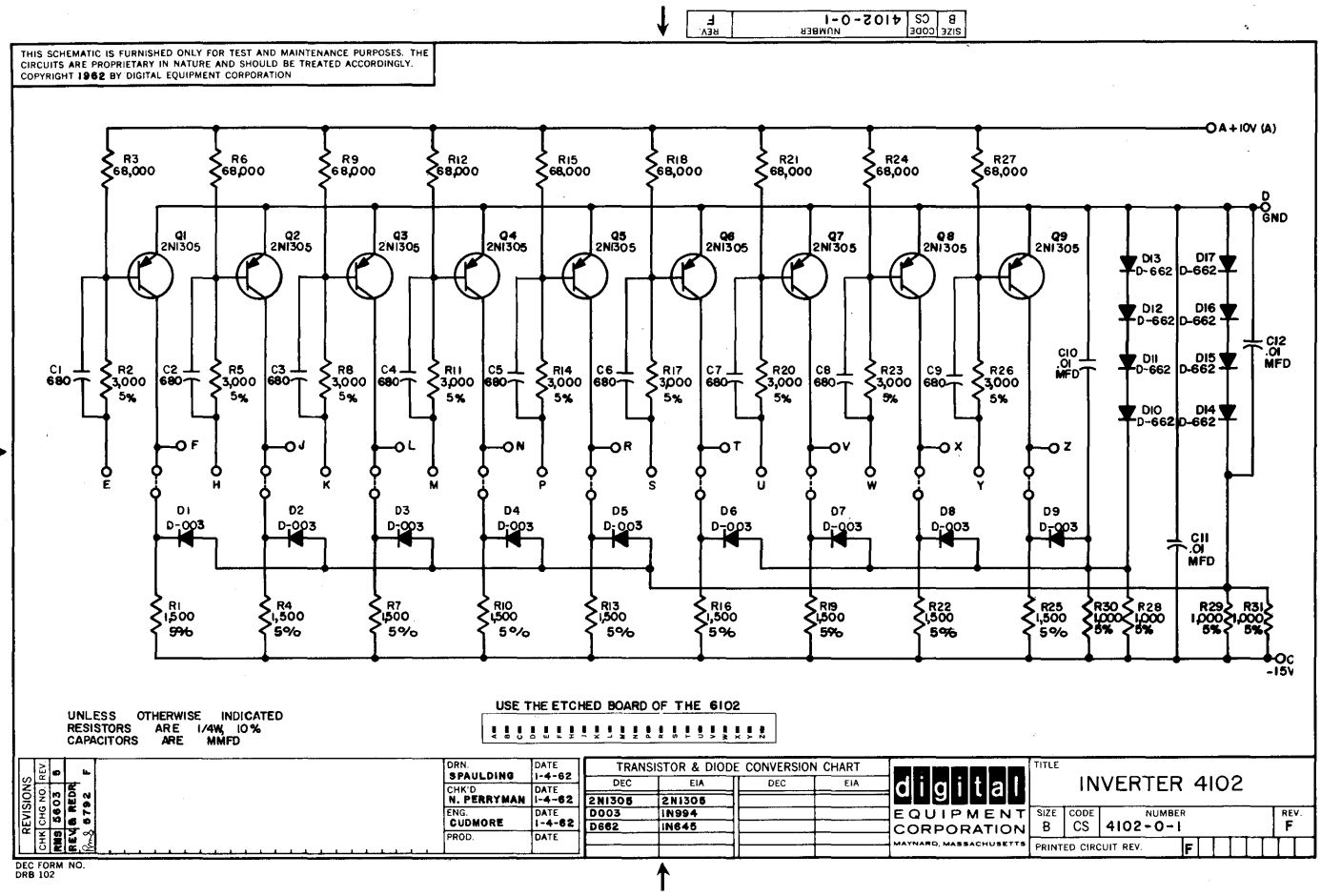
SIZE	CODE	NUMBER	REV.
B	CS	1304-0-1	AB

PRINTED CIRCUIT REV. K

DEC FORM NO. DRB 102


CS-B-1410-23
A +10V (A)
B +10V (B)
R7 3,900 5%
R8 2,200 5%
R9 18,000
R10 22,000
M
D GND
C1 6.8 MFD 35V TANT
R3 3000 5%
D4 D-664
S
U
Z
K
R1 330
R4 330
Q1 DEC 2894-1B
Q2 DEC 2894-1B
D2 D-664
R6 1,000 5%
C2 220
R5 390
D1 D-664
R11 82
T1 T2026
R12 12
R13 150 5%
C3 .001 MFD
R17 10
Q5 DEC 2894-3A
D3 D-664
T2 T2003
E
F
R16 100
C4 1000
C5 .01 MFD
R2 4,700
R14 120 5%
R15 220 5% 1/2W
C -15v
UNLESS OTHEWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
CHANGE
CH NO.
APP.
EXPER.
PRODUCTION
OTHER
DRAWN J.S. CARO 3-15-63
CHECKED
ENGINEER
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
CS-B-1410-23
PULSE GENERATOR 1410


CS-1537-5
A +10V(A)
B +10V (B)
R20 56,000
S
- PRE AMP OUT
Q2 2N1305
R13 6,810 1%
Q4 2N1305
C8 .0068 MFD 10%
R24 6,800
Q5 MA90
Q6 MA90
Q7 MA90
+LEVEL OUT
M
R4 2,740 1%
R6 1,800 5%
C2 6.8 MFD 35V
R12 3,300 5%
C5 39 MFD 10V
R16 2,700 5%
R22 4,700
R26 15,000
R30 68,000
Q8 MA90
R33 10
Q9 MD95
R2 1,470 1%
R9 4,700 5%
R14 180
R25 390
R27 1,500 5%
R7 316 1%
R1 1,470 1%
H
INPUT
F
R3 2,740 1%
R5 1,800 5%
C1 6.8 MFD 35V
R8 4,700 5%
R11 3,300 5%
C4 39 MFD 10V
R15 2,700 5%
R19 1,500 5%
D4 D-662
R23 180
R28 5,600
T1 DEC T-2003
T2 DEC T-2003
D5
D7
P
+ PULSE OUT
L
Q1 2N1305
Q3 2N1305
R10 6,810 1%
D2
R18 250 AB
R21 1,500 5%
R31 270
R35 220
C9 82
R29 3,000 5%
D6
C7 .047 MFD 10%
D1
D3 D-662
C10 47
R32 2,200
C11 .01 MFD
R34 220 1/2W 5%
R36 220 1/2W 5%
D,N GND
R17 2,200
C
-15V
R
STROBE IN
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-003
1% RESISTORS ARE 1/8W, T-0 METAL FILM
CHANGE
CH NO.
APP.
EXPER.
PRODUCTION
OTHER
DRAWN CARL J. HOLT
CHECKED
ENGINEER E.T. JOHNSON
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
CS-1537-5
DRUM SENSE AMP 1537



SIZE B CODE CS NUMBER 4102-0-1 REV F
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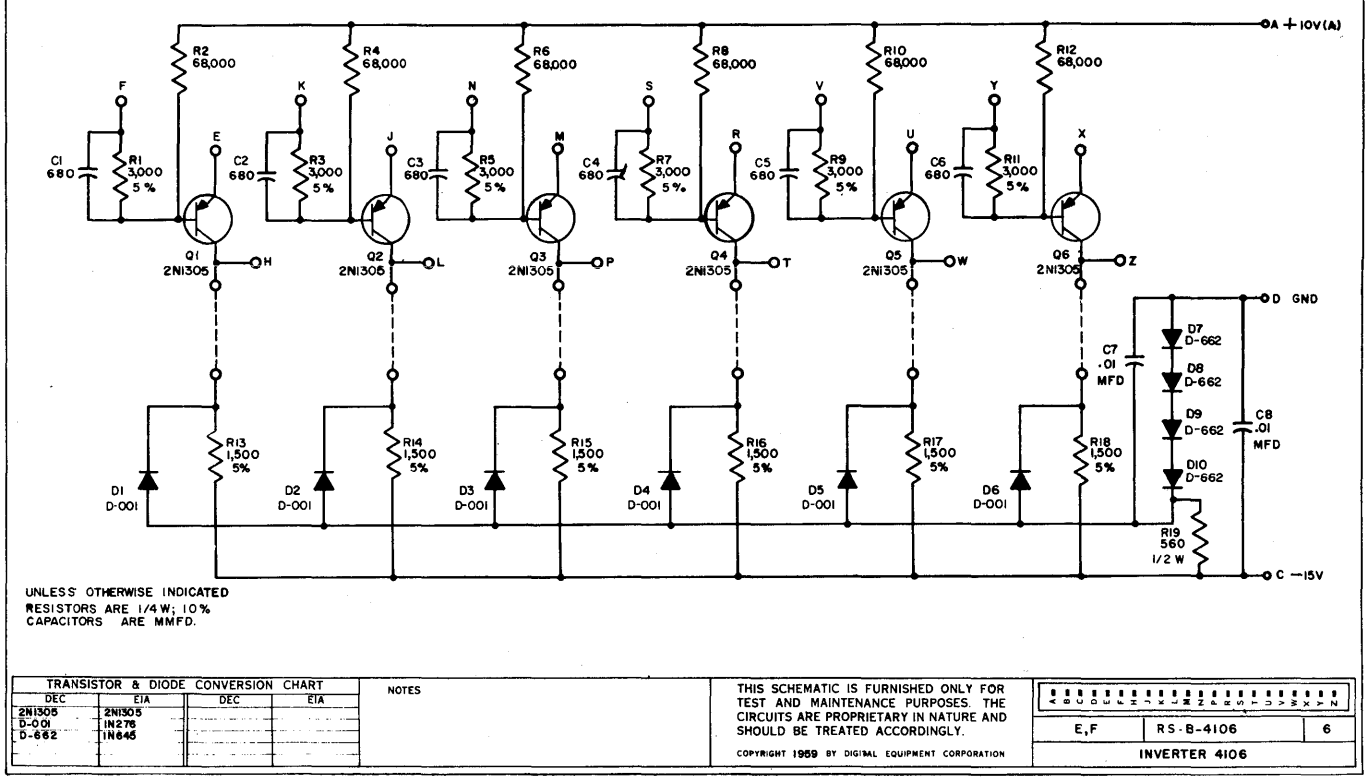
COPYRIGHT 1962 BY DIGITAL EQUIPMENT CORPORATION
A +10V (A)
D GND
C -15V
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
USE THE ETCHED BOARD OF THE 6102
REVISIONS
DRN. SPAULDING DATE 1-4-62
CHK'D N. PERRYMAN DATE 1-4-62
ENG. CUDMORE DATE 1-4-62
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
2N1305 2N1305
D003 1N994
D662 1N645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE INVERTER 4102
SIZE B CODE CS NUMBER 4102-0-1 REV. F
PRINTED CIRCUIT REV. F
DEC FORM NO. DRB 102

RS-B-4106-6



A +10V(A)
D GND
C -15V
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD.
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
2N1305 2N1305
D-001 1N276
D-662 1N645
NOTES
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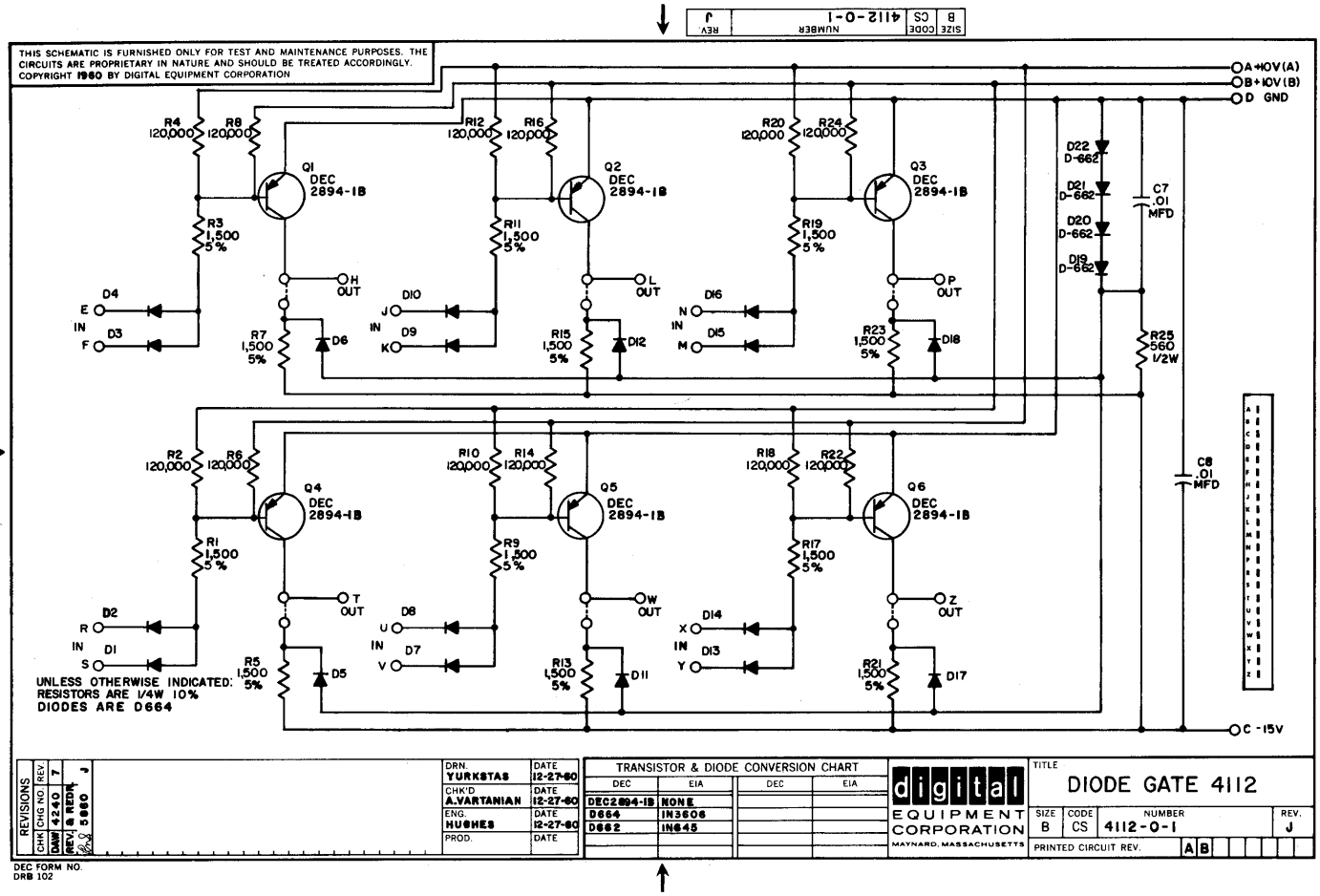
E,F RS-B-4106 6
INVERTER 4106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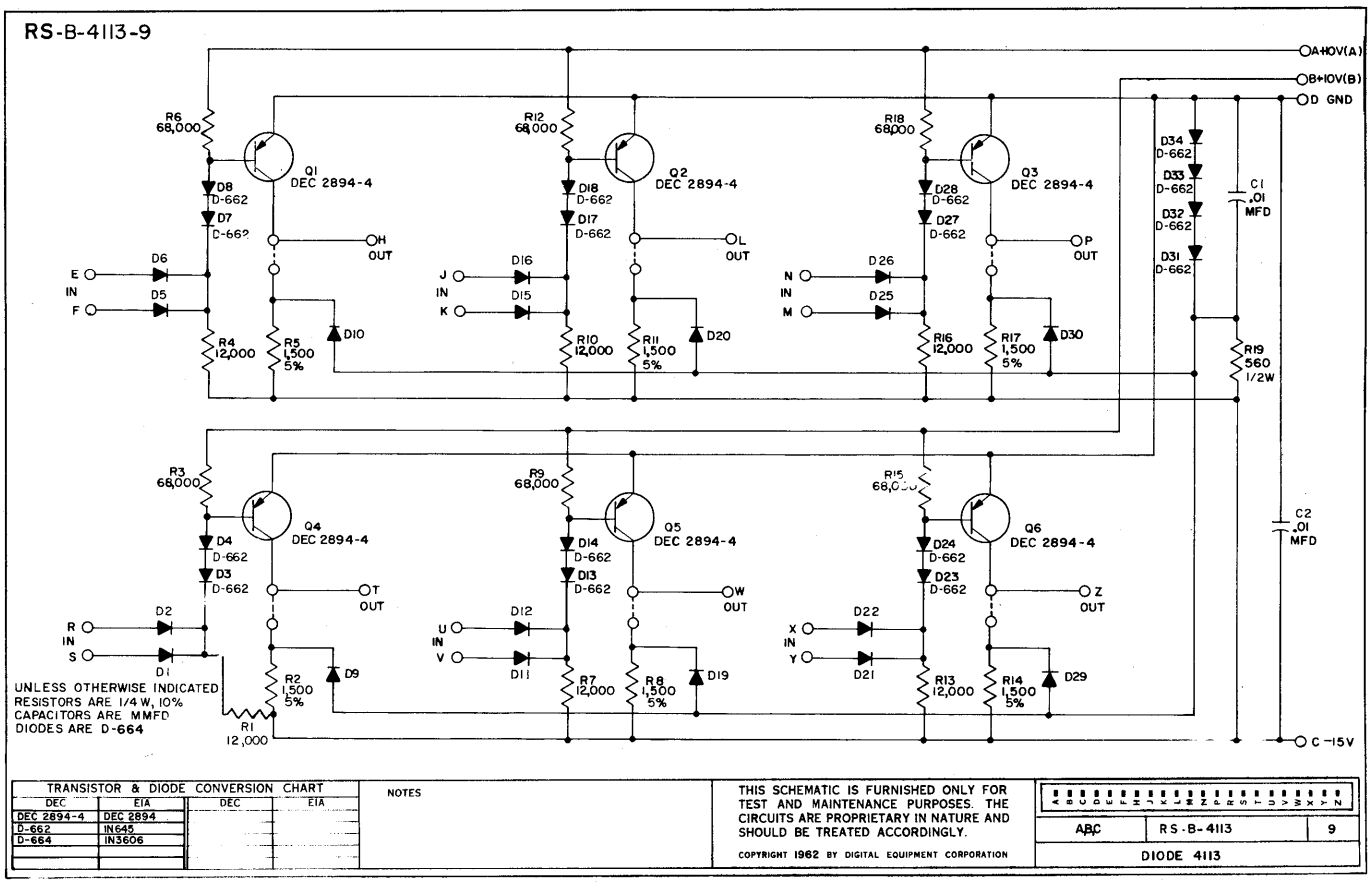
COPYRIGHT 1960 BY DIGITAL EQUIPMENT CORPORATION
A +10V(A)
B +10V(B)
D GND
C -15V
Q1 DEC 2894-1B
Q2 DEC 2894-1B
Q3 DEC 2894-1B
Q4 DEC 2894-1B
Q5 DEC 2894-1B
Q6 DEC 2894-1B
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W 10%
DIODES ARE D664
TRANSISTOR & DIODE CONVERSION CHART
DEC2894-1B NONE
D664 IN3606
D662 IN645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DIODE GATE 4112
SIZE B CODE CS NUMBER 4112-0-1 REV. J
PRINTED CIRCUIT REV. A B
DRN. YURKSTAS 12-27-60
CHK'D A.VARTANIAN 12-27-60
ENG. HUGHES 12-27-60
PROD.
REVISIONS
DEC FORM NO. DRB 102


RS-B-4113-9
A +10V(A)
B +10V(B)
D GND
C -15V
Q1 DEC 2894-4
Q2 DEC 2894-4
Q3 DEC 2894-4
Q4 DEC 2894-4
Q5 DEC 2894-4
Q6 DEC 2894-4
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTOR & DIODE CONVERSION CHART
DEC 2894-4 DEC 2894
D-662 IN645
D-664 IN3606
NOTES
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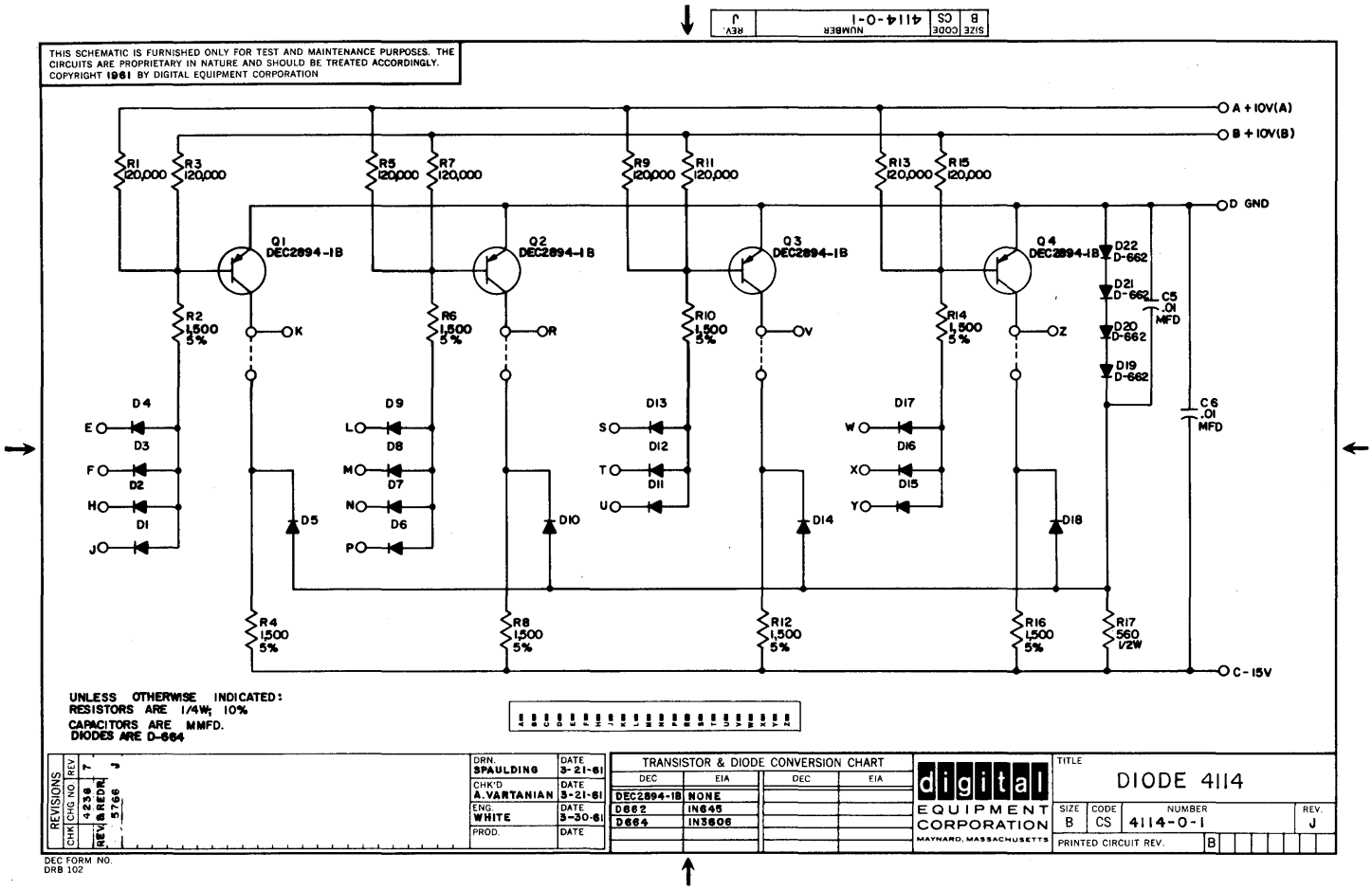
COPYRIGHT 1962 BY DIGITAL EQUIPMENT CORPORATION
A B C
RS-B-4113
9
DIODE 4113



SIZE B CODE CS NUMBER 4114-0-1 REV. J
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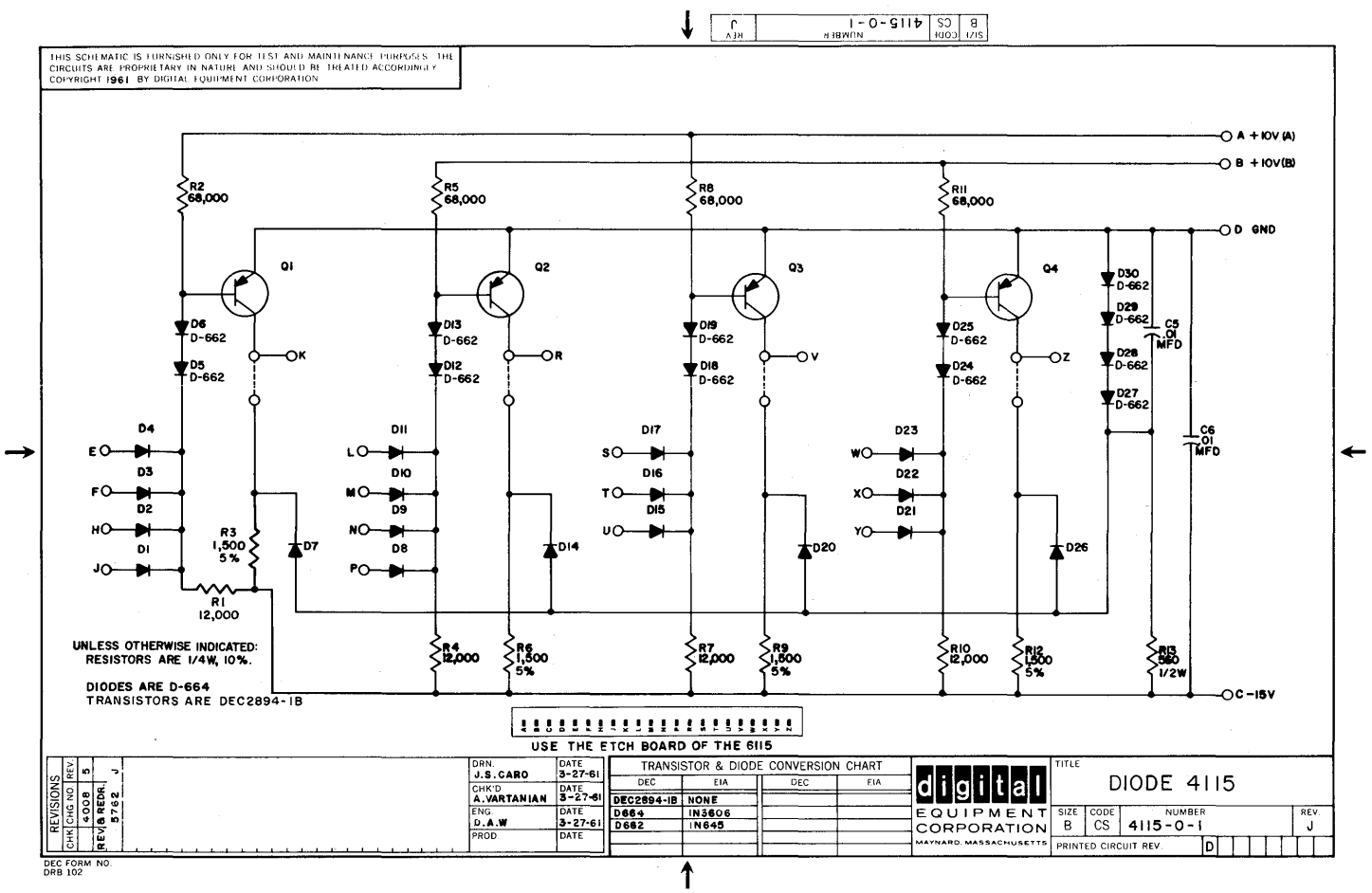
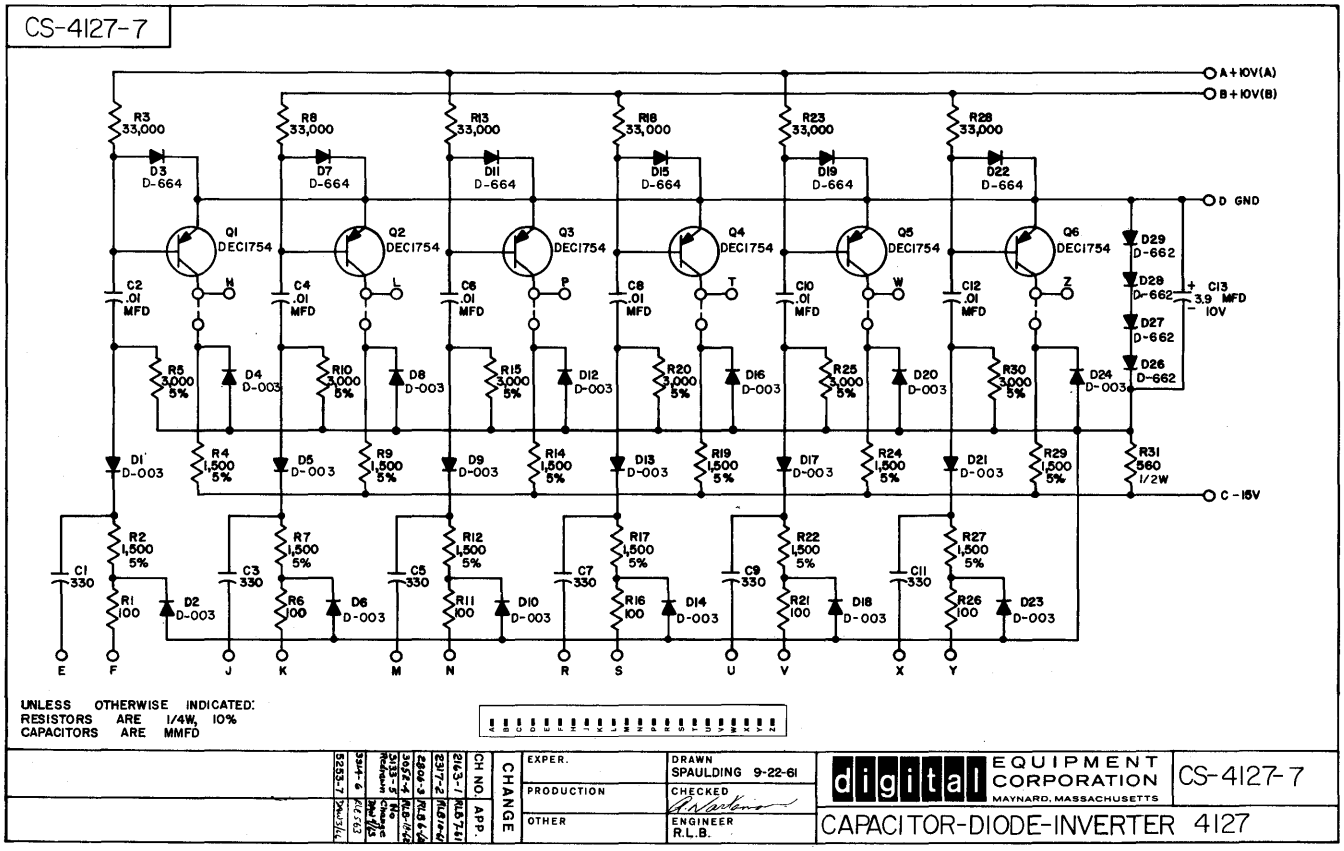
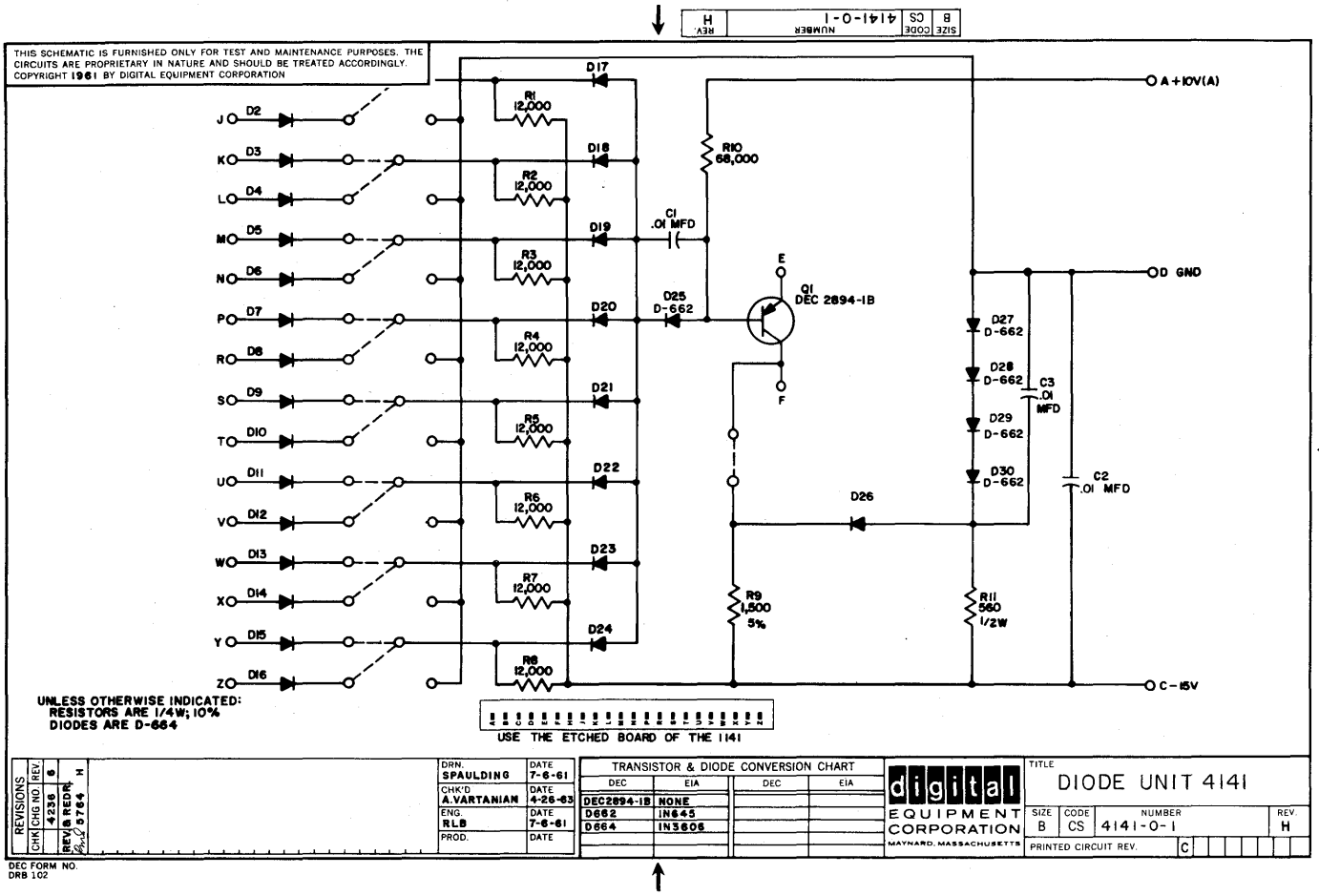
A +10V(A)
B +10V(B)
D GND
C-15V
Q1 DEC2894-1B
Q2 DEC2894-1B
Q3 DEC2894-1B
Q4 DEC2894-1B
R1 120,000
R3 120,000
R5 120,000
R7 120,000
R9 120,000
R11 120,000
R13 120,000
R15 120,000
R2 1,500 5%
R6 1,500 5%
R10 1,500 5%
R14 1,500 5%
R4 1,500 5%
R8 1,500 5%
R12 1,500 5%
R16 1,500 5%
R17 560 1/2W
D22 D-662
D21 D-662
D20 D-662
D19 D-662
C5 .01 MFD
C6 .01 MFD
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD.
DIODES ARE D-664
REVISIONS
CHK CHG NO REV
4236 7
REV & REDR. 5766 J
DRN. SPAULDING DATE 3-21-61
CHK'D A.VARTANIAN DATE 3-21-61
ENG. WHITE DATE 3-30-61
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC2894-1B NONE
D662 IN645
D664 IN3606
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DIODE 4114
SIZE B CODE CS NUMBER 4114-0-1 REV. J
PRINTED CIRCUIT REV. B
DEC FORM NO. DRB 102

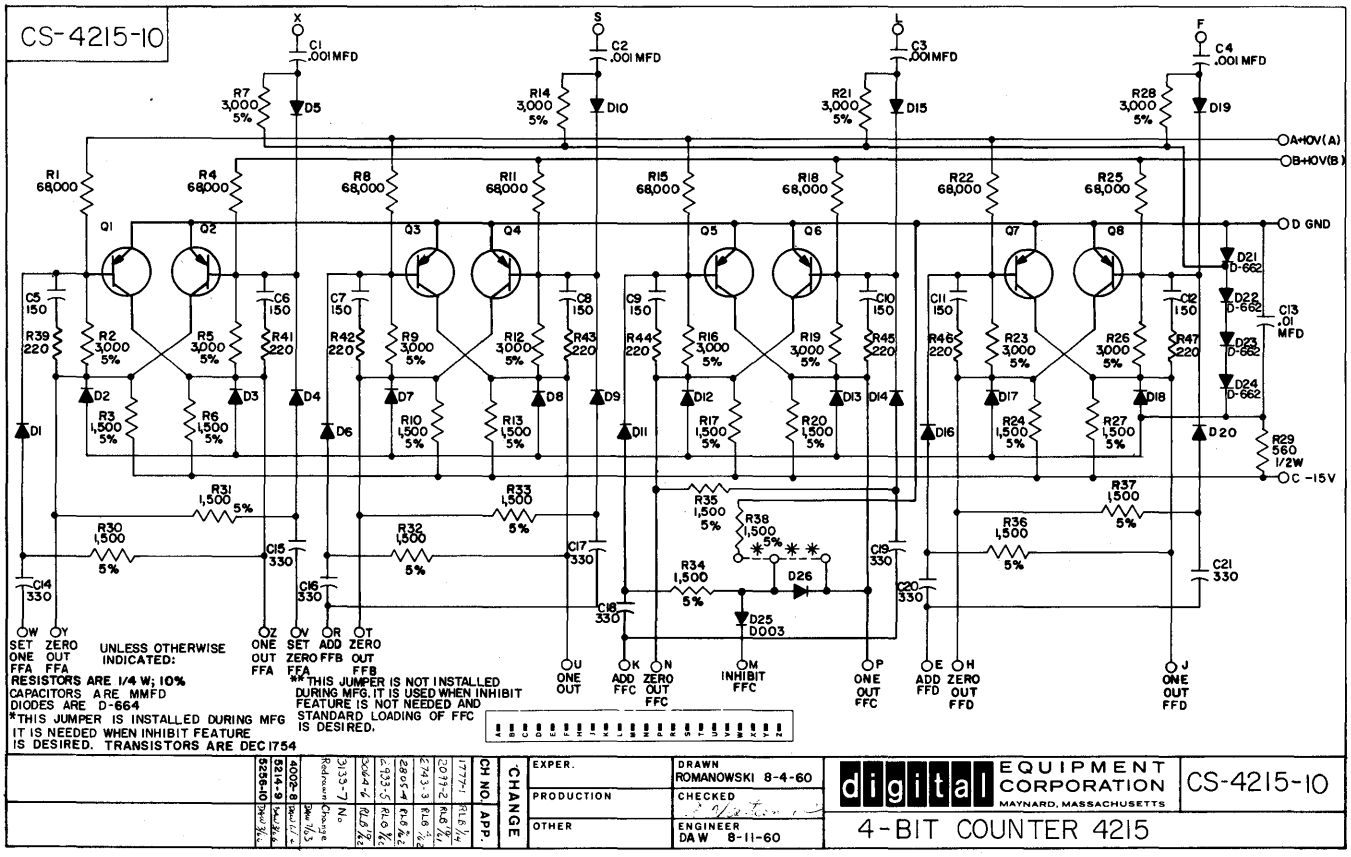


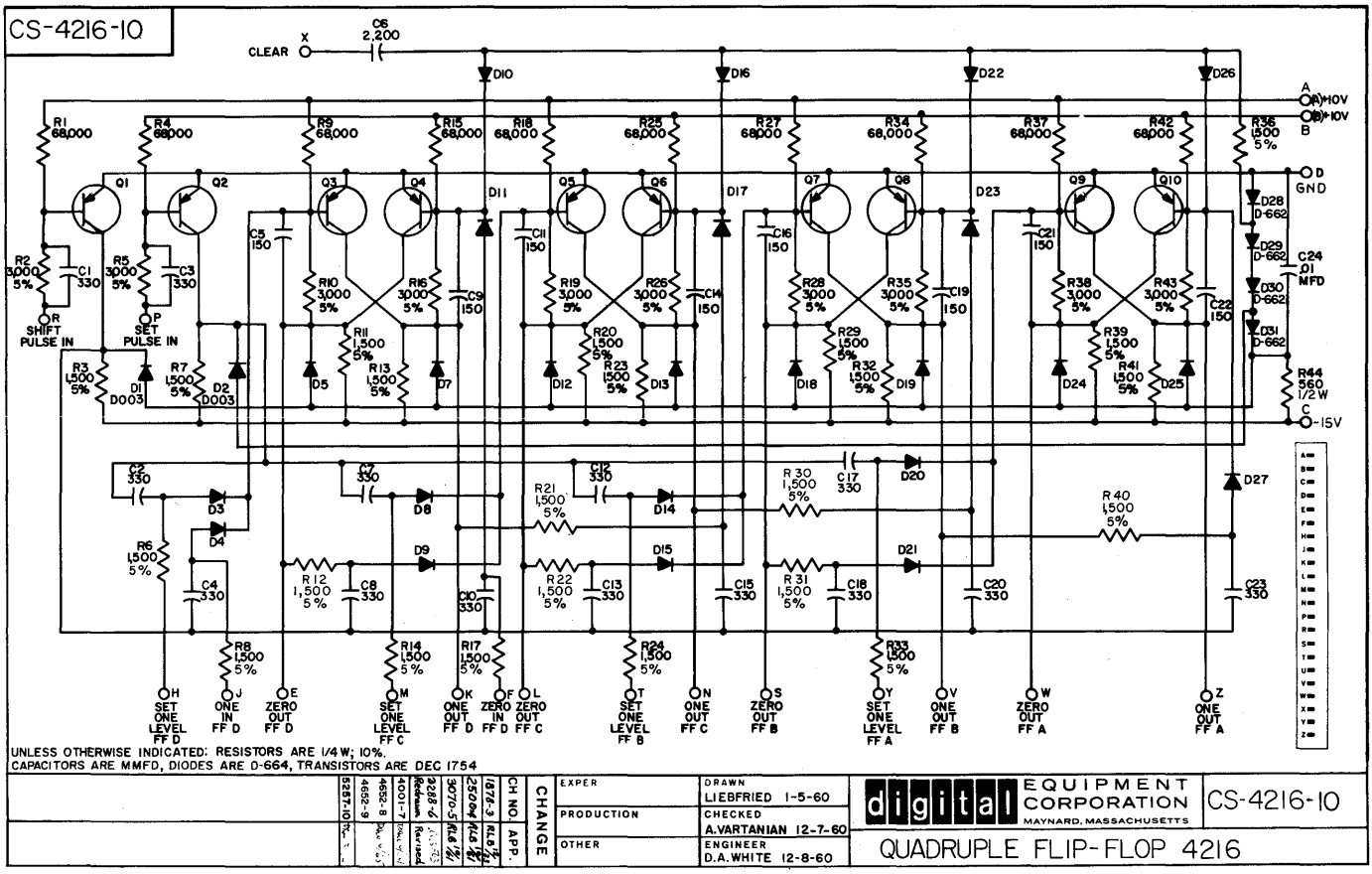
SIZE B CODE CS NUMBER 4115-0-1 REV. J
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1961 BY DIGITAL EQUIPMENT CORPORATION
A +10V(A)
B +10V(B)
D GND
C-15V
Q1
Q2
Q3
Q4
R2 68,000
R5 68,000
R8 68,000
R11 68,000
R3 1,500 5%
R1 12,000
R4 12,000
R6 1,500 5%
R7 12,000
R9 1,500 5%
R10 12,000
R12 1,500 5%
R13 560 1/2W
D30 D-662
D29 D-662
D28 D-662
D27 D-662
C5 .01 MFD
C6 .01 MFD
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%.
DIODES ARE D-664
TRANSISTORS ARE DEC2894-1B
USE THE ETCH BOARD OF THE 6115
REVISIONS
CHK CHG NO REV
4008 5
REV & REDR. 5762 J
DRN. J.S.CARO DATE 3-27-61
CHK'D A.VARTANIAN DATE 3-27-61
ENG. D.A.W DATE 3-27-61
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC2894-1B NONE
D664 IN3606
D662 IN645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DIODE 4115
SIZE B CODE CS NUMBER 4115-0-1 REV. J
PRINTED CIRCUIT REV. D
DEC FORM NO. DRB 102

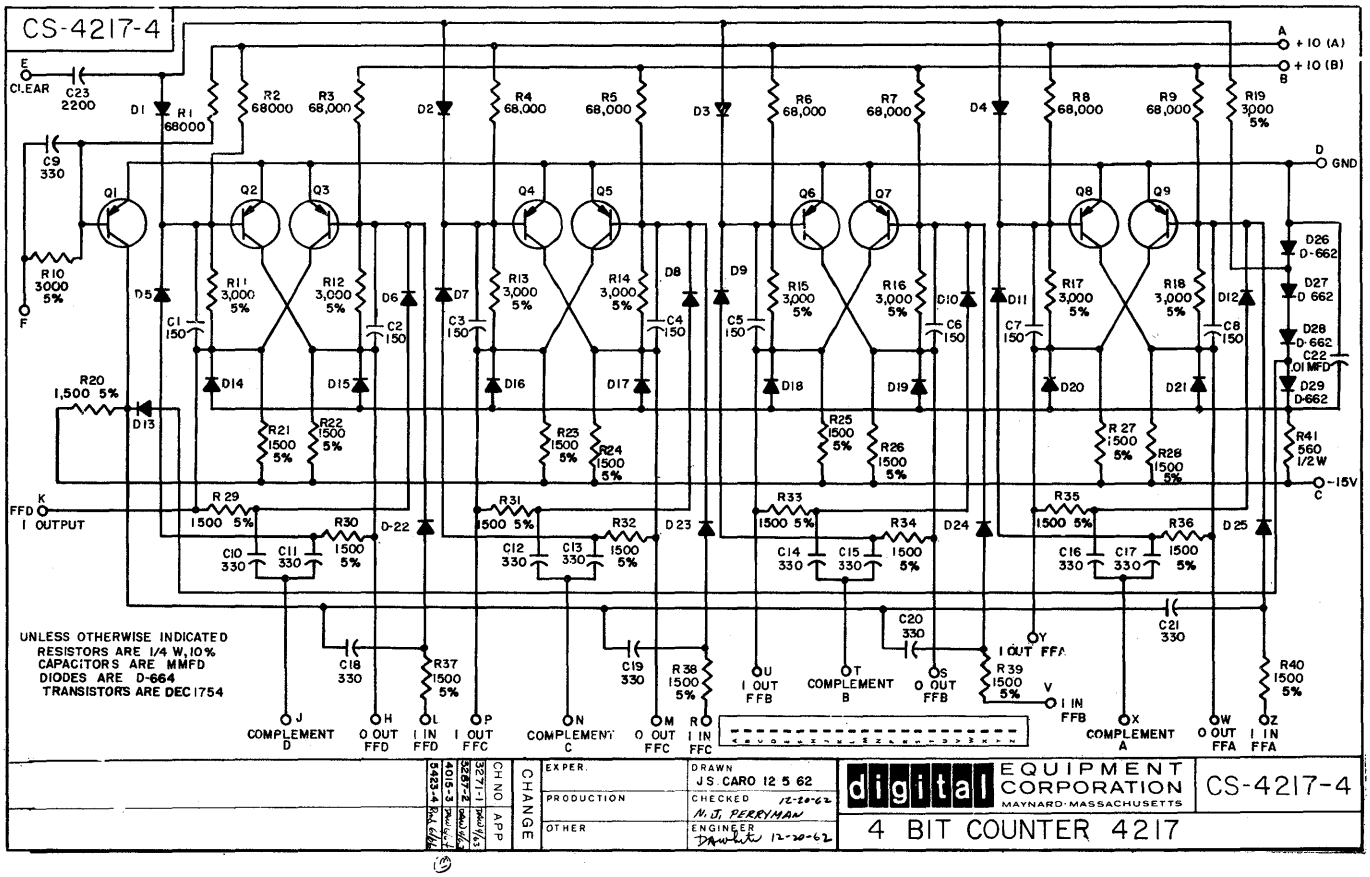


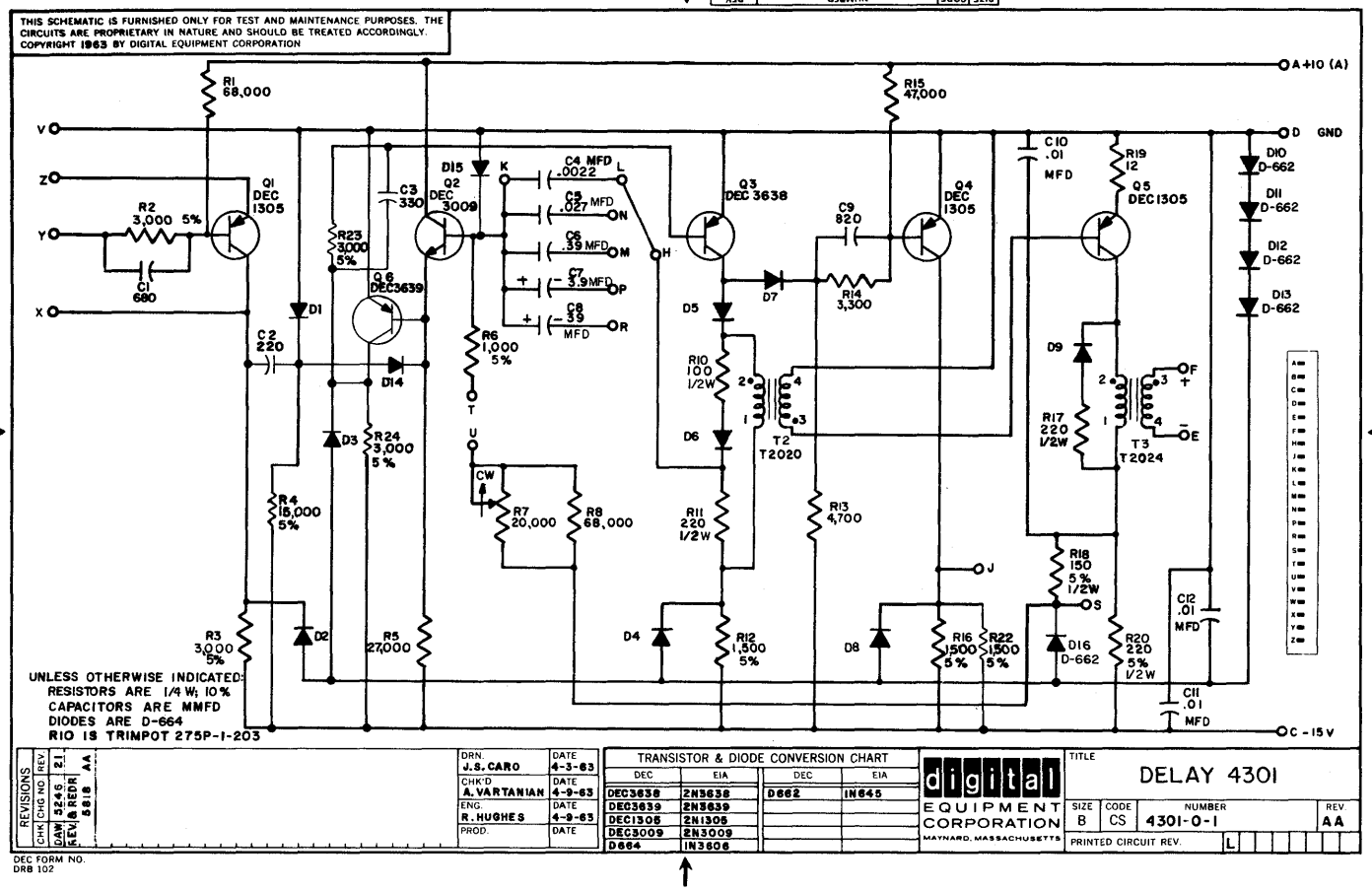


DEC FORM NO.
DRB 102


CS-4215-10
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
*THIS JUMPER IS INSTALLED DURING MFG IT IS NEEDED WHEN INHIBIT FEATURE IS DESIRED. TRANSISTORS ARE DEC 1754
**THIS JUMPER IS NOT INSTALLED DURING MFG. IT IS USED WHEN INHIBIT FEATURE IS NOT NEEDED AND STANDARD LOADING OF FFC IS DESIRED.
4-BIT COUNTER 4215
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CS-4215-10
DRAWN ROMANOWSKI 8-4-60
CHECKED
ENGINEER DAW 8-11-60


CS-4216-10
UNLESS OTHERWISE INDICATED: RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD, DIODES ARE D-664, TRANSISTORS ARE DEC 1754
QUADRUPLE FLIP-FLOP 4216
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CS-4216-10
DRAWN LIEBFRIED 1-5-60
CHECKED A.VARTANIAN 12-7-60
ENGINEER D.A.WHITE 12-8-60


CS-4217-4
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 1754
digital EQUIPMENT CORPORATION
MAYNARD·MASSACHUSETTS
CS-4217-4
4 BIT COUNTER 4217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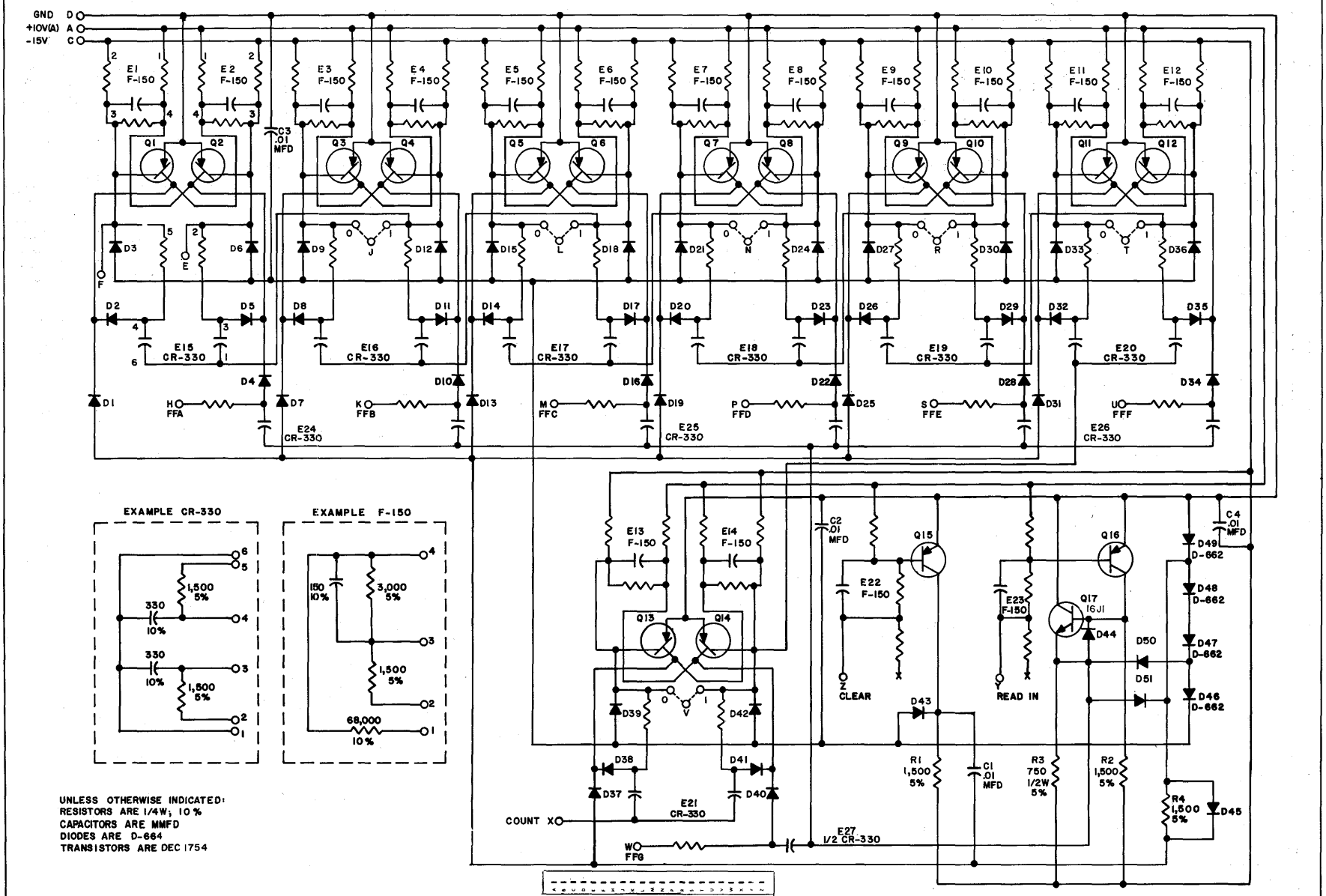
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
R10 IS TRIMPOT 275P-1-203
TRANSISTOR & DIODE CONVERSION CHART
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
DELAY 4301
SIZE B | CODE CS | NUMBER 4301-0-1 | REV AA

CS-C-4222-9



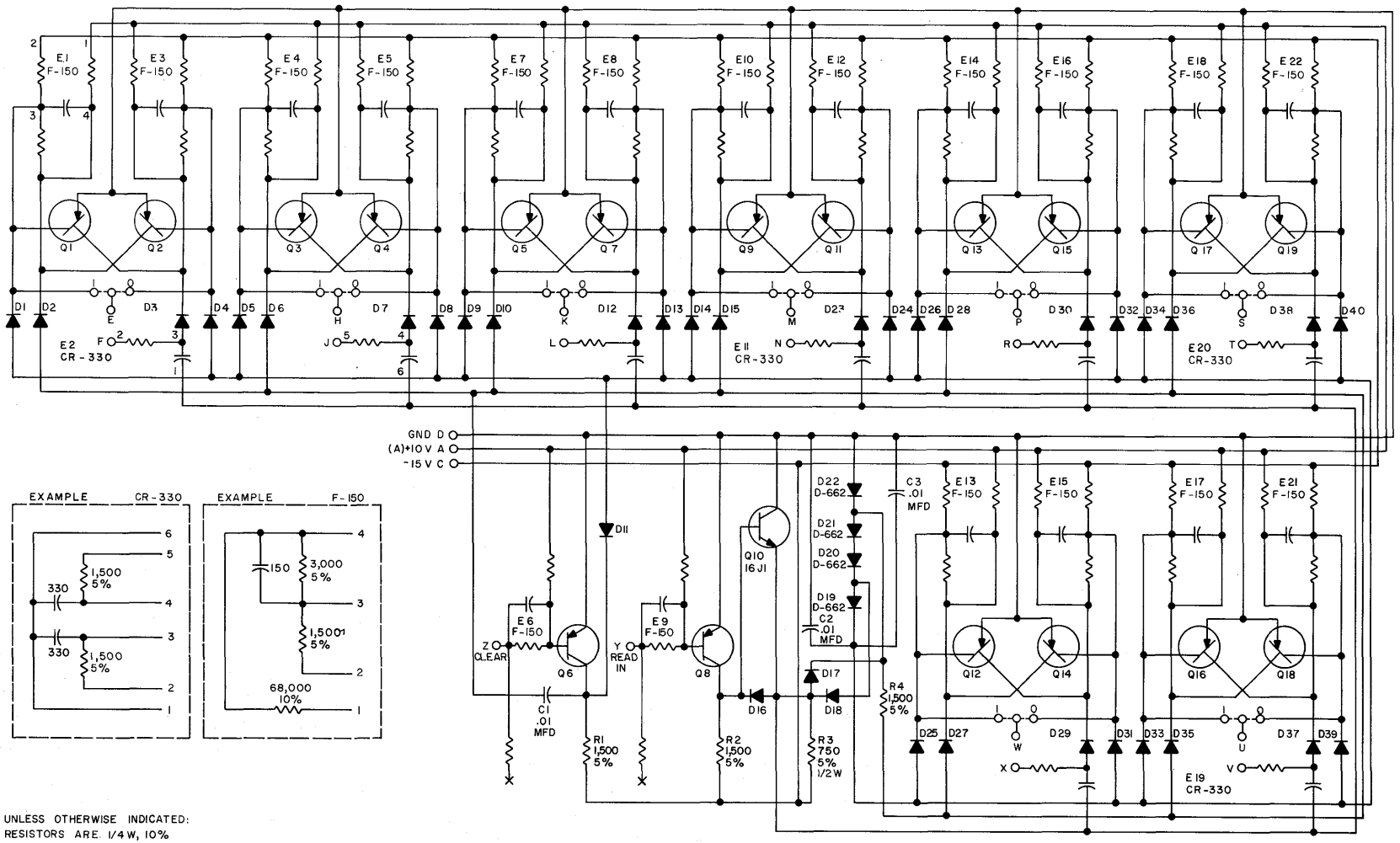
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 1754

CHANGE			
CH NO	APP	EXPER	DRAWN H.W.PORTER 5-28-63
3425-1	D.A.W. 8-63	PRODUCTION	CHECKED A.VARTANIAN 5-28-63
3610-2	D.A.W. 9-63	OTHER	ENGINEER A.FALCO 5-28-63
3625-3	D.A.W. 10-63		
3598-4	D.A.W. 10-63		
3333-5 REDR. NO CHG.	DAW 10-63		
3887-6	DAW 3/64		
4028-7	DAW 3/64		
4502-8	DAW 3/65		
4502-9			

digital EQUIPMENT CORPORATION MAYNARD·MASSACHUSETTS

CS-C-4222-9

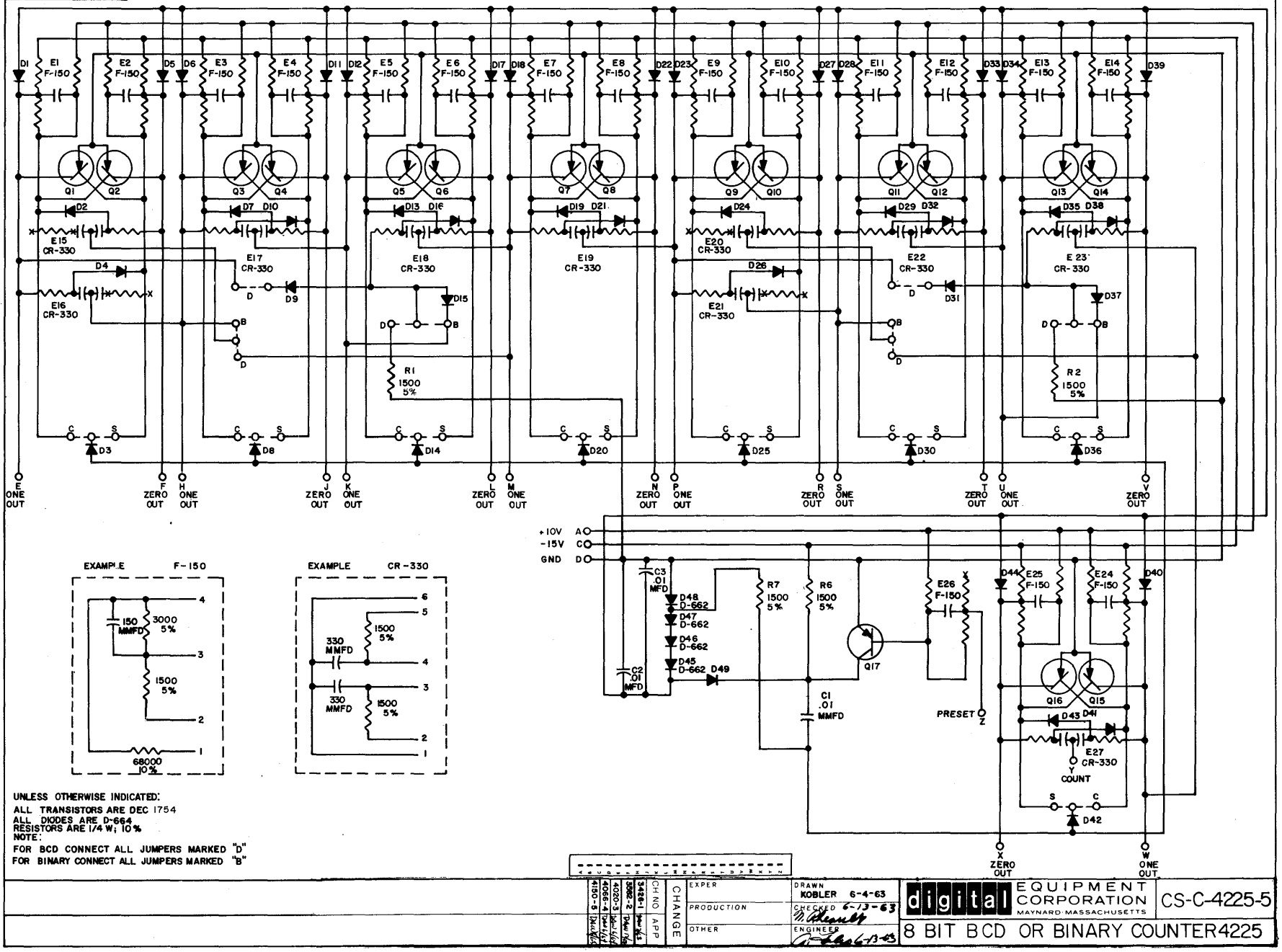
7 BIT COUNTER WITH READ IN GATES 4222



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 1754
DIODES ARE D-664

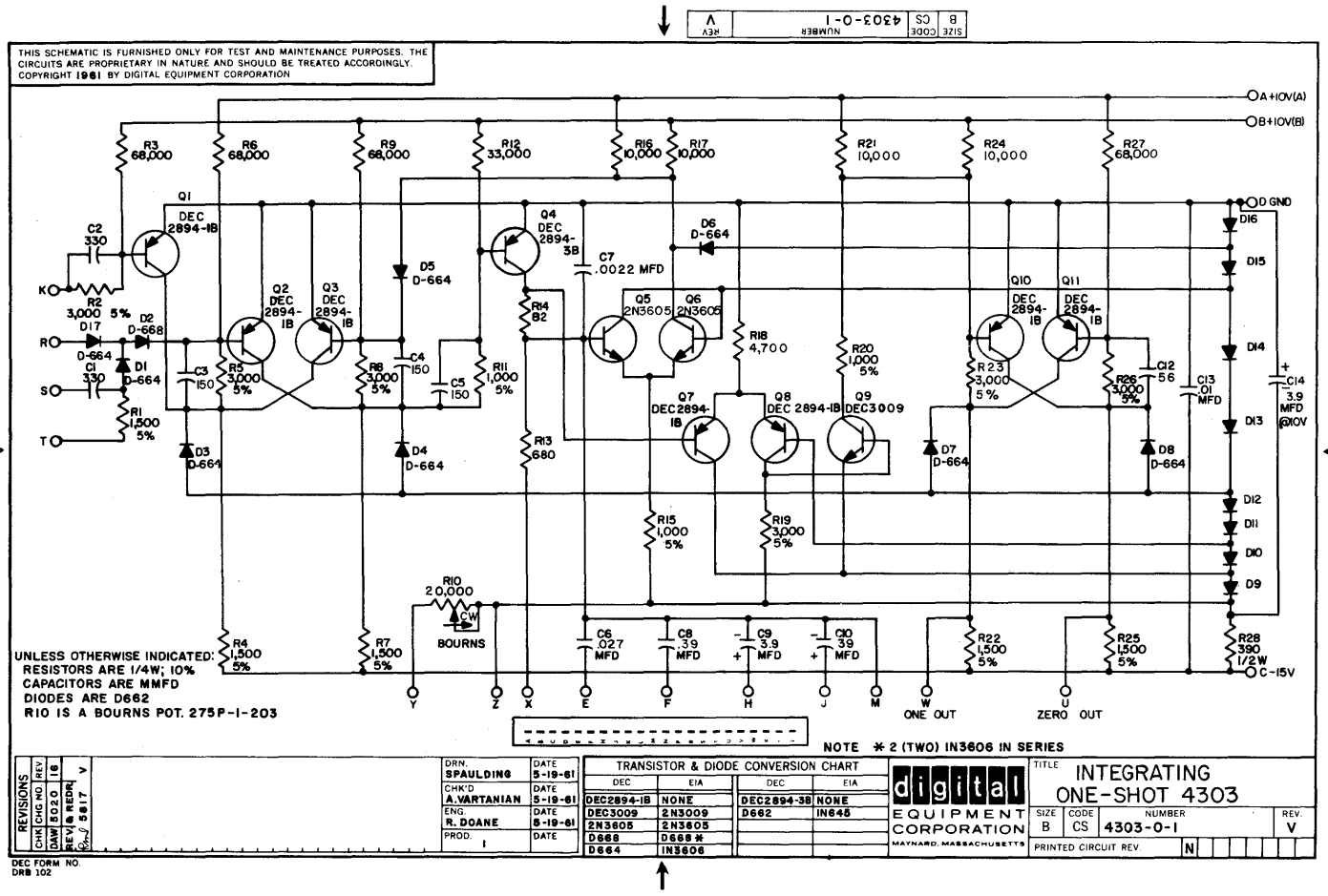
REVISIONS	ECO. NO.	ENG.
4783-7		
4503-6 REDR. AND REV.	4021-5	6-64
	3678-4	3-64
	3859-3	3-64
	3843-2	2-64
	3580-1	10-63

DRAFTSMAN I. HAHN DATE 3-8-65	CHECKER DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	CODE CS DWG. NO. C-4220 REV. 7
ENGINEER DATE	PRODUCTION DATE	TITLE 8 BIT BUFFER REGISTER 4220	



UNLESS OTHERWISE INDICATED:
ALL TRANSISTORS ARE DEC 1754
ALL DIODES ARE D-664
RESISTORS ARE 1/4 W; 10%
NOTE:
FOR BCD CONNECT ALL JUMPERS MARKED "D"
FOR BINARY CONNECT ALL JUMPERS MARKED "B"

CH NO	APP	CHANGE		
4150-5		EXPER	DRAWN KOBLER 6-4-63	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
4066-4		PRODUCTION	CHECKED 6-13-63	CS-C-4225-5
4020-3		OTHER	ENGINEER 6-13-63	8 BIT BCD OR BINARY COUNTER 4225
3582-2				
3448-1				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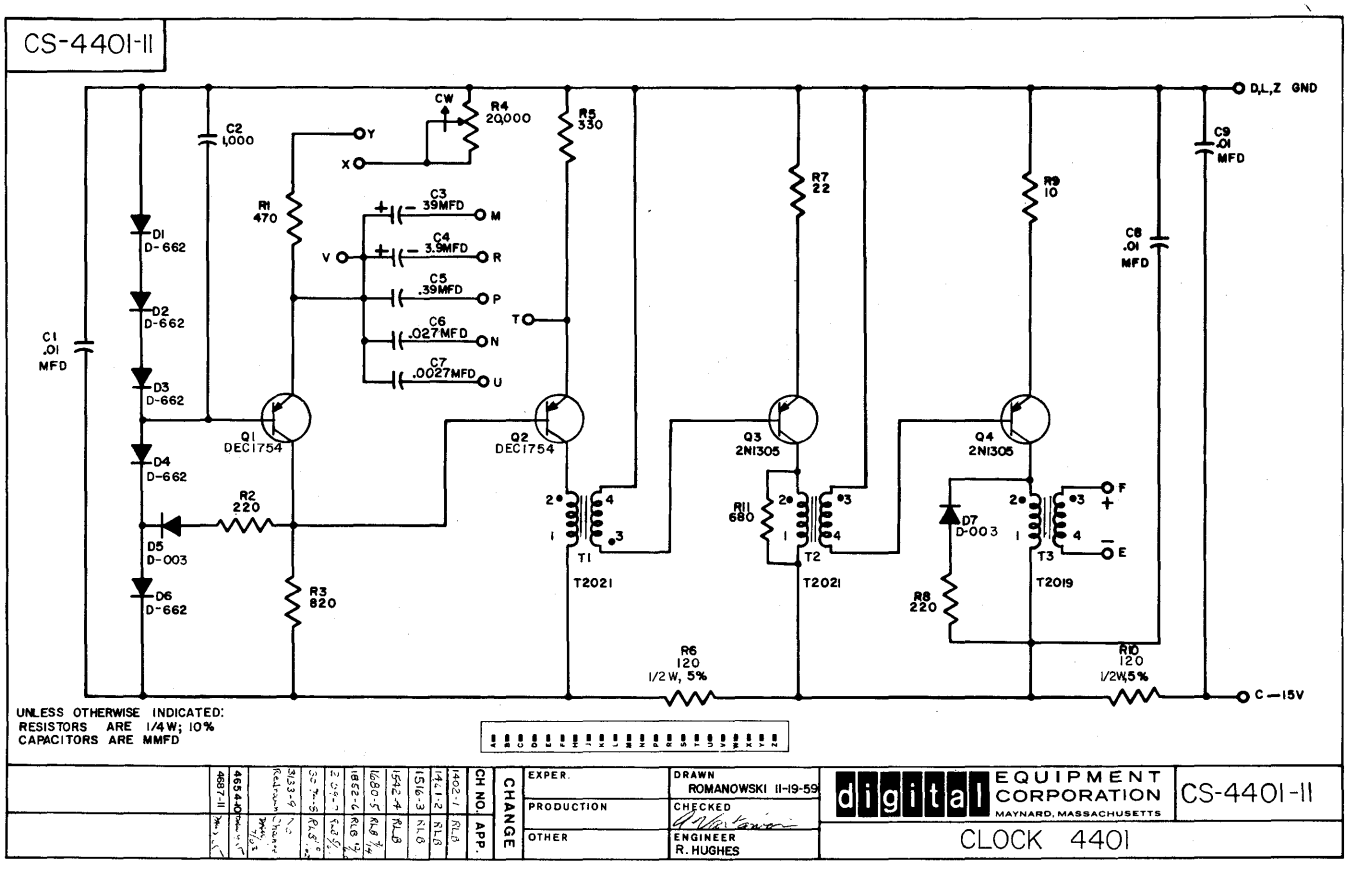
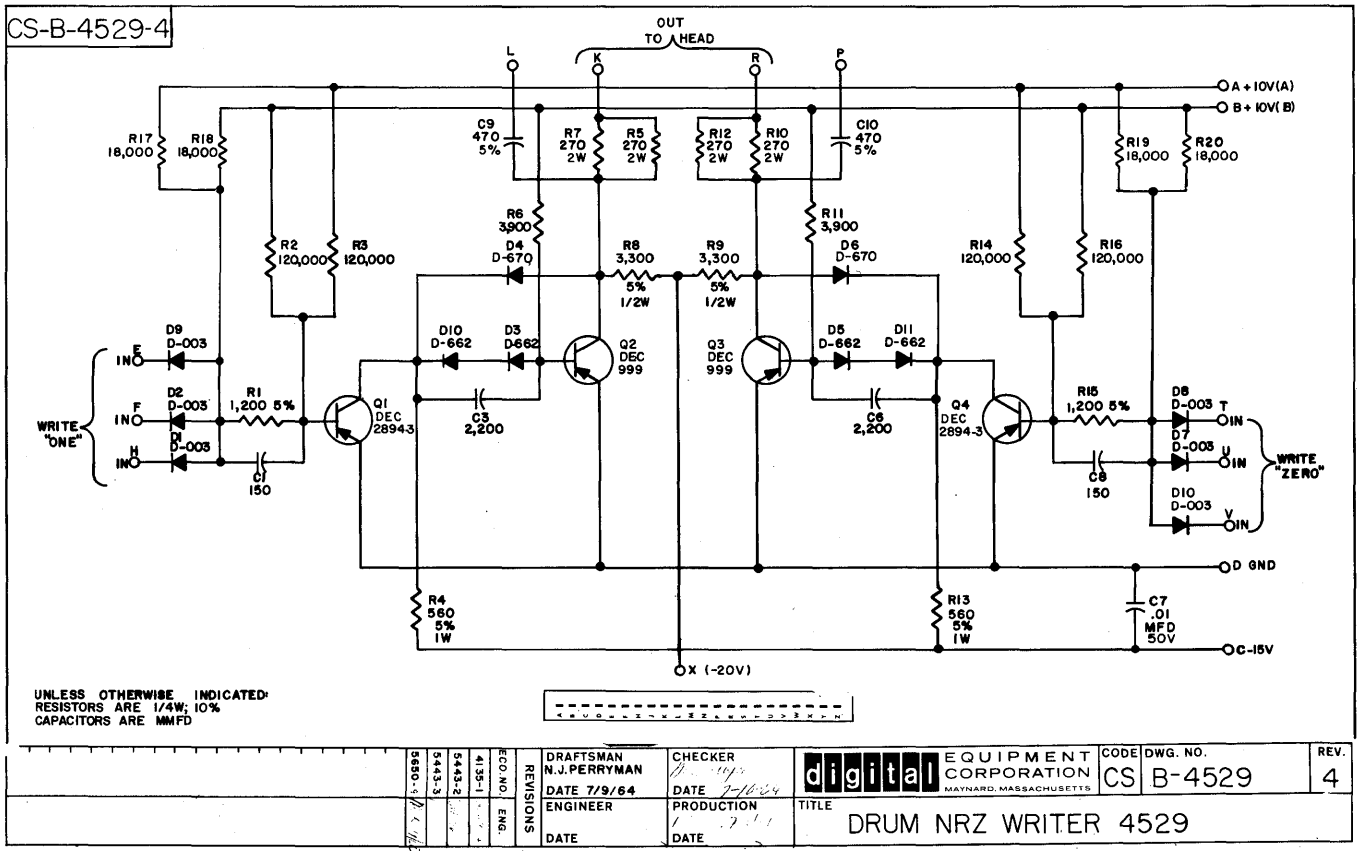
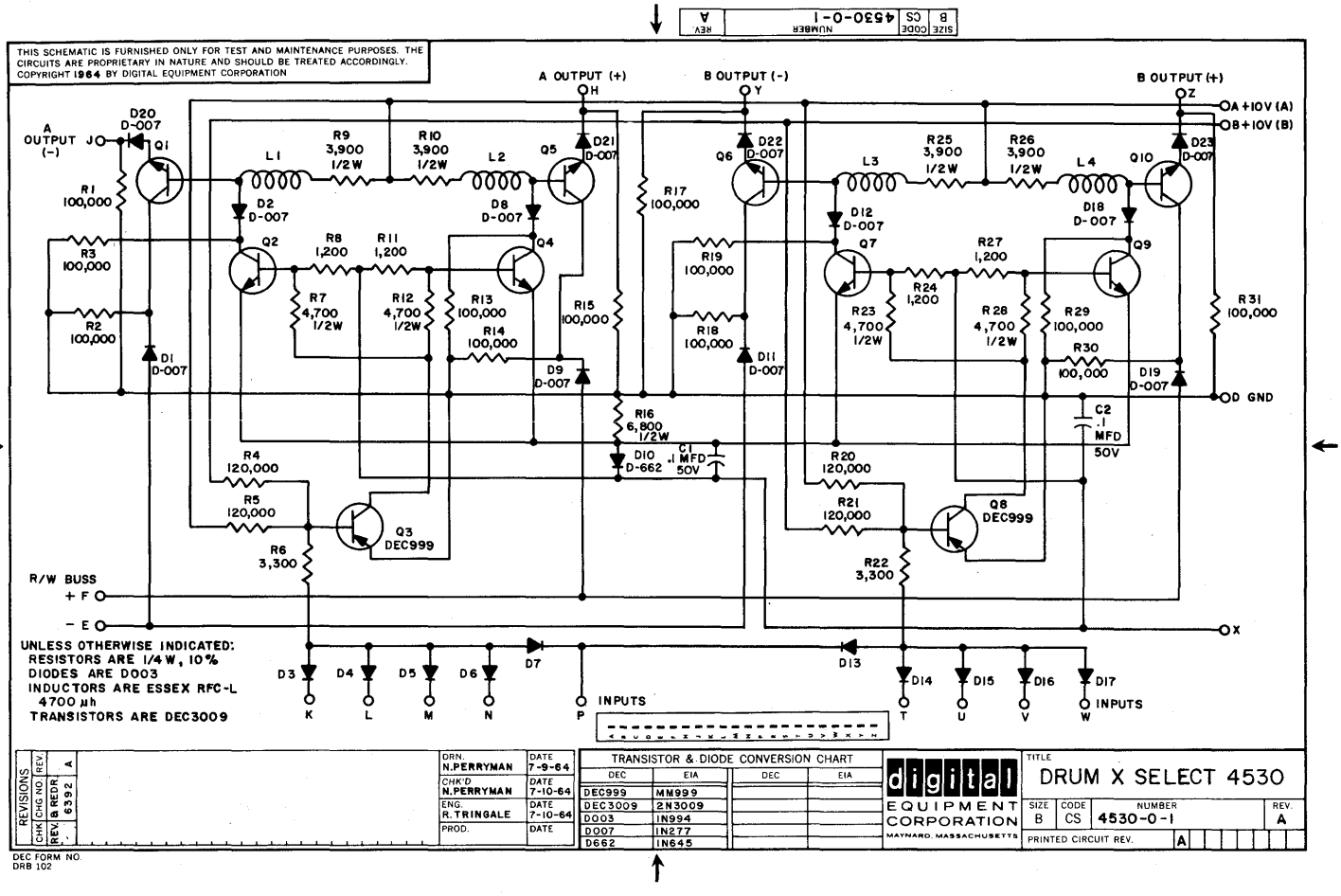
SIZE B CODE CS NUMBER 4303-0-1 REV V
A +10V(A)
B +10V(B)
D GND
C -15V
Q1 DEC 2894-1B
Q2 DEC 2894-1B
Q3 DEC 2894-1B
Q4 DEC 2894-3B
Q5 2N3605
Q6 2N3605
Q7 DEC2894-1B
Q8 DEC 2894-1B
Q9 DEC3009
Q10 DEC 2894-1B
Q11 DEC 2894-1B
R1 1,500 5%
R2 3,000 5%
R3 68,000
R4 1,500 5%
R5 3,000 5%
R6 68,000
R7 1,500 5%
R8 3,000 5%
R9 68,000
R10 20,000 CW BOURNS
R11 1,000 5%
R12 33,000
R13 680
R14 82
R15 1,000 5%
R16 10,000
R17 10,000
R18 4,700
R19 3,000 5%
R20 1,000 5%
R21 10,000
R22 1,500 5%
R23 3,000 5%
R24 10,000
R25 1,500 5%
R26 3,000 5%
R27 68,000
R28 390 1/2W
C1 330
C2 330
C3 150
C4 150
C5 150
C6 .027 MFD
C7 .0022 MFD
C8 .39 MFD
C9 3.9 MFD
C10 39 MFD
C12 56
C13 .01 MFD
C14 3.9 MFD @10V
D1 D-664
D2 D-668
D3 D-664
D4 D-664
D5 D-664
D6 D-664
D7 D-664
D8 D-664
D16
D15
D14
D13
D12
D11
D10
D9
K
R
S
T
Y
Z
X
E
F
H
J
M
W ONE OUT
U ZERO OUT
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D662
R10 IS A BOURNS POT. 275P-1-203
NOTE * 2 (TWO) IN3606 IN SERIES
REVISIONS
CHK DAW
CHG NO 5020
REV 18
REV & REDR 5817
V
DRN. SPAULDING DATE 5-19-61
CHK'D A.VARTANIAN DATE 5-19-61
ENG. R. DOANE DATE 5-19-61
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC2894-1B NONE DEC2894-3B NONE
DEC3009 2N3009 D662 IN645
2N3605 2N3605
D668 D668 *
D664 IN3606
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE INTEGRATING ONE-SHOT 4303
SIZE B CODE CS NUMBER 4303-0-1 REV. V
PRINTED CIRCUIT REV. N
DEC FORM NO. DRB 102


CS-4401-11
D,L,Z GND
C -15V
C1 .01 MFD
C2 1,000
C3 39MFD
C4 3.9MFD
C5 .39MFD
C6 .027MFD
C7 .0027MFD
C8 .01 MFD
C9 .01 MFD
CW R4 20,000
R1 470
R2 220
R3 820
R5 330
R6 120 1/2 W, 5%
R7 22
R8 220
R9 10
R10 120 1/2W,5%
R11 680
D1 D-662
D2 D-662
D3 D-662
D4 D-662
D5 D-003
D6 D-662
D7 D-003
Q1 DEC1754
Q2 DEC1754
Q3 2N1305
Q4 2N1305
T1 T2021
T2 T2021
T3 T2019
X
Y
V
T
M
R
P
N
U
F
E
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
CHANGE
EXPER.
PRODUCTION
OTHER
DRAWN ROMANOWSKI 11-19-59
CHECKED
ENGINEER R. HUGHES
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CS-4401-11
CLOCK 4401


CS-B-4529-4
OUT TO HEAD
L
K
R
P
A +10V(A)
B +10V(B)
R17 18,000
R18 18,000
C9 470 5%
R7 270 2W
R5 270 2W
R12 270 2W
R10 270 2W
C10 470 5%
R19 18,000
R20 18,000
R6 3,900
R11 3,900
R2 120,000
R3 120,000
D4 D-670
R8 3,300 5% 1/2W
R9 3,300 5% 1/2W
D6 D-670
R14 120,000
R16 120,000
D9 D-003
D10 D-662
D3 D-662
Q2 DEC 999
Q3 DEC 999
D5 D-662
D11 D-662
WRITE "ONE"
E IN
F IN
H IN
D2 D-003
D1 D-003
R1 1,200 5%
C1 150
Q1 DEC 2894-3
C3 2,200
C6 2,200
Q4 DEC 2894-3
R15 1,200 5%
C8 150
D8 D-003 T IN
D7 D-003 U IN
D10 D-003 V IN
WRITE "ZERO"
D GND
R4 560 5% 1W
R13 560 5% 1W
C7 .01 MFD 50V
C-15V
X (-20V)
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DRAFTSMAN N.J.PERRYMAN
DATE 7/9/64
CHECKER
DATE
ENGINEER
DATE
PRODUCTION
DATE
REVISIONS
ECO NO.
5650-1
5443-3
5443-2
4135-1
ENG.
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CODE CS
DWG. NO. B-4529
REV. 4
TITLE
DRUM NRZ WRITER 4529


SIZE B CS
NUMBER 4530-0-1
REV A
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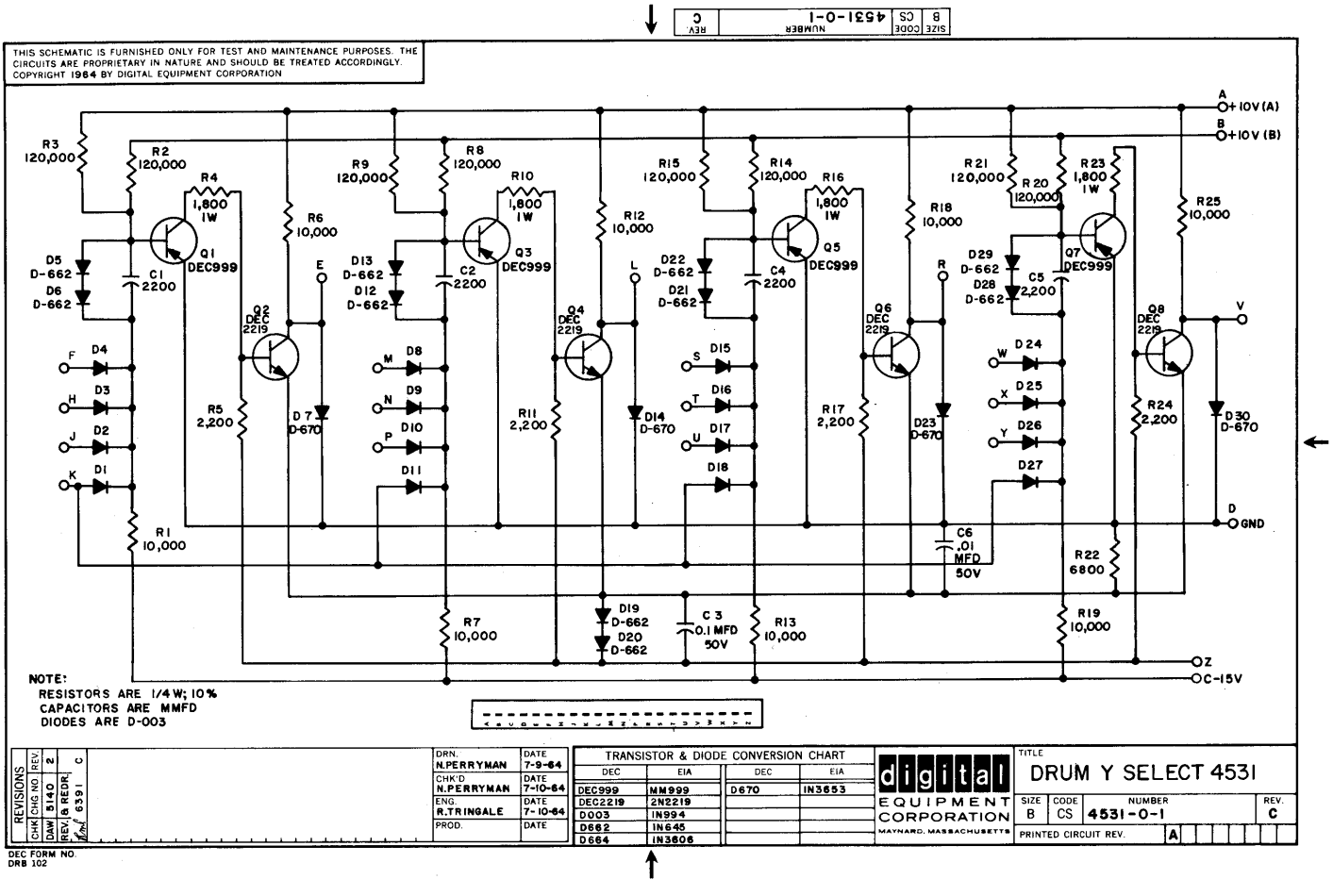
A OUTPUT (+) H
B OUTPUT (-) Y
B OUTPUT (+) Z
A +10V (A)
B +10V (B)
A OUTPUT (-) J
D20 D-007
Q1
L1
R9 3,900 1/2W
R10 3,900 1/2W
L2
Q5
D21 D-007
Q6
D22 D-007
L3
R25 3,900 1/2W
R26 3,900 1/2W
L4
Q10
D23 D-007
R1 100,000
D2 D-007
D8 D-007
R17 100,000
D12 D-007
D18 D-007
Q2
R8 1,200
R11 1,200
Q4
Q7
R27 1,200
Q9
R3 100,000
R19 100,000
R7 4,700 1/2W
R12 4,700 1/2W
R13 100,000
R15 100,000
R24 1,200
R23 4,700 1/2W
R28 4,700 1/2W
R29 100,000
R31 100,000
R2 100,000
R14 100,000
R18 100,000
D1 D-007
D9 D-007
D11 D-007
R30 100,000
D19 D-007
D GND
R16 6,800 1/2W
C1 .1 MFD 50V
C2 .1 MFD 50V
D10 D-662
R4 120,000
R20 120,000
R5 120,000
R21 120,000
Q3 DEC999
Q8 DEC999
R6 3,300
R22 3,300
R/W BUSS
+ F
- E
X
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
DIODES ARE D003
INDUCTORS ARE ESSEX RFC-L 4700 µh
TRANSISTORS ARE DEC3009
D3 D4 D5 D6 D7 D13 D14 D15 D16 D17
K L M N P INPUTS T U V W INPUTS
REVISIONS REV. A CHG NO. 6392 REDR. CHK REV.
DRN. N.PERRYMAN DATE 7-9-64
CHK'D N.PERRYMAN DATE 7-10-64
ENG. R.TRINGALE DATE 7-10-64
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC999 MM999
DEC3009 2N3009
D003 IN994
D007 IN277
D662 IN645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DRUM X SELECT 4530
SIZE B CODE CS NUMBER 4530-0-1 REV. A
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102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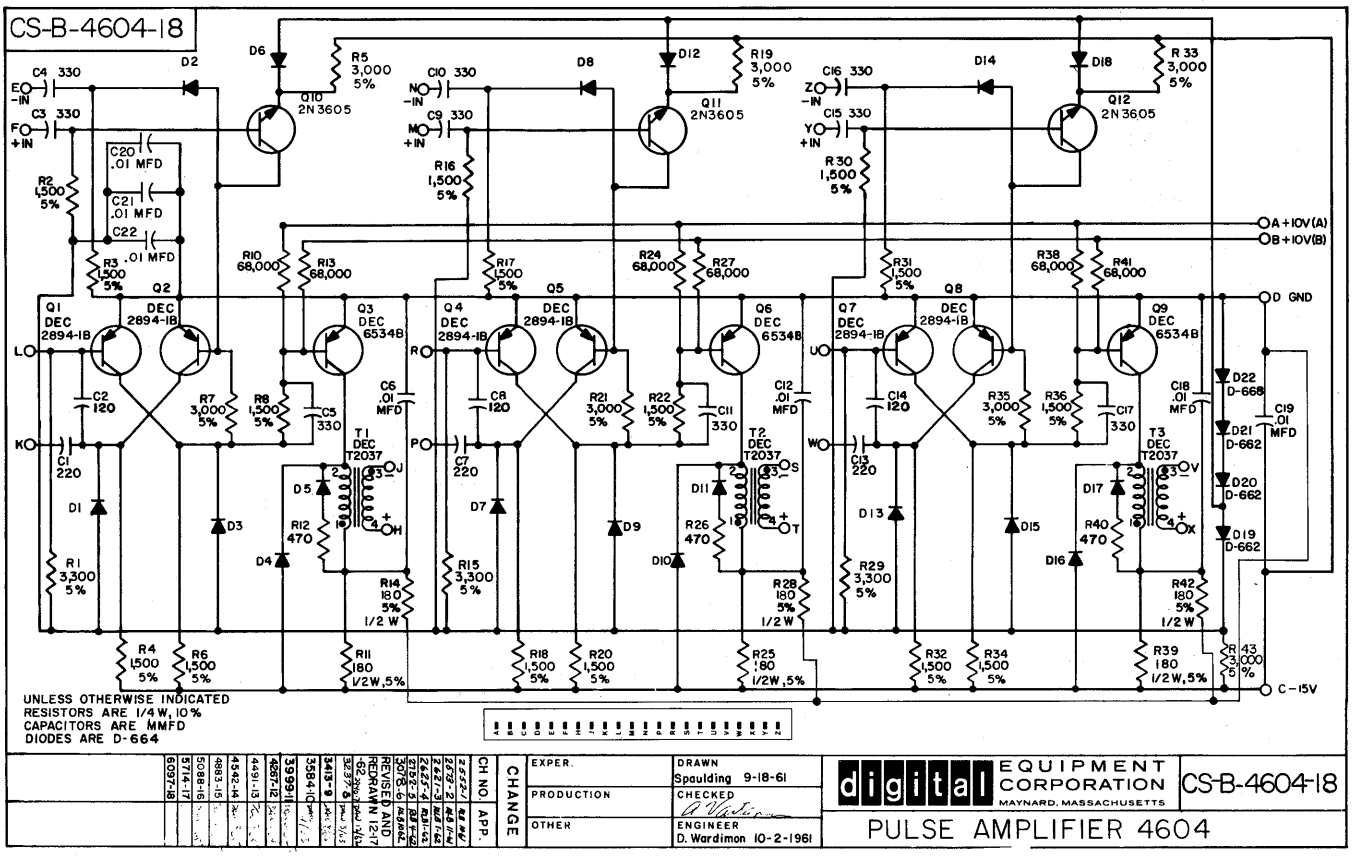
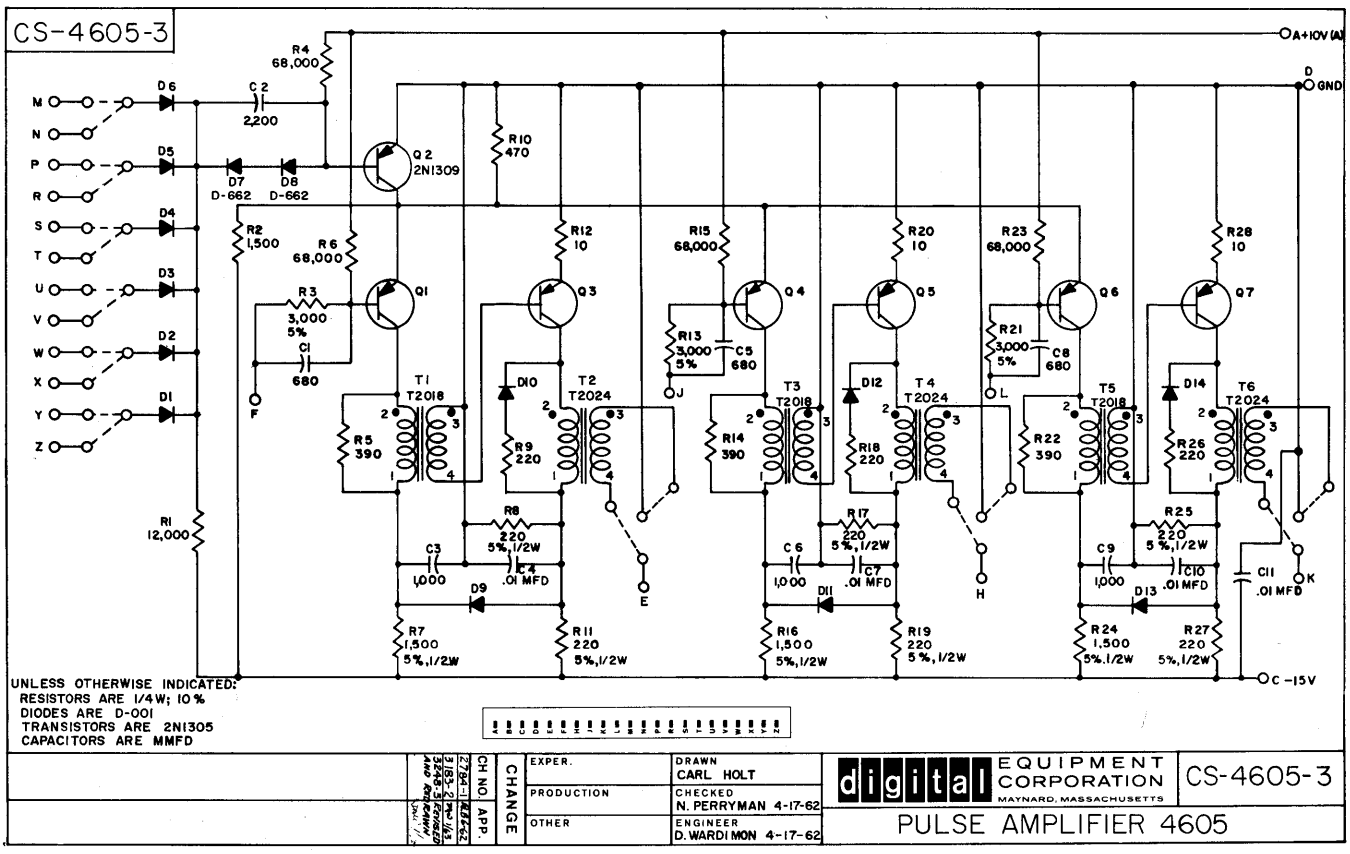
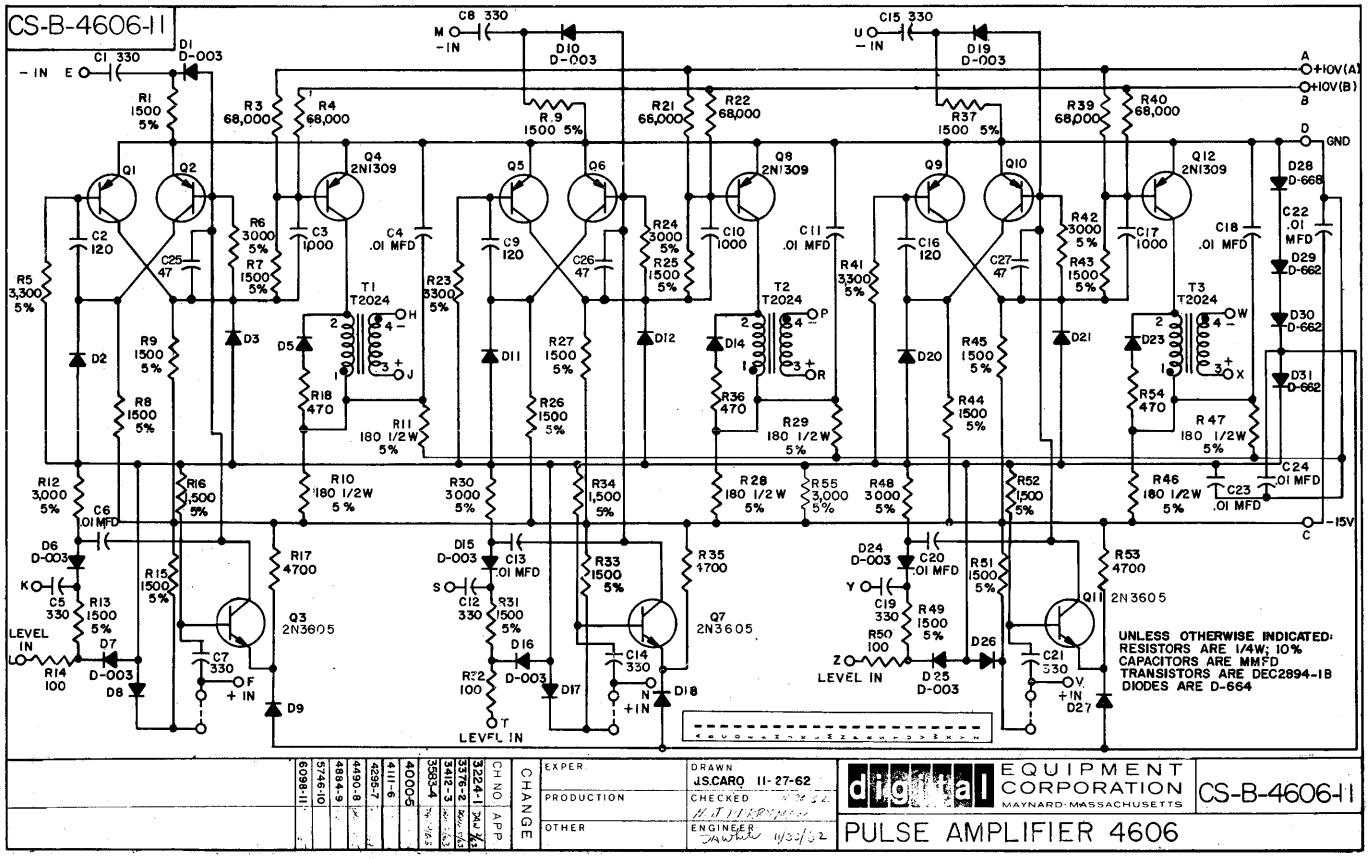
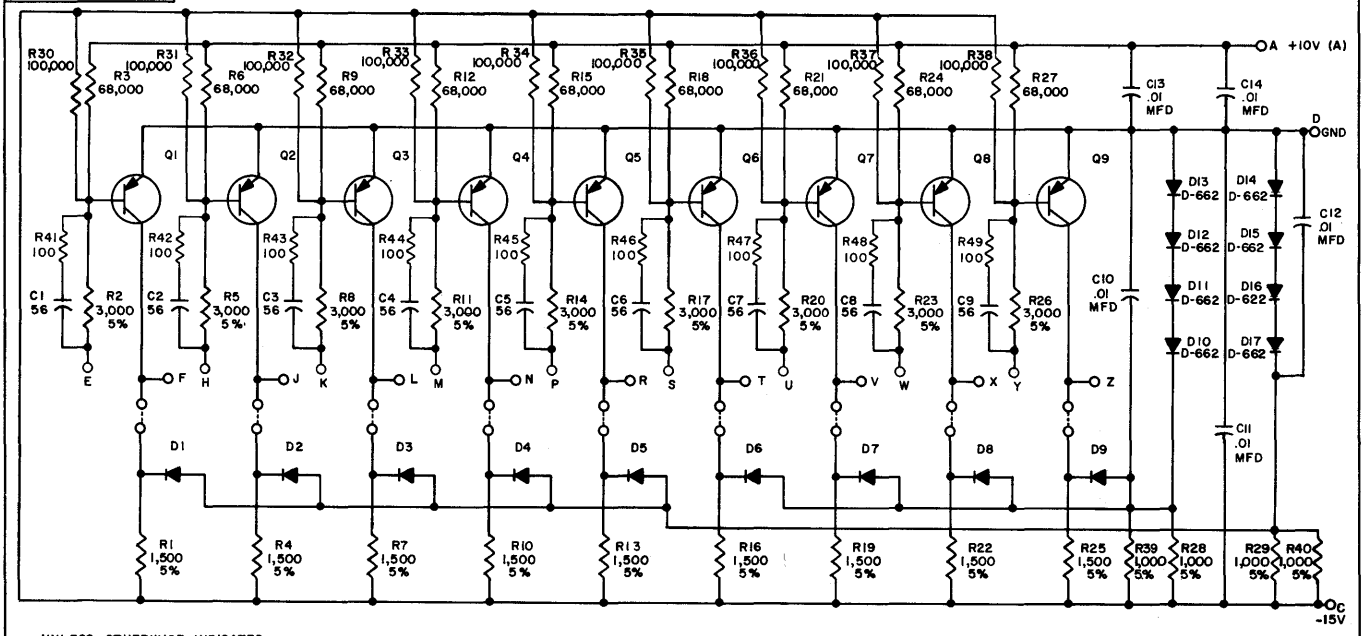
NOTE:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-003
TRANSISTOR & DIODE CONVERSION CHART
DEC 999 MM999
DEC2219 2N2219
D003 1N994
D662 1N645
D664 1N3606
D670 1N3653
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DRUM Y SELECT 4531
SIZE B CODE CS NUMBER 4531-0-1 REV. C
PRINTED CIRCUIT REV. A
DRN. N.PERRYMAN DATE 7-9-64
CHK'D N.PERRYMAN DATE 7-10-64
ENG. R.TRINGALE DATE 7-10-64
PROD. DATE
REVISIONS
DEC FORM NO. DRB 102


CS-B-4604-18
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
CHANGE
EXPER.
PRODUCTION
OTHER
DRAWN Spaulding 9-18-61
CHECKED
ENGINEER D. Wardimon 10-2-1961
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CS-B-4604-18
PULSE AMPLIFIER 4604


CS-4605-3
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-001
TRANSISTORS ARE 2N1305
CAPACITORS ARE MMFD
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
CS-4605-3
PULSE AMPLIFIER 4605


CS-B-4606-11
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC2894-1B
DIODES ARE D-664
digital EQUIPMENT CORPORATION
MAYNARD-MASSACHUSETTS
CS-B-4606-11
PULSE AMPLIFIER 4606

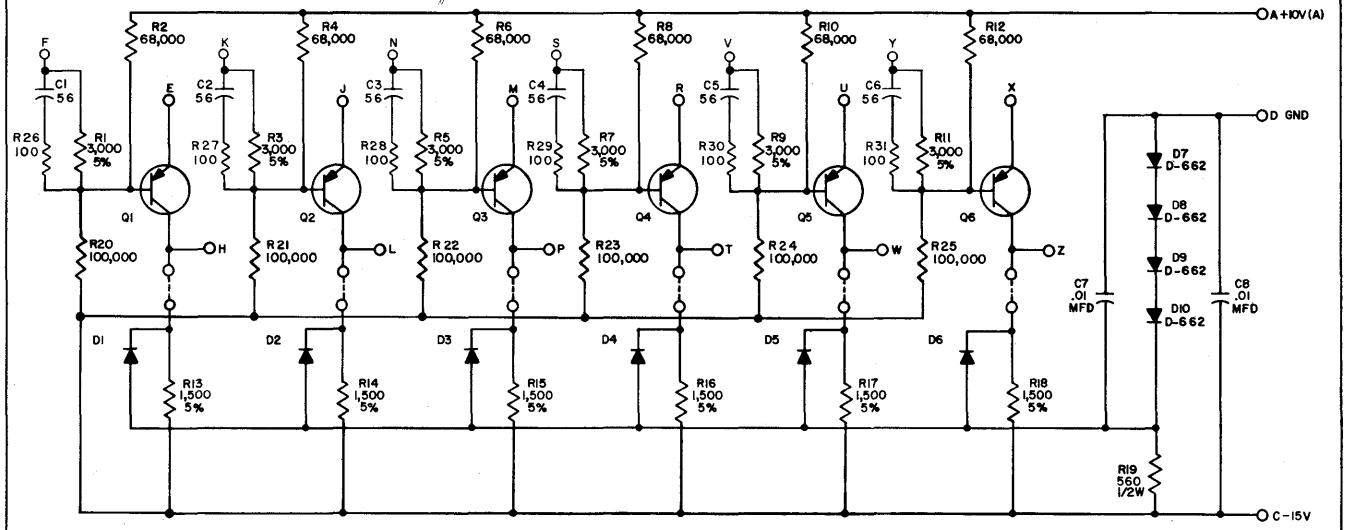
CS-B-6102-6



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-1
DIODES ARE D-664

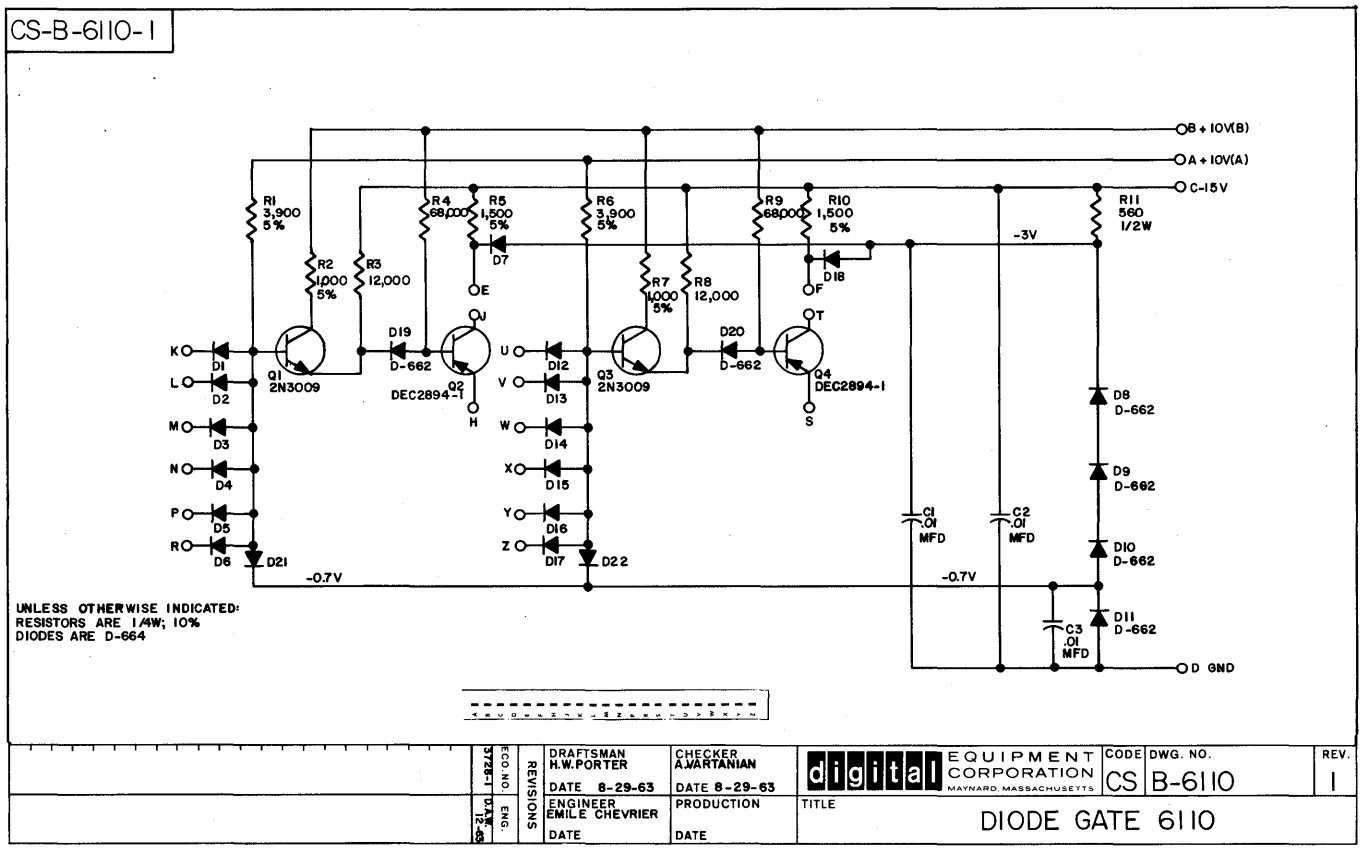
CH NO	APP	CHANGE			
5317-6			EXPER	DRAWN J.S. CARO 2-6-63	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS — CS-B-6102-6
5301-6			PRODUCTION 1	CHECKED	
4338-4			OTHER	ENGINEER	INVERTER 6102
3682-2					

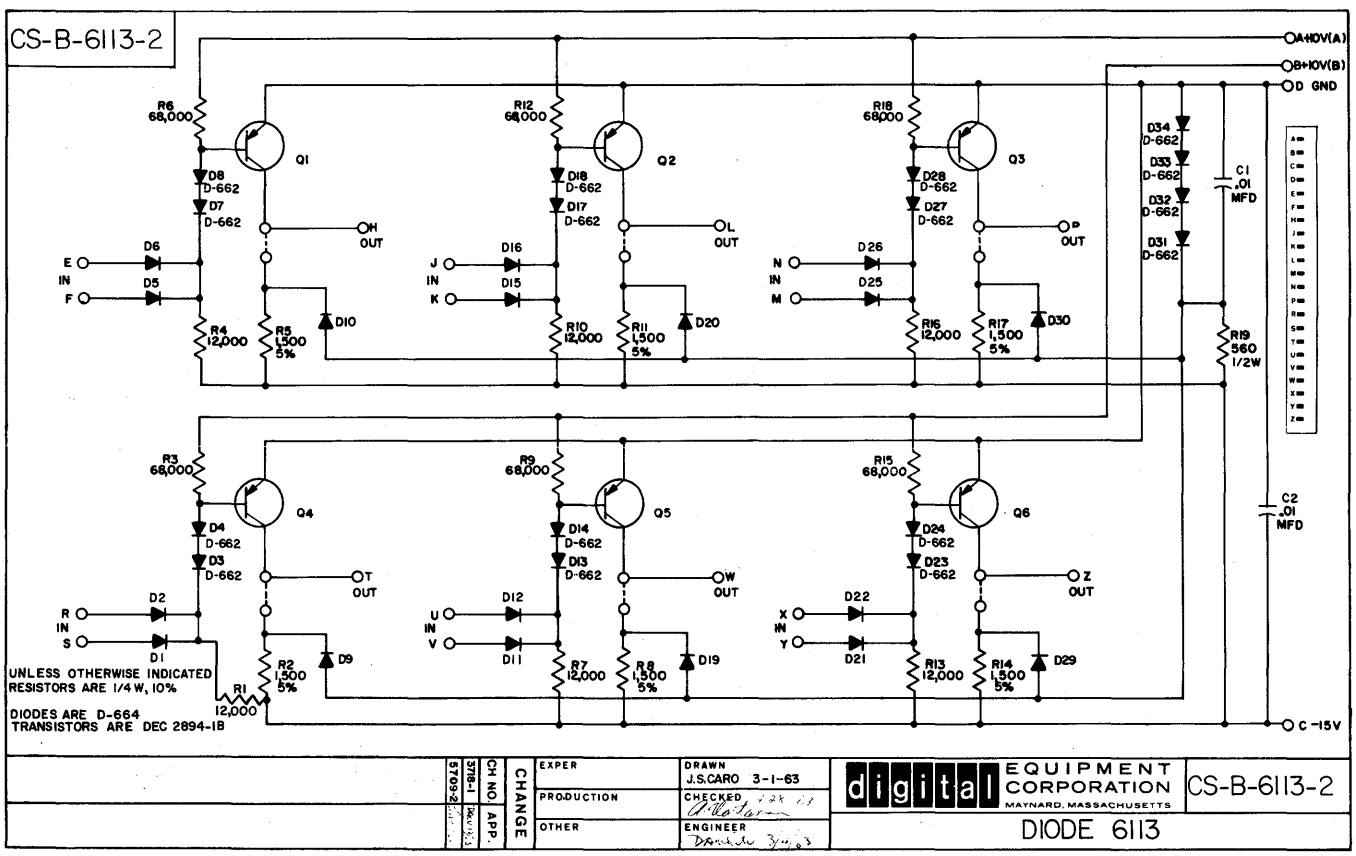
CS-B-6106-7



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-1
DIODES ARE D-664

CH NO	APP	CHANGE			
5319-7			EXPER.	DRAWN PORTER 11-6-61	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS — CS-B-6106-7
5303-6			PRODUCTION	CHECKED PERRYMAN	
3688-5			OTHER	ENGINEER DOANE 11-9-63	INVERTER 6106
2765-3					
2825-2					
2820-1					


CS-B-6110-1
B + 10V(B)
A + 10V(A)
C-15V
R1 3,900 5%
R2 1,000 5%
R3 12,000
R4 68,000
R5 1,500 5%
R6 3,900 5%
R7 1,000 5%
R8 12,000
R9 68,000
R10 1,500 5%
R11 560 1/2W
-3V
D7
D18
D19 D-662
D20 D-662
Q1 2N3009
Q2 DEC2894-1
Q3 2N3009
Q4 DEC2894-1
D8 D-662
D9 D-662
D10 D-662
D11 D-662
C1 .01 MFD
C2 .01 MFD
C3 .01 MFD
-0.7V
D GND
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-664
DRAFTSMAN H.W.PORTER DATE 8-29-63
CHECKER A.VARTANIAN DATE 8-29-63
ENGINEER EMILE CHEVRIER DATE
PRODUCTION DATE
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CODE CS
DWG. NO. B-6110
REV. 1
TITLE DIODE GATE 6110
REVISIONS
ECO. NO. 3728-1
ENG. D.A.W. 12-63


CS-B-6113-2
A+10V(A)
B+10V(B)
D GND
R6 68,000
R12 68,000
R18 68,000
Q1
Q2
Q3
D8 D-662
D7 D-662
D18 D-662
D17 D-662
D28 D-662
D27 D-662
D34 D-662
D33 D-662
D32 D-662
D31 D-662
C1 .01 MFD
H OUT
L OUT
P OUT
E IN
F
J IN
K
N IN
M
D6
D5
D16
D15
D26
D25
R4 12,000
R5 1,500 5%
D10
R10 12,000
R11 1,500 5%
D20
R16 12,000
R17 1,500 5%
D30
R19 560 1/2W
R3 68,000
R9 68,000
R15 68,000
Q4
Q5
Q6
D4 D-662
D3 D-662
D14 D-662
D13 D-662
D24 D-662
D23 D-662
C2 .01 MFD
T OUT
W OUT
Z OUT
R IN
S
U IN
V
X IN
Y
D2
D1
D12
D11
D22
D21
R2 1,500 5%
D9
R7 12,000
R8 1,500 5%
D19
R13 12,000
R14 1,500 5%
D29
R1 12,000
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-1B
C -15V
EXPER
PRODUCTION
OTHER
DRAWN J.S.CARO 3-1-63
CHECKED
ENGINEER
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CS-B-6113-2
DIODE 6113
CHANGE
CH NO. 3718-1
APP.
5709-2

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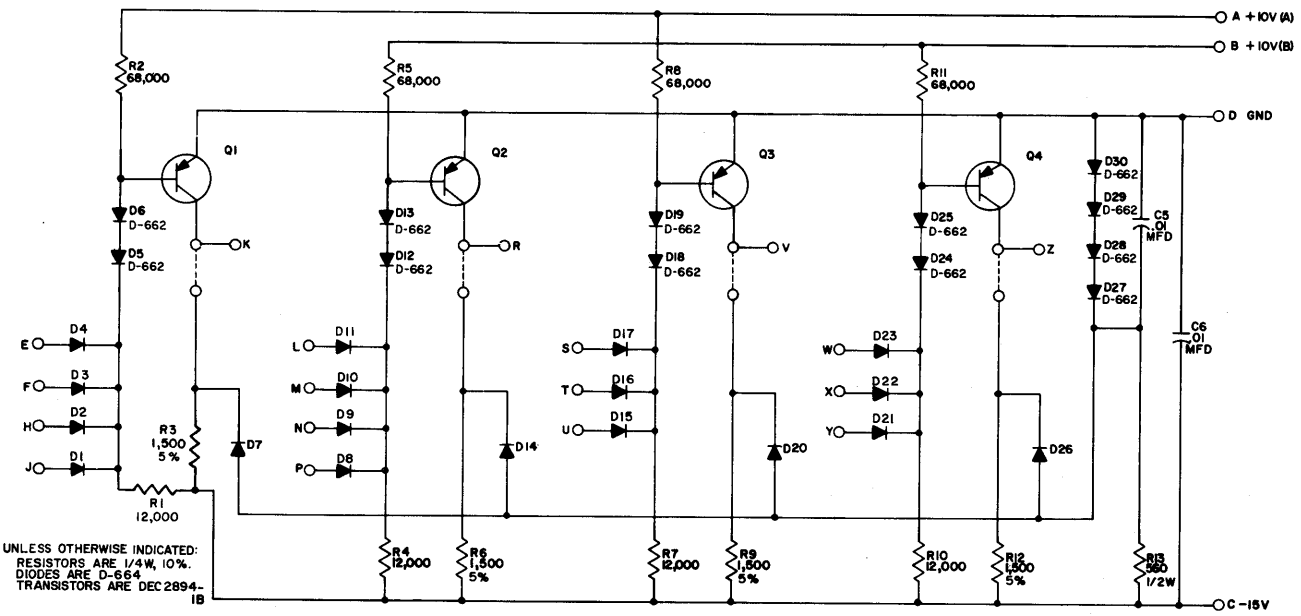

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%.
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-1B

REVISIONS			
CHK	CHG NO.	REV.	
DAW	3719	1	
REV & REDR.	5845	B	

DRN.	J.S. CARO	DATE 3-1-63
CHK'D	A. VARTANIAN	DATE 3-1-63
ENG.	D.A. WHITE	DATE 3-4-63
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC2894-1B	NONE		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DIODE GATE 6115

SIZE	CODE	NUMBER	REV.
B	CS	6115-0-1	B

PRINTED CIRCUIT REV. C D

DEC FORM NO. DRB 102

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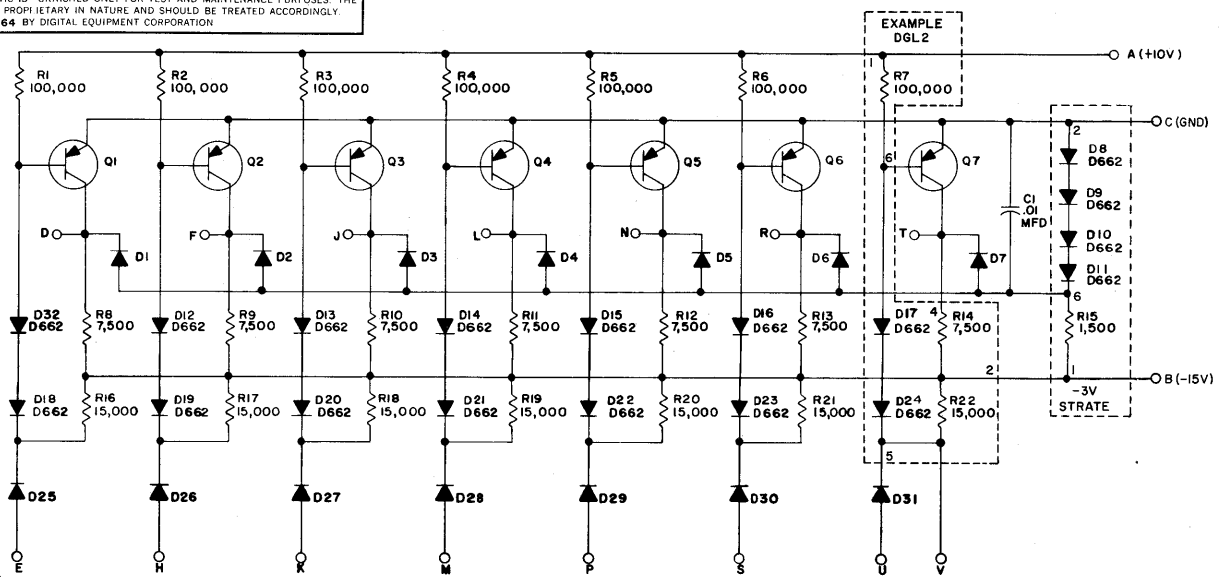

UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

REVISIONS						
CHK	CHG NO.	REV.		E	F	H
DAW	4863	1		5461	5685	6539
REV & REDR.	5377	D				

DRN	A QUELLETTE	DATE 9-1-64
CHK'D	N PERRYMAN	DATE 9-10-64
ENG.	D WHITE	DATE 9-10-64
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639B	2N3639		
D662	IN645		
D664	IN360E		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: INVERTER R107

SIZE	CODE	NUMBER	REV.
B	CS	R107-0-1	H

PRINTED CIRCUIT REV. C D

DEC FORM NO DRB 102

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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