Digital Equipment Corporation
Maynard, Massachusetts

digital

Maintenance Manual

RF08 DISK CONTROL AND RS08 DISK

DEC-08-HIEA-DA

RF08 DISK CONTROL AND RS08 DISK MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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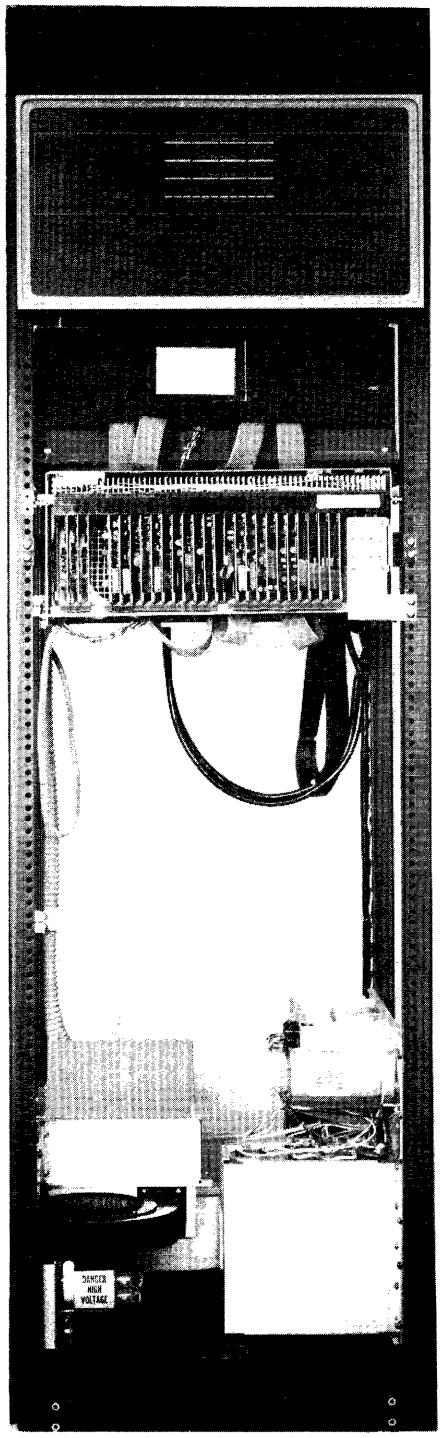
RF08 DISK CONTROL AND RS08 DISK MAINTENANCE MANUAL



RF08 Disk Control and RS08 Disk (Rack Mounted, Front View)

Chapter 1
General Description

1.1 INTRODUCTION

The RF08 Disk Control and the RS08 Disk (see Frontispiece) combine to provide high-speed bulk storage for DEC PDP-8, PDP-8/I, PDP-8/L, LINC-8 and PDP-12 computers. Each RS08 Disk has a storage capacity of 2048 words on each of 128 tracks, giving a total storage capacity of 262,144 words. Each word contains 12 bits of data, plus a 13th bit for read parity checking. The RF08 Disk Control (see Figure 1-1) controls up to four RS08 Disks (see Figure 1-2) giving the disk file a maximum storage capacity of 1,048,576 words.

The disk file operates under program control of the associated compatible computer and uses the three-cycle data break facility of the computer. While operation is identical with any central processor, all references in this manual are to the PDP-8 central processor.

The length of a data block is variable and is specified by loading the word length as a negative number into the word count (WC) register. The length of a single block is limited only by the maximum number of words (4096) that can be specified in a 12-bit register.

The starting address for a data transfer can be selected randomly. The data words in the data block are then transferred sequentially to or from the disk. The initial instruction (to read or write) executes the block transfer, which can be from 1 to 4096 words. The first address to be used for data transfer is placed in the current address (CA) register. As the block transfer proceeds, the current address register is incremented, and data is transferred sequentially to or from a block of consecutive memory addresses.

Address 7750_8 is permanently assigned as the word count register in the PDP-8; address 7751_8 is the current address register. When the disk is addressed, these memory locations are selected automatically.

1.2 SPECIFICATIONS

Specifications for the RF08 and RS08 Disk File system are summarized in Table 1-1.

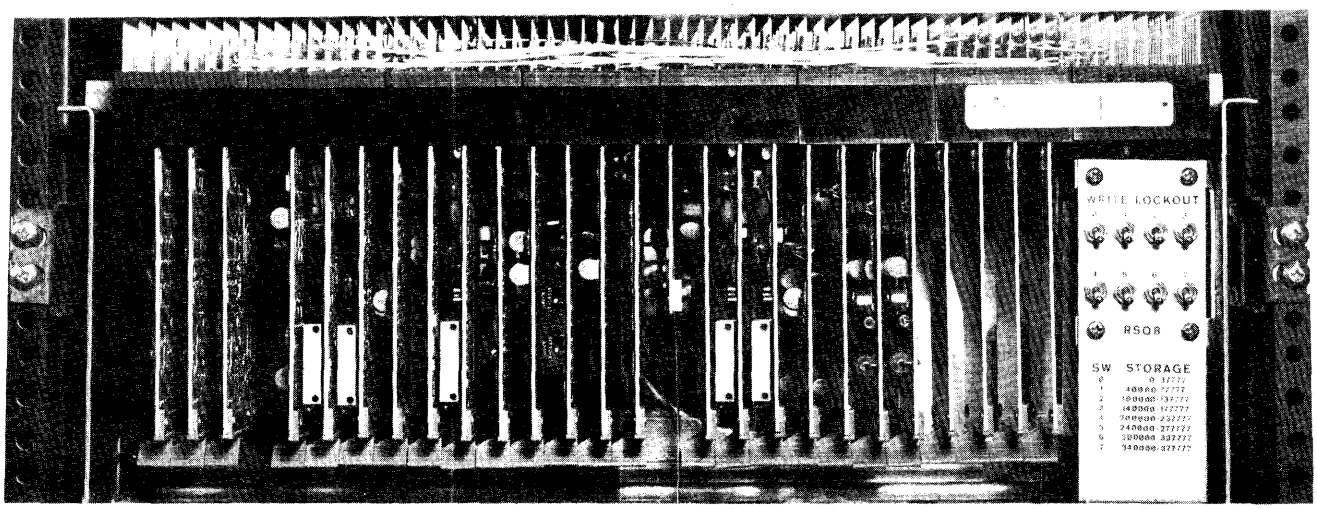


Figure 1-1 RS08 Read/Write Logic
(Logic Modules and Write-Lockout Switches)

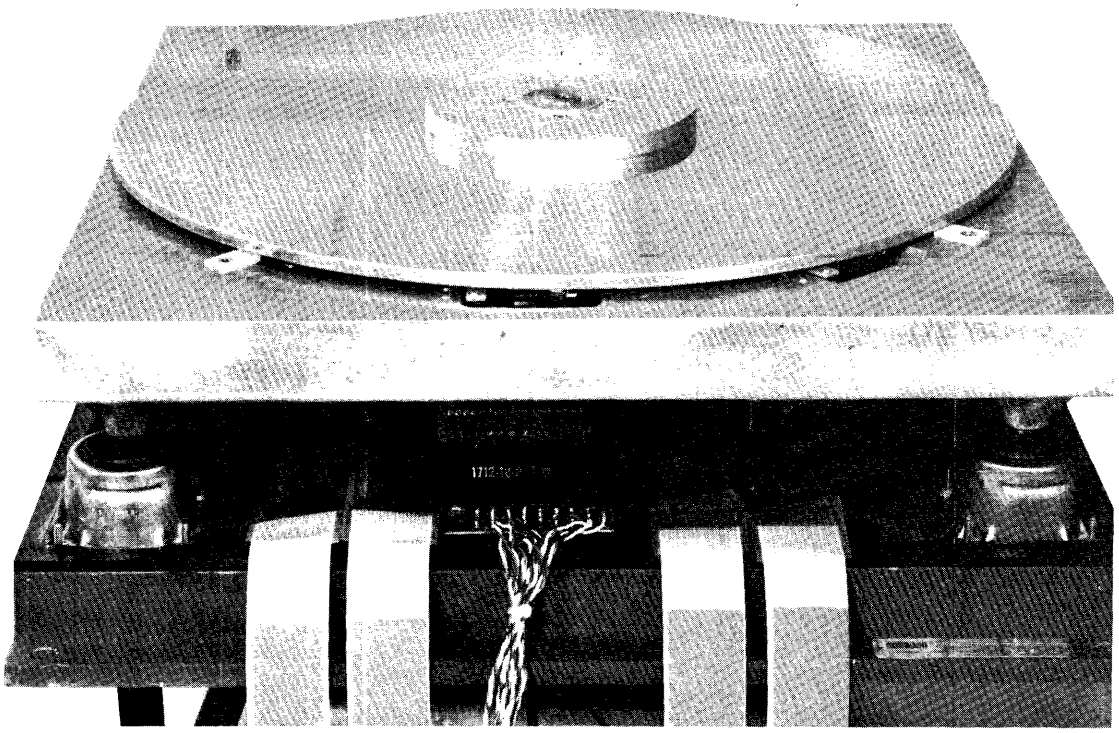


Figure 1-2 RS08M Disk (With Cover Removed)

Table 1-1
RF08 and RS08 Disk File System Summary of Specifications

Disks	Four RS08s can be controlled by one RF08 to provide storage for up to 1,048,576 words.	
Storage Capacity	Each RS08 stores 262,144 13-bit words (12 data bits plus 1 even parity bit).	
Memory Locations Used	7750_8 Word Count 7751_8 Current Address	
	60-Hz Power	50-Hz Power
Data Transfer Rate	16.0 μs per word	19.2 μs per word
Minimum Access Time	258 μs	320 μs
Average Access Time	16.9 ms	20.3 ms
Maximum Access Time	33.6 ms	40.3 ms
Program Interrupt	33 ms clock flag Data transmission complete flag Error flag	
Write Lockout Switches	Eight switches per RS08 are capable of locking out any combination of eight 16,384 word blocks in address 0 to 131,071.	
Data Tracks	128	
Words Per Track	2048	
Recording Method	NRZI	
Density	1100 bpi (maximum)	
Timing Tracks	Three, plus three spare (spares can be used to recover data on disk).	
Operating Environment	Disk Operating: Recommended temperature 60° to 100°F; a change in temperature not to exceed ±20°F/hr. Relative humidity 8% to 80%. Maximum wet bulb, 78°F; no condensation (storage or operating) can be allowed. Disk Stopped: Relative humidity 0 to 55 %, no condensation. Temperature range 0° to 120°F.	
Vibration/Shock	Adequate isolation is provided to prevent data errors. CAUTION Extreme vibrations should be avoided while the RS08 is transferring information.	
Heat Dissipation	RF08: 150W RS08: 300W	
Power Requirements (Logic Only)	115/230 Vac ± 10%, single phase, 50 ± 2 Hz or 60 ± 2 Hz, 5A (maximum) for logic power. NOTE Logic power for one RF08 and up to four RS08s is provided by one DEC Type 705B power supply. Additional line current is required for the RS08 disk motor, shown as follows.	

Table 1-1 (Cont)
RF08 and RS08 Disk File System Summary of Specifications

RS08 Motor Power Requirements	Motor Start: 5.5A for 20 ± 3s Motor Run: 4A continuous @ 115 Vac. A stepdown autotransformer is provided for 230 Vac operation.
Line Frequency Stability	Maximum line frequency drift 0.1 Hz/s. A constant frequency motor-generator set or static ac/ac inverter should be provided for installation with unstable power sources.
Motor Bearing Life	Expected operating life of at least 20,000 hours, under standard computer operating environment.
Reliability	Five recoverable errors and one nonrecoverable error in 1×10^{10} bits transferred. A recoverable error is defined as an error that occurs only once in four successive reads. All other errors are nonrecoverable. NOTE On-off cycling of the RS08 is not recommended. For this reason, the RS08 motor control operates independently of the computer power control.
Cabinet	A DEC cabinet is designed to accommodate one RF08, up to two RS08s and a power supply. Two additional RS08s can be mounted in a second cabinet. Other equipment should not be mounted in disk cabinets.
Shipping Information	Weight of an RF08, one RS08, a power supply and cabinet: 590 lb (crated) 500 lb (uncrated) Weight of an RF08, two RS08s, a power supply and cabinet: 690 lb (crated) 600 lb (uncrated) (The RF08/RS08 are shipped mounted in cabinets.)

Chapter 2
Installation

2.1 INTRODUCTION

The RF08 and RS08 mount in a standard DEC cabinet Type H950 using "Chassis-Track" slides (part number C-300-S-20). Installations with one or two RS08 Disks require a single cabinet; however, if three of four disks are to be installed, a second cabinet is required. A single power supply, Model 705B, supplies power to all logic circuits. Each disk is a sealed unit that contains the drive motor, disk, heads, and electrical networks for the heads. A separate chassis for each disk contains the RS08 Logic and Motor Control.

CAUTION

The RS08M Disk Assembly MUST NOT be opened in the field by personnel other than authorized DEC Field Engineers. Special procedures, alignment and adjustment fixtures, and cleaning equipment is required to service the disk. Any attempt to remove the recording surface by inexperienced or untrained personnel will invariably destroy the surface of the disk. Any unauthorized openings of the RS08M Disk Assembly will void all warranties applying to the unit.

2.2 REQUIREMENTS

For disk file power requirements see Figures 2-1, 2-2, and 2-3. The disk system is supplied with a 25 ft, 30A, 3-wire, pigtail line cord for North American installations. Table 2-1 specifies the Hubble connectors which are to be attached to the line cord.

2.2.1 Unpacking the RS08 Disk

Before proceeding with the following unpacking instructions, it is recommended that the cabinet front dress panel be removed and the rear door opened for easy access to the components.

Unpacking Instructions:

Step	Procedure
1	Remove the silver cloth tape from around the Disk drive motor protection pan and then remove the pan and the bag of Drierite desiccant.
2	Unwrap the Disk drive motor leads (blue, green, yellow, red, and black) from around the motor.
3	Connect the drive motor color-coded wires of Step 2 to the indicated color-coded connections on the back of the RS08 Disk motor control chassis.
4	Remove the drive motor lock located on the drive motor shaft.
5	Turn the drive motor control switches on the back of the RS08 motor control chassis to the OFF position.
6	Switch the H718 power supply line filter circuit breaker to OFF.

2.2.2 Disk Motor Power

The Disk motor operates from a 105 to 130 Vac, 60 Hz ± 2 Hz power bus (50 Hz, 230 Vac on special order). Because of synchronous drive motor characteristics, the maximum rate of ac power source frequency drift must not exceed 0.1 Hz/s. Line transients exceeding the operating voltage limits will require site provisions for regulating the power supply voltage. Disk motor power must be supplied from an unswitched bus.

Table 2-1
Primary Power Connectors
(North American Installations Only)

Line Voltage (Single Phase)			Hubbell Connector Part Number
115V	60 Hz	30A	3331-6 or 3331
230V	60 Hz	20A	none supplied
115V	50 Hz	30A	none supplied
230V	50 Hz	20A	3321-6 or 3321

2.2.3 Logic Power

The logic power supply should be connected to the central processor switched power bus. The power supply (see Figure 2-4) has sufficient capacity to power one RF08 Disk Control and four RS08 Disks. This power supply must not be used to supply power to other units. Noise generated on the power supply buses could affect data transfer reliability.

2.2.4 Ground Circuits

The cabinet containing the disk file must be grounded by mechanical connection to the central processor. All grounds must be connected to a common ground point to prevent circulating currents in the ground circuits. All grounds must be installed before connecting the unit to the ac power mains, to prevent possible damage to the logic circuits.

2.2.5 Connection of RF08 to Central Processor

Figure 2-5 shows proper cable connections between the RF08 Disk Control and the central processor and proper termination techniques at the time of installation. Cables should be routed away from ac power lines and from other data cables that might introduce noise.

2.2.6 Connection of RF08 to RS08

The cable interconnections between the RF08 Disk Control and RS08 Disk for installations with one to four RS08 Disks is shown in Figure 2-6. Cables must be routed to allow the RS08 Disk Logic Chassis to be pulled all the way out without damaging the cables.

2.2.7 Connecting the Purging Blowers

Set the H718 power supply line filter circuit breaker to ON. POWER TO THE DISK DRIVE MOTOR MUST NOT BE ON.

NOTE

The purge unit hose has not been connected at this point; therefore, turning the Disk power on purges the purge unit prior to making connection to the disk unit. This purging should be performed for at least one half hour.

After the purging period, remove the Disk unit purge cap and connect the purge unit hose to it.

2.3 ACTIVATING THE DISK

The following sequence shows the proper procedure for activating the disk.

Step	Procedure
1	Remove the disk drive motor shaft locks from each RS08M Disk in the system and check for loose wires.
2	Turn the H718A Power Line Filter ON (the switch is located in the bottom rear part of the RF08 Cabinet) and observe that the pilot lamp is illuminated, indicating that power is available at the output of H718A.

Step	Procedure
3	Turn the DISK POWER switch ON lighting the START and OPERATE lamps. This switch is located in the rear of the RS08 Disk Logic Chassis.
	NOTE The disk is inoperable while the START lamp is lit. Power transients, caused when the DISK POWER switch is operated, can cause data errors if another disk in the system is operating and transferring data.
4	Make certain the disk is running and that its blower is operating.
5	After 20 sec, the START lamp will go out; this indicates the acceleration run is complete, and the disk motor has switched to run power.
6	Repeat Steps 1 through 5 above for other disks.

2.4 PERIODIC MAINTENANCE

The air filters in the disk purging system are the only items that require periodic service or replacement. If the disk is located in a particularly dirty area, or close to a line printer, more frequent service may be necessary; however, for the average office environment, the following service schedule should be followed.

Monthly Service:

Vacuum the polyethyrene foam prefilter, located in the bottom front of the disk cabinet. The cabinet filter on top of the disk cabinet should be inspected and cleaned as required. Both operations can be performed while the system is operating.

Six Month Service:

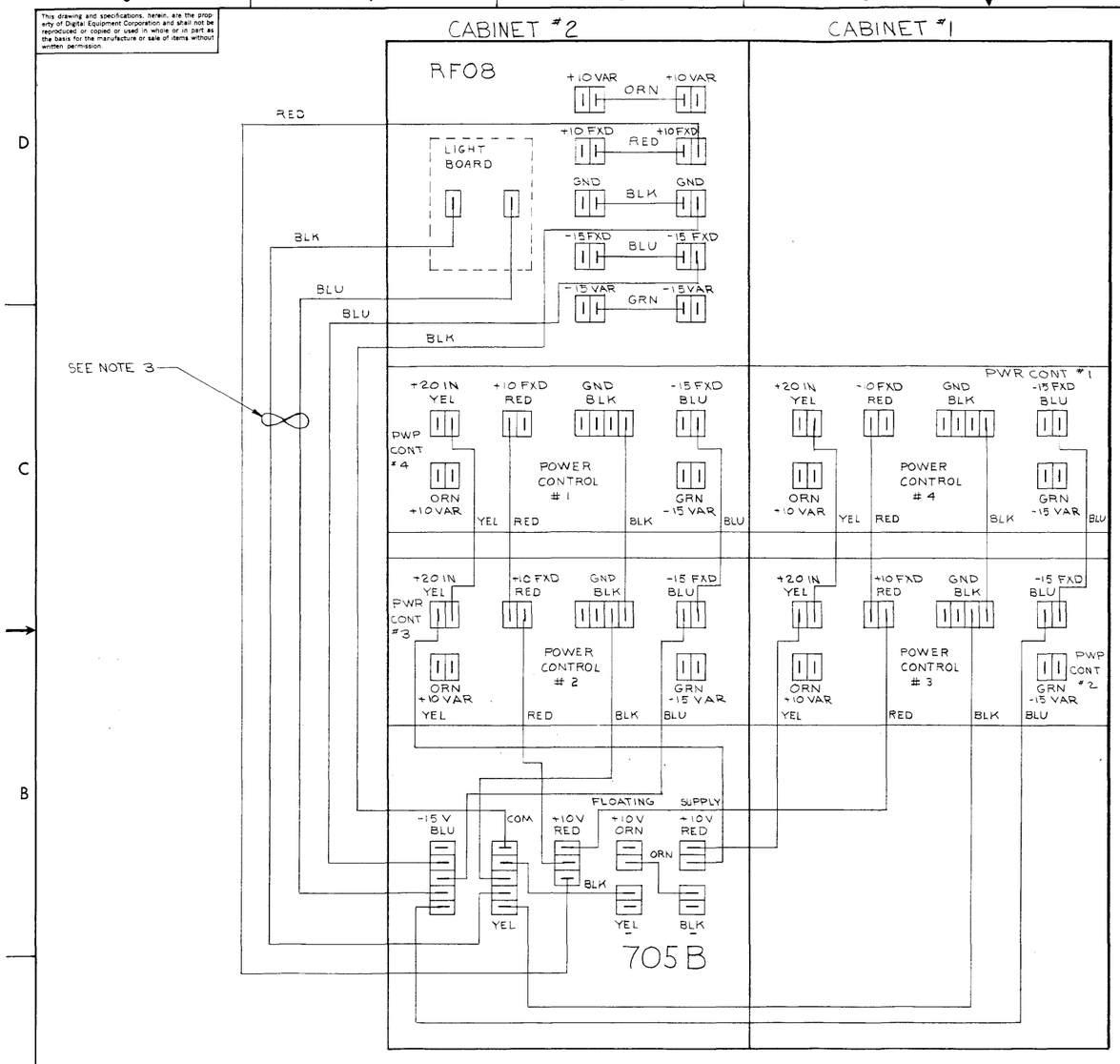
Turn off each disk at its power control panel and disconnect disk and logic power by tripping the circuit breaker on the H718A Power Line Filter and on the computer system. Perform the Monthly Service.

Additional Six Month Service:

The procedure below is followed for additional six month service.

Step	Procedure
1	Remove the foam prefilter screening and retainer, then remove the foam element. Wash the foam in warm water and detergent, rinse thoroughly and set it aside to dry.
2	Remove the hoses from the absolute filter system (top aluminum cover). Remove the eight cover screws, lift and discard the absolute filter.

Step	Procedure
3	Replace the absolute filters with DEC P/N 12-09388 filters. Carefully shake out any loose material that may be lodged on the filter.
	NOTE DO NOT blow off dust from the new filter with an air hose, since this may puncture the filter media.
4	Carefully lower the new filter into place, making certain the foam gasket faces upward.
5	Replace the top aluminum cover and tighten the hold down screws. Reinstall the foam prefilter.
6	It is necessary to let the filter purge itself before reconnecting disk hoses. Turn on the system power and H718A power. The blower is now operational. Allow the blower to run for at least 30 minutes before reconnecting the hoses.
7	Reconnect the hoses and purge the disk file for an additional 30 minutes.
8	Restart each disk system.



DC WIRING

NOTES:

1. ALL DC WIRES TO BE #14 AWG STRD TEF.
2. DC WIRES ARE TO BE KEPT SEPARATE FROM AC WIRES. DC WIRES TO BE DRESSED TO REAR RIGHT HAND CORNER OF CABINET.
3. TWIST BLU/BLK LIGHT BOARD WIRES APPROXIMATELY ONE TWIST PER INCH.
4. DRESS POWER CONTROL WIRES WITH SUFFICIENT SLACK TO PERMIT CHASSIS TRAVEL; COVER WITH SPIRAL WRAP.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

DRN. DATE 3/29/67
CHK'D. DATE 4/3/67
ENG. DATE 4/13/67
PROJ. ENG. DATE 4/13/67
PROG. DATE 4/17/67
MATERIAL
FINISH
SCALE 1
SHEET 2 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: WIRING, POWER AC, DC RF08/R208

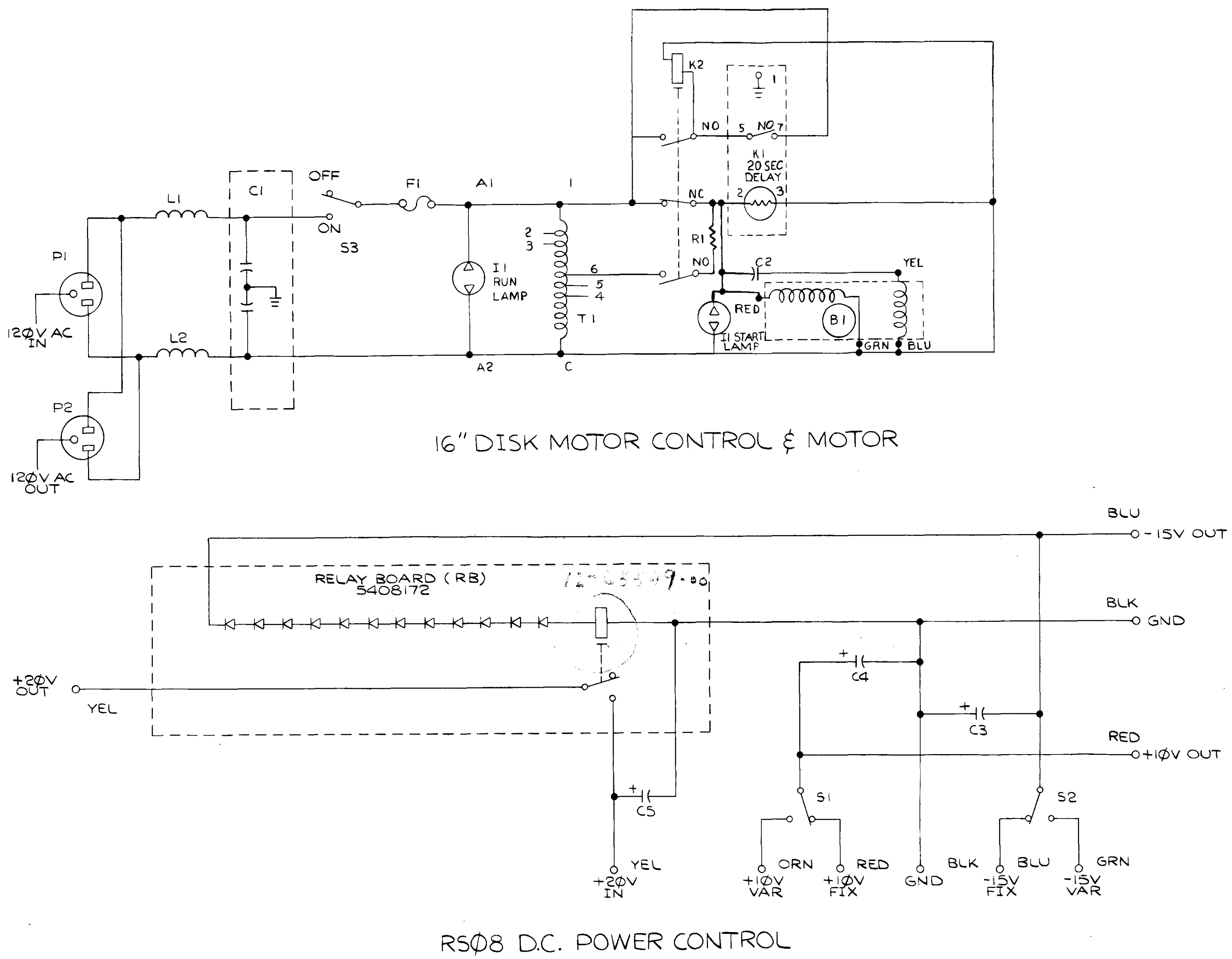
SIZE D | CODE | NUMBER MC-RS08-0-2 | REV. C

DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO 12MC 10K

Figure 2-1 dc Power Wiring Diagram



REF DESIGNATION	DESCRIPTION	PART NO.
R1	RES 1.5 Ω 10W	1300148
C1	CAP 2×.1MFD 600VDC	1002153
C2	CAP 30MFD 370V	1009122
C3,C4,C5	CAP 50MFD 50V	1000080
K1	TIMING RELAY	1209121
K2	EBERT RELAY	1209491
B1	MOTOR 50 HZ	1209003-21
B1	MOTOR 60 HZ	1209003-20
I1,I2	LIGHT PILOT 110V	1205458
T1	2:1 AUTO XMFR	1609313
S1,S2,S3	SWITCH SPDT	1202279
L1,L2	TUBE FERROXCUBE	1605147
F1	7AMP S.B. FUSE	9007224
RB	RELAY BOARD	5408172
P1	SOC 3 PIN AC MALE	1201252
P2	SOC 3 PIN FEMALE	1201251

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE POWER CONTROL AND MOTOR CONTROL

SIZE D CODE CS NUMBER 7006156-0-1 REV. C

DEC FORM NO. DRD 101

Figure 2-2 Power and Motor Control Circuit Schematic Diagram

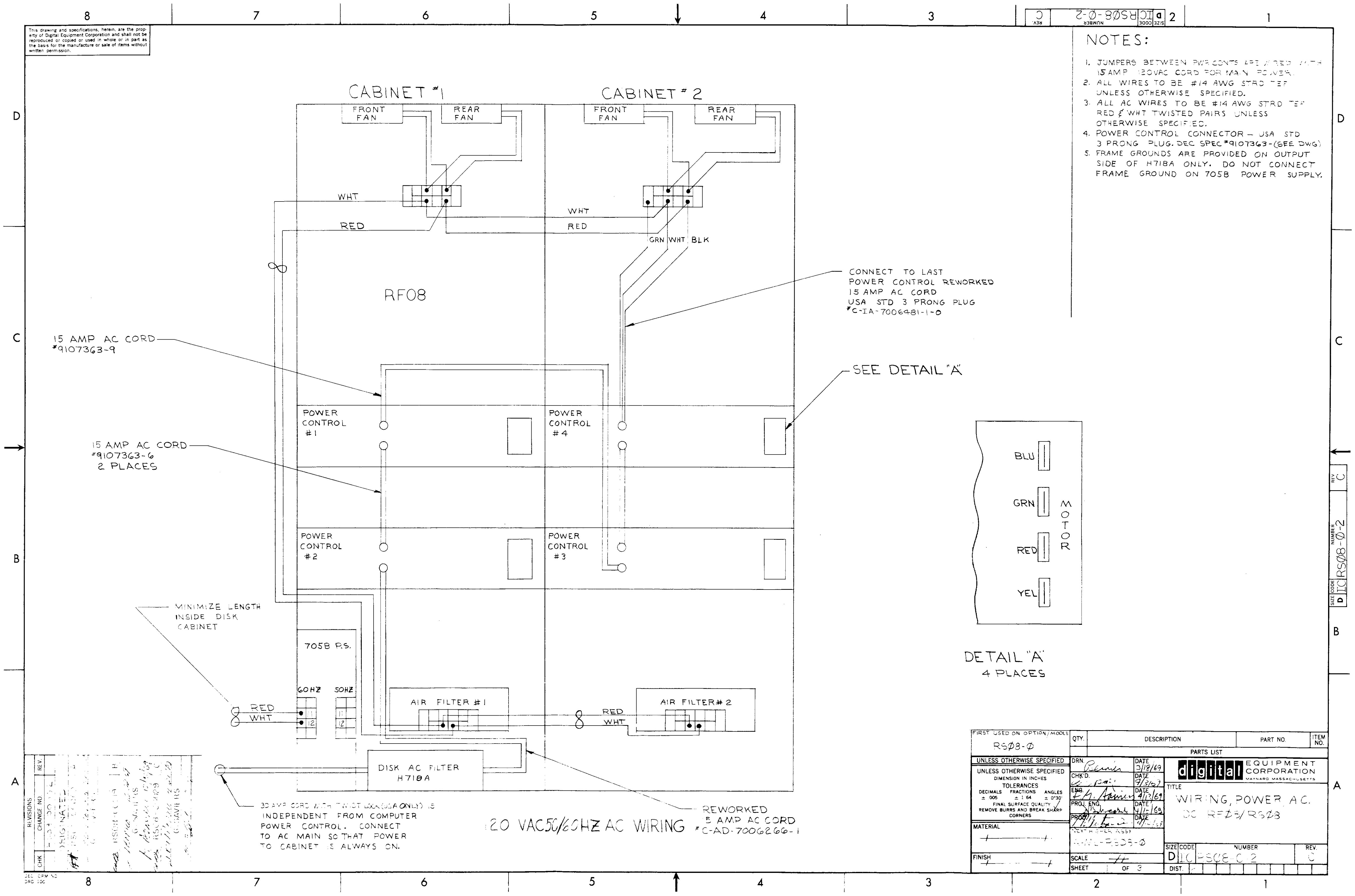


Figure 2-3 120 Vac 60 Hz Schematic Diagram

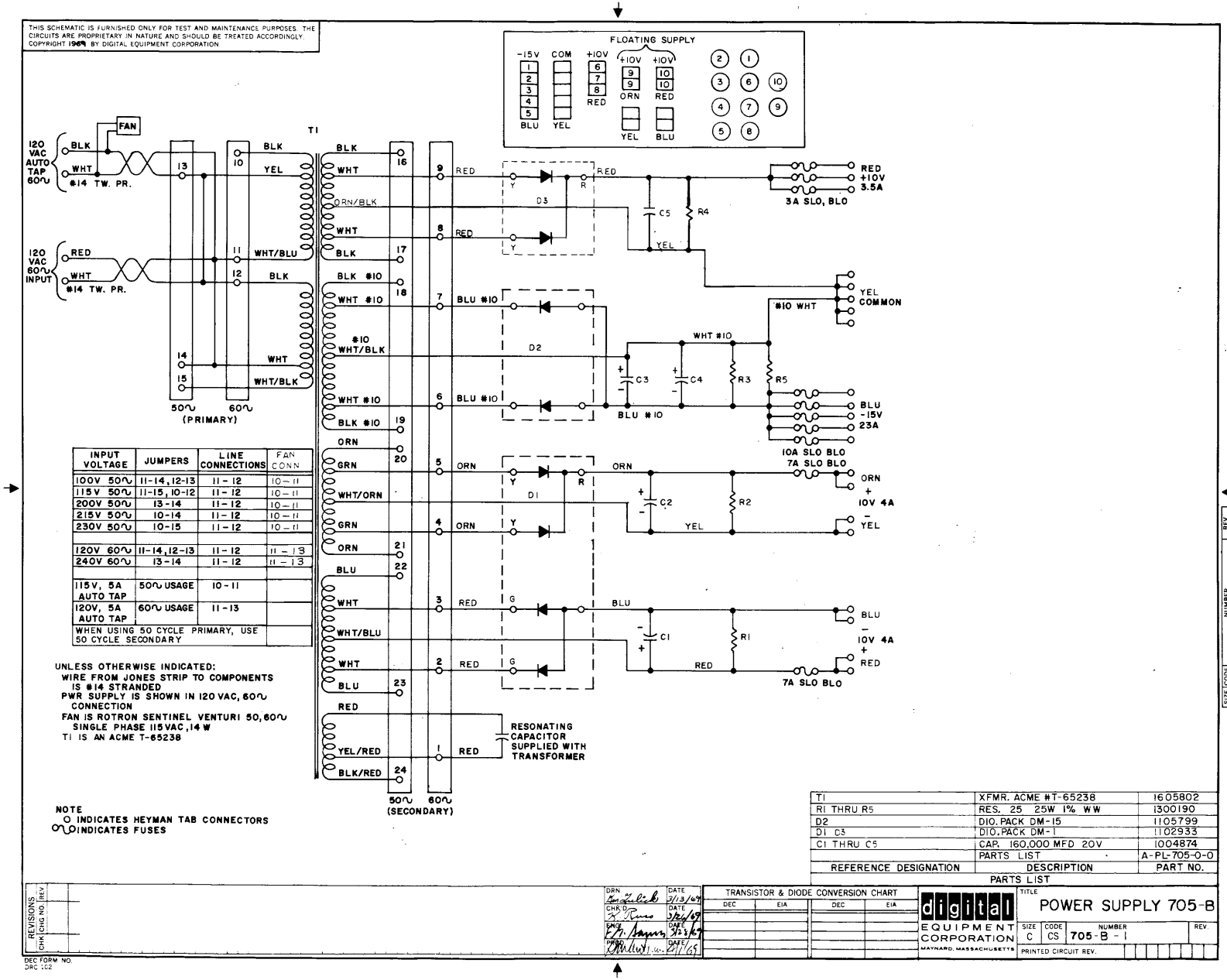
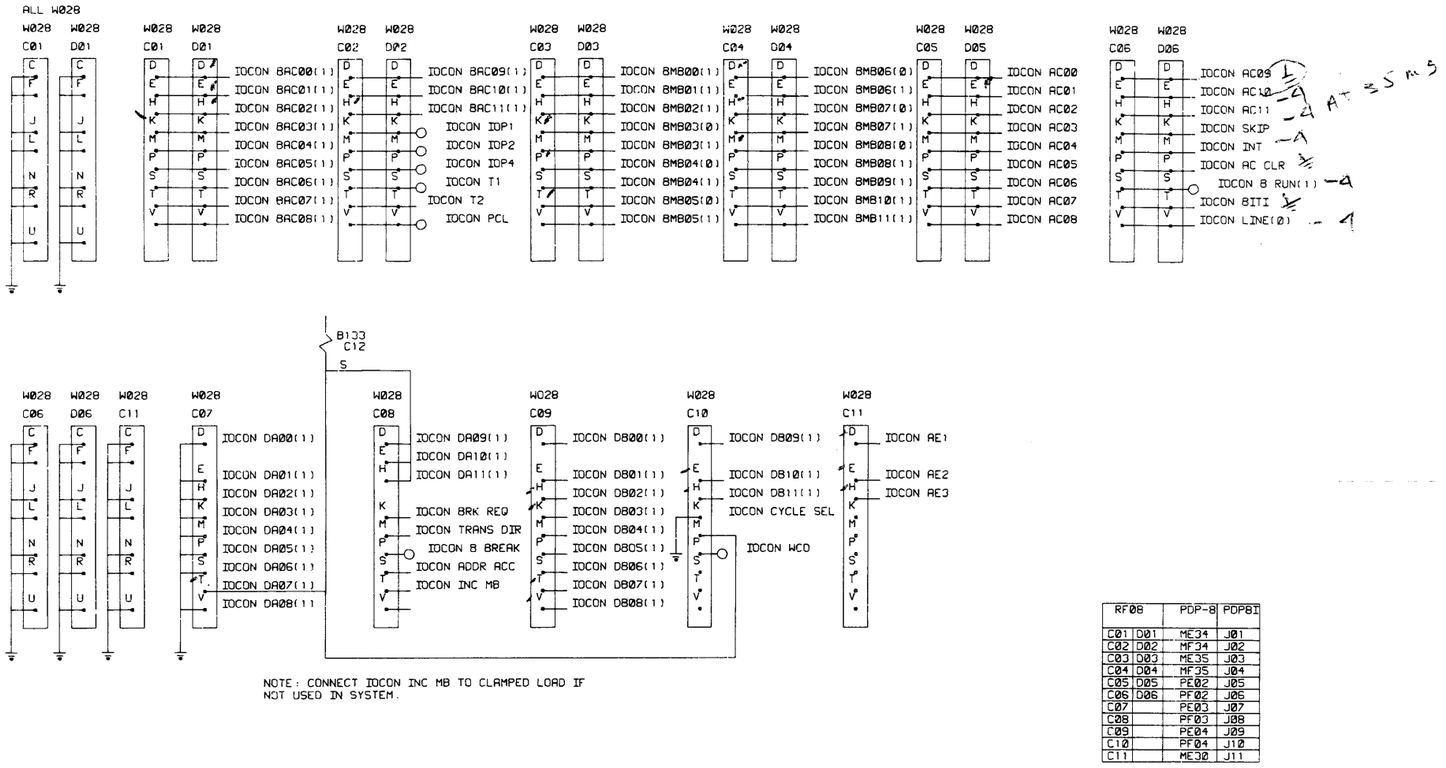


Figure 2-4 705-B Power Supply



NOTE: CONNECT IOCON INC MB TO CLAMPED LOAD IF NOT USED IN SYSTEM.

RF08		PDP-8	PDP8I
C01	D01	ME34	J01
C02	D02	MF34	J02
C03	D03	ME35	J03
C04	D04	MF35	J04
C05	D05	PE02	J05
C06	D06	PF02	J06
C07		PE03	J07
C08		PF03	J08
C09		PE04	J09
C10		PF04	J10
C11		ME30	J11

REVISIONS		
CHK	CHANGE NO.	REV.
	271	A
	BISSONNETTE 6/10/68	
	R.BRUNO 6/10/68	
5/13	RF08-00.005	B
	T. Bissonnette 9/24/69	
	R. Bruno 9/17/69	

DRN. J.BISSONNETTE	DATE 4/3/68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R.BRUNO	DATE 4/5/68	
ENG. J.A.LAMBERT	DATE 4/5/68	TITLE I/O CONNECTORS
ENGR ENG. J.A.LAMBERT	DATE 4/5/68	
ENGR. R.ANTONNUCCIO	DATE 4/7/68	
FIRST USED ON RF08		SIZE D CODE BS NUMBER RF08-0-11 REV. B
SCALE		DIST.
SHEET 1 OF 1		

Figure 2-5 RF08 to PDP-8/PDP-8/I Interconnection Cable Diagram

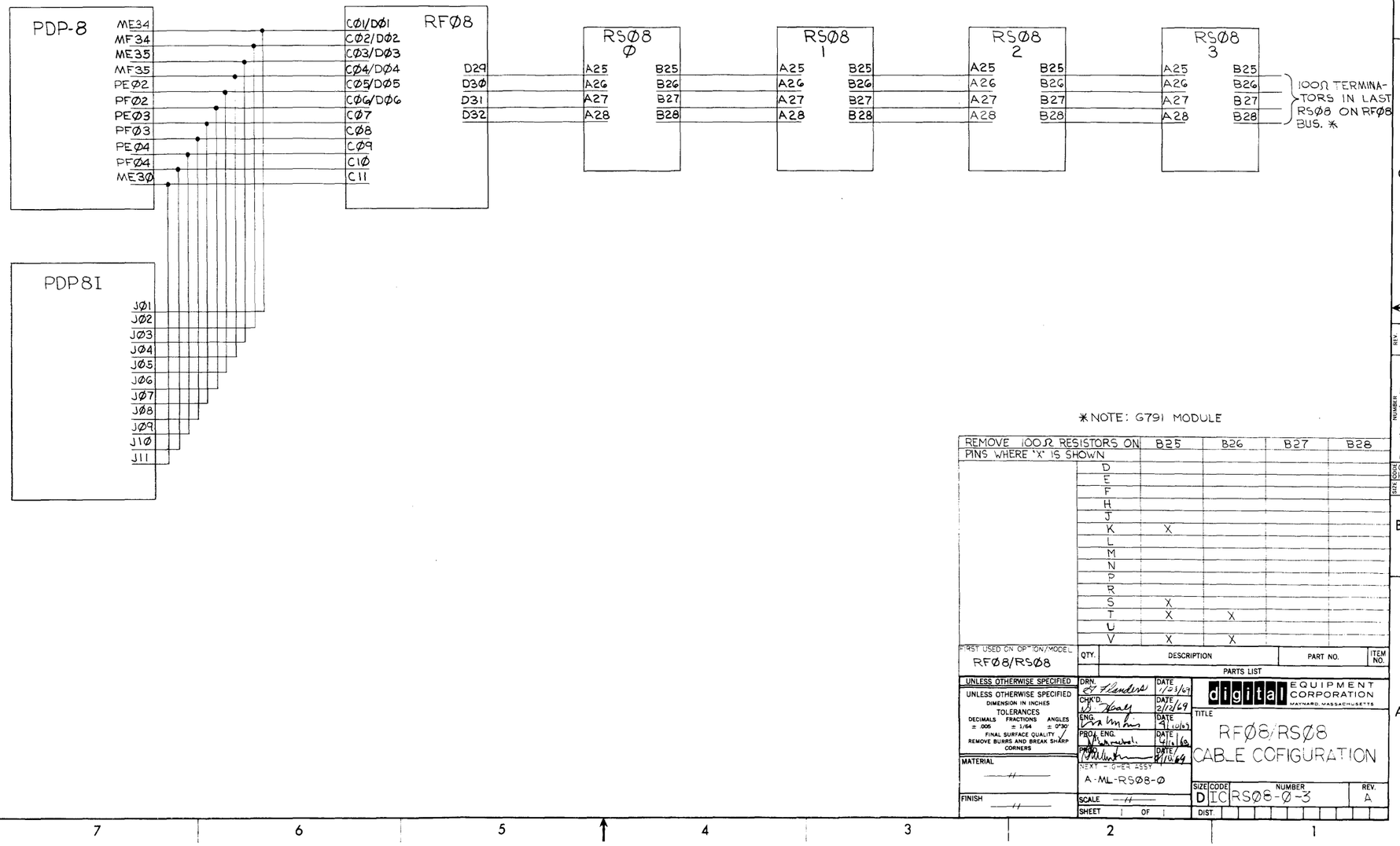


Figure 2-6 RF08 to RS08 Interconnection Cable Diagram

Chapter 3
Principles of Operation

3.1 INTRODUCTION

The description in this chapter refers to the operation of one RS08 Disk. The RF08 Disk Control is provided with control logic for addressing up to four RS08s. The disks are connected in parallel to the data address lines. Each additional disk has a modified decoding card which decodes the addresses supplied by bits 7 and 8 of the Extended Memory Address (EMA). All other functions are identical when extra disks are installed.

3.2 RS08 FUNCTIONAL DESCRIPTION

The RS08 contains a storage disk, read/write data heads, a data write driver, timing track amplifiers, and data recovery electronics. Except for head selection, all data transfers between the RS08 and RF08 are serial binary. Head selection is in parallel binary. Figure 3-1 shows the organization of the RS08; while Figure 3-2 is a circular timing diagram of the address tracks.

NOTE

Appendix B contains a typical RF08/RS08 I/O routine.

3.2.1 Timing Tracks

There are three timing tracks which are written permanently on the disk and detected by three independent read amplifiers. A set of complete spare tracks is also provided. These tracks are written on the disk in exact phase-lock with the primary set of tracks. Thus, data written on the disk can be recovered in the event the primary set of tracks is lost by accidental erasure or component failure. When switching to spare tracks, the timing track amplifiers must first be adjusted before attempting to recover data.

CAUTION

An ohmmeter should never be used to test the timing tracks. Connection of an ohmmeter to the disk heads will erase the prerecorded timing tracks. Extreme care must be used when making oscilloscope measurements near the timing track connector, since even a momentary short to the ground of these pins will erase the timing tracks.

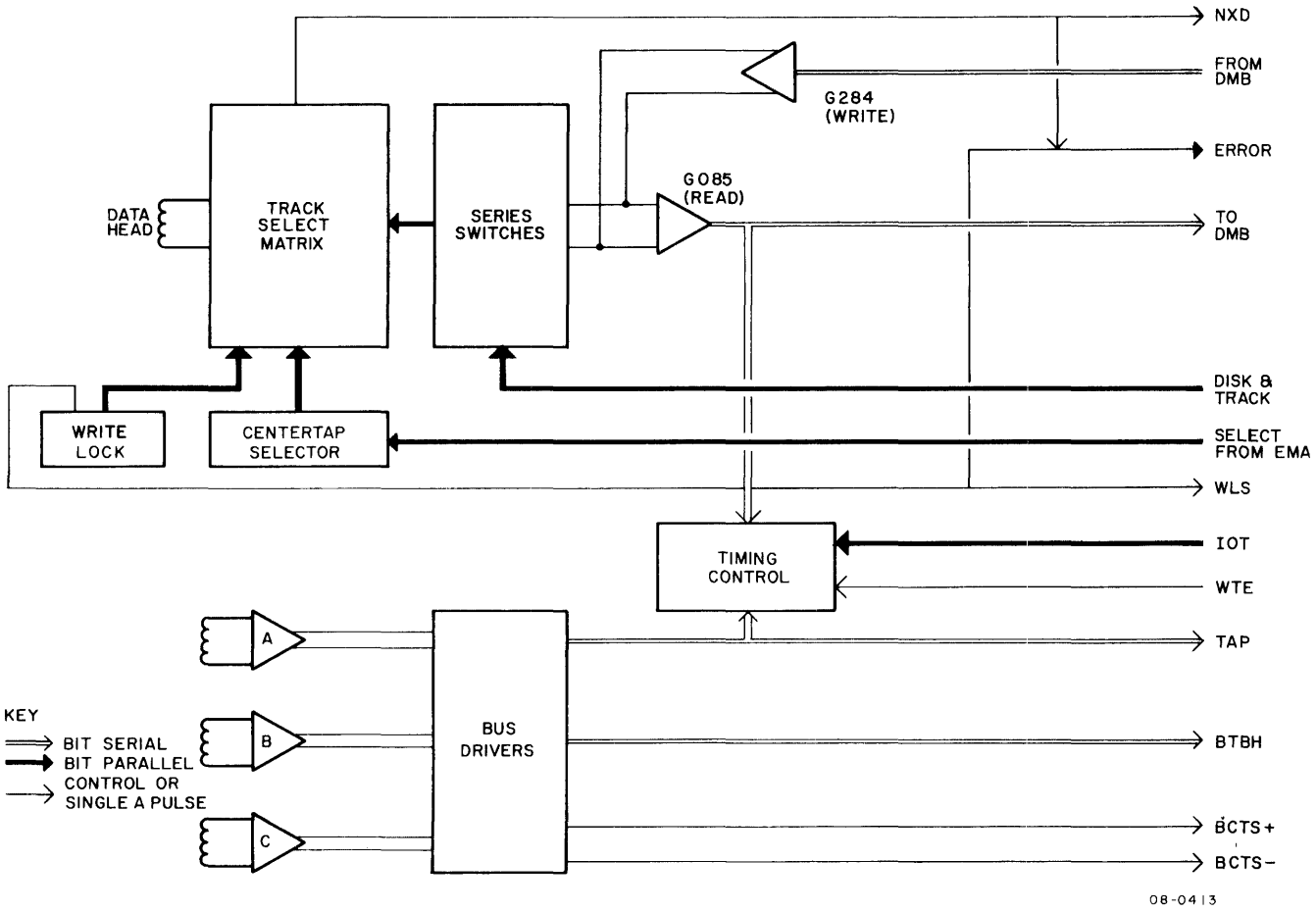
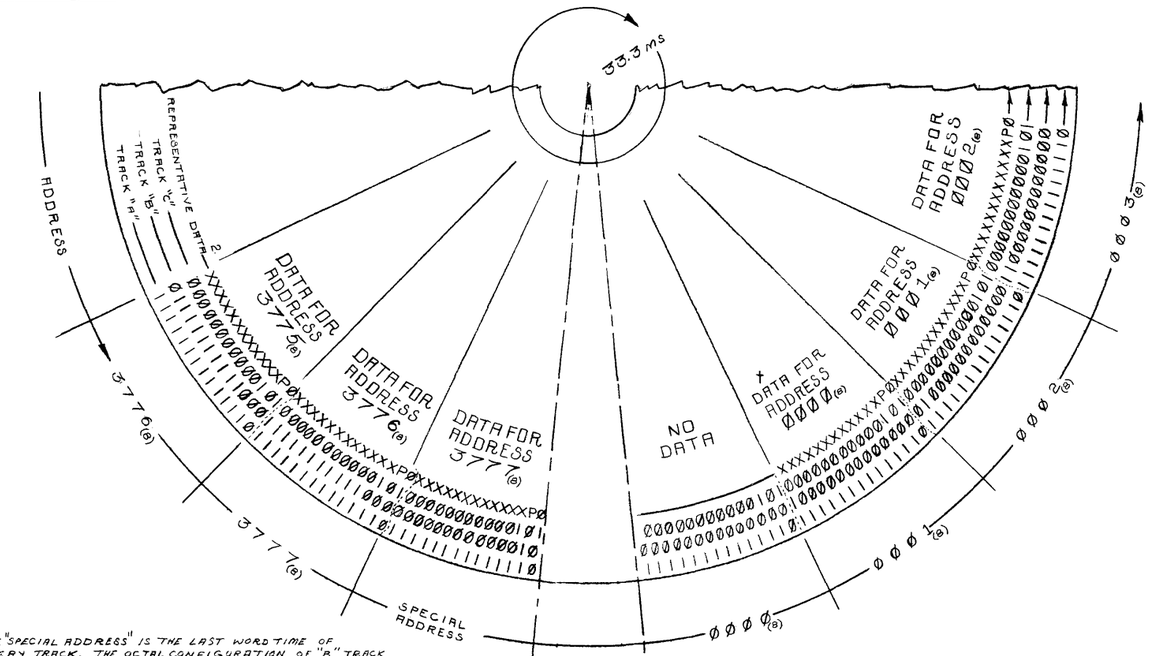


Figure 3-1 RS08 Block Diagram

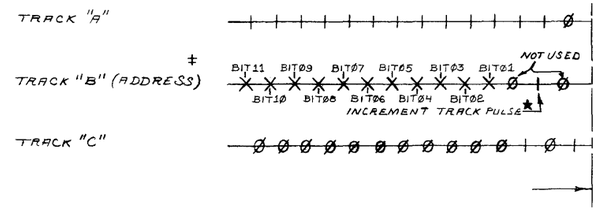
The RS08 has no circuitry for writing new timing tracks; a separate track writer (RS08TA) is used for this purpose. The timing tracks (see Figure 3-2) are identified in Sections 3.2.1.1, 3.2.1.2, and 3.2.1.3.

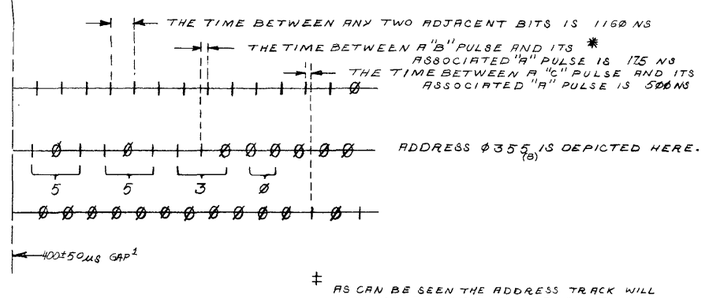
3.2.1.1 Track A, Strobe-Clock Track - This track contains thirteen 1s followed by a single 0 for each angular address. The output of this track is used to strobe all of the serial data and address operations in the RF08 and the RS08. Track A provides the clock rate for the disk: 1160 ns (60 Hz) between bits. The 13th bit provides for an even parity check; while the 14th bit-time provides a gap to permit the user to turn off/on the write amplifier. The 14th bit-time is not provided with a TAP to prevent data transfer between data words.

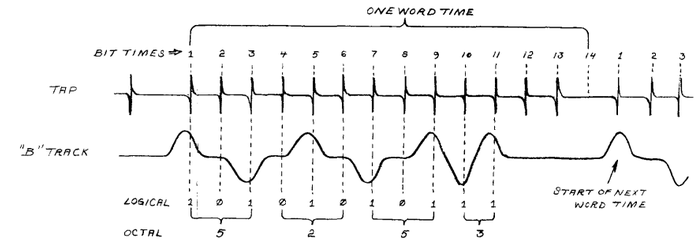
3.2.1.2 Track B, Binary Address Track - Binary addresses are written sequentially around this track. The lowest order bit is read off Track B first, and the highest order bit is read last. This sequence allows the disk memory address logic in the RF08 to increment the DMA register by performing a serial add of plus one as the address is read and compared. The binary address is placed one word before the actual location in which data for that address is written. This placement allows the disk file to locate an angular address and begin data transfer in the next word-time. An extra address, shown as a special address, has $10{,}000_8$ written onto Track B. The special



THE "SPECIAL ADDRESS" IS THE LAST WORD TIME OF EVERY TRACK. THE OCTAL CONFIGURATION OF "B" TRACK CAN BE READ AS 10,000. THE PURPOSE OF SPECIAL ADDRESS IS TO STORE THE DATA FOR THE PREVIOUS ADDRESS (3777) AND TO PRODUCE THE INCREMENT TRACK PULSE.







REVERSED = 3525

Decoding The Address Track

ANALOG AMPLIFIED "B" TRACK IS DISPLAYED ON ONE CHANNEL OF THE OSCILLOSCOPE. TRACK "A" PULSE (TRP) IS DISPLAYED ALTERNATELY ON THE OTHER CHANNEL TO GIVE A TIME RELATIONSHIP. SYNC IS EXTERNAL ON SYNC MARK. THE ADDRESS BEING DISPLAYED IS 3525.

ALL REFERENCES MADE TO 60 HZ

Symbol Code:

- 1 ALWAYS A LOGICAL "ONE"
- 0 ALWAYS A LOGICAL "ZERO" (UNLESS OTHERWISE INDICATED)
- X POSSIBLE "ONE" OR "ZERO"
- P POSSIBLE PARITY BIT. (RS-08 USES EVEN PARITY)

‡ AS CAN BE SEEN THE ADDRESS TRACK WILL COME OFF THE DISK BACKWARDS, TO DECODE AN ADDRESS, DISREGARD THE LAST THREE BIT TIMES AND READ THE REMAINING ELEVEN FROM RIGHT TO LEFT.

✱ TIME IS MEASURED FROM LEADING EDGE TO LEADING EDGE OF THE SLICED ANALOG SIGNALS.

† DATA FOR A PARTICULAR ADDRESS IS WRITTEN INTO THE NEXT SEQUENTIAL ADDRESS.

★ THE INCREMENT TRACK PULSE (OCTAL CONFIGURATION 10,000) OCCURS ONLY DURING SPECIAL ADDRESS.

1. ON THE RS-08, SYNC MARK AND THE GUARD BANDS ARE DERIVED THRU THE TIMING AND DELAY LINES NOT THRU A PHOTOCELL.
2. FOR A REPRESENTATION OF TRACK POSITIONING REFER TO THE TRACK INTERLACEMENT DIAGRAM.

REVISIONS	REV.	CHANGE NO.	CHK

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY 63
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. P. DIGREGORIO	DATE 10-29-68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D Jay Levine	DATE 9-9-69	
ENG. Jay Levine	DATE 9-9-69	TITLE RS Ø8 CIRCULAR TIMING DIAGRAM
PROJ. ENG. M. James	DATE 9-9-69	
PROD. R. Travers	DATE 9-9-69	
FIRST USED ON RS Ø8		
SCALE		SIZE D CODE TD NUMBER RSØ8-Ø-5 REV.
SHEET 1 OF 1		DIST.

DEC FORM NO. 102A

Figure 3-2 Circular Timing Diagram

address is sensed by the RF08 to instruct the disk file to switch to the next higher track. A 550 ± 50 μs head switching gap is provided to allow this switching to occur. The data for address 3777_8 is written during the special address word period; therefore, no data is recorded during address time 0000_8.

3.2.1.3 Track C, Word-End Track - Track C contains binary 1s at bit-times 12 and 14; all other bit-times contain binary 0s. These bits (binary 1s and 0s) indicate the boundaries of a data word. The binary 1 at bit-time 12 appears as BTCS- and the binary 1 at bit-time 14 appears as BTCS+. These signals are separated in the RS08 to allow them to control separate word-end functions in the RF08.

3.2.2 Disk Selection

EMA bits 7 and 8 are used to select one of the four disks that can be installed with the RF08. When only one disk is installed, it is always designated as disk 0.

A select level from the disk select circuit inhibits the reading of the address track and the reading and writing of data, except when a disk has been selected by EMA bits 7 and 8.

When more than one RS08 is installed, the address tracks of the units not selected must be disabled. A logic signal from the disk select circuit enables the recognition of the address tracks for the selected disk only. The enabled signals are then placed on a negative (-3V) OR bus between the RS08 and the RF08.

3.2.3 Track Selection

Extended memory bits 0 through 6 select the disk head using an X-Y diode matrix selector scheme. Identical paths are used for reading and writing of data on the disk.

The selection of the X diode matrix uses EMA bits 0, 1, 2 and 6 to select 1 of 16 data lines which connect to the G286 Center-Tap Selector Modules. A selected center-tap is connected to the +20 Vdc power supply through a saturated transistor; while the unselected center-taps are connected to the -15 Vdc power supply through a resistor.

The G285 Series Switch Module is used to select one of eight Y line pairs. The selected series switch enables a pair of transistors to pass the differential read or write signals. Only at the coincidence of a selected Y line pair and X center-tap are the head diodes biased into conduction. Therefore, only 1 of the 128 tracks can be read from or written on at a time. The outputs of the eight series switches are bused to permit the use of a single read and a single write amplifier.

3.2.4 Write Lock Out

Any of the eight Y lines can be locked out from writing when bit 6 of the EMA address is 0, thus, allowing the addresses for the lower half of the disk (addresses 0 to 377777_8) to be locked out in blocks of 40000_8 words. The lockout circuits are controlled by toggle switches on the RS08 unit. When EMA bit 6 is a 1, the lockout circuits are inhibited. If a locked-out track is selected by the program, a logic level is sent to the RF08 to enable setting of the appropriate flags.

3.2.5 Writing Data

The data head selected by the EMA to write data is described in Section 3.2.3. The output from the write amplifier is connected to the same point as the input to the read amplifier, permitting use of the same signal paths for reading or writing.

A "phantom center-tap" (see Figure 3-3) is used to select the direction of the write current through the head. The value of resistors R1 and R2 is large compared to the resistance of the selected head. When point A is connected to +20 Vdc through a center-tap selector, the head is enabled for writing. Writing is accomplished by connecting point B or C (one at a time) to -15 Vdc through the write amplifier. When reading, current of approximately 5 mA with good balance, flows from points B and C.

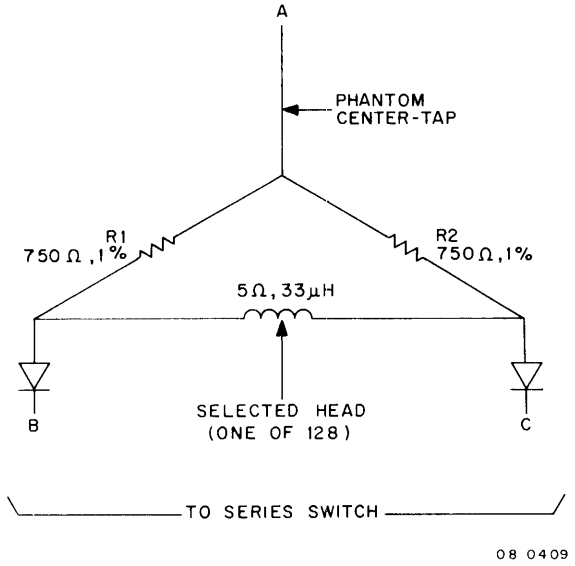


Figure 3-3 Selected Write Head Simplified Diagram

The resistance of the head is low (5 ohms); thus, equal current flows in R1 and R2 under steady state conditions. For example, if point B is connected to -15 Vdc (with point C floating) approximately 45 mA flows through the head windings. When point C is at -15 Vdc (point B is floating) approximately 45 mA flows in the opposite direction.

Saturation magnetic recording is used; thus, either polarity current is flowing when writing. Previously recorded data are always erased during writing.

The NRZI recording technique is used in the RS08 Disk. A binary 1 is represented by a change in the direction of the magnetic flux along the disk track, and a binary 0 is represented by no change in magnetic flux. A binary 1 is written by reversing the direction of write current in the head.

The Write Flip-Flop (WFF) is used in the RS08 Disk to determine the polarity of the write current. Since a change in magnetic flux represents a binary 1, the WFF circuit is toggled to write a 1 (see Figure 3-4).

3.2.6 Reading Data

When data on a track is to be read, the write drivers are disabled by a logic signal from the RF08. Figure 3-5 represents the output signals from the selected head. Head selection for the read mode is identical to the write mode; however, the output signals, which appear on the Y select lines, are supplied to an amplifier and amplitude detection circuit. Because the magnetic head can respond only to a change in magnetic flux, an output appears only when a binary 1 is written. The output voltage from the selected head is proportional to the time derivative of the magnetic flux in the head. Because of the recording surface and head parameters, the output approximates the shape of a cosine squared (bell) pulse. A binary 0 is indicated for no output signal because the magnetic flux on the disk is not altered when writing a binary 0.

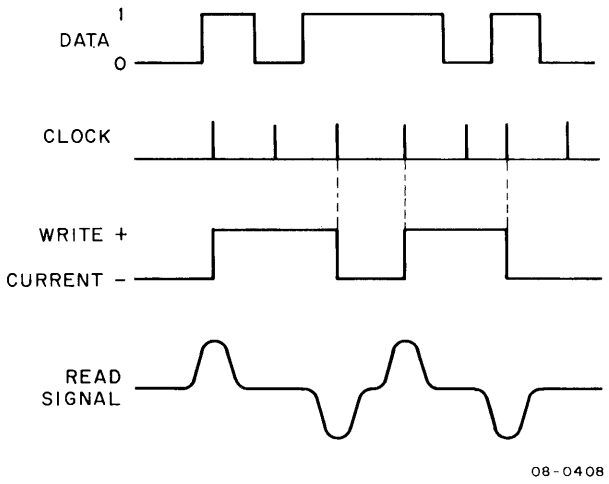


Figure 3-4 Writing Current Pulse Diagram

3.2.7 RS08 Logical Functions

In addition to converting digital write signals into current in the appropriate head and analog-to-digital conversion of data and timing track read signals, the RS08 performs logical functions on the recovered data. These logical functions are described in the following subparagraphs.

3.2.7.1 Timing Signals - The G085 Read Amplifier (see Figure 6-38) amplifies the head signals and converts them into digital form through use of a threshold detector. Separate positive and negative threshold outputs are available. For Track A (bit-strobe track) only timing information is useful; therefore, the G085 outputs are ORed for use in the RS08 and RF08. For Track B (address track) the address track data is inverted to an NRZ data output for transmission to the RF08 by the Track B Hold (TBH) flip-flop. The negative and positive outputs from Track C (word-end track) are used for separate logical functions in the RF08. Thus, the TC BTCS- and TC BTCS+ signals are transmitted directly to the RF08.

3.2.7.2 Origin Gap Pulse (PCA) - The origin gap pulse indicates that the selected disk is at its original (between address 3777_8 and 0000_8) position. As the disk revolves, Track A is continuously retriggering an R303 integrating one-shot set to 50 μs. However, 50 μs after the end of the Track A pulses, the triggering one-shot recovers and triggers the R302 one-shot which produces the 100 μs flag, thus indicating the completion of a disk revolution.

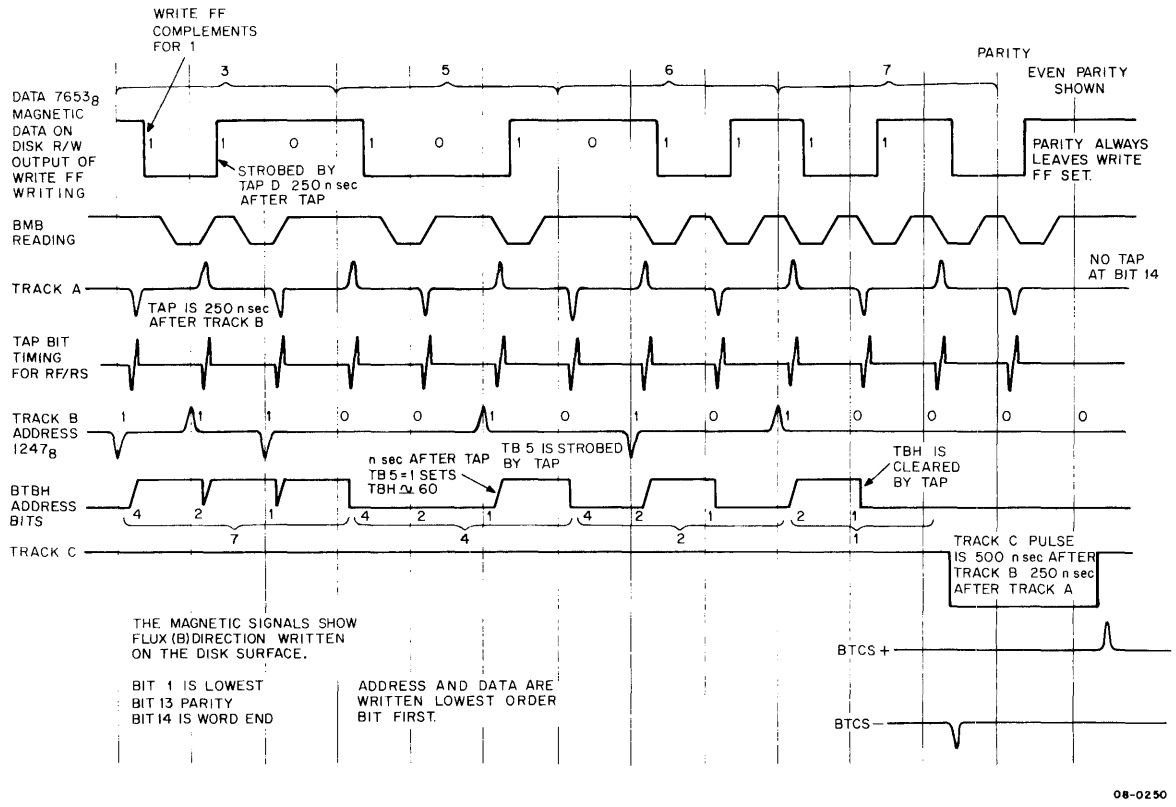


Figure 3-5 Disk Address and Data Track Timing Diagram

3.2.7.3 Data vs Timing Skew Circuits - Due to differences in electromagnetic parameters and dynamic runout of the disk surface, timing skew between data and timing signals is possible. Three B301 one-shots are used to permit skew of up to ±50% of the bit cell. The data and timing pulses are converted to standardized pulse widths by two of the one-shots. A third one-shot changes the position of the timing window (DC WIND); consequently, the standard pulses (DC DATA and DC WIND) overlap.

The DC WIND pulse is adjusted to permit the earliest and latest DC DATA pulses to overlap by the same amount. The pulses are ANDed to set the MBI register and also to indicate a data 1 has been read (see Figure 6-40). MBI is transmitted to the RF08 as the serial read data.

The Track A timing pulses clear MBI at the end of each data cell. If MBI clears, PAR is toggled to permit the parity of the data word to be computed. PAR is cleared for each word (see Figure 6-40).

Because data is written in even parity, PAR must be cleared at the end of each word if no error has occurred.

3.2.7.4 RF08/RS08 Bus - The bus is terminated in the RF08 and the last RS08. High-speed signals have 100Ω terminations at each end of the cables; consequently, signals are propagated without reflections. Slow signals, such as track select lines, are terminated through a resistor (to +10V) in the RF08 and 100Ω (to ground) in the last RS08.

With a positive to -3V swing, acceptable noise margins are maintained on the track select signals.

3.3 RF08 FUNCTIONAL DESCRIPTION

A general discussion of the RF08 circuits is followed by a detailed discussion of the functions of the RF08 (see Figure 3-6).

3.3.1 Address Registers

The RF08 has two address registers which contain separate program instructions. The DMA register contains the lowest order 11 bits of the address which corresponds to the addresses (0000_8 to 3777_8) recorded on the RF08 track. The address loaded into the DMA is compared by a bit comparator in the address control section of the RF08. The comparison is accomplished by shifting the address through the DMA and comparing the lowest order bit in the DMA with the bits of the address being read off the disk. The timing control provides timing signals for this function. When the angular address is located, a signal is sent to the data control to allow information transfer. During information transfer, the address in the DMA is incremented by 1 following each data-word transfer. At the end of data transfer, the DMA contains the address of the last data word transferred; this address can be read by the PDP-8.

The EMA is loaded by a separate command from the PDP-8, except for the lowest order bit, which is loaded with the highest order bit of the DMA address. Because the 20-bit address capability of the disk file system must be loaded from the 12-bit PDP-8 accumulator, two address transfers are required. Bits 7 and 8 of the EMA select one of four disks that can be controlled by the RF08, and bits 0 through 6 select the head in that disk (track number) that is to be used for data transfer.

The EMA register is a 9-bit binary ripple counter, which can be cleared and loaded with a parallel jam transfer.

3.3.2 Memory Buffer Registers

There are two memory buffer registers in the RF08: MBH and DMB. During the write mode, the MBH is parallel loaded with data from the PDP-8 Memory Buffer. The contents of the MBH are then transferred in parallel to the DMB. During the read mode, the MBH is loaded with data transferred in parallel from the DMB. The contents of MBH are then transferred in parallel to the PDP-8. Because the DMB register is continuously performing serial-to-parallel read or parallel-to-serial write conversions, two registers are required for each data word. Since only the bit-time (1160 ns) between words is available to load the DMB with data from the PDP-8, the MBH is required to buffer that data.

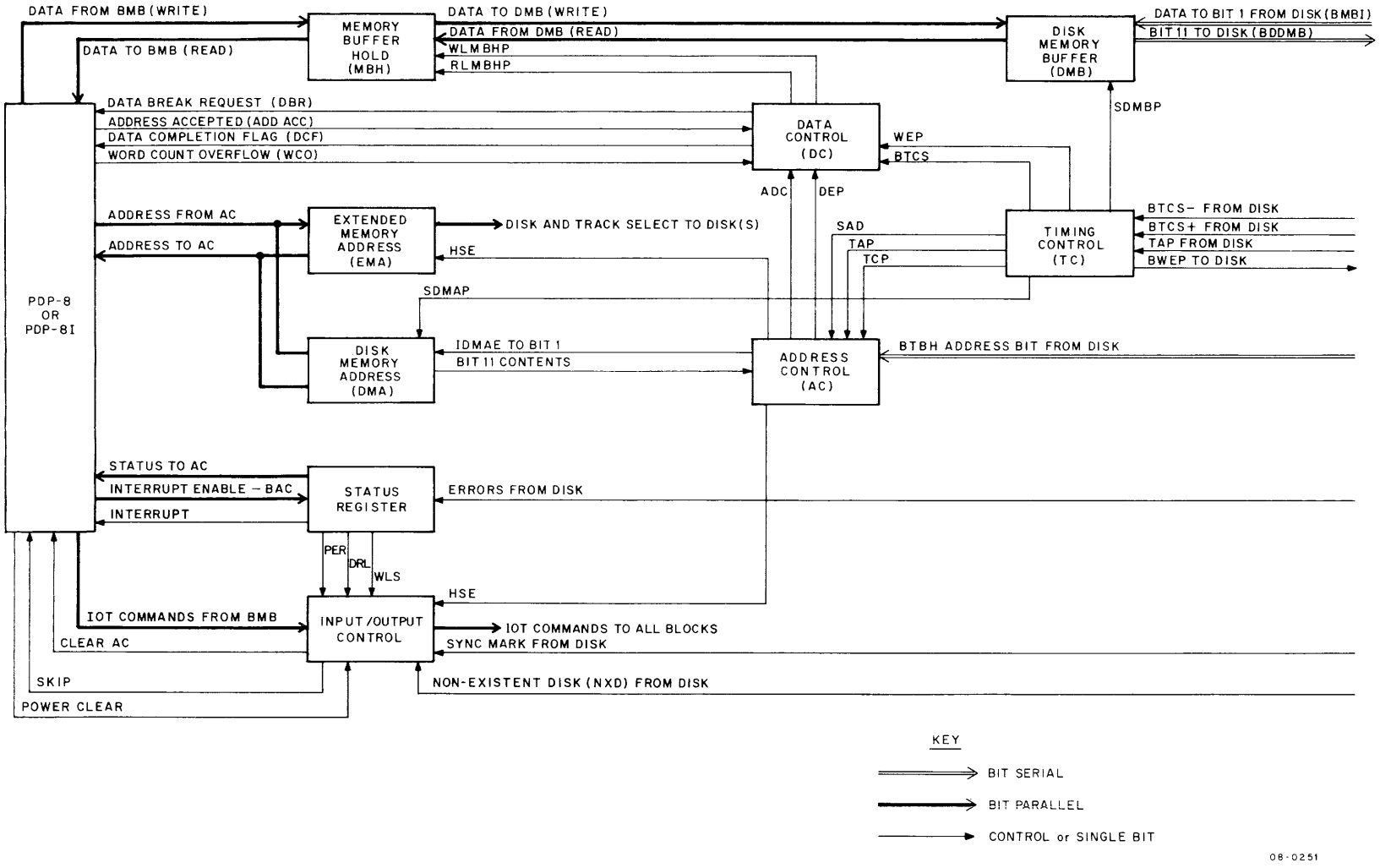


Figure 3-6 RF08 Disk Control Block Diagram

When a word transfer is complete, the next data word is parallel transferred into the DMB from the MBH when writing, or out of the DMB to the MBH when reading.

When writing, the data in the lowest order bit (DMB 11) is written on the disk. After the bit is written, the data are shifted down one bit, and the new bit in DMB 11 is written. After 12 shifts, the data have been shifted completely through the DMB, a clear signal clears the DMB flip-flops, and another parallel transfer of data from the MBH occurs.

When reading, the bit read from the disk is loaded into DMB 0. This bit is then shifted down one bit and another bit is loaded into DMB 0. The lowest order bit is written onto the disk first, causing the first bit read to be in DMB 11 after all 12 bits are read. Data are then transferred in parallel to the MBH. A double rail jam transfer is used to transfer data from DMB to MBH when in the read mode. Signals from the data control determine the direction of transfer and also the timing at BTCS+.

3.3.3 Address Control

The address control compares the address read from the disk address track with the address loaded into the DMA. When the address in the DMA has been located, the address control generates an ADC logic level which allows data transfer to begin. After each word of data is written, the address control generates a DEP; the DEP is used by the data control as an end-of-word strobe signal. The address control increments by 1 the address in the DMA, using a serial add during each word following a DEP. Therefore, the DMA is incremented by the number of data words transferred.

The address control also provides an HSE signal which increments the contents of the EMA after the last address (3777_8) is read from the address track of the disk. This allows data transfer to continue, using the next head on the disk (or the next disk when the last address on a disk has been reached). The address in the DMA is reset to 0000_8 after data has been transferred to or from the last angular address on the track.

The origin gap in the timing tracks is long enough to permit "spiral" read and write operations. While reading, the amplifier recovers from the track switching overload during the origin gap.

In multiple disk installations, the rotational positions of the disks are not synchronized and a normal rotational positioning latency occurs when spiralling between disks. The overflow from the most significant EMA bit (AC bit 4) resets the synchronizing logic for automatic disk switching. A normal address search is initiated and the transfer continues after the ADC flip-flop is set.

3.3.4 Data Control

The data control is instructed, by decoded IOT instructions, to control either the writing or reading of data. When address control supplies an ADC signal, indicating that the angular address has been located, the data control is enabled to control data transfer between the disk and memory buffers as described in Section 3.3.2. Data transfers, within the RF08, occur at the end of a data word. Data transfers received from the address control are strobed by the DEP flip-flop. In the write mode, the MBH register is loaded, and the data control is strobed by the T1 timing signal from the PDP-8.

The PDP-8 supplies a WCO pulse during the last programmed transfer. The WCO pulse ends data transfer and sets the DCF flip-flop.

3.3.5 Timing Control

The timing pulses from disk Tracks A and C are converted to clock signals in the RF08. The Track A pulse is a strobe for address search and data transfer and occurs in the first 13 of the 14 bit-times. Track C pulses signify the end of a data word and are transmitted on two separate lines.

The TAP is used to shift the address through the DMA register. A delay is provided that prevents shifting the DMA contents until the contents of bit 11 are set-up by the address control. The next 11 TAP pulses are used to generate SDMAP. After the end of the 11th shift, the circuit is reset by the Track C pulse (BTCS-), which occurs at bit-time 12. Resetting the circuit delays generation of the SDMAP for the first and last A pulse in a data word.

When the address confirmed signal is received from the address control, the TAP pulses are used to produce the SDMBP. These pulses are produced as long as data are transferred to or from the disk. There are 13 SDMAP pulses developed for each data word; however, the 13th pulse has no affect on data loaded into the DMB, because of the information transfer timing between the MBH and DMB.

Two separate Track C pulses are provided by the disk: the first, BTCS- occurs at bit-time 12 and is used to establish a WDE signal. This signal appears as a pulse and is used to present data transfer for the last two bit-times. The second pulse, BTCS+, occurs at bit-time 14, and in addition to ending the WDE hold-off period, develops the TCP and WEP. This pulse is used by other sections of the RF08 and by the RS08 to signify the end of a data word.

3.3.6 Input/Output Control

The RF08 is controlled by IOT instructions received from the PDP-8. These instructions are decoded by the W103 Device Selection Modules in the input/output control. The octal device codes assigned to the RF08 Disk Control

are 60_8, 61_8, 62_8, and 64_8. The IOP lines are used to specify the operations. Note that microprogramming of IOP lines is used for IOTs such as read (DMAR:6603) and write (DMAW:6605).

The decoded IOT instructions are gated with conditions in the RF08 and BMB lines to provide control pulses.

3.4 RF08 LOGIC DESCRIPTION

3.4.1 Address Selection

Address selection is divided between track selection and angular addressing (see Figure 3-7). The angular address is located by the DMA and the address control circuits. Track selection is performed by the EMA over a 7-bit bus to the RS08. Bits 7 and 8 of the EMA select the disk in multiple-disk installations.

3.4.1.1 Locating a Track Address - Three timing tracks are permanently recorded on the disk (refer to Section 3.2.1). An 11-bit starting address is loaded from the PDP-8 address control into the DMA by the DMAR or DMAW command at IOP time 2 or 4. When a DRE signal is generated by the input/output control, the address control begins to compare the bits in the DMA with the bits read off Track B on the disk. Figure 3-8 is a flow diagram of address comparison for track addresses (address 0000_8 to 3777_8). The special case where address 3777_8 is followed by a "special address" causes a head switch (see Figure 3-9). Figure 3-8 shows the sequence of events that follows:

a. A DMAR (6603) or DMAW (6605) is placed in the MB of the PDP-8. Either signal generates IOT 602 or IOT 604 in the RF08. Either IOT generates a LDMAP, which loads the contents of AC bits 1 through 11 into DMA bits 1 through 11. Note that the content of AC bit 0 is loaded into the EMA bit 0 at the same time; however, the EMA is not involved with track address selection.

b. The DRE flip-flop is set by either of two signals. If the disk is passing through the head switching gap, the LDMAP sets DRE. If the disk is positioned on an address, MRS is set by LDMAP. The 4-bit time counter (TCA, TCB, TCC, TCD) receives WEP (derived from BTCS+) to count to 16_{10} and reset to 0000_8 (setting the DRE). The waiting time is provided as a settling time for DMA logic. Once set, DRE remains set until all the data words have been transferred, or until the last word on the disk has been used.

c. When DRE is set at the end of a word, an enabling level is provided to allow the next TAP to set the SAD flip-flop. SAD is set by the first TAP pulse, and address search begins at the beginning of an address word.

d. The first address bits appear at the address control as BTBH and TBH. The contents of DMA 11 are ANDed with the state of the ACH. ACH is set, resulting in the generation of true IDMAE and IDMAE-, which represents the contents of DMA bit 11. The IDMAE levels and TBH levels are connected to an exclusive OR gate. If the exclusive OR is true, indicating that BTBH and DMA 11 contain complements, ABC is set, indicating that the bits do not compare. ABC was cleared by WEPD before address comparison began and remains clear if the exclusive OR is not true.

e. For the first bit comparison, TCP is not true because it is generated at bit-time 14 by BTCS+. The ACH flip-flop has been previously set. The second TAP pulse is ANDed with SAD (which is not set) to generate the SDMAP. The contents of the DMA are shifted one bit to the right. At the same time, the state of IDMAE is placed in DMA bit 1. This places the contents of DMA bit 11 into DMA bit 1; the result being rotation of the address in the DMA.

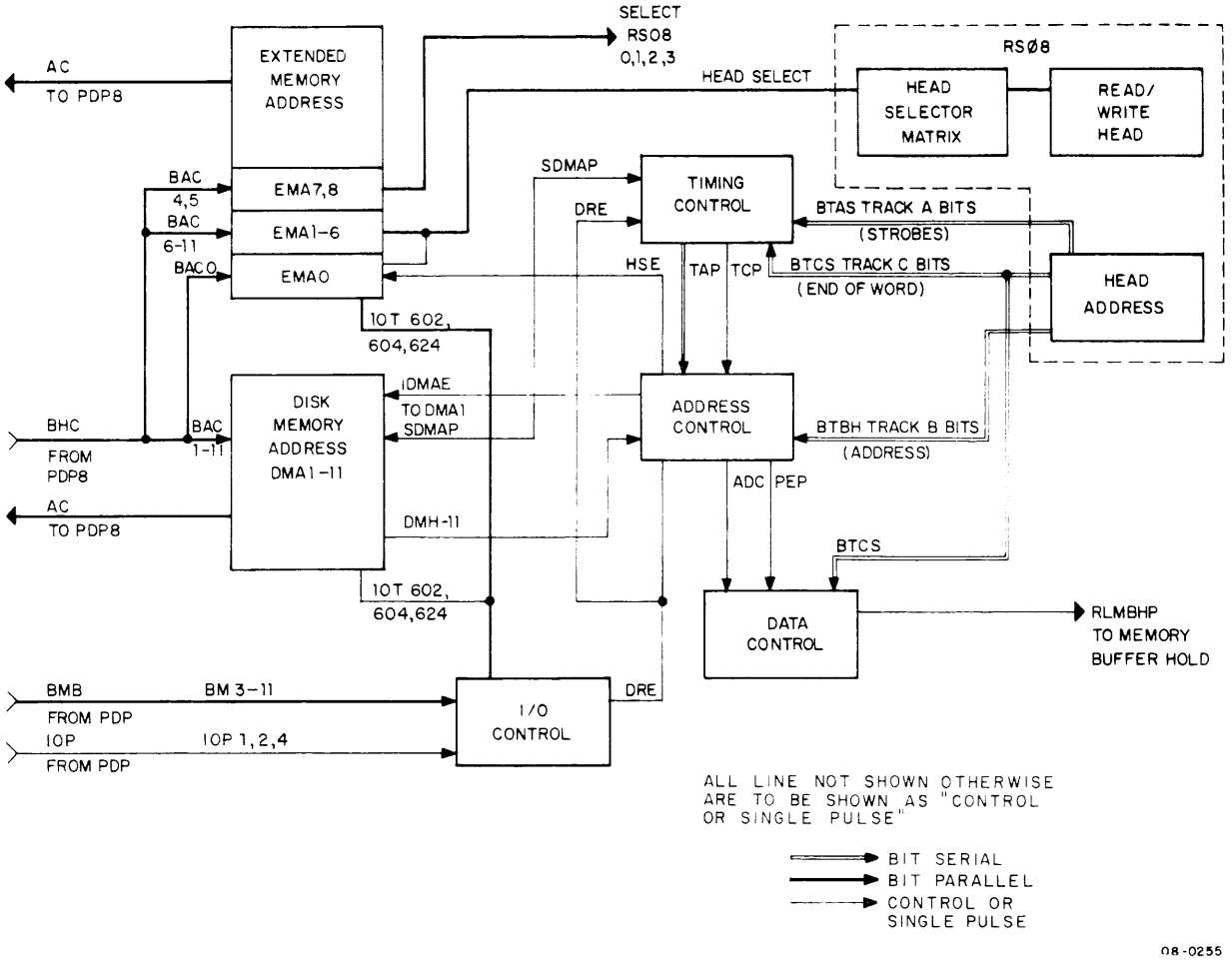


Figure 3-7 Address Selection Simplified Block Diagram

f. The new content of DMA bit 11 generates a new IDMAE, and the process returns to point 1 on the flow chart.

g. The last address bit occurs at bit-time 12. This address bit is followed by BTCS-, which resets SAD and causes a branch at point 2 on the flow chart. WDE is set, resetting SAD and inhibiting the generation of SDMAP until the first TAP pulse appears after SAD is reset (at the beginning of the next word). The first and thirteenth TAP pulses are prevented from generating SDMAP pulses.

h. ADC is cleared when the DRE has been cleared. DRE is now set, allowing the state of the ABC flip-flop to be strobed by the 13th TAP pulse. If ABC is set, the address has not been located, since at least one bit of the DMA was the complement of the associated BTBH bit. In this case, the first bit of the next address word is compared with the contents of DMA 11, and SAD is set by the first TAP pulse of the next address word. Another comparison of 11 bits takes place, and the process branches again, checking to see if ABC was set.

i. When the track address (corresponding to the address in the DMA) is read, the ABC is clear at bit-time 13. The 13th TAP pulse strobes a set command into the ADC. This enables a data transfer to begin, starting with the next word. The process continues to point 1 on the flow chart and continues shifting the contents of the DMA through one address word, until BTCS- is true again. The ADC is set on the last word; the Track C pulse derived from BTCS+ at bit-time 14 to strobe the generation of a Data End Pulse (DEP) is then enabled.

j. DEP resets ACH and the process returns to point 1 of the flow chart. When point 3 is reached, IDMAE is the complement of DMA bit 11. When SDMAP rotates the contents of the DMA, the complement of DMA 11 is placed in DMA 1. The process returns to point 1 of the flow chart after each DMA 11 (1) is placed in DMA 1 as a binary 0. When the content of DMA 11 is binary 0, ACH is set by SDMAP. Because of the propagation delay, a binary 1 is written into DMA 1. The process returns to point 1, and the remaining SDMAP shifts place the contents of DMA 11 into DMA 1. Because the address is read off with the lowest order bit first, the effect is to add one count to the DMA.

k. After the last data word is transferred, DRE is cleared by DCF. This clears ADC and also inhibits setting SAD. ABC is reset, and ACH remains set. The address control is now ready for a new address comparison when IOT 602 or 604 is generated. At the end of the data transfer, the DMA register contains either the last address used (for a read operation) or the last address used plus one (for a write operation).

3.4.1.2 Operation of the EMA - The EMA register is used to hold the two bits used to select a disk and the high-order six bits of the track select. The least significant track select bit is bit 0 of the DMA. Note that the indicator panel shows the EMA and DMA differently than they are actually implemented in the hardware.

Referring to Figure 4-2, note that the boundaries of the hardware registers are different than the PDP-8 word boundaries, also the EMA flip-flop is named according to the binary weight. For example, EMA 9 on the indicator panel is bit 2^3 in the EMA register and is named EMA 3 (see Figure 6-34). Numbering the DMA flip-flop is consistent with the PDP-8 scheme.

The EMA operates as a binary counter and is incremented once each time a head switch enable occurs. The output of the EMA is parallel binary to the disks.

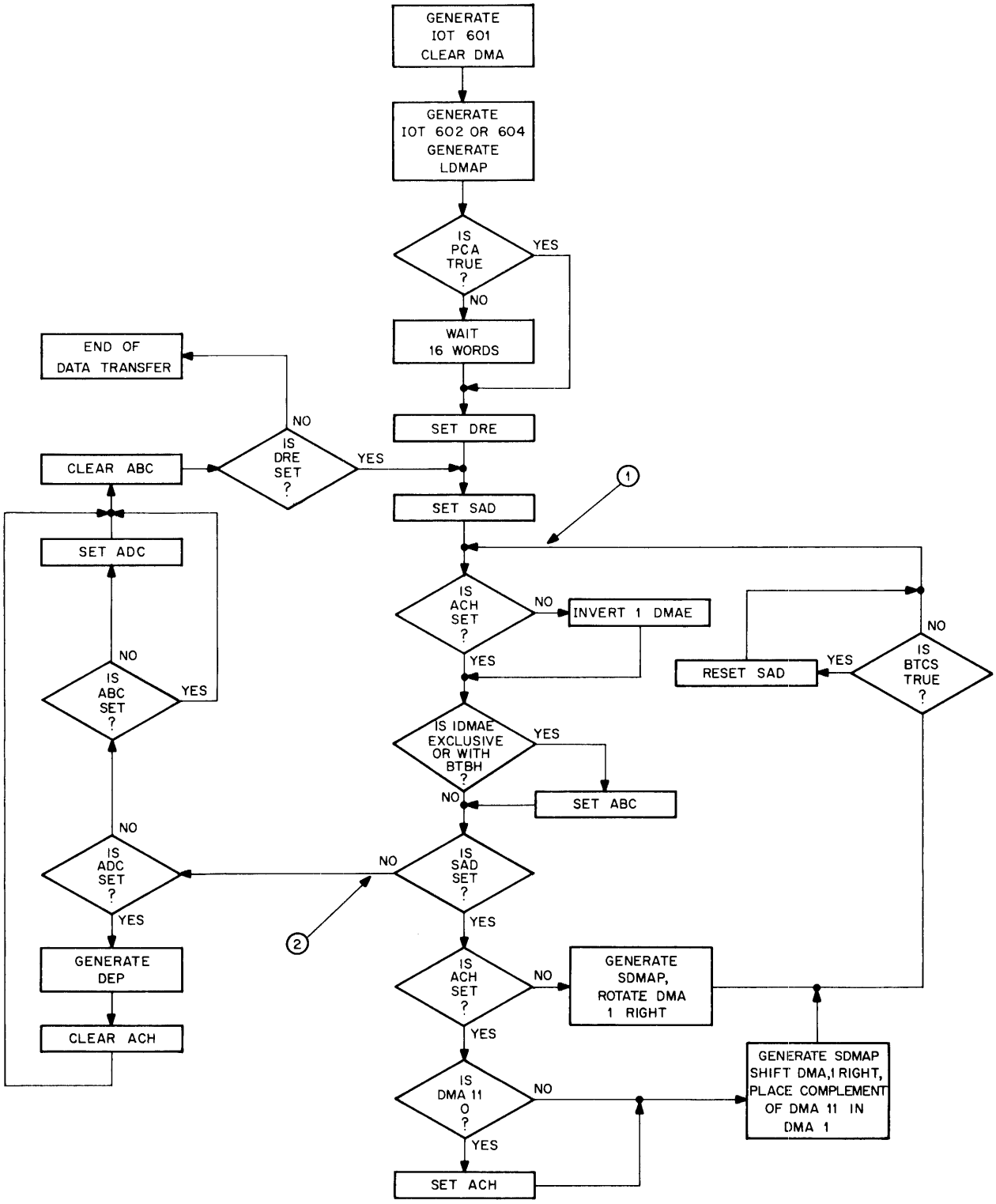


Figure 3-8 Address Flow Diagram

3.4.1.3 Head Switch Enable (HSE) - The last address on a data track is address 3777_8. One more timing address is provided, called a special address. Figure 3-2 shows the format of this special address recorded on the disk. The location of the special address corresponds to the location of data for address 3777_8, because a data word is written during the word time following the associated address. Head-switch operation differs from angular address operation, in that it increments the EMA by one count. A head-switching gap is provided immediately after incrementing to allow 550 μs for the electronic logic to respond to the new head address. The DMA is complemented to 0000_8 by addign one count to the last angular address (3777_8); therefore, no provision is made for resetting the DMA to 0. Note that the two highest order bits (bits 26 and 27) of the EMA determine which of the four possible disks is to be addressed. If the current disk is filled, the head-switching logic switches to the next higher disk. EMA bit 6 is complemented from binary 1 to binary 0 to signify this switch. Reentry into the data transfer loop is slightly different when a new disk is addressed. These differences are described in Section 3.4.1.4. Figure 3-2 shows the logic flow for the track switching sequence described below.

a. At the beginning of address word 3777_8, the DMA register contains 3776_8. Note that the contents of the DMA register follow the disk address location by 1 count, and the DMA is incremented by adding 1 to its contents, not by referring to the address read from the disk. During address 3777_8, the 11 SDMAP pulses are generated, adding 1 count to the contents of the DMA.

b. At the end of address word 3777_8, the DEP clears the ACH flip-flop. The contents of the DMA are binary 1s, except for DMA 11, which is binary 0. During the next address (special address), another 1 is added to the DMA, leaving all 1s in the DMA at the end of this address. Data for address 3777_8 are written during the special address time, and a DEP is generated at the end of special address, which clears the ACH flip-flop.

c. At the end of the special address, the ACH flip-flop is clear, inverting the contents of DMA 11. The DMA thus contains all binary 1s. The ABC flip-flop is set, because the contents of the DMA did not compare with the track address. (This condition holds true for every address following the address which compares and sets the ADC flip-flop.)

d. At the end of the special address, BTCS- goes true at bit-time 12, setting WDE. The address track at the special address contains address $10,000_8$ (all binary 0s, except at bit-time 13, which contains a binary 1). Binary 1 causes BTBH to go true at bit-time 13. BTBH is ANDed with WDE to generate the TEP. WDE is reset by BTCS+ at bit-time 14 in the normal manner.

e. The TEP pulse is used as a set pulse at the HSE flip-flop. This pulse is gated by a level at the flip-flop. For the level to be true, ADC and WCO must be set, indicating that a data transfer has occurred, and that words remain to be transferred. If these conditions are met, HSE is set. The output of HSE (1) generates an enabling level to reset ADC. However, ADC is not reset until the DEP pulse is generated at bit-time 14. Clearing ADC prevents data transfer. When ADC is reset, a pulse is sent to reset HSE.

f. EMA 0 is complemented by a set HSE. Complementing EMA 0 adds a 1 to the contents of the EMA register. Bits 0 through 6 of the EMA select the head used to read or write on the disk; adding 1 to the EMA instructs the disk to move to the next track. For a head switch on the same disk, EMA bit 7 and 8 are not changed.

g. Following the special address is a head-switching gap of approximately 550 μs. The gap is provided to allow the head-selection matrix in the RS08 to settle before attempting data transfer. A switching-gap gate (PCA) is generated in the RS08 and used in the disk switching function only.

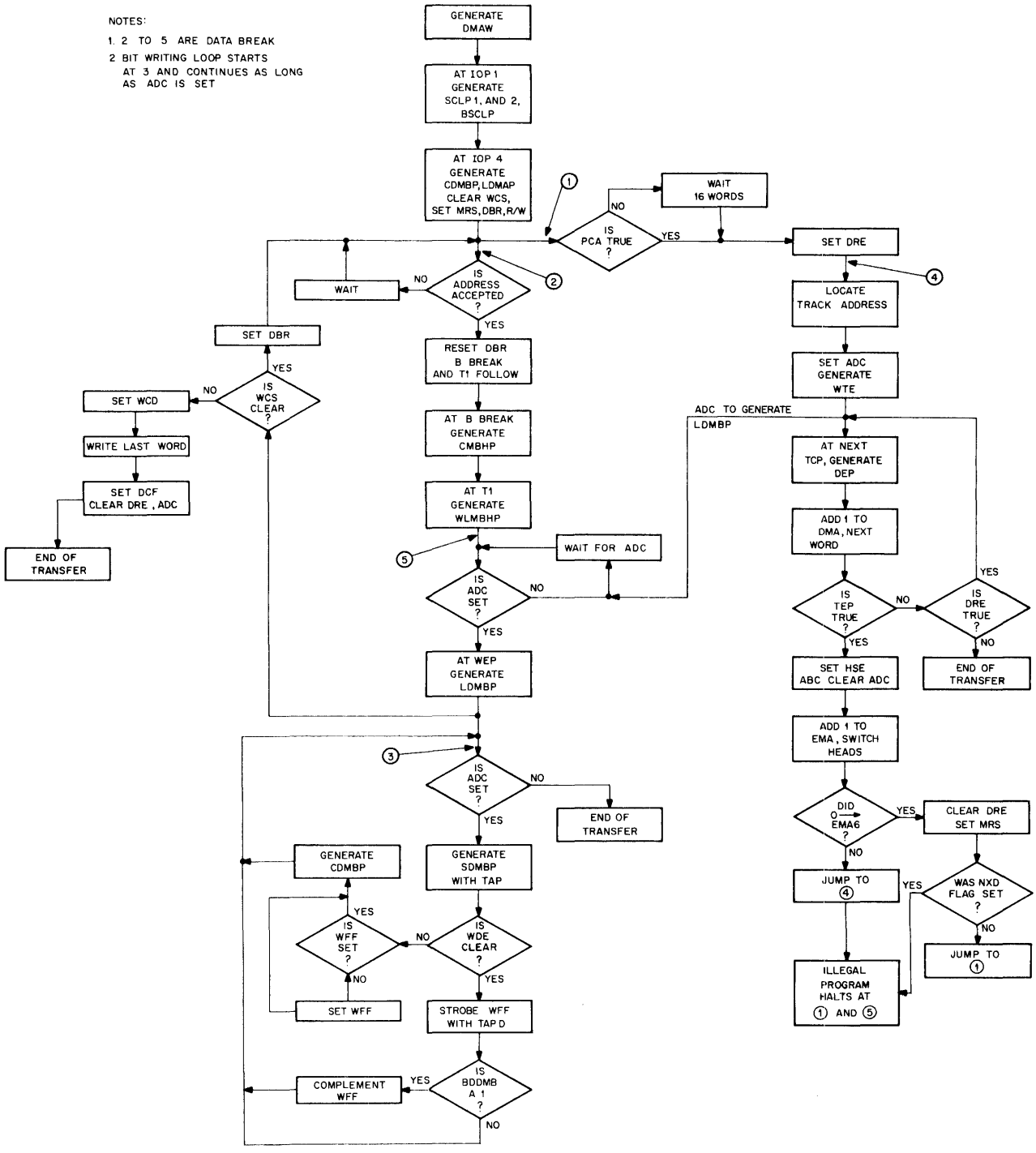


Figure 3-9 Write Flow Diagram

h. At the end of the switching gap, address 0000_8, with its associated TAP pulses and BTCS pulses, is read. To continue data transfer, this address must be confirmed, and ADC set. The contents of the DMA are 3777_8 (all binary 1s), and the ACH flip-flop is clear. The ACH and DMA 11 are exclusively ORed to form IDMAE- which effectively inverts all 1s in the DMA to 0s. Each BTBH (0) is compared with the IDMAE- signal which appears at the exclusive OR gate as 0s. DMA 11 will always be a binary 1 as the address is shifted through the DMA, and the ACH flip-flop will not be set by the SDMAP pulses, because a 0 must be present in DMA 11 at SDMAP time to set ACH. Each SDMAP pulse shifts a binary 0 into DMA bit 1; at the end of the address (word 0), the DMA contains 0000_8.

i. At the end of the address 0 word, the ABC is cleared. The TCP pulse strobes the contents of the ABC and sets ADC. However, the ACH flip-flop is still reset at the end of the address 0 word, because no DMA 11 (0) was seen. Setting the ADC also provides a pulse to set the ACH. This prevents adding 1 to the DMA during address word 1.

j. Data for address 0000_8 is written during address word 1. A DEP is generated, clearing the ACH flip-flop, and the DMA has 1 count added to it during address word 2.

k. Note that the TEP pulse sets the ABC flip-flop. This ensures that ABC does not compare the binary 0s in the special address and set ADC. This erroneous setting of the ADC cannot occur during the head-switch function; however, it could occur at the beginning of a read or write instruction. If the DMA is loaded with 0000_8 by the DMAW or DMAR instruction, and the address search starts after address 0000_8 has passed the address heads, the special address leaves the ABC flip-flop clear. Therefore, TEP is used to set ABC at special address and to prevent setting ADC.

3.4.1.4 HSE With a Full Disk - The last angular address on the last track of a disk is represented by binary 1s in bits 0 through 6 of the EMA. In this case, generation of the HSE (1) (refer to subparagraph d, Section 3.6.1.3) causes bits 0 through 6 of the EMA to go to 0 and complement bit 7. EMA 6, going from binary 1 to binary 0, provides a pulse to reset the DRE flip-flop and set the MRS flip-flop. Head switching is accomplished as previously described; however, clearing the DRE prevents address search until 16 words have been counted. The 16 word settling time is required because a new disk has been selected. If the new disk is positioned at the switching gap, the 16 word delay is bypassed, and address search starts at address 0000_8.

3.5 WRITING DATA ON THE DISK

Figure 3-10 is a simplified block diagram of the functions used in writing data on the disk. Figure 3-9 is a flow diagram that shows the sequence of operations and identifies the circuit components used. Address circuit operation is described in Section 3.4, and a discussion of the address search in this section is limited to the placement of address circuit functions in their proper positions in the writing sequence.

3.5.1 General Discussion

The writing instruction is DMAW (6605_8). This instruction, at IOP time 1, clears the DMA and the MBH registers and clears the RF08 logic to prepare for writing. At IOP time 4, the DMA register is loaded with the address of the first data word location. A separate instruction has already loaded the EMA register with the disk and track number. The three-cycle data break facility of the PDP-8 is then requested. When the PDP-8 accepts this

request, it locates the data for the first word and loads it into the MBH register. The specified track address is located, and the data is loaded into the DMB register. The data bits are then written on the disk serially, lowest order bit first, and a new request for a data break is sent to the PDP-8. While the data bits are being transferred from the DMB to the disk, a new data word is loaded into the MBH. This procedure continues, without issuing a new DMAW instruction, until the number of data words specified in the word count register have been transferred.

Information required by the PDP-8 before the DMAW instruction can be issued is described in Chapter 4. If the number of words transferred is sufficient to fill one address track (or the remainder of one), the system automatically switches to address 0000_8 of the next rack and continues writing. If the last address of the last track is used on a disk, the system automatically switches to the next disk, if one is installed. If not, an NXD flag is set and can be used in the program as an error indication. However, if the disk file has the maximum of four disks installed, a program that exceeds the capacity of the disk file will cause the system to switch to the first address of the first disk and continue writing. At the completion of writing (word count register = 0), the last address + 1 is present in the EMA and DMA registers.

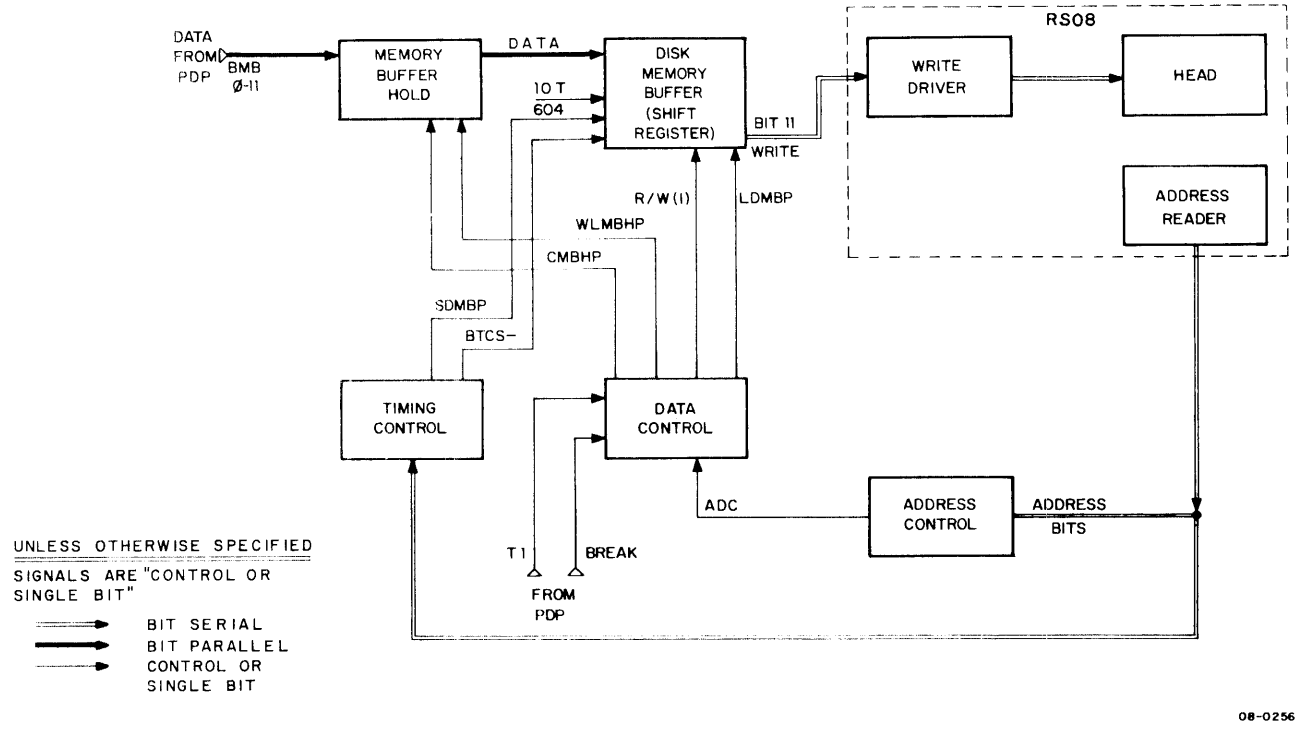


Figure 3-10 Simplified Diagram, Writing Data on the Disk

3.5.2 Logic Flow in Writing Mode

Logic signal flow for the writing mode is discussed below.

3.5.2.1 Sequence of Events that Load the DMB Register

a. The DMAW command is generated in the PDP-8, and at IOP time 1, CDMAP and SCLP 1 and 2 are generated, clearing the DMA and RF08 logic. This operation is described in Chapter 4 for the DCMA instruction.

b. At IOP time 4, the DMA is loaded with the first data word address from the accumulator of the PDP-8. The DBR is set, requesting a three-cycle data break from the PDP-8. The R/W flip-flop is set, indicating the write mode.

c. At this point, the logic flow divides into two alternate paths. Point 1 indicates the beginning of the address search which is shown on this flow chart to indicate the control the address circuits have over data transfer. The operation of the address circuits is described in detail in Section 3.3.

d. At point 2, the system waits for an Address Accepted (ADDR ACC) signal from the PDP-8, indicating the start of the data break cycle. When ADDR ACC is received, DBR is reset. The PDP-8 supplies a B Break pulse and a T1 pulse as it continues through the data break cycle.

e. The B Break pulse sets CMBH, generating a clearing pulse (CMBHP) for the MBH register. The T1 pulse follows. The B Break, T1, and R/W (1) are ANDed to reset the CMBH flip-flop and to generate WLMBHP 1 and 2. This loads the MBH register with the contents of the PDP-8 memory buffer. The data break is now completed, and the PDP-8 continues with the next instruction.

f. The disk file waits until the angular address has been located. The amount of delay depends on the time required to read the track address. The minimum time required is approximately 260 μs (the time it takes TCA, TCB, TCC, and TCD to count 16_{10} words of 16 μs each). This assumes that the correct track address appeared on the 17th word following the LDMAP pulse. TCA, TCB, TCC, and TCD are reset when any of the following conditions occur: a change takes place from read to write, from write to read, or a track select or disk select. Resetting allows the read/write amplifiers to settle before any reading or writing is done. If the address being searched on the disk is in the correct position when TCA, TCB, TCC, and TCD are counting, the time until that address appears again is 33.3 ms (60 Hz). The DBR is accepted at the end of the PDP-8 instruction in progress, within approximately 4 μs; therefore, no inhibiting logic is provided to prevent continuation if the DBR is not accepted. When the address circuits locate the track address, the ADC level goes true. The WEP (occurring at bit-time 14), the ADC level, and the R/W (1) level are ANDed to generate LDMBP, which transfers the data in the MBH to the DMB.

g. The logic flow divides after LDMBP has been generated (see Point 3, Figure 3-9). Continuation of the writing process is described in Section 3.5.2.2.

h. If the WCS is clear when LDMBP is generated, the DBR flip-flop is again set, and a new data break is initiated at point 2 on the flow diagram (see Figure 3-9).

i. When the last data word is transferred to the MBH register, the WCO pulse is received from the PDP-8. This pulse sets the WCS at point 3 on the flow diagram. This inhibits the DBR flip-flop from being set by the LDMBP pulse. Instead, the LDMBP pulse sets the WCO flip-flop. The last data word is written on the disk, and the DEP, at the end of this word, sets the DCF flip-flop. End of transfer is indicated to the PDP-8 when DCF is set. A DFSC instruction may be generated by the PDP-8 to produce a skip instruction. See Chapter 4 for a detailed description.

3.5.2.2 Writing the Data Word in the DMB on the Disk

a. At point 3 on Figure 3-9, the data word has been transferred into the DMB. In the RS08, the Write flip-flop (WFF) was set by the BSCLP. Before the address is confirmed, the buffered write (BWTE) level is false, inhibiting writing current. In addition, EMA bits 7 and 8 select the disk to be used. The select (SLT) level is true only for the disk that has been selected.

b. When ADC becomes true, indicating that the address has been located, it is ANDed with SLT and WFF (1) to energize the DSL+ data sense line. Write current flows in the head, writing a flux transition onto the disk over any previous information written on the selected track.

c. The enabling level for the WFF is provided when BWDE is true and the content of DMB 11 is a 1. If DMB 11 is a binary 0, the enabling level is not generated. The BWDE level is true (logic 1) for the first 12 bit-times, and false (logic 0) for bit-times 13 and 14.

d. The WFF is strobed by Track A Slice Buffered Delayed (TASBD), when BWTE is present. TASBD is generated by the Track A pulse and delayed 250 ns. If the enabling level at the WFF is true, the WFF is complemented by TASBD. This clears the WFF (for the first 1 written) and reverses the writing current, energizing DSL-. The magnetic flux written on the disk is reversed. For each 1 to be written on the disk, the WFF is complemented, reversing writing current direction.

e. If a binary 0 is to be written on the disk, the content of DMB is a logic 0 at BDDMB 11. This condition inhibits the enabling level at the WFF; therefore, there is no effect when TASPD strobes the WFF. The write current remains unchanged, and any previous data is erased.

f. If ADC remains true, TAP is used to generate SDMBP to write the next bit.

g. After the 12th bit is written on the disk, BTCS- occurs, setting the WDE flip-flop. This inhibits the enabling level at WFF. At the same time, however, the WDE (1) level appears as BWDE (1) at the set input to WFF. At bit-time 13, the last TAP pulse in the data word strobes WFF and sets it. If an even number of binary 1s are written, WFF is already set, and a binary 0 is written. If an odd number of binary 1s are written, WFF is set from binary 0 to 1, and a binary 1 is written. The 13th bit is the parity bit and ensures that each word has an even number of binary 1s written, including a parity bit. Because this is the last bit in a word, WFF is always set at the beginning of the next word. When reading, the number of binary 1s in a word is counted by a 1-bit register; therefore, loss of a bit in reading can be detected.

h. The process loops back to point 3 of the flow chart (see Figure 3-9) and continues as long as ADC is set. ADC can be cleared either by the end of a data transfer or by a head switch. A head switch on the same disk reenters the process at point 4 of the flow chart, and a disk switch reenters the process at point 1. When the address is confirmed again and ADC is set, the writing begins again at point 5 of the flow chart.

i. If EMA bit 6 is a binary 1 and is incremented to binary 0 during a head switch, the current disk is filled. If the next higher disk is not installed a nonexistent disk (NXD) flag is set. However, addressing a nonexistent disk prevents the timing track signals from operating the RF08 address circuits. DRE and ADC remain clear, and the process halts at points 1 and 5 of the flow chart (see Figure 3-9). The data word loaded in the MBH register cannot be written on a disk. However, the associated data break for loading this word into the MBH register has been executed, and the word count and current address registers hold a count that is 1 greater than both the number of words to be transferred and the current address. (Note that the number in the word count register is a negative number.)

3.6 READING DATA FROM THE DISK

The DMAR instruction sets the RF08 logic for reading. Initially, the address placed in the DMA register is located on the disk; once this address is located, the data is read serially from the disk, low-order bit first,

and then shifted into the DMB. At the end of each word read, the data shifted into the DMB is parallel transferred into the MBH, and a data break is requested. Meanwhile, the next data word from the next higher data address is read into the DMB. When the PDP-8 accepts the DBR, the data in the MBH is strobed into the PDP-8 memory buffer and stored in the address specified. Each data word is read until the word count is 0. The number of words read in the block is specified by placing the number in the word count register before issuing the instruction DMAR. The addresses, to which the data read is transferred, are specified by the current address register. These registers are both located in the PDP-8 and described in Chapter 4. The current address is incremented by 1 each time a DBR occurs. The series of words read from the disk is transferred to a series of addresses in core memory. The word series (in a block on a disk) are read from adjacent addresses; that is, the first word read comes from the address specified by the DMA contents, the second word comes from the next address, etc. No addresses are skipped during a block transfer.

3.6.1 Data Flow When Reading

Figure 3-11 is a block diagram of data flow when reading, and Figure 3-12 depicts the DMAR Read Logic flow. The following text is a discussion of DMAR logic flow:

a. The DMAR instruction is generated by the PDP-8. At IOP time 1, SCLP and SCLP 1 and 2 pulses are generated, clearing TCA, TCB, TCC, TCD and DMA.

b. At IOP time 2, the first disk address is loaded into the DMA. The Read/Write flip-flop is clear, enabling the contents of the MBI (in the RS08) to be read into DMB 0 when ADC becomes true.

c. Next, the track address is located as described in Section 3.4.1. ADC goes true at the end of the address word which matches the contents of the DMA register.

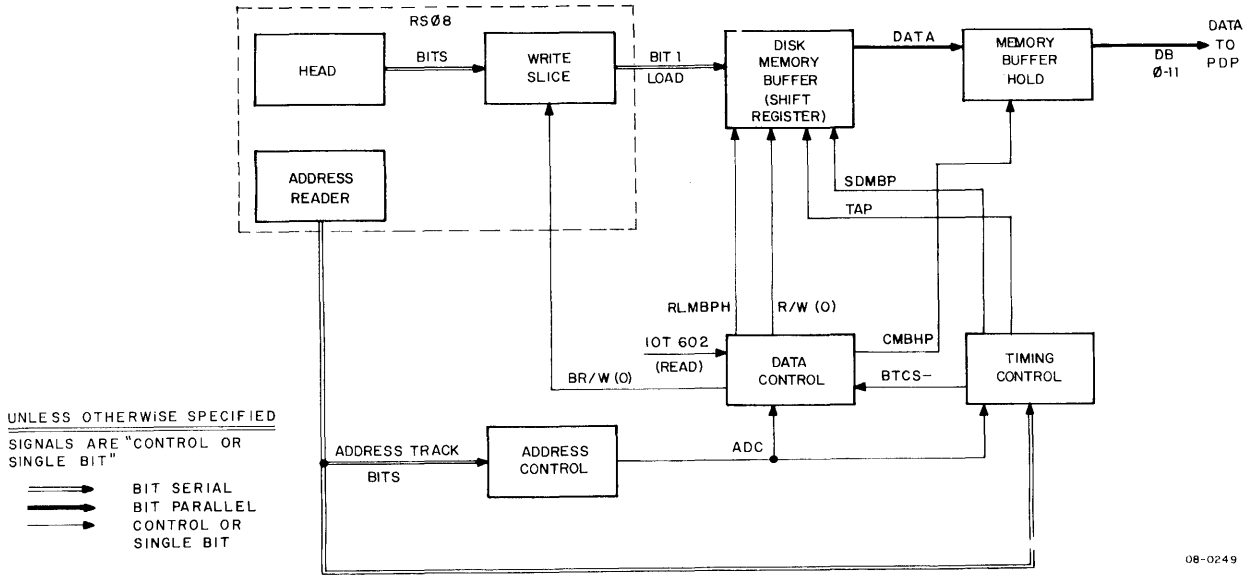


Figure 3-11 Data Flow When Reading

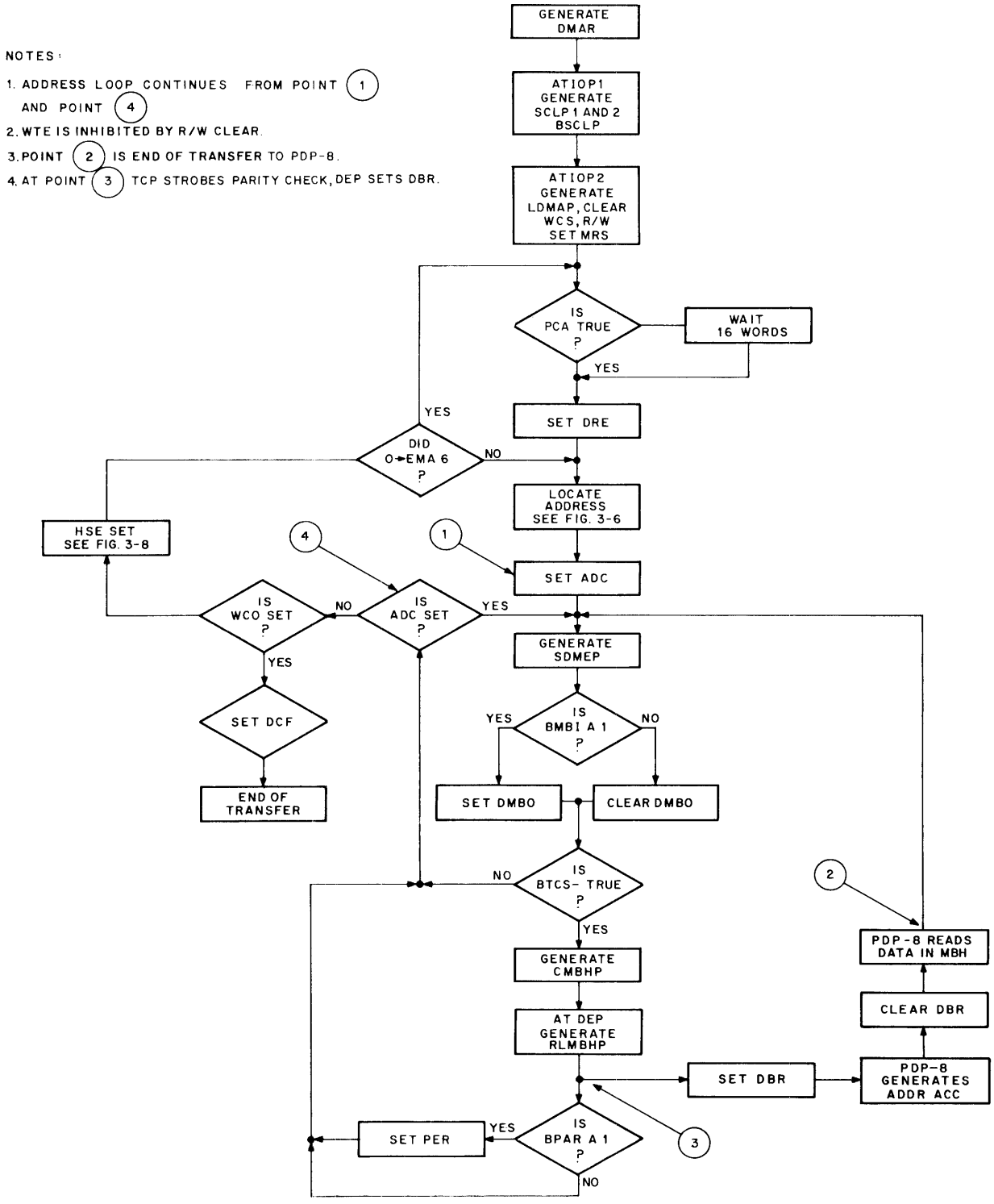


Figure 3-12 DMAR Read Flow Diagram

d. The first Track A Pulse (TAP) of the next data word generates the SDMBP shift pulse which right shifts the DMB 1 bit before any data is strobed in. There are 12 more TAP pulses in each data word, therefore, the data is shifted 12 times although SDMBP generates 13 shifts in the DMB.

e. MBI is cleared by the first TAP pulse, and the contents of MBI are delayed 40 ns before acting on DMB 0. This delay compensates for cable and logic skew time, ensuring that MBI is present at the correct time to act upon DMB 0. The contents of MBI are jam-transferred into DMB 0.

f. After the first bit of the data word is read, BTCS- is not true, and the reading process loops. ADC is set, and the second TAP pulse generates the second SDMBP pulse. This condition causes the data in DMB 0 to shift into DMB 1. Following SDMBP, the contents of MBI, representing the second bit of information read from the disk, are loaded into DMB 0.

g. At the end of a data word (bit-time 12), BTCS- goes true. BTCS- is ANDed with Read/Write (0) and ADC (1) to generate CMBHP, which clears the MBH register. At bit-time 14, BTCS+ goes true, generating the TCP pulse. TCP generates DEP which is ANDed with Read/Write (0) to generate the Read Load Memory Buffer Hold Pulses (RLMBHP 1 and 2).

h. RLMBHP 1 and 2 transfer the data in the DMB to the MBH. Only after all 12 data bits have been strobed and shifted into DMB 0, are RLMBHP 1 and 2 generated. The first data bit strobed, which is the lowest order bit, is not in DMB 11.

i. RLMBHP 1 and 2 is ANDed with WCS (0) to set the Data Break Request (DBR) flip-flop. Point 3 on the flow diagram depicts this (see Figure 3-12). WCS inhibits a DBR after the PDP-8 word count register becomes 0000_8, which signifies the end-of-transfer.

j. When the PDP-8 accepts the DBR, it generates ADDR ACC as part of the three-cycle data break which clears the DBR flip-flop. The data in the MBH register is strobed into the PDP-8 memory buffer. This point is the end of read transfer between the disk and PDP-8. If words remain to be transferred (indicated by a negative WCO), the transfer loops back to point 1 on the flow chart (see Figure 3-12).

3.6.2 Operation at the End of an Address Track

When all of the data from one address track has been read, and data transfer is to continue at the beginning of the next track, ADC is cleared, and data transfer is inhibited until the switch has been completed. When the switch has been completed, ADC is set again, and data transfer continues from address 0000_8 of the new track selected. Automatic head switching to the new track increments the EMA by 1; the new track number is the old track number +1. Operation of the head switching logic is described in detail in Section 3.4.1.3. Operation at the end of a disk, when a new disk is automatically selected, is described in Section 3.4.1.3 and 3.4.1.4 (also see Figure 3-12).

The program branches at point 4 of the flow chart (see Figure 3-12). If ADC is clear, and WCO is set, then HSE is set to indicate the end of a track. The EMA is incremented, and the next head is addressed. If EMA 6 does not go to 0, the new head is on the same disk, and address search begins at address 0000_8. This address is confirmed, and reading transfer begins at the next address time. The data is delayed one word from its associated address; therefore, the first data will be read from address 0000_8. If EMA 6 does go to 0, a new disk has been addressed. If the switch attempts to locate the new disk at any point on a track other than the head switching gap, DRE is cleared to prevent address search. When address 0000_8 is located on the new disk, reading begins again.

3.6.3 End of Data Transfer

The number of data words transferred is specified by the number placed in the Word Count Register (WCR) before the DMAR instruction is generated. Each time a data word is transferred, the WCR is incremented by 1. The 1 is added before the data word is transferred and before the contents of the WCR are checked. If the content of the WCR is 0, WCO is generated. Operation is similar to the execution of an ISZ instruction, except that the WCO pulse is generated, rather than a skip. In a read transfer, the WCO pulse clears the WCO flip-flop immediately and simultaneously sets the WCS flip-flop. The data word corresponding to the last DBR is transferred and the next data word on the disk is read into the DMB and loaded into the MBH; however, DBR is not set. DEP 1 and WCO (0) are ANDed at the input to the DCF flip-flop, setting DCF.

Chapter 4
Operation and Programming

4.1 INTRODUCTION

RF08/RS08 operation is under program control of the computer. The only operator controls are the WRITE LOCKOUT switches located on the RS08 logic chassis (see Figure 4-1).

This chapter discusses the operation and programming of a single RS08 Disk; however, it is equally applicable to all RS08s in a system, except where noted.

Power for the RF08/RS08 logic circuits is provided by the central processor switched power bus. Disk motor power is provided from a separate unswitched power bus. When the disk is at rest, the heads are in contact with the disk. When the disk is operating, the heads are held a small distance from the disk by a cushion of air.

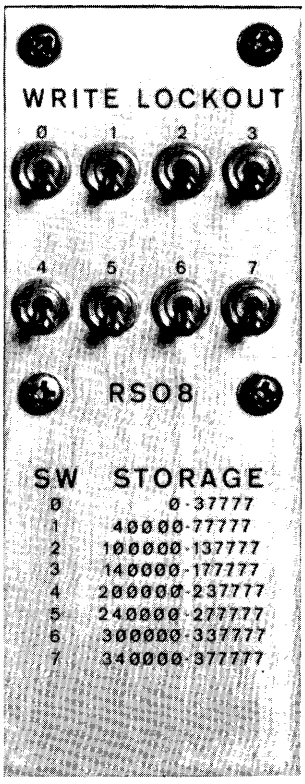


Figure 4-1 Write Lockout Switch Diagram

4.2 TABLE OF INSTRUCTIONS

Table 4-1 shows the instructions used to program the RF08/RS08. All programming instructions use standard IOT instructions with IOP pulses.

Two instructions initiate the operation of the three-cycle data break facility: instruction DMAW, which loads the Disk Memory Address register (DMA) with the contents of the AC and begins writing; and instruction DMAR, which loads the DMA with the contents of the AC and begins reading.

Table 4-1
Mnemonic and Octal Code Instructions

Mnemonic	Octal Code	Description
DCMA	6601	Generates System Clear Pulse (SCLP) at IOP time 1. Clears Disk Memory Address (DMA), Parity Error Flag (PEF), Data Request Late Flag (DRL), and sets logic to initial state for read or write. Does not clear interrupt enable or extended address registers.
DMAR	6603	Generates SCLP at IOP time 1 (see DCMA). At IOP time 2, the computer loads DMA with the contents of AC and then clears the AC. Read continues for the number of words in the WC register (PDP-8 address 7750_8).
DMAW	6605	Generates SCLP at IOP time 1 (see DCMA). At IOP time 4, the DMA is loaded with the contents of AC and the AC is then cleared. A data break is immediately requested by the RF08. When the disk angular address is located, writing begins; the disk address is incremented for each word written.
DCIM	6611	Clear the disk interrupt enable and the extended address registers at IOP time 1. This instruction, with DCMA, clears all flags.
DSAC (Maintenance Instruction)	6612	At IOP time 2, skip the next instruction if Address Confirmed (ADC) is true, thus indicating that DMA address and disk angular address compare (ABC is clear at TCP). The AC is then cleared.
DIML	6615	At IOP time 1, clear the interrupt enable and the memory address extension registers. At IOP time 4, load the interrupt enable and memory address extension registers with data in the AC and clear the AC.
DIMA	6616	Clear the accumulator at IOP time 2. At IOP time 4, load the contents of the status register into the AC for evaluation. The contents of the status register are not altered. Similar to DSAC; however, MB9 is a binary 1, inhibiting skip on ADC.
DFSE	6621	Skip next instruction if Data Request Late (DRL), Parity Error (PER), Write Locked Track Selected (WLS) or Nonexistent Disk (NXD) flag is set.
DFSC	6622	Skip next instruction if the Data Completion Flag (DCF) is set.
DISK	6623	Skip next instruction if either an error or Data Completion Flag is set. (Microprogrammed OR of DFSE and DFSC.)
DMAC	6626	Clear the AC at IOP time 2. Load the contents of the DMA into the AC at IOP time 4. The contents of the DMA are not altered.
DCXA	6641	Clears the 8 EMA register bits.
DXAL	6643	At IOP time 1, clears the 8 EMA register bits (same as DCXA). At IOP time 2, loads the EMA with bits 4 through 11 of the AC. Data in bits 0 through 3 of the AC are ignored. The AC is cleared at the end of IOP time 2 (see Figure 4-2).
DXAC	6645	Clears the AC at IOP time 1. At IOP time 4, the 8 EMA register bits are loaded into bits 4 through 11 of the AC. The contents of the EMA are not disturbed.

Table 4-1 (Cont)
Mnemonic and Octal Code Instructions

Mnemonic	Octal Code	Description
DMMT (Maintenance	6646 Instruction)	For maintenance purposes only. With the appropriate maintenance cable connections and the disk disconnected from the RS08 logic, the following standard signals may be generated at IOT 646 and associated AC bits. AC is cleared. The maintenance register is initiated by issuing an IOT 601 command. AC_{11} (1) → TTA pulse AC_{10} (1) → TTB pulse AC_{9} (1) → TTC pulse AC_{7} (1) → DATA PULSE (DATA HEAD #0) AC_{6} (1) + 1 → Photocell AC_{0} (1) + 1 → DBR Setting DBR to binary 1 causes a Data Break Request in the computer. NOTE TTA must be generated to strobe the TTB signal into the address comparison network.

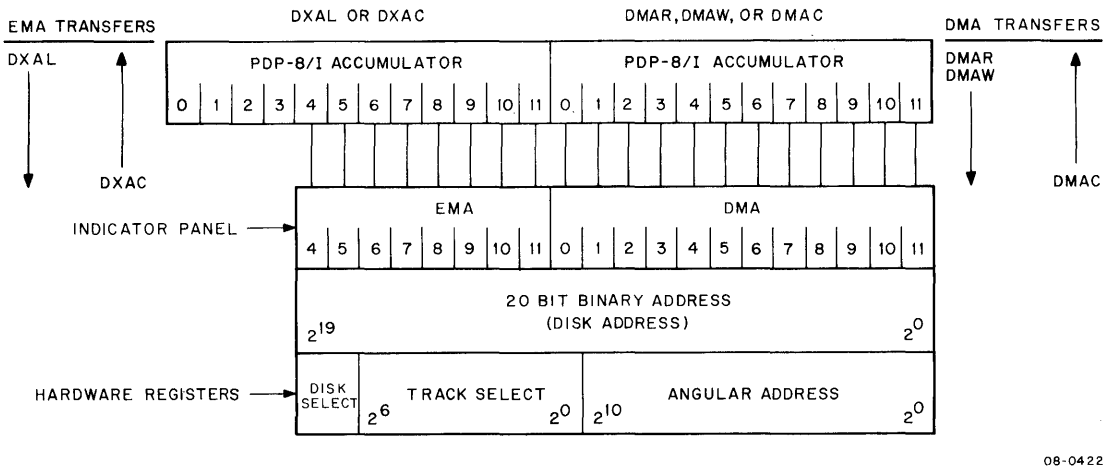


Figure 4-2 EMA and DMA Transfer Diagram

4.3 ADDRESS CONFIGURATION

To address the maximum storage capability of the disk system (1,048,576 words), a 20-bit binary address is required. The 12 lower-order bits are called the Disk Memory Address (DMA) and are transferred from the accumulator by the DMAW (write) or the DMAR (read) instructions. The eight higher-order bits, form the Extended Memory Address (EMA) and are loaded from bits 4 through 11 of the PDP-8 accumulator (see Figure 4-2).

Assignment of the PDP-8 AC bits are chosen to form a 20-bit true binary address. Because there are 2048 words per track, 11 bits are required to determine the angular address. In addition, seven bits of the address are required to specify one of 128 tracks per disk. Similarly, two bits are required to select one of four disks. Thus the sub-fields of the EMA and DMA are related to the actual physical placement of data bits.

The typical program is concerned with a true binary address rather than with angular addresses, tracks, or disks. Sequencing across tracks or disks is program transparent, except for disk switching latency.

The contents of the EMA register are loaded into the PDP-8 AC by the DXAC instruction. This instruction clears the AC at IOP time 1 and transfers the contents of EMA to the AC at IOP time 4. Because AC bits 0 through 2 are not involved in the EMA address, these bits will be 0s after the DXAC command is executed.

The highest-order bit of the EMA (bit 0) is programmed by the instructions for the DMA. The EMA instructions operate on EMA bits 1 through 7. Figures 4-1 and 4-2 show this division. Because the RF08 is programmed with a 2-word absolute address, this division becomes significant only for the maintenance of the RF08 and for critical software timing.

4.4 WRITING DATA ON THE DISK

Before data transfer can occur, two words of information must be loaded into the PDP-8 memory. Memory locations 7750_8 and 7751_8 are specified as the Word Count (WC) and Current Address (CA) registers, respectively, for the disk file by hard wiring in the RF08. The number placed in the WC register (address 7750_8) is the 2's complement of the number of words to be transferred; i.e., if seven data words are to be transferred, 7771_8 is loaded into address 7750_8. The CA (core memory location 7751_8) is always incremented before use, therefore, it is set to one less than the core memory location to be addressed for the first data word transfer.

For example, if a block transfer is to write core locations 4000_8 through 4006_8 onto the disk, the WC register should be loaded with 7771_8 and the CA register with 3777_8 before issuing the DMAW IOT. The PDP-8 then places the contents of address 4000_8 in its Memory Buffer (MB) and strobes these contents into the RF08 Memory Buffer Hold register (MBH) to begin data transfer.

The DMAW instruction establishes a Data Break Request (DBR) for the PDP-8. When the request is acknowledged by the PDP-8, a three-cycle data break transfer is selected. When the PDP-8 completes the three-cycle data break, it returns to the program, and the RS08 writes the information loaded into the MBH onto the disk. After the word is written, the RF08 generates another Data Break Request (DBR), and the three-cycle data break is repeated. The end of data transfer is signaled to the RF08 by a Word Count Overflow (WCO) from the PDP-8, when the RF08 requests the last data word to be written. When transfer is complete (DCF set), the DMA and EMA registers in the RF08 contain the address of the last data word written.

4.5 READING DATA FROM THE DISK

Reading uses the three-cycle data break facility of the PDP-8, as described in the preceding paragraphs. Before starting a read cycle, one address less than the first core address (into which information read from the disk is to be transferred) must be placed in core location 7751_8. Also, the number of words to be transferred must be placed in core location 7750_8 as the 2's complement. The Extended Memory Address (EMA) is then loaded into the EMA register from the PDP-8 accumulator with the DXAL instruction. Refer to Section 4.3 for a discussion of loading the memory address. Next, the initial disk address is placed in the PDP-8 accumulator and is loaded into the RF08 DMA register at the beginning of the DMAR read command. After the DMA address is loaded, the address is located and reading begins. At the end of the word, the data is transferred from the Disk Memory Buffer (DMB) to the Memory Buffer Hold register (MBH), and the Data Break Request (DBR) flag is set. The DMB is now free to read the next data word, while the PDP-8 accepts the data word stored in the MBH and resets the DBR flag.

As the PDP-8 advances through its data break cycle, initiated by accepting the DBR flag, it adds a 1 to both the word count (in 7751_8) and the current address (in 7751_8). When the next data word has been transferred to the DMB, the cycle repeats. This continues until the word count becomes 0, which sets the Data Completion Flag (DCF), ending data transfer. At the end of a data transfer, the disk address is one greater than the last disk address from which data was read. The new disk address is contained in the DMA and EMA registers. The EMA is loaded by the DXAL instruction, which establishes the nine high-order bits of the disk address. The 12 lower-order bits are loaded from the PDP-8 AC into the DMA with the DMAW IOT instruction.

Address 7751_8 contains the last address into which data can be stored in the PDP-8 memory. Address 7750_8 contains 0000_8.

4.6 STATUS REGISTER

The status register contains the disk flag, interrupt control bits, and core memory extension bits. These bits are described in the following paragraphs.

4.6.1 Photocell Sync Mark (PCA)

There is no photocell in the RS08, consequently, the PCA signal is generated logically. It is designated PCA because it is similar in function to the DF32 photocell. The PCA flag occurs approximately 50 μs after the last word (3777_8) appears on the tracks of the disk. The flag is set for 100 μs to indicate the origin mark on the disk.

Special logic is provided in the RF08 to override the normal 16-word synchronizing period for either the DMAW or DMAR instructions issued during this time. For example, if successive 4096 word fields are to be written continuously on the disk, the program can optimize the transfers by setting up the next transfer during PCA time to

eliminate rotational latency. Note that this feature is valuable only when the starting angular address (DMA1-DMA11) is less than 17_8.

4.6.2 Data Request Enable (DRE)

The DRE signal is used for maintenance purposes and indicates that the control is searching for an address or transferring data.

4.6.3 Write Lock Selected (WLS)

The WLS signal indicates that the selected disk address is write-locked via the switches on the RS08. The status bit is set only on the DMAW instruction. Regardless of the commands issued to the RF08, data cannot be written in a write-locked area.

4.6.4 Error Interrupt Enable (EIE)

The EIE signal enables an interrupt on the inclusive OR of WLS, DRL, NXD, and PER.

4.6.5 Photocell Interrupt Enable (PIE)

The PIE signal enables an interrupt on PCA; however, caution should be exercised when enabling this interrupt because the interrupt request lasts only 100 μs.

4.6.6 Completion Interrupt Enable (CIE)

The CIE signal enables an interrupt on completion of an operation (WCO issued by the computer).

4.6.7 Core Memory Extension Field

The core memory extension field is for data transfers.

4.6.8 Data Request Late (DRL)

This flag indicates the PDP-8 did not honor the data break request soon enough to prevent the loss of data (refer to Section 4.10).

4.6.9 Nonexistent Disk (NXD)

This flag indicates a disk has been selected that does not exist logically. A jumper card in the RS08 associates a physical disk with a logical number (refer to Section 4.8).

4.6.10 Parity Error (PER)

The PER flag indicates a parity error occurred in the read mode. The flag is set and the interrupt is requested (if EIE enabled) at the end of the erroneous word.

Care must be exercised if combinations of interrupt enables are used, since one, two, or three interrupts may occur during a single transfer, depending on the timing of the interrupt requests.

By storing the current address (CA) at the time of the PER interrupt, it is possible to approximate the location on the disk causing the error. The transfer always continues until it receives a Word Count Overflow (WCO) pulse from the PDP-8.

4.7 DATA TRANSFER INVOLVING TWO DISKS

If more than one disk is installed, a transfer can start on one disk and end on a second disk. Switching between disks is performed automatically by the RF08; i.e., no additional instructions are required in the program. Because the angular positions of RS08M disks are not synchronized, an accessing latency occurs when the transfer sequence switches from the last address of disk n to the first address of disk n + 1.

4.8 OVERFLOW OF DISK CAPACITY

When less than four disks are controlled by an RF08 Control, a read/write transfer from the last physical address causes the Nonexistent Disk (NXD) flag to be set.

If four disks are controlled by an RF08 Control, the addressing "wraps around"; i.e., the addressing will sequence from address $3,777,777_8$ to 0_8 without setting the NXD flag. Transfers continue as described in Section 4.5.

When switching disks, the RF08 logic must resynchronize to the new timing tracks. When switching tracks on a given disk, a delay must be provided to permit the read amplifier to recover. The synchronizing or amplifier recovery delays requires 16 word times. Thus, the minimum access time is 260 μs for 60 Hz disks and 320 μs for 50 Hz disks. The origin gap is of sufficient length (550 μs) to permit spiral reading or writing.

The write-to-read recovery time of the data amplifier must be considered for specialized programming applications. The amplifier recovery time depends on the data previously written. Worst case occurs after a 2048_{10} write of all zeros. Best case is defined by the minimum access time.

4.9 PROGRAMMING DIFFERENCES BETWEEN RF08/RS08 AND DF32

Programming for the RF08/RS08 follows the general programming layout of the DF32. Table 4-2 lists the mnemonic instructions and corresponding octal code for the RF08/RS08 and the DF32. Each instruction is

followed by a comparison of the differences between the two units. The addressing of both disks is similar; however, the RS08 has 2^7 tracks, while the DF32 has only 2^4. This added addressing capability is placed in the Extended Memory Address (EMA) register, which has been extended with three more significant bits. The two most significant bits address the disk by number (disk 0-3), in both units. Where the mnemonics differ, the DF32 mnemonic can be used to obtain the desired octal code during assembly.

Table 4-2
Comparison of DF32 and RF08/RS08 Instructions

DF32 Mnemonic	Octal Code	RF08/RS08 Mnemonic	RF08/RS08 to DF32 Comparison
DCMA	6601	same	Identical functions.
DMAR	6603	same	Identical functions.
DMAW	6605	same	Identical functions.
DCEA	6611	DCIM	Clears interrupt enable, does not clear EMA. Clears memory address extension on both units.
DSAC	6612	same	Identical functions.
DEAL	6615	DIML	Similar, except functions transmitted from the AC are different. EMA information not transmitted. See DXAL.
DEAC	6616	DIMA	Similar, except that functions transmitted to the AC are different. See DXAC.
DFSE	6621	same	Instruction is skipped on error, rather than skip -- no error. NXD added as an error.
DFSC	6622	same	Identical functions.
(none)	6623	DISK	New instruction. Skips on error or data completion, or both. (DFSE and DFSC combined.) Skip enabled at IOP 2.
DMAC	6626	same	Identical functions.
(none)	6641	DCXA	Clears EMA.
(none)	6643	DXAL	Clears and loads EMA with information in the accumulator.
(none)	6645	DXAC	Clears accumulator and loads address in EMA into the accumulator.
(none)	6646	DMMT	Maintenance instruction (refer to Table 4-1).

4.10 INSTRUCTION AND DATA TRANSFER EXECUTION TIMES

4.10.1 IOT Execution

All of the instructions used by the central processor to control the RF08 are IOT instructions. These are fully described in the maintenance manual for the associated user's central processor. In the PDP-8 series, execution time for an IOT instruction is approximately 4.25 μs.

4.10.2 Data Transfer

Each 12-bit data word transferred requires a three-cycle data break, (4.5 μs duration). Timing of the data break requests is controlled by disk file operation and is asynchronous with respect to central processor operation. The central processor acknowledges the highest priority Data Break Request at the end of an instruction cycle. After all data breaks are serviced, the central processor continues with the next instruction.

4.10.3 Data Break Priority

Two factors affect the latency period between the DBR and the transfer of data between the PDP-8 and the RF08. First, the data break cannot be honored until completion of the current instruction, which can be up to 18.5 μs for worst case conditions such as EAE normalize (optional). Second, any outstanding break requests from higher priority devices must be honored before responding to the RF08 Data Break Request (DBR).

If the particular installation uses the DM01 Data Multiplexer, the RF08 system must be the highest priority data break device and, therefore, should be attached to the device zero port.

The RF08 has a Data Request Late (DRL) flag which indicates that a DBR was not honored in time for normal operation. If the DRL is set, one or more words may have been omitted on a read (although the correct number of words will have been transferred). Similarly on a write, too many words can be transferred from core, but one or more may be missing "in the middle".

Depending on the duration of the latency period before the PDP-8 answers the data break, data words may be omitted (as described above) or an erroneous data transfer may occur.

If EAE normalize (NMI) is executed while the RF08 is transferring data, the DRL flag will be set to indicate an erroneous transfer. If correct data is required, the operation must be repeated.

4.10.4 Reliability

Software, utilizing the RF08/RS08 Disk subsystem, should make provisions for errors in data transfer. This does not imply that the RF08 is unreliable, but it is an acknowledgment of the fact mechanical devices are not as inherently reliable as solid state devices.

In most applications, automatic rereading of bad data is sufficient. Eight to ten rereads should be attempted before calling it a "hard" error. For applications requiring extreme reliability, additional error detection and error correction must be used. The following are useful techniques:

a. Adding longitudinal parity checks, Hamming codes, or cyclic redundancy checks into the data for additional error detection and correction.

b. Use of the RF08 address registers as a cross check after completion of a read or write operation. The registers can be compared with those values computed from the record length and starting address.

c. Reading the data immediately after it is written. A "read after write" operation is especially valuable when loading the system onto disk. It requires no additional time because the disk is much faster than the peripheral supplying the data.

d. Multiple copies of the data can be kept on the disk. For maximum protection against electronic, head, or disk failure, the data must be written on data tracks whose two most-significant octal digits differ by 03 or more and whose least-significant digits are not the same.

Chapter 5
Maintenance

5.1 INTRODUCTION

The RF08/RS08 Disk has been properly aligned at the factory prior to shipment and should not require further alignment. If, however, realignment is required, the following procedures must be performed, in the order presented.

5.2 TEST EQUIPMENT

The test equipment and diagnostic programs required for alignment are: a Type 543 Tektronix oscilloscope, or the equivalent, with two 10X probes and ground clips; Track Selection Subroutine SA0265; and Disk Data Diagnostic subroutine SA201.

5.3 TIMING TRACKS AND DATA TRACK TIMING

The following alignment procedures are to be performed on the G085 Disk Read Amplifier and Slice Module mounted in logic panel locations A02 and B02, A03 and B03, A04 and B04, A12 and B12.

5.3.1 Timing Track Gain Adjustment

The following is the proper procedure for adjusting the Timing Track Gain.

Step	Procedure
1	Calibrate the the oscilloscope to produce 1V per cm. It is important that the two 10X probes be properly compensated.
2	Ground the channel 1 probe to the ground pin of the G085 Module under test.
3	Trigger the oscilloscope from ON-LINE, set the horizontal sweep to 5 ms/cm, DC-couple the oscilloscope probe, and calibrate channel 1 to produce a vertical amplitude of 0.2 V/cm. The effective gain with the 10X probes is 1V per cm.
4	With the channel 1 probe connected to A02-T (see Figure 6-38), adjust the A section of gain control R21 to produce an average amplitude of 7V peak-to-peak.
5	Repeat Step 4, alternately connecting the channel 1 probe to A03-T (Module location A04 and B04).

5.4 TIMING TRACK SLICE ADJUSTMENT

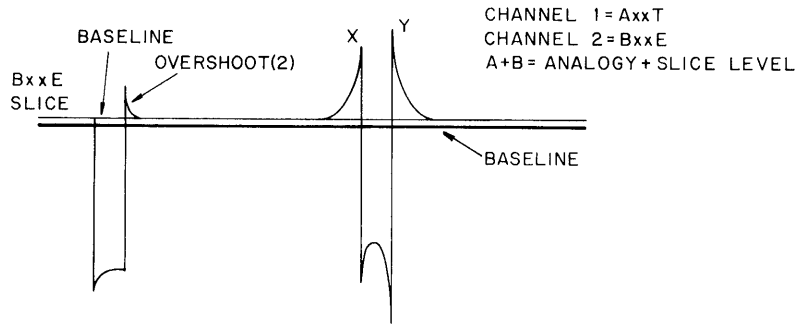
The following is the proper procedure for Timing Track Slice adjustment:

Step	Procedure
1	Before makine Slice adjustments, the positive overshoot must be recorded. Set channel 1 to produce only 0.1 V/cm, DC-couple the channel 1 probe, set the horizontal time base to 2 μs/cm, and trigger the oscilloscope from internal AC.
2	Connect the channel 1 probe to B02-E for TTA adjustment, B03-E for TTB, and B04-E for TTC (see Figure 6-38).
3	Position the oscilloscope vertical display until the baseline rests on the horizontal center graticule and place the trailing edge of the waveform on the vertical center graticule.
4	Measure and record the difference between the baseline and the positive transition over the baseline of the trailing edge.
5	Set channel 1 to produce 0.1 V/cm, DC-couple the channel 1 probe, place the oscilloscope in the ADD mode (do not invert), trigger channel 1 trace from internal AC, and set the horizontal sweep to 0.2 μs per cm. Be certain that the probes are properly compensated.
6	Connect the channel 1 probe to A02-T and ground it to A03-C; connect the channel 2 probe to B02-E and ground it to B02-C.
7	Change the horizontal sweep to 2 ns/cm and center the display on the oscilloscope horizontal center graticule. Return the sweep to 2 μs/cm and adjust the oscilloscope to produce a stable display.
8	Subtract the overshoot of the trailing edge of the slice waveform measured in Step 4 from the amplitude of the trailing edge of the sliced analog waveform shown in Figure 5-1.
9	Adjust the slice potentiometer on the G085 Module in location B02 to produce a slice level of 1.35V above the baseline (see Figure 6-20).
10	Repeat Step 9 for Timing Track B (TTB) and C (TTC) and for G085 Modules in locations A03-T, B03-T, and B04-E. When making each measurement, ground the channel probe to the module ground point. Ground termination points are shown in Figure 6-20.

5.5 GUARD BAND AND PCA ADJUSTMENT

The following is the proper procedure for guard band and PCA adjustment:

Step	Procedure
1	Set channel 1 of the oscilloscope to produce 0.1 V/cm and DC-couple the probe. Set channel 2 to 0.1 V/cm and DC-couple the probe. Place the oscilloscope in the ADD mode, trigger channel 1 only from internal DC negative, and set the horizontal sweep to 50 μs/cm.
2	Connect the channel 1 probe to B08-M on the RS08 and the channel 2 probe to A02-T.



NOTES:

1. Measure and record the overshoot (2). It is approx. 1 volt.
2. Subtract overshoot (2) from Y, then average the leading and trailing slice points to establish the slice level.

$$\text{SLICE LEVEL} = \frac{(Y-2)+X}{2}$$

08-0480

Figure 5-1 Analog Slice Waveform Diagram

Step	Procedure
3	Sync the oscilloscope and adjust the upper potentiometer on B08 until the negative-going square wave is 100 μs in duration. This time duration is of minimum value, however, 110 μs provides more reliable results.
4	Vary the potentiometer on B07 until a single spike appears centered on the square wave, thus ensuring the proper guard band.

5.6 DATA TRACK GAIN (AGC EQUALIZATION)

The following is the proper procedure for Data Track Gain adjustment:

Step	Procedure
1	To successfully perform Data Track Gain adjustments, the RF08/RS08 system must be capable of writing all 1s on every data track; it must also be capable of reading, with errors permissable, on each data track.
2	Write all 1s on all data tracks, using Disk Data Diagnostic subroutine SA201.
3	Set the oscilloscope vertical amplitude to 0.2 V/cm, set the sweep speed to 2 ms/cm triggered from ON-LINE, and connect the channel 1 probe to A12T grounding it to A12-S.
4	Using Disk Data Track selection subroutine SA0265, adjust the G085 gain potentiometer in location A12 to obtain a reading of 7V peak-to-peak on data track 000.

Step	Procedure
5	Using Disk Data Track selection subroutine SA0265, measure and record the amplitudes of all data tracks on the RS08 Amplitude Sheet. Observe the results and equalize the data tracks as required using AGC jumpers.
6	After equalizing the data tracks, set the G085 gain so that the highest amplitude track is 12V peak-to-peak.

NOTE

Average data track amplitude must never exceed 12V peak-to-peak or go below 4.5V peak-to-peak. If these conditions are not met, adjust the gain of the G085 module, located in slot A12, to compensate for the difference, then repeat Step 5.

If compensation is not met, reject the unit and change the read/write head to low or high TK.

5.7 PRELIMINARY DATA TRACK SLICE ADJUSTMENT

The following is the proper procedure for preliminary Data Track Slice adjustment:

Step	Procedure
1	Setup the oscilloscope as described in Section 5.4, Step 1; be certain to measure the overshoots.
2	Read all 1s onto the disk, using the Disk Data Diagnostic subroutine SA201.
3	Connect the channel 1 probe to B20-F and adjust DC DATA to produce 500 ns.
4	Connect the channel 1 probe to B11-F and adjust WIND to produce 500 ns.
5	Connect the channel 1 probe to B19-E and adjust B301 to produce 500 ns.
6	Set the G085 module slice level, in location B12, to 1.35V.

5.8 DATA GATING ADJUSTMENT

The following subparagraphs contain the proper procedures for adjusting their respective data gates.

5.8.1 TASD Adjustment

Step	Procedure
1	Connect the channel 1 probe to TC TAS (connection B10L); connect the channel 2 probe to TC TASD (connection B10-N) (see Figure 6-38). Internally trigger the oscilloscope from the AC, place the oscilloscope on negative, channel 1 mode only, and an alternate sweep of 100 ns/cm.

Step	Procedure
2	Adjust the B312 variable delay in location B10 to produce a 250 ns delay on channel 2 (see Figure 6-9).

NOTE

Any time the gain or slice of TTA is changed, this adjustment must be made.

5.8.2 DC WIND Adjustment

Step	Procedure
1	Connect the channel 1 probe to B11-F and monitor DC WIND.
2	Adjust B301 for a 500 ns delay to produce a 500 ns output (see Figure 6-40).

5.8.3 DC DATA Adjustment

Step	Procedure
1	Using the Track Selection subroutine SA0265, select data track 000.
2	Connect the channel 1 probe to B20-F and monitor DC DATA. Adjust B301 for a 500 ns delay to produce a 500 ns output (see Figure 6-40).

5.8.4 DC COP Optimization

Step	Procedure
1	Connect the channel 1 probe to B19-T, the 500 ns TC TAP delay (see Figure 6-40).
2	Connect the channel 2 probe to B20-F, the DC DATA output.
3	Select each data track on the switch register and record the delay between DC DATA and TC TAP.
4	Reconnect the channel 1 probe to B11-F, the DC WIND 500 ns delay.
5	Alternately switch to the data tracks having the least and most delay from TC TAP, as previously recorded. Adjust the potentiometers on B19 and B301 for a 500 ns delay until DC WIND and DC DATA coincidence are equal.
6	Reconnect the channel 1 probe to A07-H (DC DOP) and set the oscilloscope for positive triggering.
7	Observe the results of the two data tracks monitored in Step 5. If either one of the two data tracks produces a DC DOP level of less than 200 ns, the recording head corresponding to that data track must be changed.

5.8.5 Final Slice Adjustment

Step	Procedure
1	Connect the channel 1 probe to B20-F, the 500 ns DC DATA delay connection (see Figure 6-40). Raise the slice level by adjusting the control on G085 Module B12.
2	Using Disk Data Diagnostic subroutine SA201, write all 0s on the disk, then use the read operation for reading of data. Do not alternately read and write.
3	Lower the slice level until a data bit pickup occurs, then record this slice level.
4	Find the average of the two slice levels measured in Section 5.8.5, Steps 1 and 3, then set the slice level to this average.

5.8.6 Additional Adjustments

The following steps are provided to simplify the diagnosing of problems and to aid in the necessary adjustments.

A. Bit Pickups

1. Slice-to-Low: Increase the slice level using the procedures in Section 5.6. A slice adjustment compromise can be made by testing for dropouts with a 5252 pattern and checking for pickups with a 5252 or 4001 pattern.

   Following this procedure, repeat DC DOP Optimization procedures in Section 5.8.4. If a bit pickup is still present, use a write/read single-word transfer by writing all 0s onto the disk.

   To locate and observe the failing DMA, sync the oscilloscope externally from the ADC flip-flop (B21-N) as shown in Figure 6-30. Connect the channel 1 probe to A12-T and observe the resulting waveform (see Figure 6-40).

   If a varying amplitude pulse doublet appears, record the data track. This is an indication that the read/write head is defective.

2. Gain-to-High: Reduce the gain, as described in Section 5.5, and check the slice and DC DOP levels.

3. Disk Plating Inperfections: Although errors can occur on a specific data track and on the DMA, they can be localized to a single bit. To localize the problem, trigger the oscilloscope externally by connecting the channel 1 probe to the ADC flip-flop (B21-N) as shown in Figure 6-30. Connect the channel 1 probe to A12-T (see Figure 6-40) and observe the waveform with disk data set to read a one word transfer on the failing DMA (see Figure 6-33).

   If a stable single-cycle sinusoidal pulse is present, it indicates there is a hole in the magnetic recording surface requiring that the disk be replaced if the amplitude is sufficient to produce an error (refer to Section 5.6).

4. Environment: Alternating line current transients usually cause bit pickups producing random errors. The disk is precisely synchronized to the ac line frequency, thus, periodic errors can be caused by devices such as proportionally controlled heaters.

5. Matrix Failures: Test the G285 and G286 Modules.

B Bit Dropouts

1. Slice-to-High: Perform the procedures outlined in Section 5.6.

2. Gain-to-Low: Perform the procedures outlined in Section 5.6.

3. Plating-Induced Dropout: If dropouts persistently occur in a given Extended Memory Address (EMA) (see Figure 6-34) and Disk Memory Address (DMA) (see Figure 6-33), record all 1s on the disk.

Setup the oscilloscope as indicated in Section 5.8.6, Step A3, and observe the amplitude level. A sudden decrease of 50% or less (several bits in length) in the amplitude, indicates a dropout on the disk surface. If the dropout is below 1.8V peak-to-peak, the disk must be replaced.

5.8.7 G085 Module Identification

The dynamic range of the amplifier section of the G085 Amplifier Module is increased in revision D and later modules. Revision B modules can be modified to permit the increased range. On revised modules or on D or later modules, the analog signal output from Section A, pins T and U, must be less than 12V peak-to-peak. Older or unmodified modules are limited to 9V peak-to-peak. Revised B level modules can be identified by 1500 pf capacitors C11 and C12.

Chapter 6
Module Circuit Schematics

6.1 INTRODUCTION

The module schematic diagrams in this Chapter pertain to the modules used in the RF08 Disk Control and the RS08 Disk. Table 6-1 and 6-2 lists the modules and the quantity of each used in the System.

Figures 6-28 to 6-37 are the Block Schematics for the RF08 Disk Control, and Figures 6-38 to 6-43 are the Block Schematics for the RS08 Disk.

Table 6-1
Modules Used in the RF08 Disk Control

Figure	Module Type	Quantity	Description	Drawing Number
6-1	B133	8	Diode Gate	B-CS-B133-0-1
6-2	B134	3	Diode Gate	B-CS-B134-0-1
6-3	B135	4	Diode Gate	B-CS-B135-0-1
6-4	B137	1	Diode Gate	B-CS-B137-0-1
6-5	B165	11	Diode Inverter	B-CS-B165-0-1
6-6	B212	5	Dual RS Flip-Flop	C-CS-B212-0-1
6-7	B310	3	Delay Line	A-RS-B-310
6-8	B311	1	Tapped Delay Line	B-CS-B311-0-1
6-9	B312	1	Diode Gate	B-CS-B312-0-1
6-10	B611	1	Pulse Amplifier	B-CS-B611-0-1
6-11	B683	8	Bus Driver	B-CS-B683-0-1
6-12	S123	10	Diode Gate	B-CS-S123-0-1
6-13	S202	8	Dual Flip-Flop	B-CS-S202-0-1
6-14	S203	7	Triple Flip-Flop	B-CS-S203-0-1
6-15	S206	18	Dual Flip-Flop	B-CS-S206-0-1
6-16	W103	8	Device Selector	C-CS-W103-0-1

Table 6-2
Modules Used in the RS08 Disk

Figure	Module Type	Quantity	Description	Drawing Number
6-1	B133	2	Diode Gate	B-CS-B133-0-1
6-2	B134	1	Diode Gate	B-CS-B134-0-1
6-3	B135	1	Diode Gate	B-CS-B135-0-1
6-4	B137	1	Diode Gate	B-CS-B137-0-1
6-17	B152	3	Binary-to-Octal Decoder	B-CS-B152-0-1
6-5	B165	2	Diode Inverter	B-CS-B165-0-1
6-18	B172	1	Diode Gate	B-CS-B172-0-1
6-6	B212	2	Dual RS Flip-Flop	B-CS-B212-0-1
6-19	B301	3	Delay One-Shot	B-CS-B301-0-1
6-9	B312	1	Diode Gate	B-CS-B312-0-1
6-10	B611	1	Pulse Amplifier	B-CS-B611-0-1
6-11	B683	2	Bus Driver	B-CS-B683-0-1
6-20	G085	4	Disk Read Amp and Slice	B-CS-G085-0-1
6-21	G284	1	Disk Writer	B-CS-G284-0-1
6-22	G285	4	Series Switch	B-CS-G285-0-1
6-23	G286	4	Centertop Selector	B-CS-G286-0-1
6-24	R002	1	Diode Cluster	B-CS-R002-0-1
6-25	R111	1	Diode Gate	B-CS-R111-0-1
6-26	R302	1	Delay	B-CS-R302-0-1
6-27	R303	1	Integrating One-Shot	B-CS-R303-0-1
6-15	S206	1	Dual Flip-Flop	B-CS-S206-0-1

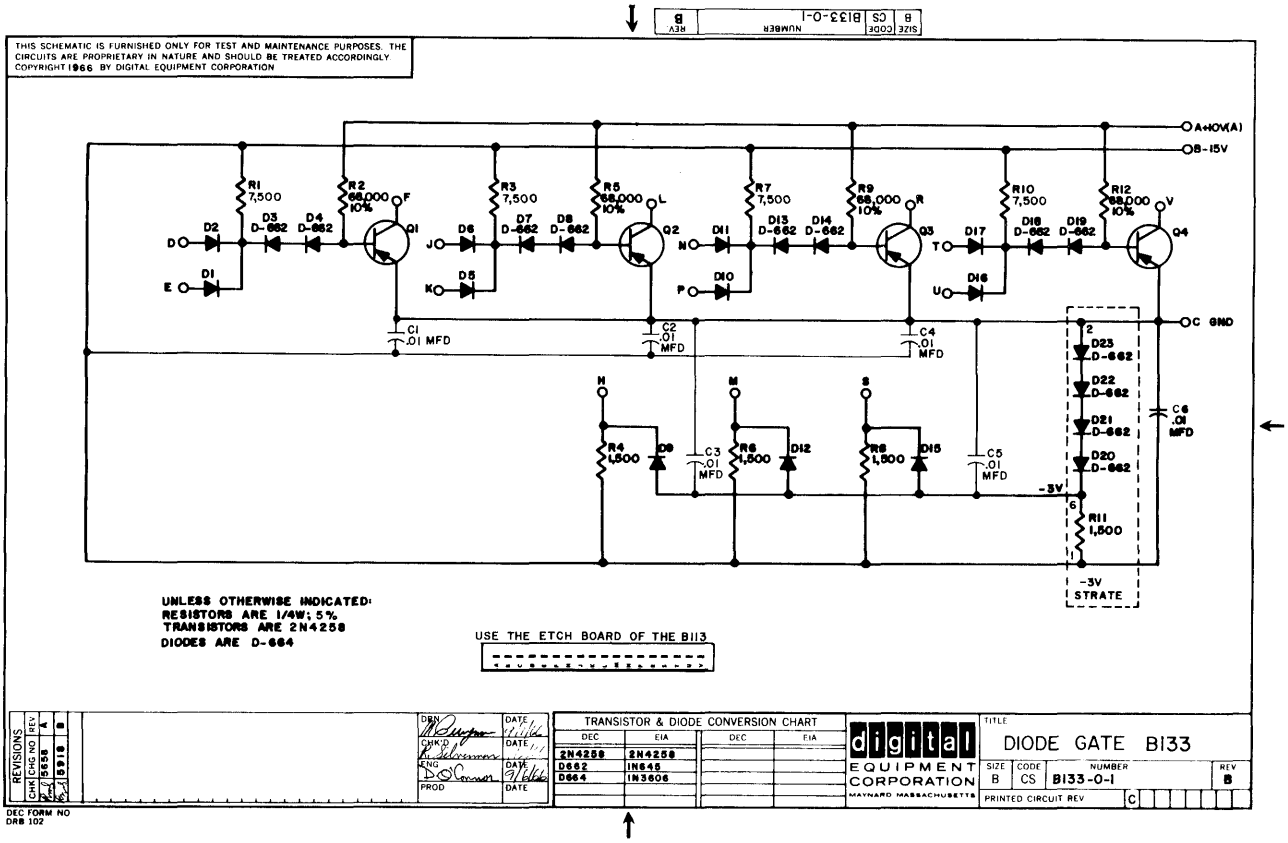


Figure 6-1 Diode Gate B133

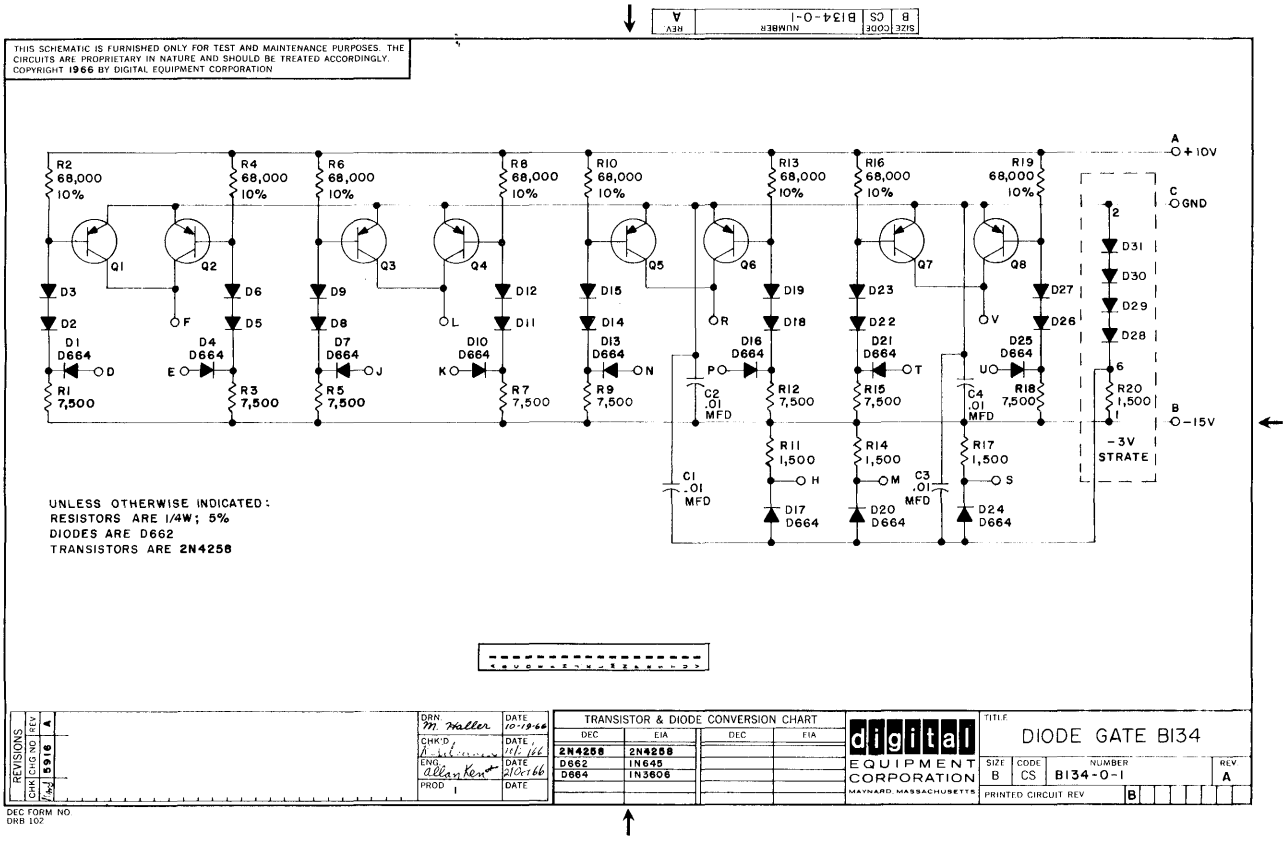


Figure 6-2 Diode Gate B134

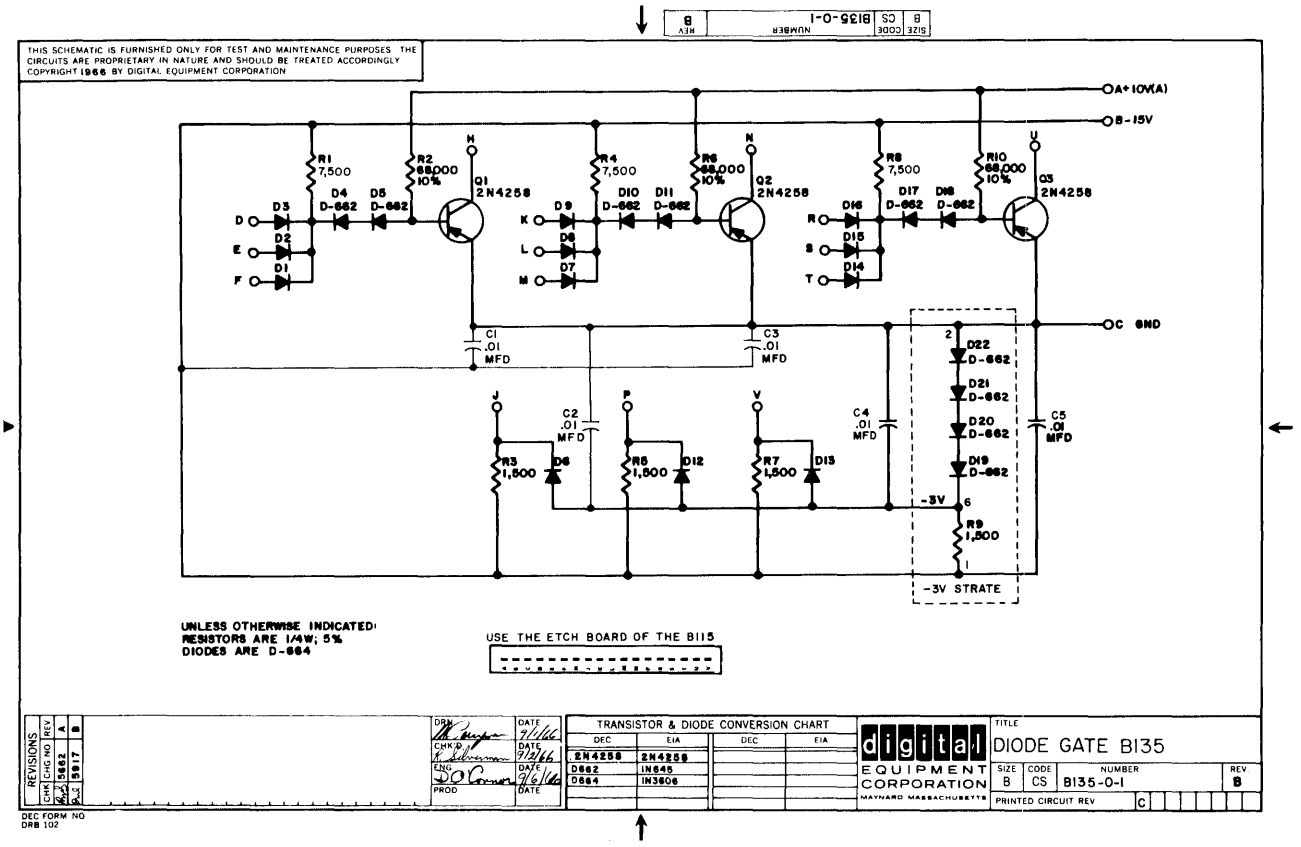


Figure 6-3 Diode Gate B135

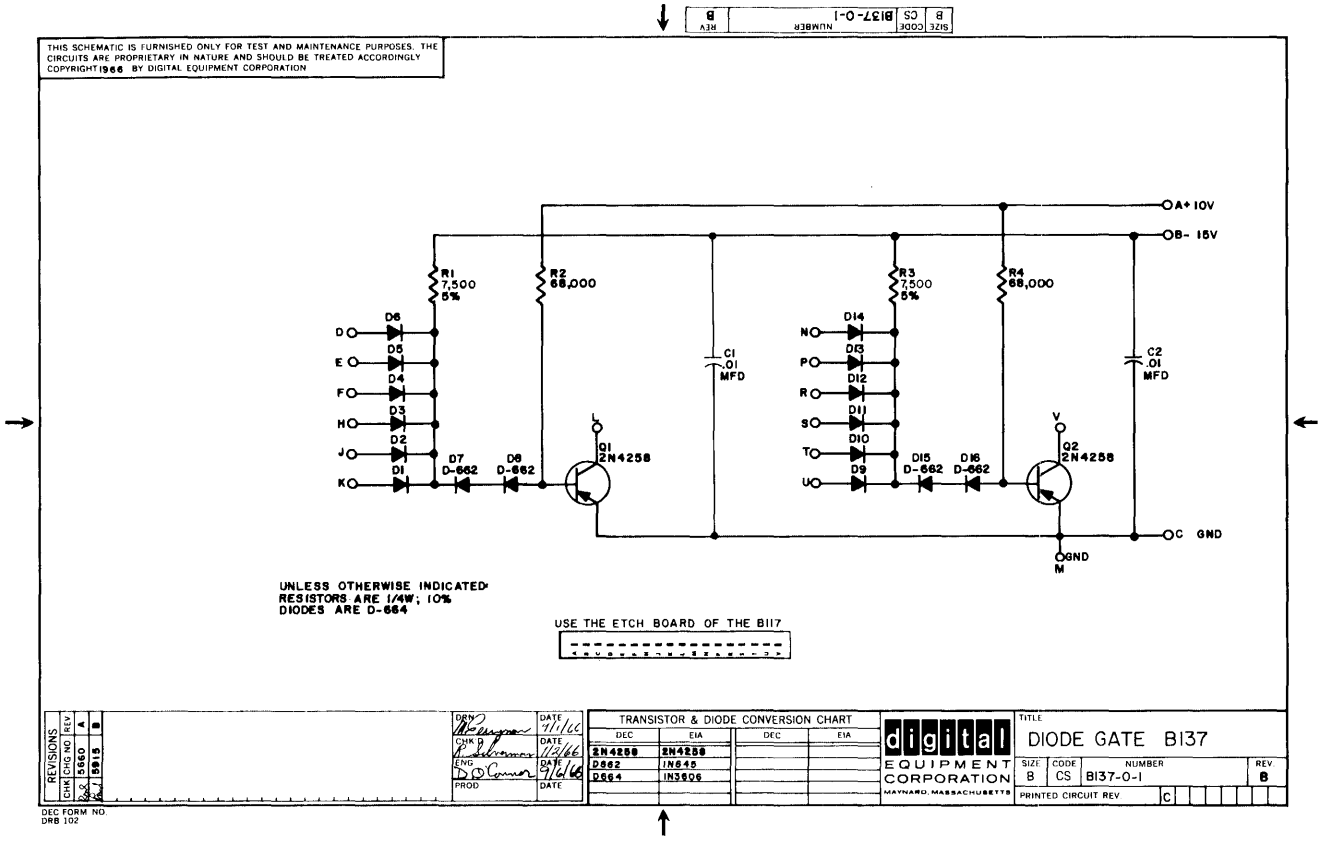


Figure 6-4 Diode Gate B137

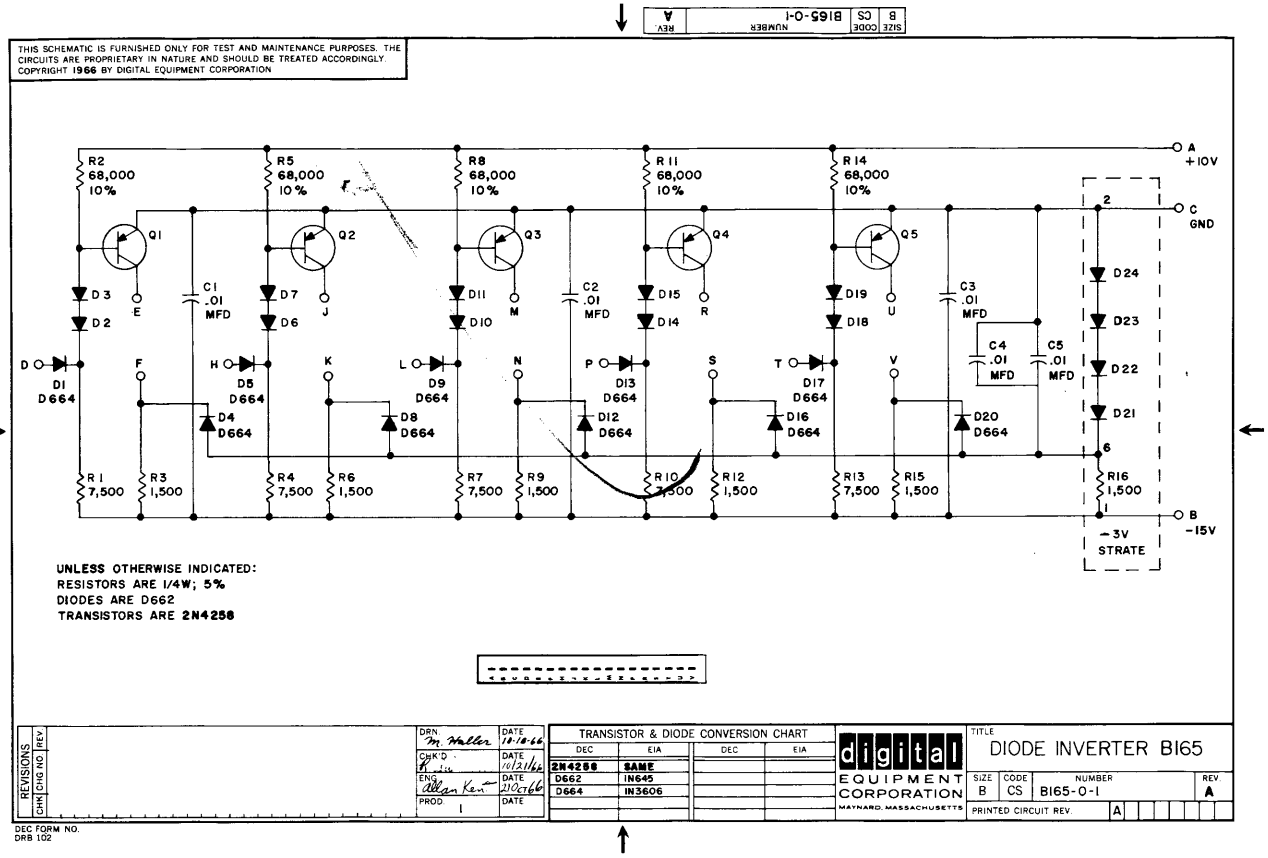


Figure 6-5 Diode Inverter B165

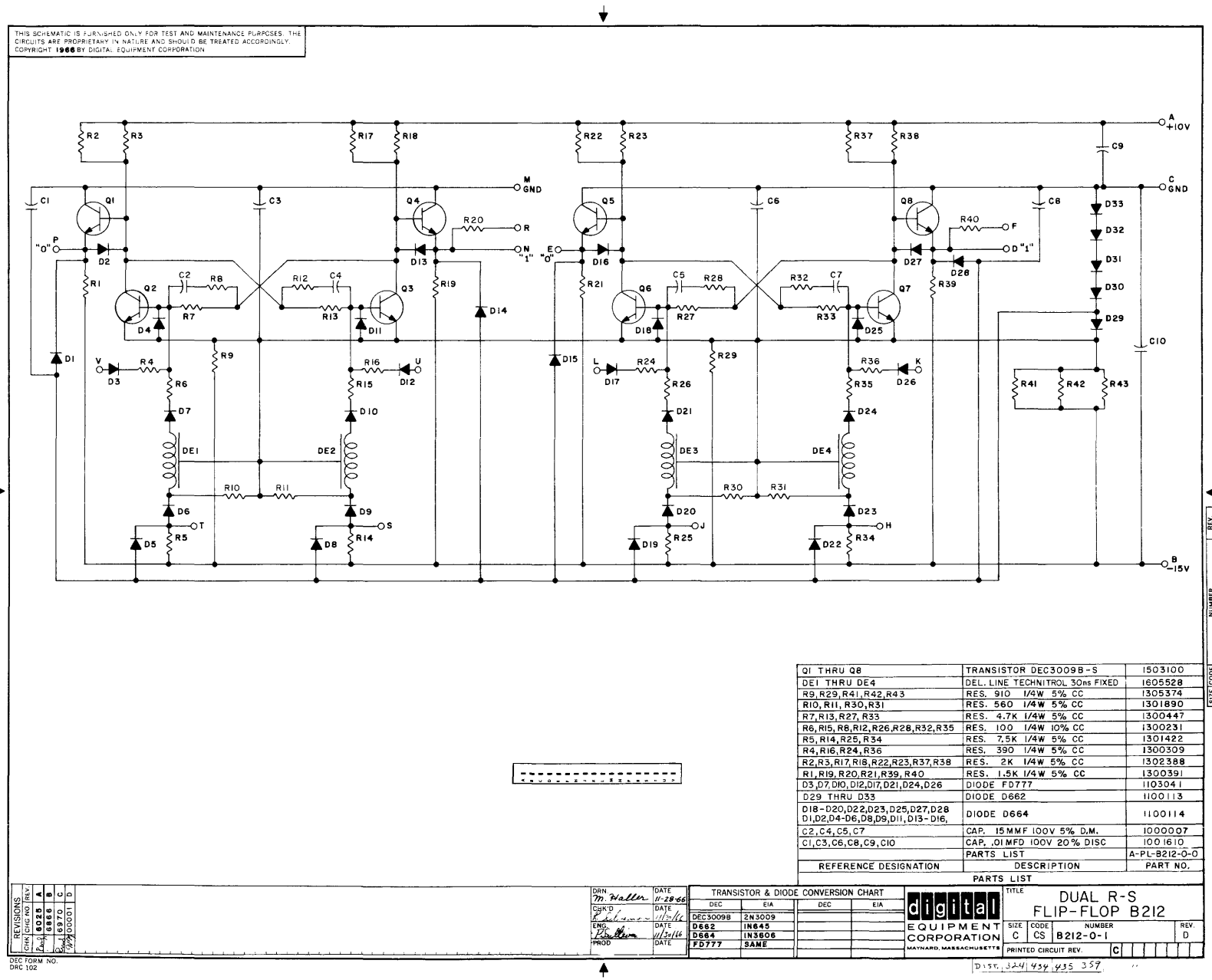


Figure 6-6 Dual RS Flip-Flop B212

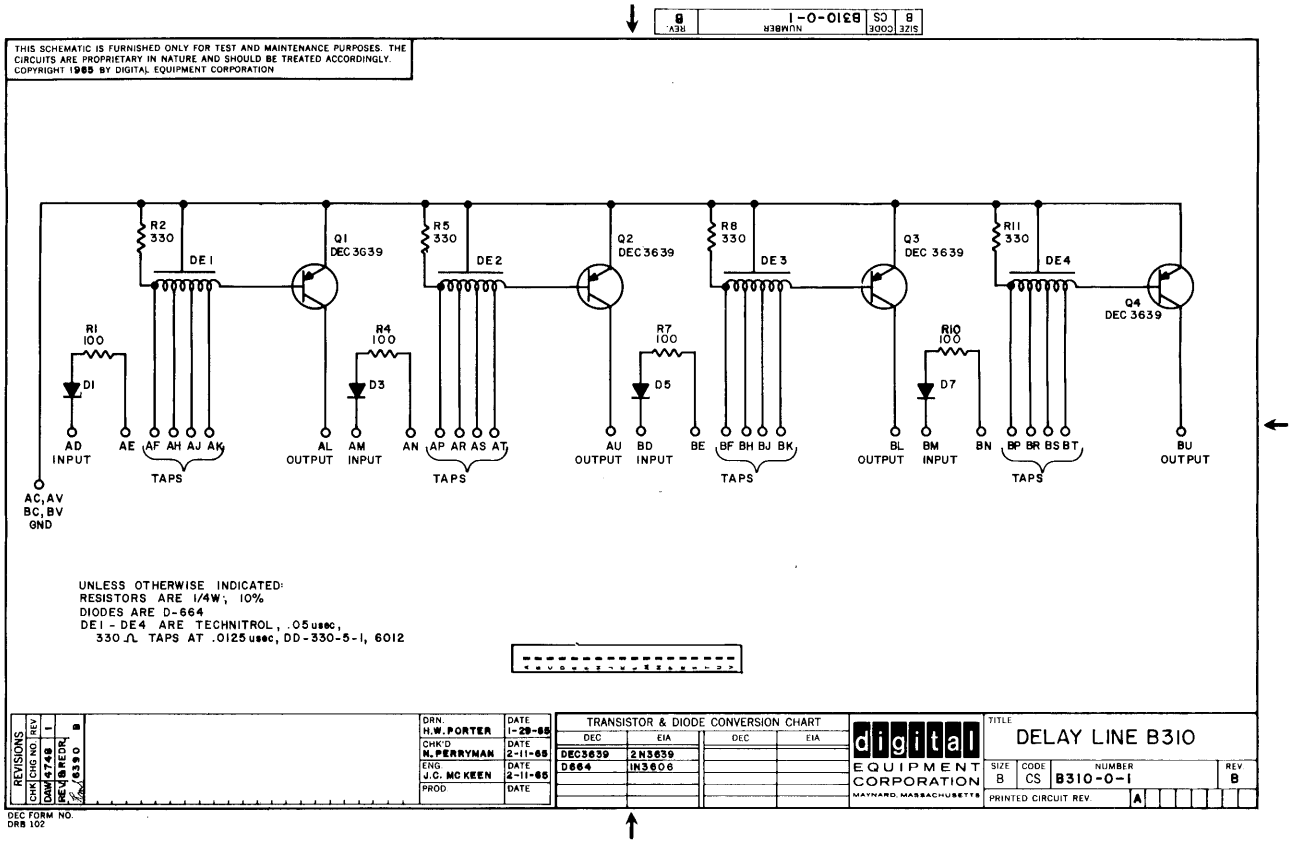


Figure 6-7 Delay Line B310

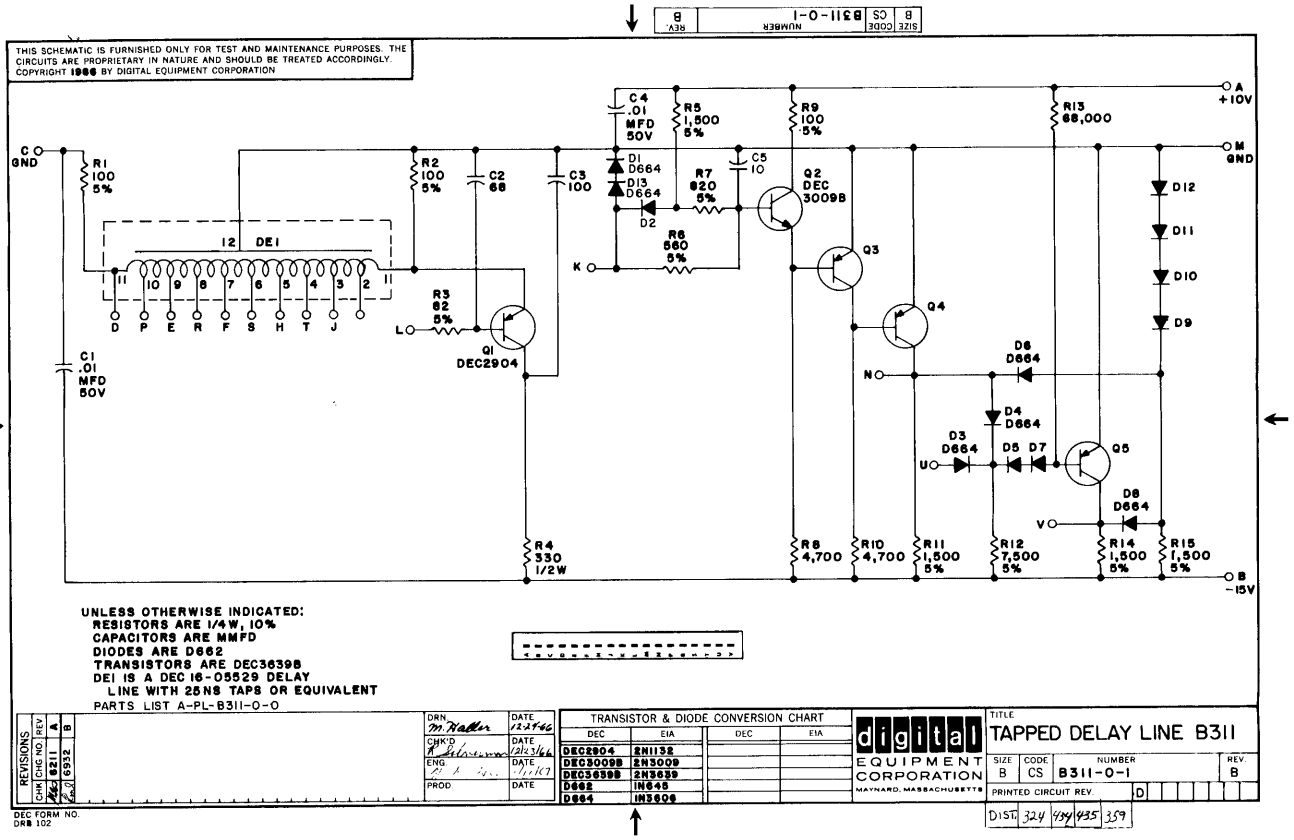


Figure 6-8 Tapped Delay Line B311

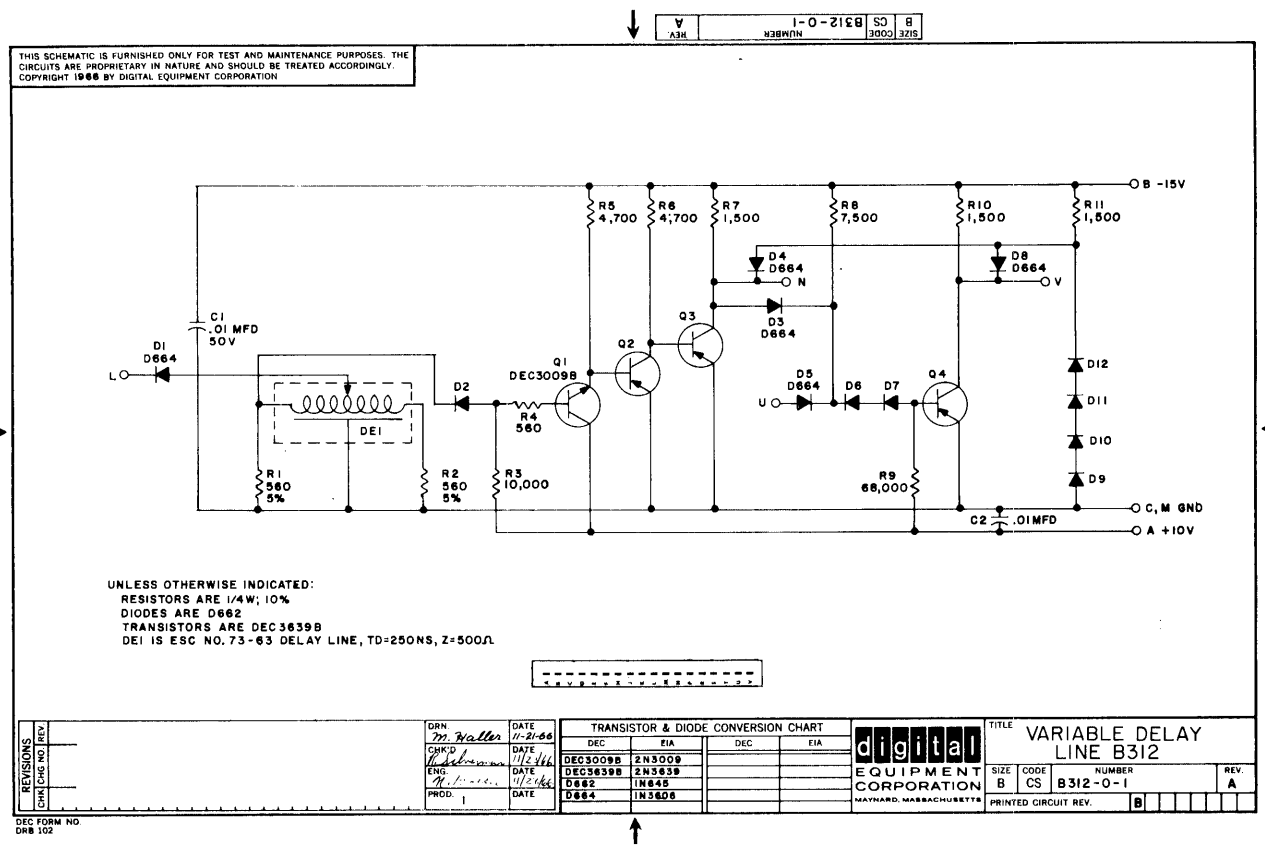


Figure 6-9 Variable Delay Line B312

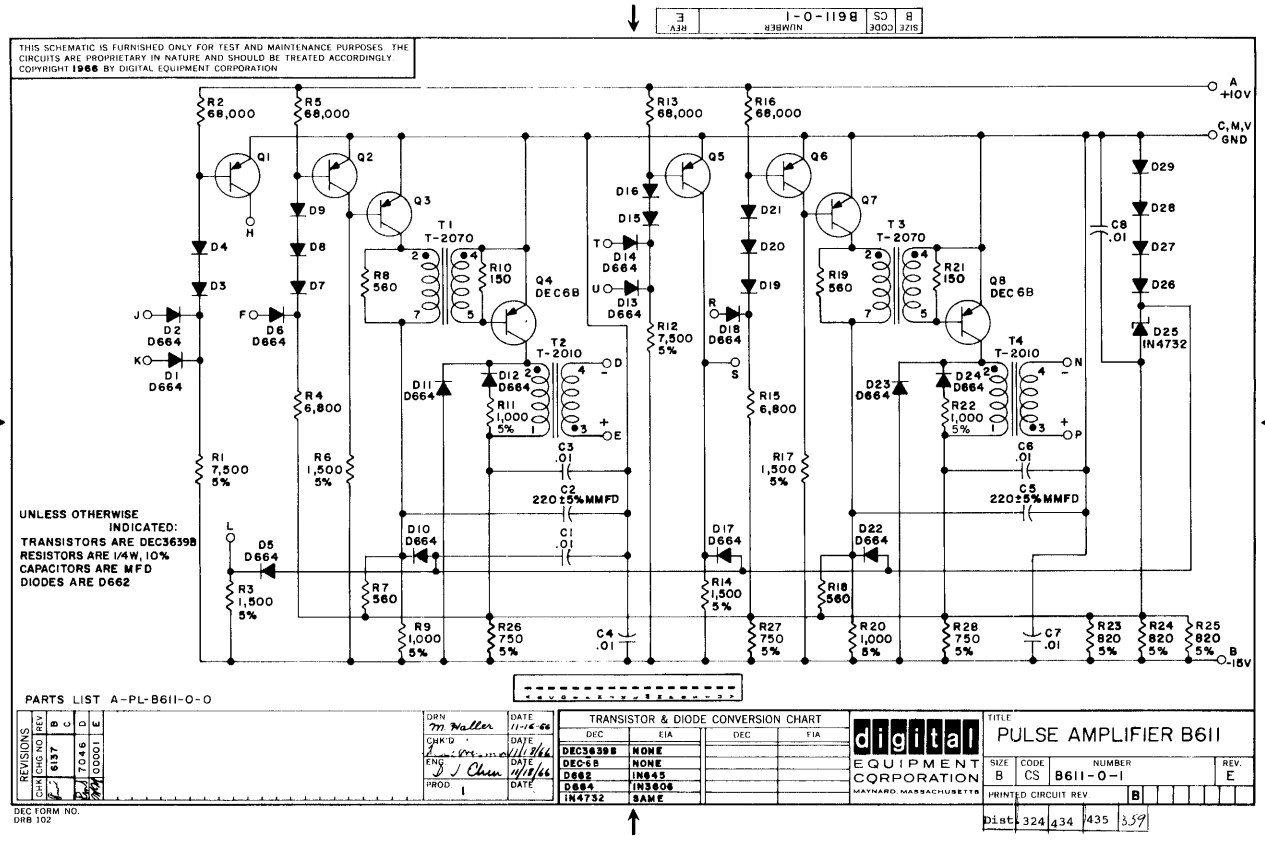


Figure 6-10 Pulse Amplifier B611

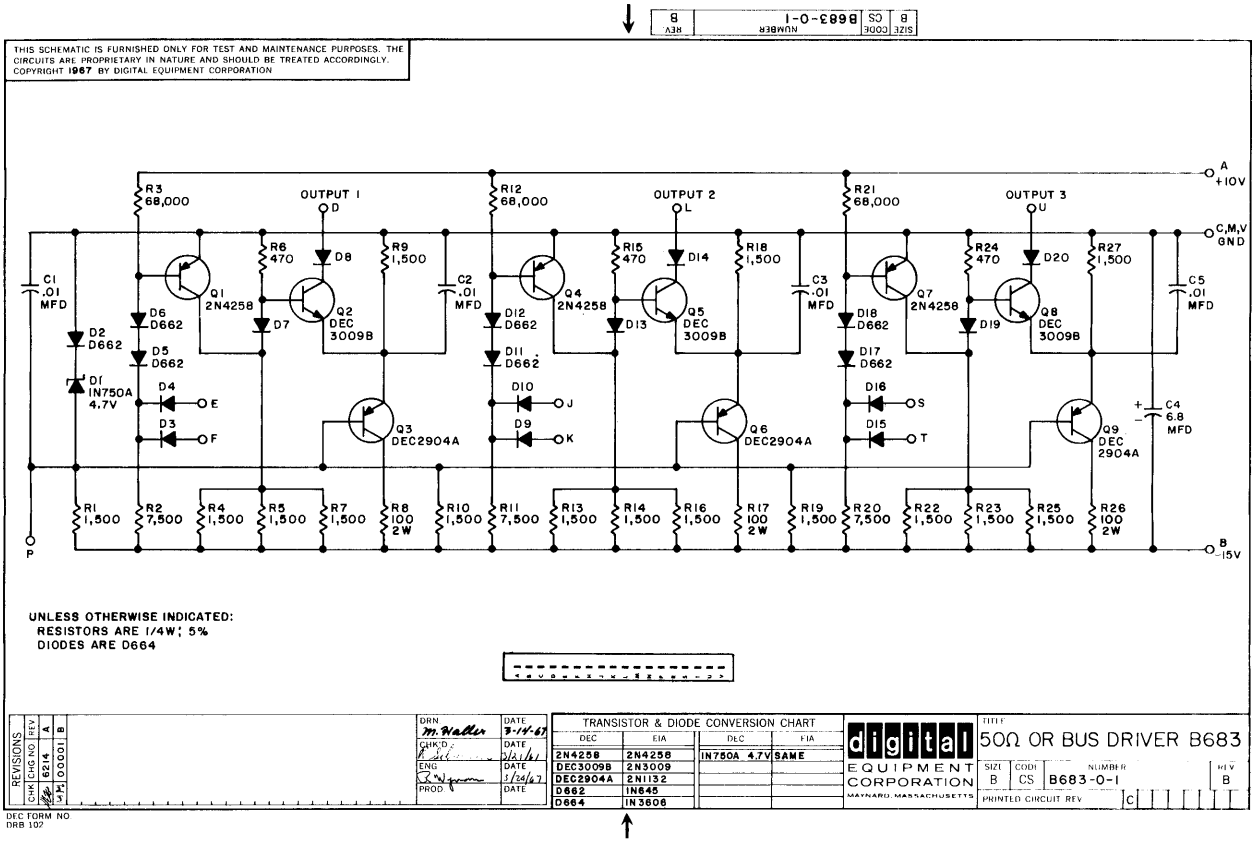


Figure 6-11 50Ω OR Bus Driver B683

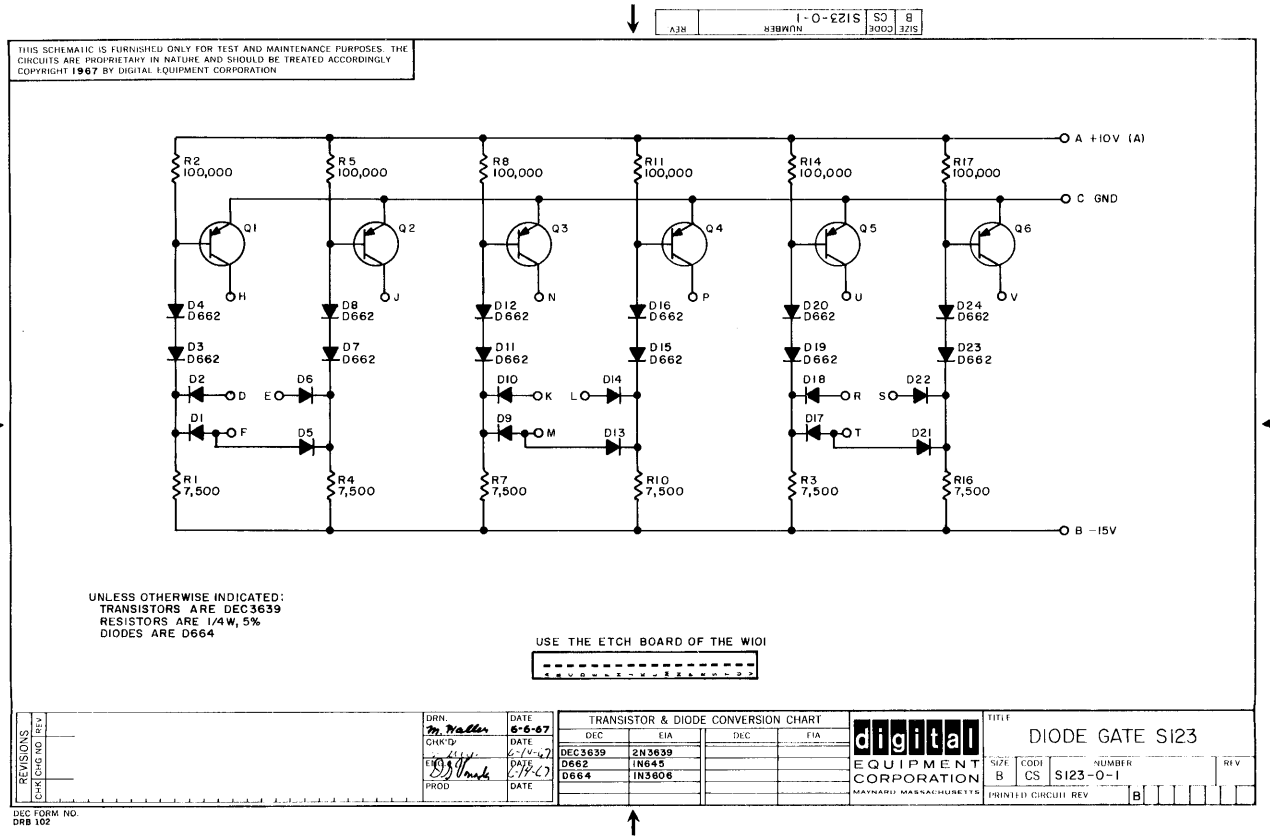


Figure 6-12 Diode Gate S123

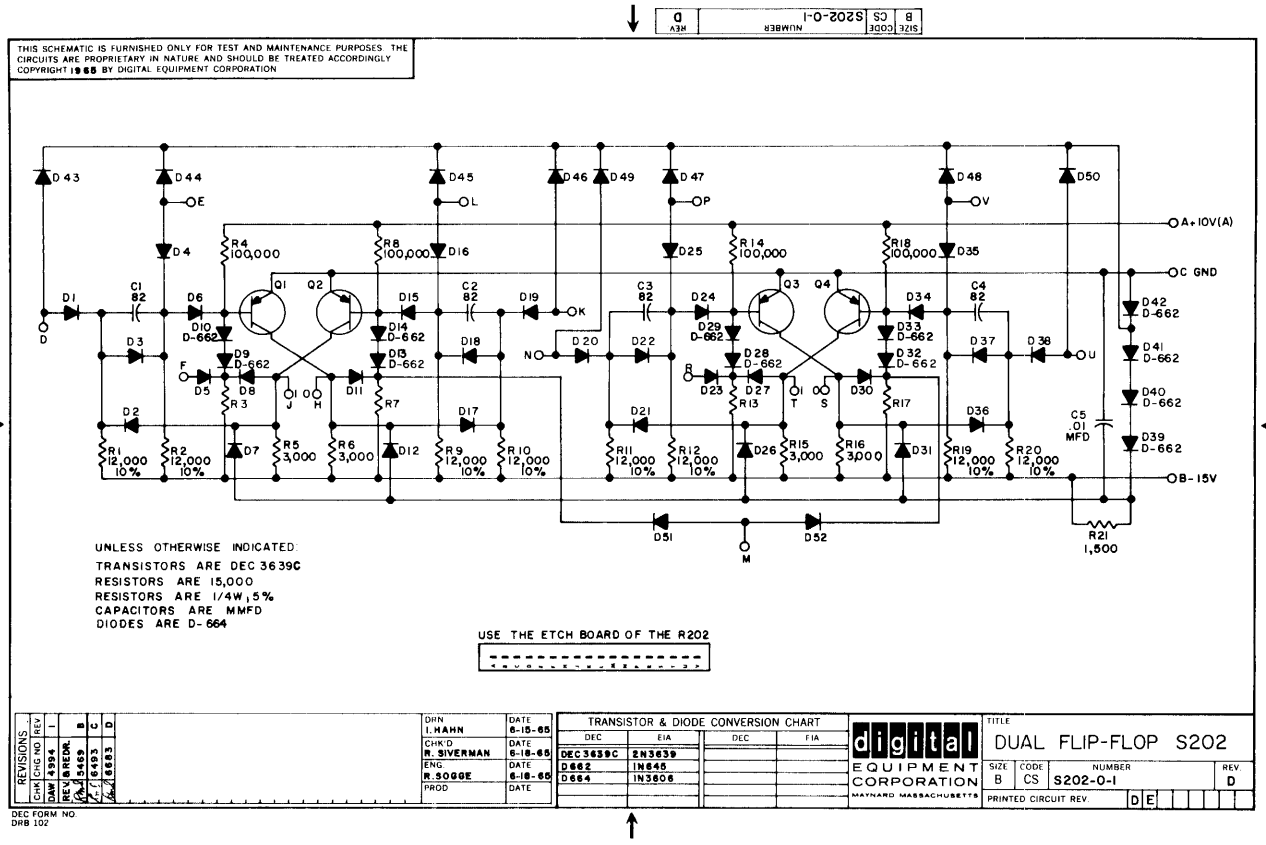


Figure 6-13 Dual Flip-Flop S202

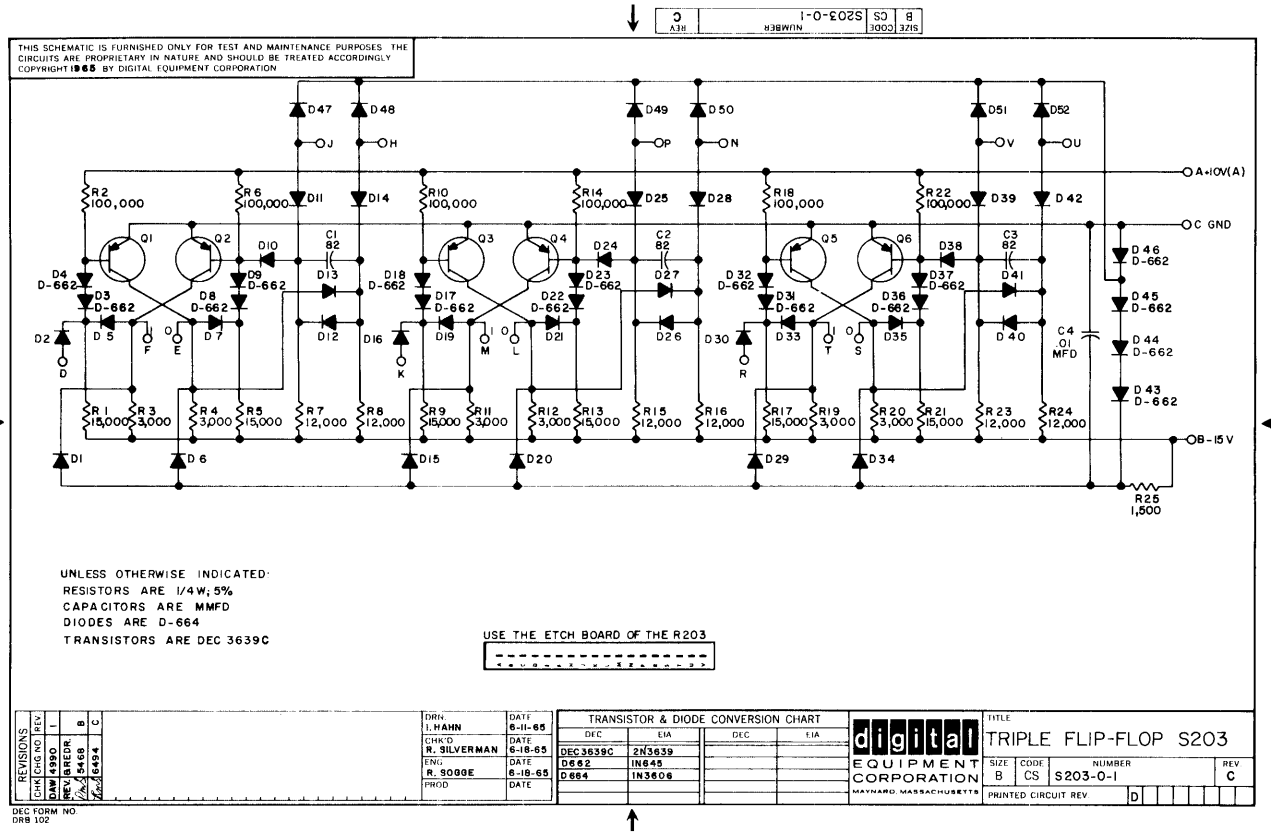


Figure 6-14 Triple Flip-Flop S203

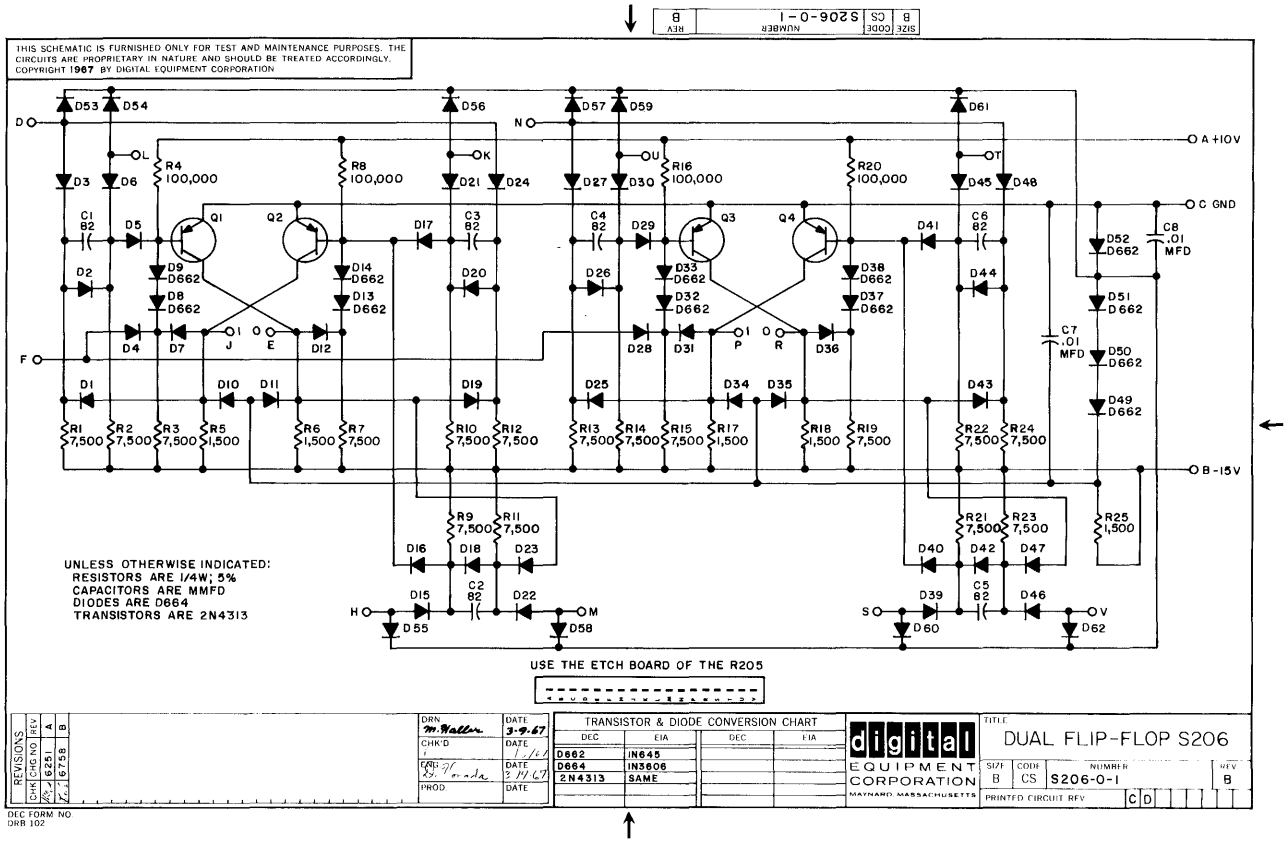


Figure 6-15 Dual Flip-Flop S206

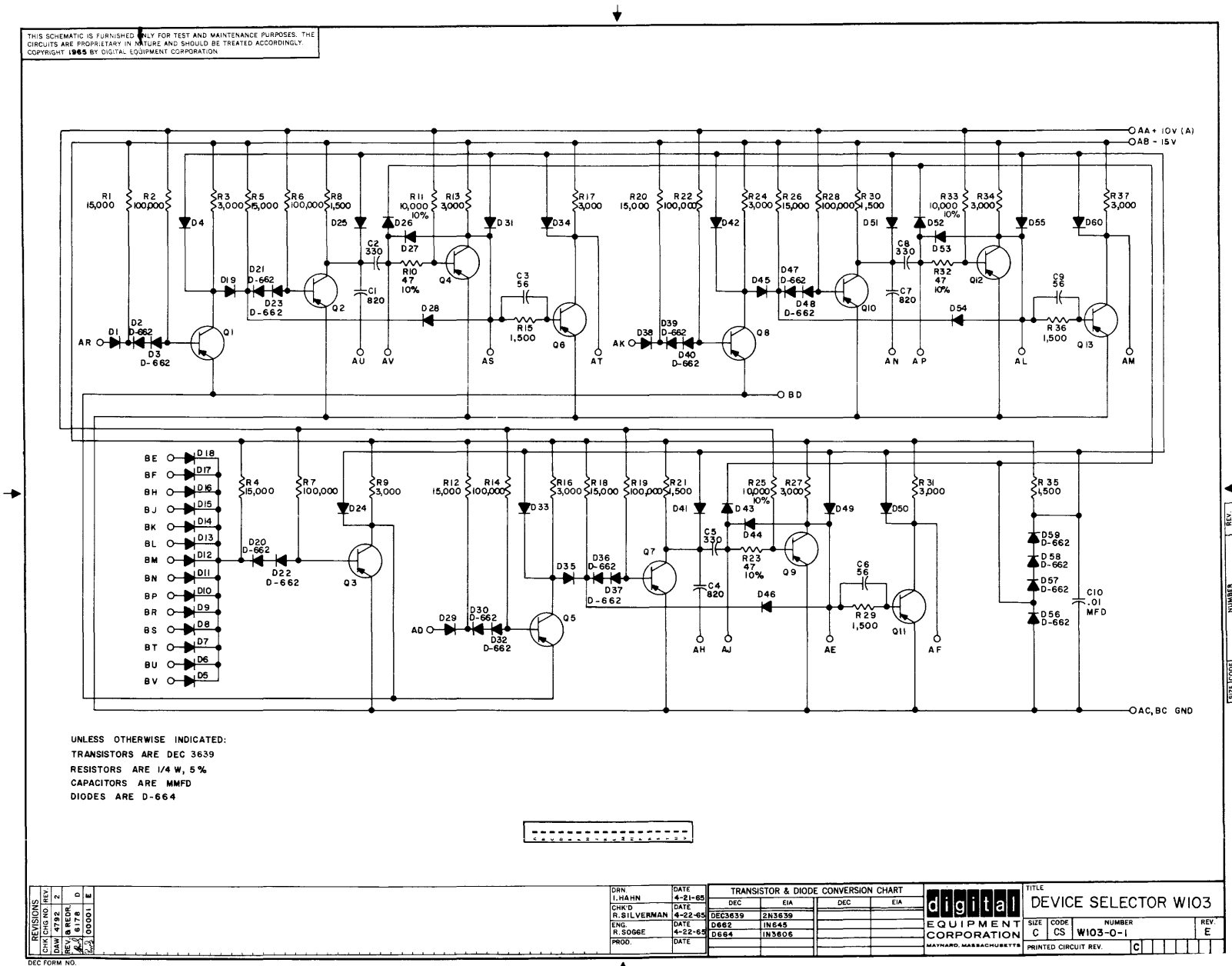


Figure 6-16 Device Selector W103

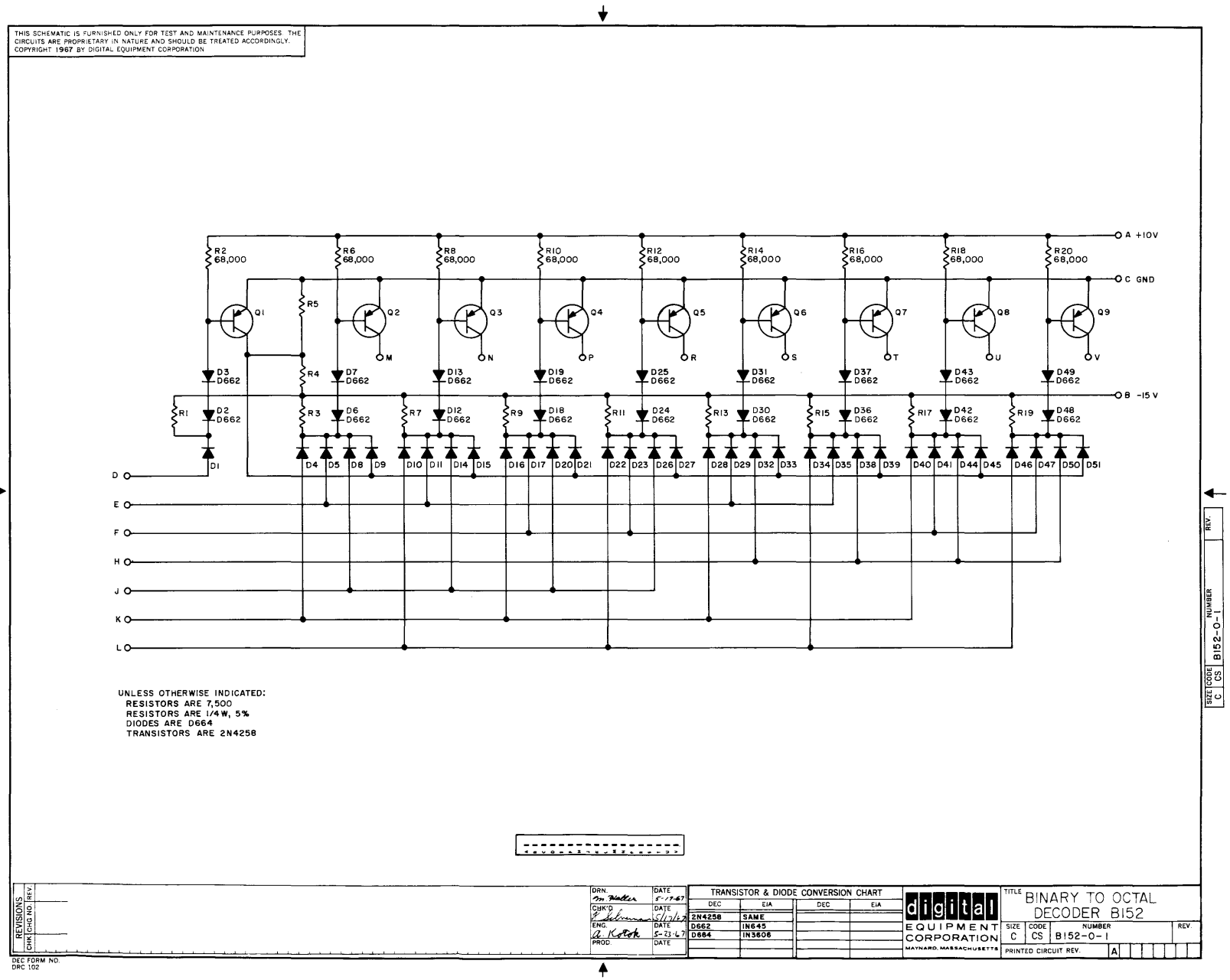


Figure 6-17 Binary-To-Octal Decoder B152

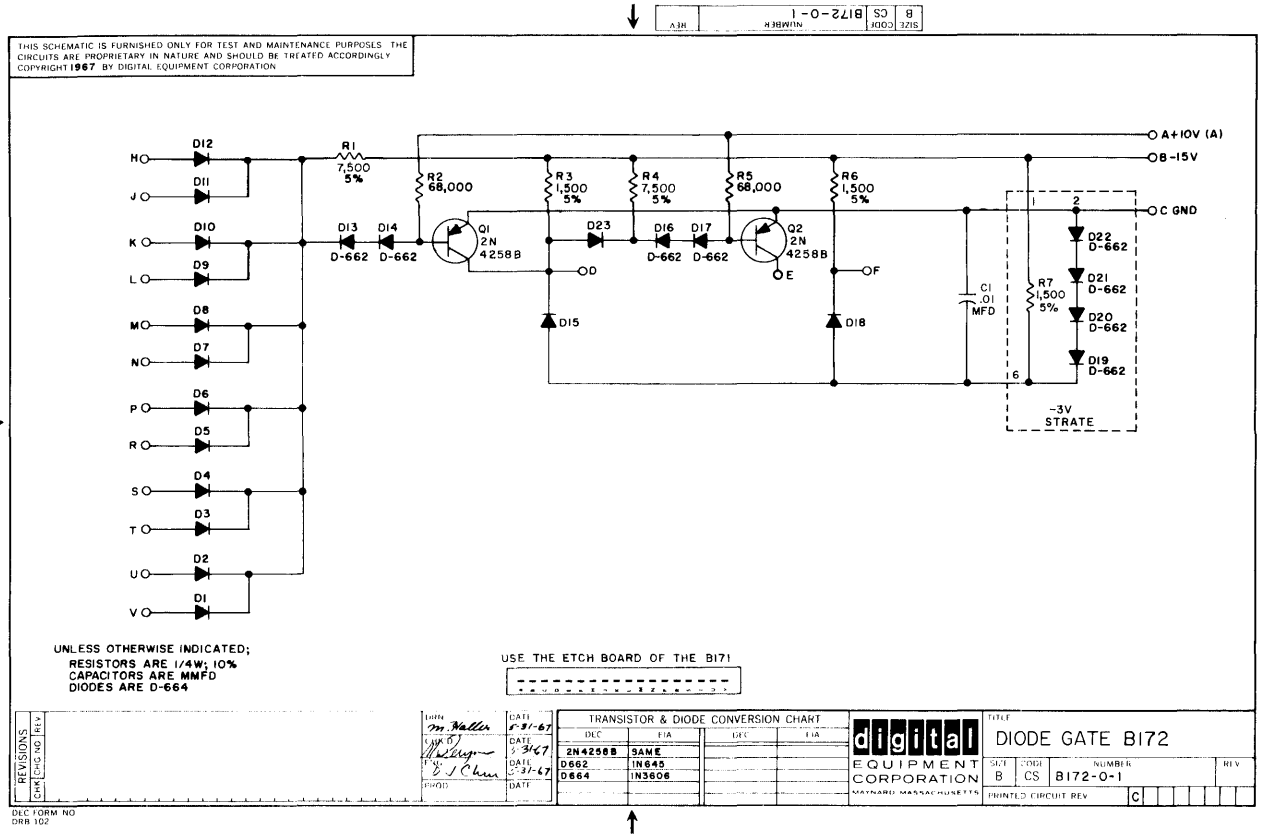


Figure 6-18 Diode Gate B172

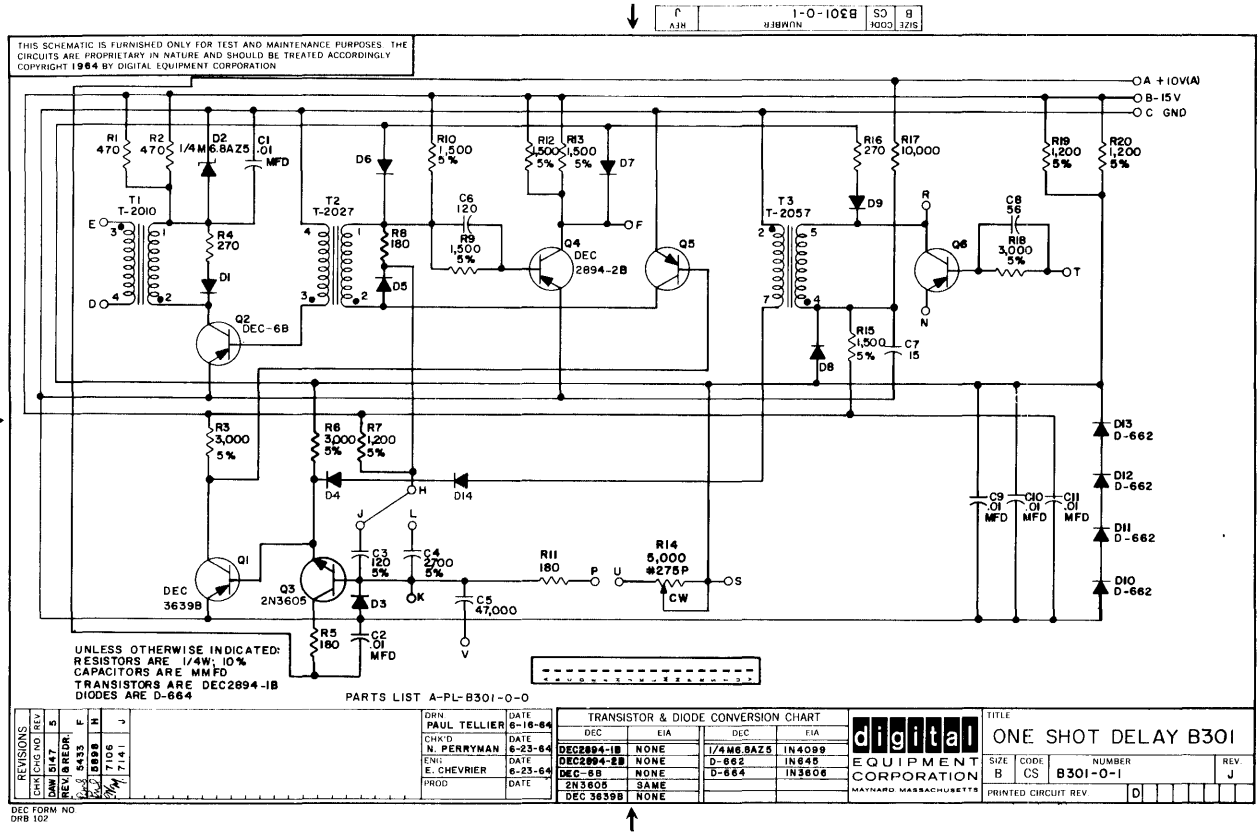


Figure 6-19 One-Shot Delay B301

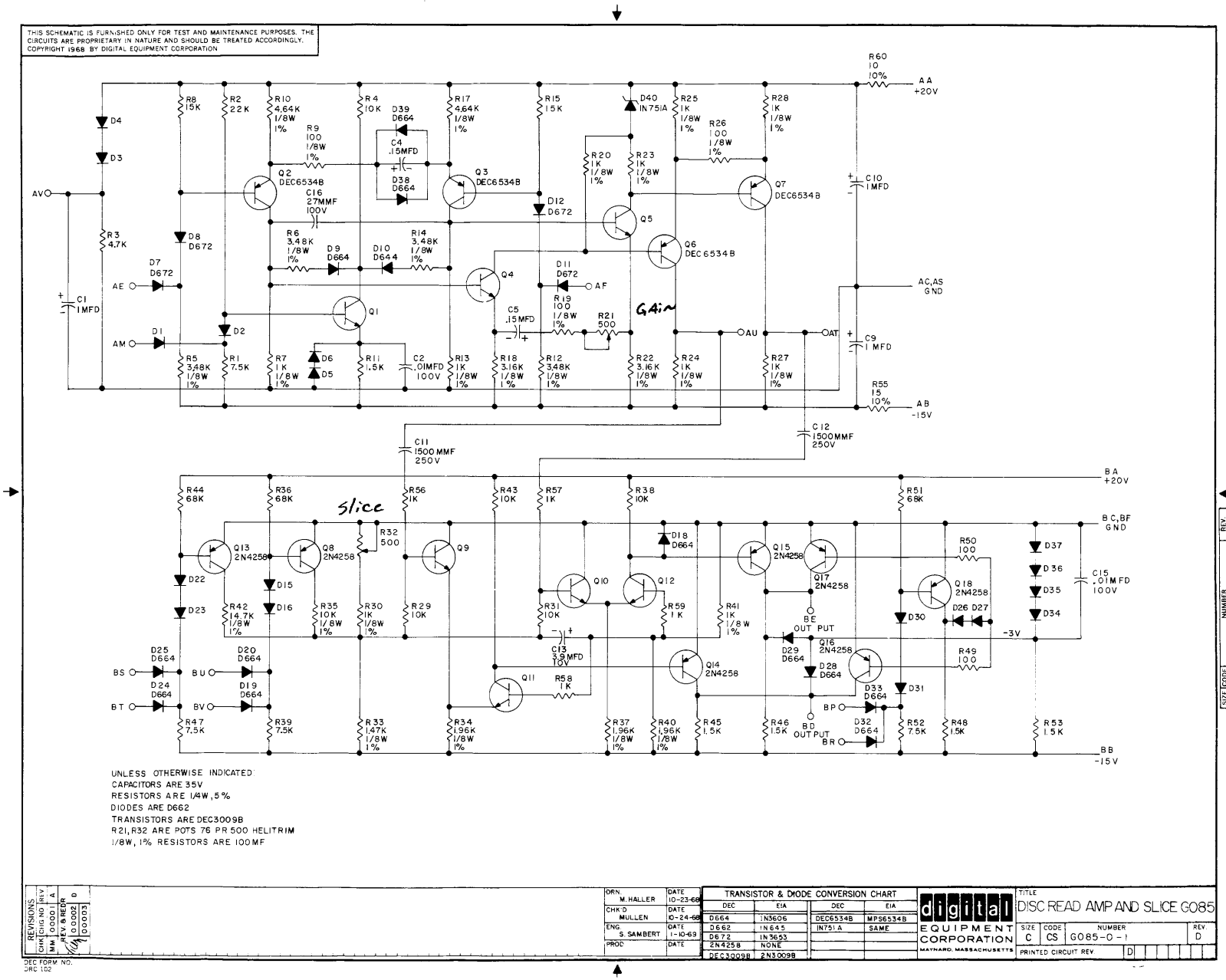


Figure 6-20 Disk Read Amp and Slice G085

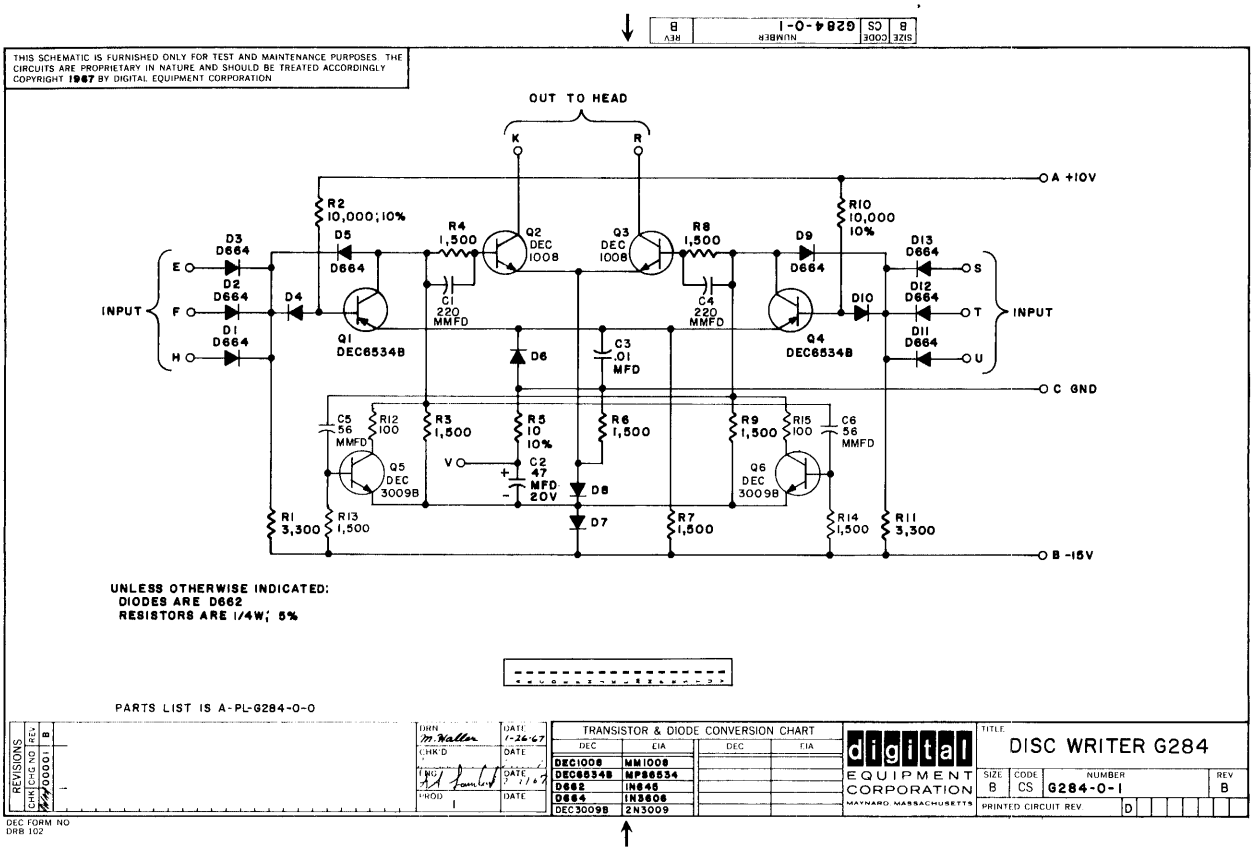


Figure 6-21 Disk Writer G284

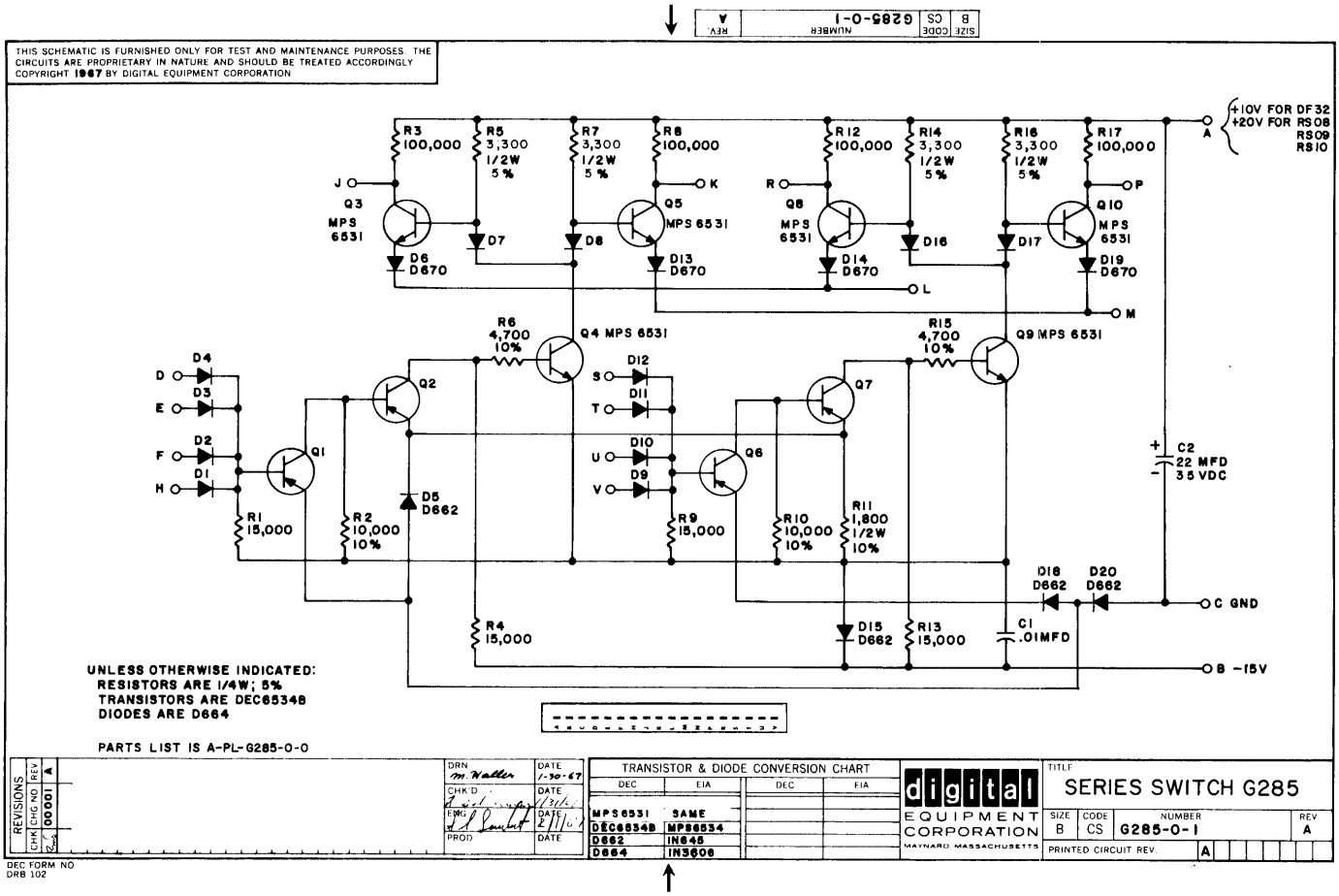


Figure 6-22 Series Switch G285

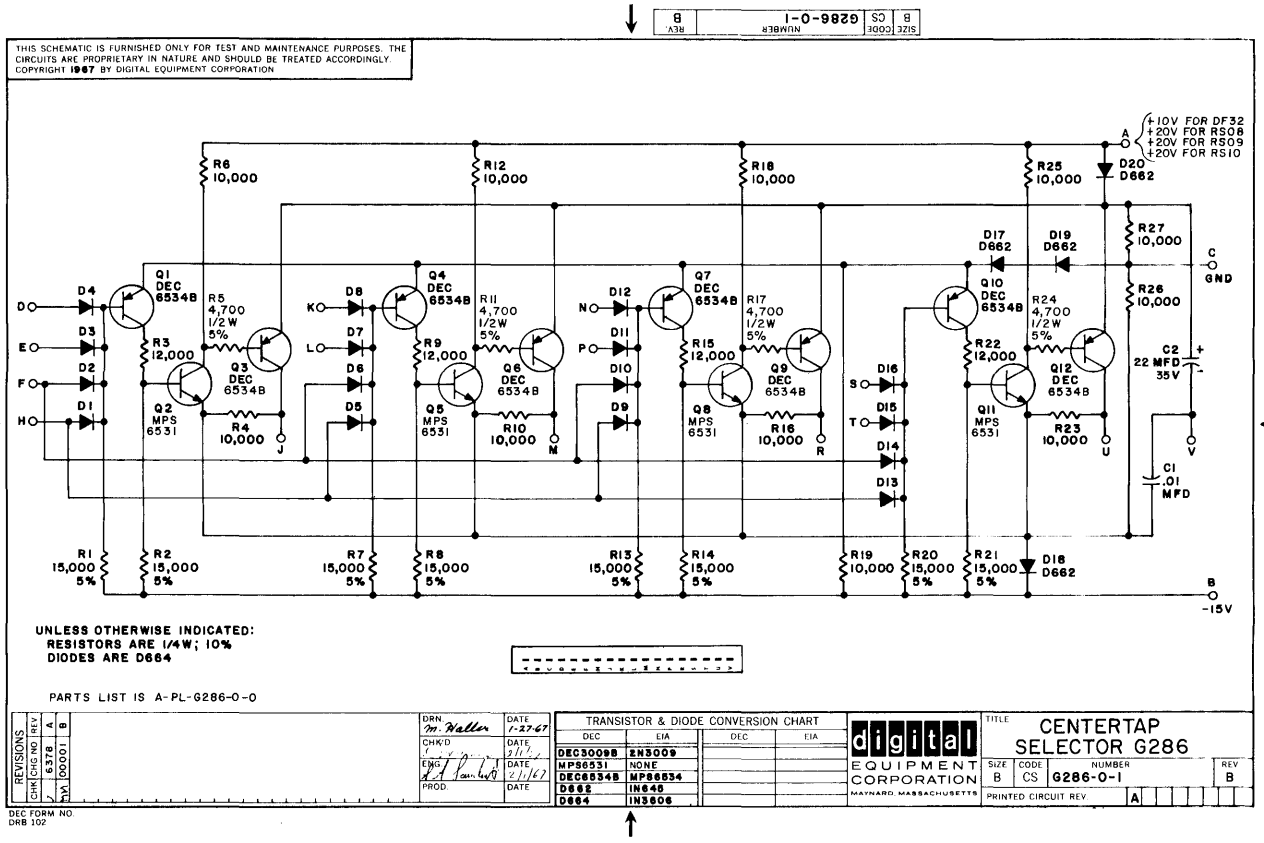


Figure 6-23 Centertap Selector G286

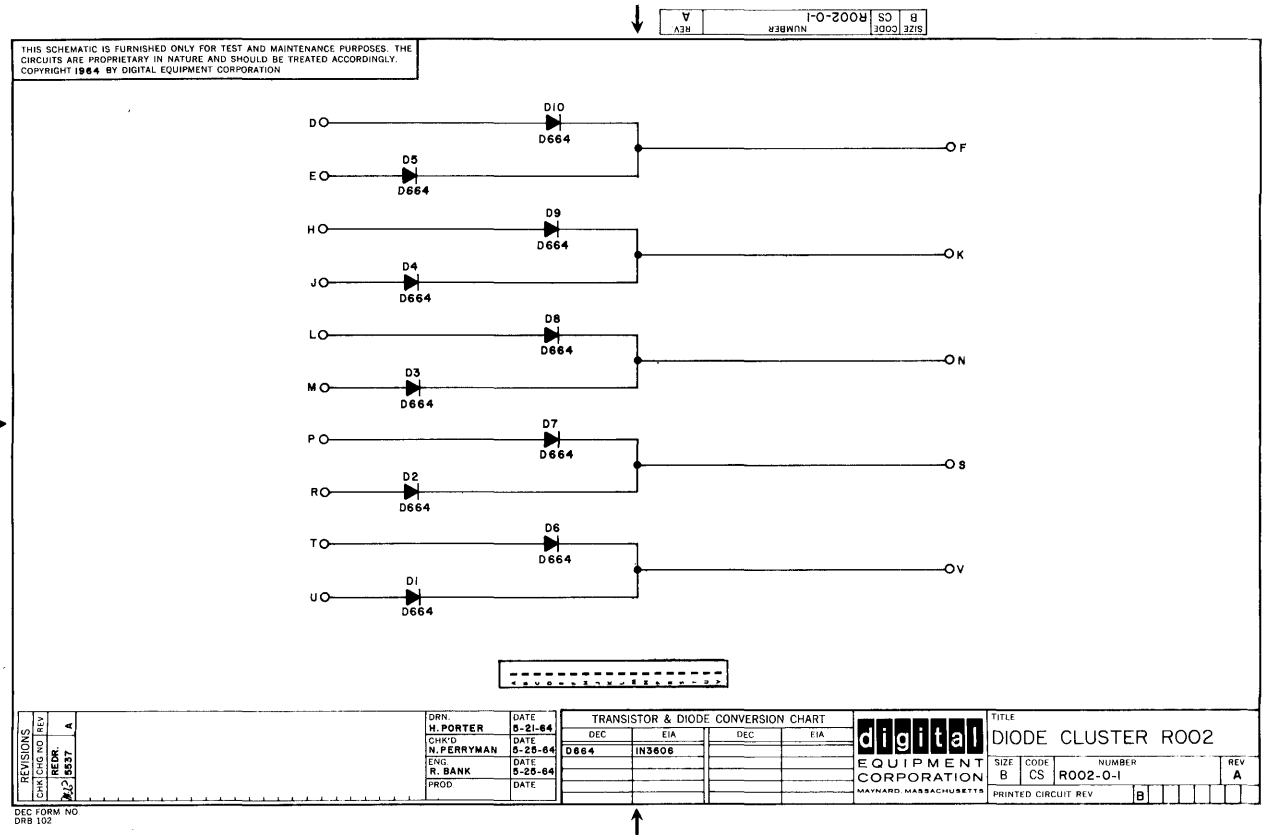


Figure 6-24 Diode Cluster R002

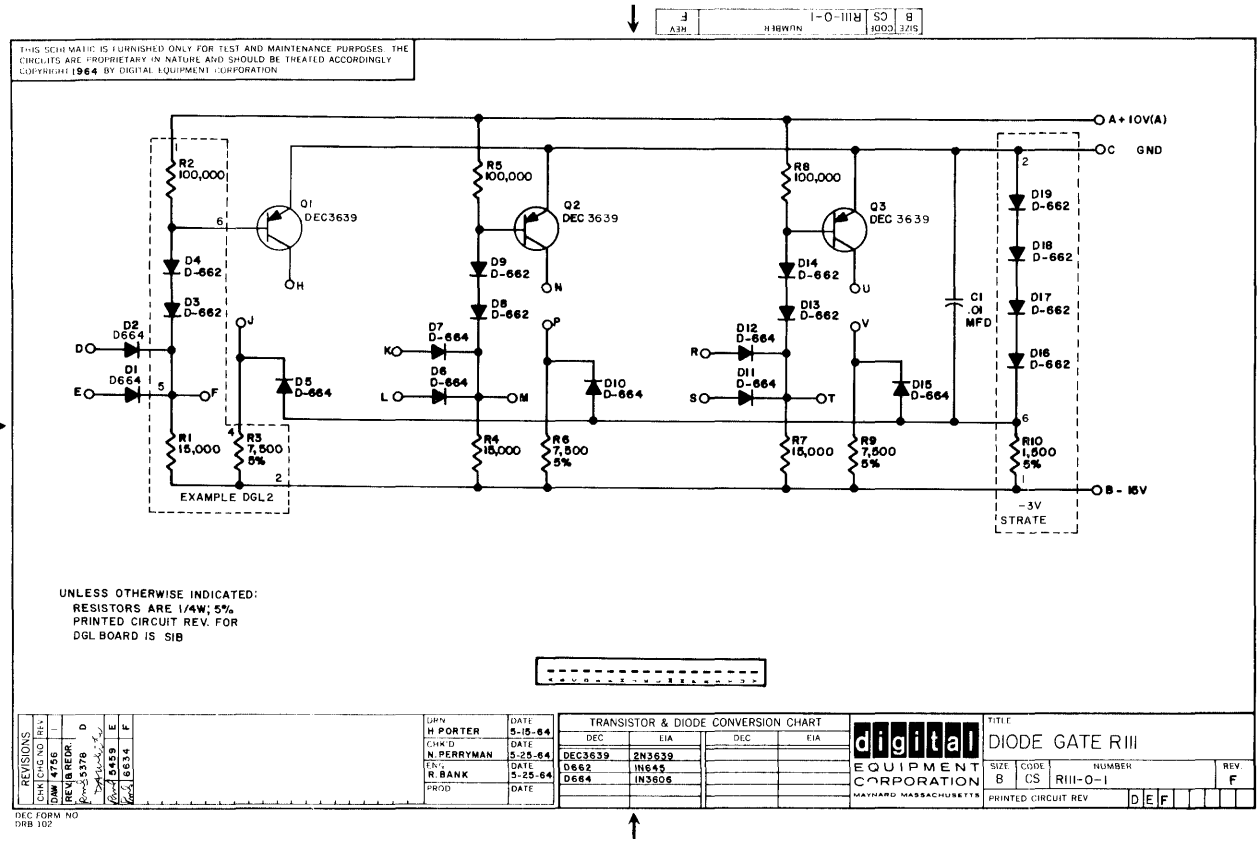


Figure 6-25 Diode Gate R111

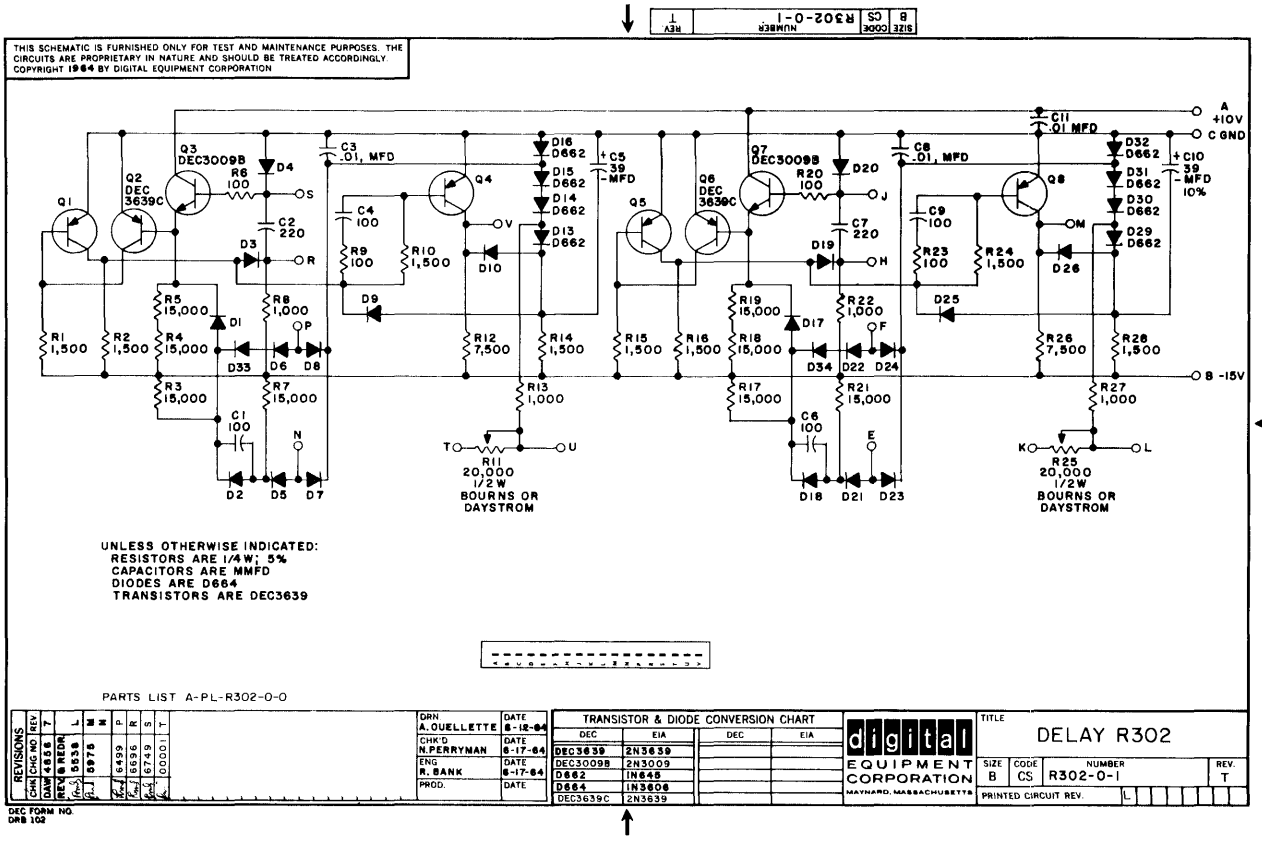


Figure 6-26 Delay R302

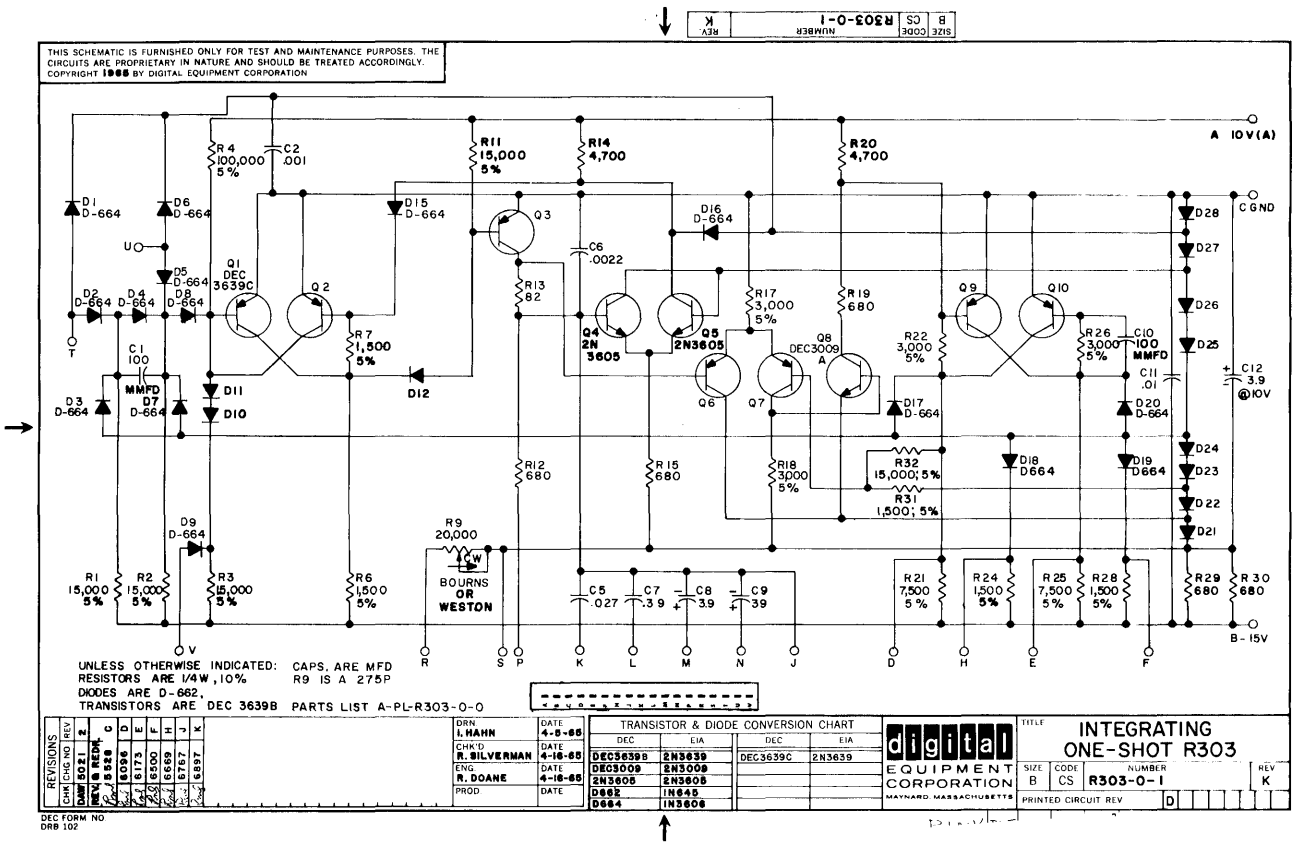
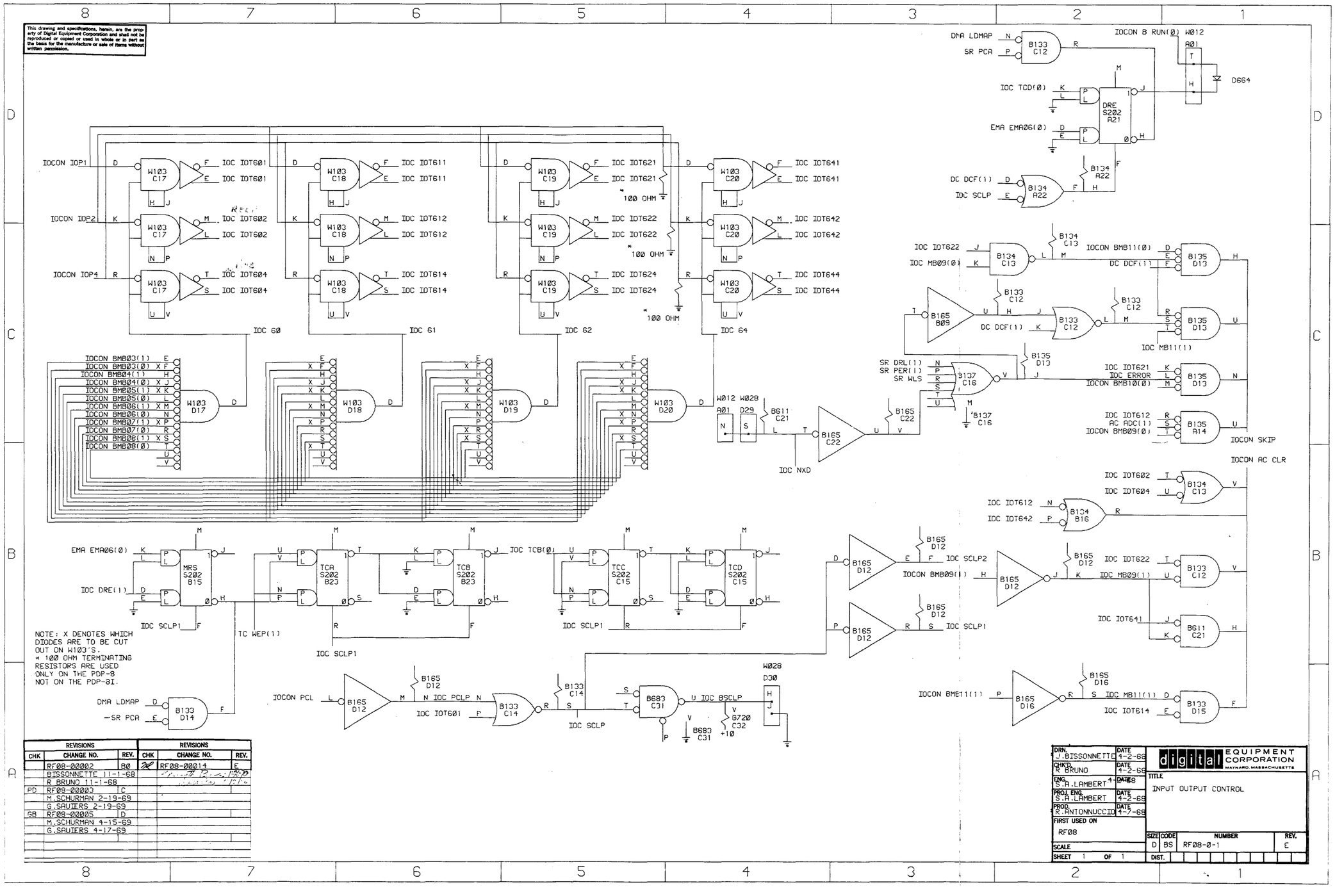


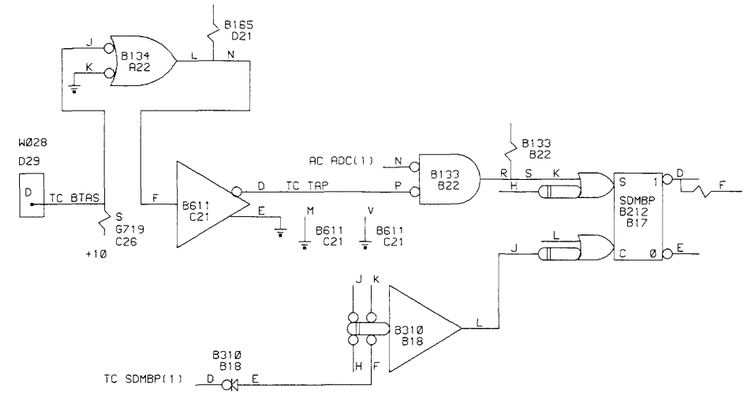
Figure 6-27 Integrating One-Shot R303

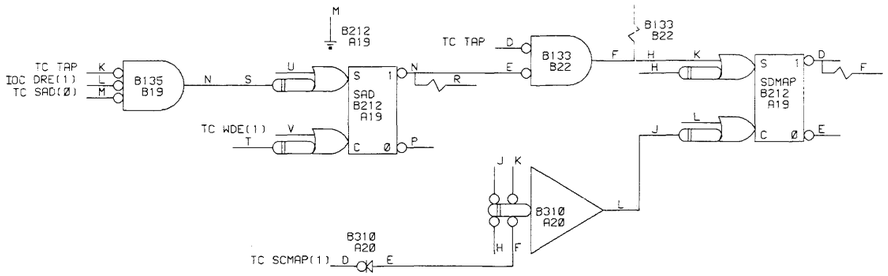


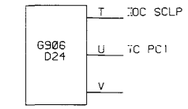
REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF08-00002	B0		RF08-00014	E
	BISSONNETTE 11-1-68				
	R.BRUNO 11-1-68				
PD	RF08-00003	C			
	M.SCHURMAN 2-19-69				
	G.SAVIERS 2-19-69				
GB	RF08-00005	D			
	M.SCHURMAN 4-15-69				
	G.SAVIERS 4-17-69				

DRN. J.BISSONNETTE	DATE 4-2-68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R.BRUNO	DATE 4-2-68	
ENG. S.A.LAMBERT	DATE 4-2-68	TITLE: INPUT OUTPUT CONTROL
PROJ. ENG. S.A.LAMBERT	DATE 4-2-68	
PROD. R.ANTONNUCCIO	DATE 4-7-68	
FIRST USED ON: RF08		SIZE D | CODE BS | NUMBER RF08-0-1 | REV. E
SCALE		
SHEET 1 OF 1		DIST.

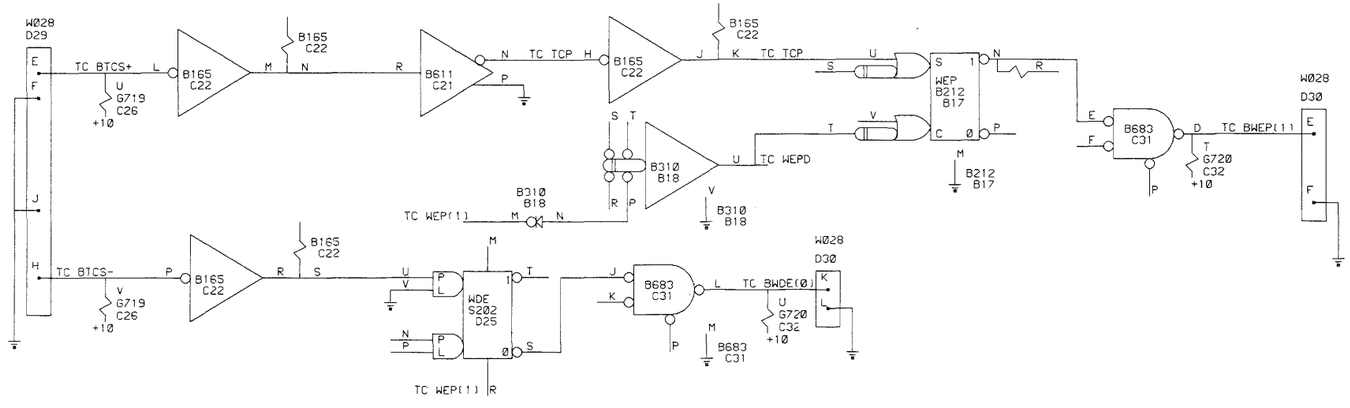
Figure 6-28 Input Output Control







NOTE: THIS MODULE GENERATES
LOCAL POWER CLEAR WHEN
-15 IS MORE POSITIVE THAN -8VOLTS.



REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF08-00002	B0	PD	RF08-00006	E
	BISSONNETTE 11-1-69			A.WASHINGTON 5-23-69	
	R.BRUNO 11-1-69			G.SAVIERS 5-23-69	
	RF08-00003	C		RF08-00014	F
	M.SCHURMAN 2-19-69				
	G.SAVIERS 2-19-69				
	RF08-00005	D			
	M.SCHURMAN 4-15-69				
	G.SAVIERS 4-17-69				

DRN. J.BISSONNETTE	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D P. BRUNO	DATE	
ENG. S.A.LAMBERT	DATE	TITLE: TIMING CONTROL
PROJ ENG. R.ANTONNUCCIO	DATE	
PROD.	DATE	
FIRST USED ON: RF08		SIZE: D | CODE: BS | NUMBER: RF08-0-2 | REV: F
SCALE		
SHEET OF		DIST.

Figure 6-29 Timing Control

NOTE: WHEN ACH IS A ZERO THE DMA WILL INCREMENT. WHEN ACH IS A ONE IT WILL NOT INCREMENT.

NOTE: ABC IS IN THE ONE STATE AT TCP TIME FOR ALL ADDRESSES EXCEPT THE ONE THAT COMPARES. (CLEAR AT TCP TIME SHOWS COMPARISON.)

NOTE: IDMAE SHOWN BELOW FOR LOADING A LOGICAL '1' INTO DMA Ø1.

REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF08-00002	B0		RF08-00014	E
	BISSONETTE 11-1-68				
	R.BRUNO 11-1-68				
PD	RF08-00003	C			
	M.SCHURMAN 2-19-69				
	G.SAVIERS 2-19-69				
GB	RF08-00005	D			
	M.SCHURMAN 4-15-69				
	G.SAVIERS 4-15-69				

DRN. J.BISSONNETTE	DATE 4-2-68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D. R.BRUNO	DATE 4-2-68	TITLE ADDRESS CONTROL	
ENG. S.A.LAMBERT	DATE 4-2-68		
PROJ. ENG. S.A.LAMBERT	DATE 4-2-68		
PROD. R.ANTONNUCCIO	DATE 4-7-68		
FIRST USED ON RF08		SIZE D	CODE BS	NUMBER RF08-0-3	REV. E
SCALE			
SHEET 1 OF 1		DIST.	

Figure 6-30 Address Control

NOTE: WHEN WCO IS A ONE, A WORD COUNT OVERFLOW PULSE HAS NOT YET OCCURED. WHEN WCO IS A ZERO IT HAS OCCURED.

Set

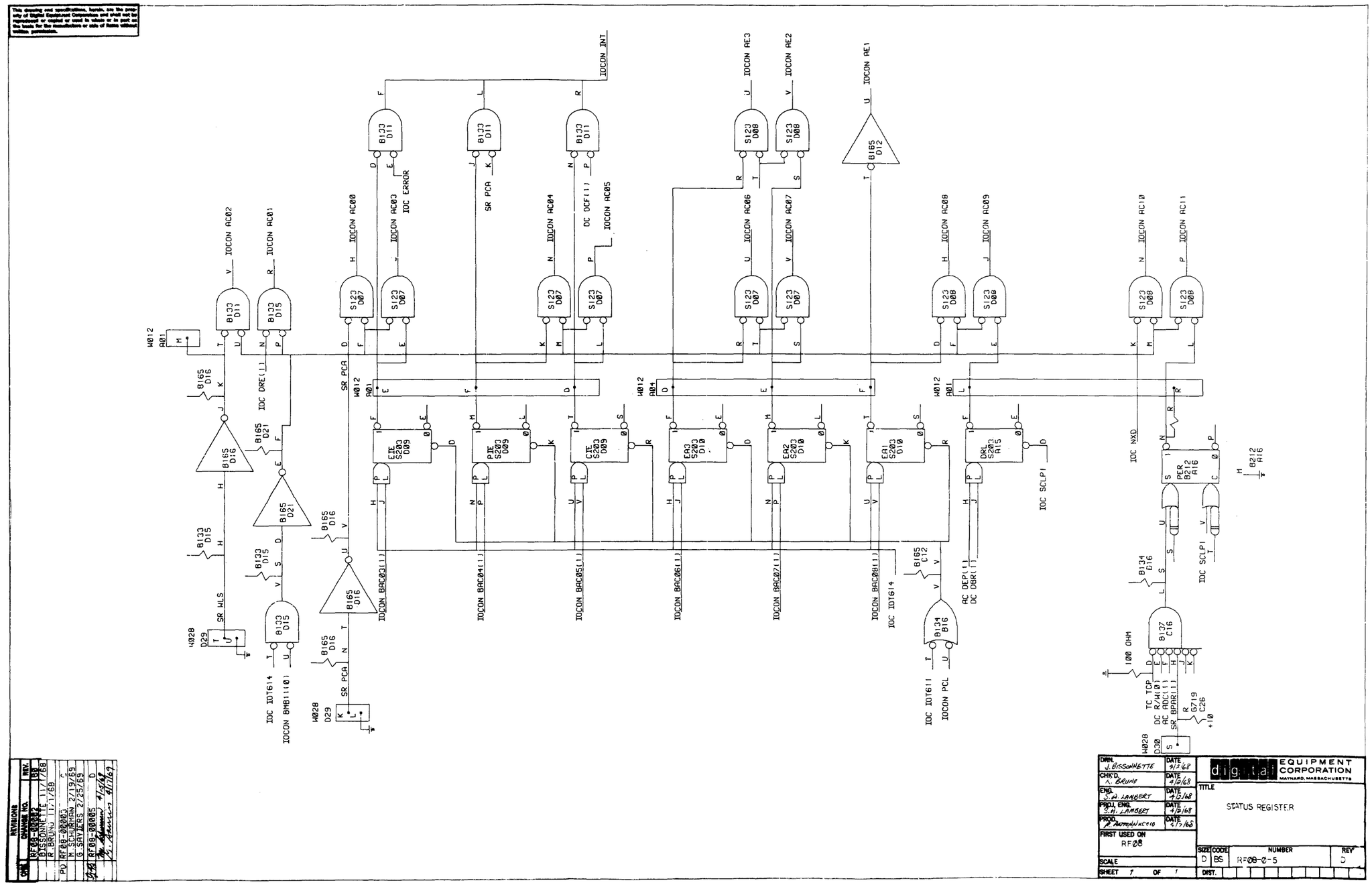
write clear

Read clear

REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF08-00002	B0	PD	RF08-00006	E
	BISSONNETTE 11-1-68			A.WASHINGTON 5-14-69	
	R.BRUNO 11-1-68			G.SAVIERS 5-23-69	
PD	RF08-00003	C		RF08-00014	F
	M.SCHURMAN 2-19-69				
	G.SAVIERS 2-19-69				
	RF08-00005	D			
	M.SCHURMAN 4-15-69				
	G.SAVIERS 4-17-69				

DRN. J.BISSONNETTE	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R.BRUNO	DATE	
ENG. S.A.LAMBERT	DATE	TITLE: DATA CONTROL
PROJ. ENG. S.A.LAMBERT	DATE	
PROD. R.ANTONNUCCIO	DATE	
FIRST USED ON: RF08		SIZE: D; CODE: 85; NUMBER: RF08-0-4; REV.: F
SCALE		
SHEET 1 OF 1		DIST.

Figure 6-31 Data Control



REVISIONS		
DASH	CHANGE NO.	INIT.
	RF08-00002	RB
	B.SSONNETTE 11/1/68	
	R. BRUNO 11/1/68	
	RF08-00005	C
	N. GOODMAN 2/19/69	
	G. SAVIERS 2/25/69	
	RF08-00005	D
	[illegible] 4/1/69	
	[illegible] 4/11/69	

DRN. J. BISSONNETTE	DATE 9/3/68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. K. BRUNO	DATE 9/9/68	
ENG. S.W. LAMBERT	DATE 9/25/68	TITLE: STATUS REGISTER
PROJ. ENG. S.H. LAMBERT	DATE 9/9/68	
PROD. [illegible]	DATE 9/9/68	
FIRST USED ON RF08		SIZE D CODE BS NUMBER RF08-0-5 REV C
SCALE		
SHEET 1 OF 1		DIST.

Figure 6-32 Status Register

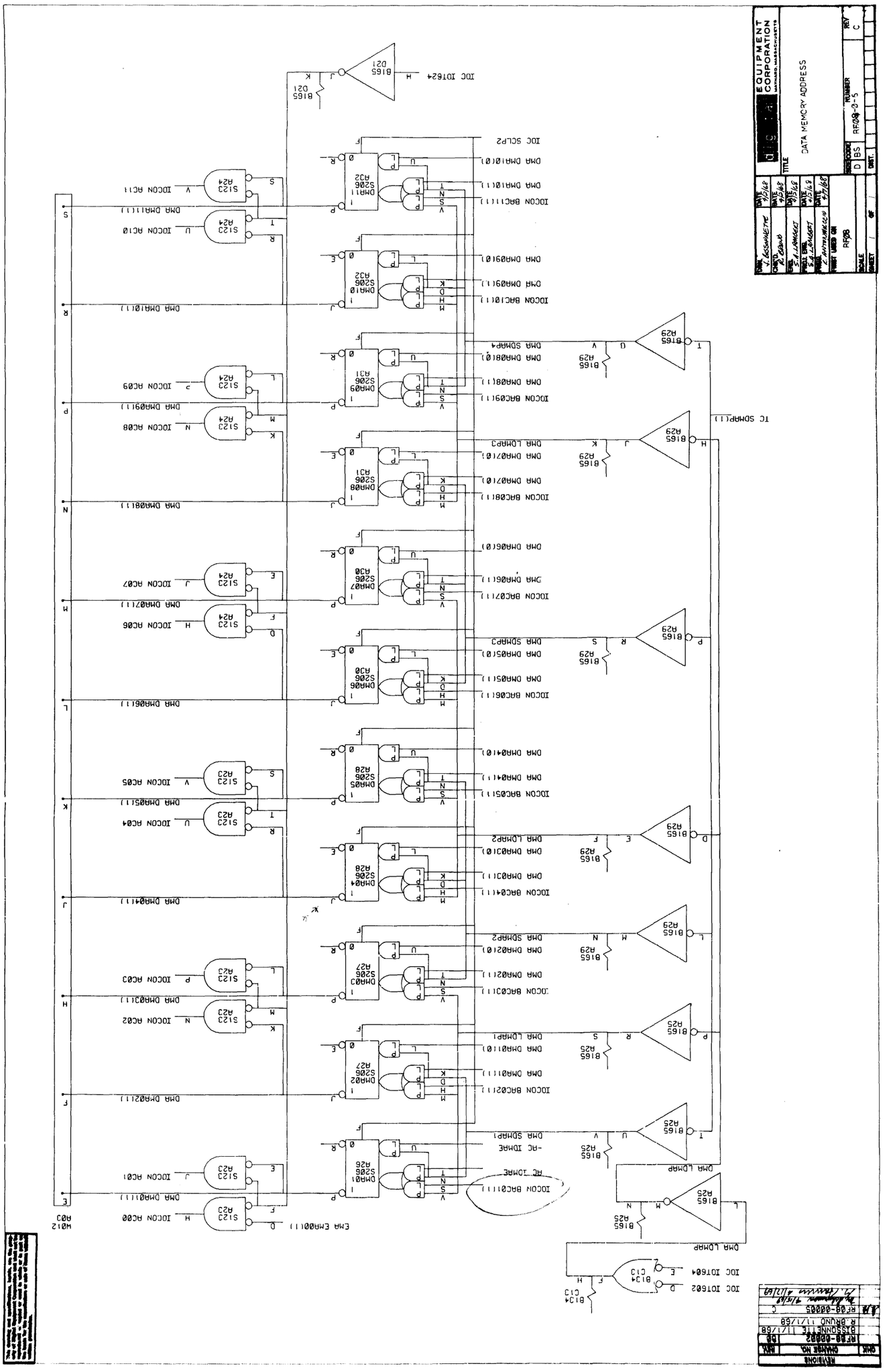


Figure 6-33 Disk Memory Address

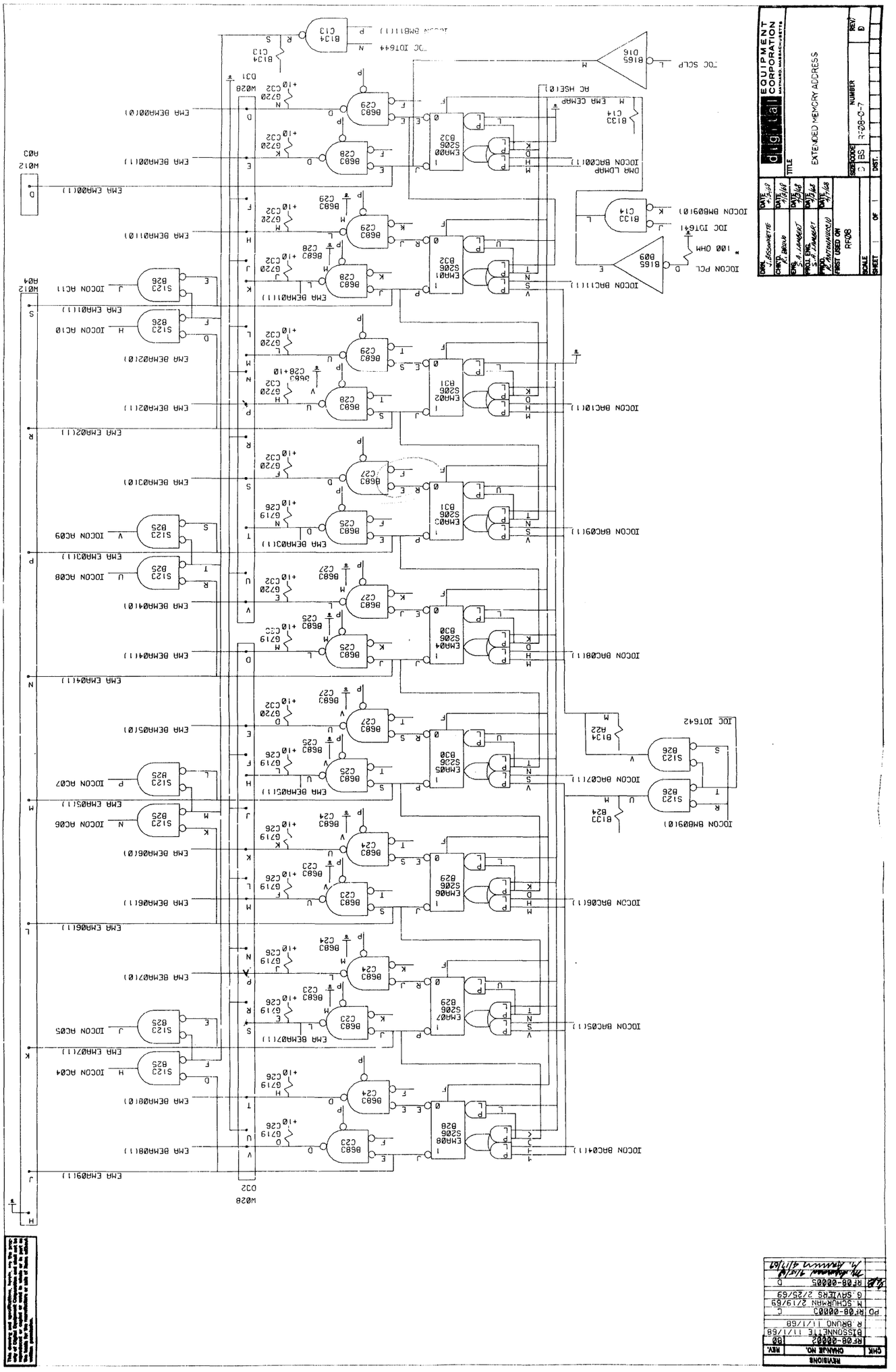
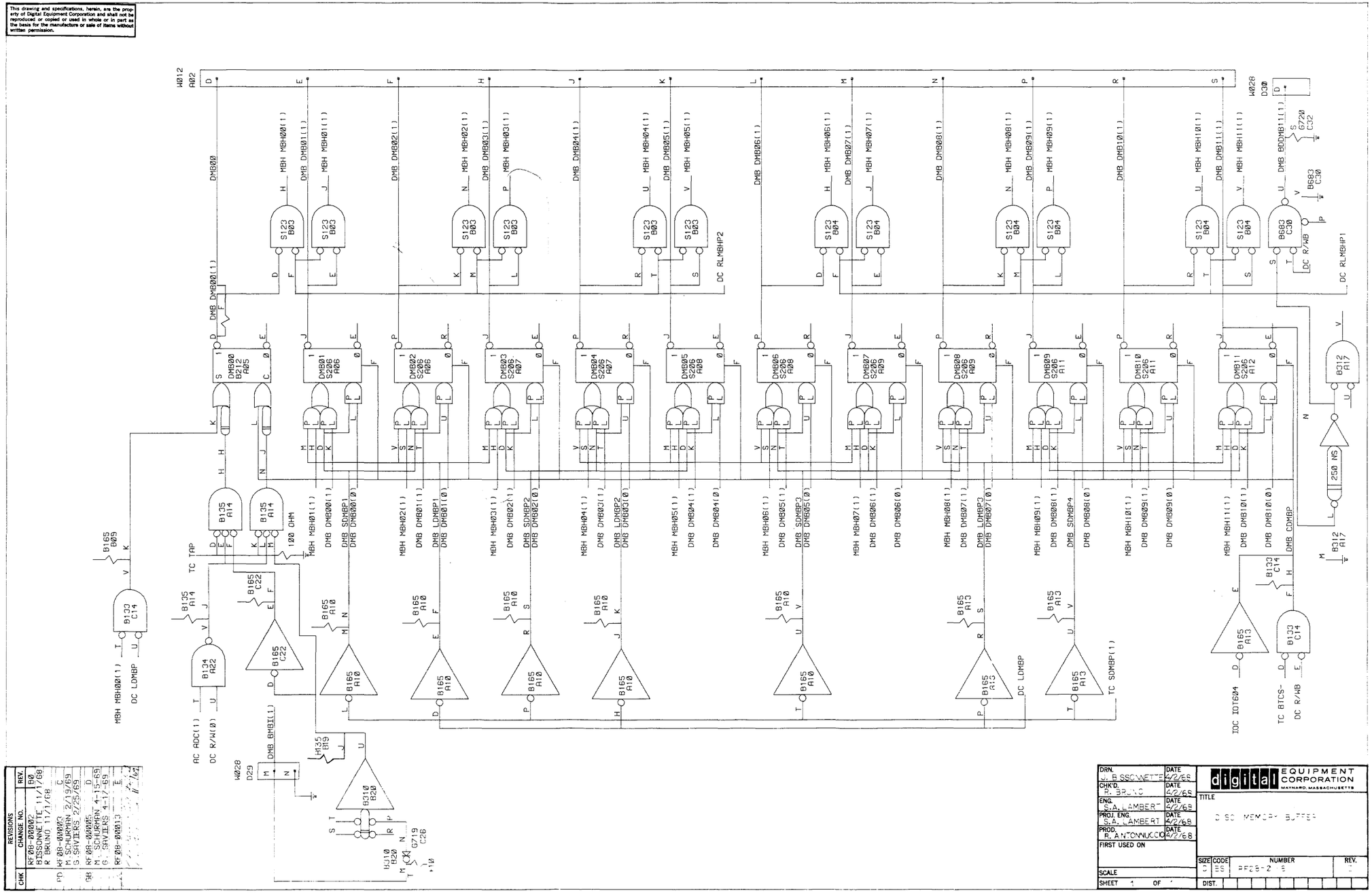


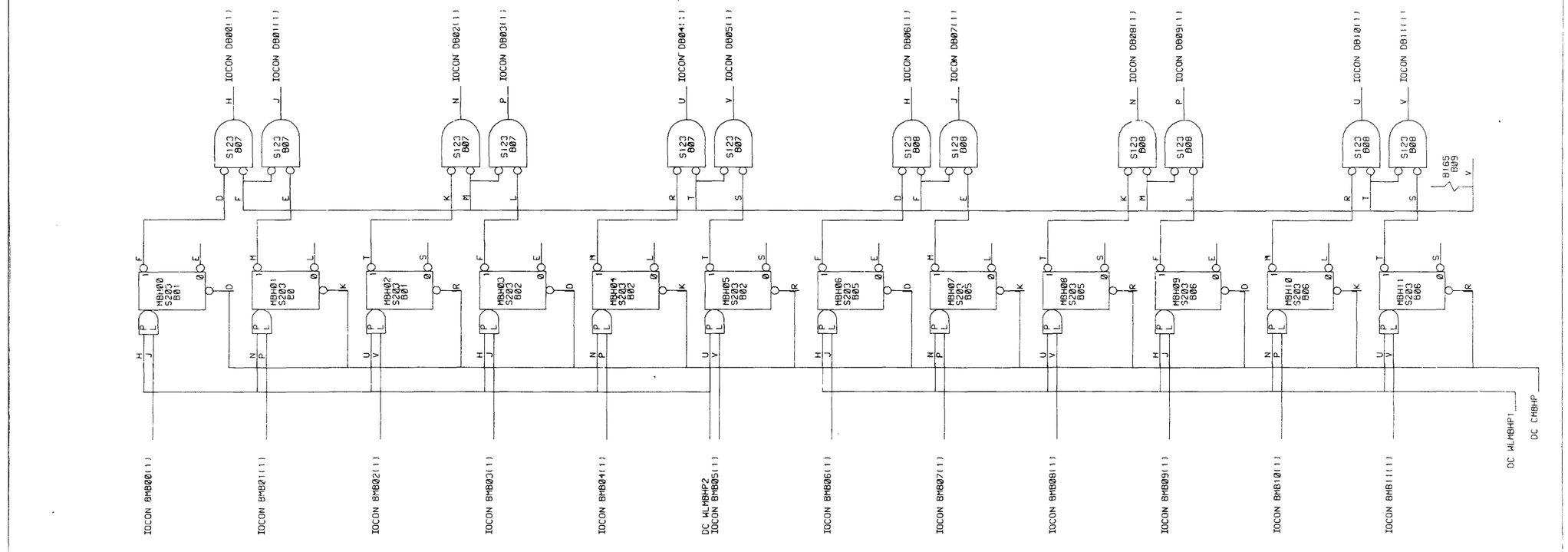
Figure 6-34 Extended Memory Address



REVISIONS			
CHK	CHANGE NO.	REV.	
	RF08-00002 B.SSONNETTE 11/1/68 R.BRUNO 11/1/68	00	
PD	RF08-00003 M.SCHURMAN 2/19/69 G.SHIVERS 2/25/69	C	
DB	RF08-00005 M.SCHURMAN 4-15-69 G.SHIVERS 4-17-69	D	
	RF08-00013	E	

DRN. J. BISSONNETTE	DATE 4/2/68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. BRUNO	DATE 4/2/68	
ENG. S.A. LAMBERT	DATE 4/2/68	TITLE D SC MEMORY BUFFER
PROJ. ENG. S.A. LAMBERT	DATE 4/2/68	
PROD. R. ANTONUCCIO	DATE 4/2/68	
FIRST USED ON		SIZE D; CODE 25; NUMBER RF28-2 E; REV. E
SCALE		
SHEET 1 OF 1		DIST.

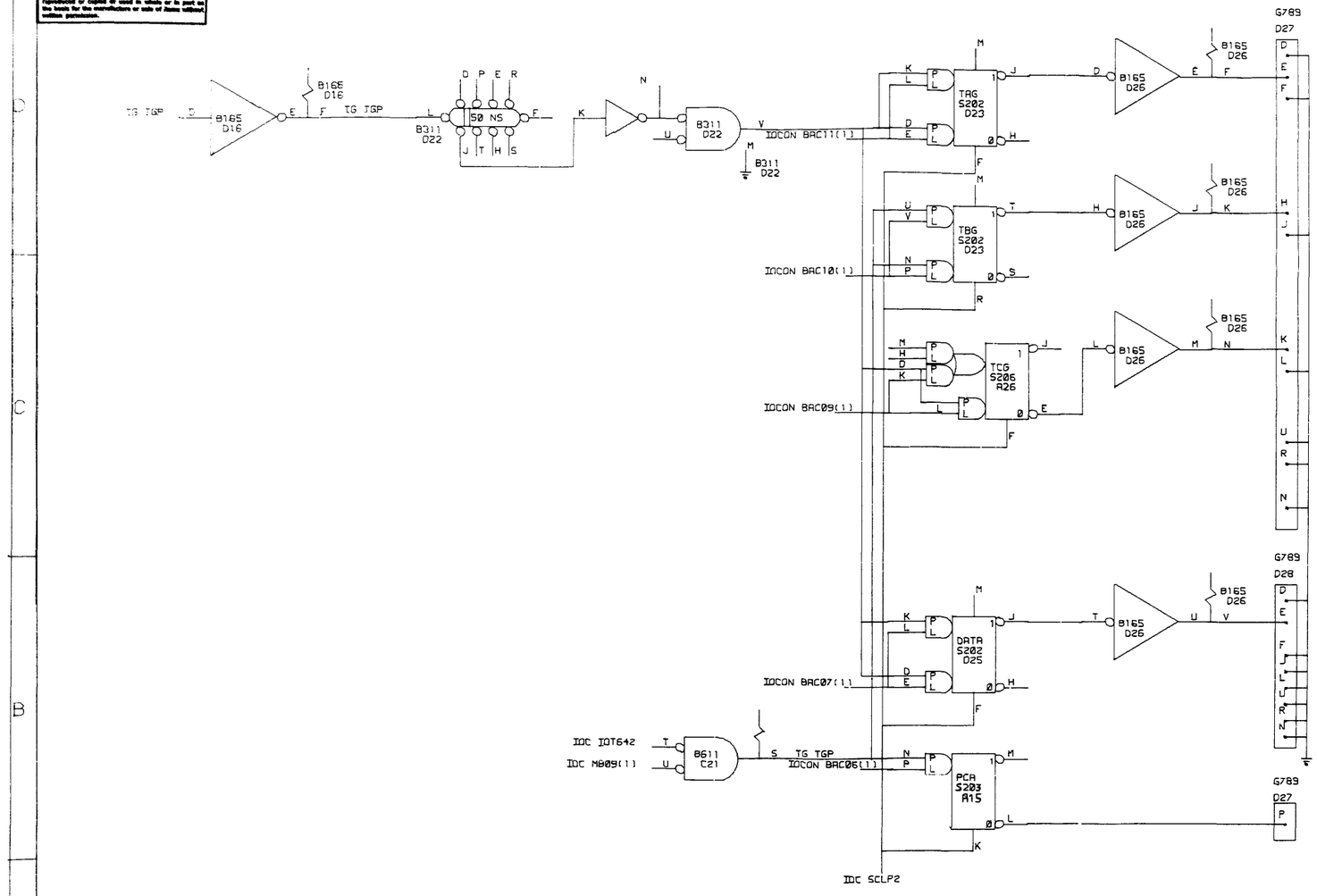
Figure 6-35 Disk Memory Buffer



REVISIONS			
CHK	CHANGE NO.		REV.
RJ			A
	DISSONNETTE 6/10/68		
	R. BRUNO 6/10/68		B
	RF08-00005		
RJ		4/16/69	
		4/17/69	

DRN. J. BISSONNETTE	DATE 4/15/68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R. BRUNO	DATE 4/16/68	
ENG. S.A. LAMBERT	DATE 4/16/68	TITLE MEMORY ADDRESS HOLD
PROJ. ENG. S.A. LAMBERT	DATE 4/16/68	
PROD. R.ANTHONY CC.10	DATE 4/19/68	
FIRST USED ON RF08		SIZE D CODE BS NUMBER RF08-0-S REV B
SCALE		
SHEET OF		DIST.

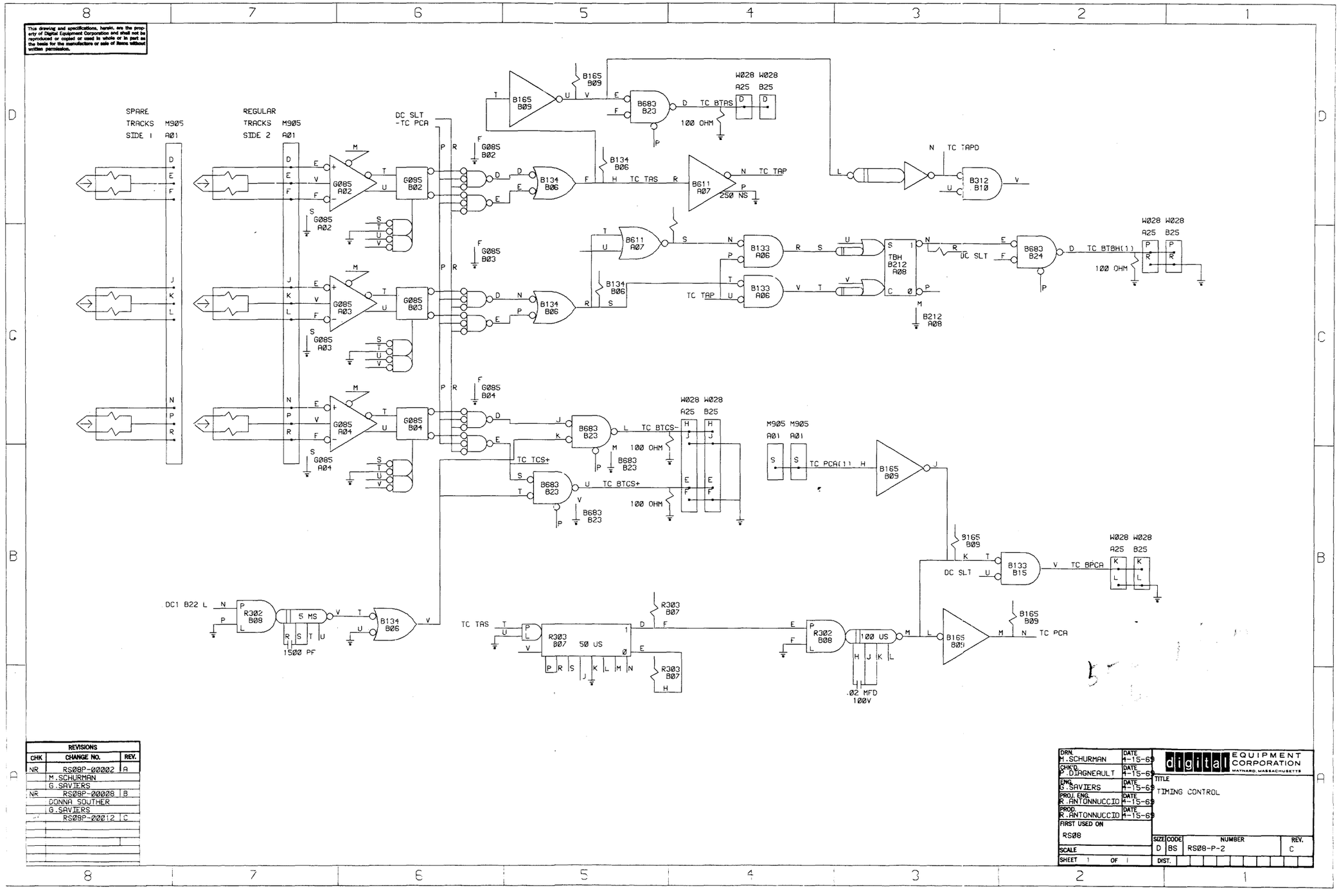
Figure 6-36 Memory Buffer Hold



REVISIONS		
ECO	COMMENT NO.	REV.
	RF08-00003	00
	J. BISSONNETTE 11/1/68	
	R. BRUNO 11/1/68	
23	RF08-00003	C
	M. Schuman 2/21/69	
	J. Lawrence 2/25/69	

DRN. BISSONNETTE	DATE 4-3-68	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R. BRUNO	DATE 4-3-68	TITLE TRACK GENERATOR
ENG. L.A. LAMBERT	DATE 4-3-68	
ENGR. ENG. L.A. LAMBERT	DATE 4-3-68	
APPD. M. MATCHNIKOFF	DATE 4-3-68	
FIRST USED ON RF08		SIZE D CODE 85 NUMBER RF08-2-10 REV. C
SCALE		DIST.
SHEET 1 OF 1		

Figure 6-37 Track Generator



REVISIONS		
CHK	CHANGE NO.	REV.
NR	RS08P-00002	A
	M.SCHURMAN	
	G.SAVIERS	
NR	RS08P-00008	B
	DONNA SOUTHER	
	G.SAVIERS	
	RS08P-00012	C

DRN. M.SCHURMAN	DATE 4-15-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P.DIAGNEAULT	DATE 4-15-69	
ENG. G.SAVIERS	DATE 4-15-69	TITLE TIMING CONTROL
PROJ.ENG. R.ANTONNUCCIO	DATE 4-15-69	
PROD. R.ANTONNUCCIO	DATE 4-15-69	
FIRST USED ON RS08		SIZE D / CODE BS / NUMBER RS08-P-2 / REV. C
SCALE		
SHEET 1 OF 1		DIST.

Figure 6-38 Timing Control

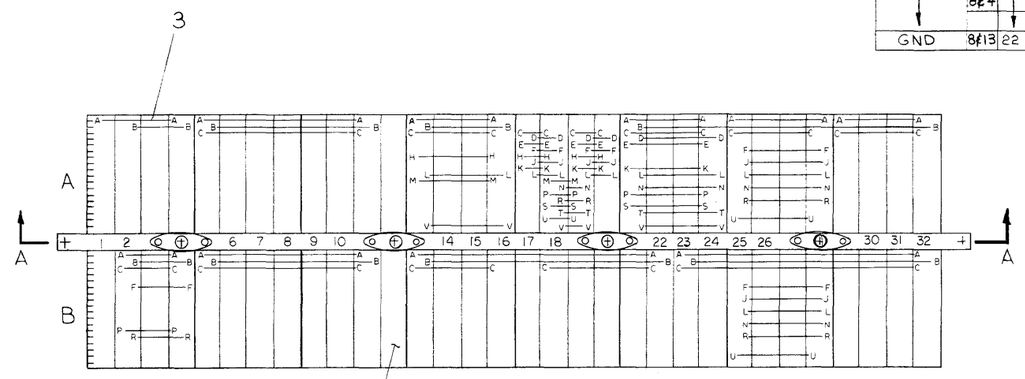
EXTERNAL COMPONENT TABLE						
ITEM	COMP	POL	FROM	TO	POL	REMARKS
14	CAP	-	B27B	B27C	+	
14	CAP	+	A28C	A28B	-	
14	CAP	+	A28A	A27C	-	
15	CAP		B08H	B08J		
16	RES		A06C	A06E		
16	RES		B11C	B11T		
16	RES		B19C	B19T		

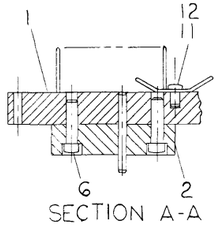
WIRE TABLE						
SIGNAL NAME	ITEM NO	DESCRIPTION AWG	COLOR	CONNECTIONS FROM	TO	REMARKS
+20V	8#7	#22	YEL	A29A	B12A	RIGHT ANGLE ROUTING THROUGH CENTER CHANNEL
-15V	8#5		BLU	B32B	B12B	
GND	8#4		WHT	BØ4C	B12C	
				B12C	L3L	
				B28C	L4L	
				AØ2C	L1L	
				AØ3C	L1L	
				AØ4C	L1L	
				A12C	L1L	
				AØ5C	L1R	
				BØ5C	L1R	
				B11C	L2L	
				B13C	L2R	
				B18C	L3L	
				B22C	L3R	
	8#4		WHT	A24C	L3R	
GND	8#13	#22	RED	A29A	B29A	

NOTE:
L=GROUND LUG
1-9=LEFT TO RIGHT
L=LEFT
R=RIGHT
EXAMPLE:
L2R=GROUND LUG#2 FROM LEFT, RIGHT HALF

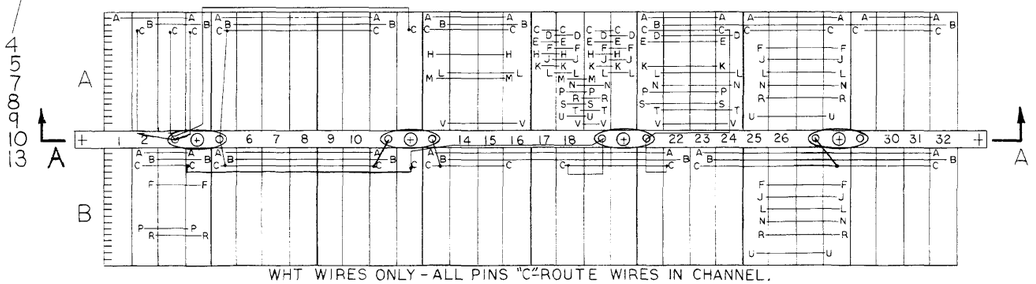
NOTES:

1. CONNECTIONS ON ITEMS #3 & 8 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
2. ALL CONN. BLOCKS TO BE GROUNDED TO GND LUGS AS PER WIRE TABLE.
3. USE YEL WIRE (ITEM #9) FOR MACHINE WRAPPED BLU WIRE (ITEM #10) FOR HAND WRAPPED WIRING.





SECTION A-A
SCALE: 1/1



WHT WIRES ONLY - ALL PINS "C" ROUTE WIRES IN CHANNEL.

REVISIONS			
CHK	CHANGE NO.	REV.	
	RSØ8-00002	—	
	ORIGINATED		
	11508 00003	A	
	11508P 00008	B	

FIRST USED ON OPTION / MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RSØ8-P		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —"—
FINISH —"—

DRN	G Flanders	DATE 1/10/69
CHK'D	D. Hardy	DATE 1/23/69
ENG.	[illegible]	DATE 2/10/69
PROJ. ENG.	[illegible]	DATE 4/10/69
PROD.	[illegible]	DATE 9/10/69

NEXT HIGHER ASSY
D-UA-RSØ8-P-Ø
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

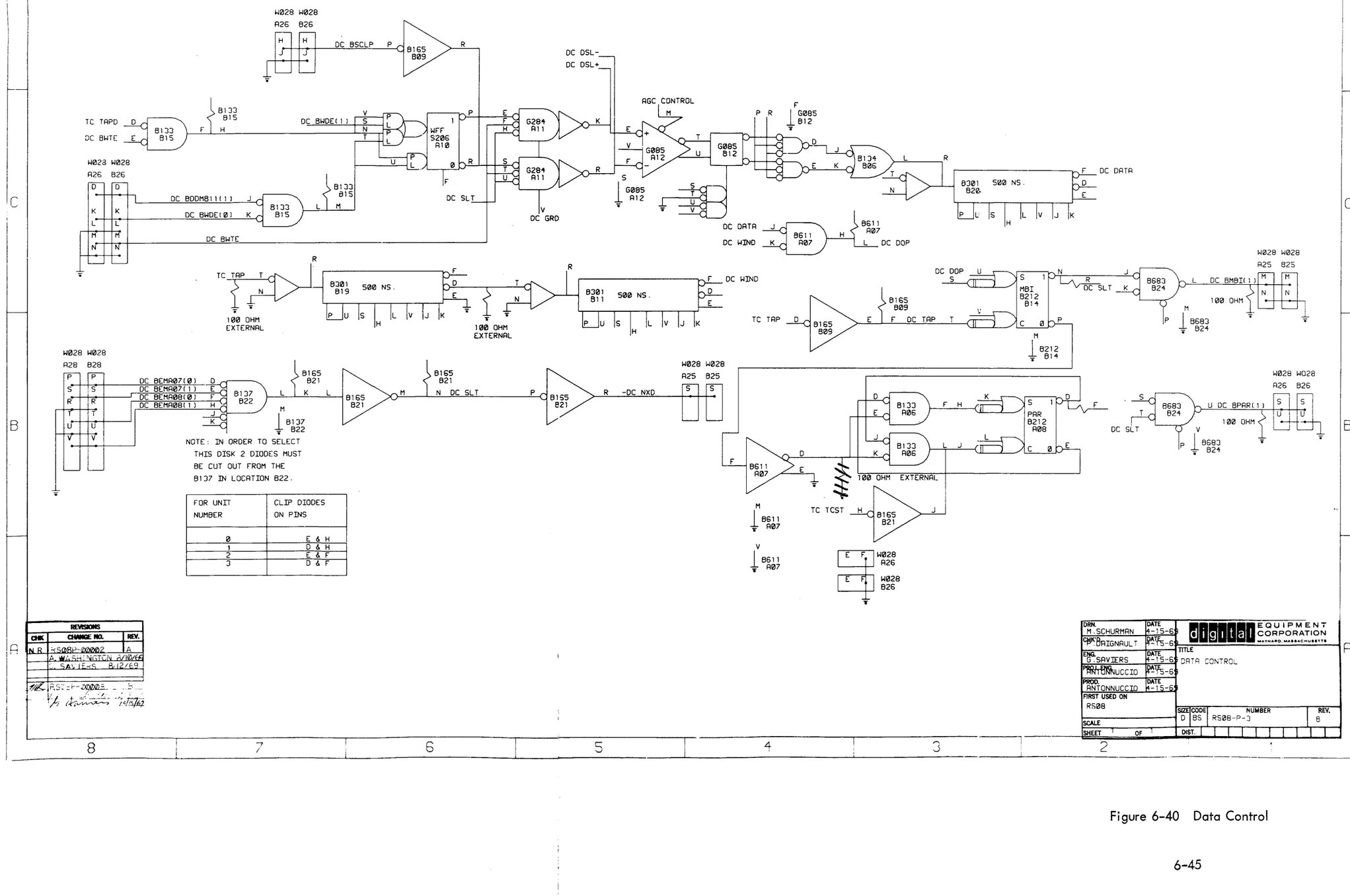
TITLE
WIRED ASSY
RSØ8-P

SIZE	CODE	NUMBER	REV.
D	AD	7006109-0-0	B

DIST.

DEC FORM NO DEC 10C

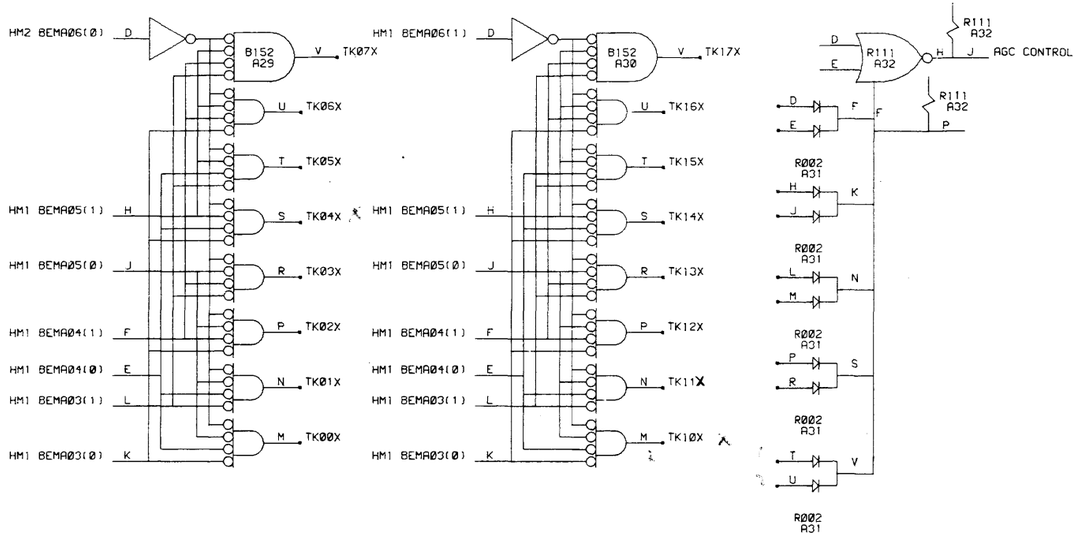
Figure 6-39 Wired Assembly



REVISIONS		
CHK	CHANGE NO.	REV.
N R	KS08P-00002	A
	A. WASHINGTON 8/10/69	
	W. SAVIERS 8/12/69	
	RS08P-00003	B

DRN. M. SCHURMAN	DATE 4-15-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. DAIGNAULT	DATE 4-15-69	
ENG. G. SAVIERS	DATE 4-15-69	TITLE: DATA CONTROL
PROJ. ENG. ANTONNUCCIO	DATE 4-15-69	
PROD. ANTONNUCCIO	DATE 4-15-69	
FIRST USED ON RS08		SIZE D | CODE 85 | NUMBER RS08-P-3 | REV. B
SCALE		
SHEET OF		DIST.

Figure 6-40 Data Control



G711 TERMINATOR BOARDS PLUG INTO LOCATIONS B25-B28 OF THE LAST RS08 LOGIC ON THE BUSS. RESISTORS ARE CUT OUT OF THEM AS FOLLOWS:

LOCATION	CUT OUT
B25	K,S,T,V
B26	T + V
B27+B28	NONE

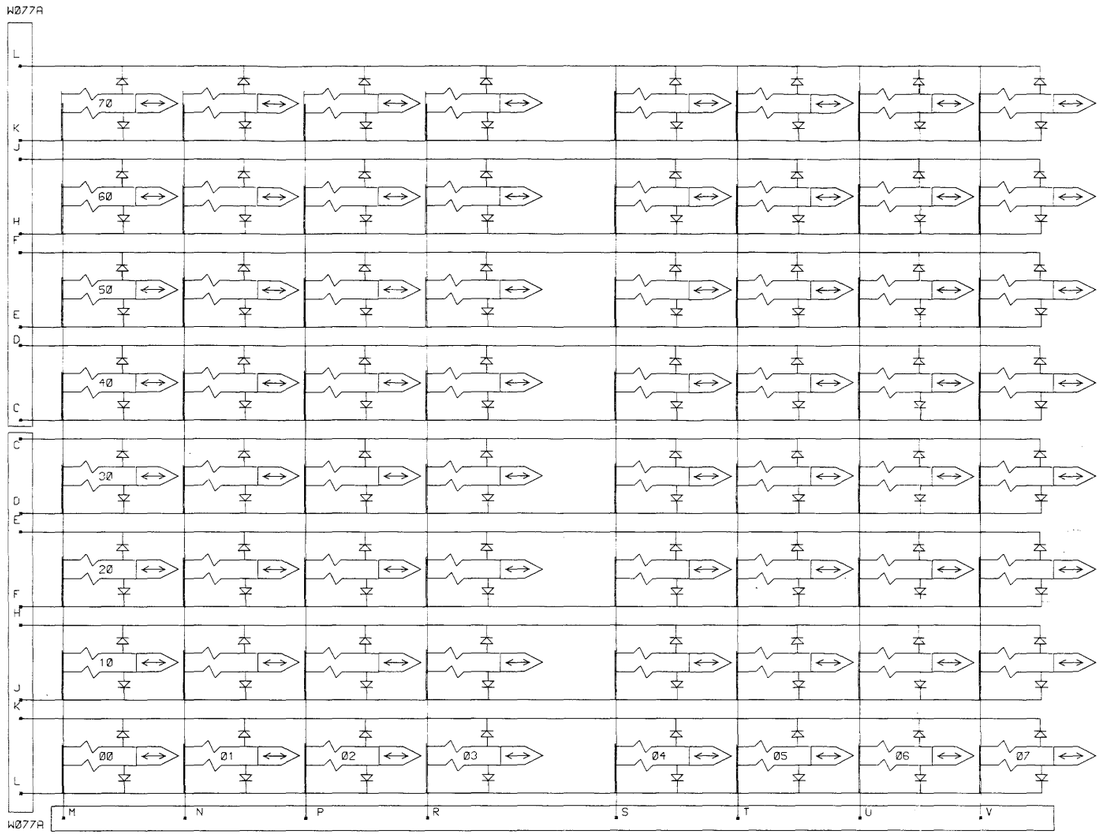
FOR GAIN CONTROL:

INCREASE GAIN FOR ANY GROUP OF EIGHT TRACKS (E.G. 130-137) BY CONNECTING TERMI-POINT JUMPERS FROM A29-A30 OUTPUTS TO OR GATE IN A31-A32. CONNECT ONLY ONE JUMPER TO EACH OR GATE INPUT.

REVISIONS		
CHK	CHANGE NO.	REV.
	RS08P-00002	A

DRN. M.SCHURMAN	DATE 4/1/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P.DIAGNEAULT	DATE 4/2/69	
ENG. G.SAVIERS	DATE 4/5/69	TITLE: AUTOMATIC GAIN CONTROL
PROJ. ENG. R.ANTONNUCCIO	DATE 4/5/69	
PROD. R.ANTONNUCCIO	DATE 4/5/69	
FIRST USED ON: RS08		SIZE D | CODE BS | NUMBER RS08-P-4 | REV. A
SCALE		
SHEET 1 OF 1		DIST.

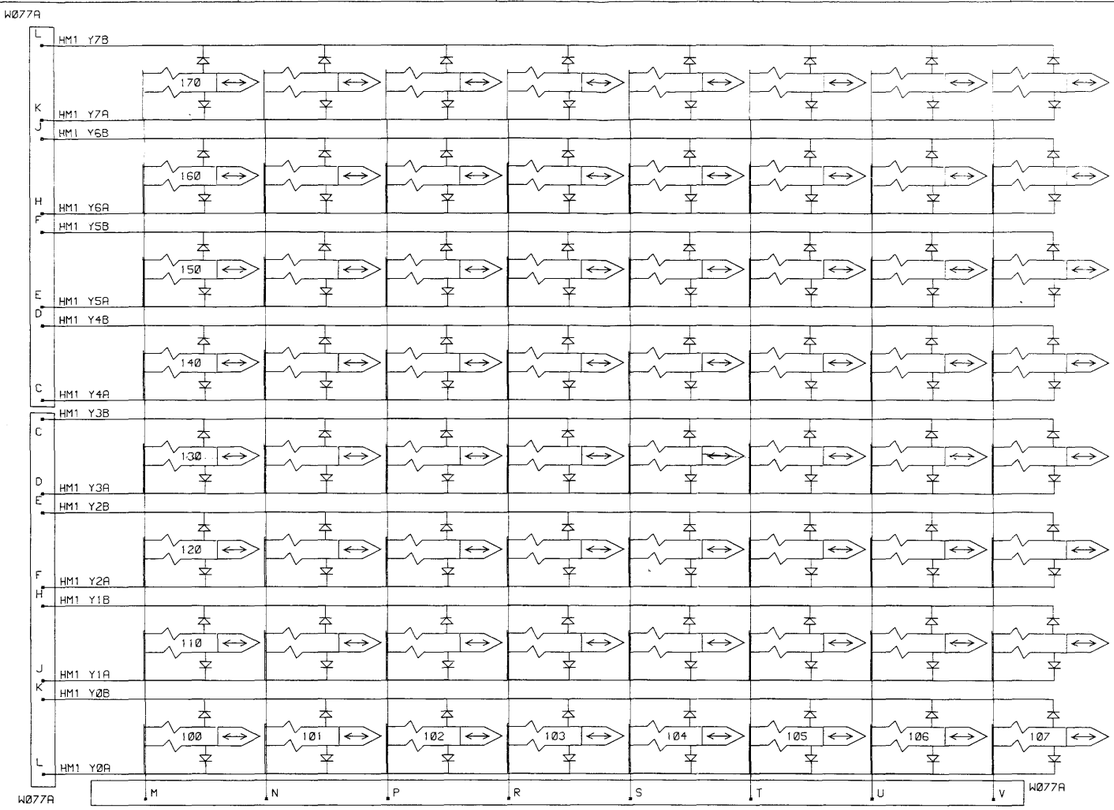
Figure 6-41 Automatic Gain Control



REVISIONS		
CHK	CHANGE NO.	REV.
	RS08M-00009	A

DRN. M.SCHURMAN	DATE 4/15/82	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
CHK'D. P.DAIGNEAULT	DATE 4/15/82		
ENG. J.SAIVERS	DATE 4/15/82	TITLE HEAD MATRIX	
PROJ. ENG. J.SMITH	DATE 4/15/82		
PROD. A.ANTONUCCIO	DATE 4/15/82		
FIRST USED ON RS08		SIZE D / CODE BS / NUMBER RS08-M-2 / REV. A	
SCALE			
SHEET 1 OF 2		DIST.	

Figure 6-42 Head Matrix



REVISIONS		
CHK	CHANGE NO.	REV.

DRN. M.SCHURMAN	DATE 4/15/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D. P.DAIGNEAULT	DATE 4/15/69	TITLE HEAD MATRIX	
ENG. B.SAIVERS	DATE 4/15/69		
PROJ. ENG. J.SMITH	DATE 4/15/69		
PROD. R.ANTONUCCIO	DATE 4/15/69		
FIRST USED ON RS08		SIZE D	CODE BS
SCALE		NUMBER RS08-M-2	REV. A
SHEET 2 OF 2		DIST.	

Figure 6-43 Head Matrix

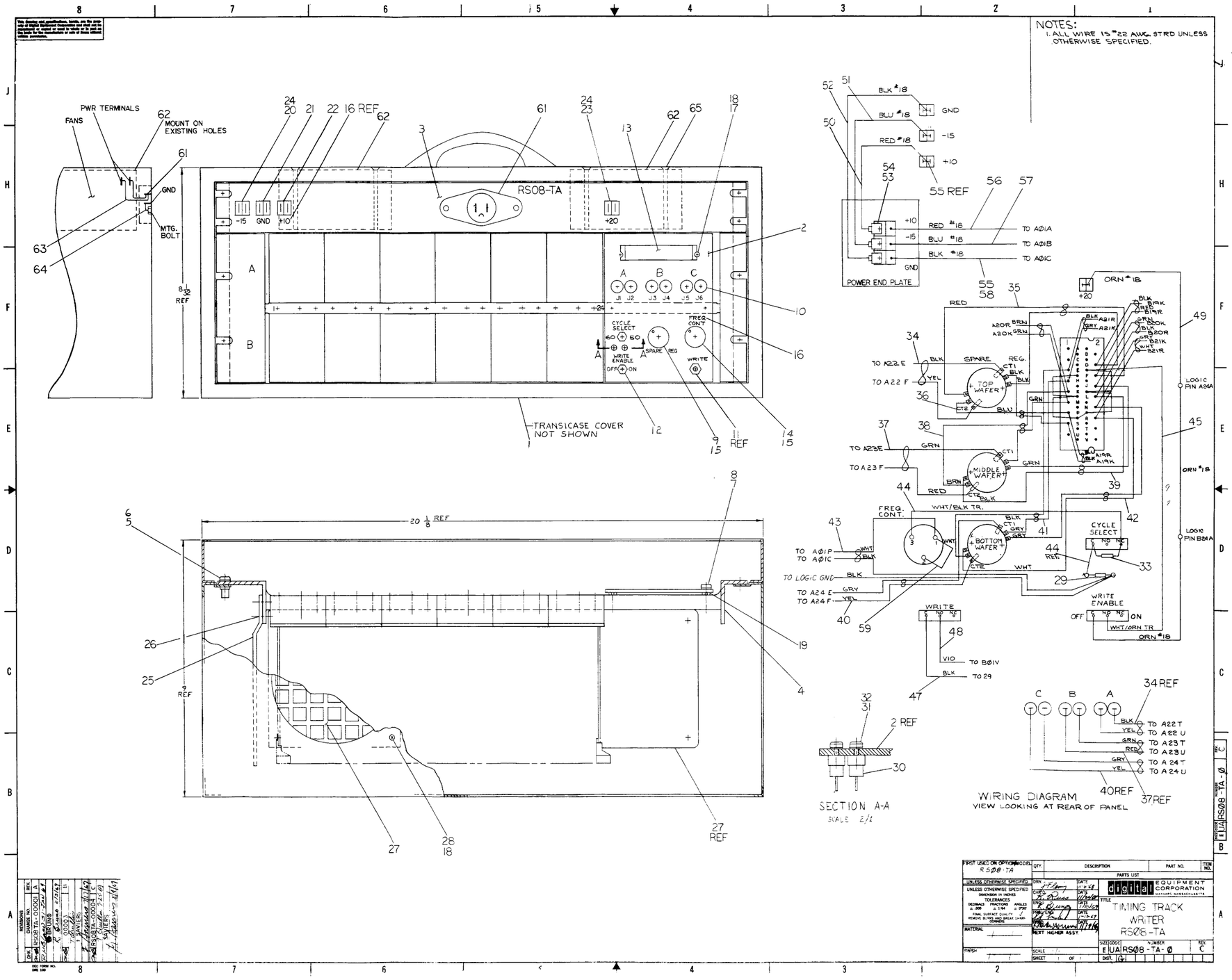
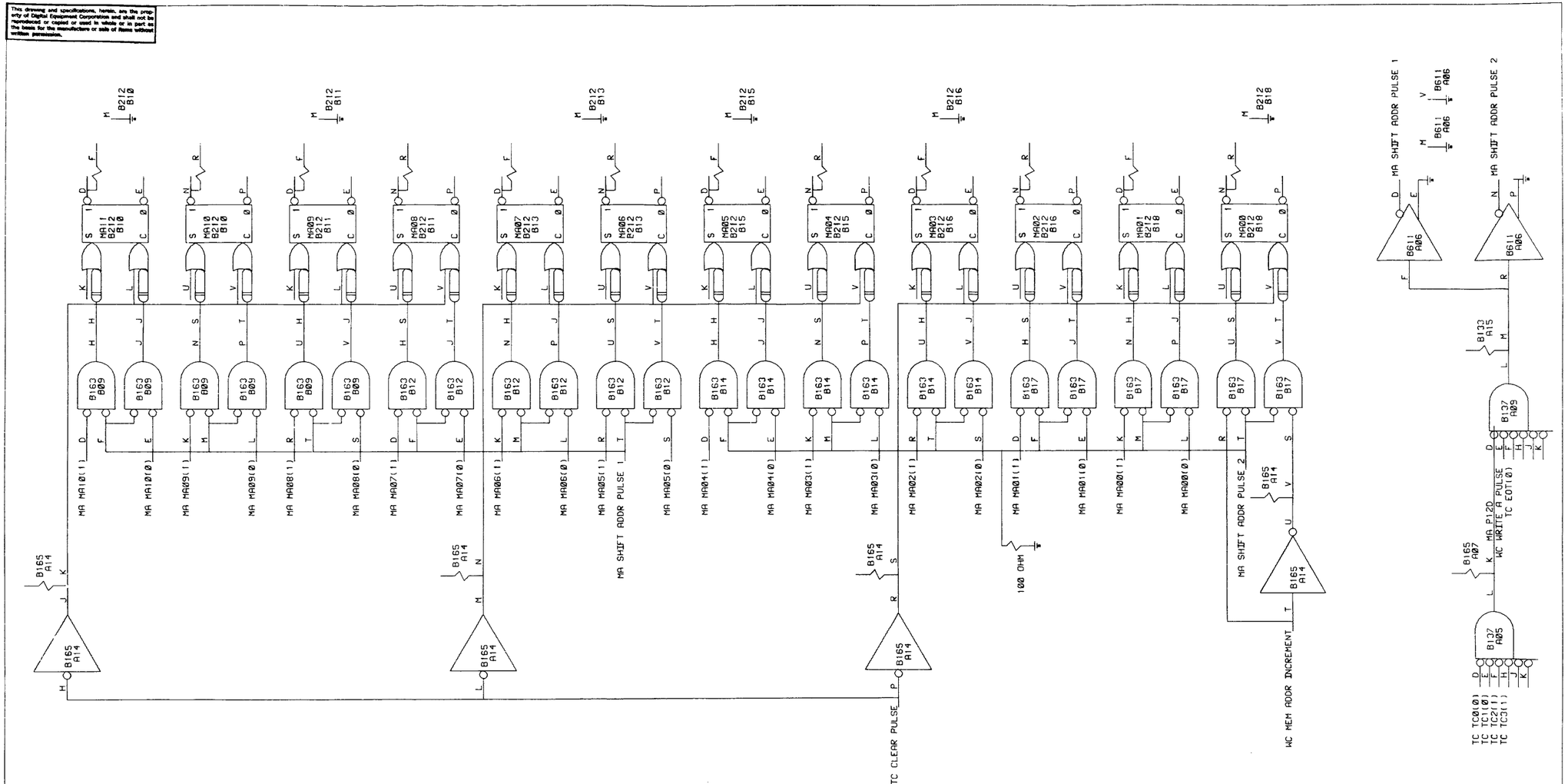


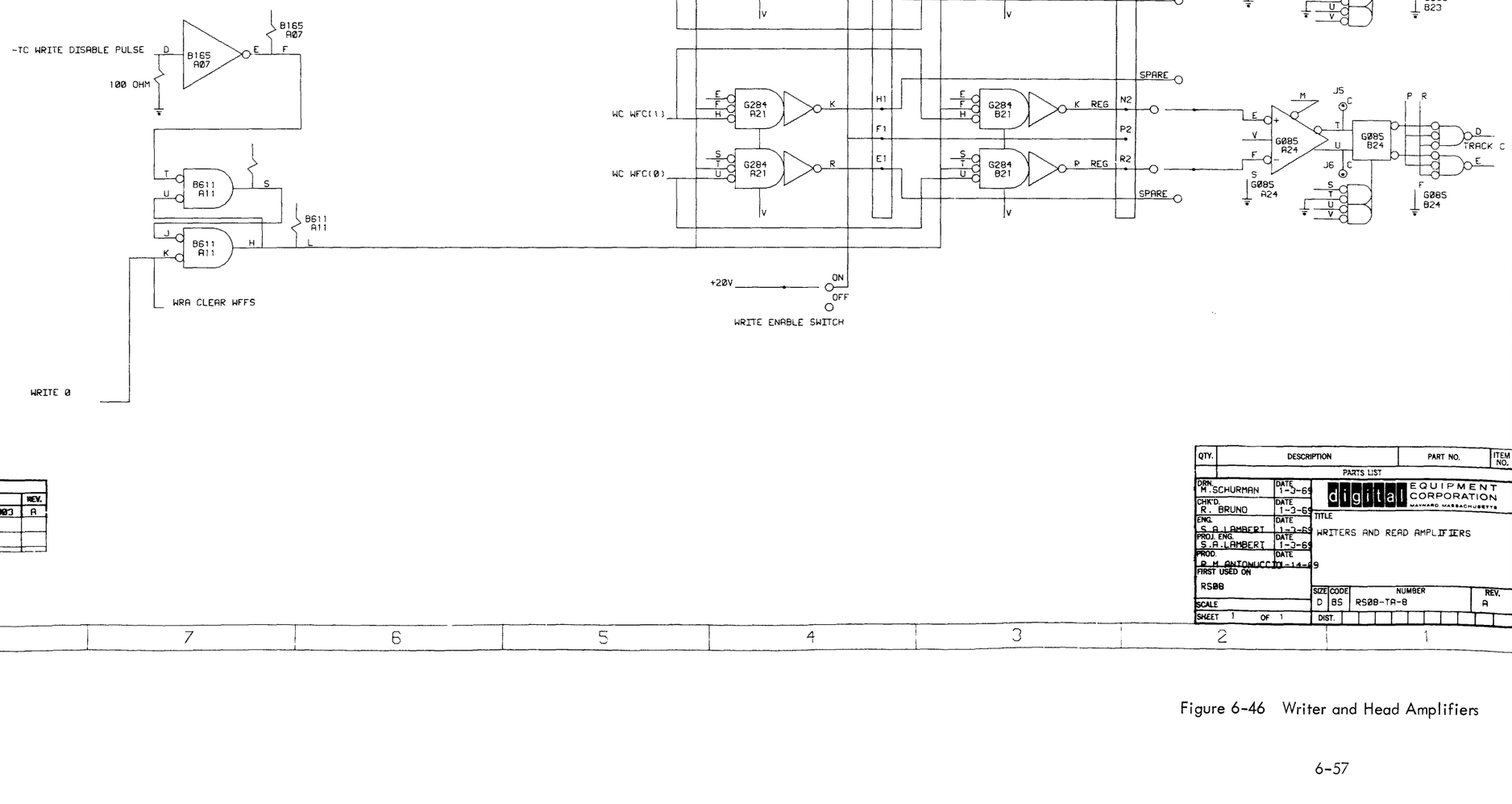
Figure 6-44 Timing Track Writer



REVISIONS		
CHK	CHANGE NO.	REV.
	Ø0002	A

DRN. M. SCHURMAN	DATE 1-3-69	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. R. BRUNO	DATE 1-3-69	
ENG. S.A. LAMBERT	DATE 1-3-69	TITLE: MEMORY ADDRESS
PROJ. ENG. S.A. LAMBERT	DATE 1-3-69	
PROD. A.M. ANTONUCCIO	DATE 1-3-69	
FIRST USED ON: RSØ8-TA		SIZE D · CODE BS · NUMBER RSØ8-TA-4 · REV. A
SCALE		
SHEET OF		DIST.

Figure 6-45 Memory Address



REVISIONS		
CHK	CHANGE NO.	REV.
	RS08-TA-00003	A
	S.A.LAMBERT	

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN. M.SCHURMAN	DATE 1-3-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D R. BRUNO	DATE 1-3-69	
ENG. S.A.LAMBERT	DATE 1-3-69	TITLE WRITERS AND READ AMPLIFIERS
PROJ. ENG. S.A.LAMBERT	DATE 1-2-69	
PROD. R.M.ANTONUCCI	DATE 1-14-69	
FIRST USED ON RS08		
SCALE	SIZE D	CODE 85 NUMBER RS08-TA-8 REV. A
SHEET 1 OF 1	DIST.	

Figure 6-46 Writer and Head Amplifiers

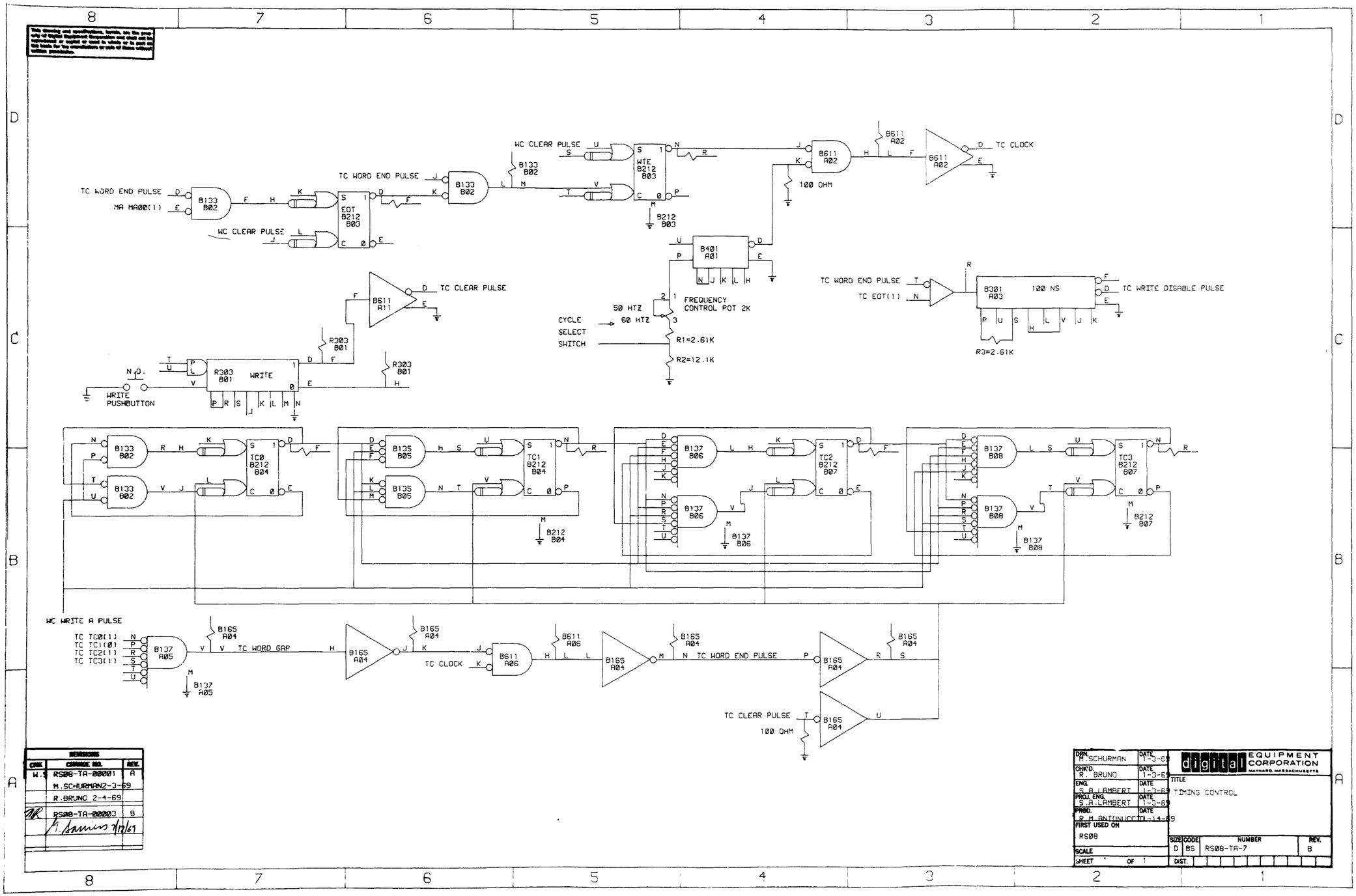


Figure 6-47 Timing Control

Appendix A
Reference Documents

A.1 RELATED DOCUMENTS AND PROGRAMS

Reference documents are listed in Table A-1, and program documents are listed in Table A-2. In addition, several program systems such as the TSS-8 Time-Sharing System use the disk file as part of the hardware required for those systems. The documents for these systems contain programming information; these programs are not listed here.

These publications can be obtained upon request from the nearest DEC field office, or from the following address:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Table A-1
Reference Documents

Document	Description
Digital Logic Handbook (C105)	Function and specifications of FLIP CHIP modules, cabinets, power supplies and accessories.
PDP-8 Maintenance Manual (F87)	Theory, operation, and maintenance information on the PDP-8 Processor.
PDP-8/I Maintenance Manual DEC-8I-HR1A-D and DEC-8I-HR2A-D)	Theory, operation, and maintenance information on the PDP-8/I Processor.
Small Computer Handbook (C500)	Describes operation and programming of PDP-8 and PDP-8/I computers.

Table A-2
Operation and Maintenance Programs

Program	Description
RF08 Software Package	Perforated program tapes and description of symbolic assembly, assembly language, and utility subroutines.
Multi Disk (Maintenance) DEC-08-D5FA	Tests system logic with the disk in operation.
Disk Data (Maintenance) DEC-08-D5FE	Tests the entire disk logic and disk including the interface, addressing and data.

Appendix B
Disk I/O Programming Example

```
/A SAMPLE OF A TYPICAL I/O ROUTINE FOR THE RF08/RS08 IS INCLUDED BELOW.

0200  4777          JMS I (DISKIO
0201  0000  FUNCT,  0             /X0=READ, X1=WRITE (X=0-7 MEMORY
                                   FIELD)
0202  0000  WDCT,   0             /* WORD COUNT
0203  0000  CORE,   0             /CORE LOCATION
0204  0000  DSKHI,  0             /HIGH ORDER 8 BITS
0205  0000  DSKLOW, 0             /LOW ORDER 12 BITS
0206  5020          JMP ERROR        /ERROR RETURN (AC=ERROR CONDITION)
                                   /NORMAL RETURN (AC=0)

0207  0000  DISKIO, 0
0210  7300          CLL CLA
0211  1607          TAD I DISKIO
0212  6615          DIML           /LOAD EXTENDED MEMORY BITS
0213  1607          TAD I DISKIO
0214  0376          AND (7
0215  7640          SZA CLA

0216  7126          STL RTL        /*2
0217  1375          TAD (3
0220  1374          TAD (6600
0221  3236          DCA RORW          /6603=READ, 6605=WRITE
0222  2207          ISZ DISKIO
0223  1607          TAD I DISK IO
0224  7041          CIA
0225  3773          DCA I (7750    /STORE = WORD COUNT
0226  2207          ISZ DISKIO
0227  1607          TAD I DISKIO
0230  3772          DCA I (7751    /LOAD CORE ADDRESS
0231  2207          ISZ DISKIO
0232  1607          TAD I DISKIO
0233  6643          DXAL           /LOAD HIGH ORDER 9

                                   /BITS OF DISK ADDRESS,
0234  1607          TAD I DISKIO
0235  2207          ISZ DISKIO

0236  0000  RORW,   0             /READ OR WRITE

0237  6623  DISK    DISK           /DONE?
0240  5237          JMP .-1        /NO
0241  6621          DFSE           /YES, ERROR?
```

```
0242  2207              ISZ DISKIO    /SKIP TO NORMAL RETURN
0243  5607              JMP I DISKIO  /RETURN

      6615  DIML=6615
      6623  DISK=6623
      6643  DXAL=6643
      6621  DFSE=6621
      0020  ERROR=20



                  $
      0372    7751
      0373    7750
      0374    6600
      0375    0003
      0376    0007
      0377    0207

      CORE    0203
      DFSE    6621
      DIML    6615
      DISK    6623
      DISKIO  0207
      DSKHI   0204
      DSKLOW  0205
      DXAL    6643
      ERROR   0020
      FUNCT   0201
      RØRW    0236
      WDCT    0202
```

Appendix C
Loading Procedure

C.1 READ-IN MODE (RIM) LOADER

The RIM Loader is a program used to load the Binary Loader. The RIM Loader must be toggled into memory using the switches on the computer console. To load the RIM Loader, follow the procedure below.

Step	Procedure
1	Determine if the RIM Loader program is correctly stored in memory by examining the following locations for the appropriate instructions (contents).

Location	Instruction	
	Model 33 ASR Reader	High-Speed Reader
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5374
7766	7006	7006
7767	6031	6011
7770	5367	5367
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000

2 If the instruction in any location does not agree with the above list, deposit the correct instruction into that location.

C.2 BINARY FORMAT (BIN) LOADER

The BIN Loader is a program used to load MAINDEC into memory. The BIN Loader tape is loaded by the RIM Loader as explained below.

The BIN Loader is loaded into locations 7612 through 7616, 7626 through 7752, and 7777, with its starting address at location 7777. A detailed description of the BIN Loader is included in the PDP-8 User's Handbook F-85.

To load the BIN Loader, follow the procedure below.

Step	Procedure
1	Determine if the RIM Loader is correctly stored in memory and make the necessary adjustments.
2	Put Binary Loader tape in the reader (always put leader-trailer code over reader head, never blank tape).
3	Turn reader ON.
4	Set Switch Register (SR) to 7756 (the starting address of the RIM Loader).
5	Depress the LOAD ADDress switch on the computer console.
6	Depress the START switch on the computer console.
7	Tape should begin reading in, if not, check the RIM Loader and start again at Step 1.
8	After the program is read in, depress the STOP switch on the computer console.

Appendix D
RF08 Signal Mnemonics

Table D-1
RF08 Signal Mnemonics

Mnemonic	Description
ABC	Address Bit Comparator flip-flop. Address track bits and Disk Memory Address (DMA) contents are compared serially. If they do not compare, ABC is set, to indicate no comparison. ABC is also set by Track End Pulse (TEP). Cleared at the end of each address word by Word End Pulse (WEP).
ADC	Address Confirmed flip-flop. Set at the end of an address word when the track address and DMA address compare (ABC clear). ADC is cleared by DRE (0), indicating that no data transfer is to occur and can be set only when DRE is 1. The set pulse is strobed in by Track C Pulse (TCP) at the end of an address word and delayed 60 ns. ADC is also cleared at the end of a track by HSE (1), DEP (1), and SCLP 1.
ACH	Address Compare Hold flip-flop. Determines the polarity of IDMAE when searching for an address and incrementing the DMA. ACH is set initially by SCLP which causes IDMAE to be true with respect to the contents of DMA 11. ACH is cleared by DEP at the end of any word in which data was transferred. This makes IDMAE the complement of the contents of DMA 11. ACH is set during the next address word by SDMAP and DMA 11 (0). This allows all of the low-order 1s and the first 0 in the DMA to be complemented as the address rotates through the DMA. ACH is also set by ADC going to set when the first address (00008) is compared after head switch, when writing a block of data.
BDDMB 11 (1)	Buffered-Delayed Disk Memory Buffer 11 (1). This signal reflects the state of DMB 11, delayed 250 ns after SDMBP. It is used as the writing command sent to the disk.
BTAS	Buffered Track A Sliced. The clock-strobe signal generated from timing Track A. This signal is differentiated to form the TAP pulses which represent the time location of each of the 13 bits of data.
BTCS-	Buffered Track C Sliced. A pulse generated at bit-time 12 from timing track C. This pulse sets WDE, denoting the end of data in each data word.
BTCS+	Buffered Track C Sliced. Generated from timing track C at bit-time 14. This pulse generates TCP and WEP, and clears WEP. Denotes the end of an address word.
CDMBP	Clear Disk Memory Buffer Pulse. Generated by IOT 604 (DMAW) and by BTCS- when writing. Clears the 12 DMB flip-flops to allow data transfer from the MBH register. Not generated during the read cycle.
CEMAP	Clear Extended Memory Address Pulse. Generated by PCL or by IOT 641 (DXAL). Generation inhibited by IOT 645 (DXAC). Clears the EMA to allow a new address to be written in from the central processor AC.

Table D-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
CIE	Completion Interrupt Enable flip-flop. Enables interrupt of the central processor by the DCF, when set. Set by IOT 614 (DIML) when central processor AC 5 is 1. Cleared by Power Clear (PCL) or IOT 611 (DCIM).
CMBH	Clear Memory Buffer Hold flip-flop. Generates CMBHP in write mode. Set by B Break (pulse) and Read/Write (R/W) (1 level) and cleared by WLMBHP- or SCLP 1.
CMBHP	Clear Memory Buffer Hold Pulse. Clears MBH before data transfer. Generated during write by CMBH (1). Generated during read by ADC (1) and R/W (0), strobed by BTCS-.
DATA	DATA flip-flop (maintenance). Complemented by TGP if central processor AC 7 is 1. Cleared by SCLP 2.
DBR	Data Break Request flip-flop. Requests three-cycle data break from central processor when disk is ready to transfer data to or from central processor. In write mode, initially set by IOT 604 (DMAW), then set by HSE (0) and WCS (0) (level), and LDMPB (pulse). In read mode, set by RLMBHP (1) and WCS (0) (pulse). Cleared by ADDR ACC or SCLP 1.
DCF	Data Completion Flag flip-flop. Set at the end of a data transfer. Set enabled by WCO (0) (level) and DEP (pulse). Also set by ROFP and NXD. Cleared by SCLP 1.
DEP	Data End Pulse flip-flop. Generates 100 ns pulse at the end of each data word transfer. Enabled by ADC (1) (level), strobed by TCP (pulse). Cleared by delay loop.
DMA	Disk Memory Address register. Eleven-bit flip-flop register which contains disk memory angular address. Loaded from central processor AC by IOT 602 (DMAR) or IOT (DMAW). Bit 1 corresponds with address bit being read from track. Address shifted through DMA 1 position toward DMA 11 by SDMAP. State of DMA 11 is written into DMA 1 at SDMAP, either true or complemented, controlled by AC, using states of IDMAE±. Contents read into central processor AC by IOT 624 (DMAC). Cleared by SCLP 2. Note that EMA bit 0 is loaded and read back to and from the central processor with these instructions but is not shifted.
DMB	Disk Memory Buffer. Twelve-bit flip-flop register which contains (during write) the data word to be written on the disk, or is loaded (during read) with the data word on the disk. Loaded with the content of the MBH by LDMPB, during write. Contents of bit 11 generates BDDMB which is used to control writing. During read, contents of each disk bit generate BMBI, which represents the data bit on the disk. The contents of BMBI are strobed into DMB 0 by TAP. Contents of the DMB are shifted one position toward DMB 11 by SDMBP. Cleared by IOT 604 (DMAW), R/W (1), and BTCS-.
DRE	Data Request Enable flip-flop. Must be set to allow address search, inhibits data transfer when clear. Set by TCD going to 0, or by LDMAP, if PCA is true. Cleared by DCF (1) or SCLP. Also cleared by EMA 6 going to 0 (level).
DRL	Data Request Late flip-flop. Error indication when set. Set by DEP if DBR is set. Cleared by SCLP 1.
EA 1, 2, 3	Extended Address flip-flops. Set to indicate selection of central processor extended memory fields. Set by IOT 614 (DIML) and contents of central processor AC 6 through 8. Cleared by PCL or IOT 611 (DCIM).
EIE	Error Interrupt Enable flip-flop. Set by IOT 614 (DIML) if central processor AC 3 is set. Cleared by PCL or IOT 611 (DM IM). Error selected for interrupt by setting EIE are: DRL, PER, WLS, and NXD.

Table D-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
EMA	Extended Memory Address register. Nine-bit flip-flop register whose contents select the disk (of 4 possible) and track (of 128 possible) for data transfer. EMA 1 through 8 is loaded with the contents of central processor AC 11-4 by IOT 642 (DXAL). EMA 0 is loaded with DMA instructions. Cleared by CEMAP. EMA 0 is also cleared by SCLP 2. Incremented by HSE (1). EMA bits 0 through 6 select track. Bits 7 and 8 (corresponding to central processor AC bits 4 and 5) select disk.
ERROR	Indicates error in operation. True for any of the following: DRL, PER, WLS, NXD.
HSE	Head Switch Enable flip-flop. Set by TEP, if ADC and WCO are set, to indicate end-of-track during data transfer. Cleared when ADC goes to 0, or by SCLP 2.
IDMAE and IDMAE-	Increment Disk Memory Address Enable levels. Used for address search and for incrementing the contents of the DMA. Polarity controlled by contents of DMA 11 and ACH. When ACH is set, IDMAE is true with respect to contents of DMA 11. When ACH is clear, IDMAE is the complement of DMA 11. Contents of IDMAE are compared with BTBH during address search. Contents of IDMAE are placed in DMA 1 at SDMAP. IDMAE- is IDMAE inverted, used by exclusive OR gate when searching for address to indicate DMA 11 (0) and to write a 0 into DMA 1.
IOT	Input/Output Timing pulse. Generated by IOP 1, 2, or 4, when present, and BMB 3 through 8 decoded to equal octal 60_8, 61_8, 62_8, or 64_8.
LDMAP	Load Disk Memory Address Pulse. Generated by IOT 602 (DMAR) or IOT 604 (DMAW) to load contents of central processor AC into DMA and EMA 0.
LDMPB	Load Disk Memory Buffer Pulse. Loads contents of MBH into DMB during write mode. Generated by WEP if ADC (1) and R/W (1).
MBH	Memory Buffer Hold register. Twelve-bit flip-flop register which buffers data between central processor and DMB. Cleared by CMBHP. Loaded in read mode with contents of DMB 0-11 by RLMBHP at end of data word on disk. Loaded with contents of central processor BMB 0-11 in write mode by WLMBHP during data break. The contents of MBH are strobed into central processor MB during read by central processor logic and into DMB during write by LDMBP.
MRS	Memory Request Synchronizer flip-flop. Controls 16-word holdoff of DRE set by TCA, TCB, TCC, and TCD. Set by LDMAP or EMA 6 going to 0 (pulse) if DRE (1) is present. Cleared by SCLP 1 or DRE going to 1. When set, MRS allows TCA to be toggled.
NXD	Nonexistent Disk. Error indication. True, if disk selected by EMA 7 and 8 is not installed in system. If four disks are installed, NXD will not go true, and one of the four disks will always be selected by EMA 7 and 8.
PCA	Switching Gap Gate. Goes true during 550 ± 50 μs gap in disk between tracks. Used to select direct set of DRE when PCA is true and LDMAP occurs.
PCA (track generator)	Photocell flip-flop. (Maintenance) Set by TGP, if BAC 6 is set. Cleared by SCLP 2.
PER	Parity Error flip-flop. Set to indicate read parity error. Set if R/W is clear, and ADC and BPAR are set, strobed by TCP.
PIE	Photocell Interrupt Enable flip-flop. Enables interrupt when switching gap gate is present. Set by IOT 614 (DIML) when central processor AC 4 is set. Cleared by IOT 614 (DCIM) or PCL.

Table D-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
ROFP	Read Overflow Pulse. Indicates last read data transfer. Set by central processor WCO pulse when R/W is 0.
R/W	Read/Write flip-flop. State determines data transfer direction. Set by IOT 604 (DMAW) for writing; cleared by IOT 602 (DMAR) for reading. Also cleared by SCLP 1.
SAD	Search Address flip-flop. Set to allow generation of SDMAP pulses. Set by first TAP pulse of each address word, if SAD is clear and DRE is set. Cleared at end of each address word by WDE. Set is delayed 60 ns to inhibit generation of SDMAP by first TAP pulse.
SCLP 1 and 2	Start-Clear Pulse. Generated by power clear (PCL) or IOT 601 (DMAC). Clears data transfer logic and DMA.
SDMAP	Shift Disk Memory Address Pulse. Generated by TAP if SAD is set. Pulse generated by a flip-flop which clears itself through a delay loop. Eleven SDMAP pulses are generated per address word.
SDMBP	Shift Disk Memory Buffer Pulse. This pulse shifts the contents of the DMB one position toward DMB 11. Generated by TAP if ADC is set. Pulse generated by flip-flop, cleared by delay loop.
TAP	Track A Pulse. Main strobe-timing pulse for the system. Generated by timing track A of the disk. There are 13 TAP pulses for each address word.
TAG	(Maintenance) Track A Generator flip-flop. Complemented by TGP, delayed if BAC 11 is set. Cleared by SCLP 2.
TBG	(Maintenance) Track B Generator flip-flop. Complemented by TGP, if BAC 10 is set. Cleared by SCLP 2.
TBH	Track B Hold (also BTBH). Contents of address track read serially from disk. Compared during address search with IDMAE to locate track address. Comparison circuit operates after ADC is set, but has no logical effect on data transfer.
TCA, TCB TCC, TCD	Time Counter flip-flops A, B, C, and D. Four-bit counter which delays setting DRE until 16 words have passed, after LDMAP. TCA toggled by WEP when enabled by MRS (1). Binary chain from TCA to TCD. TCD going from 1 to 0 sets DRE. Counter is held at 00002 by resetting MRS after 16th count. Cleared by SCLP 1.
TCG	Track C Generator flip-flop (maintenance). Complemented by TGP delayed if BAC 9 is set. Cleared by SCLP 2.
TCP	Track C Pulse. Generated by BTCS+ at bit-time 14 of each address word. Denotes end of address word.
TEP	Track End Pulse. Generated by 1 in timing track B at bit-time 13, while WDE is 1. This address is 10000_8, which is the address content of special address at the end of the track.
TGP	Track Generator Pulse (maintenance). Generated by IOT 642 (DMMT), if MB 9 is set. TGP controls generation of other maintenance pulses.
WCO	Word Count Overflow flip-flop. Set by LDMAP to indicate data transfer in process. Cleared by LDMBP and WCS (1) during write. Cleared by ROFP during read. Delay during write allows last data word to be written on disk. WCO (0) and DEP (1) indicates the actual end of data transfer by setting DCF.

Table D-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
WCS	Word Count Synchronizer. Cleared by LDMAP. Set by WCOP when Word Count Register is incremented to 0. During write, WCS indicates the WCO has occurred, and allows clearing WCO at next LDMBP. During read, WCS and WCO are complemented simultaneously.
WDE	Write Data Enable flip-flop. Set by BTCS- at bit-time 12. Cleared by WEP at bit-time 14. Set to inhibit writing data on disk and to write parity bit.
WEPD	Word End Pulse Delayed. Generated by WEP, delayed 50 ns.
WLMBHP	Write Load Memory Buffer Hold Pulse. Generates pulse which loads MBH with data stored in the central processor MB. Generated when R/W (1) and B Break true are strobed by T1. Generation of this signal is controlled by the central processor data break.
WLS	Write-Lock Status. True, when the contents of the EMA select a head in the disks which has its associated WRITE-LOCK switch set for lock which denotes an error signal.
WTE	Write Enable. True, when ADC (1) and R/W (1) are set. Level must be true to allow writing on the disk. When level is false, no write current passes through the disk head.

Appendix E
Timing Track Writer

E.1 TIMING TRACK WRITER RS-08-TA

The procedures for using the portable Timing Track Writer are provided for reference purposes only. When using the Timing Track Writer, the G085 Disk Read Amp and Slice Module output level vary because the input signal strength is dependent on the recorded level on the disk. The following procedure is an aid in using the portable Timing Track Writer.

Step	Procedure
1	Apply 115 Vac power to the Timing Track Writer cooling fans.
2	Before applying dc power, be certain that the WRITE ENABLE switch is in the OFF position.
3	Apply dc power to the unit, then plug the timing track cable connector into the Timing Track Writer.
4	Connect channel 1 of the oscilloscope to J1 and set the display to produce 5V per cm, with a time base of 0.5 ms/cm. Do not set the oscilloscope on ADD and use the time base for accuracy.
5	If the ac line voltage to the disk motor is obtained from a 60-Hz source, set the CYCLE SELECT switch to 60.
6	Enable the write and read amplifiers, then depress the WRITE switch.
7	Adjust the clock pulse by means of the FREQ CONT control. The clock rate is 1160 ns for 60-Hz power and 1390 ns for 50-Hz power. When the pulse gap width is 550 $\pm$ 50 µs, the clock is correctly adjusted. To observe the pulse gap width change, it is necessary to write every time the FREQ CONT control is rotated.
8	The first signal appearing at J1, J3, and J5 is negative going with a complementary signal appearing at J2, J4, and J6.
9	Depress the WRITE button and observe that all data tracks disappear for approximately 100 ms, followed by rewriting. Recheck the data tracks, as out-lined in Step 8, for the regular and spare tracks.
10	Disable the write and read amplifiers.
11	Turn off ac and dc power to the Track Writer and disconnect the timing track cable.

digital CONTINUATION SHEET

TITLE Addendum to "RF08 Adjustment Procedure" Dated October 8,1969

With the introduction of the GØ85D to the RSØ8 on a phase-in basis, it is imperative that one can distinguish a GØ85B from a GØ85D and a GØ85B modified to Revision D.

The major differences are the substitution of 1500pf capacitors, Rev. D, for 330pf caps., C11 and C12, Rev. B. The Rev. D board also has C3 and C6 removed, C7, C8 removed and jumpered. The GØ85D replaces R54, 562Ω, with a IN751A zener diode.

There are two very obvious differences on an ordinary GØ85B and a GØ85B modified to obtain the electronic characteristics of a GØ85D. The modified board has the two 1500pf caps., C11 and C12, there are two D664 diodes wired "back-to-back" across C4, and C3, C6 removed.

The maximum amplitude of 12v. p/p cited in the specification is for the GØ85D or modified GØ85B. For the normal GØ85B, the maximum amplitude is 9v. p/p.

In the GØ85D or modified GØ85B,the minimum amplitude is to be 4.5v/ p/p, in the GØ85B, the minimum amplitude is 4.0v p/p.

	SIZE	CODE	NUMBER	REV
	A			

DEC FORM NO
DRA 108A

SHEET ____ OF ____

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 1/28/70

TITLE Adjustment Procedure RF/RSØ8

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

PRELIMINARY COPY

ENG	APPD	SIZE	CODE	NUMBER	REV
		A			

DEC FORM NO

TITLE Adjustment Procedure RF/RSØ8

Scope: This document specifies adjustment procedures for all adjustmens in the RFØ8 and RSØ8. It is intended as a guide to production personnel and as a supplement to the RFØ8/RSØ8 Maintenance Manual (Maindec-08-H5DA-D)

Equipment:
Tektronix 453 with two 10X probes with ground clops.
Disk Data (Maindec-08-D5EA).

RSØ8 Adjustments

I. Timing Tracks and Data Track Timing
Module type - GØ85
Location AØ2 - BØ2, AØ3 - BØ3, AØ4 - BØ4, A12 - B12

A. Gain Adjustment - Timing Tracks

1. Check 453 calibration, 1v/cm. It is very important to compensate probes properly.

2. Ground scope to ground pin of amplifier being measured.

3. Trigger scope on LINE, 5ms/cm sweep speed, DC coupled Mode - Channel 1 only 0.2v/cm vertical (effective gain 1 volt/cm with 10X probes).

4. Measure amplitude at AØ2T. Adjust gain pot of GØ85, "A" section pot, for an average amplitude of 7 volts, peak to peak. See figure 1.

5. Repeat step 4 for:

A. AØ3T - GØ85 in locations AØ3 - BØ3. See figure 2.
B. AØ4T - GØ85 in locations AØ4 - BØ4. See figure 3.

B. Slice Adjustment - Timing Tracks

1. Prior to setting the slice the positive overshoot must be recorded. Set 453 as follows: Ch 1 only, 0.1v/cm DC coupled, 2µs/cm, Trigger internal AC.
(Check for proper compensation of probes at this time).

2. Place probe on BØ2E for TTA measurement (BØ3E - TTB, BØ4E - TTC).

1. Using RS-08-TA drawings and RS-08-TA functional description, employ the following procedure to align and checkout the RS-08-TA Timing Track Writer.

2. Before applying power, -15v, +10v, +20v, check to see that the "A" pin bus strip has been removed between modules 21 and 22 in both A and B level. The G085's have +20v present on pin A; all other modules, +10v.

3. Apply 115v AC for fans.

4. Apply power and check voltage levels.

5. Check to see if "write enable" switch functions properly.

6. With DC power removed and "write enable" off, connect the timing track cable to the jack on the panel.

7. Apply DC power.

8. Enable the writers, then press write PB.

9. Monitor all six jacks, J1-6, both regular and spare tracks. Adjust amplitude of the pulses at R21 of the respective G085's for 10v P/P. Do this with scope on "add" with B trace inverted.

10. Monitor J1. A gap should appear in the pulse train. It should be 550 usec $\pm$50 usec. This can be adjusted by varing the frequency. The write PB must be pressed after each time the frequency is changed. This gap appears on all timing tracks, regular and spare, simultaneously.

11. The first pulse after the gap should be negative going at J1, J3, and J5. The complements are on J2, J4, and J6.

12. Since the RS08 uses NRZI writing, a pulse will be seen only for a true bit, i.e., at "1". Track A consists of 13 ones followed by a zero. This pattern holds true for every address (sector) on the disk. Track B counts from 0000_8 to 3777_8 and cannot readily be seen with a scope. It can safely be assumed to be working if the EOT pulse, bit 12 of last address, is generated. Track C writes a "1" every bit 11 and 13.

13. Perform several write cycles and observe as in step 11 to insure proper operation.

14. After checkout is completed, place "write enable" to off.

15. Remove power from RS-08-TA.

16. Remove Timing Track cable connector.

TITLE RS-08-TA Timing Track Writer Usage Procedure

1. Apply 115v AC power to fans.

2. Before applying the DC power to the RS-08-TA Timing Track Writer, insure that the "write enable" switch is in the "off" position.

3. Plug the timing track cable connector into the RS-08-TA; then apply power to the unit.

4. Monitor the A track at J1 with the input set for 5v/cm and time base of .5msec/cm. Do not set the preamp mode to ADD. Use time base magnification for accuracy.

5. For 60 Hz AC power to the disk monor, set the frequency switch on the RS-08-TA to "60".

6. Enable the writers; then press "write".

7. Adjust the clock by means of the Frequency Control pot. The clock rate for 60 Hz disk power is 1160 nsec, for 50 Hz power the clock rate is 1390 nsec. When the gap is 550 usec wide, the clock is correct. A tolerance of $\pm$ 50 usec is permissible. To see the gap change, it is necessary to "write" every time the Frequency Control Pot is rotated.

8. The first signal on J1 is a negative going signal. The same applies to J3 and J5. A complementary signal is found on J2, J4, and J6.

9. Press the "write" button. All tracks should disappear for approximately 100 msec, then be written again. Check the tracks once again as in the previous step for <u>both</u> regular and spare tracks.

10. Disable the writers.

11. Remove power from RS-08-TA.

12. Remove the Timing Track Cable.

NOTE: The output level of the G085's will vary since input signal strength is dependent on recorded level on disc.

1. B. Cont.

3. Position the display vertically so the baseline is on the center horizontal graticule. Place the trailing edge of the waveform on the center vertical graticule.

4. Measure and record the difference between the baseline and the positive transition over the baseline of the trailing edge.

5. Change 453 setup - Channel 1 - 0.1v/cm, DC coupled
Channel 2 - 0.1v/cm, DC coupled
Mode - ADD (Do not invert)
Trigger - Internal AC, Ch. 1 only
Sweep speed - 2µs/cm
Check for proper compensation of both probes.

6. Connect channel 1 probe to AØ2T, ground this probe to AØ2C; Channel 2 probe to BØ2E, ground this probe to BØ2C.

7. Change the sweep speed to 2ms/cm and center the display about the center horizontal graticule of the CRT. Return sweep speed to 2µs/cm and adjust sync for a stable display.

8. Subtract overshoot of trailing edge of slice waveform, as recorded in step 4, from amplitude of trailing edge of sliced analog waveform. See figure 6.

9. Adjust the slice pot on the BØ2 - GØ85 for a slice. level fo 1.35 volts above the baseline. See figure 4.

10., Repeat this procedure for TTB and TTC, AØ3 - BØ3, AØ4 - BØ4, respectively. Use pins AØ3T - BØ3E and AØ4T - BØ4E for measurements. Use correct ground pins. Refer to figures 5 and 6.

C. Guard Band and PCA Adjustment

1. Set 453 up as follows: Channel 1 - Ø.1v/cm, DC coupled
Channel 2 - Ø.1v/cm, DC coupled
Mode - ADD
Trigger - Internal, DC negative, Channel 1 only
Sweep speed - 5Øµs/cm

2. Place Ch. 1 probe on BØ8M of RSØ8; Ch. 2 on AØ2T

C. Cont.

3. Sync scope and adjust upper pot on BØ8 until negative going square wave is 1ØØµs duration. (This is a minimum value - 11Øµs will provide more reliable results.)

4. Vary the pot on BØ7 until the single spike appears centered on the square wave. This insures a proper guard band.

D. Data Track Gain - AGC Equalization

1. In order to perform the adjustment correctly, the RFØ8/RSØ8 system must be able to write all ones on every track, and read (errors permissable) on each track.

2. Write all ones on all tracks using SA201 subroutine of Disc Data Diagnostic.

3. Connect Channel 1 to A12T, vertical 0.2v/cm. Set sweep speed to 2ms/cm trigger on LINE. Gnd strap to A12S.

4. Using track selection subroutine, SA0265, of Disk Data adjust gain pot of A12 - GØ85 to obtain a reading of 7 volts P/P on track ØØØ.

5. Using the track selection subroutine measured and record the amplitudes of all tracks on the "RSØ8 Amplitude Sheet". After completion of measurements scan the amplitude sheet. Using AGC jumpers, equalize track amplitudes as required. When this is done, set gain so track of highest amplitude is 12v/p/p.

NOTE: In NO case should any track amplitude exceed 12 volts p/p or be below 4.5 volts. If either of these conditions exist, adjust the gain of A12 - GØ85 to compensate, then repeat step 5. If not met, unit must be rejected, and change head of low or high TK.

E. Preliminary Slice Adjustment - Data Tracks

1. Setup the 453 in the manner prescribed in I.B.5 of this procedure. (Be sure to measure overshoot.)
2. Use SA201 subroutine to read all ones on the disc.
3. Set DC Data, B2ØF, to 5ØØ ns.
4. Set DC Wind, B11F, to 5ØØ ns.
5. Set B3Ø1 - B19F to 5ØØ ns.
6. Set slice level B12 - GØ85 to 1.35 volts.

II. Data Gating Adjustment

A. TASD

1. Channel 1 on TC TAS (B1ØL)
   Channel 2 on TC TASD (B1ØN)
   Trigger - Internal, AC, negative, Ch. 1 only
   Mode - Alt. sweep, 1ØØns/cm.

2. Adjust the variable delay B312, location B10 to obtain a 25Ø ns delay on Ch.2. See figure 5.

   NOTE: Anyting the gain or slice on TTA is changed, this adjustment must be made.

B. DC Wind

1. Monitor B11F with Ch. 1 of scope and adjust B3Ø1 location B11 for a 5ØØ ns output.

C. DC Data

1. Using track selection subroutine, select track ØØØ.

2. Monitor B2ØF with Ch. 1. Adjust for a 500ns output.

D. DC DOP Optimization

1. Place Ch. 1 on B19T.

2. Place Ch. 2 on B2ØF, DC Data.

3. Select each track on the switch register, recording the delay of DC DATA from TC TAP.

4. Place Ch. 1 on B11F, DC WIND.

5. Alternately switching to the tracks with the least and most delay from TC TAP, as recorded previously, adjust the pot on B19 - B3Ø1 until the coincidences of DC WIND and DC DATA are equal.

6. Place Ch. 1 on AØ7H, DC DOP. (Trigger Positive)

7. Observe the two tracks monitored on Step 5. If either of the two tracks produces a DC DOP of less than 2ØØns, the head corresponding to that track must be changed.

II. E. Final Slice Adjustment

1. Raise the slice level (B12 - G085) until dropouts first appear. Record this level.

2. Use SA201 subroutine to write all zeros on the disc. The use the read option. Do not alternately write and read.

3. Lower the slice level until a bit pickup occurs. Record this level.

4. Taking the levels recorded in steps 1 and 3, find the average of the two and set the slice for this level.

III. Additional Adjustments

Success in adjusting the system is very dependent on relating a given observation to some definable cause. Specific problems and suggested procedures are outlined below.

A. Bit Pickups

1. Slice too low. Increase slice level using same procedure as prescribed in I.D. A good way to compromise the slice adjustment is to test for dropouts with a 5252 pattern and check for pickups with a 5252 or 4001. After this is done, perform II, D again. If a bit pickup persists, use a write/read single word transfer, writing zeros. To locate and observe the failing DMA, sync externally to B21N (ADC) in the RF08 and observe A12T. If a varying amplitude "glitch" appears, record the track, and reject the unit for a bad head. (The ferrites are not properly grounded.)

2. Gain too high. Reduce gain - I.C. Check slice, check DOP.

3. Plating imperfections. Error always occurs in specific track and DMA. May be localized to a single bit. Trigger scope exernally on ADC, B21N in RF08. Look at A12T with Disc Data set to read a one word transfer on the failing DMA. A stable sinusoidal "Glitch" present indicates a hole in the magnetic recording surface. Reject the disk if the amplitude is sufficient to produce an error in step I.D.

III. A. 4. Enviornment - Line transients usually cause bit pickups, causing random errors. However, since the disk is precisely synchronized to the AC line frequency, period errors can be caused by devices such as proportionally controlled heaters.

5. Matrix failures - sweep test G285 and G286 boards.

B. Bit Drops

1. Slice too high, check sect. I.D.

2. Gain too low, check sect. I.D.

3. Plating induced dropout. Record all ones if the error persists in a given EMA and DMA. Setup scope as in III, A, 3. If a sudden decrease to 50% or less (several bits in length) amplitude is observed, there is a dropout on the disk surfaces. If this dropout is below 4.5 volts p/p reject disk.

DEC FORM NO
DRA 108A

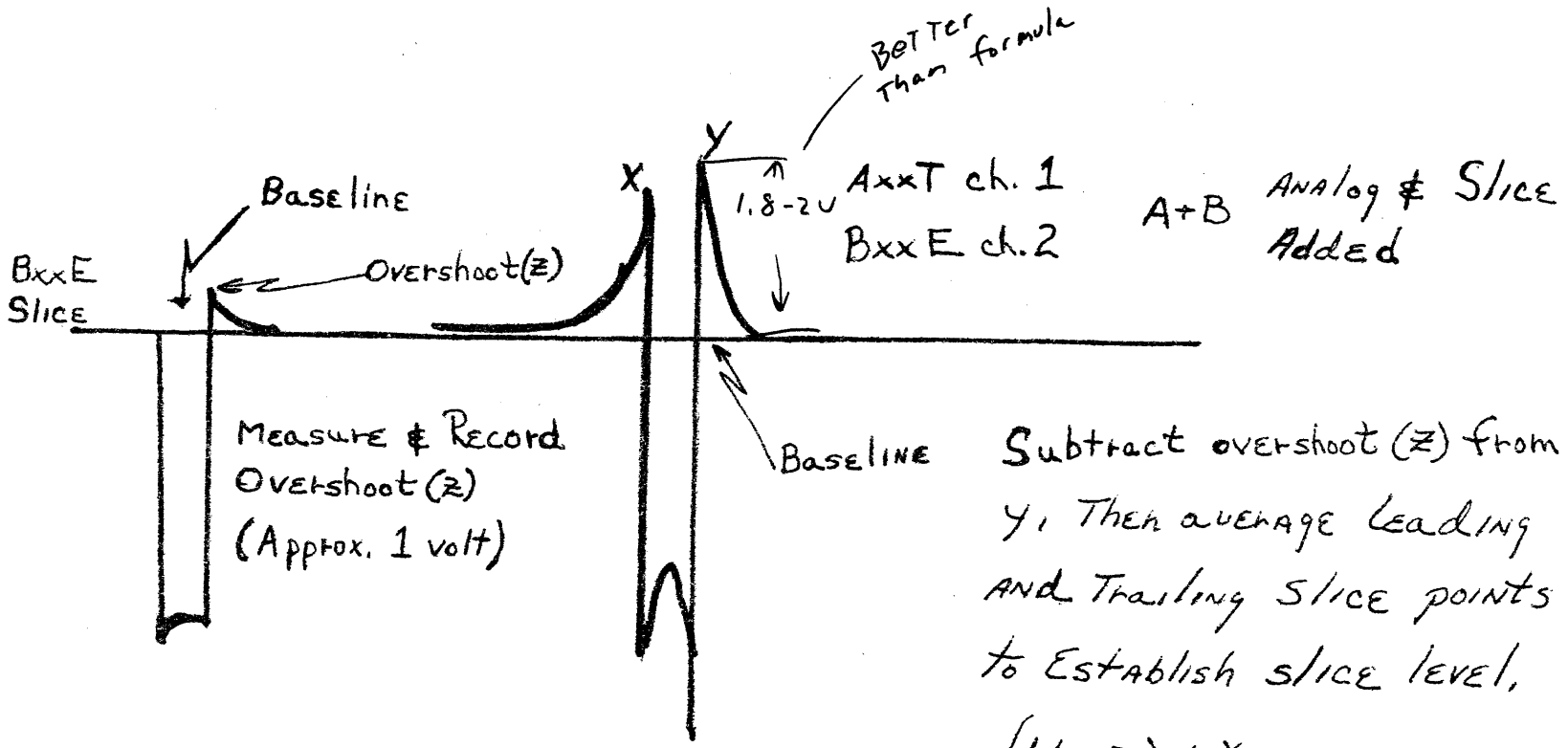
TITLE

CONTINUATION SHEET

SIZE A | CODE | NUMBER | REV

SHEET ____ OF ____

Slice Adjust
fig #6



Subtract overshoot (z) from y, Then average leading and Trailing slice points to Establish slice level,

$$\frac{(y-z)+x}{2} = \text{slice level}$$

PROGRAMMING DEPARTMENT MEMO #080-221-001-01

ADDENDUM TO DISK SYSTEM MANUAL

RF08 DISK

I. GENERAL

The RF08 Disk is a large version of the DF32. There are some minor difference in the way you program them and therefore changes in Disk I/O handlers are required. The Disk Monitor System has two handlers: one in the BUILDER and one in PIP. Both must be modified. The modification scheme for the non-interrupt BUILDER handler is an overlay patch. The modification scheme for the PIP interrrupt handler is a conditional assembly of PIP. This was done because of the significant differences between RF08 and DF32 hardware with the interrupt on.

II. BUILDING A RF08 SYSTEM

Load the BUILDER (Version 9A or later) tape. Load the RF08 Patch and follow the technique shown in the DISK MONITOR Manual, Appendix A. There is one difference in the dialog shown in the Manual: The question "PDP-8/S?" is changed to "RF08?". Answer this "YES". Answer the question.

"TYPE NUMBER OF DISK UNITS"

by typing "4" (See Figure 1)

III. Assembly of PIP (PØ212A* or later versions) for RF08 and DF32

A. RF08

Using the Assembler PAL8 (8K Pal-D Assembler) or PAL 10 (PDP-10 PAL-D create a file with one line in it:

RF08=0

This should be assembled in front of the source of PIP and will correctly generate a PIP Binary tape for the RF08 disk.

B. DF32

Assemble the source of PIP on the assemblers in Part A but without the file containing the statement:

RF08=Ø

*This version ID (as in all DISK Programs) on the first page of the listing. It means P-PIP, 02-February, 12-12th day, A- A version.

IV. Operational Characteristics of these Changes.

There are no operational difference between the RF08 and DF32 systems.

V. Configuration of RF08 System

The RF08 Disk Monitor System has 128K words (4 DF32 Disks) available to the user. The upper 128K of DISK Ø and subsequent RS08 units are not currently used or accessible by the user.

VI. Expansion Capability

The unit number position in the argument in the RF08 Disk Handler is implemented although not used currently. The command decoder has been expanded for future inclusion of DISK units 1-7, i.e. second through eighth 128K "DISK" but has been jammed to believe in only DISK Ø. A user may manually patch the command decoder to accept upper disk units and PIP will correctly copy into DISK "units" 1-7 (just as DECtapes are used). The user must also generate correct DN and SAM Blocks in Disk 1-7, justaas he must generate DN and SAM Blocks on DECtapes before they are used.

```
*TYPE SIZE OF CORE (IN K)
*4
*HIGH SPEED PAPER TAPE?
*YES
*RF08?
*YES
*DISK?
*YES
*TYPE NUMBER OF DISC UNITS
*4
*TAPE?
*YES
```

FIGURE 1

PACKAGING INSTRUCTIONS

1. Install and tighten motor lock.*
2. Disconnect blue, green, red, yellow, and black leads.
3. Wrap leads around motor housing and tape in place.
4. For disks with protruding ground screws, punch hole in neoprene gasket to accept 10-32 screw head.
5. Thoroughly clean,dust and remove foreign matter from desiccant pan.
6. Remove backing from one side of gasket, align punched hole on gasket with screw head depression on desiccant pan flange and fix gasket firmly to pan flange.
7. Place one 8-ounce bag Drierite desiccant into pan.
8. Remove remaining backing from gasket, place pan over disk motor, align screw depression on pan flange with screw head (if any,) and fix pan firmly to disk casting.
9. Using PERMACEL silver cloth tape, tape around entire flange area to secure pan to disk casting.
10. Remove air filtration hose and cap opening to seal disk from outside environment.

UNPACKING AND INSTALLATION INSTRUCTIONS FOR RS08

1. Remove silver cloth tape from pan containing desiccant (Drierite) and remove pan from motor.
2. Unwrap blue, green, yellow, red, black motor leads from motor.
3. Connect these wires to the proper color coded connections on the back of the RS08P motor control chassis.
4. Remove the motor lock.*
5. Turn the motor switches on the back of RS08P motor control chassis to OFF.
6. Be sure that the circuit breaker on the H718A Line Filter is OFF,
7. Insert power cord in the proper AC receptacle.

8. Switch the H718A Line Filter circuit breaker to ON. At this point, the hose on purge unit has not been connected and the act of turning the power on essentially purges the purge unit before connection is made to the disk unit. This purging should be done for at least ½ an hour. The disk motor should not be on.

9. After the purge period, remove the cap from disk unit, connect the purge unit hose to the disk unit, and turn the motor control chassis switch to ON. The disk should start rotating at this time.

* Note - Motor Lock is located on bottom of motor SHAFT

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