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PDP-8

AX08

LABORATORY PERIPHERAL
INSTRUCTION MANUAL

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AX08

LABORATORY PERIPHERAL INSTRUCTION MANUAL

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Type AX08 Laboratory Peripheral

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The AX08 can be considered either a multi-purpose PDP-8-series peripheral or as an integral part of the Lab-8 Hardware/Software System (PDP-8 or 8/I, AX08, Lab-8 Averaging Program. The AX08 provides a facility for monitoring up to four channels of analog information (expandable by option, see Paragraph 1.4), performing analog-to-digital conversion (ADC) for data storage at the computer, performing digital-to-analog conversion (DAC) on inputs from the computer for display, sensing time through two real-time clocks, and sensing digital inputs. For ADC, the AX08 uses the successive approximation technique. Standard PDP-8 I/O instructions initiate and monitor the operations of the AX08.

This manual provides a description of operation, programming, theory, and maintenance of the AX08. The level of discussion assumes familiarity with the PDP-8 Programmed Data Processor and a working knowledge of DEC logic symbology.

1.2 PHYSICAL DESCRIPTION

The AX08 is housed in a single cabinet designed especially to provide simple interconnection and easy access to logic modules. The back-wired panels provide interface with the PDP-8 type computers. The signal connections to the computer or to other external equipment are made via DEC cable connectors that plug directly into module slots. A control/indicator panel is located on the front of the AX08.

Power is supplied from either the computer or from a standard DEC power supply. Reference power -10V for ADC and DAC is provided by DEC Type A704.

1.2.1 Physical Characteristics

Dimensions:	Panel Width - Standard 10-1/2 in. Panel Height - Double Rack Depth 18-3/4 in.
I/O Cables:	DEC Type W011 or W021 modules located per drawing (see UML, Chapter 5)
Power:	Module power is supplied by Type 728 or (for 50 Hz operation) 728A power supplies. If the PC 8/I option is selected, the Type 779 or (for 50 Hz operation) 779A power supply is also provided. Reference voltage is provided by an A704.

1.3 FUNCTIONAL UNITS

The AX08 provides a 9-bit display with two axes and intensity control (see Paragraph 1.4), a 9-bit ADC with four channels of multiplexed input (expandable to 24) incorporating preamplifiers and sample and hold.

The basic operational flow is shown in Figure 1-1. Channel selection is accomplished by decoding IOT instructions from the computer, and conversion is controlled by command, timing, and control sequences of the computer and AX08 logic; completed analog-to-digital conversions are sent from the Y-register, through the input mixer to the computer. Computer inputs through the buffer are controlled through decoded IOT instructions and AX08 logic to provide analog outputs for display. Both ADC and DAC use the same registers and in case of simultaneous requirement, ADC has priority.

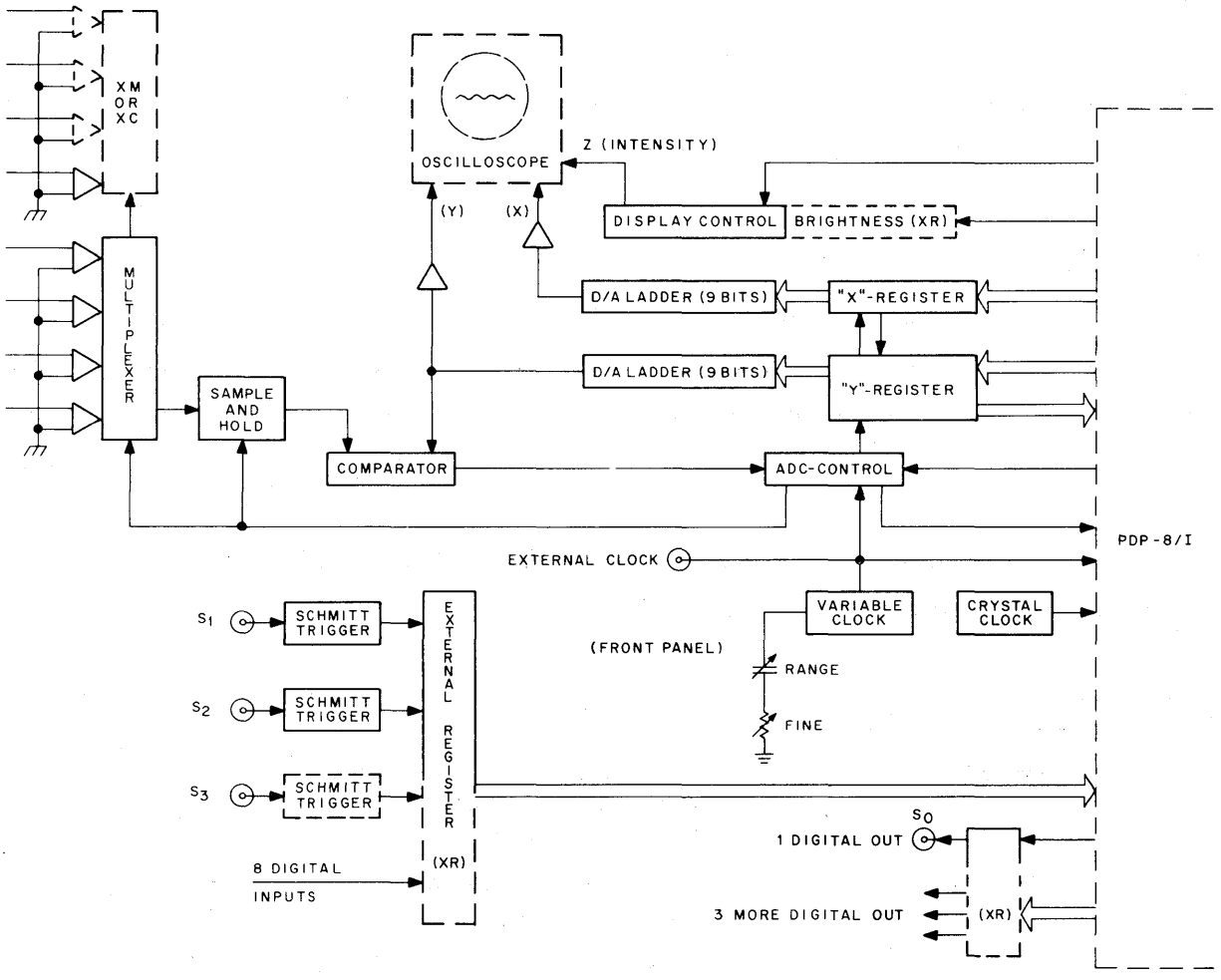


Figure 1-1 AX08 Operational Flow Diagram

The interrupt and control scheme for this is described in Chapters 2 and 3.

1.4 OPTIONS

The following options may be added to the AX08:

OPTION XR - This option expands the registers of the AX08 to include three levels of brightness control on the scope, eight digital inputs (contingency), three digital outputs and one additional pulse input. A single XR may be added to an AX08.

OPTION XM (Multiplex expansion) - The first four channels of additional analog input are included in Option XM. This includes the preamplifiers, additional multiplexing and expansion of the channel selection register. A single AX08XM may be added to an AX08.

OPTION XC - This option is for the expansion of the ADC channels beyond eight. Each AX08XC adds four channels of preamplified multiplexed analog input. Four option XC's may be added to an AX08 with XM option.

1.5 SYSTEM CHARACTERISTICS

The following tables define the major operating characteristics of AX08.

Table 1-1
Operating Characteristics
Analog-to-Digital Conversion

Conversion	Successive approximation
Word Length	9 bits including sign
Accuracy	±1/2 LSB ±0.2%
Speed	$\leq$ 17 μs
Preamplifier Input	±1.024V full scale, 50K input impedance
Sample and Hold	Full scale track in 2 μs
Number Notation	Signed 2's complement
Clocks	
Crystal Clock	Set to 100 μs
RC Timing Clock	Variable from 2 sec to 20 μs

Table 1-2
Power Requirements and Environment

Reference Voltage	-10V nominal
Input Power	Std. DEC voltages
Operating Temperature	0°C to 50°C

Table 1-3
A-D Conversion

Analog Input Voltage (±2 mV)	Digital Output (signed 2's complement) (±1/2 LSB)
+1.020	0377
+0.768	0300
+0.512	0200
+0.256	0100
+0.004	0001
+0.000	0000
-0.004	7777
-0.256	7700
-0.512	7600
-0.768	7500
-1.024	7400

1.6 REFERENCE DOCUMENTS

Title	Document No.	Description
Digital Logic Handbook	C-105	Specifications and descriptions of FLIP CHIP modules, simplified explanation of the selection and use of these modules in numerous applications.
Small Computer Handbook (1967/1968 Edition)	C800	Describes operation and programming of PDP-8/I computer.
PDP-8 Interface Manual	F-85	Contains computer organization information, detailed description of all instructions, basic PDP-8 programming data, and operating procedures.
AX08 Bulletin		Contains operation and programming data at the user's level.

CHAPTER 2
OPERATION AND PROGRAMMING

2.1 GENERAL

This chapter contains operation and programming instructions for the AX08. Since the AX08 is a special I/O device for the PDP-8 series of computers, refer to the applicable documents of PDP-8 literature for programming information.

2.2 CONTROLS AND INDICATORS

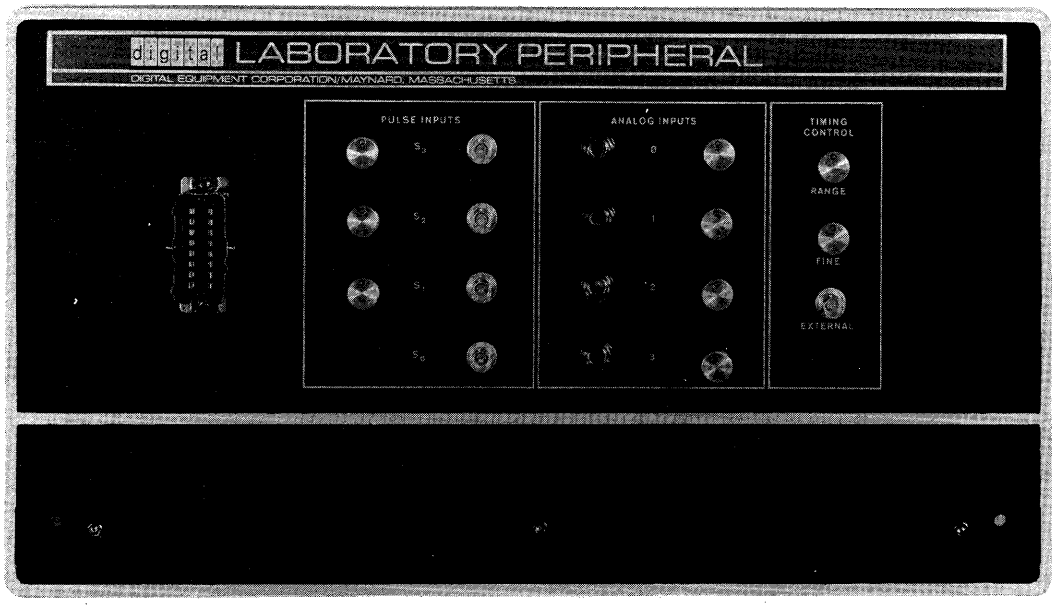


Figure 2-1 AX08 Front Panel Controls

2.3 ENABLE REGISTERS

The Enable Register is used to

a. Selectively enable interrupts for the ADC, the ADC timing error indicator, Schmitt triggers, the crystal clock and the RC clock.

b. Initialize and run the RC clock.

c. Shift between two speeds of the RC clock.

d. Provide automatic initiation of ADC upon RC or external timing pulses.

e. Enable an external clock pulse to set the RC clock flag (and cause ADC if enabled).

2.4 I/O INSTRUCTIONS

The AX08 IOT instructions are called by PDP-8 IOP 1, 2, and 4 pulses. A complete discussion of PDP-8 programmed data transfers, including IOP 1, 2, and 4 generation is contained in Chapter 2 of the PDP-8 User's Handbook.

The PDP-8 instruction op codes for the AX08 IOT's are of the form: 63AB, where A represents bits 6 through 8, and B represents bits 9 through 11 of the instruction word. All AX08 instructions are IOT instructions. Table 2-1 lists the IOT instructions and defines them in terms of IOP 1, 2 and 4 control.

Table 2-1
AX08 IOT Instructions

IOT Instruction	IOP 1	IOP 2	IOP 4
630X	DXC Clear X Register	DXL Load X from AC	DIS (6304) Intensify point
631X	DYC Clear Y Register	DYL Load Y from AC	DIS (6314) Intensify point
632X	SKXK Skip on Crystal Clk flag	SKER Skip on ADC timing error - convert command received when last conversion not yet read into AC	DSB (OPT XR) Set Brightness DSB 0 = dim DSB 1 = normal DSB 2 = bright
633X	XRIN OR external sense register into AC	SKAD Skip on ADC done	XRCL Clear all bits of external sense register that correspond to set bits in AC
634X	SKRK Skip on RC timing clock flag	ZTEN Zeros in AC clear bits in Enable Register	OTEN Ones in AC set bits in Enable Register then AC is cleared
635X	CLER Clear ADC timing error flag - and error condition 0 $\longrightarrow$ ADCERR, 0 $\longrightarrow$ ADCIP	CLXK Clear crystal clock flag	CLRK Clear RC clock flag

Table 2-1 (Cont)
AX08 IOT Instructions

IOT Instruction	IOP 1	IOP 2	IOP 4
636X	ICMX Increment multiplexer channel (set to Chan 0 if at maximum implemented channel)	RADC (6362) 0 → AC ADC buffer → AC 0 → ADC done 0 → ADCIP	ADCV (6364) Initiate Conversion
637X	ACMX Set multiplex register from AC	RADC (6372) 0 → AC ADC buffer → AC 0 → ADC DONE 0 → ADCIP	ADCV (6374) Initiate Conversion

2.4.1 Microprogramming

Microprogramming of most AX08 IOT's (except SKXK DSB or SKER DSB) is allowed. As an example of microprogramming effectiveness, note that with the combination of instructions ACMX RADC ADCV, it is possible to set up a multiplex channel, start a conversion, and read the results of a previous conversion all in one instruction.

2.5 DISPLAY CONTROL

In AX08 operations, ADC takes precedence so that a display command will have no effect if an ADC is taking place (conversion in progress or complete and value not yet read from buffer). The display control consists of two 9-bit DAC's and scope blanking facility.

The axis organization for display is shown in Figure 2-2.

Loading the Register X with DXC DXL and Y with DYC DYL drives the display as shown in Figure 2-2. Intensification is accomplished with 6304 or 6314 (DIS = 6304).

The commands DCX (Display X-Axis Clear-6301) and DYC (Display Y-Axis Clear-6311) clear the X- and Y-registers (to 000), and set X-OUT and Y-OUT to -5V. Power clear has the same effect. The IOT's DXL (Display X-Axis Load-6302) and DYL (Display Y-Axis Load-6312) load from the accumulator into the X- and Y-registers (AC bits 3-11 to X and Y bits 0-8). Since 000 in the X- and Y-registers implies half-scale, AC bit 3 is complemented before being transferred to the X-register (half-scale on X is represented in the AC as 400).

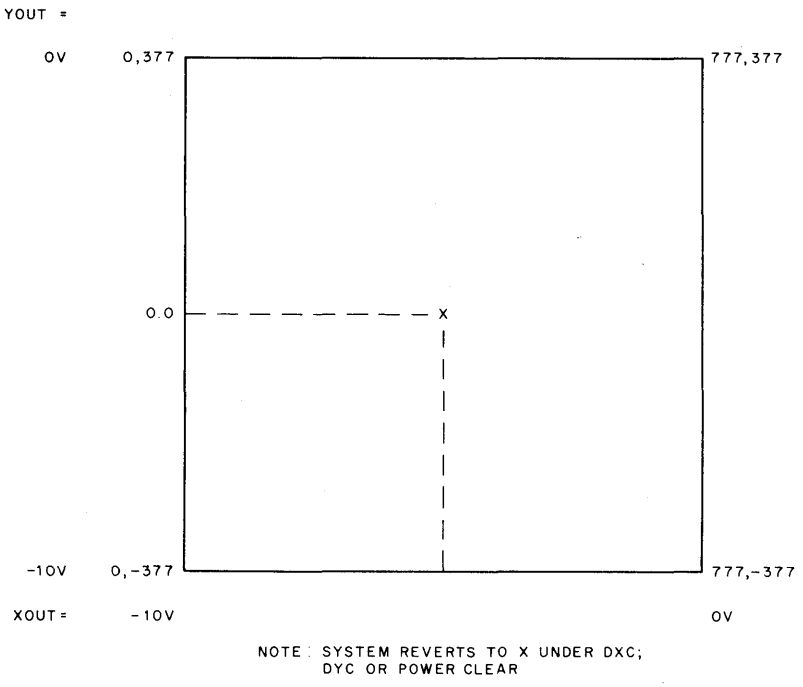


Figure 2-2 Display Axis Organization

If an ADC conversion is in process (a convert pulse has been given but RADC or CLER has not) then the display control instructions DYC, DXC, DIS DXL and DYL will have no effect. Thus, in automatic conversion mode, an inadvertent display command will not destroy the conversion.

Brightness control is set from MB bits 10 and 11 when instruction DSB (6324) is given. (Optional - option XR)

IOT's 6304 and 6314 both intensify a point; however it is obvious that within the structure of PAL III (symbolic machine language assembler, see DEC document Digital-8-3-5), it is only necessary to specify one mnemonic (DIS = 6304) to handle both sequences of micro instructions: DXC DXL DIS and DYC DYL DIS.

2.6 ENABLE REGISTER BIT CONFIGURATIONS

Enable Register flip-flop outputs, control certain optional modes of operation. A description of the Enable Register bits and how they are set from the AC with the instructions ZTEN OTEN is shown in Table 2-2.

Table 2-2
Enable Register

Flip-Flop Name	From AC Bit (1)	Effect
SKEN	0	Slows RC Clock rate by factor of 8
CVEN	1	Conversions initiated by RC or external clock pulse
RKEN	2	RC Clock flag causes interrupt
XKEN	3	Crystal clock flag causes interrupt
EREN	4	ADC timing error causes interrupt
ADEN	5	ADC Done flag causes interrupt
R4	6	R4 = 1 (option XR)
R2	7	R2 = 1 (option XR)
R1	8	R1 = 1 (option XR)
EXEN	9	External clock available as RC timer. S1, S2, S3 can cause interrupts.
CNEN	10	RC counting chain enabled
S0	11	Set pulse channel 0 (S0) Flag to 1
R4, R2, and R1 may (if implemented) be used to provide logic control of digital devices (e.g. relays).		

2.7 CLOCKS AND SCHMITT TRIGGER INPUTS

There are four instructions concerned with the two clocks in the AX08.

Crystal Clock:

IOT 6321 - Skip on crystal clock flag

IOT 6352 - Clear crystal clock flag

RC or External Clock:

IOT 6341 - Skip on RC clock flag

IOT 6352 - Clear RC clock flag

The crystal clock flag = 1 will cause an interrupt request to be generated if bit 3 of the Enable Register = 1. Note that there is no way to stop and start the crystal clock and to absolutely synchronize the clock with a program. The sequence

```
CLXK
SKXK
JMP.-1
```

will synchronize within a jitter of 0 to 5.75 μs (±30%).

The RC clock flag = 1 will cause an interrupt request to be generated if bit 2 of the Enable Register = 1.

The rate of clock pulses can be changed by a factor of 8 by changing bit 0 of the Enable Register. Bit 0 = 1 selects the slower speed. Power clear sets bit 0 = 0.

By turning the RC counting chain off and then on (OTEN with AC10) program-RC clock synchrony is possible.

The ADC may also operate in synchrony with the RC clock by setting enable register bit 1 = 1. RC clock pulses, if so enabled, cause an A/D conversion, starting at the RC pulse time. This eliminates the jitter characteristic of programmed ADC control.

The "external" input on the front panel can be used as an RC clock by setting bit 9 (1) in the Enable Register. (If the user wishes, RC clock may be disabled by bit 10 (0). Bit 9 (1) also serves to enable interrupts from pulse inputs S1, S2, or S3.

S0, S1, S2, S3 and the "contingency" inputs may be read into the AC by the instruction XRIN. (S3 and the "contingency" inputs C0 through C7 are optional, part of option XR.)

S1 through S3 are set by front panel inputs to Schmitt triggers. C0 through C7 are set by a digital logic level 0V. S0 is set under program control via the Enable Register. ENABLE 11(1).

S0 through S3 and C0 through C7 are cleared by setting corresponding bits in the AC = 1 and executing the instruction XRCL. Note that in the microprogrammed sequence: XRIN XRCL, only the bits in the register = 1, at the time of the XRIN are cleared by the XRCL. This prevents missing events that occur in the 2 μs between XRIN and XRCL (provided that the maximum rate on any single input does not exceed the programmed sampling rate on the register).

2.8 MULTIPLEXER AND ADC

Power clear sets the multiplexer register to 0s. The ICMX instruction increments this register until the largest implemented channel number is reached. The next ICMX resets the multiplex register to channel 0.

The instruction ACMX jam sets the contents of the AC into the multiplex register.

RADC clears the accumulator and the flag ADCIP then sets the AC with the contents of the ADC buffer.

ADCV initiates a conversion and sets the flag ADCIP(1). RC (or external) clock pulses cause the same action if auto conversion mode is enabled CVEN(1). 17 μs later, the conversion is complete and the ADC DONE flag is raised which causes an interrupt if ADEN(1) (see Table 2-2).

SKAD senses the state of ADC DONE. Skip is on ADC DONE(1). RADC will clear the ADC DONE flag.

The IOT's ACMX, RADC, and ADCV may be microprogrammed since ACMX jam sets the multiplex register and RADC jam sets the AC. Reading of conversion result on one channel and initiation of conversion on another may all be done in one instruction.

If conversions are done at a rate that does not permit the operating program to read the result before initiation of another conversion, the flag "ADC Timing Error" will be raised. This flag may be sensed by the instruction SKER. Skip is on ADC ERR(1). ADC ERR(1) will request an interrupt if EREN(1) - ENABLE 4(1). ADC ERR may be cleared by the instruction CLER (which also clears ADC DONE and ADCIP).

ADCIP(1) disables the display instructions 630X and 631X.

Front panel analog knobs are connected to channels 34, 35, 36 and 37 (from top to bottom)

2.9 DIAGNOSTICS

Chapter 4, Maintenance, contains descriptive material on diagnostic testing philosophy for the AX08.

CHAPTER 3
PRINCIPLES OF OPERATION

3.1 BLOCK DIAGRAM

The major functional elements of the system are shown in Figure 3-1, AX08 Block Diagram. All AX08 operations are controlled by the computer program; decoded IOT's provide the commands that initiate ADC or DAC operations, and skip and interrupt request logic alerts the computer to conditions in the AX08.

Analog inputs are processed through preamplifiers, multiplexers, and sample and hold circuits to a comparator (in the ADC Control). Successive approximation is achieved by the Y-OUT analog equivalent of the digital value in the Y-register being fed back to the comparator to control the input to the Y-register. The X-register keeps track of the step number in the approximation. Final output value of the ADC is the content of Y-register which is sent to the computer via the input mixer.

DAC for display, is accomplished by transfer of data words from the computer AC to the X- and Y-registers where the ladder networks provide the Y-OUT and X-OUT analog equivalents as outputs to the display. The display control (with option XR) provides three display intensity levels; bright, normal, or dim.

The system has two clocks: a crystal controlled clock that is set to 100 μs and an RC timing clock that is variable from roughly 20 μs to 2s. The crystal clock can be used to calibrate the RC clock.

The external register provides a buffer for inputs S0 through S2, (S0 is sync output) and as part of option XR, S3 and 8-bits of digital inputs.

The IOT decoder decodes IOT instructions from the computer to control AX08 operation together with the 12-bit Enable Register. The Enable Register provides function control levels which selectively enable interrupt conditions and in general, control optional modes of operation.

3.2 IOT DECODING

Generation of all IOT commands for the system is shown in Figure 3-2. Memory buffer bits 6, 7 and 8 from the computer provide the 3-bit code for generation of IO0 through IO7, and memory buffer bits 3, 4 and 5 when 011 enable the decoder gates. The decoded IO0 through IO7, in conjunc- with the IOP timing pulses 1, 2 and 4 from the computer, generate the IOT and major control commands for system operation.

Table 2-1 presents the generation and operation of all IOT's.

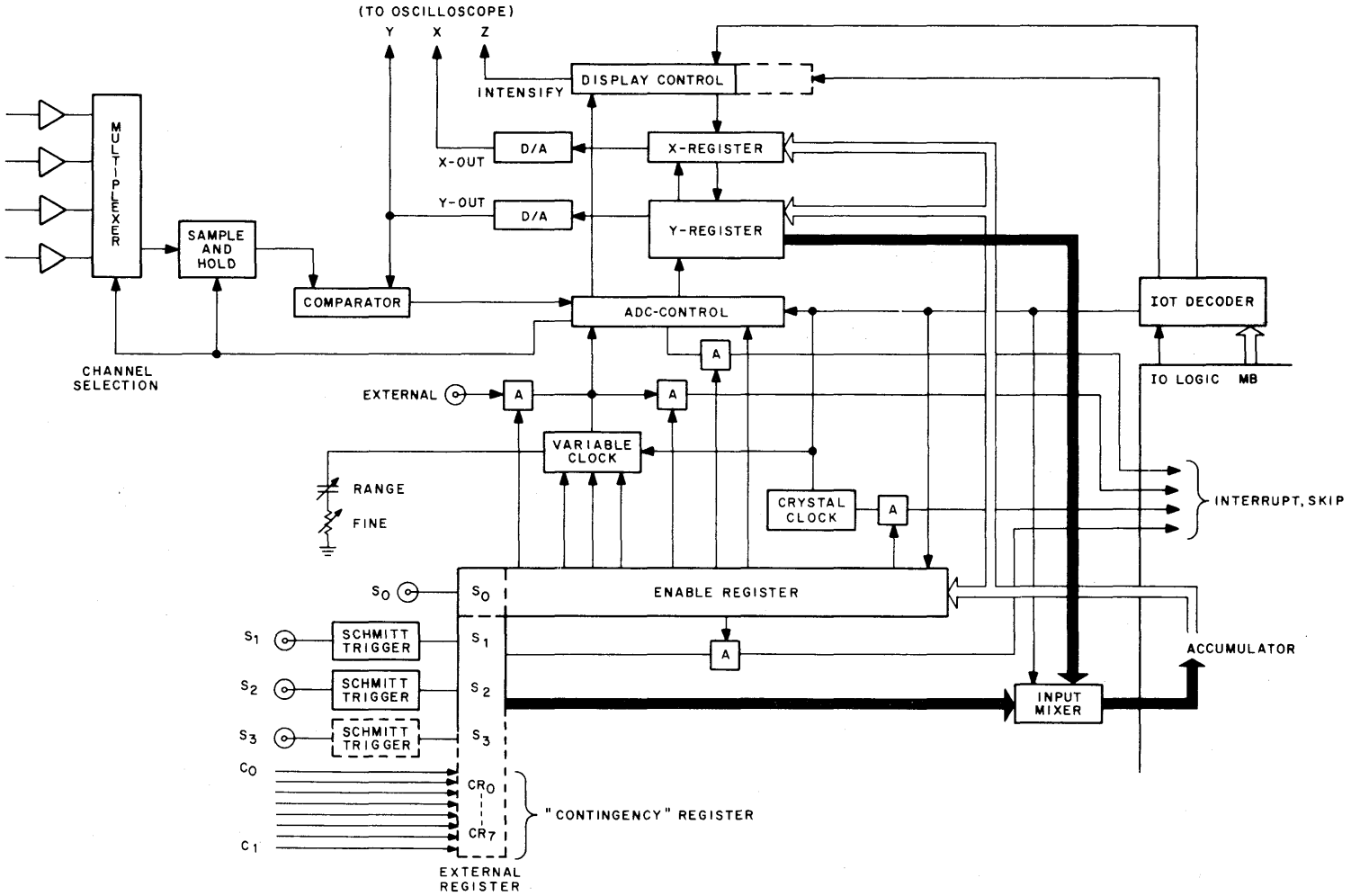


Figure 3-1 AX08 Block Diagram

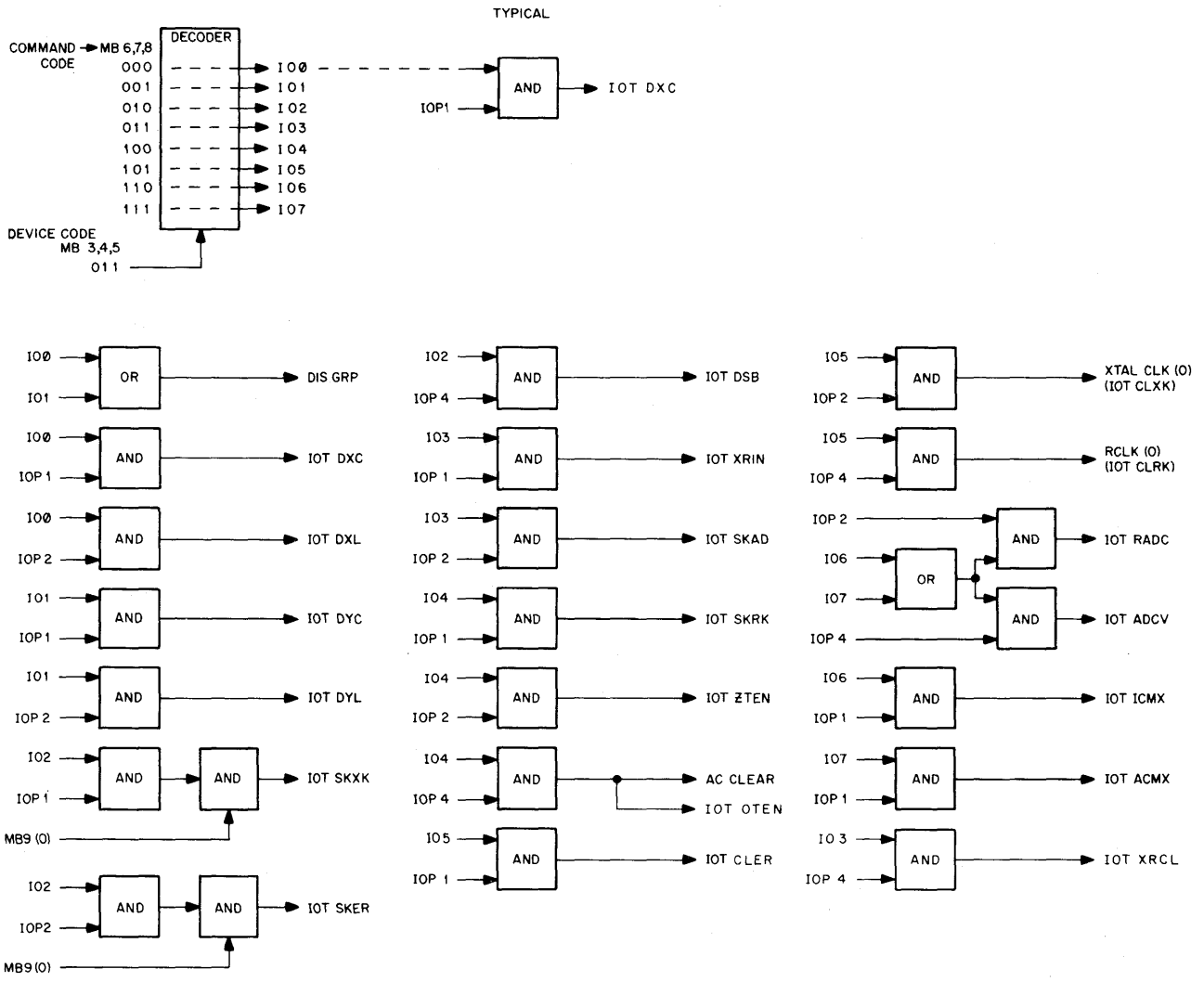


Figure 3-2 IOT Decoding Logic

3.3 CLOCKS

3.3.1 Crystal Clock

The crystal clock serves as a timer and provides a pulse every 100 μs to set the XTAL CLK flag (flip-flop) (Figure 3-3). The state of the crystal clock flag is used by the IOT SKXK (skip on crystal clock flag) to cause a skip request if the flag is set. IOT SKXK is caused by BMB bit 9(0) and the combination of IO2 decoded in the decoder (MB 6, 7, 8 as 010) and the IOP 1 pulse from the computer. To cause an interrupt request, the 1 state of the flag is ANDed with XKEN(1) from the Enable Register. XKEN is set by IOT OTEN (AC bit 3 (1)).

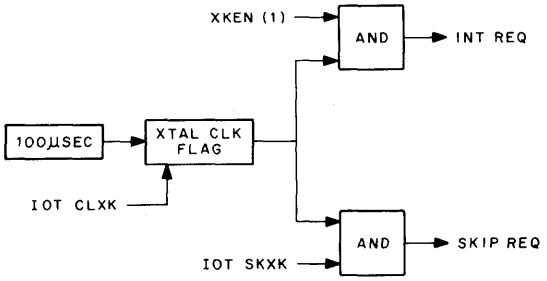


Figure 3-3 Crystal Clock Logic

3.3.2 RC Clock

The RC Clock consists of a 5-stage counter, count control logic, and output skip and interrupt request logic. The clock's counting rate is adjustable by front panel control and the RCLK flag can be set at the end of either 32 or 4 pulses from this counter chain.

The operator can control the RC clock pulse rate by using the timing control RANGE switch and the FINE (potentiometer) adjustment in the front panel. These adjustment inputs control an R401 Variable Clock that produces 100 ns pulses from a stable RC-coupled oscillator. The RANGE switch selects one of ten capacitor controlled frequency ranges; the FINE control permits fine adjustment to the desired pulse rate to provide the CNT CL pulses to the counter.

As shown in Figure 3-4, if the flag (flip-flop RCLK) is cleared and SKEN (1) is present (from the Enable Register, caused by IOT OTEN and AC0(1)), then the RCLK flag will be set every 32-clock pulses (enabled by IOT OTEN and AC bit 10(1) in the Enable Register). If SKEN (0) is present (from the Enable Register by IOT ZTEN, which commands reset if AC bit is 0, and AC bit 0 (0), the RCLK flag is set at the count of four in the counter.

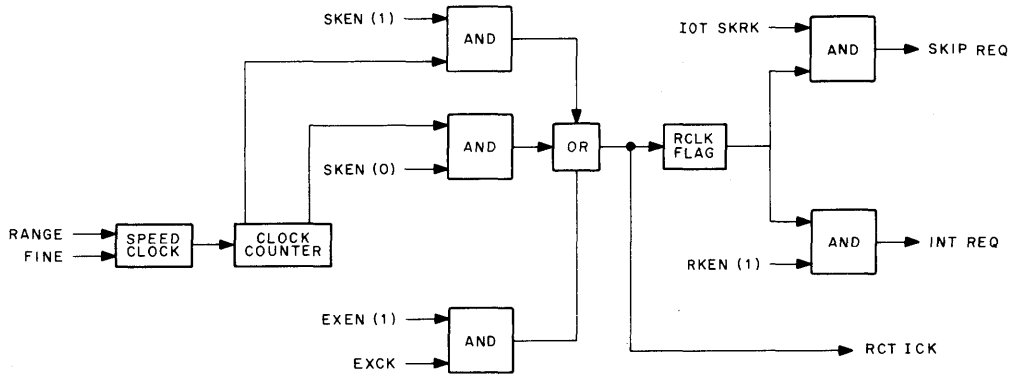


Figure 3-4 RC Clock Flag Logic

Whenever the EXEN(1) from the Enable Register is present, (set by IOT OTEN and AC 9(1)0 and positive going external clock pulse EXCK arrive, the flag RCLK will be set.

The state of the flag may be tested by the computer command IOT SKRK(skip on RC clock flag). An interrupt request occurs when RKEN (1) from the Enable Register (set by IOT OTEN and AC2(1)) and the RCLK flag is set.

3.4 ENABLE REGISTER

The Enable Register is used to:

Selectively enable interrupts from the ADC, the ADC timing error indicator, crystal controlled clock, the RC clock, and the Schmitt triggers;

Initialize and run the RC clock;

Shift between two speeds of the RC clock, one 8-times faster than the other;

Provide for automatic initiation of ADC conversion upon receipt of every RC flag setting pulse;

Enable an external clock pulse to set the RC flag instead of the RC timer provided;

Control 3 digital outputs (Optional - option XR).

The Enable Register control level flip-flops are reset under control of IOT ZTEN (zeros in the AC clear corresponding bits in the Enable Register), and are set under control of IOT OTEN (ones in the AC set bits in the enable) as shown in Figure 3-5.

Three bits of the Enable Register are reserved for the optional digital outputs. These bits, as with other bits of the Enable Register, are set with the combination of instruction ZTEN OTEN.

The effects of the Enable Register are described in Chapter 2 (Paragraph 2.5).

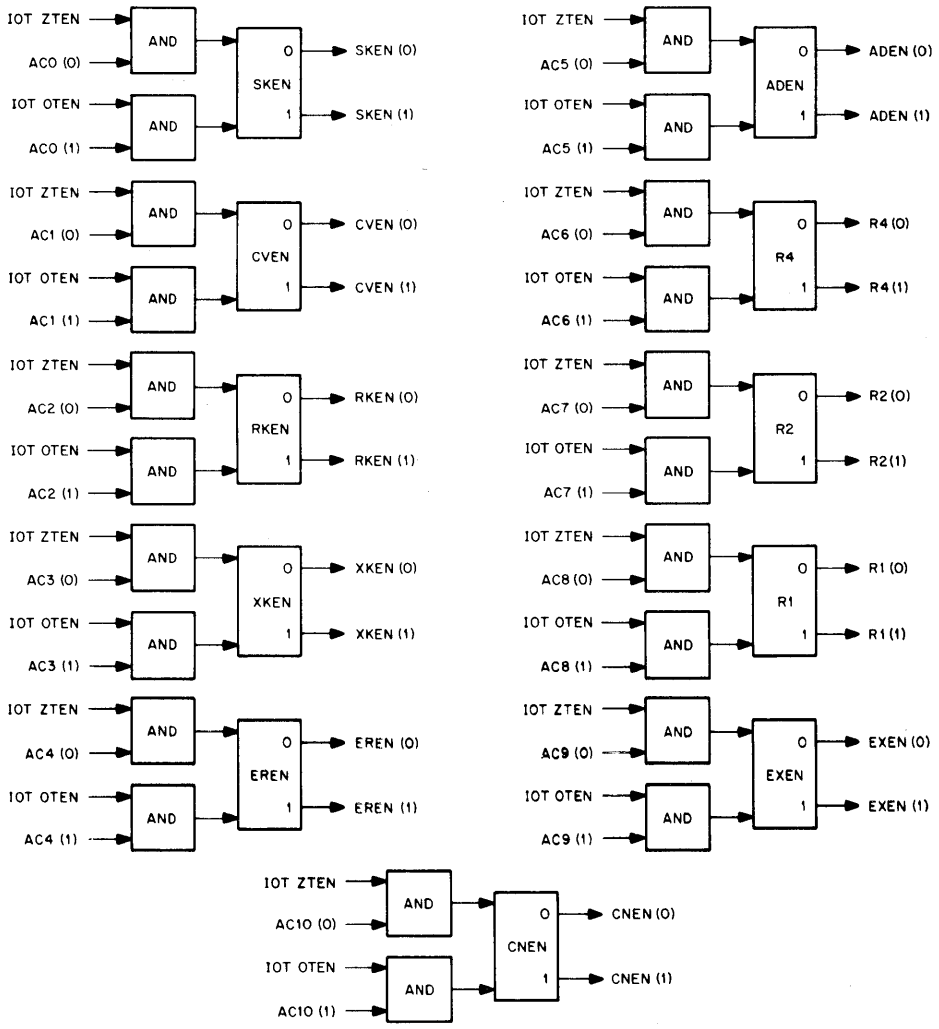


Figure 3-5 Enable Register

3.5 CONTINGENCY REGISTER - OPTIONAL (OPTION XR)

The contingency register flip-flops CR0 through CR7 are set by C0 through C7 inputs applied through the connector on the control panel. The basic logic is shown on Figure 3-6. The CR outputs are sent to the AC through the input mixer by IOT XRIN.

3.6 SYNCHRONIZATION OR "SYNC"

A level may be output on S0 (sync channel) by the instruction OTEN with AC11(1) as shown in Figure 3-7. Flip-flops S1 and S2 are set by the output of Schmitt triggers. The inputs and lower threshold levels for these Schmitt triggers are available on the front panel of the AX08. Sync S3 is part of option XR, as are the contingency inputs (C0 through C7).

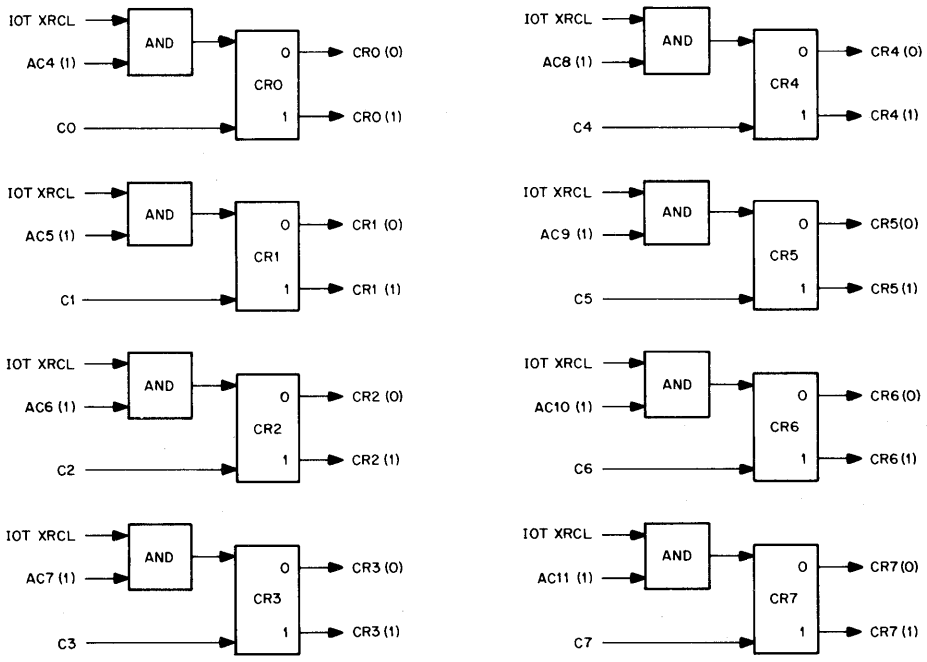


Figure 3-6 Contingency Register

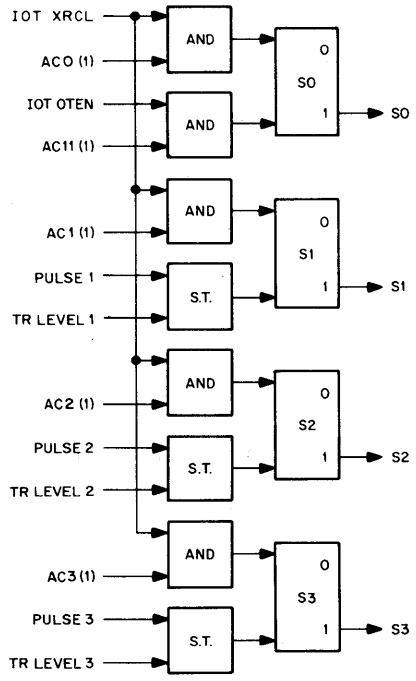


Figure 3-7 "Sync" Channel Logic

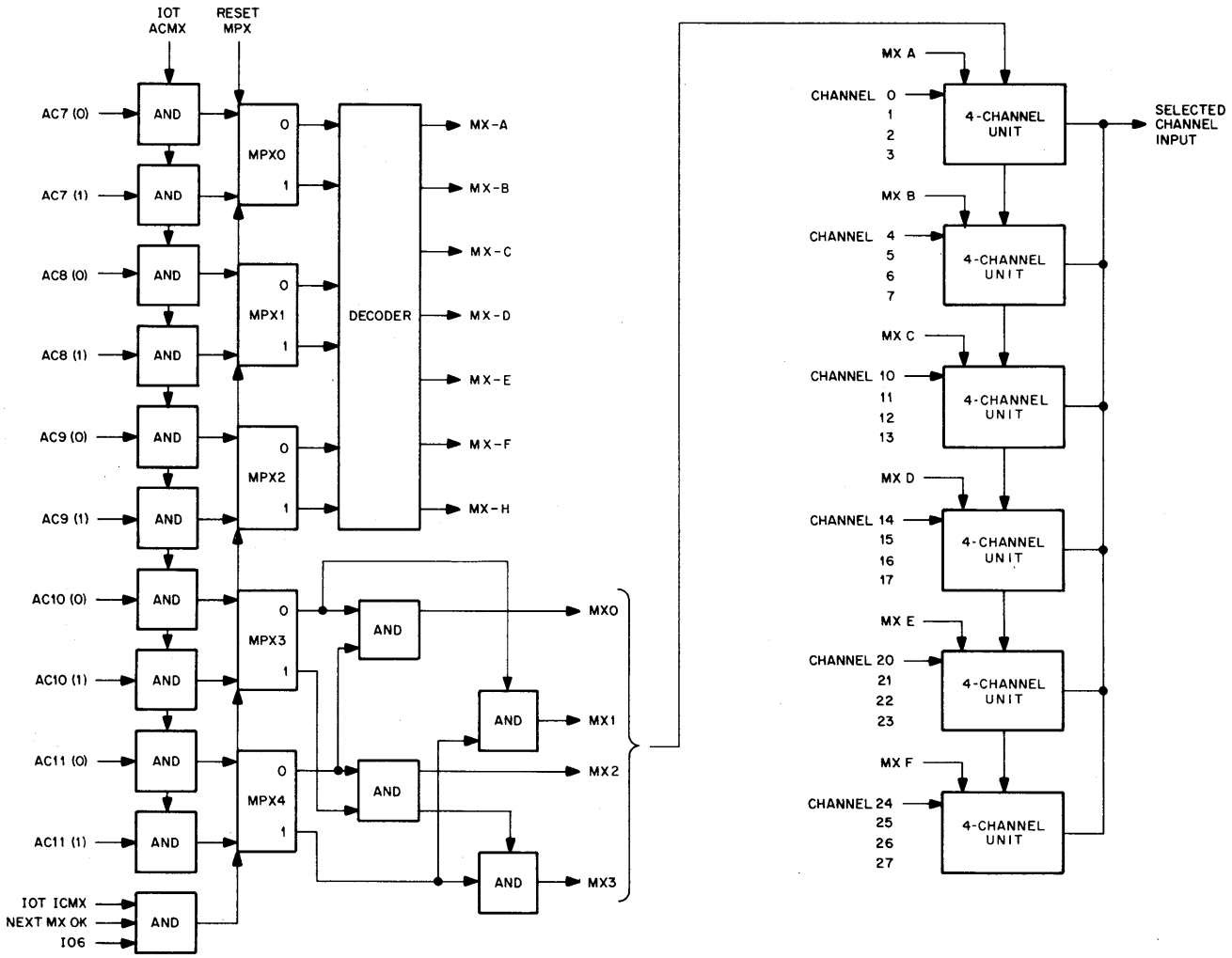


Figure 3-8 Input Channel Selection Logic

3.7 INPUT CHANNEL SELECTION

The multiplexer register is jamset from the AC7 through 11 with IOT ACMX (Figure 3-8). The register may be incremented by the IOT ICMX. A diode card (W002) is cut to decode the highest channel number implemented at each installation. If the highest channel number is reached, the multiplex register is reset to zero at the next ICMX. Thus, for all but the highest channel number in the MPX register, NEXT MX OK is available and ICMX counts the MPX register. In the highest channel, NEXT MX OK is not present, therefore ICMX will not count the register but instead generates RESET MPX, which sets the register to 0.

MX0 through MX3 select the channel within a A130 multiplexer module.
MXA through MXF select the channel group (multiplexer module) if option XM is implemented. MX-H selects the multiplexer module assigned to the front panel knobs.

3.8 ANALOG-TO-DIGITAL CONVERSION

The overall function diagram and the major timing of the analog-to-digital conversion (ADC) operation are shown in Figures 3-9 and 3-10 respectively. The converter is a 9-bit successive approximation type.

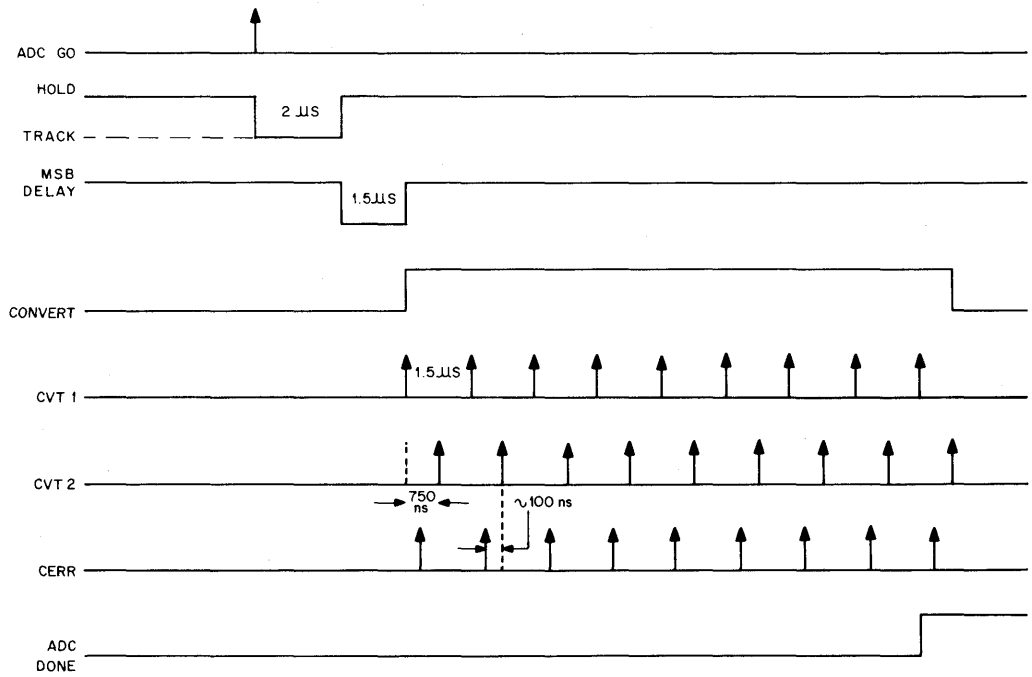


Figure 3-9 Analog-to-Digital Timing

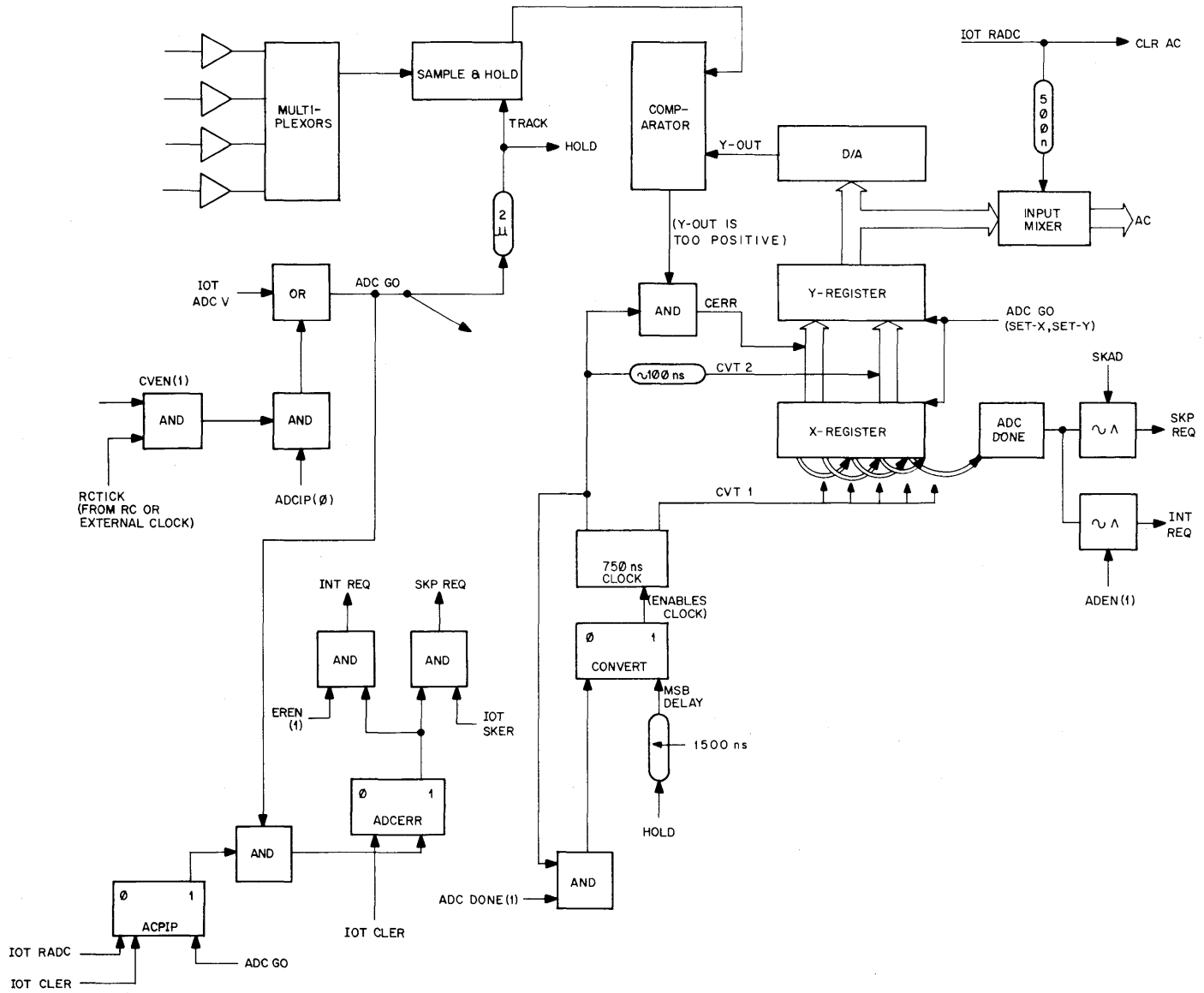


Figure 3-10 Analog-to-Digital Conversion

The ADC in the AX08 has preamplifier input channels that accept ±1.024V full scale. The input channels and multiplexing are available in multiples of from four to 24 channels. Channel select signals are applied to all multiplexer modules (a module switches 4 channels).

The conversion sequence begins by a clock pulse enabled by CVEN (1) and ADCIP (0) or by a computer command ADCV and ADCIP (0). This generates ADC GO, setting the sample and hold in the track state, which sets the X- and Y-registers to 000 (half analog scale). 2 μs later, the sample and hold returns to the hold state and a 1.5 μs delay provides settling time for the MSB (most significant bit) decision. When the 1.5 μs times out, the CV clock is enabled to generate 9 CVT 1's and CVT 2's as shown on the timing diagram.

A CVT 1 pulse shifts the X-register one place to the right as shown in Figure 3-11. X0 is complemented before shifting to X1. When the bit originally set to 0 by ADC GO is shifted (as a 1) through X8 into ADC DONE, the conversion is complete and terminates at the next CVT 2 pulse. CVT1 and CVT2 pulses are alternately generated (as shown on the timing diagram) by clock pulses which also cause generation of STROBE COMPARE pulses.

In the conversion process, the X-register serves as a step marker. One set bit is stepped through the X-register by CVT1. The active X bit is used to select which bit of the Y-register will be set by CVT2 and which bit will be cleared by CERR. CVT2 and the X-register generate test values for the DAC. The X-register is then shifted by CVT1. Slightly before the next CVT2, Y-OUT from the DAC ladder network is compared with the sample and hold output in the comparator. If, as a result, Y-OUT is too positive, STROBE COMPAR generates CERR clearing the test bit set at the last CVT2 or, for the first decision, sets to 1. This is done by using the X-register to point to the last test bit. Then CVT2, slightly after CERR time, sets the next test bit in the Y-register (CVT1 has shifted the X-register right). In this way, all bits of Y are successively set and (if this results in Y-OUT too positive) are reset. After 8 shifts, CVT1 and X8(1) set ADC DONE.

3.9 DISPLAY CONTROL

D/A ladders (X and Y) for display control, are cleared by pulses "SET X" and "SET Y" respectively. These are generated by IOT DXC and IOT DYC if there is no A/D conversion in progress (ADCIP(0)) (See Figure 3-12). IOT's DXL and DYL generate LOAD X and LOAD Y to transfer from the AC3 through 11 into X0 through X8, Y0 through Y8 (again if ADCIP(0)). AC3 is complemented before setting X0.

If option XR is implemented, DB-register and associated delays are installed. DB is power cleared to 0 which selects normal intensity (also selected at all times if XR not implemented). This

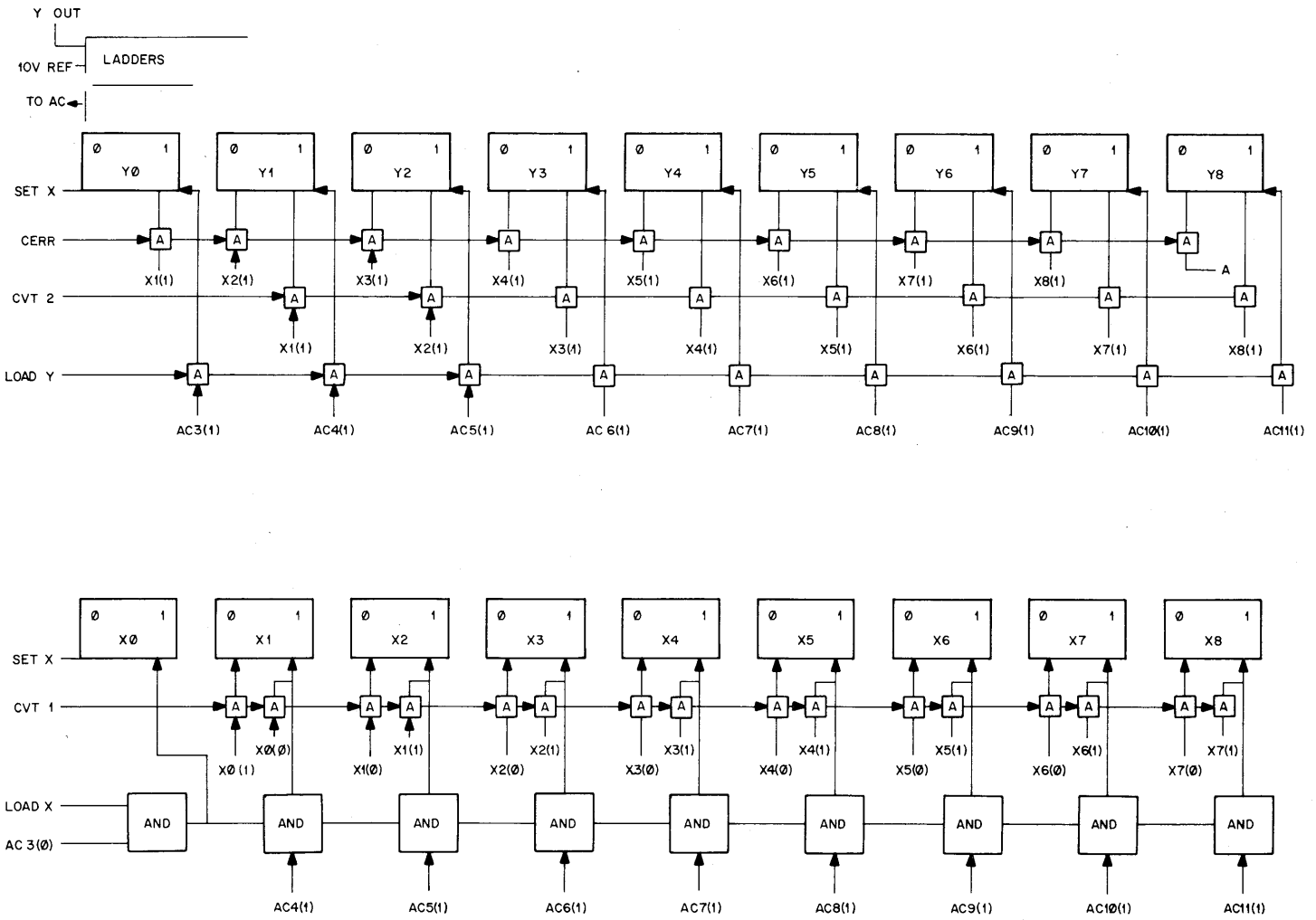


Figure 3-11 X- and Y-Registers

setting of DB disables BRIGHT and DIM intensity (see Figure 3-13). Disabling may be removed by setting either DB0(1) or DB1(1). This is done by strobing BMB10 and complement of BMB11 into DB upon IOT DSB. Thus,

DSB0: DIM - DB(01)

DSB1: NORM - DB(00)

DSB2: BRIGHT - DB(10)

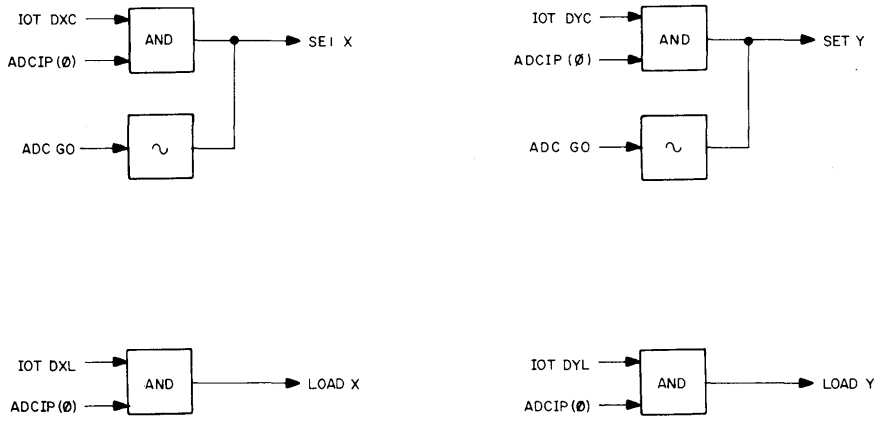


Figure 3-12 Display Command Logic

3.10 INPUT MIXERS

IOT's RADC and XRIN strobe contents of AX08 registers into accumulator as shown in Figure 3-15. RADC sends AC CLEAR with data on input mixers. AC CLEAR, causes 100 ns pulse, clearing AC. In PDP-8, the 500 ns delay insures that data is still available at AC when the internal 100 ns clear pulse ends. In the PDP-8/I these pulses are examined at IOP strobe time, the AC is disabled, and the I/O bus enabled on the transfer bus. Sign extension is performed, loading ADC buffer as a signed 2's complement, 12-bit, right-justified word. XRIN strobes entire external register (S0 through S3, CR0 through CR7) into AC as shown.

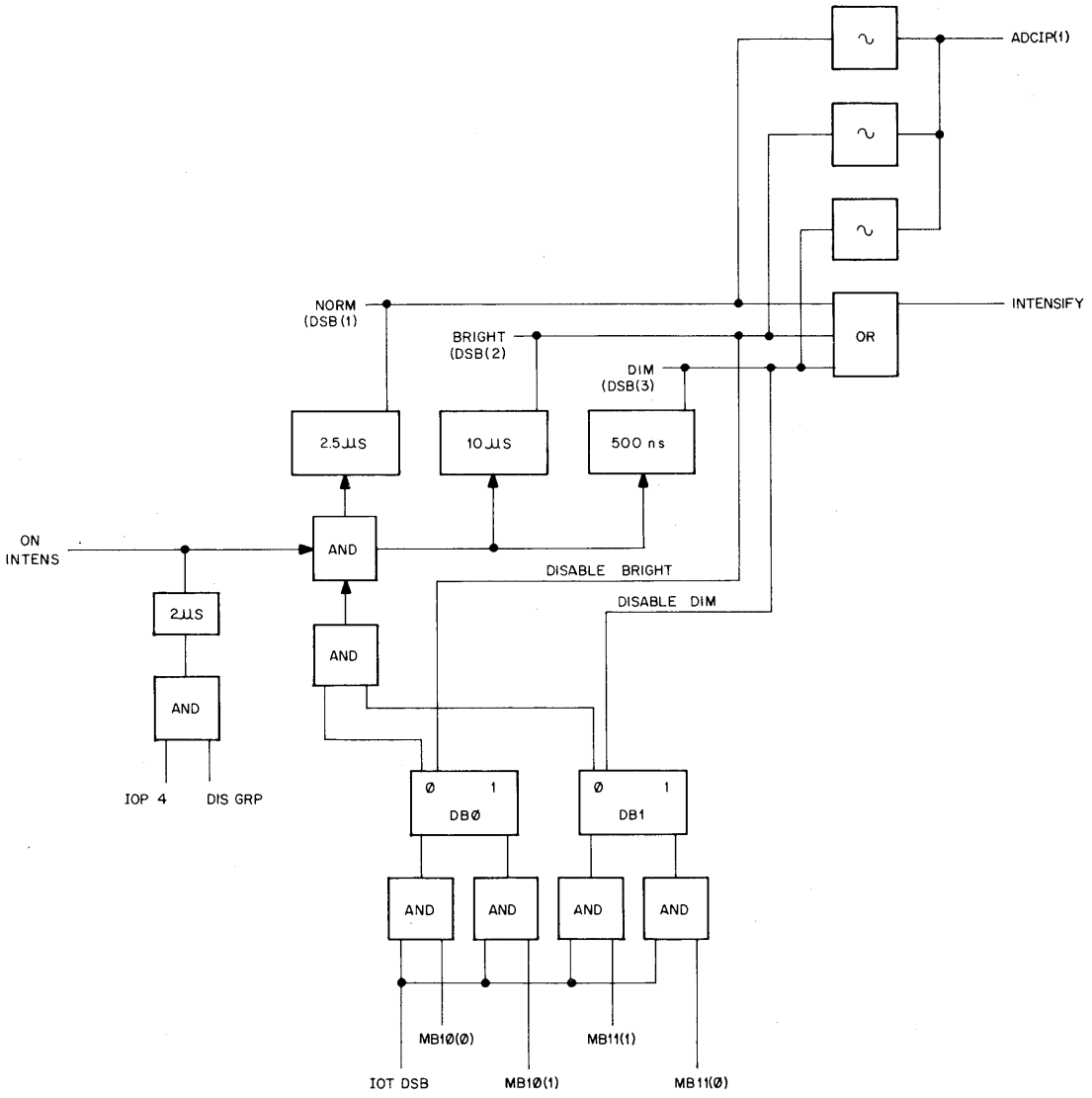


Figure 3-13 Intensity Logic

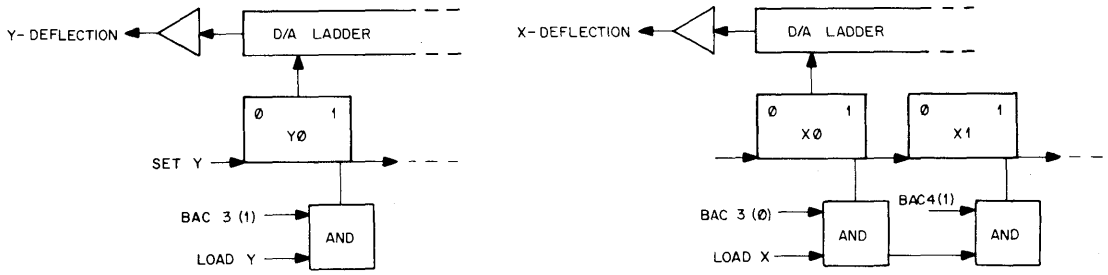


Figure 3-14 Display Registers

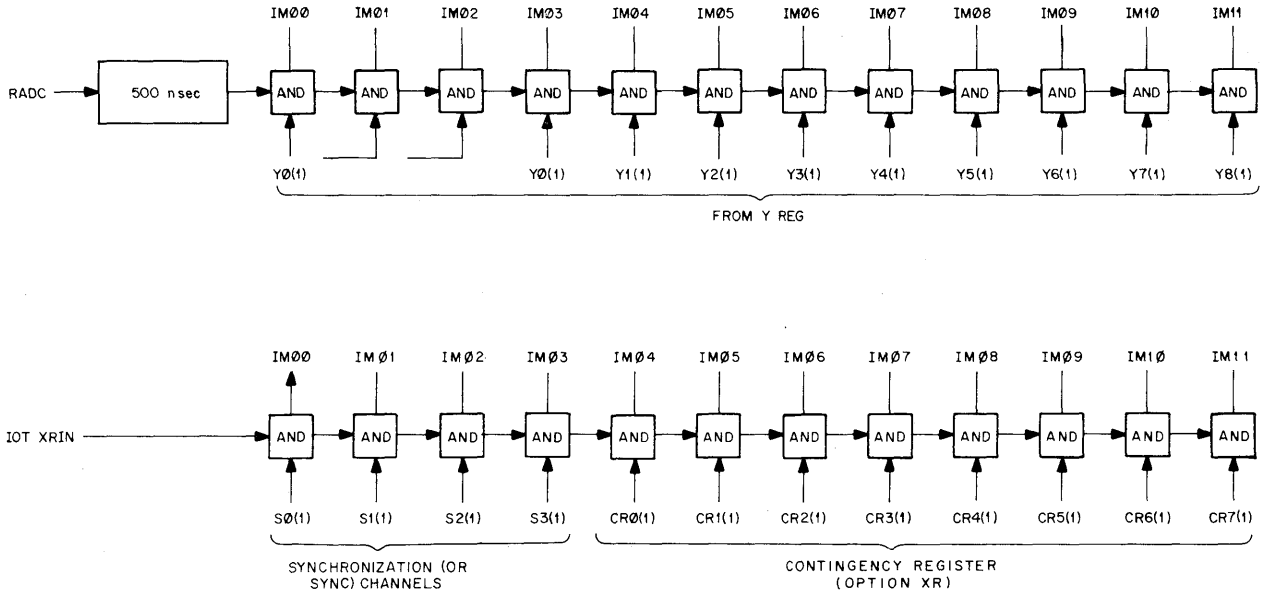


Figure 3-15 Input Mixer

CHAPTER 4
MAINTENANCE

4.1 INTRODUCTION

This chapter contains the information required for maintaining the AX08 system when operating with a PDP-8 or 8/I programmed data processor.

Preventive maintenance includes such routine periodic checks as, visual inspections, standard cleaning procedures, adjustments, and the occasional running of diagnostics to expose weakened conditions before they become malfunctions.

Both troubleshooting and preventive maintenance include procedures that range from basic power supply checks to intricate logic checking techniques involving programmed operation (diagnostics) of the processor (PDP-8 or PDP-8/I).

For a detailed understanding of diagnostic procedures, reference should be made to the pertinent processor maintenance manual and applicable software documentation.

The maintenance equipment specified in the PDP-8 Maintenance Manual with the addition of a precision voltage supply (EDC VS-11 or equivalent), is adequate for performing tests on the LAB-8 system.

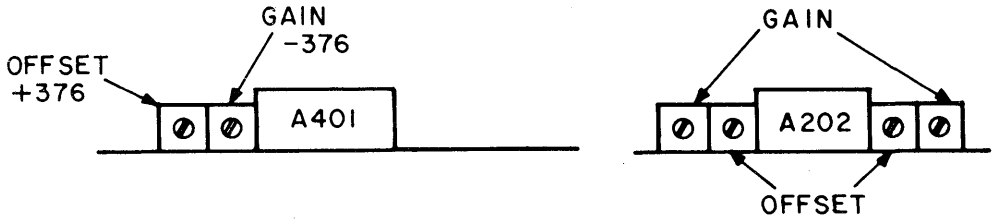
Detailed designations and location information of all modules and assemblies in the system are presented on drawings D-MU-AX08-0-11 and A-PL-AX08-0-11 listed in Chapter 6. All input/output connectors with pin and signal information are shown on drawing D-BS-AX08-0-9 in Chapter 6.

4.2 DIAGNOSTICS

The AX08 diagnostic (MAINDEC 8/I-D6AA-D) tests the functions described here. The operation of this diagnostic is described in the writeup supplied in the Software Kit.

4.3 CALIBRATION

In an operating system, (with part III of the AX08 diagnostic) readings of 0000 ±1/2 LSB is produced with 0V ±2 mV (offset); 0376 ±1/2 LSB with 1.016V ±2 mV (gain); and 7402 ±1/2 LSB with -1.016V ±2 mV. Adjustment of the A202's may be necessary from time to time to provide this calibration.



Channels 34 through 37 (front-panel knobs) may be used to set up the A401 if it should require readjustment. 1/2 to 1 turn from full stop in either direction should range the converter from -376 to 7401. If this cannot be done, set the pot to 3/4 turn from full clockwise, and adjust A401 offset to convert to 0376. Then set the pot 3/4 turn from full counter-clockwise, and adjust A401 gain to convert to 7402. Repeat until both end conditions are met.

CHAPTER 5
ENGINEERING DRAWINGS

This chapter contains copies of all engineering drawings and replacement schematics necessary to understand and maintain the Type AX08 Laboratory Peripheral System. The engineering drawings supplied here are in addition to a complete set of drawings supplied with each system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume that the drawings supplied with the equipment are correct. Drawings are listed below in the order in which they appear in the manual.

Engineering Drawings

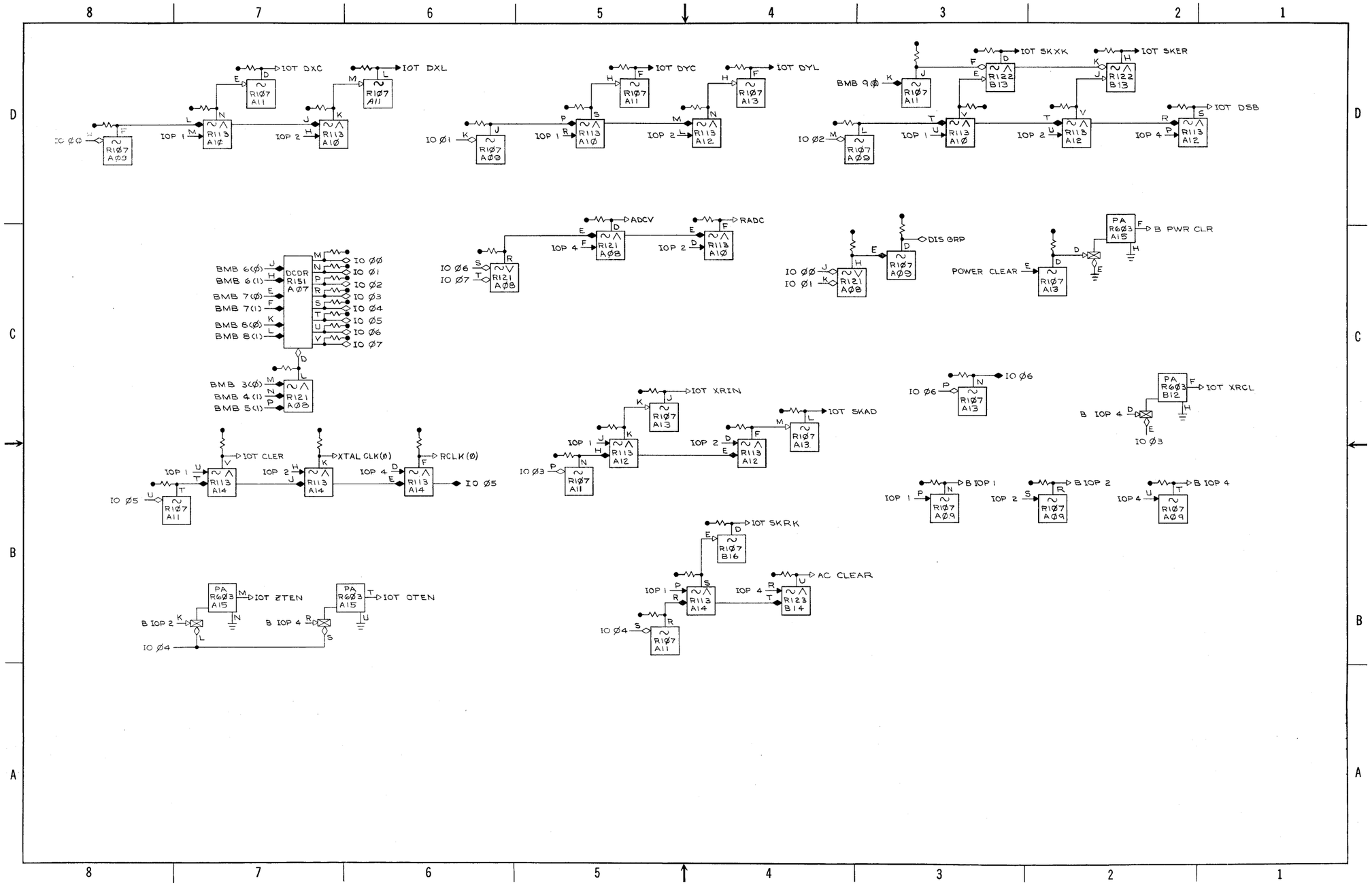
Drawing No.	Title	Revision	Page
D-BS-AX08-0-1 (Sheet 1)	IOT Decoders		5-3
D-BS-AX08-0-1 (Sheet 2)	IOT Decoders		5-5
D-BS-AX08-0-2	Timers and Synchronization or "Sync" Channels		5-7
D-BS-AX08-0-3	ADC Control		5-9
D-BS-AX08-0-4	Enable and Contingency Registers		5-11
D-BS-AX08-0-5	Buffered AC Bits and MPX IOT's		5-13
D-BS-AX08-0-6	Scope and Multiplexer Controls		5-15
D-BS-AX08-0-7	Input Mixers		5-17
D-BS-AX08-0-8	X and Y Registers		5-19
D-BS-AX08-0-9	I/O Connectors		5-21
D-BS-AX08-0-10	Additional Channels (Option XC)		5-23
D-MU-AX08-0-11 (Sheet 1)	AX08 Lab Peripheral (UML)		5-25
D-MU-AX08-0-11 (Sheet 2)	AX08 Lab Peripheral (UML)		5-27
D-AD-7005831-0-0	Control Panel Assembly	B	5-29
D-AD-7005832-0-0	Rear Panel Assembly	A	5-31

Replacement Schematics

Type	Title	Revision	Page
A130	Multiplex Linc-8	A	5-34
A202	Two Analog Preamplifiers	B	5-34
A401	Sample and Hold	A	5-35

Replacement Schematics (Cont)

Type	Title	Revision	Page
A502	Comparator	E	5-35
A601	Digital-Analog Converter	J	5-36
A604	Digital-Analog	N	5-36
A704	Reference Supply	J	5-37
A706	Power Supply for A202	A	5-37
R002	Diode Network	A	5-38
R107	Inverter	H	5-39
R113	NAND/NOR Gate	B	5-39
R121	NAND/NOR Gate	A	5-40
R122	NOR/NAND Gate	C	5-40
R123	Input Bus	B	5-41
R151	Binary to Octal Decoder	E	5-41
R202	Dual Flip-Flop	F	5-42
R203	Triple Flip-Flop	3	5-42
R205	Dual Flip-Flop	5	5-43
R302	Dual Delay Multivibrator	S	5-43
R401	Variable Clock	M	5-44
R405	Crystal Clock	J	5-44
R603	Pulse Amplifier	6	5-45
W500	High Impedance Follower		5-45
W501	Schmitt Trigger		5-46
W681	Scope Intensifier		5-46

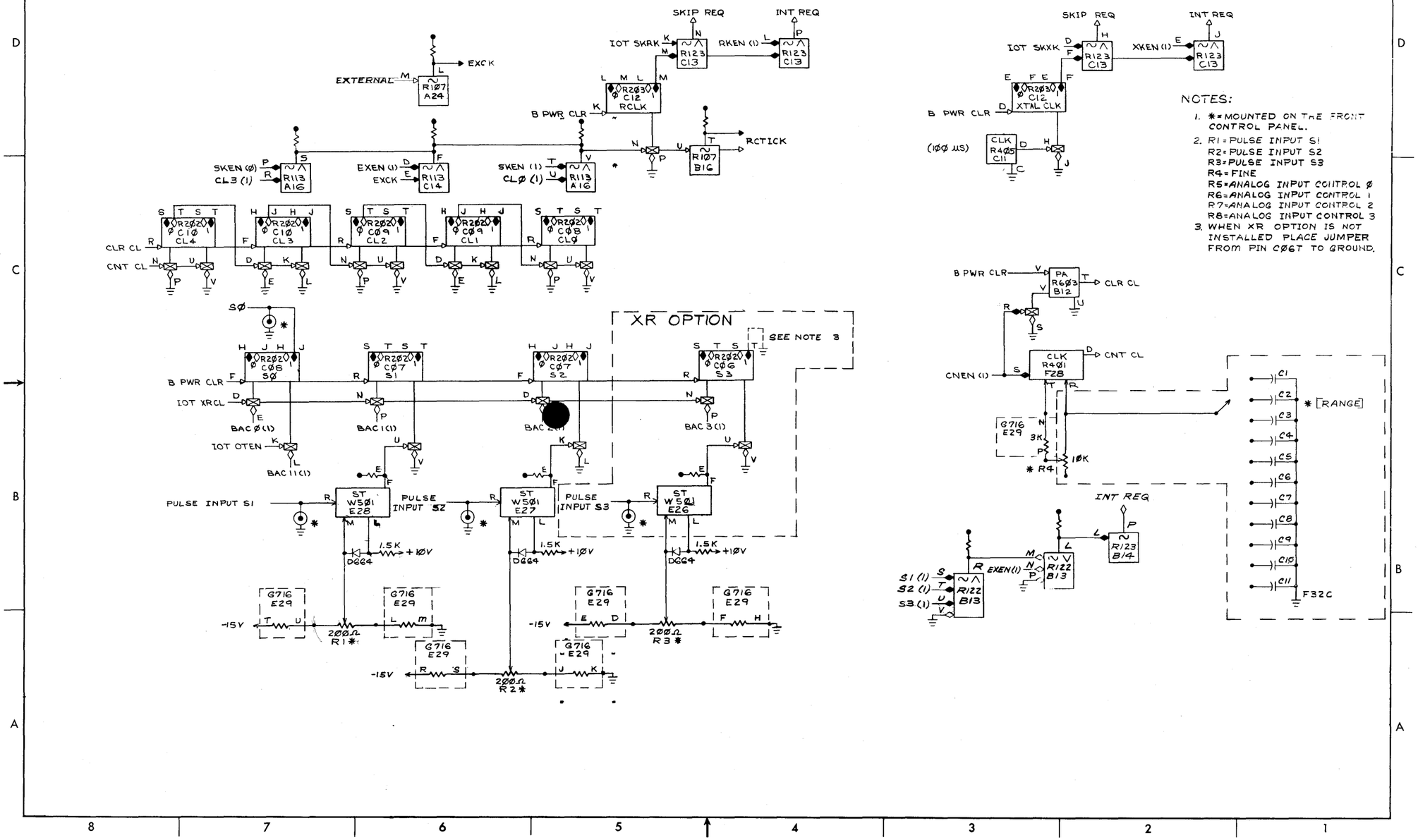


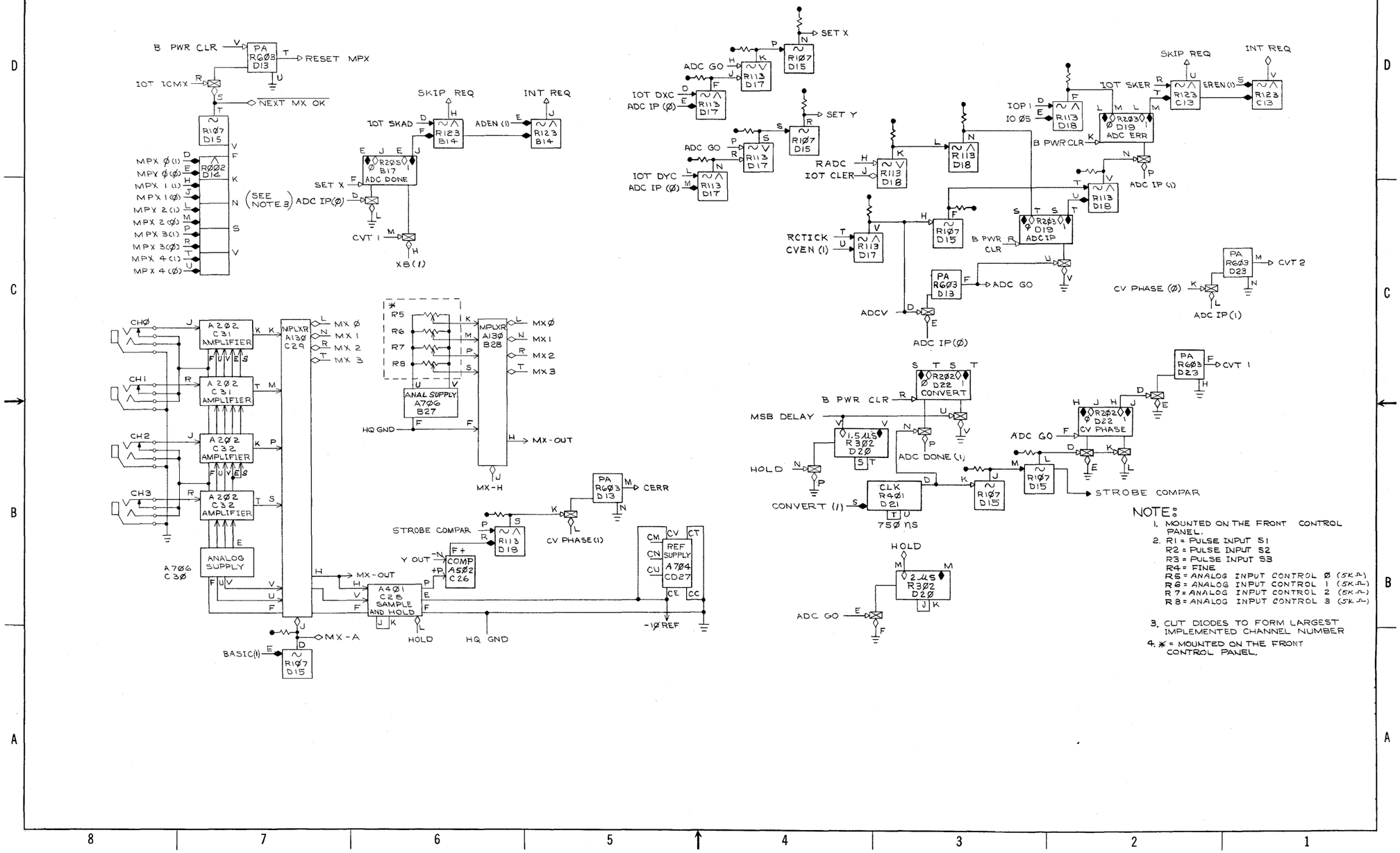
D-BS-AX08-0-1 IOT Decoders
(Sheet 1)

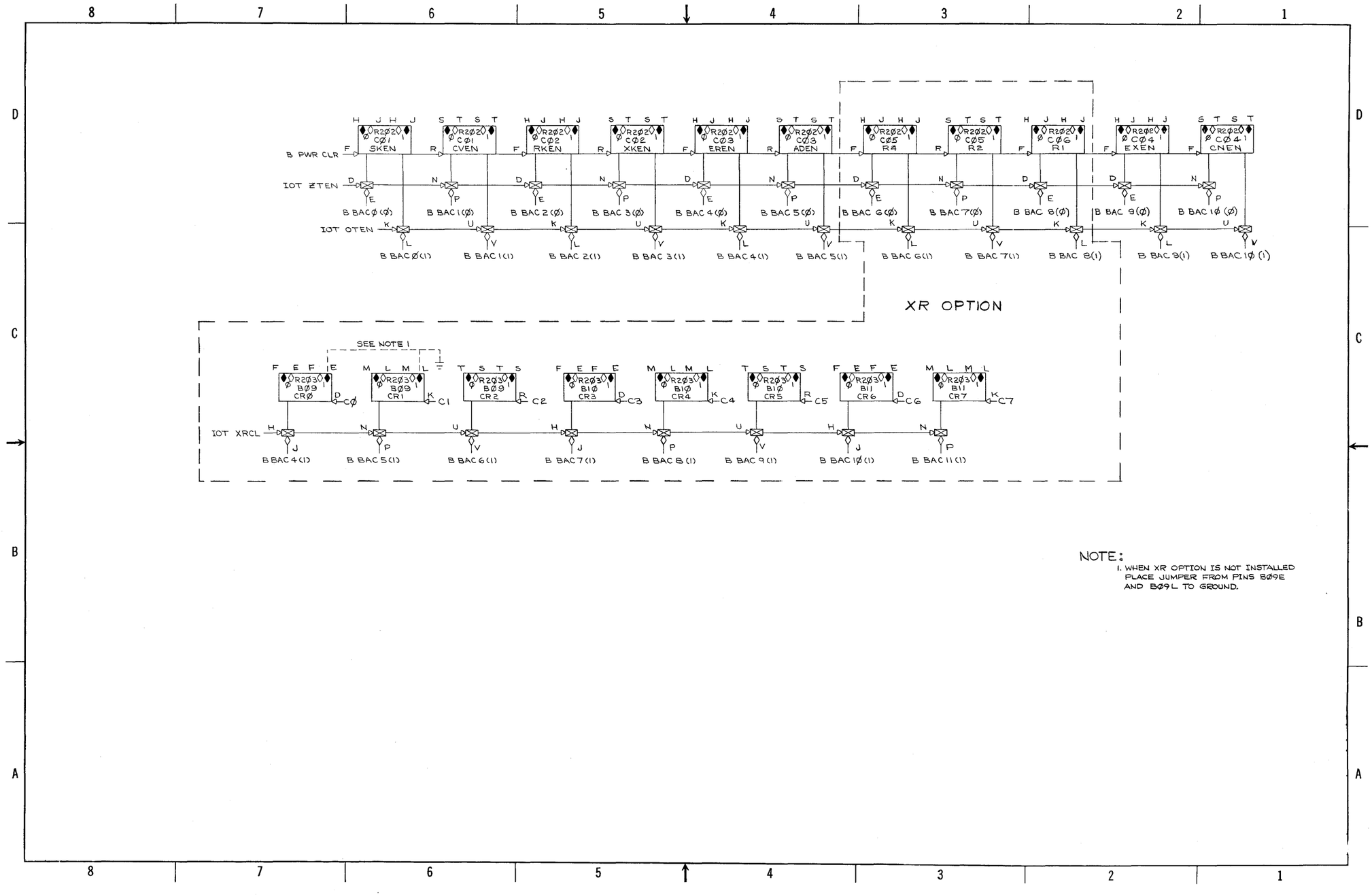
AX-Ø8 INTERFACE IOT'S 63YX

Y \ X	1	2	4
Ø	DXC CLEAR X REGISTER	DXL LOAD X FROM I'S OF AC	DIS DISPLAY (63Ø4)
1	DYC CLEAR Y REGISTER	DYL LOAD Y FROM I'S OF AC	
2	SKXK SKIP ON CRYSTAL CLOCK	SKER SKIP ON TIMING ERROR FLAG. (ADC CONVERT REQUESTED WHILE LAST CONVERSION NOT YET COMPLETED)	DSB SET BRIGHTNESS REGISTER DSB Ø SET DIM DSB 1 SET NORM DSB 2 SET BRIGHT
3	XRIN READ EXTERNAL SENSE REGISTER INTO AC	SKAD SKIP ON ADC DONE.(SET BY COMPLETION OF ADC. CLEARED BY READING ADC - RADC)	XRCL CLEAR BITS OF EXTERNAL SENSE REGISTER THAT ARE SET IN AC
4	SKRK SKIP ON RC TIMING CLOCK	ZTEN ZEROS IN AC CLEAR CORRESPONDING BITS IN ENABLE REGISTER	OTEN ONES IN AC SET CORRESPONDING BITS IN ENABLE REGISTER THEN CLEAR AC
5	CLER CLEAR TIMING ERROR FLAG	CLXK CLEAR CRYSTAL CLOCK FLAG	CLRK CLEAR TIMING CLOCK FLAG
6	ICMX INCREMENT MULTIPLEXOR (IF CHANNEL NOT IMPLENTED SET MULTIPLEX TO CHANNEL Ø)	RADC READ ADC VALUE FROM Y REGISTER CLEAR AC FIRST (6362)	ADCV CONVERT ANALOG SIGNAL (6364)
7	ACMX SET MULTIPLEX REGISTER FROM AC - SELECT ANALOG CHANNEL		

D-BS-AX08-0-1 IOT Decoders
(Sheet 2)

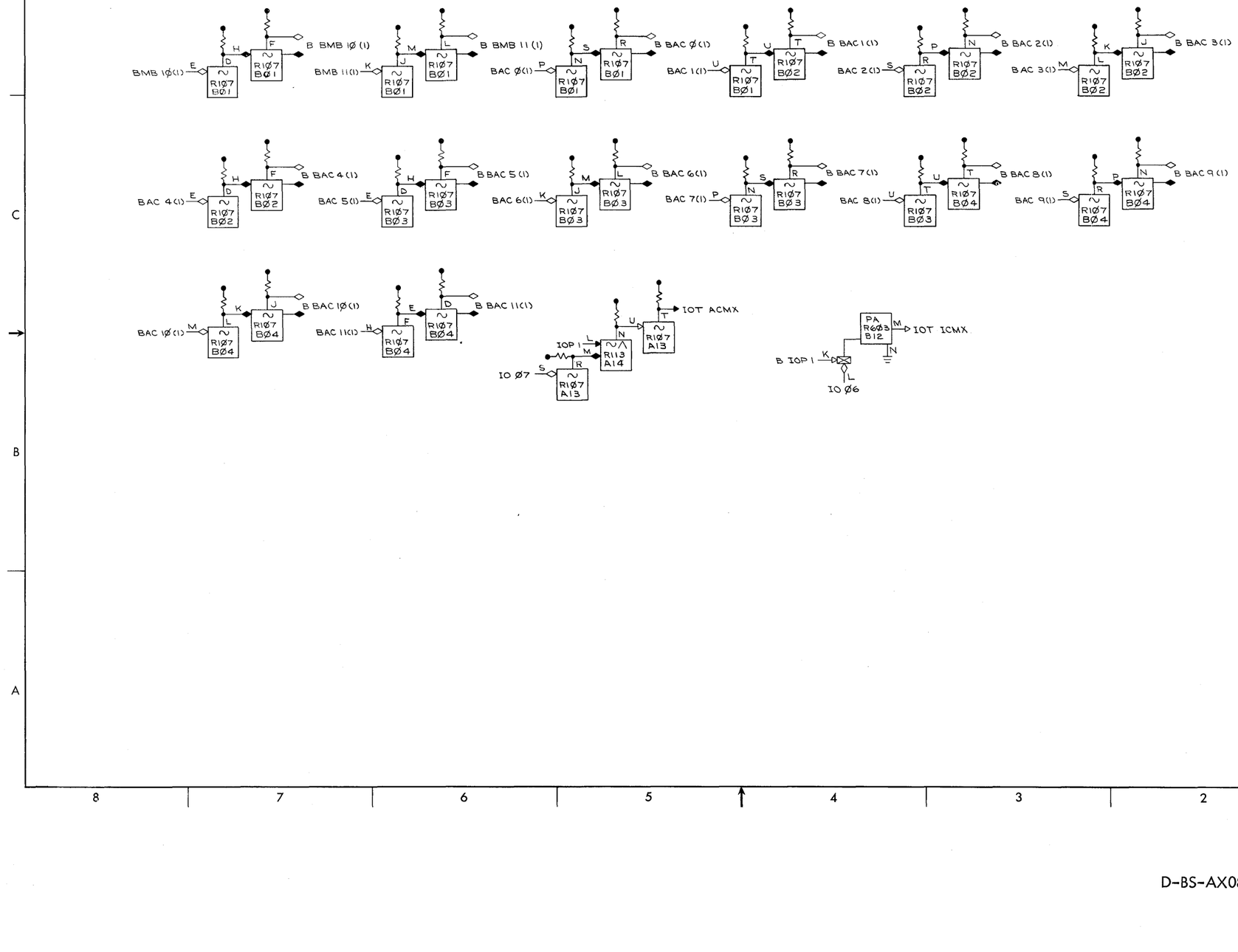

SKIP REQ
INT REQ
IOT SKRK
RKEN (1)
R123 C13
EXTERNAL
EXCK
R107 A24
B PWR CLR
R2Ø3 C12 RCLK
RCTICK
R107 B16
SKEN (Ø)
CL3 (1)
R113 A16
EXEN (1)
EXCK
R113 C14
SKEN (1)
CLØ (1)
R113 A16
R2Ø2 CØ9 CL4
R2Ø2 CØ9 CL3
R2Ø2 CØ9 CL2
R2Ø2 CØ9 CL1
R2Ø2 CØ8 CL9
CLR CL
CNT CL
XR OPTION
SEE NOTE 3
SØ
S1
S2
S3
R2Ø2 CØ8 SØ
R2Ø2 CØ7 S1
R2Ø2 CØ7 S2
R2Ø2 CØ6 S3
IOT XRCL
BAC Ø (1)
BAC 1 (1)
BAC 2 (1)
BAC 3 (1)
IOT OTEN
BAC 11 (1)
PULSE INPUT S1
PULSE INPUT S2
PULSE INPUT S3
ST W5Ø1 E28
ST W5Ø1 E27
ST W5Ø1 E26
1.5K
+1ØV
DGG4
G716 E29
-15V
2ØØΩ R1*
2ØØΩ R2*
2ØØΩ R3*
IOT XKXK
XKEN (1)
B PWR CLR
(1ØØ µs)
CLK R4Ø5 C11
XTAL CLK
NOTES:
1. * = MOUNTED ON THE FRONT CONTROL PANEL.
2. R1 = PULSE INPUT S1
R2 = PULSE INPUT S2
R3 = PULSE INPUT S3
R4 = FINE
R5 = ANALOG INPUT CONTROL Ø
R6 = ANALOG INPUT CONTROL 1
R7 = ANALOG INPUT CONTROL 2
R8 = ANALOG INPUT CONTROL 3
3. WHEN XR OPTION IS NOT INSTALLED PLACE JUMPER FROM PIN CØ6T TO GROUND.
PA R6Ø3 B12
CLR CL
CNT CL
CNEN (1)
CLK R4Ø1 F28
G716 E29
3K
1ØK
* R4
* [RANGE]
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
F32C
INT REQ
R123 B14
R122 B13
EXEN (1)
S1 (1)
S2 (1)
S3 (1)

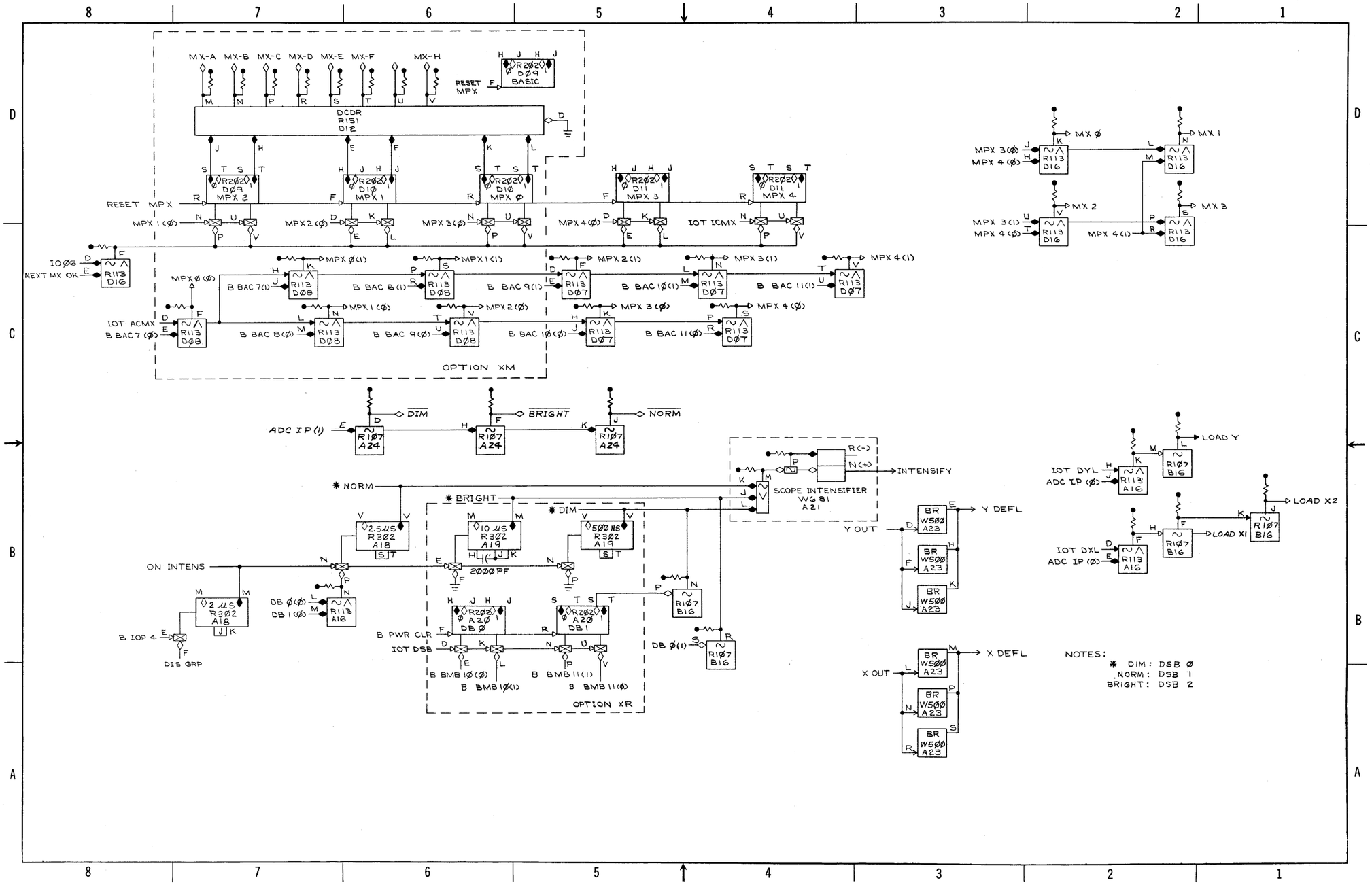

B PWR CLR
PA RGØ3 D13
RESET MPX
IOT ICMX
NEXT MX OK
R1Ø7 D15
MPX Ø (1)
MPX Ø (Ø)
MPX 1 (1)
MPX 1 (Ø)
MPX 2 (1)
MPX 2 (Ø)
MPX 3 (1)
MPX 3 (Ø)
MPX 4 (1)
MPX 4 (Ø)
RØØ2 D14
(SEE NOTE 3) ADC IP (Ø)
SKIP REQ
INT REQ
IOT SKAD
R123 B14
ADEN (1)
R2Ø5 Ø B17 ADC DONE
SET X
CVT 1
XB (1)
CH Ø
CH 1
CH 2
CH 3
A2Ø2 C31 AMPLIFIER
A2Ø2 C32 AMPLIFIER
FUSES
ANALOG SUPPLY
A7Ø6 C3Ø
MPLXR A13Ø C29
MX Ø
MX 1
MX 2
MX 3
R5
R6
R7
R8
ANAL SUPPLY A7Ø6 B27
HQ GND
MPLXR A13Ø B28
MX-OUT
MX-H
MX-A
BASIC (1)
STROBE COMPAR
R113 D18
Y OUT
COMP A5Ø2 C26
A4Ø1 C28 SAMPLE AND HOLD
HOLD
HQ GND
PA RGØ3 D13
CERR
CV PHASE (1)
REF SUPPLY A7Ø4 CD27
-1Ø REF
SET X
ADC GO
IOT DXC
ADC IP (Ø)
SET Y
IOT DYC
RADC
IOT CLER
RCTICK
CVEN (1)
ADCV
ADC IP (Ø)
IOT SKER
EREN (1)
IOP 1
IO Ø5
R2Ø3 Ø D19 ADC ERR
ADC IP (1)
R2Ø3 Ø D19 ADCIP
ADC GO
CV PHASE (Ø)
PA RGØ3 D23
CVT 2
ADC IP (1)
CVT 1
R2Ø2 Ø D22 CONVERT
MSB DELAY
1.5 µS R3Ø2 DØ
ADC DONE (1)
HOLD
CONVERT (1)
CLK R4Ø1 D21
75Ø NS
R2Ø2 Ø D22 CV PHASE
STROBE COMPAR
2 µS R3Ø2 DØ
NOTE:
1. MOUNTED ON THE FRONT CONTROL PANEL.
2. R1 = PULSE INPUT S1
R2 = PULSE INPUT S2
R3 = PULSE INPUT S3
R4 = FINE
R5 = ANALOG INPUT CONTROL Ø (5K Ω)
R6 = ANALOG INPUT CONTROL 1 (5K Ω)
R7 = ANALOG INPUT CONTROL 2 (5K Ω)
R8 = ANALOG INPUT CONTROL 3 (5K Ω)
3. CUT DIODES TO FORM LARGEST IMPLEMENTED CHANNEL NUMBER
4. * = MOUNTED ON THE FRONT CONTROL PANEL.

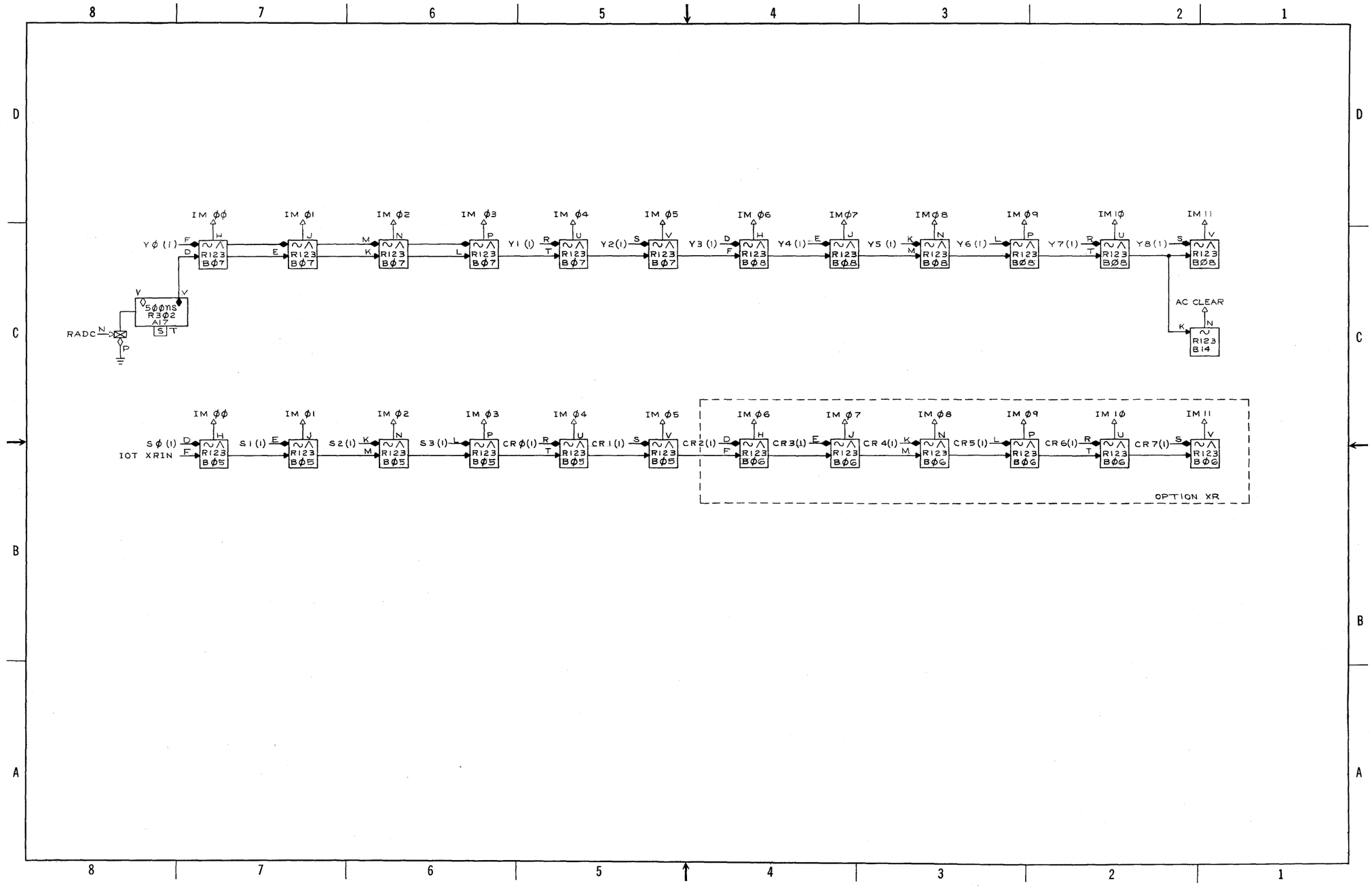


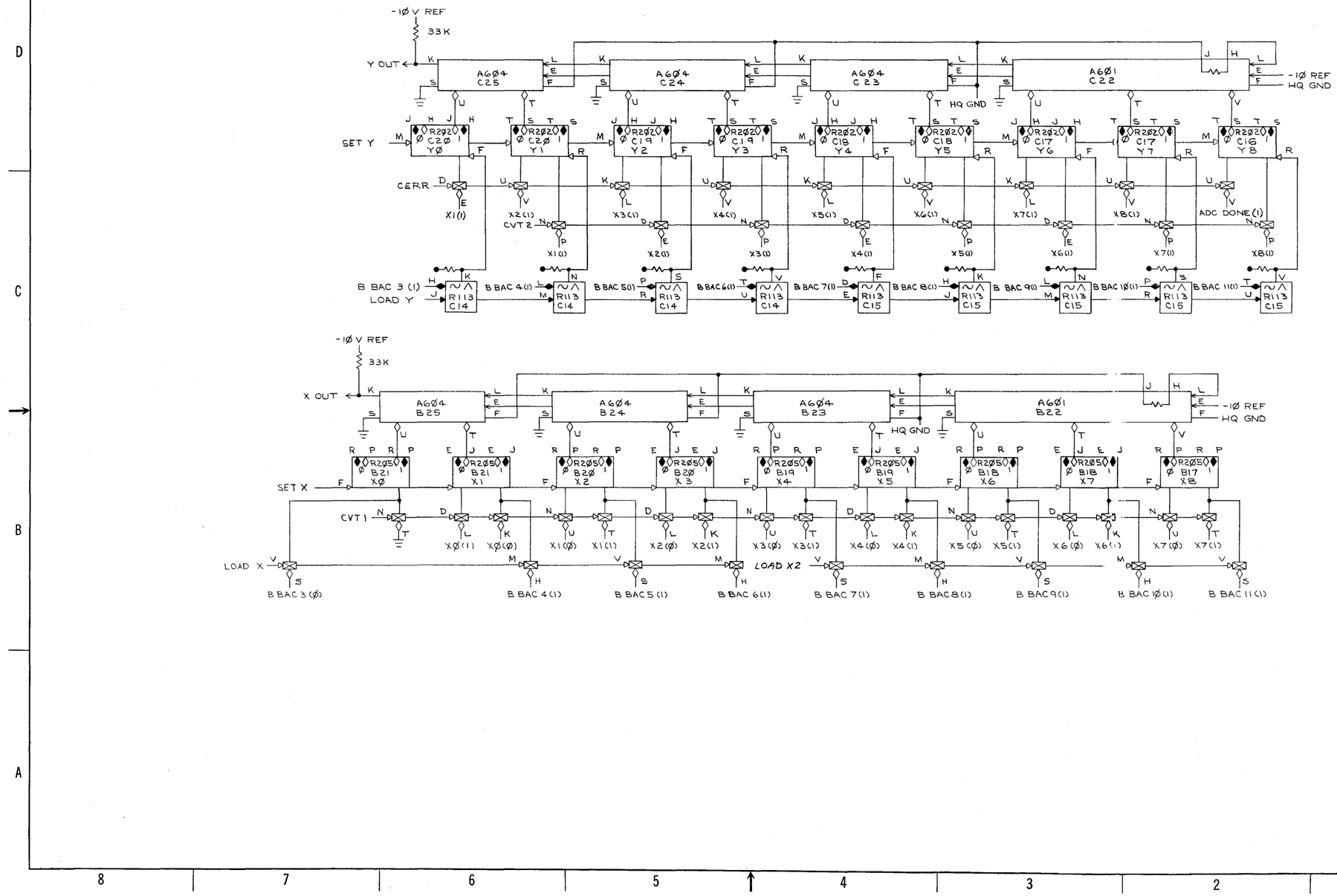
NOTE:
1. WHEN XR OPTION IS NOT INSTALLED PLACE JUMPER FROM PINS BØ9E AND BØ9L TO GROUND.

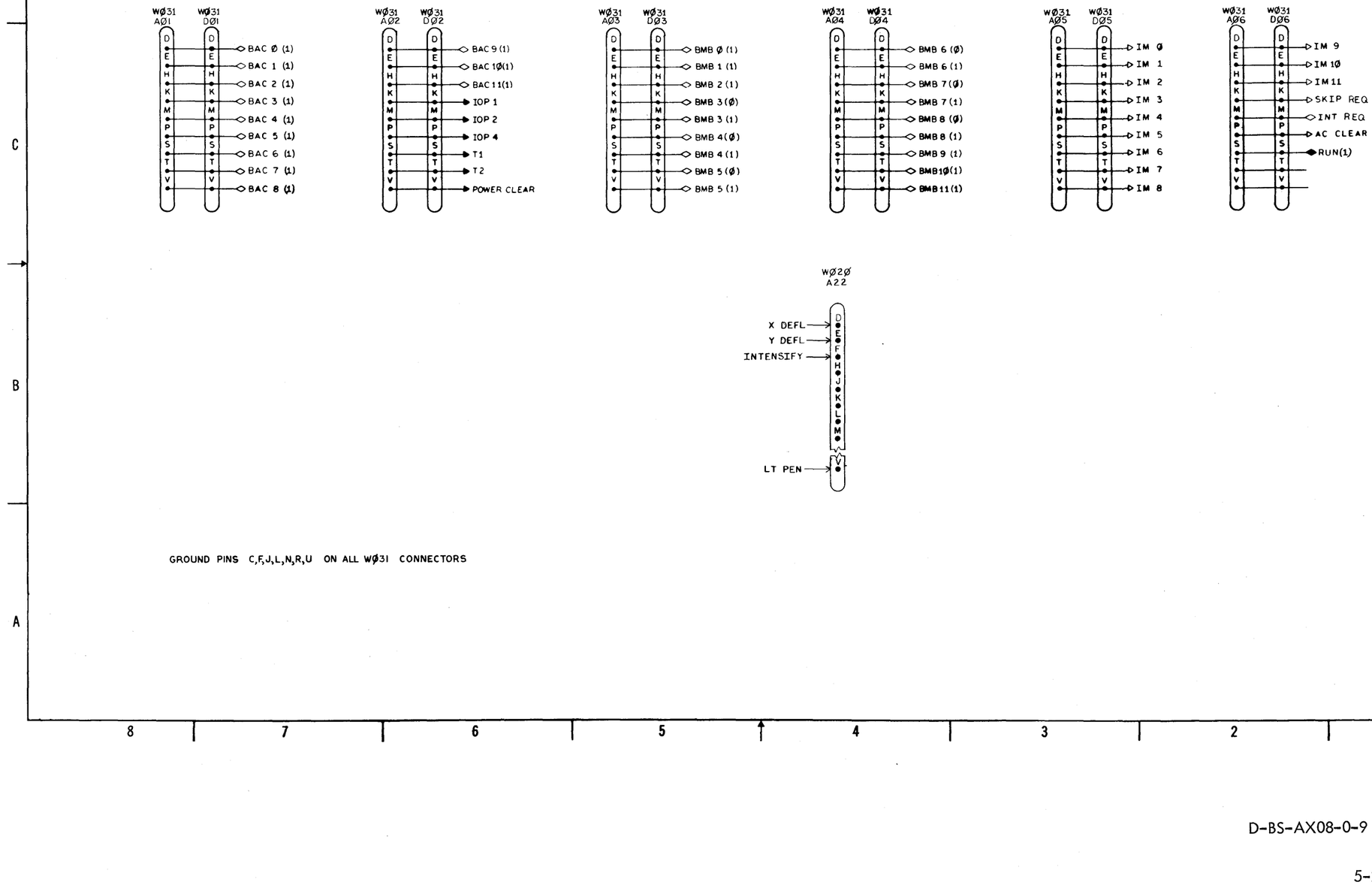
D-BS-AX08-0-4 Enable and Contingency Registers

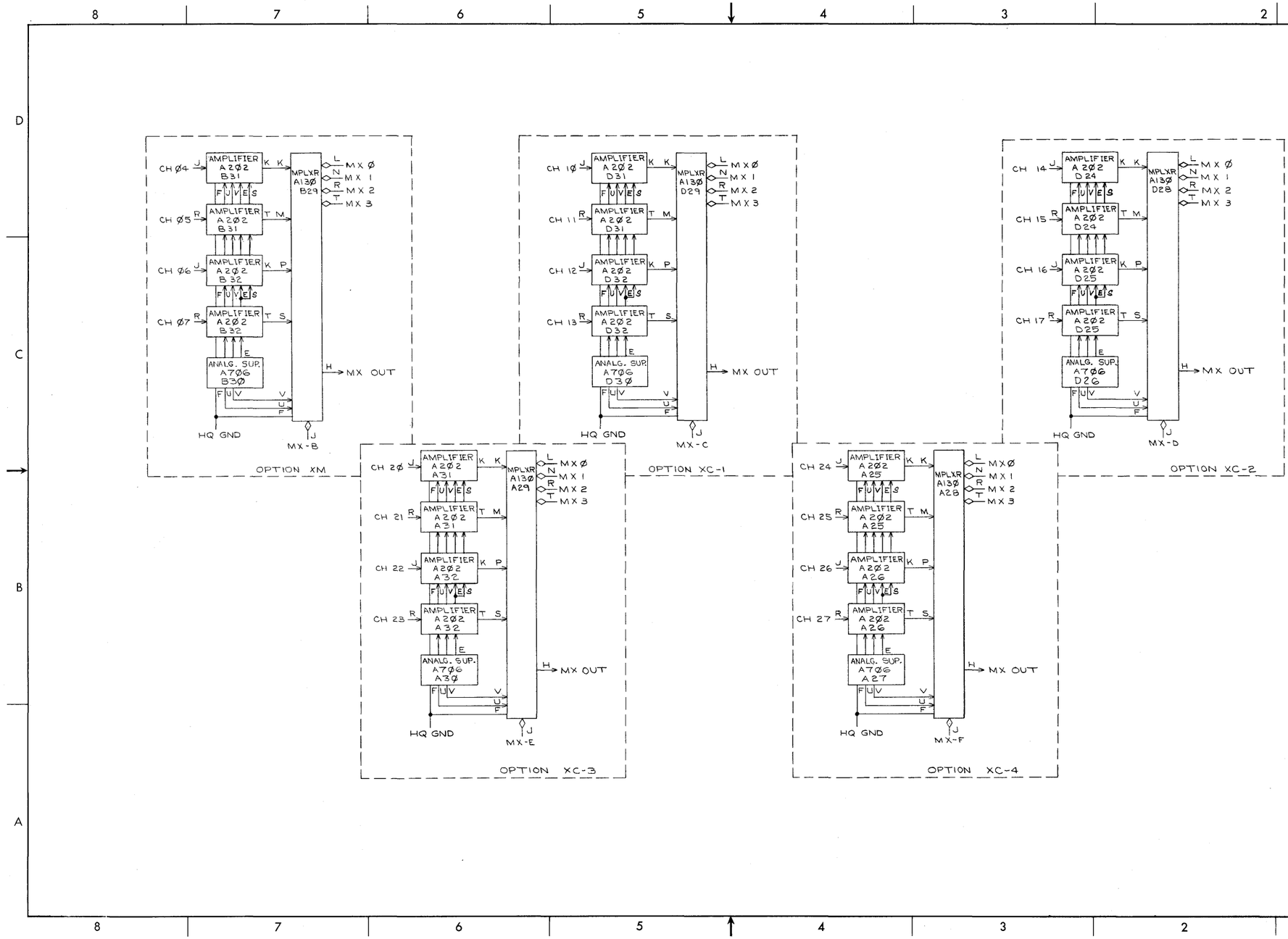

BMB 1Ø(1)
B BMB 1Ø (1)
BMB 11(1)
B BMB 11 (1)
BAC Ø(1)
B BAC Ø(1)
BAC 1(1)
B BAC 1(1)
BAC 2(1)
B BAC 2(1)
BAC 3(1)
B BAC 3(1)
BAC 4(1)
B BAC 4(1)
BAC 5(1)
B BAC 5(1)
BAC 6(1)
B BAC 6(1)
BAC 7(1)
B BAC 7(1)
BAC 8(1)
B BAC 8(1)
BAC 9(1)
B BAC 9(1)
BAC 1Ø(1)
B BAC 1Ø(1)
BAC 11(1)
B BAC 11(1)
IOP 1
IO Ø7
IOT ACMX
B IOP 1
IO Ø6
IOT ICMX
R1Ø7 BØ1
R1Ø7 BØ2
R1Ø7 BØ3
R1Ø7 BØ4
R1Ø7 A13
R113 A14
PA R6Ø3 B12


MX-A MX-B MX-C MX-D MX-E MX-F MX-H
RESET MPX
DCDR R151 D12
OPTION XM
RESET MPX
MPX 1 (Ø)
MPX 2 (Ø)
MPX 3 (Ø)
MPX 4 (Ø)
IOT ICMX
IOØ6
NEXT MX OK
MPX Ø (Ø)
IOT ACMX
B BAC 7 (Ø)
B BAC 7 (1)
B BAC 8 (Ø)
B BAC 8 (1)
B BAC 9 (Ø)
B BAC 9 (1)
B BAC 1Ø (Ø)
B BAC 1Ø (1)
B BAC 11 (Ø)
B BAC 11 (1)
ADC IP (1)
DIM
BRIGHT
NORM
* NORM
* BRIGHT
* DIM
ON INTENS
B IOP 4
DIS GRP
DB Ø (Ø)
DB 1 (Ø)
2000 PF
B PWR CLR
IOT DSB
B BMB1Ø (Ø)
B BMB1Ø (1)
B BMB11 (1)
B BMB11 (Ø)
DB Ø (1)
OPTION XR
SCOPE INTENSIFIER WG 81 A21
R (-)
N (+)
INTENSIFY
Y OUT
Y DEFL
X OUT
X DEFL
MX Ø
MX 1
MX 2
MX 3
IOT DYL
ADC IP (Ø)
IOT DXL
LOAD Y
LOAD X2
LOAD X1
NOTES:
* DIM: DSB Ø
NORM: DSB 1
BRIGHT: DSB 2

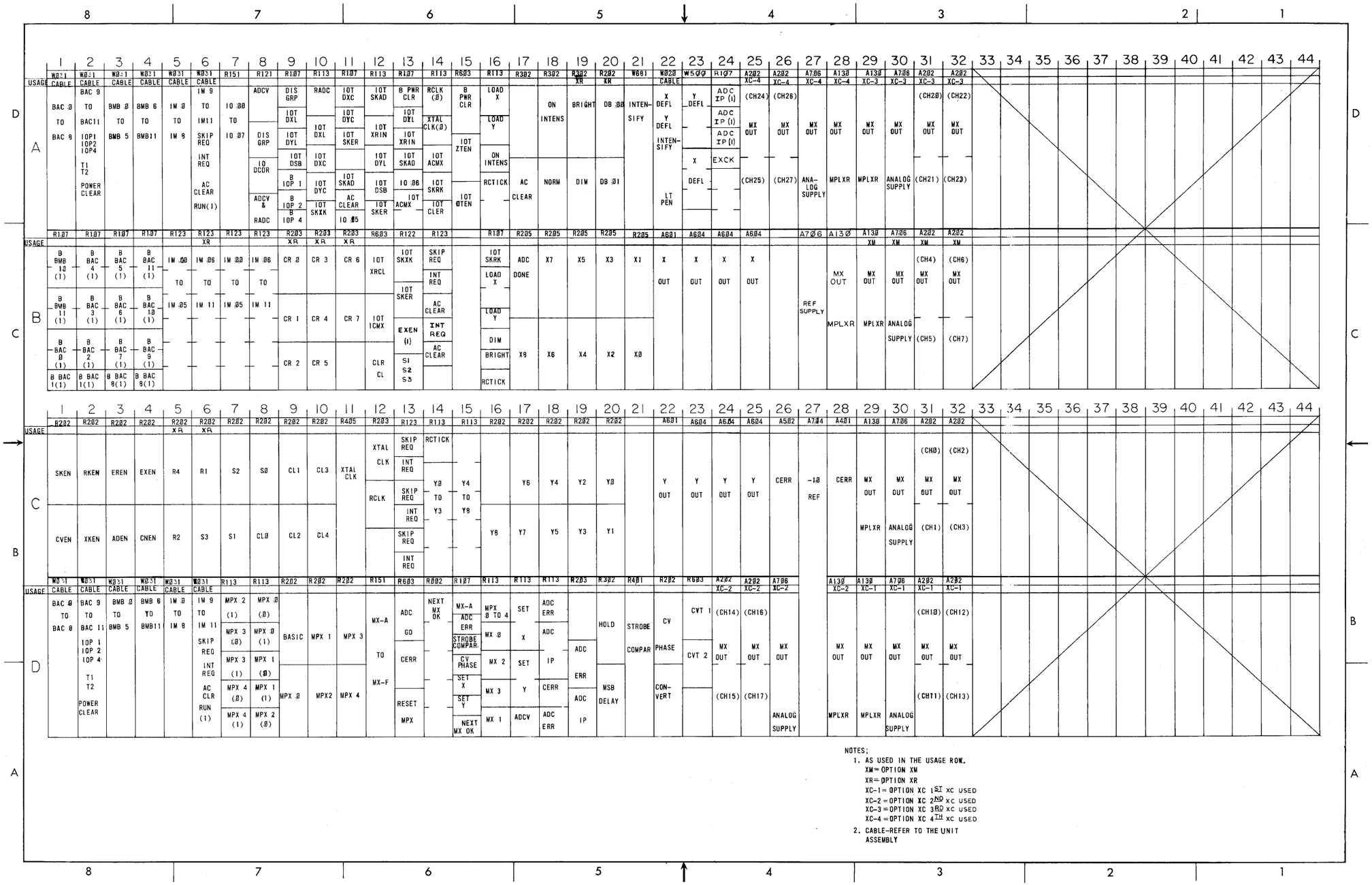

IM ϕϕ
IM ϕ1
IM ϕ2
IM ϕ3
IM ϕ4
IM ϕ5
IM ϕ6
IMϕ7
IMϕ8
IM ϕ9
IM 1ϕ
IM 11
Yϕ (1)
Y1 (1)
Y2(1)
Y3 (1)
Y4 (1)
Y5 (1)
Y6 (1)
Y7(1)
Y8(1)
R123 Bϕ7
R123 Bϕ8
R123 BØ8
5ϕϕNS R3ϕ2 A17
RADC
AC CLEAR
R123 B14
Sϕ (1)
IOT XRIN
S1 (1)
S2 (1)
S3 (1)
CRϕ(1)
CR1 (1)
CR2(1)
CR3(1)
CR4(1)
CR5(1)
CR6(1)
CR7(1)
R123 Bϕ5
R123 Bϕ6
OPTION XR


-10 V REF
33K
Y OUT
A604 C25
A604 C24
A604 C23
A601 C22
-10 REF
HQ GND
SET Y
R208 C20 Y0
R208 C19 Y1
R208 C19 Y2
R208 C18 Y3
R208 C18 Y4
R208 C18 Y5
R208 C17 Y6
R208 C17 Y7
R208 C16 Y8
CERR
X1(1)
X2(1) CVT 2
X3(1)
X4(1)
X5(1)
X6(1)
X7(1)
X8(1)
ADC DONE (1)
X1(1)
X2(1)
X3(1)
X4(1)
X5(1)
X6(1)
X7(1)
X8(1)
B BAC 3 (1) LOAD Y
B BAC 4(1)
B BAC 5(1)
B BAC6(1)
B BAC 7(1)
B BAC 8(1)
B BAC 9(1)
B BAC 10(1)
B BAC 11(1)
R113 C14
R113 C15
-10 V REF
33K
X OUT
A604 B25
A604 B24
A604 B23
A601 B22
-10 REF
HQ GND
R205 B21 X0
R205 B21 X1
R205 B20 X2
R205 B20 X3
R205 B19 X4
R205 B19 X5
R205 B18 X6
R205 B18 X7
R205 B17 X8
SET X
CVT 1
X0(1)
X0(0)
X1(0)
X1(1)
X2(0)
X2(1)
X3(0)
X3(1)
X4(0)
X4(1)
X5(0)
X5(1)
X6(0)
X6(1)
X7(0)
X7(1)
LOAD X
LOAD X2
B BAC 3(0)
B BAC 4(1)
B BAC 5(1)
B BAC 6(1)
B BAC 7(1)
B BAC 8(1)
B BAC 9(1)
B BAC 0(1)
B BAC 11(1)

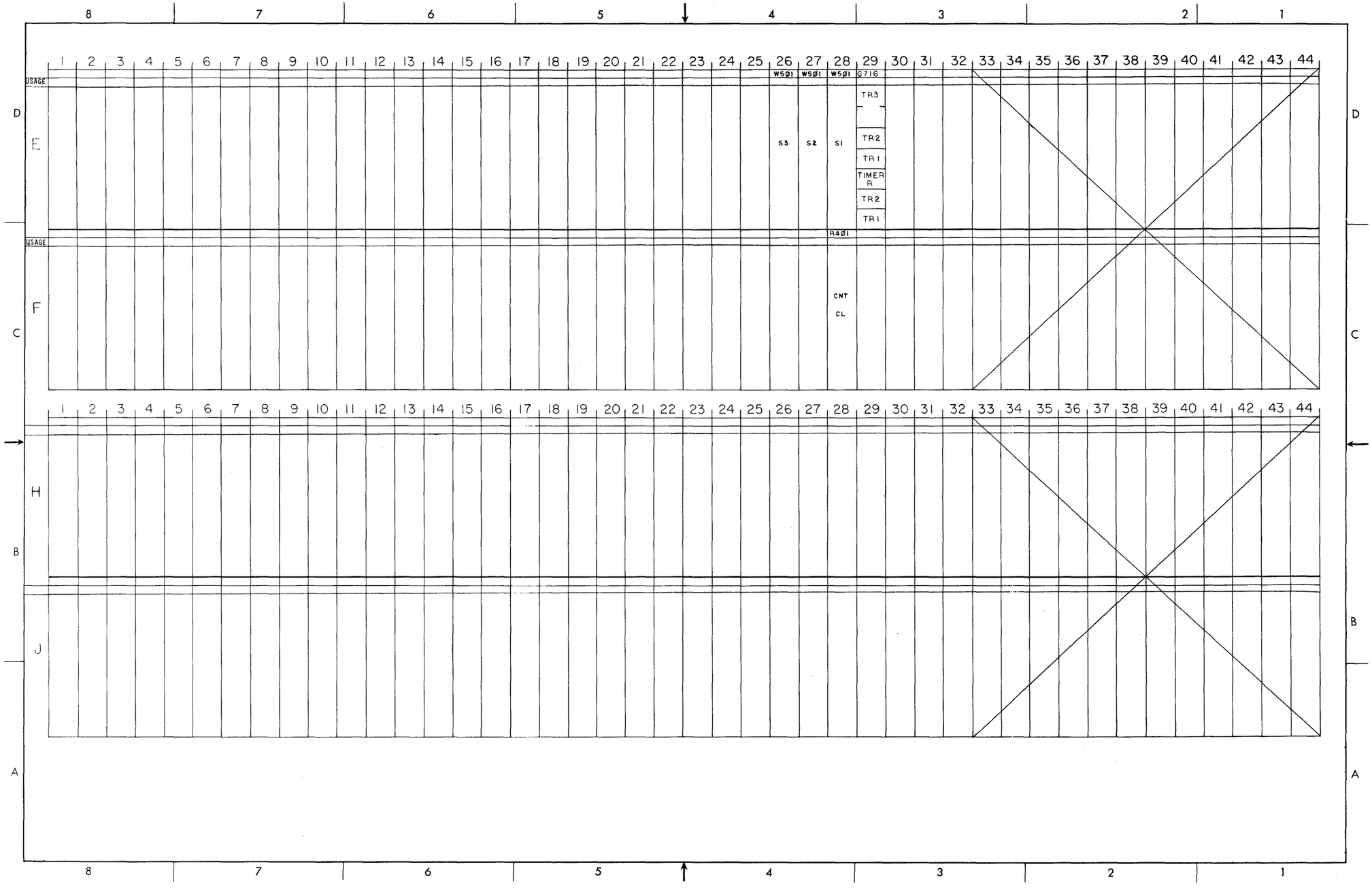

WØ31 AØ1
WØ31 DØ1
BAC Ø (1)
BAC 1 (1)
BAC 2 (1)
BAC 3 (1)
BAC 4 (1)
BAC 5 (1)
BAC 6 (1)
BAC 7 (1)
BAC 8 (1)
WØ31 AØ2
WØ31 DØ2
BAC 9 (1)
BAC 1Ø(1)
BAC 11(1)
IOP 1
IOP 2
IOP 4
T1
T2
POWER CLEAR
WØ31 AØ3
WØ31 DØ3
BMB Ø (1)
BMB 1 (1)
BMB 2 (1)
BMB 3 (Ø)
BMB 3 (1)
BMB 4 (Ø)
BMB 4 (1)
BMB 5 (Ø)
BMB 5 (1)
WØ31 AØ4
WØ31 DØ4
BMB 6 (Ø)
BMB 6 (1)
BMB 7 (Ø)
BMB 7 (1)
BMB 8 (Ø)
BMB 8 (1)
BMB 9 (1)
BMB1Ø(1)
BMB11(1)
WØ31 AØ5
WØ31 DØ5
IM Ø
IM 1
IM 2
IM 3
IM 4
IM 5
IM 6
IM 7
IM 8
WØ31 AØ6
WØ31 DØ6
IM 9
IM 1Ø
IM 11
SKIP REQ
INT REQ
AC CLEAR
RUN(1)
WØ2Ø A22
X DEFL
Y DEFL
INTENSIFY
LT PEN
GROUND PINS C,F,J,L,N,R,U ON ALL WØ31 CONNECTORS



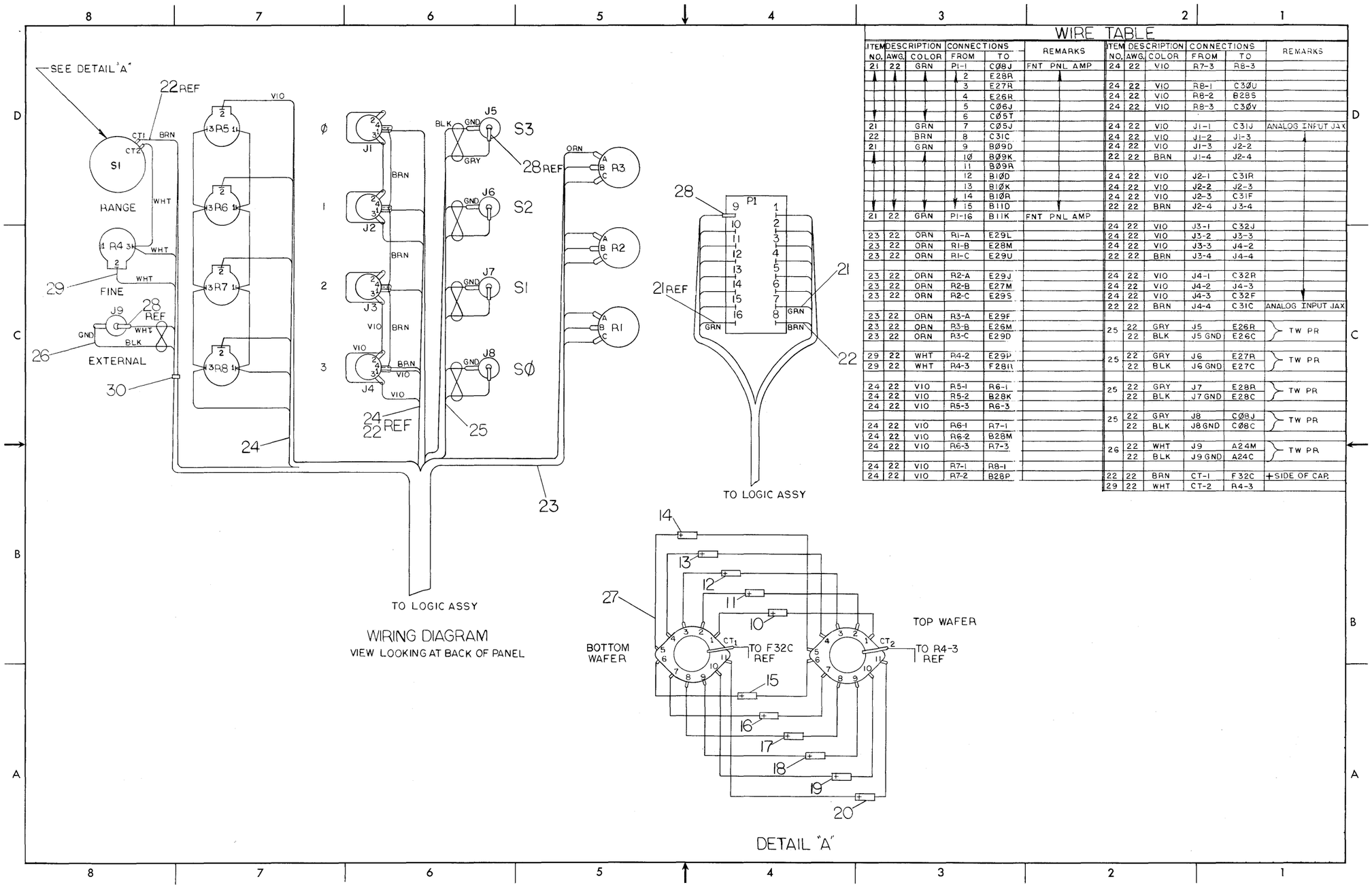
D-BS-AX08-0-10 Additional Channels
(Option XC)



D-MU-AX08-0-11 AX08 Lab Peripheral (UML)
(Sheet 1)



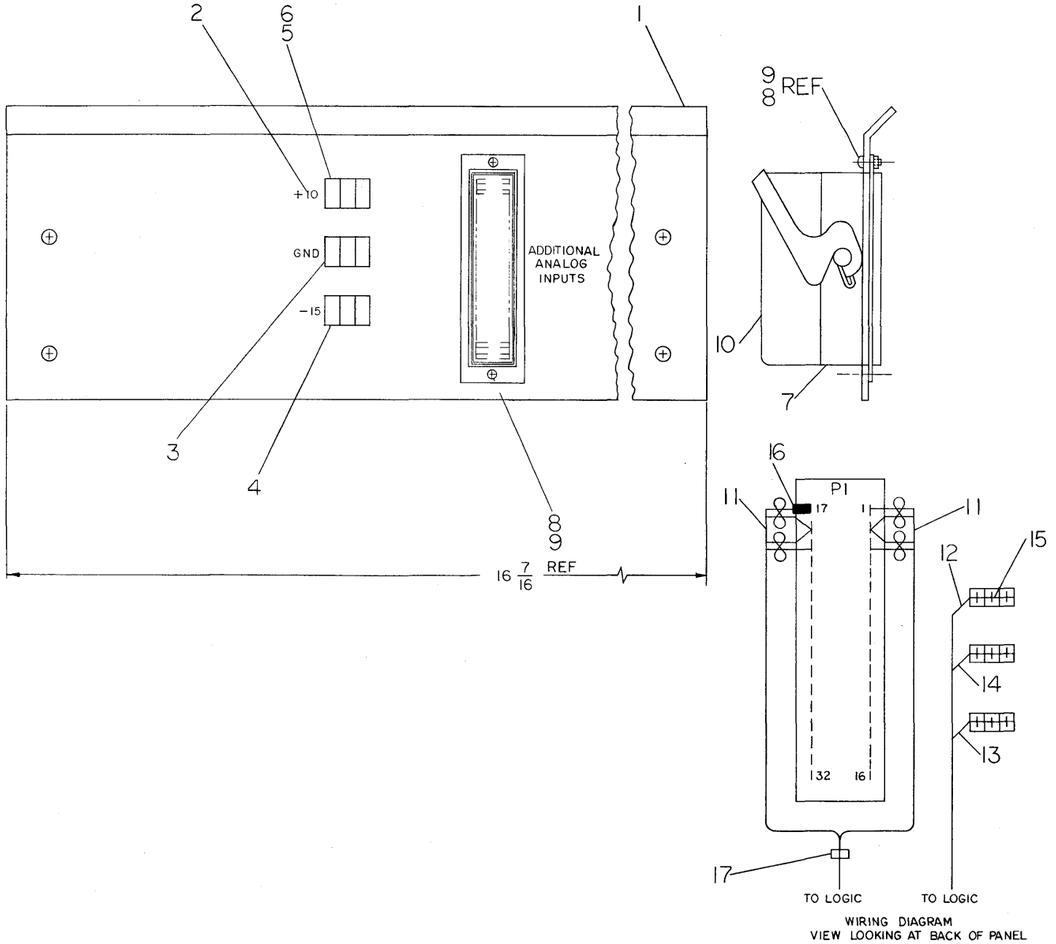
D-MU-AX08-0-11 AX08 Lab Peripheral (UML)
(Sheet 2)



WIRE TABLE

ITEM NO.	DESCRIPTION AWG.	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO	REMARKS
21	22	GRN	P1-1	CØ8J	FNT PNL AMP
			2	E28R	
			3	E27R	
			4	E26R	
			5	CØ6J	
			6	CØ5T	
21		GRN	7	CØ5J	
22		BRN	8	C31C	
21		GRN	9	BØ9D	
			10	BØ9K	
			11	BØ9R	
			12	BIØD	
			13	BIØK	
			14	BIØR	
			15	BIID	
21	22	GRN	P1-16	BIIK	FNT PNL AMP
23	22	ORN	R1-A	E29L	
23	22	ORN	R1-B	E28M	
23	22	ORN	R1-C	E29U	
23	22	ORN	R2-A	E29J	
23	22	ORN	R2-B	E27M	
23	22	ORN	R2-C	E29S	
23	22	ORN	R3-A	E29F	
23	22	ORN	R3-B	E26M	
23	22	ORN	R3-C	E29D	
29	22	WHT	R4-2	E29P	
29	22	WHT	R4-3	F28H	
24	22	VIO	R5-1	R6-1	
24	22	VIO	R5-2	B28K	
24	22	VIO	R5-3	R6-3	
24	22	VIO	R6-1	R7-1	
24	22	VIO	R6-2	B28M	
24	22	VIO	R6-3	R7-3	
24	22	VIO	R7-1	R8-1	
24	22	VIO	R7-2	B28P	

ITEM NO.	DESCRIPTION AWG.	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO	REMARKS
24	22	VIO	R7-3	R8-3	
24	22	VIO	R8-1	C3ØU	
24	22	VIO	R8-2	B28S	
24	22	VIO	R8-3	C3ØV	
24	22	VIO	J1-1	C31J	ANALOG INPUT JAX
24	22	VIO	J1-2	J1-3	
24	22	VIO	J1-3	J2-2	
22	22	BRN	J1-4	J2-4	
24	22	VIO	J2-1	C31R	
24	22	VIO	J2-2	J2-3	
24	22	VIO	J2-3	C31F	
22	22	BRN	J2-4	J3-4	
24	22	VIO	J3-1	C32J	
24	22	VIO	J3-2	J3-3	
24	22	VIO	J3-3	J4-2	
22	22	BRN	J3-4	J4-4	
24	22	VIO	J4-1	C32R	
24	22	VIO	J4-2	J4-3	
24	22	VIO	J4-3	C32F	
22	22	BRN	J4-4	C31C	ANALOG INPUT JAX
25	22	GRY	J5	E26R	TW PR
	22	BLK	J5 GND	E26C	
25	22	GRY	J6	E27R	TW PR
	22	BLK	J6 GND	E27C	
25	22	GRY	J7	E28R	TW PR
	22	BLK	J7 GND	E28C	
25	22	GRY	J8	CØ8J	TW PR
	22	BLK	J8 GND	CØ8C	
26	22	WHT	J9	A24M	TW PR
	22	BLK	J9 GND	A24C	
22	22	BRN	CT-1	F32C	+SIDE OF CAR
29	22	WHT	CT-2	R4-3	



WIRING DIAGRAM
VIEW LOOKING AT BACK OF PANEL

WIRE TABLE

ITEM NO.	AWG	COLOR	FROM	TO	REMARKS
11	22	GRN	P1- 1	B31J	} TW PAIR
		BRN	2	B31F	
		BRN	2	B31F	} TW PAIR
		GRN	3	B31R	
		GRN	4	D31J	} TW PAIR
		BRN	5	D31F	
		BRN	5	D31F	} TW PAIR
		GRN	6	D31R	
		GRN	7	D24J	} TW PAIR
		BRN	8	D24F	
		BRN	8	D24F	} TW PAIR
		GRN	9	D24R	
		GRN	10	A31J	} TW PAIR
		BRN	11	A31F	
		BRN	11	A31F	} TW PAIR
		GRN	12	A31R	
		GRN	13	A25J	} TW PAIR
		BRN	14	A25F	
		BRN	14	A25F	} TW PAIR
		GRN	15	A25R	
			16	RESERVE	
		GRN	17	B32J	} TW PAIR
		BRN	18	B32F	
		BRN	18	B32F	} TW PAIR
		GRN	19	B32R	
		GRN	20	D32J	} TW PAIR
		BRN	21	D32F	
		BRN	21	D32F	} TW PAIR
		GRN	22	D32R	
		GRN	23	D25J	} TW PAIR
		BRN	24	D25F	
		BRN	24	D25F	} TW PAIR
		GRN	25	D25R	
		GRN	26	A32J	} TW PAIR
		BRN	27	A32F	
		BRN	27	A32F	} TW PAIR
		GRN	28	A32R	
		GRN	29	A26J	} TW PAIR
		BRN	30	A26F	
11	22	BRN	30	A26F	} TW PAIR
		GRN	31	A26R	
			P1 - 32	RESERVE	
12	18	RED	+10	FØIA	POWER WIRING
13	18	BLUE	-15	FØIB	POWER WIRING
14	18	BLK	GND	FØIC	POWER WIRING

NOTES:
1. ALL WIRES TO BE SOLDERED IN PLACE
2. ALL WIRES TO LOGIC ASSY TO BE 40" ± 2" LG
3. USE BRADY MARKERS ITEM #18 TO IDENTIFY WIRES

D-AD-7005832-0-0 Rear Panel Assembly

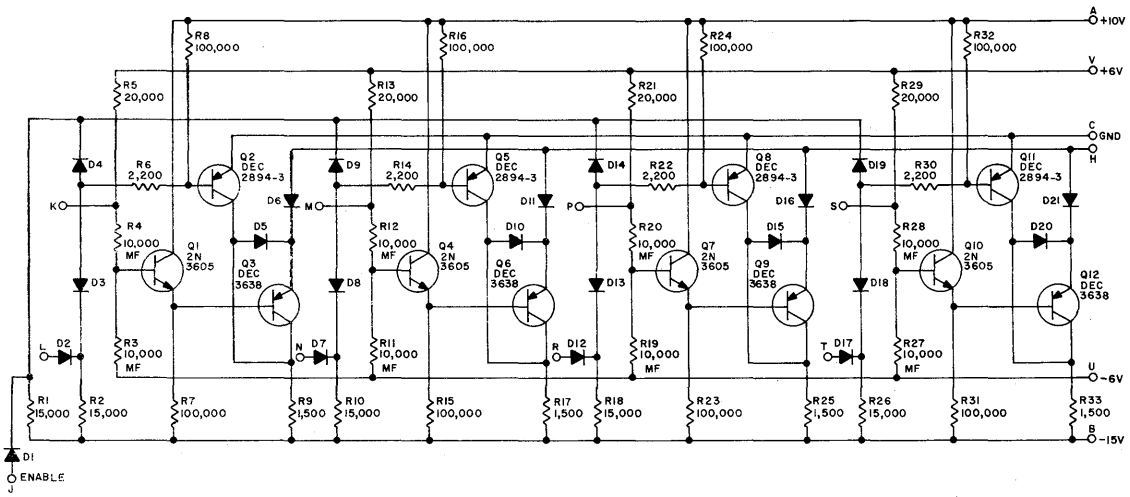
S0	C0
S1	C1
S2	C2
S3	C3
R4	C4
R2	C5
R1	C6
GND	C7

Front Panel Amphenol Connector Pins
(Front View)

4	6
HQ	HQ
5	7
10	12
HQ	HQ
11	13
14	16
HQ	HQ
15	17
20	22
HQ	HQ
21	23
24	26
HQ	HQ
25	27
GND	GND

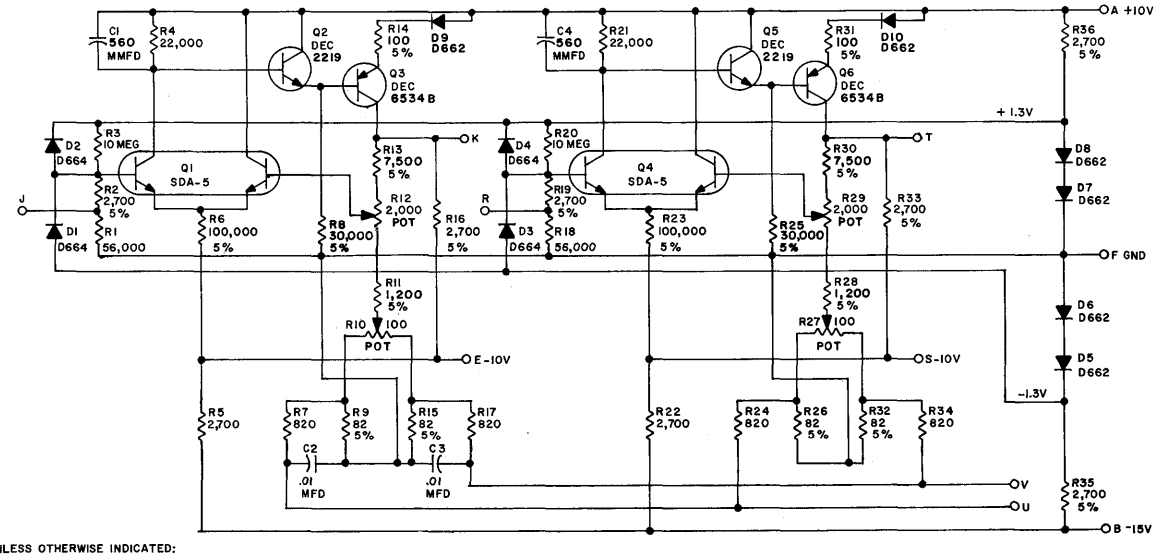
Rear Panel Amphenol Connector
(Front View of Panel)

Numbers refer to Channel Numbers, HQ is HQGND for Pair of channels on either side of GND is chassis GND.



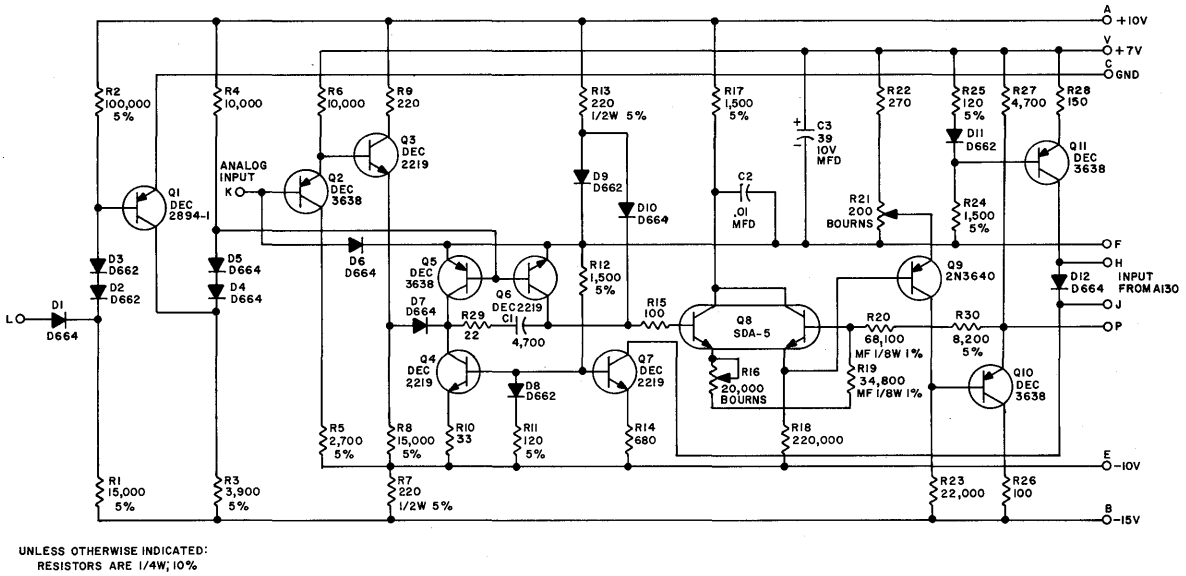
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664
MF RESISTORS ARE 1/8W; 1%

A130 Multiplex Linc-8

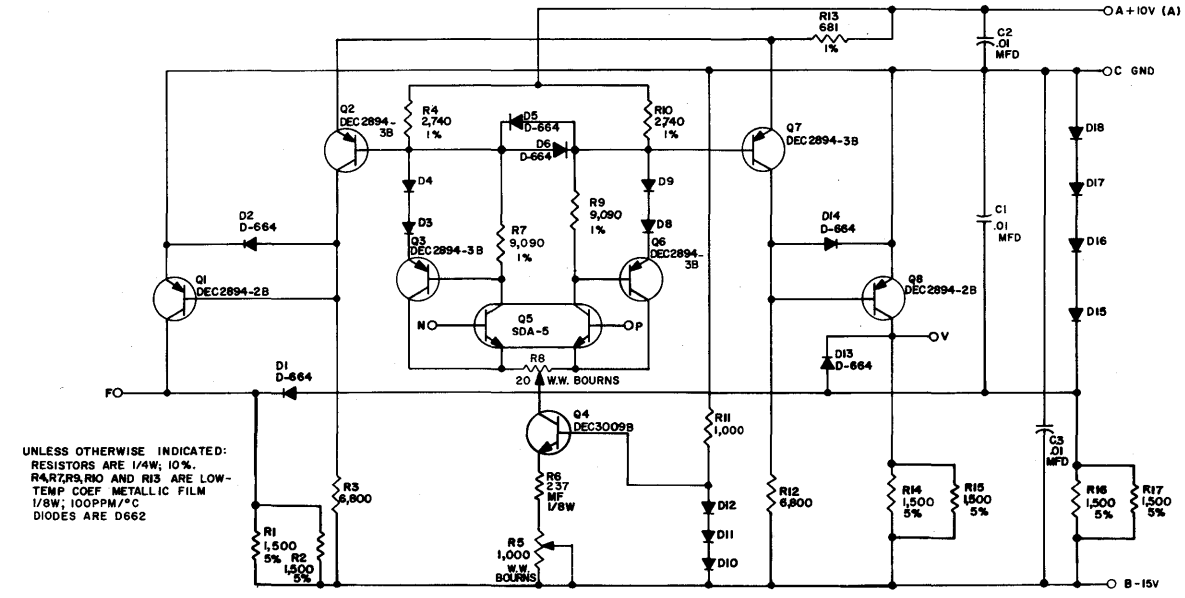


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
POTS ARE #275P

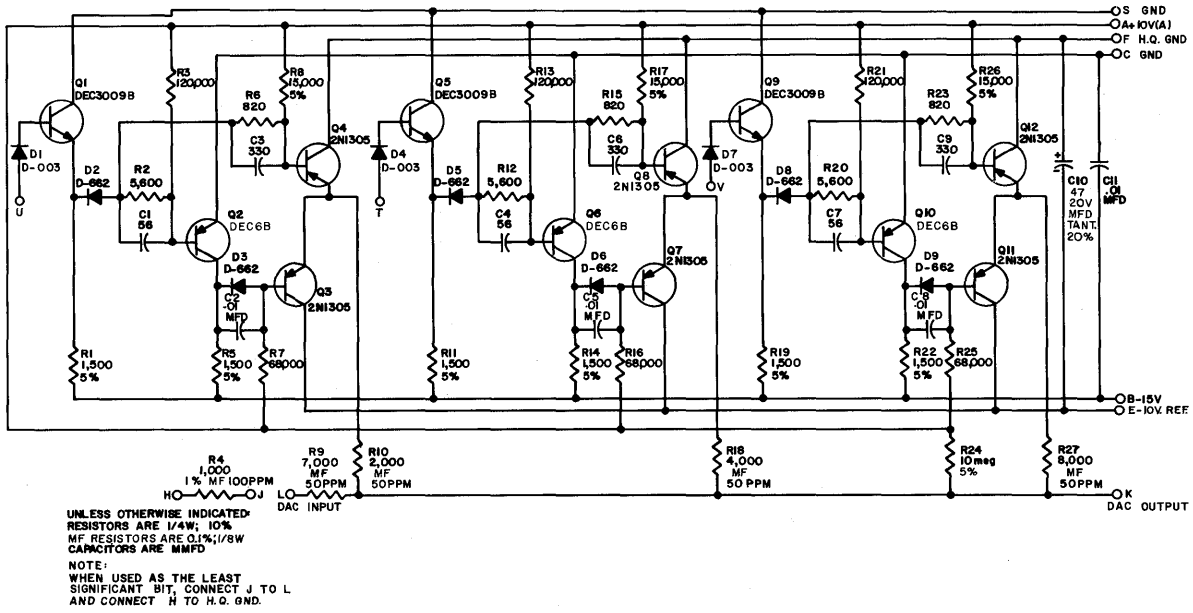
A202 Two Analog Preamplifiers



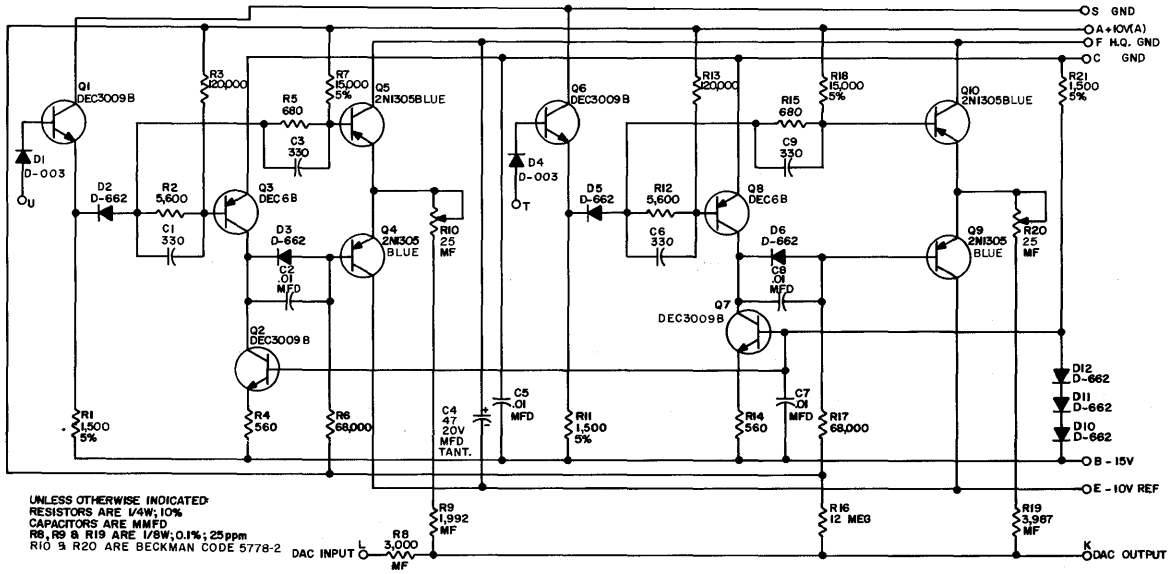
A401 Sample and Hold



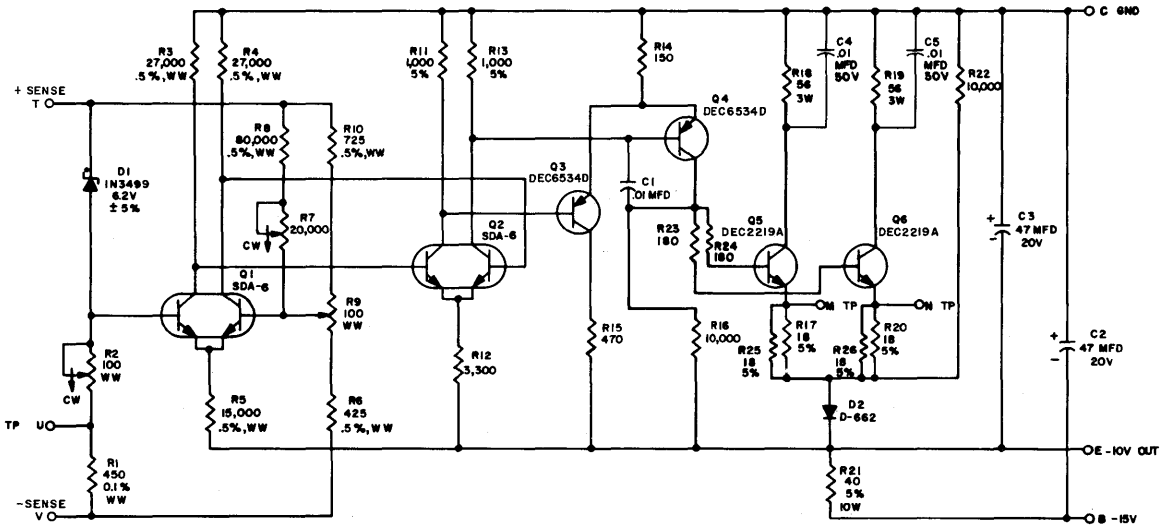
A502 Comparator



A601 Digital-Analog Converter

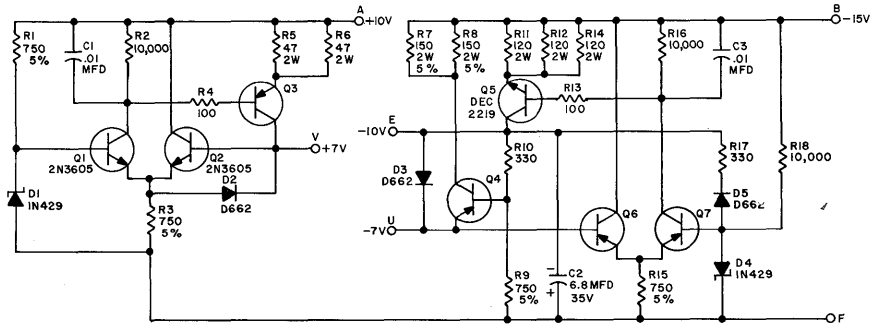


A604 Digital-Analog



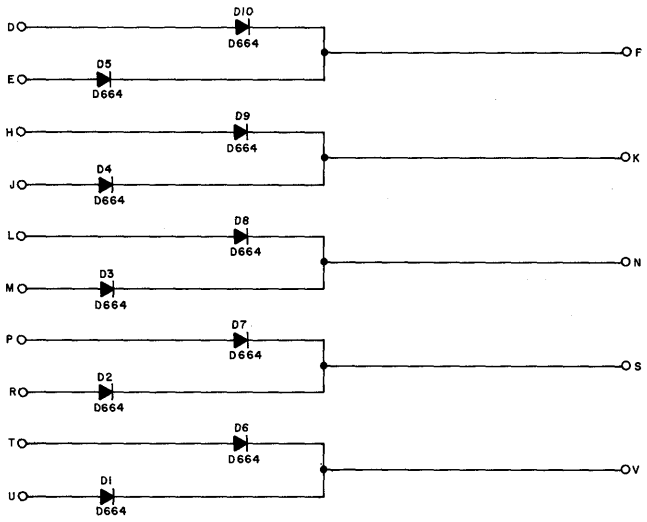
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
R10, R6 AND R1 ARE DAVEN 3PPM TYPE 1195
R3, R4, R5 AND R8 ARE DAVEN 20 PPM TYPE 1283
R2, R9 ARE 50 PPM DAYSTRUM TRANSITRIM
R7 IS A #275P

A704 Reference Supply



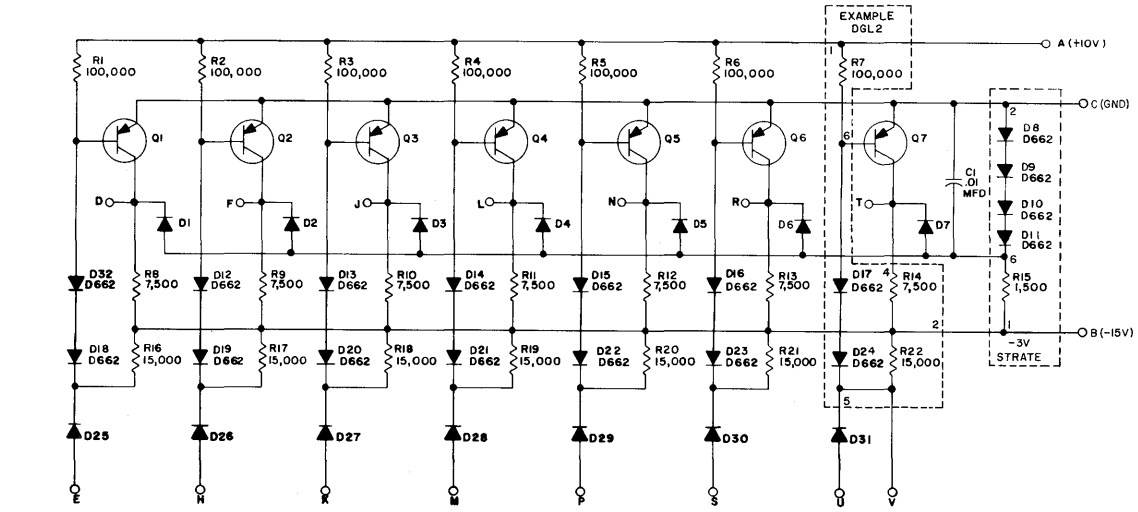
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC3638

A706 Power Supply for A202



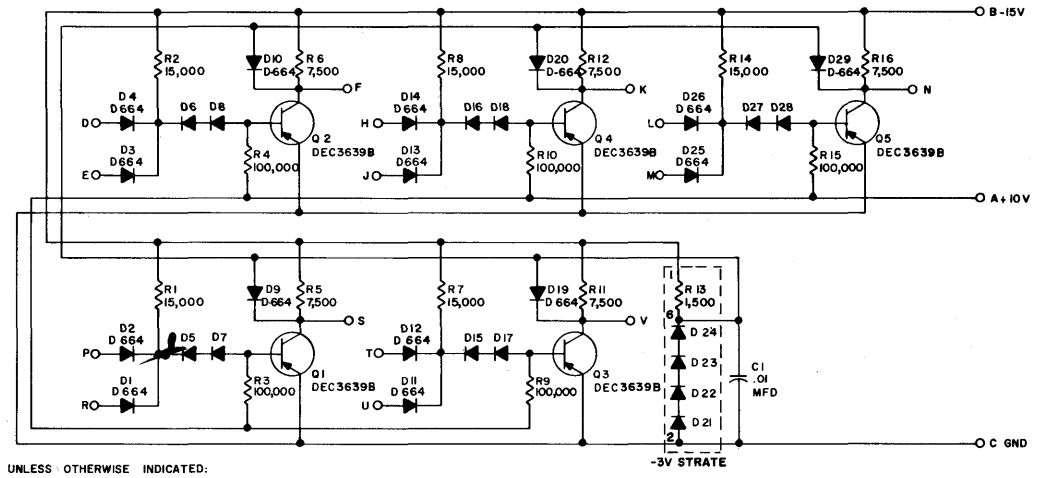
G716 Resistor Card

R002 Diode Network



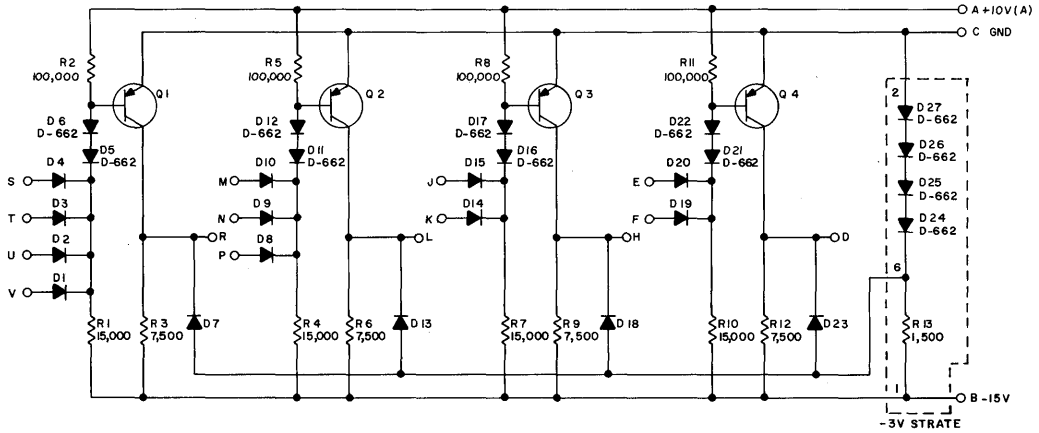
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

R107 Inverter



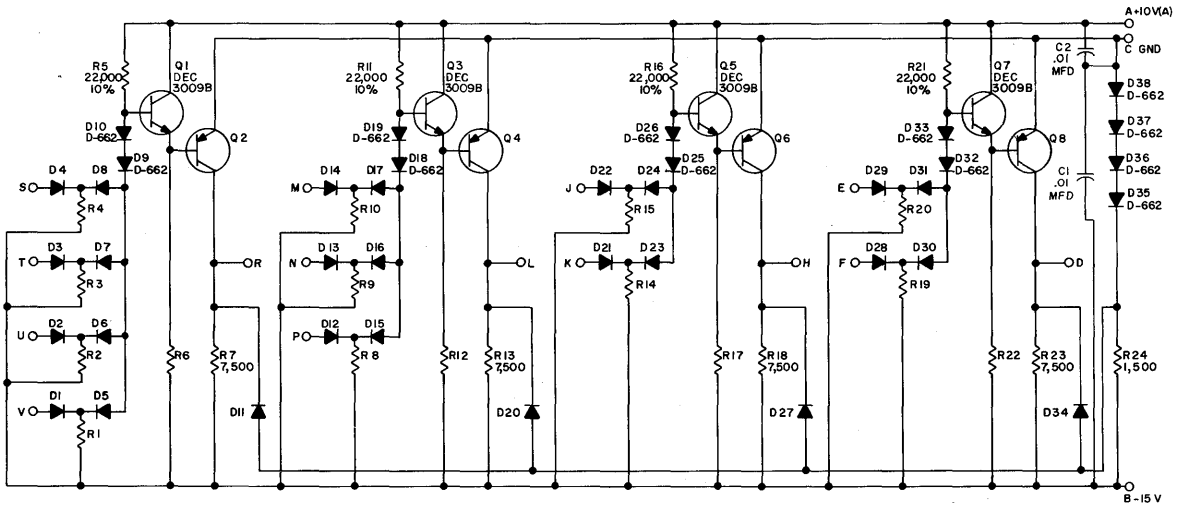
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

R113 NAND/NOR Gate



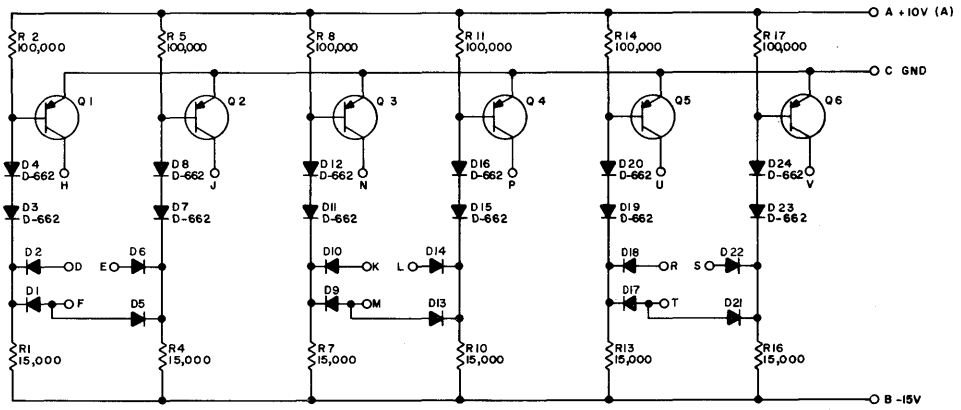
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639B
DIODES ARE D-664
RESISTORS ARE 1/4 W, 5%

R121 NAND/NOR Gate



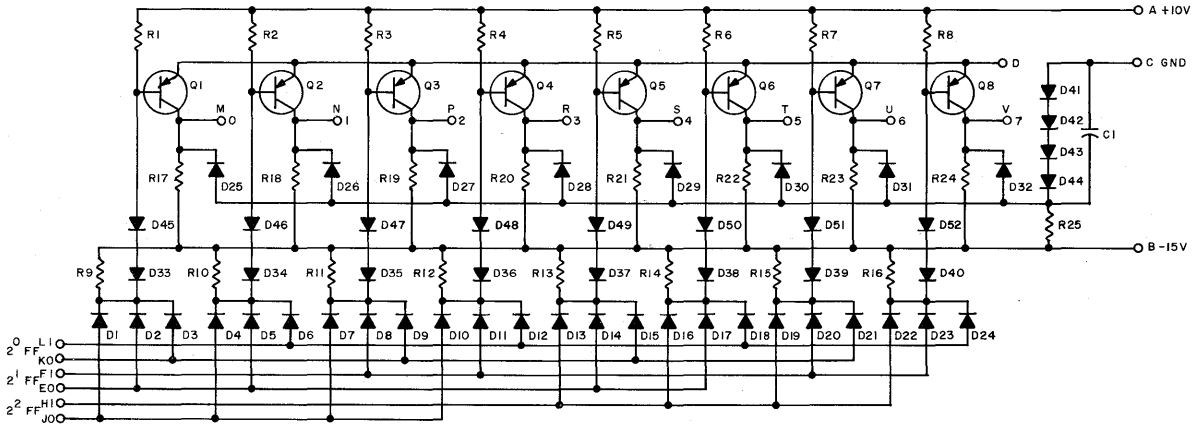
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 15,000; 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B

R122 NOR/NAND Gate

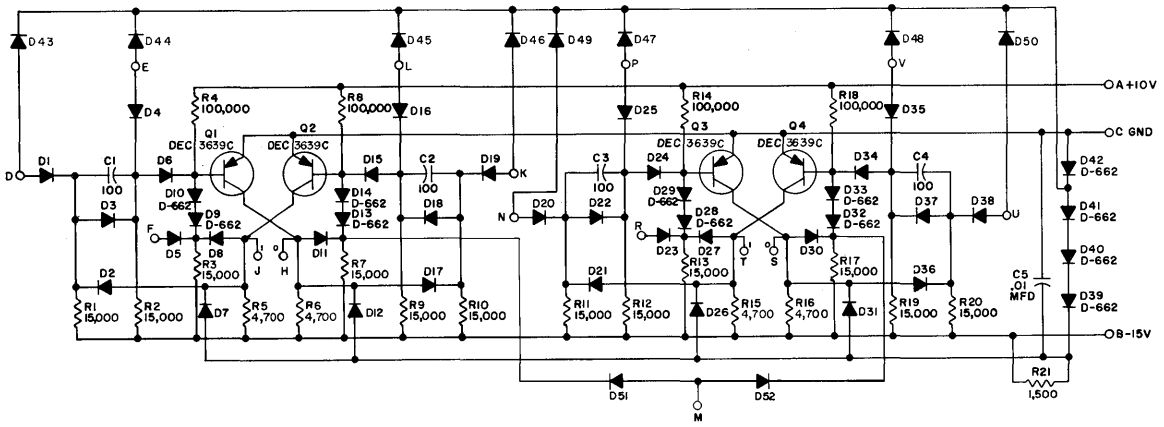


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

R123 Input Bus

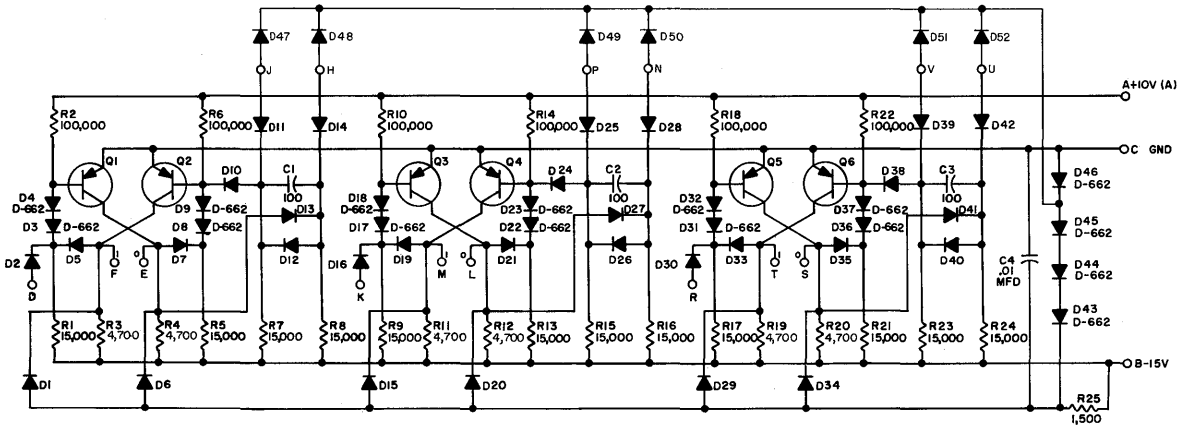


R151 Binary to Octal Decoder



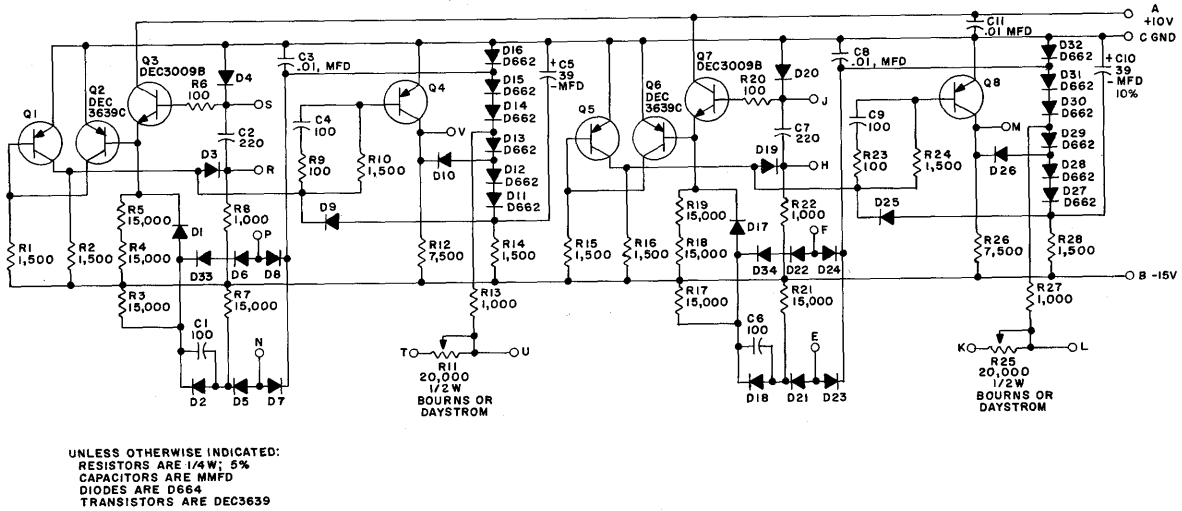
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

R202 Dual Flip-Flop

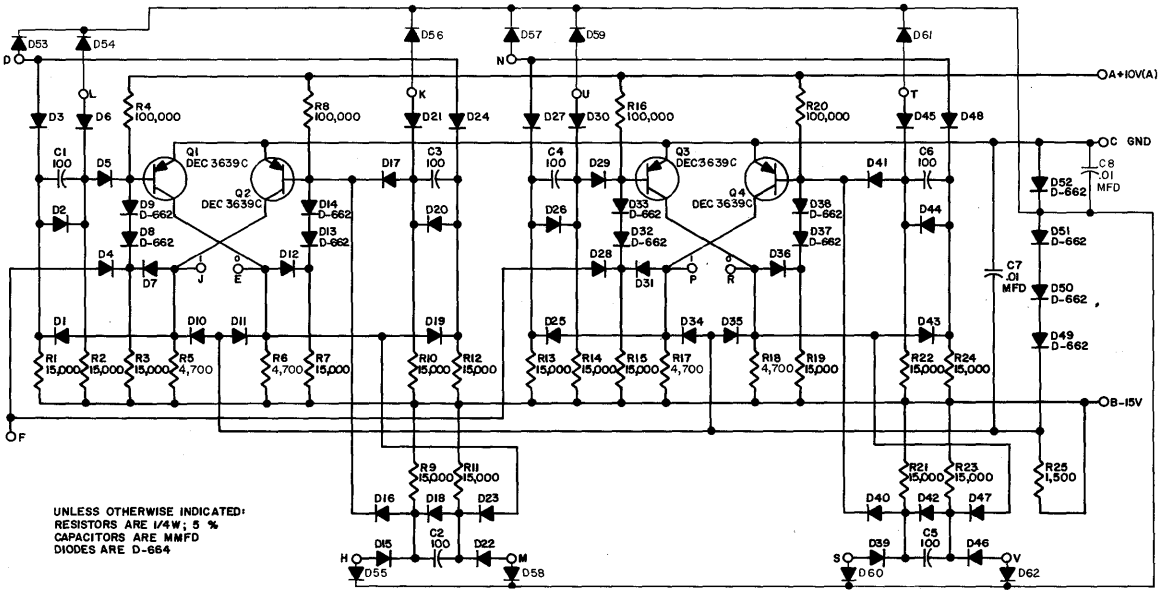


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C

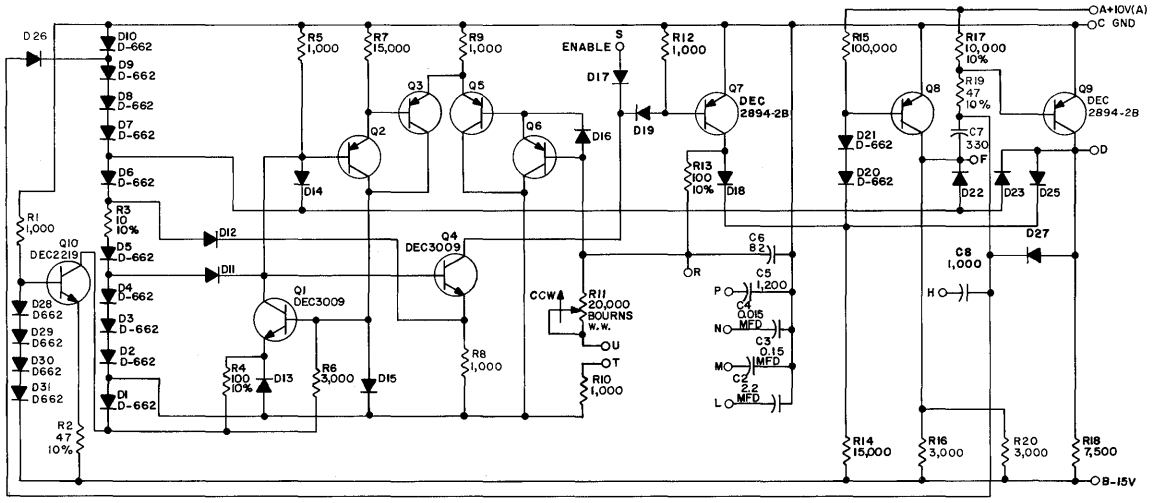
R203 Triple Flip-Flop



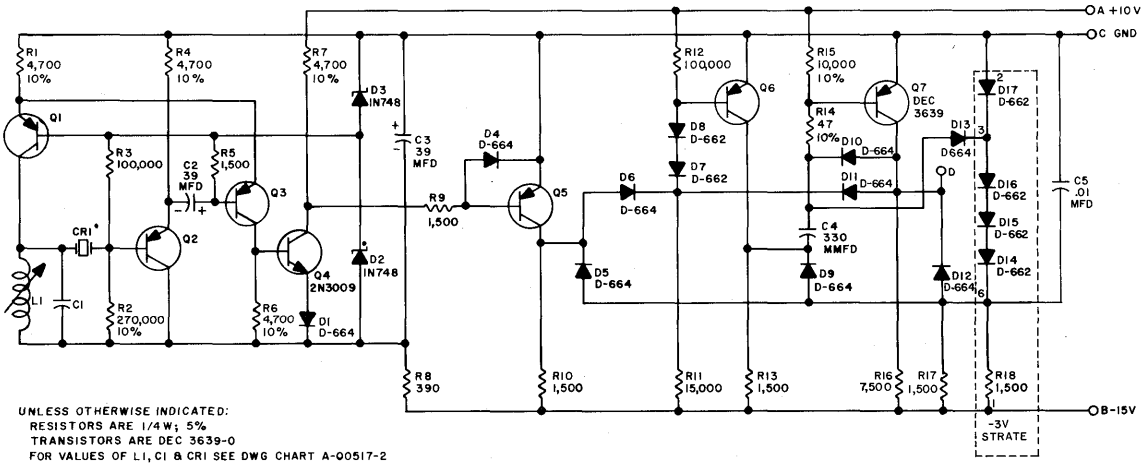
R205 Dual Flip-Flop



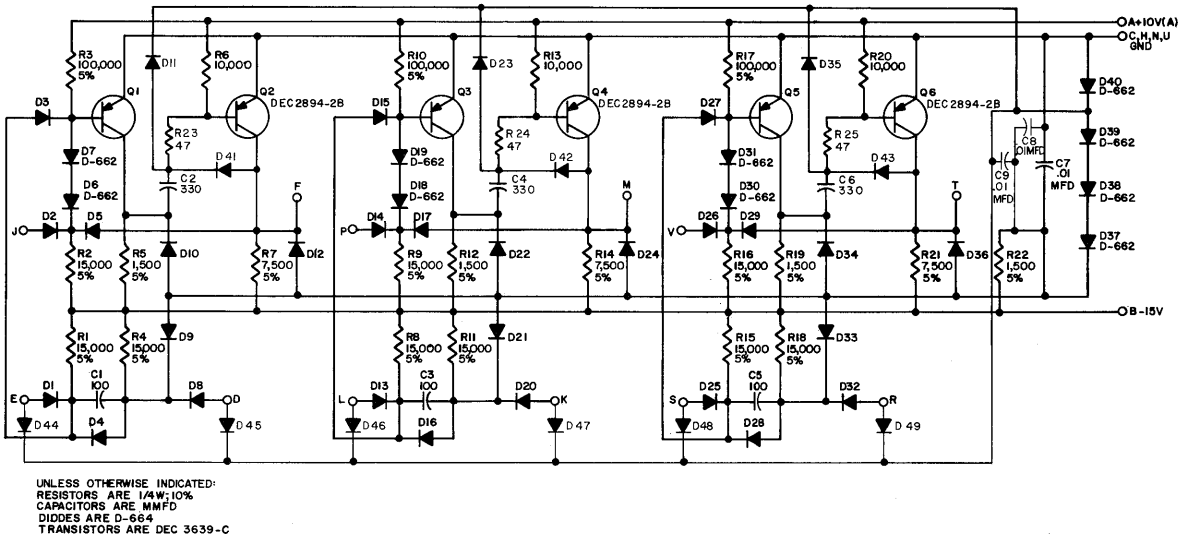
R302 Dual Delay Multivibrator



R401 Variable Clock

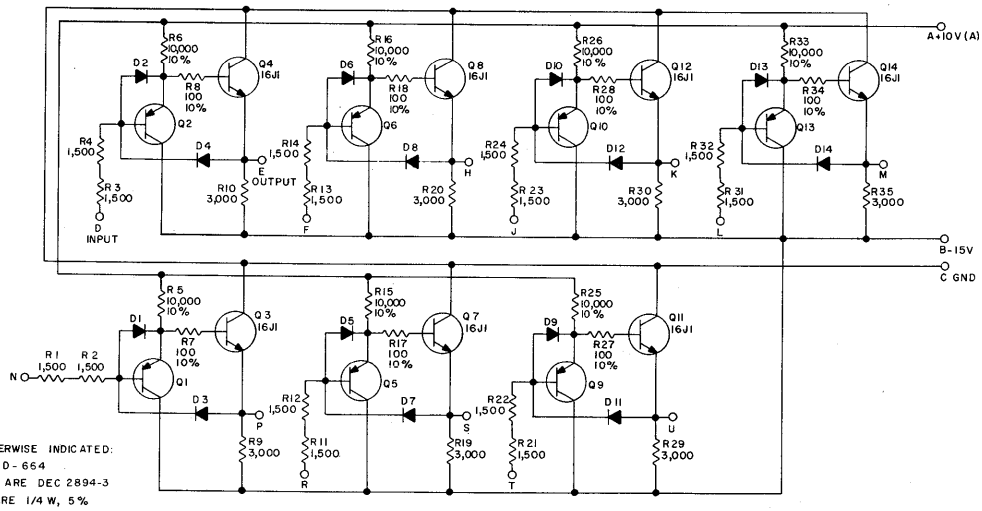


R405 Crystal Clock



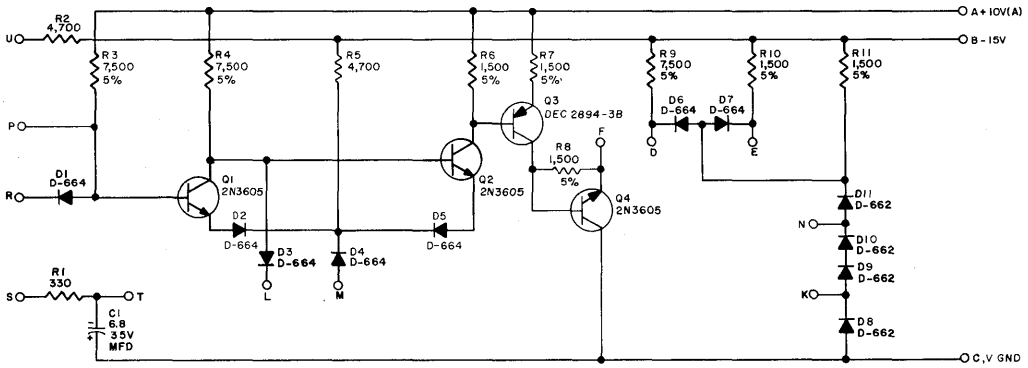
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-C

R603 Pulse Amplifier

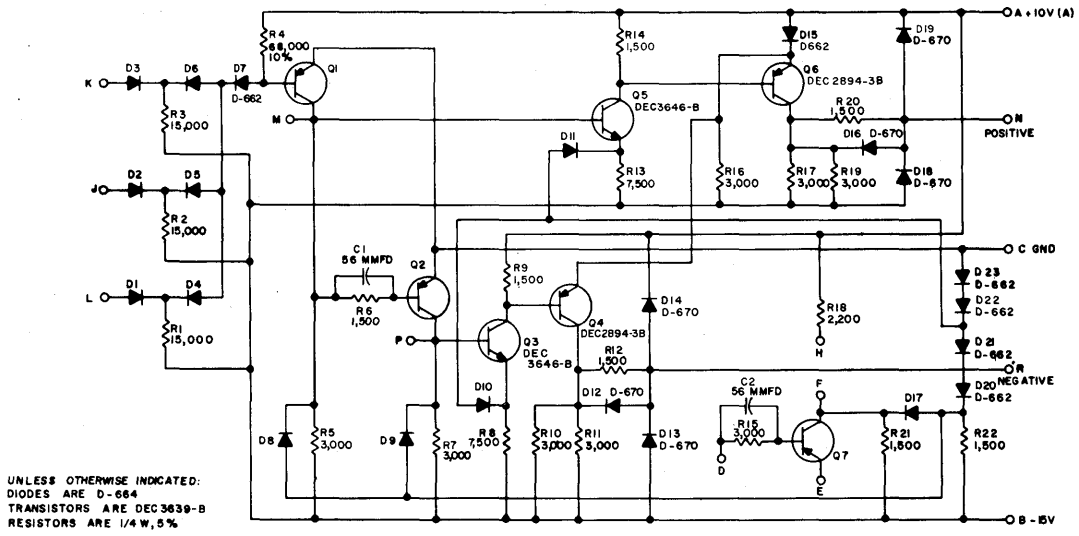


UNLESS OTHERWISE INDICATED:
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-3
RESISTORS ARE 1/4 W, 5%

W500 High Impedance Follower



W501 Schmitt Trigger



W681 Scope Intensifier