TU60 DECassette tape transport maintenance manual

DEC-00-HTU60-C-D

digital equipment corporation · maynard, massachusetts

1st Edition December 1972
2nd Printing (Rev) April 1973
3rd Printing (Rev) October 1973

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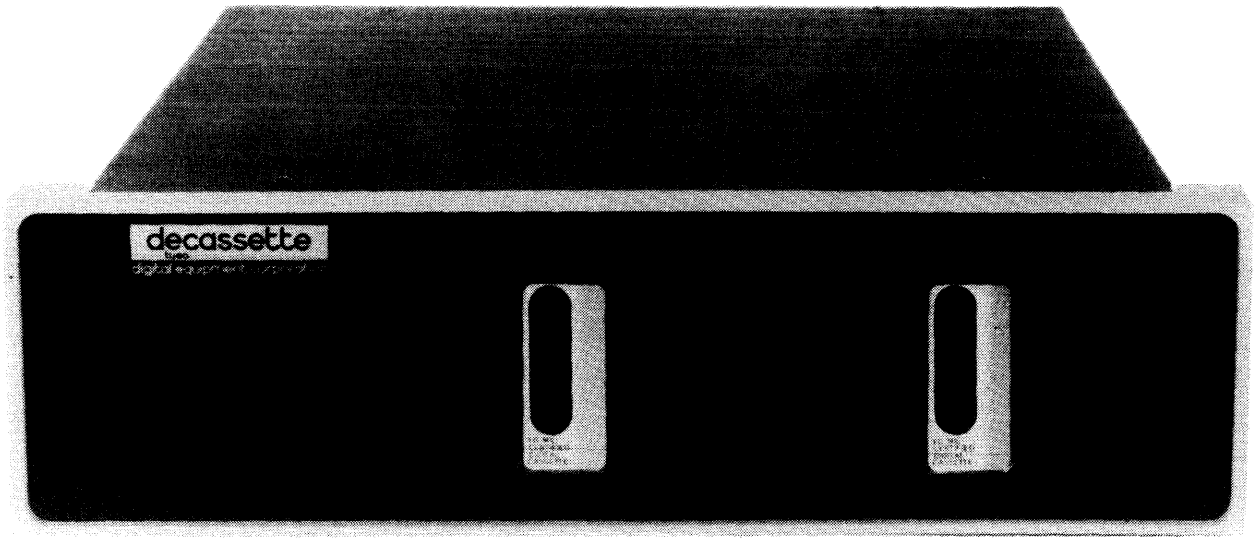


TU60 DECassette Tape Transport

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TU60 DECassette Tape Transport is a solid state, magnetic tape, data storage device. This device is composed of two individual tape drives and two electronic modules that contain all the logic and circuit components necessary for data formatting, error checking, and cassette housekeeping. The associated processor contains an interface module which is capable of: converting the processor codes into commands for transmission to the TU60, interpreting status flags received from the TU60, and storing input/output data. Each interface module can control one TU60 (2 drives). An internal H751 Power Supply furnishes +5 Vdc logic power and +15 & -15 Vdc operating power for the drive motors and operational amplifiers.

During a write operation, 8-bit data bytes are parallel transferred from the interface to the TU60, phase encoded, and serially recorded on the tape. Except for the tape length, there is no maximum limit to the number of bytes that may be grouped into a data block; however, it is not possible to replace an individual block on a recorded tape.

During a read operation, the self clocking data bits are serially read from the tape, then parallel transferred to the interface at a peak transfer rate of 562 bytes per second.

Tape motion within the digital cassette is directly controlled by two dc motors, without the use of capstans or pinch rollers. Because of this direct reel-to-reel drive system, tape speed across the read/write head varies as the take-up reel fills with tape. The tape speed for a read/write operation is approximately 6 inches per second at the beginning of the tape; however, the speed increases to approximately 12 inches per second at the end of the tape. Thus, the data blocks are written with varying bit densities, but at a constant frequency along the tape. The motion control logic within the transport ensures that tape motion stops only at a block or file gap.

1.2 CASSETTE RESTRICTIONS

It is extremely important that only DEC, 100 percent certified, Digital Tape Cassettes be used on the TU60 tape drives. The "heavy base" tape within the Digital Equipment Corporation Cassettes was specifically chosen to be compatible with the high drive tensions of the TU60. In addition, the head pressure pad material of the cassette has been carefully selected to allow proper tape stacking. For optimal operational characteristics, the dynamics of each tape drive require the use of only Digital Equipment Corporation Cassettes.

DO NOT ATTEMPT TO USE AN AUDIO CASSETTE ON THE TU60 TAPE DRIVES. Since the tape within an audio cassette is not designed to tolerate the high drive tensions of the TU60, use of this type cassette will result in extremely rapid deterioration of the tape and subsequent failure of the drive due to excessive tape oxide deposits on the read/write head and tape guides.

Because the DEC cassette is relatively more expensive than an audio cassette, it should not be used in place of an audio cassette. The lower "high-frequency rolloff" of the digital tape makes the DEC cassette a poor substitute for audio operations. In addition, the coefficient of friction of the DEC tape does not allow tape motion by capstan and pinch rollers as is usually the case with most audio recorders.

In short, the TU60 DECassette Tape Transport and the DEC, 100 percent certified, Digital Cassette are designed to be used together. Use of any cassette other than the DEC cassette may void the transport warranty.

1.3 SPECIFICATIONS

Table 1-1 lists the performance specifications of the TU60 DECassette Tape Transport. To obtain the specified data reliability, use only DEC, 100 percent certified, Digital Tape Cassettes. DEC cassettes are especially constructed to be compatible with the TU60 tape drive dynamics. Use of any other cassette will increase the data error rate and decrease the tape and transport longevity.

Table 1-1
Performance Specifications

Characteristic	Parameter
Model Designations	
TU60 AA	115 Vac, rack mounted
TU60 AB	230 Vac, rack mounted
Electrical Requirements	
Input Voltage	95 to 130 Vac @ 47–63 Hz 190 to 260 Vac @ 47–63 Hz
Input Current	1.0A
Power Dissipation	120W (409.8 Btu/hr or 103.4 Kcal/hr) max
Circuit Breaker Ratings	7A @ 115 Vac (resettable) 4A @ 230 Vac (resettable)
Power Supply	See Paragraph 4.7 for specifications
Interface Signals	
Logic Levels*	True = 0V False = +3V
Loads (TTL compatible)	Inputs: 180Ω to +5 Vdc, 390Ω to gnd Outputs: Open collector, 30 mA max sink current
Environment	
Operating Temperature	50 to 105°F (10 to 40°C)

*Except PWR OK L, Logic True = 0.9V
Logic False = open
Max Sink Current = 2 mA

Table 1-1 (Cont)
Performance Specifications

Characteristic	Parameter
Environment (Cont)	
Cassette Storage Temperature	40 to 122°F (5 to 50°C)
Operating Relative Humidity	20 to 80% (no condensation)
Altitude	0 to 10,000 ft (0 to 3048m)
Storage Medium	
Type	DEC, 100% certified, Digital Tape Cassettes
Tape Width	0.150 in. (0.381 cm)
Tape Thickness	1 mil, 0.30 mil oxide
Tape Life	Guaranteed at least 1000 end-to-end forward passes Typically 2000–6000 end-to-end forward passes
Capacity	⩾93K bytes, average rate: see Figure 1-1
Recording Density	350 to 700 bits/in. (889 to 1778 bits/cm)
Recording Method	Phase Encoding
Format	Variable block length (hardware formatted)
Drive Method	Direct (reel-to-reel)
Average Operational Speeds	
Read/Write	9.6 in./sec (3.78 cm/sec)
Search	22 in./sec (8.66 cm/sec)
Rewind	100 to 150 in./sec (39.37 to 59.05 cm/sec)
Data Transfer Rate	562 bytes/sec, average rate: see Figure 1-1
Tape Motion Times	
Start/Stop	< 20 ms read/write; < 45 ms search (linear ramp controlled)
Rewind	30 sec (max), < 20 sec typical

Table 1-1 (Cont)
Performance Specifications

Characteristic	Parameter
Bit Error Rate	
Write Errors	1 in 10^6
Read Errors	1 in 10^8 (unrecoverable) 1 in 10^7 (recoverable – 3 rereads)
Dimensions and Weight	
Width	19 in. (0.48 m)
Depth	18-1/4 in. (0.46 m)
Height	5-1/4 in. (0.13 m)
Weight	32 lb (14.06 kg)

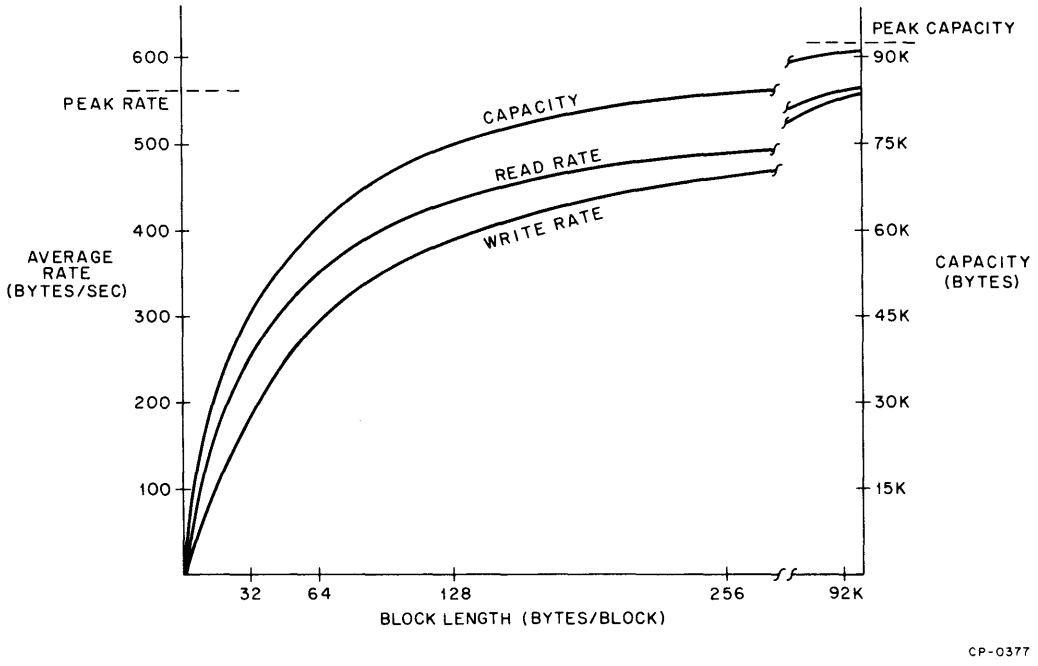


Figure 1-1 Capacity and Data Rate vs Block Length

1.4 MAJOR ASSEMBLIES

The TU60 Cassette Tape Transport is composed of the following major assemblies and systems:

- controls and indicators
- two tape drives
- two hex-sized (15.7 X 8.6 in. or 39.88 cm X 21.84 cm) logic modules
- a power supply (H751).

Figure 1-2 illustrates the locations and the subsequent paragraphs describe the functions of each of the major assemblies and systems.

1.4.1 Controls and Indicators

There are only three manual controls on the TU60. Each drive contains a separate REWIND pushbutton and a Power-On indicator. The Power ON/OFF toggle switch for the entire transport is located on the chassis rear panel. These manual controls and indicators perform the following functions:

- **REWIND** – Pressing this momentary contact pushbutton on one of the two drives, rewinds the tape on that drive, at high speed, to the Beginning-of-Tape (BOT) marker provided:

  a. a cassette is loaded

  b. tape is not moving under program control.

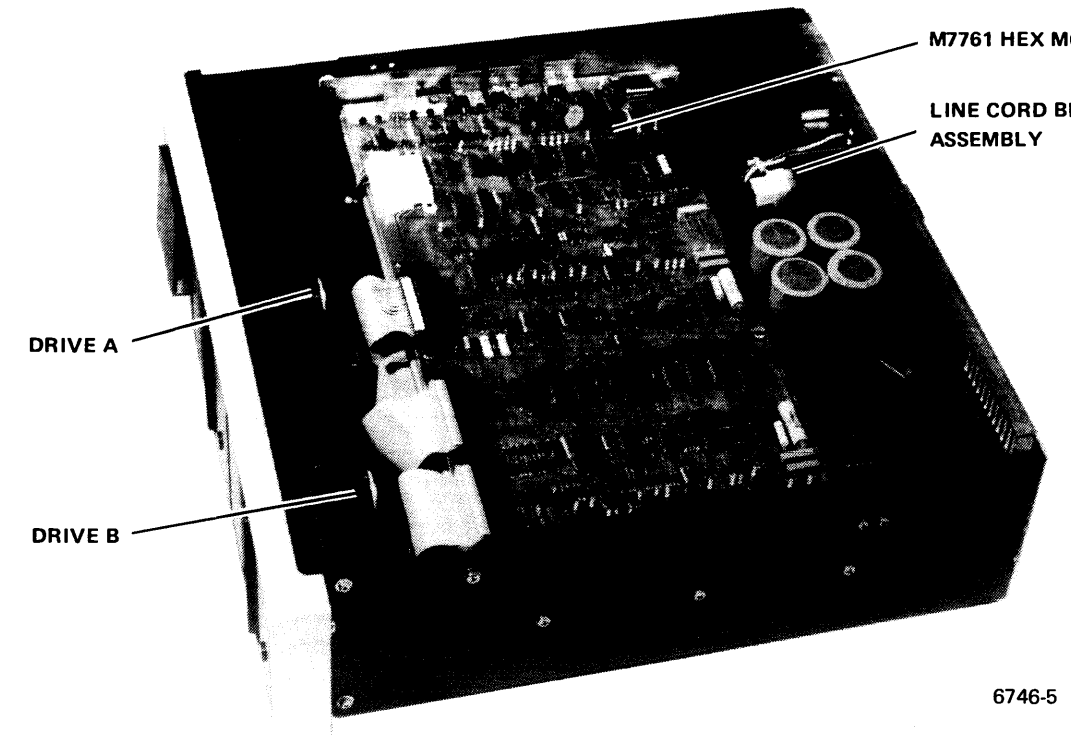
  Pressing this switch during a program controlled operation has no effect.

- **Power ON/OFF** – Placing this switch in the ON position lights both Power-On indicators (located opposite the REWIND pushbuttons on the lower door of each drive) and activates the internal dc power supply. Conversely, placing this switch in the OFF position de-activates the power supply and turns off both Power-On indicators.

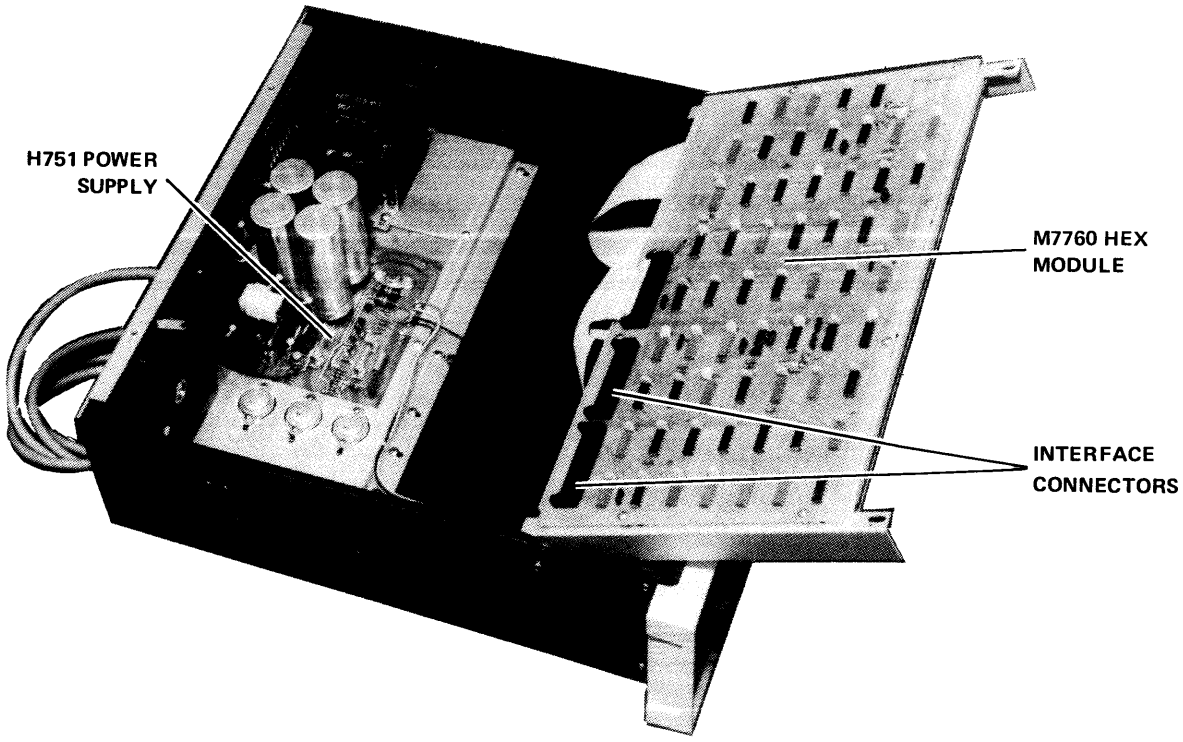
1.4.2 Drive Mechanism

Each tape drive (Figure 1-3) consists of:

- a tension motor and a servo operated control motor
- a control motor solenoid
- various interlock microswitches
- a clear leader photodetector
- two tape guides and a read/write head.

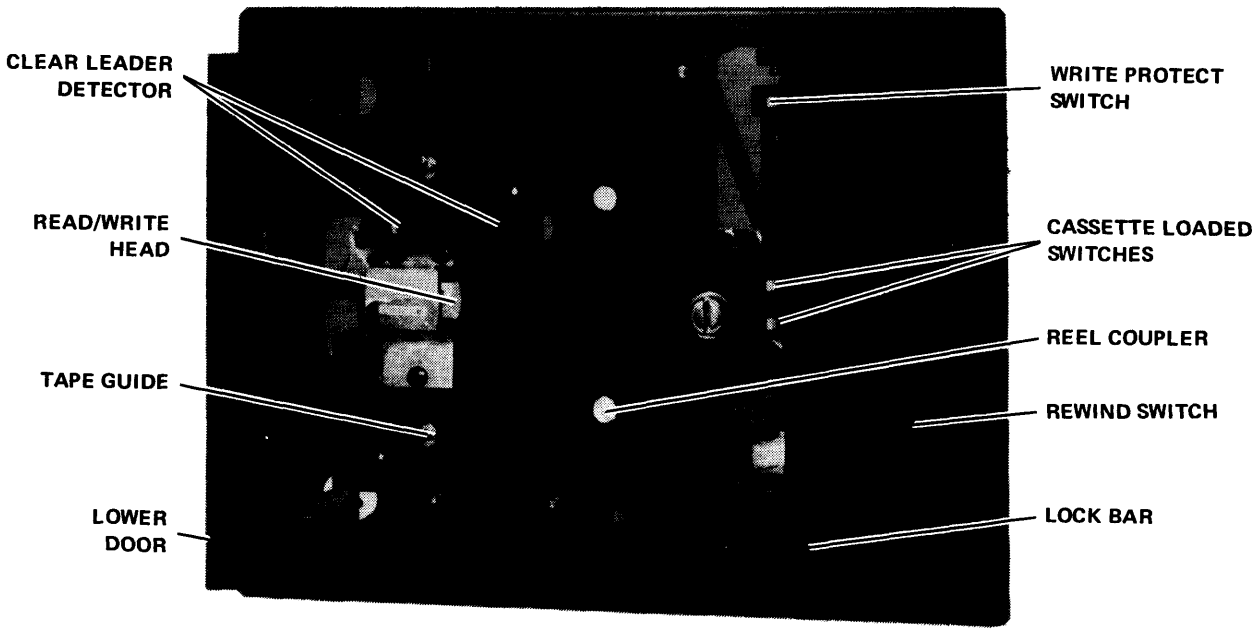


(A) Logic Modules Down

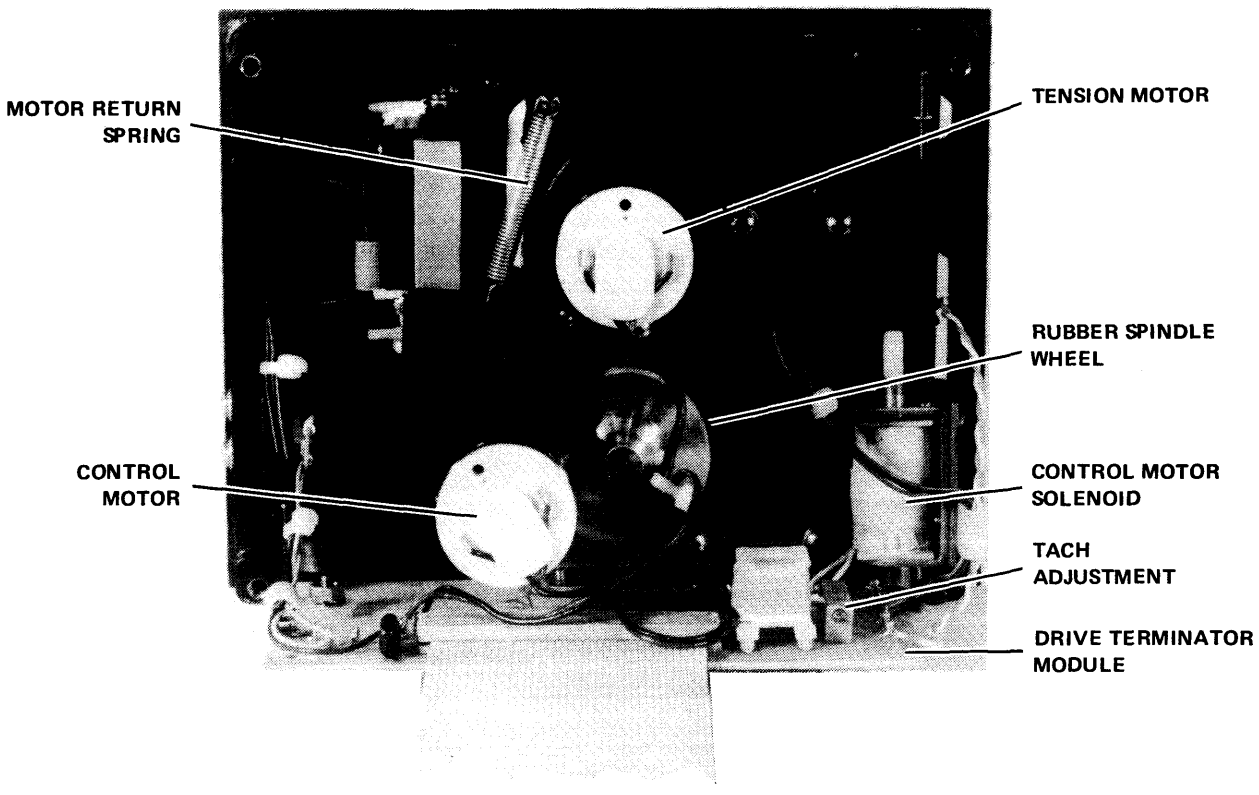


(B) Logic Modules Up

Figure 1-2 Location of Major Assemblies and Systems



(A) Drive Front View



(B) Drive Rear View

Figure 1-3 Cassette Tape Drive

If the appropriate digital cassette is properly loaded, one of the cassette loaded microswitch actuators (located on the drive lock bar) extends into a recess on the cassette, while the other switch closes against the cassette case (Figure 1-4). This switch configuration removes the unloaded interlock condition and permits tape motion upon command. Similarly, if the write protect recess on the cassette case is opened (protect tab on cassette folded back), the write protect microswitch actuator extends into this recess and inhibits write operations. When commanded, tape motion from the supply reel, over the tape guides and read/write head, and onto the take-up reel is directly controlled by the tension and control motors.

For a rewind operation (tape travel from lower to upper reel), the control motor solenoid is de-energized. This action allows the spring-loaded control motor to move away from the lower rubber sprocket wheel and thus permit the lower tape reel to turn freely. Simultaneously, the upper tension motor is turned on at constant speed to rewind the tape at rewind speed (100–150 ips) to the beginning-of-tape clear leader. Detection of the clear leader is accomplished by a photosensor (located in the drive baseplate) and a lamp which shines at an angle onto the photosensor. As tape passes between the lamp and the photosensor (Figure 1-4), light from the lamp is prevented, by the tape oxide, from reaching the photosensor. When the clear leader passes between these two elements, light from the lamp then shines through the clear leader and onto the photosensor, thus activating the sensor to stop tape motion.

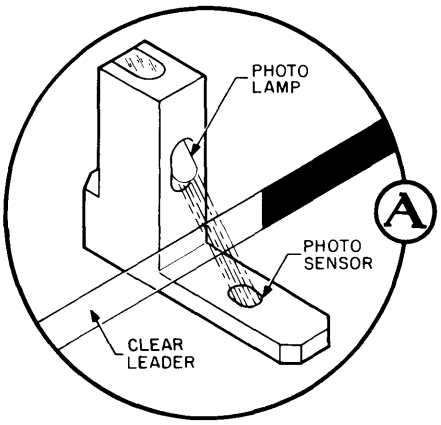
For a read, write, or search operation, the control motor solenoid remains energized, holding the control motor against the rubber sprocket wheel. During these operations, a servo system governs the velocity of this motor, to control the tape motion. For forward motion, the control motor rotates counterclockwise, while a slight reverse torque is applied to the tension motor to maintain the proper tape tension. For reverse motion, the control motor rotates clockwise, while a greater torque is applied to the tension motor to take up the tape and thus maintain the proper tape tension.

1.4.3 Logic

The M7760 and M7761 hex-sized logic modules (Figure 1-2) within the TU60 are hinged mounted to the top of the transport chassis and swing upward for easy component access during maintenance. These hex modules are interconnected by a single jumper cable and they contain all the logic and circuit components necessary to perform data formatting, error checking (CRC generation and validation), bit to byte conversion, tape motion control, and cassette housekeeping. Since most of the controller functions are performed by the logic on these modules, the associated processor contains only an interface module which is capable of translating the processor codes into commands, interpreting status flags, and storing input/output data. Each tape drive has a flat cable which plugs into the upper hex module.

1.4.4 H751 Power Supply

The H751 Power Supply, located in the rear of the TU60 chassis, furnishes +15 and -15 Vdc to a precision 12V regulator on the M7761 module. The +12 and -12 Vdc regulator output is then supplied to the sprocket motors and operational amplifiers. In addition, the H751 Power Supply furnishes a +5 Vdc precision regulated output for the logic operation. By changing the line cord breaker assembly, this power supply can operate with either 115 or 230 Vac (50/60 Hz) input line voltage. Both internal supplies are fuse protected against overcurrent and the +5 Vdc supply has a crowbar overvoltage protection circuit. (Refer to Paragraph 4.5 for a detailed description of the power supply operation.)



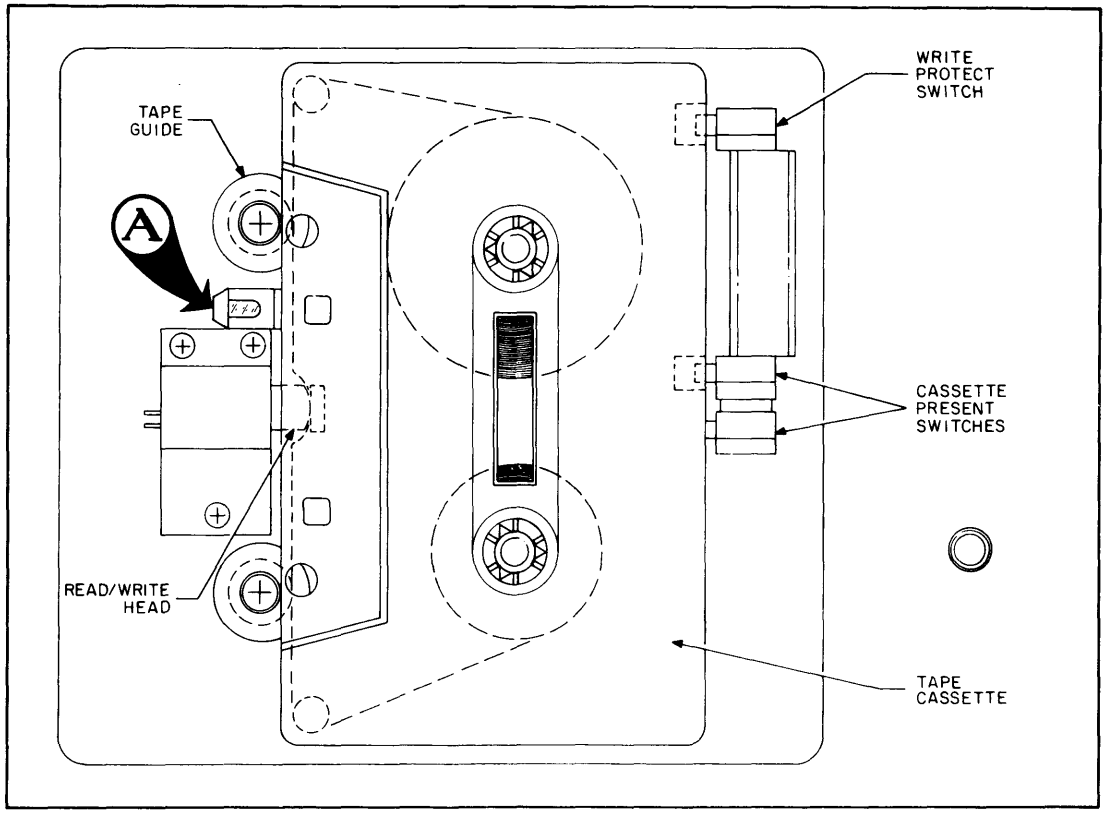


Figure 1-4 Cassette Loaded

CHAPTER 2
INSTALLATION

2.1 UNPACKING AND INSPECTION

The TU60 DECassette Tape Transport can be shipped in a rack as an integral part of a system or in a separate container. If the transport is shipped in a rack, position the rack in the final installation location and unpack it as follows:

1. Open the rear door of the rack and remove the shipping bracket. Retain the bracket for possible return shipment.

2. Slide the transport out from the rack and remove the top cover.

3. Inspect the transport and report any damage to the carrier and to Digital Equipment Corporation.

If the transport is shipped in a separate container, use care while unpacking it. Do not drop or subject the transport to unreasonable impact. Unpack the transport as follows:

1. Open the carton (Figure 2-1) and remove the foam and corrugated packing pieces.

2. Lift the transport out of the carton and remove the plastic shipping bag.

3. Remove the transport top cover and retain all packing materials for possible return shipment.

4. Inspect the transport and report any damage to the carrier and to Digital Equipment Corporation.

2.2 ELECTRICAL INSTALLATION AND CHECKOUT

1. Check the power supply line cord breaker assembly to ensure that the transport is configured properly for the input power to be used. Line cord breaker assembly BC05H is for 115 Vac operation and BC05J is for 230 Vac operation.

2. Route the interface cables through the opening beneath the fan in the rear of the transport and connect them to J1 and J2 of the M7760 module in the TU60.

3. Route the opposite end of the interface cables through the cable strain reliefs and connect them to the interface. (Refer to the appropriate interface Power Wiring and Cable Diagram for the correct cable type and processor connection.)

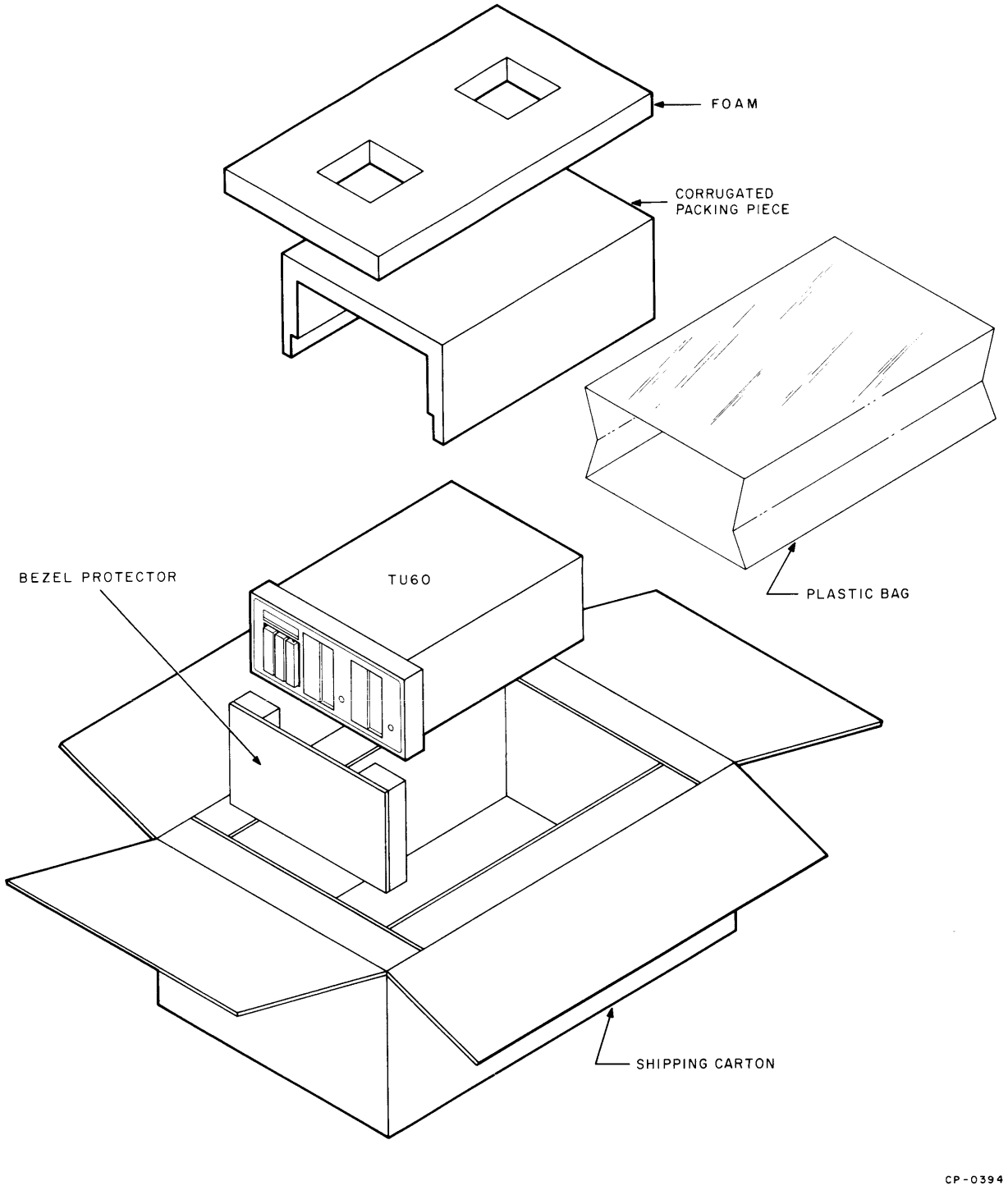


Figure 2-1 Transport Unpacking

4. Plug the power cord into the switched ac line receptacle.

5. Place the Power ON/OFF switch (located on the chassis rear panel) in the ON position and ensure that the Power-On indicators light on both drives.

6. Load a test cassette (Paragraph 2.3.1) on each drive and momentarily press both REWIND pushbuttons. Ensure that the tape completely rewinds to the BOT clear leader (about 20 seconds).

7. Momentarily press both REWIND pushbuttons again and check that the drives rewind tape for about one second.

8. Run the appropriate diagnostic tests to ensure the proper electrical and mechanical operation.

2.3 OPERATION

IMPORTANT: READ THIS PARAGRAPH PRIOR TO DRIVE OPERATION.

To obtain maximum performance and reliability from the TU60 Cassette Tape Transport, observe the following precautions and practices:

1. Before using a new cassette, or prior to using a cassette that has just been shipped or accidently dropped;

   a. Load the cassette on a drive (Paragraph 2.3.1) and perform a rewind operation.

   b. Remove the cassette, turn it over, and perform another rewind opertion.

   This is done to pack the tape neatly in the cassette and also to place the full tape reel at the proper operating tension.

2. Do not expose the cassette to excessive heat or dust. Since most tape soft errors are caused by dust or dirt, it is imperative that the tape be kept clean.

3. When not in use, store the cassettes in the plastic storage boxes or other sealed containers.

4. Always rewind the tape to the BOT leader before removing the cassette from the drive.

2.3.1 Cassette Loading and Unloading

A cassette may be loaded on the drive with the drive locking bar either opened or closed; however, it is slightly easier to load a cassette with the bar opened. It is therefore recommended that the cassette be loaded as follows, with the locking bar opened (Figure 2-2A):

1. Configure the cassette write protect tab (Figure 2-2B) for the desired operation.

NOTE

The write protect tab is located on the cassette top right, when viewed with the label side up. To inhibit a write operation, fold this tab back to open the cassette recess. To allow a write operation, return the write protect tab to close the recess hole.

2. Hold the cassette with the thumb and index finger, and insert the cassette towards the left, at approximately a 45° angle, into the drive as indicated in Figure 2-2C. Ensure that the cassette label faces outward and that the exposed cassette tape edge is to the left of the drive sprockets.

3. Apply a leftward pressure, while simultaneously rotating the cassette inward onto the drive sprockets (Figure 2-2D). This action allows the cassette tape edge to slide under the lower door (lower door opens slightly) and bottom against the tape guides and read/write head.

4. When the cassette is properly loaded, the locking bar automatically closes over the cassette back edge and the lower door closes flush with the drive frame (Figure 2-2E).

5. To remove the cassette, gently push the locking bar to the right until it detents and withdraw the cassette from the drive.

2.3.2 Normal Operating Procedure

1. Configure the cassette write protect tab for the desired operation and load the cassette (Paragraph 2.3.1).

2. Ensure that the Power-On toggle switch (located on the chassis rear panel) is in the ON position.

3. Press the manual REWIND pushbutton.

A

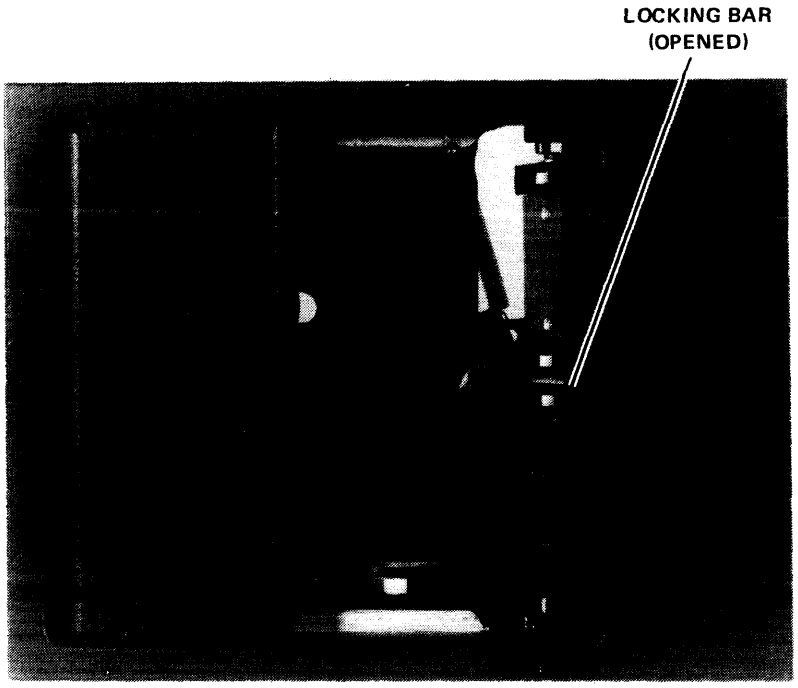
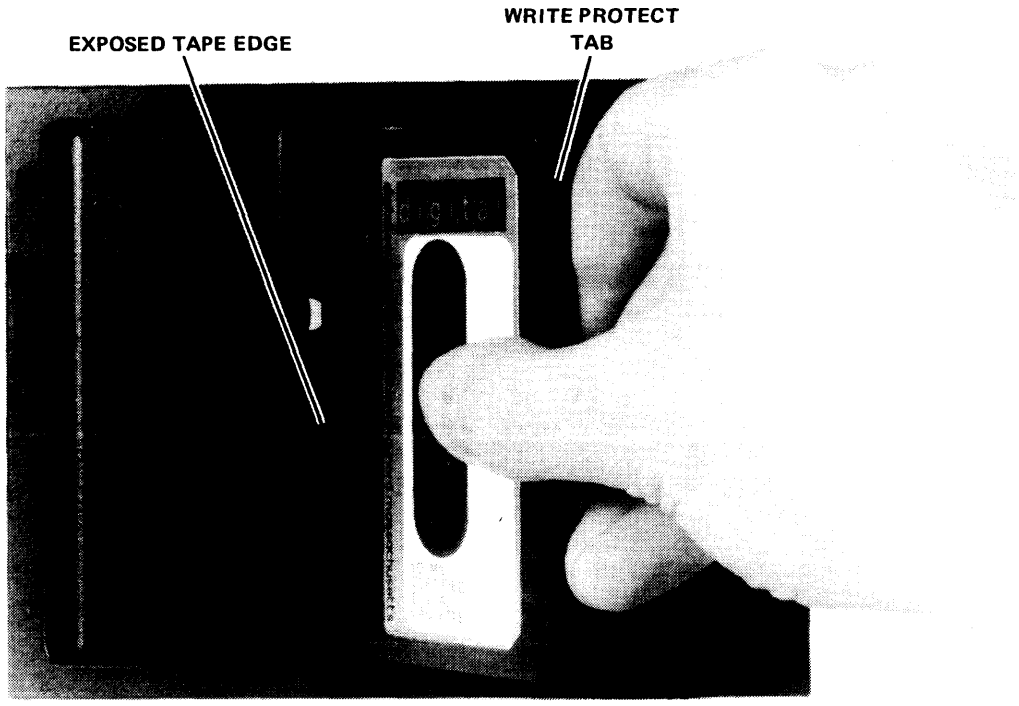


Figure 2-2 Cassette Loading Sequence

B



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C

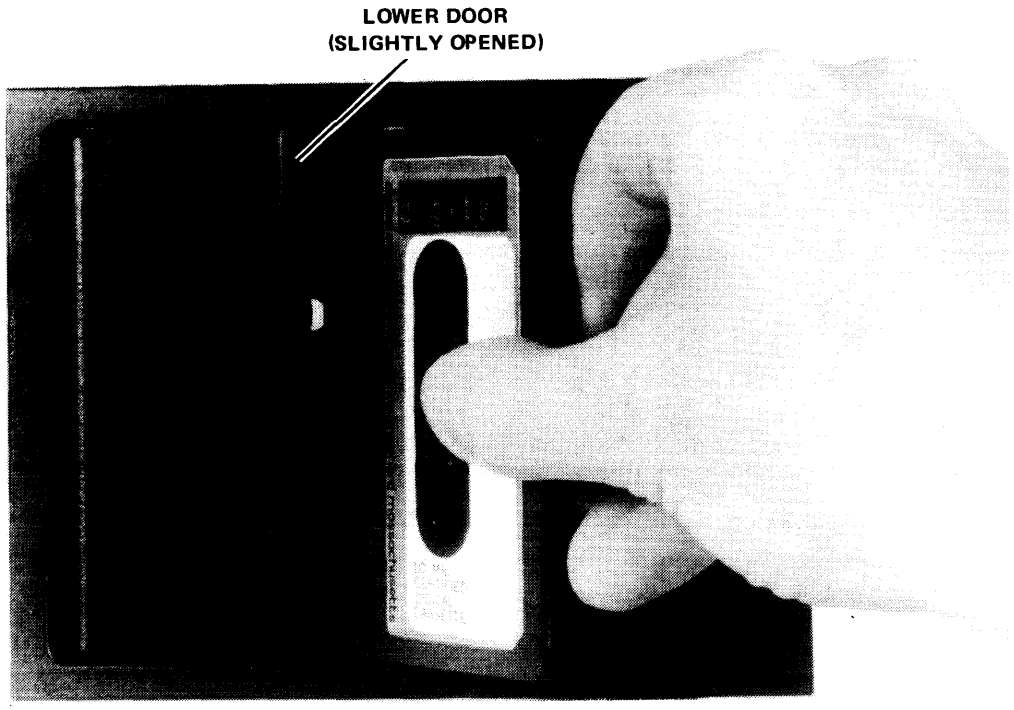

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Figure 2-2 Cassette Loading Sequence (Cont)

D

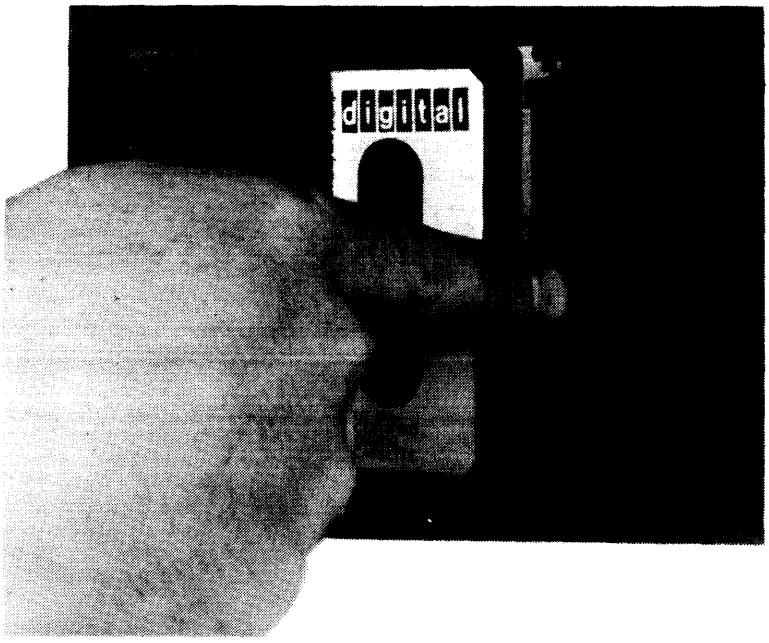

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Figure 2-2 Cassette Loading Sequence (Cont)

CHAPTER 3
I/O INTERFACE SIGNALS

The TU60 DECassette Tape Transport interface is unique in that the transport does not utilize a separate controller. All the logic and circuit components necessary for data formatting, error checking, and cassette housekeeping are contained on two logic modules within the transport chassis; while the associated processor contains an interface module that converts the processor codes into commands and transmits them to the TU60. In addition, the interface module is capable of interpreting status flags received from the TU60, as well as temporary storage of input/output data.

There are several interface signals that must be present at the TU60 during an entire operation. These signals are SELECT ENABLE L, DRIVE B L, BACK BLOCK GAP L, BACK FILE GAP L, and R/W FILE GAP. The REWIND L, R/W CRC L, TRANSFER L, and WRITE MODE L signals, however, are transmitted and then stored in the TU60. All interface signals are at ground (low) for a logical 1 and +3V (high) for a logical 0. The following paragraphs describe the functional operation of each interface signal.

3.1 INPUT INTERFACE SIGNALS

3.1.1 Select Enable L

This signal, at a logical 1, enables the TU60 input/output transmitters and receivers.

3.1.2 Drive B L

This signal selects one of the dual tape drives. A logical 1 selects drive B or a logical 0 selects drive A.

3.1.3 Start L

This signal, at a logical 1, is used in conjunction with a specific command to initiate command execution. If a command is to be performed, the drive must be in the ready state (READY L present) and the command present and stable one microsecond prior to START L. If this is the case, when START L is received, the TU60 electronics removes the READY L signal and initiates command execution. When READY L is removed, the interface then removes START L and while the command is being executed, any additional START L signals are ignored by the drive.

3.1.4 Rewind L

This motion command signal, at a logical 1, is clocked by the START L signal to trigger the Rewind one-shot and thus cause a high speed (100–150 ips) tape rewind on the selected drive, to the beginning of the tape.

3.1.5 Back Block Gap L

This motion command signal, at a logical 1, is clocked by the START L signal to cause reverse tape motion at read/write speed across a data block to the preceding pre gap.

3.1.6 Back File Gap L

This motion command signal, at a logical 1, is clocked by the START L signal to cause reverse tape motion at search speed across a data file, stopping at two-thirds of the preceding file gap.

3.1.7 R/W File Gap L

This signal, at a logical 1, is used in conjunction with the WRITE MODE L signal to initiate either forward tape motion or a write file gap operation. If WRITE MODE L is a logical 1 when this signal is clocked by the START L signal, 535 ms of tape is erased; 1.4 seconds of tape is erased if at BOT. If WRITE MODE L is a logical 0 when this signal is clocked, tape on the selected drive moves forward, stopping two thirds into the next file gap.

3.1.8 Write Mode L

This signal selects either the read or write logic. For a write or write file gap operation, this signal, at a logical 1, is clocked by the START L signal to set the Write flip-flop.

For a read operation, this signal, at a logical 0, allows the START L signal to reset the Write flip-flop. Once the specific operation is initiated, the Write flip-flop remains either set or reset until the next operation is started.

3.1.9 Transfer L

During a write operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. If this is the case, TRANSFER L sets the Trans Req flip-flop and the 8-bit byte is loaded into the TU60 Data Buffer.

During a read operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. If this is the case, TRANSFER L sets the Trans Req flip-flop to indicate that the 8-bit byte has been loaded into the Interface Buffer.

3.1.10 R/W CRC L

During a write operation, this signal, at a logical 1, causes the accumulated CRC character to be recorded on the tape. R/W CRC L is transmitted to the TU60 while the final data byte is being recorded. When this occurs, the next TRANSFER REQ L signal is inhibited and the CRC character is recorded after the final data bit is written.

During a read operation, this signal, at a logical 1, tests the CRC Register for an error. At the start of a read operation, the CRC Err flip-flop is set and remains set while the data block is being read. After the first 8 CRC bits have been read, the interface transmits R/W CRC L. When the final TRANSFER REQ L signal is generated, the CRC Register is checked for zero. If the register is not zero (data read incorrectly), the CRC Err flip-flop remains set and, when READY L is generated, a CRC ERROR L signal is also generated. If the data has been read correctly, the CRC Err flip-flop resets and a CRC ERROR L signal is not generated.

3.1.11 Initialize L

This signal, at a logical 1, removes all flags (except EOT), generates READY L and, except for a rewind operation, stops tape motion regardless of the tape position.

3.2 OUTPUT INTERFACE SIGNALS

3.2.1 Off Line L

This signal, at a logical 1, indicates that the appropriate tape cassette is not properly loaded on the selected drive; or that the clear leader sensing lamp has failed.

3.2.2 Ready L

This signal, at a logical 1, indicates that the appropriate tape cassette has been properly loaded and tape motion is not occurring on the selected drive. In general, READY L is generated when all command functions have been completed and the drive is ready for the next operation; or when a clear leader is encountered.

3.2.3 End File L

This signal, at a logical 1, indicates that a file gap has been detected or the ensuing tape is blank.

3.2.4 EOT/BOT L (End Tape)

This signal, at a logical 1, indicates that the drive has reached the end-of-tape or beginning-of-tape (clear leader photosensor uncovered). When this occurs, tape motion stops and the READY L and EOT/BOT L signals are generated. EOT/BOT L is suppressed during a rewind operation or if the drive is not in the ready state.

3.2.5 Rewind L

This signal, at a logical 1, indicates that the selected drive is performing a rewind operation.

3.2.6 Write Protect L

This signal, at a logical 1, indicates that a write protected cassette is loaded on the selected drive, or that the drive is empty. If the cassette is write protected, the selected drive will not perform any write operations.

3.2.7 Write Status L

This signal, at a logical 1, indicates that a write or write file gap operation is being performed on the selected drive.

3.2.8 Transfer Req L

During a write operation, this signal, at a logical 1, indicates that the drive is ready to receive an 8-bit byte from the Interface Buffer. The TRANSFER REQ L signal is generated one bit time before a byte is needed and this signal is removed when the interface responds with a TRANSFER L signal.

During a read operation, this signal, at a logical 1, indicates that a byte from the drive is ready to be transferred to the Interface Buffer. The interface must then respond with a TRANSFER L signal, within one bit time ($\approx$220 μs) after the TRANSFER REQ L signal is generated or a time error occurs.

3.2.9 Time Error L

This signal, at a logical 1, indicates that the interface has not responded to a TRANSFER REQ L signal within the allotted time ($\approx$220 μs).

NOTE

The processor interface contains a one byte Data Buffer which allows the program the full byte time (1.8 ms) to respond to the TRANSFER REQ L.

3.2.10 CRC Error L

This signal, at a logical 1, indicates that a CRC error has occurred during a read operation. At the start of the read operation, the CRC Err flip-flop is set. When the final CRC character is read, the CRC Register is then checked for zero. If the register is not zero, the CRC Err flip-flop remains set and when READY L is generated, a CRC ERROR L signal is also generated.

3.2.11 PWR OK L

This signal, at a logical 1, indicates that the +5V power supply is operating normally.

3.2.12 R/W Bits 1–8 (Bi-directional)

These eight lines transmit data to and from the TU60 Data Buffer.

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

Since the TU60 DECassette Tape Transport is a dual system, each drive has identical and separate motor control and servo logic. However, the selection, formatting, and read/write logic is common to both drives. It is therefore not possible to read or write from both drives simultaneously, but it is possible to perform a read or write operation on the selected drive and rewind the other drive concurrently.

Figure A-1 illustrates the major functional areas and associated signals of the TU60 Tape Transport, while this chapter only describes (in two distinct levels of detail) the logical operation of drive A. Once selected, drive B operates in an identical manner as drive A and is therefore not described. Paragraphs 4.2 and 4.3 briefly describe the over-all function of each operation that drive A can perform and Paragraph 4.5 describes these same operations in detail. Since the descriptions in Paragraph 4.5 refer to key elements and signals on the logic drawings in Appendix A, it is imperative that these drawings be used in conjunction with the text for a comprehensive understanding of each operation.

4.2 TAPE FORMAT AND MOTION CONTROL OPERATIONS

Figure 4-1 illustrates a typical TU60 data tape. The following paragraphs explain a specific command or manual control operation relative to the tape format. Before a command can be executed, however, one of the dual drives must first be selected and ready. (Refer to Paragraph 4.5.1 for a detailed description of the drive selection process.)

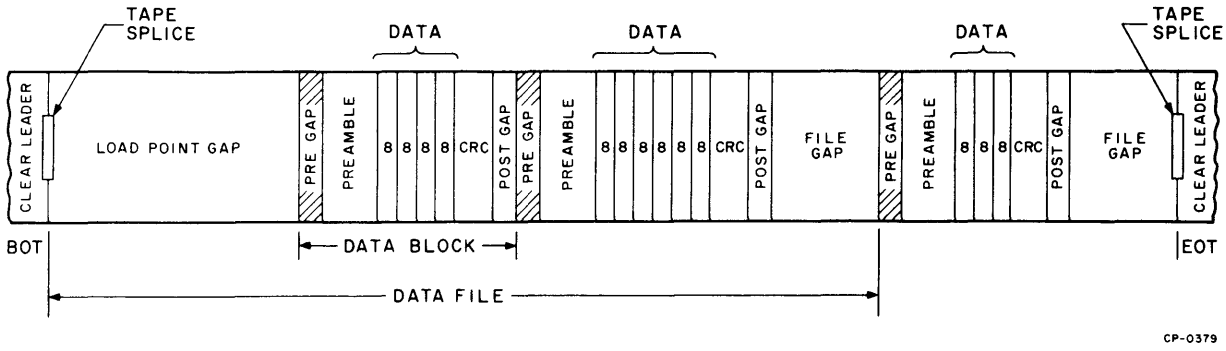


Figure 4-1 Typical Tape Format

4.2.1 Manual Rewind

To perform a manual rewind operation, the following conditions must be true:

a. the appropriate cassette is properly loaded

b. tape is not moving under program control.

Pressing the REWIND pushbutton when the preceding conditions are true sets the Rewind one-shot. If the tape is not at the beginning-of-tape (BOT) clear leader, the Rewind one-shot is held set even though the switch is released, allowing the tape to rewind completely at high speed (100–150 ips) to the BOT clear leader. If the tape is at the BOT clear leader when the REWIND pushbutton is pressed, the Rewind one-shot is set but is not held set and it times out one second later. Thus when the tape is at the BOT clear leader, backward tape motion occurs for less than one second.

Figure 4-2 illustrates the logical sequence during a manual rewind operation. Refer to Paragraph 4.5.2.1 for a detailed logic description of the preceding events.

4.2.2 Programmed Rewind

To perform a program controlled rewind operation, the interface issues a Rewind command. If the appropriate cassette has been properly loaded and the tape is not already in motion, then the READY L interface signal is present at the interface. With READY L present, the interface then transmits the program generated START L signal, which clocks the Rewind command to set the Rewind one-shot. The remainder of the program controlled rewind operation is the same as a manual rewind operation.

Figure 4-2 illustrates the logical sequence during a program controlled rewind operation. Refer to Paragraph 4.5.2.2 for a detailed logic description of the preceding events.

4.2.3 Back Block Gap

To space the tape backward one block (Figure 4-6), the interface issues a Back Block Gap (BBG) command. If the appropriate cassette has been properly loaded and the tape is not already in motion, then the READY L interface signal is present at the interface. With READY L present, the interface then transmits the program generated START L signal. If the tape is at the beginning-of-tape (BOT) clear leader, the signal INHIBIT H prevents reverse tape motion from occurring. If the tape is not at the BOT leader, reverse tape motion at read/write speed (9 ips average) occurs across an entire data block. When the tape is positioned at the preceding pre gap, the READY L interface signal is again generated and tape motion ramps to a stop.

Figure 4-3 illustrates the logical sequence during a back block operation. Refer to Paragraph 4.5.3 for a detailed logic description of the preceding events.

4.2.4 Back File Gap

A back file gap (BFG) operation is similar to the back block operation except that tape motion at search speed (22 ips average) occurs across a data file (Figure 4-6), stopping at two-thirds of the preceding file gap.

Figure 4-3 illustrates the logical sequence during a back file operation. Refer to Paragraph 4.5.4 for a detailed logic description of the preceding events.

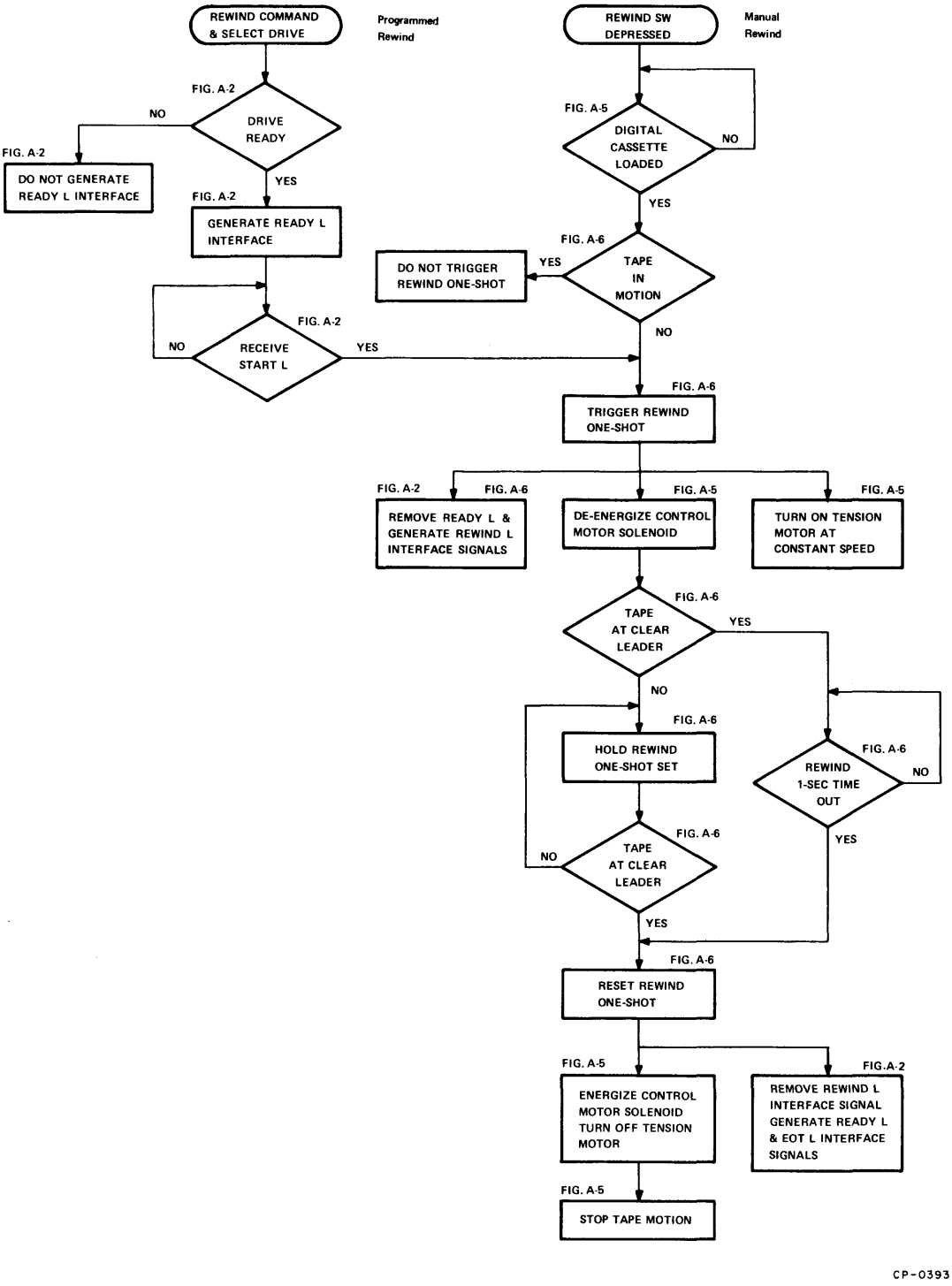


Figure 4-2 Rewind Flow Chart

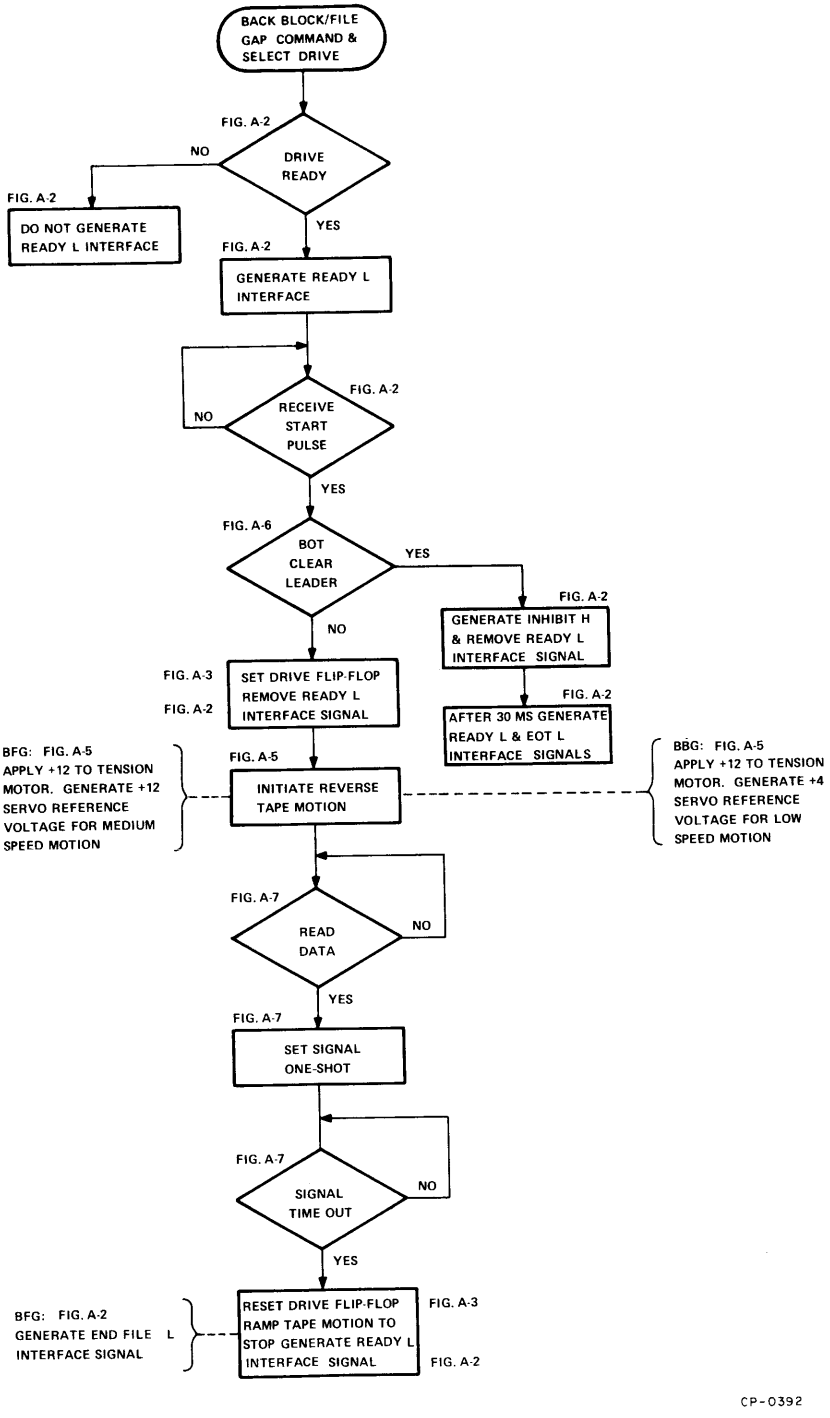


Figure 4-3 Back Block/File Gap Flow Chart

4.2.5 Forward File Gap

A forward file gap (FFG) operation differs from the other motion control operations in that forward tape motion starts at read/write speed (9 ips average), then switches to search speed (22 ips average) if data is detected before a file gap.

If the tape is at the BOT when this command is issued (Figure 4-6), forward tape motion occurs at read/write speed across the load point gap, then switches to search speed when the first data block is detected. Tape motion continues at search speed, stopping at two-thirds of the following file gap. If the tape is stopped in the post gap prior to a file gap when this command is issued, forward tape motion occurs at read/write speed for 385 milliseconds, then tape motion stops at two-thirds of the same file gap. If tape is stopped at two-thirds of the file gap or at a block gap when this command is issued, forward tape motion starts at read/write speed, but switches to search speed when data is detected. When this occurs, the tape continues to move at search speed across the entire data file, stopping at two-thirds of the following file gap. Refer to Paragraph 4.5.6 for a detailed logic description of the preceding events.

4.3 READ/WRITE OPERATIONS

4.3.1 Write File Gap

For certain specific programming operations, it may be advantageous to group consecutive data blocks together as a unit. This is accomplished by generating relatively long portions of erased tape (file gaps) before and after the data block group (Figure 4-1). Except for the available tape length, there is no limit to the number of files that may be contained on a single cassette.

To write a file gap, the interface simultaneously selects drive A (Paragraph 4.5.1), issues a Read/Write Gap command, and transmits the WRITE MODE L interface signal. If the cassette is write enabled and the drive is in the ready state, READY L is present at the interface. With READY L present, the interface then transmits the program generated START L signal to initiate forward tape motion at read/write speed (9 ips average). As the tape moves across the read/write head, the drive write circuits erase tape for 535 milliseconds. However, if the tape is at BOT when this command is issued, a 1.4 second load point gap is erased. Refer to Paragraph 4.5.7 for a detailed logic description of the preceding events.

NOTE

It is possible to perform concurrent write file gap operations; however, during forward file gap operations, two consecutive file gaps cause unspecified transport operation (may read as either 2 or 3 file gaps).

4.3.2 Write Data Block

To write a block of data (Figure 4-4), the interface simultaneously selects drive A and issues a Write command. If the drive is in the ready state, READY L is present at the interface. With READY L present, the interface then transmits the program generated START L signal to initiate forward tape motion at read/write speed (9 ips average). As the tape moves across the read/write head, the write circuits erase a 40 millisecond pre gap prior to automatically recording the preamble (thirty-two logical 0s and one logical 1).

At approximately two-thirds of the preamble write time, the drive logic issues a Transfer Request signal which allows the interface to parallel transfer the first 8-bit byte into the Data Buffer, where it is stored until after the last preamble bit is written. When the last preamble bit is written, the first data bit is serially shifted out of the Data Buffer, phase encoded, and then written onto the tape. The remaining data bits are likewise shifted, phase encoded, and placed on the tape. Simultaneously, the data bits are also applied to a 16-bit Cyclic Redundancy Check (CRC) Register, where they are accumulated into a CRC character (Paragraph 4.5.10). When the eighth bit of the data byte is written, another Transfer Request is issued and the second 8-bit data byte is parallel transferred from the interface, temporarily stored in the Data Buffer, and then shifted out onto the tape.

This process continues until all the data bytes have been transferred, at which time, the interface issues a Write CRC command. When the last data bit is written on the tape, the 16-bit CRC character is then shifted from the CRC Register, phase encoded, and written on the tape. At the completion of the CRC write operation, a 30-millisecond post gap is erased and tape motion ramps to a stop. Fifteen milliseconds after the tape has completely stopped, READY L is again generated. (Refer to Paragraph 4.5.8 for a detailed logic description of the preceding events.)

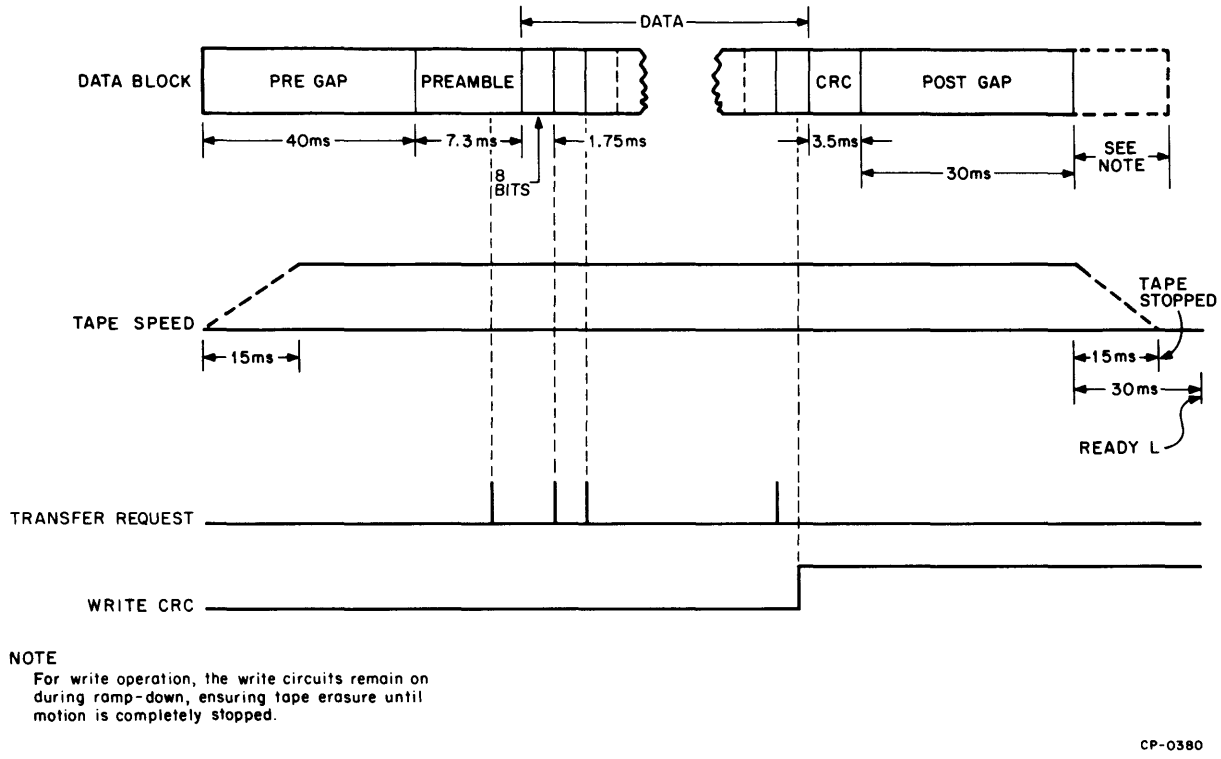


Figure 4-4 Write Data Block

4.3.3 Read Data Block/File

To read a block of data (Figure 4-4), the interface selects drive A and negates the WRITE MODE L signal. If the drive is in the ready state, READY L is present at the interface. With READY L present, the interface then transmits the program generated START L signal to initiate forward tape motion at read/write speed (9 ips average).

As the tape moves across the read/write head, preamble bits are detected. Approximately the first 24 preamble bits synchronize the read clock with the preamble bit frequency from the tape. Detection of the preamble frame bit (only logical 1 bit of the preamble) configures the drive logic to the data mode and allows the succeeding data bits to be serially shifted into the Data Buffer and also to be manipulated in the CRC Register (Paragraph 4.5.10). As the eighth bit of the first data byte is shifted into the Data Buffer, a Transfer Request signal is transmitted to the interface. The interface then stores the data byte from the eight interface lines in the Interface Buffer and responds with a Transfer signal. The second data byte is then likewise serially shifted into the Data Buffer and parallel transferred to the interface.

This process continues until all the data bytes plus the first eight bits of the CRC character have been transferred. At this time, the interface issues a Read CRC command. This command is stored in the drive logic and when the final CRC bit (16th CRC bit) is shifted into the Data Buffer, the CRC Register is tested for zero. The result of the CRC test is stored in the drive logic until the tape moves into the post gap. If the CRC Register was not zero when checked, the CRC ERROR L and READY L interface signals are generated and tape motion ramps to a stop. (Refer to Paragaph 4.5.9 for a detailed logic description of the preceding events.)

To read a data file, the interface simply selects drive A and transmits a program generated START L signal in response to every READY L signal received. If a file gap is detected while tape is being read, the END FILE L interface signal is also generated. Thus, a data file is read by successive read data block operations.

4.4 PROGRAMMING RESTRICTIONS AND COMMAND TOPOLOGY

Although all data block formatting, error checking, and cassette housekeeping are hardware controlled within the TU60, tape formatting is software controlled. For this reason, certain command sequences are illegal and if attempted, these sequences will produce error conditions or unreadable tape. Figure 4-5 illustrates some of the illegal command sequences and the resultant tape motion. The complete list of illegal sequences is as follows:

- Write then FFG or Read
- Rewind then Write
- WFG then Read or FFG
- FFG then Write
- BBG then rewrite the same block more than 3 times
- BFG then Write
- Read into file gap then Write

In addition, commands that attempt reverse motion at the BOT or forward motion at the EOT do not initiate tape motion; however, thirty milliseconds after the commands are issued, READY L and EOT/BOT L are generated. If the cassette has just been loaded and a BBG or BFG is attempted, the TU60 does not respond and the command hangs up. To properly recover from this error condition, Initialize the processor, then perform a rewind.

Figure 4-6 illustrates the normal command operation.

NOTE

Since the tape motion commands are not symmetrical and the tape velocity varies slightly from transport to transport, these commands should not be used in an attempt to replace an individual data block (other than the last block on the tape).

4.5 DETAILED LOGIC DESCRIPTIONS

The following paragraphs describe the detailed logical operation of drive A. Once selected, drive B operates in an identical manner as drive A and is therefore not described. Since the logical descriptions in these paragraphs are rather complex, it is suggested that the reader become familiar with the specific operation by referring to the simplified descriptions in Paragraphs 4.2 and 4.3 prior to reading these detailed descriptions.

4.5.1 Drive Selection

To perform any program controlled operation, a particular drive must first be selected. To accomplish this, the interface generates the SELECT ENABLE L and DRIVE B L (high for drive A, low for drive B selection) interface signals.

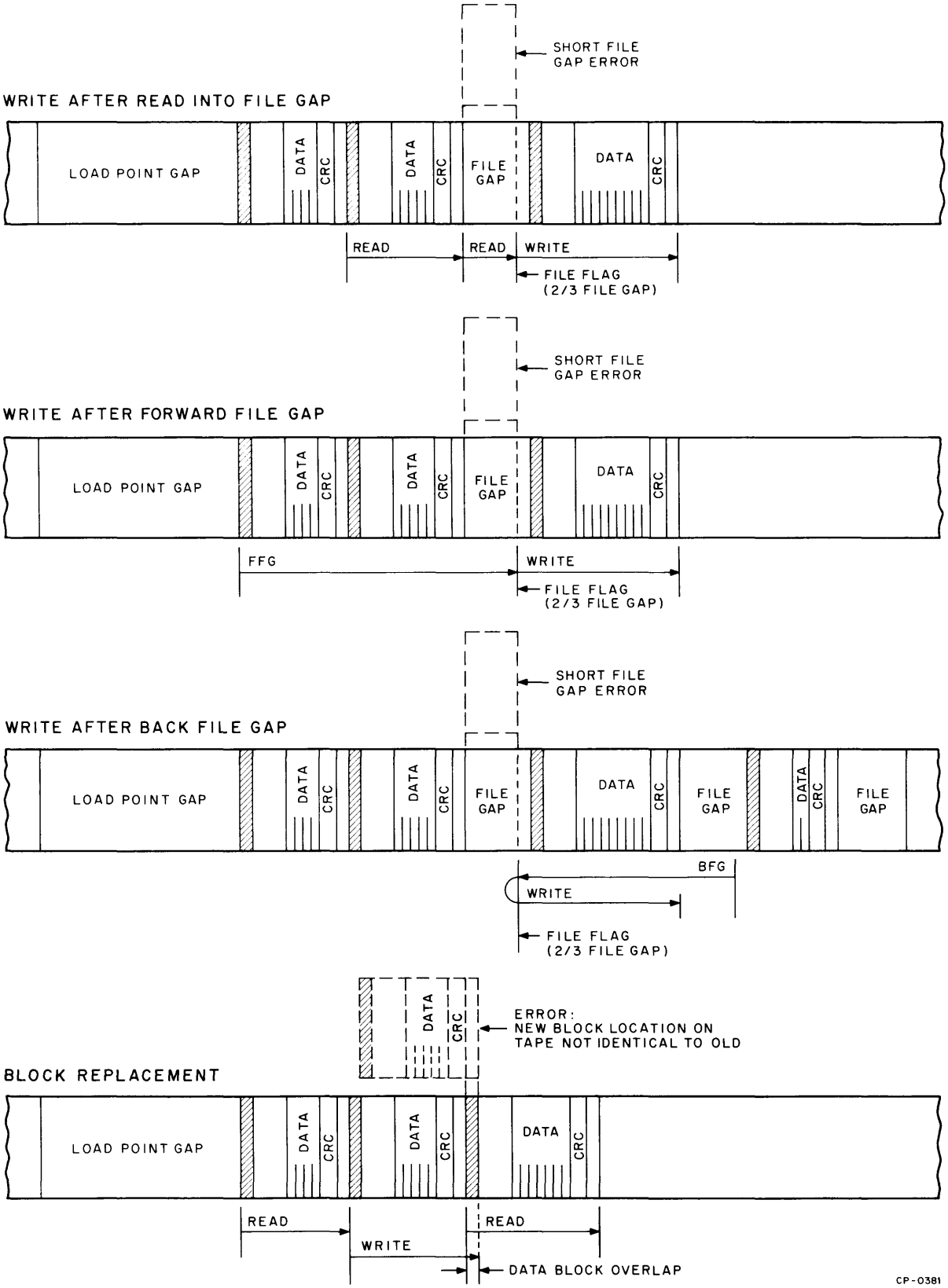


Figure 4-5 Illegal Command Sequence

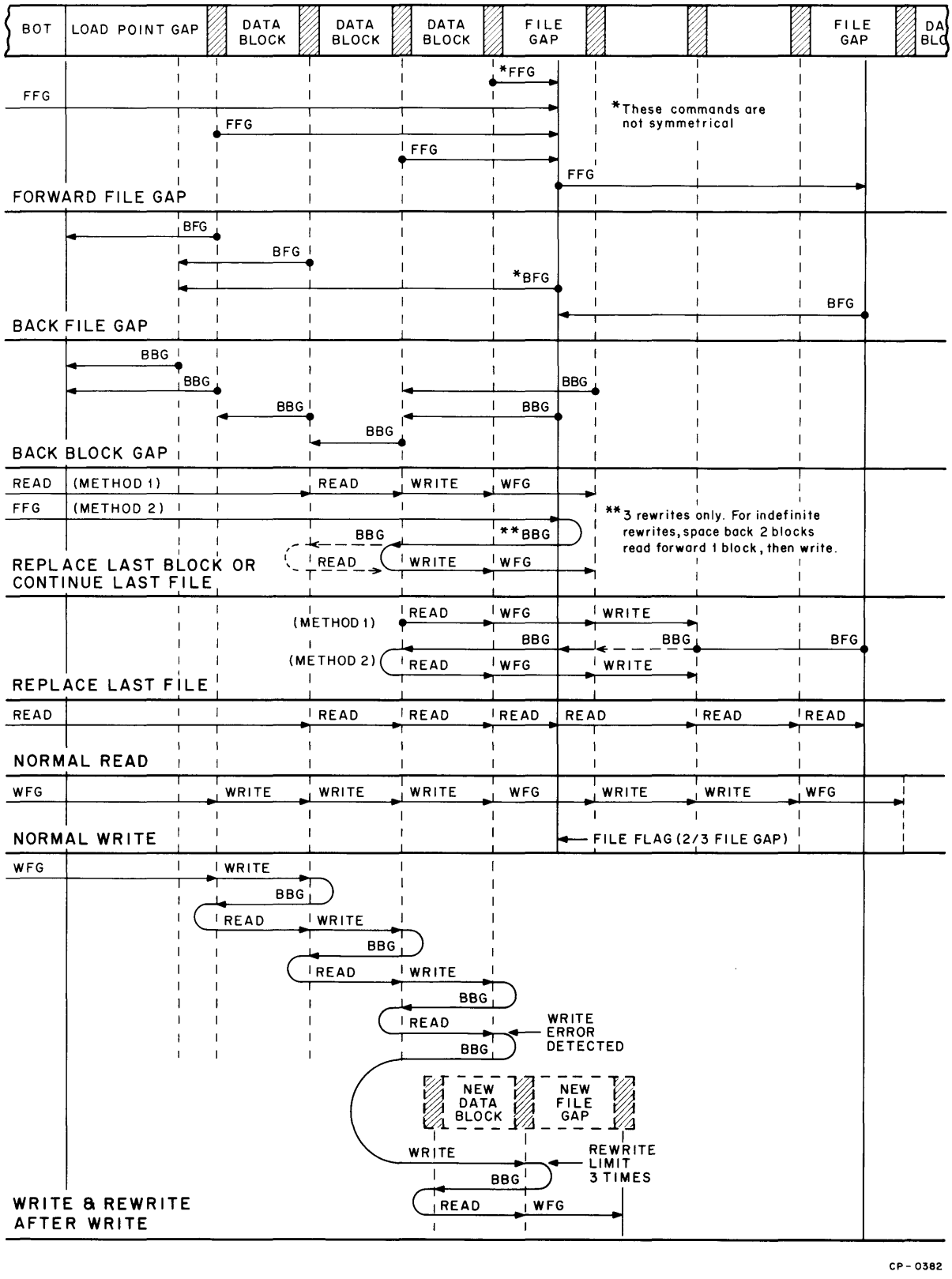


Figure 4-6 Command Topology

SELECT ENABLE L, applied to the transport interface logic (Figure A-2), enables one leg of all but the CRC and EOT/BOT output line transmitters. In addition, SELECT ENABLE L, applied through an inverter, enables one leg of all but the GO and INIT input line receivers. DRIVE B L (high), when applied to the interface logic, produces the signal DRIVE A L which, when applied to the read/write and servo logic (Figure A-7), produces the signal SEL A H/SEL B L. This internal control signal allows drive A to perform the various control and read/write operations.

4.5.2 Rewind

A rewind operation can be performed manually or under program control. The following paragraphs describe both rewind methods.

4.5.2.1 Manual Rewind – Pressing the REWIND pushbutton on the drive front panel generates the signal MANUAL REWIND A H (Figure A-6). If the appropriate tape cassette has been properly loaded, the CAS LOAD A switches (Figure A-5) are configured as shown to produce the signal LOADED A H. (Refer to Paragraph 1.4.2 for a description of the CAS LOAD microswitch operation.) LOADED A H, ANDed with REWIND A L (high if the drive is not already performing a rewind operation), produces the signal READY A L. If the tape is not in motion under program control, MOVE A H (Figure A-6) is low. This signal, applied through an inverter, is ANDed with MANUAL REWIND A H to trigger the 1-second Rewind one-shot.

With the Rewind one-shot set, REWIND A H, applied through the write protect switch, produces the signal WRITE PERMIT H (low). This signal, when applied to the read/write logic (Figure A-7), produces WRITE ENABLE H (low) to disable the write drivers and prevent a tape erasure during the rewind operation. REWIND A L, applied through a NAND gate (Figure A-6), is then ANDed with LDR A L (high if the tape is not at clear leader) to hold the one-shot set even though the switch is no longer depressed. In addition, REWIND A L, applied to the read/write and servo logic (Figure A-5), causes READY A L to come high and de-energize the Control Motor Solenoid (SOL A). This action allows the solenoid spring to move the control motor away from the rubber wheel and thus permit the cassette lower reel to turn freely. Simultaneously, REWIND A H, ANDed with LOADED A H, turns on the tension motor at constant speed (Paragraph 4.6.2) to rewind the tape.

When the tape is completely rewound, the clear leader at the beginning of the tape uncovers the clear leader photosensor. This action generates the signal LEADER A H (Figure A-6) to reset the Rewind one-shot. When the Rewind one-shot resets, REWIND A H is removed from the read/write and servo logic (Figure A-5) stopping the tension motor; while READY A L energizes SOL A. Due to the motor speed and inertia, clear leader is wound past the corner roller of the cassette before the solenoid is engaged to completely stop the tape motion.

Pressing the REWIND pushbutton while the tape is at a clear leader triggers the Rewind one-shot to produce tape motion as previously described; however, since the tape is at a clear leader, LDR A L (Figure A-6) is low. If REWIND is pressed when the tape is at the BOT clear leader, tape moves backward until the 1-second Rewind one-shot times out then tape motion stops. If REWIND is pressed when the tape is at the EOT clear leader, tape moves backward; however, before the Rewind one-shot times out, the tape oxide has moved to cover the clear leader photosensor causing LDR A L to come high and hold the Rewind one-shot set. Hence, backward tape motion continues until the BOT clear leader is detected.

4.5.2.2 Programmed Rewind – To initiate a program controlled rewind operation, the interface simultaneously selects drive A (Paragraph 4.5.1) and issues a Rewind command. REWIND CMD L applied through the transport interface logic (Figure A-2) enables the bottom leg of the set gate on the Rewind flip-flop (Figure A-6). If the appropriate tape cassette has been properly loaded, the CAS LOAD A switches (Figure A-5) are configured as shown to produce the signal LOADED A H. (Refer to Paragraph 1.4.2 for a description of the CAS LOAD microswitch operation.) LOADED A H, ANDed with SEL A H (Figure A-6), generates the signal DRIVE EMPTY H (low) which removes the OFF LINE L interface signal (Figure A-2). If the tape is not already performing a rewind operation, REWIND H is low (Figure A-6) and DRIVE L is high (Figure A-2), producing the READY L interface signal.

At this point, the interface transmits the program generated START L signal, which ANDs with READY L (Figure A-2) to produce GO H. GO H, ANDed with REWIND CMD H (Figure A-6), triggers the 1-second Rewind one-shot. With the Rewind one-shot set, REWIND A H, applied through the write protect switch, produces the signal WRITE PERMIT H (low). This signal, when applied to the read/write logic (Figure A-7), produces WRITE ENABLE H (low) to disable the write drivers and prevent tape erasure during the rewind operation. REWIND A L, applied through a NAND gate (Figure A-6), is then ANDed with LDR A L (high if the tape is not at clear leader) to hold the one-shot set even though the command terminates. In addition, REWIND A L, applied to the read/write and servo logic (Figure A-5), causes READY A L to come high and de-energize the Control Motor Solenoid (SOL A). This action allows the solenoid spring to move the control motor away from the rubber wheel and thus permit the cassette lower reel to turn freely. Simultaneously, REWIND A H, ANDed with LOADED A H, turns on the tension motor at constant speed (Paragraph 4.6.2) to rewind the tape. While the tape is rewinding, REWIND H is applied to the transport interface logic (Figure A-2) to remove the READY L and generate the REWIND L interface signals.

When the tape is completely rewound, the clear leader at the beginning of the tape uncovers the clear leader photosensor. This action generates the signal LEADER A H (Figure A-6) to reset the Rewind one-shot. When the Rewind one-shot resets, REWIND A H is removed from the read/write and servo logic (Figure A-5) stopping the tension motor; whhle READY A L energizes SOL A. Due to the motor speed and inertia, clear leader is wound past the corner roller of the cassette before the solenoid is engaged to completely stop the tape motion.

4.5.3 Back Block Gap

To space the tape backward one block, the interface simultaneously selects drive A (Paragraph 4.5.1) and issues a Back Block Gap command. BACK BLOCK GAP L, applied through the transport interface logic (Figure A-2), produces the signal REV L. REV L is then applied through an inverter (Figure A-5) to enable the top leg of the drag motor control gate, and the bottom leg of the servo input gate. If the tape is not in motion, the Drive flip-flop (Figure A-3) is in the reset state, producing the signal DRIVE L (high) which, when applied to the transport interface logic (Figure A-2), generates the READY L interface signal.

At this point, the interface transmits the program generated START L signal, which ANDs with READY L (Figure A-2) to reset the Write flip-flop. If the tape is at the beginning-of-tape (BOT) clear leader when START L is issued, and the previous command was a reverse command, the Inhibit gating circuit produces the signal INHIBIT H. INHIBIT H, applied to the bottom leg of a NAND gate, prevents D GO L from being generated and thus, reverse tape motion onto the BOT leader is prevented. In addition, INHIBIT H allows the resultant signal from START L to trigger the 30-millisecond Stop Delay one-shot. This action removes the READY L interface signal. When the Stop Delay one-shot times out, READY L is again generated, along with the EOT/BOT L interface signal to indicate a fault condition. If the tape is not at the (BOT) clear leader, INHIBIT H is not produced, resulting in the signal D GO L. This signal sets the Drive flip-flop (Figure A-3), generating DRIVE L. DRIVE L removes the READY L interface signal and enables the bottom leg of the MOVE A H gate (Figure A-5).

If the appropriate tape cassette has been properly loaded and drive A is selected, MOVE A H is generated. This signal is then ANDed with REV H at the tension motor control gate to apply +12 Vdc to the drag motor. In addition, MOVE A H is ANDed with REV H at the servo input gate to initiate reverse tape motion under servo control (Paragraph 4.6.1). Since a back block gap operation is being performed, HIGH SPEED H is low (Figure A-2). This signal, when applied through an inverter (Figure A-5), produces a +4 Vdc V REF signal. With +4 Vdc applied to the V REF terminal of the servo, reverse tape motion occurs at read/write speed (9 ips average).

As the tape moves backward across the read/write head, data from the tape triggers the Signal one-shot (Figure A-7). As long as data is present, the Signal one-shot remains set (Paragraph 4.5.9.3). 15 milliseconds after the last data transition is detected (tape in the pre gap), the Signal one-shot resets. This action removes SIGNAL H from the Drive flip-flop (Figure A-3), causing it to reset. With DRIVE L high, the MOVE A H gate (Figure A-5) is disabled, allowing tape motion to ramp to a stop. In addition, DRIVE L (high), applied to the transport interface logic (Figure A-2), generates the READY L interface signal.

4.5.4 Back File Gap

To space the tape backward one file, the interface simultaneously selects drive A (Paragraph 4.5.1) and issues a Back File Gap command. BACK FILE GAP L, applied through the transport interface logic (Figure A-2), produces the signals REV L and HIGH SPEED H. The program generated START L signal removes the READY L interface signal and conditions the tension and control motors exactly the same as for a back block gap operation (Paragraph 4.5.3). However, HIGH SPEED H, applied through an inverter (Figure A-5), produces a +12 Vdc V REF signal. In addition, HIGH SPEED H is applied to the switching circuit of the Signal one-shot (Figure A-7) to change the one-shot timeout to 75 milliseconds. With +12 Vdc applied to the V REF terminal of the servo (Figure A-5), reverse tape motion occurs at search speed (22 ips average).

The remainder of the back file gap operation is similar to the back block gap operation. However, because of the extended Signal one-shot timeout, reverse tape motion stops at two-thirds of the previous file gap (75 milliseconds after the last data transition is detected).

4.5.5 Turn-Around Clear Leader Handling

If forward tape motion is occurring near the end of the tape, and any of the reverse commands (Rewind, BBG, or BFG) are issued, it is possible that before forward tape motion has stopped the tape may have coasted onto the end-of-tape clear leader. If this occurred, the signal LDR A L (Figure A-6) would cause one of the following erroneous operations:

a. Immediately reset the Rewind one-shot, indicating that the tape has completely rewound to the beginning of the tape and is ready for forward operations.

b. Immediately reset the Drive flip-flop, indicating that the beginning of the tape has been reached and the reverse tape operation is completed.

To prevent this, whenever tape is moving forward, the Dir A flip-flop is set. When the Rewind one-shot sets for a rewind operation (Paragraph 4.5.2), the signal REWIND A L resets the Dir A flip-flop. This action triggers the 125-millisecond LDR Inhibit one-shot to inhibit the signal LDR A L for 125 milliseconds during the tape turn-around time. Similarly, for all other reverse commands, REV L (high) resets the Dir A flip-flop to trigger LDR Inhibit.

4.5.6 Forward File Gap

To space the tape forward one file, the interface simultaneously selects drive A (Paragraph 4.5.1) and issues a Read/Write Gap command.

NOTE

The Read/Write Gap command is used for both a forward file and a write file gap operation; however, for a forward file gap operation, the interface does not transmit WRITE MODE L.

R/W GAP L, applied through the transport interface logic (Figure A-2), generates the signal R/W GAP H. If the tape is not in motion, the Drive flip-flop (Figure A-3) is in the reset state, producing the signal DRIVE L (high) which, when applied to the transport interface logic (Figure A-2), generates the READY L interface signal.

At this point, the interface transmits the program generated START L signal, which ANDs with READY L (Figure A-2) to reset the Write flip-flop and also generate READ FG H. If the tape is at the end-of-tape (EOT) clear leader when START L is issued, and the previous command was a forward command, the Inhibit gating circuit produces the signal INHIBIT H. INHIBIT H, applied to the bottom leg of a NAND gate, prevents D GO L from being generated and thus, forward tape motion onto the EOT leader is prevented. In addition, INHIBIT H allows the resultant signal from START L to trigger the 30-millisecond Stop Delay one-shot. This action removes the READY

L interface signal. When the Stop Delay one-shot times out, READY L is again generated, along with the EOT/BOT L interface signal, to indicate a fault condition. If the tape is not at the EOT leader, INHIBIT H is not produced and the signal D GO L is generated. This signal sets the Drive flip-flop (Figure A-3), generating DRIVE L. DRIVE L removes the READY L interface signal and enables the bottom leg of the MOVE A H gate (Figure A-5). If the appropriate tape cassette has been properly loaded and drive A is selected, MOVE A H is generated. Since a forward file gap operation is being performed, REV L is high (Figure A-2) and HIGH SPEED H is low. REV L (high) is applied through an inverter (Figure A-5) to disable the tension motor control gate and thus apply +5 Vdc to the tension motor. In addition, REV L (high), ANDed with MOVE A H at the servo input gate, initiates forward tape motion under servo control (Paragraph 4.6.1). HIGH SPEED H (low), applied through an inverter, produces a +4 Vdc V REF signal. With +4 Vdc applied to the V REF terminal of the servo, forward tape motion occurs at read/write speed (9 ips average).

If the tape is at the beginning-of-tape (BOT) clear leader, the signal LDR H is present. LDR H, applied through an inverter (Figure A-3), disables the D input of the First LDR flip-flop. When D GO L is generated, this flip-flop resets, producing the signal FIRST LDR L. FIRST LDR L, applied through a NOR gate, holds the Tape Blank one-shot set, thus permitting tape motion across the first extended file gap.

If the tape is not at clear leader or data when the space command is received, READ FG H releases the 385-millisecond Tape Blank one-shot. If this one-shot times out before data is detected, BLANK STOP L is generated to reset the Drive and set the EOF flip-flops. DRIVE L (high) disables the MOVE A H gate (Figure A-5), allowing tape motion to ramp to a stop. In addition, DRIVE L (high) and END FILE H are applied to the transport interface logic (Figure A-2) to generate the READY L and END FILE L interface signals.

If, after tape motion is initiated, data is detected prior to the 385-millisecond Tape Blank timeout, the Signal one-shot is triggered (Figure A-7), generating SIGNAL H to set the First LDR flip-flop and also to keep the Tape Blank one-shot set. As long as data is present, the Signal one-shot remains set (Paragraph 4.5.9.3). SIGNAL H, applied to the interface logic (Figure A-2), produces HIGH SPEED H which, when applied through an inverter (Figure A-5), produces a +12 Vdc V REF signal to switch the tape servo system to search speed (22 ips average). In addition, HIGH SPEED H and R/W GAP H, applied to the switching circuits of the Signal one-shot, changes the one-shot timeout to 150 milliseconds. 150 milliseconds after the last data transition is detected (tape advanced to the next file gap), the Signal one-shot resets generating SIGNAL H (low). This signal resets the Drive and sets the EOF flip-flop (Figure A-5), producing the END FILE L interface signal and stopping tape motion two-thirds into the file gap.

4.5.7 Write File Gap

To write a file gap, the interface simultaneously selects drive A (Paragraph 4.5.1), issues a Read/Write Gap command, and transmits the WRITE MODE L interface signal.

NOTE

The Read/Write Gap command is used for both a forward file or a write file gap operation; however, for a forward file gap operation, the interface does not transmit WRITE MODE L.

R/W GAP L, applied through the transport interface logic (Figure A-2), generates the signal R/W GAP H. If the appropriate tape cassette has been properly loaded and the cassette is write enabled, Write Protect switch SW A (Figure A-5) is closed, producing the signal WRITE PERMIT H. This signal, applied through an inverter on the transport interface logic (Figure A-2) removes the WRITE PROTECT L interface signal. In addition, WRITE PERMIT H enables the lower legs of the head drivers (Figure A-7). If the tape is not in motion, the Drive flip-flop (Figure A-3) is in the reset state, producing the signal DRIVE L (high) which, when applied to the transport interface logic, generates the READY L interface signal.

At this point, the interface transmits the program generated START L signal, which ANDs with READY L (Figure A-2) to set the Write flip-flop. WRITE MODE H generates the WRITE STATUS L interface signal and also ANDs with R/W GAP H to produce the signal W GAP L. If the tape is at the end-of-tape (EOT) clear leader when START L is issued, and the previous command was a forward command, the Inhibit gating circuit produces the signal INHIBIT H. INHIBIT H, applied to the bottom leg of a NAND gate, prevents D GO L from being generated and thus, forward tape motion further onto the EOT leader is prevented. In addition, INHIBIT H allows the resultant signal from START L to trigger the 30-millisecond Stop Delay one-shot. This action removes the READY L interface signal. When the Stop Delay one-shot times out, READY L is again generated, along with the EOT/BOT L interface signal, to indicate a fault condition. If the tape is not at the EOT leader, INHIBIT H is not produced and the signal D GO L is generated. This signal sets the Drive flip-flop (Figure A-3), generating DRIVE L and DRIVE H. DRIVE L removes the READY L interface signal and enables the MOVE A H gate (Figure A-5). In addition, D GO H is ANDed with W GAP L to trigger the 535 millisecond WF Gap one-shot (Figure A-3).

If the tape is at the beginning-of-tape (BOT) clear leader, the signal LDR H is present. LDR H, applied through an inverter, disables the D input of the First LDR flip-flop. When D GO L is generated, this flip-flop resets, producing the signal FIRST LDR H. FIRST LDR H, when applied to the base of the WF Gap transistor, turns this transistor off, thus changing the one-shot timeout to 1.4 seconds. This circuit configuration allows an extended file gap ($\approx$3 times longer) to be written at the beginning of tape.

Drive H (Figure A-3) is ANDed with DATA MODE H, but because the drive is not reading or writing data DATA MODE H is low. The resulting high signal is presented to the NAND gate inputting to the Gap Time one-shot, holding it set. The output of the one-shot, GAP TIME H, inhibits the C input of the Write Encode flip-flop. Also, after being inverted twice it qualifies one input of the NAND gate inputting to the direct reset of the Write Encode flip-flop. When the first CLK 1 L pulse comes the Write Encode flip-flop will be reset, and will remain in this state throughout this entire operation.

NOTE

The Write Encode flip-flop is held reset when writing any gap to insure proper gap polarity.

Since a write file gap operation is being performed, REV L is high (Figure A-2) and HIGH SPEED H is low. REV L (high) is applied through an inverter (Figure A-5) to disable the tension motor control gate and thus apply +5 Vdc to the tension motor. In addition, REV L (high), ANDed with MOVE A H at the servo input gate, initiates forward tape motion under servo control (Paragraph 4.6.1). HIGH SPEED H (low), applied through an inverter, produces a +4 Vdc V REF signal. With +4 Vdc applied to the V REF terminal of the servo, forward tape motion occurs at read/write speed (9 ips average).

When the WF Gap one-shot times out (Figure A-3), END WFG L is generated to reset the Drive flip-flop and also to produce the signal END WRITE H. With DRIVE L high, the MOVE A H gate (Figure A-5) is disabled, allowing tape motion to ramp to a stop; however, END WRITE H triggers the 30-millisecond Stop Delay one-shot (Figure A-2) to suppress the READY L interface signal until tape motion has completely stopped.

4.5.8 Write Data Block

The TU60 uses a phase encoded method of magnetic data recording. In this method, bit cell boundaries (flux transitions) are recorded on the magnetic tape at 220 microsecond intervals. Data storage occurs at these bit cell boundaries and the binary value of the stored bit depends upon the polarity of the transition. If, for example, a negative to positive transition occurs at the bit cell boundary, a logical 0 bit is stored; however, if a positive to negative transition occurs, a logical 1 bit is stored. The transitions that may occur between bit cell boundaries are called phase flux transitions. Figure 4-7 illustrates a phase encoded waveform of a segment of tape containing 111001.

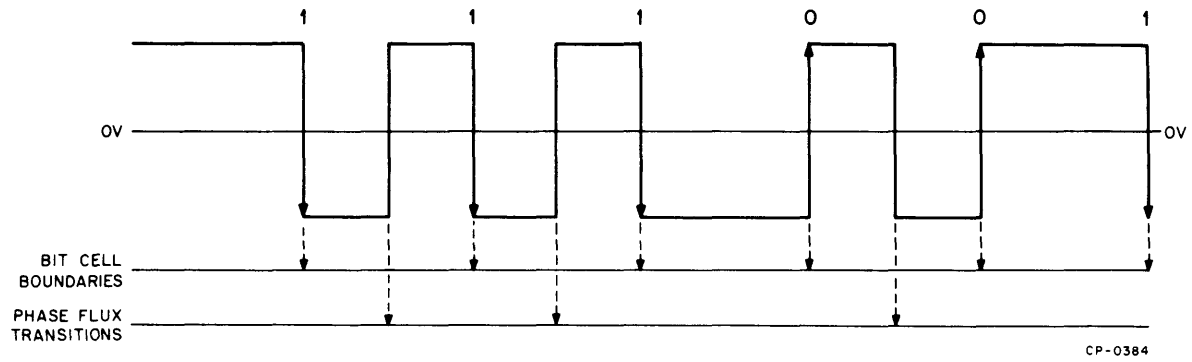


Figure 4-7 Typical Phase Encoded Waveform

Figure 4-8 illustrates and the following paragraphs describe the logical operations and control functions necessary to generate the data block.

4.5.8.1 Command Initiation – To initiate a write operation, the interface simultaneously selects drive A (Paragraph 4.5.1) and issues a Write command. WRITE MODE L, applied to the transport interface logic (Figure A-2), enables the D input of the Write flip-flop. If the appropriate tape cassette has been properly loaded and the cassette is write enabled, Write Protect switch SW A (Figure A-6) is closed, producing the signal WRITE PERMIT H. This signal, applied through an inverter on the transport interface logic, removes the WRITE PROTECT L interface signal. In addition, WRITE PERMIT H, applied to the read/write logic (Figure A-7), enables the lower legs of the head drivers. If the tape is not in motion, the Drive flip-flop (Figure A-3) is in reset state, producing the signal DRIVE L (high) which, when applied to the transport interface logic, generates the READY L interface signal.

4.5.8.2 Tape Start and Pre Gap – At this point, the interface transmits the program generated START L signal which ANDs with READY L (Figure A-2) to set the Write flip-flop and also to produce the signals CLEAR L and CLEAR H. If the tape is at the end-of-tape (EOT) clear leader when START L is issued, and the previous command was a forward command, the Inhibit gating circuit produces the signal INHIBIT H. INHIBIT H, applied to the bottom leg of a NAND gate, prevents D GO L from being generated and thus forward tape motion onto the EOT leader is prevented. In addition, INHIBIT H allows the resultant signal from START L to trigger the 30-millisecond Stop Delay one-shot. This action removes the READY L interface signal. When the Stop Delay one-shot times out, READY L is again generated, along with the EOT/BOT L interface signal, to indicate a fault condition. If the tape is not at the EOT leader, INHIBIT H is not produced and the signal D GO L is generated. This signal sets the Drive flip-flop (Figure A-3), generating DRIVE L. DRIVE L removes the READY L interface signal and enables the MOVE A H gate (Figure A-5).

Since a write data operation is being performed, DATA MODE H (Figure A-2) is high, HIGH SPEED H is low, and REV L is high. REV L (high) is applied through an inverter (Figure A-5) to disable the tension motor control gate and thus apply +5 Vdc to the tension motor. In addition, REV L (high), ANDed with MOVE A H at the servo input gate, initiates forward tape motion under servo control (Paragraph 4.6.1). HIGH SPEED H (low), applied through an inverter, produces a +4 Vdc V REF signal. With +4 Vdc applied to the V REF terminal of the servo, forward tape motion occurs at read/write speed (9 ips average).

CLEAR H sets the State flip-flop (Figure A-3), generating the signal PREAMBLE H while CLEAR L resets the CRC Time flip-flop. DATA MODE H, ANDed with DRIVE H, releases the 40-millisecond Gap Time one-shot; however, while set, this one-shot produces the signals GAP TIME H and GAP TIME L. During the pre gap time, GAP TIME H, applied to the input gates of the Write Encode flip-flop, inhibits the C input and, at the next CLK 1 L, resets the Write Encode flip-flop.

NOTE

The Write Encode flip-flop is held reset when writing any gap to insure proper gap polarity.

GAP TIME L applied through a NOR gate, clears the Byte/Preamble Counter and prevents it from incrementing.

4.5.8.3 Write Preamble and Data Byte Transfer – The next CLK 2 L pulse, after the Gap Time one-shot times out, complements the Write Encode flip-flop on the leading edge and increments the Byte/Preamble Counter to a count of 1 on the trailing edge. W DATA H (high), applied to the top head driver (Figure A-7), generates a negative to positive flux (logical 0 bit) on the tape.

NOTE

During the write operation, CLK 1 L pulses from the Write Clock (Figure A-7) may produce (depending upon the data) phase flux transitions; however, CLK 2 L pulses always produce bit cell transitions.

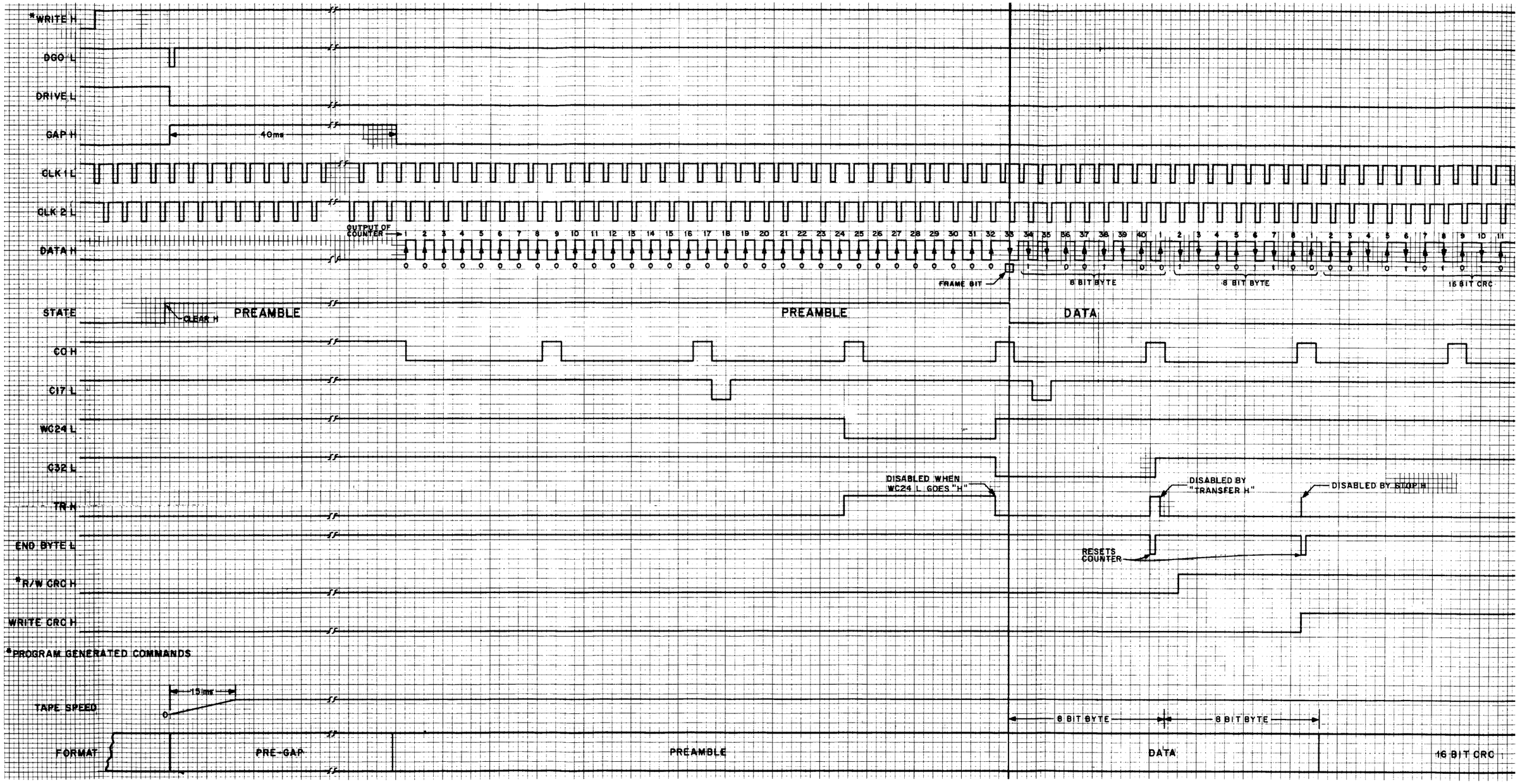
The Write Encode complement process continues until the Byte/Preamble Counter has reached a count of 32. However, at count 24, WC 24 L resets the Trans Req flip-flop, generating TR H. TR H, applied to the transport interface logic (Figure A-2), produces the TRANSFER REQ L interface signal. When the interface receives this signal, it places the first 8 bits to be recorded on the eight data interface lines and issues a TRANSFER L interface signal. TRANSFER L, applied through the transport interface logic, sets the Trans Req flip-flop (Figure A-3), thus removing the TRANSFER REQ L interface signal and also generating the signal LOAD BUFFER H. This signal, when applied to the Data Buffer, strobes the 8 parallel data bits from the interface lines into the buffer.

When the Byte/Preamble Counter has incremented to a count of 32, C 32 L disables the middle input gate of the Write Encode flip-flop, allowing the next CLK 1 L to set the Write Encode flip-flop. In addition, C 32 H, applied to the clock gate of the State flip-flop, allows the following CLK 2 L pulse to reset the flip-flop, producing the signal PREAMBLE H (low). This same CLK 2 L pulse also resets the Write Encode flip-flop, thus producing a logical 1 bit (Frame Bit) on the tape.

4.5.8.4 Write Data – PREAMBLE H (low), ANDed with WRITE CRC H (low), produces the signal DATA TIME H. DATA TIME H, applied through an inverter, is ANDed with CLK 1 L to produce SHIFT CLK H. This signal, when applied to the Data Buffer (Figure A-2), serially shifts a data bit out through the WDL inverter. In addition, CLK 1 L, applied through an inverter (Figure A-3), produces the signal CRC CLK L. This signal shifts the contents of the CRC Register (Paragraph 4.5.10). The WDL Data Buffer output, ANDed with DATA TIME H, either sets or resets the Write Encode flip-flop, depending upon the binary value (logical 1 or 0) of WDL. Correspondingly, either a logical 1 or 0 flux transition is recorded on the tape. Every CLK 1 L pulse loads the Write Encode flip-flop with a logical bit while the respective CLK 2 L pulse complements the Write Encode flip-flop and the trailing edge of the same CLK 2 L pulse increments the Byte/Preamble Counter. When the Counter has incremented to a count of 40 (one bit prior to writing the 8th bit), C0 H is ANDed with SHIFT CLK H at the clock input to the Trans Req flip-flop to generate the signal END BYTE L. This signal resets the Trans Req flip-flop, generating another TRANSFER REQ L interface signal and also clearing the Byte/Preamble Counter. The interface then transfers another 8-bit data byte as previously described and the recording process continues.

NOTE

During DATA TIME H, every count 0 produces a TRANSFER REQ L, thereby repeating the 8-bit data byte transfer and record process.


*WRITE H
DGO L
DRIVE L
GAP H
40ms
CLK 1 L
CLK 2 L
OUTPUT OF COUNTER
DATA H
FRAME BIT
8 BIT BYTE
8 BIT BYTE
16 BIT CRC
STATE
CLEAR H
PREAMBLE
PREAMBLE
DATA
C0 H
C17 L
WC24 L
G32 L
DISABLED WHEN WC24 L GOES "H"
DISABLED BY "TRANSFER H"
DISABLED BY STOP H
TR H
END BYTE L
RESETS COUNTER
*R/W CRC H
WRITE CRC H
*PROGRAM GENERATED COMMANDS
TAPE SPEED
15ms
0
8 BIT BYTE
8 BIT BYTE
FORMAT
PRE-GAP
PREAMBLE
DATA
16 BIT CRC

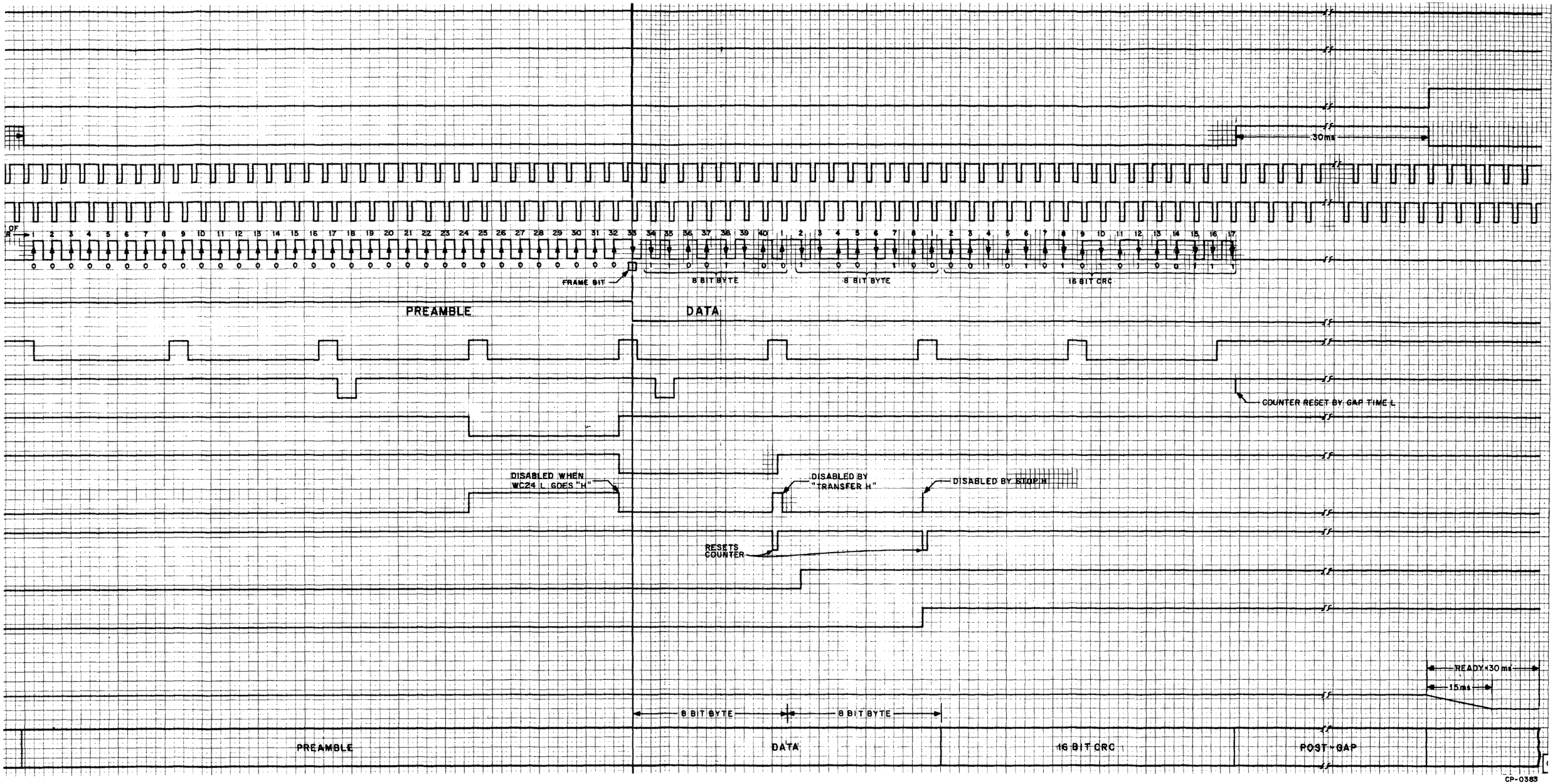


Figure 4-8 Write Timing

4.5.8.5 Write CRC Character – After the final 8 data bits have been loaded into the Data Buffer and before they are completely written onto the tape, the interface issues a Write CRC command. R/W CRC L, applied through the transport interface logic (Figure A-2), enables the D input of the CRC Time flip-flop (Figure A-3). When the Byte Counter has incremented to a count of 0 for the final data bit, C0 H again resets the Trans Req flip-flop; however, because R/W CRC H is present, this action also causes the CRC flip-flop to set, generating the signal WRITE CRC H. This signal produces STOP H which immediately sets the Trans Req flip-flop preventing this final TRANSFER REQUEST from being received by the interface logic. In addition, WRITE CRC H disables the bottom leg of the DATA TIME H gate and enables the top leg of the CRC BIT 1 L gate, applying the output from the CRC Register to the Write Encode flip-flop. (Refer to Paragraph 4.5.10 for a description of the CRC Register operation.) The content of the CRC Register is then serially shifted out, phase encoded, and recorded on the tape in the same manner as the previously described data recording process.

4.5.8.6 Post Gap and Tape Stop – When the Byte/Preamble Counter has incremented to a count of 17, C 17 L is ANDed with WRITE CRC H to again set the Gap Time one-shot. GAP TIME L, applied through a NOR gate, clears the Byte/Preamble Counter and prevents it from incrementing further. Thus, a 30-millisecond post gap is erased from the tape in the same manner as the pre gap. When the Gap Time one-shot times out, END W DATA L is produced which resets the Drive flip-flop and also generates END WRITE H. With DRIVE L high, the MOVE A H gate (Figure A-5) is disabled, allowing tape motion to ramp to a stop; however, END WRITE H triggers the 30-millisecond Stop Delay one-shot (Figure A-2) to suppress the READY L interface signal until after tape motion has completely stopped.

4.5.9 Read Data Block

Figure 4-10 illustrates and the following paragraphs describe the logical operations and control functions required to read a data block.

4.5.9.1 Command Initiation – To initiate a read operation, the interface simultaneously selects drive A (Paragraph 4.5.1) and negates the WRITE MODE L interface signal. If the appropriate tape cassette has been properly loaded and the tape is not already in motion, the Drive flip-flop (Figure A-3) is in the reset state, producing the signal DRIVE L (high) which, when applied to the transport interface logic (Figure A-2), generates the READY L interface signal.

4.5.9.2 Tape Start and Pre Gap – At this point, the interface transmits the program generated START L signal which ANDs with READY L (Figure A-2) to reset the Write flip-flop and also to produce the signals CLEAR L and CLEAR H. With the Write flip-flop reset, READ L, applied to a NAND gate, produces READ SELECT H which enables the Data Buffer output transmitters. If the tape is at the end-of-tape (EOT) clear leader when START L is issued, and the previous command was a forward command, the Inhibit gating circuit produces the signal INHIBIT H. INHIBIT H, applied to the bottom leg of a NAND gate, prevents D GO L from being generated and thus forward tape motion onto the EOT leader is prevented. In addition, INHIBIT H allows the resultant signal from START L to trigger the 30-millisecond Stop Delay one-shot. This action removes the READY L interface signal. When the Stop Delay one-shot times out, READY L is again generated, along with the EOT L interface signal, to indicate a fault condition. If the tape is not at the EOT leader, INHIBIT H is not produced and the signal D GO L is generated. This signal sets the Drive flip-flop (Figure A-3), generating DRIVE L. DRIVE L removes the READY L interface signal and enables the MOVE A H gate (Figure A-5).

Since a read operation is being performed, DATA MODE H (Figure A-2) is high, HIGH SPEED H is low, and REV L is high. REV L (high) is applied through an inverter (Figure A-5) to disable the tension motor control gate and thus apply +5 Vdc to the tension motor. In addition, REV L (high), ANDed with MOVE A H at the servo input gate, initiates forward tape motion under servo control (Paragraph 4.5.1.2). HIGH SPEED H (low), applied through an inverter, produces a +4 Vdc V REF signal. With +4 Vdc applied to the V REF terminal of the servo, forward tape motion occurs at read/write speed (9 ips average). CLEAR H sets the State flip-flop (Figure A-3), generating the signal PREAMBLE H, while CLEAR L resets the CRC Time flip-flop. During the pre gap portion of tape motion, ENERGY H (low) applied through a NOR gate, clears the Byte/Preamble Counter and prevents it from incrementing.

If the tape is at the beginning-of-tape (BOT) clear leader, the signal LDR H is present. LDR H, applied through an inverter (Figure A-3), disables the D input of the First LDR flip-flop. When D GO L is generated, this flip-flop resets, producing the signal FIRST LDR L. FIRST LDR L, applied through a NOR gate, holds the Tape Blank one-shot set, thus allowing tape motion at read/write speed across the first extended file gap. If the ensuing tape is blank, tape motion continues until the EOT leader is detected.

4.5.9.3 Preamble Detection and Read Clock Synchronization – When the preamble flux transitions on the tape pass across head A (Figure A-7), induced current flows through the read coil (J5). The direction of the current flow depends upon the polarity of the flux transitions. These small read signals (approximately 15 mV) are transmitted through series isolation diodes to the positive and negative input of a differential read preamplifier. Clipping diodes at the preamplifier input protect the preamplifier during a write operation by clipping the large write signals to 0.5V; however, during a read operation, the small read signals are unaffected. The preamplified output (approximately 300 mV) is then transmitted to a read amplifier, the output of which (approximately 5.0V) is applied to both the Block and Peak Detectors.

In the Block Detector, the 5.0V sinusoidal read waveform is applied to a threshold amplifier. The triggering level of the amplifier is adjusted so that only the portion of the read waveform that is above approximately +0.7V produces a square-wave output. This square-wave output, when applied through an integrator, progressively charges a 2.2 microfarad capacitor to +1.8V. When the capacitor reaches +1.8V, an output from the adjoining gate is ANDed with READ DATA L to trigger the 1-millisecond Energy one-shot. This action enables both the PEAKS L output gate of the Transition Detector and the D input of the Seek flip-flop. Thus, PEAKS L pulses from the Transition Detector are suppressed until at least 3 to 5 preamble bits have sufficiently charged the 2.2 microfarad capacitor. In addition, ENERGY H, applied through a NOR gate (Figure A-3), allows CLK 2 L pulses from the yet unsynchronized Read Clock (Figure A-7) to increment the Byte/Preamble Counter.

Simultaneously, in the Peak Detector (Figure A-7) the 5.0V sinusoidal waveform is applied directly to the positive input of a comparator, while the negative input to the comparator is delayed by a 47 mH coil. The comparator converts the read signal peaks into square-wave transitions (Paragraph 4.6.4) that occur slightly after the read signal peak. The Peak Detector square-wave output (READ DATA L) is then applied to two Transition Detector gates and also to the serial input of the Data Buffer (Figure A-2). The upper (negative) Transition Detector gate (Figure A-7) produces a negative pulse for every positive square-wave transition, while the lower (positive) Transition Detector gate is disabled by SEEK H (low).

Hence, during the preamble read time, only the positive square-wave transitions (which occur at the bit cell boundaries) produce a PEAKS L output. The PEAKS L output is then applied to the phase lock loop to slew the voltage controlled oscillator (VCO) until the oscillator output matches the phase and frequency of the applied PEAKS L signal (Paragraph 4.6.3). Thus, the Read Clock VCO is synchronized to only the bit cell boundary frequency. READ DATA L is also ANDed with BUF READ H to trigger the 15-millisecond Signal one-shot.

While the Read Clock VCO is synchronizing, the Byte/Preamble Counter (Figure A-3) increments to a count of 24. C 24 H sets the Seek flip-flop (Figure A-7), generating the signal SEEK H. This signal removes the preset input to the Sync flip-flop and also enables the lower (positive) Transition Detector gate. In addition, SEEK H, applied to the formatter logic (Figure A-3), clears the Byte/Preamble Counter and prevents it from incrementing further during the remainder of the preamble.

4.5.9.4 End Preamble (Frame Bit Detection) – With SEEK H applied to the positive Transition Detector gate (Figure A-7), POS PEAKS L (which are now occurring at the phase flux transitions) are generated. Since the Read Clock VCO is now synchronized with the bit cell boundary frequency, these additional POS PEAKS L pulses must not be applied to the phase lock loop. To prevent this, the signal BLANK H (derived from the VCO), which occurs during the middle 50 percent of the bit cell, is ANDed with SEEK H to disable the lower leg of the PEAKS L gate. Thus, during the phase flux transition time, PEAKS L pulses are not applied to the phase lock loop. In addition, the leading edge of BLANK H produces CLK 1 L pulses (Figure 4-9) while the trailing edge produces CLK 2 L pulses.

As long as positive transitions (logical 0 bits) are occurring in the preamble, READ DATA and CLK 1 L pulses keep the Sync flip-flop set. When the preamble Frame Bit (logical 1 bit) occurs, READ DATA L allows CLK 1 L to reset the Read Sync flip-flop. This action generates the signal READ SYNC L which resets the State flip-flop (Figure A-3), producing the signal PREAMBLE H (low).

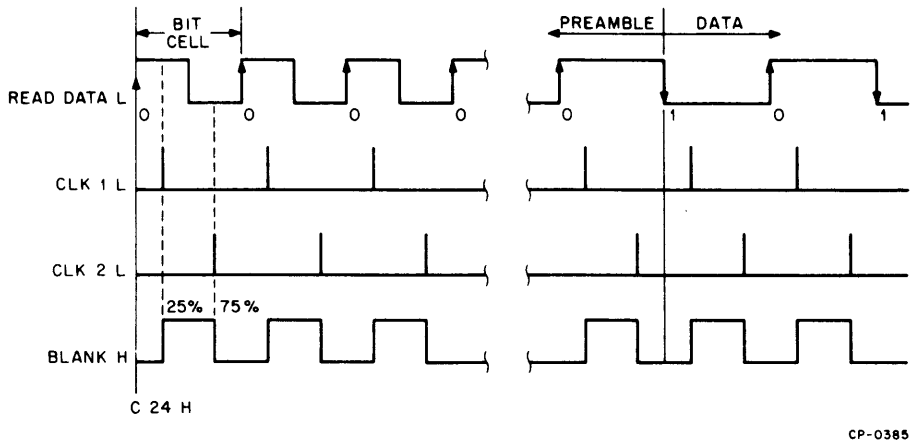


Figure 4-9 Simplified Blank H and Read Clock Timing

4.5.9.5 Data Detection – With the State flip-flop reset, PREAMBLE H (low), ANDed with SEEK H, allows the trailing edge of the first CLK 2 L pulse after the Frame Bit to increment the Byte Counter to a count of 1. In addition, PREAMBLE H (low) enables the DATA TIME H gate, allowing the next CLK 1 L pulse to produce a SHIFT CLK H pulse. This pulse, when applied to the Data Buffer (Figure A-2), serially shifts the first read data bit into the buffer. Simultaneously, DATA TIME H is applied through an inverter to enable a CRC CLK L pulse which shifts the same data bit into the CRC Register. (Refer to Paragraph 4.5.10 for a description of the CRC Register operation.) The following CLK 2 L pulse increments the Byte Counter to a count of 2. BLANK H (Figure A-7) still disables the PEAKS L output during phase flux transitions; however, when a negative or positive transition occurs at a bit cell boundary, the BLANK H signal is not present and the PEAKS L output is enabled. Thus, the phase lock loop remains synchronized to only the bit cell boundary frequency.

As the remaining bits in the first data byte are read from the tape, SHIFT CLK H pulses (generated at CLK 1 L time) load them into the Data Buffer and CLK 2 L pulses increment the counter. When the Byte Counter has incremented to a count of 8 (one-half bit prior to reading the 8th data bit), C0 H is produced (Figure A-3). C0 H is then ANDed with the next SHIFT CLK H at the clock input of the Trans Req flip-flop to generate END BYTE L and simultaneously, the 8th bit is loaded into the Data Buffer. END BYTE L clears the Byte Counter and also resets the Trans Req flip-flop, generating TR H. This signal, when applied to the transport interface logic (Figure A-2), produces the TRANSFER REQ L interface signal. When the interface receives this signal, it loads the 8 parallel bits from the interface lines into the Interface Buffer and issues a TRANSFER L interface signal. The reading process continues as previously described and another 8-bit data byte is serially loaded into the Data Buffer and then parallel transferred to the interface.

NOTE

During DATA TIME H, every count 0 produces a TRANSFER REQ L, thereby repeating the 8-bit data byte transfer to the interface.

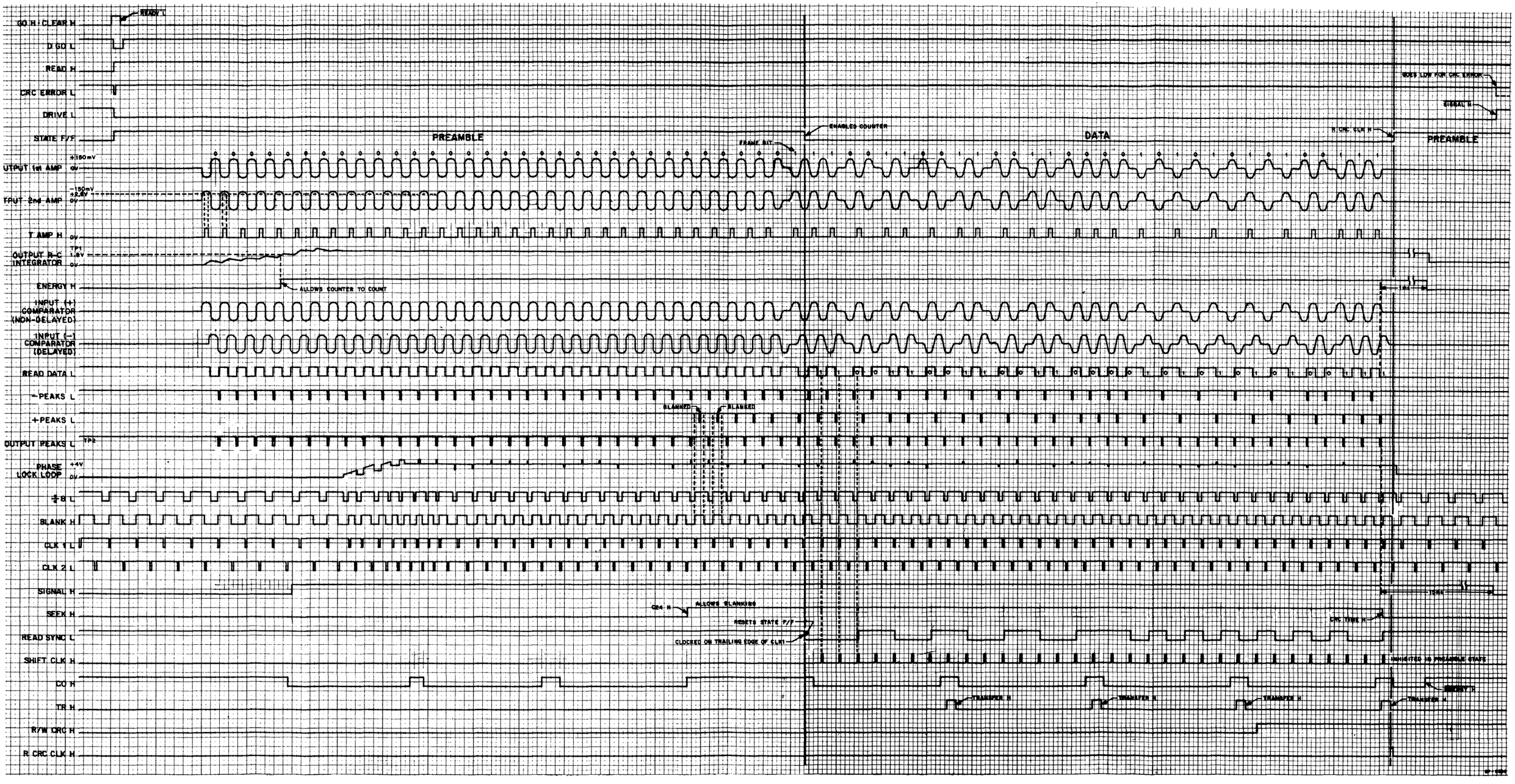


Figure 4-10 Read Timing

4.5.9.6 Read CRC Character – After the first 8 bits of the CRC character have been transferred to the interface, the interface issues a Read CRC command. R/W CRC L, applied through the transport interface logic (Figure A-2), enables the D input of the CRC Time flip-flop (Figure A-3) and is also ANDed with WRITE L (high) to enable the lower leg of the R CRC CLK H gate. The remaining 8 CRC bits are serially loaded into the Data Buffer as previously described. When the Byte Counter has incremented to a count of 8 (one-half bit prior to reading the 16th CRC bit), C0 H is produced, then SHIFT CLK L again resets the Trans Req flip-flop to produce the signal TR H; however, because R/W CRC H is present, this action also causes the CRC Time flip-flop to set. TR H generates another TRANSFER REQ L to the interface and when the interface responds with the TRANSFER L interface signal, the Trans Req flip-flop sets. This action produces the signal R CRC CLK H which, when ANDed with GOOD CRC H (high only if the CRC Register is zero), resets the CRC Err flip-flop (Figure A-2). However, because the flip-flop output is combined with DRIVE L (high), the CRC ERROR L interface signal is not generated until tape motion begins to ramp to a stop.

4.5.9.7 Tape Stop – There are two methods by which tape motion can stop:

a. If, after the last CRC flux transition is detected, there is no noise on the read signal, the Peak Detector stops producing the square-wave signal READ DATA L. Removal of READ DATA L allows the 1-millisecond Energy one-shot to time out.

b. If, after the last CRC flux transition is detected, noise is present on the read signal, the Peak Detector continues to produce the square-wave READ DATA L; however, the 2.2 microfarad capacitor begins to discharge below the 1.8V threshold. This action also allows the Energy one-shot to time out.

For either case, when the Energy one-shot times out, the 2-millisecond Energy Clear one-shot is triggered, the output of which grounds the 2.2 microfarad capacitor and prevents it from recharging for at least 2 milliseconds. In addition, with the Energy one-shot reset, PEAKS L pulses are prevented from triggering the 15-millisecond Signal one-shot. When the Signal one-shot times out (tape blank for 15 ms), SIGNAL H (low), applied through a NOR gate (Figure A-3), resets the Drive flip-flop. With DRIVE L (high), the MOVE A H gate (Figure A-5) is disabled and tape motion ramps to a stop. DRIVE L (high) is also applied to the transport interface logic, generating the READY L interface signal and, if the CRC Err flip-flop has not reset by this time, the CRC ERROR L interface signal is also generated to indicate that a CRC error has occurred.

4.5.9.8 Tape Blank Stop – If a Read command is issued and the ensuing tape is blank, tape motion is initiated as previously described; however, when the Drive flip-flop sets (Figure A-3), the signal TAPE READING L is produced. This signal releases the 385-millisecond Tape Blank one-shot. As the tape moves across the read/write head, data from the tape generates the signal SIGNAL H which, when applied through an inverter, keeps the Tape Blank one-shot set. If data is not detected for 385 milliseconds, SIGNAL H is not produced and the Tape Blank one-shot times out. This action generates the signal BLANK STOP L, which resets the Drive flip-flop stopping tape motion as previously described. In addition, BLANK STOP L sets the EOF flip-flop to generate the END FILE L interface signal.

4.5.10 CRC Character

The Cyclic Redundancy Check (CRC) character is a 2-byte (16 bits), mathematically derived character which is recorded at the end of a data block. This character serves no function during a write operation, however, during a read operation, the CRC character is used to check the validity of the data block just read. The following paragraphs describe only the functional operation of the CRC logic.

4.5.10.1 CRC Derivation – At the start of a write operation, GO H is applied through an inverter (Figure A-4) to reset each stage of the 16-bit CRC Register. During the write operation, as each data bit is recorded on tape, it is also simultaneously applied to the WD L input gate of the CRC logic. Since WRITE CRC H is low at this time, the top leg of the input gate to the first exclusive OR circuit is enabled, thus allowing the output from the final CRC Register stage (2^0) to be recirculated and exclusively ORed with the incoming data. The CRC CLK L pulses that are generated in the formatter logic (Paragraph 4.5.8.4) shift the contents of the CRC Register in such a manner that the entire data block is divided by a selected CRC divisor ($2^{15}+2^{14}+2^2+2^0$) which is contained in the single flip-flop register elements shown on the logic drawing. The mathematical expression for this operation is:

$a_n 2^n+....a_3 2^3+a_2 2^2+a_1 2^1+a_0 2^0$ a = the coefficient of the bit position

$2^{15}+2^{14}+2^2+2^0$ n = the number of bit positions in the data block.

After the data block has been recorded, WRITE CRC H is generated (Paragraph 4.5.8.5) to disable the first exclusive OR input gate and inhibit additional exclusive OR operations. Only the remainder from the division process is now contained in the CRC Register. The CRC CLK L pulses, generated during the write CRC time, serially shift the division remainder out of the CRC Register, and this output (CRC BIT 1 L) is applied to the input gate of the Write Encode flip-flop (Figure A-3). Here, the division remainder is phase encoded and written onto the tape as the CRC character.

4.5.10.2 CRC Validation – During a read operation, each data bit that is retrieved from the tape (Paragraph 4.5.9.5) is manipulated in the CRC Register in exactly the same manner as it was during the CRC derivation. When the CRC character on the tape is encountered (Paragraph 4.5.9.6), it is added to the contents of the CRC Register and the resultant is then divided by the same selected CRC divisor ($2^{15}+2^{14}+2^2+2^0$). Since the original division remainder is added to the CRC Register at the end of this new division process, if all the data and CRC bits that were previously written on the tape are retrieved, the CRC Register should equal zero. The set output from each register stage is applied to the zero detection gates. If the CRC Register is zero, each input to the zero detection gate is low and the signal GOOD CRC H is generated. If any input to the zero detection gate is high (CRC Register not zero), the signal GOOD CRC H is not produced and, when READY L is generated, a CRC ERROR L interface signal is also transmitted to the interface.

4.5.11 Error and Logic Power Indications

Except for the Power-On lamp, there are no indicators on the TU60 DECassette Tape Transport. If, during normal operation of a selected drive, the +5V power supply (logic power) fails or a Time or CRC error occurs, these fault indications are transmitted (via interface signals) to the interface. Thus, the processor can monitor the fault status of each drive merely by selecting it. The following paragraphs describe the logical operation of the error and logic power monitoring circuits.

4.5.11.1 CRC Error – The CRC ERROR L interface signal (Figure A-2) is generated if an invalid CRC test occurs during a read operation (Paragraph 4.5.9.6).

4.5.11.2 Time Error – During a read or write operation, whenever a data byte is ready for transfer via the interface lines, the Trans Req flip-flop (Figure A-3) resets to generate the signal TR H. TR H enables the D input of the Time Err flip-flop (Figure A-2). If the interface does not respond with a TRANSFER L signal to set the Trans Req flip-flop and remove TR H by the time the next SHIFT CLK H signal is produced ($\approx$220 μs from TR H time), the Time Err flip-flop sets and a TIME ERROR L interface signal is generated.

4.5.11.3 Power OK – The PWR OK L interface line indicates the status of the +5 Vdc logic power. During normal operation, +5 Vdc from the regulated supply is applied through a 220-ohm resistor (Figure A-7) to a 3.3V Zener diode. If the +5 Vdc is greater than approximately 4.1V, the Zener diode conducts to turn on transistor Qi1 and supply a ground, through the isolation diode, to the PWR OK L interface line. If the +5 Vdc drops below approximately +4 Vdc, the Zener diode stops conducting, turning off transistor Q11. This circuit configuration leaves the PWR OK L line floating, thus indicating a fault condition to the interface.

4.6 ANALOG CIRCUIT ANALYSIS

4.6.1 Control Motor Servo System

The control motor servo system (Figure 4-11) controls the tape speed during all operations except rewind. The four basic tape operational speeds (read/write forward, reverse; search forward, and search reverse) are obtained from the servo system through an 8:1 speed reduction wheel on the drive. The search speeds are 2.2 times faster than the read/write speeds.

The servo system is composed of the following functional circuits:

- a ramp and reference generator that produces four separate reference voltage levels (desired speed commands) and controlled ramps to these levels
- a tachometer circuit that electronically generates a voltage which is proportional to the actual motor speed
- an error amplifier that amplifies the signal resulting from the comparison of the desired speed to the actual speed
- a power amplifier that amplifies the error signal and applies it to the motor to either speed up or slow down the motor.

The following paragraphs describe the servo operation.

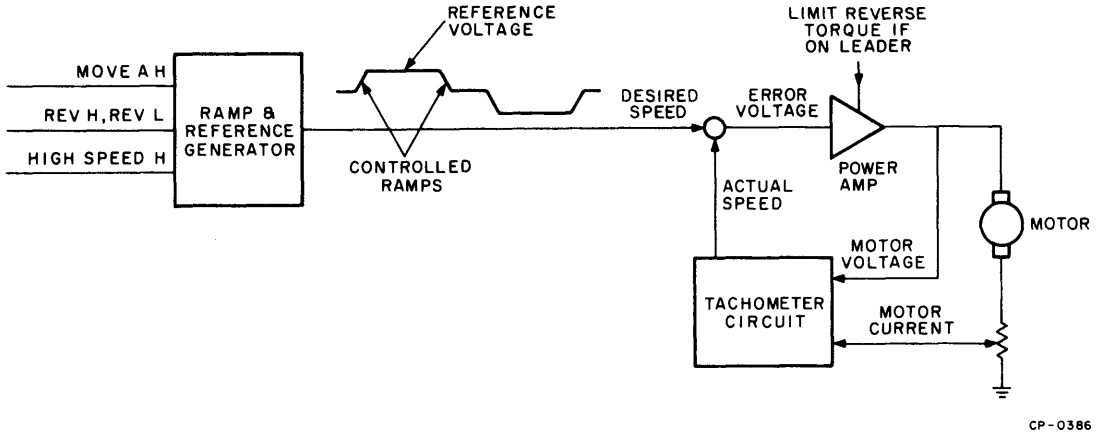
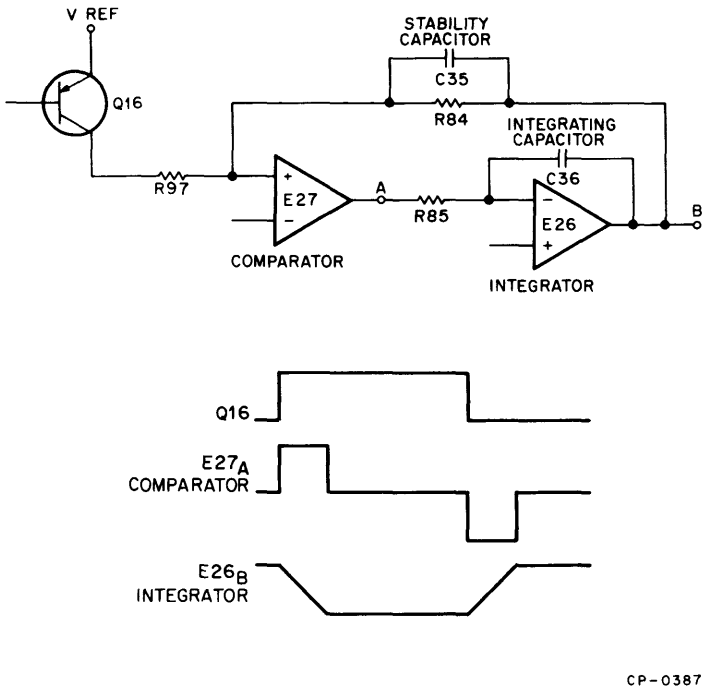


Figure 4-11 Simplified Control Motor Servo System

4.6.1.1 Ramp and Reference Generator – For a read/write speed, forward operation, MOVE A H is ANDed with REV L (high) at the upper E29 gate (Figure A-5) to apply a turn-on bias to the base of transistor Q16. With Q16 conducting, a positive voltage from the +4 Vdc V REF signal is applied to the non-inverting (+) input of comparator E27. This positive voltage causes E27 to saturate and apply a positive voltage to integrator E26 (see figure). The output of E26 is a negative ramp signal with a time constant determined by R85 and C36. This negative ramp signal is then fed back through R84 to decrease the positive comparator input to zero volts. With the comparator input at zero volts, the RAMP A signal at TP25 is precisely controlled by the comparator at 75 percent of the voltage at TP32. When MOVE A H goes low, the comparator saturates in the opposite direction, causing the integrator output to ramp to zero volts. This zero volt output is again precisely maintained by the comparator.



Reverse operation is similar to the forward operation except that the positive voltage from the V REF signal is now applied to the negative input of the comparator (Figure A-5). The resultant positive ramp signal from the integrator is then fed back to the positive comparator input, thereby equalizing the negative and positive comparator inputs.

For a search speed operation, HIGH SPEED H is applied through an inverter to turn on transistor Q23. With Q23 conducting, a larger positive voltage from the +12 Vdc V REF signal is applied to the comparator. This larger positive input results in a higher reference voltage; however, the ramp and reference generator operation is identical to the read/write speed operation.

Potentiometer R143 adjusts the actual speed of the motor by varying the desired speed reference level into the error signal amplifier.

NOTE

During forward operations, the comparator saturation voltage and the input reference voltage (V REF) are obtained from the same positive regulated supply. Hence, no adjustment of the acceleration ramp time is necessary. However, the deceleration ramp time is obtained jointly from both the positive and negative supplies and thus, to obtain the correct deceleration ramp slope, an adjustment of the negative regulated supply is required.

4.6.1.2 Tachometer Circuit – In a closed loop servo system, a speed sensing, feed-back control signal is required to prevent uncontrolled motor velocity. In the TU60, this control or tachometer signal is electronically derived in the tachometer circuit. The tachometer circuit (Figure A-5) consists of operational amplifier E25, resistors R92, R93, R94, R95, Tach Pot A, and a 1.5-ohm wirewound copper resistor which is in parallel with Tach Pot A.

NOTE

To minimize the effects of temperature changes, the 1.5-ohm resistor is composed of copper to match the thermal coefficient of resistance of the armature.

With Tach Pot A adjusted correctly, the various components in the tachometer circuit operate as a balanced bridge circuit (Figure 4-12). To initiate forward tape motion, a negative voltage from the power amplifier is applied to the control motor winding. Since the motor is not turning at this time, the bridge is balanced and equal voltages appear at both center taps of the bridge. With this circuit condition, the differential input to the tach amplifier is zero, resulting in a zero volt output at TP19. When the motor starts to turn, a back emf is created, which unbalances the bridge and generates a positive TACH AMP A signal at TP19. As the motor speed increases, the TACH AMP A signal increases and conversely, if the motor speed decreases, the TACH AMP A signal also decreases.

Since different motors have slightly different armature resistances, Tach Pot A is used to electrically balance the bridge with the various motors that may be used. When Tach Pot A is adjusted correctly (approximately two-thirds of its travel), the magnitude of the amplified TACH AMP A signal is directly proportional to the motor speed. The entire servo circuit is designed to operate properly even with a slight misadjustment of the Tach Pot A setting. However, if the setting is too low, the motor speed decreases noticeably as the load increases, and the drive sprocket will not have a stiff feel. (Refer to the electrical adjustments in Chapter 5.) If the setting is too high, the motor will creep or oscillate.

During forward motion, the tape tension is maintained by simultaneously applying a small amount of reverse torque to the tension motor. During reverse motion, the tachometer circuit operates in a similar manner; however, a positive voltage is applied to the control motor winding, which causes the control motor to rotate in the opposite direction. When this occurs, the bridge unbalances in the opposite direction and a negative TACH AMP A signal is produced. To move the tape backwards, a greater amount of reverse torque is applied to the tension motor, thus causing the reverse reel to attempt to rotate faster than the control reel can unwind the tape. These reel conditions effectively maintain the correct tape tension in the reverse direction.

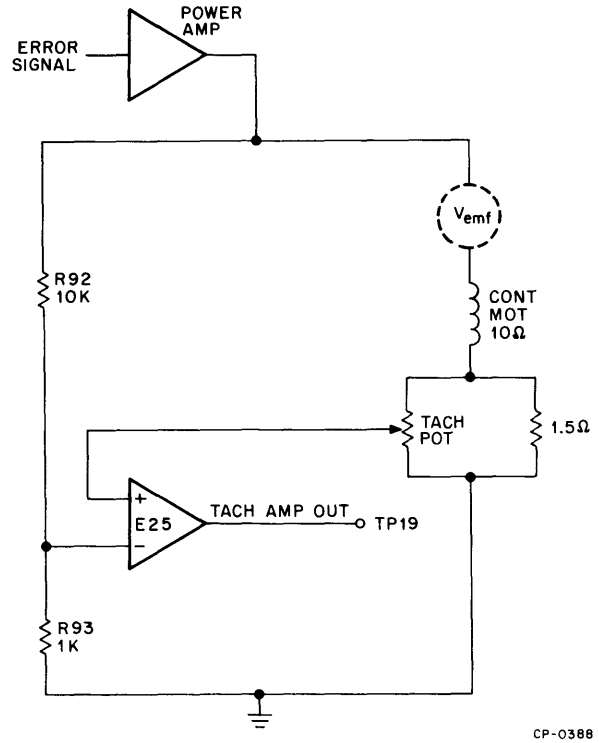


Figure 4-12 Tachometer Circuit

4.6.1.3 Error and Power Amplifiers – During the initiation of tape motion, the acceleration ramp signal is applied to the non-inverting input (+) of error amplifier E24 (Figure A-5). The E24 output is then coupled to a power amplifier consisting of Q25, Q26, Q37, and Q38. The power amplifier has a net gain of one, and a ±.6V threshold level. The output of the power amplifier is then applied to the control motor to allow starting current to flow through the motor armature. As the motor accelerates to the desired speed, the TACH AMP A signal is summed with the desired speed signal at the input to E24. This action reduces the input level of E24, thus reducing the current through the motor and subsequently slowing the motor acceleration. When the motor velocity equals the desired speed, the TACH AMP A signal balances the desired speed signal, hence, further acceleration is inhibited and a constant motor velocity is maintained. As the tape winds onto the take-up reel, the additional load tends to slow the control motor. When this occurs, the TACH AMP A signal decreases, unbalancing the sum junction and applying more current through the motor armature to increase the motor speed. Conversely, if the motor speed increases, the TACH AMP A signal increases to decrease the motor speed.

If the tape is stopped at BOT or EOT, the signal LDR H is present. This signal, applied through an inverter, turns on Q39 and prevents Q38 from conducting. With Q38 off, current through the motor is limited to a level determined by R182 and Q25. This circuit configuration permits reverse tape motion to occur at the EOT leader; however, if a Reverse command is issued at the BOT leader, tape counter winding onto the tension reel is prevented due to the reduced current through the armature.

4.6.2 Tension Motor Control Circuit

During a forward or reverse operation, the tension motor operates in conjunction with the control motor to maintain the proper tape tension. However, during a rewind operation, the tension motor operates independent of the control motor to rewind the tape at a controlled rate (100–150 ips).

When performing a forward operation, REV L is high. This signal, applied through an inverter (Figure A-5), disables the upper E18 gate to turn off Q23 and Q14. Since a rewind operation is not being performed, REWIND A L (high), ANDed with LOADED A H, produces READY A L. This signal turns on transistor Q11 to couple +5V through diode D18, applying +4V to the tension motor armature. With +4V applied to the tension motor, low torque reverse motion is produced.

When performing a reverse operation, REV L, applied through the inverter, enables the upper E18 gate which turns on transistors Q13 and Q14. With these transistors conducting, D18 is reverse biased and +12V is applied to the tension motor to produce high torque reverse motion.

When performing a rewind operation, the tension motor control circuit operates as a balanced bridge circuit (Figure 4-13). REWIND A H, ANDed with LOAD A H, applies ground to point A. With point A at ground, transistor Q12 is biased into conduction by the positive voltage from the +5V source on its base. With Q12 conducting, base current is applied to Q13 and Q14, thus supplying a large positive voltage to point B.

As the motor accelerates, a back emf is created that reduces the Q12 base bias at point C. This action reduces the Q12 conduction and hence reduces the voltage at point B. By the time the motor has obtained the rewind speed, the voltage at point B is too low to allow further acceleration, and hence a constant velocity is maintained.

As the tape rewinds onto the tension reel, the additional load tends to slow the motor. When this occurs, the back emf decreases, increasing the voltage at point C. This in turn increases the voltage at point B, applying more current through the armature to maintain a constant velocity for the increased reel load.

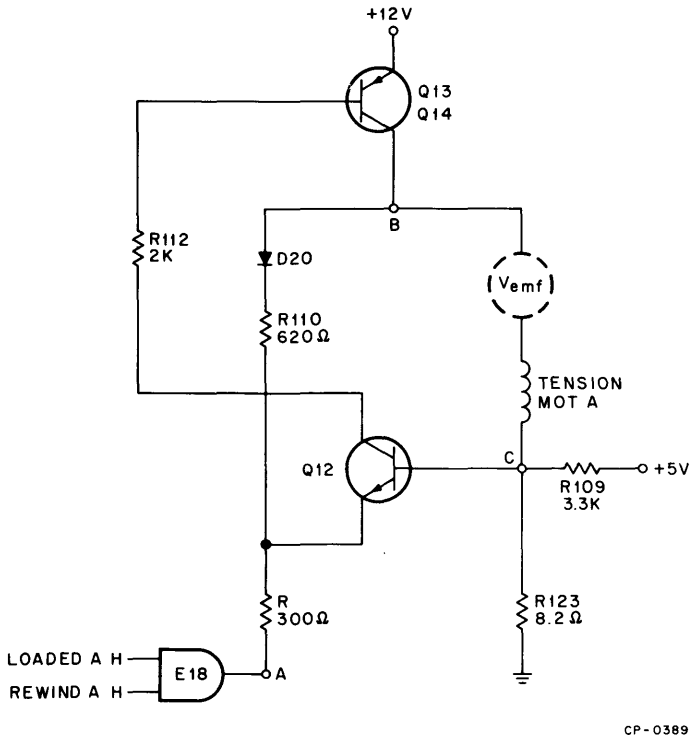
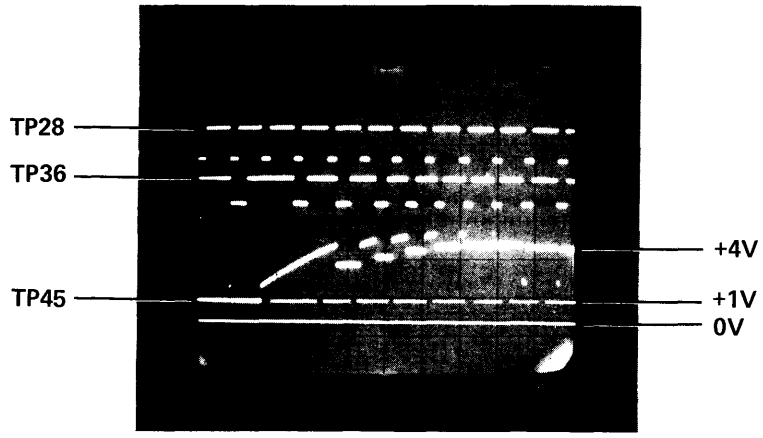


Figure 4-13 Rewind Control Circuit

4.6.3 Phase Lock Loop

The phase lock loop (Figure A-7) synchronizes the read clock pulses (CLK 1 and CLK 2) with the bit cell frequency from the tape. This circuit consists of: a phase detector E44, a voltage controlled oscillator (VCO) E45, and a transistor amplifier Q24. Initially, without an input from the tape (PEAKS L pulses) at pin 1 of the phase detector, +1V is produced at TP45 to maintain an approximate 20 kHz output from the VCO.



During a read operation, WRITE H (low) is applied through an inverter to enable E31 and supply the 20 kHz VCO output to the divide-by-eight E38 counter. The resultant 2.5 kHz reference signal is then fed back to pin 3 of the phase detector. As tape moves across the read/write head, negative PEAKS L pulse generated by the preamble are applied to pin 1 of the phase detector. The 2.4 kHz reference signal is then compared in the phase detector to the incoming PEAKS L pulses. Since the PEAKS L pulses occur at a higher frequency than the initial reference frequency, the PEAKS L pulses lead the reference signal. This condition causes pin 13 of the phase detector to go low, causing pin 5 to also go low for the duration of the time difference between signals (see figure).

The low on pin 5 is then coupled through transistor Q24 to pin 9 of the phase detector. With pin 9 low, the output at pin 8 is a positive ramp signal with a time constant determined by R6 and C47. This positive ramp is applied through R153,C44 to balance the sum junction of the base of transistor Q24. This positive voltage is also coupled to pin 12 of the VCO to slew up the VCO frequency until the reference frequency matches the tape frequency.

NOTE

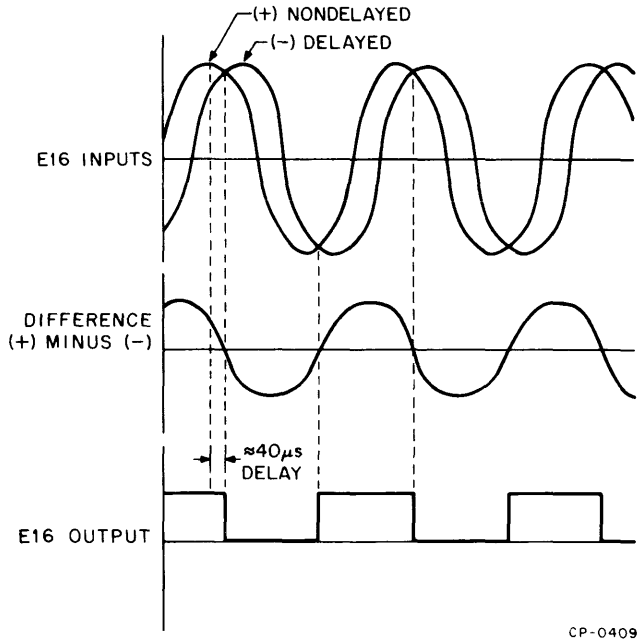
Since the phase detector operates only on the negative signal transitions, when the frequencies are matched, the phase relationship is also matched.

If, while the tape is in motion, the PEAKS L signal lags the reference signal (tape frequency lower than the reference frequency), pin 2 of the detector goes low, causing pin 10 to go high for the duration of the time difference between signals. With pin 10 high, the pin 8 output is decreased, thus reducing the VCO frequency.

When the reference frequency matches the phase and frequency of the PEAKS L pulses, the voltage at TP45 is approximately +4V. This positive voltage is controlled by the phase detector to keep the VCO frequency locked at exactly 8 times the bit cell frequency. When locked, the nominal VCO frequency is 35 kHz and the divide-by-eight reference frequency is approximately 4.5 kHz.

4.6.4 Peak Detector

The peak detector (Figure A-7) converts the sinusoidal read waveform into a square-wave with transitions that occur at the sine wave peaks. This circuit consists of: a differential voltage comparator E20, an inductive delay network L1,C24, and an inverter E28. During a read operation, the read sine wave is applied directly to the (+) comparator input and through delay network L1,C24 to the (-) input. Hence, the (-) comparator input is delayed by approximately 40 μs (see figure). Both inputs are then subtracted in the comparator to produce a square-wave output with transitions that occur slightly later than the nondelayed sine wave peaks.



4.7 POWER SUPPLY

The H751 Power Supply, located in the rear of the TU60 chassis, is composed of a +15 and -15 Vdc series regulated supply and a +5 Vdc series regulated supply. With the use of separate line cord breaker assemblies, the H751 can operate from either 115 or 230 Vac (50/60 Hz) input line voltage. For 115 Vac operation, line cord breaker assembly BC05H connects the dual primaries of the input transformer (Figure A-8) in parallel. For 230 Vac operation, line cord breaker assembly BC05J must be installed to connect the transformer dual primaries in series. With either transformer configuration, 115 Vac is maintained across each primary. The applicable H751 specifications are as follows:

SIZE	10-1/2 in. long 5-1/8 in. wide 5 in. high
INPUT VOLTAGE	95–130 Vac @ 50/60 Hz 190–260 Vac @ 50/60 Hz
POWER DISSIPATION	100W max
REGULATED OUTPUTS	+5 ± 0.25 Vdc, 4A, 50 mV ripple @ full load +15 ± 1.4 Vdc, 2.5A, 300 mV ripple @ full load -15 ± 1.4 Vdc, 2.5A, 300 mV ripple @ full load * +12, +2-1 Vdc, 100 mV ripple -12, ± 1.5 Vdc, 300 mV ripple

4.7.1 +15 and -15 Vdc Supply Operation

When the power supply is activated, a full-wave rectifier, located on BR1, converts the ac transformer output to positive pulsating dc. Filter capacitor C2 removes most of the dc pulses and applies about 25 Vdc through series resistor R2 to the diode voltage regulator. Here, Zener diodes D1 and D2 plus temperature compensating diodes D3 through D6 maintain +16 Vdc at the base of current amplifier Q5. The +15.5 Vdc at the emitter of Q5 is further reduced by Q2 to +15 Vdc. This 15 Vdc is then applied through 3A fuse F1 to a series regulator on the rewind logic (Figure A-6), where the voltage is regulated to +12 Vdc in a similar manner as the +5 Vdc regulation described in Paragraph 4.7.2. Buffer capacitor C7 of the power supply discharges into the external load whenever the voltage input from the full-wave rectifier swings below +16 Vdc. The 3A series fuse furnishes overcurrent protection for the supply.

The -15 Vdc supply operates in a similar manner as the +15 Vdc supply; however, reverse biasing for the negative regulator requires a PNP transistor (Q6) and a slightly different circuit configuration to produce the -15 Vdc output.

4.7.2 +5 Vdc Supply Operation

The +5 Vdc power supply is composed of the following operational circuits:

- a full-wave bridge rectifier and filter (BR2, C9 and C10)
- a series regulator (Q4)
- a reference voltage generator (D13, Q10 and Q11)
- a difference amplifier (Q8 and Q9)
- an overvoltage crowbar (D12).

When the power supply is activated, a bridge rectifier, located on BR2, converts the ac transformer output to pulsating dc. Filter capacitors C9 and C10 remove the pulsating dc, applying a positive dc voltage through 5A fuse F3 to the collector of series regulating transistor Q4. Zener diode D13 and transistors Q10,Q11 establish a constant +5 Vdc reference voltage at the base of Q9. Transistor Q8 compares the output voltage to the reference voltage and, if the external load fluctuates, Q8 generates a small error signal that is out-of-phase with the direction of the load fluctuation. This error signal is transmitted through current amplifiers Q7 and Q12 to the base of series regulator Q4; increasing or decreasing Q4 conduction and thus maintaining an essentially constant output voltage. If a severe overvoltage condition occurs, excessive current through D12 triggers the overvoltage SCR (Q1) into conduction, applying ground to the output terminal and causing the 5A fuse to open.

*These voltages are controlled by the 12V regulator on the M7761 module (Figure A-6).

4.7.3 Power Clear Circuit

During the initial power-up phase, the power clear circuit (Figure A-7) accomplishes the following:

- disables the write circuits to inhibit any erroneous write operations
- presets the Dir flip-flops to force an "end leader" indication if the tape is at either clear leader
- resets the Rewind one-shots to prevent a spontaneous tape rewind.

Application of power to the TU60 supplies +5V through a 220-ohm resistor to charge a 150-microfarad capacitor. While the capacitor is charging (approximately 30 ms), transistor Q20 is held cut-off, keeping Q19 cut-off and also generating the internal control signal PWR CLR H. With Q19 off, the head driver circuits are disabled, preventing spurious noise from causing a write operation.

PWR CLR H, applied through a NAND gate (Figure A-5), produces LOADED A H (low). This signal, when applied to the rewind logic (Figure A-6), sets the Dir A flip-flop. If the tape is at either leader when Dir A is set, only the "end leader" indication is produced. (If this is the case, before normal tape operations can be initiated, a rewind operation must first be performed even though the tape may actually be at the BOT.) Simultaneously, PWR CLR H is also applied through a NOR gate to reset the Rewind one-shot and thus inhibit a spontaneous rewind operation during the initial power application.

Approximately 30 milliseconds after the initial power application, the 150-microfarad capacitor (Figure A-7) has charged to approximately +4.1V. When this occurs, the Zener diode conducts to turn on Q20 and ground the PWR CLR H signal. This action removes the PWR CLR H signal, however, by this time, power is fully applied and the transport logic circuits have stabilized.

CHAPTER 5
MAINTENANCE

5.1 RECOMMENDED TOOLS AND TEST EQUIPMENT

Table 5-1 lists the recommended tools and test equipment that are to be used with the standard tools for proper maintenance of the TU60 Tape Transport.

5.2 PREVENTİVE MAINTENANCE

When the tape transport is operated in a normal office environment on an eight-hour system basis (four hours of actual transport operation), perform the preventive maintenance (PM) procedures as indicated in Table 5-2. An abnormally dirty environment or a greater transport operation time may require more preventive maintenance than that indicated in the schedule. During the PM procedures, unless specifically indicated, do not alter any adjustments on drives that are performing satisfactorily.

To obtain maximum performance and reliability from the TU60 DECassette Tape Transport, observe the following operating precautions and practices:

1. Before using a new cassette, or prior to using a cassette that has just been accidently dropped:

    a. Load the cassette on a drive and press the REWIND pushbutton to perform a rewind operation.

    b. Remove the cassette, turn it over, and perform another rewind operation.

    This is done to pack the tape neatly in the cassette and also to place the full tape reel at the proper operating tension.

2. Do not expose the cassette to excessive heat (Table 1-1) or dust. Since most tape soft errors are caused by dust or dirt, it is imperative that the tape be kept clean.

3. When not in use, store the cassettes in the plastic storage boxes or other sealed containers.

4. To prevent accidental exposure of the tape oxide to foreign matter, always rewind the tape to the BOT clear leader and then press the REWIND pushbutton again before removing the cassette from the drive.

Table 5-1
Recommended Tools and Test Equipment

Equipment	Manufacturer and Model/Part No.
Multimeter	Triplett 310 or Simpson 360
Oscilloscope	Tektronix 453
Oscilloscope Probes	
Voltage (X10-2 required)	Tektronix P6010
Current	Tektronix P6019 clip-on with passive terminator
Field Service Tool Kit	DEC 29-18303
Spline Key Kit (size 0.48)	Bristol Co. SS-408, DEC 29-16131
TU60-K Cassette (2 required)	DEC 36-11226
TU60-R Speed/Skew Reference Cassette (1 required)	TU60-R
General Purpose Cleaner (non-flammable)	
Magnetic Head Cleaner	Miller Stephenson, MS-200 (or equivalent)
Cotton Swabs	DEC 90-08436
Soft Clean Cloths	
Vacuum Cleaner	
Cassette Drive Coupling (3 mm)	DEC 12-11279
Cassette Tension Motor	DEC 12-11111
Control Motor Assembly	DEC 70-09139
Spindle Assembly	DEC 70-09146
Fan Filter	DEC 12-11343
DEC-O-LOG	ECO log and computer on-line synopsis

Table 5-2
Preventive Maintenance Schedule

Quarterly PM (250 Hours*)	Semi-Annual PM (500 Hours*)	Annual PM (1000 Hours*)	Biennial PM (2000 Hours*)		Estimated Performance Time (minutes)
X	X	X	X	Clean tape heads and guides	2
			X	Check tape guides for wear; rotate if worn	1
X	X	X		Clean spindle assembly	
	X	X	X	Install F-coded ECOs as required	20
	X	X	X	Clean interior and exterior of equipment	
X	X	X	X	Clean fan filter; replace if necessary	
	X	X	X	Inspect wiring and components	
		X	X	Check regulated power supply voltages	2
			X	Replace tension motor	30
			X	Replace control motor assembly	
			X	Replace control spindle assembly	
			X	Coarse tachometer check	2
		X	X	Servo loop adjustment	25
		X	X	Head azimuth check	2
		X	X	-12 Vdc regulator (deceleration ramp) check	5
			X	Timing checks and adjustments	35
X	X	X	X	Run MAINDEC diagnostic programs	60

*Times are equivalent to 4 hours of TU60 operation during an 8-hour system day.

5.2.1 Quarterly PM (250 hours)

1. Clean the tape heads and guides using the appropriate head cleaner and a soft, lint-free cloth or cotton swab.

CAUTION
Do not allow the head cleaner fluid to contact the tape surface as this will destroy the protective coating.

2. Inspect the spindle assembly on each drive. On the rubber wheel cleaning is required, use a small brush and non-flammable cleaner.

3. Remove the fan filter and clean it with a mild liquid detergent (e.g., Ivory) and warm water. Rinse the filter in clear water, squeeze dry, and reinstall.

4. Run the appropriate MAINDEC diagnostic programs as described in the diagnostic descriptions.

5.2.2 Semi-Annual PM (500 hours)

1. Consult the DEC-O-LOG and review the ECO status of each drive. Install any outstanding F-coded ECOs.

2. Clean, inspect, repair, replace, or adjust the following items:

    a. Inspect the transport interior and exterior for cleanliness.

    b. Check the fan for proper operation and cleanliness.

    c. Clean the fan filter (Paragraph 5.2.1, Step 3).

    d. Inspect the wiring, lamps, and components for defects.

    e. Inspect the spindle assembly for wear or dirt. Clean the spindle (Paragraph 5.2.1, Step 2) or replace it (Paragraph 5.2.4, Step 3) as necessary.

    f. Clean the tape heads and guides with the appropriate head cleaner (Paragraph 5.2.1, Step 1).

3. Run the appropriate MAINDEC diagnostic programs as described in the diagnostic descriptions.

5.2.3 Annual PM (1000 hours)

1. Consult the DEC-O-LOG and review the ECO status of each drive. Install any outstanding F-coded ECOs.

2. Clean, inspect, repair, replace, or adjust the following items:

    a. Inspect the transport interior and exterior for cleanliness.

    b. Check the fan for proper operation and cleanliness.

c. Clean the fan filter (Paragraph 5.2.1, Step 3).

d. Inspect the wiring, lamps, and components for defects.

e. Inspect the spindle assembly for wear or dirt. Clean the spindle (Paragraph 5.2.1, Step 2) or replace it (Paragraph 5.2.4, Step 3) as necessary.

f. Clean the tape heads and guides with the appropriate head cleaner (Paragraph 5.2.1, Step 1).

3. Perform the following checks and adjustments:

   a. power supply voltage checks (Paragraph 5.3.1)

   b. servo loop adjustments (Paragraph 5.3.3)

   c. head skew check (Paragraph 5.3.4)

   d. -12 Vdc regulator check (Paragraph 5.3.5).

4. Run the appropriate MAINDEC diagnostic programs as described in the diagnostic descriptions.

5.2.4 Biennial PM (2000 hours)

1. Consult the DEC-O-LOG and review the ECO status of each drive. Install any outstanding F-coded ECOs.

2. Clean, inspect, repair, replace, or adjust the following items:

   a. Inspect the transport interior and exterior for cleanliness.

   b. Check the fan for proper operation and cleanliness.

   c. Clean the fan filter (Paragraph 5.2.1, Step 3).

   d. Inspect the wiring, lamps, and components for defects.

   e. Clean the tape heads and guides (Paragraph 5.2.1, Step 1). If wear is evident on the guide, loosen the retaining screw, rotate the guide, and tighten the retaining screw.

3. Replace the control motor assembly, cassette tension motor, and spindle assembly as follows:

   a. Use an appropriate hex-head wrench to remove the three mounting bolts on the rear of each drive. (When the drive is separated from the TU60 front chassis, the cable length on the Berg connector is sufficient to allow access to each drive.)

   b. Remove the five Phillips-head screws adjacent to the reel couplers and remove the screw, located next to the tape-loaded microswitches, from the front of the drive. This allows removal of the control motor assembly, cassette tension motor, and spindle assembly.

   c. Detach the spring on the control motor and re-use the spring when the new motor is installed.

d. Mark and disconnect the wires for the control and tension motors from the drive terminator module.

e. Install the new tension motor and the new spindle assembly; then install the new control motor assembly.

f. Connect and solder the power leads to each motor and replace the control motor spring.

4. Perform the following checks and adjustments:

a. power supply voltage checks (Paragraph 5.3.1)

b. coarse tachometer check (Paragraph 5.3.2).

CAUTION

Perform the coarse tachometer check after the new control motor has been installed to ensure that any large oscillations in the motor do not cause overheating and damage.

c. servo loop adjustments (Paragraph 5.3.3)

d. head azimuth check (Paragraph 5.3.4)

e. -12 Vdc regulator check (Paragraph 5.3.5)

f. write file gap one-shot (Paragraph 5.3.6)

g. gap time one-shot (Paragraph 5.3.7)

h. threshold (Paragraph 5.3.8)

i. signal one-shot (Paragraph 5.3.9)

j. tape blank one-shot (Paragraph 5.3.10).

5. Run the appropriate MAINDEC diagnostic programs as described in the diagnostic descriptions.

5.3 ADJUSTMENT PROCEDURES

The following adjustment procedure is written for the Rev D etch, or later, M7761 Servo and Read Write Module. The same procedure will work with the Rev C etch; although all TP numbers are changed, the mnemonic remains unchanged. A test point conversion chart for the M7761 Servo and Read Write Module is presented at the beginning of Appendix A, Reference Drawings.

All measurement setups given are for the actual oscilloscope setting, assuming a X10 probe is to be used. All measurements, unless otherwise stated, will be made with the Channel 1 probe and the CH mode switch in the CH 1 position.

5.3.1 Supply Voltages

Verify all five supply voltages before attempting to set up the TU60.

1. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Auto Trigger
A Sweep Time	2 ms/div
CH1 Gain	See Table 5-3, dc
Trigger	Free Running

2. Measure voltage according to Table 5-3.

Table 5-3
Voltage Check

Designation	Measuring Point	CH1 Gain Setting	Voltage Specification
+15 Vdc	J7-pin 1 on M7761	.5 V/div	+15 ± 1.4 Vdc, 300 mV ripple
-15 Vdc	J7-pin 2 on M7761	.5 V/div	-15 ± 1.4 Vdc, 300 mV ripple
+5 Vdc	J7-pin 4 on M7761	.1 V/div	+5 ± .25 Vdc, 50 mV ripple
+12 Vdc	TP46 on M7761	.5 V/div	+12, +2-1 Vdc, 100 mV ripple
-12 Vdc	TP47 on M7761	.5 V/div	-12, ± 2 dc* 100 mV ripple

*If this voltage is out of tolerance, refer to Paragraph 5.3.5.

5.3.2 Coarse Tachometer Adjustment

This adjustment is done to prevent motor damage on a completely out of adjustment servo; under normal conditions it need not be done.

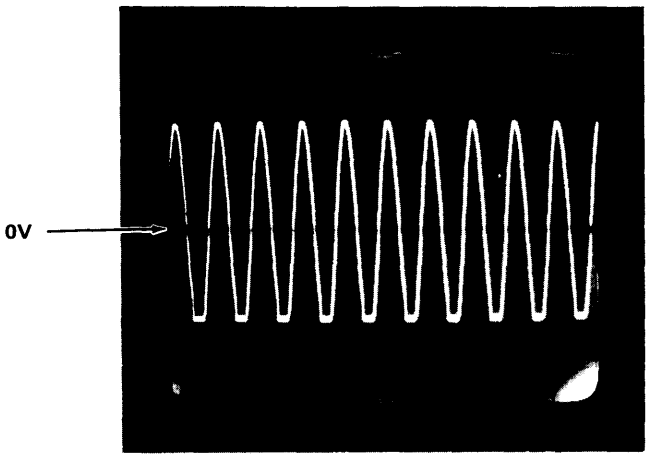
1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

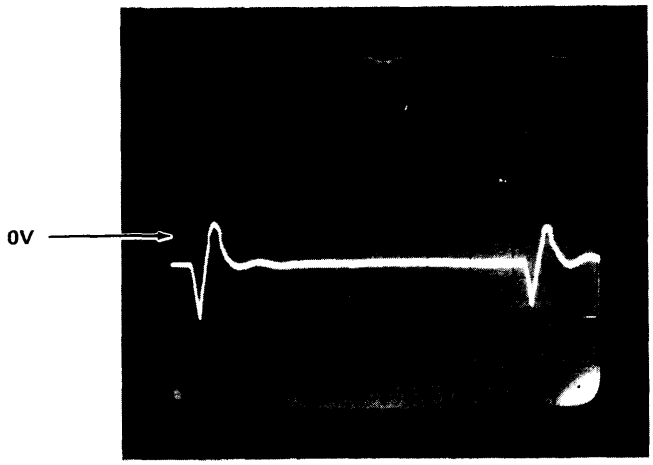
Horiz Display	A
A Sweep Mode	Auto Trigger (free running)
A Sweep Time	2 ms/div
CH1 Gain	.2 V/div (X10 probe), dc

3. Connect the oscilloscope probe to TP20 (AMP A) of the M7761 module and observe the oscilloscope display for oscillations or creep (Figure 5-1). If oscillations or creep are present, adjust Tach Pot A (located on the drive terminator module, Figure 5-3), counterclockwise until the oscillations stop (no ac signal); then adjust Tach Pot A another two turns counterclockwise.

4. Connect the oscilloscope probe to TP9 (AMP B) and repeat Step 3, adjusting Tach Pot B, (located on the drive B terminator module).



(A) Tach Oscillations



(B) Creep

Figure 5-1 Coarse Tachometer Adjustments

5.3.3 Servo Loop

To prevent interaction of the servo adjustments, simultaneously adjust the drive A and B servo loops according to the following paragraph sequence. Do not attempt any individual adjustments unless the previous adjustments have first been checked. Table 5-4 lists the servo adjustments in the sequence that they must be performed. Ensure that both drives are configured as indicated for the adjustment being performed.

Table 5-4
Servo Loop Adjustments: Summary

Adjustments	Drive Configuration	Tape Motion	Scope Setting	Test Points	Indications
Coarse Speed (Speed Pot) (5.3.3.1)	A and B Loaded	Read	2 ms @ .1V, free running	TP24 (Speed A) TP11 (Speed B)	-2.7 ± 0.5 Vdc
Solenoid (5.3.3.2)	A and B Unloaded	Read	5 ms @ 10 mV	Across Tach Pot	-275 to -325 mV
Balance* (Balance Pot) (5.3.3.3)	Only Opposite Drive Loaded	None	5 ms @ 20 mV, free running	TP20 (AMP A) TP9 (AMP B)	0V ± .2V
Fine Tach* (Tach Pot CW-CCW) (5.3.3.4)	A and B Loaded	Read	10 ms @ .2V, pos int	TP20 (AMP A) TP9 (AMP B)	Adj CW for oscillations, then back-off 1-1/4 turns.
Fine Speed* (Speed Pot) (5.3.3.5)	A and B Loaded-ref cassette on drive to be adj.	Read	2 ms @ .2V, pos int	TP2 (AMP 2 OUT)	Adj. for pulse interval marked on ref tape label.

*Drives must be mounted to chassis when these adjustments are performed.

5.3.3.1 Coarse Speed

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Auto Trigger (free running)
A Sweep Time	2 ms/div
CH1 Gain	.1 V/div, dc

   Connect the oscilloscope probe to TP24 (Speed A) of the M7761 module.

3. Use the appropriate tape motion routine listed in Paragraph 5.4.1 or 5.4.3 and perform a read operation on drive A.

4. Adjust Speed Pot A for -2.7 ± 0.5 Vdc oscilloscope indications.

5. Connect the oscilloscope probe to TP11 (Speed B) and repeat Steps 3 and 4 for drive B, adjusting Speed Pot B.

5.3.3.2 Control Motor Solenoid

1. Unload the cassette from both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Auto Trigger (free running)
A Sweep Time	5 ms/div
CH1 Gain	10 mV/div

3. Connect the oscilloscope probe and the probe ground across the two test points (TP2 high, TP1 gnd) on the edge of the terminator module located beneath drive A. On earlier models without test points, connect the probe ground to G (gnd) on the terminator module. Connect the oscilloscope probe to the red lead on the control motor (lower motor).

NOTE

Be careful not to affect motor position or cause side to side motion with oscilloscope probe.

4. Use the appropriate tape motion routine listed in Paragraph 5.4.1 or 5.4.3 and perform a continuous read operation.

5. Cover the EOT photosensor and press one of the cassette loaded microswitches. The lower spindle should be rotating at approximately read speed.

6. Monitor the scope display for a -275 to -325 mV average dc indication (Figure 5-2). If the voltage is not correct, loosen the two solenoid screws (Figure 5-3) and slide the solenoid up or down until the proper voltage is obtained. (Access to screws on both drives can be made by removing drive A from the frame.)

7. Repeat Steps 3 through 6 for drive B.

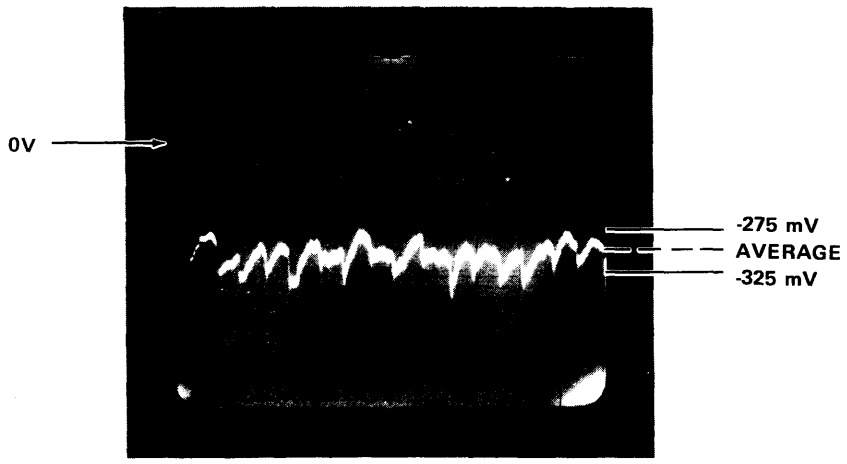


Figure 5-2 Control Motor Solenoid Adjustment

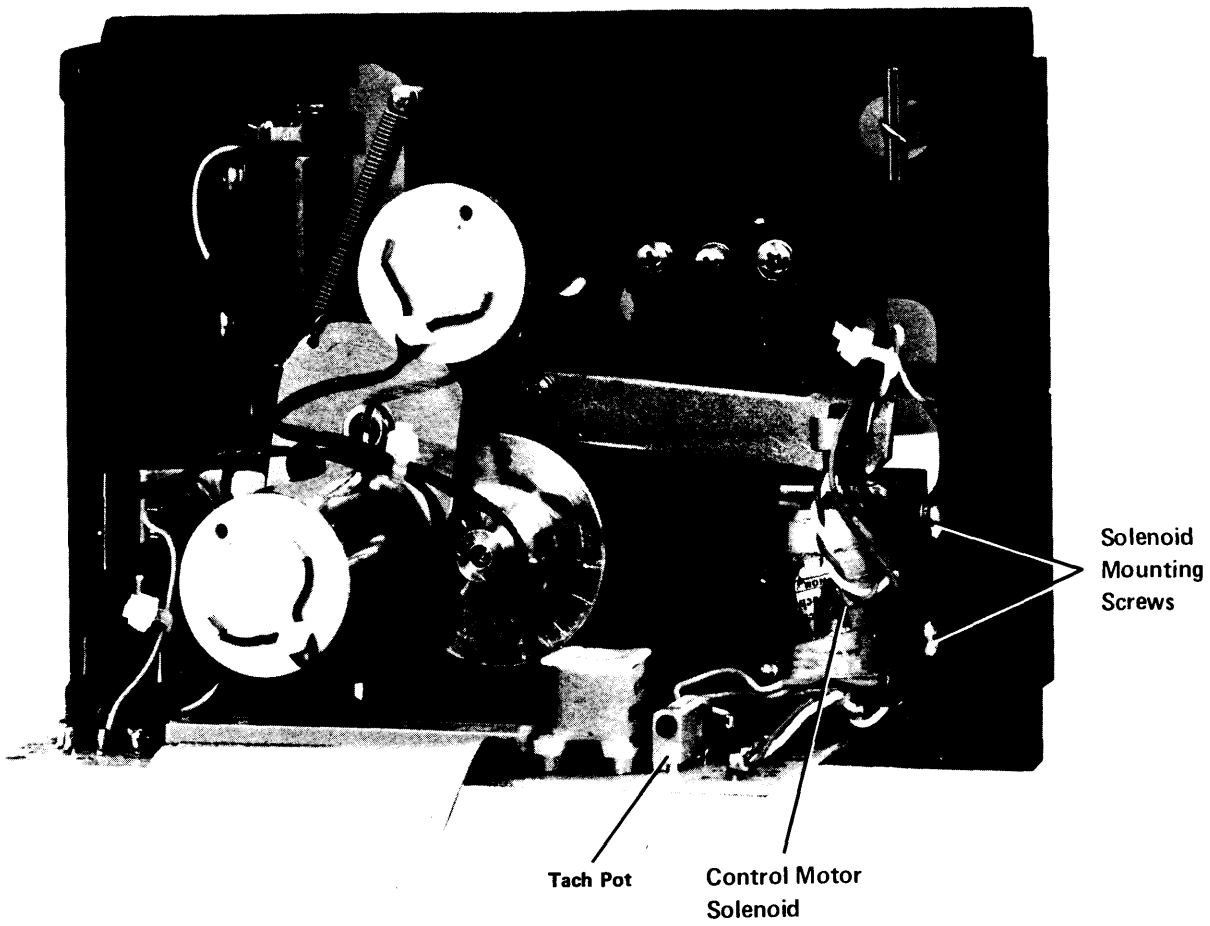


Figure 5-3 Solenoid Mounting Screws

5.3.3.3 Balance

NOTES

1. **Drive must be mounted in frame and chassis for all the following adjustments.**

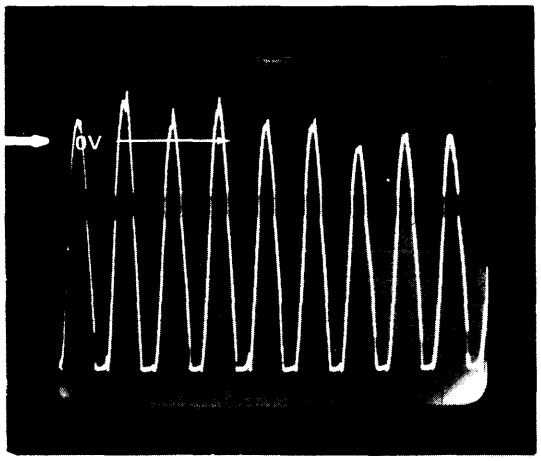
2. **Load a cassette into the drive opposite the one to be tested (e.g., drive A to be tested: drive A empty; drive B loaded).**

1. Load a cassette into drive B.

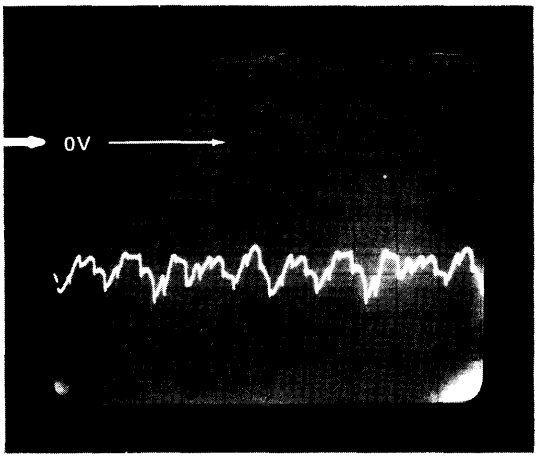
2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Auto Trigger (free running)
A Sweep Time	5 ms/div
CH1 Gain*	20 mV/div, dc

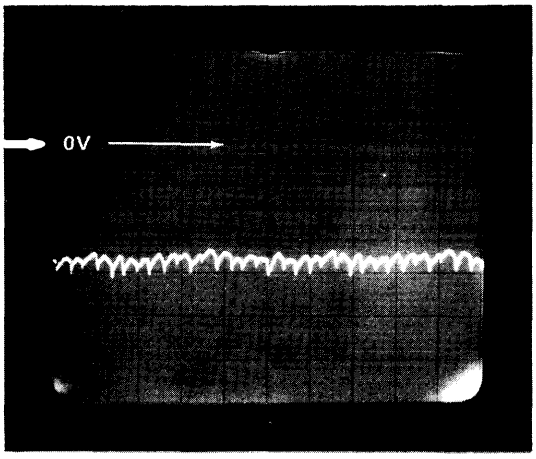
*Oscilloscope grounded on TP13 on REV D etch or later, and on crystal holder on REV C, M7761.



(A) Oscillations



(B) Back Off Point Where Oscillations Stop



(C) Final Adjustment

Figure 5-4 Fine Tachometer Adjustments

3. Connect the oscilloscope probe to TP20 (AMP A) and adjust Bal Pot A for a 0V ± 200 mV oscilloscope indication.

4. Remove the cassette from drive B and load it into drive A.

5. Connect the oscilloscope probe to TP9 (AMP B) M7761 and adjust Bal Pot B for 0V ± 200 mV indication.

5.3.3.4 Fine Tachometer Adjustment

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Auto Trigger (free running)
A Sweep Time	10 ms/div
Vertical Sensitivity	.2 V/div, dc

Connect the oscilloscope probe to TP20 (AMP A) of the M7761 module.

3. Use the appropriate tape motion routine listed in Paragraph 5.4.1 or 5.4.3 and perform a read operation on drive A.

4. Adjust Tach Pot A (located on the drive A terminator module) clockwise until oscillations occur (Figure 5-4A), then back off until they stop (Figure 5-4B). Then back off 1-1/4 more turns (Figure 5-4C).

5. Connect oscilloscope probe to TP9 (AMP B) and repeat Steps 3 and 4 for drive B, adjusting Tach Pot B (located in drive B terminator module).

5.3.3.5 Fine Speed

1. Load the Speed/Skew Reference Cassette (speed label out) into drive A and a cassette into drive B. Perform a manual rewind.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	.2 ms/div
CH1 Gain	.2 V/div, dc
A Trigger	CH1 only, SLOPE and LEVEL +, HF REJ, Int.

Connect the oscilloscope probe to TP2 (AMP 2 out) of the M7761 module.

3. Use the appropriate tape motion routine listed in Paragraph 5.4.1 and 5.4.3 and perform a read operation on drive A.

4. Adjust Speed Pot A until the interval between positive pulses equals 1 ms ± .05 ms or what is called out on the label of the speed/skew cassette. Waveform appears as shown in Figure 5-5.

5. Load the reference cassette into drive B and load cassette drive A.

6. Perform a manual rewind on drive B.

7. Perform a read operation on drive B and adjust Speed Pot B as in Step 4.

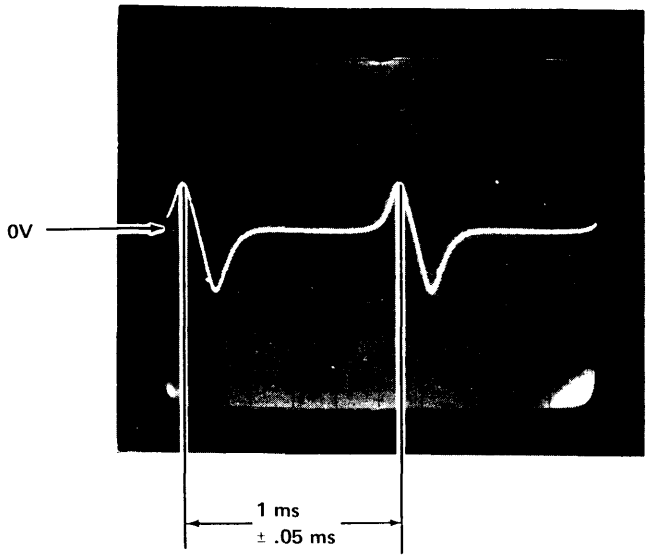


Figure 5-5 Fine Speed Adjustment

5.3.4 Head Skew

1. Load the Speed/Skew Reference Cassette into the drive to be adjusted (skew label out). Perform a manual rewind on the drive to be adjusted.

2. Set the oscilloscope controls as follows:

Sweep Time	0.2 ms/div
Vertical Sensitivity	20 mV/div
Trigger	Positive, HF REJ, normal trigger, internal – or auto trigger if necessary.

3. Use the appropriate tape motion routine listed in Paragraph 5.4.1 or 5.4.3 and perform a continuous read operation on the drive to be adjusted.

4. Connect the oscilloscope probe to TP2 (AMP 2 OUT) of the M7761 module and adjust the oscilloscope controls to attempt to obtain the waveform indicated in Figure 5-6.

5. Turn the head alignment screw (Figure 5-7) for a minimum peak-to-peak signal. Hold the cassette pressed back lightly to simulate the lower door action.

6. Remove the reference cassette.

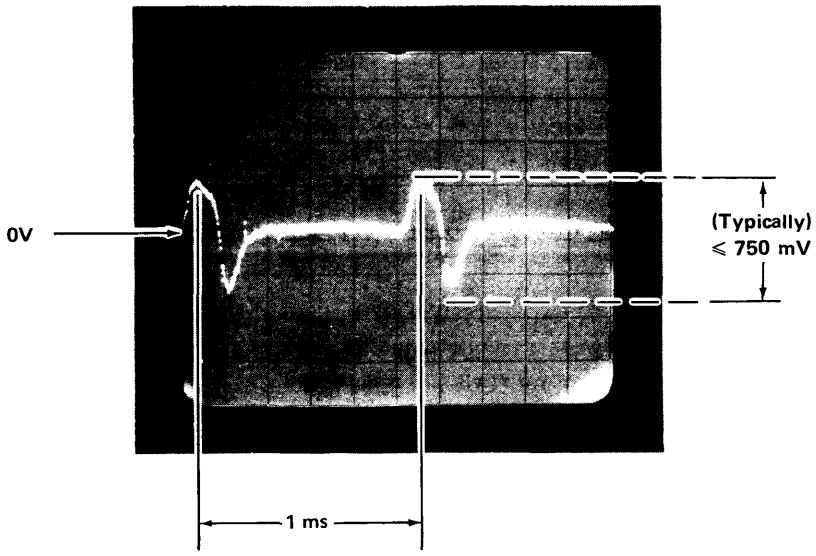


Figure 5-6 (Skew) Adjustment

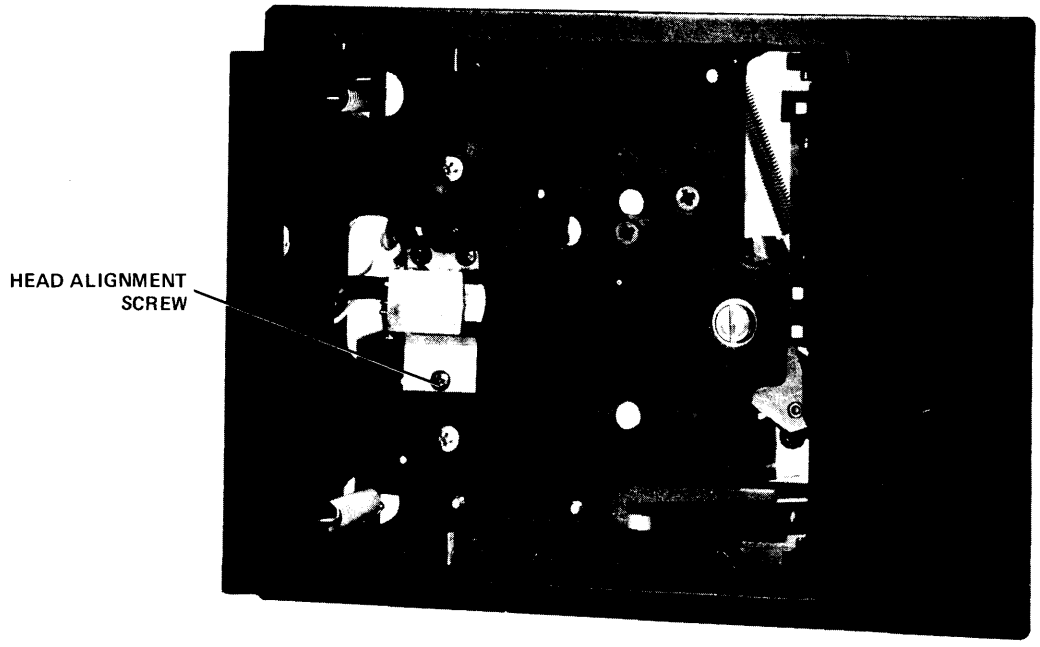


Figure 5-7 Head Skew Adjustment

5.3.5 -12 Vdc Regulator (Deceleration Ramp)

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A int. during B
A Sweep Mode	Normal Trigger
A Sweep Time	20 ms/div
CH1 Gain	.1 V/div, dc
A Trigger	CH1 only, SLOPE and LEVEL- HF REJ, Int.

   Connect the oscilloscope probe to TP25 (Ramp A) of the M7761 module.

3. Select drive A and use the appropriate Write Continuous Data Blocks diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to write one-byte data blocks (data = 0). Inhibit error printouts, loop on test sequence, and do not stop on error, switches should be up.

4. Adjust the oscilloscope controls to obtain the waveform indicated in Figure 5-8. Intensity and Delay Time Multiplier may have to be adjusted to obtain this waveform. Now expand the sweep by adjusting the oscilloscope as follows:

B Sweep Mode	B starts after delay time
B Sweep Time	5 ms/div

Switch the oscilloscope horizontal display to delayed sweep (B) and use the Delay Time Multiplier control to expand the appropriate portion of the waveform. Measure the negative slope time (X), add 2 milliseconds to this measurement, and record it.

Measure the positive slope (Y) and compare it to the recorded value previously obtained. If the Y slope does not equal the recorded value, adjust -12V Regulator Adjustment (RAMP) on the M7761 module until the Y slope equals the recorded value.

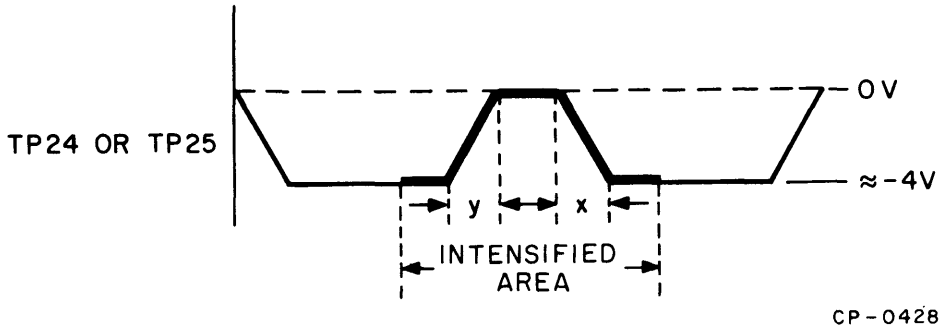


Figure 5-8 -12 Vdc Regulator Adjustment

5.3.6 Write File Gap One-Shot

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	0.1 sec/div
CH1 Gain	.2 V/div, dc
A Trigger	CH1 only, SLOPE and LEVEL +, LF REJ, Int.

Connect the oscilloscope probe to TP2 (WF GAPH) of the M7760 module.

3. Select drive A and use the appropriate WFG diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive Write File Gap operation. Inhibit error printout, do not stop on error, and pause between commands. Switches should be up.

4. Adjust the oscilloscope controls to obtain the waveform indicated in Figure 5-9. Ensure that the following adjustment is not made on the first file gap off the leader.

5. Adjust R12 (Pot A) on the M7760 module until t equals 535 ms ± 20 ms.

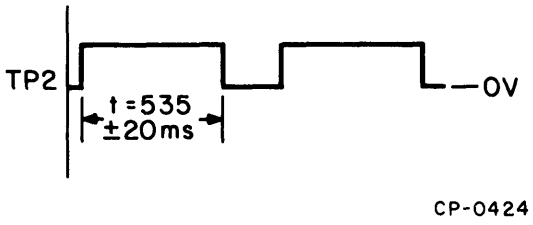


Figure 5-9 Write File Gap Waveform

5.3.7 Gap Time One-Shot

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	10 ms/div
CH1, CH2 Gain	0.2 V/div
A Trigger	CH1 only, SLOPE and LEVEL -, LF REJ, Int.
CH Mode	Chop

3. Select drive and use the appropriate Write Continuous Data Blocks diagnostic routine listed in Paragraph 5.4.5 or 5.4.4 to write one-byte data blocks (data = 0). Inhibit error printouts, do not stop on error, and loop on test sequence. Switches should be up.

4. Connect the Channel 1 oscilloscope probe to TP6 (drive L) and the Channel 2 probe to TP17 (GAP Time H) of the M7760 module. Adjust the oscilloscope controls to obtain the waveforms indicated in Figure 5-10.

5. Adjust R23 (Pot B) on the M7760 module until t equals 40 ± 2 ms (t_1 should equal 30 ± 5 ms).

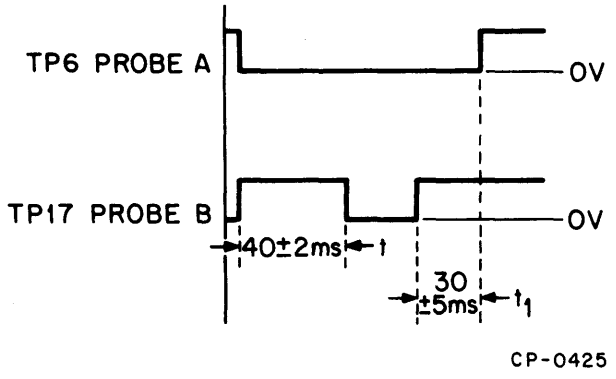


Figure 5-10 Gap Time Waveform

5.3.8 Threshold

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Format both cassettes A and B by using the appropriate Write Continuous Data Blocks diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to write the tapes with one-byte long (of 377 data) blocks. Start the program and record about ten seconds on each tape.

CAUTION

Since the tape speed and read signal amplitude varies as the tape winds up, this adjustment must be done at the beginning ten seconds of tape. A loop with the Test Sequence switch up will cause a rewind to occur at first error. This error will occur when the tape reads off the formatted ten seconds of Step 2 above, or at the first real error.

3. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	.2 ms/div
CH1 Gain	.1 V/div
CH2 Gain	.2 V/div
A Trigger	Positive, internal, HF REJ, CH1 only.
CH Mode	Chop

4. Connect the Channel 1 oscilloscope probe to TP33 (THRESHOLD DELAY) and the Channel 2 to TP31 (ENERGY H) of the M7761 module.

5. Use the appropriate Read Continuous Data Blocks diagnostic listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive read data block operations on drive A. Set switches for inhibit error printout, do not stop on error, and loop on test sequence. Adjust the oscilloscope controls to obtain the waveforms indicated in Figure 5-11. Trigger from Channel 1 as *close* to the base line (0V) as possible.

6. Adjust R142 (Threshold pot) on the M7761 module until t equals 1 ms ± 0.05 ms on drive A. Record the time t.

7. Repeat Step 5 for drive B.

8. Remeasure the time t. If t is now longer than on drive A, readjust as in Step 6 using drive B instead.

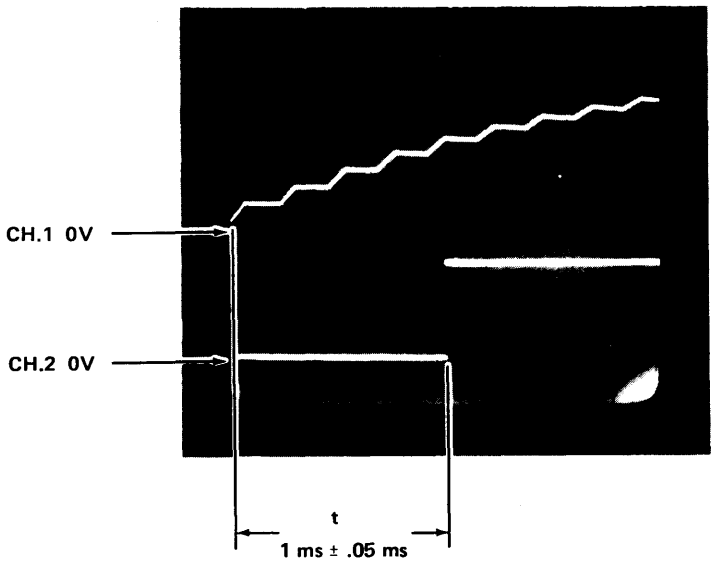


Figure 5-11 Threshold Waveform

5.3.9 Signal One-Shot

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Select drive A and use the appropriate WFG & Data diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to format the test tape into one-byte blocks (of 000 data) separated by file gaps. Record at least 1/4 to 1/2 of the tape.

3. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	20 ms/div
CH Mode	Chop
CH1, CH2 Gain	.2 V/div, dc
A Trigger	HF REJ, CH1 only, SLOPE and LEVEL +, Int.

4. Use the appropriate FFG Diagnostic Routine listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive Forward File Gap operations. Inhibit error printouts, do not stop on error. Switches should be up.

5. Connect the Channel 1 oscilloscope probe to TP2 (AMP 2 OUT) and Channel 2 to TP39 (SIGNAL L) of the M7761 module. Adjust the oscilloscope controls to obtain the waveforms indicated in Figure 5-12.

6. Adjust R130 (Signal) on the M7761 module until t equals 150 ± 5 ms.

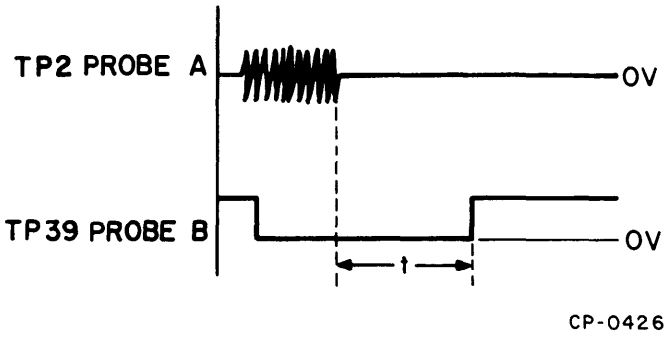


Figure 5-12 Signal Time Waveform

7. Stop tape motion and use the Read Data and Read into File Gap diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive Read Data and Read File Gap operations. Inhibit error printouts, do not stop on error. Switches should be up.

8. Change the oscilloscope sweep time to 5 ms/div and check that t now equals 13 to 15 ms. If time indication is not within tolerance, adjust R130 until this time is just within tolerance; set oscilloscope sweep time to 20 ms/div, then recheck Steps 4, 5, and 6 to ensure they are still within specifications.

9. Before starting this step, ensure that at least 1/4 of the tape is wound onto the control reel (lower). Use the BFG diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive Back File Gap operations. Inhibit error printouts, do not stop on error. Switches should be up.

10. Change the oscilloscope sweep time to 10 ms/div and check that t now equals 65 to 85 ms.

5.3.10 Tape Blank One-Shot

1. Load cassettes into drives A and B and perform a manual rewind on both drives.

2. Omit this step if tape is already formatted as in Paragraph 5.3.8. Select drive A and use the appropriate WFG & Data diagnostic routine listed in Paragraph 5.4.2 or 5.4.4 to format the test tape into one-byte blocks (000 data) separated by file gaps.

3. Set the oscilloscope controls as follows:

Horiz Display	A
A Sweep Mode	Normal Trigger
A Sweep Time	50 ms/div
CH1, CH2 Gain	.2 V/div dc
CH Mode	Chop
A Trigger	Internal 1, LF REJ, CH1 only, SLOPE and LEVEL +

4. Use the appropriate Read Data and Read into File Gap diagnostic listed in Paragraph 5.4.2 or 5.4.4 to perform repetitive Read Data and Read File Gap operations. Inhibit error printout, and do not halt on error. Switches should be set.

5. Connect Channel 1 oscilloscope probe to TP39 (Signal L) of the M7761 module, and Channel 2 to TP6 (Drive L) of the M7760 module. Adjust the oscilloscope to obtain the waveforms indicated in Figure 5-13.

6. Adjust R24 (Pot C) on the M7760 module until t equals 385 ± 15 ms.

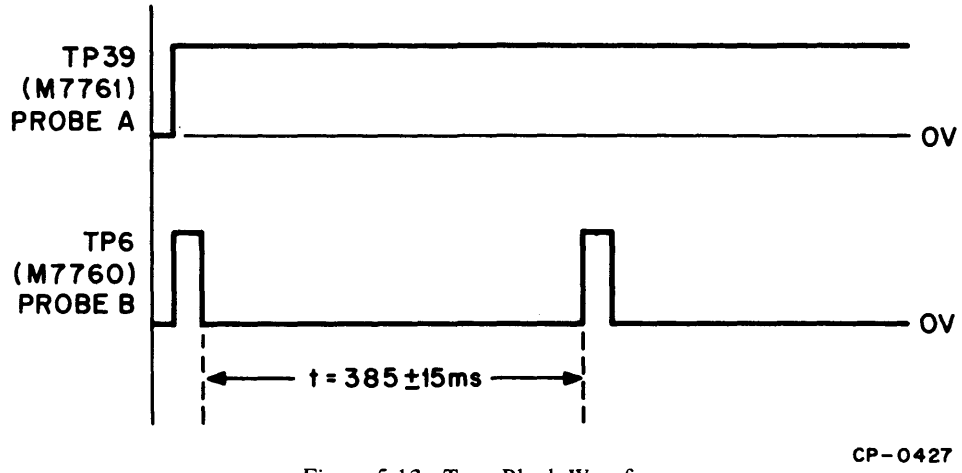


Figure 5-13 Tape Blank Waveform

5.4 TEST PROGRAMS AND DIAGNOSTIC ROUTINES

5.4.1 PDP-8 Tape Motion Routines

Program

MEM Location	Instruction
7000	7604
7001	67 X 4
7002	67 X 6
7003	5200

Switch Setting for Tape Motion Program*

Operation	Switch Setting
Stop**	0000
Read Drive A	0200
Read Drive B	0300
BBG Drive A	0230
BBG Drive B	0330

*Manual rewind may be necessary before motion will proceed.

**If the tape is not block formatted, it may be necessary to halt the test program and issue an Initialize or Clear instruction to stop the tape motion.

5.4.2 PDP-8 Diagnostic Routine – MAINDEC-08-DHTAA

Refer to diagnostic write up for instructions for each routine. Set location 0067 = 0000 for drive A, or = 0100 for drive B.

Starting Address	Function*
0205	Write File Gaps (WFG)
0206	Write Continuous Data Blocks
0207	Read Continuous Data Blocks
0210	WFG & Data Blocks
0211	Read a File Gap and a Block of Data
0212	Forward File Gap (FFG)
0213	Back Space File Gap (BFG)

Switch Settings

SR1 = 1	Loop on test sequence
SR3 = 1	Inhibit error printout
SR4 = 1	Don't halt on error
SR5 = 1	Pause 200 ms between functions

*Static test must be run once (SA 200) before above functions run.

5.4.3 PDP-11 Tape Motion Routines

Program

MEM Location	Instruction
200	013737
202	177570
204	177500
206	000137
210	000200

Switch Settings for Tape Motion Routines

Operation	Drive A	Drive B
Read	00005	00405
Space Back Block	00011	00411
Space Fwd Block	00015	00415
Write	00003	00403
Rewind	00017	00417

5.4.4 PDP-11 Diagnostics Routines

Switch Settings

SR15 = UP	Halt on error
SR14 = 1	Loop on test
SR9 = 1	Loop on error
SR10 = 1	Ring bell on error
SR13 = 1	Inhibit error printout
SR7 = 1	Pause (200 ms)
SR8 = 1	Do not change drive

5.5 CORRECTIVE MAINTENANCE

Corrective maintenance is written to aid the technician in locating problems in the TU60. While troubleshooting is a useful tool, it can never be complete to the extent that all problems will be found through its use.

5.5.1 Troubleshooting

Some of the most difficult problems to troubleshoot are:

a. Temperature sensitive components
b. Open or shorted etch under an IC or other component
c. Cold solder joints

Methods that may help locate these types of problems are:

a. Heat gun and pressurized freon to heat and cool components.

b. Open etch may be found by tracing the signal until it disappears (at the open circuit) and by visual inspection. Short circuits may be found by inspection and by component replacement. Cutting etch should be reserved for a last resort measure.

c. Cold solder joints are best located by tapping, moving, or otherwise mechanically stressing components. A hot soldering iron on doubtful connections is often useful.

Difficult areas discussed in this section are listed below.

Logic	Paragraph
Power, DC	5.5.2
Drive Status	5.5.3
Drive Servo Balance	5.5.4
Drive Speed (R/W and Search)	5.5.5
Servo Ramp	5.5.6
Tension Motor Circuits	5.5.7
Write Clock	5.5.8
Signal One-Shot	5.5.9
Preliminary Data Handling	5.5.10
Phase-Lock-Loop and Reading Data	5.5.11

5.5.2 Power, DC

Shorts and Opens

1. Check all the power transistors for shorts, particularly the servo power transistors (Figure A-5).

2. Check the power diodes (IN4004 D1, D3, D17, D19) for shorts (Figure A-5).

    a. D1, D17 parallel the solenoids and shorting would cause the -15V and/or negative regulator to malfunction.

    b. D3 and D19 parallel the tension motors. Shorting might cause the +5V, +15V or positive regulator to have a power failure.

3. Check the four electrolytic capacitors in the positive or negative regulator for shorts (Figure A-6).

    a. Positive – C55 6.8 μF, C57 47 μF
    b. Negative – C52 6.8 μF, C54 47 μF

4. It is possible that one of the .1 μF filter capacitors is shorted (Figure A-6).

    a. +12V – C3, C32, C63
    b. -12V – C2, C33, C64

Regulator Troubleshooting (Figure A-6)

1. Positive regulator too low in voltage, or zero.

    a. Zener diode D29 shorted.
    b. Q33 shorted, Q34, Q35, Q36 open.

2. Positive regulator too high in voltage.

    a. Zener diode D29 open.
    b. Q33, Q34, or Q35 shorted.
    c. Q36 open.

3. Negative regulator too low or high in voltage.

    a. Similar to positive regulator (see 1 and 2 above)
    b. 2K pot has a "dead spot."

5.5.3 Drive Status (Figure A-6)

1. EOT/BOT status bit does not become low when the sensor is over clear leader.

    a. Check E23, E16, and then E22 for incorrect output.

2. EOT/BOT status bit is low all the time.

    a. E22 output is high all the time due to defective E22 or a shorted input.
    b. Connector J6 has an open.

3. Manual rewind does not occur on Drive A.

    a. Check manual rewind command at E12 (continuity to J3-TT).

    b. Check E21 (especially check that the clear input is not at ground and force clearing the rewind mono).

4. Rewind STAYS and never clears.

    a. Check that E21 is not being pulled to ground by E12, or a short. Also check E12's inputs, (the output of E12 being ground force sets the one-shot).

    b. Check the leader circuitry.

5. Rewind takes one second to clear when the drive detects leader (does not clear immediately).

    a. Check that clear pulse appears at E21 when leader has passed over (pulse is roughly 5 μs long) if pulse is present, problem should be E21. If pulse is not present, check E28 for a level, and E15 for a pulse. C21 might be open.

5.5.4 Drive Servo Balance

Drive A (Figure A-5)

1. Servo does not balance.

    a. Check TP19 for several millivolts movement when the balance pot is adjusted.

    b. Check TP25, the ramp generator output to be less than 20 mV (with no tape movement). If it is not, check Q16, Q15 to be off and TP22 and TP23 to be high.

    c. Check the power amp transistors Q25, Q26, Q37, and Q38 (with no tape movement). Emitter and base to be about zero volts, collector equal to V ref.

Drive B (Figure A-5)

1. Servo does not balance.

    a. Check TP7 for several millivolts movement when the balance pot is adjusted.

    b. Check TP12 to be less than 20 mV. If it is not, check Q6 and Q7 to be off and TP8 and TP10 to be high.

    c. Check the power amp transistors Q27, Q28, Q40, and Q41 (with no tape movement). Emitter and base is to be about zero volts, collector equal to V ref.

5.5.5 Drive Speed (R/W and Search) (Figure A-5)

Because Drives A and B are similar, only Drive A is described.

1. Forward and reverse speeds are not nearly equal.

    a. Check to ensure that Q16 and Q15 saturate when the drive moves forward or reverse.

    b. Measure V ref at TP32 for forward and reverse command to produce the same voltage.

2. No high speed or no low speed.

    a. At high speed, Q23 saturates and should be roughly 12 V. At low speed, this should drop to about 5.5 V. Only the ratio is important. It should be 2.1–2.3 to 1.

Speeds

R/W	Search	Test Point
+5.5V	+12V	TP32
-4V	-8V	TP25 & 12
-4V	-8V	TP20 & 9
+2.5V	+5.2V	TP19 & 7

All of the above voltages are approximate.

    b. If you are lacking high speed, check TP32 while issuing alternate high and low speed commands. If readings do not double, the transistor Q23 is not turning on. Check TP44 and trace HIGH SPEED H through E43.

    c. No low speed, transistor Q23 may be shorted, E43 may be defective, etc.

5.5.6 Servo Ramp (Figure A-5)

Since Drive A and B circuits are similar, only Drive A is discussed here.

1. Negative ramp is not 15 ± 3 ms.

    a. Check ramp adjustment.

    b. Check E27, E26 and their supply voltages. Check that E27 output swings at least 10 V each side of ground.

2. Drive A ramp not linear.

    a. Gain of E26 too low or C36 not connected properly.

3. Negative ramp cannot be adjusted to within 2 ms of positive ramp.

    a. Check negative supply voltage and positive supply voltage. Negative supply should be adjustable to be equal to or up to 2 V less than the positive supply voltage.

    b. E27 may not be saturating properly.

5.5.7 Tension Motor Circuits (Figure A-5)

Since both tension motor circuits are similar, only Drive A is discussed here.

1. While moving in reverse, the tension motor is exerting low torque.

    a. Q13 and Q14 are not turned on. Check E18 for Rev H signal while executing a reverse command.

2. Tension motor always exerting high torque.

    a. Check E18 while alternately changing direction.
    b. Check Q13 and Q14 for shorts.
    c. Q12, Q13, or Q14 may always be on.

5.5.8 Write Clock (Figure A-7)

1. Either clock pulse missing:

    a. Check TP35 and TP37 for narrow negative Clock 1 and Clock 2 spikes. If both are present, check J6-TT and J6-RR for the clock signals.

    b. If clock pulses are present at TP35 or TP37 but not both, check E39, C47, and C48.

    c. If clock pulses are not present at TP35 or TP37, check that the crystal oscillator is working by scoping through divider chain, E39, E38, E32, and clock selector E31.

2. Clock period of BLANK H at TP38 is not 223 ms, or is not jitter free (Figure A-7).

    a. Check that E31 has selected the WRITE CLOCK signal, rather than the READ VCO signal, by examining frequencies at E31. (The unit should be in write mode and the output should show the inversion of the input.) Change E31 if not true.

    b. Frequency is double, triple, quadruple, or just different. The crystal may be bad, or the compensation network R193 – 220 Ω and C46 – .01 may be bad.

5.5.9 Signal One-Shot (Figure A-7)

1. 150 ms time looks like 75 ms time.

    a. Q22 is shorted or being turned on all the time.

2. 150 ms time looks like 15 ms time.

    a. Q21 is shorted or being turned on all the time.

3. 75 ms time looks like 150 ms.

    a. Q22 is not turning on. Scope both sides of R136.

4. Adjusting the signal pot R130 has no effect on the time.

    a. Check the voltage at the wiper of the pot while turning pot. It should go from 4-1/2 to 5V. R138 may not be grounded.

5. All times look too short or too long.

    a. Check the timing capacitor C41 and replace if faulty.

6. All three times 150, 75, 15 ms cannot all be brought into spec.

    a. Replace the signal mono E33.

5.5.10 Preliminary Data Handling (Figure A-7)

1. No data at TP2.

    a. Check TP1. If signal present, check C1, R4, or replace E1.
    b. Check D5 or D6 for shorts.
    c. If one drive selection only works, check diodes D10, D11, D12, D13.
    d. Check TP26 for +5 when SEL A signal is true, less than 2V when SELECT B is true.
    e. Check TP27 for +5 when SEL B signal is true, less than 2V when SELECT A is true.
    f. Check Write Data transitions at E28.
    g. Check WRITE ENABLE H at E11. Check Write Data transitions at E11.

5.5.11 Phase-Lock-Loop and Reading Data (Figure A-7)

1. Frequency control signal never goes high, TP45.

    a. Verify that data is appearing at Amp 2 output TP2.

    b. Verify that ENERGY H TP31 is going H (after several data transitions). If it does not, go to step 2. If it does, go to step 3.

2. Frequency control signal never goes high, Energy high (TP31) never goes high, and data appears at TP2.

    a. Energy one-shot E36 is not triggering. Check that the clear pin is not low E36. Check for peak detector output transitions. Check TP33 for a logic high, if not check the Energy Clear one-shot and the 7406, which can keep TP33 at ground.

3. Frequency control signal never goes high, ENERGY goes high, and data appears at TP2.

    a. Look for a defective phase detector E44, or Q24. Check the remaining resistive components and etch attached to E44.

4. Rise time not 2 ms or less.

    a. Change Q24 and check surrounding resistors.

5. Frequency control does not drop on a drive selection change.

    a. Check the energy clear circuitry consisting of one shot E36, E43, E14 and E35. Output of E43 should go low momentarily each time the selection is changed.

6. Read signal amplitude too low or too high with either drive selected.

    a. Check the peak to peak preamble signal at TP1. It should be .2V approximately. The output at TP2 should be 25 times larger or about 5V peak to peak on the preamble. If the gain of Amp 2 is not approximately 25, look for a shorted output (if too low) or replace E1. (The voltages indicated are for the beginning of tape; at the end of tape, the voltages are double.)

7. The voltage at TP1 has a large dc value of more than a volt or is close of saturation, check the common mode rejection by checking R29, R31, R28, and R31.

8. Read signal amplitude too low on one drive only.

    a. Check for loading of the selected drive by the unselected drive. Check all outputs of E11, check TP20 and TP27. One of the test points should be at 4.5 to 5V, the second at less than 2.0V.

9. SEEK L does not go low at least 3 bits before the last bit of preamble.

    a. Check E41. Check that INHIBIT SEEK L is not low.

    b. Verify that the D input (E41) goes high when ENERGY H goes high in the early part of the preamble.

    c. The clock input Clk 24H may be open or ground (if open, it will always be floating H).

10. Energy H one-shot time wrong (not .5 to 2.5 ms).

    a. Check the Energy one-shot timing components R145, C42, D26. If time too short, check that pin 9 remains qualified (low) until the last peak; if it does not check the read level, and the threshold delay RC network R141, C49, R158.

    b. Replace E36.

11. Energy Clear one-shot time wrong (not 1 to 3 ms).

    a. Check timing components R146, C43.
    b. Replace E36.

12. Energy Clear one-shot triggers on rising and falling edge of ENERGY H.

    a. Replace C87 and check related etch.

13. Errors are made with read level and read speed in center position.

    a. The VCO IC may be defective. E45 is the Voltage Controlled Oscillator (VCO).
    b. Energy one-shot may be clearing randomly.

14. Errors made at frequency limits. VCO does not seem to be in proper range.

    a. Check C60 (8200 pF) and read VCO E45. Replace E45.
    b. Check Q24, and the network around E44.

APPENDIX A
REFERENCE DRAWINGS

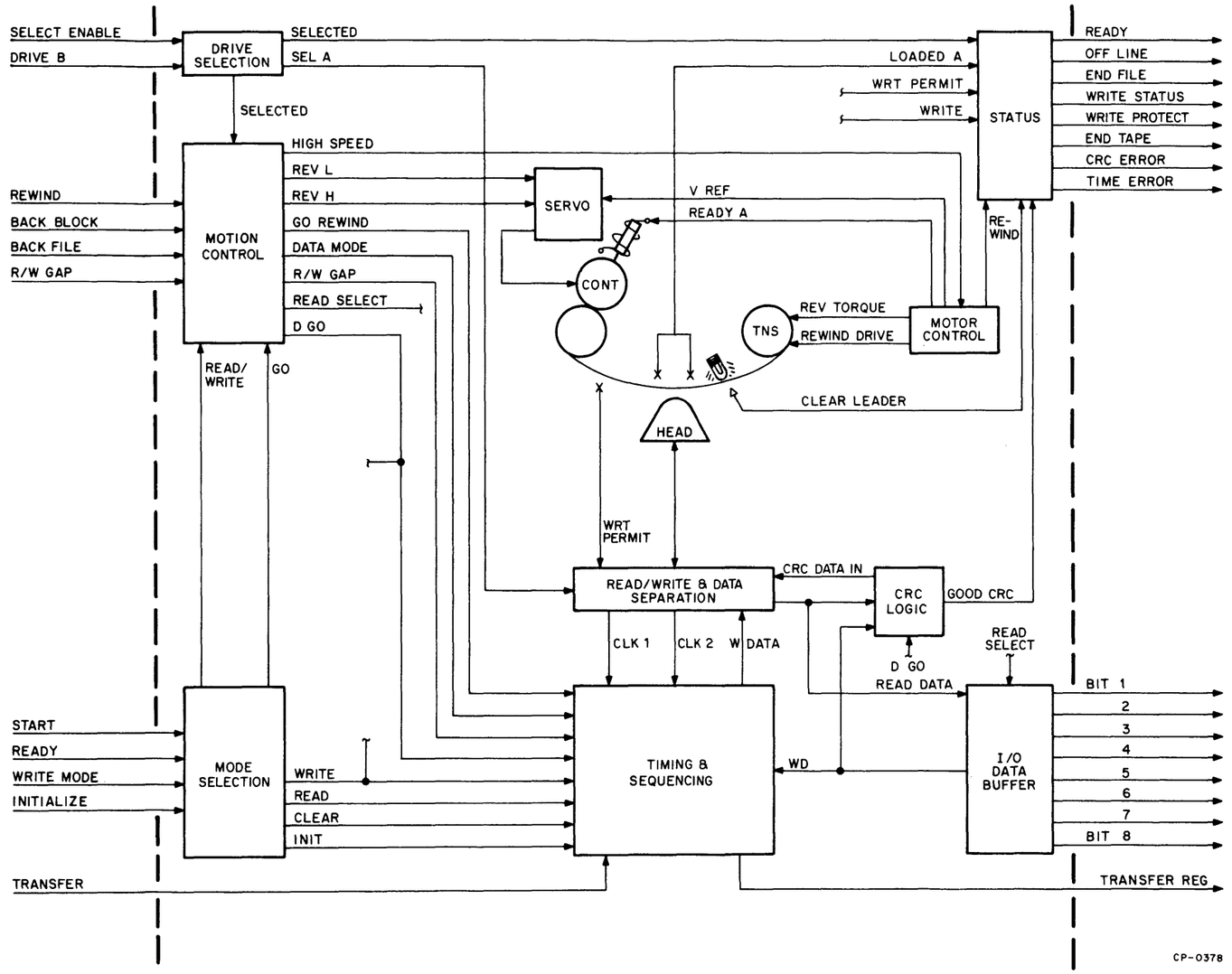


Figure A-1 Functional Block Diagram

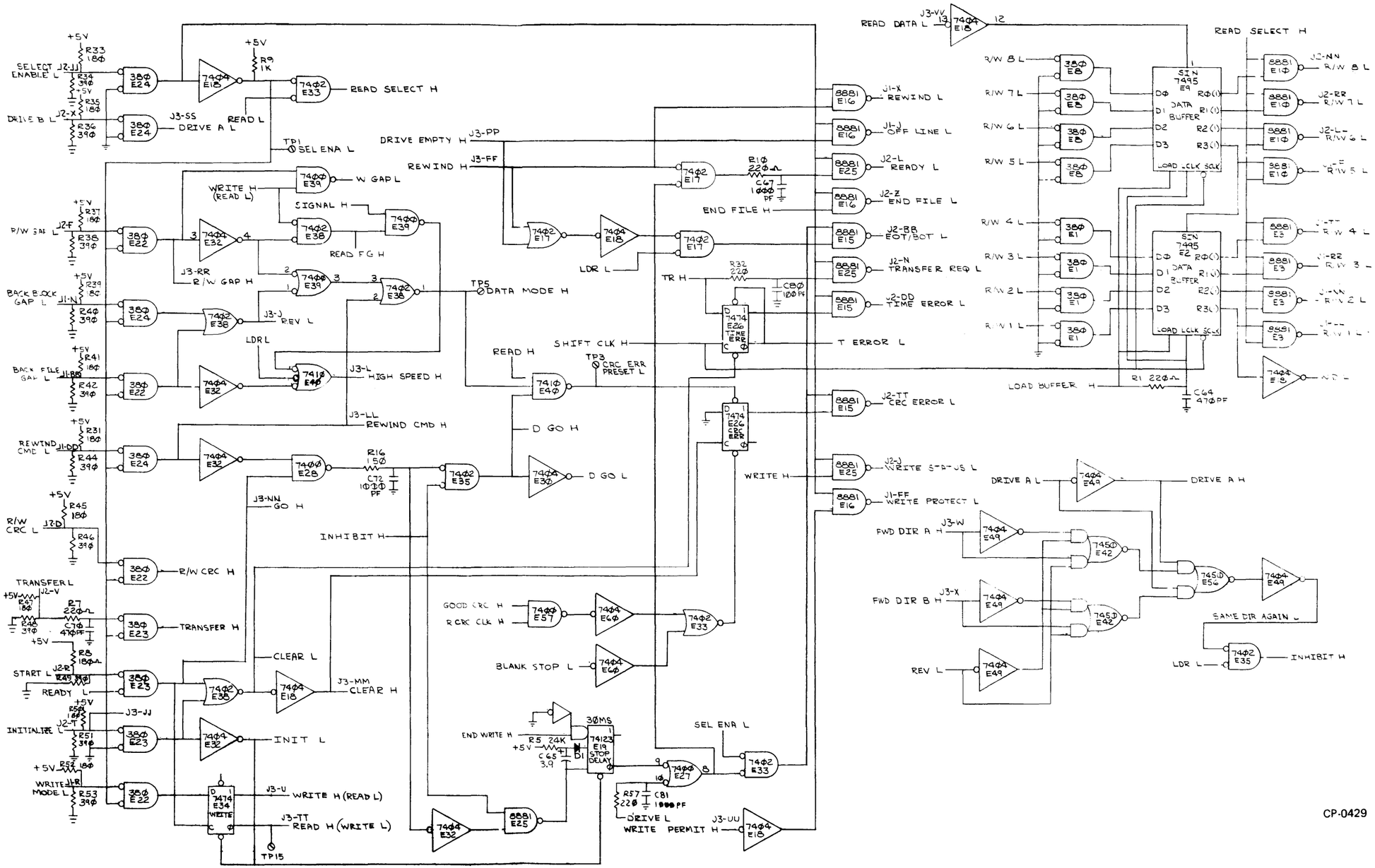


Figure A-2 Interface Logic

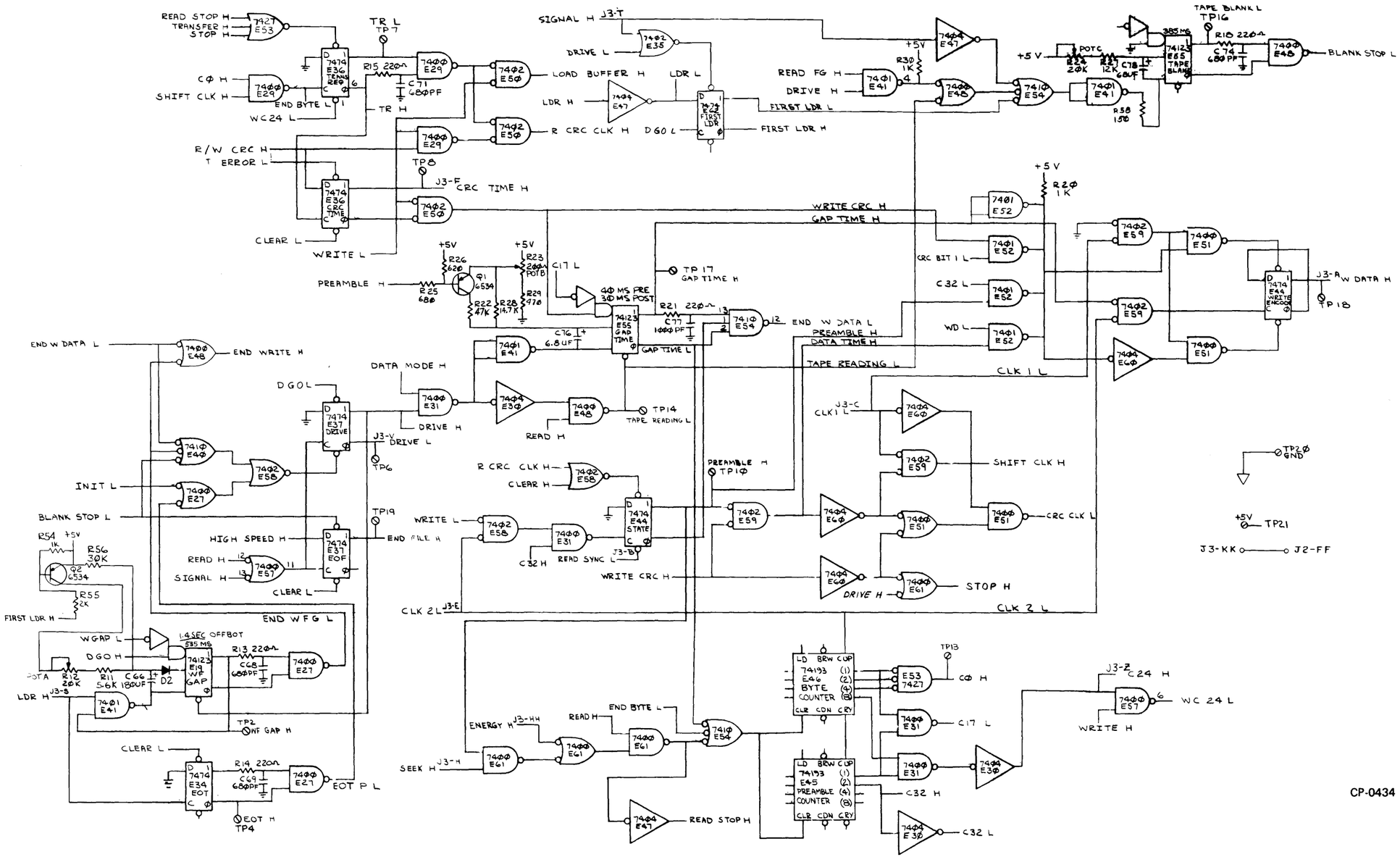
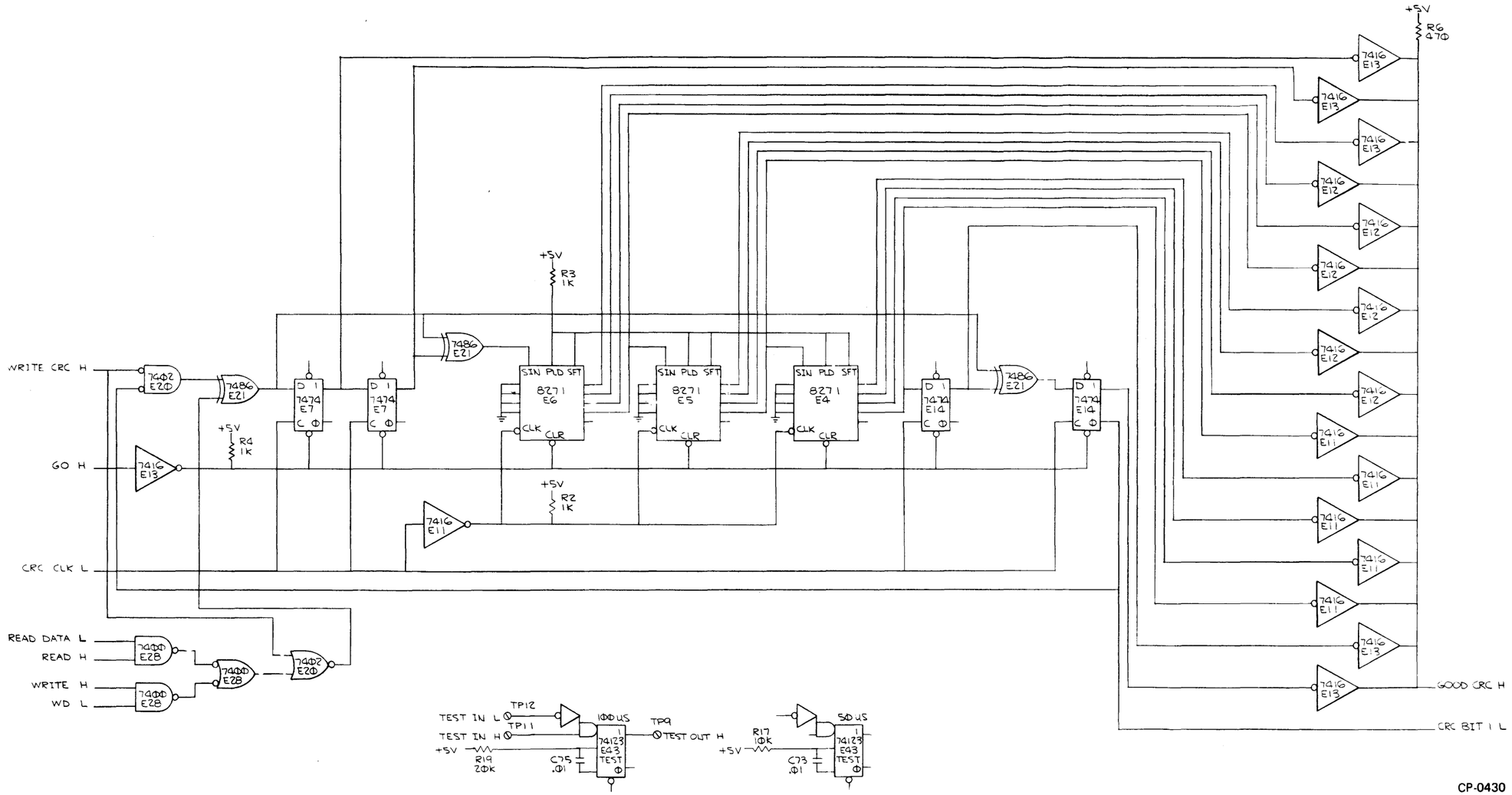


Figure A-3 Formatter Logic



CP-0430

Figure A-4 CRC Logic

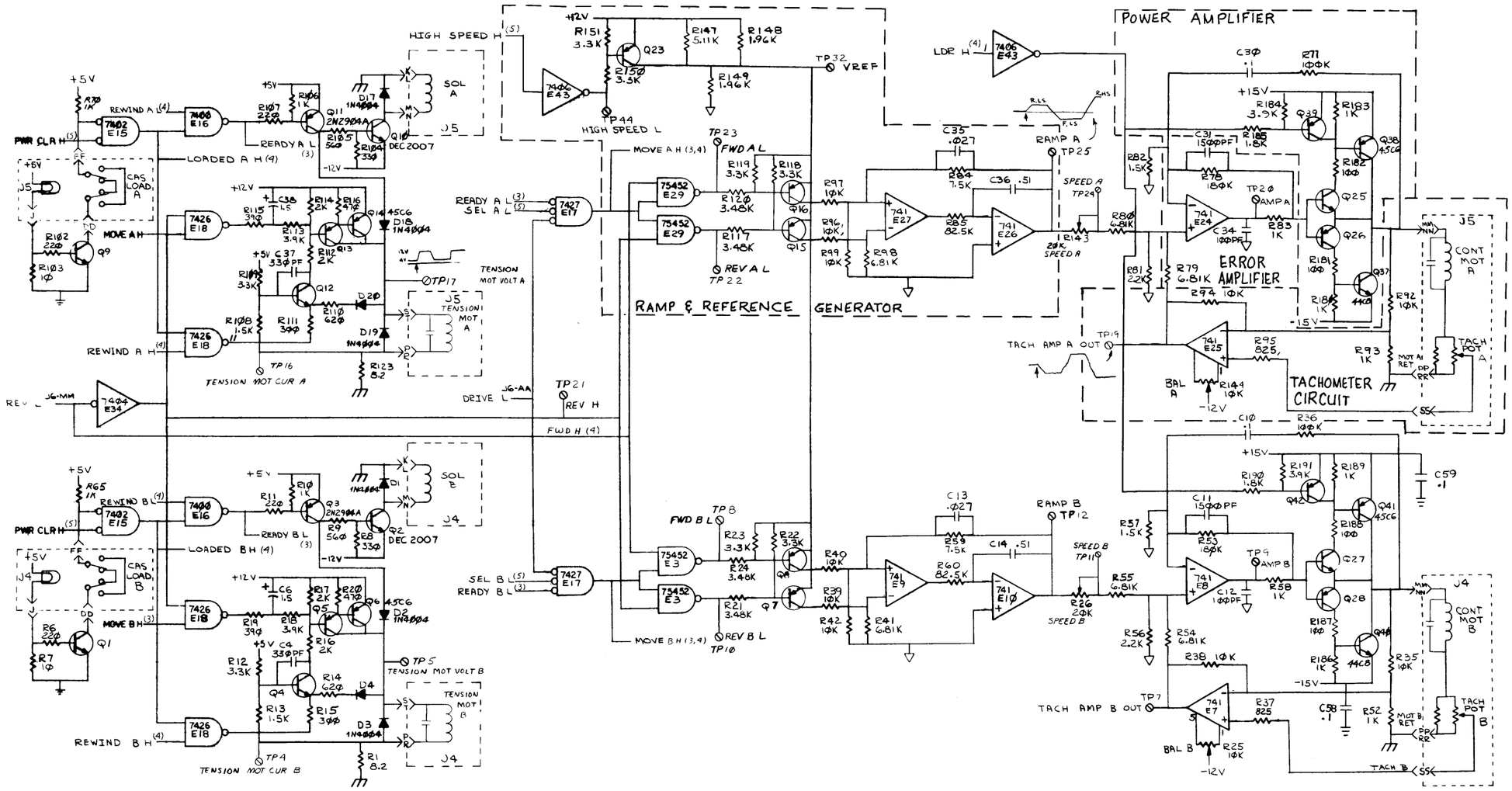
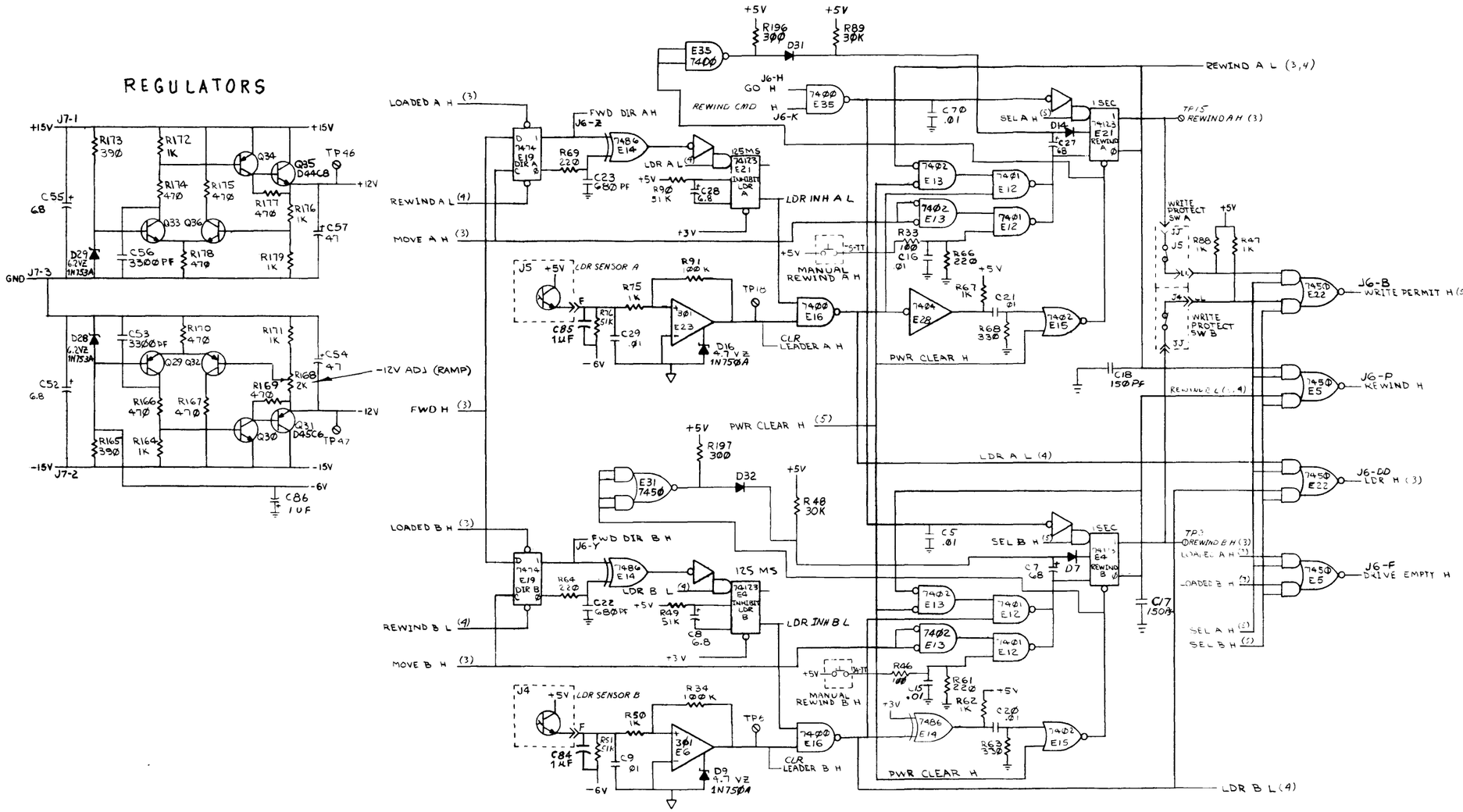


Figure A-5 Motor and Servo Logic



CP-0432

Figure A-6 Rewind Logic

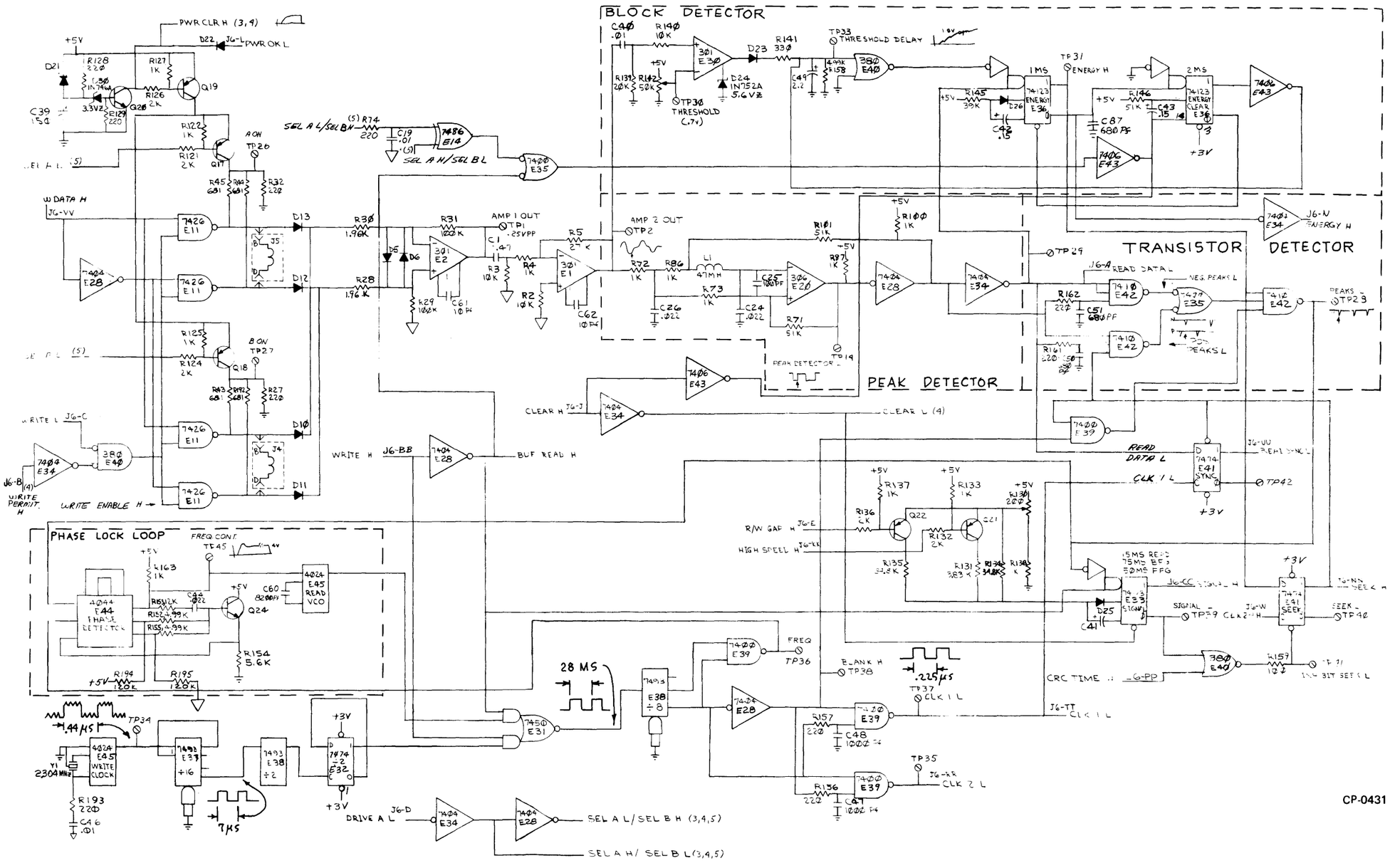
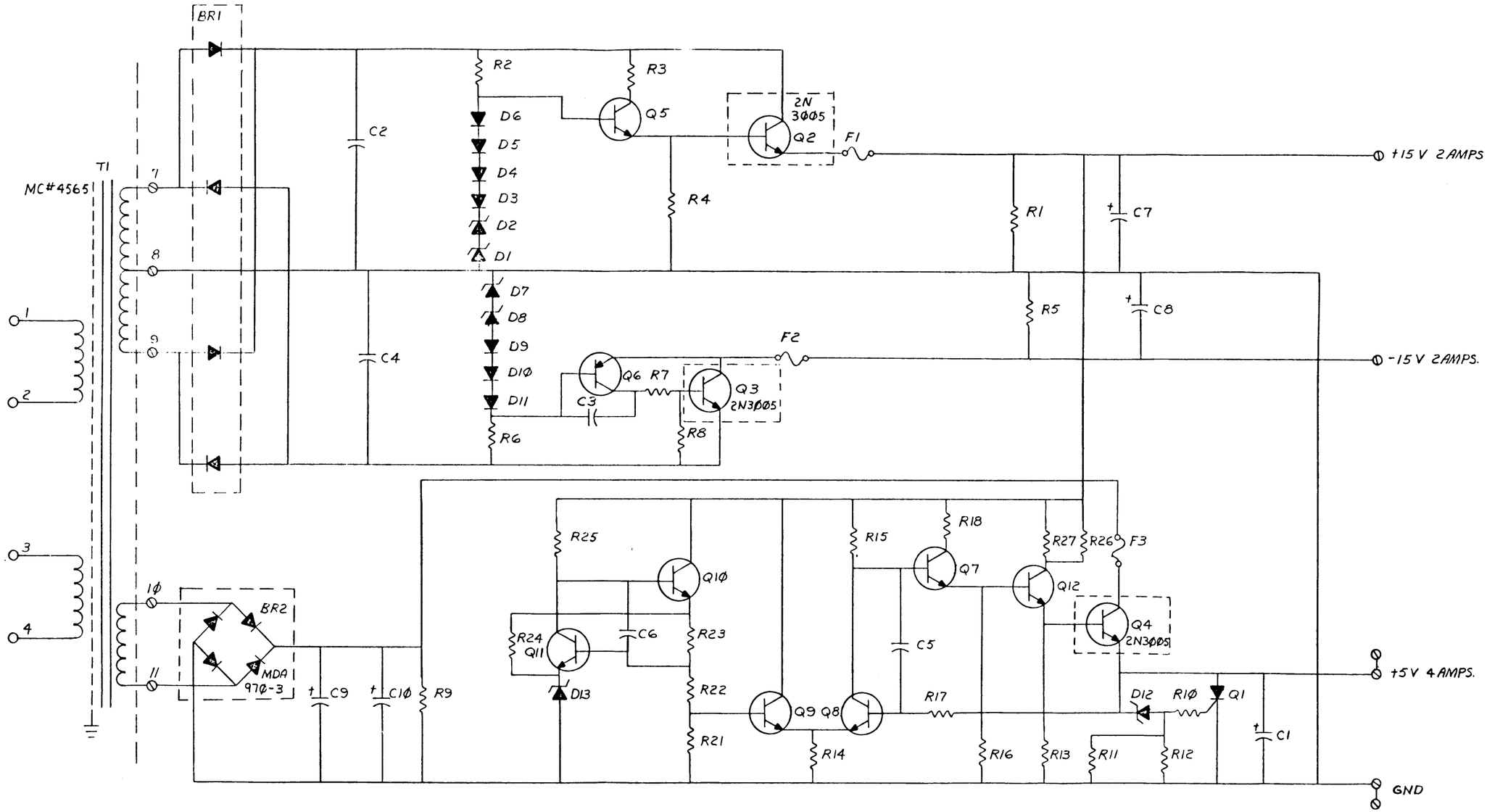


Figure A-7 Read/Write Logic



O INDICATES HOLES FOR DIODE BRIDGE
Q2, Q3, Q4, BR2 & T1 ARE MOUNTED ON CHASSIS/HEAT SINK

CP-0435

Figure A-8 H751 Power Supply

TU60 DECassette TAPE TRANSPORT
MAINTENANCE MANUAL
DEC-00-HTU60-C-D

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