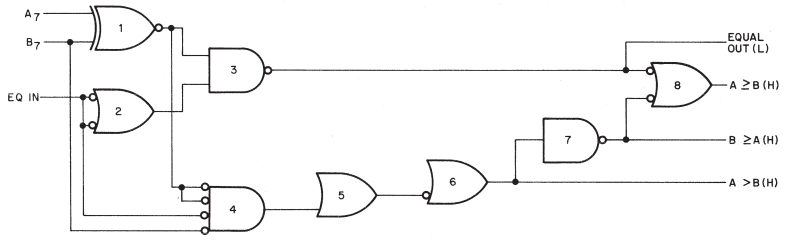
POWER: 58 mA (typical) at +5V.

3.4.11 M167 Magnitude Comparator

The M167 module compares the magnitude of two 8-bit binary numbers and provides four outputs defining the relationships of these numbers. For example, for two numbers designated A and B, the comparator defines whether A = B, A > B, A ⩾ B, or B ⩾ A. In addition, an EQUAL IN input enables cascading of modules so that comparison can be performed for greater than 8-bit numbers. For the comparison of less than 8-bit numbers, unused comparison inputs are connected to +3V and the EQUAL IN input is connected to ground.

The basic logic structure for a binary stage consists of an EXCLUSIVE OR, two 2-input NAND/NOR gates (one used as an inverter) and one 4-input NAND/NOR as shown in Figure 3-15. The remaining logic elements in Figure 3-15 are common to all stages. A truth table is provided for the stage; it assumes all higher order inputs are equal (EQUAL IN in 0V).



EQUAL IN	A_7	B_7	EQUAL OUT	A≥B	B ≥A	A>B
T (0V)	0 (0V)	0 (0V)	T (0V)	T (+3V)	T (+3V)	F (0V)
T	0	1	F	F	T	F
T	1	0	F	T	F	T
T	1	1	T	F	T	F

Figure 3-15 M167 Comparator Simplified Diagram

A principle use of this module is to compare track addresses for a write lockout function. For this application, a track address is connected to the "A" input, write lockout switch levels are connected to the "B" inputs, and the A > B output controls the write operation. With this arrangement, a write operation is disabled whenever the track address is equal to or less than the write lockout switch setting. In addition, the write lockout function can be disabled entirely by simulating a track address-greater-than-switch input to the MSB stage. For this function, the MSB "B" input is connected to ground and the MSB "A" input is switched to +3V. Conversely, to enable the write lockout function, the MSB "A" input need only be switched to 0V.

INPUTS: Voltage levels of 0V and +3V (typical) for all TTL inputs.

Pin	Use	Drive or Load
F2	A_0 (MSB)	1 TTL load
H1	A_1	
E2	A_2	
F1	A_3	
C1	A_4	
J1	A_5	
K1	A_6	
B1	A_7 (LSB)	

INPUTS: (cont)

Pin	Use	Drive or Load
H2	B_0 (MSB)	2 TTL loads
S1	B_1	
D2	B_2	
E1	B_3	
D1	B_4	
M1	B_5	
M2	B_6	
A1	B_7 (LSB)	
U2	EQUAL IN	3 TTL loads

OUTPUTS: Voltage levels of 0V and +3V (typical) for all outputs.

Pin	Use	Drive or Load
P1	EQUAL OUT (L)	7 TTL loads
R1	EQUAL OUT (H)	10 TTL loads
V1	A > B (H)	8 TTL loads
U1	B ⩾ A (H)	9 TTL loads
L1	A ⩾ B (H)	10 TTL loads

POWER:

Pin	Use
A2	20 mA at +5V
C2, T1	GND

3.4.12 M205 D-Type Flip-Flop

The M205 module contains five D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input 20 ns (maximum) before the CLOCK pulse and the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns.

INPUTS: D inputs present 1 TTL unit load each.
C inputs present 2 TTL unit loads each.
SET inputs present 2 TTL unit loads each.
CLEAR inputs present 3 TTL unit loads each.

OUTPUTS: Each output (0 and 1) is capable of driving 10 TTL unit loads. Two +3V supplies (U1 and V1), capable of 25 unit loads, are available.

POWER: 100 mA (maximum) at +5V.