MEMORY TUNING PROCEDURE

PDP-8

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PDP-8 MEMORY TUNING PROCEDURE

This procedure describes a method for checking out and tuning the basic 4K core memory and memory wing of the PDP-8 digital computer, using the rest of the computer (central processor wing and power supply). It is assumed that all of the equipment used is in working condition and properly calibrated.

TEST EQUIPMENT REQUIRED

The following test equipment is required for checking out and tuning the memory and memory wing, in addition to the ordinary hand tools. If the specified equipment is not available, a substitute may be used if its parameters equal or exceed those of the specified item.

Test Equipment	Manufacturer and Model
Digital Computer	DEC, PDP-8
Oscilloscope	Tektronix, Type 547
Preamplifier	Tektronix, Type 1A1
Voltage Probes (2)	Tektronix, Type P6Ø1Ø
Current Probe with Terminator or Preamplifier	Tektronix, Type P6Ø16
Multimeter	Triplet, 63Ø-NA
Program Tapes*	DEC, Maindec 8Ø2 (Checkerboard-Low and Checkerboard-High)

*Optional, requires that an ASR-33 Paper Tape Reader be available.

PRELIMINARY

This part of the procedure is to be used before a new memory wing is first installed. If the memory wing has previously been checked out, go on to the next part, POWER. Figure 1 shows the flow of operations in this part.

Components

Check that all the modules listed below are installed in their correct locations. From the module side, location 1 is on the right and location 32 is on the left.

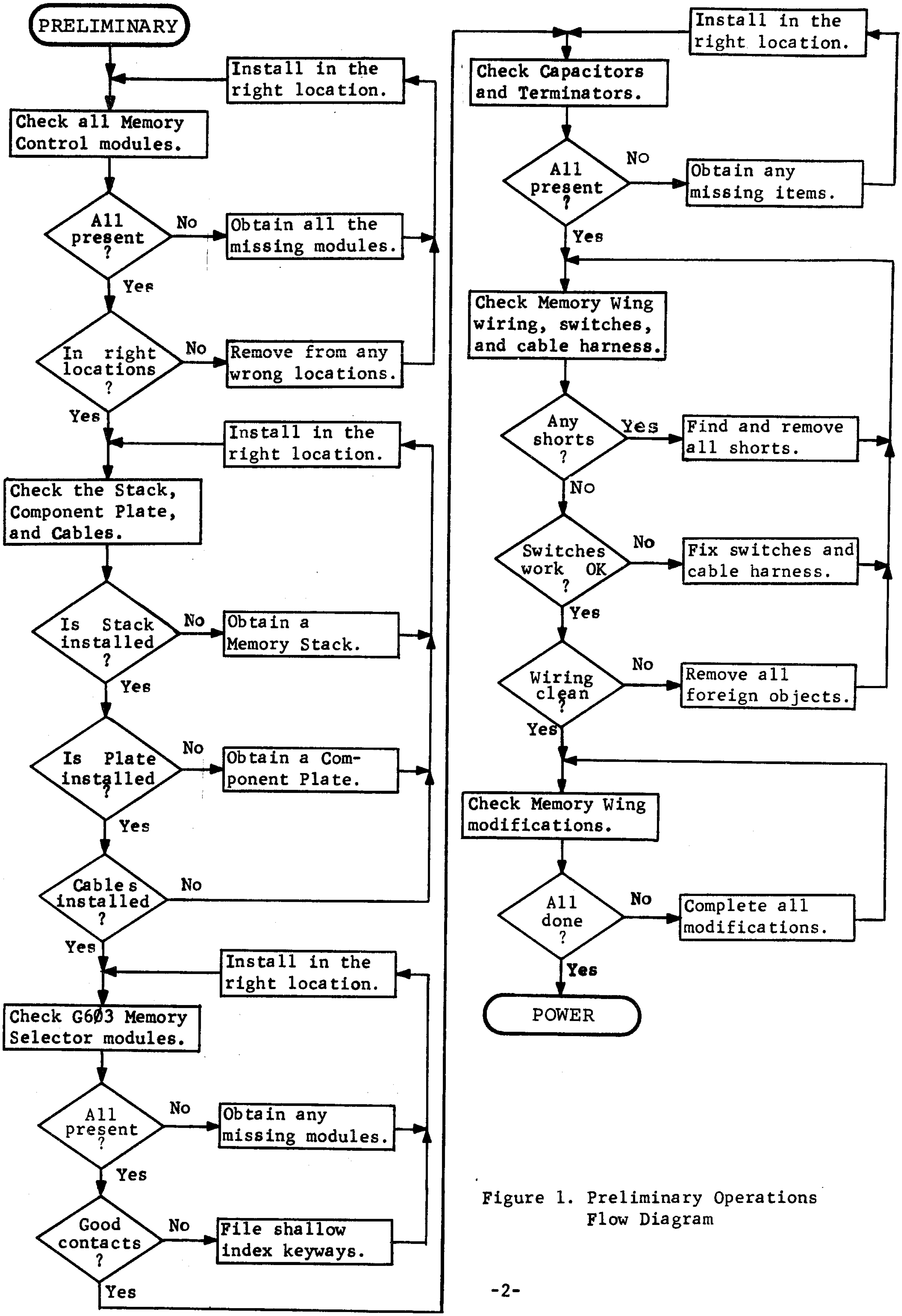

Figure 1. Preliminary Operations Flow Diagram

Location	Module	Location	Module	Location	Module
MA25	GØØ7	MCDØ6	G2Ø9	MC19	W6Ø7
MA26	GØØ7	MCDØ7	G2Ø9	MC2Ø	B6Ø2
MA27	GØØ7	MCDØ8	G2Ø9	MC21	G2Ø8
MA28	GØØ7	MCDØ9	G2Ø9	MC22	G2Ø8
MA29	GØØ7	MCD12	G2Ø9	MC24	G2Ø8
MA3Ø	GØØ7	MCD13	G2Ø9	MC25	G2Ø8*
MA31	GØØ7*	MCD14	G2Ø9	MD19	B1Ø4
MB25	GØØ7	MCD15	G2Ø9	MD2Ø	B36Ø
MB26	GØØ7	MC16	B684	MD21	G2Ø8
MB27	GØØ7	MD16	B2Ø4	MD22	G2Ø8
MB28	GØØ7	MCD17	W3ØØ	MD24	G2Ø8
MB29	GØØ7	MCD18	W3ØØ		
MB3Ø	GØØ7				
MB31	GØØ8				

*Installed only when the 188 Parity Option is used.

Check that the core stack is fastened to the wing at MAB9-24 and the current limiting resistors are installed on the component plate at MAB1-8. The two WØ25 connectors with white wires from the core stack should be plugged into MCD1Ø and MCD11; the WØ25 connector with colored wires should be plugged into MCD23.

Check that eight G6Ø3 Memory Selection Matrix modules are plugged into the sockets on the side of the core stack, and that their contacts align with the connector contacts. If the contacts are not aligned, remove the module, file the shallow index keyway deep enough to align the contacts, and replace the module.

Check that a 6.8 microforad 35 vdc capacitor is connected from the sense amplifier +1ØA, -15B, and +1ØD busses in either MA25-31 or MB25-3Ø to ground. Also check that a 22 ohm resistor is connected from the MEM STROBE bus at MA25L to ground.

Wiring

Check each of the power connections on the memory wing frame for shorts to ground or each other. Use an ohmmeter set to the X1Ø scale and the positive probe on ground. With all the marginal power switches off (down), all connections except +1Ø and -15 should read ∞: the latter should read less than 1ØØ ohms. With all the marginal switches on MC (up), the

+1Ø and -15 connections should read ∞ and the +1ØMC and -15MC connections should read less than 1ØØ ohms.

Check both the + and - sides of the R/W and INH terminals on the power supply for any short to ground. When this has been done, the memory wing can be mounted on the main computer frame, the power wires can be connected, and the cables from the central processor wing plugged into the memory wing.

Check the memory wing logic wiring for loose or broken wires, and foreign objects such as solder whiskers, pieces of wire, etc. Remove all foreign objects.

Check that all modifications have been made. In particular, check that one wire connects the following terminals together. If other wires are present or go to different terminals, remove them and install the correct wire.

MD17E	to	MD175
MC17S	to	MD17M
MC18P	to	MD18S
MC18M	to	MD18M
MC18H	to	MD18F

NOTE: These connections may be shown wrongly on the W3ØØ modules at the lower left of print BS-D-8M-Ø-15.

Power

Logic Power

Unplug the R/W and INH wires from their connections on the memory wing and be sure thay are not touching anything. Then turn the POWER switch on: the fans should now be running. Set the voltmeter to the 3Ø vdc scale and measure the +1Ø volts on all the +1Ø volt busses (A terminals) in the memory wing: it should be +1Ø ± 1/2 volts dc. Then measure the -15 volt busses (B terminals): they should have -15 ± 1/2 volts dc on them.

Memory Power

Switch the voltmeter to the 6Ø vdc scale and measure the voltage across the R/W and INH connectors at the power supply. Each should read 3Ø ± 3 volts dc. If either is too low, turn the power switch off and check for a low resistance path.

Turn the POWER switch off, plug the R/W and INH wires into their connectors on the memory wing, and place the voltmeter probes across the INH terminals. Then turn the POWER switch back on and check the voltage. If less than 27 volts or significantly less than previously measured, turn the POWER switch off and check the inhibit circuit in the memory wing. If normal,

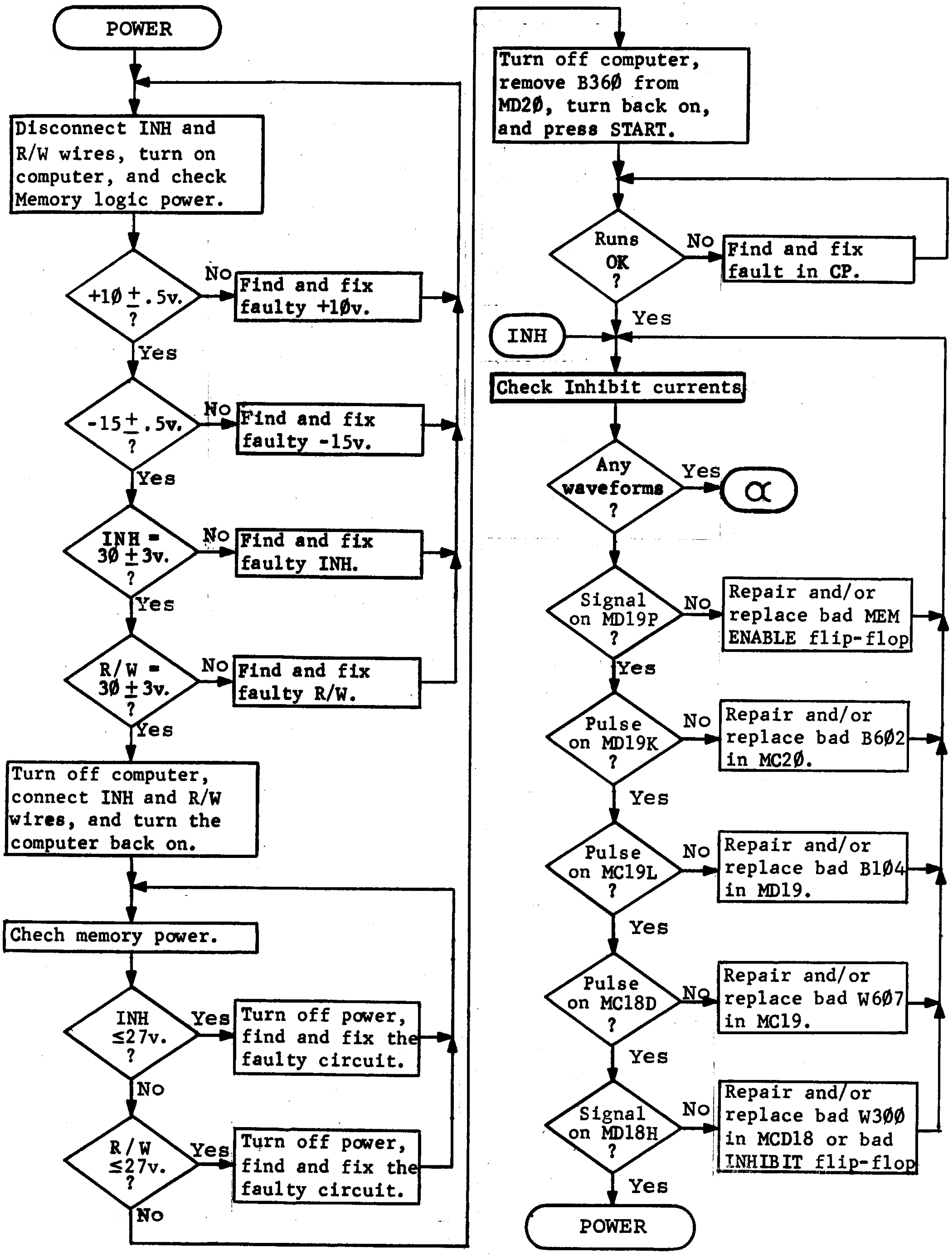

Figure 2. Power Check Procedures Flow Diagram, sheet 1.

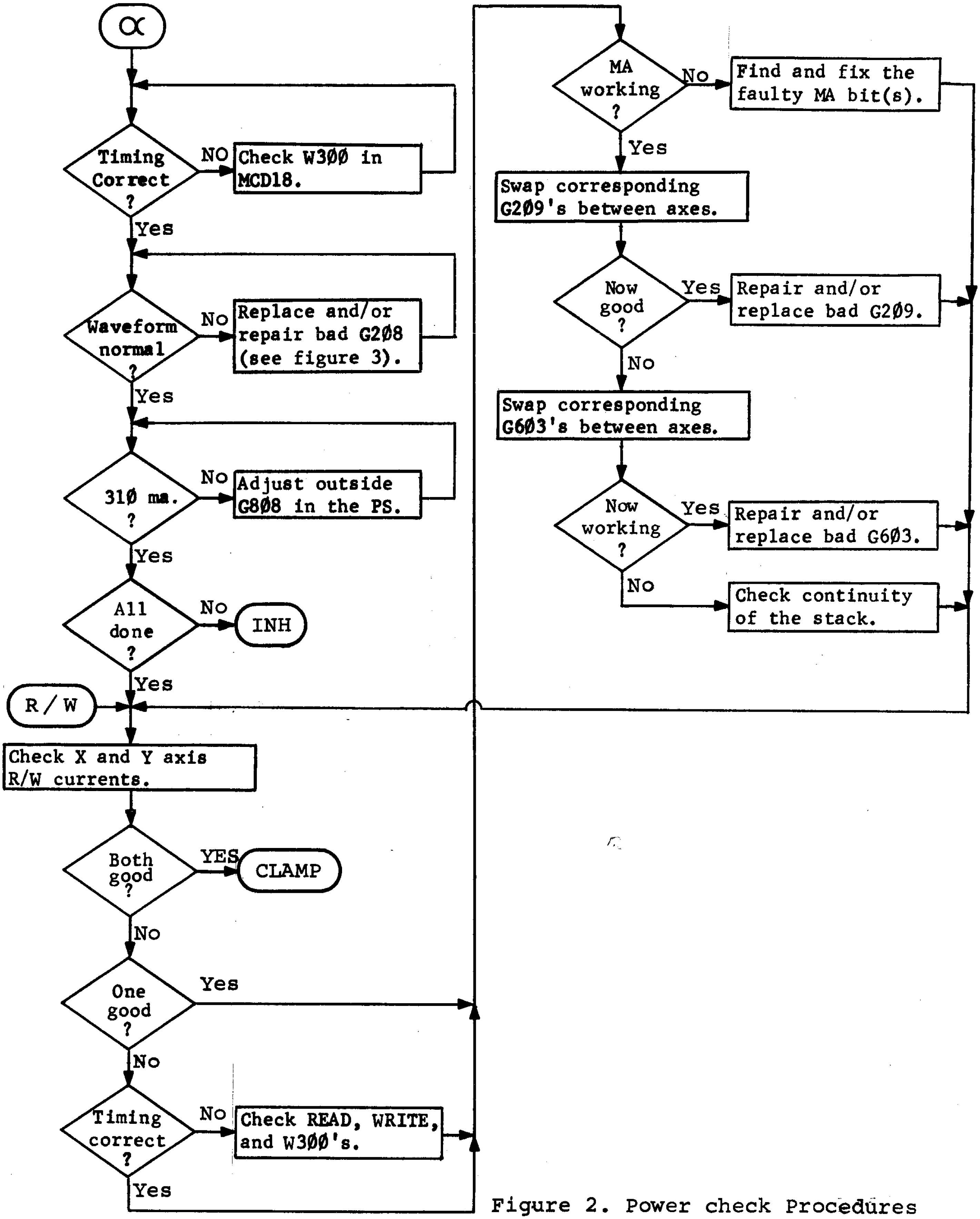

Figure 2. Power check Procedures Flow Diagram, sheet 2.

check the R/W voltage: again turn the POWER switch off if less than 27 volts or significantly less than previously measured.

Turn the POWER switch off and remove the B36Ø module from MD2Ø. (This is the MEMORY STROBE delay module — when missing the MB register can never be set by the contents of any cores). Now turn the POWER switch back on and, after the memory power delay, press the START key. The computer should run continuously, cycling through memory as it reads and writes all zeros. The AND, FETCH, EXECUTE, and RUN indicators should be on. If not working properly, correct the trouble before proceeding further.

Inhibit Current

Set up the oscilloscope for external triggering, and trigger it with the BT2A pulse. (This is a negative pulse obtained at MD3ØU). Then connect the current probe and its terminator or preamplifier to the input of channel 1 and a voltage probe to the input of channel 2. Calibrate both probes, then adjust the sensitivity of channel 1 for 5Ø milliamperes per centimeter and of channel 2 for 2 volts per centimeter.

Observe the bit 5 inhibit current by placing the current probe around the yellow wire from MC 24N. If normal, adjust the potentiometer on the outside G8Ø8 (located in the power supply) for an inhibit pulse amplitude of 31Ø milliamperes. If not normal, move the current probe to another yellow wire in the same vicinity and adjust the inhibit current.

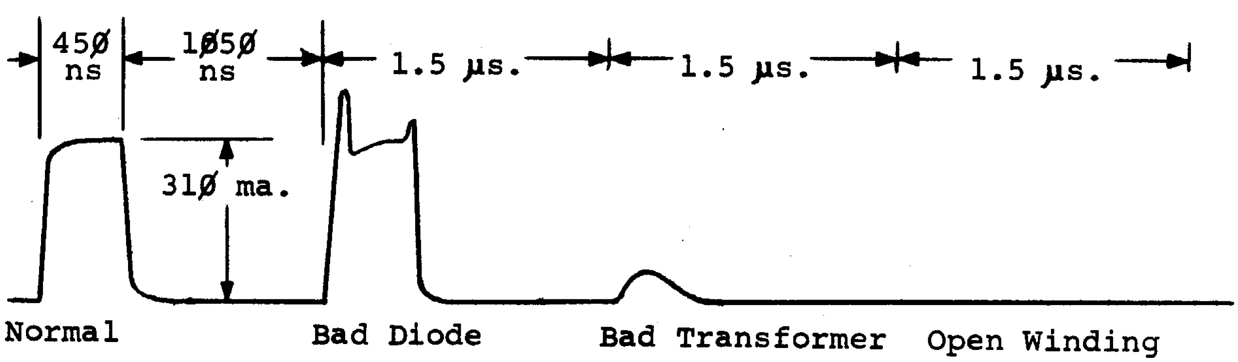

Figure 3. Representative Inhibit Current Waveforms.

Check all 12 (or 13 if the Parity Option is used) inhibit currents. Use the yellow wires from the terminals listed below. If the timing is wrong, check the INHIBIT flip-flop in the B2Ø4 at MD16 (see drawing BS-D-8M-Ø-15) and/or the W3ØØ at MCD18. If one bit is abnormal, swap the G2Ø8 module with a known good one to determine if the module is bad. Be sure the POWER switch is off when removing and replacing modules.

Bit	Output	Bit	Output	Bit	Output
Ø	MC21E	4	MC24E	8	MD22E
1	MC21N	5	MC24N	9	MD22N
2	MC22E	6	MD21E	1Ø	MD24E
3	MC22N	7	MD21N	11	MD24N
				P	MC25N

Read/Write Current

Observe the Y axis read and write current waveforms by placing the current probe around the yellow wire from MC12N. If normal, adjust the potentiometer on the inside G8Ø8 (located in the power supply) for read and write pulse amplitudes of 33Ø milliamperes. If not normal, decrease the oscilloscope sweep speed and observe the abnormal envelope. Then, with alternate sweeps in use, look at the outputs and inputs of the G2Ø9 modules in MCD12-15 to determine which (if any) is faulty. (Use drawing BS-D-8M-Ø-13). Turn off the POWER switch and swap the seemingly-bad module(s) for a good one(s) to see if the G2Ø9 module or G6Ø3 module is at fault. If not these modules, check the MB levels.

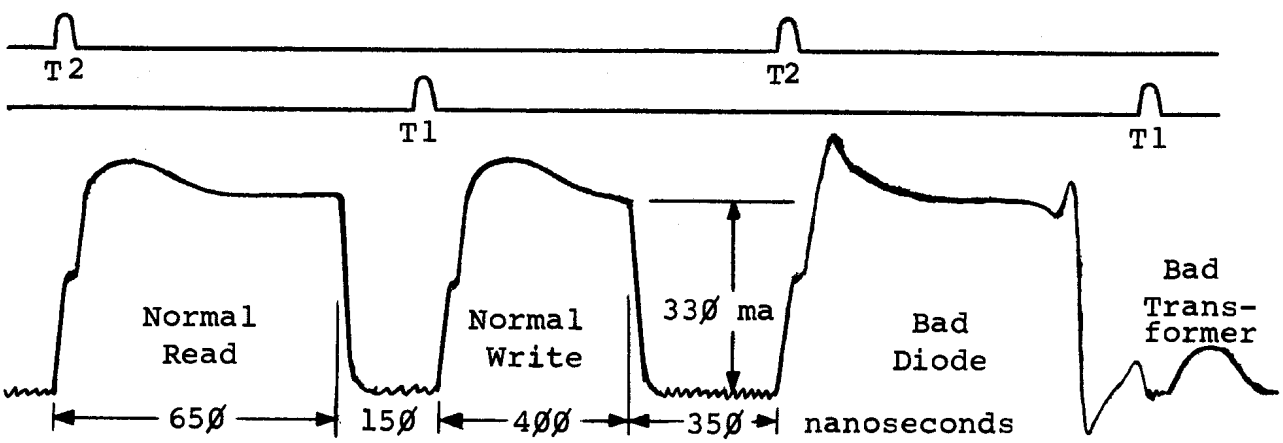

Figure 4. Representative Read and Write Current Waveforms.

Observe the X axis read and write current waveforms by placing the current probe around the yellow wire from MCØ9N. These should be the same as those for the Y axis. If the amplitude has not already been set, adjust it for 33Ø milliamperes with the inside G8Ø8 in the power supply. Be sure all malfunctions are corrected in both axes before proceeding further.

CLAMPS

First Stage Clamp

Check the first stage clamp voltage with respect to -15 volts. Set the voltmeter to the 6 volt dc scale, place the negative probe on the -15 volt bus (B terminals), and look at terminals MA31M and MB3ØM. Each should read approximately 4.Ø volts. If different, check the circuit for low-resistance shorts.

Second Stage Clamp

Check the second stage clamp voltage with respect to -15 volts. Change the voltmeter to the 12 volt dc scale and look at terminals MA31N and MB3ØN with the positive probe. The meter should read approximately 7.2 volts. If not, adjust it to this value with the lower potentiometer on the GØØ8 in MB31.

Now place the oscilloscope voltage probe on terminals E and F of every sense amplifier in MA25-31 or MB25-3Ø. Both terminals should show identical signals at +8.Ø volts dc. Readjust the second stage clamp voltage for this operating level if it is different. If any individual GØØ7 Sense Amplifiers are at different levels, check both the first and second stage clamp voltages at terminals M and N, respectively, to be sure they are the same as the other modules. If not, remove and check the module.

STATIC BALANCE

Remove the sense lines from the GØØ7 sense amplifiers, set the voltmeter to the Ø.3 volt dc scale and measure the voltage between terminals E and F of all the sense amplifiers in MA25-31 and MB25-30. These should be within ± 25 millivolts of each other, but may be as much as 75 millivolts if the memory has been tuned before. If more than 75 millivolts, adjust the balance potentiometer R4 on the module for a minimum voltage. If a good balance cannot be obtained, the module must be repaired. Before removing it, check the first and second stage clamp voltages to see if they are different from the other sense amplifiers.

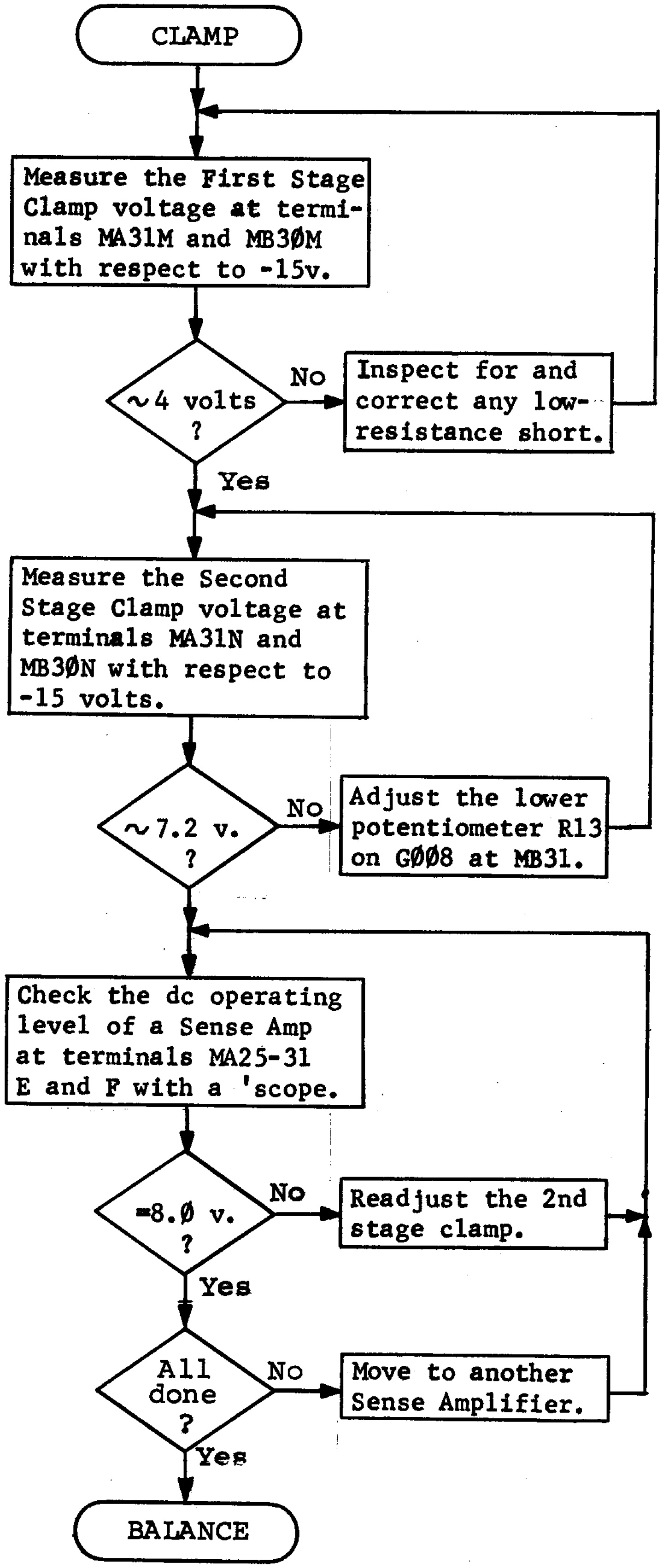

Figure 5. Clamp Procedure Flow Diagram.

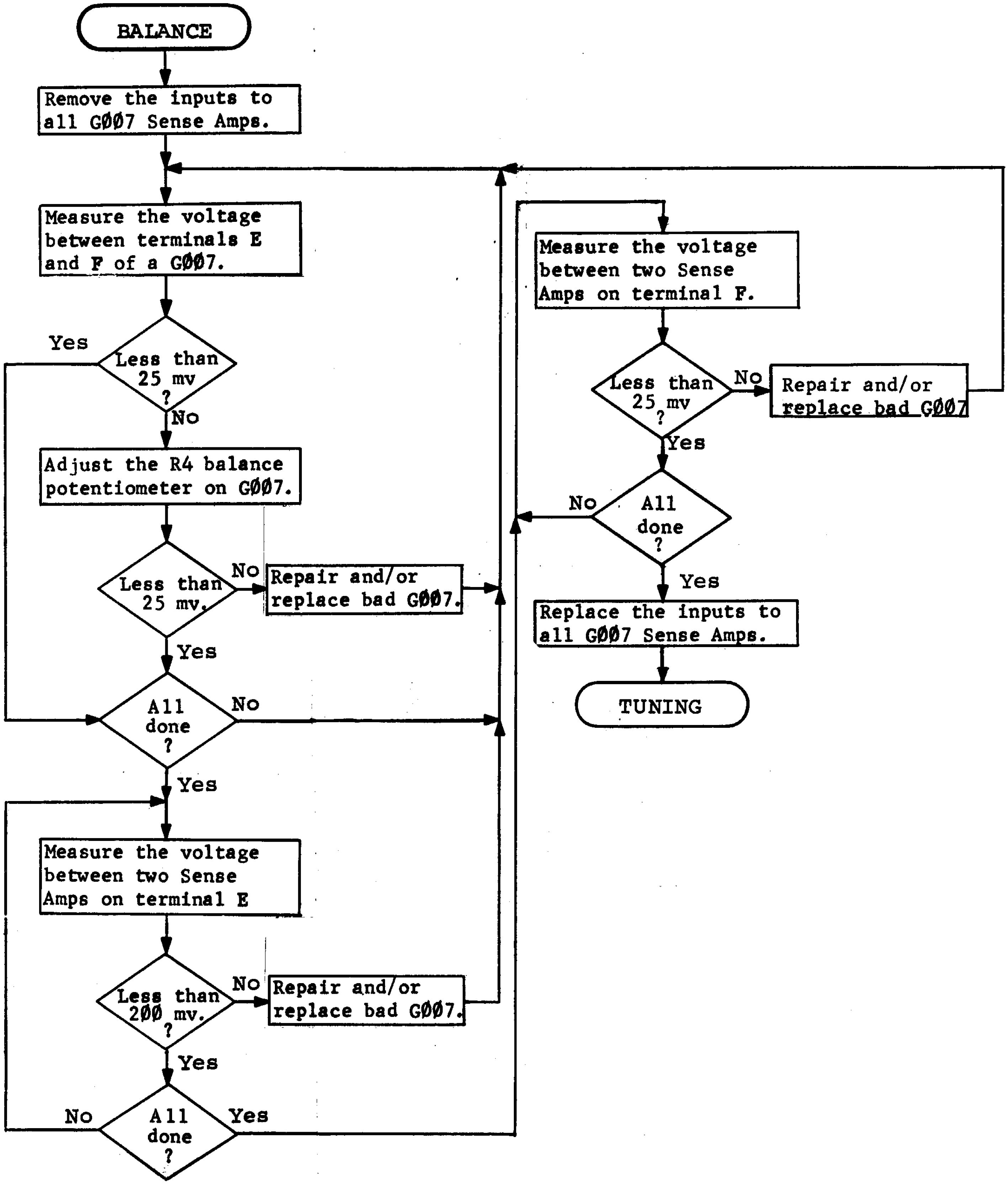

Figure 6. Static Balance and DC Tracking Procedure Flow Diagram

DC TRACKING

With the inputs of all the sense amplifiers open, measure the voltage difference between the modules on terminals E and on terminals F. Set the voltmeter on the Ø.3 volt dc scale and put one probe on terminal E of some sense amplifier such as bit Ø in MA25. Then look at terminal E of the other sense amplifiers, being careful about the polarity. The reading between the highest and the lowest must not exceed 2ØØ millivolts. If any module is more than 2ØØ millivolts from the others, recheck its static balance and readjust if necessary. If it is still more than 2ØØ millivolts from the others, it must be removed and repaired.

Repeat the above process for terminals F of all the sense amplifiers. When finished, connect the core sense lines to the modules. Use drawing BS-D-8M-Ø-15 to locate any specific sense amplifiers.

SLICE VOLTAGE

Set the voltmeter to the 12 volt dc scale and measure the slice voltage between ground and MA31H. It should be +7.2 volts (Ø.8 volts less than the sense differential amplifier dc levels). If different, adjust the upper potentiometer on the GØØ8 at MB31 for this voltage.

SENSE AMPLIFIER TUNING

Replace the oscilloscope current probe with the second voltage probe, and set the channel 1 gain to 1 volt per centimeter. Now look at the slicer output, terminal J, of all the sense amplifiers in MA 25-31 and MB25-3Ø. A dc level of +Ø.7 volts should be observed. Place the channel 2 probe on terminal E, then F, of the same module and check that there is no slicer response during the core=Ø responses of the amplifier. Be sure all sense amplifiers are checked, and that the core=Ø response of the amplifier does not exceed Ø.5 volts.

With probe 1 on MA25J and probe 2 on MA25E (bit Ø), place a temporary jumper from ground to MC21D. (This is the bit Ø inhibit driver: the jumper disables it, causing a 1 to be written in this bit throughout the memory). The core=1 response of the amplifier should now be seen on channel 1.

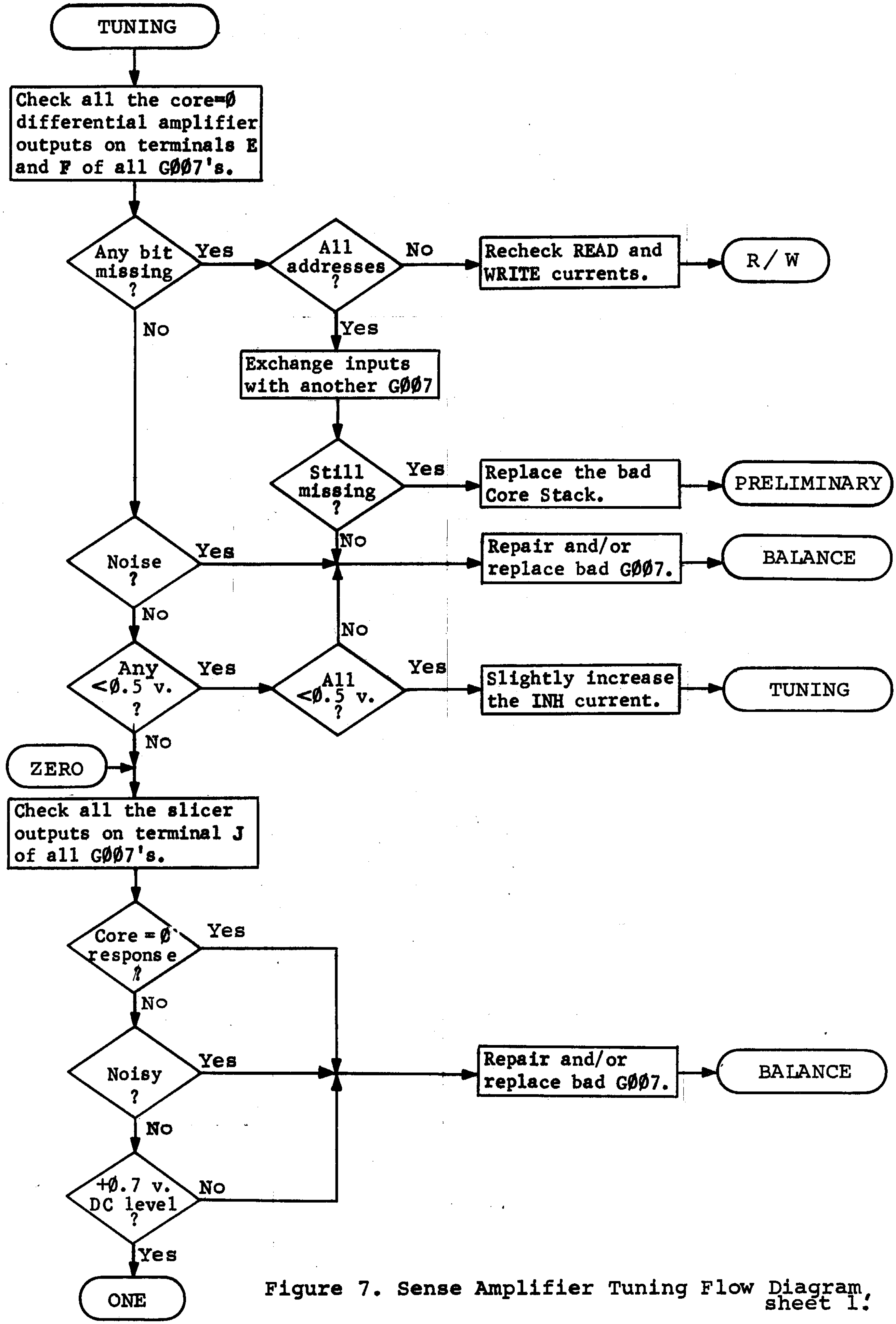

Figure 7. Sense Amplifier Tuning Flow Diagram, sheet 1.

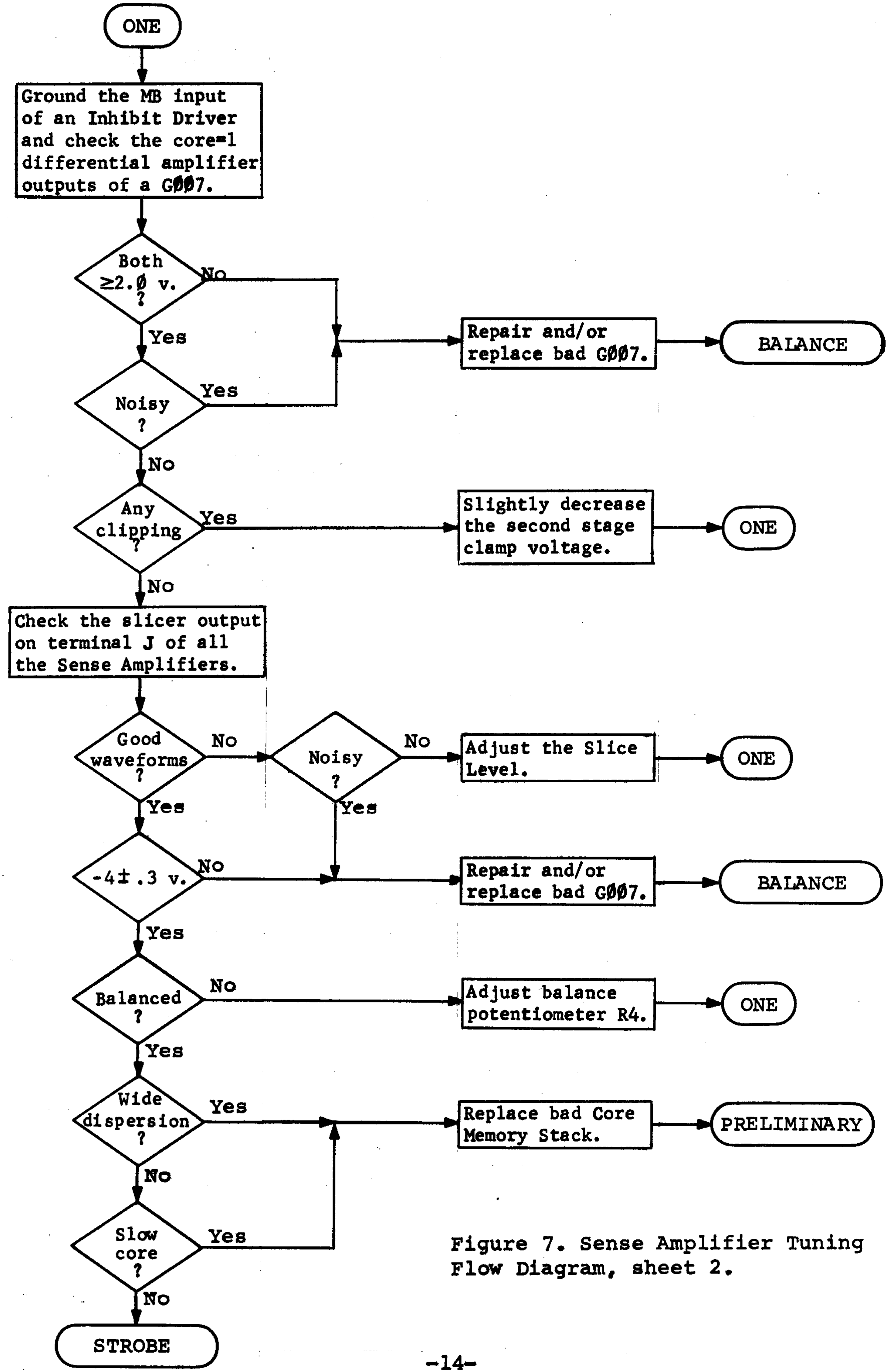

Figure 7. Sense Amplifier Tuning Flow Diagram, sheet 2.

Check that the amplitude of this signal is at least 2 volts, and that no core=Ø responses are produced. The slicer output must have a negative trapazoidal wave for each core=1 response, both negative and positive. See Figure 7 for representative waveforms.

Check the slicer output waveform on terminal J carefully. Its amplitude must go to -4.Ø ± Ø.3 volts. Its width, at the +Ø.7 volt dc level, must equal the width of the core=1 response at the +7.2 volt slice level. There should be a little time jitter in the rising and falling times: this should equal the same time jitter of the core=1 output at the slice level caused by differences of core response. This is called the core dispersion.

If the sense amplifier is both statically and dynamically balanced, then each half of the differential amplifier and slicer will have equal gain and two equal response waveforms will be produced as the computer cycles through the alternating core arrangement. Slightly readjust the potentiometer on the sense amplifier to minimize the difference between the two falling and rising waveforms: try to get the rising waveforms to coincide. If the sense amplifier cannot be dynamically balanced, it must be removed and repaired.

If any core has a slow response time, the falling waveform will be delayed and/or distorted (See Figure 8). If this occurs, the core stack must be rejected. To look at a specific location, connect a temporary jumper from ground to PD18D, shorting out the COUNT PC pulse. Then set the switch register to the address desired, press LOAD ADDRESS, and finally press START.

If there is a lot of time jitter in the falling and rising waveforms, it can be caused by excessive core dispersion, poor common mode rejection in the differential amplifiers, or read and write currents that are too great or which do not change linearly. Poor common mode rejection can be recognized because other sense amplifiers will not show this problem. When this occurs, the sense amplifier must be removed and repaired. When the problem is in the memory, examine the read and write current waveforms carefully. If they are smooth and the proper size (33Ø milliamperes), then the core stack has too much dispersion and it must be rejected. However, try a smaller read and write

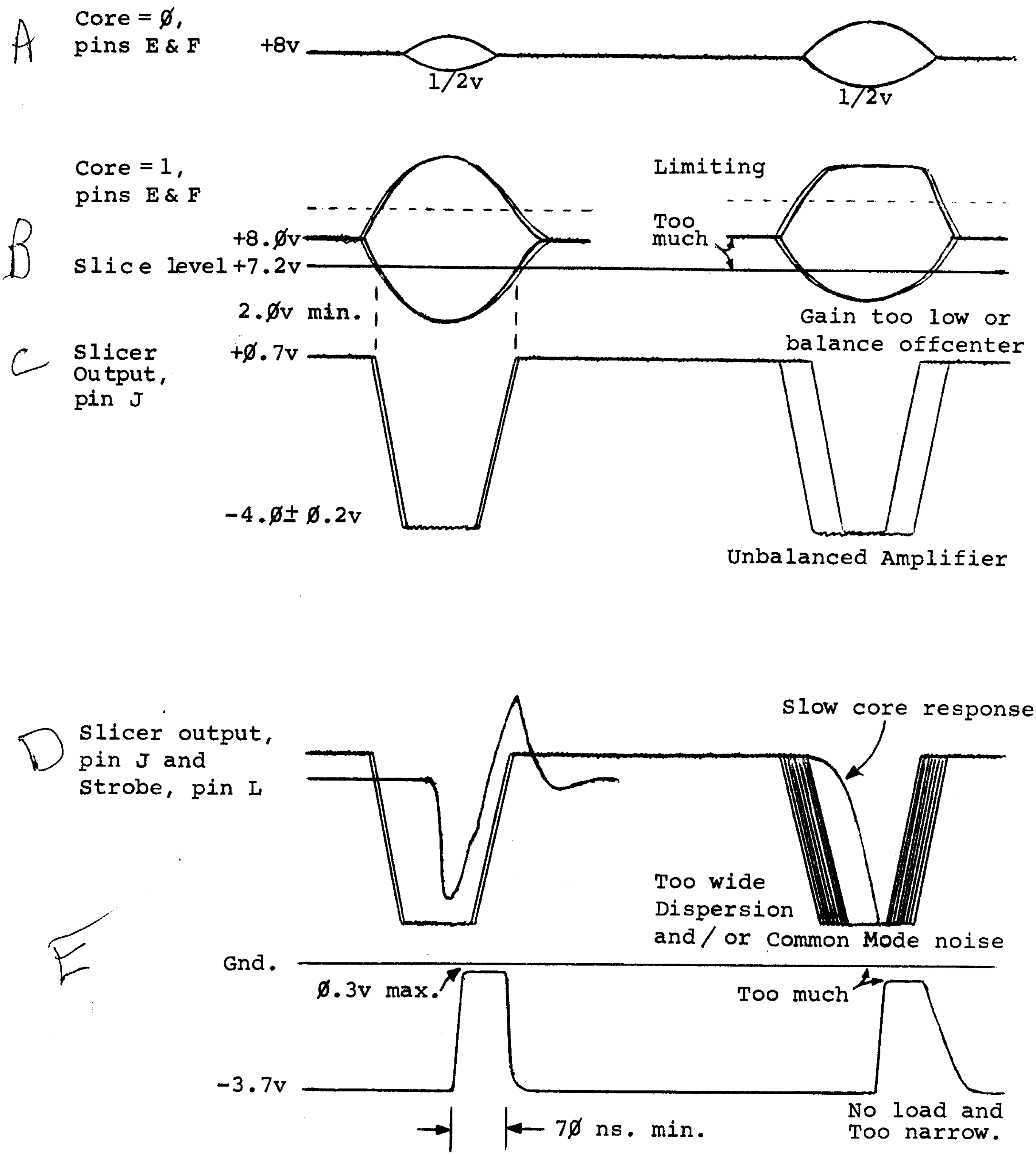

Figure 8. Typical Sense Amplifier Output Waveforms

current (and consequently a smaller inhibit current) and see if this improves the slicer waveforms. (Be sure you can get a 2 volt core=1 response from the differential amplifiers).

Repeat the above process for every bit, placing the jumper and probes at the locations listed below.

Bit	Ground Jumper	Probe 1 (slicer)	Probe 2 (amplifier)
Ø	MC21D	MA25J	MA25E or F
1	MC21T	MB25J	MB25E or F
2	MC22D	MA26J	MA26E or F
3	MC22T	MB26J	MB26E or F
4	MC24D	MA27J	MA27E or F
5	MC24T	MB27J	MB27E or F
6	MD21D	MA28J	MA28E or F
7	MD21T	MB28J	MB28E or F
8	MD22D	MA29J	MA29E or F
9	MD22T	MB29J	MB29E or F
1Ø	MD24D	MA3ØJ	MA3ØE or F
11	MD24T	MB3ØJ	MB3ØE or F
P	MC25T	MA31J	MA31E or F

STROBE

Turn the POWER switch off, replace the B36Ø in MD2Ø, and ground MD24T with a temporary jumper. Turn the POWER switch back on, and press START. Place probe 1 on MB3ØJ and observe the output of the bit 11 slicer. Place probe 2 on MB3ØT and observe the MEMORY STROBE pulse. Adjust the delay line on the B36Ø at MD2Ø until the leading edge of the MEMORY STROBE pulse occurs at or just past the midpoint of the slice output. Refer to Figure 8D for typical waveforms.

Check the SA11 pulse output by moving probe 1 to MB3ØK. The pulse must go positive to -Ø.3 volts at least, and must be at least 8Ø nanoseconds wide. If not, the sense amplifier module must be removed and repaired. Then check all the other output pulses by grounding the corresponding inhibit driver inputs. (Note that the instruction register decoder may require ground jumpers on PB27H, PB27F, and PB27L in order to cycle when grounding bits Ø, 1, and 2).

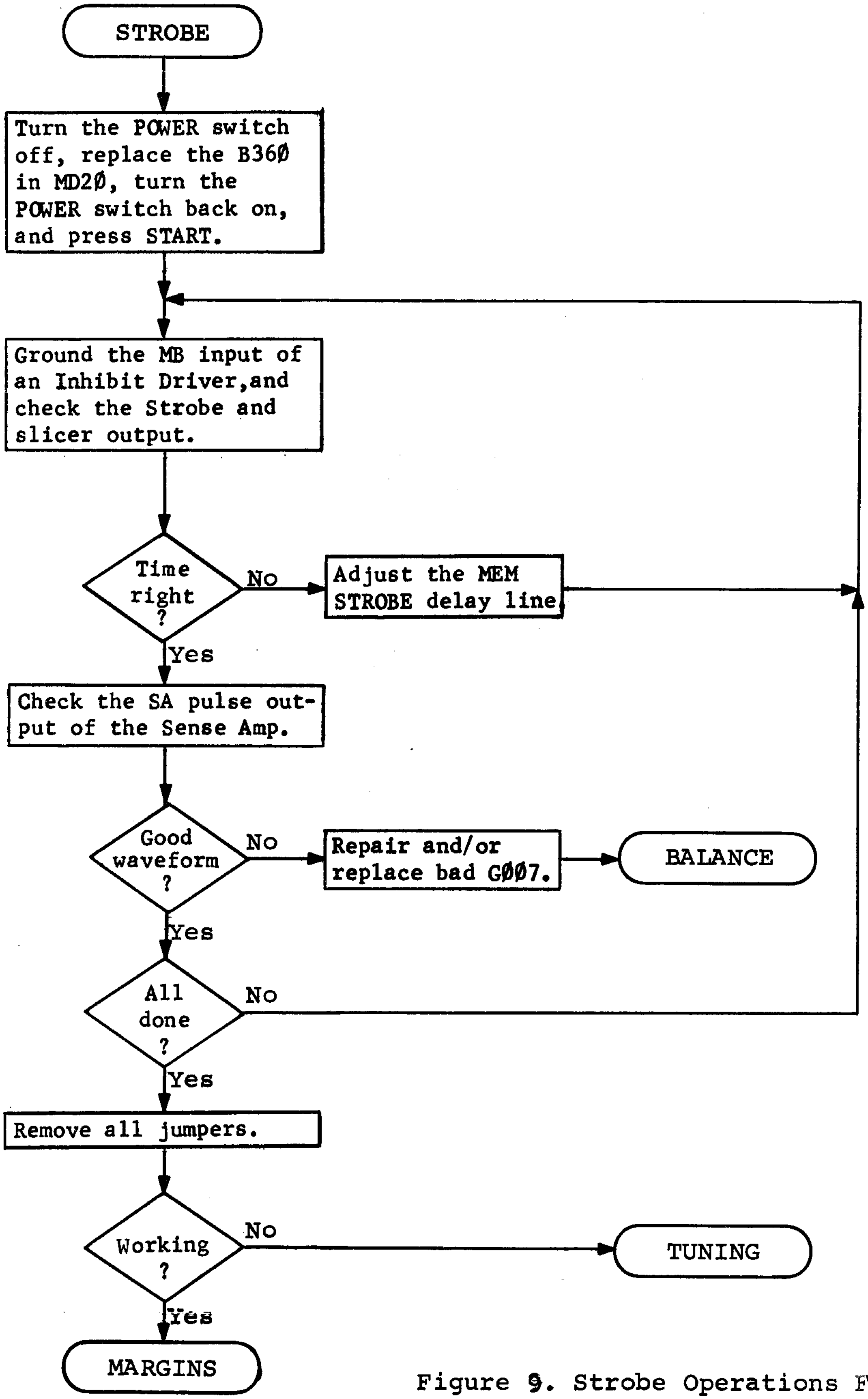

Figure 9. Strobe Operations Flow Diagram

Bit	Ground Jumper	Probe 1 (pulse output)
Ø	MC21D	MA25K
1	MC21T	MB25K
2	MC22D	MA26K
3	MC22T	MB26K
4	MC24D	MA27K
5	MC24T	MB27K
6	MD21D	MA28K
7	MD21T	MB28K
8	MD22D	MA29K
9	MD22T	MB29K
1Ø	MD24D	MA3ØK
11	MD24T	MB3ØK
P	MC25T	MA31K

Remove all jumpers when finished. Then check that both 1's and Ø's can be deposited and examined throughout the memory.

MARGINS

If the ASR 33 or other paper tape reader is available and working, first load the RIM Loader subroutine into memory (see Appendix 1), then read in the checkerboard-low tape. If a paper tape reader is not available, load this program in memory manually. Set the Switch Register (SR) to ØØØ1 and press LOAD ADDRESS, then set the SR to Ø1ØØ* and press START.

Place probe 1 on the slice level bus (H terminals in MA25-31 and MB25-30) and probe 2 on the output of some differential amplifier (terminal E or F in MA25-31 or MB25-3Ø). Set both channels for a gain of 2 volts per centimeter with ground reference on the lowest grid line.

Turn the SENSE AMP switch on the memory wing to MC, then very slowly decrease the +1Ø volt marginal voltage. When the program halts at location 71, record the contents of the ACCUMULATOR indicators (the bit that is on or off is the bit (sense amplifier) that failed) and the marginal voltage. Then return the marginal voltage to +1Ø volts and press CONTINUE.

* For EMI or Ferroxcube core memories. Refer to the Maindec 8Ø2 write-up if other memories are used.

The computer will halt again at location 74, with the ACCUMULATOR indicators containing the address where the error occurred. The sense amplifiers must be able to operate with the marginal voltage reduced 5.5 volts (to +4.5 volts), and normally will operate 6 volts below normal (at +4 volts).

Press CONTINUE again to resume testing, and slowly increase the +10 volt marginal voltage until the program again halts at location 71. Once again note which single bit in the ACCUMULATOR indicaters is on or off, decrease the marginal voltage to +1∅ volts, then press CONTINUE. Now note the address, and press CONTINUE again to resume testing. The sense amplifiers must be able to operate with the marginal voltage increased 5.5 volts (to +15.5 volts), and normally will operate 6 volts above normal (at +16 volts).

If the voltage spread is at least 11 volts and centered at +1∅ volts, then the memory is working passably (it's working well if the spread is 12 volts or more). If the spread is reasonably wide but not centered, set the marginal voltage to whichever margin it will work at, then change the slice level until the program fails at this point. Return the marginal voltage to normal, press CONTINUE twice to restart the program, and vary the marginal voltage to the other extreme until the program again fails. In this manner the marginal spread can be centered using the slice level.

Rebalancing a sense amplifier can also help it to meet the marginal conditions. With the program running at normal marginal voltage, place probe 1 on terminal J of the sense amplifier that fails at high margins and observe the slicer output. Then place probe 2 on the MEMORY STROBE bus (terminal L) and adjust the two traces for a common ground reference. Now increase the marginal voltage and observe the slicer output move to the left as the sense amplifier speeds up. When the program fails (the trailing edge of the strobe pulse will occur with the trailing edge of the slicer output), reduce the marginal voltage a little bit and restart the program (by pressing CONTINUE twice), then adjust the balance potentiometer on the sense amplifier module until the two traces at the trailing edge of the slicer output are as nearly together as possible. Then increase the marginal voltage again and see if it has improved enough. If it has, then check the lower marginal voltage limit to see if it has changed.

The same procedure can be used to improve the lower marginal voltage limits. In this case, the slicer output moves to the right as the sense amplifiers slow down.

If the same bit fails at both the upper and lower limits, it is due to either a poor core output in that plane, or a low sense amplifier gain, or both. Place probe 1 on terminal J of this module, and probe 2 on all the other slicer outputs (terminal J) and observe the relative widths of the waveforms when the program is running at normal margins. Find the sense amplifier with the widest response, and swap the two modules (be sure to turn the POWER switch off). Then check to see how much this has improved the margins.

Changing the read/write current, inhibit current, and/or the second stage clamp voltage can improve the marginal voltage limits slightly if done correctly. However, once any of these are changed, the slice level and probably one or more of the others must also be readjusted and a new set of marginal voltage limits established. Increasing the read and write currents increases the core=1 response and the noise in the rest of the core. The optimal inhibit current will produce the smallest core=Ø response (as seen on terminals E and F). The second stage clamp voltage changes the operating level of both the second stage of the differential amplifiers and the slicer, with only small changes in gain and common mode noise rejection. The second stage clamp should only be changed slightly if limiting is noticed on one side of any sense amplifier output at either terminal E or F.

APPENDIX 1

RIM LOADER

The readin mode (RIM) loader is a short program that reads the contents of another program tape and loads it into memory. The program tape must be punched in the RIM format, i.e., first an absolute address and then the information to be placed in that address. This program will only work with the 33 ASR reader, and must be loaded into memory manually.

Location	Content	Mnemonic	Comments
77ØØ	6Ø32	KCC	/Clear ac and reader flag.
77Ø1	6Ø31	KSF	/Skip if flag is set.
77Ø2	5Ø31	JMP .-1	/Do it again if flag is clear.
77Ø3	6Ø36	KRB	/Read buffer when filled.
77Ø4	71Ø6	CLL RTL	/Clear link and rotate left twice.
77Ø5	7ØØ6	RTL	/Rotate left twice again for checks.
77Ø6	751Ø	SPA	/Skip if not leader or trailer.
77Ø7	53Ø1	JMP 77Ø1	/Repeat if leader or trailer.
771Ø	7ØØ6	RTL	/Rotate left twice if program.
7711	6Ø31	KSF	/Skip if flag is set.
7712	5311	JMP .-1	/Do it again if flag is clear.
7713	6Ø34	KRS	/Read buffer without clearing ac.
7714	742Ø	SNL	/Skip if link is set.
7715	372Ø	DCA I .+3	/Deposit information in address.
7716	332Ø	DCA .+2	/Deposit address.
7717	53ØØ	JMP 77ØØ	/Repeat the entire program.
772Ø	ØØØØ	Z	/Storage for absolute address.

APPENDIX 2

CHECKERBOARD

The following programs are Checkerboard-Low and Checkerboard-High. These may be loaded manually into memory in the event that the program tapes are not available, the RIM Loader is not working, or these programs do not work correctly. For a full description, flow chart, and operating instructions, refer to the MAINDEC 8Ø2 Memory Checkerboard Test manual.

Location			Instruction		
Low	High	Tag	Low	High	Mnemonic
1	745Ø		7121	7121	CLL CML IAC
2	7451		31Ø7	3353	DCA COM
3	7452	STX	76Ø4	76Ø4	LAS
4			1111		TAD MUD
5	7453		31Ø5	3354	DCA PAT
6			1111		TAD MUD
7	7454		31Ø6	3355	DCA SA
1Ø	7455	STB	21Ø7	2353	ISZ COM
11	7456		11Ø7	1353	TAD COM
12	7457		Ø1Ø3	Ø352	AND DOT
13	746Ø		764Ø	764Ø	SZA CLA
14	7461		11Ø2	1351	TAD NOT
15	7462		1Ø77	135Ø	TAD HOT
16	7463		3Ø25	3272	DCA Y
17		STC	11Ø1		TAD POT
	7464	STC		1347	TAD SOT
2Ø	7465		11Ø6	1355	TAD SA
21	7466		765Ø	765Ø	SNA CLA
22	7467		5ØØ3	5252	JMP STX
23	747Ø		11Ø5	1355	TAD PAT
24	7471		Ø1ØØ	Ø346	AND ROT
25	7472	Y	ØØØØ	ØØØØ	
26	7473		11Ø2	1351	TAD NOT
27	7474		1Ø77	135Ø	TAD HOT
3Ø	7475		3Ø33	33ØØ	DCA X
31	7476		11Ø5	1354	TAD PAT
32	7477		Ø1Ø3	Ø352	AND DOT

33	7500	X	0000	0000	
34	7501		7040	7040	CMA
35	7502		7420	7420	SNL
36	7503		5047	5314	JMP CCK
37	7504		3506	3755	DCA I SA
40	7505	STD	2106	2355	ISZ SA
41	7506		2105	2354	ISZ PAT
42	7507		1106	1355	TAD SA
43	7510		0104	0345	AND BOT
44	7511		7650	7650	SNA CLA
45	7512		5017	5264	JMP STC
46	7513		5031	5276	JMP X-2
47	7514	CCK	3110	3356	DCA WRD
50	7515		1506	1755	TAD I SA
51	7516		7041	7041	CMA IAC
52	7517		1110	1356	TAD WRD
53	7520		7640	7640	SZA CLA
54	7521		5070	5335	JMP CC3
55	7522		1110	1356	TAD WRD
56	7523		7040	7040	CMA
57	7524		3506	3755	DCA I SA
60	7525		1506	1755	TAD I SA
61	7526		7001	7001	IAC
62	7527		1110	1356	TAD WRD
63	7530		7640	7640	SZA CLA
64	7531		5070	5335	JMP CC3
65	7532	CC2	1110	1356	TAD WRD
66	7533		7100	7100	CLL
67	7534		5037	5304	JMP STD -1
70	7535	CC3	1506	1755	TAD I SA
71	7536	E1	7402	7402	HLT
72	7537		7200	7200	CLA
73	7540		1106	1355	TAD SA
74	7541	E1A	7402	7402	HLT
75	7542		7300	7300	CLA CLL
	7543			7300	CLA CLL
76	7544	CC4	5065	5332	JMP CC2
77	7550	HOT	7640	7640	/Constant
100	7546	ROT	0200	0200	/Constant
101		POT	0100	0100	/Constant
102	7551	NOT	0010	0010	/Constant
103	7552	DOT	0002	0002	/Constant

1Ø4	7545	BOT	ØØ77	ØØ77	/Constant
1Ø5	7554	PAT	ØØØØ	ØØØØ	/Variable
1Ø6	7555	SA	ØØØØ	ØØØØ	/Variable
1Ø7	7553	COM	ØØØØ	ØØØØ	/Variable
11Ø	7556	WRD	ØØØØ	ØØØØ	/Variable
111		MUD	Ø112		/Constant
	7547	SOT		Ø4ØØ	/Constant