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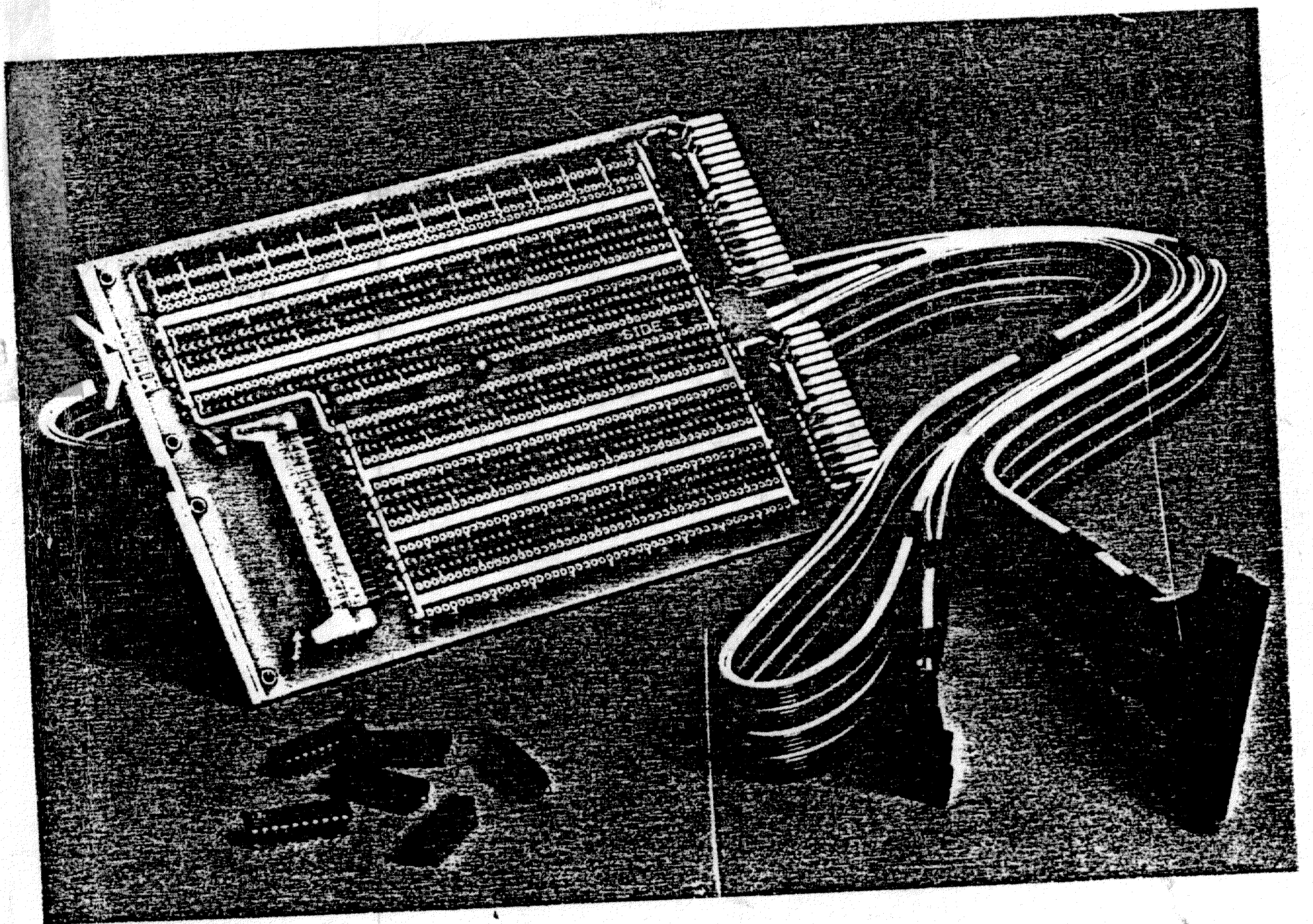
chipkit

users manual

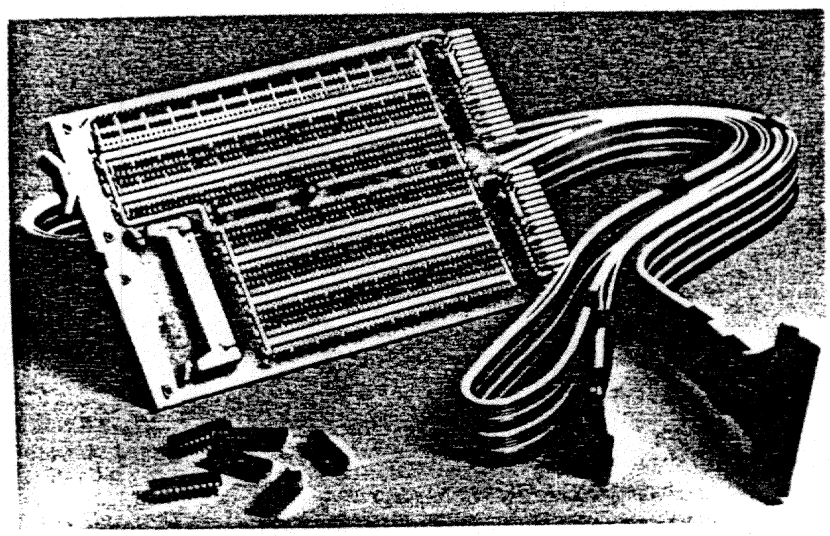


CONTENTS

DC010 DIRECT MEMORY ACCESS LOGIC

INTRODUCTION

This Users Manual contains descriptions, specifications, and circuit diagrams for the five integrated circuits available in CHIPKITS for use in LSI-11 bus interfaces. The bus receiver and bus driver chips usually used with the LSI-11 are also covered, and the W9512 wire wrappable module included with the designers kits is described.



DCK11-AC and AD CHIPKITS include LSI IC chips, a wire wrappable board, and an interface cable.

The DCK11 series of proprietary LSI integrated circuits, developed by DIGITAL for its own use, is now available to LSI-11 users. These ICs, available in sets called CHIPKITS, make design of LSI-11 bus interfaces easier than ever. Prior to these kits, a designer of custom LSI-11 program control or Direct Memory Access (DMA) interfaces had two alternatives: modify a standard product or design a new one. Now there is a third choice that will be the best—the CHIPKIT. The kits contain the ICs needed to build the foundation of nearly any LSI-11 interface, and are available either with or without a DIGITAL wire wrappable board and plug-in cable. For spares or special applications, the individual ICs are available in tubes of 18 of one type.

The CHIPKITS minimize the chip count required to implement bus circuitry. This permits the designer to build an interface foundation on the double-height wire wrappable board provided, and still have ample room left for his special circuitry. The compraratively small chip count results in backplane space savings, increased system reliability, lower system cost, and a greater opportunity for value to be added by the CHIPKIT customer to the finished product.

The CHIPKITS in this program are:

DCK11-AC — Designers Program Control Bus Interface CHIPKIT, consisting of:

- 1 DC003 Interrupt Chip
- 1 DC004 Protocol Chip
- 4 DC005 Transceiver/Address Decoder/Vector Select Chips
- 1 W9512 Double-height, extended-length, wire wrappable module
- 1 BC07D-10 ten-foot, 40-conductor plug-in cable

DCK11-AA — Program Control Bus Interface CHIPKIT, consisting of the six chips of the above DCK11-AC, but no module or cable.

These kits are ideal for building the foundations of program control bus interfaces to the LSI-11. They are functionally similar to DIGITAL's DRV11-P Bus Foundation Module, an assembled, ready-to-use option.

DCK11-AD — Designers DMA Bus Interface CHIPKIT, consisting of:

- 1 DC003 Interrupt Chip
- 1 DC004 Protocol Chip
- 4 DC005 Transceiver/Address Decoder/Vector Select Chips
- 2 DC006 Word Count/Bus Address Chips
- 1 DC010 DMA Control Chip
- 1 W9512 Double-height, extended-length, wire wrappable module
- 1 BC07D-10 ten-foot, 40-conductor plug-in cable

DCK11-AB — DMA Bus Interface CHIPKIT, consisting of the nine chips of the above DCK11-AD, but no module or cable

These kits are ideal for building the foundations of DMA bus interfaces to the LSI-11. They are functionally similar to DIGITAL's DRV11 B General Purpose DMA Interface Module.

Additional Information

To learn more about CHIPKIT applications, pricing, etc., call Digital's Sales Support experts, 9:00 AM to 5:00 PM Eastern time: (603) 884-7009.

Brief Specifications of CHIPKIT Integrated Circuits

Absolute Maximum Ratings:

Supply Voltage (Vcc)	+7V
Input Voltage (VI)	+5.5V
Operating Temp. (Ta)	+32°F to +158°F (0°C to +70°C)
Storage Temp. (Ts)	−149°F to +302°F (−65°C to +150°C)

Recommended Operating Conditions:

Supply Voltage (Vcc)	4.75V (Min.) 5.0V (Norm), 5.25V (Max)
Supply Current (Vcc)	DC003: 140 mA (Max) DC004, DC005: 120 mA (Max) DC006: 170 mA (Max) DC010: 160 mA (Max)
Free Air Temperature	+32°F to +158°F (0°C to +70°C)
Relative Humidity	10% to 95%, non-condensing

Physical Dimensions:

DC003, 18-pin	0.3" center	DEC 19-12730-00
DC004, 20-pin	0.3" center	DEC 19-12729-00
DC005, 20-pin	0.3" center	DEC 19-13040-00
DC006, 20-pin	0.3" center	DEC 19-14035-00
DC010, 20-pin	0.3" center	DEC 19-14038-00
W9512 Wire Wrappable Module	Double height, extended length, single width.	
BC07D-10 Cable	10', 40-conductor ribbon cable, with 40-pin (female) mating connector (H856) installed on one end only; prestripped on other end.	

Detailed specifications, circuit diagrams, pin/signal descriptions, and timing diagrams for each IC follow in this Users Manual.

DC003 Interrupt Logic (DEC #19-12730-00)

The interrupt chip is an 18-pin, 0.762 cm center ×2.349 cm long (max) (0.3 in center × 0.925 in long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisy-chain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high current open-collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{CC} supply is 140 mA.

Figure 1 is a simplified logic diagram of the DC003 IC. Figure 2 shows the test conditions used to derive the data presented in the Electrical Characteristics. Figure 3 shows the timing for the "A" interrupt section while Figure 4 shows the timing for both "A" and "B" interrupt sections. Table 1 describes the signals and pins of the DC003 by pin and signal name.

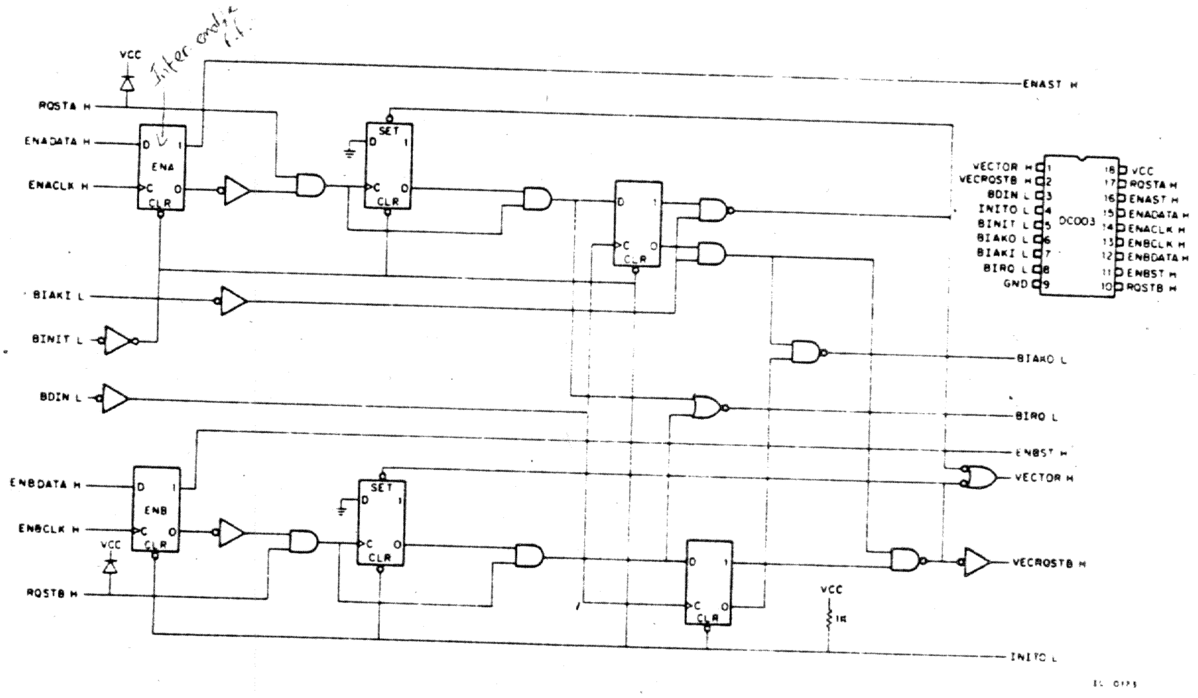


Figure 1 DC003 Simplified Logic Diagram

Table 1 DC003 Pin/Signal Descriptions

Pin	Signal	Spec Group	Description
1	VECTOR H	I	Interrupt Vector Gating. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L.
2	VECRQSTB H	I	Vector Request "B." When asserted, indicates RQST "B" service vector address is required. When unasserted, indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address; VECRQSTB H is normally bit 2 of the vector address.
3	BDIN L	III	Bus Data In. This signal, generated by the processor BDIN, always precedes a BIAK signal.
4	INITO L	I*	Initialize Out. This is the buffered BINIT L signal used in the device interface for general initialization.
5	BINIT L	III	Bus Initialize. When asserted, this signal brings all driven lines to their unasserted state (except INITO L).
6	BIAKO L	II	Bus Interrupt Acknowledge (Out). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated.
7	BIAKI L	III	Bus Interrupt Acknowledge (In). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.

*Open collector with 1K ohm pullup resistor

Table I DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Spec Group	Description
8	BIRQ L	II	Bus Interrupt Request. This signal is generated when this device needs to interrupt the processor. The request is generated by a false to true transition of the RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated interrupt enable or the removal of the associated request signal.
10 17	RQSTB H RQSTA H	III III	Device Interrupt Request. When asserted with the enable flip-flop set, will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.
11 16	ENBST H ENAST H	I I	Interrupt Enable Status. This signal indicates the state of the interrupt enable internal flip-flop which is controlled by the signal ENX (where X is either A or B) DATA H and the ENX (where X is either A or B) CLK H clock line.
12 15	ENBDATA H ENADATA H	I I	Interrupt Enable Data. The level on this line, in conjunction with the ENX (where X is either A or B) CLK H signal, determines the state of the internal interrupt enable flip-flop. The output of this flip-flop is monitored by the ENX (where X is either A or B) ST H signal
13 14	ENBCLK H ENACLK H	I I	Interrupt Enable Clock. When asserted (on the positive edge), interrupt enable flip-flop assumes the state of the ENX (where X is either A or B) DATA H signal line.

Specifications

DC003 Electrical Characteristics

DC003 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	Symbol	Conditions*	Min	Max	Unit
High-level input voltage	V_{IH}	(See Fig. 2A, 2B)	2.0		V
Low-level input voltage	V_{IL}	(See Fig. 2A, 2B)		0.8	V
Input clamp voltage	V_I	$V_{CC} = 4.75$ V $I_I = -18$ mA (See Fig. 2C)		−1.2	V
High-level output voltage	V_{OH}	$V_{CC} = 4.75$ V $I_O = -1$ mA (See Fig. 2A)	2.7		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_O = 20$ mA (See Fig. 2B)		0.5	V
Input current: at maximum input voltage	I_I	$V_{CC} = 5.25$ V $V_I = 5.5$ V (See Fig. 2D)		1	mA
High-level input current	I_{IH}	$V_{CC} = 5.25$ V $V_I = 2.7$ V† (See Fig. 2D)		50	μA
Low-level input current	I_{IL}	$V_{CC} = 5.25$ V $V_I = 0.5$ V‡ (See Fig. 2E)		−0.55	mA
Short-circuit output current	I_{OS}	$V_{cc} = 5.25$ V§‖ (See Fig. 2F)	−40	−100	mA
Supply current	I_{CC}	$V_{CC} = 5.25$ V (See Fig. 2G)		140	mA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

† I_{IH} = 100 μA at pins 12 and 15.

‡ I_{IL} = -2.0 mA at pins 12 and 15.

§ Not more than one output shall be shorted at a time and duration shall not exceed 1 second.

‖ Does not apply to pin 4.

DC003 Bus Driver
(Specification Group II – Open Collector)

Parameter Name	Symbol	Conditions[1]	Min	Max	Unit
Output reverse current	I_{OR}	$V_{CC} = 4.75$ V $V_{OH} = 3.5$ V (See Fig. 2A)		25	μA
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_{SINK} = 70$ mA $I_{SINK} = 16$ mA (See Fig. 2B)		 0.8 0.5	 V V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC003 Bus Receiver
(Specification Group III – High Input Z)

Parameters Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 2A, 2B)	1.53 1.70		V V
Low-level input voltage	V_{IL}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 2A, 2B)		1.30 1.47	V V
Input clamp voltage	V_I	$V_{CC} = 4.75$ V $I_I = -18$ mA $I_I = +18$ mA (pins 10 and 17 only) (See Fig. 2C)		 −1.2 6.25	 V V
High-level input current	I_{IH}	$V_I = 3.8$ V $V_{CC} = 0$ V (Do not do for pins 10 and 17) $V_{CC} = 5.25$ V (See Fig. 2D)		40 40	μA μA
Low-level input current	I_{IL}	$V_I = 0$ V $V_{CC} = 0$ V (Do not do for pins 10 and 17) $V_{CC} = 5.25$ V (See Fig. 2E)		−10 −10	μA μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

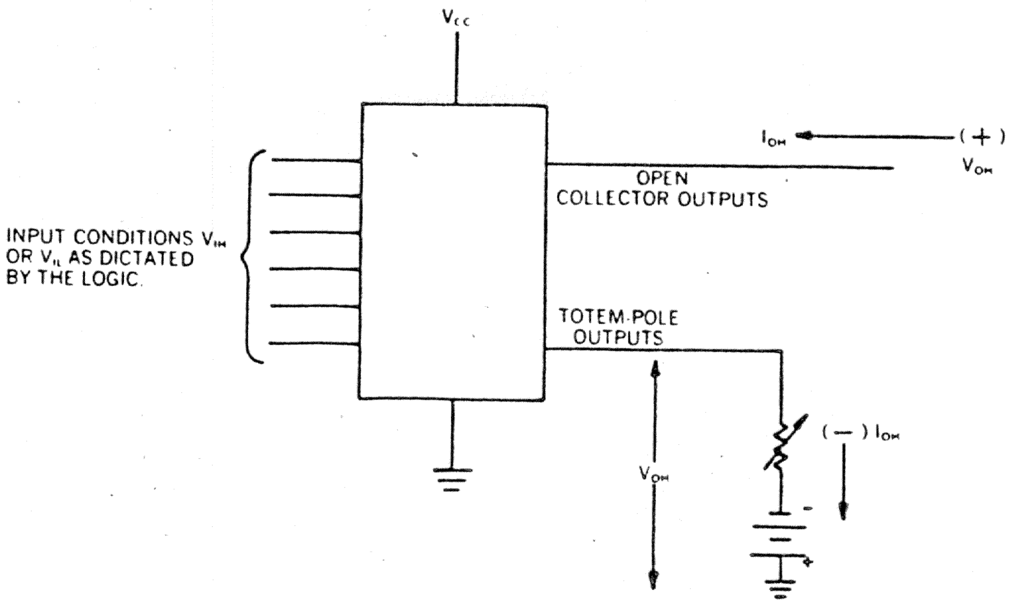


Figure 2A — DC Test Circuit (V_{IH}, V_{IL}, V_{OH}, I_{OH})

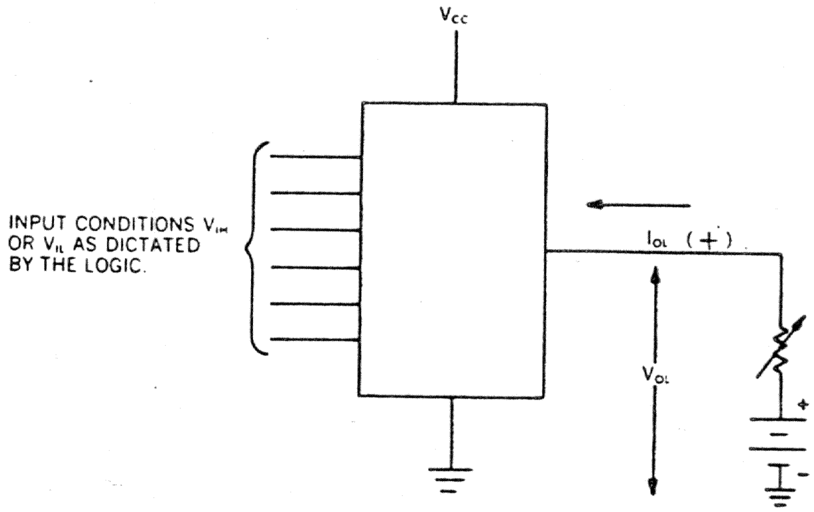


Figure 2B — DC Test Circuit (V_{IH}, V_{IL}, V_{OL})

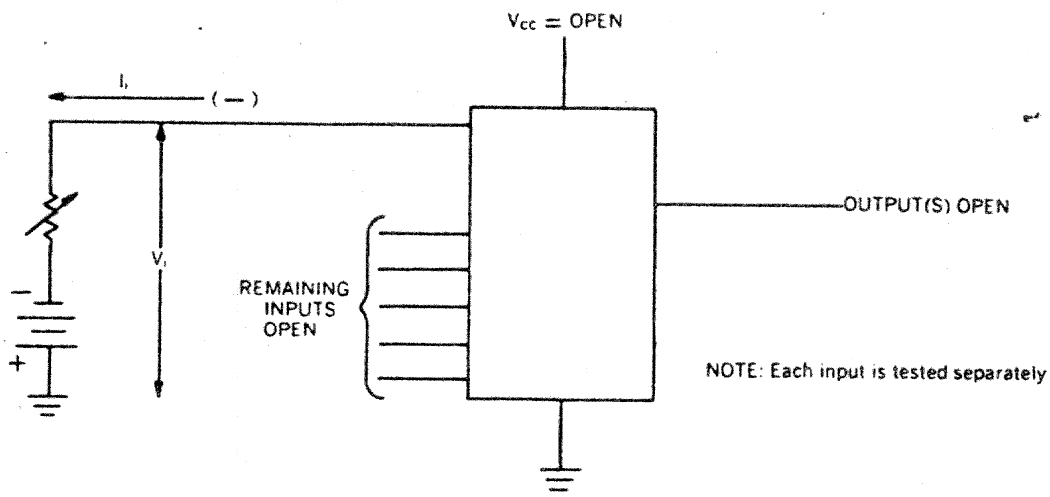


Figure 2C — DC Test Circuit (V_I)

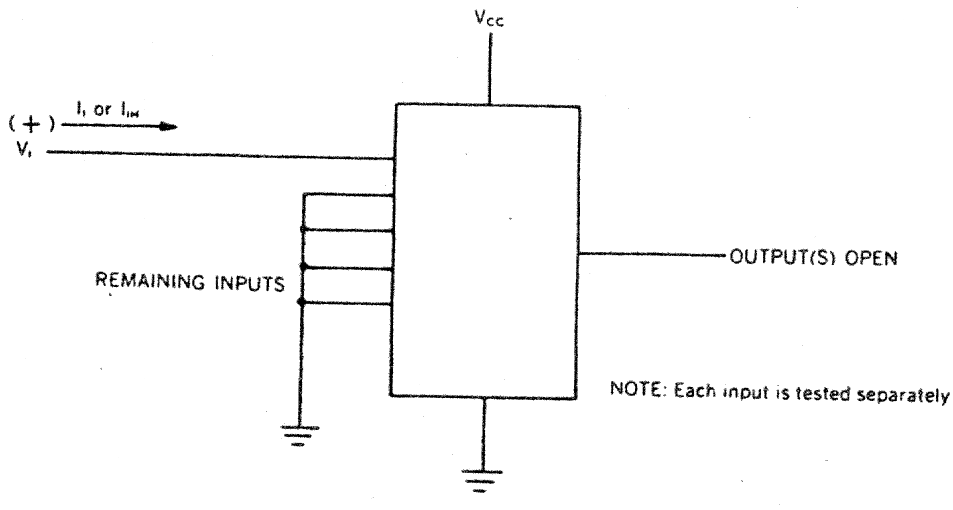


Figure 2D — DC Test Circuit (I_I, I_{IH})

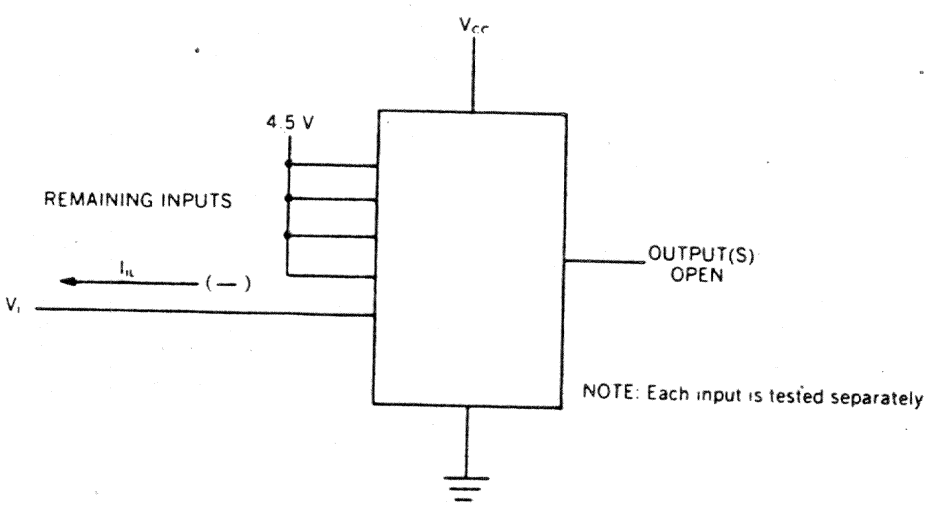


Figure 2E — DC Test Circuit (I_{IL})

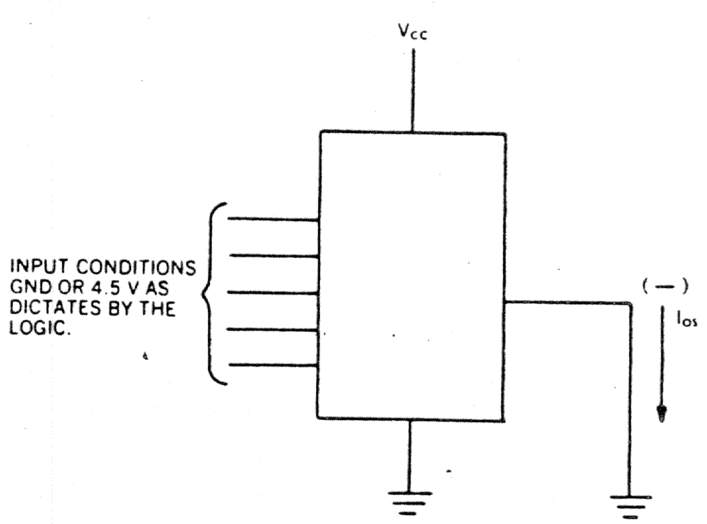


Figure 2F — DC Test Circuit (I_{OS})

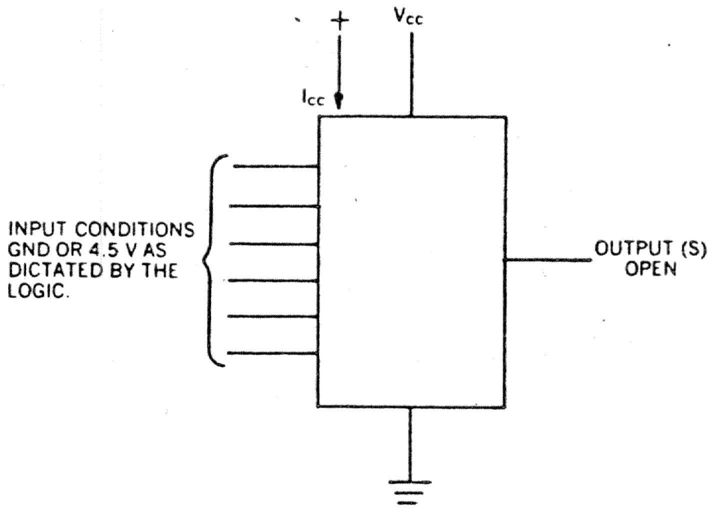


Figure 2G — DC Test Circuit (I_{CC})

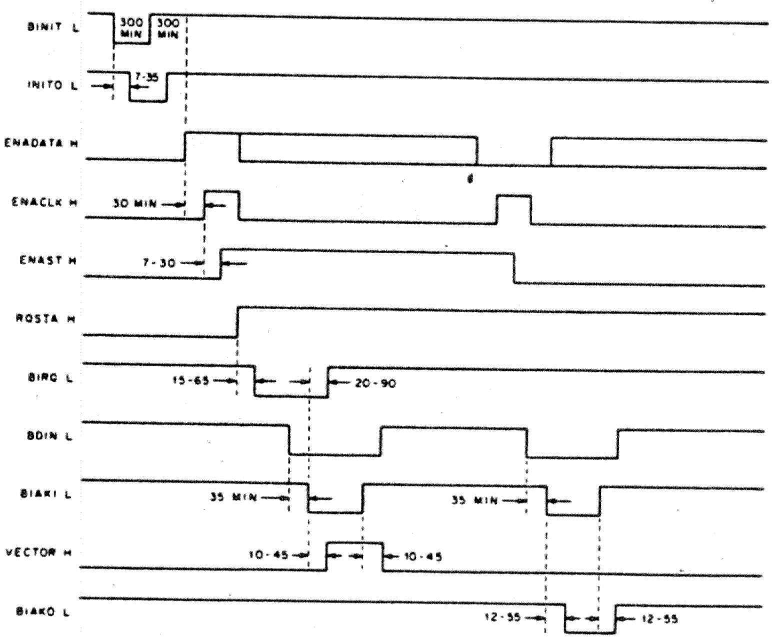
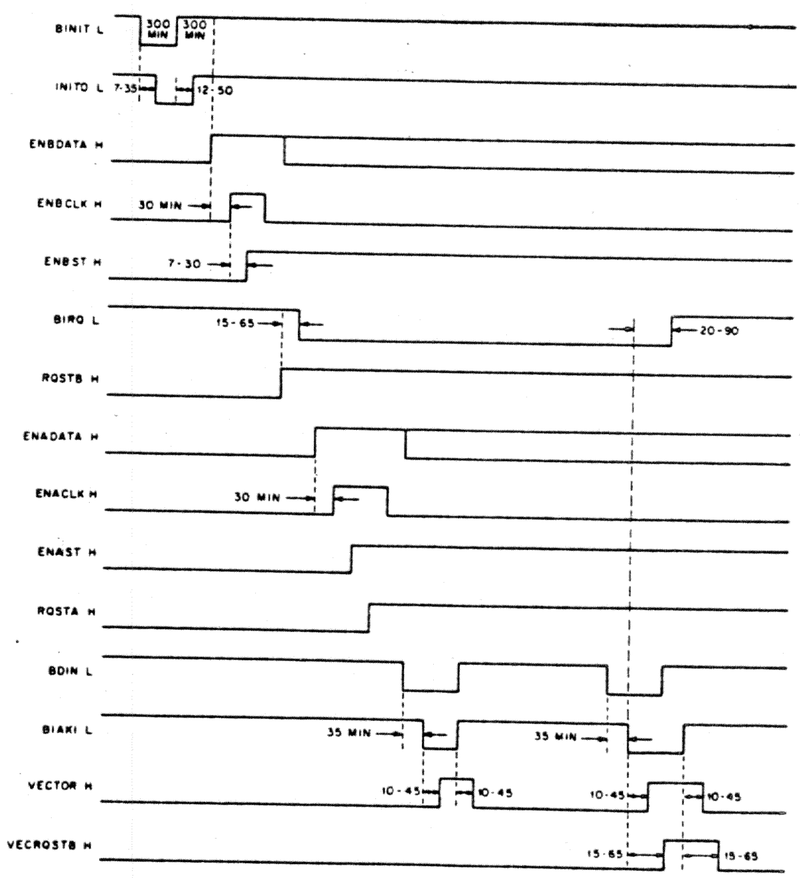


Figure 3 DC003 "A" Interrupt Section Timing Diagram



NOTE
Times are in nanoseconds

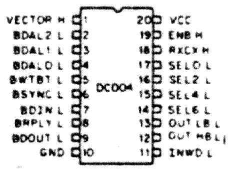
11-4151

Figure 4 DC003 "A" and "B" Interrupt Sections Timing Diagrams

DC004 PROTOCOL LOGIC (DEC #19-12729-00)

The protocol chip is in a 20-pin 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP device that functions as a register selector, providing the signals to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1 K ± 20 percent resistor is necessary. External RCs can be added to vary the delay (see Table 3). Maximum current required from the Vcc supply is 120mA.

Figure 5 is a simplified logic diagram of the DC004 IC. Signal timing with respect to different loads is shown in Table 3 and in Figure 7. Figure 6 shows the test conditions used while Figure 8 shows the loading for the test conditions. Signal and pin definitions for the DC004 are presented in Table 2.



NOTE

The pin names shown in this diagram are for the situation where the DC004 is connected to the internal 3-state bus of the DC005s not connected directly to the LSI-11 bus.

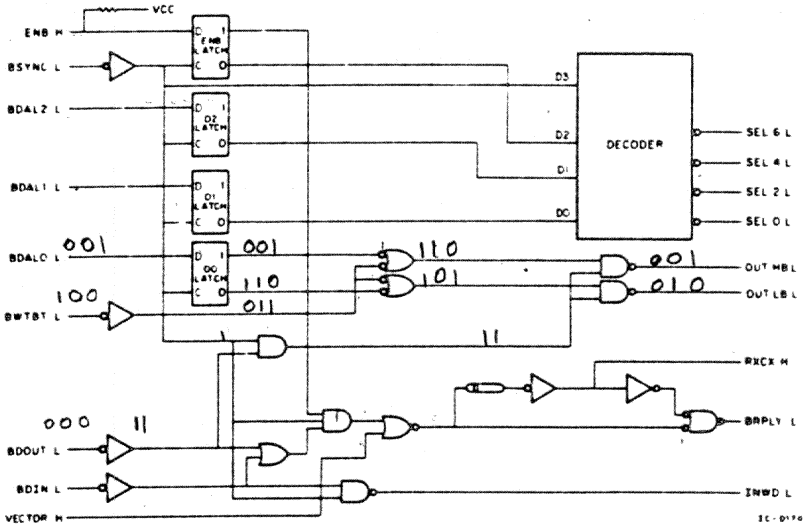


Figure 5 DC004 Simplified Logic Diagram

BDOUT	BWTBT	BDALO	OUT.HB	OUTLB
0	1	0	0	0
0	0	0	0	1
0	0	1	1	0

Table 2 DC004 Pin/Signal Descriptions

Pin	Signal	Spec Group	Description
1	VECTOR H	I	Vector. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	II II II	Bus Data Address Lines. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	II	Bus Write/Byte. While the BDOUT L input is asserted, this signal indicates a byte or word operation: Asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUT LB L and OUT HB L.
6	BSYNC L	II	Bus Synchronize. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	II	Bus Data In. This is a strobing signal to effect a data input transaction. Generates BRPLY L through the delay circuit and INWD L.
8	BRPLY L	III	Bus. Reply. This signal is generated through an RC delay by VECTOR H OR'd with BDIN L or BDOUT L and the AND of BSYNC L and latched ENB H.
9	BDOUT L	II	Bus Data Out. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. Generates BRPLY L through the delay circuit.
11	INWD L	I	In Word. Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUT LB L OUT HB L	I I	Out Low Byte, Out High Byte. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.

Table 2 DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Spec Group	Description
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	I I I I	Select Lines. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted.
18	RXCX H	III	External Resistor Capacitor Node. This node is provided to vary the delay between the BDIN L, BDOUT L, or VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{CC} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	I*	Enable. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

* TTL input with 850 Ω pull-up resistor to VCC.

DC004 Electrical Characteristics

TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	(See Fig. 6A, 6B)	2.0		V
Low-level input voltage	V_{IL}	(See Fig. 6A, 6B)		0.8	V
Input clamp voltage	V_I	$V_{CC} = 4.75$ V $I_I = -18$ mA (See Fig. 6C)		−1.2	V
High-level output voltage	V_{OH}	$V_{CC} = 4.75$ V $I_O = -1$ mA (See Fig. 6A)	2.7		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_O = 20$ mA (See Fig. 6B)		0.5	V
Input current at maximum input voltage	I_I	$V_{CC} = 5.25$ V $V_I = 5.5$ V† (See Fig. 6D)		1	mA
High-level input current	I_{IH}	$V_{CC} = 5.25$ V $V_I = 2.7$ V† (See Fig. 6D)		50	μA
Low-level input current	I_{IL}	$V_{CC} = 5.25$ V $V_I = 0.5$ V (See Fig. 6E)		−0.70	mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.25$ V‡ (See Fig. 6F)	−40	−100	mA
Supply current	I_{CC}	$V_{CC} = 5.25$ V (See Fig. 6G)		120	mA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

† Limits for pin 19 are:
$I_I = 1.40$ mA; $I_{IH} = -2.25$ mA min, −3.85 mA max.
$I_{IL} = -4.5$ mA min, −8.0 mA max.

‡ Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC004 Bus Receiver
(Specification Group II – High Input Z)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	V_{CC} = 4.75 V V_{CC} = 5.25 V (See Fig. 6A, 6B)	1.53 1.70		V V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V V_{CC} = 5.25 V (See Fig. 6A, 6B)		1.30 1.47	V V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA (See Fig. 6C)		−1.2	V
High-level input current	I_{IH}	V_I = 3.8 V V_{CC} = 0 V V_{CC} = 5.25 V (See Fig. 6D)		40 40	μA μA
Low-level input current	I_{IL}	V_I = 0V V_{CC} = 0 V V_{CC} = 5.25 V (See Fig. 6E)		−10 −10	μA μA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC004 Bus Driver
(Specification Group III – Open Collector)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
Output reverse current	I_{OH}	V_{CC} = 4.75 V V_{OH} = 3.5 V (See Fig. 6A)		25†	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_{SINK} = 70 mA‡ I_{SINK} = 16 mA‡ I_{SINK} = 15 mA§ (See Fig. 6B)		0.8 0.5 0.5	V V V

*Ambient operating temperature (T_A) = 0° to 70° C unless otherwise specified.
†65 μA for pin 18 (RXCX H).
‡Applies to Pin 8 (BRPLY L) only.
§Applies to Pin 18 (RXCX H) only.

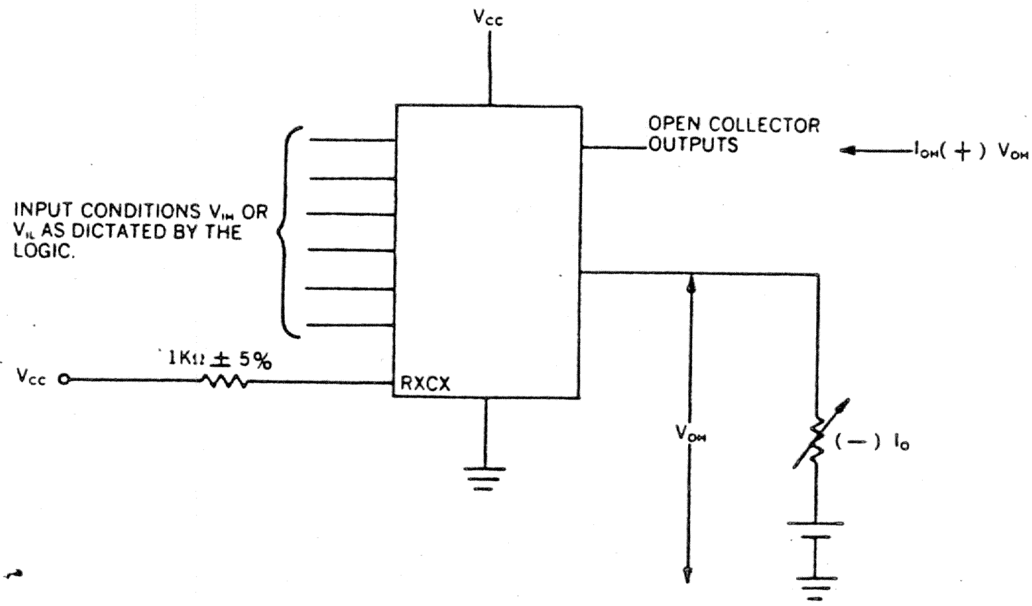


Figure 6A DC Test Circuit (V_{IH}, V_{IL}, V_{OH}, I_{OH})

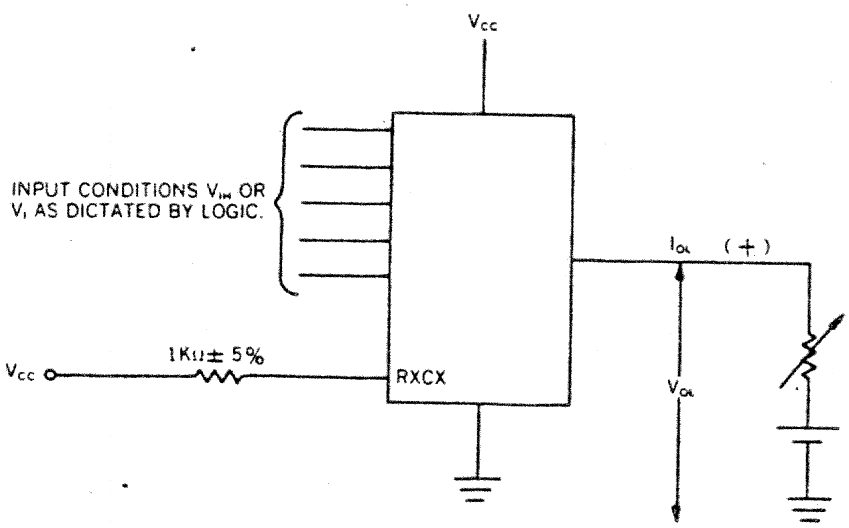


Figure 6B DC Test Circuit (V_{IH}, V_{IL}, V_{OL})

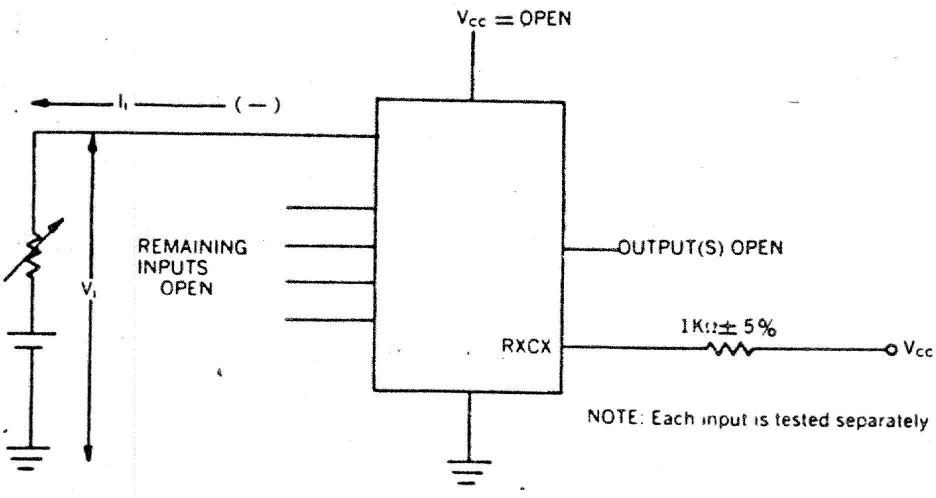


Figure 6C DC Test Circuit (V_I)

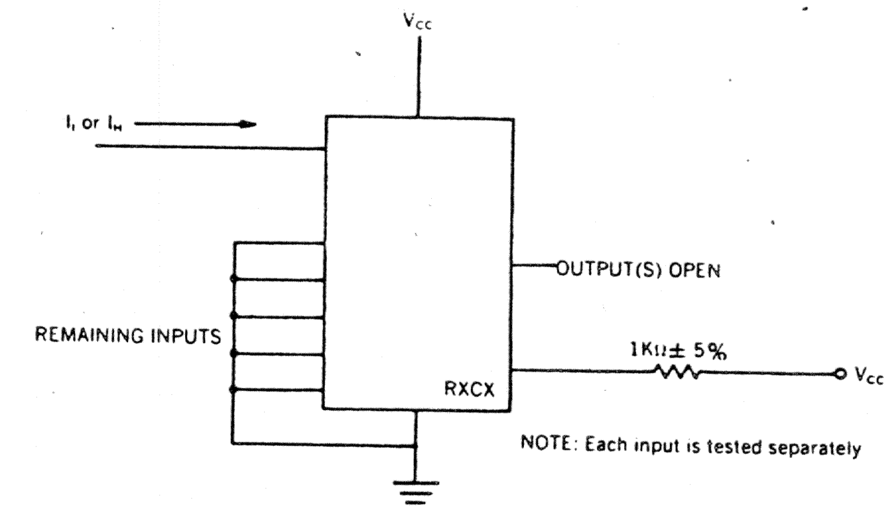


Figure 6D DC Test Circuit (I_I, I_{IH})

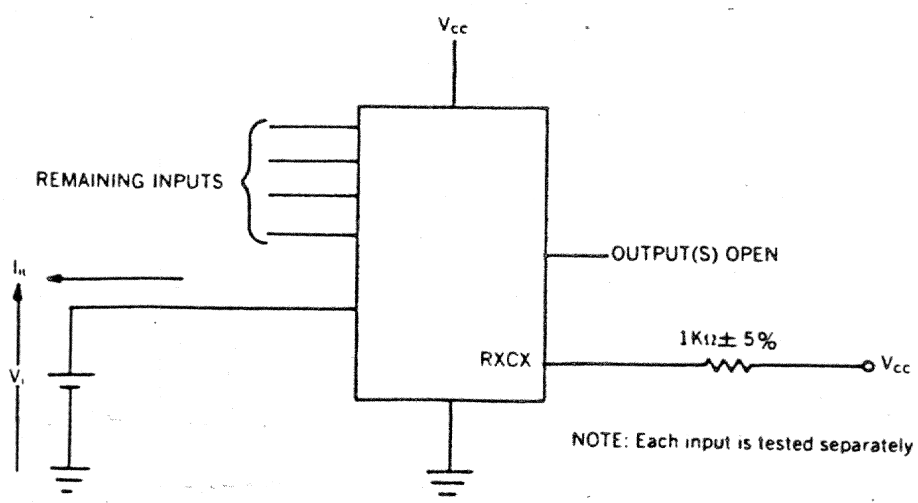


Figure 6E DC Test Circuit (I_{IL})

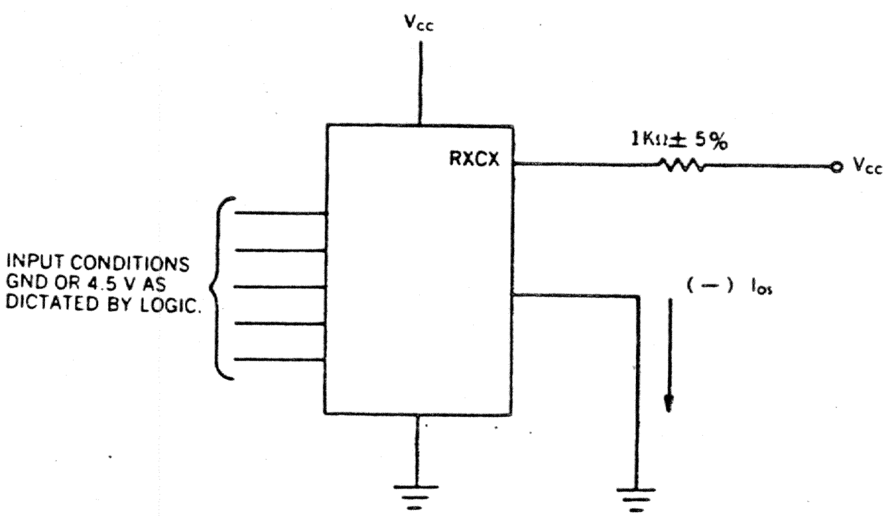


Figure 6F DC Test Circuit (Ios)

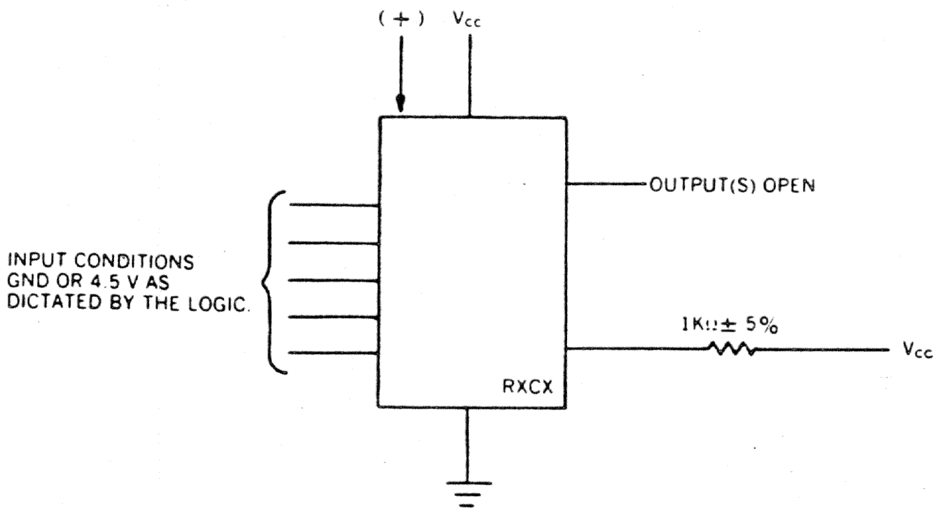


Figure 6G DC Test Circuit (Icc)

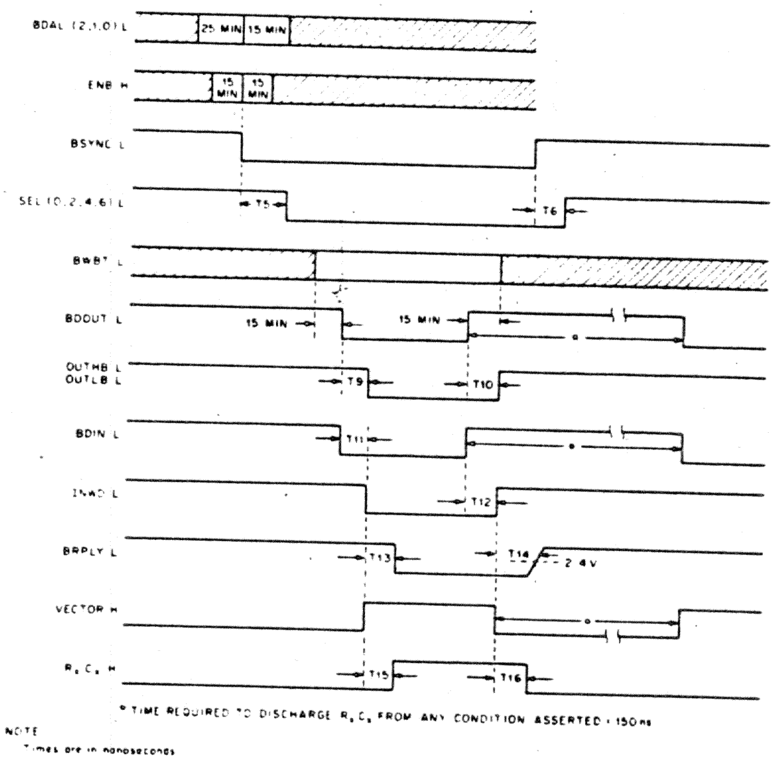


Figure 7 DC004 Timing Diagram

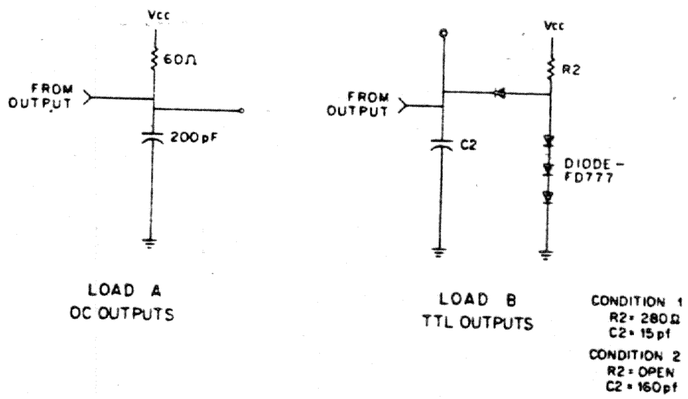


Figure 8 DC004 Loading Configurations for Table 3

Table 3 DC004 Signal Timing vs Output Loading

	Signal	With Respect to	Signal	Condition	Output Being Asserted (ns) Min	Output Being Asserted (ns) Max	Output Being Negated (ns) Min	Output Being Negated (ns) Max	Fig. 5 Reference
	SEL (0.2,4,6) L (Load B)		BSYNC L	2	15	40	5	30	T5, T6
	OUT LB L (Load B)		BDOUT L	2	5	30	5	30	T9, T10
	OUT HB L (Load B)		BDOUT L	2	5	30	5	30	T9, T10
	INWD L (Load B)		BDIN L	2	5	30	5	30	T11, T12
Pin 18 Connection RX = 330 Ω ± 5% CX = 15 pF ± 5%	BRPLY L (Load A)		OUT LB L (Load B)	1	20	60	−10	45	T13, T14
	BRPLY L (Load A)		OUT HB L (Load B)	1	20	60	−10	45	T13, T14
	BRPLY L (Load A)		INWD L (Load B)	1	20	60	−10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	—	30	70	0	45	T13, T14
Pin 18 Connection RX = 4.64K ± 1% CX = 220 pF ± 1%	BRPLY L (Load A)		OUT LB L (Load B)	1	300	400	−10	45	T13, T14
	BRPLY L (Load A)		OUT HB L (Load B)	1	300	400	−10	45	T13, T14
	BRPLY L (Load A)		INWD L (Load B)	1	300	400	−10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	—	330	430	0	45	T13, T14
Pin 18 Connection RX = 330 Ω ± 5% CX = 15 pF ± 5%	RXCX H	(Load A)	OUT LB L	—	10	50	10	50	T15, T16
	RXCX H	(Load A)	OUT HB L	—	10	50	10	50	T15, T16
	RXCX H	(Load A)	INWD L	—	10	50	10	50	T15, T16
	RXCX H	(Load A)	VECTOR H	—	10	50	10	50	T15, T16

See Figure 8.

DC005 TRANSCEIVER LOGIC (DEC # 19-13040-00)

The 4-bit transceiver is a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in. center X 1.08 in. long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high drive (70 mA) open collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tri-state drivers. Data on this port are the logical inversion of the data on the bus side.

Three address "jumper" inputs are used to compare against three bus inputs to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states: receive data, transmit data, and disable.

Maximum current required from the V_{CC} supply is 120 mA.

Figure 9 is a simplified logic diagram of the DC005 IC. Timing for the various functions is shown in Figure 11. Signal and pin definitions for the DC005 are presented in Table 4. Figure 10 shows the test conditions used to derive the data listed in the Electrical Characteristics.

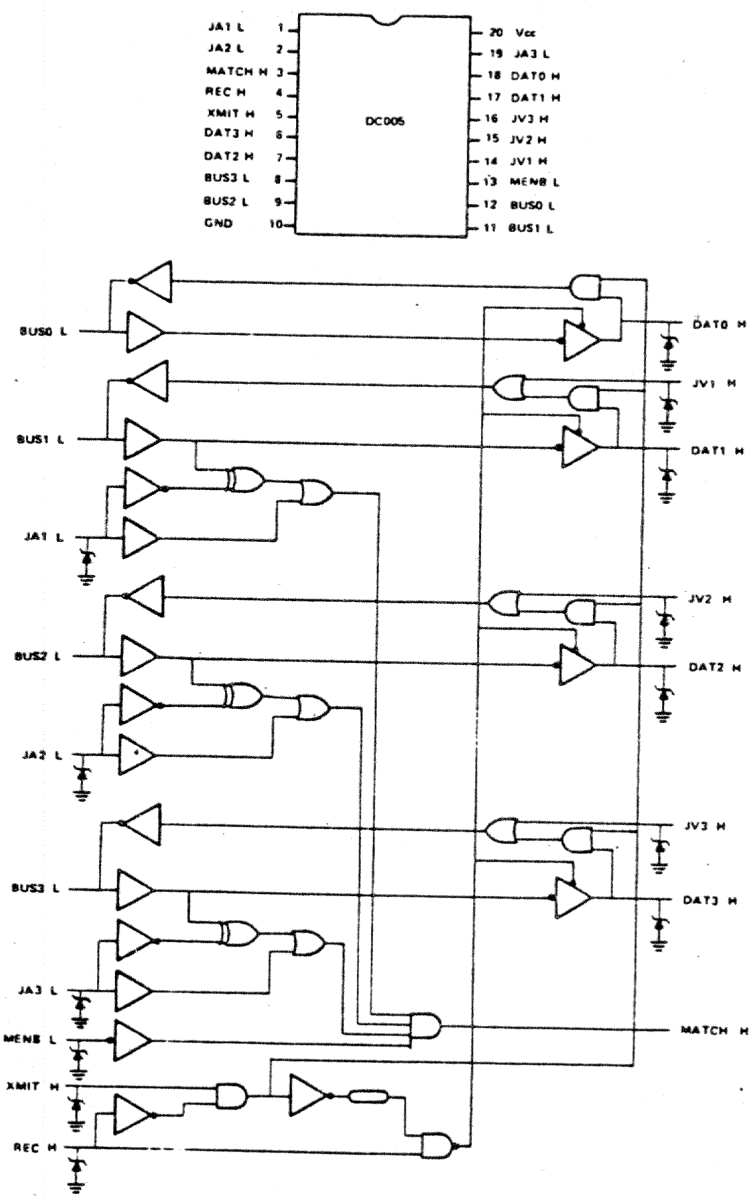


Figure 9 DC005 Simplified Logic Diagram

IC DC005

Table 4 DC005 Pin/Signal Descriptions

Pin	Signal	Spec Group	Description
	BUS(3:0) L		
12	BUS0 L	II + III	Bus Data. This set of four lines constitutes the bus side of the transceiver. Open collector outputs; high-impedance inputs. Low = 1.
11	BUS1 L	II + III	
9	BUS2 L	II + III	
8	BUS3 L	II + III	
	DAT(3:0) H		
18	DAT0 H	I	Peripheral Device Data. These four tri-state lines carry the inverted received data from BUS (3:0) when the transceiver is in the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS (3:0). When in the disabled mode, these lines go open (HI-Z). High = 1.
17	DAT1 H	I	
7	DAT2 H	I	
6	DAT3 H	I	

Table 4 DC005 Pin/Signal Descriptions (Cont)

Pin	Signal	Spec Group	Description
	JV(3:1) H		Vector Jumpers. These inputs, with internal pull-down resistors, directly drive BUS (3:1). A low or open on the jumper pin will cause an open condition on the corresponding bus pin if XMIT H is low. A high will cause a one (low) to be transmitted on the bus pin. Note that BUS0 L is not controlled by any jumper input.
14	JV1 H	V	
15	JV2 H	V	
16	JV3 H	V	
13	MENB L	II	Match Enable. A low on this line will enable the Match output. A high will force Match low, overriding the match circuit.
3	MATCH H	III	Address Match. When BUS (3:1) match with the state of JA (3:1) and MENB L is low, this output is open; otherwise it is low.
	JA(3:1) L		Address Jumpers. A strap to ground on these inputs will allow a match to occur with a one (low) on the corresponding BUS line; an open will allow a match with a zero (high); a strap to V_{CC} will disconnect the corresponding address bit from the comparison.
1	JA1 L	IV	
2	JA2 L	IV	
19	JA3 L	IV	
5	XMIT H	I	Control Inputs. These lines control the operation of the transceiver as follows.
4	REC H	I	

REC	XMIT	
0	0	DISABLE: BUS, DAT open
0	1	XMIT DATA: DAT → BUS
1	0	RECEIVE: BUS → DAT
1	1	RECEIVE: BUS → DAT

To avoid 3-state signal overlap conditions, an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode and delays 3-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.

DC005 Electrical Characteristics

DC005 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	(See Fig. 10A, 10B)	2		V
Low-level input voltage	V_{IL}	(See Fig. 10A, 10B)		0.8	V
Input clamp voltage	V_I	$V_{CC} = 4.75$ V $I_I = -18$ mA (See Fig. 10C)		−1.2	V
High-level output voltage	V_{OH}	$V_{CC} = 4.75$ V $I_O = -1$ mA (See Fig. 10A)	3.65		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_O = 20$ mA (See Fig. 10B)		0.5	V
Input current at maximum input voltage	I_I	$V_{CC} = 5.25$ V $V_I = 5.5$ V (See Fig. 10D)		1	mA
High-level input current	I_{IH}	$V_{CC} = 5.25$ V $V_I = 2.7$ V REC XMIT (See Fig. 10D)		 100 50	 μA μA
Low-level input current	I_{IL}	$V_{CC} = 5.25$ V $V_I = 0.5$ V REC XMIT (See Fig. 10E)		 −2.2 −1.1	 mA mA
Short-circuit output current	I_{OS}	$V_{CC} = 5.25$ V† (See Fig. 10F)	−40	−100	mA
Supply current	I_{CC}	$V_{CC} = 5.25$ V (See Fig. 10G)		120	mA
Off state (high-impedance state) output current (DAT pins only)	$I_{O(OFF)}$	$V_{CC} = 5.25$ V $V_I = 3.65$ V $V_I = 0.5$ V		 100 −0.36	 μA mA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

† Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC005 Bus Receiver
(Specification Group II – High Input Z)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 10A, 10B)	1.53 1.70		V V
Low-level input voltage	V_{IL}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 10A, 10B)		1.30 1.47	V V
Input clamp voltage	V_I	$I_I = -18$ mA $V_{CC} = 4.75$ V (See Fig. 10C)		−1.2	V
High-level input current (includes open-collector leakage on bus pins)	I_{IH}	$V_I = 3.8$ V			
MENB		$V_{CC} = 0$ V $V_{CC} = 5.25$ V		40 40	μA μA
BUS		$V_{CC} = 0$ V $V_{CC} = 5.25$ V (See Fig. 10D)		65 65	μA μA
Low-level input current	I_{IL}	$V_I = 0.5$ V $V_{CC} = 0$ V $V_{CC} = 5.25$ V (See Fig. 10E)		−10 −10	μA μA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 Bus Driver
(Specification Group III – Open Collector)

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level output current (reverse current—match output only)†	I_{OH}	$V_{CC} = 4.75$ V $V_{OH} = 5.25$ V (See Fig. 10A)		25	μA
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_{SINK} = 8$ mA (Match) $I_{SINK} = 70$ mA (Bus) $I_{SINK} = 16$ mA (Bus) (See Fig. 10B)		0.5 0.8 0.5	V V V

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

† For bus pins, see I_{IH} under specification group II.

DC005 (Specification Group IV – Ternary State Inputs)

Parameter Name	Symbol	Conditions[1]	Requirements Min	Max	Unit
Low-level input voltage	V_{IL}	(See Fig. 10A)		0.3	V
High-level input voltage	V_{IH}	(See Fig. 10A)	4.75		V
Open circuit input voltage	V_{OP}	$4.75 < V_{CC} < 5.25$	1	2	V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 (Specification Group V – TTL Input with Pull-Down)

Parameter Name	Symbol	Conditions[1]	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	(See Fig. 10A)	2		V
Low-level input voltage	V_{IL}	(See Fig. 10A)		0.8	V
Input clamp voltage	V_I	$V_{CC} = 4.75$ V $I_I = -18$ mA (See Fig. 10C)		−1.2	V
High-level input current	I_{IH}	$V_{CC} = 5.25$ V $V_I = 2.4$ V (See Fig. 10D)		1.2	mA
Low-level input voltage forcing input current	V_{II}	$V_{CC} = 4.75$ V $I_I = 0.1$ mA (See Fig. 10H)		0.8	V
Input current at low-level	I_{IL}	$V_{CC} = 5$ V $V_I = 0.4$ V (See Fig. 10E)	50	200	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

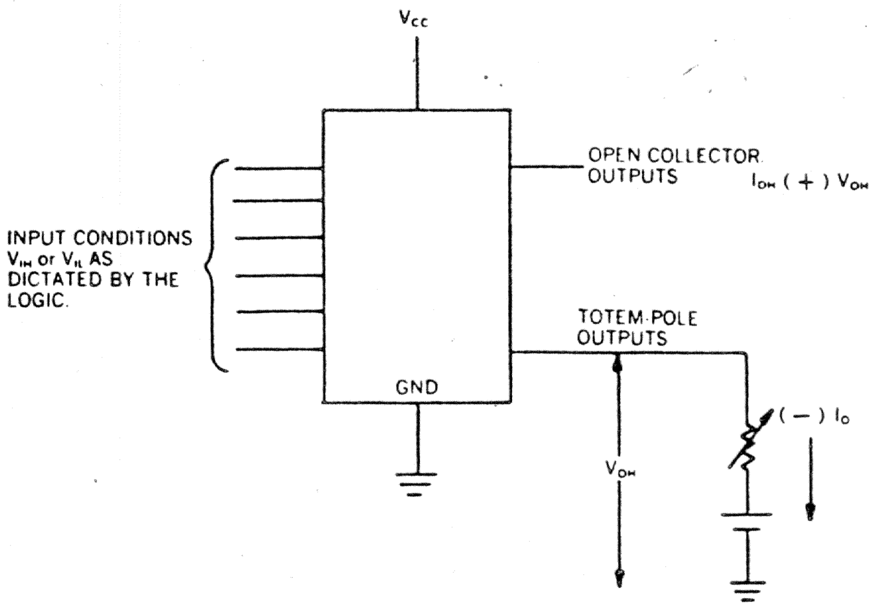


Figure 10A DC Test Circuit — V_{IH}, V_{IL}, V_{OH}, I_{OH}

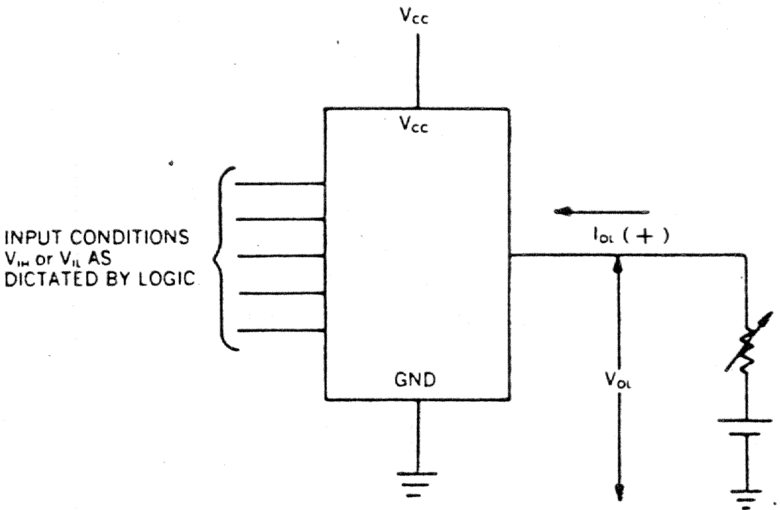


Figure 10B DC Test Circuit — V_{IH}, V_{IL}, V_{OL}

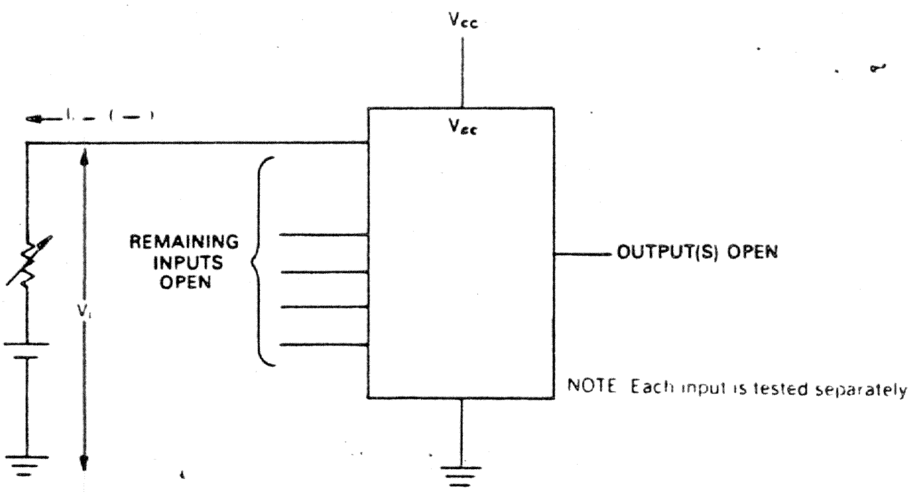


Figure 10C DC Test Circuit — V_I

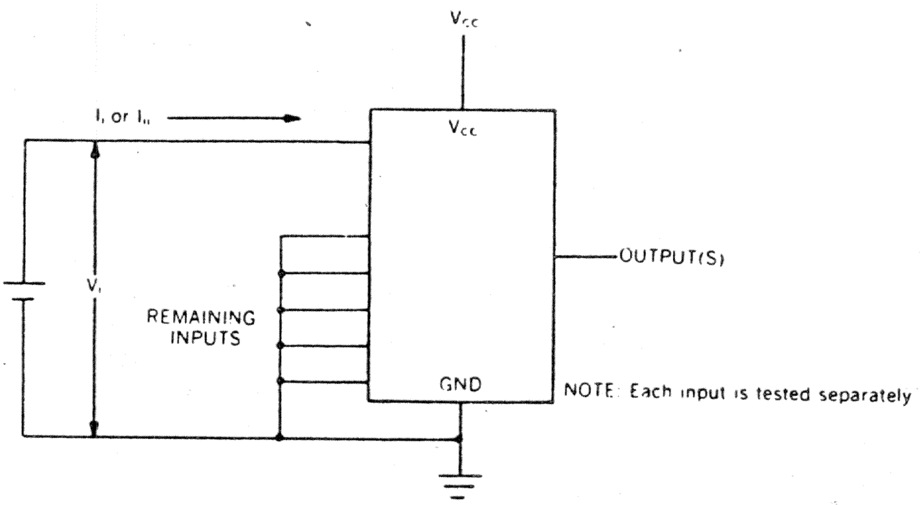


Figure 10D DC Test Circuit — I_I, I_{IH}

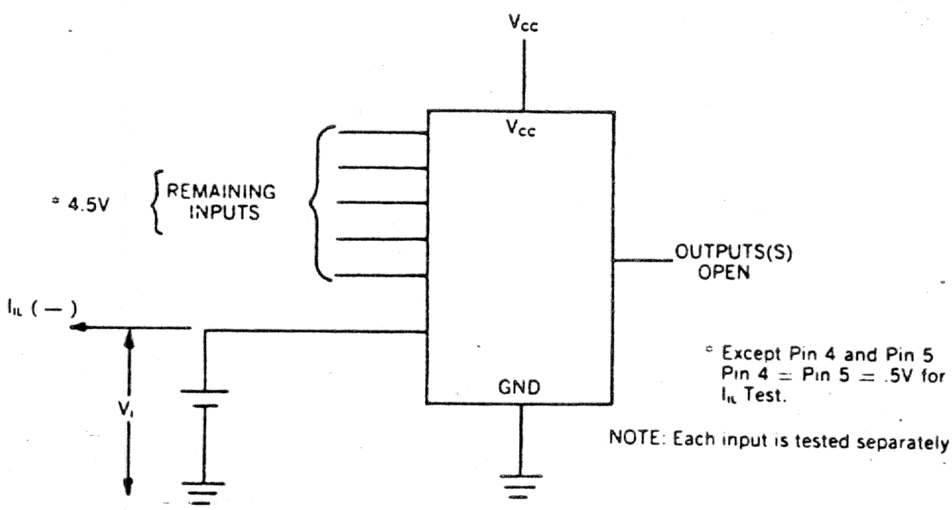
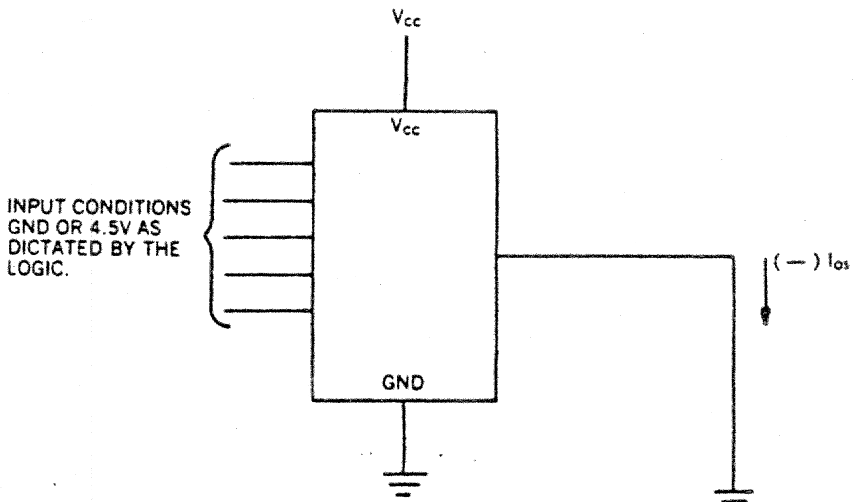


Figure 10E DC Test Circuit — I_{IL}



NOTE: Only one output be shorted at a time and the duration should not exceed more than a second.

Figure 10F DC Test Circuit — I_{OS}

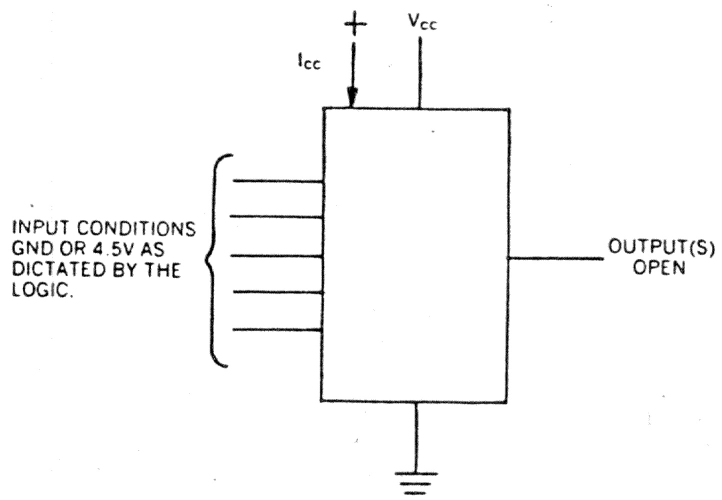


Figure 10G DC Test Circuit — I_{cc}

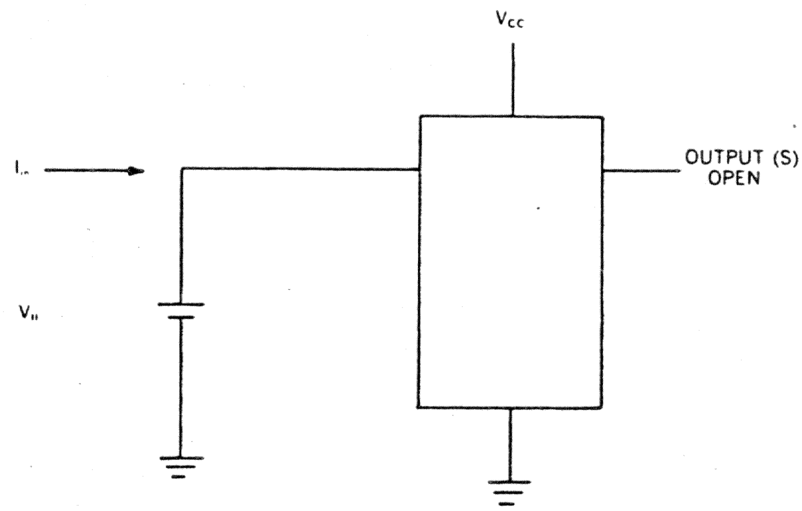


Figure 10H DC Test Circuit — V_{II}

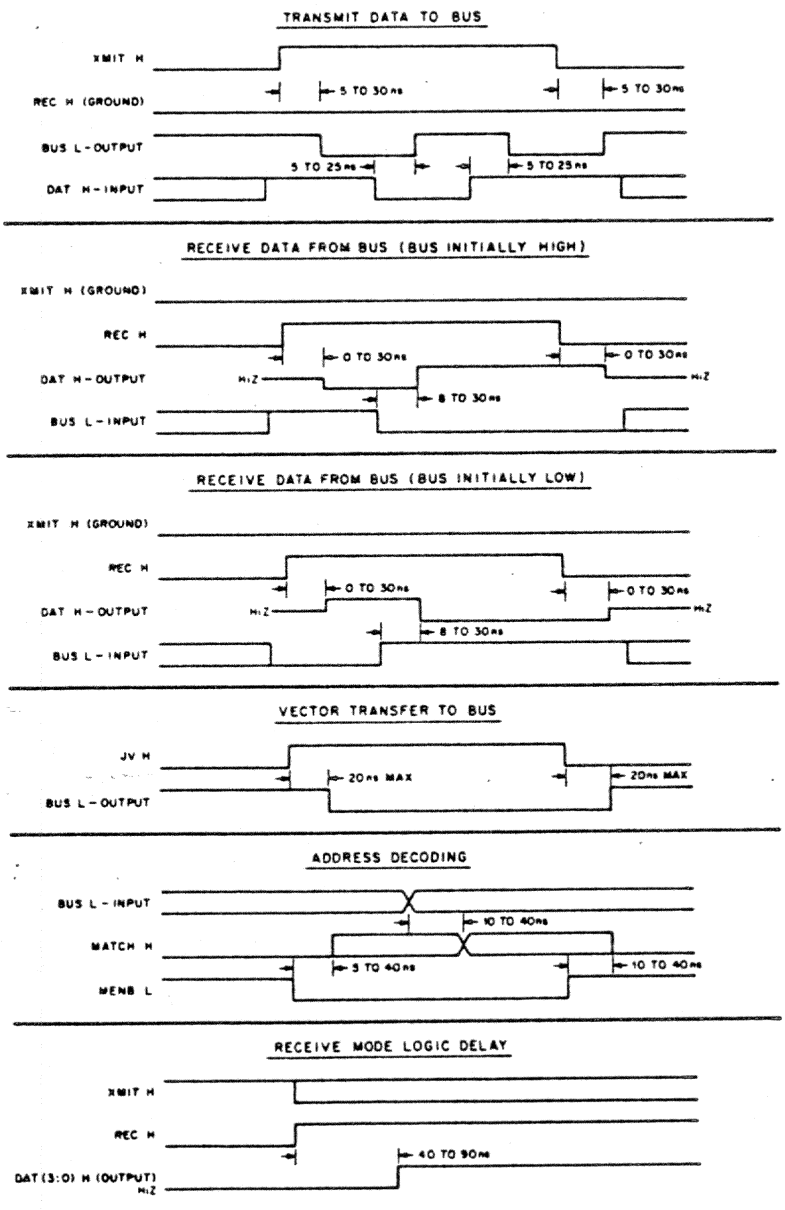


Figure 11 DC005 Timing Diagram

DC006 WORD COUNT/BUS ADDRESS LOGIC (DEC # 19-14035-00)

The word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the 3-state side of the DC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (byte) count and another for bus address. Two DC006 ICs may be cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters may be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word byte counter) is always incremented by one; the A counter (bus address) may be incremented by one or two for byte or word addressing, respectively.

Data from the DC006 IC is placed on the 3-state bus via internal 3-state drivers. Each counter is separately read by RD and the corresponding select line.

Figure 12 is a block diagram of the DC006 IC while Figure 13 illustrates a simplified logic diagram. Figures 15 and 16 illustrate input and output voltage waveforms. Figure 17 shows the timing diagram of the DC006 while the setup time and pulse width switching characteristics are presented in Tables 6 and 7. The DC006 pin/signal description is presented in Table 5. Figure 14 shows the various test conditions employed to derive the data presented in the Electrical Characteristics.

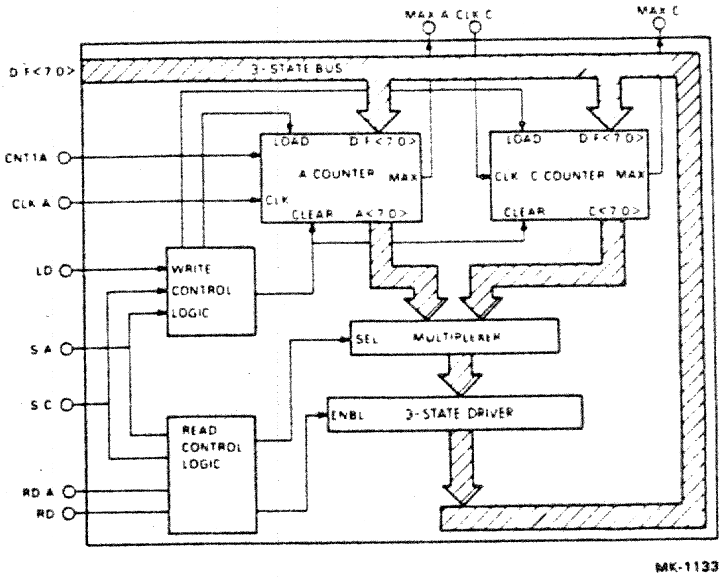


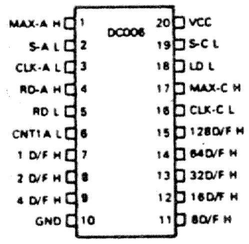
Figure 12 DC006 Simplified Block Diagram

TRUTH TABLES

WHERE
- L = TTL LOW
- H = TTL HIGH
- X = DON'T CARE
- Z = HIGH IMPEDANCE
- ↓ = HIGH TO LOW TRANSITION

READ CONTROL

INPUTS				OUTPUTS
LD H		S-A	S-C	D/F<7:0>
RD-A	RD			
L	L	L	L	CLEAR A&C AND READ C
L	L	L	H	A<7:0>
L	L	H	L	C<7:0>
L	L	H	H	Z
L	H	X	X	Z
H	L	L	L	CLEAR A&C AND READ A
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	CLEAR A&C AND READ A
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>



WRITE CONTROL

INPUTS			FUNCTION
RD. A = L, RD = H	S-A	S-C	
LD			
↓	L	L	*ILLEGAL
↓	L	H	LOAD A<7:0>
↓	H	L	LOAD C <7:0>
X	H	H	WC SA NOT SELECTED
H	L	L	CLEAR BOTH COUNTERS
H	L	H	LOADING DISABLED
H	H	L	LOADING DISABLED

*ILLEGAL CONDITION BECAUSE A LOAD OPERATION AND A CLEAR OPERATION IS ATTEMPTED SIMULTANEOUSLY RESULT OF THIS CONDITION IS CLEAR.

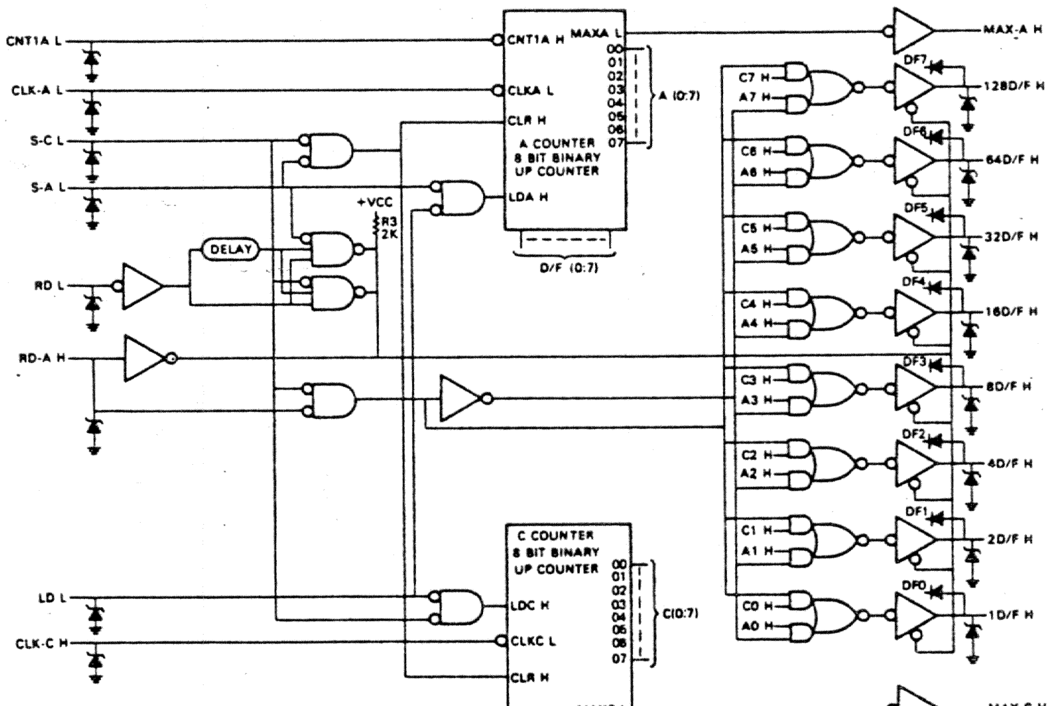


Figure 13 DC006 Simplified Logic Diagram

Table 5 DC006 Pin/Signal Descriptions

Pin	Signal	Description
6	CNT1A L	Count A Counter by 1 (TTL Input). This signal controls the least significant bit of the A counter. When CNT1A is low, the A counter increments by one. When high, the LSB is prevented from toggling, hence the counter increments by two. When two counters are cascaded, CNT1A on the high-order counter should be grounded.
3	CLK-A L	Clock A Counter (TTL Input). This clock signal increments the A counter on its negative edge. The counter is incremented by one or two, depending on CNT1A. CNT1A and LD must be stable while CLK-A is high.
16	CLK-C L	Clock C Counter (TTL Input). This clock signal increments the C counter by one on its negative edge. LD must be stable while CLK-C is high.
2	S-A L	Select A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 13).
19	S-C L	Select C Counter (TTL Input). This signal allows the selection of the C counter according to the truth tables (Figure 13).
4	RD-A H	Read A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 13).
5	RD L	Read (TTL Input). This signal allows the read operation to take place according to the truth tables (Figure 13).
18	LD L	Load (TTL Input). When this signal goes through a high-to-low transition, the load operation is allowed to take place according to the truth tables (Figure 13). No data changes permitted while LD is low.

Table 5 DC006 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
7–9 11–15	D/F (7:0) H	Data Bus (Bidirectional, 3-State Outputs/ TTL Inputs). These eight bidirectional lines are used to carry data in and out of the selected counter.
1	MAX-A H	Maximum A Count (TTL Output). This signal is generated by ANDing CLK-A and the maximum count condition of counter A (count 376 when counting by 2 or count 377 when counting by 1).
17	MAX-C H	Maximum C Count (TTL Output). This signal is generated by ANDing CLK-C and the maximum count conditions of counter C (count 377).

DC006 Electrical Characteristics

DC006 TTL (TTL Input and Output Pins)

Parameter			Requirements		
Name	Symbol	Conditions*	Min	Max	Unit
High-level input voltage	V_{IH}	(See Fig. 14A, 14B)	2		V
Low-level input voltage	V_{IL}	(See Fig. 14A, 14B)		0.8	V
Input clamp voltage	V_I	V_{CC} = Open $I_I = -18$ mA (See Fig. 14C)		−1.2	V
High-level output voltage	V_{OH}	$V_{CC} = 4.75$ V $I_O = -1$ mA (See Fig. 14A)	2.7		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_O = 20$ mA (See Fig. 14B)		0.5	V
Input current at maximum input voltage	I_I	$V_{CC} = 5.25$ V $V_I = 5.5$ V (See Fig. 14D)		1	mA
High-level input current Except 3-state 3-state pin	I_{IH}	$V_{CC} = 5.25$ V $V_I = 2.7$ V (See Fig. 14D)		 50 55	 μA μA
Low-level input current CLKA, CLKC CNTIA D/F(7:0),LD,RD, SC,SA RD-A	I_{IL}	$V_{CC} = 5.25$ V $V_I = 0.5$ V (See Fig. 14E)		 −1.1 −1.7 100 200	 mA mA μA μA
Off-state high impedance state—output current 3-state only	$I_{O(OFF)}$	$V_{CC} = 5.25$ V $V_O = 3.75$ V (See Fig. 14A)		100	μA
Short-circuit output current	I_{OS}	$V_{CC} = 5.25$ V† (See Fig. 14F)	−40	−100	mA
Supply current	I_{CC}	$V_{CC} = 5.25$ V (See Fig. 14G)		170	mA

*Ambient operating temperature (T_A) = 0° to +70° C; $V_{CC} = 5.0 \pm 0.25$ unless otherwise specified.

† Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

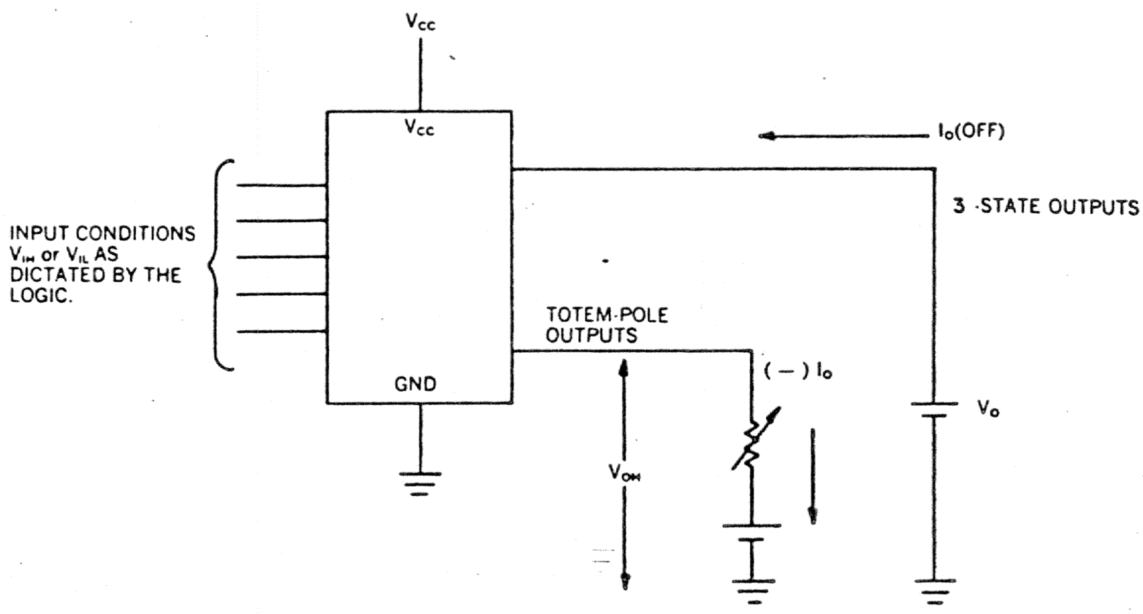


Figure 14A DC Test Circuit (V_{IH}, V_{IL}, V_{OH}, $I_{O(OFF)}$)

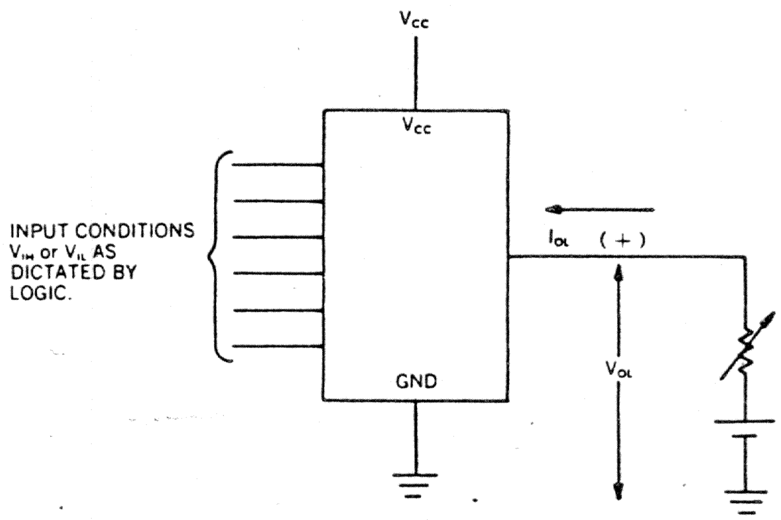


Figure 14B DC Test Circuit (V_{IH}, V_{IL}, V_{OL})

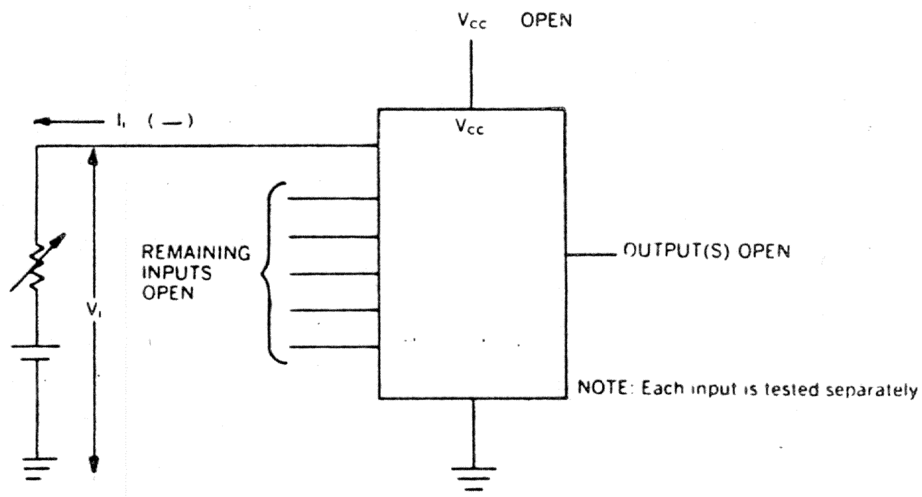


Figure 14C DC Test Circuit (V_I)

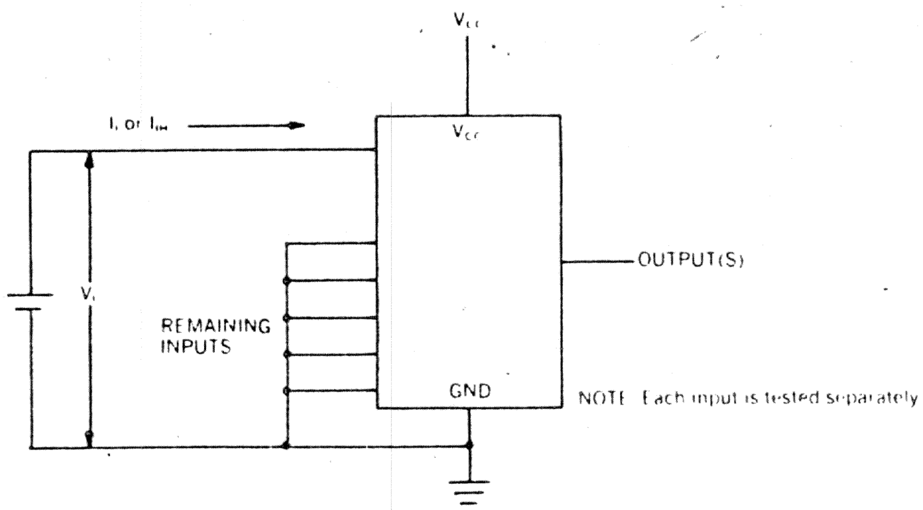


Figure 14D DC Test Circuit (I_I, I_{IH})

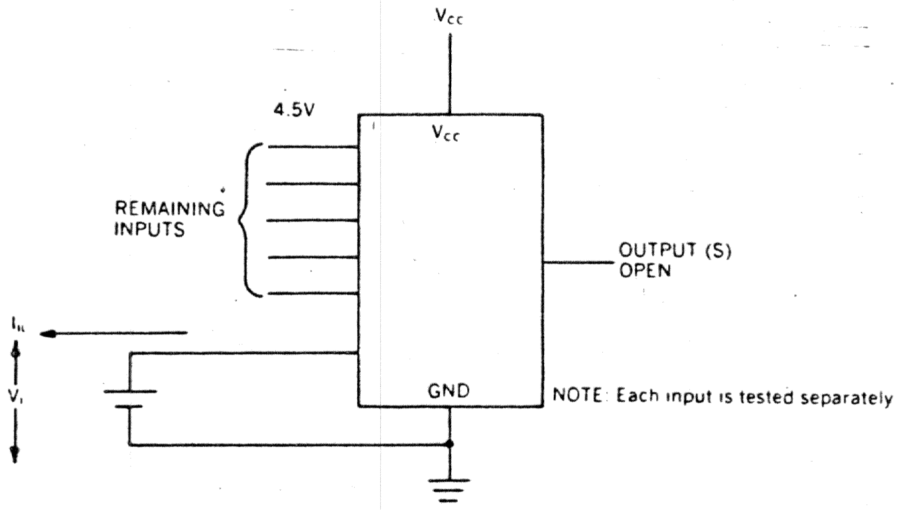
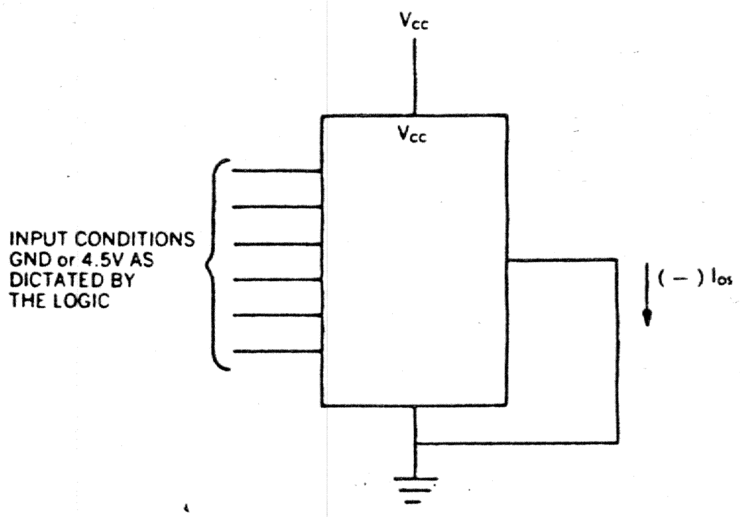


Figure 14E DC Test Circuit (I_{IL})



NOTE: Only one output should be shorted at a time, and the duration should not exceed more than a second.

Figure 14F DC Test Circuit (I_{OS})

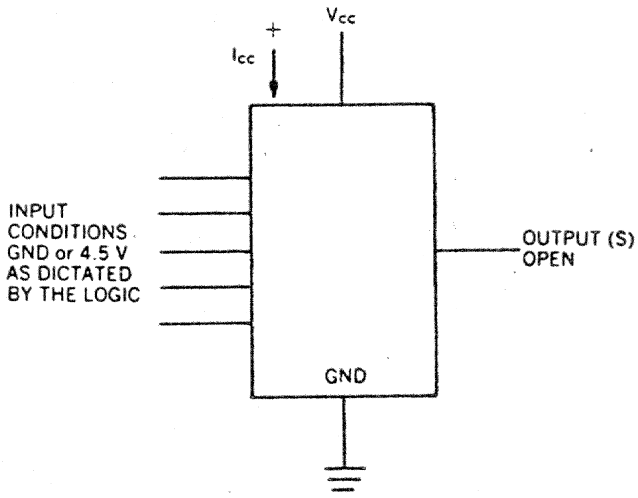


Figure 14G DC Test Circuit (Icc)

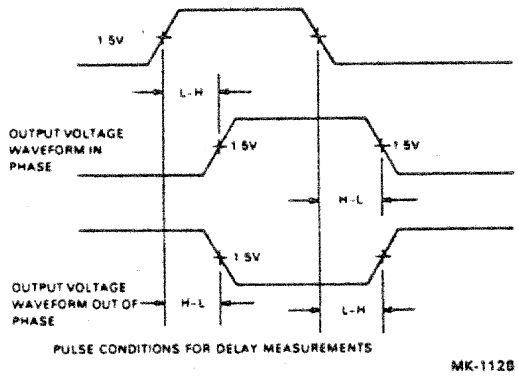


Figure 15 Input Voltage Waveform

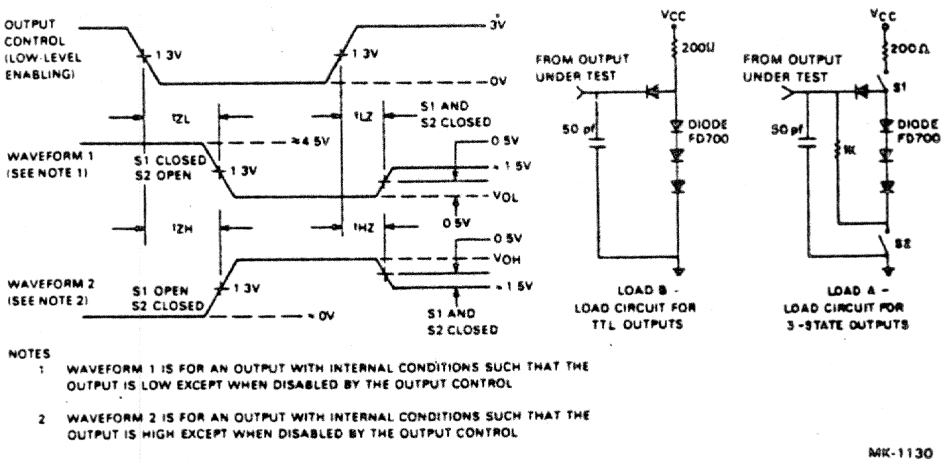


Figure 16 Outputs Voltage Waveforms (3-State)

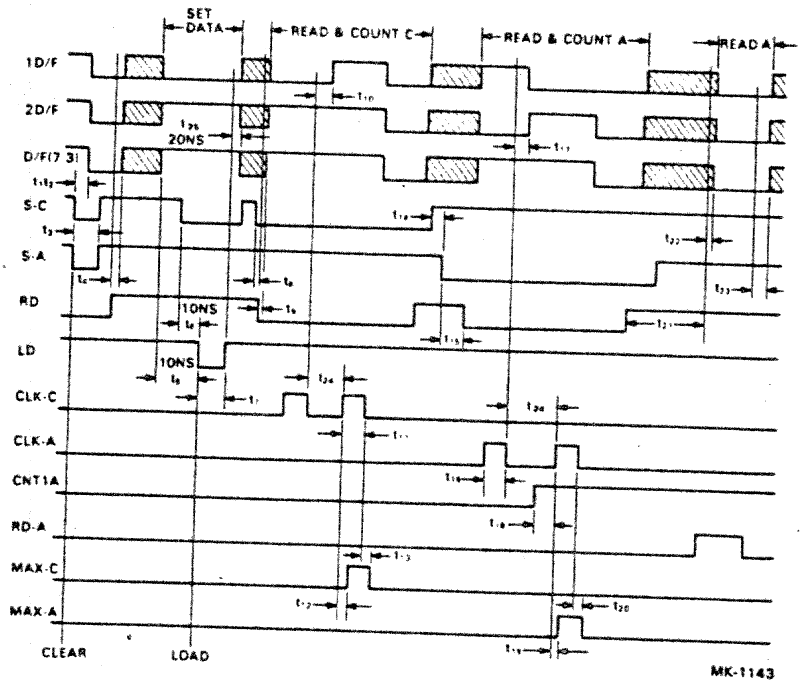


Figure 17 DC006 Timing Diagram

Table 6 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min
t_3	Pulse width (min)	S-C to S-A	50 ns
t_5	Setup time	D/F (7:0) to LD	10 ns
t_6	Setup time	S-C to LD	10 ns
t_7	Pulse width (min)	LD	90 ns
t_8	Setup time	S-C to RD	20 ns
t_{11}	Clock pulse width (min)	CLK-C (HI)	40 ns
t_{14}	Setup time	S-C to S-A	20 ns
t_{15}	Setup time	S-A to RD	10 ns
t_{16}	Clock pulse width (min)	CLK-A (HI)	40 ns
t_{18}	Setup time	CNT1A to CLK-A	45 ns
t_{21}	Setup time	RD to RD-A	15 ns
t_{24}	Clock off time (min)	CLK-A, CLK-C	40 ns
t_{25}	Data hold time	LD to DATA IN	20 ns

*VCC = 5.0 ± 0.25 V.

Table 7 Switching Characteristics*

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_1	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A = 0.4V (C Counter)	15	80
t_2	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A = 0.4V (A Counter)	15	80
t_4	RD	L-H	D/F (7:0)	D/F (7:0)-Z	Load A	10	30
t_9	RD	H-L	D/F (7:0)	Z-D/F (7:0)	Load A	34	80
t_{10}	CLK-C	H-L	D/F 1	L-H	Load A	18	55
t_{12}, t_{19}	CLK-C CLK-A	L-H	MAX-C MAX-A	L-H	Load B	10	35
t_{13}	CLK-C	H-L	MAX-C	H-L	Load B	10	35
t_{17}	CLK-A	H-L	D/F 2	L-H	Load A	18	55
t_{20}	CLK-A	H-L	MAX-A	H-L	Load B	10	35
t_{22}	RD-A	L-H	D/F (7:0)	Z-L Z-H	Load A Load A	10 10	30 30
t_{23}	RD-A	H-L	D/F (7:0)	L-Z H-Z	Load A Load A	8 8	25 25

* Loads are presented in Figure 16.

$V_{CC} = 5.0 \pm 0.25$ V

DC010 DIRECT MEMORY ACCESS LOGIC (DEC # 19-14038-00)

The direct memory access (DMA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device for primary use in DMA peripheral device interfaces using the LSI-11 bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DATI, DATO, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up bus mastership.

Figure 18 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are presented in Figure 19 and the DC010 voltage waveforms are shown in Figure 21. Table 8 describes the signals and pins of the DC010 by pin and signal name. Figures 22 through 26 show the timing for the DC010 while the setup time and pulse width specifications are listed in Table 9. The switching characteristics are presented in Table 10. Figure 20 shows the various test conditions employed to derive the data presented in the Electrical Characteristic.

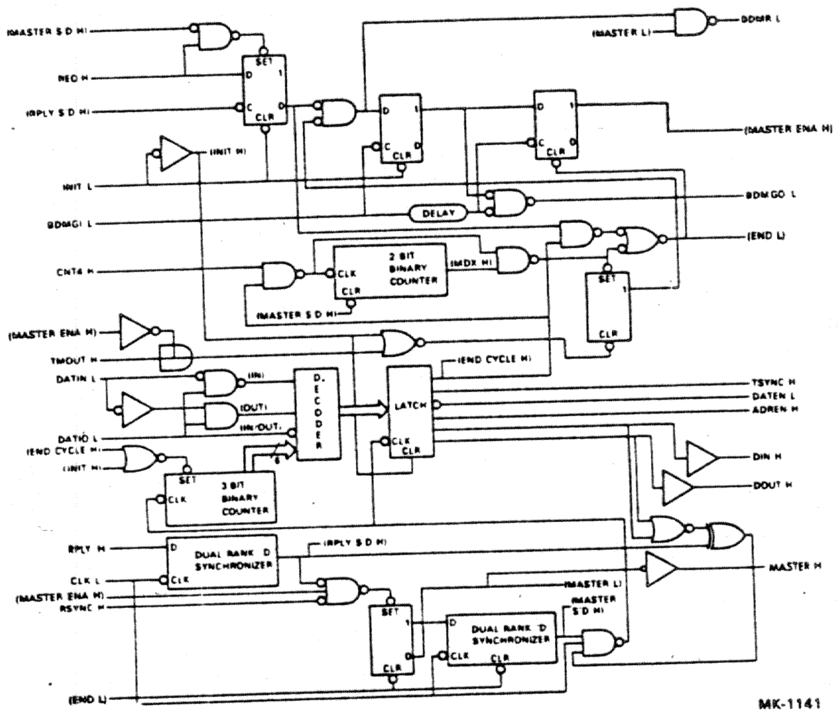
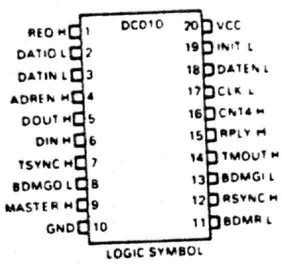


Figure 18 DC010 Simplified Logic Diagram



TRUTH TABLE

WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE

INPUTS		TRANSFER TYPE
DATIN	DATIO	
X	L	DATIO
L	H	DATI
H	H	DATO

MK-1132

Figure 19 DC010 Logic Symbol/Truth Table

Table 8 DC010 Pin/Signal Descriptions

Pin	Signal	Description*
1	REQ H	Request (TTL Input). A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L	DMA Grant Input (Hi-Z Input). A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise this signal is delayed and output as BDMGO L.
16	CN14 H	Count Four Input (TTL Input). A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open, this pin will assume a high state.
14	TMOUT H	Time-Out (TTL Input/Open Collector Output). This I/O pin is low while MASTER ENA is high. It goes into high impedence when MASTER ENA is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been negated due to the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	Data In (TTL Input). This signal allows the selection of the type of transfers to take place according to the truth table (Figure 19).
2	DATIO L	Data In/Out (TTL Input). This signal allows the selection of the type of transfer to take place according to the truth table (Figure 19). During a DATIO transfer, this signal must be toggled in order to allow the completion of the output portion of the I/O transfer. If left open, this pin will assume a high state.

* Refer to Figures 22 through 26.

Table 8 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description*
12	RSYNC H	Receive Synchronize (TTL Input). This signal allows the device to become master according to the following relationship: RSYNC L • RPLY L • MASTER ENA H = MASTER
17	CLK L	Clock (TTL Input). This clock signal is used to generate all transfer timing sequences.
15	RPLY H	Reply (TTL Input). This signal is used to enable or disable the clock signal. This signal also allows the device to become master according to the following relationship: RSYNC L • RPLY L • MASTER ENA H = MASTER
19	INIT L	Initialize (TTL Input). This signal is used to initialize the chip to the state where REQ is needed to start a bus request transaction. When INIT is low, the following signals are negated: BDMR L, MASTER H, DATEN L, ADREN H, SYNC H, DIN H, DOUT H.
11	BDMR L	DMA Request (Open Collector Output). A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	Master (TTL Output). A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.
8	BDMGO L	DMA Grant Output (Open Collector Output). This signal is the delayed version of BDMGI if no request is pending; otherwise, it is not asserted. This output may be tied directly to the bus.

* Refer to Figures 22 through 26.

Table 8 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description*
7	TSYNC H	Transmit Synchronize (TTL Output). This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	Data Enable (TTL Output). This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	Address Enable (TTL Output). This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	Data In (TTL Output). This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	Data Out (TTL Output). This signal is asserted to indicate that the bus master device has output valid data.

* Refer to Figures 22 through 26.

DC010 Electrical Characteristics

Parameter Name	Symbol	Conditions*	Requirements Min	Max	Unit
High-level input voltage	V_{IH}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 20A, 20B)	2.0 1.53 1.70		V‖ V**†† V‖
Low-level input voltage	V_{IL}	$V_{CC} = 4.75$ V $V_{CC} = 5.25$ V (See Fig. 20A, 20B)		0.8 1.30 1.47	V‖ V**†† V**††
Input clamp voltage	V_I	V_{CC} = open $I_I = -18$ mA (See Fig. 20C)		1.2	V‖ **††
High-level output voltage	V_{OH}	$V_{CC} = 4.75$ V $I_O = -1$ mA (See Fig. 20A)	2.7		V‖
Low-level output voltage	V_{OL}	$V_{CC} = 4.75$ V $I_O = 8$ mA $I_O = 70$ mA (See Fig. 20B)		0.5 0.8	V‖ V#††
Input current at maximum input voltage	I_I	$V_{CC} = 5.25$ V $V_I = 5.5$ V $V_{CC} = 0$ to 5.25 V $V_I = 3.8$ V (See Fig. 20D)		1.0 1.5 40 65	mA‡ mA§ μA** μA††
High-level input current	I_{IH}	$V_{CC} = 5.25$ V‡ $V_I = 2.7$ V $V_I = 2.7$ V§ $V_I = 3.8$ V $V_I = 3.8$ V (See Fig. 20D)		50 300 40 65	μA μA μA** μA††
Low-level input current	I_{IL}	$V_I = 0.5$ V‡ $V_{CC} = 5.25$ V $V_{CC} = 5.25$ V§ $V_{CC} = 0\text{-}5.25$ V $V_{CC} = 0\text{-}5.25$ V (See Fig. 20E)		−1.4 −2.0 −10 −10	mA mA μA** μA††
Output leakage current	I_{OH}	$V_{CC} = 4.75$ V $V_O = 5.25$ V (See Fig. 20A)		25	μA#
Short-circuit output current†	I_{OS}	$V_{CC} = 5.25$ V (See Fig. 20F)	−15	−60	mA‖
Supply current	I_{CC}	$V_{CC} = 5.25$ V (See Fig. 20G)	125 TYP	160	mA

*Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

† Nor more than one output shall be shorted at a time and the duration shall not exceed 1 second.

‡ Except CNT4 (pin 16), DATIO L (pin 2).

§ CNT4 H (pin 16), DATIO L (pin 2).

‖ TTL.

OC.

** HI-Z.

†† HI-Z SCHMIDT IN/OC OUT.

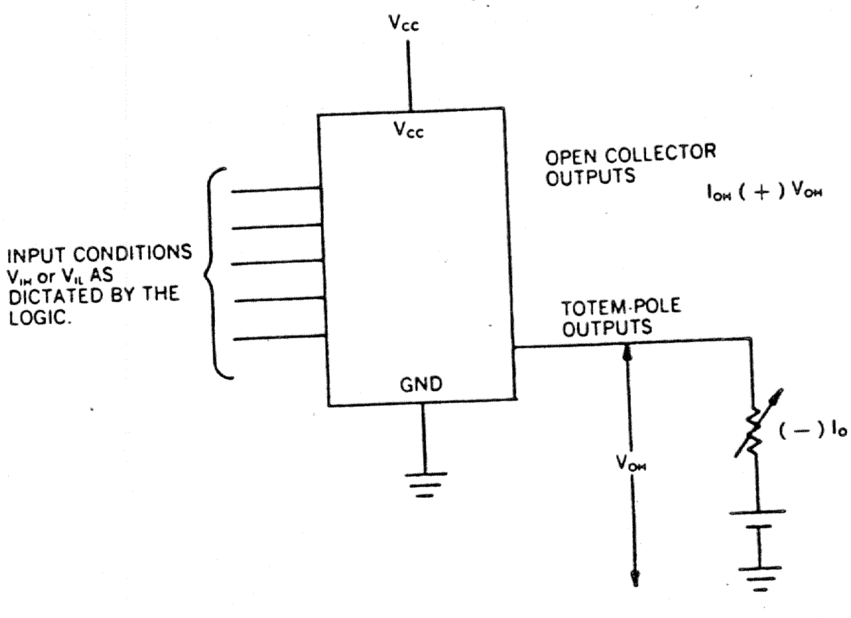


Figure 20A DC Electrical Test Condition — V_{IH}, V_{IL}, V_{OH}, I_{OH}

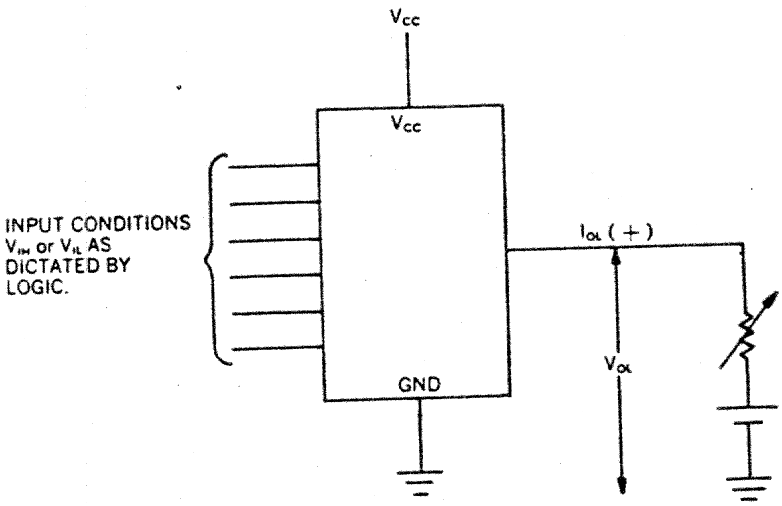


Figure 20B DC Electrical Test Condition — V_{IH}, V_{IL}, V_{OL}

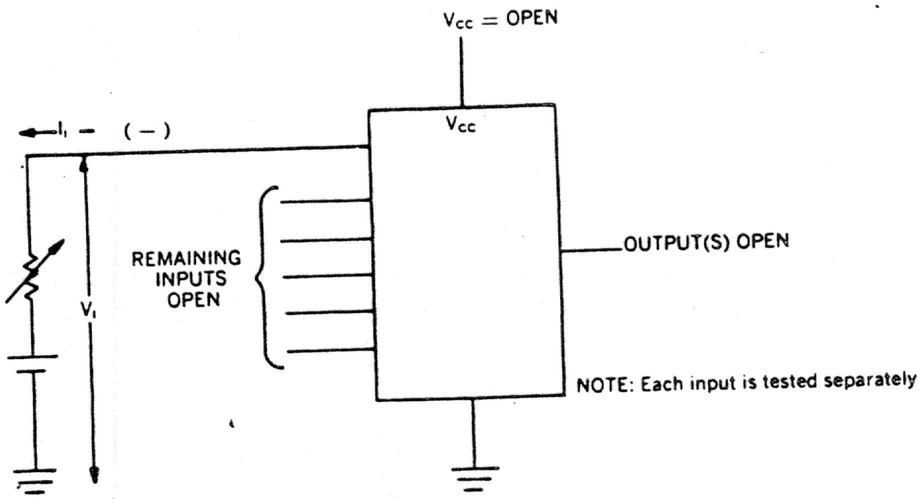


Figure 20C DC Electrical Test Condition — V_I

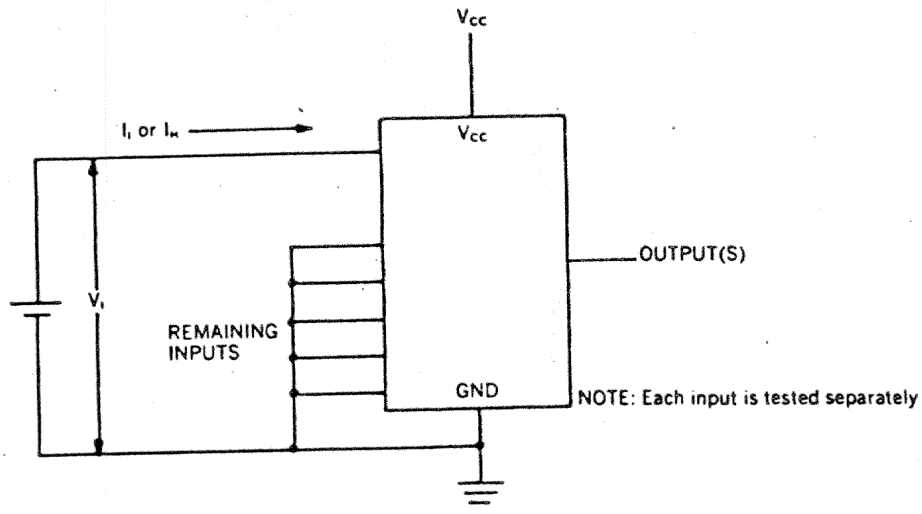


Figure 20D DC Electrical Test Condition — I_{IH}, I_I

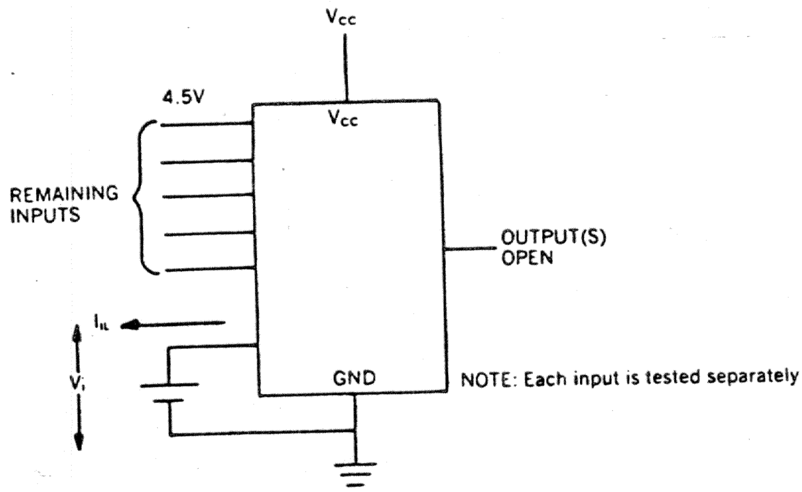
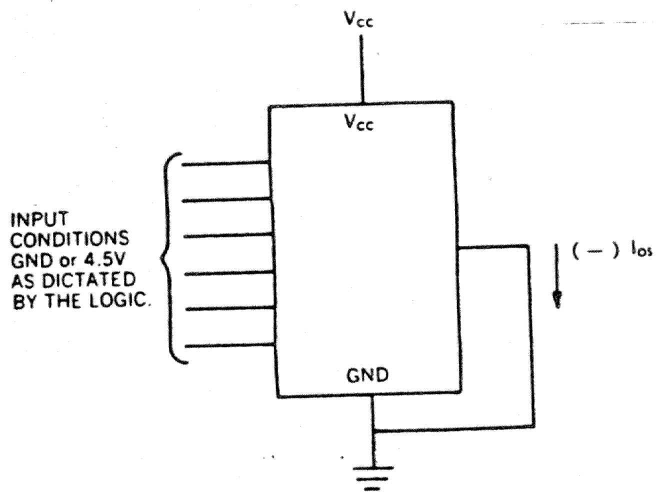


Figure 20E DC Electrical Test Condition — I_{IL}



NOTE: Only one output should be shorted at a time, and the duration should not exceed more than a second.

Figure 20F DC Electrical Test Condition — Ios

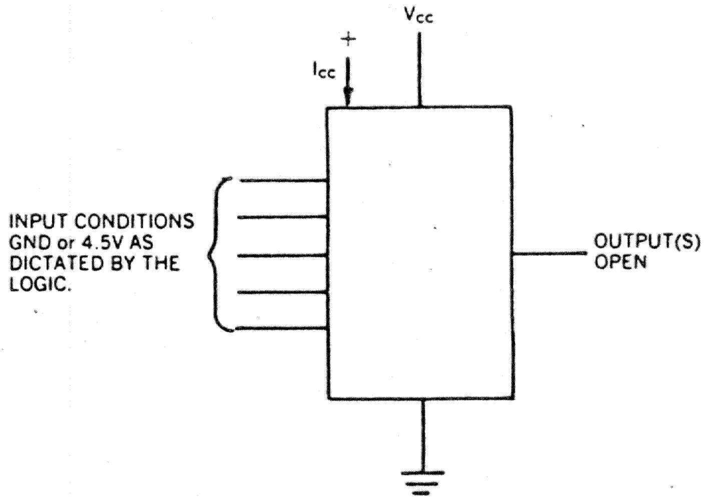


Figure 20G DC Electrical Test Condition — Icc

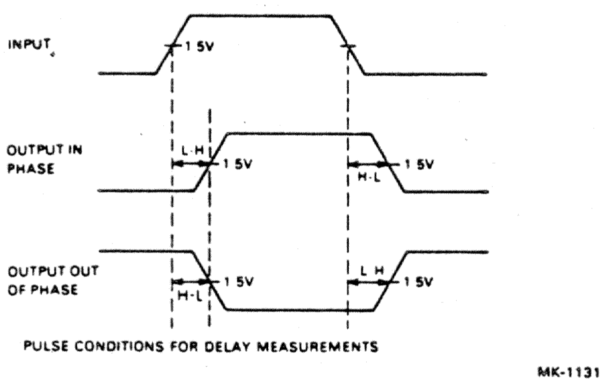


Figure 21 DC010 Voltage Waveforms

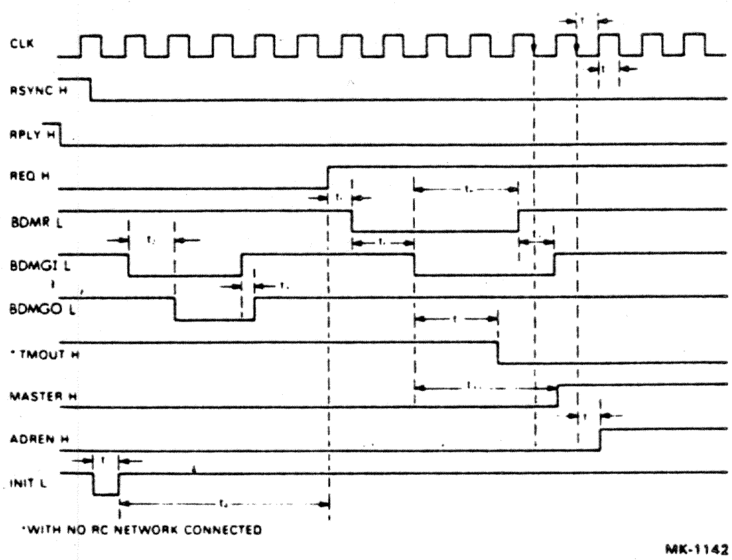


Figure 22 DC010 Timing Diagram, DMA Request/Grant

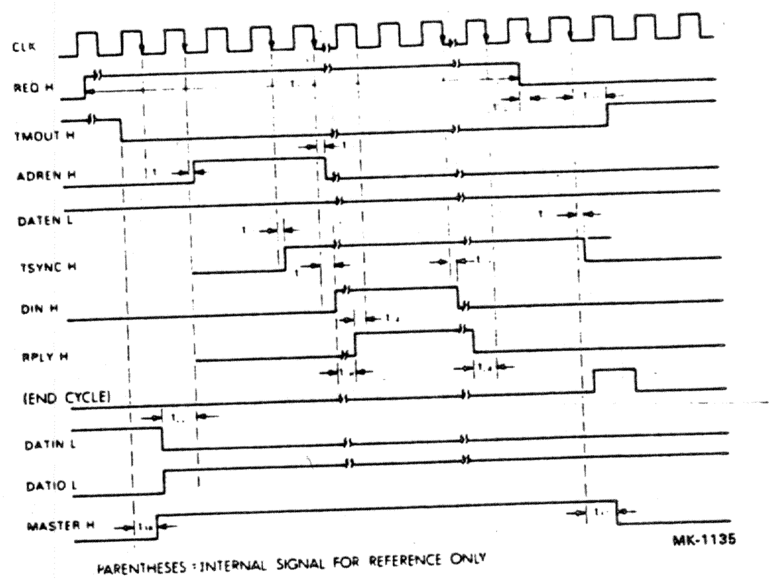


Figure 23 DC010 Timing Diagram (Sheet 1 of 2) (DIN one transfer)

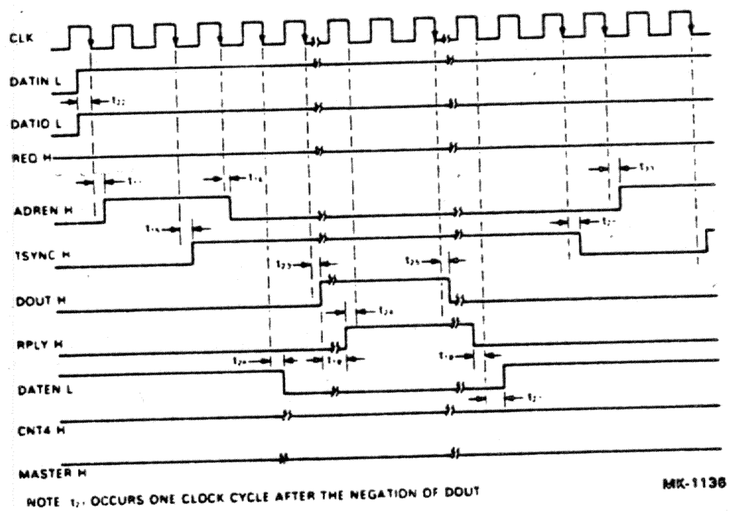


Figure 24 DC010 Timing Diagram (Sheet 2 of 2) (DOUT)

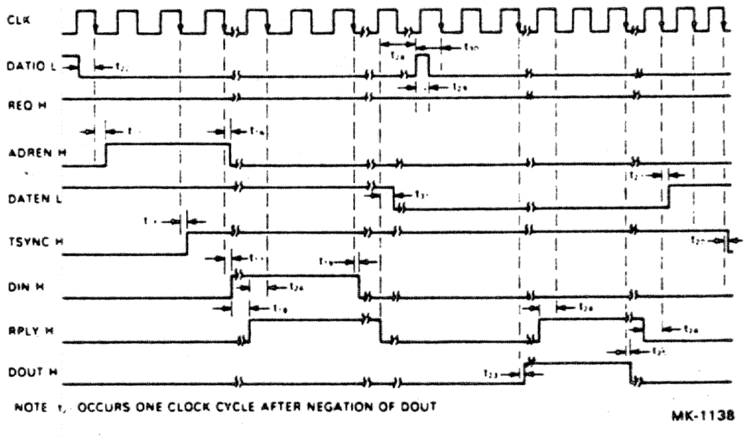


Figure 25 DC010 Timing Diagram (DATIO—Multiple Transfer)

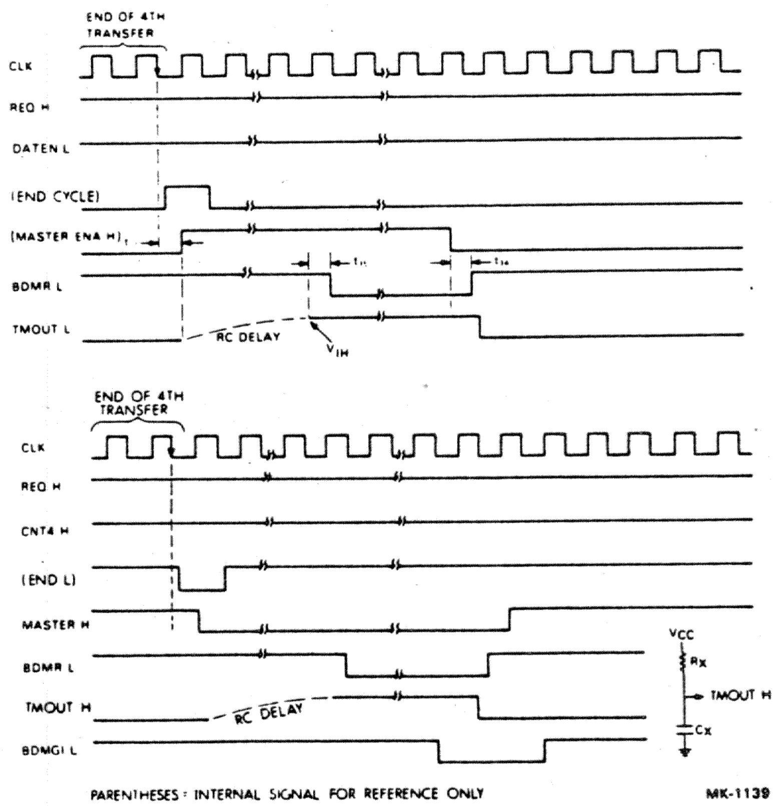


Figure 26 DC010 Timing Diagram (Time-Out)

Table 9 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min	Max
t_1	Pulse width (min)	INIT	35 ns	
t_4	Setup time	INIT to REQ.	25 ns	
t_6	Setup time	BDMR to BDMGI	35 ns	
t_9	Setup time	BDMR to BDMGI	0 ns	
t_{12}	Pulse width (min)	CLK (low)	60 ns	
t_{13}	Pulse width (min)	CLK (high)	60 ns	
t_{14}	Setup time	REQ to CLK	35 ns	
t_{18}	Setup time	DIN to RPLY	0 ns	
t_{22}	Setup time	DATIN, DATIO to CLK	60 ns	
t_{24}	Setup time	RPLY to CLK	30 ns	
t_{28}	Setup time	RPLY to DATIO	35 ns	
t_{29}	Pulse width	DATIO	30 ns	1 clock period
t_{30}	Setup time	DATIO to CLK	65 ns	
t_{32}	Pulse width (min)	REQ	35 ns	

*V_{CC} = 5.0 ± 0.25 V

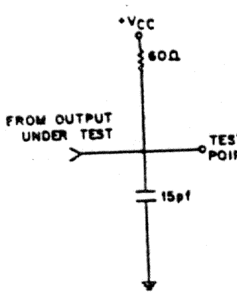
Table 10 Switching Characteristics

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_2	BDMGI	H-L	BDMGO	H-L	Load A	95	220
t_3	BDMGI	L-H	BDMGO	L-H	Load A	15	60
t_5	REQ	L-H	BDMR	H-L	Load A	25	70
t_7	BDMGI	H-L	TMOUT	H-L	Load A	85	230
t_8	BDMGI	H-L	BDMR	L-H	Load A	117	306
t_{11}*	CLK	H-L	ADREN	L-H	Load B	15	60
t_{15}	CLK	H-L	TSYNC	L-H	Load B	18	60†
t_{16}	CLK	H-L	ADREN	H-L	Load B	20	65†
t_{17}	CLK	H-L	DIN	L-H	Load B	18	60†
t_{19}	CLK	H-L	DIN	H-L	Load B	18	60
t_{20}	CLK	H-L	TSYNC	H-L	Load B	18	60
t_{21}	CLK	H-L	TMOUT	L-H	Load B	30	90
t_{23}	CLK	H-L	DOUT	L-H	Load B	60	175
t_{25}	CLK	H-L	DOUT	H-L	Load B	20	65†
t_{26}	CLK	H-L	DATEN	H-L	Load B	20	65†
t_{31}	RPLY	H-L	DATEN	H-L	Load B	20	65
t_{27}	CLK	H-L	DATEN	L-H	Load B	20	65†
t_{33}*	CLK	H-L	ADREN	L-H	Load B	18	60
t_{35}	TMOUT	L-H	BDMR	H-L	Load B	20	75
t_{36}	BDMGI	H-L	MASTER	L-H	Load B	90	242
t_{37}	CLK	H-L	MASTER	H-L	Load B	18	66
t_{38}	R SYNC or RPLY	H-L	MASTER	L-H	Load B	10	58

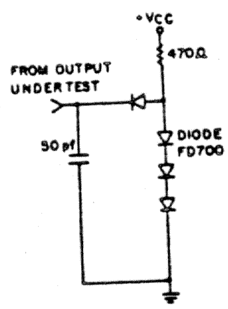
*t_{11} represents the first time ADREN is asserted.
t_{33} represents the subsequent times that ADREN is asserted.

†These propagation delays meet the following requirements.

$t_{15}-t_{16} \leq 10$ ns
$t_{15}-t_{17} \leq 10$ ns
$t_{16}-t_{26} \leq 10$ ns
$t_{25}-t_{27} \leq 20$ ns
$t_{23}-t_{26} \geq 40$ ns
$t_8-t_{36} \geq 27$ ns



LOAD A
FOR OC OUTPUTS



LOAD B
FOR TTL OUTPUTS

BUS RECEIVERS AND BUS DRIVERS

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 27. To perform the receiver and driver functions, DIGITAL Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 11. A typical bus driver circuit is shown in Figure 28. Note that 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package. Bus receiver (8640), bus driver (8881), and bus transceivers (8641) are shown in Figures 29, 30, and 31, respectively. Table 12 presents the characteristics for the type 8641 bus transceiver.

These receiver and driver ICs are available in quantities of ten each with the following order numbers

IC Type	Order No.
8881	957
8640	956
8641	964

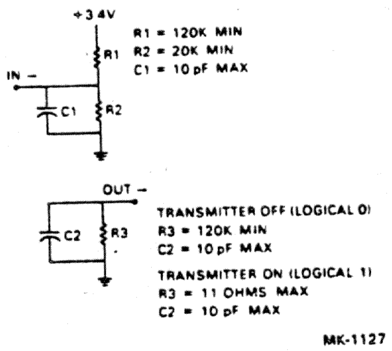


Figure 27 Bus Driver and Receiver Equivalent Circuits

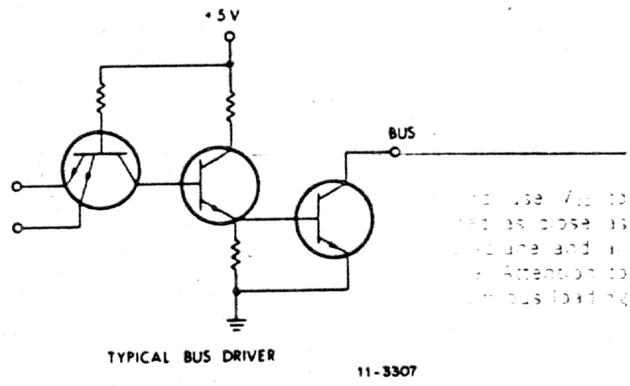


Figure 28 Typical Bus Driver Circuit

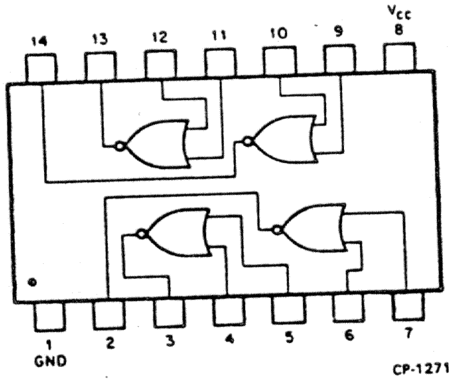


Figure 29 8640Quad 2-Input NOR Gate (Bus Receiver)

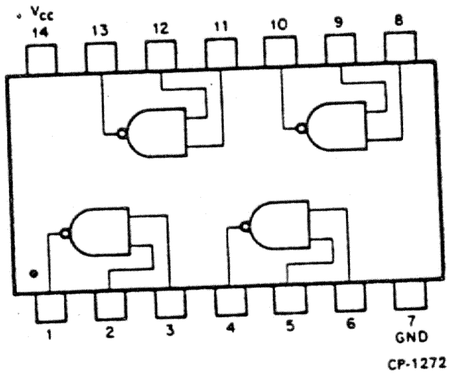


Figure 30 8881 Quad 2-Input NAND Gate (Bus Driver)

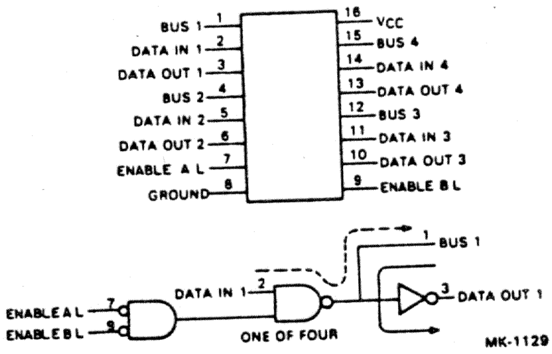


Figure 31 8641 Quad Unified Bus Transceiver (Bus Receiver/Driver)

Table 11 LSI-11 Bus Driver, Receiver Characteristics

Device	Characteristic	Sym	Specifications	Notes
Receiver (8640)	Input high voltage	V_{IH}	1.7 V min	1
	Input low voltage	V_{IL}	1.3 V max	1
	Input current at 3.8 V	I_{IH}	80 μA max	1,2
	Input current at 0 V	I_{IL}	−10 μA max	1,2
	Output high voltage	V_{OH}	2.4 V min	
	Output high current	I_{OH}	−2 mA max	2
	Output low voltage	V_{OL}	0.4 V max	
	Output low current	I_{OL}	20 mA max	2
	Propagation delay to high state	TPDH	10 ns min 35 ns max	3, 4
	Propagation delay to low state	TPDL	10 ns min 35 ns max	1.4
Driver (8881)	Input high voltage	V_{IH}	2.0 V min	
	Input low voltage	V_{IL}	0.8 V max	
	Input high current	I_{IH}	40 μA max (VIN = 2.4 V)	
	Input low current	I_{IL}	-2.0 mA max	
	Output low voltage 70 mA sink	V_{OL}	0.8 V max	1
	Output high leakage current at 3.5 V	I_{OH}	25 μA max	1,2
	Supply current	I_{CC}	55 mA max (8881) 40 mA max (8640)	
	Propagation delay to low state	TPDL	25 ns max	1,4
	Propagation delay to high state	TPDH	35 ns max	1,4

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. Current flow is defined as positive if into the terminal.
3. Conditions of load are 390 Ω to +5 V and 1.6 kΩ in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
4. Times are measured from 1.5 V level on input to 1.5 V level on output.

Bus receivers and drivers should be well grounded and use V_{CC} to ground bypass capacitors. These gates should be located as close as practical to the module fingers which plug into the backplane and all etch runs to the bus should be kept as short as possible. Attention to these cautions should yield a module design with minimum bus loading (capacitance).

Table 12 LSI-11 Bus Transceiver Characteristics for 8641

Device	Characteristic	Symbol	Spec	Condition
Receiver	Input high voltage	V_{IH}	1.7 V min	V_{CC} = 5.25 V
	Input low voltage	V_{IL}	1.3 V max	V_{CC} = 4.75 V
	Input current at 2.4 V	I_{IH}	40 μA max	
	Input current at .4 V	I_{IL}	−1.6 mA max	
Driver	Output low voltage	V_{OL}	.7 V max	70 mA sink
	Output high voltage	V_{OH}	2.4 V max	Output = 2 mA
	Output high current	I_{OH}	100 μA max	Output = 4 V
	Output low current	I_{OL}	−85 μA max	Output = OV
	Supply current	I_{CC}	90 mA max	V_{CC} = 5.25 V

APPLICATIONS—GENERAL

DIGITAL's CHIPKITS are offered in two groups: the Program Control kits (DCK11-AA and -AC) and the DMA kits (DCK11-AB and -AD).

A program control interface is used when

- low- to medium-speed data transfers are satisfactory
- it is allowable to interrupt the processor for each data transaction

The Program Control kits contain integrated circuits DC003, DC004 and DC005 which supply the logic necessary to provide a program transfer interface to the LSI-11 bus. These chips perform bus address decoding, interrupt vector generation, bus drive/receive, and LSI-11 bus protocol functions. A program control interface application circuit is presented under Program Control CHIPKIT Application.

A DMA interface is used when

- high-speed data transfer is required
- minimum software overhead is required
- multiple transfers, independent of processor operations, are required
- programmed data paths (e.g., to certain sections of memory) must be established

The DMA kits contain the integrated circuits in the Program Control kits plus the DC006 and DC010. These additional chips perform DMA control and word count/bus address register functions needed for DMA data transfers to the LSI-11. A DMA interface application circuit is presented under DMA CHIPKIT Application.

PROGRAM CONTROL CHIPKIT APPLICATION

In Figure 32, the transceivers (four DC005s) provide data lines D0 through D15 to reflect the state of the bus BDAL lines when REC H is asserted, and to drive the BDAL lines when XMIT is asserted. Address and interrupt vector information for interrupt request and device selection is also provided by the DC005. The device address is set up using input lines A3 through A12, while the interrupt vector address is set up using input lines V3 through V8.

When the address lines (JA input on DC005s) match the state of the associated BDAL lines, the MATCH will float high such that all DC005s will let ENB H on the DC004 be asserted, thus enabling the DC004 to look for proper synchronizing signals from the bus. Once these synchronizing signals (BDIN, BDOUT, BSYNC, and BWTBT) are present, the DC004 generates the control signals (INWD L, OUT HB L, OUT LB L and SEL 0, 2, 4, 6) for the user's device.

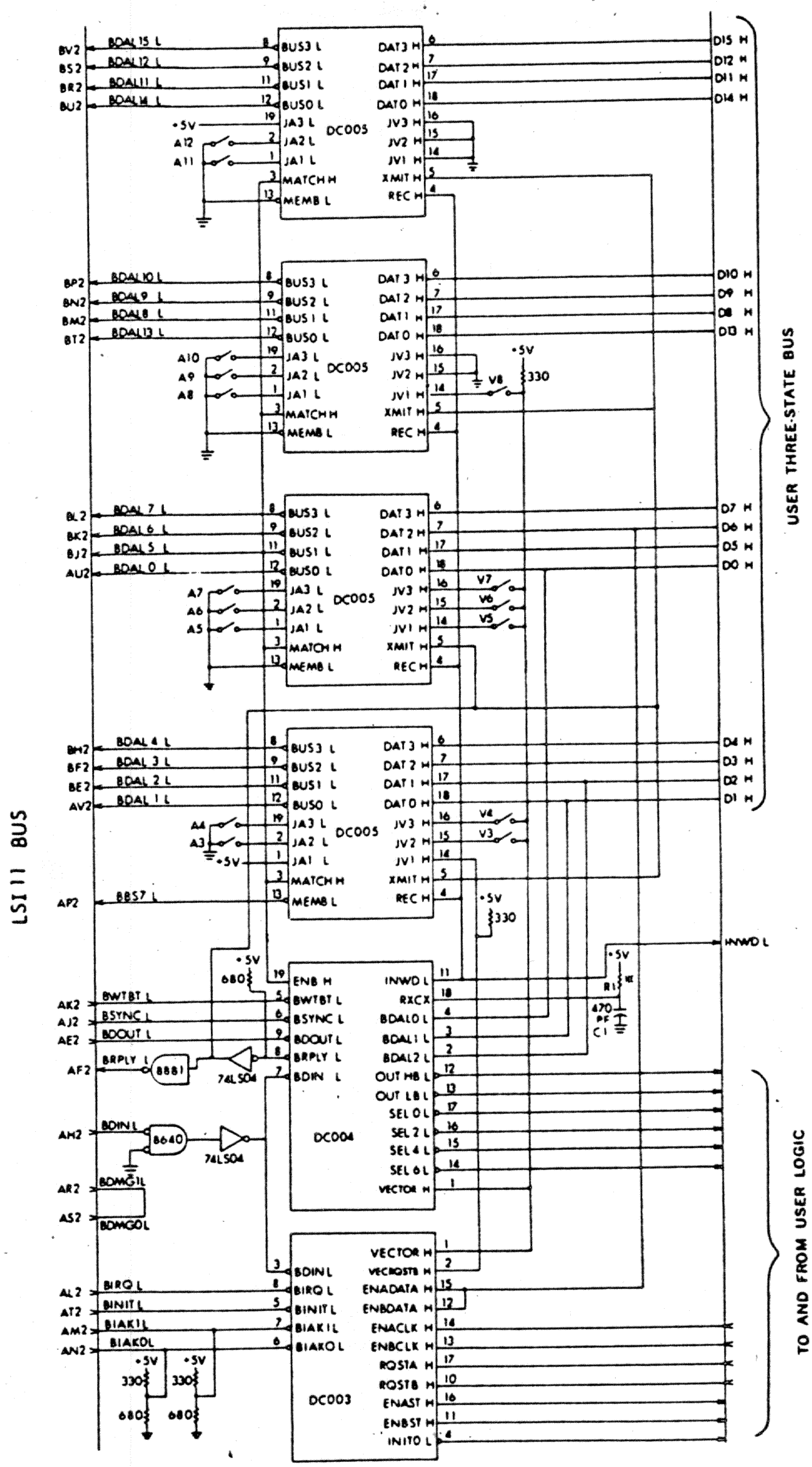
The protocol logic (DC004) functions as a register selector to provide the signals necessary to control data flow into and out of the user's word registers. When the proper device address has been decoded by the device address comparator (all DC005s), ENB H goes high, thus enabling the DC004 protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic producing one of the SEL outputs while bit D0 and BWTBT are decoded for output word/byte selection (OUT HB L, OUT LB L). The device select line (SEL 0, 2, 4, 6) and word/byte select lines (INWD L, OUT HB L, OUT LB L) are used by user's logic. Each SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers.

Either BDIN L or BDOUT L, depending on the bus cycle, will initiate a delay whose value is dependent on the time constant of the RC network connected to pin RXCX H of the DC004. The end of this delay will initiate a reply to the CPU indicating that the address has been received.

The interrupt logic (DC003) performs an interrupt transaction. Two channels (A and B) are provided for generating two interrupt requests, with channel A having the highest priority. The interrupt enable flip-flop within the interrupt logic must first be set when the user's device is to control the LSI-11 bus. This is accomplished by asserting (logic H) the ENX DATA* line and then clocking the enabled flip-flop by asserting the ENX CLK* line. With the interrupt enable flip-flop set, the user's device may then make an interrupt request by asserting (logic H) RQSTX*. When RQST is asserted and the interrupt enable flip-flop is set, the interrupt logic asserts BIRQ L to the bus which initiates the bus "handshake" operation. This operation terminates with the generation of the vector address by the DC005 under the control of the DC003.

The interrupt logic available to the user indicates the status of the interrupt logic enable flip-flops. Each line is asserted (logic H) when the appropriate interrupt enable flip-flop is set. These status lines can function as part of the user's control status register (CSR). The VECRQSTB H line is asserted (logic H) when the device connected to channel B has been granted use of the bus for interrupt vector transfer operation. When VECRQSTB H is unasserted (logic L), the user's device connected to channel A of the interrupt logic has been granted use of the bus. The INITO L output from the interrupt logic can be used to initialize the user's logic.

* X may be either A or B depending on which half of the interrupt logic is being enabled.



NOTE:
CLOSE SWITCH FOR ONE
OPEN SWITCH FOR ZERO

Figure 32 DCK11 Bus Interface Typical Application

The drawings on the following pages show example circuits that may be helpful in applying the CHIPKITS.

This example is the interrupt enable bit for interrupt A which connects to bit 6 of the example CSR.

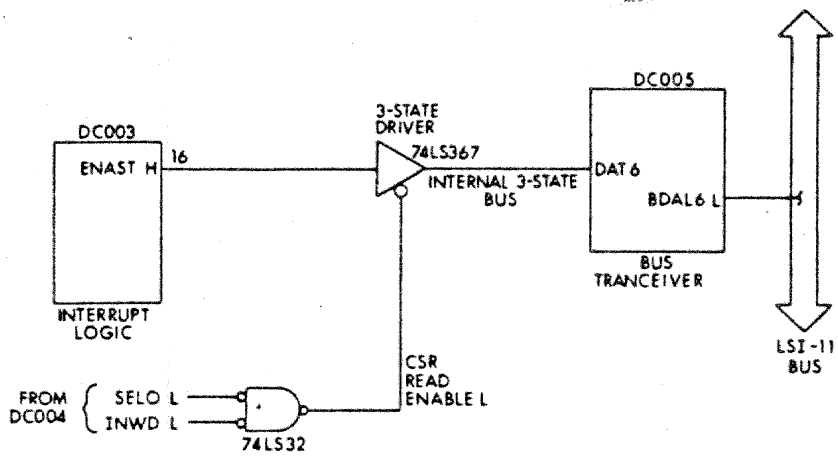


Figure 33 Typical CSR Bit

This example is the A interrupt request and a DATA READY status bit. (Bit 7 of the CSR).

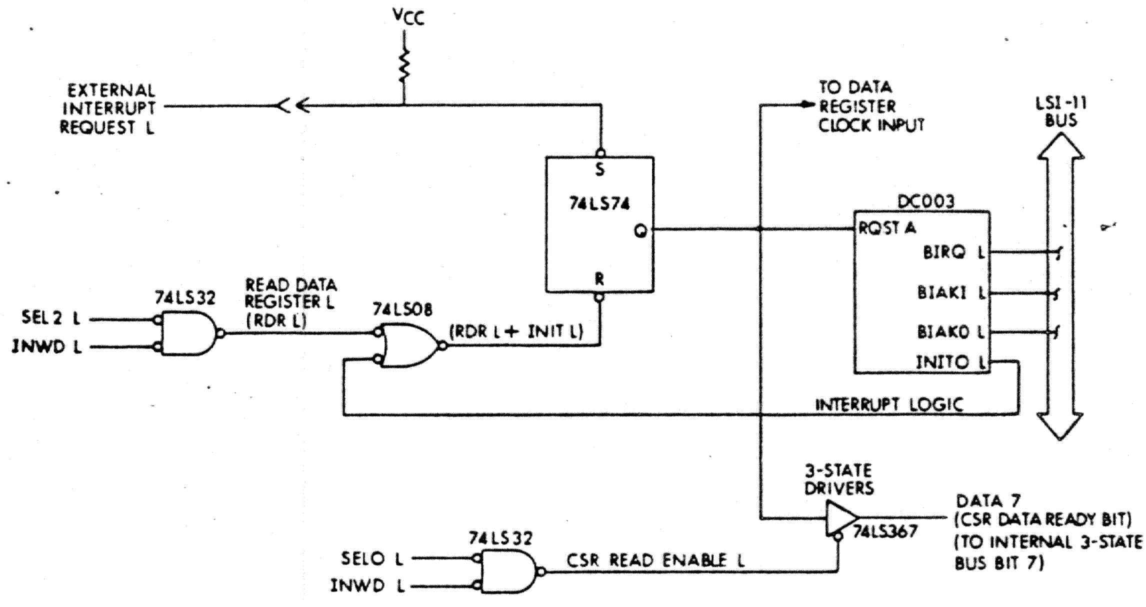


Figure 34 Typical Interrupt Request

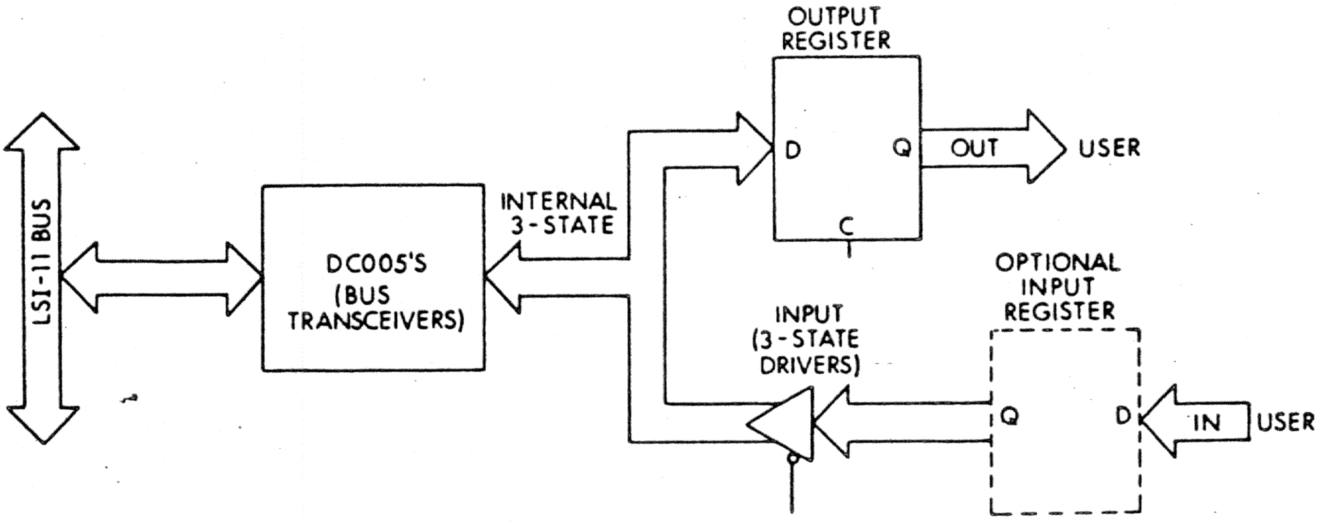
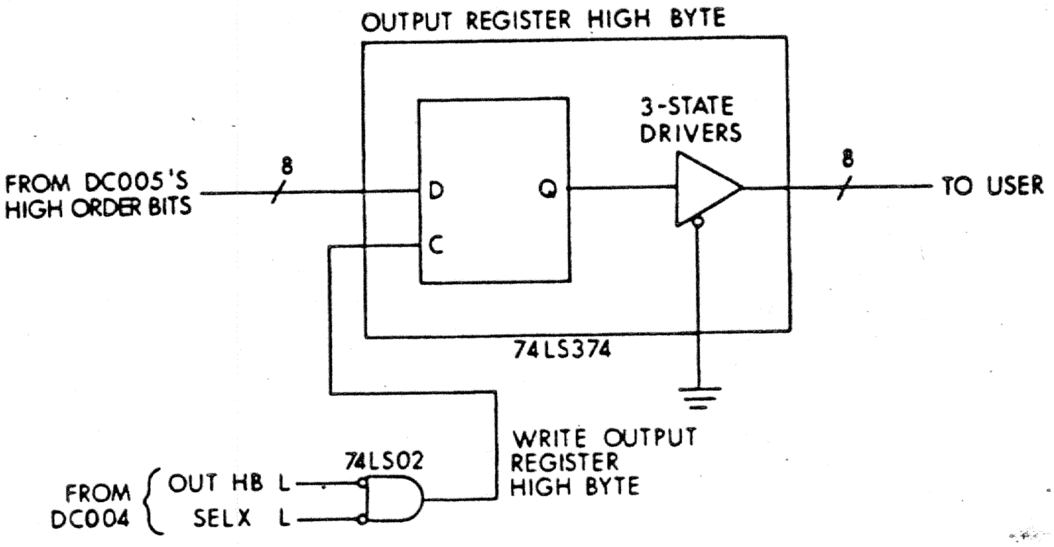


Figure 35 Data Path Flow Diagram



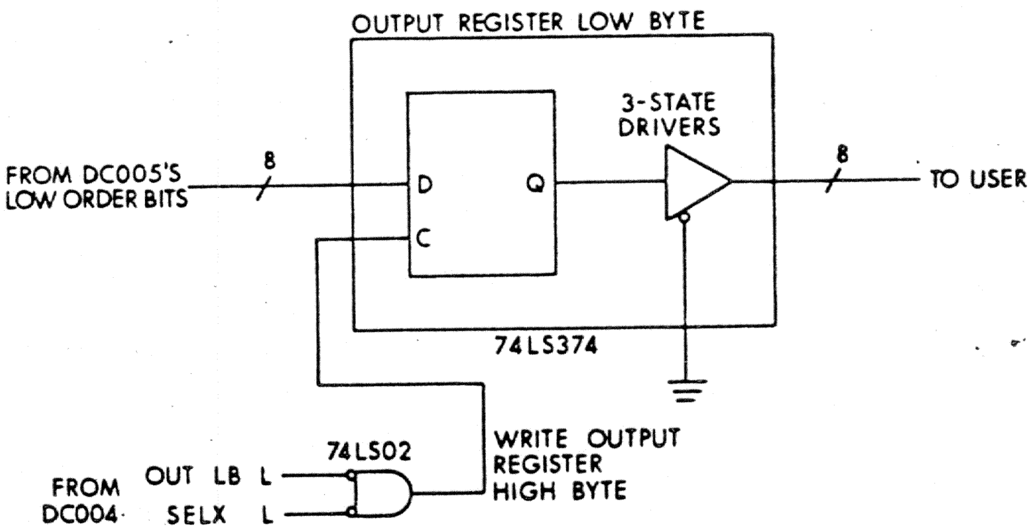


Figure 36 Example of Output Register

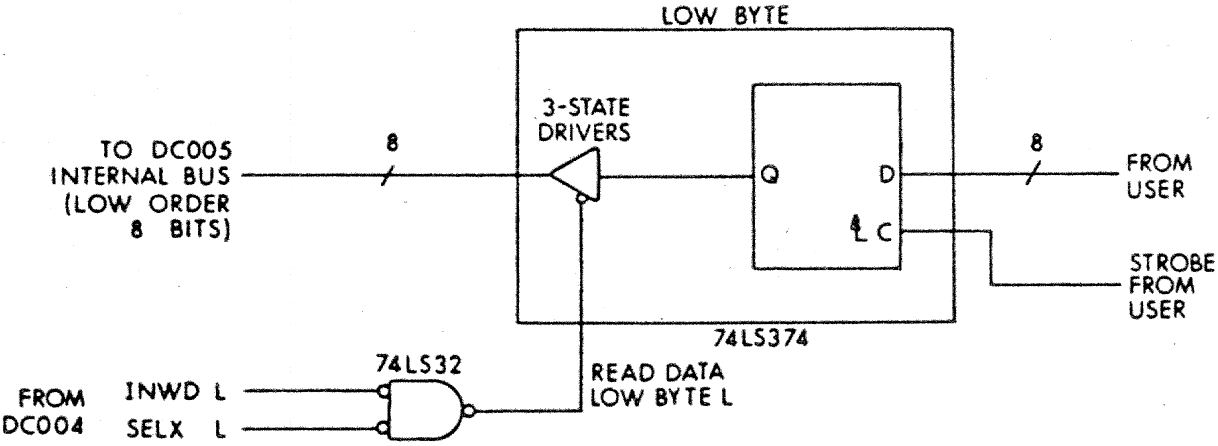


Figure 37 Example of Input with Register (BYTE)

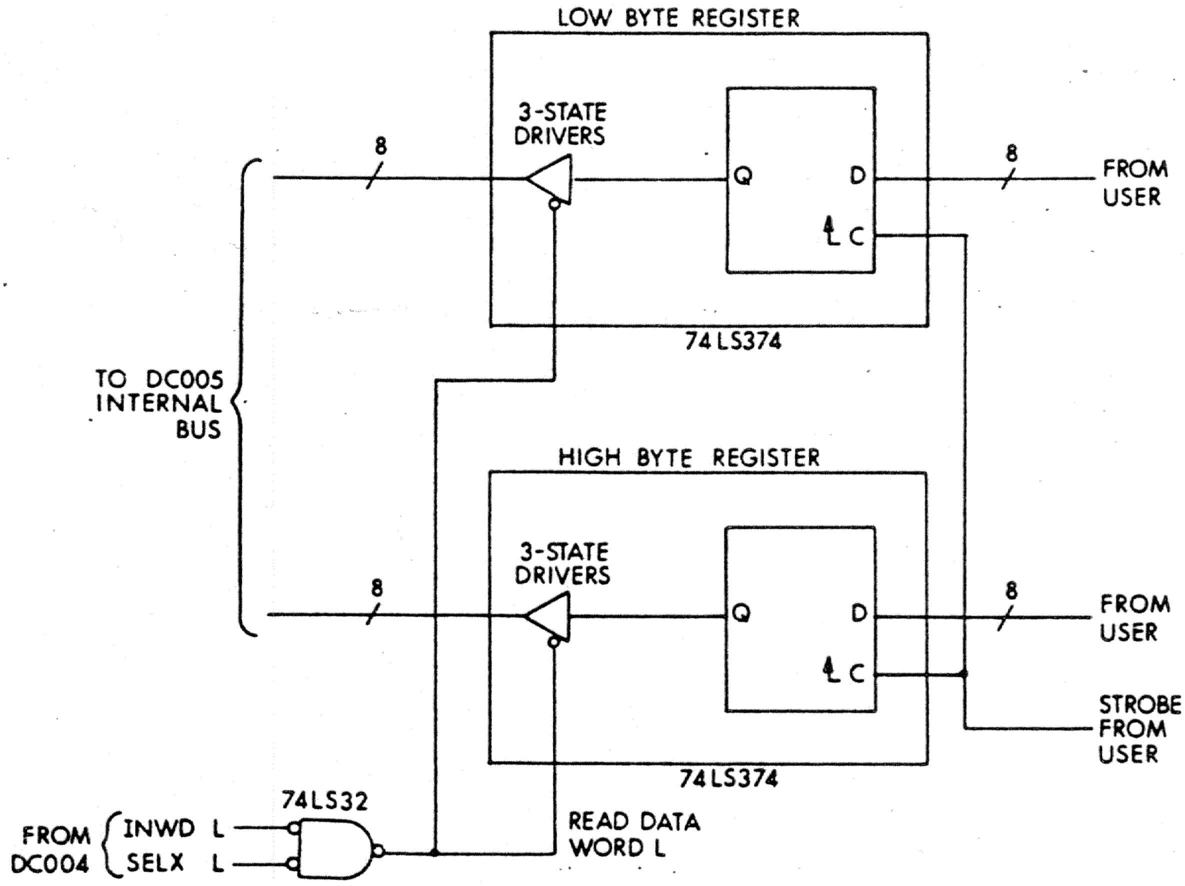
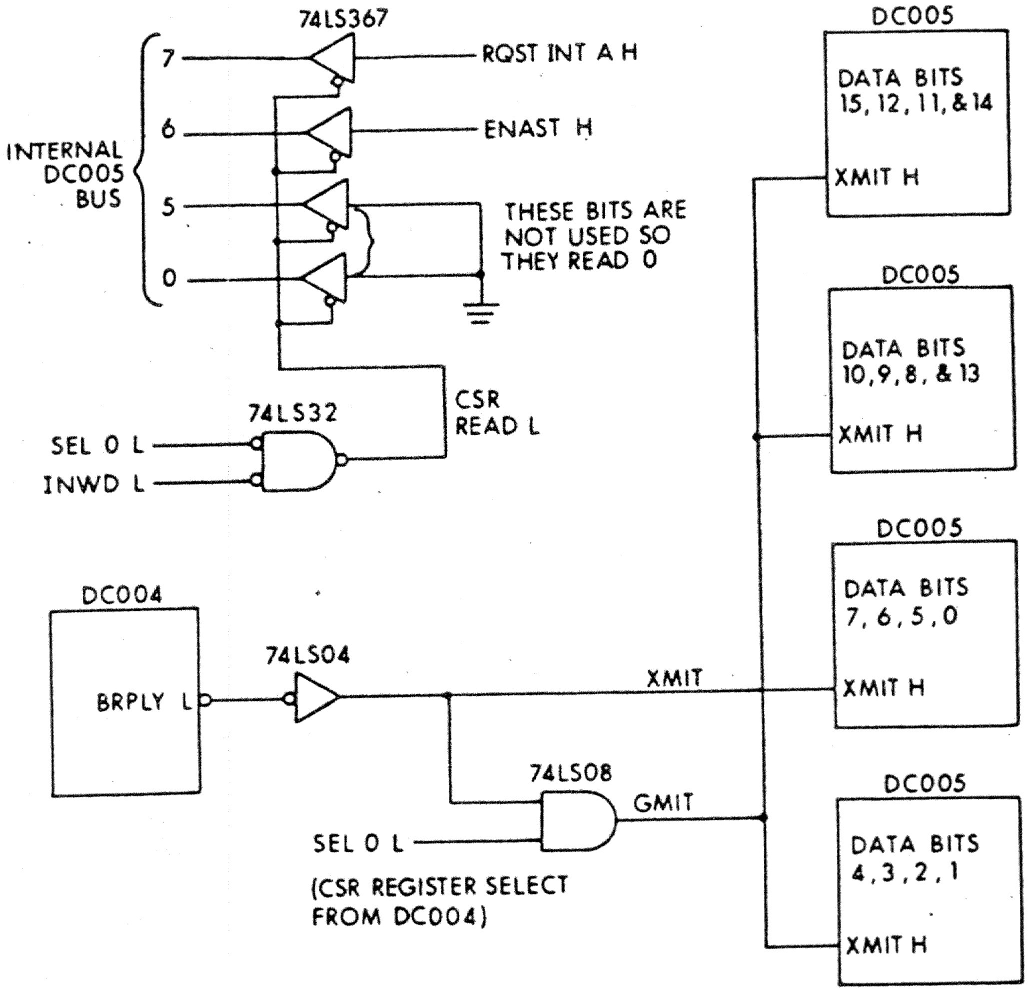


Figure 38 Example of Input with Register (WORD)



WHEN THE CSR IS READ (SEL 0 L = 0) THE SIGNAL GMIT WILL BE 0 CAUSING THE UNUSED DC005 BITS TO BE READ AS ZEROS. (HIGH ON BDAL LINES) FOR ANY OTHER REGISTER GMIT = XMIT.

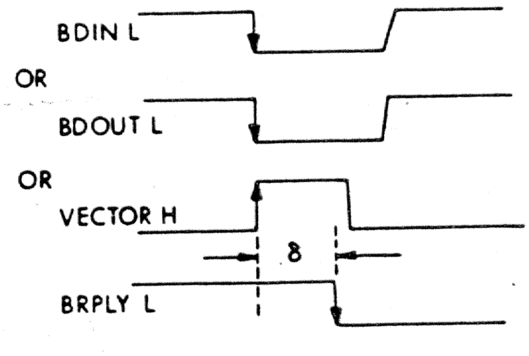
Figure 39 Example Circuit to Cause Unused CSR Bits to be Read as Zeros

BUS REPLY DELAY TIMES

Bus Replv Delays as a function of RC values connected to pin 18 RXCX H. DC004

Delay = [.318 (R)(C)] + 50 ns

1. RX = 1KΩ 5%
   CX = 0
   Delay ≅ 50 ns from falling edge of BDIN L, or BDOUT L, or rising edge of VECTOR H to BRPLY L falling edge.
2. RX = 1KΩ 5%
   CX = 470 pf 5%
   Delay as described in item 1 above ≅ 200 ns.
3. RX = 10KΩ 5%
   CX = 1000 pf 5%
   Delay as described above. ≅ 3.2 usec



WHERE 8 = DELAY DESCRIBED IN ITEMS 1-3

DMA CHIPKIT APPLICATION

Referring to Figure 40, four DC005 transceivers are used to handle the first 16 BDAL lines (BDAL 0–BDAL 15) from the LSI-11 bus and to provide the interface to the internal 3-state bus. The transceivers are enabled to receive data from the LSI-11 bus when the REC H line is driven high. Similarly, the transceivers transmit data to the LSI-11 bus when the XMIT H line is driven high. Normally, the DC005s are in the receive state (REC H line asserted) and allow the transceivers to monitor the LSI-11 bus for device addresses.

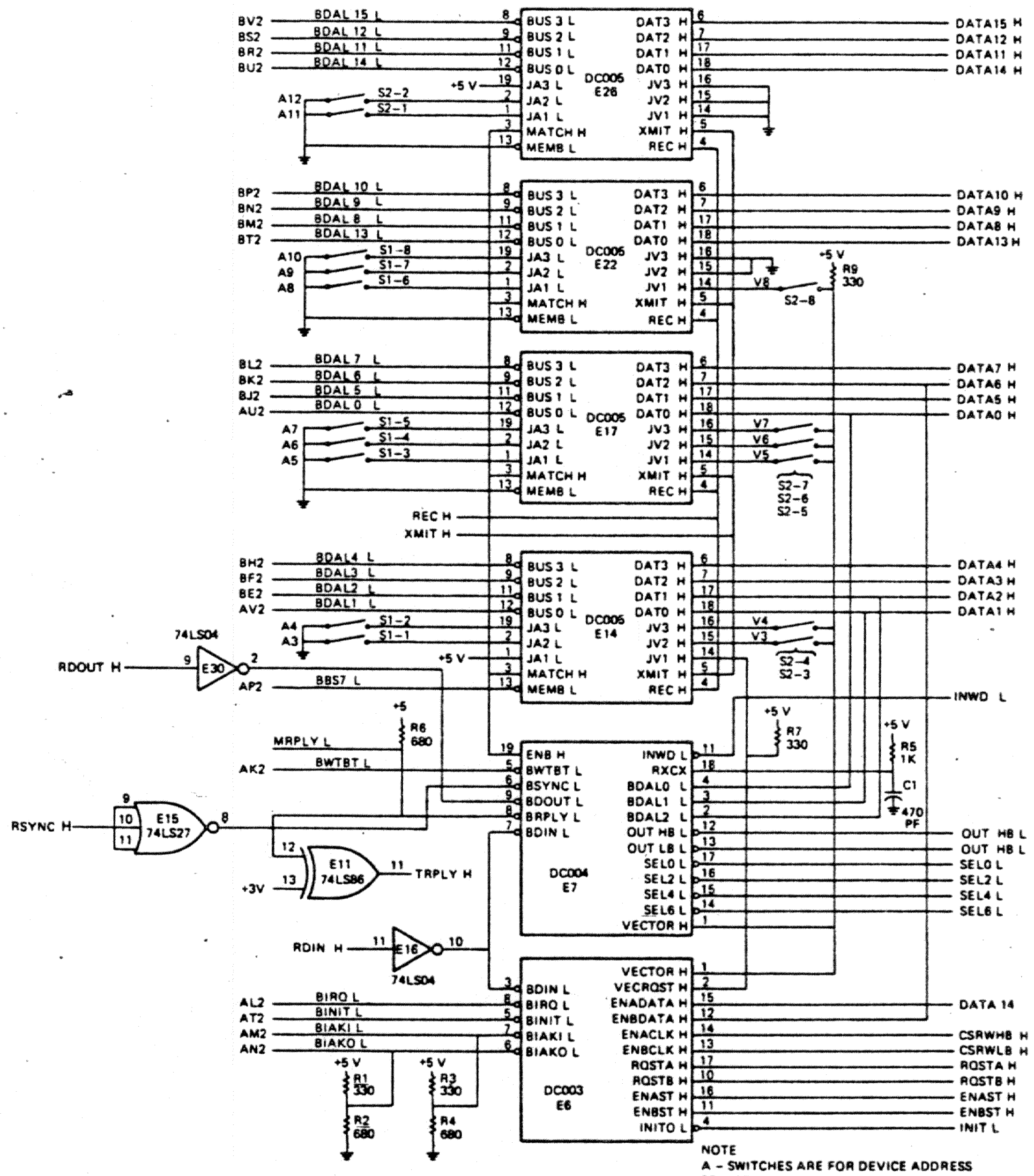
Device address and vector switch inputs to the transceivers provide convenient address and vector selection.

Switches A3 through A12 are the device address selection switches, and switches V3 through V8 are for vector selection. Switches are ON (closed) for a 1 bit and are OFF (open) for a 0 bit. The switch settings for the device addresses and vector are shown in Figures 41 and 42 respectively. The addressable registers are:

Register	Bank 7 Octal Address
Bus Address Register	1XXXX0
Word Count Register	1XXXX2
Control/Status Register	1XXXX4
Output Buffers	1XXXX6

The user selects a base address for the bus address register and sets the device address selection switches to decode this address. The remaining register addresses are then properly decoded as sequential addresses beyond the bus address register.

The DC004 is the internal register selector. This integrated circuit monitors BDAL lines 0, 1, and 2 to determine which register address has been placed on the LSI-11 bus. The states of BDOUT and BDIN are also monitored to determine the type of transfer (DATO or DATI). When an address for an internal register is placed on the LSI-11 bus, one of the SEL outputs from the DC004 is driven low. This selects that particular register for the transfer of data. The direction of transfer (into or out of



NOTE
A – SWITCHES ARE FOR DEVICE ADDRESS SELECTION.
V – SWITCHES ARE FOR VECTOR SELECTION.
CLOSE (ON) SWITCH FOR "1".
OPEN (OFF) SWITCH FOR "0".

Figure 40 Typical Application (DC003, DC004, DC005)

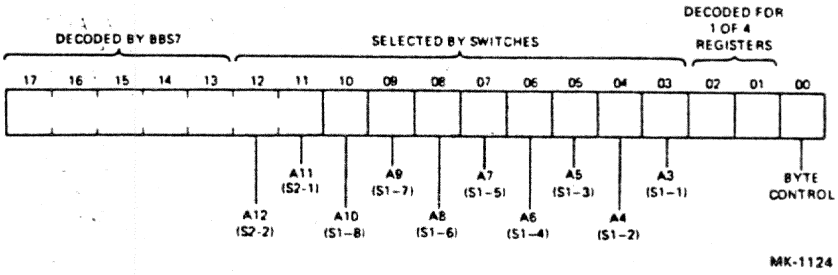


Figure 41 Device Address Select Format

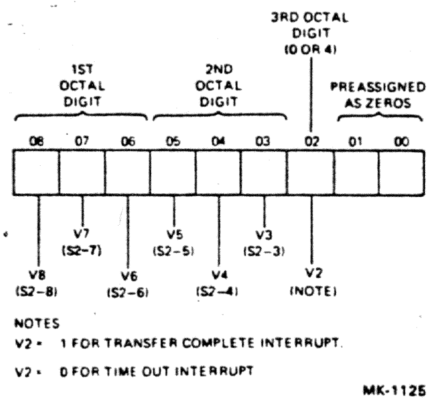


Figure 42 Interrupt Vector Select Format

the master device) is determined by the state of the OUT HB L, OUT LB L, or INWD L lines. Internal register selection is summarized as follows:

Control Line	Select	Register
INWD L (Read)	SEL 0 L	Bus Address Register
INWD L (Read)	SEL 2 L	Word Count Register
OUT HB L (Write High Byte)	SEL 0 L	Bus Address Register
OUT HB L (Write High Byte)	SEL 2 L	Word Count Register
OUT LB L (Write Low Byte)	SEL 0 L	Bus Address Register
OUT LB L (Write Low Byte)	SEL 2 L	Word Count Register
INWD L (Read)	SEL 4 L	Control/Status Register
OUT HB L and MRPLY L (Write CSR High Byte)	SEL 4 L	Control/Status Register
OUT LB L and MRPLY L (Write CSR Low Byte)	SEL 4 L	Control/Status Register
OUT HB L and MRPLY L (Write High Byte)	SEL 6 L	Output Buffer
OUT LB L and RMPLY L (Write Low Byte)	SEL 6 L	Output Buffer

Note that MRPLY L is the BRPLY L output of the DC004 and is used along with OUT HB L and OUT LB L to write either the high or low byte in the control/status register or the output buffers. Write byte selection for the bus address register and the word count register is controlled only by the OUT HB L and OUT LB L lines. Words can be written to the control/status register or the output buffer registers by driving both OUT HB L and OUT LB L to the low state at the same time.

The DC004 integrated circuit was designed to operate directly from the LSI-11 bus. However, since the introduction of the DC005, the DC004 is usually interfaced to the LSI-11 bus through DC005. Bus signals (BDAL lines) passing through the DC005 are inverted. Therefore, BDAL 0, 1, and 2 signals applied to the DC004 are inverted. Because of this inversion, it is necessary to change the nomenclature on pins 12 through 17 on the DC004. The difference in nomenclature between DC004s operated directly from the LSI-11 bus and through a DC005 are as follows.

From Bus (Non-Inverted BDAL 0, 1, 2)		From DC005 (Inverted BDAL 0, 1, 2)	
Pin	**Signal**	**Pin**	**Signal**
12	OUT LB L	12	OUT HB L
13	OUT HB L	13	OUT LB L
14	SEL 0 L	14	SEL 6 L
15	SEL 2 L	15	SEL 4 L
16	SEL 4 L	16	SEL 2 L
17	SEL 6 L	17	SEL 0 L

It is recommended that when a DC005 is used, the DC004 be interfaced to the LSI-11 bus through the DC005 to avoid unnecessary bus loading.

Note: All references in the manual made to the DC004 are as if being interfaced to the DC005.

The DC003 IC performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DC003 has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the DC003 must be set. This is accomplished by asserting (logic 1) the ENX* DATA line to the DC003 (writing bit 14 or bit 6 to a one) and then clocking the enable flip-flop by asserting (positive transition) the DC003 ENX* CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logic 1) RQST. RQST must be held asserted until the interrupt is serviced. When the RQST is asserted and the interrupt enable flip-flop is set, the DC003 asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L. This causes the DC003 to assert (logic 1) VECTOR H, which is applied to the DC005. VECTOR H at the DC005 causes the device vector to be placed on the BDAL lines to the processor. Interrupts are produced for bus time-outs (CSR bits 15 and 14) and at the completion of a block transfer (CSR bits 7 and 6).

* X may be either A or B

DMA Application
Figure 43 shows the DMA control (DC010), the word count/bus address registers (both DC006), the output buffers (both 74LS273s), and the input drivers (74LS367s).

The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA data transfers. After becoming bus master, the DC010 produces the signals necessary to perform a DIN or DOUT bus cycle as specified by the control lines. An 8-MHz free-running clock is provided by E21. This clock is used by the DC010 to generate all transfer timing sequences. The actual clock frequency is not critical and can be any frequency up to 8.3 MHz, provided it is symetrical. An RC time constant provided by resistor R14 and capacitor C2 provides a delay for the reassertion of BDMR to the LSI-11 bus. This allows other direct memory access devices to obtain the bus during the time the CNT4 logic releases the bus and re-requests the bus.

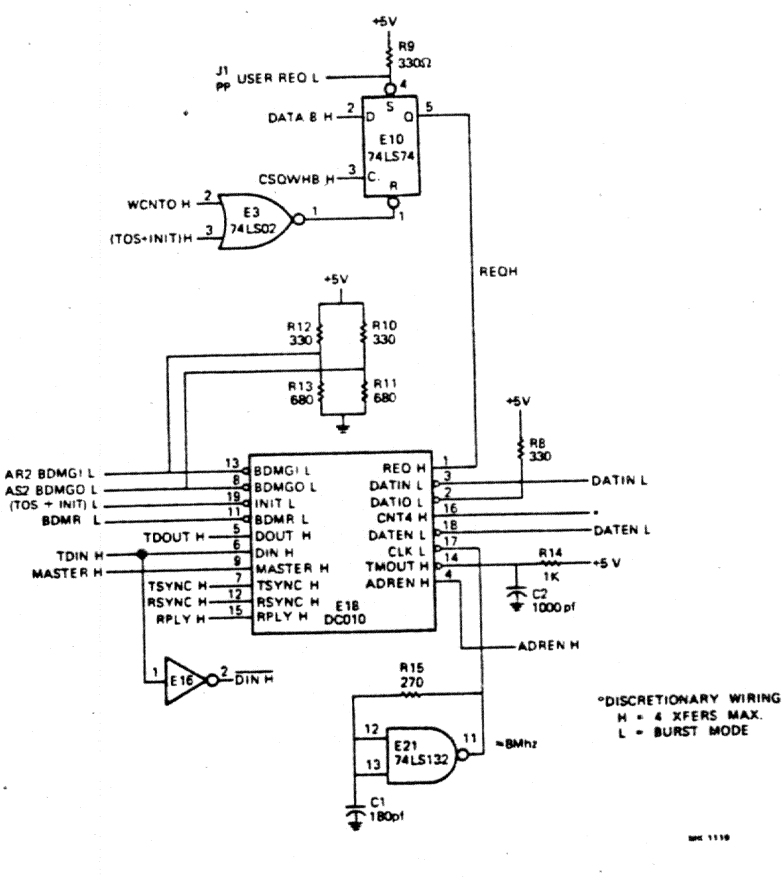


Figure 43 Typical Application
(DC006, DC010, Output Delay, and Input Drives)
(Sheet 1 of 2)

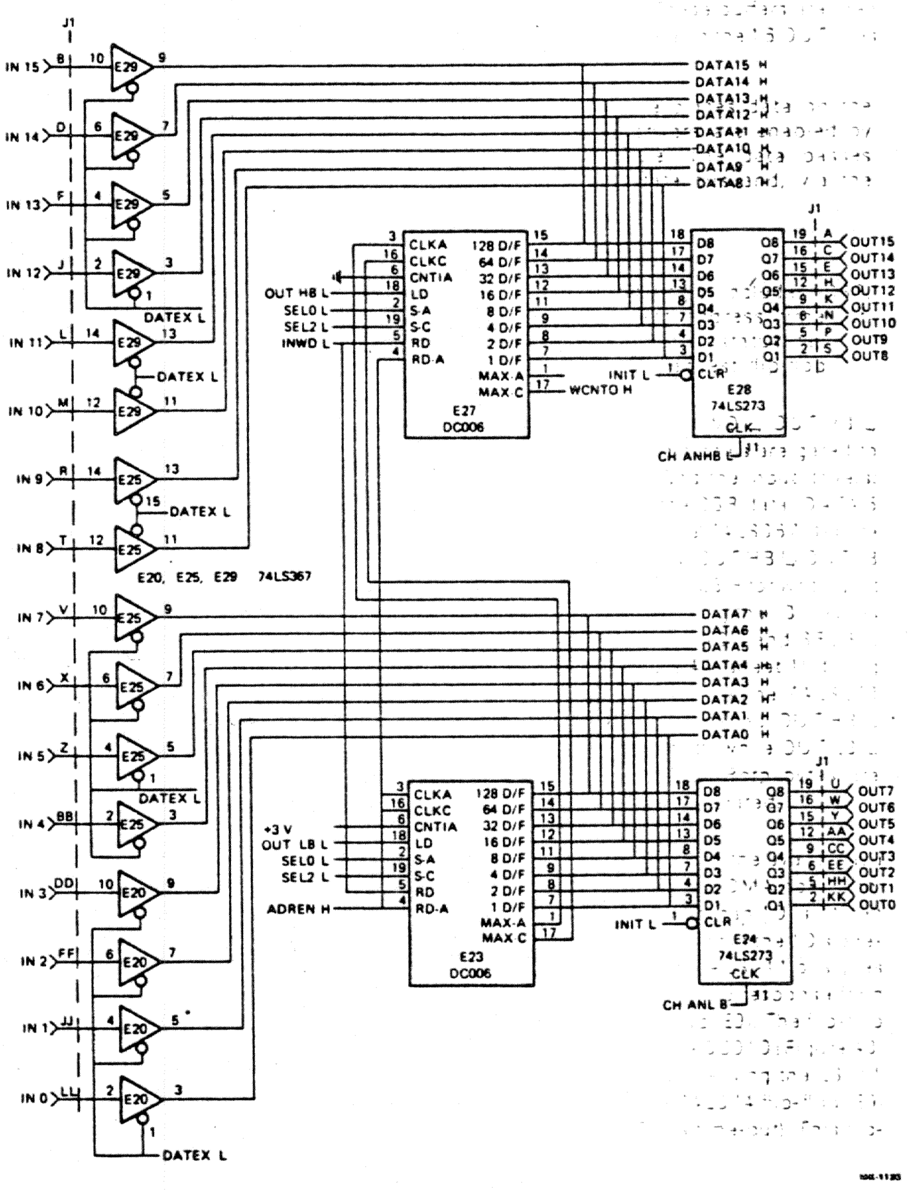


Figure 43 Typical Application
(DC006, DC010, Output Delay, and Input Drives)
(Sheet 2 of 2)

User devices initiate bus requests by driving the set input of the request flip-flop (E10) low. This asserts REQ to the DC010 and generates BDMR L to the LSI-11 bus. When the DC010 becomes bus master, it asserts ADREN H to the DC006 bus address registers. ADREN H allows the bus address registers to place the address of the slave (memory) onto the internal bus and, via the DC005 transceivers, onto the LSI-11 bus. The request flip-flop (E10) remains set until the DC006 word count overflows to zero (WCNTO). WCNTO then resets the request flip-flop.

Two DC006 word count/bus address register ICs are used to provide 16 bits each of word count and bus address. The least significant bits of the word count and bus address are provided by DC006/E23; the most significant bits are provided by DC006/E27. Register A is the bus address register and register C is the word count register. Both registers can be read or written under program control from the LSI-11 bus. Registers are selected by:

• Read bus address register	SEL 0 L INWD L
• Write high byte of bus address register	SEL 0 L OUT HB L
• Write low byte of bus address register	SEL 0 L OUT LB L
• Read word count register	SEL 2 L INWD L
• Write high byte of word count register	SEL 2 L OUT HB L
• Write low byte of word count register	SEL 2 L OUT LB L

The bus address register is incremented by 2 for word transfers. To accomplish the increment by two, the CNT1A input to the least significant DC006 (E23) must be high, and the CNT1A input to the most significant DC006 (E27) must be grounded. Clocking for DC006 E23 is provided by the transition of the ADREN H line from the DC010. When bus address register DC006 E23 overflows, MAX-A goes high, thus clocking the DC006 E27 bus address register.

The word count register is incremented by one each time a word is transferred. Initially, the word count register is loaded under program control, with the 2's complement of the number of words to be transferred. As words are transferred, the word count register is incremented toward zero. When DC006 E23 overflows, MAX-C goes high. MAX-C clocks the DC006 E27 word count register until DC006 E27 overflows. When E27 overflows, WCNTO H is generated; WCNTO H then resets the request flip-flop (E10), thus terminating data transfers.

During DMA data transactions, input data from the DATI bus cycle is placed on the internal 3-state bus via the DC005 transceivers and is applied to the 74LS273 (E28 and E24) output buffers. These buffers are then clocked by CHANHB L and CHANLB L, thus placing the data on the 16 OUT lines to the user's device.

For output data transfers (DATO), the user's device places data on the 16 IN lines to the 74LS367 3-state drivers. The drivers are enabled by DATEX L, which is asserted during a DATO cycle. The data passes through the drivers, is applied to the internal 3-state bus and, via the DC005 transceivers, to the LSI-11 bus.

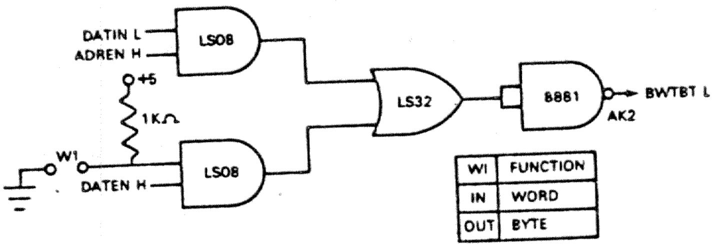
Miscellaneous Logic
Miscellaneous logic is shown in Figure 44. This logic includes CSR, output buffer and input driver control, non-existent address time-out, DC005 transceiver receive/transmit control, the control/status register (CSR), additional transceivers (8641s), and the "B" request flip-flop.

The CSR, output buffers, and input driver control receive INWD L, OUT HB L, OUT LB L, SEL 4 L, SEL 6 L, DATEN H, and $\overline{\text{DIN H}}$. These signals are gated to produce enable signals for the CSR, the output buffers, and the input drivers. CRSRD L is produced by INWD L and SEL 4 L to enable the CSR data (DATA 5 through DATA 14) (Figure 44, sheet 1) to pass through the 74LS367 3-state drivers and onto the LSI-11 bus via the DC005 transceivers. OUT HB L, OUT LB L, SEL 4 L, and MRPLY L produce either CSRWHB H or CSRWLB H for writing bit 6 of the CSR (74LS74 E10 on Figure 44, sheet 1), or for clocking the "B" reques flip-flop. DATEX L is generated either by DATEN H or by INWD L and SEL 6 L. DATEX enables the 74LS367 3-state input drivers (Figure 44, sheet 1) during an "input" cycle. The CHANHB L and CHANLB L signals clock the 74LS273 output buffers during an "output" cycle. When bytes are transferred, OUT HB L, MRPLY L and SEL 6 enable the high byte (CHANLB asserted), while OUT LB L, MRPLY L and SEL 6 L enable the low byte (CHANLB L). Both bytes are simultaneously transferred (word transfer) when $\overline{\text{DIN H}}$ is negated.

The non-existent address time-out provides a 10 s time-out in the event that a non-existent address is requested on the LSI-11 bus during a DMA operation. This prevents hanging-up the LSI-11 bus for periods longer than 10 s. When the DC010 becomes bus master, ADREN H is asserted and clocks the 10 s one-shot (E8) (see Fig. #44 sheet 2 of 3). Normally RPLY L from the LSI-11 bus goes low and the one-shot is cleared. However, if RPLY L is high (no response from slave), the one-shot times out and clocks the 74LS74 flip-flop (E9). The flip-flop is set, generating (TOS + INIT) L; this signal is applied to the DC010 (Figure 43, sheet 1) clearing the internal synchronization circuit and releasing the LSI-11 bus (TOS + INIT) H resets the request flip-flop (E10). The 74LS74 flip-flop (E9) can be set and reset with CSRWB H and DATA 15 (CSR bus time-out). This flip-flop is automatically reset during power-up.

TRANSFER CONTROL

The BWTBT L signal controls the types of transfers. This signal is asserted (L) during address time for DATO or DATOB transfers and is unasserted (H) during address time for DATI transfers. This signal must also be asserted (L) at data time to indicate byte transfers or unasserted (H) to indicate word transfers.



WI	FUNCTION
IN	WORD
OUT	BYTE

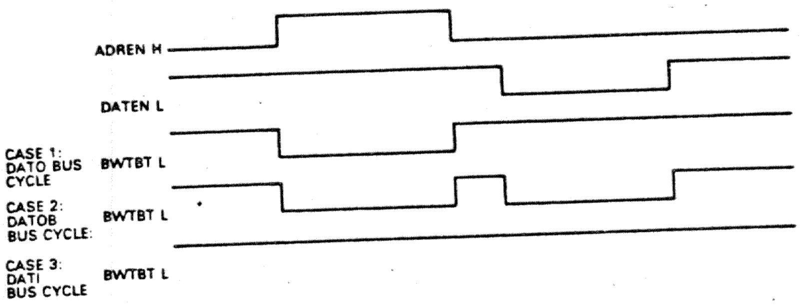


Figure 44 BWTBT L Circuitry and Logic Timing

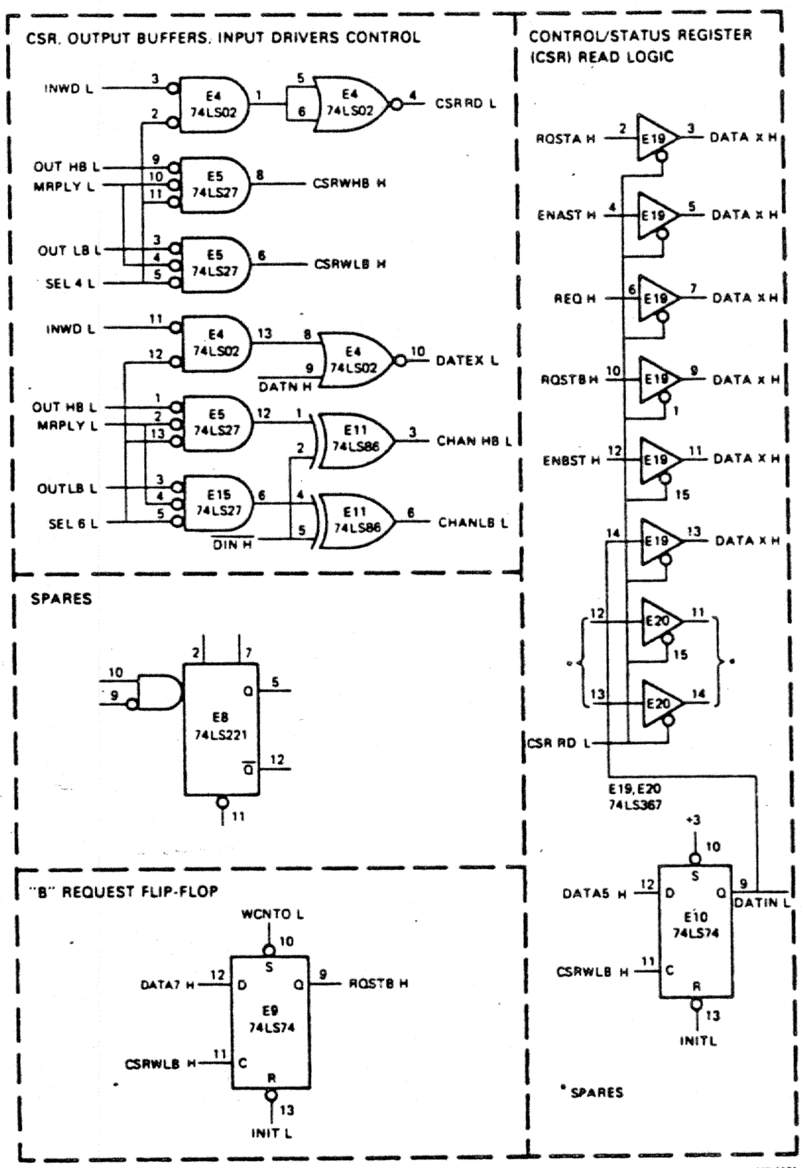


Figure 45 Typical Application (Miscellaneous Logic) (Sheet 1 of 3)

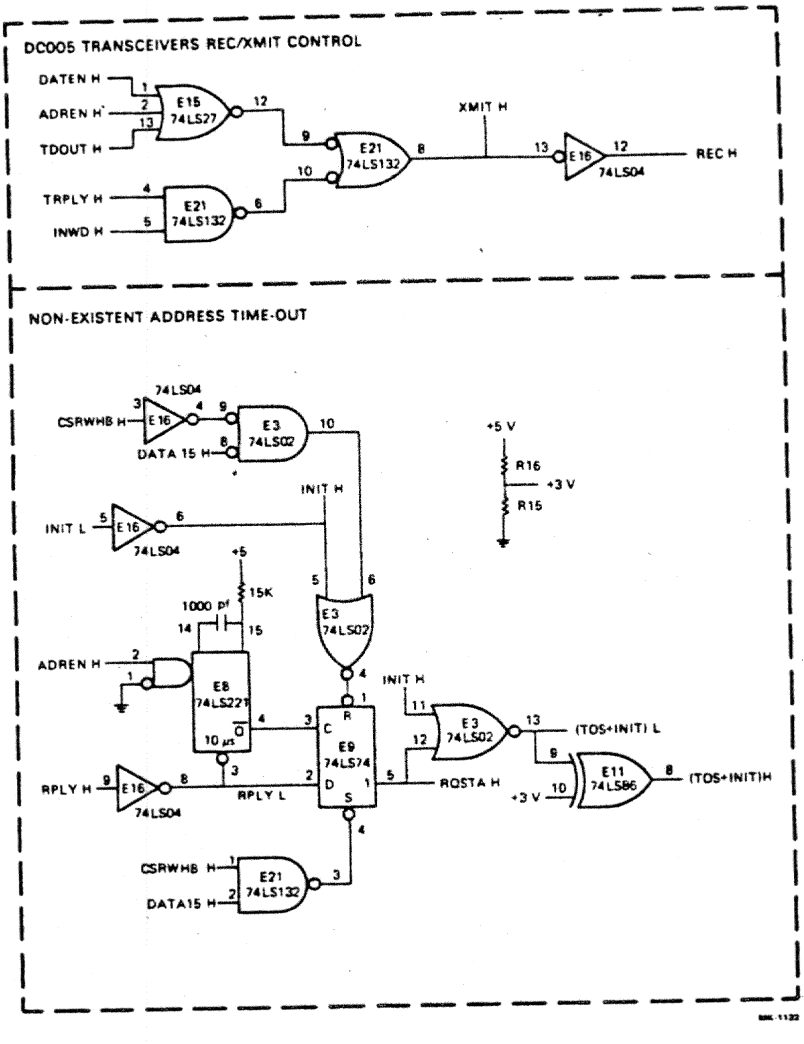


Figure 45 Typical Application (Miscellaneous Logic)
(Sheet 2 of 3)

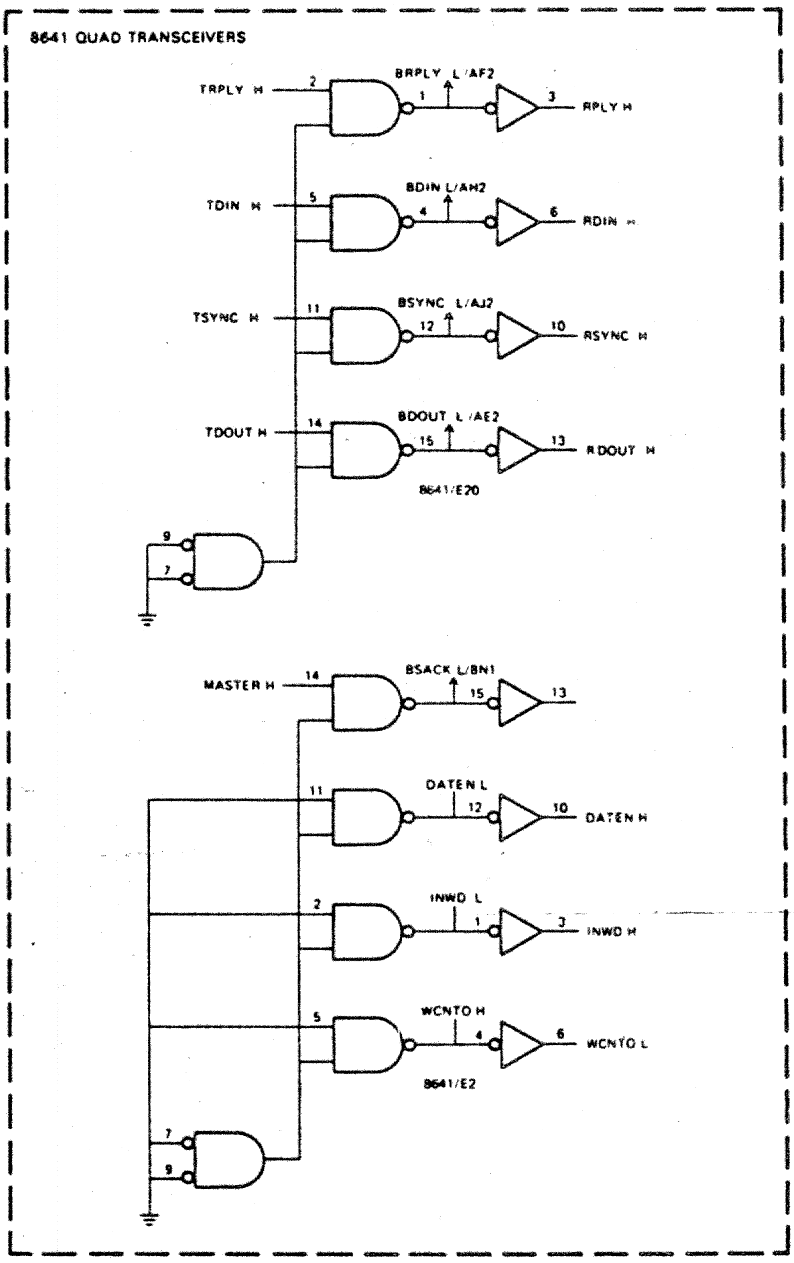


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Figure 45 Typical Application (Miscellaneous Logic)
(Sheet 3 of 3)

The DC005 transceiver receive/transmit control detemines the state of the DC005 transceivers in Figure 40. Normally, the transceivers are in the receive state to accept device addresses from the LSI-11 bus. When REC H is asserted (high), XMIT is negated (low). XMIT is asserted (high) when transferring data to the LSI-11 bus (TDOUT, DATEN, and ADREN are high; TRPLY, INWD are low). REC is asserted (high) when receiving data from the LSI-11 bus (TDOUT, DATEN, and ADREN are low; TRPLY, INWD are high).

The control/status register (CSR) (Figure 44, sheet 1) has six active bits and is a read/write register comprised of 74LS367 3-state drivers and flip-flops which are part of other logic circuits shown in Figure 44, sheet 1, and Figure 44, sheet 2. Figure 45 shows the CSR format. The CSR bits are described in Table 13.

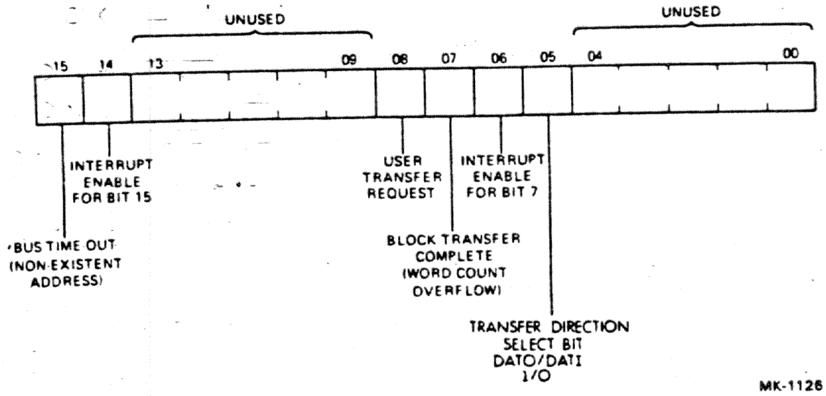


Figure 46 Control/Status Register (CSR) Format

The quad transceivers (8641) shown in Figure 44 sheet 3, supplement the DC005 transceivers for interfacing to the LSI-11 bus. In this particular application, the 8641s are permanently enabled by grounding pins 7 and 9.

Table 13 CSR Bit Descriptions

Bit	Name	Description
00 01 02 03 04	Unused	
05	DATO/DATI	When set to a 1, indicates a DATO cycle; when set to a 0, indicates DATI bus cycle.

Table 13 CSR Bit Descriptions (Cont)

Bit	Name	Description
06	Interrupt enable for bit 7	This bit must be set (1) to enable the word count overflow interrupt at the end of a block transfer. When set to 0, the interrupt is inhibited.
07	Block transfer complete	This bit sets (1) when the word count register overflows, providing bit 06 is set.
08	User transfer request	The user's device must set (1) this bit to make a bus request and transfer data. User REQ L (J1-PP) must be driven low (0) to set bit 08. This bit is always read as a zero. This is an example for test purposes.
09 10 11 12 13	Unused	
14	Interrupt enable for bit 15	This bit must be set (1) to enable the bus time-out interrupt. When set to a 0, the interrupt is inhibited.
15	Bus time-out	This bit sets (1) when a slave on the LSI-11 bus does not respond with BRPLY within 10 μs after being addressed. Bit 14 must be set (1) to enable the bus time-out interrupt.

ADDITIONAL INFORMATION AND DATA FOR USE WITH DMA CHIPKIT APPLICATIONS

Logic to Support DATIO and DATIO B Bus Cycles

The circuit shown in Figure 46 is used to toggle the DATIO L input to the DC010 when it is used for DATIO, DATIO B bus cycles. As shown by the dotted line this circuit may be used with a hard-wired configuration where only DATIO, DATIO B cycles are used or connected to a CSR bit for selection of the type of bus cycle to be used. Although this circuit was not part of the original DMA application information and therefore no CSR bit exists in the drawings, it was added to the board to verify that the board could perform DATIO and DATIO B bus cycles.

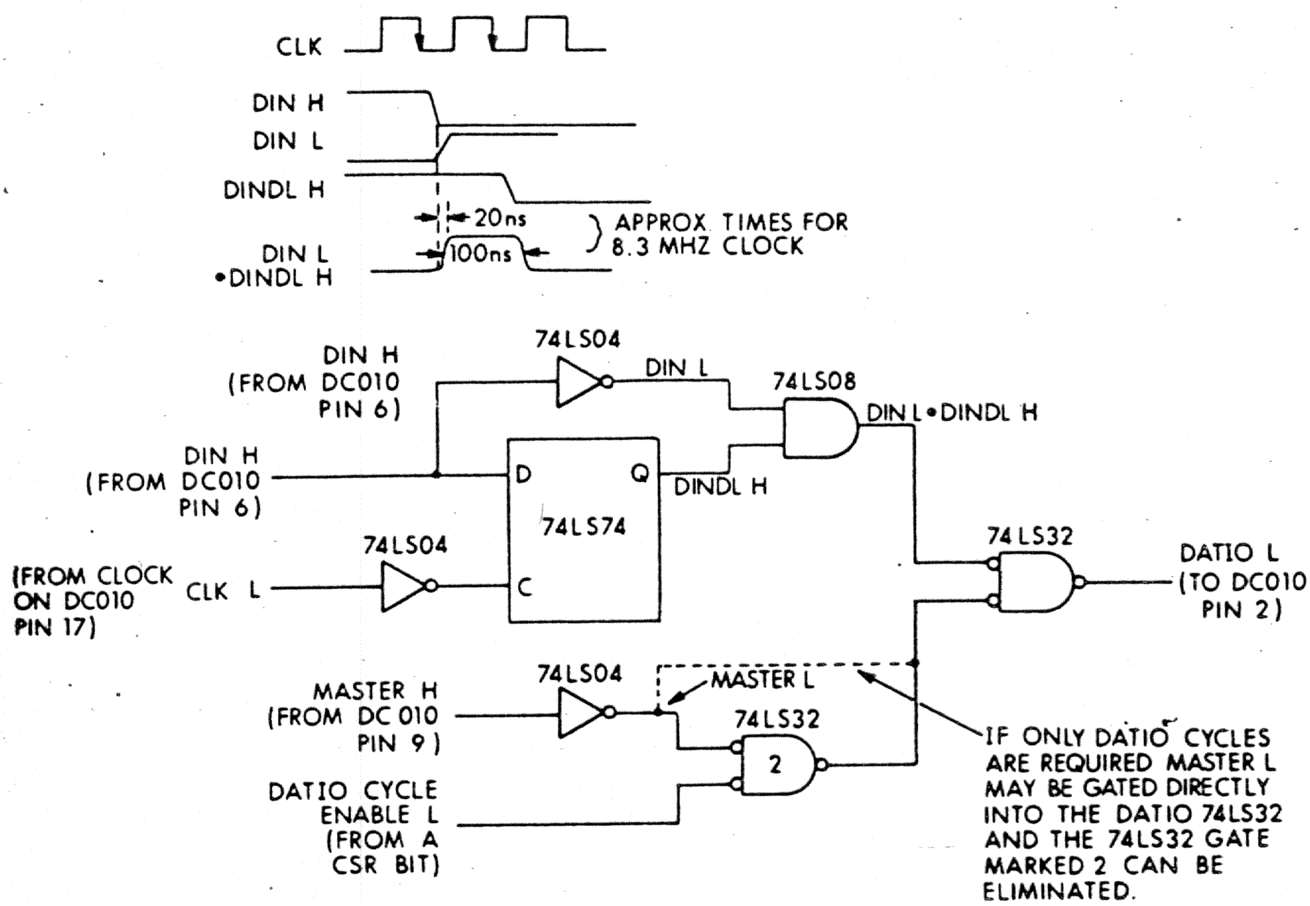


Figure 47 Additional Logic Required to Support DATIO Bus Cycles

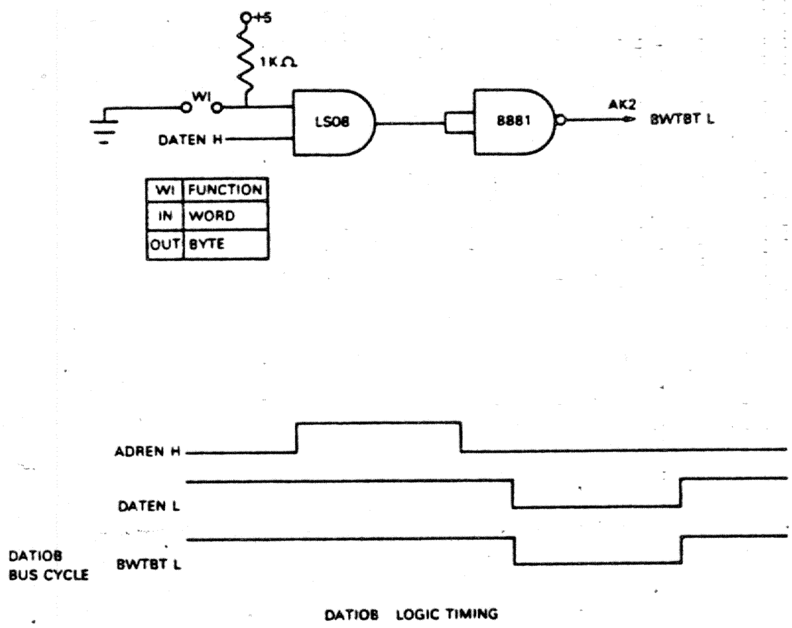


Figure 48 DATIOB Logic Timing

TIME DELAYS FOR BUS DMA REQUEST

Time delay to recapture the LSI-11 Bus as a function of the RC Values tied to pin 14 (TMOUT H). (NOTE: All times "Burst" Mode-No Refresh.)

1. R = 1K ± 5%
   C = 0

   Time delay from falling edge of MASTER H to rising edge of MASTER H with CNT 4 H pin high ≅ 820 nsec.

2. R = 1K ± 5%
   C = 1000 pf ± 5%

   Delay as described above ≅ 1.2 usec.

3. R = 1K ± 5%
   C = 6000 pf ± 5%

   Delay as described above ≅ 2.3 usec.

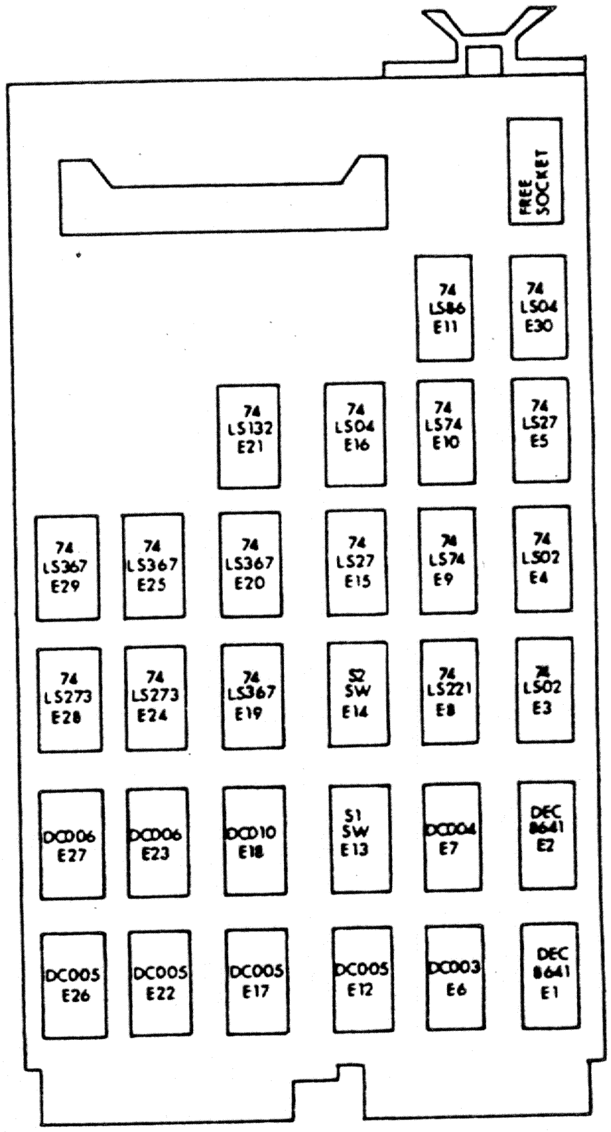


Figure 49 IC Layout Diagram for DMA Application Board

```
                                          .ABS              ;ASSEMBLE ABSOLUTE FOR ODT LOADING PURPOSES

       000220                             .=220             ;VECTOR SPACE
000220 001054                             TIMOUT            ;TIME OUT ERROR NEW PC
000222 000200                             ^B10000000        ;INTERRUPT INHIBIT FOR PS
000224 001066                             XFERDN            ;TRANSFER COMPLETE (XFER DONE) NEW PC
000226 000200                             ^B10000000        ;INTERRUPT INHIBIT FOR PS

       001000                             .=1000            ;MAINLINE ROUTINE
001000 012706 001000              START:  MOV     #START,SP         ;INIT STACK POINTER BELOW PROGRAM SPACE
001004 106427 000000                      MTPS    #0                ;ENABLE THE INTERRUPT SYSTEM
001010 012737 001104 177400               MOV     #BUF,@#177400     ;INIT THE CURRENT ADDRESS REG IN DMA
001016 013737 001100 177402               MOV     @#XFRNO,@#177402          ;INIT THE WORD COUNTER REGISTER

                                          ;GET DATA FROM THE LOCATION 'DATA' TO USE IN BLOCK XFER VIA DMA
001024 013737 001102 177406               MOV     @#DATA,@#177406 ;PUT 'DATA' IN OUTPUT REG, DUAL PORTED

                                          ;ENABLE THE DMA OPERATION REGISTER
001032 012737 040140 177404               MOV     #^B0100000001100000,@#177404
001040 052737 000400 177404               BIS     #^B0000000100000000,@#177404     ;SET REQUEST FLAG VIA DIAGNOSTIC

001046 000001                             WAIT    ;UNTIL INTERRUPT BY SOMEONE
001050 000167 177724                      JMP     START   ;LETS DO IT AGAIN!


                                                  ;SERVICE ROUTINE FOR TIME OUT ERROR FROM DMA MODULE
001054 042737 040000 177404       TIMOUT: BIC #^B0100000000000000,@#177404          ;CLEAR TIME OUT FLAG
001062 000000                             HALT
001064 000002                             RTI               ;CONTINUE ON A PROCEED FROM ODT
                                                            ;SERVICE ROUTINE FOR DATA BLOCK XFER COMPLETE
001066 042737 000200 177404               XFERDN: BIC #^B0000000010000000,@#177404          ;CLEAR DONE FLAG
001074 000000                             HALT
001076 000002                             RTI               ;CONTINUE ON A PROCEED FROM ODT

                                  ;CONSTANTS FOR THE PROGRAM
001100 177770                     XFRNO:  -10     ;AT ASSEMBLY DEFAULT TO 8 DECIMAL TRANSFERS
001102 123456                     DATA:   123456            ;AT ASSEMBLY DEFAULT DATA PATTERN FOR XFER
001104                            BUF:                      ;REST OF MEMORY AVAILABLE DEFAULT FOR BUFER

       001000                             .END    START
```

Figure 50   Test Program Used with DMA Application Board

HARDWARE FOR CHIPKITS

Two of the CHIPKITS, the DCK11-AC Program Control and the DCK11-AD DMA, are each supplied with an appropriate cable and module as described below. DIGITAL also makes a large variety of compatible hardware, including other modules and cables, connectors, mounting accessories, system enclosures, and cabinets, that you can use to complete your system. This hardware is described in the following DIGITAL publications:

- The DIRECT SALES CATALOG, presenting many items that you order directly from DIGITAL
- The CHIPKIT BROCHURE

To obtain these publications, or for more detailed information on these and other Accessories and Supplies Group products, write today:

DIGITAL EQUIPMENT CORPORATION
Circulation Dept. RQ/W83
460 Amherst Street
Nashua, NH 03063

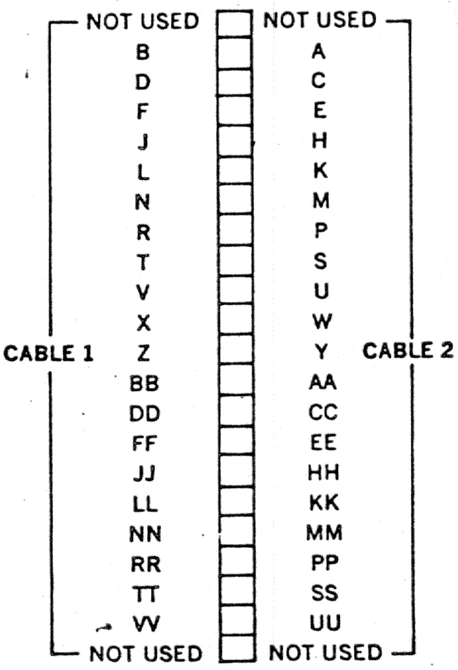
Cable BC07D-10

Ribbon Cable Assembly BC07D-10 is fabricated from two 20-conductor ribbon cables and a 40-pin female connector; the two ribbon cables each comprise twenty 22 AWG conductors which are cemented side-by-side. The ribbon cables are joined approximately every 10 inches with electrical tape. The conductors are terminated at one end by the 40-pin connetor and are unterminated at the other end.

SPECIFICATIONS

Conductors	
Number of conductors:	40
Gauge:	22 AWG, stranded (7/30)
Material:	Copper, tinned
Insulation:	PVC
Characteristic impedance:	76.5 ohms
DC resistance/foot:	0.0166 ohm
Capacitance/foot:	29.27 picofarads
Inductance/foot:	0.149 μ henries
UL style number:	1061
Cable	
Width:	1.1 inch (nominal)
Thickness:	0.102 inch (nominal)
Standard length:	10 feet ($\pm$3 inches)
UL style number:	2476
Connector	
Type:	H856
Mates with:	H854

Cable Assembly BC07D
Connector (H856) Pin Layout Diagram
(shown mating-side up)



40-Conductor Ribbon Cable Assembly BC07D
Conductor Insulation Color Code

Cable 1		Cable 2	
Pin	Color	Pin	Color
B	BLK	A	BLK
D	BRN	C	BRN
F	RED	E	RED
J	ORN	H	ORN
L	YEL	K	YEL
N	GRN	M	GRN
R	BLU	P	BLU
T	VIO	S	VIO
V	GRY	U	GRY
X	WHT	W	WHT
Z	BLK	Y	BLK
BB	BRN	AA	BRN
DD	RED	CC	RED
FF	ORN	EE	ORN
JJ	YEL	HH	YEL
LL	GRN	KK	GRN
NN	BLU	MM	BLU
RR	VIO	PP	VIO
TT	GRY	SS	GRY
VV	WHT	UU	WHT

Module W9512

The W9512 is a double height, extended length, single width module with handle (see Figure 50). This wire wrappable module enables a user to easily configure special interface logic for the LSI-11 computer system.

The W9512 module will accept a variety of IC package types and discrete components. The printed circuit on each board connects the appropriate edge connector pins to the V_{CC} plane on side 1 of the board and the ground plane (GND) on side 2. The remaining edge connector pins terminate to a double row of wire wrap pins for user designated functions. Each module also includes a 40-pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire wrap pins. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and to prevent shorting of wire wrap pins. The wire wrap pins and components are mounted on side 1 of each module. Rows of predrilled holes accept IC packages with pin spacings of 0.3 in. (.762 cm), 0.4 in. (1.01 cm) and 0.6 in. (1.52 cm). Universal area on the W9512 modules is the area which accepts IC packages with standard pin spacings. These areas have four rows of predrilled holes spaced at 0.3 in. (.762 cm), 0.4 (1.01 cm) and 0.6 in. (1.52 cm).

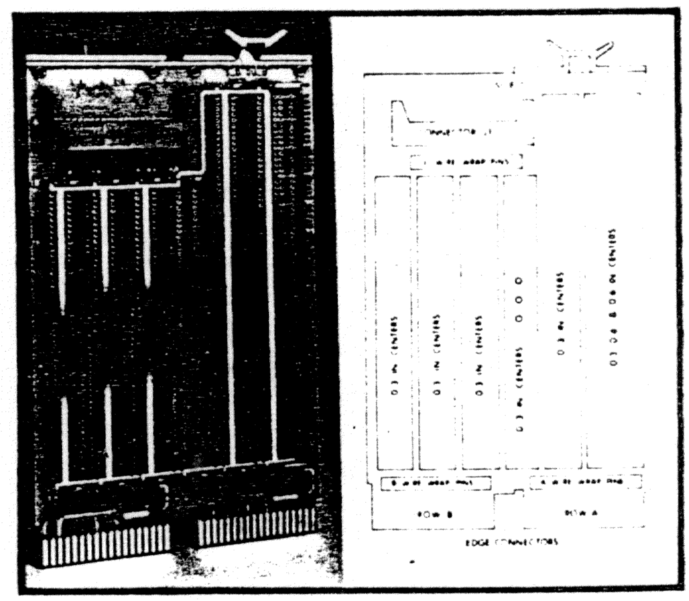


Figure 51 Physical Layout of the W9512 Module

APPENDIX
LSI-11 Bus Timings

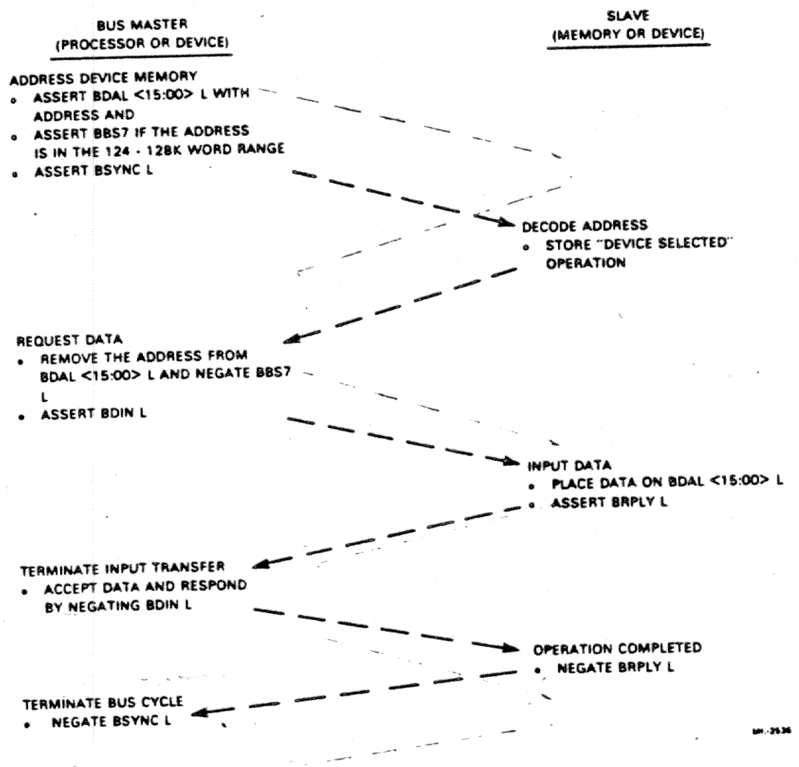
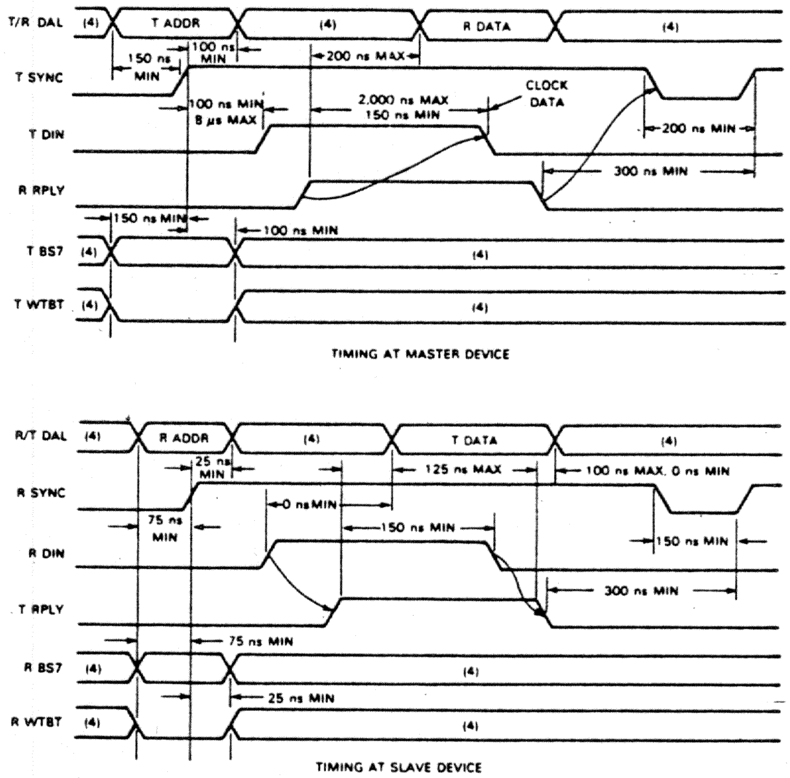


Figure 52 DATI Bus Cycle



NOTES:

1. TIMING SHOWN AT MASTER AND SLAVE DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS
2. SIGNAL NAME PREFIXES ARE DEFINED BELOW:
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT
3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX
4. DON'T CARE CONDITION

MK 2537

Figure 53 DATI Bus Cycle Timing

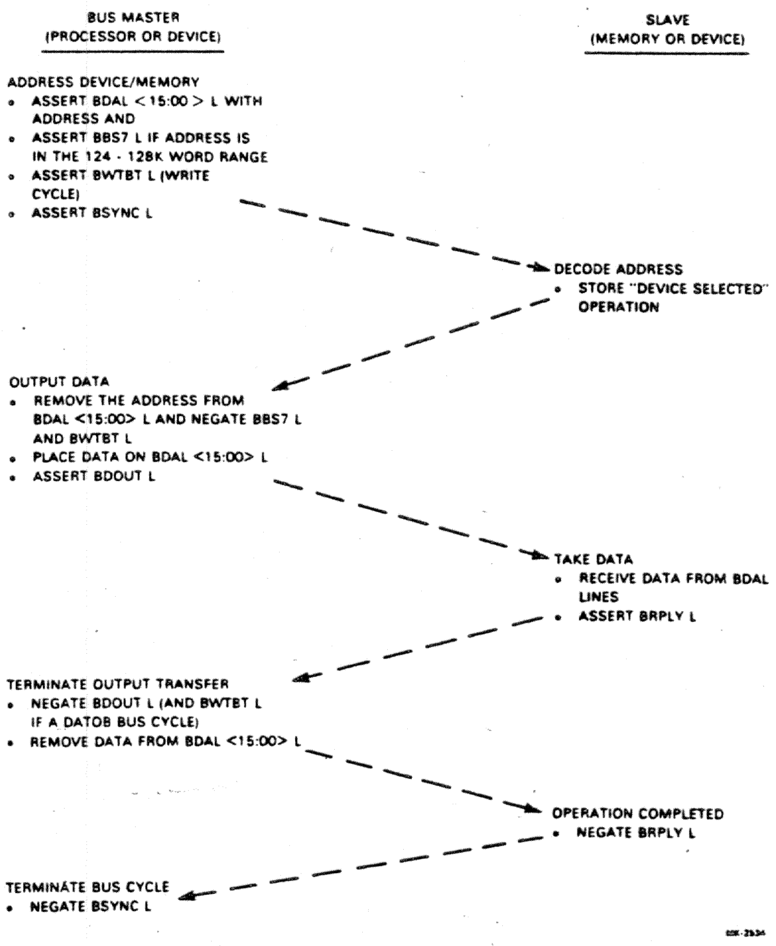
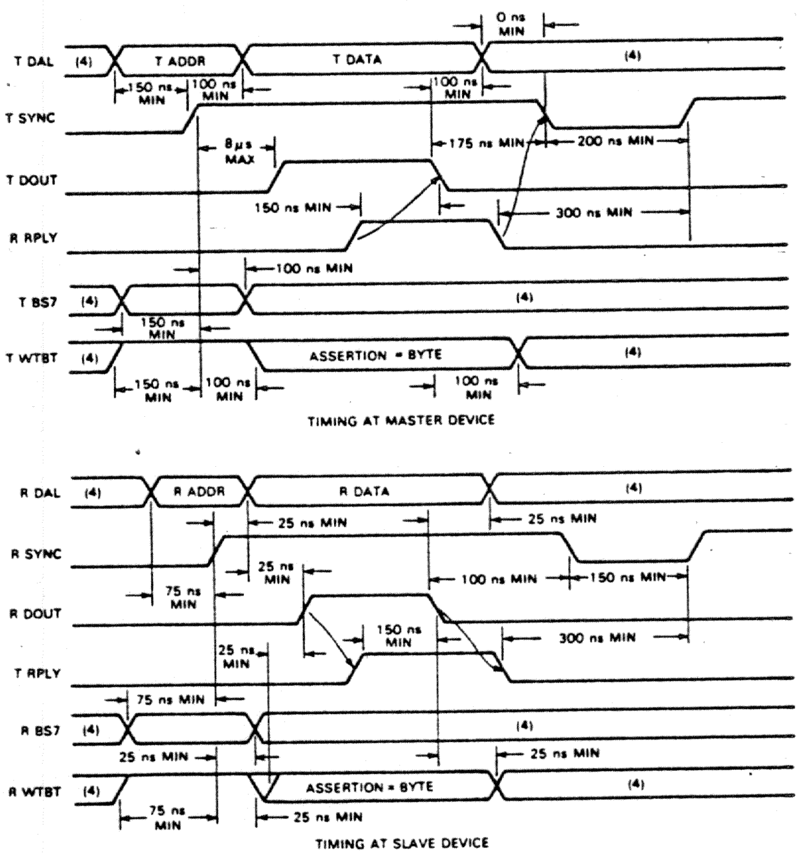


Figure 54 DATO or DATOB Bus Cycle



NOTES

1. TIMING SHOWN AT MASTER AND SLAVE DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS
2. SIGNAL NAME PREFIXES ARE DEFINED BELOW
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT
3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX
4. DON'T CARE CONDITION

Figure 55 DATO or DATOB Bus Cycle Timing

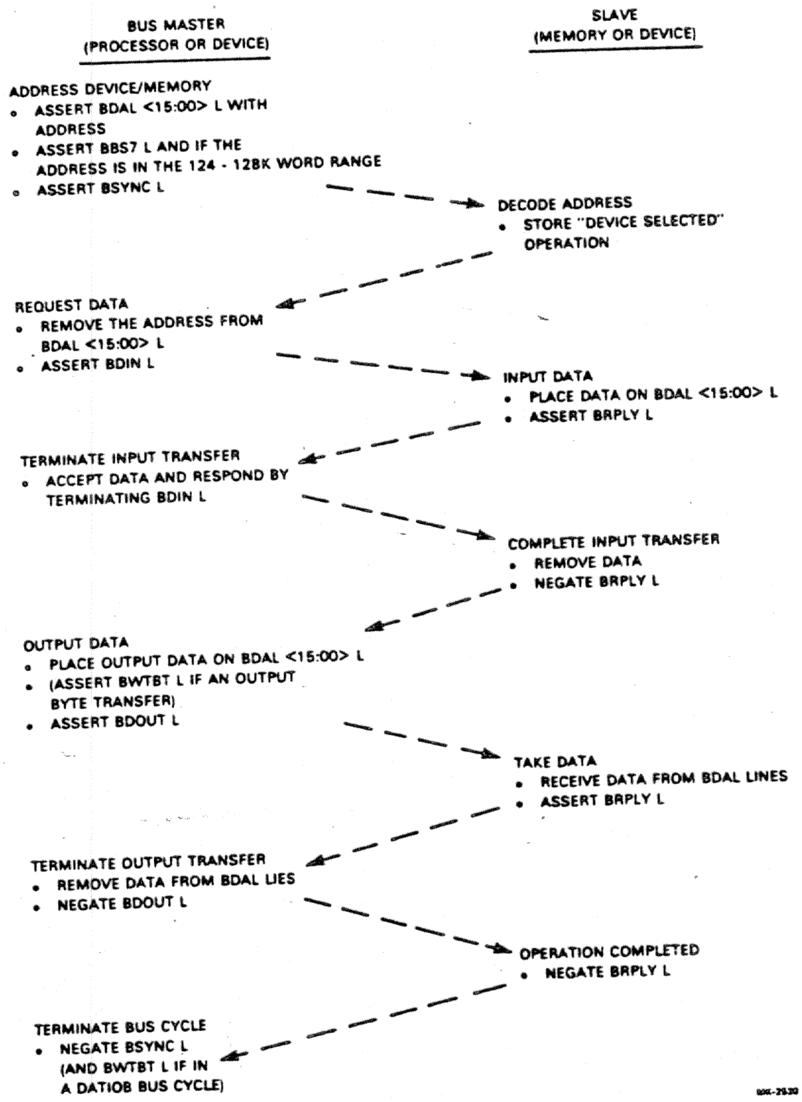
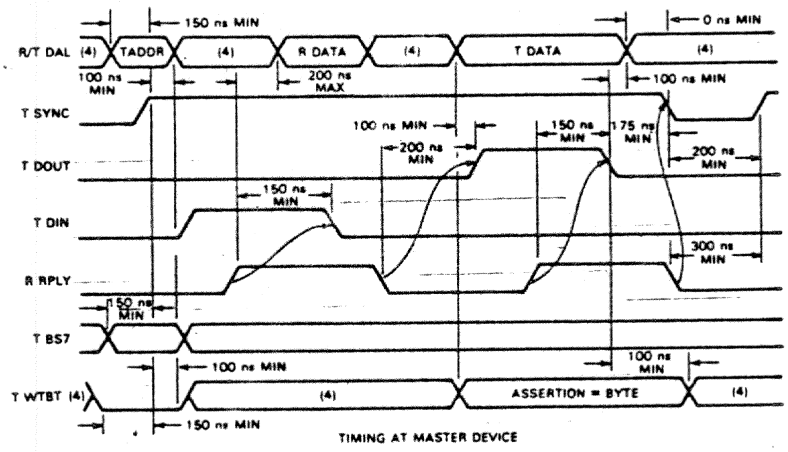


Figure 56 DATIO or DATOB Bus Cycle



NOTES:

1. TIMING SHOWN AT REQUESTING DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS
2. SIGNAL NAME PREFIXES ARE DEFINED BELOW
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT
3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX.
4. DON'T CARE CONDITION

Figure 57 DATIO or DATOB Bus Cycle Timing

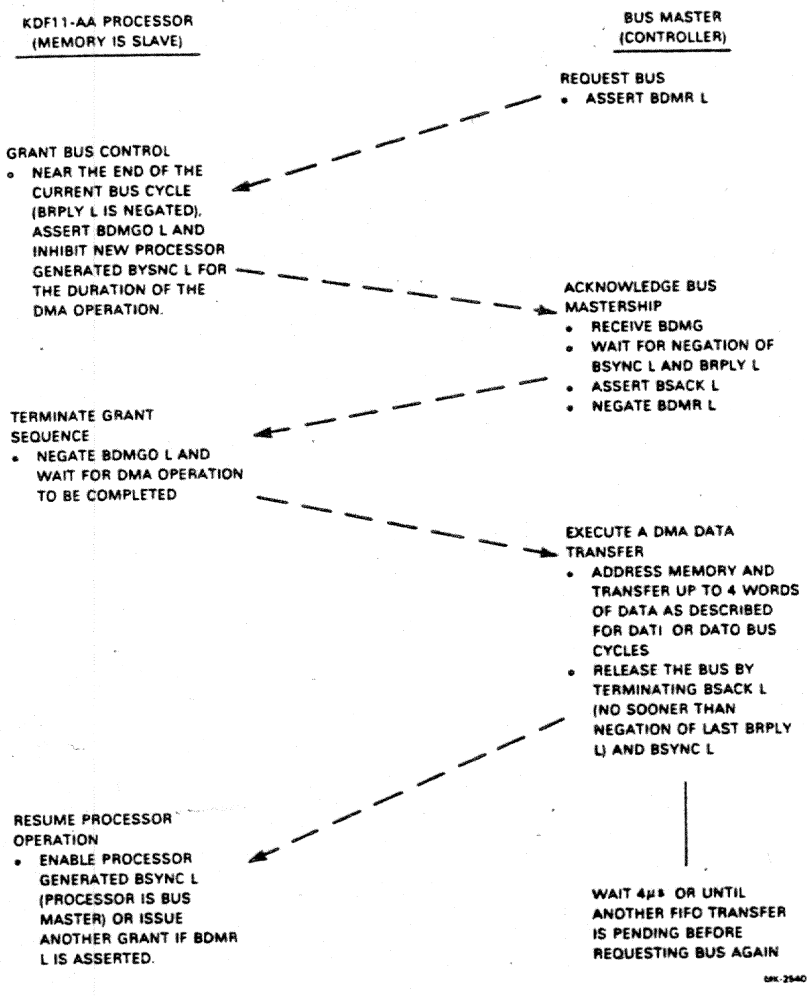
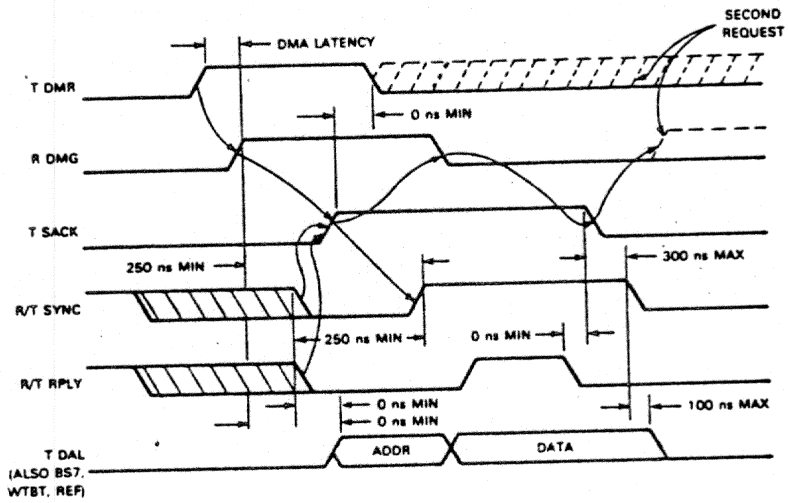


Figure 58 DMA Bus Cycle



NOTES:
1. TIMING SHOWN AT REQUESTING DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS.

2. SIGNAL NAME PREFIXES ARE DEFINED BELOW:
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT

3. BUS DRIVER OUPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX

MR 2941

Figure 59 DMA Bus Cycle Timing