

EK-VAXV3-HB-001

VAX
Maintenance
Handbook

VAX-11/750

1983 Edition

Prepared by Educational Services
of
Digital Equipment Corporation

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DECtape	Pre-compiled	Work Processor

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CMI, UNIBUS, AND MASSBUS

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TROUBLESHOOTING AIDS

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CHARTS AND MACROS



CHAPTER 1
INTRODUCTION

INTRODUCTION

This handbook is a summary of VAX-11/780 system performance information. It is intended to serve as a single source reference for RUTGERS field service, and for Engineering, Manufacturing, and Training personnel.

The material encompasses detailed information available in manuals and service manuals and in reference print sets. It contains tables, diagrams, and procedures, and updates VAX-11/780 usage to facilities with the VAX-11/780 system, its peripherals and accessories.

For further information, refer to the manuals VAX-11/780 and VAX-11/780 accessory library, and in tables included in this manual that list related hardware manuals.

Hard copy documents may be ordered through the nearest RUTGERS sales office, the Commodore and Supplies Group, including International Products Distributors, or directly from the following addresses.

Commodore and RPS:

Digital Equipment Corporation
440 Kennedy Blvd.
Bedford, MA 01531

Atlas Publishing and Circulation Division, Inc.
Customer Service Division

Digital peripherals:

Digital Equipment Corporation
100 Morris Blvd.
Bedford, MA 01531

Atlas Publishing and Circulation Division, RPS

Technical descriptions and service manuals are also available in microfiche. For information, or materials provided (including performance print sets and diagnostic teststand manuals)

Digital Equipment Corporation,
Micropublishing Systems, R0284
12 Maple Drive
Bedford, MA 01531

VAX-11/750 SYSTEM HARDWARE MANUALS

Title	Document Number
VAX-11/750 System Architecture and Technical Description	DA-DA111-10
VAX-11/750 Bus and Interface Technical Description	DE-DE111-10
VAX-11/750 Memory System Technical Description	DE-DE111-10
DE-10 KMS-10 Adapter Technical Description	KA-1011-10
DE-100 Terminal DE-100 Interface Terminal Description	KA-1011-10
DE-100 Floppy Disk Adapter and Terminal Description	KA-1011-10
VAX-11/750 ATIO Wave System Technical Description	DE-DE111-10
VAX Architecture Guide	DA-DA111-10
VAX Hardware Handbook	DA-DA111-10
VAX Software Handbook	DA-DA111-10
VAX System Kit, Expansion Guide	DA-DA111-10
VAX-11/750 Installation and Maintenance "User Manual"	DA-DA111-10
VAX-11/750 User's Guide	DA-DA111-10
VAX Hardware Handbook, VAX system	DA-DA111-10
VAX Diagnostic System Users Guide	DA-DA111-10
VAX-11/750 Diagnostic System Configuration Manual	DA-DA111-10
VAX-11/750 Diagnostic Kit Hardware Guide	DA-DA111-10
VAX-11/750 Data Acquisition Reference Manual	DA-DA111-10

*Available only on order form

VAX-11/750 SYSTEM HARDWARE MANUALS (CONT)

DATE	DESCRIPTION	Docu. No.
2072	Interchangeable Mechanical Manual	72-80758-TV
2072	Options User Guide	52-80758-10
2072	Options Installation Guide	22-80758-11
2072	Technical Change Notice	11-80758-01
2072	Original Design Guide	07-19400-09
2072-11/750	Psychometric Reference Manual	07-19400-09
2072-11/750	Software Reference Manual	07-19400-09
2072-11/750	Change Notice	72-70758-01
2072-11/750	Service Map	22-80758-12
2072-11/750	PC Multiauth	72-11758-01
2072-11/750	Keyboard Card Sheet	22-11758-01
2072	Installation Data Sheet	22-0267-10

VAX-11/750 PERIPHERAL MANUALS

KA10	Technical Manual	KA-21A10-1P
KA11	Technical Manual	KA-21A11-1P
KA12	Technical Manual	KA-21A12-1P
KA13	Technical Manual	KA-21A13-1P
KA14	Technical Manual	KA-21A14-1P
KA15	Technical Manual	KA-21A15-1P
KA16	Technical Manual	KA-21A16-1P
KA17	Technical Manual	KA-21A17-1P
KA18	Technical Manual	KA-21A18-1P
KA19	Technical Manual	KA-21A19-1P
KA20	Technical Manual	KA-21A20-1P
KA21	Technical Manual	KA-21A21-1P
KA22	Technical Manual	KA-21A22-1P
KA23	Technical Manual	KA-21A23-1P
KA24	Technical Manual	KA-21A24-1P
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KA30	Technical Manual	KA-21A30-1P
KA31	Technical Manual	KA-21A31-1P
KA32	Technical Manual	KA-21A32-1P
KA33	Technical Manual	KA-21A33-1P
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KA74	Technical Manual	KA-21A74-1P
KA75	Technical Manual	KA-21A75-1P
KA76	Technical Manual	KA-21A76-1P
KA77	Technical Manual	KA-21A77-1P
KA78	Technical Manual	KA-21A78-1P
KA79	Technical Manual	KA-21A79-1P
KA80	Technical Manual	KA-21A80-1P
KA81	Technical Manual	KA-21A81-1P
KA82	Technical Manual	KA-21A82-1P
KA83	Technical Manual	KA-21A83-1P
KA84	Technical Manual	KA-21A84-1P
KA85	Technical Manual	KA-21A85-1P
KA86	Technical Manual	KA-21A86-1P
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KA96	Technical Manual	KA-21A96-1P
KA97	Technical Manual	KA-21A97-1P
KA98	Technical Manual	KA-21A98-1P
KA99	Technical Manual	KA-21A99-1P
KA00	Technical Manual	KA-21A00-1P

VAX-11/750 PERIPHERAL MANUALS (CONT)

Model	Document Number
DDP-11 Technical Subsystem Operator Reference Card	KK-18010-11
AK01/87 Technical Description Manual	KK-18117-87
AK05/87 Operator Manual	KK-18117-87
TK01/87 Disk Drive Service Manual	DS-89011-87
AK01/87 FDS Operating/Loading Manual	KK-18118-87
AK01/87 Database Core Manual	KK-18119-87
AK01 Disk Drive I/O	KK-18117-87
AK01 Technical Description Manual	KK-18117-87
AK01 Controlled I/O	KK-18117-87
AK01 Technical Manual	KK-18117-87
RP01 Disk Drive Software Manual	DS-89011-87
RP01 Disk Drive I/O	DS-89011-87
RP01/87 User's Guide	DS-89011-87
RP01/87 Disk Subsystem Service Manual	DS-89011-87
RP02/87 Database Equipment Core	DS-89011-87
RP02/87 I/O Subsystem	DS-89011-87
RP01 Subsystem Technical Manual	DS-89011-87
RP01 Subsystem Operator Guide	KK-18117-87
RP01 Subsystem Database Equipment Core	DS-89011-87
RP01 Pocket Service Guide	KK-18117-87
RP01-87 Magnetic Tape Subsystem I/O	KK-18118-87
RP01-87 Magnetic Tape Subsystem	KK-18118-87
RP01-87 Magnetic Tape Subsystem I/O	DS-89011-87
RP01-87 Magnetic Tape Subsystem I/O	DS-89011-87

VAX-11/750 PERIPHERAL MANUALS (CONT)

Title	Document Number
RM75 Disk Drive Service Manual	75-05987-02
RM75 Disk Subsystem Service Guide	11-00000-01
RM75 Disk Drive LRU	07-00000-10
RM75 DR Workbooks	06-00000-08
RM77 Magnetic Tape Transport V1	06-01017-04
RM77 Magnetic Transport Manual V2	06-010-0100
RM77 Installation Update	06-00000-01
RM77 Magnetic Transport Model's Guide	01-00000-00
TR77 Magnetic Tape Assembly	11-00000-01
TR77 Magnetic Tape Transport TPO	06-00000-05
TR770000 Magnetic Transport Equipment Data	74-00000-02
TR770000 DR Workbooks	07-00000-00
RM80 Disk Drive Technical Association	06-00000-00
RM80 Disk Drive Service Manual	06-00000-01
RM80 Disk Drive Service Guide	06-00000-00
RM80 Disk Drive Service Guide	06-00000-01
RM80 Disk Drive Customer Data Package	06-00000-00
RM80 Disk Drive TPO	06-00000-00
TR800000 SYMMETRY Magnetic Disk Manual	06-00000-00
TR800000 SYMMETRY Magnetic Disk	06-00000-00
TR80 DR0 Magnetic LRU	01-00000-01

VAX-11/760 MAINTENANCE PHILOSOPHY

VAX-11/760 system maintenance consists of the repair or replacement of modules, components, or complete hardware units, depending on the type of hardware under test and the level of testing that applies to each unit.

General test methods and procedures for replacing units apply alike to the diagnostic CPU module or device and to diagnostic testing. If replacing the unit doesn't solve the problem, the module must be replaced.

Preventive maintenance for internal CPU modules such as the Diagnostic Processor (DPR) modules (DPR) and the Diagnostic Processor (DPR) consists of regular inspections of the processor diagnostic addresses & failures.

The DPR module (DPR) and the Diagnostic Processor (DPR) must be replaced if the diagnostic addresses indicate a failure. Attached external test units usually follow strict replacement rules (DPR) and are replaced according to their respective maintenance procedures.

The following table provides an overview of the preventive actions prescribed for various units of the VAX-11/760 system (Table).

VAX-11/750 MAINTENANCE PHILOSOPHY (CONT)

GPU MODULES

Module Name (Hex)	Module Number (Hex)	Level of Replacement		Workaround
		Component/ Gate Array	Software Module	
Cache (400)	12802 141	Primary (inter-processor handling)	Secondary	Replace module if the unit cannot do test 200 the problem.
Memory Array (400)	18704 141	Primary	Secondary	Replace module if the gate arrays do not fix the problem.
Memory Array (400)	18704 141	Primary	Secondary	Fixed by gunting and, if necessary, RCM, RGF, or Test 6.
GPU Control (400)	18705 141		Primary	As diagnostic to test this module.

NOTE:

A user to determine the condition of the GPU on his own, could check as follows: the 18705 starts diagnostic module (DM) and go in place.

```

CPU 100
RAM 110
DMA 200 3
.
.
.
DMA 1000
    
```

Performing this test produced a series of address pointers.

10 DMA = 1000 (last).
The CPU is ok.

The GPU is also shown as the 18706 maintenance has results (M) to customers.

VAX-11/750 MAINTENANCE PHILOSOPHY (CONT)

CPU OPTIONS

Part # (MFR#)	Model # (MFR#)	Component Name Array	Level of Support	Replace Module	Notes/Comments
80000 CPU 8000	13801 16		Primary		Requires Van Cleft Key used to run with distributed facility or remotely. Test by running BSAFE, BAF
81000 CPU 8100	13801 17		Primary		Tested by running TRK601000.
820000 Processor 8200	18700 17, 191		Primary		Do not flush VMA and MVA.
82000 CPU 8200	18700 17, 191		Primary		Do not flush MVA and MVA. Do not flush for new MVA allocation. CPU location SR with training for first and second MVA and MAF800 (option 2100).
CHI/Key 83000 8300		Primary Diagnose (Diagnose) & Testing	Secondary		Microcode device, the CPU controls memory re- location when changing, data buffering, set and restore and scanning sub- system. Test by running TRK601000.
840 10 MVA 8400	10001 110				840 10 and 84000 are memory array modules
840 20 MVA 8400	10000 110				840 20 is 16,384000 per memory array module
8500 Control 8500			Replace module of drive unit		850 000, 850000 B and 10000000 MVA, etc.

VAX-11/750 MAINTENANCE PHILOSOPHY (CONT)

THE REMOTE DIAGNOSTIC FACILITY

The customer is required to provide a coin-operated telephone line and computer for DDD's Remote Diagnostic Center (RDC) service facility.

The DDC option will be installed in all VAX-11/750 systems during installation to provide the ability to the customer during the warranty period. If all the calls in the backplane are all accounted with the assistance of experienced consultants.

CONTACTING THE DDC

Basic steps:

1. The customer calls the DDC toll free number when there is a problem.

1-800-426-6570	For DDC consultation (24 hr. access)
1-800-426-6842	For Field Service assistance
1-800-426-1884	U.S. F.A. February 1982 employees only

The following will apply to DDC's (remote diagnosis):

2. The DDC performs remote computer fault isolation and the customer the following options to the branch office.
3. The branch office sends a Field Service Engineer with parts to correct the problem.

For CPU Problems:

1. The engineer takes the CPU option and CPU test in the office.
2. The engineer runs the microdiagnostic cassette tapes


For customer with non-PC computers, the CPU test is installed in the VAX-11/750 backplane and is removed when work is complete.

The CPU test is a fault simulator used to specifically detect and analyze a string of chips coverage of the gate circuit.

3. The engineer performs comparison tape replacement (CTR) by replacing the individual gate arrays.

When the customer reports the fault on CPU test or other CPU-related failures, the failure module or assembly is replaced.

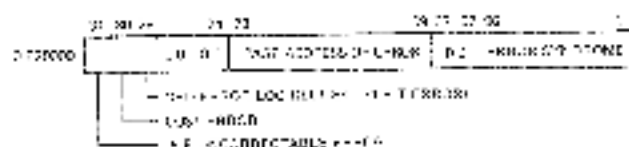
REMARKS: The DDC should be worked with the DDC re-writer also to provide a case history of failures for the VAX-11/750.



CHAPTER 2
SYSTEM REGISTERS

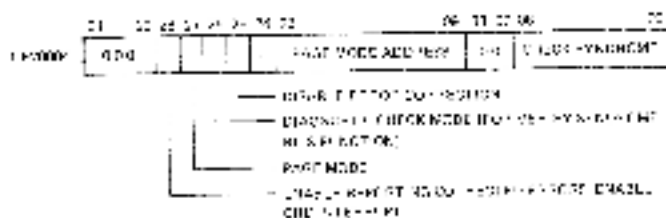
CMD (MS750) REGISTERS

CONTROL/STATUS REGISTER 0 (CSR 0)



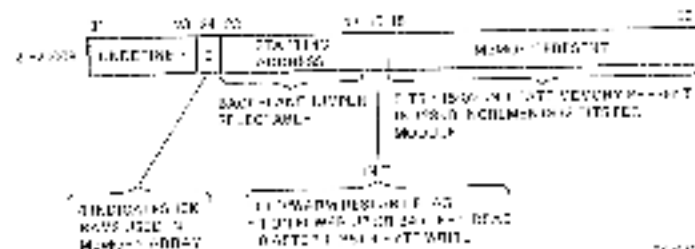
100

CONTROL/STATUS REGISTER 1 (CSR 1)



100

CONTROL/STATUS REGISTER 2 (CSR 2)



100

INTERNAL PROCESSOR REGISTER (IPR) SUMMARY

Address	Mnemonic	Depth	Name
87	ESP		Term. Error Pointer
88	EBP		Base/Frame Pointer
89	ESP		Supervisor Stack Pointer
90	ESP		User Stack Pointer
91	ESP		Interrupts Stack Pointer
92-97	Reserved		
98	PRR0		PR Task Register
99	PRR1		PR Length Register
9A	PRR2		PR Task Register
9B	PRR3		PR Length Register
9C	PRR4		System Base Register
9D-9E	Reserved		System Length Register
10	PRR5		Priority Control - Task Base
11	PRR6		System Control - Task Base
12	PRR7		Task/PR Priority Base
13	PRR8		PR Task Register
14	PRR9	R/O	Terminal Interrupt Request Register
15	PRR10		Software Interrupt Request Register
16	Reserved		
17	CR12PR	R/O	CR Task Register
18	PRR11		Terminal Error Control/Status
19	PRR12	R/O	PRR Task and Control Register
1A	PRR13	R/O	Terminal Count Register
1B	PRR14		Time of Day Register
1C	PRR15		Console Storage Controller Status
1D	PRR16	R/O	Console Storage Controller Data
1E	PRR17		Console Storage Controller Status
1F	PRR18	R/O	Console Storage Controller Data

*Registers are read/write unless otherwise specified.
 R/O means read-only; W/O means write only or neither.
 The specified suffix(es):

INTERNAL PROCESSOR REGISTER (IPR) SUMMARY (CONT)

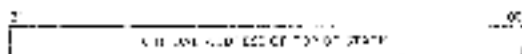
Address	Hexonic	Type*	Name
20	IRCS		Console Receive Control/Status
21	IRTS	R/O	Console Receive Data Buffer
22	LRCS		Console Receive Control/Status
23	LRDS	R/O	Console Receive Data Buffer
24	TRTS		Translation Buffer Disable Register
25	CDLR		Cache Disable Register
26	NCZSR		Cache Check Error Summary Register
27	CAER		Cache Error Register
28	SCCS	R/O	Serialized Control/Status
29-36	Reserved to RISCY	R/O	Initialize RISCY
38	MMI		Memory Management Initial
39	TRTS	R/O	Translation Buffer Data (All)
4A	YPTS	R/O	Translation Buffer Data (Single)
4B	TRTS		Translation Buffer Data
7C	Reserved		
7D	MMI		Switchboard Monitor Register - ¹¹ Hex 7D04
7E	SDI	R/O	System Identification
3F	MMI	R/O	From Translation Buffer for TR III

*R/O means read-only, W/O means write-only, and
R/W means read-write, N/A means Not Applicable to RISCY
(the specified hex-hexic):

INTERNAL PROCESSOR REGISTERS

PC 1000

PC 000 007 MULTI-STAGE POINTER
 PC 001 007 EXCLUSIVE-STAGE POINTER
 PC 002 007 SUPERVISOR STACK POINTER
 PC 003 007 USER STACK POINTER
 PC 004 007 INITIATOR STACK POINTER

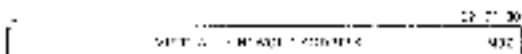


PC 005 007

PC 005 REGISTER
 RESERVED AND NOT IMPLEMENTED

PC 006 007

PC 006 REGISTER
 RESERVED AND NOT IMPLEMENTED



PC 007 007

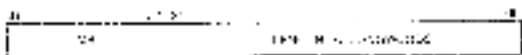
PC 007 REGISTER
 RESERVED AND NOT IMPLEMENTED

PC 008 007

PC 008 REGISTER
 RESERVED AND NOT IMPLEMENTED

PC 009 007

PC 009 REGISTER
 RESERVED AND NOT IMPLEMENTED



INTERNAL PROCESSOR REGISTERS (CONT)

HEX NAME

IPF #10 PCB8

PROCESS CONTROL BLOCK BASE

HEXIDE000000 - ALL IF 000000

000000

000000

HEXIDE000000 - ALL IF 000000

HEXIDE

IPF #11 PCB9

SYSTEM CONTROL BLOCK BASE

HEXIDE000000 - ALL IF 000000

000000

000000

HEXIDE000000 - ALL IF 000000

HEXIDE

IPF #12 PCB1

INTERLUPT PRIORITY LEVEL REGISTER

00

000000

HEXIDE000000 - ALL IF 000000

HEXIDE000000

IPF #13 PCB5

SET LEVEL REGISTER

HEXIDE000000 - ALL IF 000000

00

000000

HEXIDE000000 - ALL IF 000000

HEXIDE000000

IPF #14 PCB6

SYSTEM BASE REGISTER

HEXIDE000000 - ALL IF 000000

000000

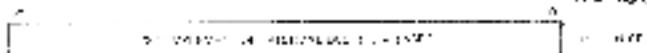
000000

HEXIDE000000 - ALL IF 000000

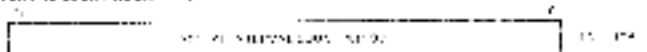
HEXIDE

INTERNAL PROCESSOR REGISTERS (CONT)

INTERNAL CPU INTERNAL COUNT REGISTER (COUNT)



INTERNAL CPU INTERNAL REGISTER (REGISTER)



INTERNAL CPU INTERNAL CLOCK CONTROL AND STATUS REGISTER (REGISTER)



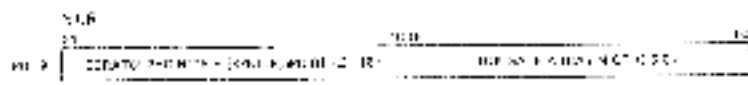
INTERNAL CPU INTERNAL CLOCK CONTROL AND STATUS REGISTER (REGISTER)



INTERNAL CPU INTERNAL REGISTER (REGISTER)

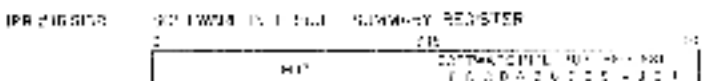
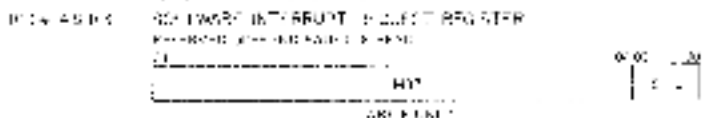
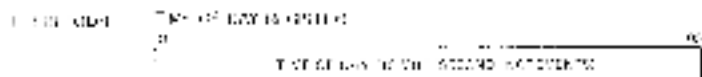
INTERNAL PROCESSOR REGISTERS (CONT)

INTERNAL REGISTER HARDWARE USAGE



100-11

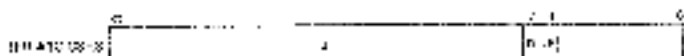
INTERNAL PROCESSOR REGISTERS (CONT)



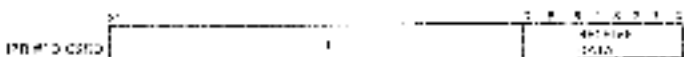
0-00

0-00

CONSOLE STORAGE TRANSMIT STATUS



CONSOLE STORAGE RECEIVE STATUS



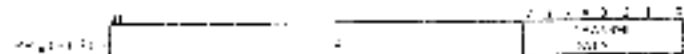
CONSOLE STORAGE

CONSOLE STORAGE TRANSMIT STATUS



TOTAL

CONSOLE STORAGE TRANSMIT DATA



CONSOLE STORAGE

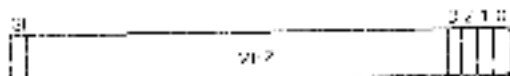
0-00

INTERNAL PROCESSOR REGISTERS (CONT)

TABLE 1. INTERNAL REGISTER GROUP DISABLE GROUP 0
 (SEE CODE GROUP CONDITIONS)

PR 421 REGISTER 32-BIT ADDRESS BUFFER GROUP DISABLE REGISTER PR 421

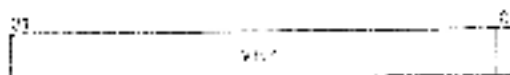
THIS REGISTER CONTAINS THE FOLLOWING:



C = DATA BUFFER RELOAD VIZ
 E = ERROR RELOAD VIZ
 G = REPLACE GROUP 0
 1 = REPLACE GROUP 1
 0 = GROUP 0 GROUP 1
 1 = MEM 0 GROUP 1
 0 = MEM 0 GROUP 0

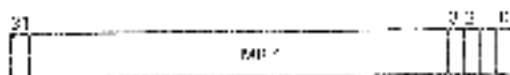
PR 426 REGISTER GROUP DISABLE FLIP-FLOP PR 426

1 = GROUP IS DISABLED



PR 427 REGISTER CACHE ERROR REGISTER PR 427

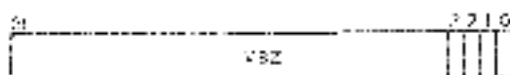
THIS REGISTER CONTAINS THE FOLLOWING:



C = TAG PARITY ERROR
 E = DATA PARITY ERROR
 G = LOST TAG
 C = LOST

PR 428 REGISTER HARDWARE CHECK ERROR SUMMARY REGISTER PR 428

THIS REGISTER INDICATES THAT THE ADDRESS AT WHICH A TUPLE IS
 CURRENTLY BEING ERROR REGISTER, WRITING A 1 TO THE
 INDICATES ITS GROUP PARITY REGISTER



C = ERROR, REFER TO BUS ERROR REGISTER
 E = TAG PARITY ERROR
 G = LOST TAG
 1 = LOST TAG
 0 = LOST TAG

7-1-1988

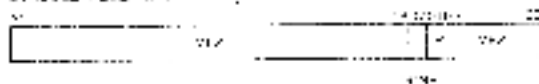
INTERNAL PROCESSOR REGISTERS (CONT)

PR 100 - SPACE ACCELERATOR CONTROL/STATUS

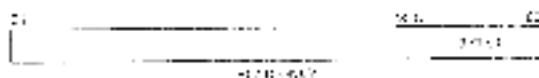


PR 101 -

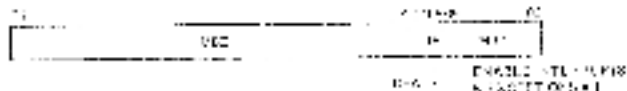
PR 101 - CONSOLE RECEIVE CONTROL/STATUS



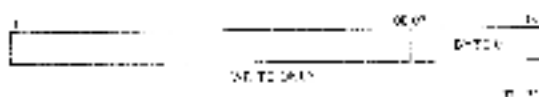
PR 102 - LOCAL RECEIVE DATA BUFFER



PR 103 - SERIAL TRANSMIT CONTROL/STATUS

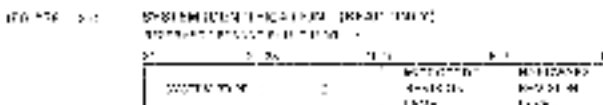
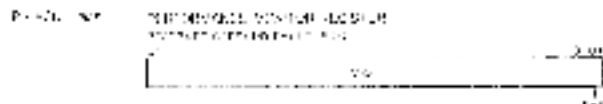
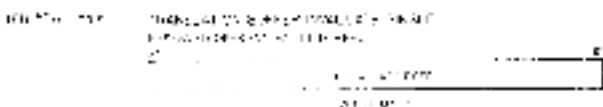
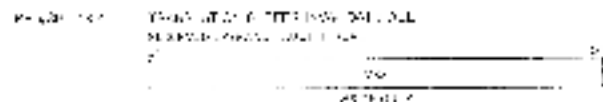
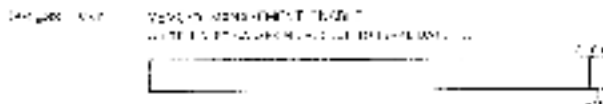


PR 104 - SERIAL TRANSMIT DATA BUFFER



INTERNAL PROCESSOR REGISTERS (CONT)

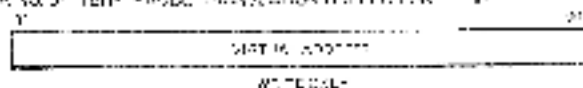
00000000



BIT	NAME	DESCRIPTION	INITIAL VALUE
31	SYSTEM OVERFLOW	System overflow flag	0
30	SYSTEM OVERFLOW	System overflow flag	0
29	SYSTEM OVERFLOW	System overflow flag	0
28	SYSTEM OVERFLOW	System overflow flag	0
27	SYSTEM OVERFLOW	System overflow flag	0
26	SYSTEM OVERFLOW	System overflow flag	0
25	SYSTEM OVERFLOW	System overflow flag	0
24	SYSTEM OVERFLOW	System overflow flag	0
23	SYSTEM OVERFLOW	System overflow flag	0
22	SYSTEM OVERFLOW	System overflow flag	0
21	SYSTEM OVERFLOW	System overflow flag	0
20	SYSTEM OVERFLOW	System overflow flag	0
19	SYSTEM OVERFLOW	System overflow flag	0
18	SYSTEM OVERFLOW	System overflow flag	0
17	SYSTEM OVERFLOW	System overflow flag	0
16	SYSTEM OVERFLOW	System overflow flag	0
15	SYSTEM OVERFLOW	System overflow flag	0
14	SYSTEM OVERFLOW	System overflow flag	0
13	SYSTEM OVERFLOW	System overflow flag	0
12	SYSTEM OVERFLOW	System overflow flag	0
11	SYSTEM OVERFLOW	System overflow flag	0
10	SYSTEM OVERFLOW	System overflow flag	0
9	SYSTEM OVERFLOW	System overflow flag	0
8	SYSTEM OVERFLOW	System overflow flag	0
7	SYSTEM OVERFLOW	System overflow flag	0
6	SYSTEM OVERFLOW	System overflow flag	0
5	SYSTEM OVERFLOW	System overflow flag	0
4	SYSTEM OVERFLOW	System overflow flag	0
3	SYSTEM OVERFLOW	System overflow flag	0
2	SYSTEM OVERFLOW	System overflow flag	0
1	SYSTEM OVERFLOW	System overflow flag	0
0	SYSTEM OVERFLOW	System overflow flag	0

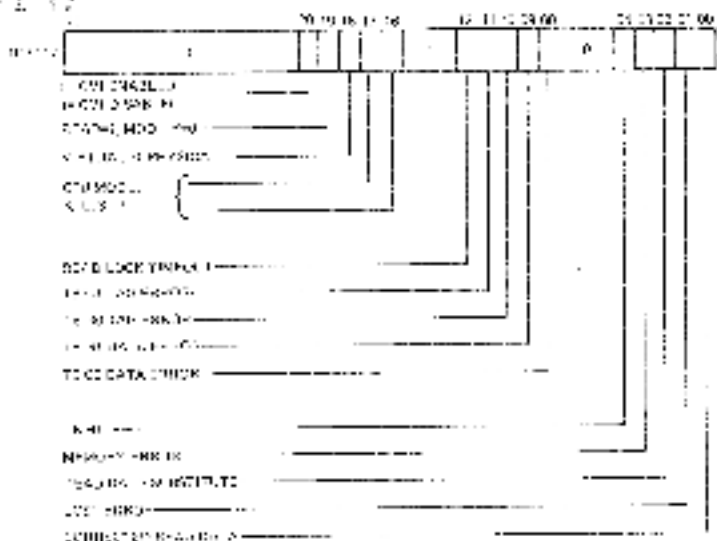
INTERNAL PROCESSOR REGISTERS (CONT)

REG 03 - TEMP. PROG. TRANSLATION BUFFER FOR TRAIT



15-16

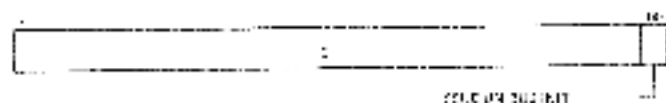
R/E 17



MODE LOCK PROCESSOR REGISTER

15-16

REG 04 - RESET INITIALIZE NUMBER



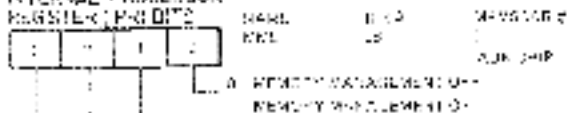
16-RESET PROGRAM REGISTER

15-16

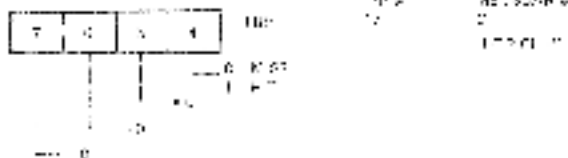
INTERNAL PROCESSOR REGISTERS (CONT)

YIP REGISTER BIT DEFINITIONS

INTERNAL PROCESSOR REGISTER CONTROL BITS



0: 00000000
 1: 00000001
 2: 00000010
 3: 00000011



0: 00000000
 1: 00000001
 2: 00000010
 3: 00000011



0: 00000000
 1: 00000001
 2: 00000010
 3: 00000011

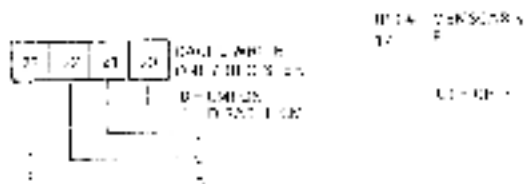
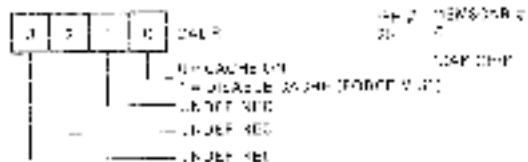
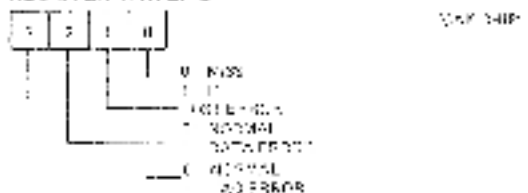


0: 00000000
 1: 00000001
 2: 00000010
 3: 00000011

INTERNAL PROCESSOR REGISTERS (CONT)

CACHE REGISTER BIT FIELDS

INTERNAL PROCESSOR REGISTER (INHIBITS) bit MP bit 4 bit 0 bit 1 bit 2



10-20-1

INTERNAL PROCESSOR REGISTERS (CONT)

TE AND CACHE CONTROL/STATUS REGISTER BIT FIELDS

INTERNAL PROCESSOR REGISTER (PRIBITS)

Bit	NAME	IP14	IP14 AREA
1	MEMERR	25	0
2			0
3			0
4			0

- 1 MEMERR = 0: NO MEMORY ERROR
- 1 MEMERR = 1: MEMORY ERROR
- 2 NORMAL
- 2 UNCORRECTED UNUSABLE DATA
- 3 NORMAL
- 3 ERROR (ERR) NOT A CORRECTION ERROR
- 4 NORMAL
- 4 BUS ERROR (ERR) NOT A CORRECTION ERROR

INTERNAL PROCESSOR REGISTER (SECBITS)

Bit	NAME	IP14	IP14 AREA
1	ERRERR	14	9
2			0
3			0
4			0

- 1 ERRERR = 0: NO ERROR
- 1 ERRERR = 1: CORRECTED SEND DATA
- 2 NORMAL
- 2 BUS ERROR
- 3 NORMAL
- 3 UNCORRECTED UNUSABLE DATA ERROR
- 4 NORMAL
- 4 MEMORY ERROR

INTERNAL PROCESSOR REGISTER (MEMERR)

Bit	NAME	IP14	IP14 AREA
1	ERRERR	17	1
2			0
3			0
4			0

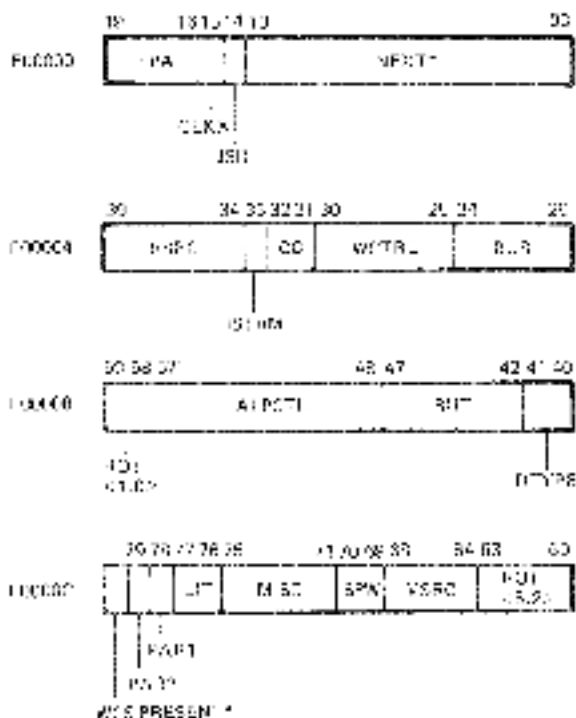
- 1 ERRERR = 0: NO ERROR
- 1 ERRERR = 1: MEMORY ERROR
- 2 NORMAL
- 2 BUS ERROR
- 3 NORMAL
- 3 UNCORRECTED UNUSABLE DATA ERROR
- 4 NORMAL
- 4 MEMORY ERROR

INTERNAL PROCESSOR REGISTER (MEMERR)

Bit	NAME	IP14	IP14 AREA
1	ERRERR	17	2
2			0
3			0
4			0

- 1 ERRERR = 0: NO ERROR
- 1 ERRERR = 1: MEMORY ERROR
- 2 NORMAL
- 2 BUS ERROR
- 3 NORMAL
- 3 UNCORRECTED UNUSABLE DATA ERROR
- 4 NORMAL
- 4 MEMORY ERROR

WCS (K1750) REGISTER DATA WRITE FORMAT



NOTE: WCS ADDRESS SPACE IS 00000 THROUGH 00110

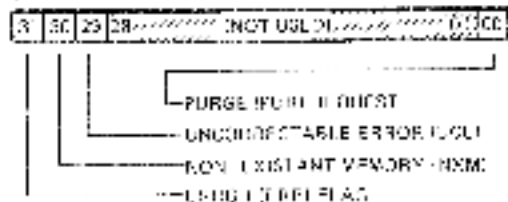
BIT 6000 IS WRITTEN AS 1 ON THE LAST WORD
 WRITTEN TO THE WCS. WCS WILL NOT BE EXECUTED
 UNLESS WCS WILL BE EXECUTED.

10-1000

UBI AND SUB REGISTERS

UBI OR SUB (0x750) CONTROL/STATUS REGISTER (C&S)

0x750: A10x000000



17-246

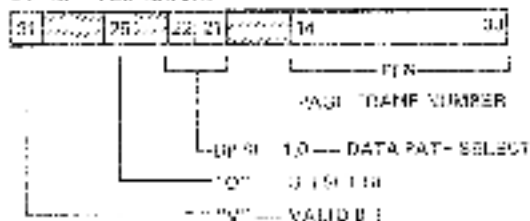
UBI Addresses

Control/Status Register	UBI Address	SUB Address	Buffered Code Addr
UBI 1	E32284	717874	UBI 1
UBI 2	F17708	752874	UBI 2
UBI 3	F1770C	752878	UBI 3

UBI AND SUB REGISTERS (CONT)

UBI OR SUB MAP REGISTER DATA

CV DATA LONGWORD



16-0014

CV DATA FIELD

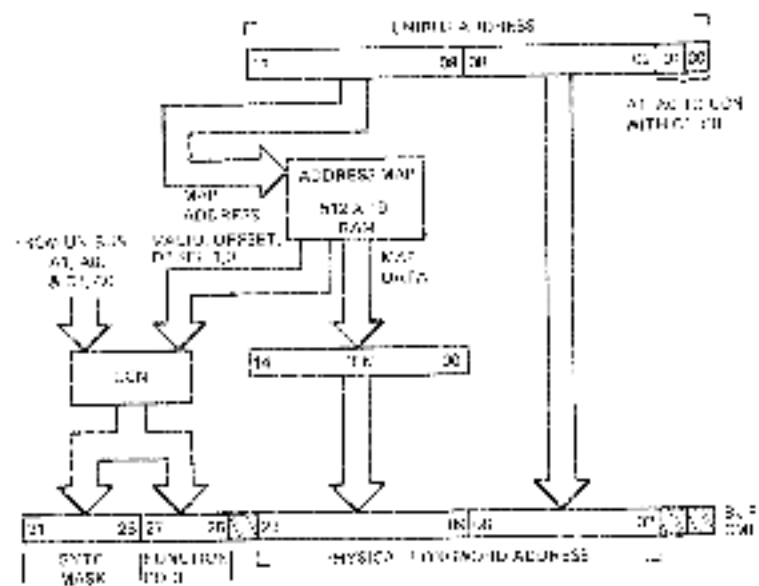
Bit	Field	Description
31	VALID	VALID
23-16	TAG	Tag
15-8	TAG BANK NUMBER	Tag Bank Number
7	DATA PATH SELECT	Data Path Select
6	DATA PATH	Data Path
5-0	DATA	Data

MAP Register Addresses

MAP Register	MAP Address	SUB Address
MAP 000	E10000	F00000
MAP 001	F10000	F00004
...
MAP 009	E10008	F00008
MAP 010	F10008	F0000C

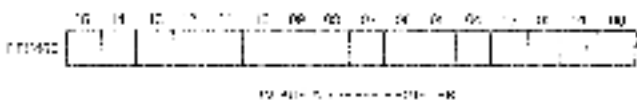
UBI AND SUB REGISTERS (CONT)

UNIBUS TO CMI MAP ADDRESS TRANSLATION



UBI AND SUB REGISTERS (CONT)

UBT REGISTERS

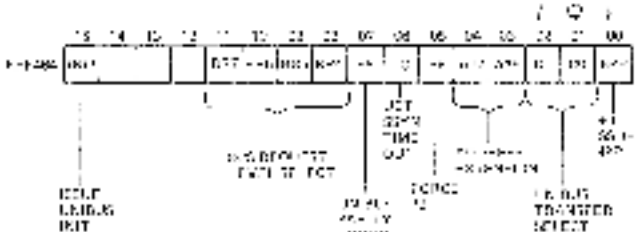


UBT0[15:0] = 0000000000000000



UBT1[15:0] = 0000000000000000

UBT CONTROL STATUS REGISTER



UBT0 - 0000
UBT1 - 0000

UBT0 - 0000
UBT1 - 0000
UBT2 - 0000
UBT3 - 0000

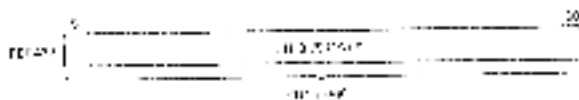
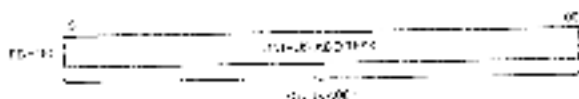


UBT2

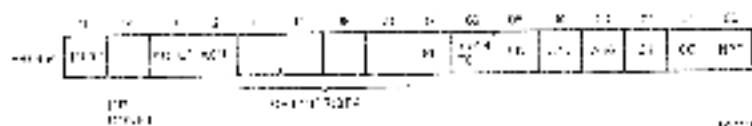
UBI AND SUB REGISTERS (CONT)

IPEC REGISTERS

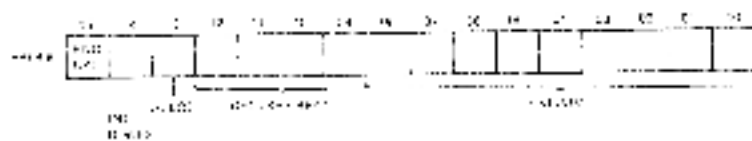
UNIBUS Address and Data Registers



Control Register 1 (CR1)



Control Register 2 (CR2)



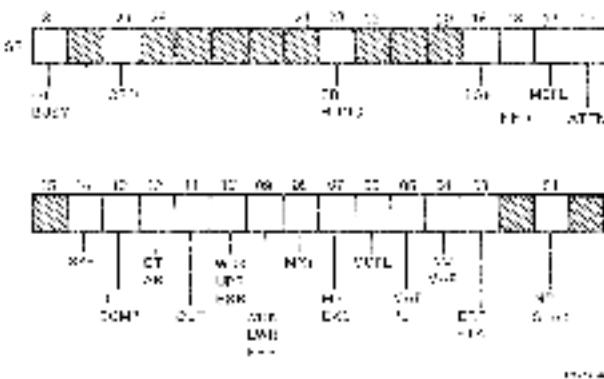
MBA (RH75G) REGISTERS

MBA INTERNAL REGISTERS

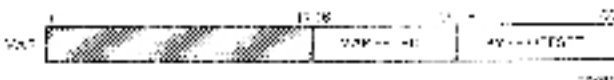
Control Register (CR) – F95004



Status Register (SR) – F28008



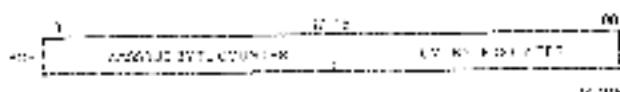
Virtual Address Register (VAR) – F2800C



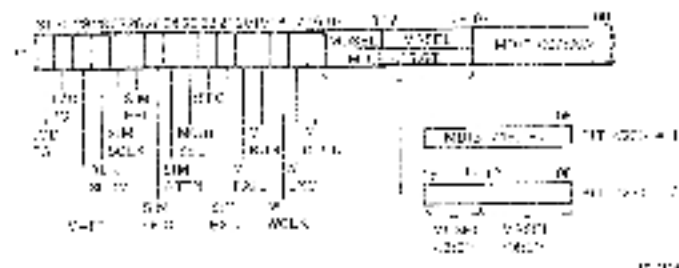
MBA (RH750) REGISTERS (CONT)

MBA INTERNAL REGISTERS (CONT)

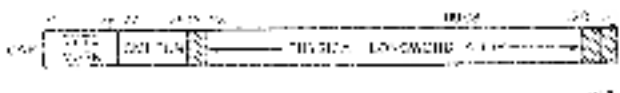
Byte Count Register (BCR) – F2B010



Diagnostic Register (DR) – F2B014

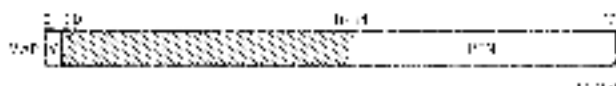


Command Address Register (CAR) – F2B01C

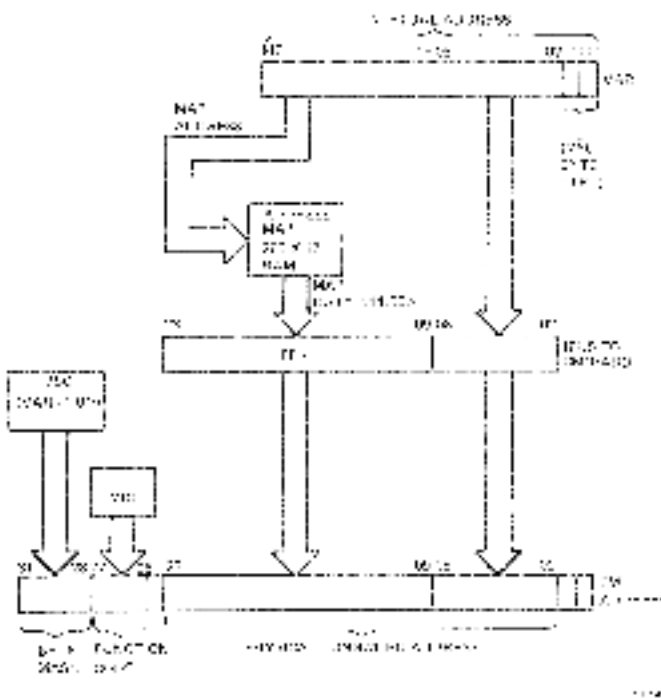


MBA (RH/50) REGISTERS (CONT)

MBA MAP REGISTER DATA – F2820C – F28BFC



MBA TO GMI MAP ADDRESS TRANSLATION



MPA (RH750) REGISTERS (CONT)

MASSBUS EXT. (INAL) DEVICE REGISTERS

Drive Control Register (R0) - F28460

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										0	0	0	0	0	0

0000

Attention Summary Register (R4) - F28410

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
							0	0	0	0	0	0	0	0	

0000

0211 REGISTERS

REGISTRATION
DATE

1962-12-12

1963-01-15

1963-02-18

1963-03-21

1963-04-24

1963-05-27

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-01	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-02	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-03	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-04	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-05	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-06	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-07	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0211-08	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

REGISTRATION DATE: 1962-12-12
 1963-01-15
 1963-02-18
 1963-03-21
 1963-04-24
 1963-05-27

RKR11 REGISTERS

100 FM
 101 FM
 000
 100-10
 100-10
 100

REGISTERS

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

REGISTERS										REGISTERS									
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

RK51: REGISTERS (CONT)

REGISTER OVERVIEW REGISTER

REG 5

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

 SYSTEM
 ADDRESS
 0-10
 0000-1000
 0000-1000

REG 10

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

DATA REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

REGISTER ADDRESS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

REGISTER ADDRESS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

REGISTER OVERVIEW REGISTER

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

REGISTER OVERVIEW REGISTER

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

REGISTER OVERVIEW REGISTER

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

REGISTER OVERVIEW REGISTER

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

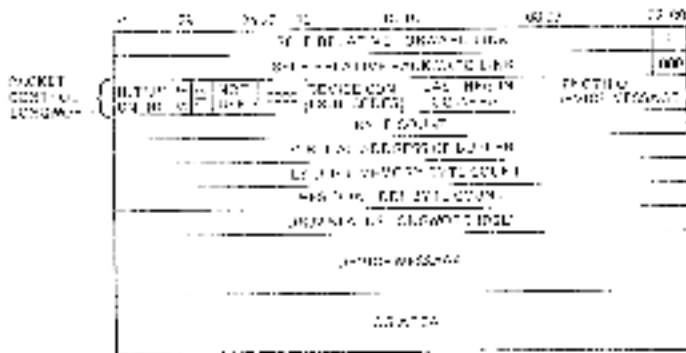
DP750 REGISTERS

DP750 COMMAND BLOCK



44

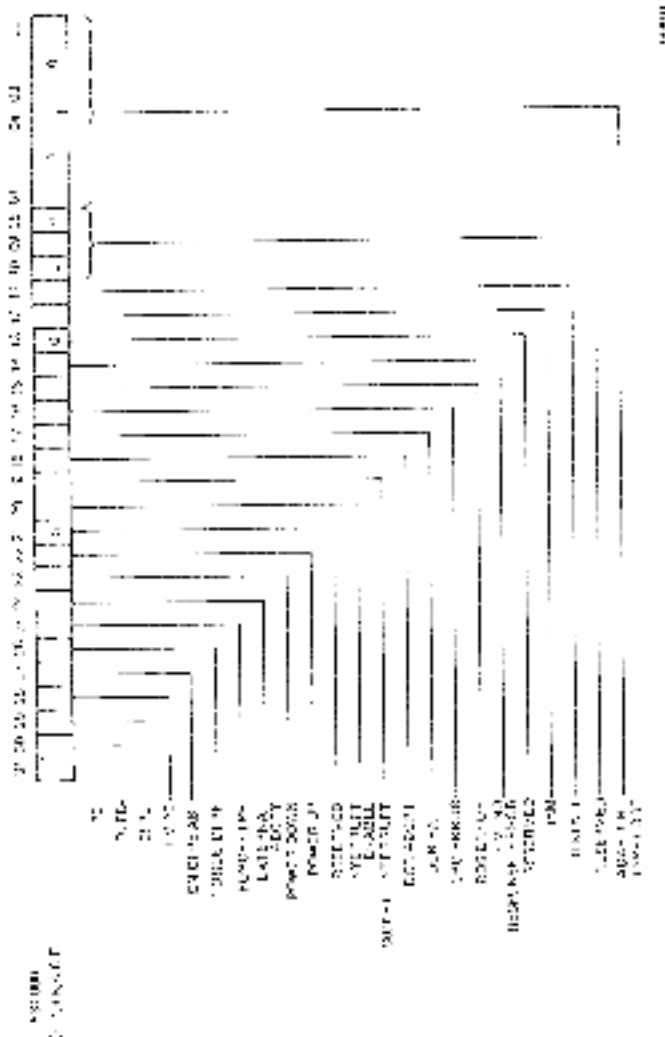
DP750 COMMAND PACKET



44

DR750 REGISTERS (CONT)

DR750 DCR REGISTER - READ FORMAT



DH750 DCH REGISTER - WRITE FORMATS

CONTROL FIELD 1
DECODER

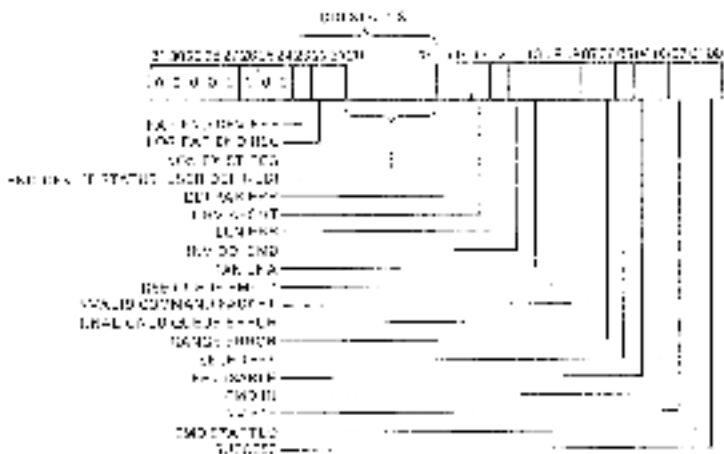
- 0 - NO OP
- 1 - CLEAR POWER KEY - 0110
- 2 - CLEAR POWER/ANALOG BIT 00
- 3 - ECOP
- 4 - CLEAR TEST/ANALOG BIT CONDITION
 4000110001101110
 0000000000000000
 0000000000000000
 0000000000000000
- 5 - PAR TEST/TEST/ANALOG BIT 00
- 6 - PAR TEST/TEST/ANALOG BIT 01
- 7 - PAR TEST/TEST/ANALOG BIT 10

CONTROL FIELD 2
DECODER

- 0 - NO OP
- 1 - PAR TEST/TEST/ANALOG BIT 11
- 2 - PAR TEST/TEST/ANALOG BIT 10
- 3 - PAR TEST/TEST/ANALOG BIT 01
- 4 - PAR TEST/TEST/ANALOG BIT 00
- 5 - PAR TEST/TEST/ANALOG BIT 11
- 6 - PAR TEST/TEST/ANALOG BIT 10
- 7 - NO OP

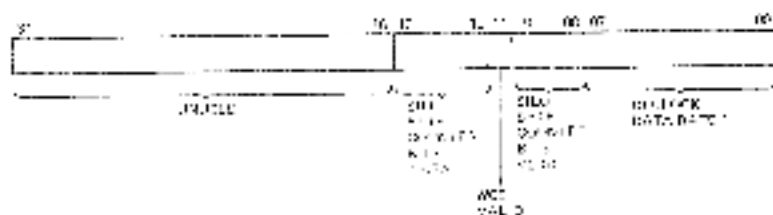
DR750 REGISTERS (CONT)

DR750 STATUS LONGWORD



DR756 REGISTERS (CONT)

DR750 UTILITY REGISTER



DR750 UTILITY REGISTER
 DR750 UTILITY REGISTER

15-10

DR750 GLOCK DATA RATE SELECTION

Utility Register 01 0000 0000
 (DR750/0000)

P0 to P9	00
P0	1.10
P1	2.50
P2	2.88
P3	1.78
P4	1.50
P5	1.50
P6	1.90
P7	1.10
P8	1.00
P9	3.90
P0	3.00
P1	3.00
P2	3.00
P3	3.00
P4	3.00
P5	3.00
P6	3.00

*Timing of these registers by the JCL were not
 provided.

DR750 REGISTERS (CONT)

DR350 DEVICE VECTORS

Base Address	Device Number	REG	OFF	REG#	OFF
210000	8	20	168	168	168
210008	11	207	160	167	160
210010	12	20	176	169	168
210018	15	157	174	167	174
210020	14	155	170	165	170
210028	17	150	170	160	170

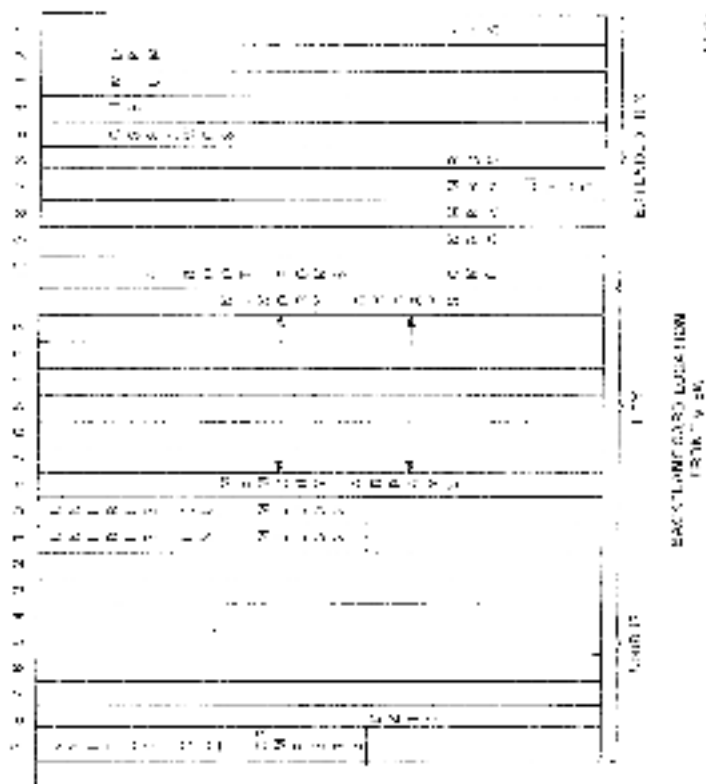
*Default interrupt level is 80h.

CHAPTER 3

MODULES AND GATE ARRAYS

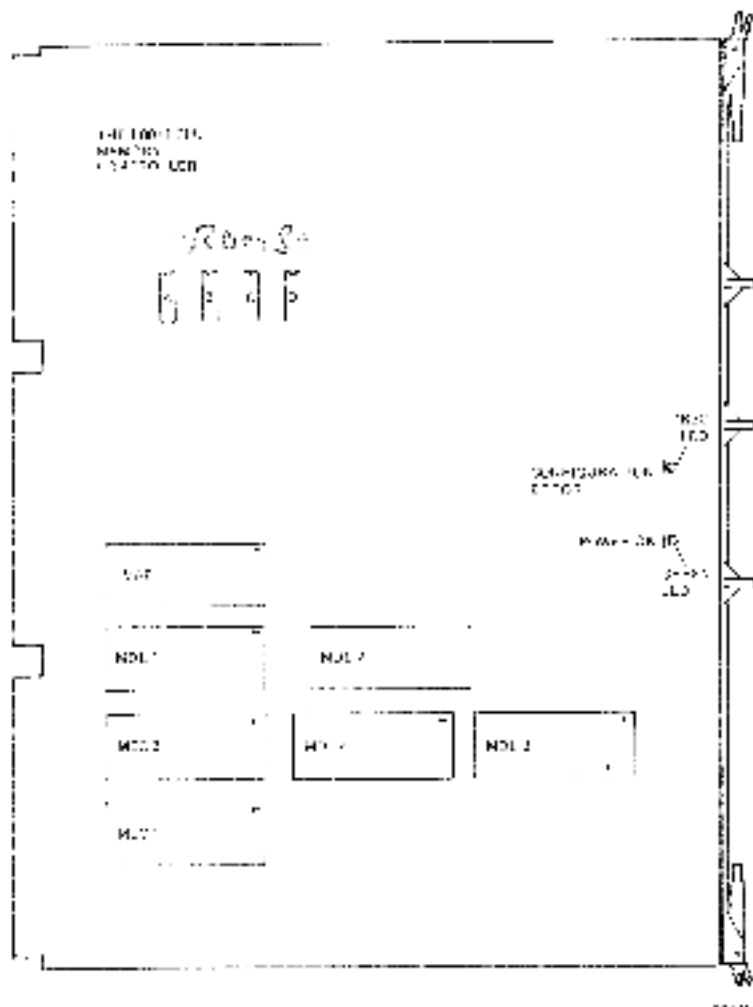


VAX 11/760 MODULE UTILIZATION

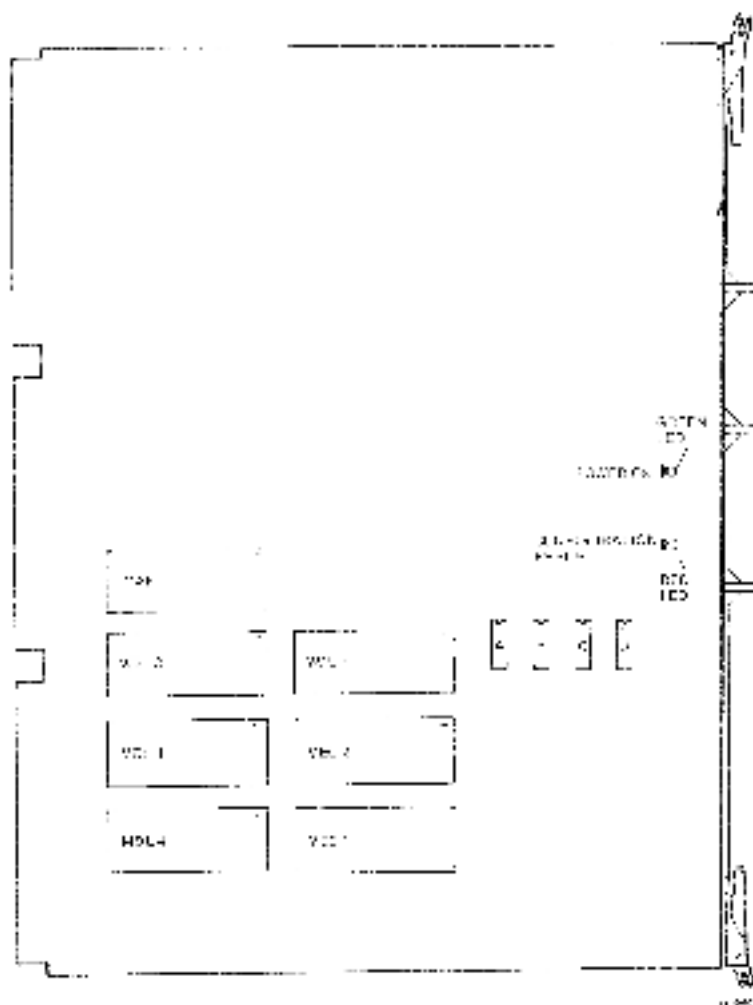


CABLE
TO
RACK 414
VPC

DMC GATE ARRAY LAYOUT (L0011)



CMC GATE ARRAY LAYOUT (L0016)



CMC GATE ARRAY DESCRIPTION

- MEM** - 2048 memory data bits (KDB) which make up the data path between the CMT and array, the CMT and the configuration registers, and also the bootstrap ROMs to array.
- MEM** - Two memory array locations (MEM) whose default location is 000000, and default 000 between single bit, 000000.
- MEM/ROM** - One memory address processor (MEM) which is the CMT and one array address decoder (MEM) which is the CMT. Memory bits are located to enable memory array and bootstrap starting address. Address control lines are also located and memory array load population is detailed.

BD01STRAP DEVICE ROMS

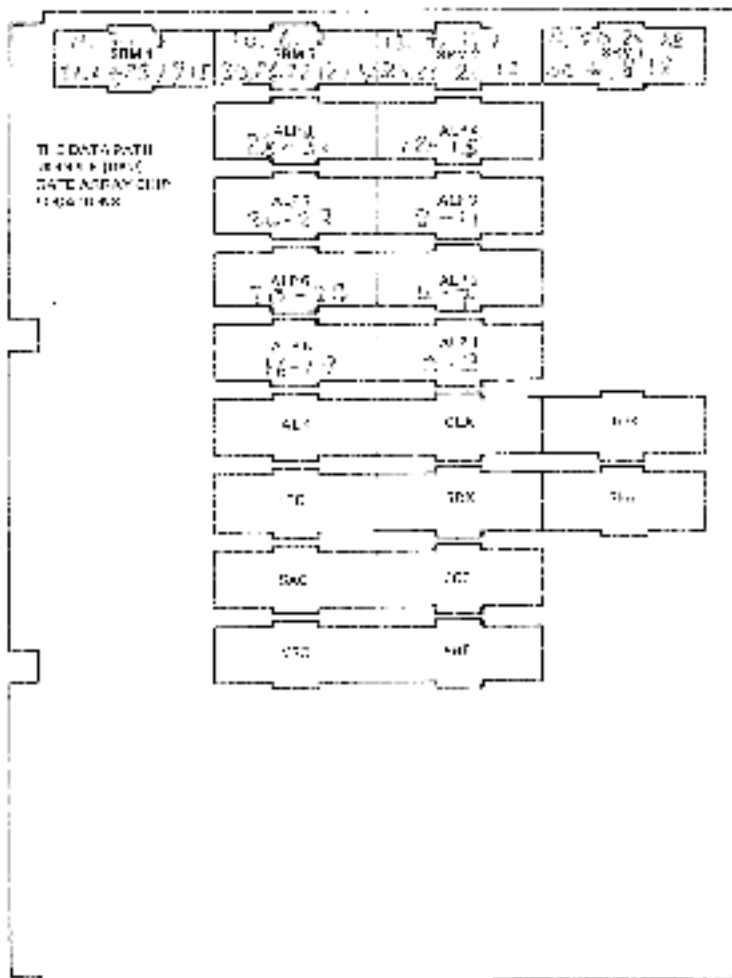
ROM Part Number	Location	Device Type	Control Line	Notes
21-88888-01	B	1K8	MEM	
21-88888-02	B	1K8	MEM	
21-88888-03	B	1K8	MEM	

Additional serial serial processor (SP) is required for MEM.

ROM Starting Microaddresses

Device	Starting Microaddress
A	MEM
B	MEM
C	MEM
D	MEM

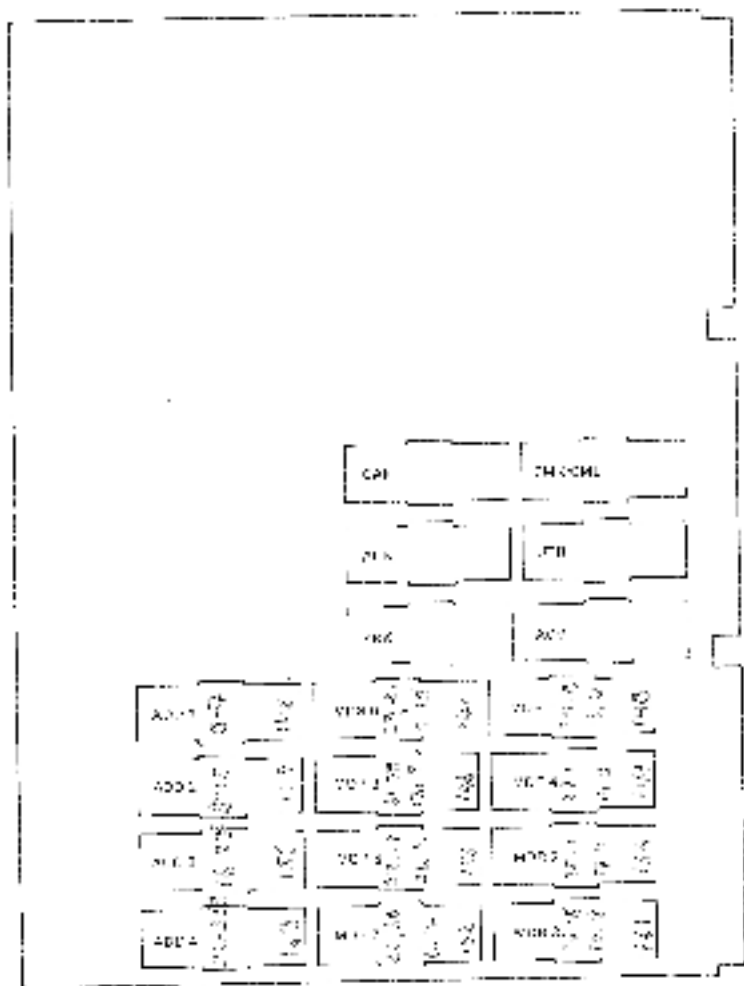
DM91 GATE ARRAY LAYOUT (L0002)



DPM GATE ARRAY DESCRIPTION

- 76F - Four 16-bit parallel multipliers (76FM) which perform 64 functions under the control of the BAK.
- 76S - One super control control (76SC) chip controls 76F operations.
- 76P - Eight arithmetic logic processor (76P) chips work as the arithmetic logic unit (ALU) of the CPU. One 76P performs most of the data manipulations during the execution of each instruction.
- 76T - One arithmetic logic control (76TC) chip controls ALU operations by decoding instruction inputs and generating the necessary signals.
- 76V - One super look-ahead (76VL) chip contains the logic that the ALU uses to generate and propagate carries.
- 76Z - One three operation control (76ZC) chip controls the programmable internal logic slices.
- 76D - One construction register decoder (76DR) chip processes the IR inputs. Some use signals and control signals from the output of other decoders (76R), decoder 16, and generates signals to control the internal arithmetic routines.
- 76A - One addressable addressing (76AA) chip controls the 64 multiplexed register addressing. Contains logic that keeps track of general purpose registers (GPR) addresses and autoincrement.
- 76C - One register initialization and clear (76CI) chip is associated with the 76Z decoders, bus-line arbitration, and system blanks.
- 76G - One condition code (76CC) chip is associated with the condition codes for each 76P and comparability code instructions. It stores 244 bits (E, O, N, Z, C, S, V, and D), and masks the bits at the request of the processor.
- 76Q - One microsequencer (76QS) chip, together with the 76C section, forms the 8BT microsequencer that sequences the CPU microcode.
- 76H - One programmable ASIC (76HW) chip contains 8BT state, status flags, the stack and LRU, and other four performed control logic of the 8BT microsequencer.

MIC GATE ARRAY LAYOUT (L5003)

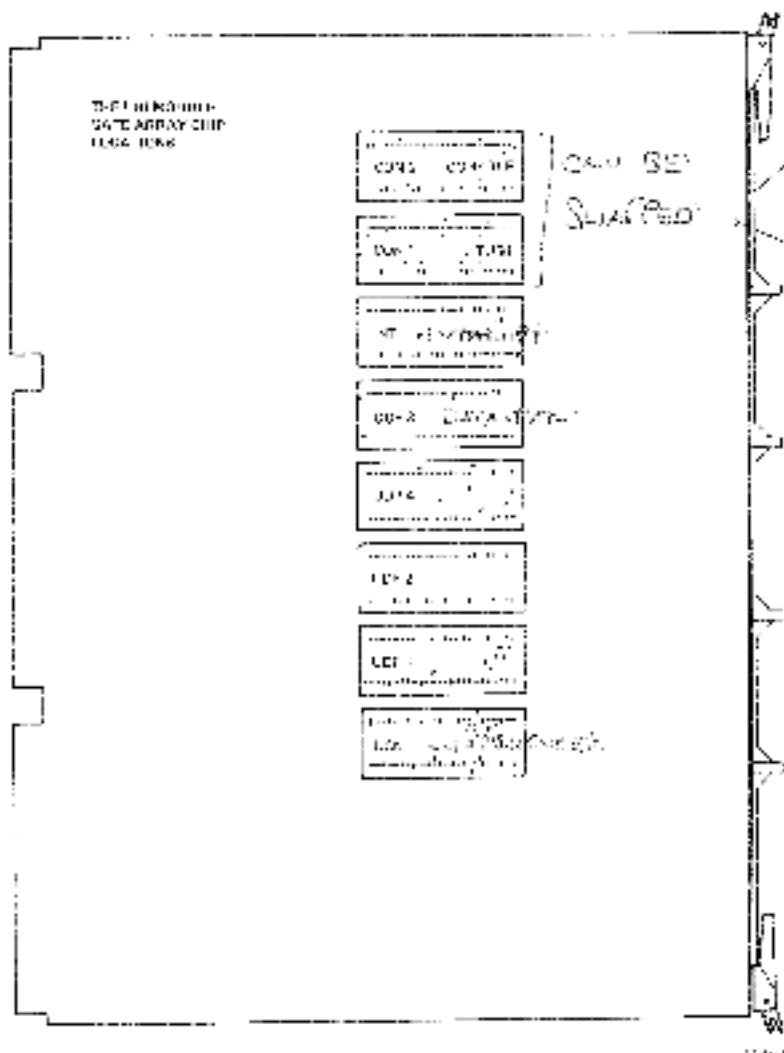


503

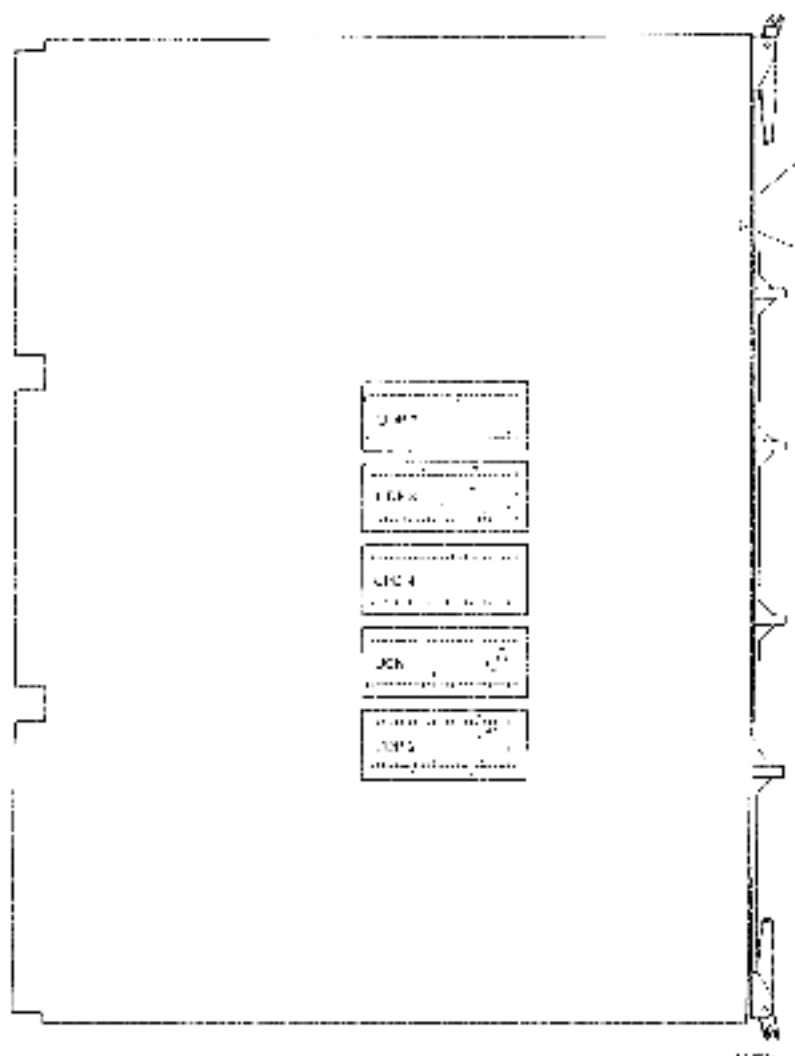
MIC GATE ARRAY DESCRIPTION

- MEM - Eight memory data buffers (MEM) chips handle logic that controls data flow to or from the CPU via the M, D, S, M-H, or S-H bus.
- PRV - One address control (PRV) chip handles address control instructions. It decodes system bus memory requests with the PC address. It also replaces error beeps on a line during program execution.
- ADR - One address control (ADR) chip controls the MIC addressing logic.
- ADR - Four address (ADR) chips work with the PC and SA registers and their load values.
- CRK - One CRT control (CRK) chip monitors and translates CRT control signals. It also monitors under certain conditions, a CRT chip is installed in the plane for the 6770.
- CRK - One cache control (CRK) chip monitors or disables cache. It controls the transfer of data to or from the MEM chips.
- UCP - One addressing (UCP) chip monitors address conditions that cause a violation.
- SPV - One access violation (SPV) chip detects access violations, control store parity errors, CPU reserved addresses, undefined data, and user memory violations.

UBI GATE ARRAY LAYOUT (L0004)



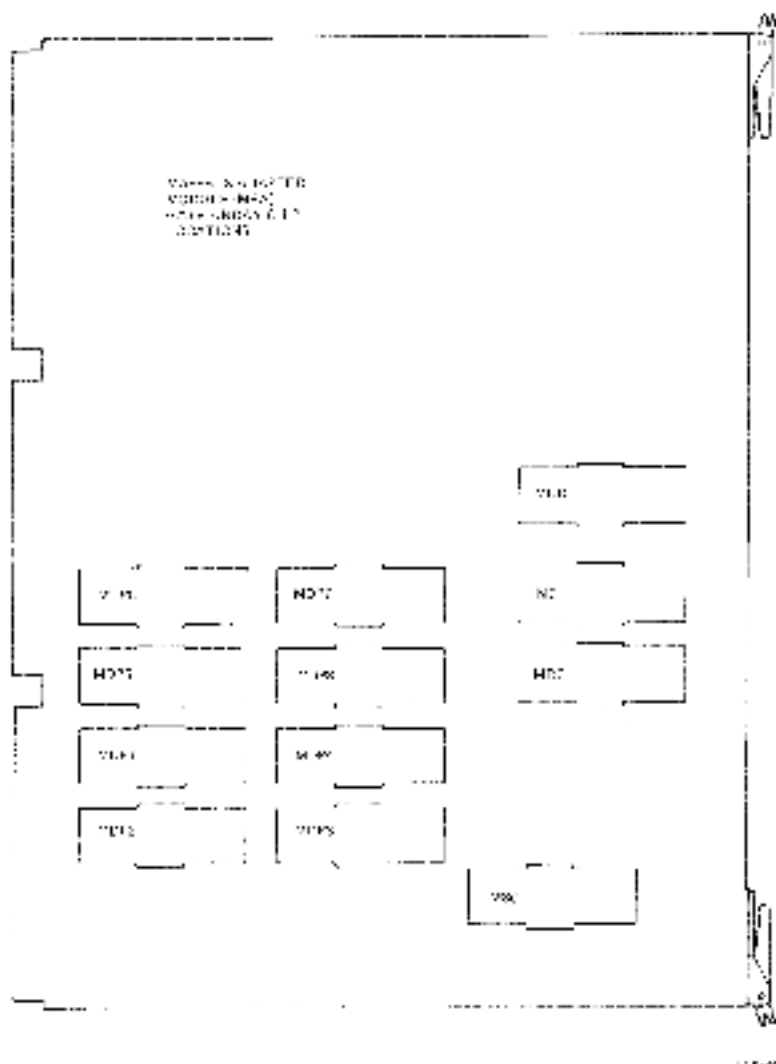
SUB GATE ARRAY LAYOUT (L0010)



URI AND SUB-GATE ARRAY DESCRIPTION

- 039 - Main HBTMS Data path (DPA) chips make up the data path logic for the HBT and HBT. All address and data information passes through the HBT between four tristate buffers (DPA, R/P DPA, JP DPA, LS address). Contains address logic and various logic for the Latched Data paths and for CPU access to HBT or HBT and HBT registers.
- 03K - On UNTEB control (HBT) this works in conjunction with the HBT and HBT control logic to provide microprogrammed memory access operations. Contains the logic and error flags for the buffered data paths, performs interpretation between the HBT and HBTMS control signals and defines operations.
- 03T - On internal HBT chip to the JP, performs arbitration to provide 21 interrupt requests and stored values on the transmitter lines to show the CPU. Contains all of the HBT, which also the UNTEB for transactions from the CPU, arbitrates bus requests (PBA) from the back end, and issues bus grants (PBA).
- 03K - The control (CPU) chips on the HBT such as HBT, Serial/Parallel I/O for communication between the CPU and the HBT and control beyond the HBT. Contains limited control beyond consumer recognition.

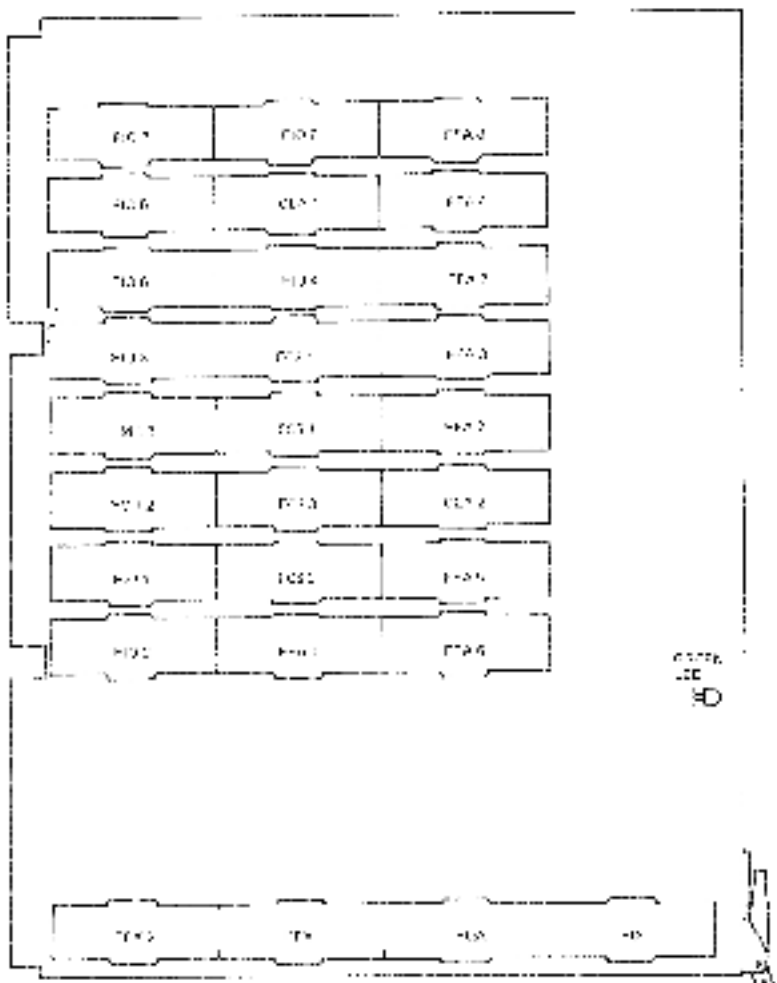
MEA GATE ARRAY LAYOUT (LD007)



MBA GATE ARRAY DESCRIPTION

- M01** - Eight 16800 3 data ports (M01) chips receive data between five controllers (ports 0007, 0008, 0009, 0010, 0003). All addresses and data information is received through bus 0001. Each chip address bus 0 and compare bus 0 for bus access to M01 and M00000 controller.
- M02** - One 168000 data bus control (M02) chip maintains and performs status on multiple bus cycling and on bus parity and validity. It is used and coordinated the start and end of bus transfers. Contains and controls bit stream on the bus and initiates the parity/valid chip status.
- M03** - One 168000 interface control (M03) chip maintains M02 and CPU interface and CPU attention status generation and checking and program interrupt. Provides the CPU control codes for bus transfers on the CPU and controls bus address translations. Status logic detects bus transfer with interrupt on external registers and directs the bus to proceed the transfer.
- M04** - One 16800 register control (M04) chip responds to the M01 on CPU transfers with incomm of external peripheral. Detects the issue of a valid data transfer control and returns 1 for the M02. Provides control signals to the control bus via the CONTROL bus/inter means that control strobing in the M02 registers.
- M05** - One 16800 data control (M05) chip maintains data transfer functions such as last control word loading and alignment between bus 0001 and the M02 registers. Provides the CPU address, control bus/inter on CPU parity conditions, and generates and checks parity on CPU and M02000 data. Provides the CPU data bus with the M02 controller on the CPU.

FPA GATE ARRAY LAYOUT (LD0001)



*LOWER LEVELS ARE NOT SHOWN (FPA GATE ARRAY IS NOT LOCATED HERE)

FPA GATE ARRAY DESCRIPTION

- FPA - Eight floating functional arithmetic (FFA) chips form the arithmetic logic unit (ALU) of the CPU. The ALU performs most of the data manipulations during the execution of floating-point instructions. It outputs the 64-bit ZW bus to the CPU.
- CLA - Two carry look ahead (CLA) chips contain logic used by the ALU and addresses a 16-bit bus.
- FLC - Eight floating input/output (FIO) chips interface operands from the M bus and W bus. Also interface to bus operand registers.
- YCH - Four floating carry shifter (YCS) chips perform right or left shifts in multiples of four. Produce a 64-bit output from a 64-bit input.
- PGA - Two floating quick aligner (PGA) chips position the PC8 for certain operations.
- THR - Two fraction multiplier (FRM) chips contain most of the logic that performs fraction multiplication.
- TKX - Two floating exponent (FV) chips form the exponent data path.
- SCV - Two floating condition code (FCC) chips process all operands to certain condition code codes for traps, faults, and the ZW.

GATE ARRAY PART NUMBER/MODULE CROSS-REFERENCE

Gate Number	Gate Reference	Original Part. No.	Host Module	Original Number	Gate Pinout
70025	108	19-11000	098	1	108-100-010P
70027	908	1-1488	NTC	-	108-08-15, 21N
				2	171-79-1, 1, 80
				3	122-18-11, 21N
				4	123-11-19, 21N
				5	124-11-25, 21N
				6	125-13-21, 21N
				7	126-11-15, 19
				8	127-13-23, 21N
70028	ALL	19-11001	098	1	123-08
				2	127-04
				3	111-04
				4	125-12
				5	119-11N
				6	123-08
				7	117-11
				8	111-11
70029	APD	19-14011	K12	1	177-03
				2	125-03
				3	123-10
				4	127-04
70030	000	19-14012	098	1	
70041	008	19-14025	057	1	10-008
				2	10-056-10
70042	018 208	19-14016	098	1	
				2	070-100N
				3	127-02N
70043	108	1-1688	K12	-	180, 84, 88, 13, 16, 28, 21, 25, 120
				2	121, 85, 29, 13, 17, 21, 25, 19, 11N
				3	121, 26, 8, 1, 18, 29, 25, 18, 11N
				4	171, 77, 11, 15, 19, 29, 27, 11N
70044	808	19-14088	098	1	
70045	408	19-14089	098	1	
70047	787	19-14040	098	1	
70049	500	19-14091	098	1	

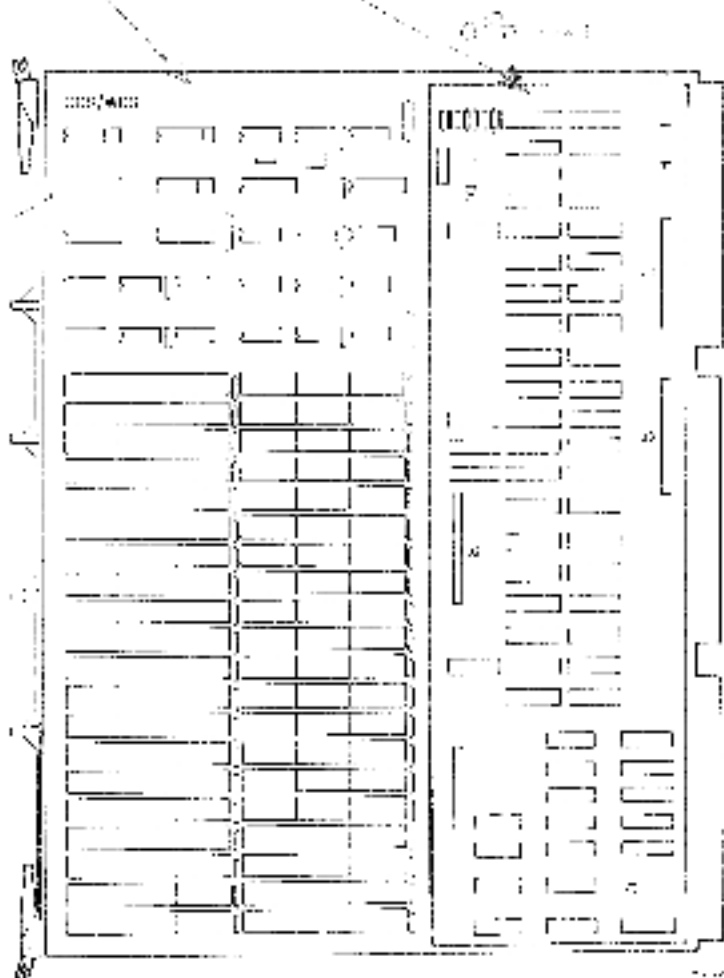
GATE ARRAY PART NUMBER/MODULE CROSS-REFERENCE (CONT)

Orig. Part No.	Chip No.	Part No.	Module	Quantity	Gate Array
70611	HEP	19-14702	JSL706	1	628,32,75,75
				2	75,75,75,75
				3	628,32,75,75
				4	75,75,75,75
70612	JCB	19-14703	INT/700		
70620	TCB	19-14704	APN	1	
70621	NSD	19-14705	JPN	1	
70622	ABD	19-14706	APN	1	
70627	DMF	19-14707	R77	1	
70628	EM7	19-14708	R2C	1	
70628	BC4	19-14709	R1L	1	
70629	EM7	19-14704	R6F	1	
70627	EM7	19-14704	R1L	1	
70628	EM7	19-14704	R1L	1	
70629	EM7	19-14704	EM7	1	
70630	EM7	19-14704	JPC	1	
70631	EM7	19-14704	EM7	1	631,60
				2	631,60
70632	EM7	19-14704	EM7	1	632,71
70633	EM7	19-14704	EM7	1	633,60
				2	633,60
				3	633,60
				4	633,60
70634	EM7	19-14704	EM7	1	634,55,71,70
				2	634,55,71,70
				3	634,55,71,70
				4	634,55,71,70
				5	634,55,71,70
				6	634,55,71,70
				7	634,55,71,70

GATE ARRAY PART NUMBER/MODULE CROSS-REFERENCE (CONT)

DATA BOOK PART NUMBER	DATA BOOK REFERENCE	DATA BOOK PART NO.	Module REF CODE	Package Number	DATA BOOK REF CODE
DL167	PGA	19-14711	PGA	1 2 3 4	DL167A-80...840 DL167B-80...850 DL167C-11...860 DL167D-11...870
DL030	PGA	19-14710	PGA	1 2 3 4 5 6 7 8	DL030A DL030B DL030C DL030D DL030E DL030F DL030G DL030H
DL025	PGA	19-14710	PGA	1 2	DL025A, DL025B DL025C, DL025D
DL041	PGA	19-14710	PGA	1	DL041A DL041B
DL042	PGA	19-14710	PGA	1	
DL043	PGA	19-14710	PGA	1	
DL046	PGA	19-14710	PGA	1 2 3 4 5 6 7 8	DL046A, DL046B DL046C, DL046D DL046E, DL046F DL046G, DL046H DL046I, DL046J DL046K, DL046L DL046M, DL046N DL046O, DL046P
DL176	PGA	19-14710	PGA	1	
DL167	PGA	19-14711	PGA	1	
DL048	PGA	19-14710	PGA	1	
DL049	PGA	19-14710	PGA	1	
DL156	PGA	19-14710	PGA	1	DL156A
DL051	PGA	19-14710	PGA	1	DL051A (see page 1)

CCS MODULE WITH WCS (LOADS)



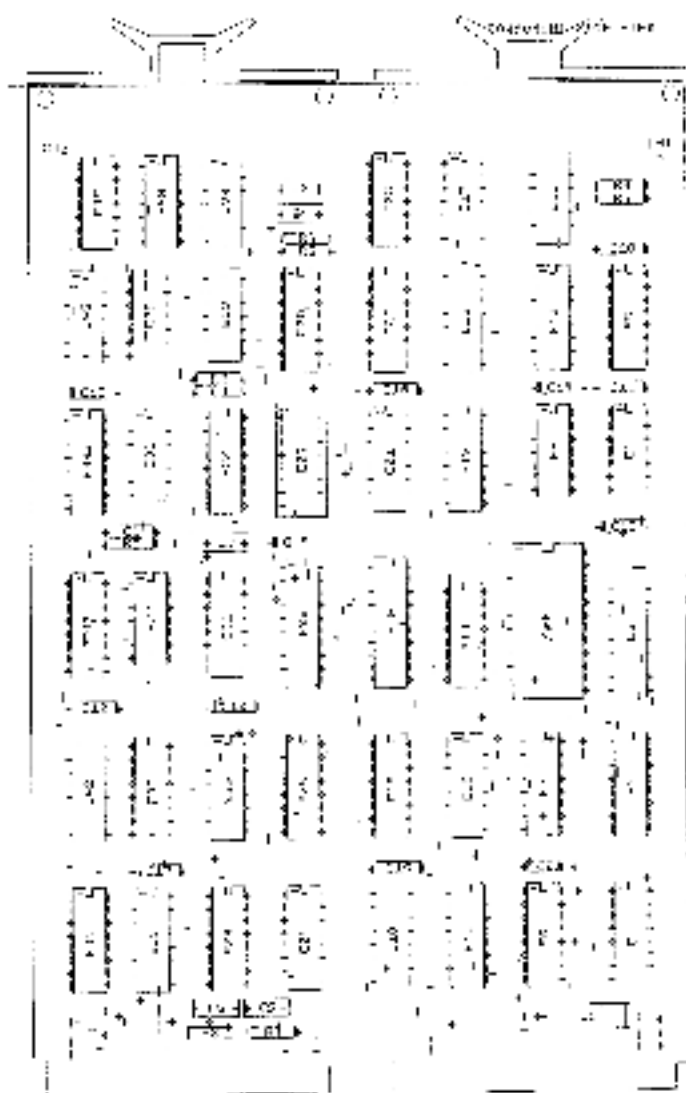
CCS MODULE ROM LAYOUT

					V10				V10				V10				V10			
	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117		
1000-1009	8100	8101	8102	8103	8104	8105	8106	8107	8108	8109	8110	8111	8112	8113	8114	8115	8116	8117		
1000-1009	8120	8121	8122	8123	8124	8125	8126	8127	8128	8129	8130	8131	8132	8133	8134	8135	8136	8137		
1000-1009	8140	8141	8142	8143	8144	8145	8146	8147	8148	8149	8150	8151	8152	8153	8154	8155	8156	8157		
1000-1009	8160	8161	8162	8163	8164	8165	8166	8167	8168	8169	8170	8171	8172	8173	8174	8175	8176	8177		
1000-1009	8180	8181	8182	8183	8184	8185	8186	8187	8188	8189	8190	8191	8192	8193	8194	8195	8196	8197		

NOTE: THE PRODUCTION PARTS IS reserved for those parts which require to be used with other parts.

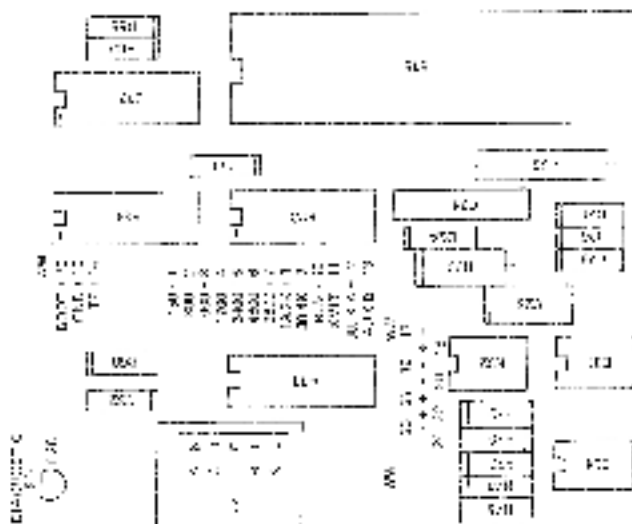
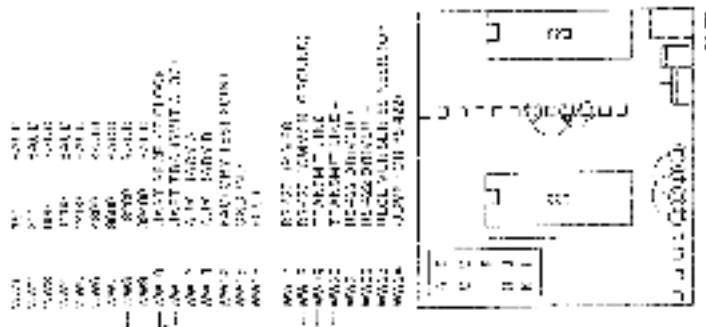
	V10									
	100	101	102	103	104	105	106	107	108	109
1000-1009	8200	8201	8202	8203	8204	8205	8206	8207	8208	8209
1000-1009	8210	8211	8212	8213	8214	8215	8216	8217	8218	8219
1000-1009	8220	8221	8222	8223	8224	8225	8226	8227	8228	8229
1000-1009	8230	8231	8232	8233	8234	8235	8236	8237	8238	8239
1000-1009	8240	8241	8242	8243	8244	8245	8246	8247	8248	8249

UET COMPONENT LAYOUT



NOTE: See circuit card to refer to schematic. All 74183-3-4.

TU58 INTERFACE COMPONENT AND JUMPER LAYOUT



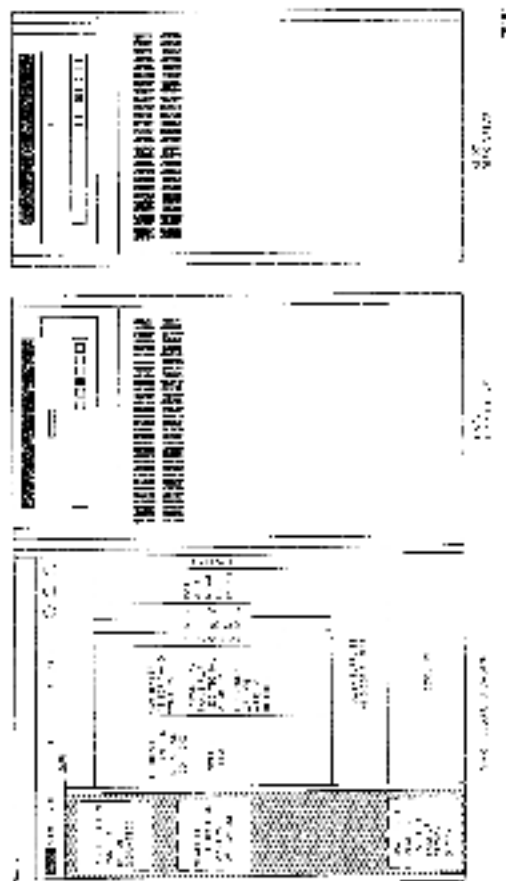
GROUND (C) REV. 8/68

CHAPTER 4
CONFIGURATION AND CABLING



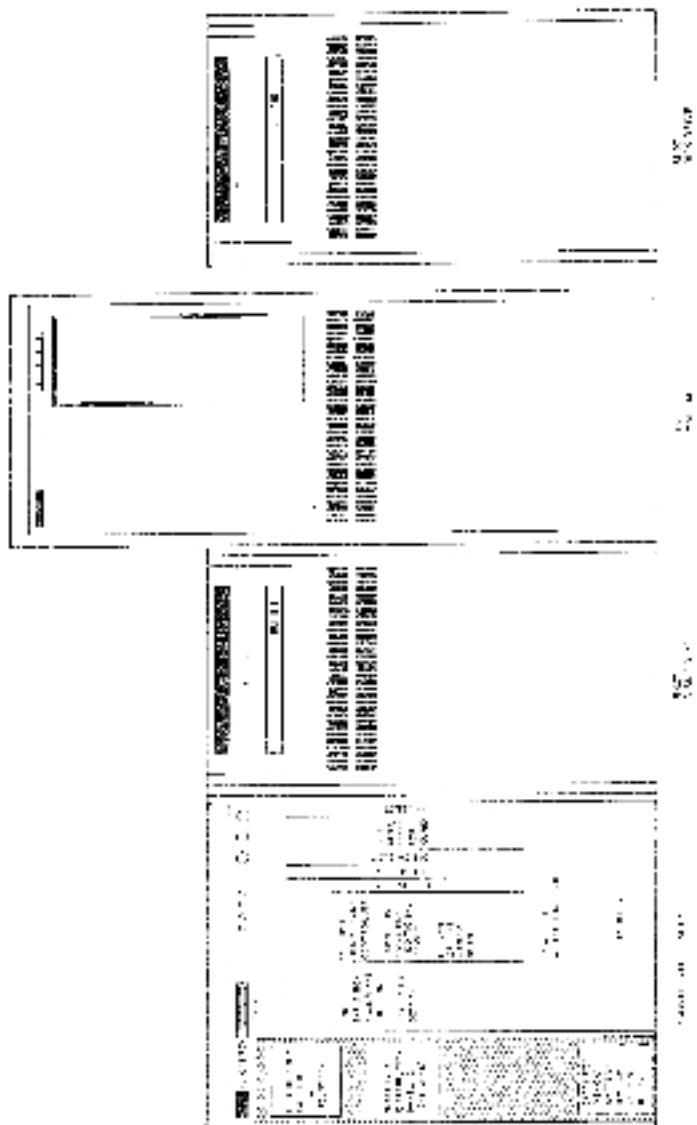
VAX-11/750 SYSTEM CONFIGURATIONS

DUAL RK07 SYSTEM



VAX 11/750 SYSTEM CONFIGURATIONS (DDNT)

DUAL RK07 SYSTEM WITH TS11



VAX-11/750 SYSTEM CONFIGURATIONS (CONT)

MINIPOST SYSTEM



Figure 1-1



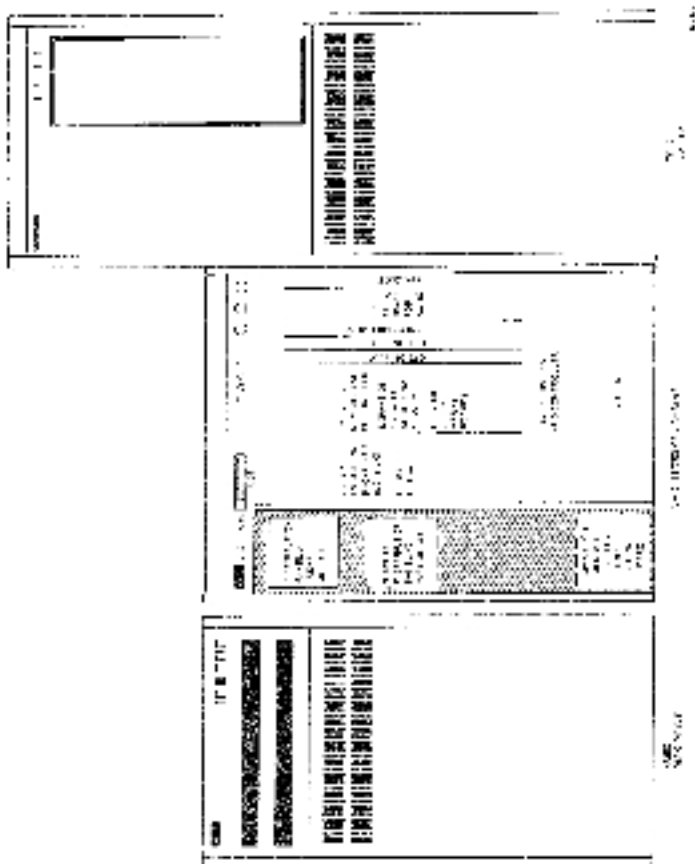
Figure 1-2



Figure 1-3

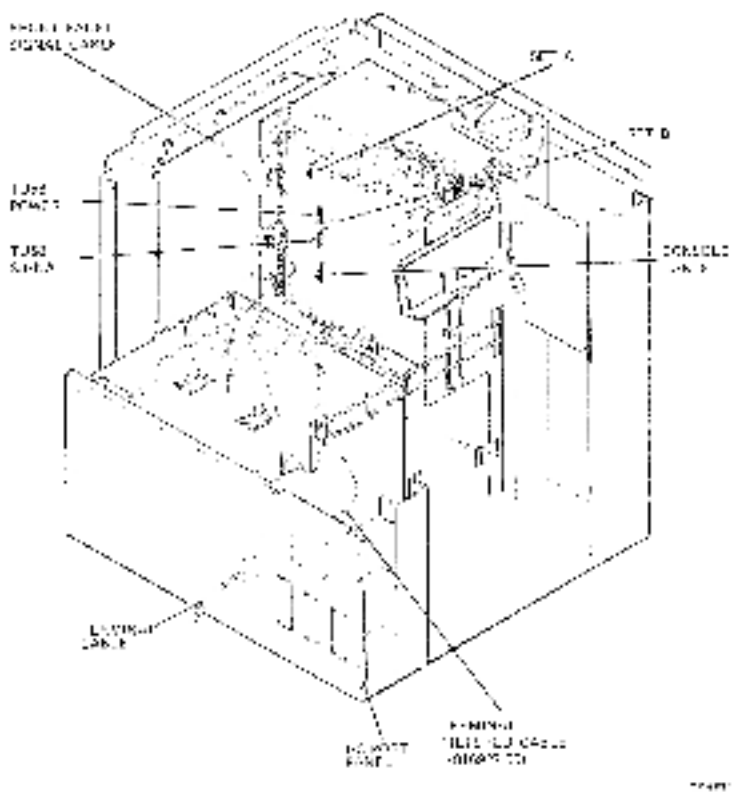
VAX-11/750 SYSTEM CONFIGURATIONS (CONT)

RMU01811 SYSTEM



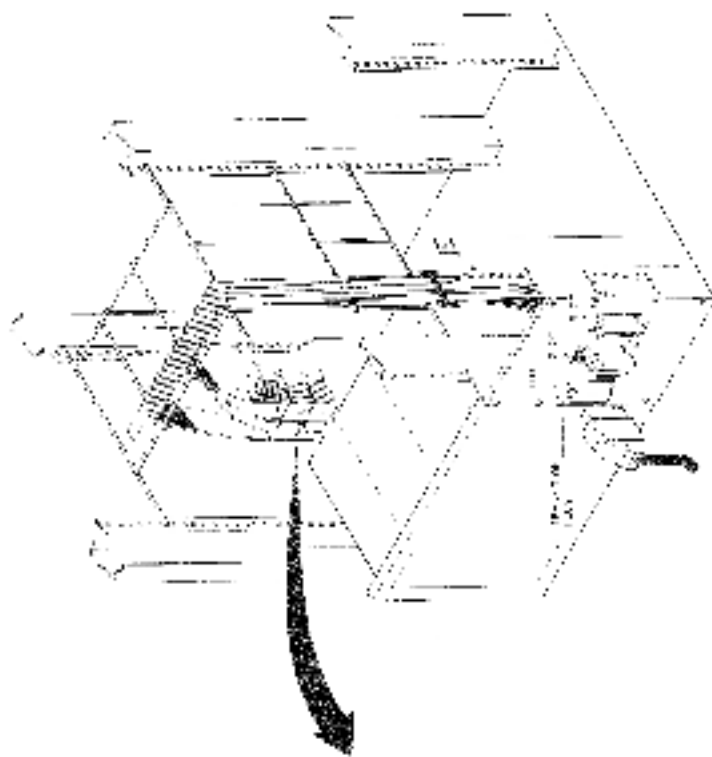
SYSTEM CABLING DIAGRAMS

TUBE AND FRONT PANEL CABLES



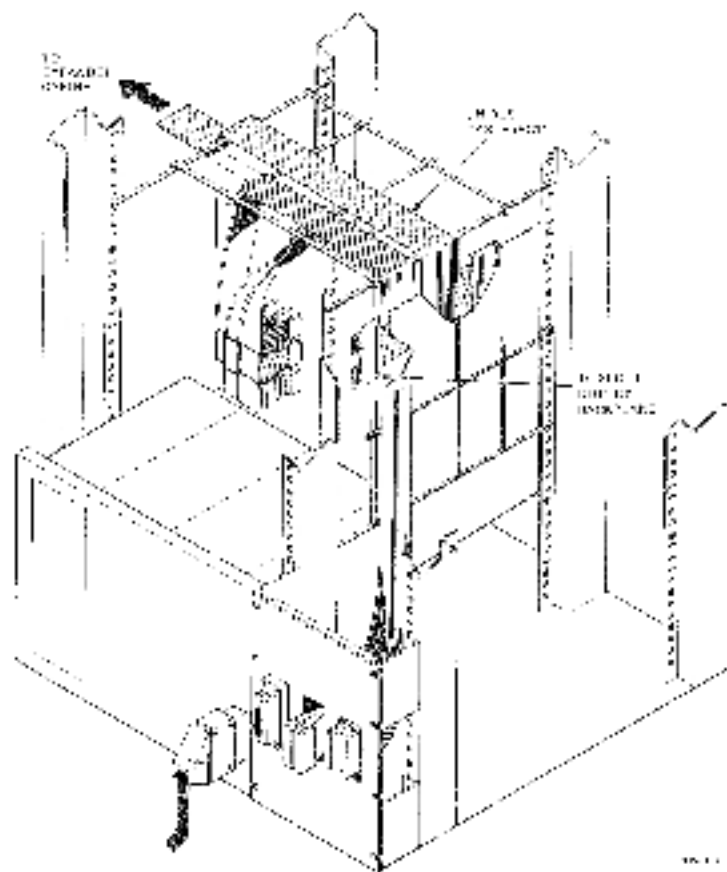
SYSTEM CABLING DIAGRAMS (CONT)

MASSBUS CABLES



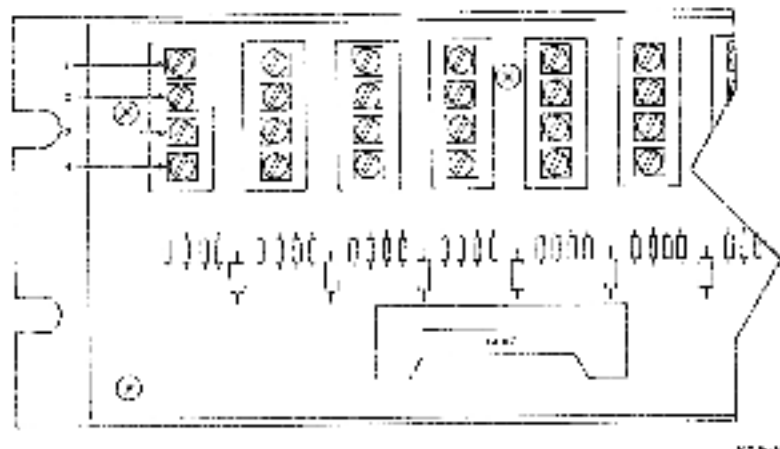
SYSTEM CABLING DIAGRAMS (CONT)

UNITARY CABLES



SYSTEM CABLING DIAGRAMS (CONT)

DZ11 DISTRIBUTION PANEL

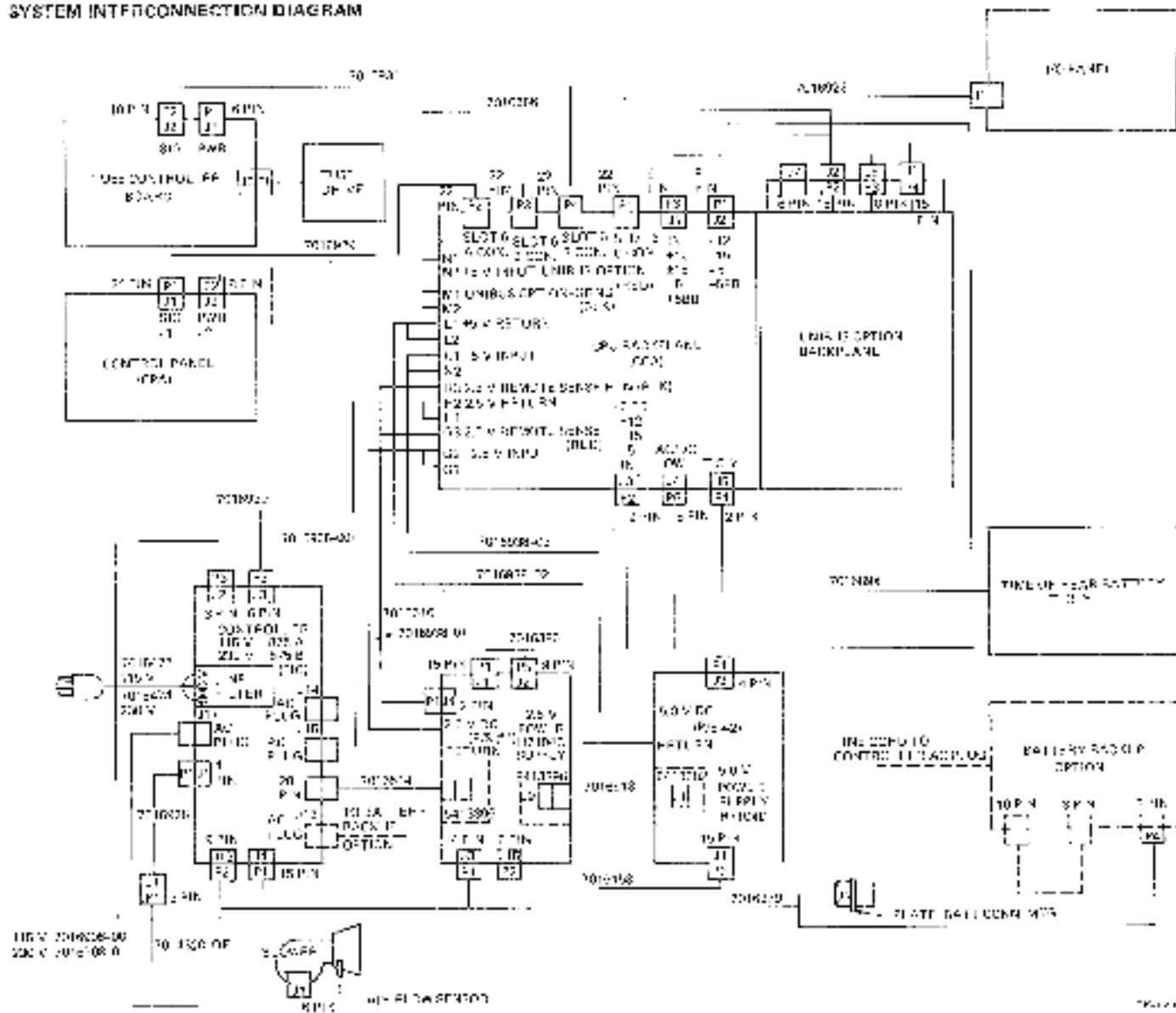


DZ11 DISTRIBUTION TERMINALS

Terminal Number	Signal
1	SEC
2	SEC
3	ATC
4	ATC

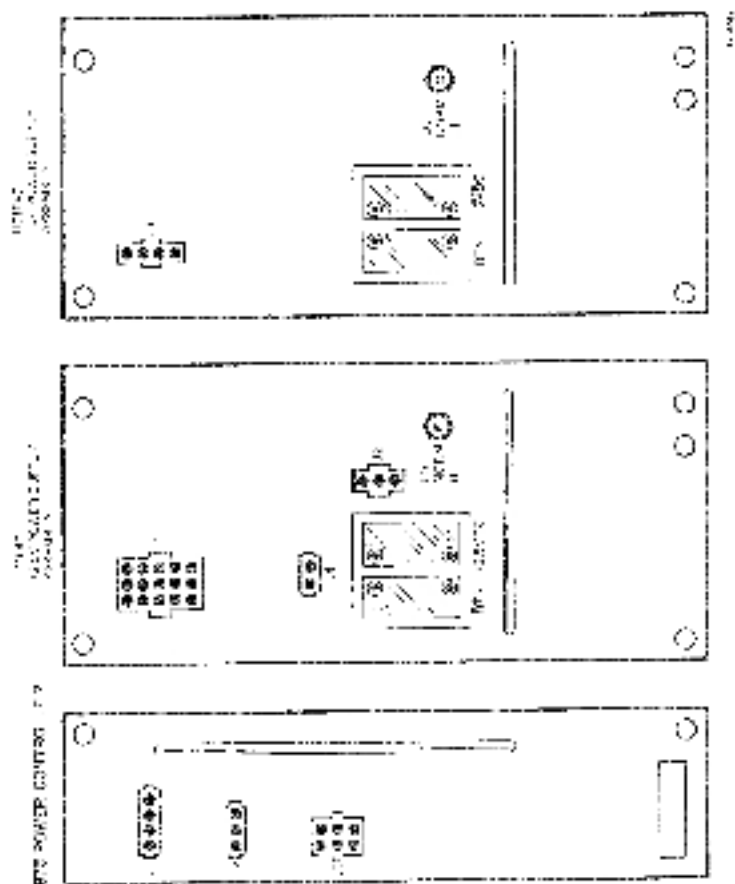
VAX-11/750 POWER SYSTEM

SYSTEM INTERCONNECTION DIAGRAM



VAX-11/750 POWER SYSTEM (CONT)

VAX-11/750 POWER SUPPLY, PART 1

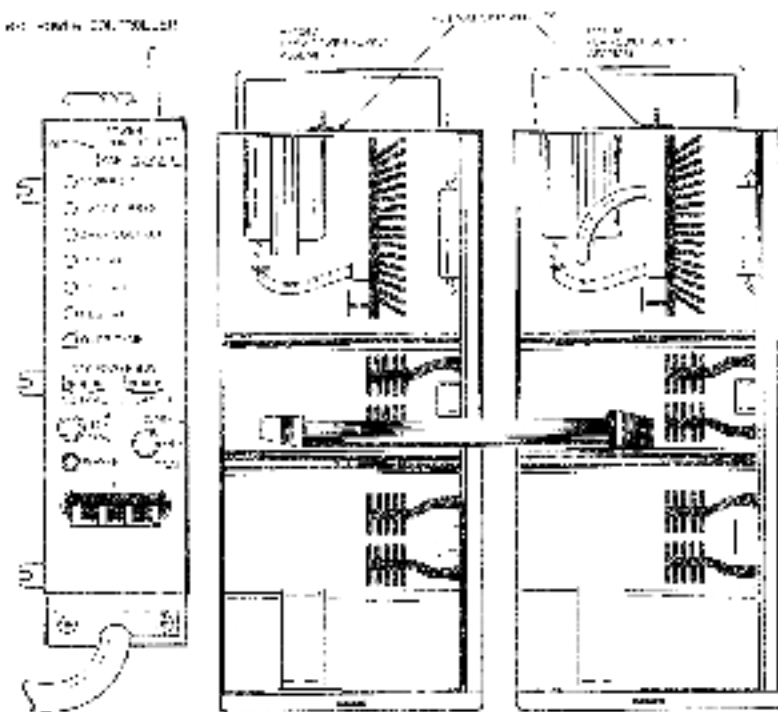


706

VAX-11/750 POWER SYSTEM (CONT.)

VAX-11/750 POWER SUPPLY, PART 2

FIG. 1-10. MAIN CONTROLLER



VAX-11/750 POWER SYSTEM (CONT)

The AC power controller panel consists of eight indicators, one circuit breaker, one REMOTE/LOCAL selector, and 11 switches (10 on the AC and one on the DIGITAL power bus controller).

AC POWER CONTROLLER PANEL

Indicator	Definition
AC ON	The green AC ON indicator is on when the power system is functioning normally. It is off if any fault indicator is on in the power supply system.
OVERCURRENT	The red OVERCURRENT indicator is on when there is an overcurrent condition in the 12.5 V or 5 V power supply. The affected power supply is indicated by the fault indicator being on.
OVERCURRENT	The red OVERCURRENT indicator is on when there is an overcurrent condition in the +2.5 V or +7 V power supply. The affected power supply is indicated by the fault indicator being on.
-5 V FAIL	The red -5 V FAIL indicator is on when there is a malfunction in the -5 V power supply.
+12.5 V FAIL	The red +12.5 V FAIL indicator is on when there is a malfunction in the 12.5 V power supply.
+5 V FAIL	The red +5 V FAIL indicator is on when there is a malfunction in the +5 V, +12 V, or +7-12 V power supply.
OVER TEMP	The green OVER TEMP indicator is on when there is an overtemperature condition in the -5 V or +12.5 V power supply. The indicator is on only, however, when the system is shut down by an overtemperature condition due to the controller.
FAULT	The POWER indicator is on when the controller is plugged into a live AC power source. It is an indicator that is on or off.

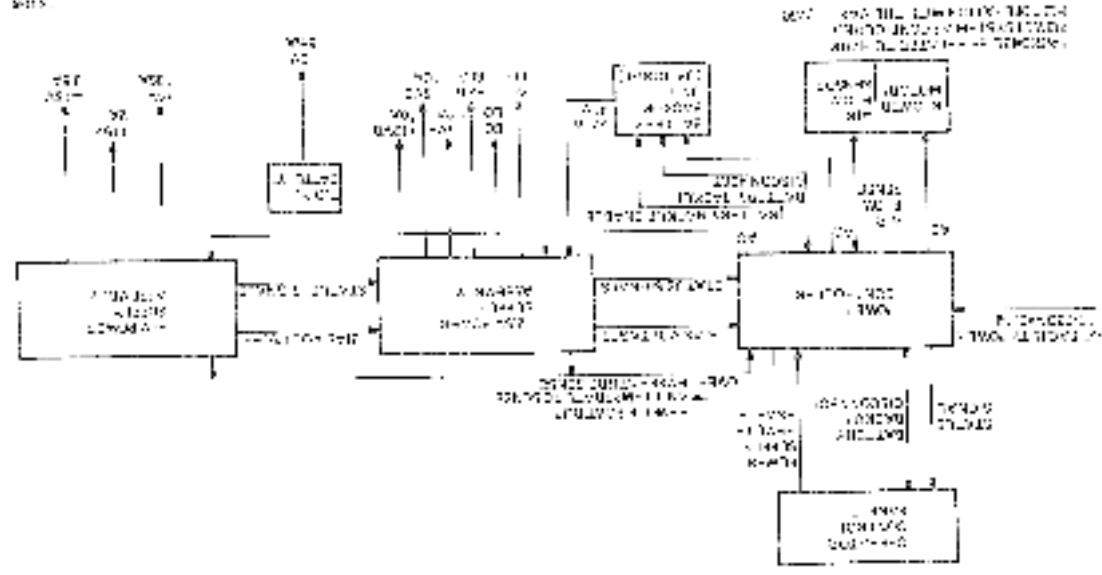
VAX-11/750 POWER SYSTEM (CONT)

REMOTE/LOCAL SWITCH

Position	Definition
REMOTE	This is the normal operating position. An external AC power is applied to the power bus. Whether AC power is controlled by the key-operated switch on the front panel.
OFF	No external AC power can be applied to the system.
LOCAL	Selected AC power is applied to the system regardless of the position of the AC power switch.
CIRCUIT BREAKER (CB)	CB is the main circuit breaker to the power supply system. When in the ON position, unfiltered AC power is applied to the power bus and whether AC power is determined by the position of the REMOTE/LOCAL switch. When in the OFF position, AC power cannot be applied to the power bus.
DC POWER BUS	There are two 240VAC power bus conductors: neutral and ground. Each conductor provides a signal to REMOTE signal bus and is inter-connected between the 110V power system and remote power systems. There is a half-second delay on AC power bus conductors supply CB.

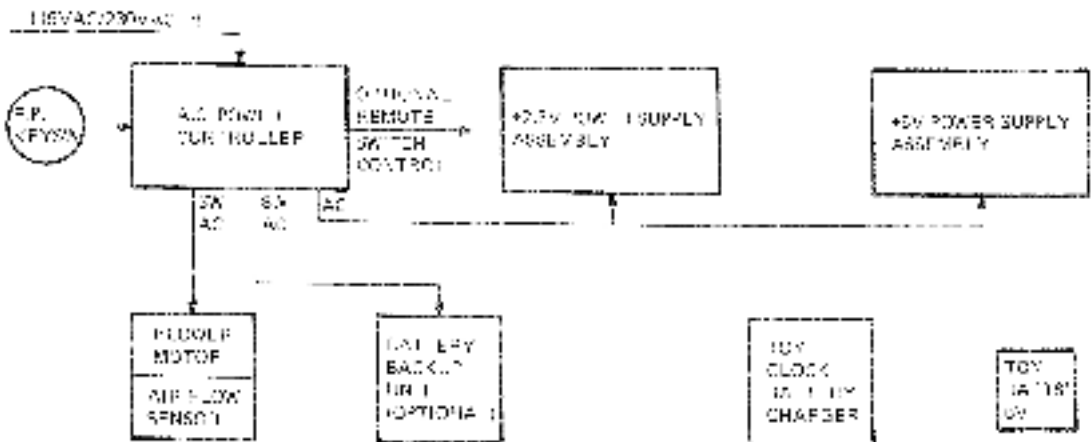
VAX-11/750 POWER SYSTEM (CONT)

HYPER POWER SYSTEM BLOCK DIAGRAM



VAX-11/750 POWER SYSTEM (CONT)

AC POWER DISTRIBUTION



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VAX-11/750 POWER SYSTEM (CONT.)

DC POWER DISTRIBUTION

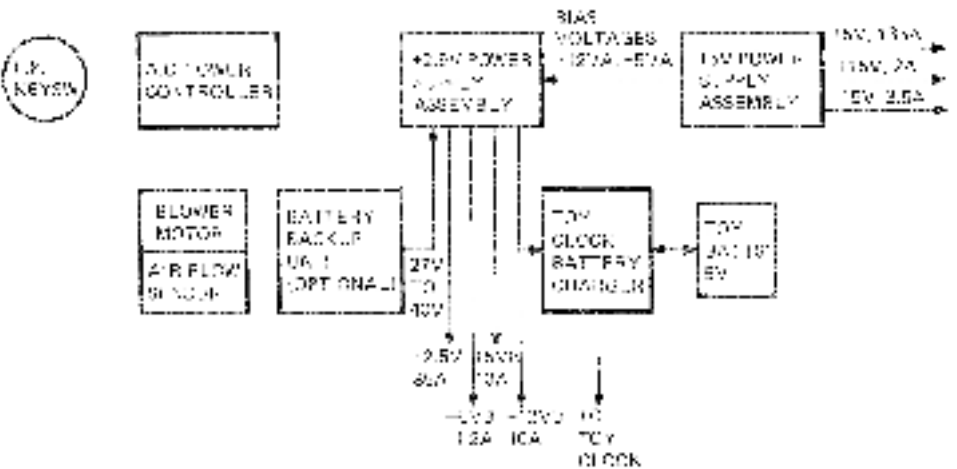
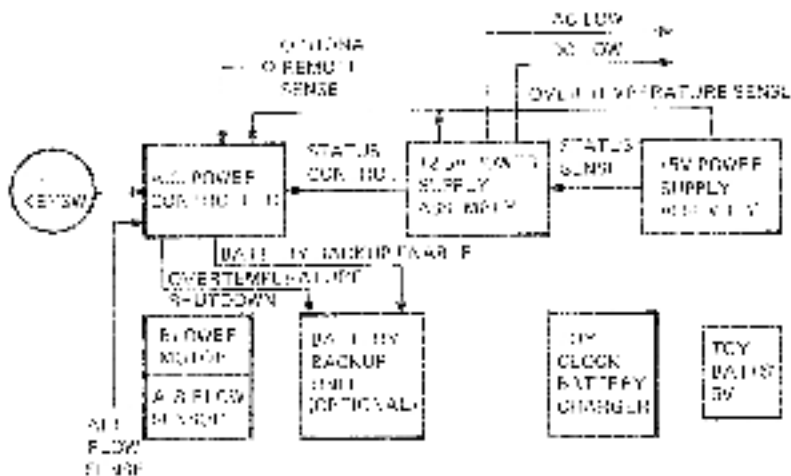


Fig. 1

(V. KEYSW)

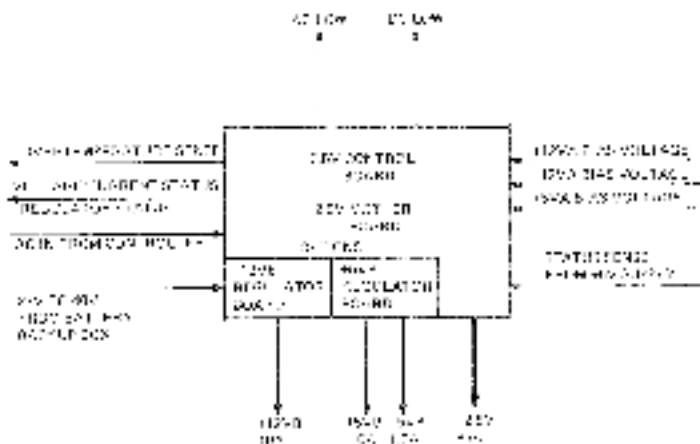
VAX-11/750 POWER SYSTEM (CONT)

POWER SYSTEM SENSING



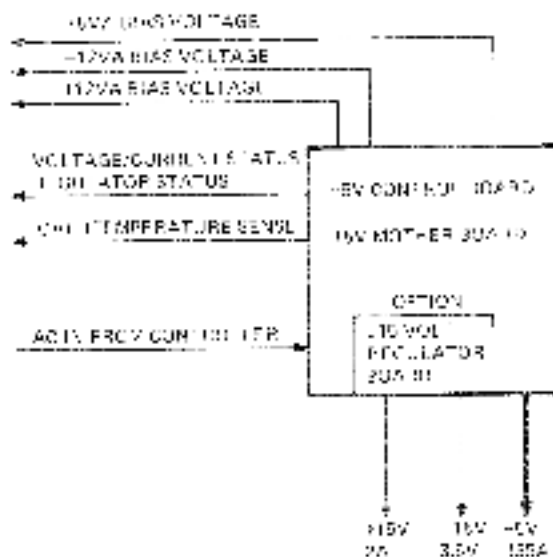
VAX-11/750 POWER SYSTEM (CONT)

42.5 V POWER SUPPLY BLOCK DIAGRAM



VAX-11/750 POWER SYSTEM (CONT)

-5 V POWER SUPPLY BLOCK DIAGRAM



11-474

VAX-11/750 POWER SYSTEM (CONT)

APPLYING SYSTEM POWER

Use the following procedure to initially apply power to the system.

1. Ensure that the CPU's main circuit breaker (CB) and the ac power controller is off (down).
2. Verify that the two percent voltage switch on the power supply unit is in the center position (up).
3. Place the FRENCH/LOCAL switch on the ac power control in Panel 1, the LOCAL position. The CPU power key lock switch on the front panel should be in the off position.
4. Connect the CB circuit or power cable to the external ac power source. The power down indicator on the ac power controller should now be on.
5. Move the CB circuit breaker to the on position (up).
6. Power can now be applied to the CPU by the key lock system on the top front panel.

CPU CABINET POWER REQUIREMENTS

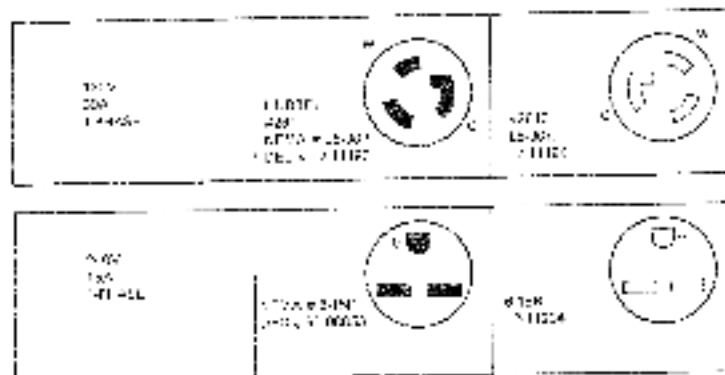
Single phase	Maximal	Minimal	Optimal
VAC (RMS)	120	98	128
Phase to ground	120	98	128
Phase to ground*	120	98	128
Neutral to ground	0/A	0/A	0/A
Harix	60	57	54
Harix	58	57	57
Current (amperes)			15.2 A at 50 Hz
Vac (RMS)	240	198	256
Phase to ground	240	198	256
Phase to ground*	240	197	256
Neutral to ground	0/A	0/A	0/A
Harix	60	57	53
Harix	58	57	53
Current (amperes)			2.5 A at 108 Vac

CAPTION

Separation required with separate power cables must be provided when the same ac line phase as the CPU or Charge may result to the equipment. Also, systems that are interconnected by cables and share the same logic and/or chassis grounding must share the same phase.

VAX-11/750 POWER SYSTEM (CONT)

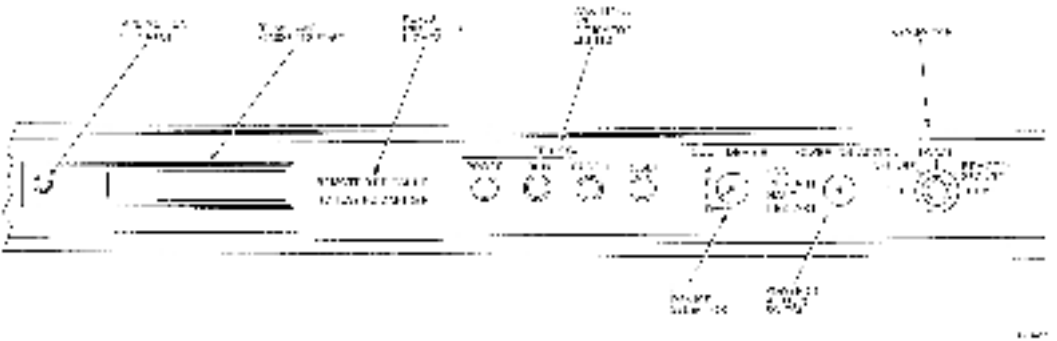
STANDARD POWER PLUGS AND RECEPTACLES



CHAPTER 5
BOOTSTRAPPING AND OPERATION



MAX 11750 FRONT PANEL



VAX-11/750 FRONT PANEL (CONT)

CONSOLE PANEL INDICATORS

Indicator	Description
POWER	Indicates that the console subsystem is supplied with normal voltage. On a VAX-11/750 processor, you have partial power and still have the ARP and allow diagnostic testing.
DISK	The CPU is in program mode, running a user memory sequence.
POWER	Green display to indicate a control store (COS or MCS) parity error. Failure of this device is double control store parity error and CPU clock stopped.
ARSTN Switch	Pressing the ARSTN switch causes the system to perform the action selected by the POWER or STOPPED switch. Press ARSTN and proceed.
TRNTRF S	Lower key switch is in the TRNTRF or TRNTRF STOPPED position.
RD PWRUP	CPU has a failure. Enable for store has seconds time to enable power-up as part of logic self-test.
RD 1187	Bus lock condition is performing self-test.
RD 11811A	External signal detected from CPU.
RD 11811B	Ready to start a search or search, allowing addresses a read or write to be accepted.

VAX-11/750 FRONT PANEL (CONT)

CONSOLE SWITCH FUNCTIONS

Position	Description
Power Key (Default)	
OFF	Switched on power is removed from the system. Restoration of power is still applied.
LOCAL	Normal operation. All power is applied and the console controls the system from the console. Operator mode - The operator utilizes console commands. Program mode - The operator can interact with the system program. CTRL/C and CTRL/D are not passed to the system program but are recognized by the console software.
LOCAL SECURE	Normal operation as for LOCAL except as follows: Operator mode - The local terminal and the RESET switch are disabled. Program mode - CTRL/C and CTRL/D are ignored by the console software and are passed to the system program.
REMOTE	System responds only to the console terminal and to a remote RESET or CTRL/D to abort program errors.
REMOTE SECURE	System responds only to the console terminal and remote CTRL/C or CTRL/D are passed to the system program. The console operator can enable the remote RESET store to terminate calls with the local operator.

VAX-11/750 FRONT PANEL (CONT)

CONSOLE SWITCH FUNCTIONS (CONT)

operator Description

MODE or Action Switch

STOP The console subsystem performs a check up before clearing the console and displaying a panel entry, or when the RESET switch is pressed. The test is performed from the device selected by the BOOT DEVICE SWITCH.

RESTART/BOOT On a power fail, usually, the CPU attempts to initialize resources needed for a valid program parameter block (PAB). If the bus is valid, the program returns to its previous operating state. If not, the system performs a bootstrap sequence from the device selected by the BOOT DEVICE SWITCH.

PAUSE The program fails and no action is accepted.

RESTART/PAUSE A request is attempted as for RESTART. If unsuccessful, however, the program fails.

BOOT DEVICE SWITCH (Physical Device)

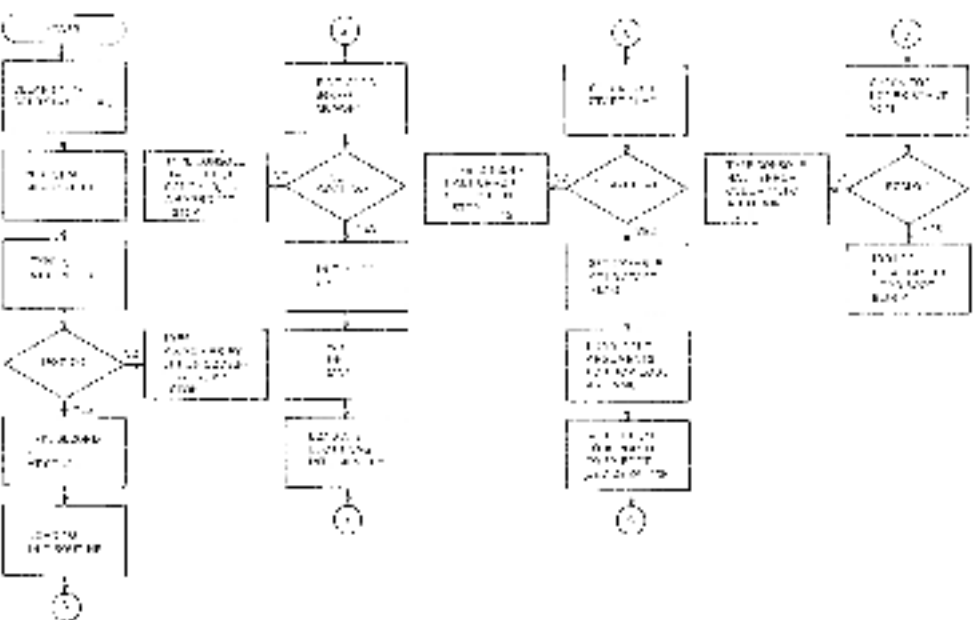
Device A Disk boot ROM

Device B System Disk Boot ROM (DB - PARALLEL, DR - SERIAL)

Device C Alternate Disk Boot ROM

Device D Spare

CONSOLE SUBSYSTEM ACTION ON A ROOT



BOOTSTRAP SEQUENCE

The following steps are required to obtain a running system on a VAX-11/750 processor.

1. The operator powers up the VAX 11/750 system.
2. The VAX 11/750 microcode decoder powers up and follows the power-on strategy described in the BOOTSTRAP microcode block located at the processor system board.
 - a. If the microcode decoder performs a correct, it will perform a bootstrap from the default address to be 11.
 - b. If the decoder fails, the microcode program enters control state program.
 - 1) Issue the console command (11) to the console terminal.
 - 2) Through interactive commands to bootstrap the source by means of the console including control of a user-supplied bootstrap device.
3. The microcode program looks up and executes the bootstrap device read-only memory (ROM). This ROM is 156 bytes and contains a valid routine for the entry and a bootstrap. The valid routine reads bytes 0 from the bootstrap device and jumps to the last valid entry. The valid routine sets the last block in line and the ROM current to read arbitrary blocks from the bootstrap device into memory.
4. The last block containing the logical block address, time, and entry address of the program to be executed in the bootstrap process. This program can be either 1) user-supplied bootstrap, when the bootstrap device is the user's device, or 2) VMS ROM, when the bootstrap device is the source disk.
 - a. If the bootstrap operation is performed from the console VMS ROM code using standard BOOTP, the user must enter BOOTP commands to set the console input device and to load and start VMS ROM.
 - b. If the bootstrap operation is performed directly from the source disk using VMS ROM, the microcode program locates and executes input device.

BOOTSTRAP SEQUENCE (CONT)

5. **VMIBOX** is the primary bootstrap program. It contains CPU independent code and CPU dependent routines. It also contains a set of primitive and interrupt-driven routines for all possible system devices and a detailed file system for loading and linking of user programs level 1 and bootstrap level 2 files. **VMIBOX** performs the following steps:
 - a. Reads the required system and user values calculated from the required entries in the startup parameter block (SPB).
 - b. Reads the system identifiability routines to determine the processor type and to select the table of appropriate processor dependent data and control data.
 - c. Enters into the control and pattern of memory. A page frame number (PFN) array is constructed. On one unit (by a boot flag), memory is sorted for primary, nonallocable parity errors. **VMIBOX** constructs, in the SPB, a table indexed by user number of all memory controllers and for address errors.
 - d. Based on register values, one of the following occurs:
 - (1) A boot block of the designated system is not further used; will be sent into memory and given control.
 - (2) A file named `[SYSTEM]SYSDISK.PRM` will be read into memory and given control.
 - (3) A file named `[SYSTEM]CPU.PRM` will be read into memory and given control.
 - (4) A file specified by the user in response to a request will be read into memory and given control.
6. **VMIBOX** is the standard secondary bootstrap program. It performs initial loading routines for the program administrator. **VMIBOX** performs the following steps:
 - a. Loads current authorized bootflag from `SYSDISK`.
 - b. Loads up the bootstrap device driver file and system information about it.
 - c. The register or one or two disks, prompts the user to specify current system parameters next step. The user can change the start-up routine procedure name and modify system parameters using `SET` or a previously created parameter file. New parameters override the "current" parameters on the next bootstrap operation.
 - d. Sets up SPB, `VMIBOX`, `OS`, and `OSV` into their frame.
 - e. Reads the control routine into high address memory.
 - f. Loads and transfers to level code.

SOOTSTRAP SEQUENCE (CONT)

7. The system initialization program consists of four stages: BOOT, SWSRSTW, SWSRSTWDS, and SWSRSTWDS2000.

a. SW is part of SWSRSTW. It performs the following:

- (1) Tests SW mapping and sets the SW to system space
 - (2) Prints the system initialization message
 - (3) If requested by name of the local file, stops at the ADDRESS breakpoint
 - (4) Terminates the system SW program
 - (5) Allocates available physical page (PPN) strings set up by SWSR to the file page list
 - (6) Initializes the system page table for paged and contiguous blocks
 - (7) Initializes I/O requests using the list of present channels generated by SWSRSTW. To this function, control is made of adapted register space (only the number of pages within a channel is supported) and at the channel specific requests to allocate and set up data structures and to initialize the adapted hardware. To initialize the BEWDS adapters, the 80 byte 120 page of the SWSRDS is mapped.
- SWK structures allocated are:
- SWSRSTW - adapted control block
 - channel request block
 - channel description block
 - BEWDS - channel control block
- (8) Forwards all channel requests with SWK to SWKs
 - (9) Converts the selected SWSRSTW system device list into a page set and uses the 40 user entry and local device reorganization routines as a result of the list reorganization address in the BEW.

BOOTSTRAP SEQUENCE (CONT)

- 1.00 Load the CPU dependent code into the nonpaged pool and link it into the system.
- 1.01 Link the bootstrap loader into expanded pool and reformat the interrupt vectors, load the drivers in use for the system disk into nonpaged pool, connect the interrupt vectors, and format the rest of the system disk. The path for the system disk device name is as follows:
- | | |
|-------------|---|
| device name | indicates the primitive driver, where the device name is stored. |
| controller | the controller designation in "00", "01", or "02" for the floppy, hard, or hard controller of this kind of adapter. For example, 02 the number of the system device in the system address, the number for is 01, note that for a generally non-floppy system, it is possible to use the ADDRESSABLE system primitive to direct the controller to name incompatibly with I/O. Therefore, some may be required when modifying 001- for a controller of possible system disk across multiple system. |
| unit | Number from 000.000 to 000.999.999. |
- 1.02 Add the location of the present drivers into memory 000.000 to the address table.
- 1.03 Perform initialization of system drivers.
- 1.04 Show memory table code of CPU into the pool and execute it. The bootstrap code deallocate space occupied by initial options by GORSEN to the free memory list. The memory table then turns to the next one, until it reaches the end of INITIAL being mapped to the stack.

BOOTSTRAP SEQUENCE (CONT)

6. `BOOT` performs the following:
 - 1) If necessary or requested, prompts for the time of day
 - 2) Writes back system partition to `93,1&8`
 - 3) Creates some input names
 - 4) Sets up swapping and locking files
 - 5) Checks the `MS3-17` BIOS image and system version. If in an upgrade space situation
 - 6) Mounts the system disk (JCR process omitted)
 - 7) Creates the job controller, `SYCOP`, and `CRIBIT`
 - 8) Creates the `STARTUP` process
7. `STARTUP` reads input (and the `STARTUP` command procedure, which caused it to run)
 - 1) Creates logical names
 - 2) Run `SYSDISKCHK93320` to configure the I/O system
 - 3) Checks known images
 - 4) Loads `PARAMS` `SYSTEM`, `CON`
 - 5) `exit`
8. `SYSTEM` is run by `STARTUP` or, if by other user, `SYSCONS`
 - a. Programs for dynamic loading of new controllers to `CRIBIT`, (use operators, `mt`), and various devices are permanently part of the operating kernel
 - b. provides for a specified set of new parameter files that have an attached manual
 - c. handles paging, swapping, and source code files

BOOTSTRAP SEQUENCE (CONT)

INPUT ARGUMENTS

Five general registers receive the following input arguments from the console subsystem.

- R1 = word address of a KASPER address (KASPER address specified in the BOOT command).
- R2 = page address of the CRTDIS file page overlaid with the CONTROL address (CRDIS address and device specified in the BOOT command).
- R3 = device file number to which address specified in the BOOT command.
- R4 = software disk control block (BLOCKS structure specified in the BOOT command).
- R5 = device address + 16384 on the 512K level of quad memory.

BOOTSTRAP SEQUENCE (CONT)

SOFTWARE BOOT CONTROL FLAGS

Flag	Hex Value	Function
1	B/71	Transfer control to the loader. The loader transfers to a new beginning of disk partition.
	B/72	Default. This flag is passed through to SMP and means the user or the manufacturer designer to be included in the transfer system.
2	B/74	Initial breakpoint. If this flag is set, and the executive debugger code is included (L21) L21.0, a breakpoint will occur immediately after executive code loading begins.
3	B/78	Not used on the VAX-11/750.
4	B/7A	Diagnostic mode. This flag causes a loop by the user for the diagnostic supervisor.
5	B/7B	Execution breakpoint. This flag means the bootstrap to stop at a breakpoint after performing necessary initial actions.
6	B/7D	Image header. This flag is used to transfer address from the image header of the boot file will be used. Otherwise, control will transfer to the first byte of the boot file.
7	B/7E	Emergency inhibit. This flag inhibits the loading of memory during bootstrapping.
8	B/7F	File name. Causes the bootstrap to utilize the name of the boot file.
9	B/700	File before transfer. Causes a file instruction to be executed before transfer to the secondary boot file. This option is useful for debugging.

SD B/10 Dev:

```

> SYSBOOT > SET STATE "run" & B/1000000000
        (e.g. disk & console)

```

```

SYSBOOT > CONT (continue) to boot vms

```

B/10 Dev: B/1000000000 in SYSBOOT.CMD in B/1000000000
 B/1000000000 in SYSBOOT.CMD in B/1000000000

SD B/1000 Dev:

```

FILENAME: SYSBOOT.CMD
DATE: 1981-11-13

```

```

Boot image instruction
should be: 00000000
to a system file (e.g.
SYSBOOT.CMD

```

BOOTSTRAP SEQUENCE (CONT)

VOID PRIMARY BOOT FAILURES

boot is the device name for the disk.
The list indicates a fatal error and the type of error is reported.

STATUS: disknot present	Indicates that the CPU is not a 900 1/2719 or 900 1/2720. Check the disk type of word, OS module is 900.
STATUS: unexpected exception	Indicates that one of the following exceptions occurred: <ol style="list-style-type: none">1. access violation2. breakpoint on code3. breakpoint on data4. illegal trap5. page fault error
STATUS: illegal register used in check	Indicates that a register check occurred. Check if registers being used in REXXME and EBP68Y commands. I/O can't be used.
STATUS: concurrent disks	Both top section check boot program) and on-line system disk is being used.
STATUS: unable to write boot file	The error code [10000] (SYSTEM) or [10001] in the boot file, and cannot find [SYSTEM] or [SYSTEM].
STATUS: boot file not available	Indicates that [SYSTEM] or [SYSTEM] is not available on device disk. Check or rebuild.
STATUS: I/O error reading boot file	Indicates a physical reading error. File from disk by boot device (OS module error).

CONSOLE COMMANDS

Command	Description														
CMR,CF	Enter console mode, issues OK prompt.														
CMR,CD	Enter ROM console mode, issues ROM prompt.														
CMR	Exits console mode.														
CMR,?	Displays command														
ROMS: * (CMR) (FILE) (SIZE) (ADDRESS) (TYPE) (NAME)															
@ (FILE) (TYPE) (SIZE) (ADDRESS) (TYPE) (NAME)															
CMR,CMR:	<table border="0"> <tr> <td>/A</td> <td>See size to type</td> </tr> <tr> <td>/B</td> <td>See size to type</td> </tr> <tr> <td>/C</td> <td>See size to address</td> </tr> <tr> <td>/D</td> <td>Physical address space</td> </tr> <tr> <td>/E</td> <td>Virtual address space</td> </tr> <tr> <td>/F</td> <td>File name</td> </tr> <tr> <td>/G</td> <td>ROM type</td> </tr> </table>	/A	See size to type	/B	See size to type	/C	See size to address	/D	Physical address space	/E	Virtual address space	/F	File name	/G	ROM type
/A	See size to type														
/B	See size to type														
/C	See size to address														
/D	Physical address space														
/E	Virtual address space														
/F	File name														
/G	ROM type														
Address: CMR:	The number of physical or virtual address														
CMR:	File address														
<CMR>	next address (repeat only)														
<CMR>	OK														
CMR	Processor halt command														
CMR	Processor initialize command; invalidates read control, issues addresses INT0 and INT00 INT1.														
CMR	Task command; runs microcontroller routine.														
CMR, CMR:	Start command; performs initialize functions, starts specified hex address to run all static program there.														
CMR, CMR:	Task command; performs initialize functions and starts program at address contents of the PC.														
CMR	Continue command; starts program at current contents of the PC without initializing function.														
CMR	Single-step the program while the PC is loaded.														
CMR	Stop command; stops the device as entered by front panel device control.														

CONSOLE COMMANDS (CONT)

FORMAT Description

FORMAT

= [QUALIFIER] [S,] [MODE] [OFF]

QUALIFIER:	/x	Initial condition of microassembly.
	/bus number	Address bus channel (max 16).
	/s	Serial
	/	Adapter code
	/	Unit number

Examples:

xxxx /OFF	Each device specified by MODE.
xxxx/x 1070	Bus 1070 on adapter specified by DEPT and Initial microassembly.
xxxx/s /OFF	xxxx has serial bus adapter to its own bus. Initial adapter on 1070.
xxxx/x/x 1 1070	Channel 1070 in PU.
xxxx/x 1070 /S10-41P	Serial channel on code in 1070.
xxxx/s 1 27	Channel number of adapter.
xxx	Perform processor initialization.
xxxx/x/x /OFF	Reset diagnostic supervisor from DEPT, without adapter.

xxxx Perform additional commands requested for use by manufacturing or selected test device (MODE) that communicates with the console to transfer data between itself and memory.

Binary Load:

xxxxxxx [ADDRESS] [COUNT] [ADDRESS] [COUNT] [STRING]

ADDRESS	Starting address of the load
COUNT	Number of bytes to be transferred (maximum 64K) hex number, with 0 for a serial load complement operation of the channel string
STRING	String of binary data
COUNT	Serial complement checksum on the data

Binary Store:

xxxxxxx [ADDRESS] [COUNT] [ADDRESS] [COUNT]

ADDRESS	Starting address of the store
COUNT	Number of bytes to be transferred (assigned 00 via hex number, all else hex * only)
COUNT	Serial complement checksum of the channel string

CONSOLE COMMANDS (CONT)

CONSOLE COMMAND ERROR CODES

Code	Description
020	Memory expand or deposit failed: address violation (A20), address error not valid (A20), machine check, bus error, OS parity error, OS/390 parity error.
021	Error in command (PR or RPL)
022	Checks in error on API load or unload
023	Attempt to boot from unauthorized device (DR, DR, DR, or DR)
024	Controller not A, B, C, or D in boot sequence

CONSOLE HALT CODES

Code	Description
H	User console command executed
H0	CP/CPA halt at single machine execution code (2200)
H4	Interrupt error not valid
H5	Double bus error error 0x -
H7	Program halt: instruction executed (0x02)
H8	Warm start = 1, halt at device
H9	Warm start = 0, halt disabled or not present
H9	Change code: instruction executed on interrupt start
H9	Change code: instruction executed, variable check not = 4

BOOT, POWER-UP, AND INITIALIZATION HALT CODES

Code	Description
00	Halt instruction on console boot command, halt 000, or 00000000 failed
01	Power-up error: first CPU, CPU or 000000000000
02	Power-up error: start flag failed 0000 or 000000000000
03	Power up, console first code 0000 or 000000
04	Power up 000 failed, not an emergency console boot
05	Power up, halt start flag not during local boot/online
06	Power-up halt CPU to halt position
07	Microcode load failed

08: not valid

CONSOLE COMMANDS (CONT)

MICROVERIFY ERROR CODES

Code	9740	2000	Reason/Reason Message
9741	980	981	980: MDRS read 981: MDRS read in MDRS of MDRS
9742	982	983	982: MDRS read 983: MDRS read in MDRS
9743	984	985	984: MDRS read in MDRS 985: MDRS read in MDRS
9744	986	987	986: MDRS read in MDRS 987: MDRS read in MDRS
9745	988	989	988: MDRS read in MDRS 989: MDRS read in MDRS
9746	990	991	990: MDRS read in MDRS 991: MDRS read in MDRS
9747	992	993	992: MDRS read in MDRS 993: MDRS read in MDRS
9748	994	995	994: MDRS read in MDRS 995: MDRS read in MDRS
9749	996	997	996: MDRS read in MDRS 997: MDRS read in MDRS
9750	998	999	998: MDRS read in MDRS 999: MDRS read in MDRS
9751	1000	1001	1000: MDRS read in MDRS 1001: MDRS read in MDRS
9752	1002	1003	1002: MDRS read in MDRS 1003: MDRS read in MDRS
9753	1004	1005	1004: MDRS read in MDRS 1005: MDRS read in MDRS
9754	1006	1007	1006: MDRS read in MDRS 1007: MDRS read in MDRS
9755	1008	1009	1008: MDRS read in MDRS 1009: MDRS read in MDRS
9756	1010	1011	1010: MDRS read in MDRS 1011: MDRS read in MDRS
9757	1012	1013	1012: MDRS read in MDRS 1013: MDRS read in MDRS
9758	1014	1015	1014: MDRS read in MDRS 1015: MDRS read in MDRS
9759	1016	1017	1016: MDRS read in MDRS 1017: MDRS read in MDRS
9760	1018	1019	1018: MDRS read in MDRS 1019: MDRS read in MDRS
9761	1020	1021	1020: MDRS read in MDRS 1021: MDRS read in MDRS
9762	1022	1023	1022: MDRS read in MDRS 1023: MDRS read in MDRS
9763	1024	1025	1024: MDRS read in MDRS 1025: MDRS read in MDRS
9764	1026	1027	1026: MDRS read in MDRS 1027: MDRS read in MDRS
9765	1028	1029	1028: MDRS read in MDRS 1029: MDRS read in MDRS
9766	1030	1031	1030: MDRS read in MDRS 1031: MDRS read in MDRS
9767	1032	1033	1032: MDRS read in MDRS 1033: MDRS read in MDRS
9768	1034	1035	1034: MDRS read in MDRS 1035: MDRS read in MDRS
9769	1036	1037	1036: MDRS read in MDRS 1037: MDRS read in MDRS
9770	1038	1039	1038: MDRS read in MDRS 1039: MDRS read in MDRS
9771	1040	1041	1040: MDRS read in MDRS 1041: MDRS read in MDRS
9772	1042	1043	1042: MDRS read in MDRS 1043: MDRS read in MDRS
9773	1044	1045	1044: MDRS read in MDRS 1045: MDRS read in MDRS
9774	1046	1047	1046: MDRS read in MDRS 1047: MDRS read in MDRS
9775	1048	1049	1048: MDRS read in MDRS 1049: MDRS read in MDRS
9776	1050	1051	1050: MDRS read in MDRS 1051: MDRS read in MDRS
9777	1052	1053	1052: MDRS read in MDRS 1053: MDRS read in MDRS
9778	1054	1055	1054: MDRS read in MDRS 1055: MDRS read in MDRS
9779	1056	1057	1056: MDRS read in MDRS 1057: MDRS read in MDRS
9780	1058	1059	1058: MDRS read in MDRS 1059: MDRS read in MDRS
9781	1060	1061	1060: MDRS read in MDRS 1061: MDRS read in MDRS
9782	1062	1063	1062: MDRS read in MDRS 1063: MDRS read in MDRS
9783	1064	1065	1064: MDRS read in MDRS 1065: MDRS read in MDRS
9784	1066	1067	1066: MDRS read in MDRS 1067: MDRS read in MDRS
9785	1068	1069	1068: MDRS read in MDRS 1069: MDRS read in MDRS
9786	1070	1071	1070: MDRS read in MDRS 1071: MDRS read in MDRS
9787	1072	1073	1072: MDRS read in MDRS 1073: MDRS read in MDRS
9788	1074	1075	1074: MDRS read in MDRS 1075: MDRS read in MDRS
9789	1076	1077	1076: MDRS read in MDRS 1077: MDRS read in MDRS
9790	1078	1079	1078: MDRS read in MDRS 1079: MDRS read in MDRS
9791	1080	1081	1080: MDRS read in MDRS 1081: MDRS read in MDRS
9792	1082	1083	1082: MDRS read in MDRS 1083: MDRS read in MDRS
9793	1084	1085	1084: MDRS read in MDRS 1085: MDRS read in MDRS
9794	1086	1087	1086: MDRS read in MDRS 1087: MDRS read in MDRS
9795	1088	1089	1088: MDRS read in MDRS 1089: MDRS read in MDRS
9796	1090	1091	1090: MDRS read in MDRS 1091: MDRS read in MDRS
9797	1092	1093	1092: MDRS read in MDRS 1093: MDRS read in MDRS
9798	1094	1095	1094: MDRS read in MDRS 1095: MDRS read in MDRS
9799	1096	1097	1096: MDRS read in MDRS 1097: MDRS read in MDRS
9800	1098	1099	1098: MDRS read in MDRS 1099: MDRS read in MDRS

CONSOLE COMMANDS (CONT)

MICROVERIFY ERROR CODES (CONT)

Code	PG#	Test Name/Block Message
101		AS/IR/CSR bit test
	0P1	Block in AS 3180
	0P2	Block in AS 3181
	0P3	Block in AS
	0P4	Block in CSR
102		Source address increment test
	111	Block containing one beta byte, no
	112	other containing 2 bytes from EP or
		incrementing by 1
	114	Block containing an unaligned instruction
		or incrementing by 2
	117	Block incrementing by 4
103		RMP/D-IRK test
	121	Block loading DSRM ROM address 1
	122	Block loading/loading ROMM
	124	Block loading DSRM ROM address 2
	127	Block loading/loading ROMM
	128	Block loading DSRM ROM address 1
	129	Block loading/loading ROMM
	130	Block loading DSRM ROM address 4
	131	Block loading/loading ROMM
104		BRX/DIRK test continued
	141	Block loading DSRM ROM address 1
	142	Block loading/loading ROMM
	144	Block loading DSRM ROM address 4
105		Cache parity error test
	151	Failed to get cache parity error
	152	off machine check error primary register
	153	and cache check register
106		IR parity error test
	161	Failed to get group 0 IR parity error
	162	Bad IR group parity error register
	164	Bad machine check error primary register
	165	Failed to get group 1 IR parity error
	166	Bad IR group parity error register
	167	Bad machine check error primary register
107		Control store parity error test
	171	Failed to get control store parity error
	172	from in control store parity error
108		Cache test
	181	Block filling cache with zeros
		Load/store test initially 1-4
	182	Block filling cache with zeros
		Double the write size

BC0158 COMMANDS

The following lists descriptions of the commands that can be entered to the translation source program. They are listed in alphabetical order.

BOOT

!([device-name])

Reboot the system from the specified device. If you omit the device name, the system is booted using the default bootable system procedure (HDPBOJCPD). Note that you cannot enter the BOOT command procedure to the BOOT board unless you manually modify this command within a command procedure.

DEPOSIT

!([length],[size],[location value])

Deposit a value in the specified location. The location is interpreted according to the location and size qualifiers. The location qualifier can be specified as follows:

- !G general register
- !T internal processor register
- !R physical memory

The size qualifiers can be specified as follows:

- !b byte
- !w word
- !l longword

If you do not specify the location and size qualifiers, the default values established by a previous command are used.

BOOTER COMMANDS (CONT)

EXAMINE

EX *nn-qual,addr-ptr* *n* *location*

Display the contents of the specified location. The location is interpreted according to the location and size qualifiers; the location qualifier can be expressed as follows:

/R general register
/A address pointer register
/P physical address

The size qualifier can be expressed as follows:

/B byte
/W word
/L longword

If you do not specify any location and size qualifiers, the default values established by a previous command are used.

HELP

Press any key to get help files at the console terminal. You cannot qualify this command with a command procedure.

LOAD

LO *file-spec* [*ADDRESS*]

Loads a file from the bootstrap device into memory, starting at the address specified with the *ADDRESS* qualifier. If you omit the *ADDRESS* qualifier, the file is loaded into memory beginning at the first 128K address.

START

S *value*

Transfer control to the value specified. You generally use this command with the LOB command.

@file-spec

Qualifies the name of the command procedure specified. You cannot qualify a command procedure file-spec if you then use *ADDRESS*, but you can specify initial command procedure.

CHAPTER 6
RDM AND MICRODIAGNOSTICS



RDM INSTALLATION

RDM HARDWARE

The following hardware is supplied with the indicated IBM options:

Option	Hardware (and serial)	Group
RC704-01	ROM module (L2005) Error handling module Diagnostic kit VLSI serial interface cable (78-16521) Voice interface module (RC704-21) RC704 options rack module (22-RC704-01)	100
RC704-02	ROM module (L2005) Diagnostic kit VLSI serial interface cable (78-16521) Voice interface rack module (22-RC704-01) (Module 201 not supplied by customer)	100/101

PREINSTALLATION

The following steps must take place before installation of the RDM:

1. The customer's service configuration must be established and a system cost estimate worksheet supplied to the District Diagnostic Center (DDC).
2. The customer must bring and furnish the telephone company with the following information on the system to be used:
 - a. Model number
 - b. Manufacture's name
 - c. Ring modulation circuit
 - d. Toll registration number
 - e. Voice bank direct connect type description
 - f. Telephone number or time/line or study facts that may be supplied by the DDCM district office.

ROM INSTALLATION (CONT)

INSTALLATION PROCEDURE

The following is the procedure for installing the ROM module and hardware.

1. Perform an orderly shutdown of the operating system. When power down the system by turning the console power key switch to OFF.
2. The ROM module is supplied with the correct user band code set to 367 based by jumpers on the module. Further includes LED a dipswitch in the location presently occupied by the jumpers.

The band code is selected by jumpers M0, M1, M2, M3, M4, M5 by switch positions B107-1 through 41 as shown below.

In setup, move jumper M-7 on the opposite end of the module from the B107 B108 jumpers.

Band Code	M0 or B107-1	M1 or B107-2	M2 or B107-3	M3 or B107-4
373	On	On	Off	On
429	Off	On	Off	On
623	On	Off	Off	On
1,204	Off	Off	Off	On
2,198	On	On	On	Off
3,584	Off	On	On	Off
7,288	On	Off	On	Off
6,296	Off	Off	On	Off
7,288	On	On	Off	Off
8,180	Off	On	Off	Off
19,282	On	Off	Off	Off

3. Install the L2628 module in slot 6 of the expanded bus controller.

Refer to the ROM and ROM module illustrations for the next steps.

4. On the pin side of the CPU backplane, carefully remove the following cables from the left side of slot 6 (odd numbered slots on the right side of slot 7 (even numbered pins), away from the main vertical plane out):
 - a. Left panel cable from M
 - b. HW cable from S
 - c. Console cable from C

CAUTION

Make sure there are two open pins between the module holes and the mainline board edge plugs.

RPM INSTALLATION (CONT)

5. Plug the IBM 61-based cable assembly (IBM 8021) into the socket 12 (pin 17 on the left side of slot 6). Attach the assembly to the backland of that pin 1 is on top and pin 22 is on the bottom (see 826-93).

CAUTION

When installing this cable, be sure that it is connected properly and that the two bottom pins 200-91 and 205-91 are left disconnected.

6. Attach the filtered power assembly to the I/O port panel using the 6-32 screws provided with the cover plate.
7. Attach the power tag around the filtered cable using the wire strap and tighten it to provide support of the tag.
8. Plug the power cable into the IBM filtered cable connector in the I/O port panel and secure.
9. Remove the system cable as necessary and connect it to the nodes. Use 0.75 volt or 1.5 volt (depending on) that requires 1.15 amp power source.

CAUTION

Never do power plug any more from the VAX-11/750 internal power distribution system. This violation of regulations and cabinet power integrity.

INSTALLATION VERIFICATION

Use the following procedure to verify RPM installation.

1. Perform diagnostic software and program tests.
2. Power up the system by turning the power device switch to A, the power-on action switch to ON/OFF, and the power key switch to 200V.
3. Observe the RPM power-up self test. When power-up, the fault indicator should turn on for about ten seconds. Inspect the installation if the fault indicator does not turn on or does not turn off, or if there is no console message of error message with the test, RPM, or RPM code. If the installation is correct, remove the RPM. Install another RPM or return the cables to their original position.

ROM INSTALLATION (CONT)

1. The power of the IC switches, the console terminal printing the following:

```

* *
87902780 16
???
```

1. Perform the ROM installation tests described later in this chapter yourself or ask the ROM technicians to perform an installation verification.
2. For console heating by the ROM, turn the console power key switch to OFF.
3. Check with the DDC from the console terminal or by telephone for results of the verification.

ROM REMOVAL

Removing the ROM is the reverse of the installation procedure. If removal is necessary, only installation steps 1 through 4 need to be performed in reverse. The power cables and connectors are left in place.

CAUTION

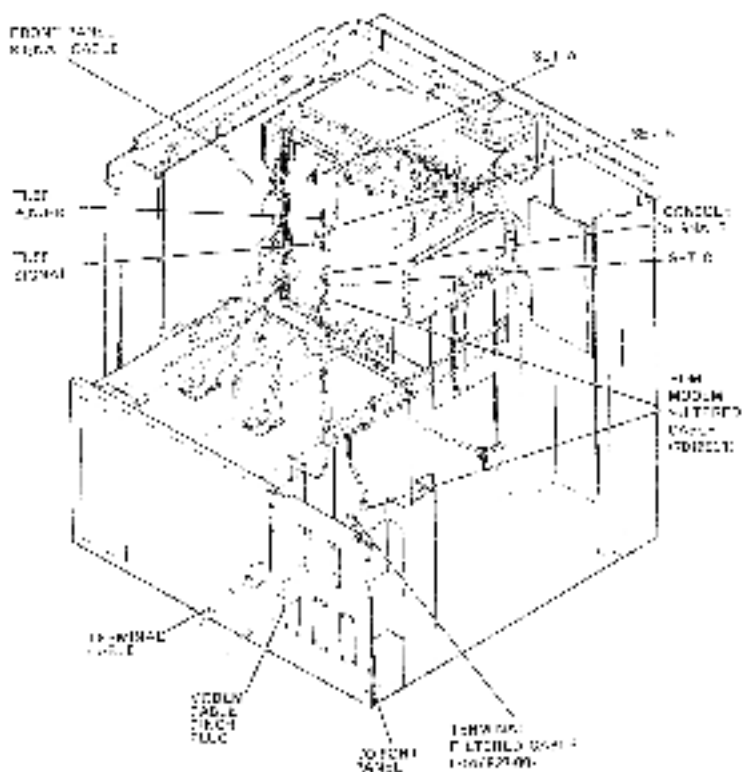
Always power down the system before installing or removing the ROM.

INSTALLATION OUTSIDE THE UNITED STATES

DAICOM does not provide factory with ROM options outside the United States. The shipping practices and procedures of a given country must be followed to obtain a ROM there. Refer to the ROM98 Option Installation Guide (TM-37077-TM) for specifications on modern FASC with ROM.

RDM INSTALLATION (CONT)

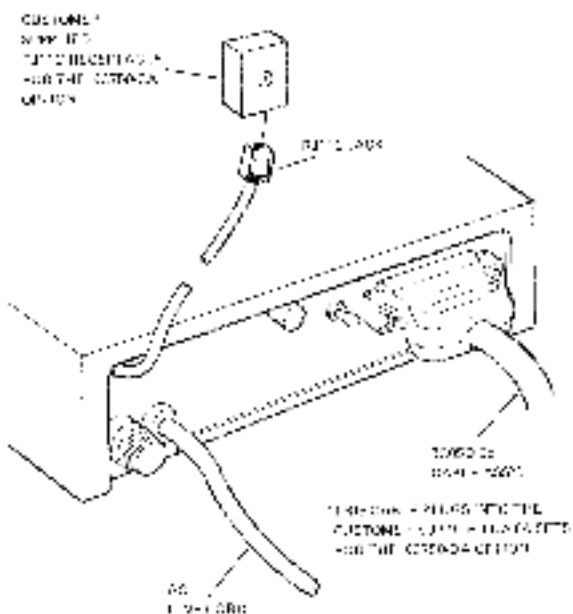
RDM CABLING



7-0173

HDM INSTALLATION (CONT)

MODEM CABLING



10/10/00

RDM INSTALLATION (CONT)

HDM/MODEM SIGNALS

REF Pin	IR 15921 (RDM) Conn. Pin	EIA (RS232-C) Signal Name	EIA Ref.	DM Circuit
CR011	1	Receive Data	RD	RA
CR012	2	Signal Ground	SG	AG
CR013	3	Transmitted Data	TD	TA
CR014	4	Received Data	RD	RA
CR015	5	Request to Send	RS	TA
CR016	6	Clear to Send	CS	CA
CR017	7	Data Set Ready	DSR	DR
CR018	8	Data Terminal Ready	DTDR	DA
CR019	9	Ring Indicator	RI	RA
CR020	10	Carrier Detect	CD	CA
CR021	11 (Unused)	Transmit Enable	TE	TA

SELECTED CPU BACKPLANE SIGNALS

Pin	Signal Name
CR022	Ground
CR023	RDM Internal Serial Out to CPU serial in
CR024	RDM Internal Serial In to CPU serial out
CR025	Control hand shake 1
CR026	Control hand shake 2
CR027	Control hand shake 3
CR028	Control hand shake 4
CR029	Control hand shake 5
CR030	Control hand shake 6
CR031	Control hand shake 7
CR032	Control hand shake 8
CR033	Control hand shake 9
CR034	Control hand shake 10
CR035	Control hand shake 11
CR036	Control hand shake 12
CR037	Control hand shake 13
CR038	Control hand shake 14
CR039	Control hand shake 15
CR040	Control hand shake 16
CR041	Control hand shake 17
CR042	Control hand shake 18
CR043	Control hand shake 19
CR044	Control hand shake 20
CR045	Control hand shake 21
CR046	Control hand shake 22
CR047	Control hand shake 23
CR048	Control hand shake 24
CR049	Control hand shake 25
CR050	Control hand shake 26
CR051	Control hand shake 27
CR052	Control hand shake 28
CR053	Control hand shake 29
CR054	Control hand shake 30
CR055	Control hand shake 31
CR056	Control hand shake 32
CR057	Control hand shake 33
CR058	Control hand shake 34
CR059	Control hand shake 35
CR060	Control hand shake 36
CR061	Control hand shake 37
CR062	Control hand shake 38
CR063	Control hand shake 39
CR064	Control hand shake 40
CR065	Control hand shake 41
CR066	Control hand shake 42
CR067	Control hand shake 43
CR068	Control hand shake 44
CR069	Control hand shake 45
CR070	Control hand shake 46
CR071	Control hand shake 47
CR072	Control hand shake 48
CR073	Control hand shake 49
CR074	Control hand shake 50
CR075	Control hand shake 51
CR076	Control hand shake 52
CR077	Control hand shake 53
CR078	Control hand shake 54
CR079	Control hand shake 55
CR080	Control hand shake 56
CR081	Control hand shake 57
CR082	Control hand shake 58
CR083	Control hand shake 59
CR084	Control hand shake 60
CR085	Control hand shake 61
CR086	Control hand shake 62
CR087	Control hand shake 63
CR088	Control hand shake 64
CR089	Control hand shake 65
CR090	Control hand shake 66
CR091	Control hand shake 67
CR092	Control hand shake 68
CR093	Control hand shake 69
CR094	Control hand shake 70
CR095	Control hand shake 71
CR096	Control hand shake 72
CR097	Control hand shake 73
CR098	Control hand shake 74
CR099	Control hand shake 75
CR100	Control hand shake 76
CR101	Control hand shake 77
CR102	Control hand shake 78
CR103	Control hand shake 79
CR104	Control hand shake 80
CR105	Control hand shake 81
CR106	Control hand shake 82
CR107	Control hand shake 83
CR108	Control hand shake 84
CR109	Control hand shake 85
CR110	Control hand shake 86
CR111	Control hand shake 87
CR112	Control hand shake 88
CR113	Control hand shake 89
CR114	Control hand shake 90
CR115	Control hand shake 91
CR116	Control hand shake 92
CR117	Control hand shake 93
CR118	Control hand shake 94
CR119	Control hand shake 95
CR120	Control hand shake 96
CR121	Control hand shake 97
CR122	Control hand shake 98
CR123	Control hand shake 99
CR124	Control hand shake 100

RDM INSTALLATION TESTS

The following series of tests can be run in the order given.

VAX CPU TEST

To verify CPU operation, after the ROM has been installed, boot the VMS tape into memory and check the status of the following:

```
U/1 25 100RT>
100RT>
```

Cache is flushed and the CPU status indicates that the CPU should allow an entry on the bus to be initiated while EISA is loaded. The diagnostic runs repeatedly until it is stopped by CTRL/C. The following messages summarize the procedure.

```
0000/1 25 100RT>
0000/1 25
4>

EYKKA - 4.8 done!
EYKKA - 4.8 done!
0000/1
0128 done 07
000
```

In this it shows a status for some number. The EYKKA diagnostic should run at least twice before being stopped. CTRL/C may have to be typed more than once to stop EYKKA.

Next, use the VAX firmware to write and read back data with VAX memory locations. Type the following to see the results:

```
0000/1 25 100RT>
0000 + 000000000000
0000 + 000000000000
0000 + 000000000000
0000 + 000000000000
0000 + 000000000000
0000 + 000000000000
```

Next, type the following to see the memory:

```
0000 00000000      F      00000000      00000000
000000000000      F      00000000      00000000
000000000000      F      00000000      00000000
000000000000      F      00000000      00000000
000000000000      F      00000000      00000000
000000000000      F      00000000      00000000
000000000000      F      00000000      00000000
```

If the results look good, you may wish to copy the data. The test can be run.

RDM INSTALLATION TESTS (CONT)

VAX MEMORY BUS TEST

This test verifies the ability of the RDM hardware to read and write data into VAX memory. (The VAX CPU user manual is the correct data format.)

At the first level, data enter the RAM console state is follows.

```
SYNCHRONIZE
WIDE
```

Reading VAX memory.

```

RDM> READS
RDM> READS          P  80000  2280387
RDM> READS          P  80000  2FF8FF8
RDM> READS          P  00001  8AAAAAA
RDM> READS          P  00000  5555555
RDM> READS (ZERO)   P  20FF0  8148875
RDM> READS         P  00000  87654321
```

Copying to memory.

```

RDM> 8 20FF0 (11111)
RDM> 1 80000
RDM> 3E8L 8AAAAA0000
RDM> 4 0000A00000
```

Reading memory.

```

RDM> 80000
RDM> 80000          P  80280  0FF0111
RDM> 20FF0 (300)   P  82780  0000387
RDM> 80000          P  82FF0  0000555
RDM> 80000          P  81780  8888888
```

To the data read from memory is just the same as data sent to it. In this sense, the test has failed.

RDM INSTALLATION TESTS (CONT)

VAX CONTROL STORE PARITY CHECK

This test examines the REX's ability to know whether the VAX clock is running, to stop the VAX clock, and to check the parity of the VAX control store. (The VAX manual has test 3 should be run before this test.)

If the REX is working properly, it will allow us check VAX control store parity while the VAX clock is running. To order to see if the REX can detect the VAX clock, ask it to do a parity check while the VAX clock is running.

```
REX>PRT>STOP
      CLS
      REX>
```

Check that the REX can stop the VAX clock.

```
REX>STOP>STOP
      CPU STOPPED LEAD 8966      REX 8966
```

In this dialog, 0 stands for zero output.

Now test the REX's ability to check the VAX control store parity. The error has been masked at microaddress 127D.

```
RDM>PARITY CHECK LEAD 127D
      REX>
```

If any parity address appears in the response, a parity error has been detected in that address of the VAX control store.

MICROBREAK POINT AND TRACE

This test examines the REX's logic test stops the VAX clock when the REX executes the microinstruction at a preset microaddress called the microbreak point. The test also examines the REX's ability to store VAX control store addresses. A trace is listing of the DR addresses of the last 25 microinstructions executed, or the extent of their execution. (The VAX manual says parity errors should be run before this test.)

First, initialize the CPU to trace.

```
RDM>RST>RST>
      #
      REX>80/88 TO
      #
      REX>80/88 TO
      REX>
```

RDM INSTALLATION TESTS (CONT)

set the interrupter pin:

```
ADDRESS 3200000
RST
```

This interrupter pin happens to be the address of the CPU's carriage return microinstruction. When the CPU sees a carriage value, the RDM's will then stop the CPU clock.

Return to the RDM control panel. The CPU clock's carriage returns in the program.

```
ADDRESS 32000
OFF 320000 0000 0000 0000 0000
```

Move to the next hexadecimal number and RST, indicating the address of the next microinstruction to be executed.

Just check that the RDM does a carriage return every time.

```
ADDRESS 32000
```

DATA	DATA	DATA 32000
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	
0000	0000	

Since the interrupter was used to display in the loop, the loop value display will be zero. It should be a combination of address 3200000, RDM's pin, and a carriage return microinstruction. number 3200000 is the address of the next microinstruction to be executed.

Just check the address of the loop microinstruction is executed (32000) is the address of the carriage return microinstruction. For address 32000 and RDM, the loop is set to RDM's pin and a carriage return.

RDM INSTALLATION TESTS (CONT)

MICRODIAGNOSTIC RUN TEST

The test RDM appears to come from a microdiagnostic ROM on the VAX. It will be located at the next time the system is in the RDM mode unless the microdiagnostic ROM is in the data path with RDP or microdiagnostic ROM. About the only hope with this program is to use some panels. The following dialogue is how the microdiagnostic tests RDP memory and run it below.

```
READY TO RUN
PLEASE WAIT
EPCBA-002-00 RDP-011-00
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20,
02, 03, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30,
END OF DATA 01

RDM TEST 01
01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20,
02, 03, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30,
END OF TEST 01

UNDETECTABLE
RDM
```

Note that the RDM prompt is displayed when the system is in the microdiagnostic state.

If the program is not the same as it's just given and the test has been performed previously, replace the ROM with a spare. If a spare is not available, remove the existing ROM and return the hardware table to the original condition.

ROM COMMANDS (CONT)

ROM CONTROL KEY FUNCTIONS

Key	Description
CTRL/D	Enter ROM control command mode
CTRL/R	Toggle ROM control mode and red
CTRL/J	Abort current command line
CTRL/L	Insert 8 characters during line editing
CTRL/O	Retype current command line
CTRL/P	Control current function while ROM is in command
CTRL/S	Display CPU status to screen terminal
CTRL/Z	Display CPU status to screen terminal

ROM CONSOLE COMMANDS

Command	Function
ADDR#	Execute - uses the following command switches: D# ADDRESS# Data size is byte W# ADDRESS# Data size is word L# ADDRESS# Data size is longword E# ADDRESS# Execute ROM status registers and add ADDRESS# in the range of 0000 0000 /N# Toggle next address /P Execute previous address D# Load data last executed or repeated in the address
BRND#	Repeat - uses the following command switches: D# ADDRESS# <DATA> Data size is byte W# ADDRESS# <DATA> Data size is word L# ADDRESS# <DATA> Data size is longword R# Repeat data in next address P = <DATA> Repeat data in previous address E# <DATA> Load data last executed or repeated in the address
BRK#L#	Initialize - initializes a user-defined memory to memory BR, load a user-defined memory ADDR and hold signals. (P# is used with a register to implement user-defined memory problems.)
FLSR#	Return - switches system from ROM control mode to CPU program mode. Stop-on-exception. If on, it disables.
RNDRST#	Reset - switches system from ROM control mode to ROM control mode. Resets to at least level of the memory bus. CPU program mode, control for the system. CPU program mode whether the CPU is running or not. Stop-on-exception. If on, remains enabled.

RDM COMMANDS (CONT)

RDM CONSOLE COMMANDS (CONT)

COMMAND	FUNCTION
ROBATA	ON/OFF - enables data paths between local and remote terminal during an RD session.
RTSTAT	show - displays 8085 CPU operating status.
STATSTAT	show status - displays current real time level of the hardware including in the RDM.
STATUSDP	Repeat - continually repeats last command given until CTRL/C is typed. CTRL/C stops output to terminal.
STATUS COMMANDS	Repeat name - continually repeats specified command until CTRL/C is typed. CTRL/C stops output to the terminal.
STATUS ADDRESS	entry mode - show CPU status, check flag, the specified starting address. Shows all loaded word addresses 16K 12 is user to find. For check must be stopped by a key command, and may be checked by specifying addresses 32K4 ranging 16K 100K over the board when 32K4 4P.
STATUS	stop - shows the clock.
STATUS	stop - stops clock and stops instruction on an RDM clock. Displays address of instruction currently latched in CPU and address of the next instruction.
REPORT / P	16K 12K - addresses of instructions to be in 4 clock ticks. Displays current address latched in CPU and data to be latched in the next 4 clock ticks.
STATUS	clock - controls the CPU clock.
STATUS	stop - displays in register when the current clock addresses stored in the 8K diagnostic control when 100K. CTRL/C or CTRL/D halts display of the loaded addresses. The clock may be stopped by a key command.
STATUS OPERATION	Microaddress - holds the CPU and latches selected microaddress to 16K latches. CPU bus feedback and checks parity on the address data. May be used with program for scope bus. Stop or allow each function to be disabled.

ROM COMMANDS (CONT)

RUN CONSOLE COMMANDS (CONT)

Command	Function
ROM>LPC ADDRESS	Microaddress/PC = temporarily placed selected microaddress to PC address from built-in ROM clock (PC), used to locate hardware in the PC memory location via CPU address bus is not changed. (see PC-internal manual, 1-28), 1-30, 1-31, 1-32.
ROM>E ADDRESS	PC = enables user configuration function. PC is not in address when the PC address bus sends the selected address. The command is then used to force user access to the PC to reach that point in the PC.
ROM>C	Clear = clear system configuration function.
ROM>LPC	Line = user to access external control line to the ROM LAD with the user program. (ROM LAD with file or file control control to access the ROM LAD is given. This line is managed if it is a power bus or if the ROM, ROM, or LAD is returned to given.
ROM>M	memory = memory line bus to be continuously address until ROM LAD is given.
ROM>LPC ADDRESS (ADDRESS)	Line = read the user file data from the PC. If necessary, address the last of the specified address. May be used to read the PC if the user does not have the functionality to do so, or if the file is not properly loaded to an will not block. PC reads only the PC from block to address the last.
ROM>LPC	Line = loads the selected file address. (ADDRESS) user PC in ROM LAD and read data (ADDRESS) from PC. Reading is managed if an error is detected or (ADDRESS) is typed. (ADDRESS) user switches to the command state, saving the PC's program.
ROM>LPC	Configuration = user (ADDRESS) as for the LAD. (ADDRESS) is the command state with the PC (ADDRESS).
ROM>LPC ADDRESS	Line = user (ADDRESS) as for the LAD. (ADDRESS) user PC from PC. The file name and address of the hardware and the file type of user are (ADDRESS).

FOR THE MICROADDRESS

RDM COMMANDS (CONT)

RDM CONSOLE ERROR CODES

Code Description

Tape Functional Errors

TAP:01 Tape LABC - Device filament
 TAP:02 Tape LABC - Error from HART
 TAP:03 Tape LABC - Data not ready dropped
 TAP:04 Tape LABC - Error on operation
 TAP:05 Tape LABC, error received
 TAP:06 Tape LABC name maximum exceeded
 TAP:07 Tape LABC packet (inhibit) operation code
 TAP:08 Tape LABC11 packet received
 TAP:09 Tape file not found
 TAP:10 Tape directory error
 TAP:11 Tape key received (no command or data)
 TAP:12 Tape read length error (not all 1000000 bits)
 TAP:13 Tape bad packet number
 TAP:14 Tape LDC operation code
 TAP:15 Tape error dropped
 TAP:16 Tape filament not found
 TAP:17 Tape data check error
 TAP:18 Tape write protocol error
 TAP:19 Tape cartridge not present
 TAP:20 Tape bad data amount
 TAP:21 Tape partial operation (end of record)
 TAP:22 Tape diagnostic failure

Console terminal errors

TMR:01 Terminal HART - Device filament
 TMR:02 Terminal HART - Error from LABC
 TMR:03 Terminal HART - Data not ready dropped
 TMR:04 Terminal HART - Error on operation
 TMR:05 Terminal HART, error received
 TMR:06 Terminal maximum name buffer exceeded
 TMR:07 Terminal CTRL-D received
 TMR:08 Terminal carriage input longer than buffer
 TMR:09 Terminal receive line CR error

RDM COMMANDS (CONT)

RDM CONSOLE ERROR CODES (CONT)

Code	Description
CPL Errors	
CM1009	Maximum I/O history
CM1011	Paralleled read I/O
CM1012	Read call subscription
General Errors	
ERR008	ERR008
ERR011	Error handling complete message
ERR012	ERR012
ERR013	ERR013
ERR014	ERR014
ERR015	ERR015
ERR016	ERR016
ERR017	ERR017
ERR018	ERR018
ERR019	ERR019
ERR020	ERR020
ERR021	ERR021
ERR022	ERR022
ERR023	ERR023
ERR024	ERR024
ERR025	ERR025
ERR026	ERR026
ERR027	ERR027
ERR028	ERR028
ERR029	ERR029
ERR030	ERR030
ERR031	ERR031
ERR032	ERR032
ERR033	ERR033
ERR034	ERR034
ERR035	ERR035
ERR036	ERR036
ERR037	ERR037
ERR038	ERR038
ERR039	ERR039
ERR040	ERR040
ERR041	ERR041
ERR042	ERR042
ERR043	ERR043
ERR044	ERR044
ERR045	ERR045
ERR046	ERR046
ERR047	ERR047
ERR048	ERR048
ERR049	ERR049
ERR050	ERR050
ERR051	ERR051
ERR052	ERR052
ERR053	ERR053
ERR054	ERR054
ERR055	ERR055
ERR056	ERR056
ERR057	ERR057
ERR058	ERR058
ERR059	ERR059
ERR060	ERR060
ERR061	ERR061
ERR062	ERR062
ERR063	ERR063
ERR064	ERR064
ERR065	ERR065
ERR066	ERR066
ERR067	ERR067
ERR068	ERR068
ERR069	ERR069
ERR070	ERR070
ERR071	ERR071
ERR072	ERR072
ERR073	ERR073
ERR074	ERR074
ERR075	ERR075
ERR076	ERR076
ERR077	ERR077
ERR078	ERR078
ERR079	ERR079
ERR080	ERR080
ERR081	ERR081
ERR082	ERR082
ERR083	ERR083
ERR084	ERR084
ERR085	ERR085
ERR086	ERR086
ERR087	ERR087
ERR088	ERR088
ERR089	ERR089
ERR090	ERR090
ERR091	ERR091
ERR092	ERR092
ERR093	ERR093
ERR094	ERR094
ERR095	ERR095
ERR096	ERR096
ERR097	ERR097
ERR098	ERR098
ERR099	ERR099

VAX-11/750 DIAGNOSTICS

VAX-11/750 Diagnostic programs are available under the following levels of installation:

- Level 1 - VMS operating system based diagnostic programs that can be run without the diagnostic supervisor.
 - disk, see 4.3, 4.7.4.6, 4.8
- Level 2B - Diagnostic supervisor based programs. Only Diagnostic disk is loaded on VMS based disks.
 - Peripheral diagnostics not supported by the supervisor in the shared mode.
 - Level 2 diagnostic control program
- Level 3 - Diagnostic supervisor based programs that can be run on-line under VMS or in the standalone mode.
 - Low level control program
 - Isolated and reliability-based peripheral diagnostics
- Level 4 - Diagnostic supervisor based programs that can only be run in the standalone mode.
 - Isolated level peripheral diagnostic
 - Reliability-based peripheral diagnostics
 - VMS monitor diagnostics
- Level 5 - Standalone control programs that run within the supervisor.
 - Hardware instruction set (tests the basic functions necessary to run the supervisor)
- Level 6 - Console based diagnostics that run only in the standalone mode.
 - Microcode testing
 - Console operating program
 - Microcode program

VAX-11/750 DIAGNOSTICS (CONT)

Device	Part	Qty.	Description	Reference Number
	10000	1	Diagnostic Support Unit	1, 2, 3
	10000	5	Microchannel Support Unit	1, 2
K1170	7000	5	Micro Channel Buffer Module (MBC)	1
	7000	5	Micro Channel Buffer Module (MBC)	1
	7000	4	Cache/Control Buffer Module	1
	7000	7	Micro Channel Transceiver (MBC-1000)	1, 10, 12, 13
K1171	7000	1	Micro Channel Buffer Module	1, 11
	7000	2	Micro Channel Buffer Module	1
	7000	2	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1172	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1173	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1174	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1175	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1176	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1177	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1178	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1179	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1180	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1181	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1182	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1183	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1184	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1185	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1186	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1187	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1188	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1189	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1190	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1191	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1192	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1193	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1194	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1195	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1196	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1197	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1198	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1199	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1
K1200	7000	1	VAX Micro Channel Buffer Module	1
	7000	1	VAX Micro Channel Buffer Module	1

NOTE: Refer to the appropriate VAX diagnostic listing index (D11000) for the complete component list and the associated hardware.

VAX-11/750 DIAGNOSTICS (CONT)

Machine	Model	Level	Description	Err. Cause # Number
0100	70000	2	VAX 7000/00000/0000 Data Reliability	0, 10, 12
	70000	1	VAX 7000/00000 Functional	00
0200	70000	2	VAX 7000/00000/0000 Data Reliability	0, 10, 12
	70000	1	VAX 7000/00000 Functional	0
	70000	1	VAX 7000/00000 Functional	14
0400	70000	2	VAX 7000/00000/0000 Data Reliability	0, 10, 12
	70000	1	VAX 7000/00000 Functional	14
	70000	1	DATA CORRUPT ON	10, 12
	70000	1	VAX 7000/00000 Functional	16
0600	80000	1	VAX 8000/00000/TIME D. C. Reliability	0, 10, 12
	80000	2	VAX 8000/00000 Functional	0
0700	80000	2	VAX 8000/00000/0000 Data Reliability	0
	80000	1	VAX 8000/00000 Functional	20
1000	80000	2	VAX 8000/00000/0000 Data Reliability	0, 10, 12
	80000	2	VAX 8000/00000 Functional	0
	80000	1	8000 Print Bad	0
	80000	1	8000 Error Code	0
	80000	1	8000 Error Code Correction	20
1200	70000	2	VAX 7000/00000/0000 Data Reliability	0, 10, 12
	70000	2	VAX 7000/00000 Functional	0
	70000	1	VAX 7000/00000 Repair	20
1300	70000	2	VAX 7000/00000 Data Reliability	0
	70000	1	VAX 7000/00000 Functional	14
1600	70000	1	VAX 7000/00000 Data Reliability	0
	70000	1	VAX 7000/00000 Control Repair	20
1700	70000	1	VAX 7000/00000 Data Reliability	0
	70000	1	VAX 7000/00000 Functional	14

NOTE: Rows in columns of the diagnostic listing indicate that the error diagnostic occurred and that ADDRESS number.

MICROMONITOR (MICROMON) COMMANDS

Command	Function
MICROM	Release - supplies known MICROM and returns to PCV controls, 20000.
MICMON	Diagnose - performs TPC diagnosis on from the PCV diagnostic control block (DDB).
MICMON TA:CRASH:ADDS:ID	Diagnose - initiates program control flag and starts execution loop of test program in PCV for specified number of passes.
MICMON TA:CRASH:ADDS:ID:OK	Diagnose - OK
MICMON TA:CRASH:ADDS:ID:NOTOK	Diagnose - resources supplied from program or PCV.
MICMON TA:CRASH:ADDS:ID:NOTOK:OK	Diagnose - conditionally releases specified unit until stopped by an error or 200000.
MICMON OK	Diagnose - runs diagnostic routine 200000000.
MICMON	Continue - resumes PCV test of below word of 200000.
MICMON	Loop - sets loop flag and loops until program detected and restarted error.
MICMON CL:OK	set flag - sets specified program control flag.
MICMON CL:NOTOK	clear flag - clears specified program control flag.
MICMON CL	show flags - displays current status of the program control flags.
MICMON V	show vbus - displays current signal status on the availability bus (20000).
MICMON BR:BUS:ADDRESS	OK - execution of bus program at specified address.

MICROMONITOR (MICMON) COMMANDS (CONT)

Command	Function
KL0000 00 00	Steps through UCS internal instructions on a clock cycle.
KL0000 00 01	Steps through CPU internal instructions, stopping before the last P clock cycle or a function of the phase stack.
KL0000 00 02 (STEP/NO)	For each instruction = steps through usable instructions in current block. If step is qualified, step function occurs when the instruction or branch is ready to be executed. If step is not qualified, stepping begins on the next possible instruction of the current block containing a loop (L) or continue (C) command.
KL0000 00 (CPU-ADDRESS)	Clears CPU counter to last address, if specified, immediately stops CPU on last P clock cycle (1000 hex is added to desired address). Also occurs with M mode when the current address matches CPU address.
KL0000 00 (CPU-ADDRESS) (CPU-ADDRESS)	Get current CPU bit - sets specified control bit in the specified CPU address (bits <00-08>).
KL0000 00 (CPU-ADDRESS) (CPU-ADDRESS)	Clears control bit bit - clears specified control bit in the specified CPU address.
KL0000 (REGISTER) 00	
KL0000 (REGISTER) (NUMBER)	Displays the following specified registers:
00	Virtual address register (VAR)
01	Memory address register (MADR)
02	CU program counter (PC)
03	CU link register (LDR)
04-07	Block registers 0 through 7
08-09	MEM registers 0 through 7
0A	Processor status register (PSR)
0B	Memory stack register (MSR)
0C	MEM data register (MDR)
0D-0F	Status and control registers 0 through 3
10	Stack stack
11	Step counter

MICROMONITOR (MICMON): COMMANDS (CONT)

MICROMONITOR PROGRAM CONTROL FLAGS

FLAG	Function
HALT	Hold on error - returns to the monitor on a program detected error.
LOOP	Loop on error - loops on program detected error, also will display the status, the HALT flag when set is cleared and the STOP flag when the maximum loop. The loop may include specific instructions and JCR instructions from the GPRICOP or the GPRPROM instructions in the falling edge of the LS flag is set or a stack-up occurs, the program then set loop on alternate condition in GCR. This will be clear to inhibit error messages.
ERR	No error return - inhibits error messages.
ERRL	Hold on error - error halt on the first, then every fifth occurrence of an error.
LF	Fetch forward - when used with LOOP flag, program does not step over on JCR instructions but loops instead between the ERROR and EXERR pseudo instructions.
QS	Quality assurance - each test reports on if an error was detected.
PR	Print - monitor prints test cases and results.
SA	Signature analysis - when with signature analysis is fully diagnosed results. Loop returns on test to position whether or not an error occurs. Also, provides the type errors on the backplane: Error/stop window, test 6, pin 476 Error pin 481, test 1, pin 171 The signature analyzer analyzes test patterns by displaying a value (signature) if the signal pattern is steady. This value is compared with the value from a known good pattern to make failures.

MICROMONITOR (MICROM) COMMANDS (CONT)

VISIBILITY BUS (VBUS) SIGNALS

File Number (Location)	File Number (Hex)	Signal Name	Port Bus	Bus
06	05	VB023 P0R0R MA PA L	PT011	
06	07	VB023 P0R0R CASH0 PA L	PT011	
06	08	VB023 P0R0R PA0 H	PT011	
06	09	VB023 ST0P 0T0H L	PT011	
06	24	VB024 000P 00R R	VB020	
06	05	VB025 001 00R0 L	VB020	
06	06	VB025 001 00R0B L	PT011	
06	07	VB025 00R 0000 L	PT011	
06	08	VB025 00R00 B R	VB020	
06	09	VB025 00R00 B L	VB020	
06	2A	VB026 0000R 0 T	VB020	
06	2B	VB026 0000R 0 L	VB020	
06	2C	VB026 00R 0T0T 0H L	VB020	
06	2E	VB026 00R00 L	VB020	
06	2E	VB026 00R00R PA00 IN L	VB020	
06	2F	VB026 0000 00T L	VB020	
06	29	VB026 0000 00B L	VB020	
06	2A	VB026 00B 0000L R	VB020	
06	2B	VB026 00R00 0000 L	VB020	
06	2C	VB026 00R00 0000 R	VB020	
06	2D	VB026 00R00 0000 L	VB020	
06	2E	VB026 00R00 0000 R	VB020	
06	2F	VB026 00R00 0000 R	VB020	
06	2A	VB027 00R00 0000 00 L	VB020	
06	2B	VB027 00R00 0000 00 L	VB020	
06	2C	VB027 00R00 0000 00 L	VB020	
06	2D	VB027 00R00 0000 00 L	VB020	
06	2E	VB027 00R00 0000 00 L	VB020	
06	2F	VB027 00R00 0000 00 L	VB020	
06	2A	VB028 00R00 0000 00 L	VB020	
06	2B	VB028 00R00 0000 00 L	VB020	
06	2C	VB028 00R00 0000 00 L	VB020	
06	2D	VB028 00R00 0000 00 L	VB020	
06	2E	VB028 00R00 0000 00 L	VB020	
06	2F	VB028 00R00 0000 00 L	VB020	
06	2A	VB029 00R00 0000 00 L	VB020	
06	2B	VB029 00R00 0000 00 L	VB020	
06	2C	VB029 00R00 0000 00 L	VB020	
06	2D	VB029 00R00 0000 00 L	VB020	
06	2E	VB029 00R00 0000 00 L	VB020	
06	2F	VB029 00R00 0000 00 L	VB020	
06	2A	VB030 00R00 0000 00 L	VB020	
06	2B	VB030 00R00 0000 00 L	VB020	
06	2C	VB030 00R00 0000 00 L	VB020	
06	2D	VB030 00R00 0000 00 L	VB020	
06	2E	VB030 00R00 0000 00 L	VB020	
06	2F	VB030 00R00 0000 00 L	VB020	

CHAPTER 7
BLOCK DIAGRAMS



VAX-11/750 BASIC DIAGRAM

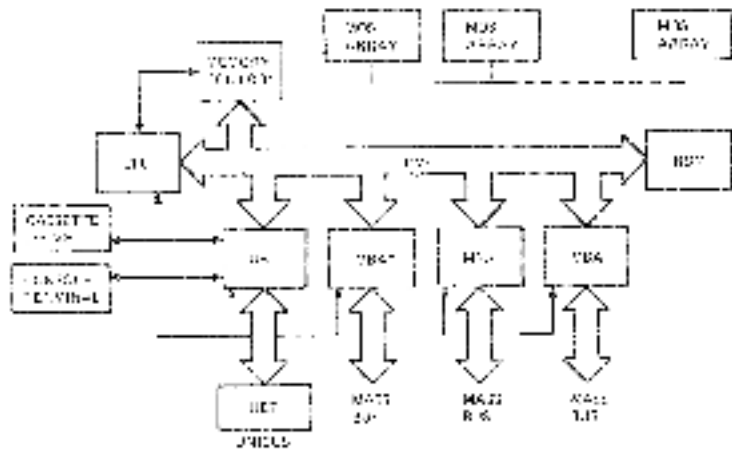
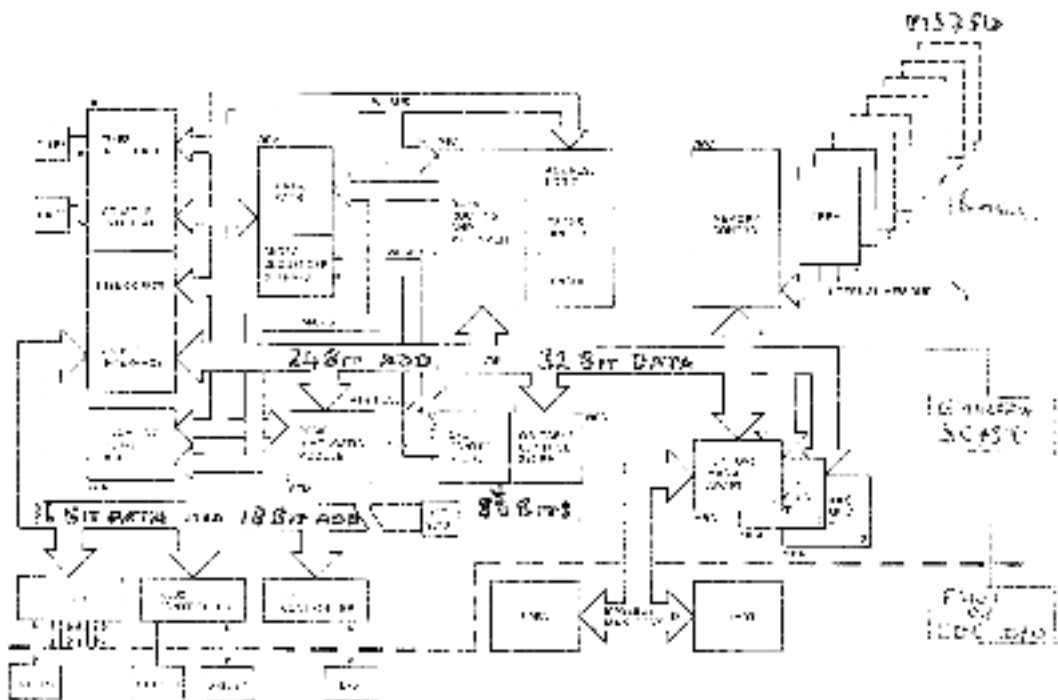
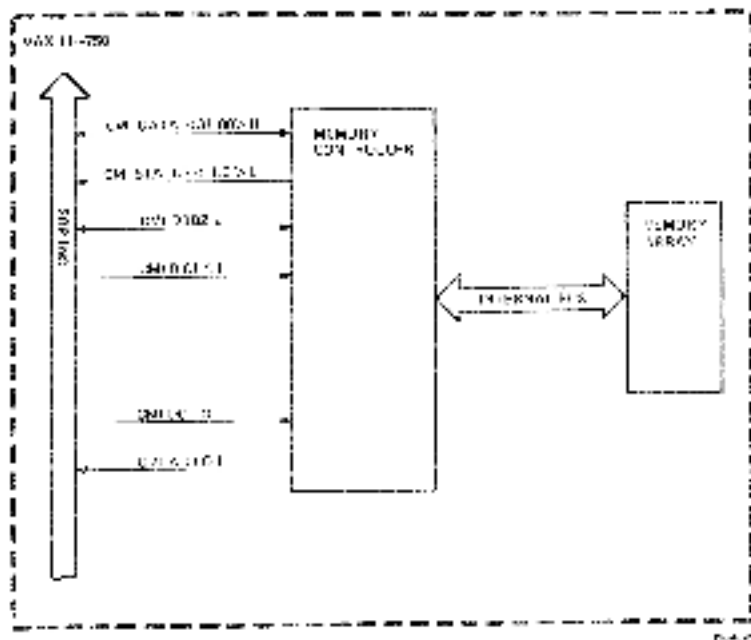


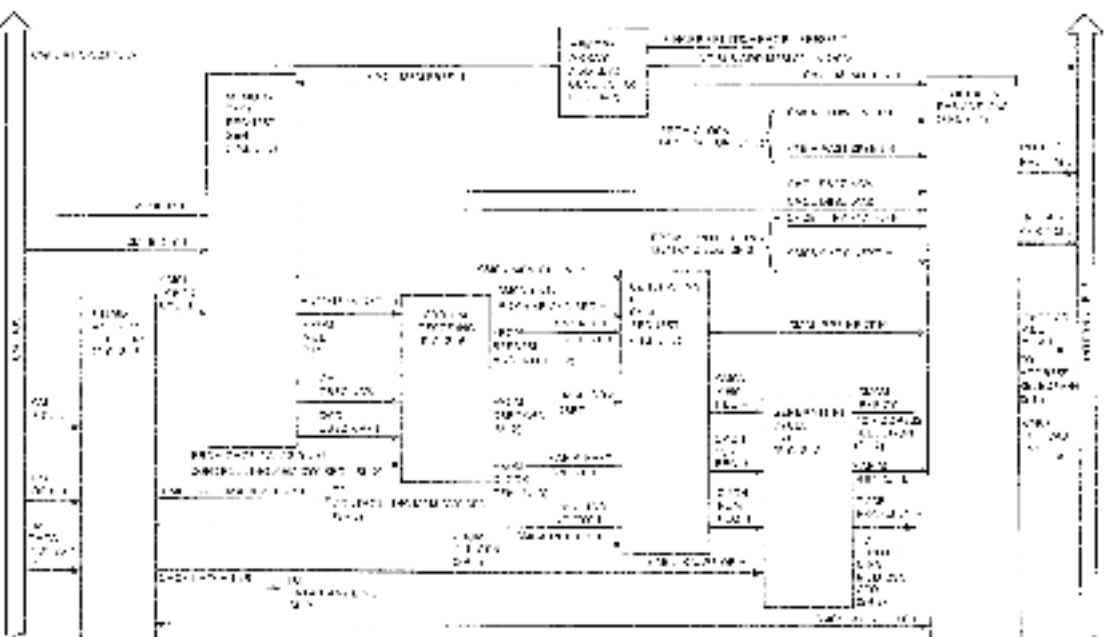
FIGURE 1-10 VAX-11/750 BASIC DIAGRAM

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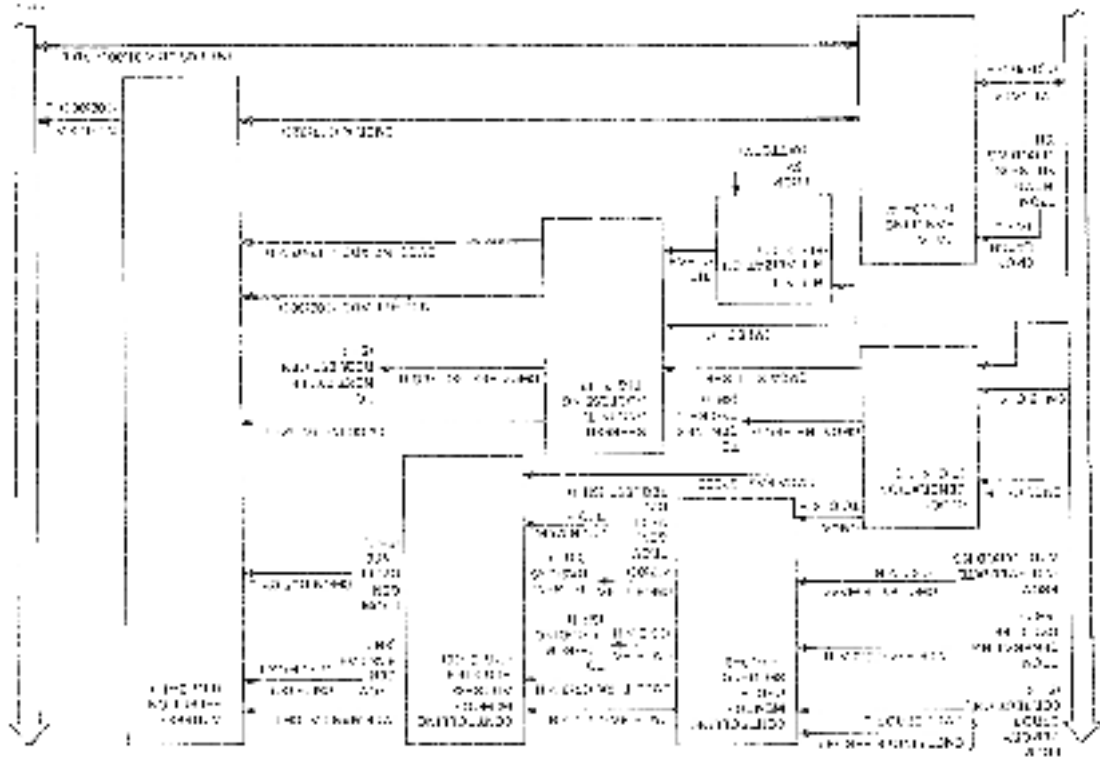


CMC (M575D) BASIC DIAGRAM

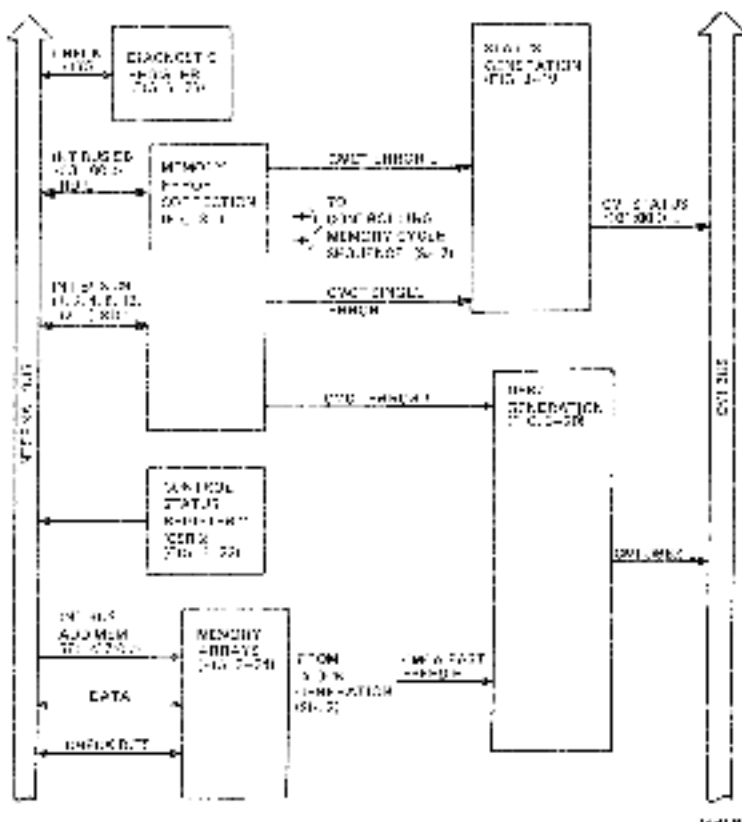




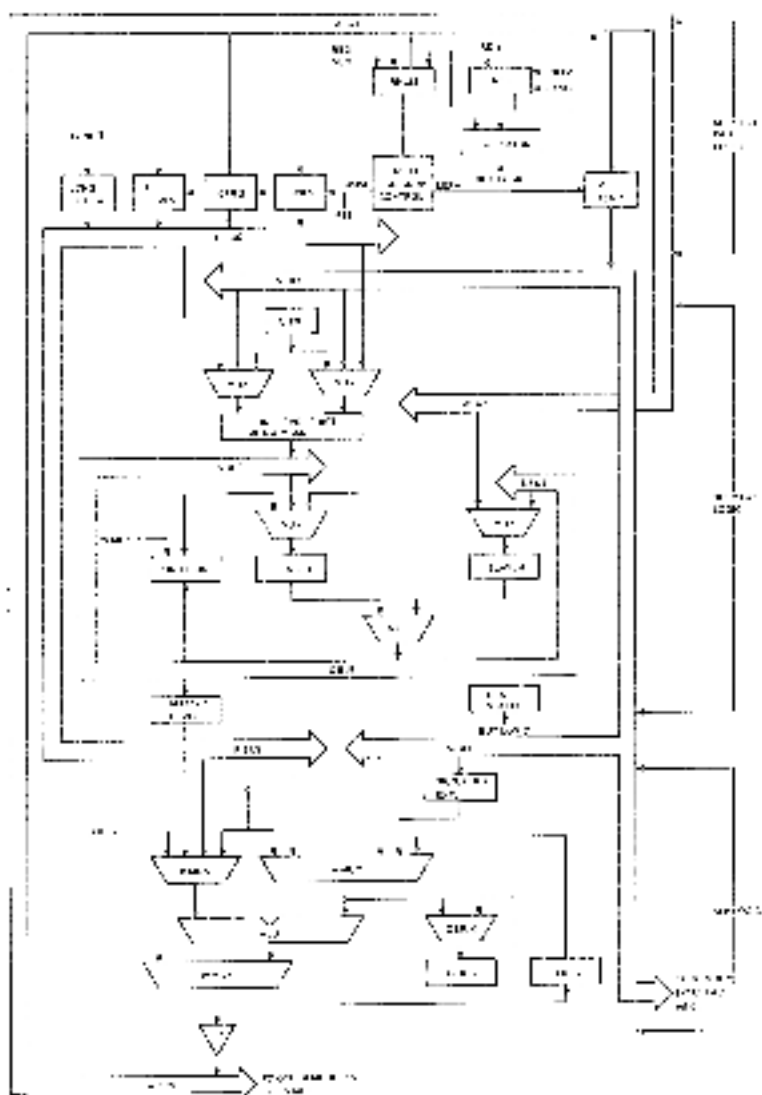
CMC (MS750) BLOCK DIAGRAM, PART 2



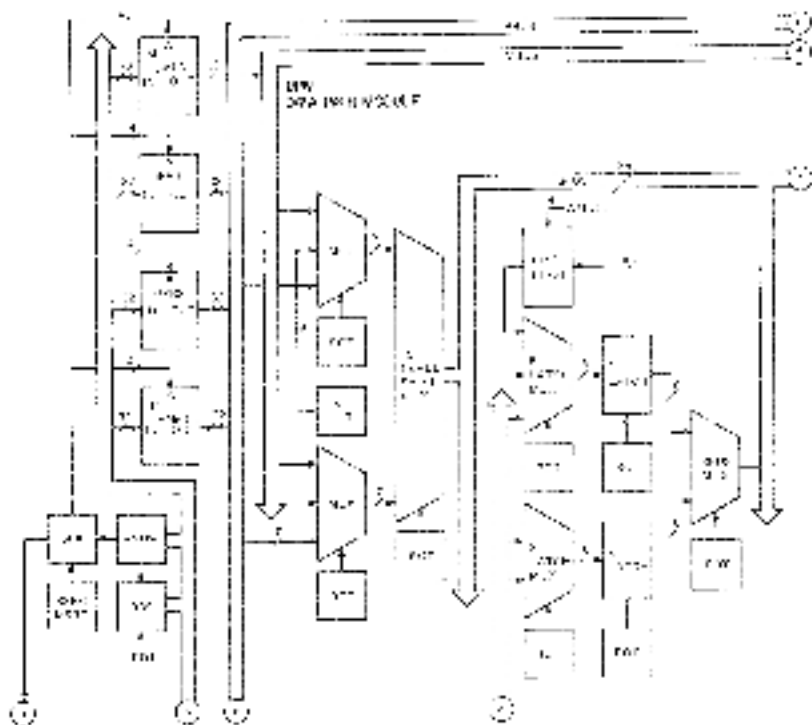
CNC (MS75D) BLOCK DIAGRAM, PART 3



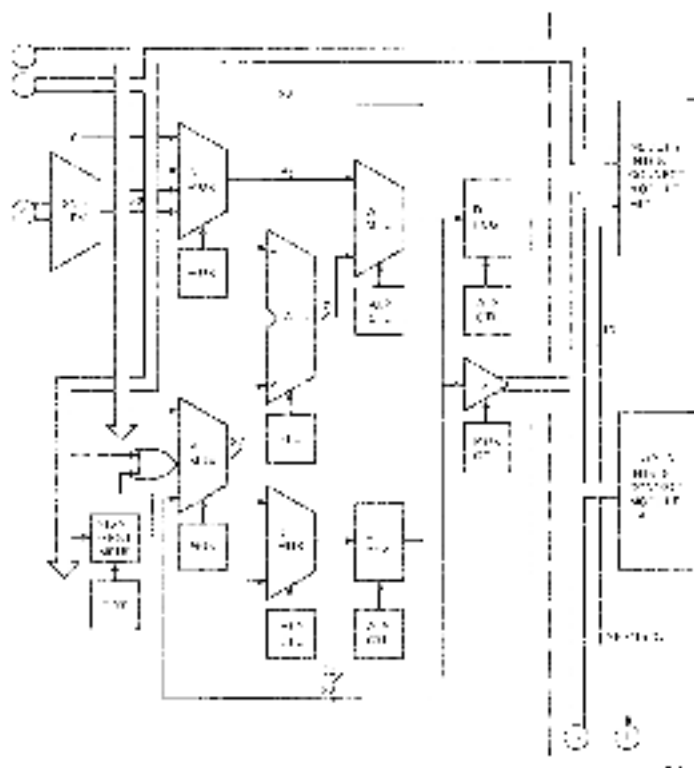
DFM BASIC DIAGRAM



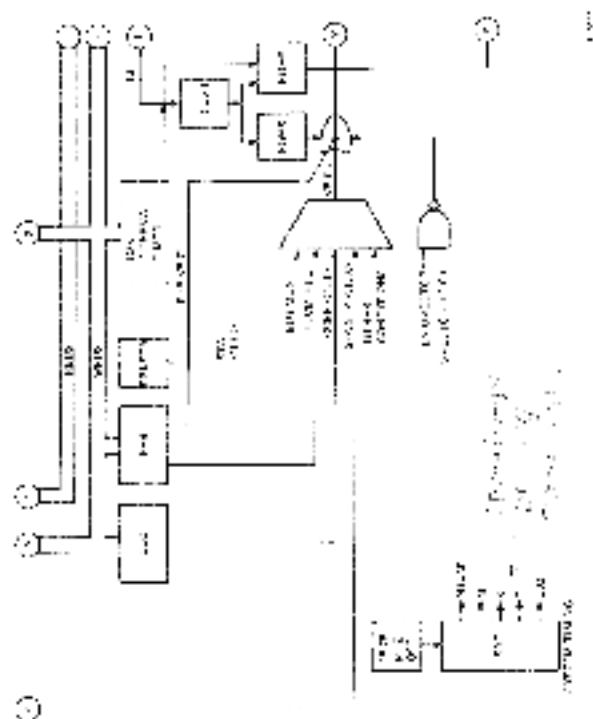
DPM BLOCK DIAGRAM, PART 1



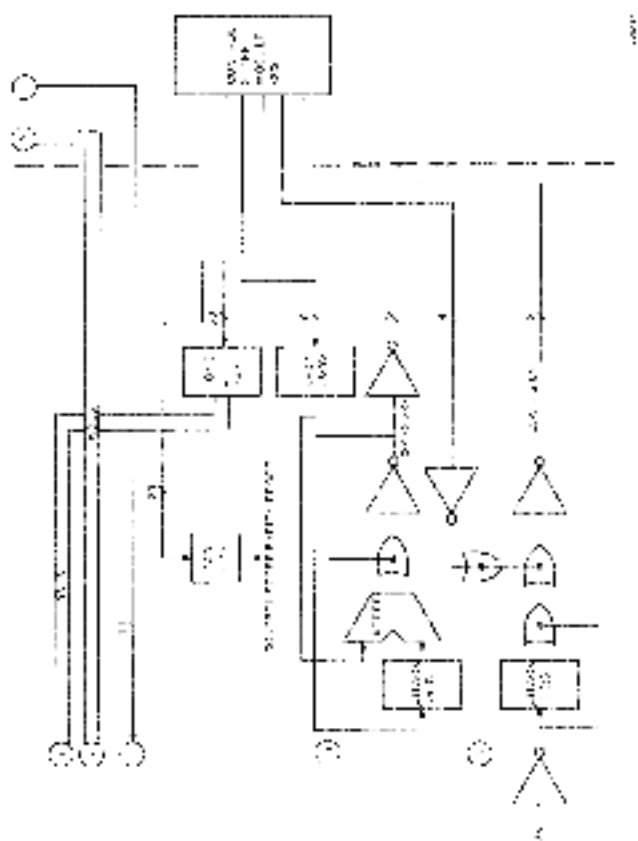
DPM BLOCK DIAGRAM, PART 2



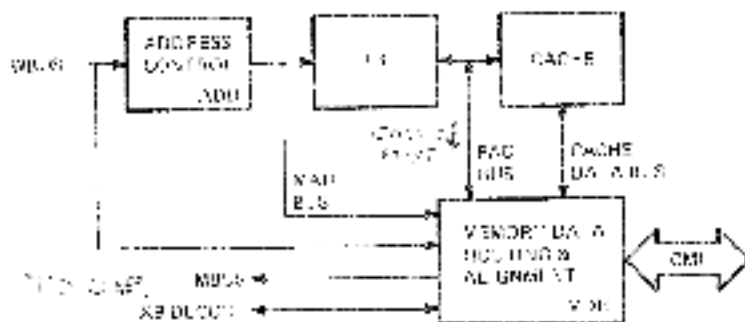
OPM BLOCK DIAGRAM, PART 3



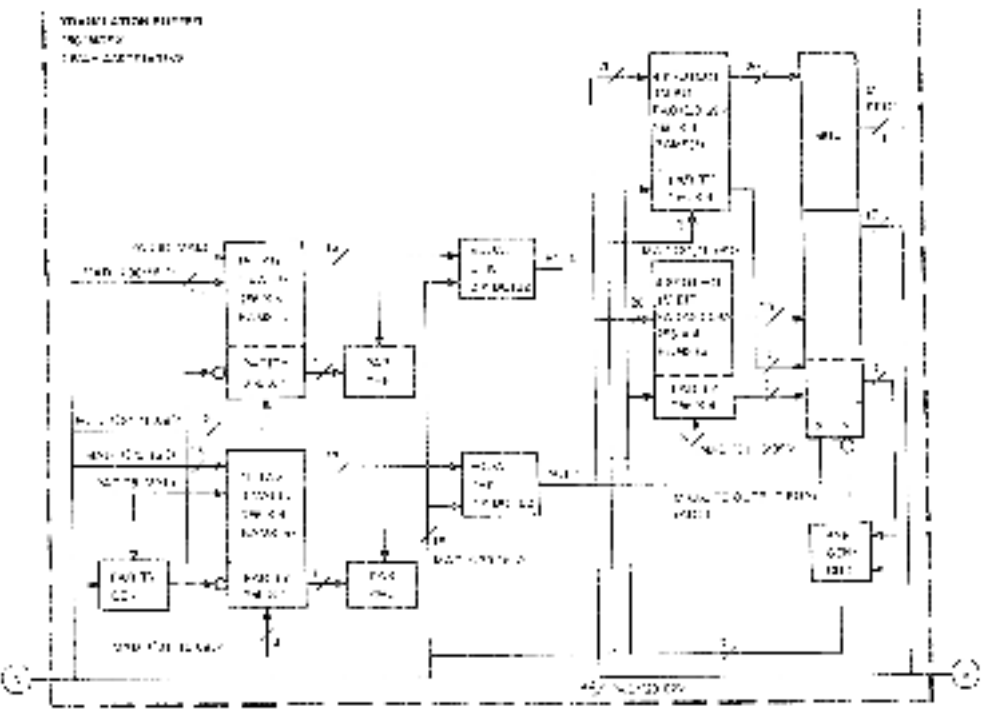
DPM BLOCK DIAGRAM, PART 4



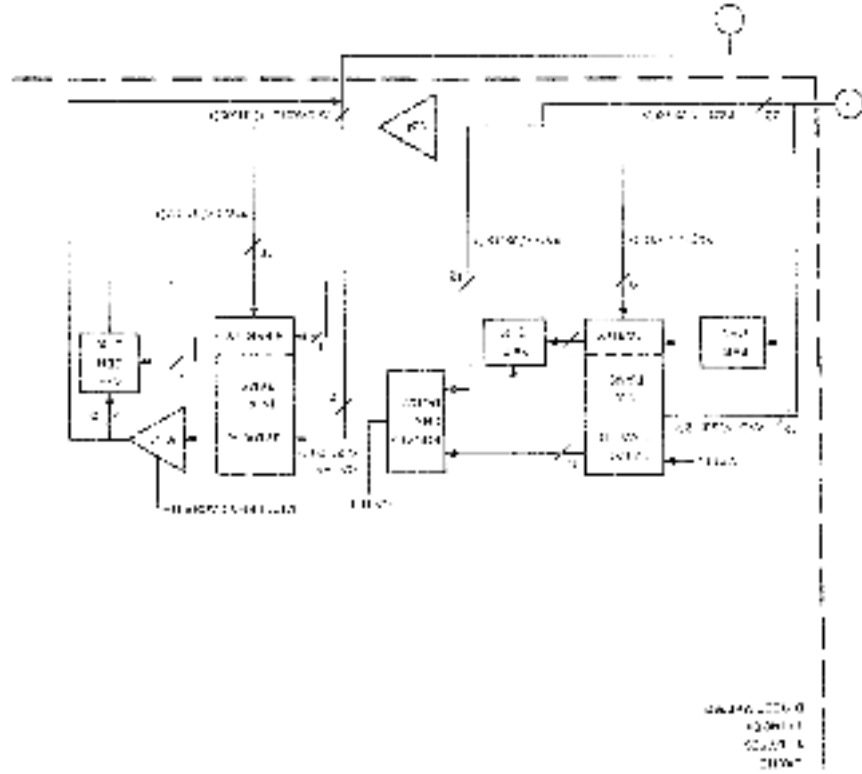
MIC BASIC DIAGRAM



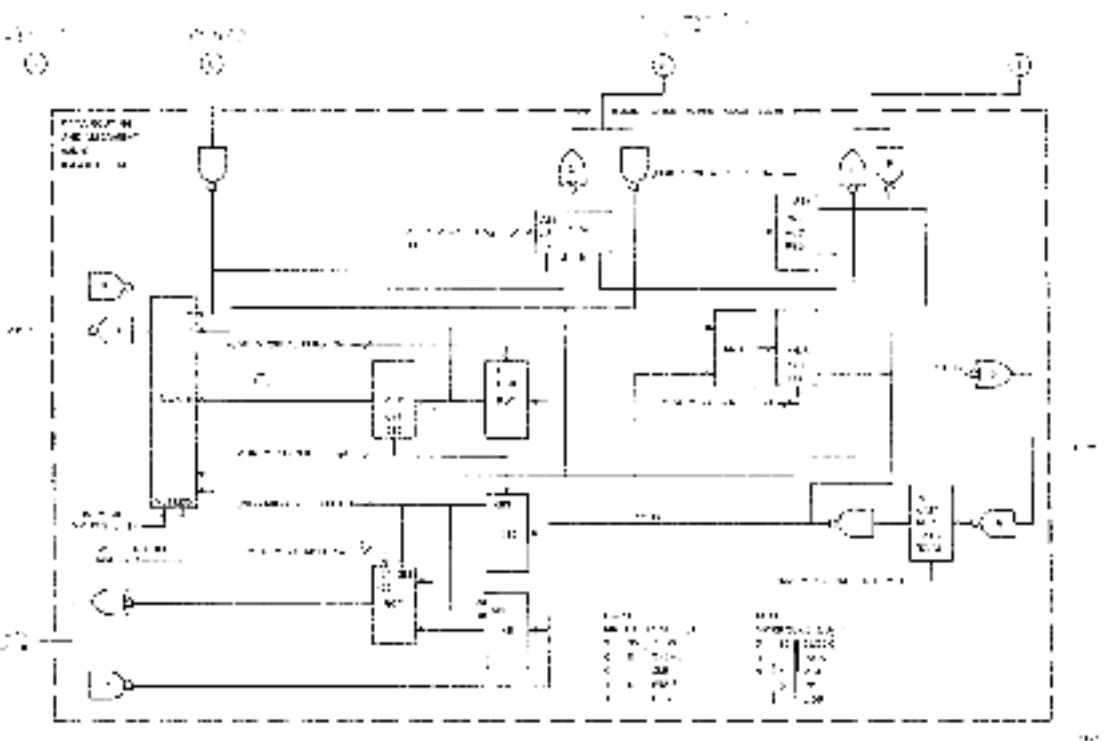
10-10



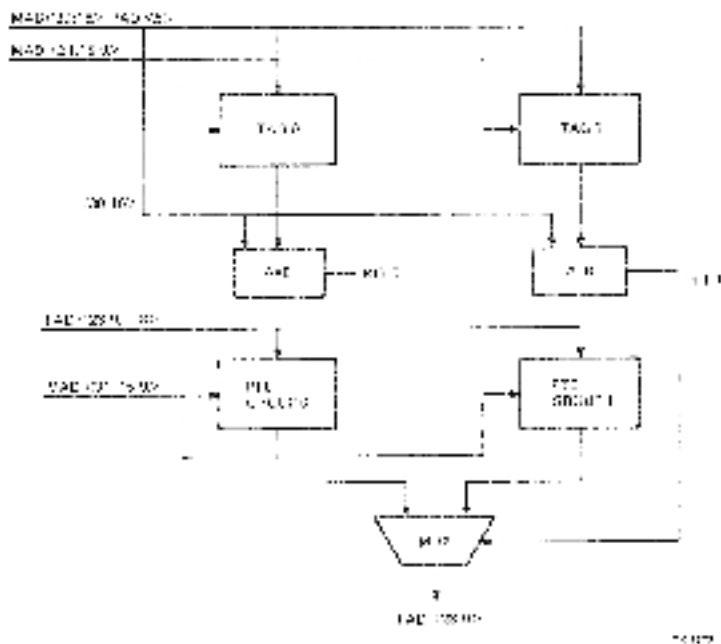
MIC BLOCK DIAGRAM, PART 3



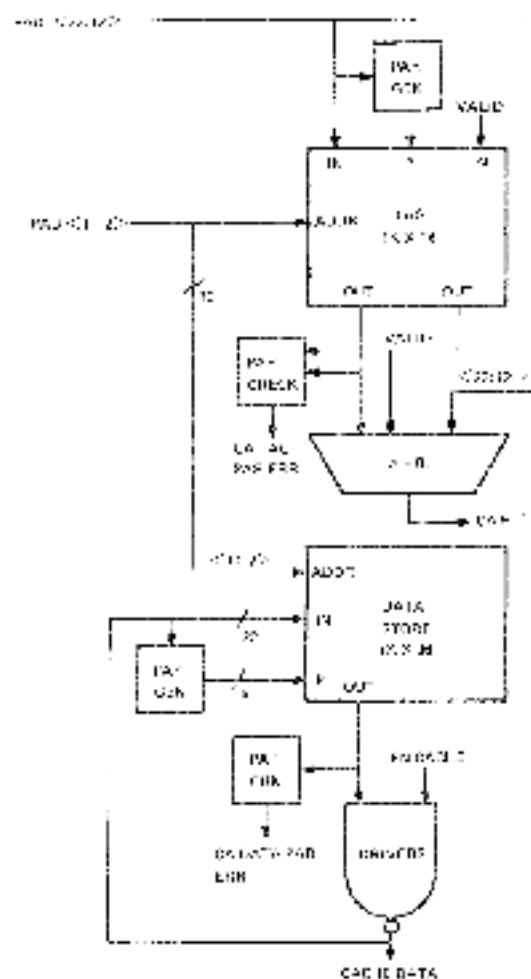
MIC BLOCK DIAGRAM, PART 4



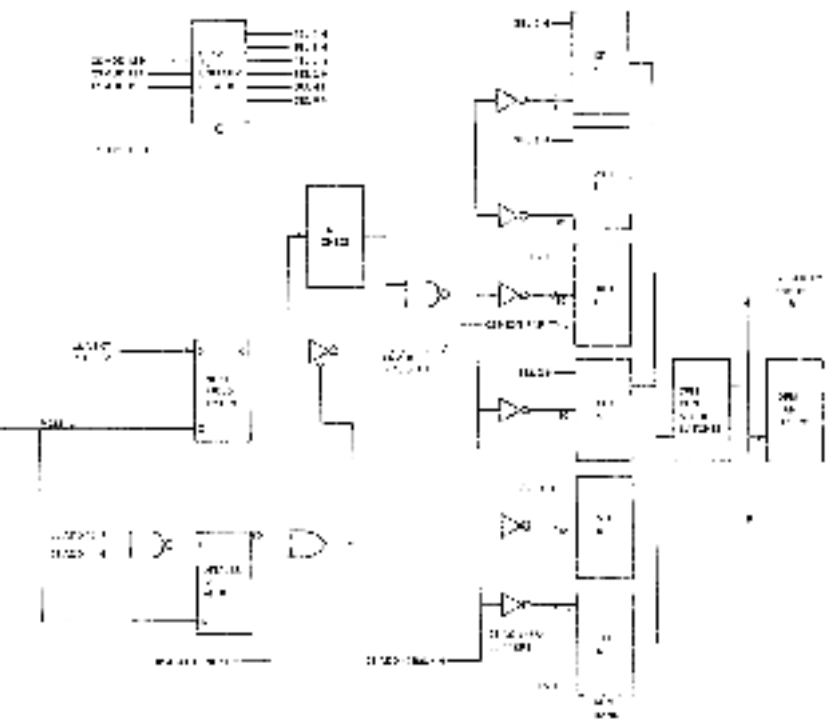
TR FUNCTIONAL DIAGRAM

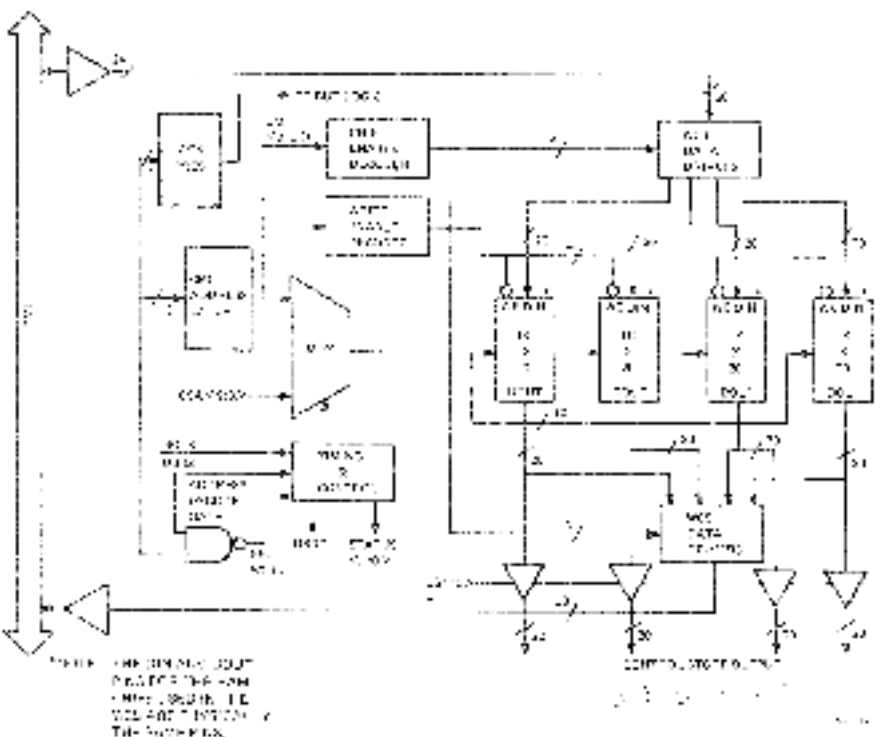


CACHE FUNCTIONAL DIAGRAM



COS BLOCK DIAGRAM

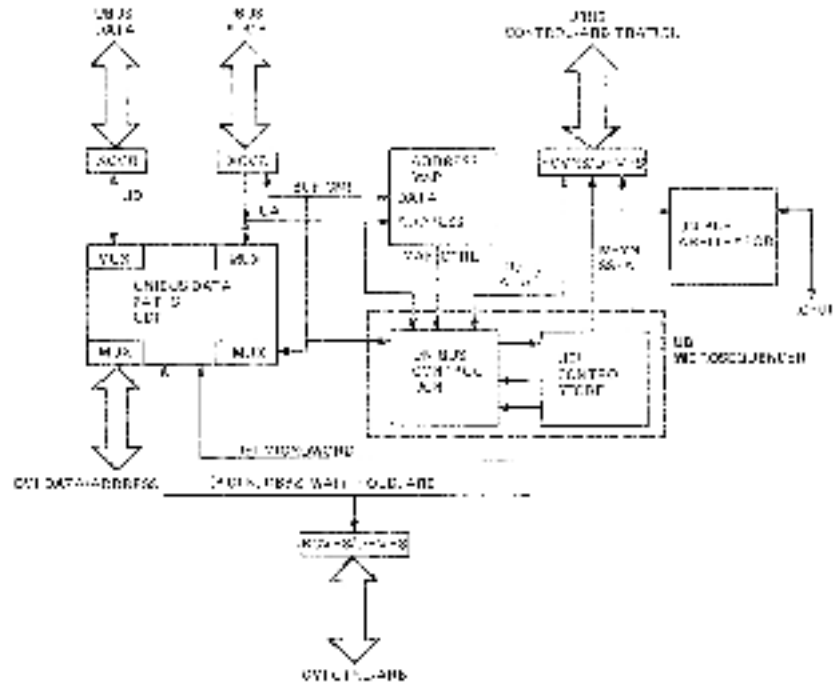




		1973						1974					
		900			900			900			900		
		900						900					
		900						900					
		900						900					
		900						900					
		900						900					
		900						900					
1	1	1	1	1	1	1	1	1	1	1	1	1	
2	2	2	2	2	2	2	2	2	2	2	2	2	
3	3	3	3	3	3	3	3	3	3	3	3	3	
4	4	4	4	4	4	4	4	4	4	4	4	4	
5	5	5	5	5	5	5	5	5	5	5	5	5	
6	6	6	6	6	6	6	6	6	6	6	6	6	
7	7	7	7	7	7	7	7	7	7	7	7	7	
8	8	8	8	8	8	8	8	8	8	8	8	8	
9	9	9	9	9	9	9	9	9	9	9	9	9	
0	0	0	0	0	0	0	0	0	0	0	0	0	

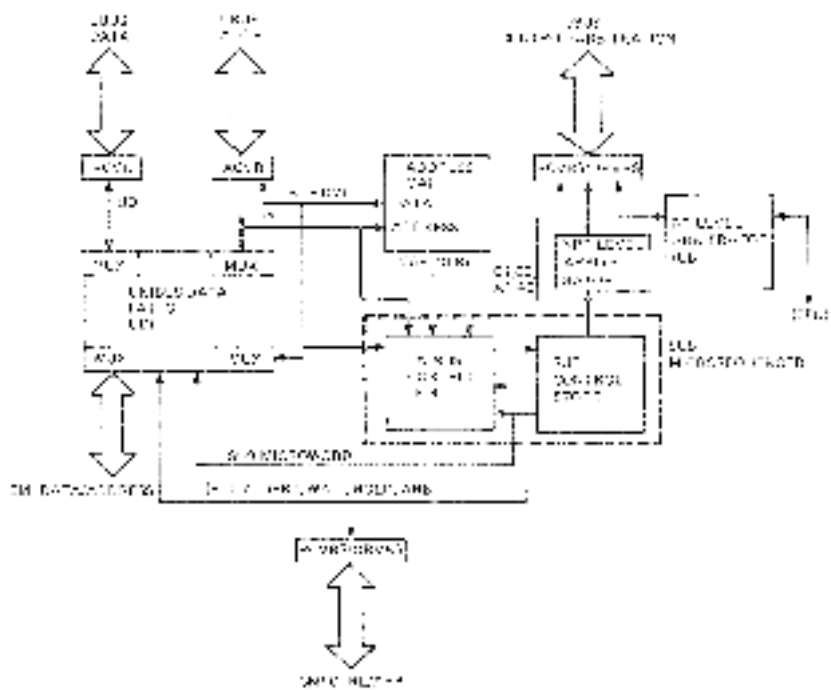
Source: Yearly Microgrid Energy Demand Data
 from the National Energy Survey.

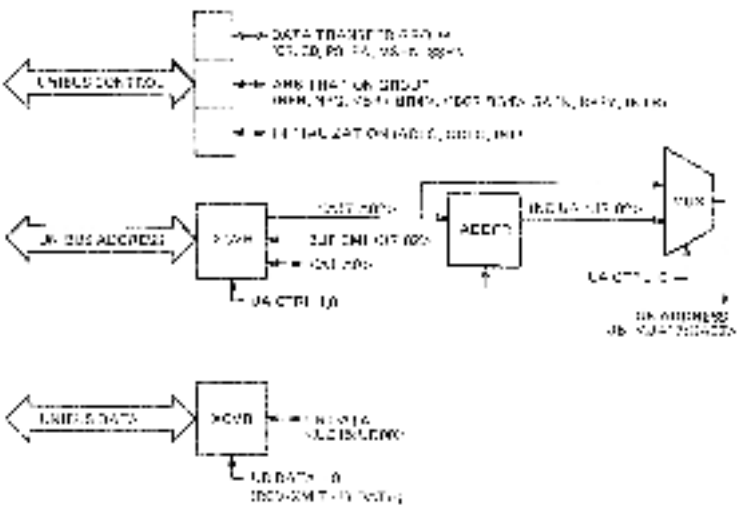
1973	
1973	900
1974	900
1975	900
1976	900
1977	900
1978	900
1979	900
1980	900
1981	900
1982	900
1983	900
1984	900
1985	900
1986	900
1987	900
1988	900
1989	900
1990	900
1991	900
1992	900
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2012	900
2013	900
2014	900
2015	900
2016	900
2017	900
2018	900
2019	900
2020	900
2021	900
2022	900
2023	900
2024	900
2025	900
2026	900
2027	900
2028	900
2029	900
2030	900



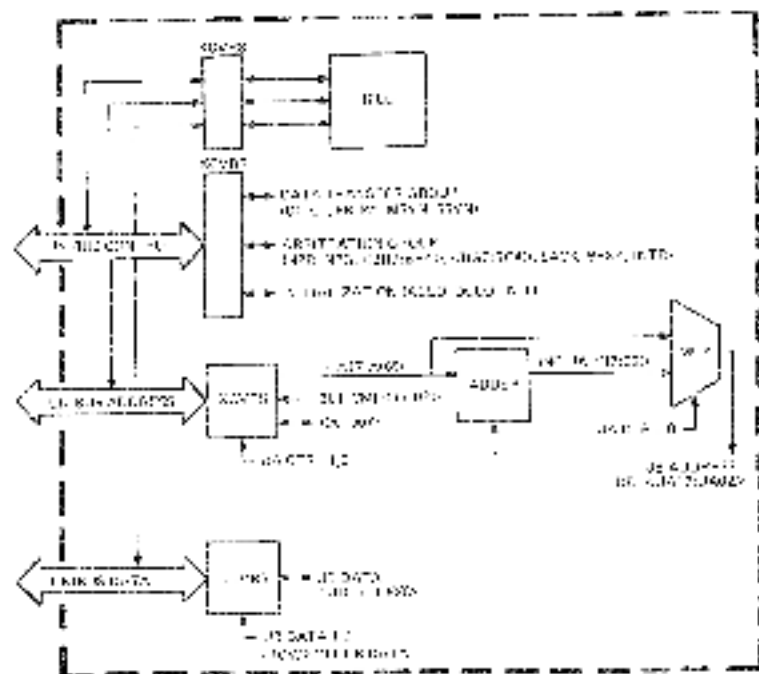


7-108

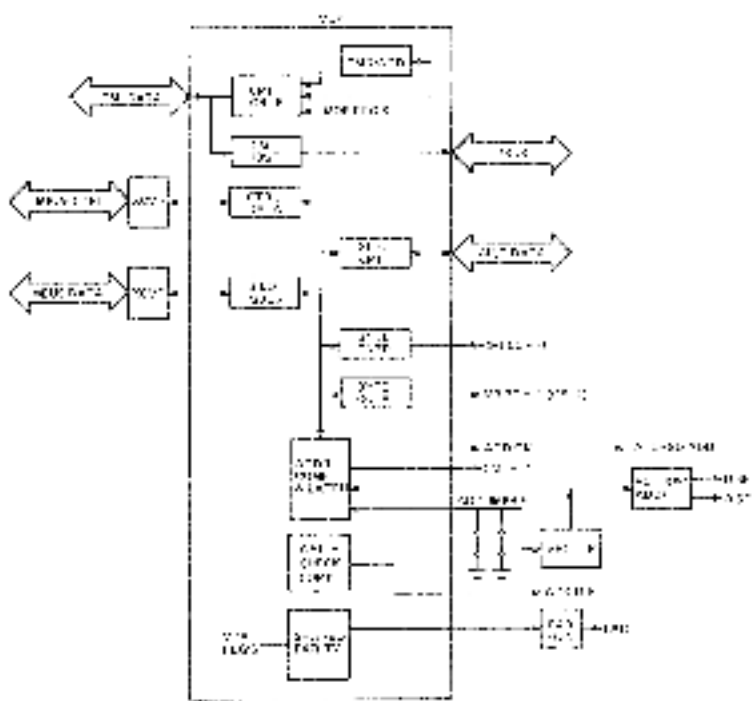




SUB INTERFACE TO SECOND UNIBUS LINES

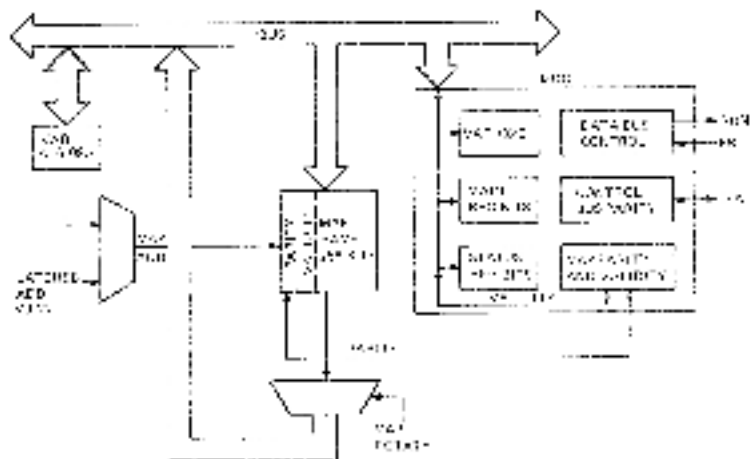
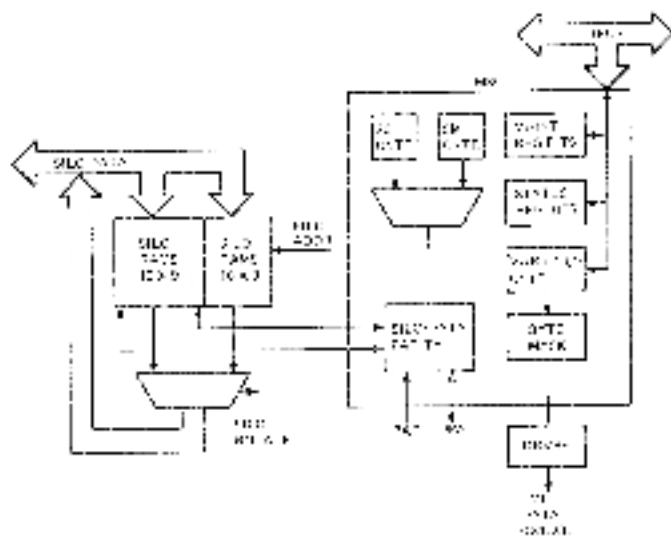


MBA (RM750) BLOCK DIAGRAM, PART 1

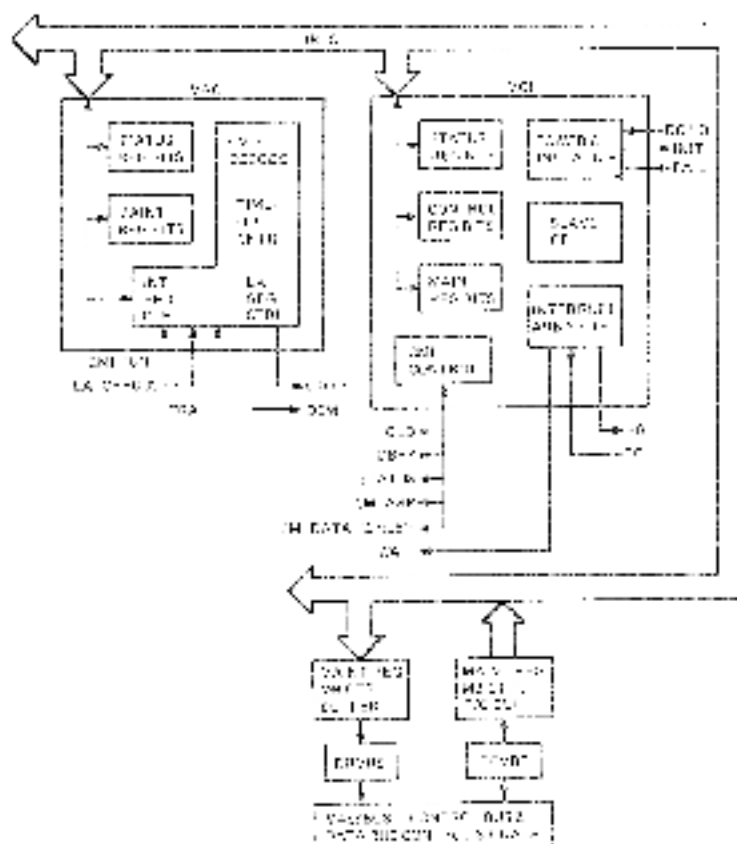


1/75

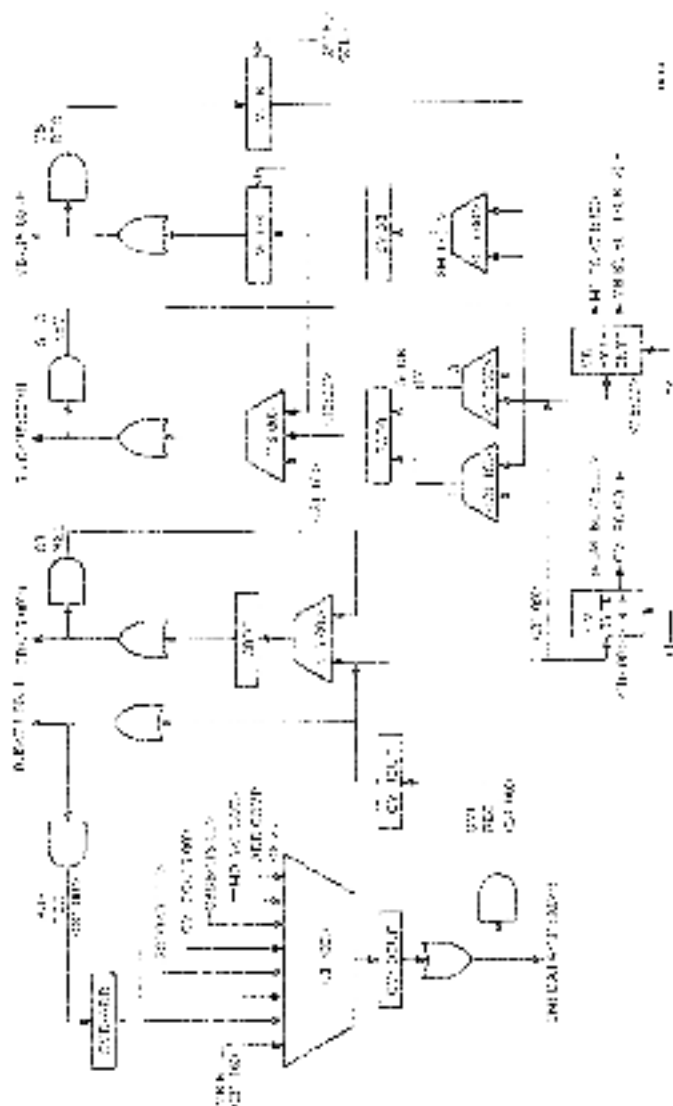
MBA (RH75G) BLOCK DIAGRAM, PART 2



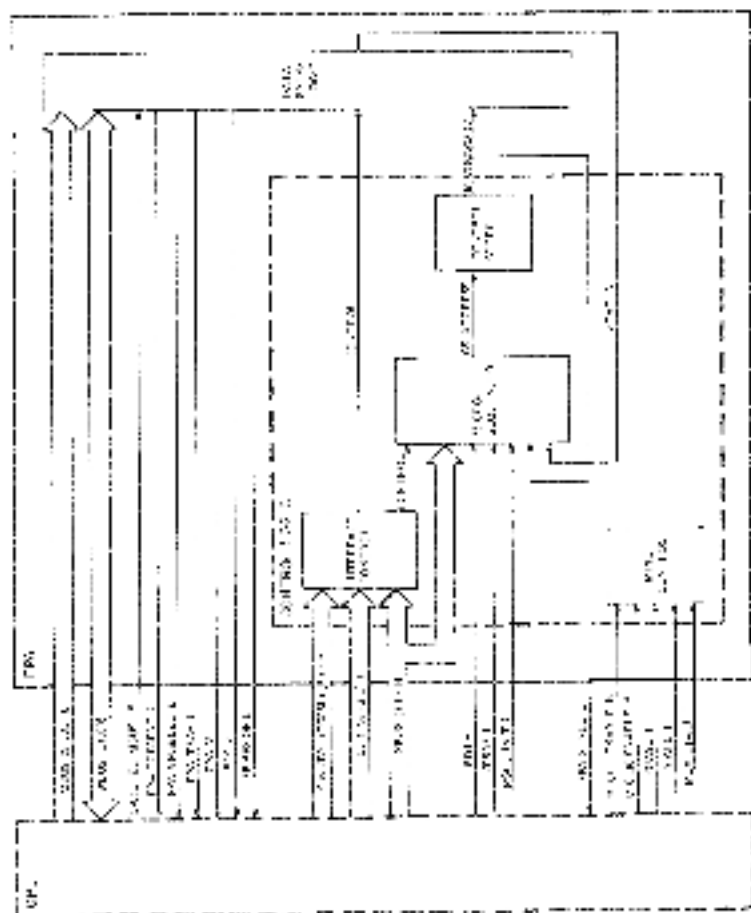
MBA (R11750) BLOCK DIAGRAM, PART 3

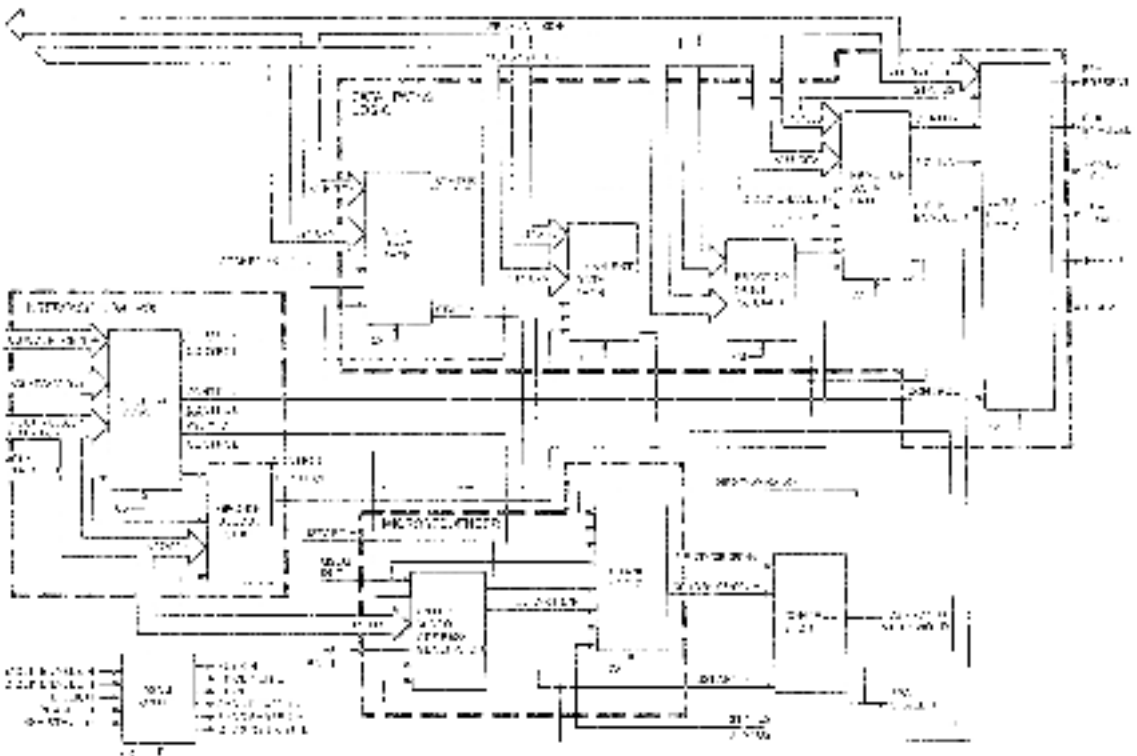


MOP DATA FLOW BLOCK DIAGRAM

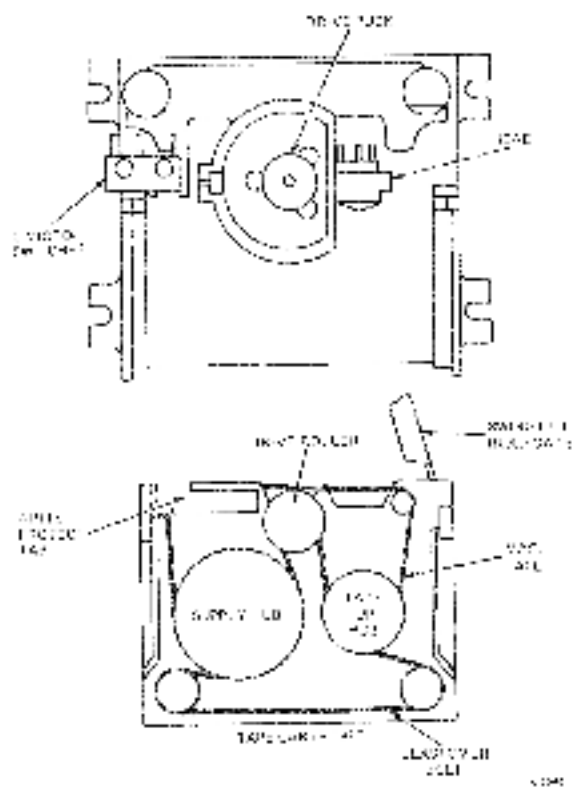


FPA (FP750) BASIC DIAGRAM

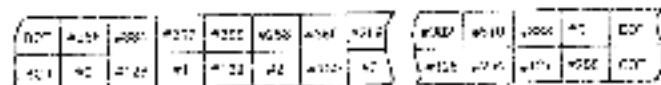




TUBE DRIVE/CARTRIDGE DIAGRAM

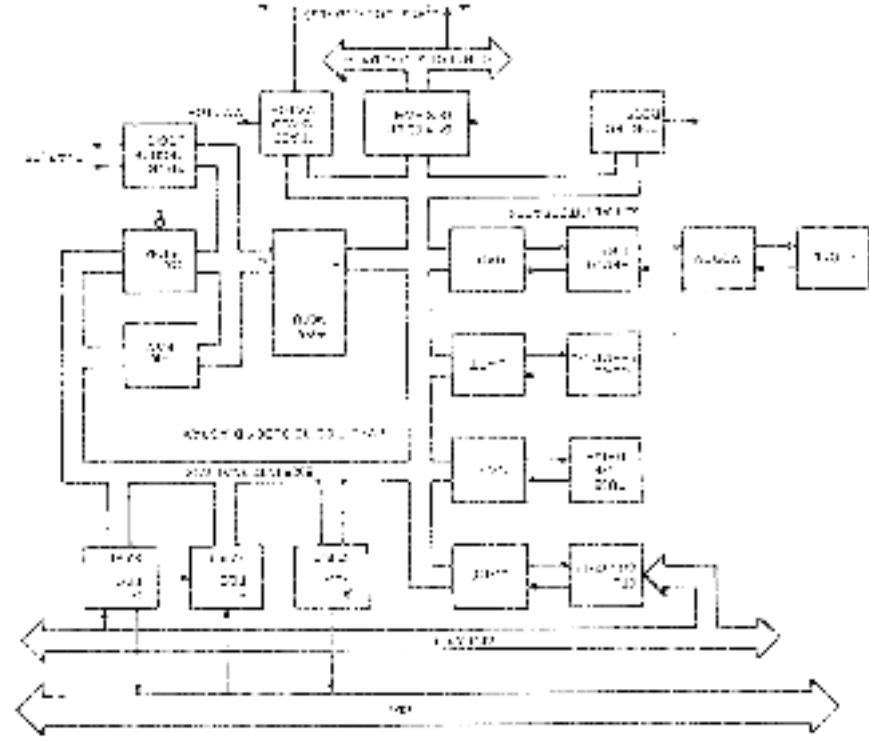


TUBE CASSETTE TAPE BLOCK LOCATIONS



1040

ROM BLOCK DIAGRAM



CHAPTER 8

CMI, UNIBUS, AND MASSBUS



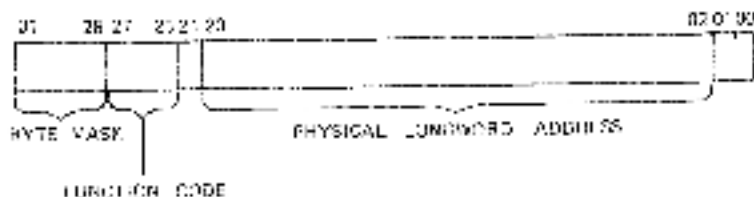
CM1 PHYSICAL ADDRESS MAP

00000	00000	RAM (1 MB)	1 ADDRESS
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	15 200 F
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	15 200 F
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	15 200 F
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	15 200 F
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	
00000	00000	RAM (1 MB)	

CM1 PHYSICAL ADDRESS MAP

CM1 ADDRESS AND DATA FORMAT

CM1 ADDRESS FORMAT

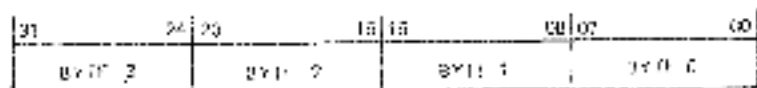


1-00005

CM1 BYTE MASK AND FUNCTION BITS

Byte Mask Bit	Physical Value for Transfer	Function Bit			CM1 operation
		27	26	25	
0x0000	Byte 0 0x00	0	0	0	Read
0x0001	Byte 0 0x01	0	0	1	Read lock
0x0002	Byte 1 0x00	0	1	0	Read parity (disabled)
0x0003	Byte 1 0x01	0	1	1	Read parity (disabled)
		1	0	0	Write
		1	0	1	Write unlock
		1	1	0	Write parity (disabled)
		1	1	1	Write parity (disabled)

CM1 DATA FORMAT



1-00004

CMI SIGNAL DESCRIPTION

Signal Lines Description

Timing Group

Σ CLK 1 Σ CLK 1 is generated by the CMI to synchronize all system sub-clocks.

One Σ CLK 1 pulse is fixed one rising edge of T_{CLK} 1 in the middle of T_{CLK} 1 to CLK 100 and 100 to CLK 100 T_{CLK} 1.

Control/Status and DATA OUT IP

CMI DATA (31-82) One CMI data line is fixed enabled by a valid CMI_{EN} has information for the CMI_{EN} command control or status. The only status provides control and address information on the same as the CMI address format, and address used for one T_{CLK} system. Data is then transferred on the lines in the CMI data format.

All address of the CMI address are ignored when four bytes (one largest of Data CMI) are transmitted on the lines and the valid data is returned by the Data CMI.

MODE

CMI DATA signals are asserted on a logic 1 at a nominal +3.3 V (typ.). All other CMI signals are asserted at a logical ground level.

Data Bus Busy (DBB) DBB is used to indicate by the master for one T_{CLK} T_{CLK} 1 while it places the CMI address of the slave on the CMI data lines. DBB is then asserted by the slave when the data transfer is complete. If the slave is immediately ready to respond, it may then assert DBB.

RDY RDY is used to temporarily block all CMI transactions. RDY, for example, requires extra 0 data valid to perform a localisation. RDY is not part of the CMI transaction and does not exceed T_{CLK} 1.

INT INT is asserted by a CMI subscriber to indicate a processor interrupt. It is held until the write vector resolution is performed.

DMI SIGNAL DESCRIPTION (CONT)

Signal Name Description

Priority Arbitration Group

ARBITRATOR A. ARB level is applied to each subsystem and is used to give control of the DMU. If both or a higher priority level is not selected when a subsystem wants to use the DMU, the subsystem assumes control of the DMU, assuming MRW and the 20 address of a given subsystem.

If still of a higher priority level is selected, the subsystem proceeds to use primarily but to hold all operations of lower priority until it gains control. Priority on the DMU is assigned as follows:

```

ARB0  MRW - highest priority
ARB1  reserved
ARB2  reserved
ARB3  RPI
ARB4  MRW or RPI
ARB5  MRW or MRW (with LOG)
ARB6  MRW or RPI (with RPI)
ARB7  CPU - lowest priority (from MRW
      address of ARB level)
    
```

Status Group

STATUS Status is transferred by a signal to indicate the condition under which it returns data to the master. STATUS bit combinations are specified as follows:

Status Bit

- 1 0
- 9 0 MRW - The master tried to access non-
 se-lectable data (MRW or RPI) of
 write data.
- 8 1 MRW - read data returned to the master
 carried an uncorrectable error.
- 7 0 MRW - corrected read data was returned
 to the master.
- 6 1 MRW - the read data had an error.

VAX-11/750 BACKPLANE

DMI SIGNAL PIN ASSIGNMENTS ON OPTION SLOTS

SLACK #	Signal	Pin	Pin	Pin
		41	47	17
		41	54	
		45	46	
		47	48	
		49	410	
	-2V	411	417	
		417	417	
		418	418	
		417	418	
		419	419	43
		421	412	
	GRD	421	414	413
		422	416	
		422	418	
	+2V	428	418	
		431	432	
		431	434	
		437	438	18
		439	440	
	PLAT TEST 0-7	441	412	SLJ1 SEL 3-4
	GRD	441	414	SLJ2
		447	416	
	+2V	447	418	
		448	418	
	GRD	451	407	GRD
	RDY REQ 0-1	454	404	RDY REQ 0-1
	CNT ARR 0-1	454	406	
	GRD OUT [A]	457	408	+0
	CNT ARR 1-1	459	410	PLD 0-1 [A] L
	ARR IN 0 [A]	461	412	CNT ARR 1-1
	CNT ARR 0-1	462	412	ARR IN 1 [A] L
	15V	468	420	CNT ARR 1-1
	LSUB BUS [A] H	467	418	LSUB BUS 0-1 [A] L
	LSUB BUS [A] H	469	418	LSUB BUS 0-1 [A] L
	CNT	471	412	SLJ
	LSUB BUS [A] H	471	414	LSUB BUS 0-1 [A] L
		471	416	19
	LSUB BUS [A] H	477	416	LSUB BUS 0-1 [A] L
	LSUB BUS 1	479	418	LSUB BUS L
	LSUB BUS 0	481	417	LSUB BUS L
	15V	482	404	CNT ARR 1-1
	CNT ARR 0-1	482	406	CNT ARR 1-1
	CNT ARR 1-1	482	408	CNT ARR 0-1
	CNT ARR 0-1	489	410	CNT ARR 0-1
	15V	491	412	CNT ARR 0-1
	CNT NEXT 0	491	414	0

VAX-11/750 BACKPLANE (CONT)

DMI SIGNAL PIN ASSIGNMENTS ON OPTION SLOTS (CONT)

BLK 07 0	DM1 DATA 0 0	P1	0	122	
	DM1 DATA 1 0	P2	04	DM1 DATA 1 0	
	DM1 DATA 3 0	P3	06	DM1 DATA 1 0	
	DM1 DATA 5 0	P7	08	DM1 DATA 0 0	
	DM1 DATA 7 0	P9	2,2	DM1 DATA 1 0	
	2,2	P11	010	DM1 DATA 0 0	
	DM1 DATA 18 0	P13	014	DM1 DATA 11 0	
	DM1 DATA 20 0	P15	016	DM1 DATA 13 0	
	DM1 DATA 22 0	P17	018	DM1 DATA 5 0	
	DM1 DATA 24 0	P19	P23	+	
	DM1 DATA 27 0	P1	P10	DM1 DATA 18 0	
	DM1	P25	P16	DM1	
	DM1 DATA 10 0	P26	P17	DM1 DATA 0 0	
	DM1 DATA 21 0	P27	P18	DM1 DATA 10 0	
	DM1	P19	P20	DM1 DATA 20 0	
	DM1 DATA 04 0	P31	P23	DM1 DATA 15 0	
	DM1 DATA 06 0	P32	P34	DM1 DATA 20 0	
	DM1 DATA 08 0	P35	P36	DM1 DATA 20 0	
	DM1 DATA 00 0	P37	P37	+	
	DM1 DATA 31 0	P19	P40	DM1 DATA 0 0	
	DM1 DATA 1 0	P41	P40	DM1 DATA 1	
	DM1	P41	P41	DM1	
	DM1 0 CLR L	P45	P47	+	
	DM1	P47	P48	EXT 00	
	DM1	P49	P50	+	
	DM1	P11	P11	DM1	
		P55	P57		
		P58	P59		
		P60	P61		
		P62	P63		
		P64	P64		
		P65	P65		
		P67	P67		
		P68	P68		
		P69	P69		
		P70	P70		
		P71	P71		
		P72	P72		
		P73	P73		
		P74	P74		
		P75	P75		
		P77	P77		
		P79	P80		
		P81	P81		
		P82	P82		
		P83	P83		
		P84	P84		
		P85	P85		
		P87	P87		
		P88	P88		
		P89	P89		
		P91	P92	DM1	
		P93	P94	+	
		P95	P97		

SLOT 0 AVAILABLE 0

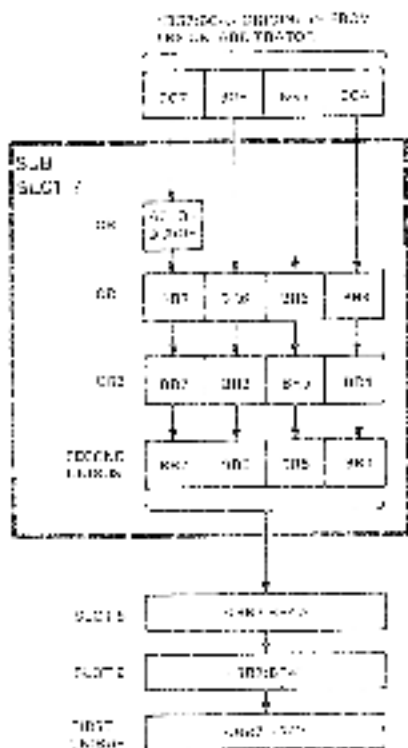
VAX-11/750 BACKPLANE (CONT)

UMI SIGNAL PIN ASSIGNMENTS ON OPTION SLOTS (CONT)

BOARD	BOARD	01	02	03
		01	04	
		05	06	
		07	08	
		09	10	
		11	12	
		13	14	
		15	16	
		17	18	
		19	20	
		21	22	
		23	24	
		25	26	
		27	28	
		29	30	
		31	32	
		33	34	
		35	36	
		37	38	
		39	40	
		41	42	
		43	44	
		45	46	
		47	48	
		49	50	
		51	52	
		53	54	
		55	56	
		57	58	
		59	60	
		61	62	
		63	64	
		65	66	
		67	68	
		69	70	
		71	72	
		73	74	
		75	76	
		77	78	
		79	80	
		81	82	
		83	84	
		85	86	
		87	88	
		89	90	
		91	92	
		93	94	
	200	241	242	ONE
	200	243	244	ONE
	205	247	248	INT0/5 INT0/7
	205	249	250	-5
	207	251	252	ONE
	251	254		
	255	256		
	257	258		
	259	260		
	261	262		
	263	264		
	265	266		
	267	268		
	269	270		
	271	272		
	273	274		
	275	276		
	277	278		
	279	280		
	281	282		
	283	284		
	285	286		
	287	288		
	289	290		
	291	292		ONE
	293	294		-5

VAX-11/750 BACKPLANE (CONT)

BUS GRANT CHAIN AND CONTINUITY JUMPER



1. SHOWS THE ONLY
 METHOD OF BUS GRANTING
 BETWEEN THE TELETYPE
 DRIVER AND THE TELETYPE
 DRIVER. THE TELETYPE
 DRIVER IS THE ONLY
 DEVICE WHICH CAN
 GRANT THE BUS TO
 THE TELETYPE DRIVER.

VAX-11/750 BACKPLANE (CONT)

BUS GRANT CHAIN AND CONTINUITY JUMPERS (CONT)

Each of the three backplane option slots is hard-wired to one DM controller for bus bus at level and when it is installed, and is therefore not to be changed.

All of the following continuity jumpers must be in place on an empty slot. They must all be removed from the slot when the DM controller is installed.

Bus Grant Level	Remove All Jumpers
B07	B07 to A06
B06	A08 to A04
B05	B05 to A08
B04	B07 to B08

CAUTION

Before the DM is unpacked for installation, refer to the DM's installation procedure that specifies the use of a VTEC9000 net and ground cord to prevent static discharge damage.

Grounding must first be made between a snap connector on the net and a good ground on the system. Connection is then made from a wrist strap worn by the installer to an Alligator clip that is fastened to the net.

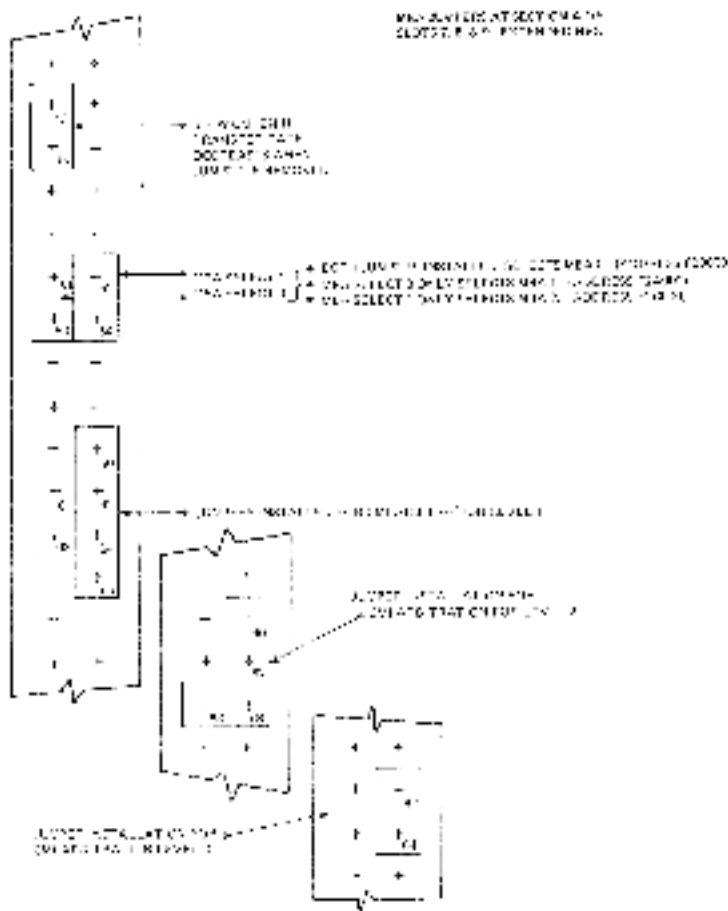
The net is placed on the VTEC9000 net and removed. The module is then removed from the bus, the protective covering removed, and the module laid flat on the VTEC9000 net. This brings it to the same potential as the DM's.

With the wrist strap still in place, the DM's module is plugged into slot 1 to avoid cabling errors, and to place the second DM1506 at first priority in the bus grant chain.

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VAX-11/750 BACKPLANE (CONT.)

MBA INSTALLATION JUMPERS



VAX-11/750 BACKPLANE (CONT)

MBA INSTALLATION JUMPERS (CONT)

MBA Select Jumpers

On Select PCB As Shipped	Terminal Block Jumpers
MSB 2	MSB TO MS1 (MS0) MS4 TO MS3 (MS0)
MSB 1	MS1 TO MS0 (MS4 removed)
MSB 0	MS4 TO MS3 (MS1 removed)
ROM (M) jumper	MS1 TO MS0 (MS0 normally in place). Removing this jumper reduces the rate at which the ROM is loaded and is critical on the CPU before ROM is MBL and after it is cleared.

MBA CMI Arbitration Jumpers

On Select PCB As Shipped	MSB	Terminal Block Jumpers
MSB 2	MSB 2	MS4 TO MS3 (MSB MS5 TO CMT MS6 MS1)
MSB 2	MSB	MS4 TO MS3 (MSB MS5 TO CMT MS6 MS2) MS2 TO MS1 (MS1 MS5 MS3 TO MS)
MSB 1	MSB 2	MS4 TO MS3 (MSB MS5 TO CMT MS6 MS1) MS1 TO MS0 (MS1 MS5 MS3 TO MS) MS2 TO MS1 (CMT MS6 MS3 MS)

MBA Interrupt Priority Plug

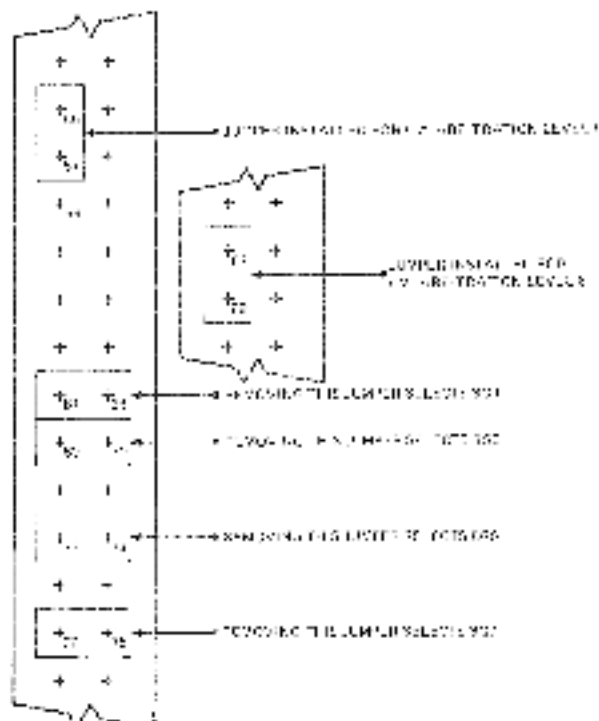
On PCB MSB 01 IR Priority Level	IR Priority Plug Part Number
1	54-88710-02
2	54-88710-03
3	54-88710-04
4	54-88710-05

Consult IR level plug, supplied

VAX-11/750 BACKPLANE (CONT)

RESERVED ARBITRATION JUMPHS

SEE BACKSET ADDRESS SECTION FOR
EXTENDED JUMP ADDRESS RANGE

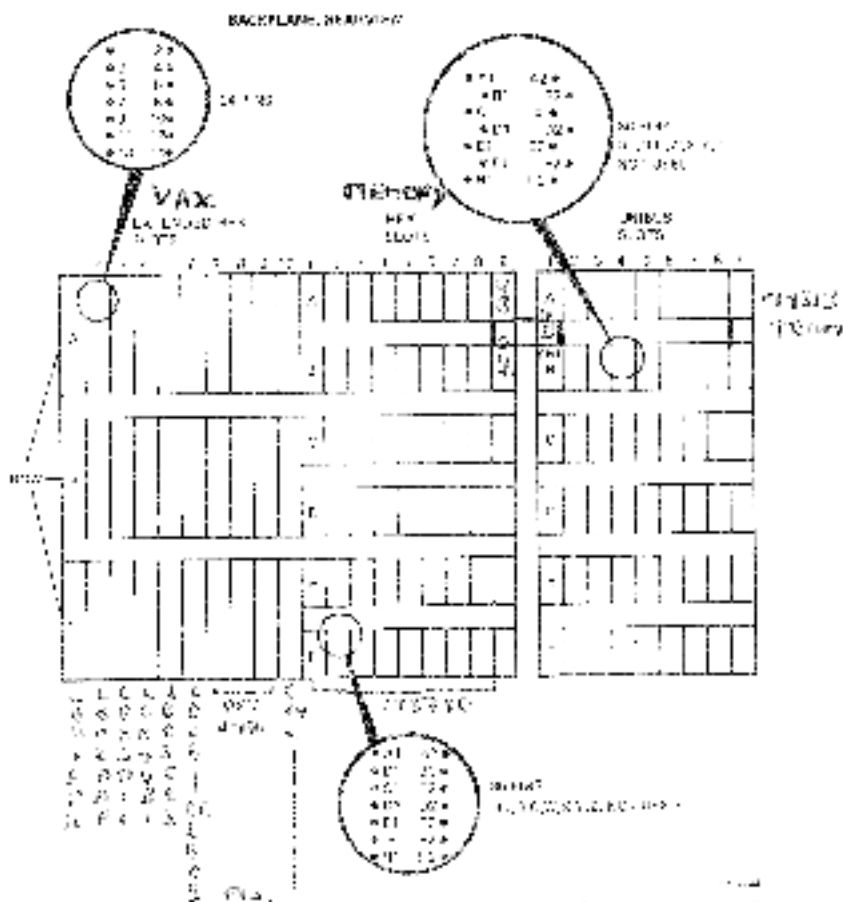


7-2002

VAX-11/750 BACKPLANE (CONT)

MODULE BLOCK LAYOUT

90% \pm ARE REV 7 OR 8.



1000 - 1/2 mod. (REV 6. str)
 1010 - 1/2 mod. (REV 6. str)
 1020 - 1/2 mod. (REV 6. str)
 level and mod.
 cross and link

VAX-11/750 BACKPLANE (CONT)

MODULE PIN BREAKOUTS

1	→	07
2	→	04
3	→	05
4	→	03
5	→	00
6	→	0C
7	→	09
8	→	08
9	→	0A
10	→	0B
11	→	06
12	→	01
13	→	02
14	→	0E
15	→	0D
16	→	0F
17	→	04
18	→	05
19	→	03
20	→	00
21	→	0C
22	→	09
23	→	08
24	→	0A
25	→	0B
26	→	06
27	→	01
28	→	02
29	→	0E
30	→	0D
31	→	0F
32	→	04
33	→	05
34	→	03
35	→	00
36	→	0C
37	→	09
38	→	08
39	→	0A
40	→	0B
41	→	06
42	→	01
43	→	02
44	→	0E
45	→	0D
46	→	0F
47	→	04
48	→	05
49	→	03
50	→	00
51	→	0C
52	→	09
53	→	08
54	→	0A
55	→	0B
56	→	06
57	→	01
58	→	02
59	→	0E
60	→	0D
61	→	0F
62	→	04
63	→	05
64	→	03
65	→	00
66	→	0C
67	→	09
68	→	08
69	→	0A
70	→	0B
71	→	06
72	→	01
73	→	02
74	→	0E
75	→	0D
76	→	0F
77	→	04
78	→	05
79	→	03
80	→	00
81	→	0C
82	→	09
83	→	08
84	→	0A
85	→	0B
86	→	06
87	→	01
88	→	02
89	→	0E
90	→	0D
91	→	0F
92	→	04
93	→	05
94	→	03
95	→	00
96	→	0C
97	→	09
98	→	08
99	→	0A
100	→	0B

1	→	07
2	→	04
3	→	05
4	→	03
5	→	00
6	→	0C
7	→	09
8	→	08
9	→	0A
10	→	0B
11	→	06
12	→	01
13	→	02
14	→	0E
15	→	0D
16	→	0F
17	→	04
18	→	05
19	→	03
20	→	00
21	→	0C
22	→	09
23	→	08
24	→	0A
25	→	0B
26	→	06
27	→	01
28	→	02
29	→	0E
30	→	0D
31	→	0F
32	→	04
33	→	05
34	→	03
35	→	00
36	→	0C
37	→	09
38	→	08
39	→	0A
40	→	0B
41	→	06
42	→	01
43	→	02
44	→	0E
45	→	0D
46	→	0F
47	→	04
48	→	05
49	→	03
50	→	00
51	→	0C
52	→	09
53	→	08
54	→	0A
55	→	0B
56	→	06
57	→	01
58	→	02
59	→	0E
60	→	0D
61	→	0F
62	→	04
63	→	05
64	→	03
65	→	00
66	→	0C
67	→	09
68	→	08
69	→	0A
70	→	0B
71	→	06
72	→	01
73	→	02
74	→	0E
75	→	0D
76	→	0F
77	→	04
78	→	05
79	→	03
80	→	00
81	→	0C
82	→	09
83	→	08
84	→	0A
85	→	0B
86	→	06
87	→	01
88	→	02
89	→	0E
90	→	0D
91	→	0F
92	→	04
93	→	05
94	→	03
95	→	00
96	→	0C
97	→	09
98	→	08
99	→	0A
100	→	0B

1	→	07
2	→	04
3	→	05
4	→	03
5	→	00
6	→	0C
7	→	09
8	→	08
9	→	0A
10	→	0B
11	→	06
12	→	01
13	→	02
14	→	0E
15	→	0D
16	→	0F
17	→	04
18	→	05
19	→	03
20	→	00
21	→	0C
22	→	09
23	→	08
24	→	0A
25	→	0B
26	→	06
27	→	01
28	→	02
29	→	0E
30	→	0D
31	→	0F
32	→	04
33	→	05
34	→	03
35	→	00
36	→	0C
37	→	09
38	→	08
39	→	0A
40	→	0B
41	→	06
42	→	01
43	→	02
44	→	0E
45	→	0D
46	→	0F
47	→	04
48	→	05
49	→	03
50	→	00
51	→	0C
52	→	09
53	→	08
54	→	0A
55	→	0B
56	→	06
57	→	01
58	→	02
59	→	0E
60	→	0D
61	→	0F
62	→	04
63	→	05
64	→	03
65	→	00
66	→	0C
67	→	09
68	→	08
69	→	0A
70	→	0B
71	→	06
72	→	01
73	→	02
74	→	0E
75	→	0D
76	→	0F
77	→	04
78	→	05
79	→	03
80	→	00
81	→	0C
82	→	09
83	→	08
84	→	0A
85	→	0B
86	→	06
87	→	01
88	→	02
89	→	0E
90	→	0D
91	→	0F
92	→	04
93	→	05
94	→	03
95	→	00
96	→	0C
97	→	09
98	→	08
99	→	0A
100	→	0B

HEX PIN BREAKOUT

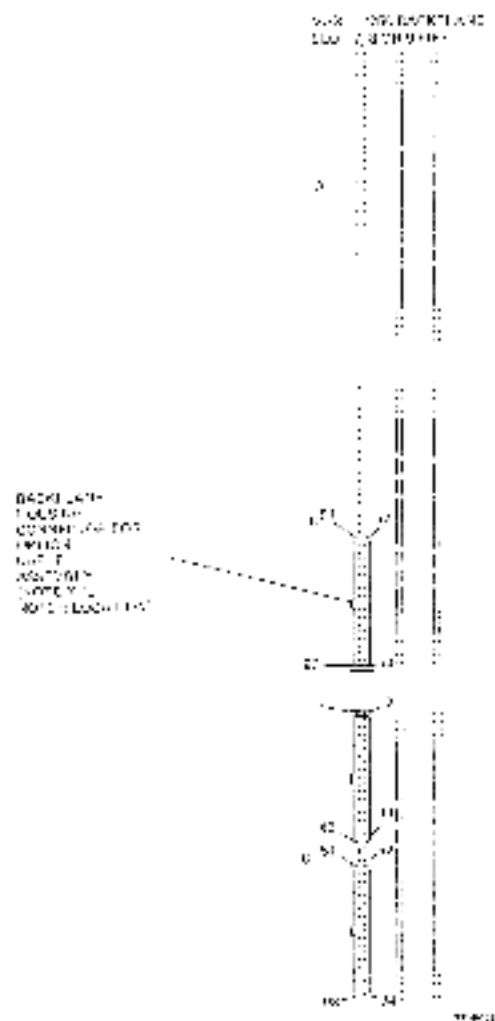
UNIBUS PIN BREAKOUT

EXTENDED HEX
PIN BREAKOUT

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VAX-11/750 BACKPLANE (CONT)

BACKPLANE CONNECTOR HOUSING INSTALLATION DIAGRAM



UBI AND SUB PHYSICAL ADDRESS SPACE

		16X16 DATA LONGWORD	
UBI FIRST ENERGIES		UNUSFD	F00000
		CSR1	F00004
		UN2	F00008
		CSR3	F0000C
		UN3LD	F00010
		MAP	F00014
		UN3LD	F00018
		UN3LD	F0001C
		UN3LD	F00020
		UN3LD	F00024
SUB- SECOND ENERGIES		CSR1	F00028
		CSR2	F0002C
		CSR3	F00030
		UN3LD	F00034
		MAP	F00038
		UN3LD	F0003C
		UN3LD	F00040
		UN3LD	F00044

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FIRST AND SECOND UNIBUS REGISTER SUMMARY

DBI Address	RAM Address	Register Name	Description/Comments
F00704	F07044	CCR 1	CCR for CCR 1
F00708	F07048	CCR 2	CCR for CCR 2
F0070C	F0705C	CCR 3	CCR for CCR 3
F07080	F08020	MAP 20	physical base address
F07084	F08024	MAP 21	
F00780	F08028	MAP 22	
F00784	F0803C	MAP 23	The 32 K map addresses are accessed in increments of four through the range of map 20 (hex).
F00788	F08040	MAP 24	
F0078C	F08044	MAP 25	
F00790	F08048	MAP 26	The physical map addresses may be obtained by adding the MAP register number to the previous base address.
F00794	F08054	MAP 27	
F00798	F08060	MAP 28	
F0079C	F08064	MAP 29	-
F007A0	F08068	MAP 30	
F007A4	F08074	MAP 31	
F007A8	F08078	MAP 32	-
F007AC	F08084	MAP 33	
F007B0	F08088	MAP 34	
F07087	F08080	MAP 35	physical base address for "MINI" I/O devices.
F0708E	F08088	MAP 36	
F07095	F08096	MAP 37	
F0709C	F08104	MAP 38	The CPU address of a source is obtained by converting the data access address to hexadecimal and adding it to the physical base address.
F070A3	F08112	MAP 39	
F070AA	F08120	MAP 40	
F00770	F00700	MAP 41	-
F00774	F00704	MAP 42	
F00778	F00708	MAP 43	
F0077C	F0070C	MAP 44	-
F00780	F00710	MAP 45	
F00784	F00714	MAP 46	
F00788	F00718	MAP 47	-
F0078C	F0071C	MAP 48	
F00790	F00720	MAP 49	
F00794	F00724	MAP 50	-
F00798	F00728	MAP 51	
F0079C	F00734	MAP 52	
F007A0	F00738	MAP 53	-
F007A4	F0073C	MAP 54	
F007A8	F00740	MAP 55	
F007AC	F00744	MAP 56	-
F007B0	F00748	MAP 57	
F007B4	F0074C	MAP 58	
F007B8	F00750	MAP 59	-
F007BC	F00754	MAP 60	
F007C0	F00758	MAP 61	
F007C4	F0075C	MAP 62	-
F007C8	F00760	MAP 63	
F007CC	F00764	MAP 64	
F007D0	F00768	MAP 65	-
F007D4	F0076C	MAP 66	
F007D8	F00770	MAP 67	
F007DC	F00774	MAP 68	-
F007E0	F00778	MAP 69	
F007E4	F0077C	MAP 70	
F007E8	F00780	MAP 71	-
F007EC	F00784	MAP 72	
F007F0	F00788	MAP 73	
F007F4	F0078C	MAP 74	-
F007F8	F00790	MAP 75	
F007FC	F00794	MAP 76	
F00800	F00798	MAP 77	-
F00804	F0079C	MAP 78	
F00808	F007A0	MAP 79	
F0080C	F007A4	MAP 80	-
F00810	F007A8	MAP 81	
F00814	F007AC	MAP 82	
F00818	F007B0	MAP 83	-
F0081C	F007B4	MAP 84	
F00820	F007B8	MAP 85	
F00824	F007BC	MAP 86	-
F00828	F007C0	MAP 87	
F0082C	F007C4	MAP 88	
F00830	F007C8	MAP 89	-
F00834	F007CC	MAP 90	
F00838	F007D0	MAP 91	
F0083C	F007D4	MAP 92	-
F00840	F007D8	MAP 93	
F00844	F007DC	MAP 94	
F00848	F007E0	MAP 95	-
F0084C	F007E4	MAP 96	
F00850	F007E8	MAP 97	
F00854	F007EC	MAP 98	-
F00858	F007F0	MAP 99	
F0085C	F007F4	MAP 100	

NOTE: In address ranges not listed with the RAM address, reading the 8008 I/O requests that return 8008 data (0000).

FIXED DEVICE ADDRESS AND VECTOR ASSIGNMENTS

Assigned I/OBUS devices normally occupy vector addresses through 254 (hex) (07E through 0FE hexadecimal).

Setting I/OBUS devices may be assigned vector addresses through 254 (hex) (07E through 0FE hexadecimal).

UNIT/BS Device	Address Base	Address Size	Vector Base	Vector Size	No. of Units/ Comments
AK11-11	774000	0	7E	4	1st unit
AK11	774000	0			4 extra units
AA11	774040	4			1 unit
AD11	774100	4	130	2	1
AJ11	774140	8			1
AT11-A	774200	2	180	4	1
AP11	774200	4	18	2	1
A111	774400	8			1
BA11-DB	774520	3			1
BT11-DB	774540	1			1
BU11-DB	774880	256			1
BP11-DB	774864	32			1
BR11-DB	774160	12			1
BS11-DB	774280	5			1
BT11-DB	774360	37			1
BU11-DB	774880	128			1
BT11-DB/DB	774880	256			1
BR11			104	2	1 175 class
BR11	774150	2			1 175 class
BU11-DB/DB	774160	4	150	4	1
BU11	764070	4	170	2	1 175 hardware
CP11			114	4	
CP11	764080	4	170	4	1 175 hardware
CP11/DB	764080	1024			1
DC11	774880	4			16
PL11-A	774560	4			1
Microchannel	762000	4			1
RT11			210	2	
RT11/RT11-A/B	774560	4	150		1 - unit only
RT11/RT11-A/B	765800	4			16
RT11-A/B/DB	774510	4			31
SL11-A	774010	4			4
SL11-B	776580	4			16
SL11-A	776580	16			4
SL11-A	774540	1	807	4	1st L1C
SL11-A	774560	4			1 2nd L1C
SL11-A	776580	4			16
SL11-DB/DB	774580	4			16 - hardware
SL11	774880	4			16
SL11-A	774880	4			16
SL11-DB	774580	1			16

FIXED DEVICE ADDRESS AND VECTOR ASSIGNMENTS (CONT)

DEVICE Device	Address Base	Address Size	Vector Base	Vector Size	Max. # of Channels
DC11	77460	4			100
DC11-A01	77468	4			150
DC11-E-101	77472	4	100	2	2
DC11-E-102	77476	4			
DC211	78772	4			100
DC211-A0	78776	4	100	2	2
DC211-E-1	78780	4			100
LS11	78828	64			
PC11	77428	4			
TC11	77028	4			
XX11	76688	16			2
XX11	76688	4	700		2
Storing Address Placing Vector	76878	1000			
PC11	77460	4	100	1000	1
PC11-PC11-1	77460	4	100	2	1
PC11-PC11-2	77460	4	100	2	1
PC11-PC11-3	77460	4	100	2	1
PC11-PC11-4	77460	4	100	2	1
PC11-PC11-5	77460	4	100	2	1
PC11-PC11-6	77460	4	100	2	1
PC11-PC11-7	77460	4	100	2	1
PC11-PC11-8	77460	4	100	2	1
PC11-PC11-9	77460	4	100	2	1
PC11-PC11-10	77460	4	100	2	1
PC11-PC11-11	77460	4	100	2	1
PC11-PC11-12	77460	4	100	2	1
PC11-PC11-13	77460	4	100	2	1
PC11-PC11-14	77460	4	100	2	1
PC11-PC11-15	77460	4	100	2	1
PC11-PC11-16	77460	4	100	2	1
PC11-PC11-17	77460	4	100	2	1
PC11-PC11-18	77460	4	100	2	1
PC11-PC11-19	77460	4	100	2	1
PC11-PC11-20	77460	4	100	2	1
PC11-PC11-21	77460	4	100	2	1
PC11-PC11-22	77460	4	100	2	1
PC11-PC11-23	77460	4	100	2	1
PC11-PC11-24	77460	4	100	2	1
PC11-PC11-25	77460	4	100	2	1
PC11-PC11-26	77460	4	100	2	1
PC11-PC11-27	77460	4	100	2	1
PC11-PC11-28	77460	4	100	2	1
PC11-PC11-29	77460	4	100	2	1
PC11-PC11-30	77460	4	100	2	1
PC11-PC11-31	77460	4	100	2	1
PC11-PC11-32	77460	4	100	2	1
PC11-PC11-33	77460	4	100	2	1
PC11-PC11-34	77460	4	100	2	1
PC11-PC11-35	77460	4	100	2	1
PC11-PC11-36	77460	4	100	2	1
PC11-PC11-37	77460	4	100	2	1
PC11-PC11-38	77460	4	100	2	1
PC11-PC11-39	77460	4	100	2	1
PC11-PC11-40	77460	4	100	2	1
PC11-PC11-41	77460	4	100	2	1
PC11-PC11-42	77460	4	100	2	1
PC11-PC11-43	77460	4	100	2	1
PC11-PC11-44	77460	4	100	2	1
PC11-PC11-45	77460	4	100	2	1
PC11-PC11-46	77460	4	100	2	1
PC11-PC11-47	77460	4	100	2	1
PC11-PC11-48	77460	4	100	2	1
PC11-PC11-49	77460	4	100	2	1
PC11-PC11-50	77460	4	100	2	1
PC11-PC11-51	77460	4	100	2	1
PC11-PC11-52	77460	4	100	2	1
PC11-PC11-53	77460	4	100	2	1
PC11-PC11-54	77460	4	100	2	1
PC11-PC11-55	77460	4	100	2	1
PC11-PC11-56	77460	4	100	2	1
PC11-PC11-57	77460	4	100	2	1
PC11-PC11-58	77460	4	100	2	1
PC11-PC11-59	77460	4	100	2	1
PC11-PC11-60	77460	4	100	2	1
PC11-PC11-61	77460	4	100	2	1
PC11-PC11-62	77460	4	100	2	1
PC11-PC11-63	77460	4	100	2	1
PC11-PC11-64	77460	4	100	2	1
PC11-PC11-65	77460	4	100	2	1
PC11-PC11-66	77460	4	100	2	1
PC11-PC11-67	77460	4	100	2	1
PC11-PC11-68	77460	4	100	2	1
PC11-PC11-69	77460	4	100	2	1
PC11-PC11-70	77460	4	100	2	1
PC11-PC11-71	77460	4	100	2	1
PC11-PC11-72	77460	4	100	2	1
PC11-PC11-73	77460	4	100	2	1
PC11-PC11-74	77460	4	100	2	1
PC11-PC11-75	77460	4	100	2	1
PC11-PC11-76	77460	4	100	2	1
PC11-PC11-77	77460	4	100	2	1
PC11-PC11-78	77460	4	100	2	1
PC11-PC11-79	77460	4	100	2	1
PC11-PC11-80	77460	4	100	2	1
PC11-PC11-81	77460	4	100	2	1
PC11-PC11-82	77460	4	100	2	1
PC11-PC11-83	77460	4	100	2	1
PC11-PC11-84	77460	4	100	2	1
PC11-PC11-85	77460	4	100	2	1
PC11-PC11-86	77460	4	100	2	1
PC11-PC11-87	77460	4	100	2	1
PC11-PC11-88	77460	4	100	2	1
PC11-PC11-89	77460	4	100	2	1
PC11-PC11-90	77460	4	100	2	1
PC11-PC11-91	77460	4	100	2	1
PC11-PC11-92	77460	4	100	2	1
PC11-PC11-93	77460	4	100	2	1
PC11-PC11-94	77460	4	100	2	1
PC11-PC11-95	77460	4	100	2	1
PC11-PC11-96	77460	4	100	2	1
PC11-PC11-97	77460	4	100	2	1
PC11-PC11-98	77460	4	100	2	1
PC11-PC11-99	77460	4	100	2	1
PC11-PC11-100	77460	4	100	2	1

*per channel xxx assignments

FIXED DEVICE ADDRESS AND VECTOR ASSIGNMENTS (CONT)

INTERRUPT DEVICE	Address Base	Address Size	Vector Term	Vector Size	No. of Lines/ Comments
RDSP	771008	8			8
RTDSD	772018	8			1
RTSDI-DA	767048	20			1
RTSDI-DA	772098	20			1
PLI1	776408	20			1 - 0007/0011
KMI1	772100	1			1
RTDI-DB	771008	8			1
RTDII-11	772080	20			1
RTDI/RTDII	772100	1			1
RTDI1	772008	8			1
RTI	772008	8			1
RTDII-8	776008	4	121000	8	1 - RTDI/RTDII-DB
RTDII-8	776008	4	121000	8	1 - RTDI/RTDII-DB
RTDI1/RTDII	772008	4	RTI	8	1
RTDI1	772008	4	RTI	8	1 - RTDI device
RTDII-11	772008	8			1
RTDII-11 Reserved			RTI	8	
RTDII-11 RTI Reserved			RTI	8	
RTDII-11 Reserved			RTI	8	
Instructions					
RTDII-11 Breakpoint/			RTI	8	
Trace Trap					
RTDII-11 I/O Trap			RTI	8	
RTDII-11 Error Out			RTI	8	
RTDII-11 FRT Trap			RTI	8	
RTDII-11 I/O LAMP			RTI	8	
RTDII-11 FLAG			RTI	8	
RTDII	777008	4			1
RTDII	777018	8	210	8	1
Reserved	778018	10			1
Reserved	778448	8			1
Reserved	778100	4			1
Reserved	778100	4			1
Reserved	778100	4			1
Reserved	778000	4			1
Reserved	778000	4			1
Reserved	778000	4			1
Reserved	778000	4			1
Reserved	778000	4			1
Reserved	778000	4			1
RTDII-11	778000	100			1
RTDII-11	778000	100			1
RTDII	778000	8	244	8	1
RTDII/RTDII-RTI	776100	12	170	8	1 - RTDI/RTDII/RTI
RTDII/RTDII	776400	8	210	8	1
RTDII/RTDII	776400	8	170	8	1
RTDII/RTDII	776400	8	80	8	1
RTDII	776400	8	170	8	1
RTDII/RTDII/RTI	776000	12	200	8	1 - RTDI/RTDII
RTDII/RTDII/RTI	776000	12	200	8	1 - RTDI/RTDII
RTDII	776000	16	200	8	1
RTDII/RTDII	776000	16	170	8	1 - RTDI/RTDII

FIXED DEVICE ADDRESS AND VECTOR ASSIGNMENTS (CONT)

IRTECLO Device	Address Range	Access Class	Vector Base	Vector Size	No. of Device Connections
RS11/211	777178	1	167	1	1
RS11/211	777178	4	167	1	1
RS1378 (Fixed Comp)			167	1	
RS1378 (Scheduling)			167	1	
RS1381					
System Software Reserved			113	1	
System Software Reserved			049	8	
TA (Module A)	777188	1	168	1	1
TL 1	777196	1	214	2	1
TL16	777196	16	214	2	1 - SR72/RT11
TRACOL	777200	17			1
TR11/RT11	777520	8	210	2	1
TR79	764804	4			1
TS11	777520	2	214	2	1
T. Device/17	777574	16	224	2	1 - SR72/RT11
T. NS	777580	1			1
TR78	777480	32	214	2	1 - SR72/RT11
US6	777154	2	156	2	1 - JCB Device
US711	777174	2	204	2	
US7 (VTR)	777182	1			256
US1	777172	1			
USAR18 (Vp)	777282	64			1
USAR18 - Reserved for OS/VS			164	1	
USAR18 (Reserved)			172	4	
USAR18 (Reserved)			214	4	
VS11	777804	4			4
VT48	777804	17			1
VZ11	777882	1..			2
VS11	777537	1	126	2	1

FLOATING ADDRESS UNIBUS DEVICES

Bank/ Owner	ADDRESS DEVICE	Address Size
1	LS11	4
2	TS11	4
3	TS13	4
4	LS11-LS11	4
5	LS11	4
6	LS11A	4
7	KS11	4
8	TS11	4
9	TS11-13	4
10	TS12	4
11	LS11A	4
12	LS11	4
13	MS11	4
14	MS11	4
15	MS11-13	4
16	MS11-13	4
17	MS11-13	4
18	KS11	4
19	KS11	4
20	KS11-13	4
21	MS11-13	4
22	MS11	4
23	TS11	4
24	MS11-13	4
25	MS11-13	4
26	LSA	4
27	LSA	16

FLOATING VECTOR UNIBUS DEVICES

Bus of Device	Device Location	Size	Bus of Device	Device Location	Size
1	EX11	4	35	EX11	2
1	EX10B	4	36	EX11-B	4
2	EX11	2	37	EX11-XTS-80K	2
4	EX11-A	4	38	EX11-C	4
2	EX11-B	4	39	EX11	2
2	EX112-B	10	40	EX11	2
4	EX11A/113-A	2	41	EX11-B	2
1	EX11	2	42	EX11-B	2
4	EX11-A	2	43	EX11-B	2
1	EX11	2	44	EX11	2
4	EX11-B/EX11	2	45	EX11-B	2
1	EX11-A	4	46	EX11/EX11	2
8	EX11-B	4	47	EX11	2
8	EX11-B	4	48	EX11	2
8	EX11-B	4			
10	EX11-B/EX11	4			
11	EX11	4			
12	EX11	2			
13	EX11	2			
14	EX11-A	4			
15	EX11	4			
16	EX11	4			
17	EX11	4			
18	EX11	4			
19	EX11	4			
20	EX11	4			
21	EX11-A	4			
22	EX11	4			
23	EX11	4			
24	EX11-B/EX11	4			
25	EX11	4			
26	EX11	4			
27	EX11	4			
28	EX11	4			
29	EX11	4			
30	EX11	4			
31	EX11	4			
32	EX11	4			
33	EX11	4			
34	EX11/EX11	2			

UMBUS SIGNAL DESCRIPTION

Signal Name	Description
Data Transfer Lines	
DB Address (A17:A0)	The address lines are provided by the master device to select a slave in an address of local register address. A17:A0's address is 16-bit wide (A0's specifies the lower or lower byte of the word of DATA transfer).
DB Data (D15:D0)	The data lines are enabled to transfer data information between the master and the slave.
Control (C1:C0)	Two control signals are provided by the master device to control the slave to perform data transfer operations. Provided directly in specified with respect to the master as follows:
	0 = 0V
R 2	DATA IN (DATAI) = a word of DATA is transferred to the master from the slave.
R 1	DATA IN READY (DATAI) = a DATA is supplied by a slave or DATA to the same location.
I 2	DATA OUT (DATAO) = a word of DATA is transferred from the master to the slave.
I 1	DATA OUT READY (DATAO) = a Data of DATA is transferred from the master to the slave. The READY or DATA OUT is specified by A0's.
parity (P1:P0)	The parity signals are provided by the slave as a DATA transfer as follows (P0 is not currently used, one is not defined):
	00 = 0V
	01 = 0V Error
	1 2 = Parity Error
	0 = Undefined
	1 = Undefined
Master Sync (MSYN)	MSYN is asserted by the master to indicate to the slave that valid address and control information along with data or a DATAI is present on the bus.
Slave Sync (SSYN)	SSYN is asserted by the slave in response to MSYN from the master. It indicates to the master that DATA's data has been placed from or DATAO's data is accepted on the DB data lines.

UNIBUS SIGNAL DESCRIPTION (CONT)

signal lines device pin

pin-to-pin pin-to-pin

Bus Request (BR#)	BR# is asserted by an I/O device for a bus transaction directly with master. The processor intervention is optional.
Master/Slave Grant (MSG#)	MSG# is the processor response to the BR#. It indicates to the I/O device that it will be the next MASTER master when the current master has completed its operation.
Bus Request Acknowledge (BRA#)	BR# is asserted by an I/O device for a processor interrupt. Processor information is required for servicing.
Bus Grant (MSG#)	MSG# is the processor response to a BR#. It is directed to the I/O device when it will be the next MASTER master. Only the highest request receives a bus grant of any size.

NOTES

All UNIBUS signals are asserted at a nominal ground plane except for the reset signals (RST#,RST#BAR) which are asserted at a nominal +3.5 V level.

Bus Acknowledge (BRA#)	BRA# is asserted by the BR# or BR# requesting device that has received a grant. This device becomes the new MASTER when the current master completes its operation and releases BR#.
Bus Busy (BB#)	BB# is asserted by the current master to indicate that the device is in use.
Interrupt (INT#)	INT# is asserted in a one of two by an interrupting device that has received a grant. It informs the CPU that an interrupt vector address is present on the DE bus lines. INT# is also an active concept of BR#.

UNIBUS SIGNAL DESCRIPTION (CONT)

Signal Name	Description
initialization strobe	
initialization strobe	INIT is asserted by bus DR0 and is passed to the DR1 and DR2 is asserted on the first INITBUS low. A system bootstrap is done if DR1 is asserted. The positive assertion for about 100 microseconds after the assertion of INIT.
DR bus (DR0)	DR0 is available from each system power supply and is asserted if no bus-external address occurs. DR0 on the first INITBUS asserts DR1 to both the first and second DRBUS. DR0 on the second INITBUS asserts DR2 status on the DR1 if the DR1 attempts to access a second DRBUS device.
DR bus (DR1)	DR1 works as an incoming power address. DR0 on the first INITBUS initiates the power-up of DR1 device and may be used in peripheral devices to facilitate operations and power down. DR1 on the second DRBUS passes the DR1 to DR2 status. The procedure of the DR1 bus is DR2 of the DR1 device.

UNIBUS CABLE PIN ASSIGNMENTS

Pin	Signal Name	Pin	Signal Name
A73	TR78 L	B41	TR77 R
A72	TR78 R	B42	TR77 L
A71	TR77 L	B43	TR76 R
A62	CR0770	B44	CR0760
A61	TR67 F	B45	TR67 L
A59	GR0760	B47	CR0750
A51	TR67 F	B48	CR0740
A52	TR67 L	B49	TR66 R
A53	TR66 R	B50	TR66 L
A54	TR66 L	B51	TR65 R
A55	TR65 R	B52	TR65 L
A56	TR65 L	B53	TR64 R
A57	TR64 R	B54	TR64 L
A58	TR64 L	B55	TR63 R
A59	TR63 R	B56	TR63 L
A60	TR63 L	B57	TR62 R
A61	TR62 R	B58	TR62 L
A62	TR62 L	B59	TR61 R
A63	TR61 R	B60	TR61 L
A64	TR61 L	B61	TR60 R
A65	TR60 R	B62	TR60 L
A66	TR60 L	B63	TR59 R
A67	TR59 R	B64	TR59 L
A68	TR59 L	B65	TR58 R
A69	TR58 R	B66	TR58 L
A70	TR58 L	B67	TR57 R
A71	TR57 R	B68	TR57 L
A72	TR57 L	B69	TR56 R
A73	TR56 R	B70	TR56 L
A74	TR56 L	B71	TR55 R
A75	TR55 R	B72	TR55 L
A76	TR55 L	B73	TR54 R
A77	TR54 R	B74	TR54 L
A78	TR54 L	B75	TR53 R
A79	TR53 R	B76	TR53 L
A80	TR53 L	B77	TR52 R
A81	TR52 R	B78	TR52 L
A82	TR52 L	B79	TR51 R
A83	TR51 R	B80	TR51 L
A84	TR51 L	B81	TR50 R
A85	TR50 R	B82	TR50 L
A86	TR50 L	B83	TR49 R
A87	TR49 R	B84	TR49 L
A88	TR49 L	B85	TR48 R
A89	TR48 R	B86	TR48 L
A90	TR48 L	B87	TR47 R
A91	TR47 R	B88	TR47 L
A92	TR47 L	B89	TR46 R
A93	TR46 R	B90	TR46 L
A94	TR46 L	B91	TR45 R
A95	TR45 R	B92	TR45 L
A96	TR45 L	B93	TR44 R
A97	TR44 R	B94	TR44 L
A98	TR44 L	B95	TR43 R
A99	TR43 R	B96	TR43 L
A100	TR43 L	B97	TR42 R
A101	TR42 R	B98	TR42 L
A102	TR42 L	B99	TR41 R
A103	TR41 R	B100	TR41 L
A104	TR41 L	B101	TR40 R
A105	TR40 R	B102	TR40 L
A106	TR40 L	B103	TR39 R
A107	TR39 R	B104	TR39 L
A108	TR39 L	B105	TR38 R
A109	TR38 R	B106	TR38 L
A110	TR38 L	B107	TR37 R
A111	TR37 R	B108	TR37 L
A112	TR37 L	B109	TR36 R
A113	TR36 R	B110	TR36 L
A114	TR36 L	B111	TR35 R
A115	TR35 R	B112	TR35 L
A116	TR35 L	B113	TR34 R
A117	TR34 R	B114	TR34 L
A118	TR34 L	B115	TR33 R
A119	TR33 R	B116	TR33 L
A120	TR33 L	B117	TR32 R
A121	TR32 R	B118	TR32 L
A122	TR32 L	B119	TR31 R
A123	TR31 R	B120	TR31 L
A124	TR31 L	B121	TR30 R
A125	TR30 R	B122	TR30 L
A126	TR30 L	B123	TR29 R
A127	TR29 R	B124	TR29 L
A128	TR29 L	B125	TR28 R
A129	TR28 R	B126	TR28 L
A130	TR28 L	B127	TR27 R
A131	TR27 R	B128	TR27 L
A132	TR27 L	B129	TR26 R
A133	TR26 R	B130	TR26 L
A134	TR26 L	B131	TR25 R
A135	TR25 R	B132	TR25 L
A136	TR25 L	B133	TR24 R
A137	TR24 R	B134	TR24 L
A138	TR24 L	B135	TR23 R
A139	TR23 R	B136	TR23 L
A140	TR23 L	B137	TR22 R
A141	TR22 R	B138	TR22 L
A142	TR22 L	B139	TR21 R
A143	TR21 R	B140	TR21 L
A144	TR21 L	B141	TR20 R
A145	TR20 R	B142	TR20 L
A146	TR20 L	B143	TR19 R
A147	TR19 R	B144	TR19 L
A148	TR19 L	B145	TR18 R
A149	TR18 R	B146	TR18 L
A150	TR18 L	B147	TR17 R
A151	TR17 R	B148	TR17 L
A152	TR17 L	B149	TR16 R
A153	TR16 R	B150	TR16 L
A154	TR16 L	B151	TR15 R
A155	TR15 R	B152	TR15 L
A156	TR15 L	B153	TR14 R
A157	TR14 R	B154	TR14 L
A158	TR14 L	B155	TR13 R
A159	TR13 R	B156	TR13 L
A160	TR13 L	B157	TR12 R
A161	TR12 R	B158	TR12 L
A162	TR12 L	B159	TR11 R
A163	TR11 R	B160	TR11 L
A164	TR11 L	B161	TR10 R
A165	TR10 R	B162	TR10 L
A166	TR10 L	B163	TR9 R
A167	TR9 R	B164	TR9 L
A168	TR9 L	B165	TR8 R
A169	TR8 R	B166	TR8 L
A170	TR8 L	B167	TR7 R
A171	TR7 R	B168	TR7 L
A172	TR7 L	B169	TR6 R
A173	TR6 R	B170	TR6 L
A174	TR6 L	B171	TR5 R
A175	TR5 R	B172	TR5 L
A176	TR5 L	B173	TR4 R
A177	TR4 R	B174	TR4 L
A178	TR4 L	B175	TR3 R
A179	TR3 R	B176	TR3 L
A180	TR3 L	B177	TR2 R
A181	TR2 R	B178	TR2 L
A182	TR2 L	B179	TR1 R
A183	TR1 R	B180	TR1 L

MEA PHYSICAL ADDRESS SPACE

EMI DATA LONGWORD	
MEA-40 INT. REGISTERS	F20400
MEA-40 EXT. REGISTERS	F0F400
MEA-40 MAP REGISTERS	F20000
UNUSED	F28000
	F29F00
MEA-41 INT. REGISTERS	F2A000
MEA-41 EXT. REGISTERS	F0A400
MEA-41 MAP REGISTERS	F2A000
UNUSED	F2B100
	F2BFF0
MEA-42 INT. REGISTERS	F2C000
MEA-42 EXT. REGISTERS	F0C400
MEA-42 MAP REGISTERS	F2C000
UNUSED	F2D000
	F2DFF0

TC-8428

MBA AND MASSBUS REGISTER SUMMARY

REG. NO.	REG. NAME	REG. TYPE	REG. VALUE	REG. ADDRESS	REG. DATA
0000	00000000	0000	00000000	00000000	00000000
0001	00000001	0000	00000001	00000001	00000001
0002	00000002	0000	00000002	00000002	00000002
0003	00000003	0000	00000003	00000003	00000003
0004	00000004	0000	00000004	00000004	00000004
0005	00000005	0000	00000005	00000005	00000005
0006	00000006	0000	00000006	00000006	00000006
0007	00000007	0000	00000007	00000007	00000007
0008	00000008	0000	00000008	00000008	00000008
0009	00000009	0000	00000009	00000009	00000009
0010	0000000A	0000	0000000A	0000000A	0000000A
0011	0000000B	0000	0000000B	0000000B	0000000B
0012	0000000C	0000	0000000C	0000000C	0000000C
0013	0000000D	0000	0000000D	0000000D	0000000D
0014	0000000E	0000	0000000E	0000000E	0000000E
0015	0000000F	0000	0000000F	0000000F	0000000F
0016	00000010	0000	00000010	00000010	00000010
0017	00000011	0000	00000011	00000011	00000011
0018	00000012	0000	00000012	00000012	00000012
0019	00000013	0000	00000013	00000013	00000013
0020	00000014	0000	00000014	00000014	00000014
0021	00000015	0000	00000015	00000015	00000015
0022	00000016	0000	00000016	00000016	00000016
0023	00000017	0000	00000017	00000017	00000017
0024	00000018	0000	00000018	00000018	00000018
0025	00000019	0000	00000019	00000019	00000019
0026	0000001A	0000	0000001A	0000001A	0000001A
0027	0000001B	0000	0000001B	0000001B	0000001B
0028	0000001C	0000	0000001C	0000001C	0000001C
0029	0000001D	0000	0000001D	0000001D	0000001D
0030	0000001E	0000	0000001E	0000001E	0000001E
0031	0000001F	0000	0000001F	0000001F	0000001F
0032	00000020	0000	00000020	00000020	00000020
0033	00000021	0000	00000021	00000021	00000021
0034	00000022	0000	00000022	00000022	00000022
0035	00000023	0000	00000023	00000023	00000023
0036	00000024	0000	00000024	00000024	00000024
0037	00000025	0000	00000025	00000025	00000025
0038	00000026	0000	00000026	00000026	00000026
0039	00000027	0000	00000027	00000027	00000027
0040	00000028	0000	00000028	00000028	00000028
0041	00000029	0000	00000029	00000029	00000029
0042	0000002A	0000	0000002A	0000002A	0000002A
0043	0000002B	0000	0000002B	0000002B	0000002B
0044	0000002C	0000	0000002C	0000002C	0000002C
0045	0000002D	0000	0000002D	0000002D	0000002D
0046	0000002E	0000	0000002E	0000002E	0000002E
0047	0000002F	0000	0000002F	0000002F	0000002F
0048	00000030	0000	00000030	00000030	00000030
0049	00000031	0000	00000031	00000031	00000031
0050	00000032	0000	00000032	00000032	00000032
0051	00000033	0000	00000033	00000033	00000033
0052	00000034	0000	00000034	00000034	00000034
0053	00000035	0000	00000035	00000035	00000035
0054	00000036	0000	00000036	00000036	00000036
0055	00000037	0000	00000037	00000037	00000037
0056	00000038	0000	00000038	00000038	00000038
0057	00000039	0000	00000039	00000039	00000039
0058	0000003A	0000	0000003A	0000003A	0000003A
0059	0000003B	0000	0000003B	0000003B	0000003B
0060	0000003C	0000	0000003C	0000003C	0000003C
0061	0000003D	0000	0000003D	0000003D	0000003D
0062	0000003E	0000	0000003E	0000003E	0000003E
0063	0000003F	0000	0000003F	0000003F	0000003F
0064	00000040	0000	00000040	00000040	00000040
0065	00000041	0000	00000041	00000041	00000041
0066	00000042	0000	00000042	00000042	00000042
0067	00000043	0000	00000043	00000043	00000043
0068	00000044	0000	00000044	00000044	00000044
0069	00000045	0000	00000045	00000045	00000045
0070	00000046	0000	00000046	00000046	00000046
0071	00000047	0000	00000047	00000047	00000047
0072	00000048	0000	00000048	00000048	00000048
0073	00000049	0000	00000049	00000049	00000049
0074	0000004A	0000	0000004A	0000004A	0000004A
0075	0000004B	0000	0000004B	0000004B	0000004B
0076	0000004C	0000	0000004C	0000004C	0000004C
0077	0000004D	0000	0000004D	0000004D	0000004D
0078	0000004E	0000	0000004E	0000004E	0000004E
0079	0000004F	0000	0000004F	0000004F	0000004F
0080	00000050	0000	00000050	00000050	00000050
0081	00000051	0000	00000051	00000051	00000051
0082	00000052	0000	00000052	00000052	00000052
0083	00000053	0000	00000053	00000053	00000053
0084	00000054	0000	00000054	00000054	00000054
0085	00000055	0000	00000055	00000055	00000055
0086	00000056	0000	00000056	00000056	00000056
0087	00000057	0000	00000057	00000057	00000057
0088	00000058	0000	00000058	00000058	00000058
0089	00000059	0000	00000059	00000059	00000059
0090	0000005A	0000	0000005A	0000005A	0000005A
0091	0000005B	0000	0000005B	0000005B	0000005B
0092	0000005C	0000	0000005C	0000005C	0000005C
0093	0000005D	0000	0000005D	0000005D	0000005D
0094	0000005E	0000	0000005E	0000005E	0000005E
0095	0000005F	0000	0000005F	0000005F	0000005F
0096	00000060	0000	00000060	00000060	00000060
0097	00000061	0000	00000061	00000061	00000061
0098	00000062	0000	00000062	00000062	00000062
0099	00000063	0000	00000063	00000063	00000063
0100	00000064	0000	00000064	00000064	00000064

MBA REGISTER OFFSETS

MBA PHYSICAL DASP ADDRESSES

PGA Number	Physical Base Address (Hex)	Offset Hex	Offset Dec	Offset Hex	Offset Dec
PGA 0	100000	00	0	00	0
PGA 1	200000	00	0	00	0
PGA 2	300000	00	0	00	0

*Spanned by level 15.

MBA INTERNAL REGISTER OFFSETS

PGA Address Internal Register	Offset to PGA Physical Base Address
00 - Configuration/Status (R/W)	000 Read Only
01 - Control (R/W)	004 Read/Write
02 - Victim Address (R/W)	008 Read Only
03 - Byte Count (R/W)	00C Read/Write
04 - Diagnostic (R/W)	010 Read/Write
05 - Address Register Address	014 Read/Write
06 - Configuration/Status (R/W)	018 Address Register to CPU
	020 Read Only

MBA MAP REGISTER OFFSETS

PGA Address MAP Register	Offset to PGA Physical Base Address
MAP 00	000
MAP 01	004
--	--
--	--
--	--
MAP 0E	0F0
MAP 0F	0F4

The PGA MAP register addresses are reserved for addresses 00000000 through 0000000F (hex) (00000000-0000000F).

MBA REGISTER OFFSETS (CONT)

MBA EXTERNAL (MANSBUS) REGISTER OFFSETS

Mansbus Register	Mansbus Address							
	0	1	2	3	4	5	6	7
00	000	000	000	000	000	000	000	000
01	004	004	004	004	004	004	004	004
02	008	008	008	008	008	008	008	008
03	00C	00C	00C	00C	00C	00C	00C	00C
04	010	010	010	010	010	010	010	010
05	014	014	014	014	014	014	014	014
06	018	018	018	018	018	018	018	018
07	01C	01C	01C	01C	01C	01C	01C	01C
08	020	020	020	020	020	020	020	020
09	024	024	024	024	024	024	024	024
0A	028	028	028	028	028	028	028	028
0B	02C	02C	02C	02C	02C	02C	02C	02C
0C	030	030	030	030	030	030	030	030
0D	034	034	034	034	034	034	034	034
0E	038	038	038	038	038	038	038	038
0F	03C	03C	03C	03C	03C	03C	03C	03C
10	040	040	040	040	040	040	040	040
11	044	044	044	044	044	044	044	044
12	048	048	048	048	048	048	048	048
13	04C	04C	04C	04C	04C	04C	04C	04C
14	050	050	050	050	050	050	050	050
15	054	054	054	054	054	054	054	054
16	058	058	058	058	058	058	058	058
17	05C	05C	05C	05C	05C	05C	05C	05C
18	060	060	060	060	060	060	060	060
19	064	064	064	064	064	064	064	064
1A	068	068	068	068	068	068	068	068
1B	06C	06C	06C	06C	06C	06C	06C	06C
1C	070	070	070	070	070	070	070	070
1D	074	074	074	074	074	074	074	074
1E	078	078	078	078	078	078	078	078
1F	07C	07C	07C	07C	07C	07C	07C	07C

NOTE: The offset value, when added to the bus address base address, is transferred to the drive unit and register select input on the Mansbus control bus.

MASSBUS SIGNAL DESCRIPTION

Signal Name	Description
Data Bus Signals	
<p> Address Data Strobe (ADSD) (288) </p>	<p> The parallel data path transmits bus data between the M80 and the drive. The M80 addresses 10 bits to the drive at a time and the address data strobe enables the data transfer. The address data strobe is active low and is asserted by the M80 for writes to drives that require parity checking. </p>
<p> Data Strobe Parity (DPS) </p>	<p> DPS is the complementary signal to data bus data. It is asserted by the M80 on writes to drive parity transmitters. It is asserted by the drive on read parity drive (RDPC) or write check (WDPC) transmitters. </p>
<p> DR </p>	<p> When a data transfer command is written to a drive's control register, the drive connects to the data bus and asserts DR. DR is then deasserted by the M80 to start transmission. DR is asserted by the drive at the end of each block of sectors on the trailing edge of data. If DR is not deasserted, the format on the bus may be corrupted. If not, the operation terminates. </p>
<p> Completed (DPC) </p>	<p> DPC is asserted by the drive that has received a data transfer command and is deasserted by the M80 bus in a sector. If the drive is not able to get DPC because of an error condition, the M80 status set and bit is set. On the M80 status register, DPC is negated on the trailing edge of the last bit of the operation. </p>
<p> End of Block </p>	<p> EOB is asserted by the drive for two micro-seconds after the final bit of each block of sectors. EOB may be asserted earlier in error conditions when it is necessary to terminate the operation immediately. </p>
<p> Exception (DPE) </p>	<p> DPE is asserted by the active drive when an abnormal condition occurs during data transmission. EAC is asserted on systems that are not on the trailing edge of data. Also, on the assertion of data, the EAC is set in the M80 status register. </p> <p> EAC deasserts when asserts in the active drive during data transfer from sector of status message signaled by the M80 line. An error on drive does not assert EAC during data transfers that occur in sectors until the operation has been aborted or terminated and the drive is no longer active. </p>

MASBUS SIGNAL DESCRIPTION (CONT)

Signal Name	Description
Drive Clock (MCLK)	MCLK is generated by the active data to control the data bus data clocking in the MSB. On read from drive (RD) or write back (WR) operation, the drive changes duty on the acquisition of MCLK. The MUA then clocks data on the acquisition of MCLK.
Active Clock (MACK)	The MUA provides ACK and returns it to the drive as MCK on write to drive (WR) operation. The MUA changes data on the acquisition of MCK. The drive then clocks data on the acquisition of MCLK.
Control Bus Section	
Control Bus Data (MCDATA)	The parallel data path transmits control and data information between the MUA and the drive. A CPU read or write to a drive's control/status logic.
Control Bus Ready (MCRDY)	CRA is the addressable bit for control bus data. It is asserted by the MUA on a CPU write to a drive's control or status register. It is asserted by the drive on a CPU read of a drive's control or status register.
Control Bus Drive (MCDRV)	CDRV is asserted by the MUA when the register is a CPU write (read the MUA to the device). CDRV is asserted by the MUA when the register is a CPU read (from the drive to the MUA).
Drive Select (MDSSEL)	The MUA asserts a three-bit code to select one of eight available drive units.
Register Select (MRSSEL)	The MUA asserts a five-bit code to select a register within the drive.
Command (MCOM)	COM is asserted by the MUA to perform a control bus transfer with a drive. It is asserted after the MS, DS, and RSTN lines are settled (and the control bus data lines are settled) and transfer to a CPU read.
Response (MRES)	RES is asserted by the drive in response to COM from the MUA. It is asserted when the drive clocks control bus data to its selected register on a CPU write. It is asserted after delay to control data - asserted on the control bus data line from the selected register on a CPU read. It is negated when the register ID, MS, and DS is received from the MUA.

MASSBUS SIGNAL DESCRIPTION (CONT)

Signal Name	Description
Attention (ATTN)	<p>ATTN is asserted by the controller drive as a result of a change of status such as the completion of a sector transfer or error. ATTN is also asserted by a previously active drive when its 20 bit ID address either indicates that program an error.</p> <p>ATTN is a request for services to processor interrupt. The attention active signal is used by the controller drive to determine the request by drive(s).</p>
Track Lias (TRML)	<p>TRML is asserted by the MSA to indicate a system error of bit 40. TR is asserted as a system parameter by writing a one to the TRML bit of the MSA control register. It must not be written while the drive is performing the action of which execution of the current command and perform drive's has caused condition.</p> <p>In a dual port drive, the drive accepts the TRML command only from the MSA host in control. If asserts the unusual track error condition when in the idle state.</p>
FSM	<p>FSM is asserted by the MSA to indicate that a sector loss fault condition exists or that the MSA is in the performance mode while FSM is asserted, all data transfer operation of the DMTS or DMS signal's.</p>

MASSBUS CABLE PIN ASSIGNMENTS

Label	Pin	Polarity	Signal Name
1	1	-	MSB - 008
2	2	+	
3	3	-	MSB - 001
4	4	-	
5	5	-	MSB - 002
6	6	-	
7	7	-	MSB - 003
8	8	-	
9	9	-	MSB - 007
10	10	+	
11	11	+	
12	12	+	MSB - 005
13	13	-	
14	14	+	MSB - 010
15	15	+	
16	16	+	MSB - 021
17	17	-	
18	18	-	MSB - 020
19	19	+	
20	20	+	MSB - 024
21	21	-	
22	22	-	MSB - 026
23	23	+	
24	24	+	MSB - 028
25	25	-	
26	26	-	MSB - 023
27	27	+	
28	28	+	MSB - 011
29	29	-	
30	30	+	MSB - 017
31	31	-	
32	32	-	MSB - 014
33	33	+	
34	34	+	MSB - 010
35	35	+	
36	36	+	MSB - 009
37	37	-	
38	38	+	MSB - 006
39	39	-	
40	40	0kV	Signal Ground

*Alternate pin assignments

NOTE

MASSBUS cables are terminated on all conductors.

MASSBUS CABLE PIN ASSIGNMENTS (CONT)

170 Cable	Pin*	Polarity	Signal Name
12B15 B	5	-	MASS DR0
	6	-	MASS DR1
	7	-	MASS DR2
	8	-	MASS DR3
	9	-	MASS DR4
	10	-	MASS DR5
	11	-	MASS DR6
	12	-	MASS DR7
	13	-	MASS DR8
	14	-	MASS DR9
	15	-	MASS DR10
	16	-	MASS DR11
	17	-	MASS DR12
	18	-	MASS DR13
	19	-	MASS DR14
	20	-	MASS DR15
	21	-	MASS DR16
	22	-	MASS DR17
	23	-	MASS DR18
	24	-	MASS DR19
	25	-	MASS DR20
	26	-	MASS DR21
	27	-	MASS DR22
	28	-	MASS DR23
	29	-	MASS DR24
	30	-	MASS DR25
	31	-	MASS DR26
	32	-	MASS DR27
	33	-	MASS DR28
	34	-	MASS DR29
	35	-	MASS DR30
	36	-	MASS DR31
	37	-	MASS DR32
	38	-	MASS DR33
	39	-	MASS DR34
	40	-	MASS DR35
	41	-	MASS DR36
	42	-	MASS DR37
	43	-	MASS DR38
	44	-	MASS DR39
	45	-	MASS DR40
	46	-	MASS DR41
	47	-	MASS DR42
	48	GND	Ground

MASSBUS CABLE PIN ASSIGNMENTS

NOTE

MASSBUS CABLES ARE INSTALLED AND LABELED.

MASSBUS CARLE PIN ASSIGNMENTS (CONT)

Y/O Code	Pin	Definition	Signal Name
EXP-8-0	A 1	-	MASS 012
	Z 2	+	MASS 011
	C 3	+	MASS 013
	D 4	-	MASS 014
	E 5	+	MASS 015
	H 6	+	MASS 016
	K 7	-	MASS 018
	L 8	+	MASS 017
	J 9	+	MASS 019
	M 10	-	MASS 020
	P 11	+	MASS 021
	R 12	+	MASS 022
	S 13	-	MASS 023
	T 14	+	MASS 024
	V 15	+	MASS 025
	W 16	+	MASS 026
	X 17	-	MASS 027
	Y 18	-	MASS 028
	AA 19	+	MASS 029
	BB 20	-	MASS 030
	CC 21	+	MASS 031
	DD 22	+	MASS 032
	EE 23	+	MASS 033
	FF 24	+	MASS 034
	GG 25	-	MASS 035
	HH 26	+	MASS 036
	II 27	+	MASS 037
	JJ 28	+	MASS 038
	KK 29	+	MASS 039
	LL 30	+	MASS 040
	MM 31	+	MASS 041
	NN 32	+	MASS 042
OO 33	+	MASS 043	
PP 34	+	MASS 044	
QQ 35	+	MASS 045	
RR 36	+	MASS 046	
SS 37	+	MASS 047	
TT 38	+	MASS 048	
UU 39	+	MASS 049	
VV 40	+	MASS 050	

*Alternate pin assignments:

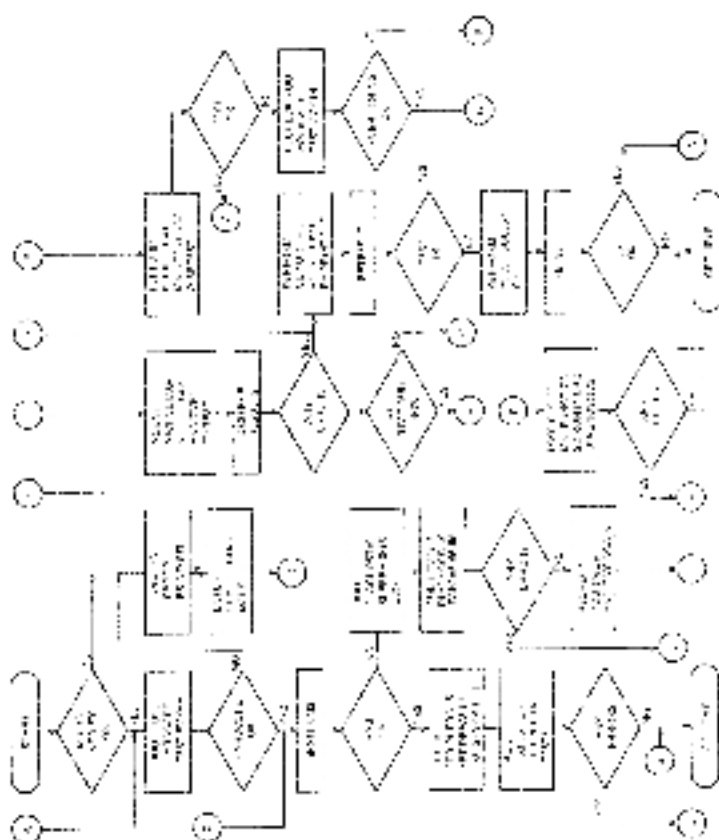
KIT

MASSBUS cables are installed as shown.

CHAPTER 9
TROUBLESHOOTING AIDS



SYSTEM TROUBLESHOOTING FLOW



UNIBUS TROUBLESHOOTING WITH THE UET OR IPEC

First DEVICE - The following sequence of unibus commands causes the UET to execute a single MPP read (DATA transfer) from memory.

1. `UNIBUS 27 1`
`UNIBUS/M/P 832184 1`
`UNIBUS/M/P 832188 00000000`

`UNIBUS/M/P 1823 1204000`
`UNIBUS/M/P 832188 8`
`UNIBUS/M/P 832184 1`

Initial the CPU
 output the MPP 1
 Set up bus MPP address 8 for
 validity, MPP 1, MPP 1887
 Load data to memory 123
 Set MPP bus address to 8
 Set MPP bus 1000 bit

2. Wait the results:

`UNIBUS 28 100` Reading bus data register
 should return 8475 as data

3. Increment the bus address register:

`UNIBUS/M/P 832188 2` Set bus address to 2
`UNIBUS/M/P 832184 1` Set MPP bus 1001 bit

4. Wait the results:

`UNIBUS 28 100` Execute MPP data register
 should return 1234 as data

Second DEVICE - This sequence causes the UET to execute a single memory.

1. `UNIBUS 27 1`
`UNIBUS/M/P 832184 1`
`UNIBUS/M/P 832188 00000000`

`UNIBUS/M/P 1807 1204000`
`UNIBUS/M/P 832188 8`
`UNIBUS/M/P 832184 1`

Initialise CPU
 output MPP 1
 Set up bus MPP address 8 for
 validity, MPP 1, MPP 1887
 Load data to memory 123
 Set bus bus address to 8
 Set MPP bus 1001 bit

2. Wait the results:

`UNIBUS 28 100` Reading bus data register
 should return 1234 as data

3. Increment the bus address register:

`UNIBUS/M/P 832188 2` Set bus address to 2
`UNIBUS/M/P 832184 1` Set MPP bus 1001 bit

4. Wait the results:

`UNIBUS 28 100` Reading bus data register
 should return 1234 as data

UNIBUS TROUBLESHOOTING WITH THE JET OR IPED (CONT)

The following subroutines can be used in a user program to find correct data path and MAP address combinations.

MAP address:	DEC	HEX	
	418804	E32F80	MAP physical base address
	418804	E32E84	(MAP locations are centered
	-	-	on increments of 4)
	-	-	
	E32F28	F02F00	
	F1882C	E32F0C	
Map data:	DTF -	88230700	direct data path
	DTF 1 -	88280700	
	DTF 2 -	88480700	
	DTF 3 -	88580700	
CR data:	CSI	CSI	
	758700	212020	Base (see DTF for the DDT)
	758704	757870	CR0 1 (see DTF)
	758708	252070	CR0 1 (see DTF 2)
	75870C	757870	CR0 1 (see DTF 3)
Breakpoint addresses:	JET	TRU	
	EPF667	F02F60	Bus address register
	EPF669	F02F62	Bus mask register
	EPF66A	F02F63	TRU
	EPF66B	EPF667	TRU CR0, JET TRU
			mask register

Further operations can be performed using control bits of the following control register:

- CR020 = 0011000 bits
- CR0210 = 00100000000000000000000000000000
- CR0212 = 00101000000000000000000000000000

CR0	CR0	function
0	0	CR01
0	1	CR01L
	2	CR01R
	-	CR01B

To do a JET or TRU with a user program, load the bus data register in one of the memory banks with one word of data (55555555) and CR020 or CR0212.

THE FILE UTILITY

FROM may be used to copy files from FROM to disk or from disk to disk. It may be used to build new files or when existing files have been corrupted. It provides both hard to use (plain) and easy to use (Lisp) ways for the user to interact with files.

Take the tape to copy from the source file drive to a FROM cassette, do the following (FROM runs only 'DIR' and does not use controller codes):

```
1 FROM SYS$SYSTEM:SYS$DISK
SYS$DISK:CONSOLE:CONSOLE
SYS$DISK:DIR
1 FROM SYS$SYSTEM:SYS$DIR
1 FROM SYS$DISK:SYS$DIR:DIR
1 FROM FROM
FROM:1/DIR/1          (first tape directory = opt 0001)
FROM:1/DIR/2         (second tape directory = opt 0001)
FROM:1/DIR/3        (third tape directory = opt 0001)
      (to device)      (from device)
```

BY default codes

```
TR = tape mode (TR, RT, RR, DR, DR, DR, DR)
LD = delete special file
LD = formatted binary (DR, DR, DR, DR)
DR = formatted ASCII (DR) error extensions
DR = multiple file to disk (file naming disk)
DR = tape mode storage configuration
DR = RLL format (system)
DR = RLL format (user)
```

```
END)          (when operation is complete)
1
```

page to disk (RLL) = To copy from a tape cassette to the source disk, do the following:

```
1 FROM SYS$SYSTEM:SYS$DISK
SYS$DISK:CONSOLE:CONSOLE
SYS$DISK:DIR
1 FROM SYS$SYSTEM:SYS$DIR
1 FROM SYS$DISK:SYS$DIR:DIR
1 FROM FROM
FROM:1/DIR/1 = SYS$DISK:SYS$DIR/DIR
      (to device)      (from device)
```

```
END)          (when operation is complete)
1
```

THE WRITEROOT UTILITY

The WRITEROOT utility may be used to write a boot block on any bootable disk. A booting operation is normally performed from the boot block that is block 2 of the system disk. If block 2 is bad, the system can only be booted from the 1088, which the system is running upon; the boot block can be rewritten using WRITEROOT.

NOTE
The operator must have LOG_IO privilege to use the WRITEROOT facility.

To exit WRITEROOT, type the following command:

```
Q RUN SYS$SYSTEM:WRITEROOT
```

The program then asks three questions:

1. Target system device:

Enter the name of the device that will have the boot block written and the boot block size if not VMS/386 (for example: DKA0 or DSK0: [diskname]). Specify the target system device (disk) as for any other VMS/386 device.

```
ad = device type  
c = controller designation  
n = unit number
```

An example: 'DKA0' or 'DSK0' and 'S' or 'L' for controller A.

2. Total size of boot file name:

To rewrite the boot block, press `BOOTFILE=bootfile`.

3. Boot load address or primary bootstrap in hex:

To rewrite the boot block, press `BOOTADDR=address` in hex.

WRITEROOT then writes the boot file specified on the first line to the address specified on the third line.

THE WRITEBOOT UTILITY (CONT)

WRITEBOOT is to be used to write a boot block on a CDROM containing data using these capabilities:

Target device address: 0110000000

Block = 0000 (for normal boot) or 0001 (for boot)

Block size of boot file code: 1 or 2

Block = 1x if RIGHT is pressed

Enter raw address of primary bootblock in hex:

00000000 (if RIGHT is pressed)

Block 1 address and 2 addresses are the only bootable programs from CDROM. Your bootable programs are currently 0000, 0001 and 0002. To write bootable data using these addresses:

Filename	Size	Start Address	Description
BOOTABLE001	1	0000	Bootable CDROM
BOOTABLE002	1	0001	IB and cache
BOOTABLE003	1	0002	Alternate operation
BOOTABLE004	1	0003	BOOTABLE address

MACHINE CHECKS

The CHECKR bit of the CR3, CR4, CR8, and CR9 registers multiple to all cache parity errors. These indications may also appear in operation registered hardware checkpoints when the system error log is enabled, although there is nothing wrong with the system.

CHEKRR is only valid when the system is in at the machine check status after one of the following:

- Memory error
- TD parity error
- Cache parity error
- Control plane parity error

CHEKRR provides the location of MCHKRR registers of the CR003 address. The MCHKRR registers are 32-bit registers that follow the logic plane error and failure indications whenever occur when the error code does an MCHKR from this register. The format machine checks are included here for instructions.

TRANSLATION BUFFER OR BUS ERROR

This machine check was caused by mapping a non-existent page with a 6000000 system service and then accessing that page in user mode.

Exception PC	00000000	
Error PV	00000000	(interrupt priority level = 2 processor state = user P state code = 0000)
Summary code	00000000	Translation buffer or bus error
VA Lupa code	00000000	
PC at error	00000000	
ADR	00000000	
ERR	00000000	Opn code = 0000 Vidcode Raid
BTM	00000000	
EBM	00000000	
ESM	00000000	Memory error
ERR	00000000	General reference Bus error

MACHINE CHECKS (CONT)

In the case of a machine check, logical addresses are passed to the VAX 11/780, no translated address is passed onto the stack. This is because the physical address format is contained within gate arrays and there is no direct method of obtaining the physical address.

The MCR's register may be used to determine what type of exception machine check occurred. The bits are defined as follows:

	CR0	CR2	CR3	CR7
MSB:	ERR TRR	TR PARITY	R	SE ERRSR

CR0 and CR2 are in the stack layout, so error occurred transferring address for read data. CR3 register layout are then as read as determining the type of memory error.

The CR7 register will indicate what type of error occurred. Bit CR7 indicates a memory write bit CR7 indicates an unacceptable stack. Unacceptable errors will interrupt the processor. CR7 CR0 CR2 and CR3 error write unacceptable errors will cause machine checks.

	CR0	CR2	CR3	CR7
MSB	ERR ERRSR	ERRSR ERRSR	ERR ERRSR	ERR ERRSR

If the unacceptable error bit in the CR7 is 1, this exception is not be caused but it was a reference to a non-existent location. If the CR7 parity error bit CR7 in the MCR's register is 1, a non-zero type of parity error caused the non-existent.

The MCR's register can be used to determine what the error was. If machine check was not caused by a memory error or SE parity error, a cache parity error is the only other possibility. The CR7 contains the data to test parity information.

Several other machine checks may occur in the VAX-11/780.

- A. Parity parameter = 107. This error occurs only if the instruction's opcode RRR is not accepted by CR7. The parity error only occurs if there is no CR parity error and the CR7 field is 0. This may cause a jump instead of the instruction output.
- B. Parity parameter = 106. This is a microsequencing error that occurs in the microcode jump to filler code in the control stack. CR7 contains the error code of filler code occurred. This only happens if there is no CR parity error.

MACHINE CHECKS (CONT)

The following description illustrates the last possible occurrence of machine checks. The control store parity error code that the VAX-11/750 machine check input device has indicated is 07 where the 07 parity error occurred pursuant to the check. This information cannot be saved because the VAX-11/750 does not have a 32-bit save register like the VAX-11/800. If, in addition, however, to the present information 05 parity error machine checks by using the DSK as follows:

```
05          ; stop the application
XXXXXXXX 05
05000000
05000000          ; end dump of error code at OS address 0700

RFP, RFP00      ; return to previous mode
0500          ; continue running application
```

When the 05 parity error occurs, the following message is printed at the console:

```
CHECK STOPPED DSK 0500 0500 0700

DUMP 05          ; the Y-AD command will permit you to see a
                ; trace of where the application has been

DUMP 0500        0500 0700
0500          ; XXXX is the address of the instruction causing the 05
0500          ; parity error
.
.
0500          ; 05 microinstruction 007 age

0700
```

Since this message is so generic that the error occurs in the 0500 place, supplying the 0500 message will usually prevent this type of problem. The following is a description of the 05 parity error machine check.

MACHINE CHECKS (CONT)

CONTROL STORE PARITY ERROR

A machine check was caused by a single bit in a 2000 instruction stored in the 2000. A G and B floating-point allocation program was performed and when the program execution was complete, the error was observed. The error message appeared:

```

Exception PC      30000000
Error PC          03000000      2 LIT
                                Interrupt priority level = 8
                                Priority mode = 0000
                                Interrupt mode = 0000

Memory error      00000000      Control store parity error

CA load req      00000000
PL cl error      00000000
MVA              00000000
MVA              00000000      CPU mode = 0000
                                Signal
                                0000

RUC              00000000
RUCR             00000000
RASH             00000000      Cache hit

RUC              00000000
RUCR             00000000      Control store parity
                                error message = 0000
    
```

In this type of machine check exception, all useful information could not be provided because the processor had caused a control store parity error and there is no way to determine what happened.

It should be noted that in the machine check error message register (MCR) bits that byte 2 contains the location 'P'. These bits are the address of the instruction that caused the machine check. Was written the address into the field of the MCR in memory so that the MCR was available for access at the location that was the control store parity error.

WRITING SFRS

GENERAL GUIDELINES

Software Performance reports (SFRs) provide feedback to DIGITAL on problems with software and provide help to customers with troubleshooting their hardware.

The following guidelines cover the information that should be provided with a SFR. Especially on the problem, this information will vary in quantity and content. Remember that the goal is to present the information isolated, the easier it will be to resolve the problem.

1. Scenario

The user should supply a complete scenario, usually in the form of a batch log or manual listing, that will show exactly how the problem was produced. Supplying only the action produced by the problem is not enough. The problem may be caused by an interactive session, various system events, network packages, devices, SYSTEM parameters, etc. symbols, or logical names. Some or all of the display generated by the following variables may be needed for different problems:

```
SHOW LAYOUT PAGE
SHOW SYMBOL TABLES
TRY SYSTEM WILDCARD
IN ASCII
SHOW CALL
SHOW ADDRESS
```

2. User Problem Steps

The user should describe in particular, step by step, every screen, error message, etc. For example, if the execution of a very large program causes a problem, the user should describe the program to include only the code that causes the problem or write a small program that demonstrates the problem. This action has two benefits: first, the user may trap logic errors, etc. second, the software engineer looking into the problem does not have to understand unnecessary material.

WRITING SPDS (CONT)

4. Machine Readable Files

If possible, supply any software needed to reproduce the problem. This may include source programs, input files, sample data, or control procedures. If source programs are submitted, also include any libraries or require files referenced. Input files must be provided in machine-readable format. The console media or 1/2 inch tape are the best ways to include with the SPB.

If the problem involves a system error, include the system dump.

The data should be written onto an IBM® output disk or an IBM® tape. For example, the following commands will copy the system dump to an IBM tape:

```
SDIIT UNIT: TAPPE
SDIIB UNIT: DUMPE
SDIY UNIT:RAC,RSBCNR,DSB MTAP:
SD DUMPE UNIT:
```

To copy files to the console station, use the following commands:

```
FROM SYSSTATED:STDPPE
CONSOLE CONSOLE

[At this time, insert the console media and
place a scratch volume in the console tape unit.]

SDIIT UNIT: SPPEAPE
SDIIB UNIT: SPPEAPE
SDIY UNIT:RAC,RSBCNR,DSB [UNIT]
SDIY UNIT:RAC,RSBCNR,DSB [UNIT]DUMPE
SDIIB UNIT: DUMPE
```

When machine-readable data is provided in printed format, the user should include the exact hardware that was used to write the data and the methods used to read it. Other terminal name problems will usually not be used. For example, using RAC without the unit will create a dump file that is completely unusable, because the simulated 1/2 inch tape is not a file.

All machine-readable media submitted with SPB will be returned to the customer.

WRITING SPRS (CONT)

4. System Environment

Every computer site has a different type of workload. Some problems only appear under certain conditions. For example, some sites give different classes of users a different queue priority. These sites may have problems that other sites do not. This information can be very important in diagnosing the problem, especially for system bugs or crashes.

The user should describe any special software loaded on the user. Any unusual hardware devices on the system should also be mentioned.

Software version numbers should be included. For example, if there is a problem with accessing local symbols during a DEXTRA session, the version numbers of DEXTRA and all compilers/loaders should be specified.

If any patches other than from maintenance updates are being used, these should be mentioned in the SPR.

5. User Analysis Options

Optionally, the user may include an analysis of the problem. Any useful diagnostic information should be included such as: "When the error happened, the problem message was reproduced" or "In version 2.05, this problem does not occur."

6. Problem Specific Information or Inquiry

Very big different types of problems will require different types of information. The following table shows the information available needed for different types of problems.

WRITING SFRS (CONT)

Problem:	Information to include:
System Inquiries/Errors:	<p>A machine readable copy of the system dump 2110 0080 be included.¹⁶ (Output from the 2110 unit by model 300 or 301). Because it usually does not include enough information to diagnose the problem.)</p> <p>A copy of the error log at the time of the error should also be included because many system problems are triggered by hardware errors.¹⁷</p>
Problem check:	<p>To a machine check, include a copy of the error log.¹⁸</p> <p>A machine readable copy of the system dump 2110 should also be included.¹⁹</p>
System being:	<p>When a system restarts (after the new operator on any terminals), the system should be actually reloaded and the system dump 2110 included with the SFR.</p> <p>When the system is shut down in this way, the message listing is very important and should be included with the SFR.</p> <p>On the VAX-11/100 console terminal, press:</p> <pre> ^P HALT ^C^D^A </pre> <p>On the VAX-11/750 console terminal, enter:</p> <pre> ^P ^C^D ^C^A^V ^C ^D ^D ^V D&C P 0039907 D P 170007 ^C </pre>

WRITING SPRS (CONT)

date will mean the system is not check in, will be recognized by IBM developers as a "fixed" problem.

A description of the hardware giving back has should also be included.

Executive

If the user suspects a problem with systemive work, include a listing of the system parameters. These can be obtained by issuing `SYSTEM` and entering either `NO DISPLAY` and `PRINT/PRINTAL` commands.

A machine readable copy of the source program showing the program plus iterations, device files, and build if any should also be included, if possible.

Include a copy of the error log at the time of the problem.²²

Device

For any supported use of a device driver error, include a copy of the error log at the time of the problem.²³

Files

If the problem appears to be with a file, a comparison (for `AMODE/EQU`) on two files and its directory should be included. If possible, include a machine readable copy of the file itself.

Installation

For a problem that is intermittent or that cannot be reproduced, include a copy of the error log at the time of the problem.²⁴

WRITING SPTS (CONT)

Profile	Information to include
Command language input/probers	When submitting an SPT on a command language input/prober, it is important to show all syntax (NAME SPNO/FILE/DIRNAME) and logical name (SPTN LOGIC/PATH) before the body.
Job control card	If the job control card starts, it will print a message on the console and write a file named SPTJOBSTAT, SPTJOBLOG, and SPTJOBPRINT, and a work as readable copy of the SPTJOBSTAT file.
Tabulation	If the user encounters a problem with the LIBRARY, include the following information: <ol style="list-style-type: none"> 1. A readable readable copy of the library itself 2. Machine readable copies of all input files to the library 3. Information (DIRNAME/FILE) on the library file 4. Information (LIBRARY/SPNO/FILE) on the library contents <p>If the problem can be duplicated at will, include the scenario and any relevant files used.</p>
Trace	If the user encounters a problem with the LIBRARY, include machine readable copies of the object files and libraries used in the link along with a call log (LINK/TRACE/FILE).
Notes	For a device problem, supply manufacturer and of the device involved in the problem. This information should include the version number of the operating system and device, the hardware on both systems, and the patch level of the device software on the non-SPT system, if applicable.

WRITING SPRS (CONT)

From: _____	Information to include:
Workable _____	<p>7. The user subject a problem with the terminal device, provide the following information:</p> <ol style="list-style-type: none">1. A list of terminal parameters (unless in the manual)2. The type of terminal3. The type of code (if any)4. Any special terminal equipment5. Any unusual terminal configuration <p>If the problem involved reports of a message, it is also useful for the maintainer to know if the work on a six line operation can be performed from a different account or with the source and destination codes reversed.</p>
Supplier/Assembler _____	<p>11. The user successfully completed with the assistance of a computer, the user has source program that caused the problem. It is very important to include all source files and programs that are referenced by the source program, also.</p> <p>It is usually important to limit the scope of the problem when programming SPRs as suppliers.</p> <p>Include the exact location on the computer and the version number of the operating system.</p>
*The raw data file (SYSTEMS\SYSTEMS\SYSTEMS) and the formatted output from the SDA utility, should be included. Formatted output usually does not include all the information needed to solve the problem.	
**A raw data file (SYSTEMS\SYSTEMS\SYSTEMS) and the formatted output from the SDC utility, should be included. Formatted output does not include all the information needed to solve the problem.	

WRITING SPRS (CONT)

The following are priority explanations should be used as a guideline for determining the priority of an SPR:

1. Most production work cannot be run. Functionality that user app. has cannot be a major use of system. System will not last, necessary capabilities cannot be used as intended.
2. Some production work cannot be run. Certain capabilities are not used by, or otherwise degraded, but collector has sufficient excess capacity.
3. All production work can be run with some impact on user. Significant impact intervention required, excess production performance degraded but intervention has excess capacity.
4. All production work can be run with no significant impact on user. Risk in coll. or backg. reduced, collg's bypass procedure exists.
5. No system modifications needed to return to normal production. Suggestions, consultation, documentation exists.

GENERAL NOTES

VAX-11/750 TROUBLESHOOTING TIPS

1. When troubleshooting, place the console's power-on action switch in the HOLD position. If you do not, the CPU will try to connect to a CPU held around for any reason.

2. If the console panel does not respond when power is turned on, power to the CPU module and bus to the CPU board (RFD01) should appear.

Step 10 may be typing CTRL followed by a carriage return (ASCII hex address 0). The next control char should respond will be printed. If the address is 85, the bus is working. If the address is 8000, the bus is probably connected and the microcode is in loop waiting for its microcode.

Step 10 may be executed by the console display. The console can follow this sequence. If control characters have been cleared, typing "TEST/CTRL" when the CPU panel shows a trace of the bus to control words address should indicate that it very useful to the CPU at bus to a loop.

3. If the console cannot be reset, you may try to execute and debug modules in memory and to the console from the console panel (RFD01). Also execute and debug the kernel to see if possible.

If a reply comes to console from the console panel, you will see if it is successful from the CPU panel. This usually indicates whether the CPU and memory are working or not. However, certain locations cannot be accessed from the CPU panel.

The console panel can only read (RFD) is always present on the bus. RFD01, so it should be possible to read on or depend on the console register at location RFD01A. This location is RFD01B for the internal programmable exercises control (RFD01) on the console (RFD01). The console default should be set to physical addresses) and used from the console to "RFD01" address space, which is "1111 1111 1111 1111" when a check of the console binary address. (This character is 101 and 301 RFD01A/RFD01B).

4. For a partly boot of the console when by typing "RFD01" from the CPU panel. Full console control words parity is required. Sometimes checking with location 80 4 h/w with a parity error in any address other than 1700 (hex) instruction A problem in the console state.

GENERAL NOTES (CONT)

- Always run the IBM Microdiagnosics before the Microdiagnosics (see Chapter 6, IBM Publications 299-1).

- Value zero that the console had the "check console elements" and the "check FDCs" are disabled. This can be checked by an examine of the SIB registers 000/1 000/RTM. The bit 10000 of the SIB registers are 10 111000. These console console cases are correct as of the date of this document.

```
SIB 000/1000 Type zero (the SIB 11710 01  
SIB 000/1000 = 1110000 1000/00 1000/00 0 = 01  
SIB 000/1000 = 1110000 1000/00 1000/00 0 = 01
```

Refer to Power Bulletin 116, 171, and 287 for dates 2000 to 2000.

- The current revisions are microdiagnosics 2000:

```
RC230 - Rev. 6.7 Microdiagnostic Partner (INTEND)  
RC230 - Rev. 6.7 Micro 2000  
RC240 - Rev. 6.1 Micro 2000
```

- RC230 does not test the first memory array module. The first 256-Ki bytes array is tested by the Microdiagnosics.

- Earlier versions of RC230 may not report errors all errors, as time were not updating errors. Check periodically to find out when the updated version will be available.

- Each parity sensor in the VAX-11/780 is a backing check to occur on location 0000 11. This can be checked as a total error. In the VAX-11/780, the VAX-11/780 does not attempt to obtain good data from memory or a media parity error.

GENERAL NOTES (CONT)

DW750 INSTALLATION

The DW750 is typically installed in slot 7 of the extended rack backplane. To make cable routing easier and to place the bus at high priority in the bus plane, the:

CAUTION

Refer to the DW750 installation procedure that specifies use of the VTL05000 and kit to prevent access from audio channels. Also see figures and tables in Chapter 8 about the hardware bus plane, shelf and mounting by Jurgens and NSA installation supports.

If one or more DW750 KRESCOS adapters are already in place, they may be moved to slots 6, 7 and 8, and one CRT CRT level is added to the following example:

Example 1: NSA Data Link Installation

Slot	Device	Base Address	CRT Bus Level
7	NSA 1	112040	AB0 1
8	NSA 1	112040	AB0 2
9	-	150040	AB0

Example 2: NSA Audio DW750 Installation

Slot	Device	Base Address	CRT Bus Level
7	NSA	112040	AB0 1
8	NSA 0	112040	AB0 2
9	NSA 1	112040	AB0 3

UNIBUS EXERCISER (UBE) ON THE SECOND UNIBUS

The K7550 UBE module may be plugged into an 870 slot in the second UNIBUS computer bus to test hardware and software.

UBR Base CRT Address: 00000 1770000 actual

UBR Address: Nil

CHAPTER 10
CHARTS AND MACROS



RTEMP AND GPR FUNCTIONS

FILE NO	ASRO	ASSIGNMENT FUNCTION
1	00	DUAL PORT TEMP 0
2	01	DUAL PORT TEMP 1
3	02	DUAL PORT TEMP 2
4	03	DUAL PORT TEMP 3
5	04	DUAL PORT TEMP 4
6	05	DUAL PORT TEMP 5
7	06	DUAL PORT TEMP 6
8	07	DUAL PORT TEMP 7
9	08	DUAL PORT TEMP 8
10	09	DUAL PORT TEMP 9
11	0A	DUAL PORT TEMP 10
12	0B	DUAL PORT TEMP 11
13	0C	DUAL PORT TEMP 12
14	0D	DUAL PORT TEMP 13
15	0E	MEMORY MANAGEMENT TEMP 1
16	0F	MEMORY MANAGEMENT TEMP 2

FILE NO	ASRO	ASSIGNMENT FUNCTION
0	10	GPR 0
1	11	GPR 1
2	12	GPR 2
3	13	GPR 3
4	14	GPR 4
5	15	GPR 5
6	16	GPR 6
7	17	GPR 7
8	18	GPR 8
9	19	GPR 9
10	1A	GPR 10
11	1B	GPR 11
12	1C	GPR 12
13	1D	GPR 13
14	1E	STACK POINTER
15	1F	REG. 33 (LOCAL TEMPORARY)

12-1778

PRIVILEGED IPR AND MTEMP FUNCTIONS

REG NO	IPRD	ASSIGNMENT/PURPOSE
0	00	KERNEL STACK POINTER
1	01	EXECUTIVE STACK POINTER
2	02	SUPERVISOR STACK POINTER
3	03	USER STACK POINTER
4	04	INTERUPT STACK POINTER
5	05	PROCESS CONTROL BLOCK BASE
6	06	MEMORY MANAGEMENT TEMP 0
7	07	MEMORY MANAGEMENT TEMP 0
8	08	MESSAGE REGISTER
9	09	MESSAGE REGISTER
10	0A	IP LENGTH REGISTER
11	0B	IP LENGTH REGISTER
12	0C	SYSTEM BASE REGISTER
13	0D	SYSTEM LENGTH REGISTER
14	0E	MARKET/INITIAL REGISTER
15	0F	MEMORY MANAGEMENT TEMP 0

REG NO	MSRD	ASSIGNMENT/PURPOSE
0	00	MESSAGE REGISTER
1	01	MESSAGE REGISTER
2	02	MESSAGE REGISTER
3	03	MESSAGE REGISTER
4	04	MESSAGE REGISTER
5	05	MESSAGE REGISTER
6	06	MESSAGE REGISTER
7	07	MESSAGE REGISTER
8	08	MESSAGE REGISTER
9	09	MESSAGE REGISTER
10	0A	MESSAGE REGISTER
11	0B	MESSAGE, CPU FAULTS & ABT TRAP
12	0C	MESSAGE REGISTER OFFSET
13	0D	MEMORY MANAGEMENT TEMP 0
14	0E	SYSTEM CONTROL BLOCK BASE
15	0F	SOFTWARE STATE/MASK REGISTER

7-136

RSRC ASSIGNMENTS

YR/ QTR/ D SER	ROOM SERIES	USER/ACTIVITY
1000	TRKPT/CLERK	
01	WATERFR	
02	WM UNIT	*
1000	FOOD	
11	SP	
12	CLIP-GR	*
20	CAF	*
21	REP	
22	STP	*
23	USP	
24	SP	*
25	FOOD	
26	WATERFR	
27	ST/TEMP	*
28	FOOD	
29	FOUR	*
30	FOOD	*
31	FOOD	*
32	FOOD	*
33	FOOD	*
34	FOOD	*
35	FOOD	*
36	FOOD	*
37	FOOD	*
38	FOOD	*
39	FOOD	*
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98	FOOD	*
99	FOOD	*
00	FOOD	*

4-100

RSEC ASSIGNMENTS (CONT)

BASE NUMBER HEX	BASE REGISTER	DEFINITION
71	TEMP 0	
72	DEVID	*
73	TEMP	
74	ADDR	*
75	TEMP0	
76	* UNP0	UNP0
77	TEMP0	TEMP
78	TEMP0	TEMP
79	TEMP0	TEMP
7A	TEMP0	TEMP
7B	TEMP0	TEMP
7C	TEMP0	TEMP
7D	TEMP0	TEMP
7E	TEMP0	TEMP
7F	TEMP0	TEMP

* UNP0

1 00000.076 00000.000 00000.000 00000.000 00000.000
 1 00000.077 00000.000 00000.000 00000.000 00000.000

1000 00000.000 00000.000 00000.000 00000.000
 1001 00000.000 00000.000 00000.000 00000.000
 1002 00000.000 00000.000 00000.000 00000.000
 1003 00000.000 00000.000 00000.000 00000.000
 1004 00000.000 00000.000 00000.000 00000.000
 1005 00000.000 00000.000 00000.000 00000.000
 1006 00000.000 00000.000 00000.000 00000.000
 1007 00000.000 00000.000 00000.000 00000.000
 1008 00000.000 00000.000 00000.000 00000.000
 1009 00000.000 00000.000 00000.000 00000.000
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CHARTS

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UNITED STATES DEPARTMENT OF JUSTICE

REPORT DATA

UNIT	DESCRIPTION	QTY	UNIT PRICE	TOTAL PRICE	REMARKS
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UNITED STATES DEPARTMENT OF JUSTICE
 FEDERAL BUREAU OF INVESTIGATION
 WASHINGTON, D. C. 20535
 REPORT OF THE SPECIAL AGENT IN CHARGE
 DATE OF REPORT: 10/15/50
 TITLE: ...

CHARTS (CONT)

205

CHARTS (CONT)

LINE NO.	DESCRIPTION	AMOUNT	CHECK NO.	DATE
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CHARTS (CONT)

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CHARTS (CONT)

Chart No.	Chart Title	Scale	Author	Year	Notes
1001	Chart 1001	1:50,000	U.S. Navy	1950	
1002	Chart 1002	1:50,000	U.S. Navy	1950	
1003	Chart 1003	1:50,000	U.S. Navy	1950	
1004	Chart 1004	1:50,000	U.S. Navy	1950	
1005	Chart 1005	1:50,000	U.S. Navy	1950	
1006	Chart 1006	1:50,000	U.S. Navy	1950	
1007	Chart 1007	1:50,000	U.S. Navy	1950	
1008	Chart 1008	1:50,000	U.S. Navy	1950	
1009	Chart 1009	1:50,000	U.S. Navy	1950	
1010	Chart 1010	1:50,000	U.S. Navy	1950	
1011	Chart 1011	1:50,000	U.S. Navy	1950	
1012	Chart 1012	1:50,000	U.S. Navy	1950	
1013	Chart 1013	1:50,000	U.S. Navy	1950	
1014	Chart 1014	1:50,000	U.S. Navy	1950	
1015	Chart 1015	1:50,000	U.S. Navy	1950	
1016	Chart 1016	1:50,000	U.S. Navy	1950	
1017	Chart 1017	1:50,000	U.S. Navy	1950	
1018	Chart 1018	1:50,000	U.S. Navy	1950	
1019	Chart 1019	1:50,000	U.S. Navy	1950	
1020	Chart 1020	1:50,000	U.S. Navy	1950	
1021	Chart 1021	1:50,000	U.S. Navy	1950	
1022	Chart 1022	1:50,000	U.S. Navy	1950	
1023	Chart 1023	1:50,000	U.S. Navy	1950	
1024	Chart 1024	1:50,000	U.S. Navy	1950	
1025	Chart 1025	1:50,000	U.S. Navy	1950	
1026	Chart 1026	1:50,000	U.S. Navy	1950	
1027	Chart 1027	1:50,000	U.S. Navy	1950	
1028	Chart 1028	1:50,000	U.S. Navy	1950	
1029	Chart 1029	1:50,000	U.S. Navy	1950	
1030	Chart 1030	1:50,000	U.S. Navy	1950	
1031	Chart 1031	1:50,000	U.S. Navy	1950	
1032	Chart 1032	1:50,000	U.S. Navy	1950	
1033	Chart 1033	1:50,000	U.S. Navy	1950	
1034	Chart 1034	1:50,000	U.S. Navy	1950	
1035	Chart 1035	1:50,000	U.S. Navy	1950	
1036	Chart 1036	1:50,000	U.S. Navy	1950	
1037	Chart 1037	1:50,000	U.S. Navy	1950	
1038	Chart 1038	1:50,000	U.S. Navy	1950	
1039	Chart 1039	1:50,000	U.S. Navy	1950	
1040	Chart 1040	1:50,000	U.S. Navy	1950	
1041	Chart 1041	1:50,000	U.S. Navy	1950	
1042	Chart 1042	1:50,000	U.S. Navy	1950	
1043	Chart 1043	1:50,000	U.S. Navy	1950	
1044	Chart 1044	1:50,000	U.S. Navy	1950	
1045	Chart 1045	1:50,000	U.S. Navy	1950	
1046	Chart 1046	1:50,000	U.S. Navy	1950	
1047	Chart 1047	1:50,000	U.S. Navy	1950	
1048	Chart 1048	1:50,000	U.S. Navy	1950	
1049	Chart 1049	1:50,000	U.S. Navy	1950	
1050	Chart 1050	1:50,000	U.S. Navy	1950	

CHARTS (CONT)

NO.	PRICE	MARK	Symbol	Description	Yield	Maturity
127	100.00					
128	100.00					
129	100.00					
130	100.00					
131	100.00					
132	100.00					
133	100.00					
134	100.00					
135	100.00					
136	100.00					
137	100.00					
138	100.00					
139	100.00					
140	100.00					
141	100.00					
142	100.00					
143	100.00					
144	100.00					
145	100.00					
146	100.00					
147	100.00					
148	100.00					
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194	100.00					
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198	100.00					
199	100.00					
200	100.00					

NOTE: THESE ANALYSES ARE FOR THE PURPOSE OF INFORMATION ONLY. THE YIELD IS NOT GUARANTEED. THE YIELD IS SUBJECT TO CHANGE WITHOUT NOTICE. THE YIELD IS NOT GUARANTEED. THE YIELD IS SUBJECT TO CHANGE WITHOUT NOTICE.

CHARTS (CONT)

121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200
121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200

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CHARITYS (CONT)

170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000
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CHARTS (CONT)

Chart No.	Chart Name	Scale	Notes
1125	Chart No. 1	1:50,000	
1126	Chart No. 2	1:50,000	
1127	Chart No. 3	1:50,000	
1128	Chart No. 4	1:50,000	
1129	Chart No. 5	1:50,000	
1130	Chart No. 6	1:50,000	
1131	Chart No. 7	1:50,000	
1132	Chart No. 8	1:50,000	
1133	Chart No. 9	1:50,000	
1134	Chart No. 10	1:50,000	
1135	Chart No. 11	1:50,000	
1136	Chart No. 12	1:50,000	
1137	Chart No. 13	1:50,000	
1138	Chart No. 14	1:50,000	
1139	Chart No. 15	1:50,000	
1140	Chart No. 16	1:50,000	
1141	Chart No. 17	1:50,000	
1142	Chart No. 18	1:50,000	
1143	Chart No. 19	1:50,000	
1144	Chart No. 20	1:50,000	
1145	Chart No. 21	1:50,000	
1146	Chart No. 22	1:50,000	
1147	Chart No. 23	1:50,000	
1148	Chart No. 24	1:50,000	
1149	Chart No. 25	1:50,000	
1150	Chart No. 26	1:50,000	
1151	Chart No. 27	1:50,000	
1152	Chart No. 28	1:50,000	
1153	Chart No. 29	1:50,000	
1154	Chart No. 30	1:50,000	
1155	Chart No. 31	1:50,000	
1156	Chart No. 32	1:50,000	
1157	Chart No. 33	1:50,000	
1158	Chart No. 34	1:50,000	
1159	Chart No. 35	1:50,000	
1160	Chart No. 36	1:50,000	
1161	Chart No. 37	1:50,000	
1162	Chart No. 38	1:50,000	
1163	Chart No. 39	1:50,000	
1164	Chart No. 40	1:50,000	
1165	Chart No. 41	1:50,000	
1166	Chart No. 42	1:50,000	
1167	Chart No. 43	1:50,000	
1168	Chart No. 44	1:50,000	
1169	Chart No. 45	1:50,000	
1170	Chart No. 46	1:50,000	
1171	Chart No. 47	1:50,000	
1172	Chart No. 48	1:50,000	
1173	Chart No. 49	1:50,000	
1174	Chart No. 50	1:50,000	
1175	Chart No. 51	1:50,000	
1176	Chart No. 52	1:50,000	
1177	Chart No. 53	1:50,000	
1178	Chart No. 54	1:50,000	
1179	Chart No. 55	1:50,000	
1180	Chart No. 56	1:50,000	
1181	Chart No. 57	1:50,000	
1182	Chart No. 58	1:50,000	
1183	Chart No. 59	1:50,000	
1184	Chart No. 60	1:50,000	
1185	Chart No. 61	1:50,000	
1186	Chart No. 62	1:50,000	
1187	Chart No. 63	1:50,000	
1188	Chart No. 64	1:50,000	
1189	Chart No. 65	1:50,000	
1190	Chart No. 66	1:50,000	
1191	Chart No. 67	1:50,000	
1192	Chart No. 68	1:50,000	
1193	Chart No. 69	1:50,000	
1194	Chart No. 70	1:50,000	
1195	Chart No. 71	1:50,000	
1196	Chart No. 72	1:50,000	
1197	Chart No. 73	1:50,000	
1198	Chart No. 74	1:50,000	
1199	Chart No. 75	1:50,000	
1200	Chart No. 76	1:50,000	

CHARTS (CONT)

PLANS LISTED BY STATE

PL	PLAN NO.	PLAN NAME	PLAN TYPE	PLAN NO.	PLAN NAME	PLAN TYPE
111	111-1	State of Alaska	State	111-1	State of Alaska	State
112	112-1	State of Arizona	State	112-1	State of Arizona	State
113	113-1	State of Arkansas	State	113-1	State of Arkansas	State
114	114-1	State of California	State	114-1	State of California	State
115	115-1	State of Colorado	State	115-1	State of Colorado	State
116	116-1	State of Connecticut	State	116-1	State of Connecticut	State
117	117-1	State of Delaware	State	117-1	State of Delaware	State
118	118-1	State of Florida	State	118-1	State of Florida	State
119	119-1	State of Georgia	State	119-1	State of Georgia	State
120	120-1	State of Hawaii	State	120-1	State of Hawaii	State
121	121-1	State of Idaho	State	121-1	State of Idaho	State
122	122-1	State of Illinois	State	122-1	State of Illinois	State
123	123-1	State of Indiana	State	123-1	State of Indiana	State
124	124-1	State of Iowa	State	124-1	State of Iowa	State
125	125-1	State of Kansas	State	125-1	State of Kansas	State
126	126-1	State of Kentucky	State	126-1	State of Kentucky	State
127	127-1	State of Louisiana	State	127-1	State of Louisiana	State
128	128-1	State of Maine	State	128-1	State of Maine	State
129	129-1	State of Maryland	State	129-1	State of Maryland	State
130	130-1	State of Massachusetts	State	130-1	State of Massachusetts	State
131	131-1	State of Michigan	State	131-1	State of Michigan	State
132	132-1	State of Minnesota	State	132-1	State of Minnesota	State
133	133-1	State of Missouri	State	133-1	State of Missouri	State
134	134-1	State of Montana	State	134-1	State of Montana	State
135	135-1	State of Nebraska	State	135-1	State of Nebraska	State
136	136-1	State of Nevada	State	136-1	State of Nevada	State
137	137-1	State of New Hampshire	State	137-1	State of New Hampshire	State
138	138-1	State of New Jersey	State	138-1	State of New Jersey	State
139	139-1	State of New Mexico	State	139-1	State of New Mexico	State
140	140-1	State of New York	State	140-1	State of New York	State
141	141-1	State of North Carolina	State	141-1	State of North Carolina	State
142	142-1	State of North Dakota	State	142-1	State of North Dakota	State
143	143-1	State of Ohio	State	143-1	State of Ohio	State
144	144-1	State of Oklahoma	State	144-1	State of Oklahoma	State
145	145-1	State of Oregon	State	145-1	State of Oregon	State
146	146-1	State of Pennsylvania	State	146-1	State of Pennsylvania	State
147	147-1	State of Rhode Island	State	147-1	State of Rhode Island	State
148	148-1	State of South Carolina	State	148-1	State of South Carolina	State
149	149-1	State of South Dakota	State	149-1	State of South Dakota	State
150	150-1	State of Tennessee	State	150-1	State of Tennessee	State
151	151-1	State of Texas	State	151-1	State of Texas	State
152	152-1	State of Utah	State	152-1	State of Utah	State
153	153-1	State of Vermont	State	153-1	State of Vermont	State
154	154-1	State of Virginia	State	154-1	State of Virginia	State
155	155-1	State of Washington	State	155-1	State of Washington	State
156	156-1	State of West Virginia	State	156-1	State of West Virginia	State
157	157-1	State of Wisconsin	State	157-1	State of Wisconsin	State
158	158-1	State of Wyoming	State	158-1	State of Wyoming	State

CHARTS (CONT)

CLASS	GRADE LEVEL	CLASS	DESCRIPTION	PERIODS	PERIODS	PERIODS
1100	11	1100	1100	1100	1100	1100
1101	11	1101	1101	1101	1101	1101
1102	11	1102	1102	1102	1102	1102
1103	11	1103	1103	1103	1103	1103
1104	11	1104	1104	1104	1104	1104
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1119	11	1119	1119	1119	1119	1119
1120	11	1120	1120	1120	1120	1120
1121	11	1121	1121	1121	1121	1121
1122	11	1122	1122	1122	1122	1122
1123	11	1123	1123	1123	1123	1123
1124	11	1124	1124	1124	1124	1124
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1157	11	1157	1157	1157	1157	1157
1158	11	1158	1158	1158	1158	1158
1159	11	1159	1159	1159	1159	1159
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1162	11	1162	1162	1162	1162	1162
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1164	11	1164	1164	1164	1164	1164
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1167	11	1167	1167	1167	1167	1167
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1172	11	1172	1172	1172	1172	1172
1173	11	1173	1173	1173	1173	1173
1174	11	1174	1174	1174	1174	1174
1175	11	1175	1175	1175	1175	1175
1176	11	1176	1176	1176	1176	1176
1177	11	1177	1177	1177	1177	1177
1178	11	1178	1178	1178	1178	1178
1179	11	1179	1179	1179	1179	1179
1180	11	1180	1180	1180	1180	1180
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1182	11	1182	1182	1182	1182	1182
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1185	11	1185	1185	1185	1185	1185
1186	11	1186	1186	1186	1186	1186
1187	11	1187	1187	1187	1187	1187
1188	11	1188	1188	1188	1188	1188
1189	11	1189	1189	1189	1189	1189
1190	11	1190	1190	1190	1190	1190
1191	11	1191	1191	1191	1191	1191
1192	11	1192	1192	1192	1192	1192
1193	11	1193	1193	1193	1193	1193
1194	11	1194	1194	1194	1194	1194
1195	11	1195	1195	1195	1195	1195
1196	11	1196	1196	1196	1196	1196
1197	11	1197	1197	1197	1197	1197
1198	11	1198	1198	1198	1198	1198
1199	11	1199	1199	1199	1199	1199
1200	11	1200	1200	1200	1200	1200

CHARTS (CONT)

FIG. 1. The first 1000 ... with most negative eigen

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Number	Value	Order	Label
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1100

CHARTS (CONT)

PROBABLY AND SPECIFIC POINT

TYPE - "TYPE" "TYPE"

1111

ADDRESS	TYPE	DESCRIPTION
1111	1	1111
1112	2	1112
1113	3	1113
1114	4	1114
1115	5	1115
1116	6	1116
1117	7	1117
1118	8	1118
1119	9	1119
1120	10	1120
1121	11	1121
1122	12	1122
1123	13	1123
1124	14	1124
1125	15	1125
1126	16	1126
1127	17	1127
1128	18	1128
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1166	56	1166
1167	57	1167
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1169	59	1169
1170	60	1170

CHARTS (CONT)

100 - MARIJUANA

1970 - 1974

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MARIJUANA SEIZURES	
YEAR	AMOUNT (LBS)
1970	150
1971	180
1972	220
1973	250
1974	300

YEAR	AMOUNT (LBS)	VALUE (\$)
1970	150	15000
1971	180	18000
1972	220	22000
1973	250	25000
1974	300	30000

YEAR	AMOUNT (LBS)	VALUE (\$)
1970	150	15000
1971	180	18000
1972	220	22000
1973	250	25000
1974	300	30000

YEAR	AMOUNT (LBS)	VALUE (\$)
1970	150	15000
1971	180	18000
1972	220	22000
1973	250	25000
1974	300	30000

CHARLES (CONT)

DATE	TIME	FROM	TO	REMARKS
05/11	12:11	101	101	ARRIVE
05/11	12:15	101	101	DEPART
05/11	12:20	101	101	ARRIVE
05/11	12:25	101	101	DEPART
05/11	12:30	101	101	ARRIVE
05/11	12:35	101	101	DEPART
05/11	12:40	101	101	ARRIVE
05/11	12:45	101	101	DEPART
05/11	12:50	101	101	ARRIVE
05/11	12:55	101	101	DEPART
05/11	13:00	101	101	ARRIVE
05/11	13:05	101	101	DEPART
05/11	13:10	101	101	ARRIVE
05/11	13:15	101	101	DEPART
05/11	13:20	101	101	ARRIVE
05/11	13:25	101	101	DEPART
05/11	13:30	101	101	ARRIVE
05/11	13:35	101	101	DEPART
05/11	13:40	101	101	ARRIVE
05/11	13:45	101	101	DEPART
05/11	13:50	101	101	ARRIVE
05/11	13:55	101	101	DEPART
05/11	14:00	101	101	ARRIVE
05/11	14:05	101	101	DEPART
05/11	14:10	101	101	ARRIVE
05/11	14:15	101	101	DEPART
05/11	14:20	101	101	ARRIVE
05/11	14:25	101	101	DEPART
05/11	14:30	101	101	ARRIVE
05/11	14:35	101	101	DEPART
05/11	14:40	101	101	ARRIVE
05/11	14:45	101	101	DEPART
05/11	14:50	101	101	ARRIVE
05/11	14:55	101	101	DEPART
05/11	15:00	101	101	ARRIVE
05/11	15:05	101	101	DEPART
05/11	15:10	101	101	ARRIVE
05/11	15:15	101	101	DEPART
05/11	15:20	101	101	ARRIVE
05/11	15:25	101	101	DEPART
05/11	15:30	101	101	ARRIVE
05/11	15:35	101	101	DEPART
05/11	15:40	101	101	ARRIVE
05/11	15:45	101	101	DEPART
05/11	15:50	101	101	ARRIVE
05/11	15:55	101	101	DEPART
05/11	16:00	101	101	ARRIVE
05/11	16:05	101	101	DEPART
05/11	16:10	101	101	ARRIVE
05/11	16:15	101	101	DEPART
05/11	16:20	101	101	ARRIVE
05/11	16:25	101	101	DEPART
05/11	16:30	101	101	ARRIVE
05/11	16:35	101	101	DEPART
05/11	16:40	101	101	ARRIVE
05/11	16:45	101	101	DEPART
05/11	16:50	101	101	ARRIVE
05/11	16:55	101	101	DEPART
05/11	17:00	101	101	ARRIVE
05/11	17:05	101	101	DEPART
05/11	17:10	101	101	ARRIVE
05/11	17:15	101	101	DEPART
05/11	17:20	101	101	ARRIVE
05/11	17:25	101	101	DEPART
05/11	17:30	101	101	ARRIVE
05/11	17:35	101	101	DEPART
05/11	17:40	101	101	ARRIVE
05/11	17:45	101	101	DEPART
05/11	17:50	101	101	ARRIVE
05/11	17:55	101	101	DEPART
05/11	18:00	101	101	ARRIVE
05/11	18:05	101	101	DEPART
05/11	18:10	101	101	ARRIVE
05/11	18:15	101	101	DEPART
05/11	18:20	101	101	ARRIVE
05/11	18:25	101	101	DEPART
05/11	18:30	101	101	ARRIVE
05/11	18:35	101	101	DEPART
05/11	18:40	101	101	ARRIVE
05/11	18:45	101	101	DEPART
05/11	18:50	101	101	ARRIVE
05/11	18:55	101	101	DEPART
05/11	19:00	101	101	ARRIVE
05/11	19:05	101	101	DEPART
05/11	19:10	101	101	ARRIVE
05/11	19:15	101	101	DEPART
05/11	19:20	101	101	ARRIVE
05/11	19:25	101	101	DEPART
05/11	19:30	101	101	ARRIVE
05/11	19:35	101	101	DEPART
05/11	19:40	101	101	ARRIVE
05/11	19:45	101	101	DEPART
05/11	19:50	101	101	ARRIVE
05/11	19:55	101	101	DEPART
05/11	20:00	101	101	ARRIVE
05/11	20:05	101	101	DEPART
05/11	20:10	101	101	ARRIVE
05/11	20:15	101	101	DEPART
05/11	20:20	101	101	ARRIVE
05/11	20:25	101	101	DEPART
05/11	20:30	101	101	ARRIVE
05/11	20:35	101	101	DEPART
05/11	20:40	101	101	ARRIVE
05/11	20:45	101	101	DEPART
05/11	20:50	101	101	ARRIVE
05/11	20:55	101	101	DEPART
05/11	21:00	101	101	ARRIVE
05/11	21:05	101	101	DEPART
05/11	21:10	101	101	ARRIVE
05/11	21:15	101	101	DEPART
05/11	21:20	101	101	ARRIVE
05/11	21:25	101	101	DEPART
05/11	21:30	101	101	ARRIVE
05/11	21:35	101	101	DEPART
05/11	21:40	101	101	ARRIVE
05/11	21:45	101	101	DEPART
05/11	21:50	101	101	ARRIVE
05/11	21:55	101	101	DEPART
05/11	22:00	101	101	ARRIVE

CHARTS (CONT)

MS - Part - LARA, ERIC - Volume 1 - Complete Instructions for use

CODE	DESCRIPTION	UNIT	PERIOD	PERIOD	PERIOD	PERIOD	PERIOD
0100	GENERAL INSTRUCTIONS						
0110	GENERAL INSTRUCTIONS						
0120	GENERAL INSTRUCTIONS						
0130	GENERAL INSTRUCTIONS						
0140	GENERAL INSTRUCTIONS						
0150	GENERAL INSTRUCTIONS						
0160	GENERAL INSTRUCTIONS						
0170	GENERAL INSTRUCTIONS						
0180	GENERAL INSTRUCTIONS						
0190	GENERAL INSTRUCTIONS						
0200	GENERAL INSTRUCTIONS						
0210	GENERAL INSTRUCTIONS						
0220	GENERAL INSTRUCTIONS						
0230	GENERAL INSTRUCTIONS						
0240	GENERAL INSTRUCTIONS						
0250	GENERAL INSTRUCTIONS						
0260	GENERAL INSTRUCTIONS						
0270	GENERAL INSTRUCTIONS						
0280	GENERAL INSTRUCTIONS						
0290	GENERAL INSTRUCTIONS						
0300	GENERAL INSTRUCTIONS						
0310	GENERAL INSTRUCTIONS						
0320	GENERAL INSTRUCTIONS						
0330	GENERAL INSTRUCTIONS						
0340	GENERAL INSTRUCTIONS						
0350	GENERAL INSTRUCTIONS						
0360	GENERAL INSTRUCTIONS						
0370	GENERAL INSTRUCTIONS						
0380	GENERAL INSTRUCTIONS						
0390	GENERAL INSTRUCTIONS						
0400	GENERAL INSTRUCTIONS						
0410	GENERAL INSTRUCTIONS						
0420	GENERAL INSTRUCTIONS						
0430	GENERAL INSTRUCTIONS						
0440	GENERAL INSTRUCTIONS						
0450	GENERAL INSTRUCTIONS						
0460	GENERAL INSTRUCTIONS						
0470	GENERAL INSTRUCTIONS						
0480	GENERAL INSTRUCTIONS						
0490	GENERAL INSTRUCTIONS						
0500	GENERAL INSTRUCTIONS						

TABLE 1. (Cont.)											
TABLE 2. (Cont.)											
TABLE 3. (Cont.)											
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TABLE 98. (Cont.)											
TABLE 99. (Cont.)											
TABLE 100. (Cont.)											

MACROS

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MACROS (CONT)

1521	MACRO	MACRO	MACRO
1522	MACRO	MACRO	MACRO
1523	MACRO	MACRO	MACRO
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1526	MACRO	MACRO	MACRO
1527	MACRO	MACRO	MACRO
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1533	MACRO	MACRO	MACRO
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MACRS (CONT)

1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100																																																																																																																																																																																
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MACROS (CONT)

LINE	SYMBOLS	MACRO
1001	MACRO	MACRO
1002	MACRO	MACRO
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1050	MACRO	MACRO

NOTES

- 11/780 - STAR (1MB) TTL
- 11/750 - COMET (0.7MB) ECL 4/A
uses 20V D.
- 11/730 - NEBULA.

COMET BUS, 24 BIT ADD
 10MB OF MEMORY. TOP 1MB
 USED AS I/O SPACE
 FE0000 - FFFFFF - UNIBUS AND S2
 MICRO MEMORY AT ROOT, 9% OVER SHARED
 9:9% - OTHER CH.

DATA PATH PC - 32 BIT 4 GIG VA
 PA - 24 BIT - 10MB, SMALL MEMORY
 TO TRANSLATE FROM VA TO PA.

7 LEVELS OF ADDRESSING (7 IS MINIMUM)
 7 - UNIBUS/PC (LOCAL/REMOTE BUS)
 6 } NOT USED
 5 }
 4 - VISA (CONTAINS INT LOGIC)
 3 }
 2 } FOR OPTIONS
 1 }
 0 - CPU.

LEVELS SET BY LINES.
 B.2 LEVELS ARE 4, 5, 6, 7.

NOTES

- 4 Bytes = WORD
- 8 " = BYTE
- 16 " = WORD
- 32 " = LONGWORD
- 64 " = QUADWORD

NOTE

INSTRUCTIONS FETCHED ON LONGWORD BOUNDARIES ARE EXECUTED ON BYTE BOUNDARIES.

LOW END ADDRESS MEMORY,
DISABLE CACHE

>>> BIT 25 = 1 (DIFFER FROM INT REG 25). WORK IN BYTE MODE

>>> E/A 0 = EXAMINE NEW PURPOSE REGISTER 0-1.

>>> BU DU AD
 / ↓ \
 DEV. CHANNEL DRIVE

8 = 0/13 I/O MODE.
 CTRL P GIVES TO
 >>> - ENABLE I/O

DS > } PROGRAM I/O MODE.
 ROM 50 >

NOTES

AVAILABLE DIAGNOSTICS.

DEC. TRAC. CHUCKY EV4,
FROM REVISOR, BE IP. ERRO7 LOG.

DEC UNLICENSED DIAGS

UNDER DIAG SUBROUTINE, ECSAA-EXE

PL ESSAA (012 8/16 0001)

DD > - FORMATIONS FOR:

RA 80/80/160

RM03/05

RM 80

RP06/7

RA07.

EX01/2

EV5BA - AUTOSIZER.

PL EV5BA.

DD > HELP DEV (PAGE)

LISTS AVAILABLE TESTS FOR THAT
DEVICE.

DD > HELP EG EV2LR

NOTES

MASSBUS.

NEW CABLE LENGTH = 160'

SID.

N/W LINKS }
 SUTRONES } SIGNATURE.

MICROCODE REV. N/W SYS REV

PRESENCE OF DOC. 8 - THIS AFFECTS
 OPERATION OF VMS.

REV 8 - REV B B/R. 4004

3 - 8 - REV C - - - - 4006

3 - C - REV D - - - - 4002

NOTES

NOTES

1. The following are the names of the authors of the papers in this volume: [illegible]

VWD

Does equipment used support standard type of maintenance effort to improve the quality and usefulness of our publications?

What information is available to you on the use of equipment in your organization? (Name, title, organization, and telephone and address of all those to whom you are referred.)

What type of maintenance is used? _____

How many people are responsible for this effort? _____

Does your organization have a maintenance program? (Yes/No) _____

Does it include your work? _____ Why? _____

Please describe the maintenance program in your organization and the type of equipment used, including an inventory of all equipment used in your organization.

Name _____ Title _____

Address _____

City/State _____ Telephone _____

Organization _____ Title _____

Additional comments for use by the author(s):

Equipment used: _____
 Procedures for equipment used: _____
 P.O. Order #2205
 Technical literature: _____

See also: _____
 Telephone: _____

Order No. FR-VAX750-115 _____

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