

EX-TMBFF-MM-PRE



TMB11/TU10W
DEC magtape system
maintenance manual
(TMB11-E/F system)

PRELIMINARY

SEPTEMBER 1976

digital equipment corporation • maynard, massachusetts

Preliminary Edition.

SEPTEMBER 1976

Copyright © 1976 by Digital Equipment Corporation.

The material in this manual is for informational purposes and is subject to change without notice.

Digital Equipment Corporation assumes no responsibility for any errors which may appear in this manual.

Printed in U.S.A.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	DECtape	PDP
DECCOMM	DECUS	RSTS
DECsystem-10	DIGITAL	TYPESET-8
DECSYSTEM-20	MASSBUS	TYPESET-11
		UNIBUS

TABLE OF CONTENTS

CHAPTER 1 General Information

- 1.1 Introduction
- 1.2 General Description
 - 1.2.1 System Configuration
 - 1.2.2 Physical Description
- 1.3 System Functional Description
- 1.4 Applicable Documents
- 1.5 Specifications

CHAPTER 2

Unpacking, Installation and Acceptance Testing

- 2.1 Site Planning and Considerations
 - 2.1.1 Space Requirements
 - 2.1.2 Power Requirements
 - 2.1.3 Environmental Requirements
- 2.2 Unpacking
 - 2.2.1 TU10W Cabinet Unpacking
 - 2.2.2 TMB11 Unpacking
- 2.3 Inspection
- 2.4 TU10W Cabinet Installation
- 2.5 TMB11 Installation/Cabling
 - 2.5.1 System Unit Installation
 - 2.5.2 Module Installation
 - 2.5.3 Unibus Cabling
 - 2.5.4 CONTROLLER/MASTER DRIVE CABLING
 - 2.5.5 Securing Cables
- 2.6 TU10W Cabling
- 2.7 Acceptance Testing

Chapter 7

MS926 Theory of Operation

7.1 General

7.2 Status/Command Logic

7.2.1 Command Logic

7.2.2 Status Logic

7.3 Drive Start Up

7.3.1 Drive Start Signals

7.3.2 Start Up Delay

7.4 Write Sequence

7.4.1 Nine Track Normal

7.4.1.1 Write Data

7.4.1.2 Write End of Record

7.4.2 Seven Track Normal

7.4.3 Nine Track File Mark

7.4.3.1 Write Data

7.4.3.2 Write End of Record

7.4.4 Seven Track File Mark

7.5 Read Sequence

7.5.1 Read Data

7.5.2 Error Detection

7.5.3 File Mark Detection

7.5.4 End of Record Detection

7.5.4.1 Nine Track Normal

7.5.4.2 Zero CRC or LRC Characters

7.5.4.3 Seven Track and File Mark

7.6 Drive Stop

Fig. No.	Title
7-1	M8926 Simplified Flow Diagram
7-2	M8926 Detailed Flow Diagram
7-3	M8926 Block Diagram
7-4	RWS and CRWS Timing Diagram
7-5	Command Latch Up Flow Diagram
7-6	STATUS/COMMAND Block Diagram
7-7	M8926 Timing Diagram
7-8	Drive Start Up Flow Diagram
7-9	Start/Stop Control Block Diagram
7-10	Write Flow Diagram
7-11	Write Block Diagram
7-12	Read Flow Diagram
7-13	Read Block Diagram
7-14	End of Record Timing Non-Zero CRC and LRC
7-15	End of Record Timing, Zero CRC
7-16	End of Record Timing, Zero LRC
7-17	End of Record Timing, Seven Track and File Mark
7-18	End of Record Flow Diagram
7-19	End of Record Block Diagram
7-20	Drive Stop Flow Diagram
8-1	TU10W Regulator Board and Fan
8-2	TU10W +5V Regulator Circuit

PREFACE

The TU10W transport is very similar (in many areas identical) to the TU16 transport with respect to both transport hardware and electronic modules. In this manual reference is made to the TU16/TM02 maintenance manual for information on the TU10W transport that is identical to TU16 information.

Specifically the references are from Chapter 5 (System Maintenance) for maintenance on the transport, and from Chapter 8 (TU10W theory of Operation). Chapter 8 covers the differences between the TU10W transport and TU16 transport. This information pertains to the new areas that would not be documented in the TU16 manual.

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The TMB11-EX/FX* DECmagtape System (TMB11/TU10W)† is a magnetic tape storage system that interfaces with the PDP-11 family of processors and peripherals and provides storage for digital information. The system reads and records digital data in parallel in an industry-compatible NRZI format at a maximum data transfer rate of 36,000 tape characters per second. Tape density and tape character format are program selectable. Forward/reverse tape speed is 45 in./sec, while rewind is performed at 150 in./sec. The TMB11/TU10W tape drive system also has forward and reverse read/space capability.

1.2 General Description

1.2.1 System Configuration

The basic TMB11/TU10W DECmagtape System configuration is a TMB11 controller and a TU10W master tape transport. From one to seven "slave" transports may be added to make a maximum possible configuration of one TMB11 controller and eight tape transports. The

* The TMB11-EX is a 9-track system. The TMB11-FX is a 7-track system. "X" specifies the system voltage and frequency requirements (see table 1-1).

†The TMB11-EX/FX system is commonly referred to by its component subunits, the TMB11 and the TU10W, hence the manual title TMB11/TU10W DECmagtape System Maintenance Manual. Within this manual the system is referred to as the TMB11/TU10W.

master tape transport is composed of a "host" transport and an M8926 interface module. The M8926 interfaces the "host" transport and the slave transports (if any) to the TMB11 via the BC11A controller cable. All the tape transports are "daisy chained" on the slave bus making them essentially in parallel with each other. Figure 1-1 is an illustration of the TMB11/TU10W system configuration.

1.2.2 Physical Description

The TMB11 (Figure 1-2) consists of the following six modules:

1. M105-Address Selector Module
2. M795-Word Count and Bus Address Module
3. M796-Unibus Master Control
4. M7821-Interrupt Control Module
5. M7911-Tape Drive Interface
6. M7912-TMB11 Unibus Registers

The six modules are plugged into a TMB11 system unit that is mounted in an expander box. Unibus input, Unibus output, and tape transport cabling also connect to the system unit.

The TU10W tape transport is contained in a single 19 inch (48.3 cm) cabinet along with an 861 power controller (Figure 1-3). Figures 1-4 and 1-5 illustrate front, rear and side views of the transport and identify many of the TU10W components and subassemblies.

The TMB11 Controller interfaces the DECmagtape system to the PDP-11 Unibus. It controls data transfers, issues control commands to the TU10W master, and monitors system operation. Each TMB11 can control one master transport and up to seven slave transports.

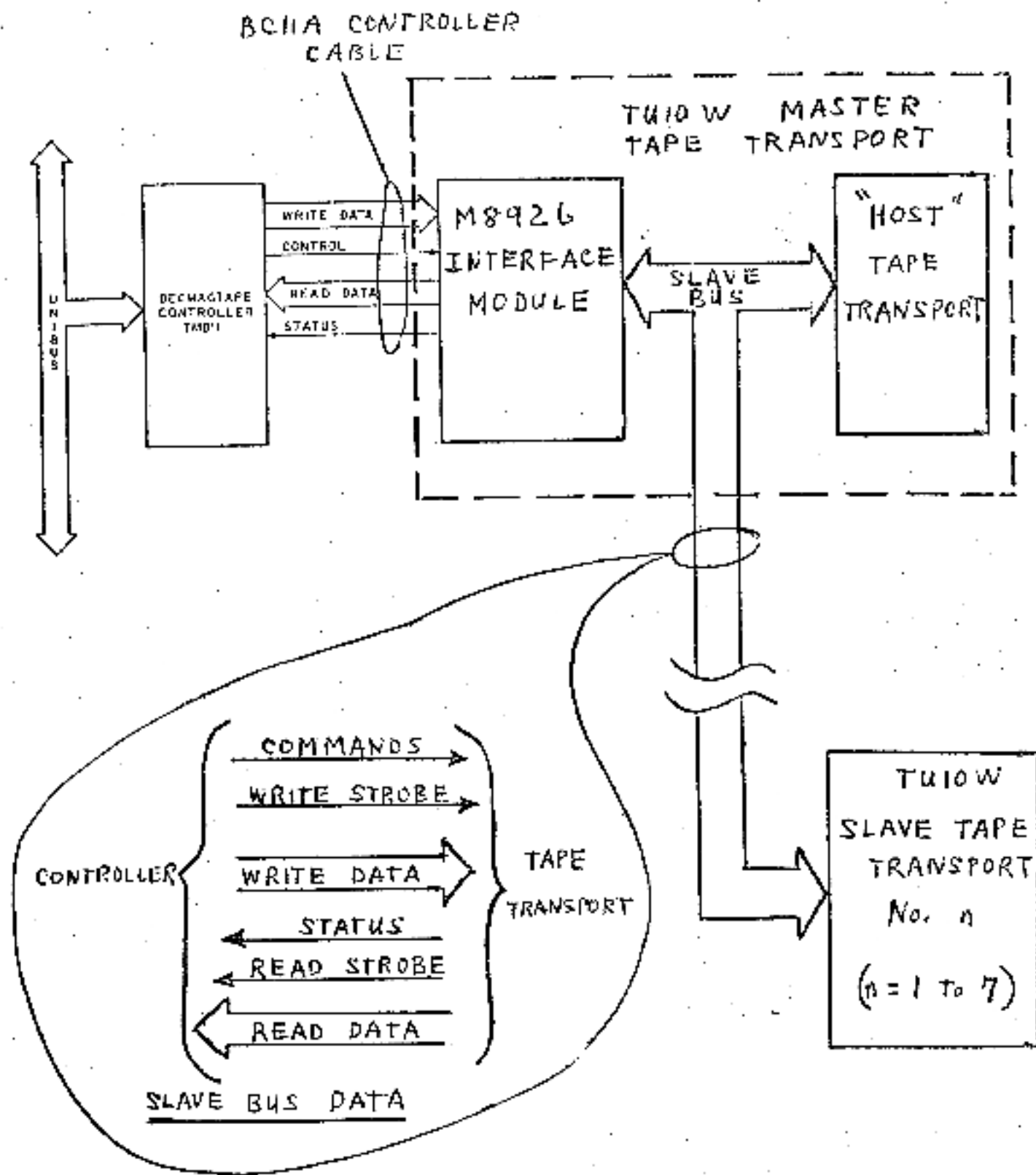
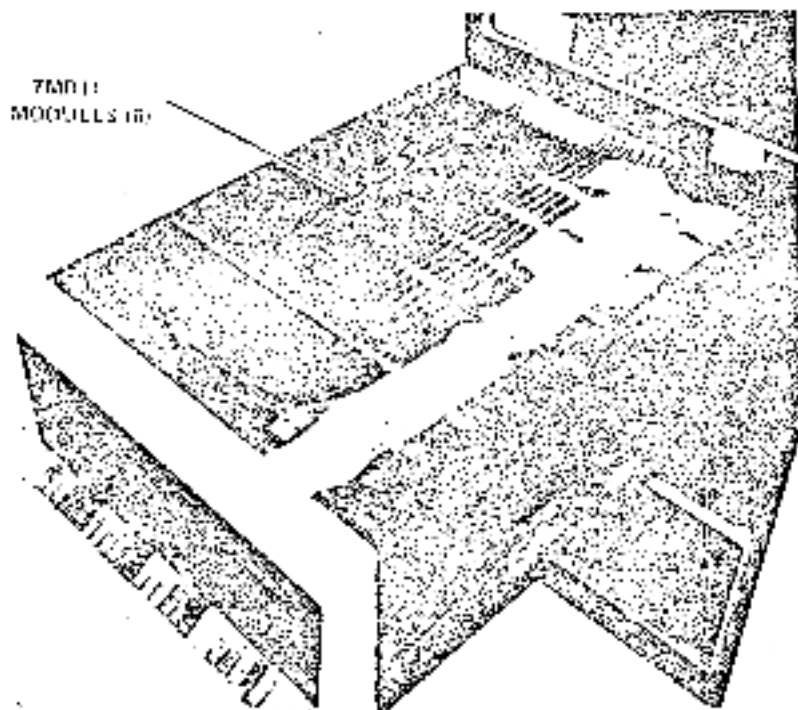
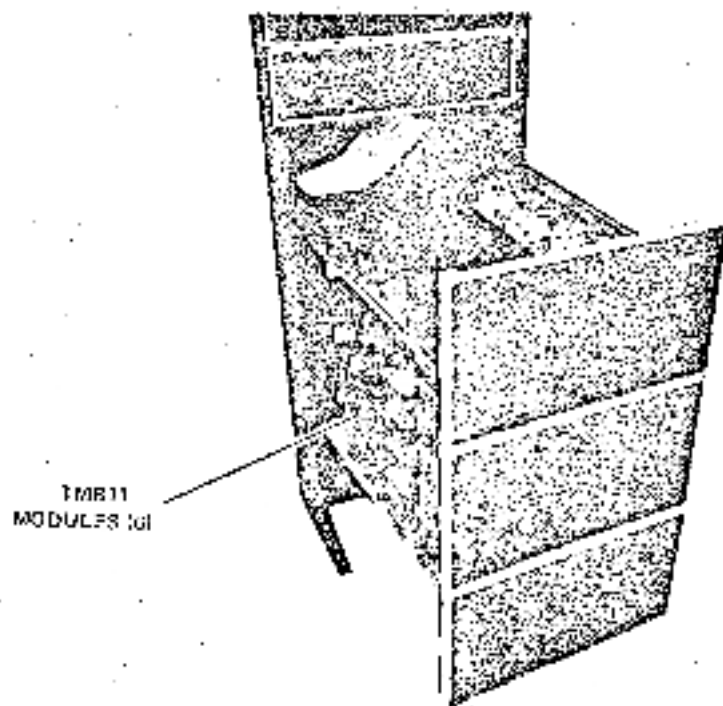


FIG. 1-1 THB11/TU10W Tape Drive System Configuration



7941 5

A. Installed in BA11K Expander Box



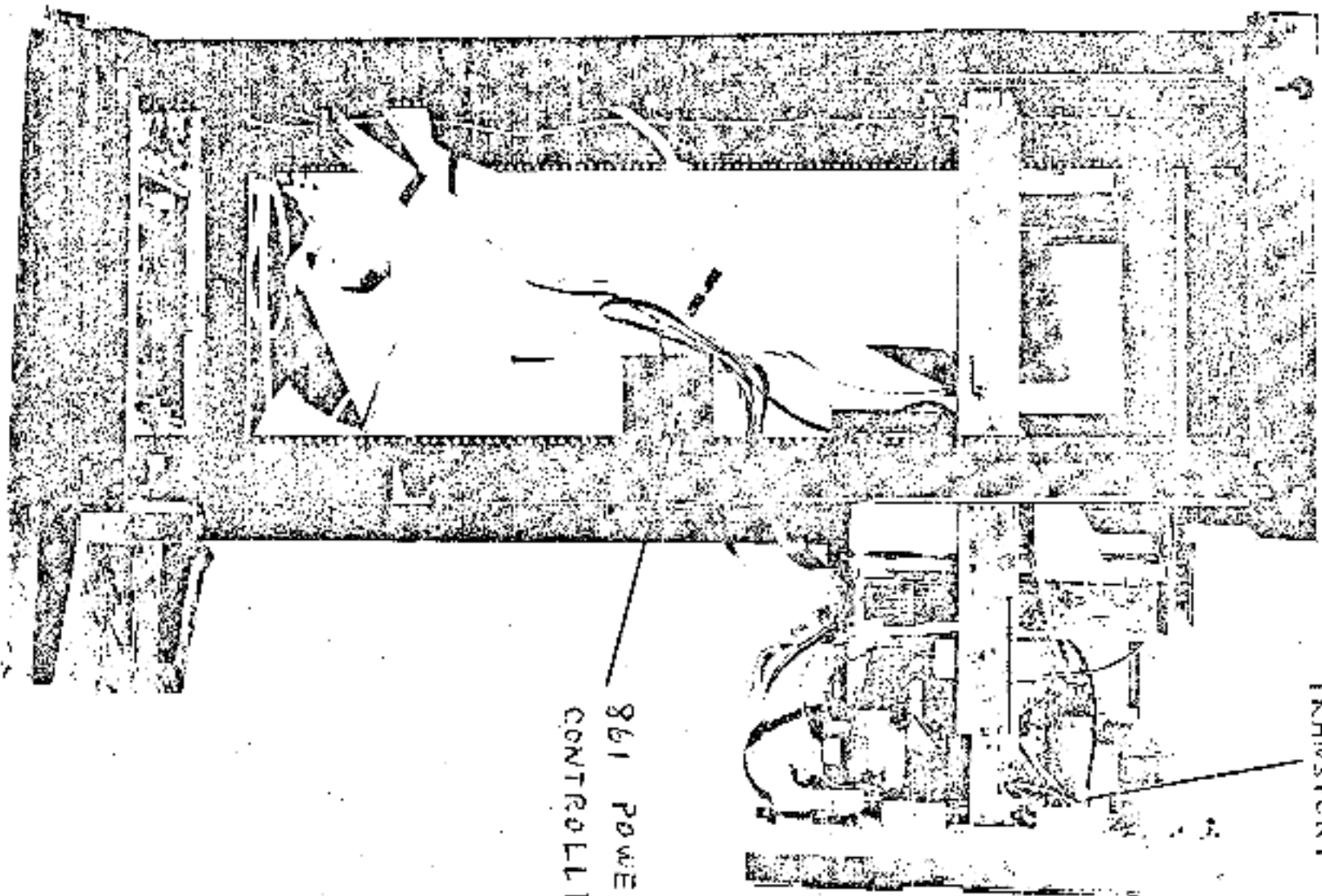
7997 2

B. Installed in BA11F Expander Box

Figure 1-2 TMB11 Controller

1-3

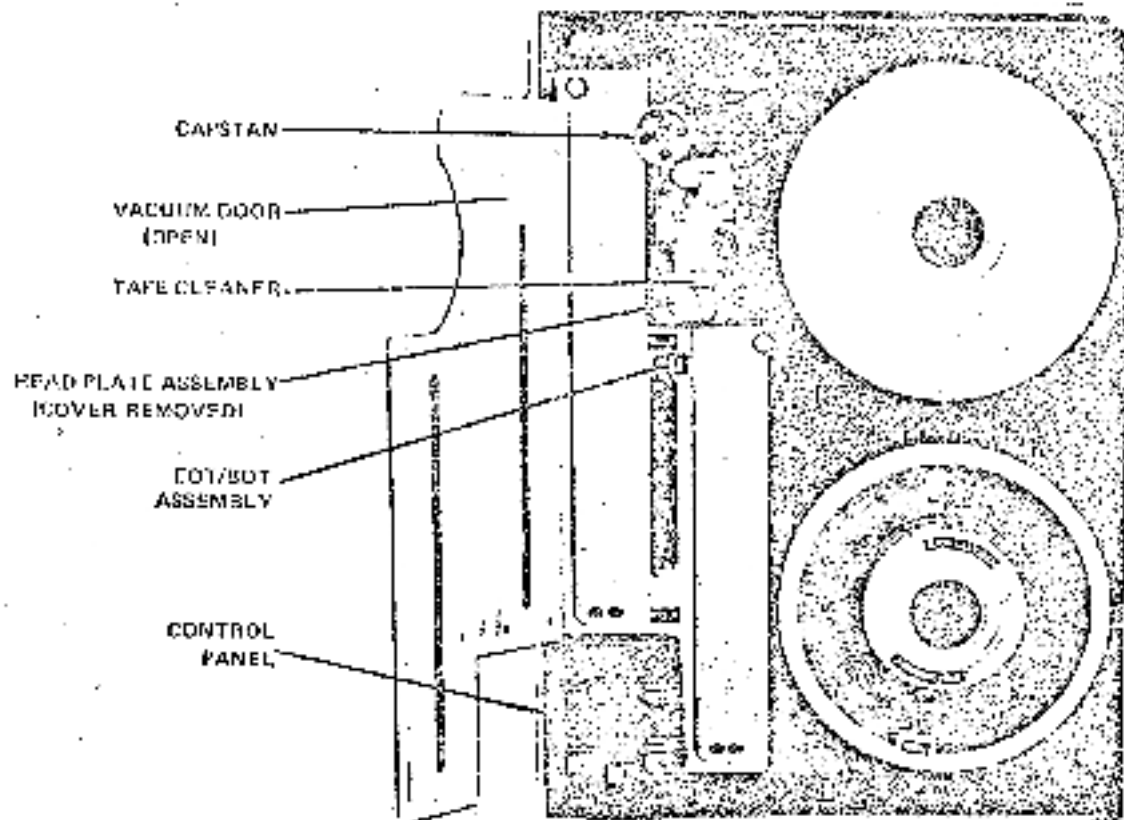
1-4



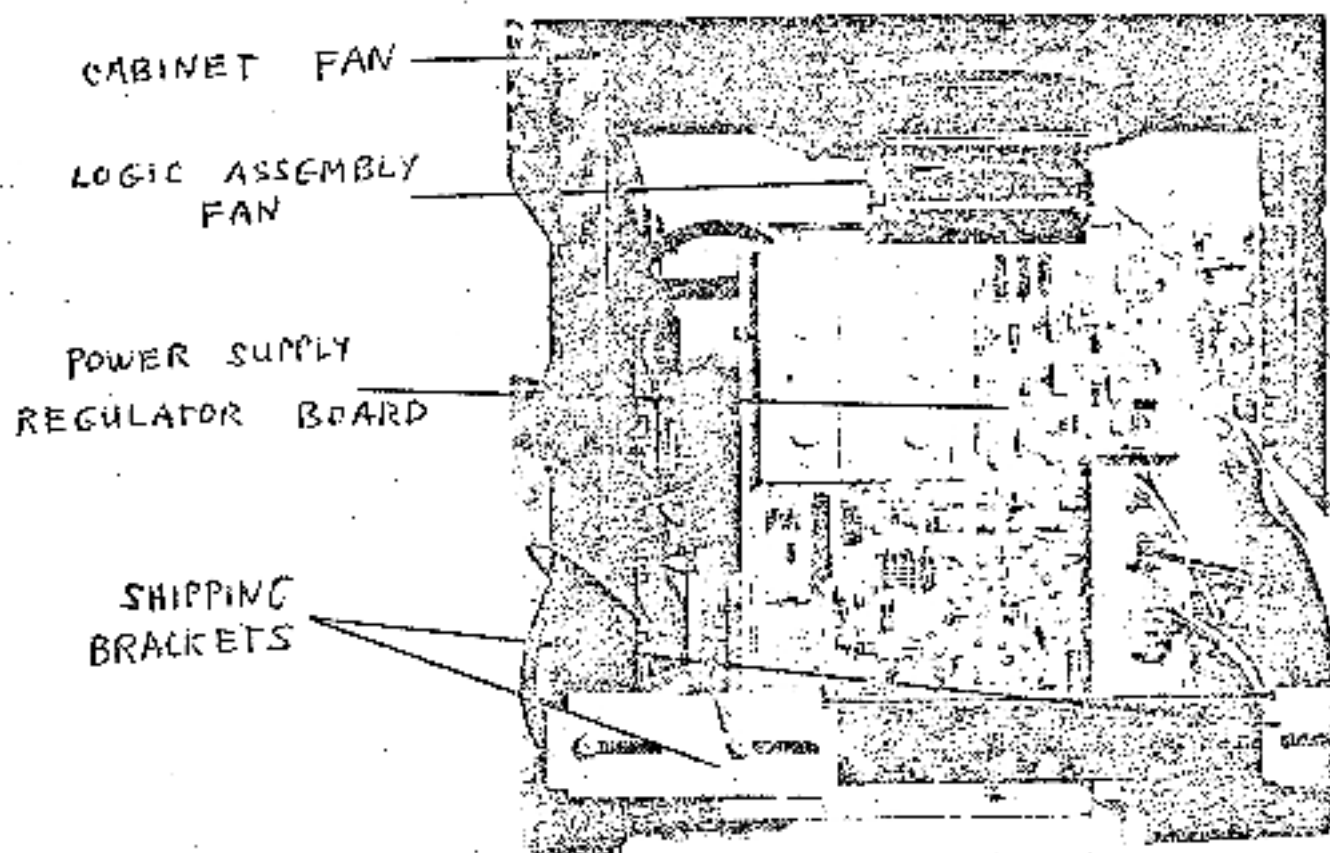
TU10W TAPE
TRANSPORT

861 POWER
CONTROLLER

Fig 1-3 TU10W with Transport Extended



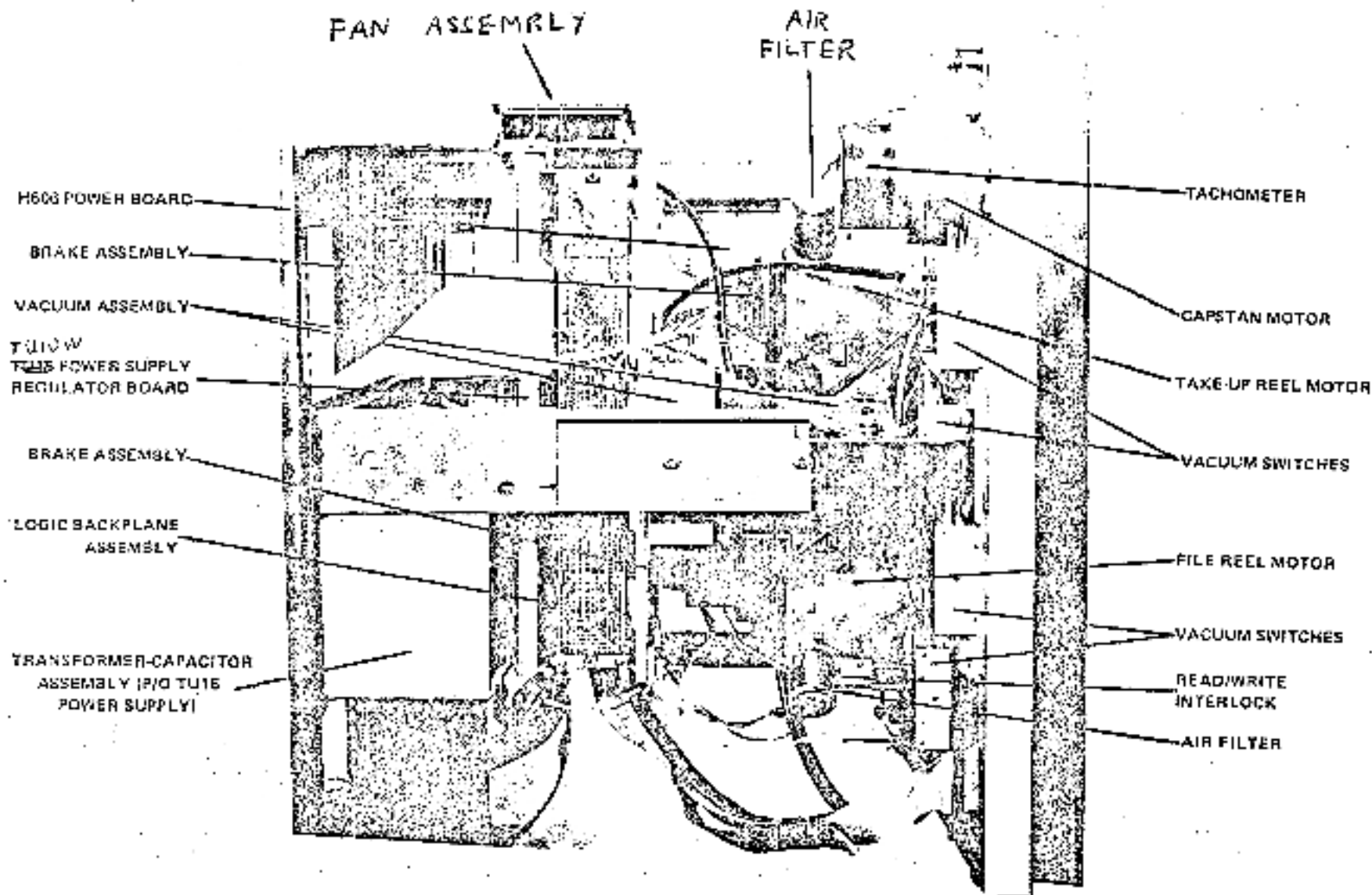
A. FRONT VIEW



B. REAR VIEW

FIG. 1-4

TU10W Transport, Front and Rear Views

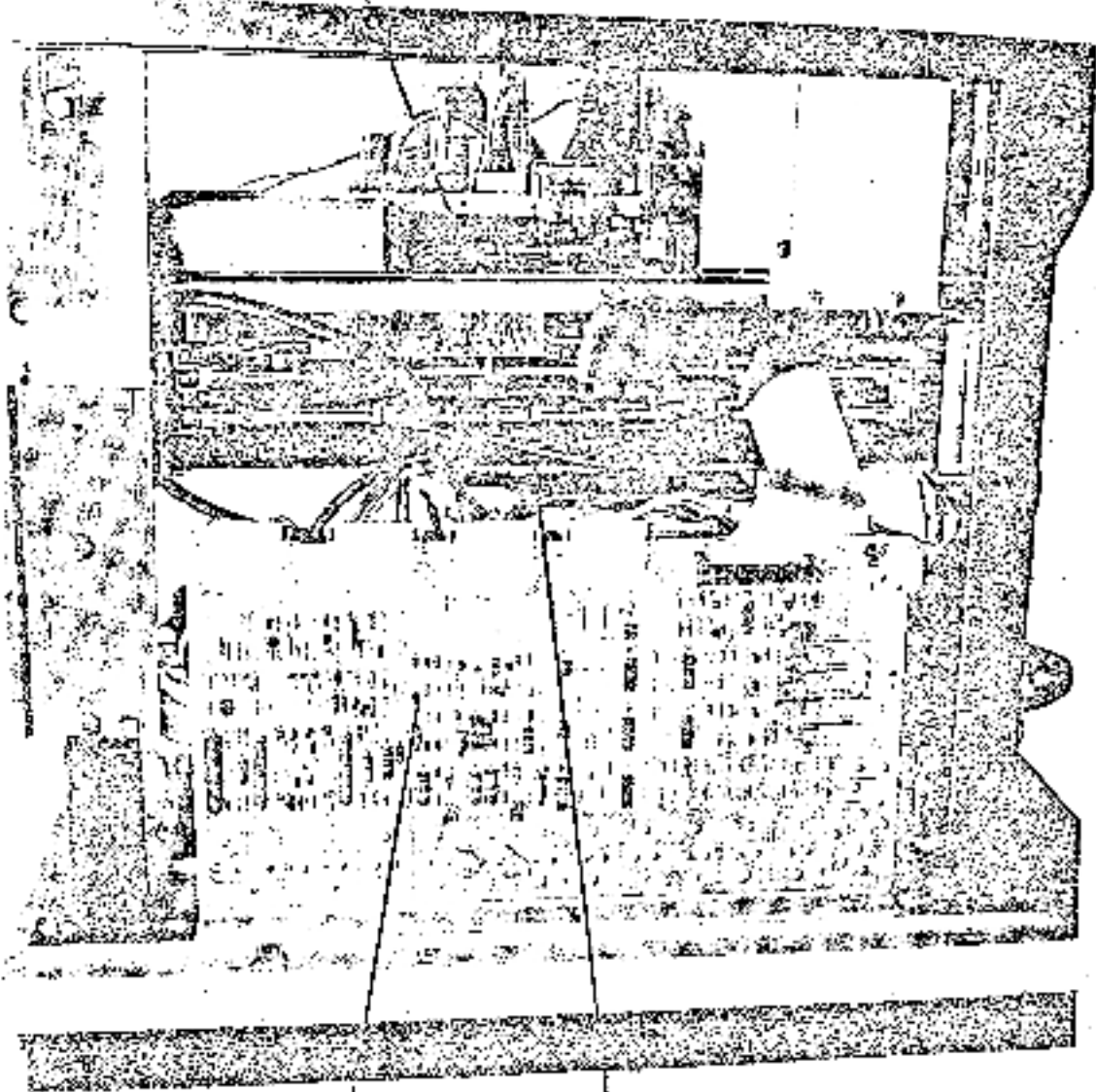


A. Left Side

FIG. 1-5

TU10W Transport, Side Views

POWER
SUPPLY
REGULATOR
BOARD



H606
POWER BOARD

LOGIC
ASSEMBLY

B. Right Side

The TU10W master transport consists of an M8926 interface module and a "host" transport. The M8926 processes commands from the controller and issues motion and read/write commands to the host and slave transports; the M8926 also monitors status lines from the host and slave transports. Any status changes at the selected transport are reported immediately to the controller. In response to inputs from the M8926 module, the host transport controls tape motion and records and reads data on magnetic tape.

The TU10W slave transport consists of a tape transport only. In response to inputs from the M8926 module in the master transport, it controls tape motion and records and reads data on magnetic tape.

The various models of the TU10W transport are identified by a two-letter dashed suffix. The first letter of the suffix designates the number of tracks on the transport; E for a 9 track transport, F for a 7 track transport. The second letter identifies the transport as a master or a slave (A,B,C,D=master; E,F,H,J=slave) and specifies the voltage and frequency requirements. Table 1-1 summarizes the TU10W models and their identifying suffix.

Table 1-1 TU10W Models

TU10W-EX=9 track			TU10W-FX=7 track		
Master/Slave	X=	Voltage/Freq	Master/Slave	X=	Voltage/Freq
Master	A	115v/60 Hz	Master	A	115v/60 Hz
	B	230v/60 Hz		B	230v/60 Hz
	C	115v/50 Hz		C	115v/50 Hz
	D	230v/50 Hz		D	230v/50 Hz
Slave	E	115v/60 Hz	Slave	E	115v/60 Hz
	F	230v/60 Hz		F	230v/60 Hz
	H	115v/50 Hz		H	115v/50 Hz
	J	230v/50 Hz		J	230v/50 Hz

1.3 SYSTEM FUNCTIONAL DESCRIPTION

The basic functions performed by the controller are: off-line, read, write, write EOF, space forward, space reverse, write-with-extended-IRG, and rewind. Each of these functions is briefly described in Table 1-2.

Table 1-2 Controller Functions

Function	Description
Off-Line	<p>The off-line function is used when it is desired to return control to the tape transport so that tape can be rewound, reels changed, etc. without using processor time.</p> <p>The off-line function places the selected tape transport in the off-line (local) mode and causes it to begin a rewind operation.</p> <p>The controller cannot write on or read from the magnetic tape when the off-line function is used.</p>
Read	<p>This function permits reading from the magnetic tape. During the read operation, the data portion of the record is loaded into the controller data buffer for transfer to the memory. The LRC and CRC characters are read but not transferred into memory.</p>

Write

This function permits writing on the magnetic tape. During the write operation, data from the bus is loaded into the controller data buffer register. The controller then transfers the data to the tape transport write heads. The necessary LRC and CRC characters are generated by the master transport and written on the tape following the data. The write function advances the tape one record.

Write EOF

This function writes an end-of-file (EOF) mark on the tape. When selected, this function erases a 3-in. segment of tape prior to writing the first character. The EOF mark and the associated LRC character are considered one record. The EOF mark is an octal 23 character (9-track drive; octal 17 for 7-track drive) followed by an octal 23 (or octal 17) LRC character.

Space Forward

This function is used to skip over a number of records to find a specific record on the tape. When selected, the space forward function causes the tape transport to advance a specified number of records. The number of records is determined by the value in the

byte record counter. This value is loaded into the byte record counter by the program.

Space forward is used for tape positioning only and, therefore, does not affect information stored on the tape or in memory.

Space Reverse

This function is identical to the space forward function except the tape moves in the reverse rather than in the forward direction.

Write-with-Extended-IRG

This function is identical to the write function except that a 3-in. segment of tape is erased before writing the first character.

Rewind

This function is used for rewinding the tape on the feed reel so that the tape can either be unloaded from the transport or operation can start at the beginning of the tape. When this function is used, the tape moves in the reverse direction, at a much higher speed (150 in./sec) than for other functions, until the beginning-of-tape (BOT) marker is detected. When the BOT marker is detected, the tape slows down and comes to a complete stop at a point beyond the BOT marker. It then moves forward until the BOT marker is again detected, whereupon, it comes to a final stop.

Rewind is used for tape positioning only and has no effect on information stored on the tape or in the memory.

Figure 1-6 is a functional block diagram of the TMB11/TU10W DECmagtape System. The processor initiates a TMB11/TU10W operation by addressing the TMB11 registers via the address decoder and loading the operation parameters into the registers. The BUS CO-C1 bits specify an out transfer (with respect to the processor) causing SEL OUT to be asserted for the particular register addressed. As each register is selected, the processor places the appropriate data on the Unibus data lines which is then loaded into the register with the SEL OUT strobe. Thus, the command register receives the type of operation to be performed; the byte-record count register receives the number of bytes to be transferred; and the current memory address register receives the memory address of the first byte to be transferred.

The command register selects which transport is to be involved in the transfer via the SEL 0-SEL 2 lines, supplies the function command to the command decoder which generates the required commands for the tape transport, and asserts the GO bit to the start logic. When the start logic senses that the tape transport has been selected (SELR) and is ready (TUR), it asserts SET to the transport to start the operation.

If a read operation is commanded, the transport command logic asserts FOR to the tape drive system which drives the capstan servo and moves the tape forward. When the tape is up to speed the M8926 read channels are enabled by READING and start to transfer data from the read heads to the controller. The read data from the tape transport (RDS-RD7, RDS) is checked for CRC, LRC and vertical parity errors by the M8926 board.

If any such errors are detected, the TMB11 error logic is notified (CRCE, LRCE, VPE) for appropriate corrective action.

The read data is supplied to the controller along with a read strobe (RDS) which signifies the availability of read data from the transport RD0-RD7 becomes CHAN0-CHAN7 and is gated to the data buffer register where it is loaded into the register by RDS.

RDS also requests an NPR transfer from the NPR logic. When the request is granted BUS BBSY is asserted by the logic along with DATA→BUS which gates the output of the data buffer to the Unibus data bus (BUS D00-D15) via the register select output multiplexer. DATA→BUS accomplishes this by asserting either HI DATA BYTE or LO DATA BYTE from the read byte select logic according to whether the CMA register is addressing the low byte or the high byte in memory. Thus, the data bytes from the data buffer will output on either BUS D00-D07 or BUS D08-D15. The next character read will output on the alternate half of the data bus. When the NPR logic receives BUS SSYN from the memory it asserts NPR CLEAR BBSY which increments the byte-record counter and the CMA register to prepare for the next transfer.

When the M8926 read logic detects the end of a record it asserts CRCS (9 track only) and LRCS to the controller and RD CLR PLS to the motion control logic. The motion control logic asserts EMD and STOP to the drive to stop the capstan servo motor.

If a write operation is commanded by the command register, the GO BIT, in addition to enabling the start operation logic, requests an NPR transfer from the NPR logic. When the request is granted, the logic asserts

BUS BBSY and BUS MSYN. The memory responds with SSYN to indicate that the first data character is on the data bus (BUS D00-D15). The NPR logic asserts DATA STB 2 which loads the data character into the data buffer, thus making it available to the transport as WDO-WD7. The data character enters the data buffer via one of two gates. In the write mode CMA BIT 00 asserts either SEL LO BYTE or SEL HI BYTE according to whether the CMA register is addressing the low byte or the high byte in memory, thereby enabling the gate corresponding to the location of the character on the data bus.

Meanwhile, the start operation logic has asserted SET to the transport which, as in a read operation, will cause the transport command logic to assert FOR and start the capstan servo system moving forward. When the tape is up to speed the drive sends WRT CLK pulses to the write channels and writing of the data characters begins. WDR (write data ready) from the controller enables the write channels which transfer the write data from the controller to the write heads in the tape drive. The write channel logic also produces REC pulses which record the data characters on tape via the write heads. A parity bit is generated for each character and is recorded on tape along with the character. When all the data has been transferred to tape WDR negates enabling the end of record generator which functions to place the CRC character (9-track only) and the LRC character on tape.

Each time a data character (not the CRC or LRC character) is written on tape, a WRS pulse is issued to the controller requesting the next character to be written. The WRS pulse makes an NPR request from the NPR logic and the cycle is repeated. Note that in a write operation, t

GO BIT makes the first NPR request and the WRS strobes make the second and subsequent requests. After the NPR logic issues DATA STB 2 it asserts NPR CLEAR BBSY which increments the byte/record counter and the CMA register to prepare for the next transfer. When the byte/record counter senses that the desired number of bytes have been transferred (written), it asserts CARRY OUT 2 which negates WDR to the transport thereby signaling the M8926 write logic to write the end of record check characters (CRC and LRC).

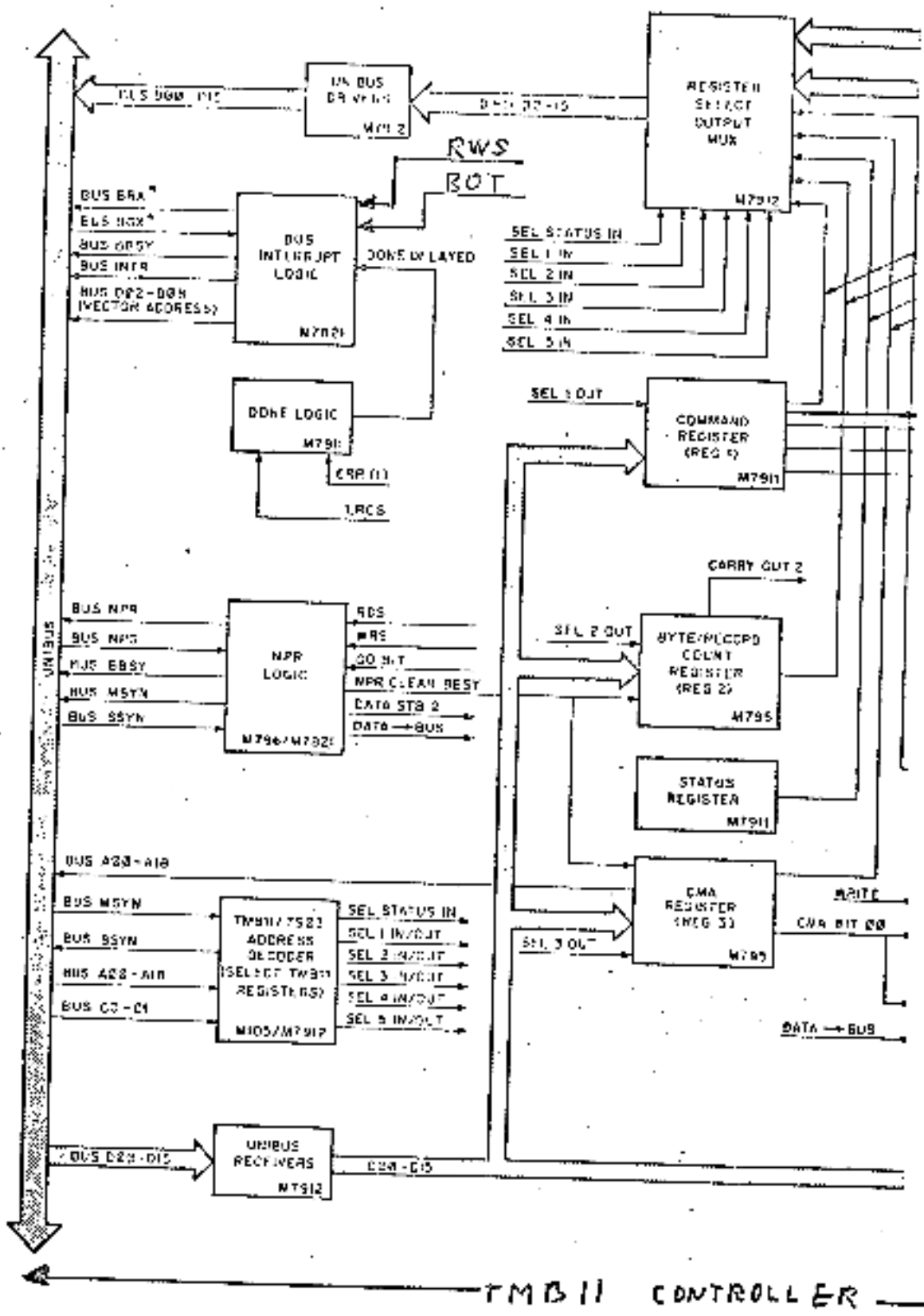
The M8926 read logic is enabled during a write operation and reads each character right after it is written. When the read logic detects (reads) the end of the record it issues a CRCS (9-track only) and LRCS strobe to the controller.

The LRCS strobe at the end of the record indicates to the controller that the data transfer is completed. The LRCS strobe is applied to the done logic which then asserts DONE DELAYED to the bus interrupt logic. The interrupt logic requests a bus interrupt to notify the processor that the command operation has been completed and the TMB11/TU10W is ready for another command.

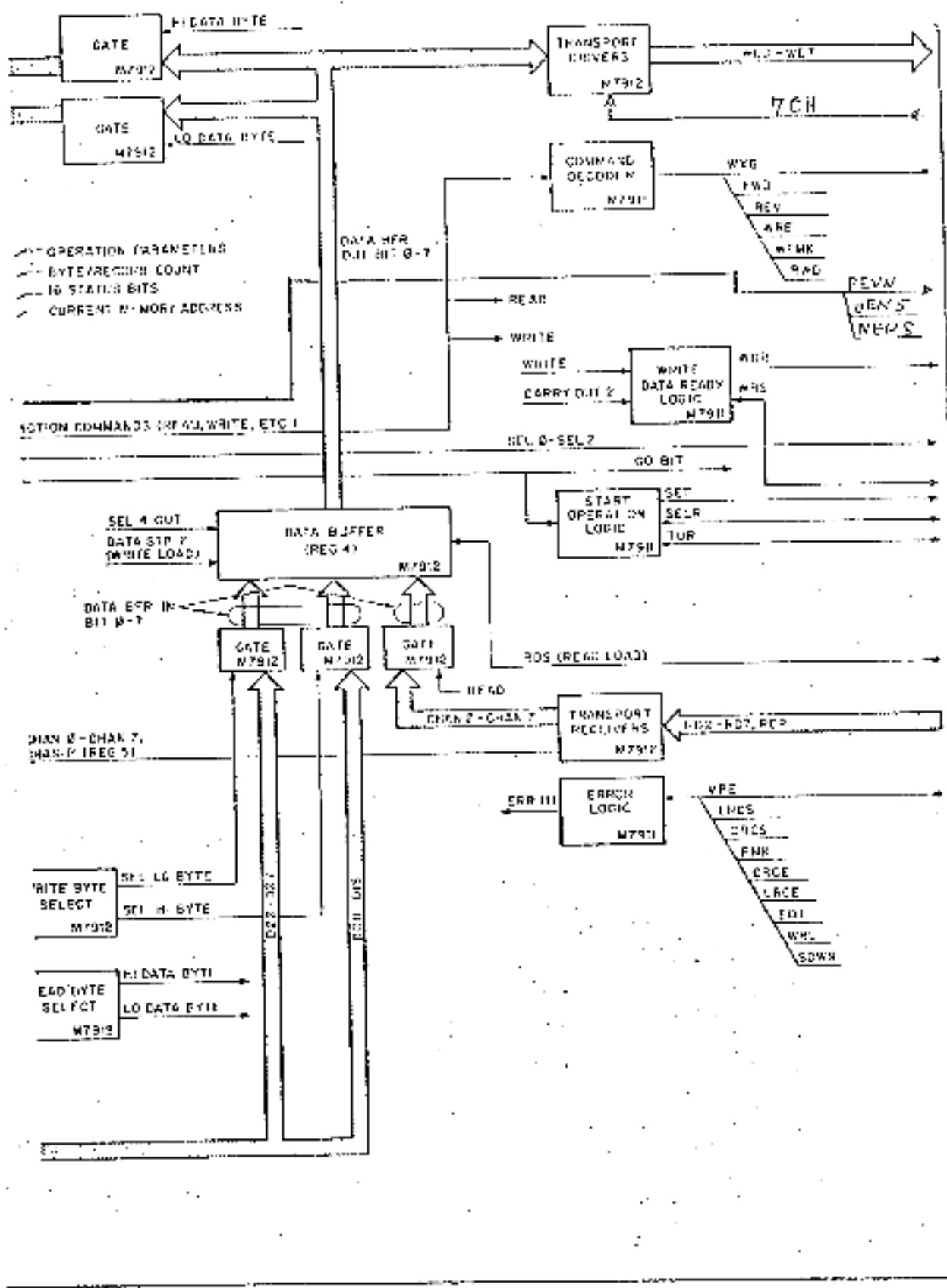
The TMB11 error logic monitors transport status including parity, CRC, and LSC errors and asserts ERR(1) to the done logic if an error condition exists. Some types of errors warrant terminating an operation before it is completed while others wait until the end of the operation before asserting ERR(1).

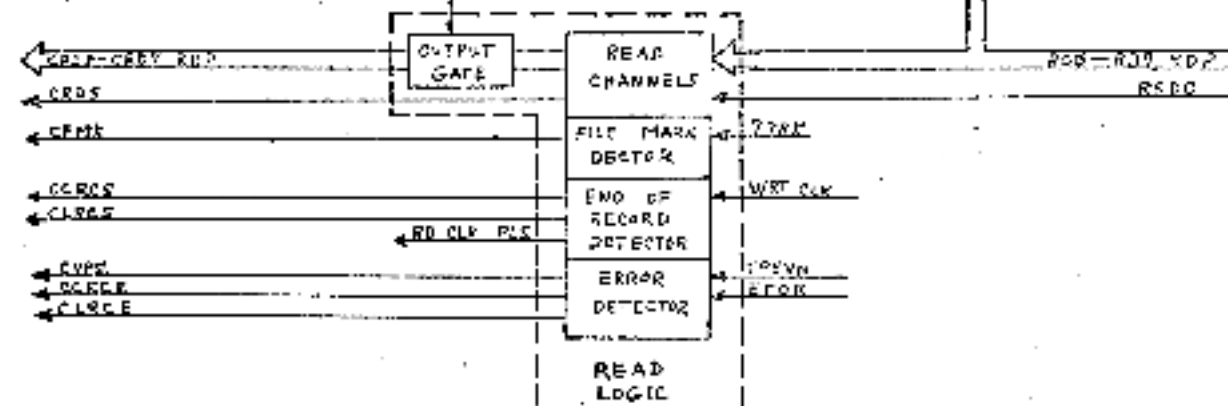
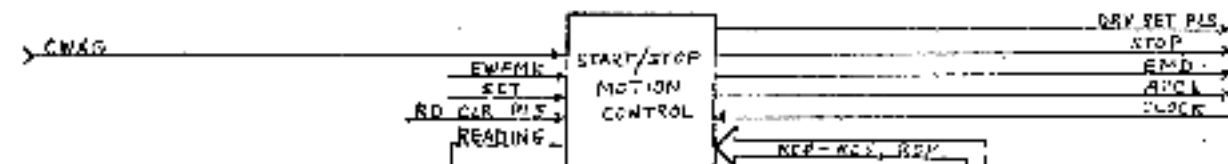
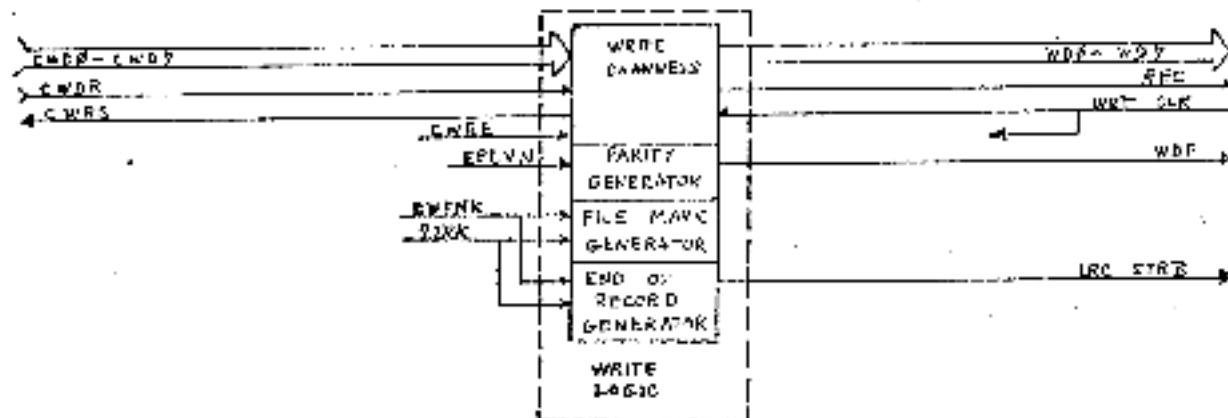
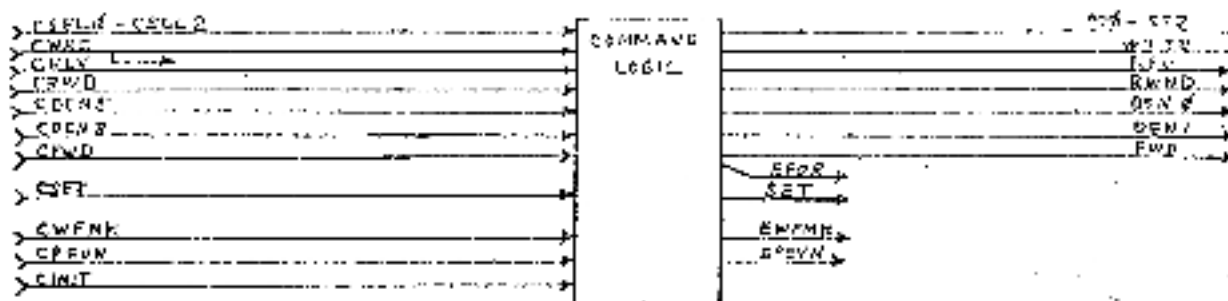
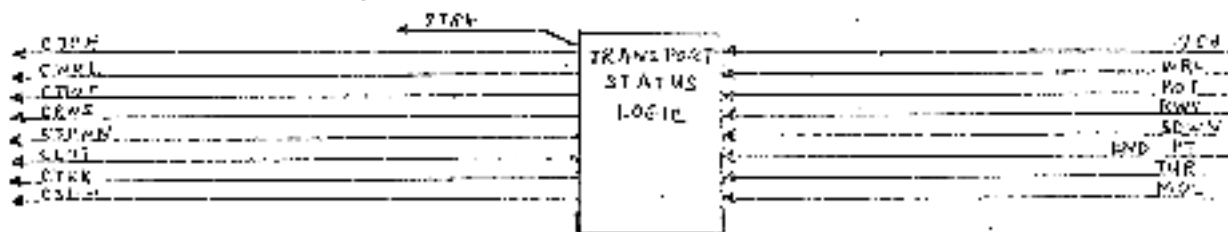
The processor can read the TMB11 registers by addressing the registers and requesting an in-transfer (with respect to the processor) via the BUS CO-C1 bits. The address decoder then asserts SEL IN for the particular register selected which gates the register bits out to the data bus via the register select output multiplexer.

Detailed operation of the TMB11 is given in chapter 6 of this manual. Detailed operation of the M8926 interface board and the TU10W tape transport are given in chapters 7 and 8. Figure 1-6 can be used along with the functional block diagrams and flow diagrams contained therein.



TMB II CONTROLLER





TAP E
TRANSFOR

M8926
INTERFACE
BOARD

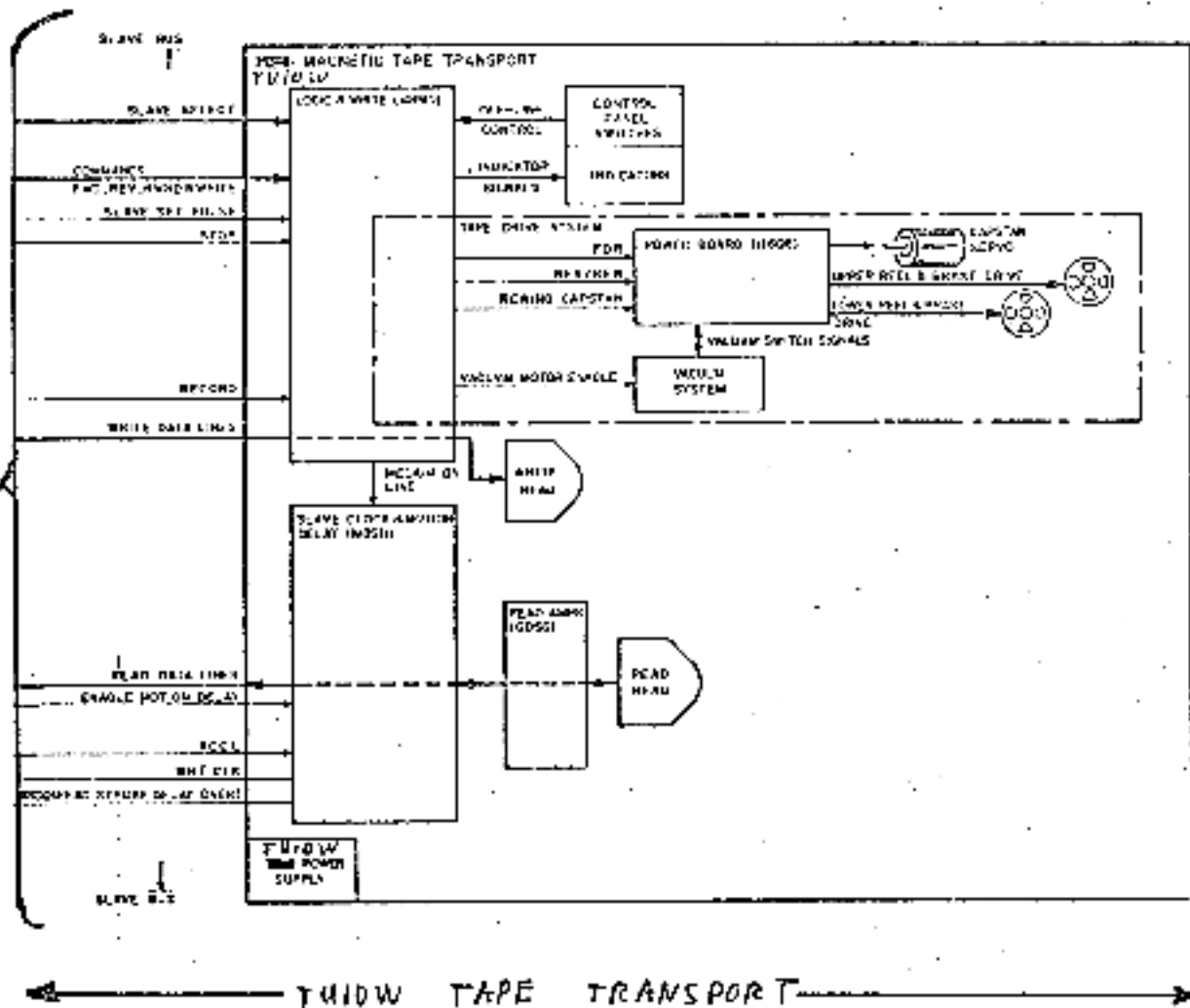


FIG. 1-6

TMBtt/TU10W Functional Block Diagram

1.4 APPLICABLE DOCUMENTS

Table 1-3 lists documents that are applicable to the TMB11/TU16W DECmagtape System.

Table 1-3 Applicable Documents

Title	Number	Description
861-A,B,C Power Controller Maint. Manual	EK-861AB-MM-002	Contains theory of operation and maintenance instructions for the 861 Power Controller
TU16/TM02 tape drive system Maint. Manual	EK-TU16-MM-002	Contains theory of operation and maintenance instructions for the TU16/TM02 tape drive system
PDP-11 Processor and Systems Manual	•	A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 system
PDP-11 Processor Handbook	†	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
PDP-11 Peripherals Handbook	112-00973-2908	A handbook devoted to a discussion of the various peripherals used with PDP-11 systems. It also provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
DIGITAL Logic Handbook, 1973-74 Edition		Presents functions and specifications of the K-series logic modules, accessories, and connectors used in the TMB11 Controller and the TU16W DECmagtape Transport. Includes other types of logic produced by DEC but not used with PDP-11 devices.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

*Applicable manuals are furnished with the system at time of installation. The document number depends upon the specific PDP-11 family processor.

†Use the processor handbook unique to the actual CPU.

1.5 SPECIFICATIONS

Table 1-4 contains operational, environmental, mechanical and electrical specifications for the TMB11/TU10W Tape Drive System.

Table 1-4 TMB11/TU10W Specifications

Category	Parameter	Specification
Main Specifications	Storage medium	1/2 in. (1.27 cm) wide magnetic tape (industry compatible)
	Capacity/tape reel	23 million characters
	Data transfer rate	36,000 char/sec
	Drives/control, maximum	8
Data Organization	Number of tracks	7 or 9
	Recording Density	200, 556, 800 bpi; program selectable
	Interrecord gap	0.5 in. (1.27 cm) minimum; 0.65 in. nominal
	Recording method	NRZI; industry compatible
Tape Motion	Speed; Forward and Reverse	45 in./sec (1.14m/sec)
	Rewind speed	150 in/sec (3.8m/sec)
	Tape drive	single capstan; vacuum columns
	Start/stop distance	0.25 in. (6.3mm)
	start/stop time	8 ms maximum
Tape Characteristics	Width	0.5 in (1.27 cm)
	Length	2400 ft. (731.6m)
	Type	Mylar base, iron-oxide coated
	Thickness	1.5 mils (0.038 mm)
	Tension	8.0 oz (227 g)
	Reel diameter	10.5 in (26.7 cm)
	Reel hub	3.69 in (9.37 cm) diameter (industry standard)
Mechanical	TMB11 Controller	Mounts in a single 16-1/2X2-1/4 in. system unit (41.9X5.7 cm)
	Tape drive, mounting	Mounts on slides in a standard 19 in (48.3 cm) cabinet
	TU10W Transport (without cabinet)	
	Depth	25 in. (0.64m)
	width	19 in. (0.48m)
	Height	26 in. (0.65 m)
Weight	150 lb (70kg)	

	861 Power Controller	
	Depth	8 in. (0.20m)
	Width	19 in. (0.40m)
	Height	5 in. (0.13m)
	Weight	10 lb (4.54kg)
Interchannel Displacement	Write	75 μ in. (1.9 μ m) maximum
	Read	75 μ in. (1.9 μ m) maximum
	Erase head	Full width
Power	Input current (TMB11)	5A at +5Vdc
	Input current (TU10W)	8A at 115V; 4A at 230V
	Input Power	264W at 115V; 132W at 230V
	Voltage	115/230Vac \pm 10%
	Frequency	47 to 63 Hz; single phase
Operating Environment	Temperature	15 $^{\circ}$ C to 32 $^{\circ}$ C*
	Relative humidity	20% to 80%, with maximum wet bulb 25 $^{\circ}$ C and minimum dew point 2 $^{\circ}$ C (no condensation)*
	Altitude	8000 ft (2438m)
Miscellaneous	BOT, EOT detection	Photoelectric sensing of reflective strip, industry compatible
	Broken tape detection	Vacuum fail-safe
	Magnetic head	Dual gap, read after write, 0.15 in. (0.4cm) gap
	Electrical skew	Write deskew only. Read skew mechanically aligned

*Magnetic tape operation is more reliable if the temperature is limited to 65 $^{\circ}$ to 75 $^{\circ}$ F (18 $^{\circ}$ to 24 $^{\circ}$ C) and the relative humidity to 40 to 60%.

CHAPTER 2

UNPACKING, INSTALLATION, AND ACCEPTANCE TESTING

2.1 SITE PLANNING AND CONSIDERATIONS

2.1.1 Space Requirements

Figure 2-1 illustrates the space and service clearances required. Adequate space must be provided to slide the equipment out of the rack for servicing and to open the front door on the TU10W DECmagtape transport. The TU10W and TMB11 are housed in separate cabinets. If the cabinets are separated by long distances, consideration should be given to overhead trenching ducts for the cabling.

2.1.2 Power Requirements

The TMB11/TU10W DECmagtape System can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained to within 10 percent of the nominal value and the frequency should not vary more than 3 Hz.

2.1.3 Environmental Requirements

The TU10W DECmagtape should be located in an area free of excessive dust and dirt or corrosive fumes and vapors. To ensure proper cooling, the bottom of the cabinet and the fan inlet at the top of the cabinet must not be obstructed. The operating environment should have cool, well-filtered, humidified air; a temperature range of 15° to 27°C; and relative humidity of 40 to 60 percent.

2.2 UNPACKING

The TMB11 may be shipped in two different configurations: installed in an equipment rack or packaged separately. Unpacking and installation procedures vary depending on the system configuration. For example,

make per port...

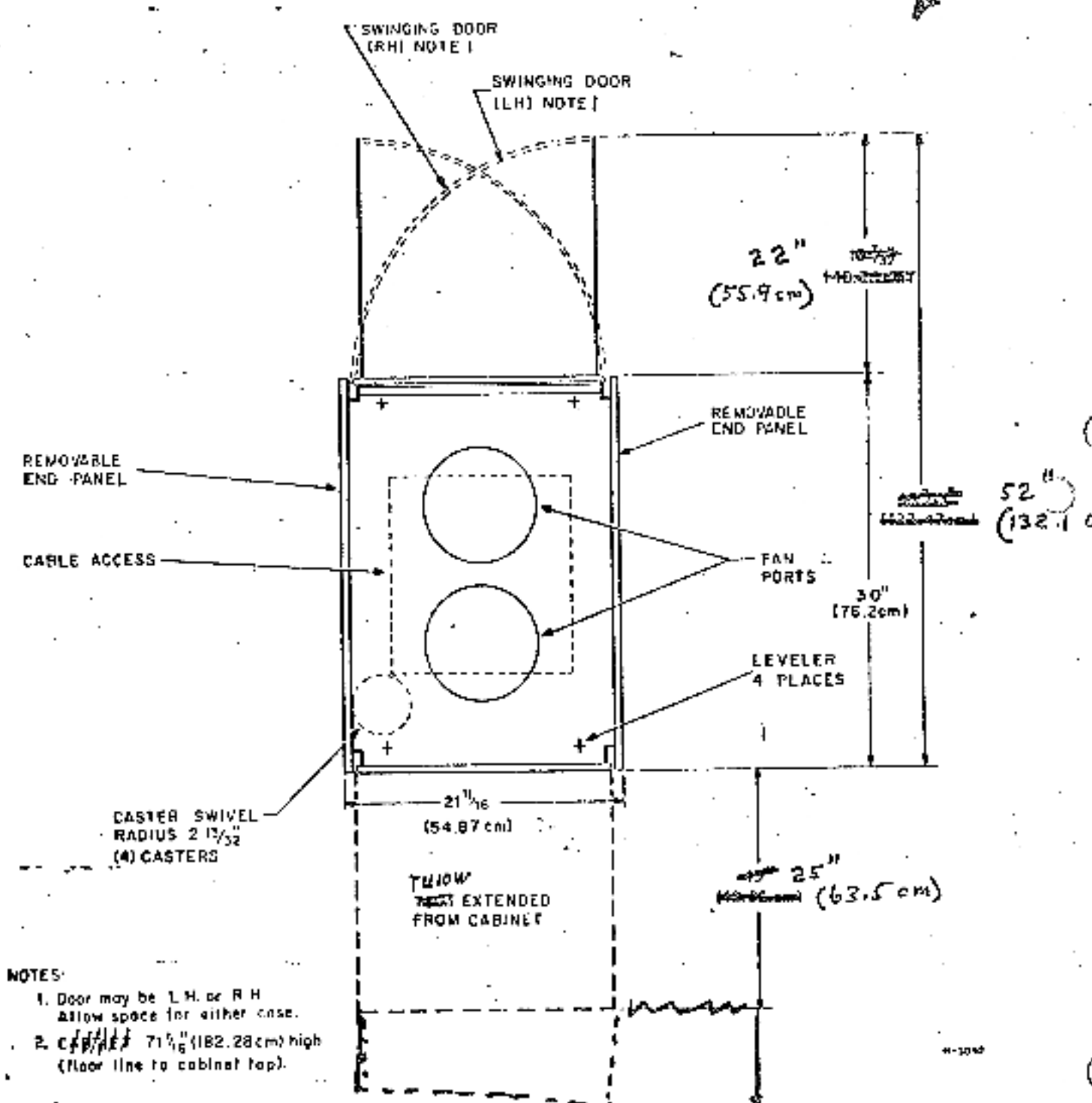


Figure 2-1 Space and Service Clearance, Top View

If the user has ordered a complete PDP-11 system the TMR11 is shipped installed in its appropriate rack. However, if only a part of the system is shipped because the user already has a basic PDP-11 system, then the TMR11 is shipped separately with the appropriate cables.

2.2.1 TMR11 Cabinet Unpacking

To unpack the cabinet, proceed as follows:

1. Remove outer shipping container.

NOTE

The container may be either heavy corrugated cardboard or plywood. In either case, remove all metal straps first, then remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter.

2. Remove the polyethylene cover from the cabinet.
3. Remove the tape or plastic shipping pins from the cabinet rear access door.
4. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting side rails and are exposed by opening the access door(s). Remove the bolts.
5. Raise the leveling feet above the level of the roll-around casters.
6. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.
7. Roll the system to the proper location for installation.

2.2.2 TMB11 Unpacking

Before unpacking the TMB11 controller check the shipping list to ensure that the correct number of packages has been received. Check the shipping list for the correct TMB11 module types. Carefully remove each device from its shipping carton.

2.3 INSPECTION

After removing the equipment from its container(s), inspect it and report any damage to the responsible shipper and the local DIGITAL sales Office. Inspect as follows:

1. Inspect all switches, indicators, and panels for damage.
2. Remove equipment covers where necessary and inspect for loose or broken modules, blower or fan damage, and loose nuts, bolts, screws, etc.
3. Inspect wiring side of logic panels for bent pins, broken wires, loose external components, and foreign material.
4. Check TU10W transport(s) for any foreign material that may have lodged in the tension arm, reel hubs, and other moving parts.
5. Check TU10W power supply for proper seating of fuses and power connectors.
6. Inspect each TMB11 module for shipping damage.

2.4 TU10W CABINET INSTALLATION

To install the TU10W cabinet, proceed as follows:

1. Lower the leveling feet so that the cabinet is resting on the floor, not on the roll-around casters.
2. Use a spirit level to level the cabinet; ensure that all leveling feet are firmly on the floor.

3. Remove the shipping screws that secure the equipment to the cabinet.
4. If two or more cabinets are to be bolted together, install filler strips (P/N D052-G) between the cabinets as shown in Figure 2-2. Tighten the bolts that secure the cabinet groups together and then recheck that the cabinets are level.
5. After the TU10W has been positioned per the site plan, loosen the two shipping brackets that secure the transport to the rear of the cabinet frame (see Figure 2-3).

NOTE

If the TU10W is to be reshipped or installed in a new location, the shipping brackets should be repositioned and tightened.

6. Ensure that the TMB11 cabinet and the TU10W cabinet are tied to the same ground or install a ground strap between the cabinets.
7. If necessary, clean all outer surfaces.

2.5 TMB11 Installation/Cabling

Ensure that power is removed from the PDP-11.

2.5.1 System Unit Installation

1. Extend the expander box on its slides and remove the module access cover. (An extended EA11K and EA11F box is shown in Figure 1-2.)
2. Install a TMB11 system unit into the expander box using the two captive screws (Figure 2-4).
3. Install the option power harness by connecting the fast-on

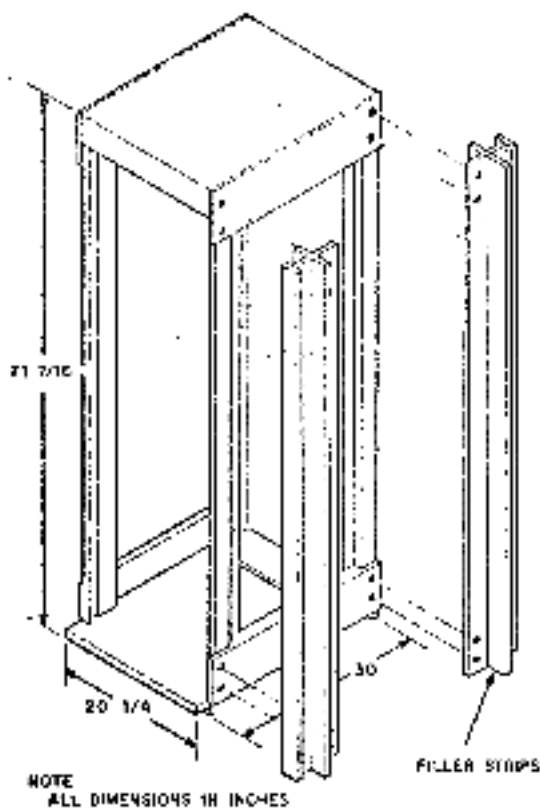


Figure 2-2 Installation of Filler Strips

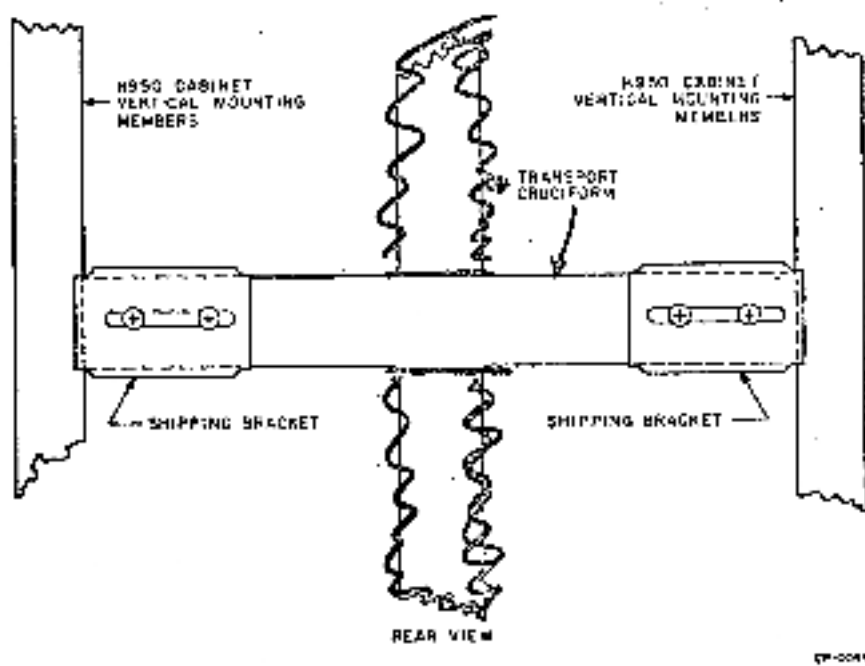


Figure 2-3 Transport Hold-Down Shipping Bracket

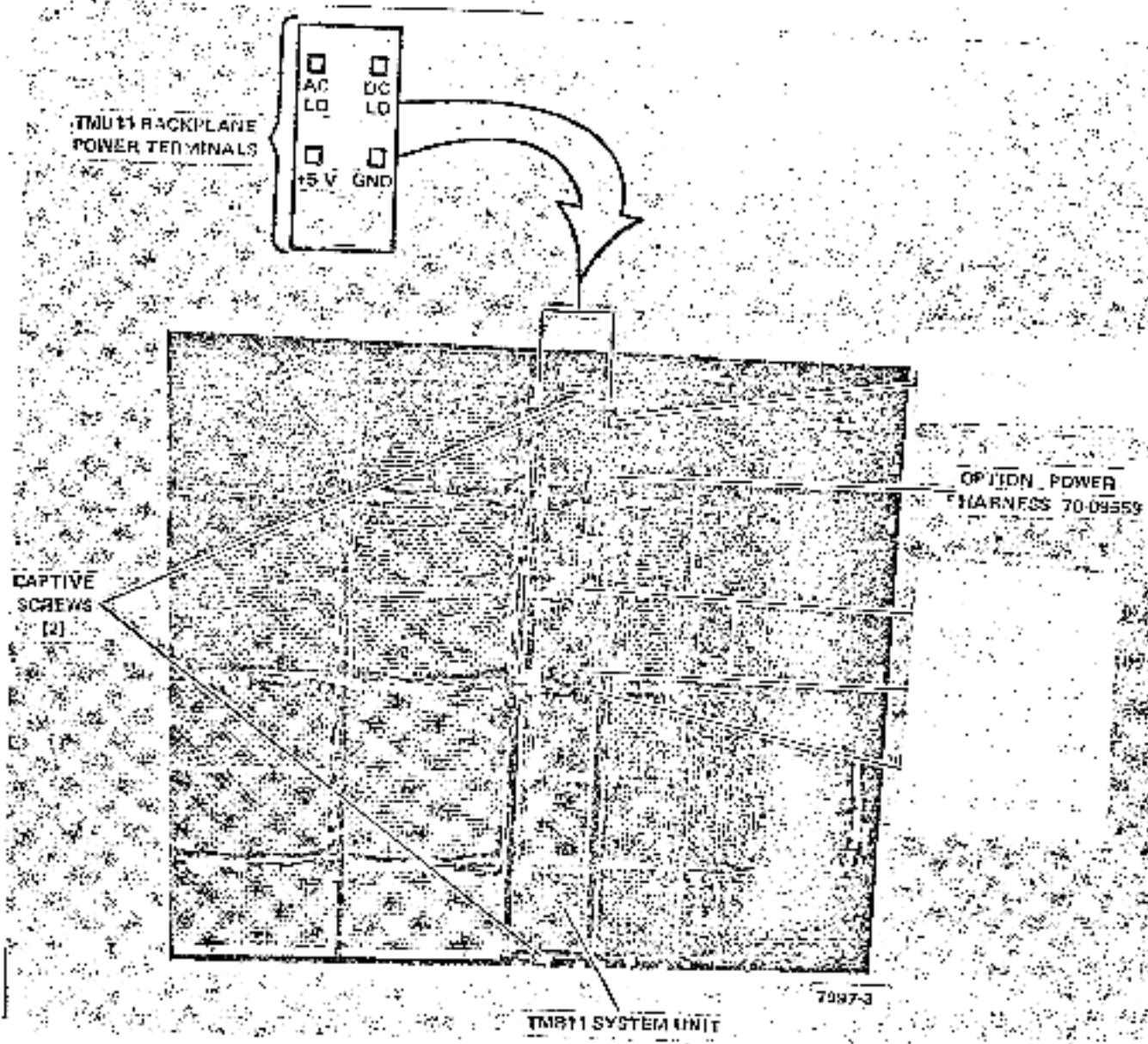


Figure 2-4 Expander Box Backplane (BA11F box shown)

connectors to the system unit backplane and the harness plug(s) to the expander box (Figure 2-5).

4. Dress the option power harness along the top of the DA11F expander box as shown in Figure 2-5. If a BA11K box is used dress the harness underneath the expander box.

2.5.2 Module Installation

1. Check the jumpers on the M7821 module for a bus interrupt address of 224.
2. Check the priority jumper on the M7912 module for the correct interrupt priority level (usually BR5).
3. Check the jumpers on the M105 module for the correct address range for the TMB11 registers (772520 to 772536).
4. Plug the six TMB11 modules and a M930 terminator module into the system unit according to Figures 2-6, 2-7, and engineering drawing BD-TMB11-6-7.

2.5.3 Unibus Cabling--System units are connected to the Unibus in daisy-chain fashion as shown in Figure 2-8. Each unit has a Unibus in- and a Unibus out-jack. A BC11A cable connects the Unibus into the first system unit. M920 jumper modules connect the Unibus to the other system units in a given configuration. An M930 terminator module is installed in the Unibus out-jack of the last system unit in the chain. If the Unibus is to be carried onto another expander box, a BC11A Unibus cable is used to connect the Unibus from the Unibus out-connector of the last system unit in the first box to the Unibus in-connector of the first system unit in the second box. The Unibus is terminated by an M930 module installed in the out-jack of the last system unit.

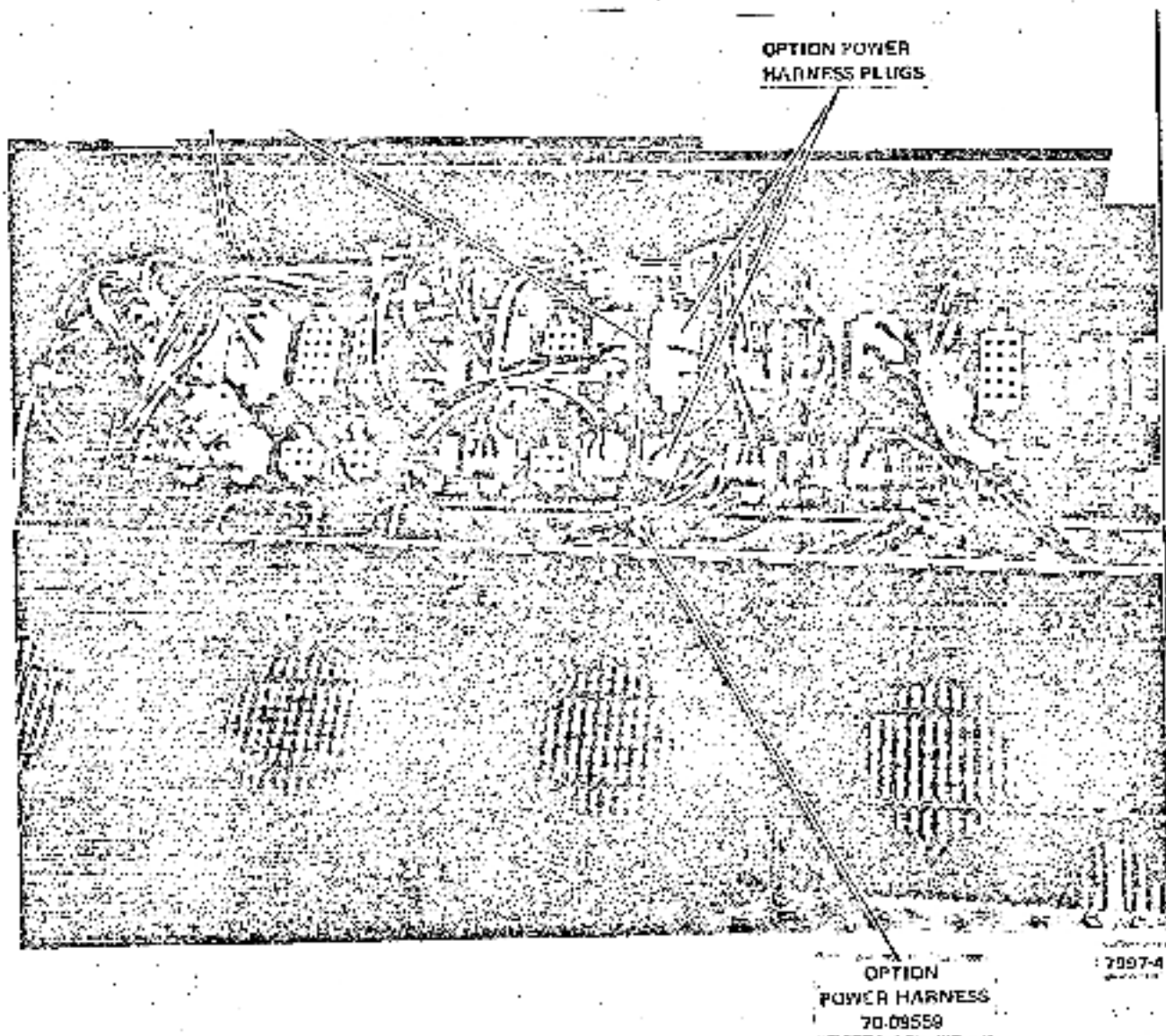


Figure 2-5 Power Cabling of TMB11 System Unit in BA11F Box

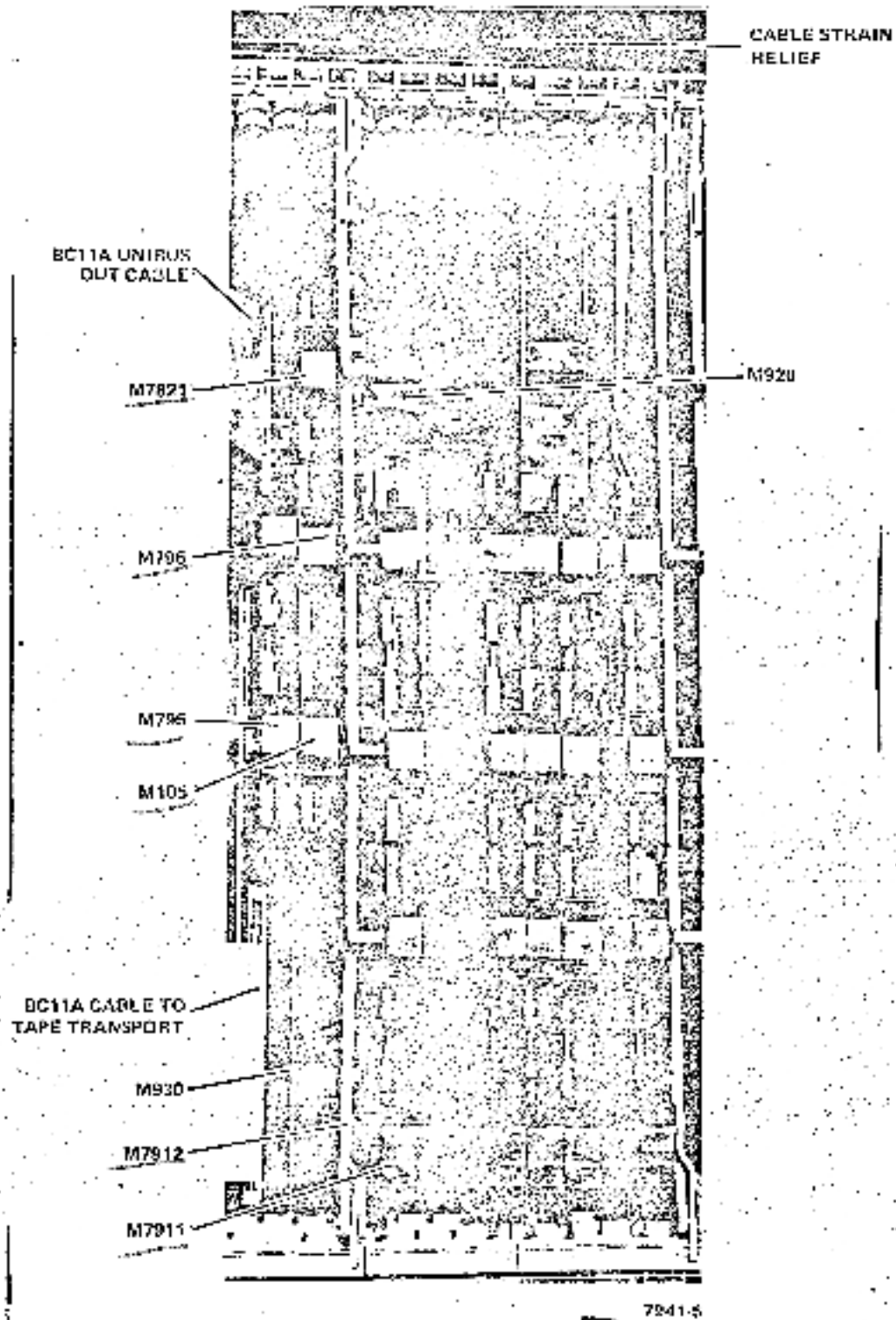


Figure 2-6 TMB11 Module Location and Cabling in BA11K Box

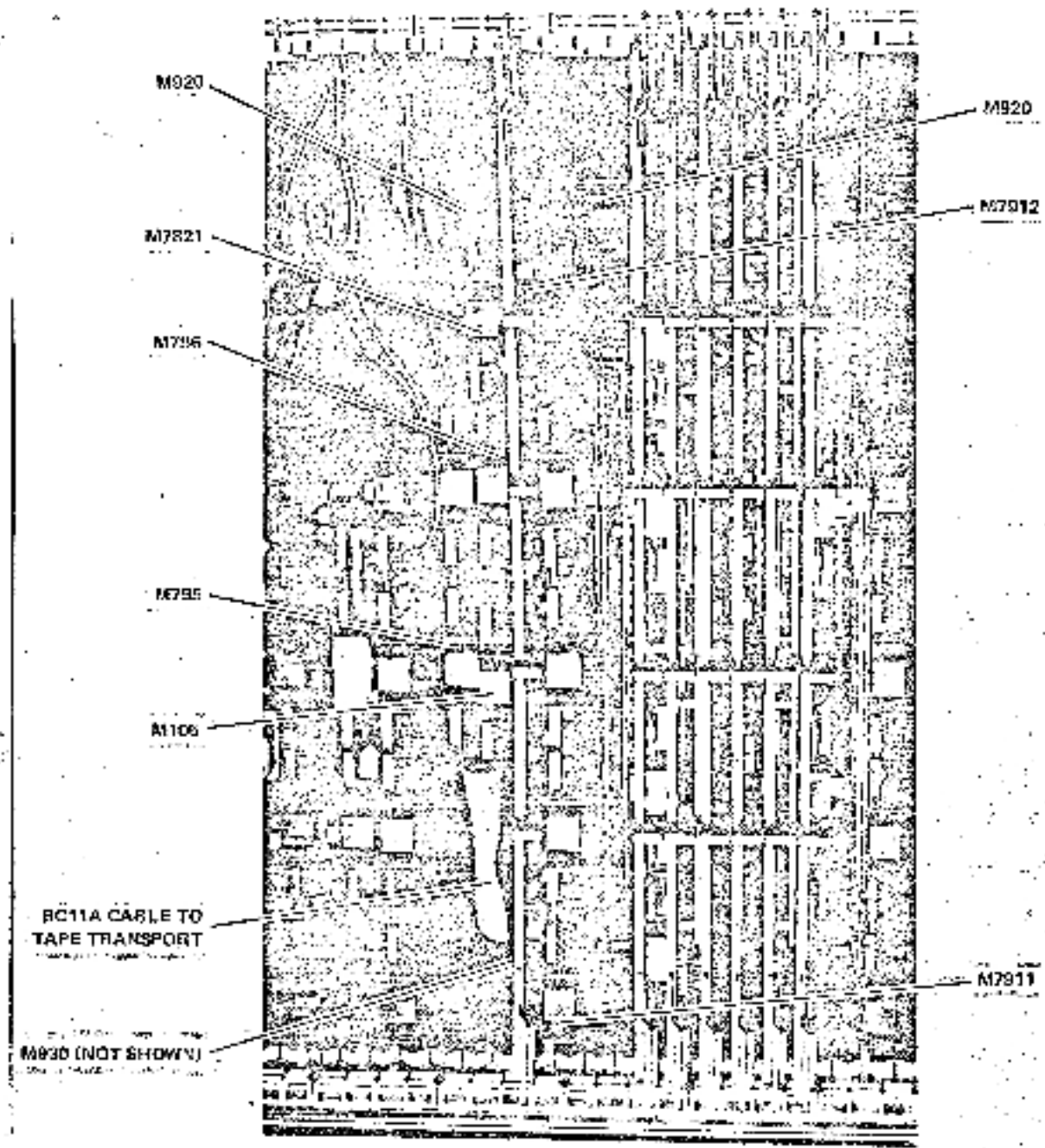


Figure 2-7 TMB11 Module Location and Cabling in BA11F Box

Install the Unibus in-cable, Unibus out-cable, M920 jumper and/or M930 terminator according to the particular configuration. The Unibus in-connections on the TMB11 system unit are slots B1 and B2. The Unibus out-connections are slots A4 and B4 (Figure 2-9 and engineering drawing DD-TMB11-9-7). The configuration shown in Figure 2-6 utilizes a Unibus out-cable and an M920 bringing the Unibus in from the next system device. The configuration shown in Figure 2-7 uses M920 jumpers for both input and output Unibus connections.

NOTE

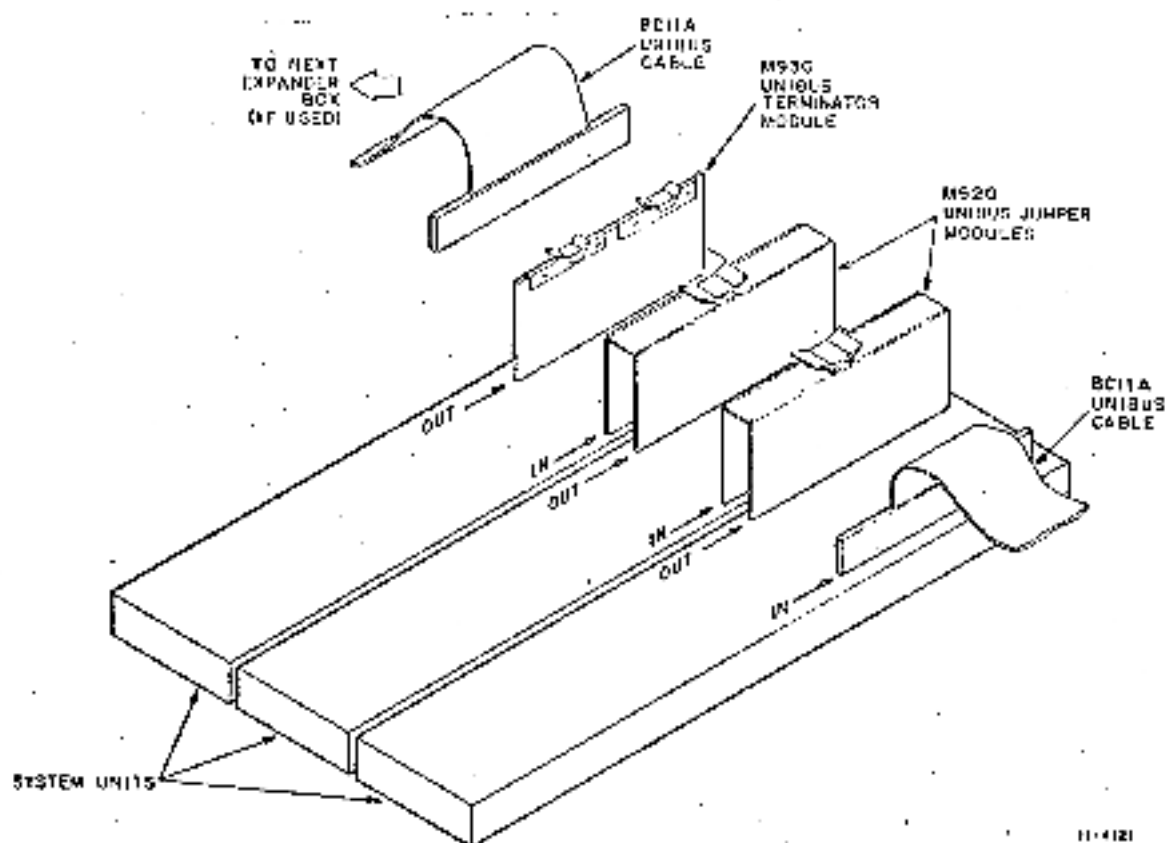
BC11A cable connectors will plug into the system units either way but will not fully seat if incorrectly installed. Make sure the connectors are fully seated and that the notches on the connector edges are up against the system unit slots.

2.5.4 Controller/Master Drive Cabling--Connect the BC11A cable to slots E4 and F4 on the system unit (Figure 2-9). Install an M930 terminator module into slots E3 and F3 to terminate the cable. (Figure 2-6 and engineering drawing DD-TMB11-9-7).

2.5.5 Securing Cables--If the installation is performed in a BA11F expander box, lift the cable trough cover and feed the BC11A cable(s) through the trough and the cable holding bracket.

If the installation is performed in a BA11K expander box, perform the following:

1. Remove one screw from the center strain relief and loosen the other (Figure 2-6).



11-4121

Figure 2-8 Unibus Cabling

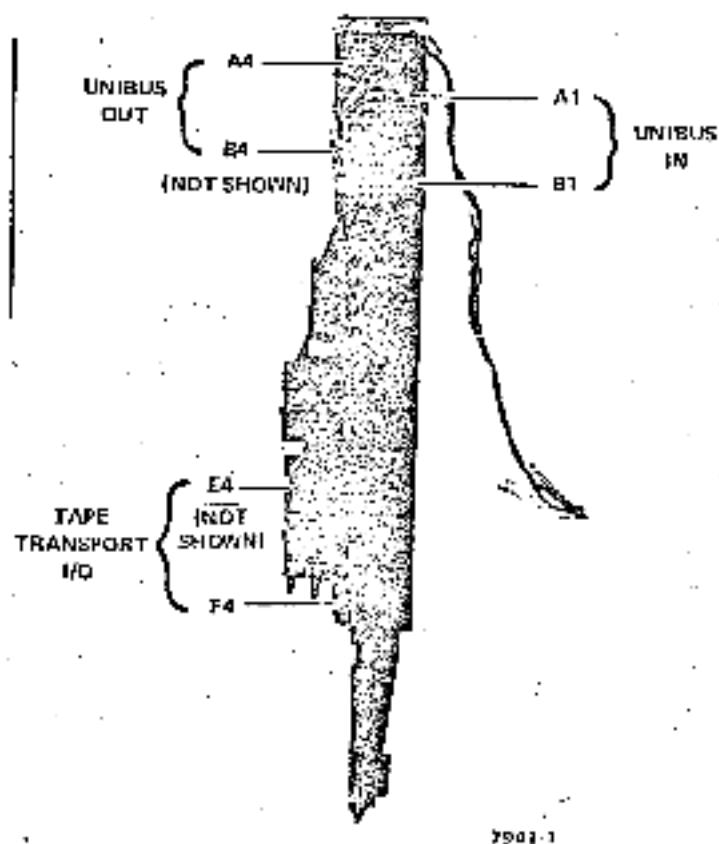


Figure 2-9 TMB11 Mounted in System Unit

2. Swing the strain relief out and place the BC11A cable(s) up against the edge of the chassis.
3. Swing the top of the strain relief back into place.
4. Insert the removed screw and tighten both screws.

2.6 TU10W Cabling

1. Slide the TU10W master transport out of the cabinet.
2. Remove the M8926 interface board from the transport system unit assembly.
3. Install M851 edge connectors on the J and K jacks of the M8926 board (Figure 2-10).
4. If there is only one TU10W in the system (the master drive) install P8800 terminators into jacks J1, J2 and J3 as shown in Figure 2-10.
5. Feed the BC11A cable from the TME11 through the slot between the system unit and the logic sheet-metal chassis (Figure 2-11).
6. If the system contains two or more tape drives, route three BC06R slave bus cables through the same slot used in step 5 but from underneath (Figure 2-11).
7. Position the M8926 board in its approximate location and connect the BC11A controller cable to the M851 edge connectors on the M8926 (Figure 2-12).
8. If this is a multidrive system, connect the three BC06R slave cables to J1, J2 and J3 on the M8926 board. Connect the cables so that the smooth side is up (Figure 2-13). Mark the BC06R slave cables.
9. Insert the M8926 board into the system unit.
10. If this is a multidrive system, secure the slave cables with the cable strain relief (Figure 2-11).

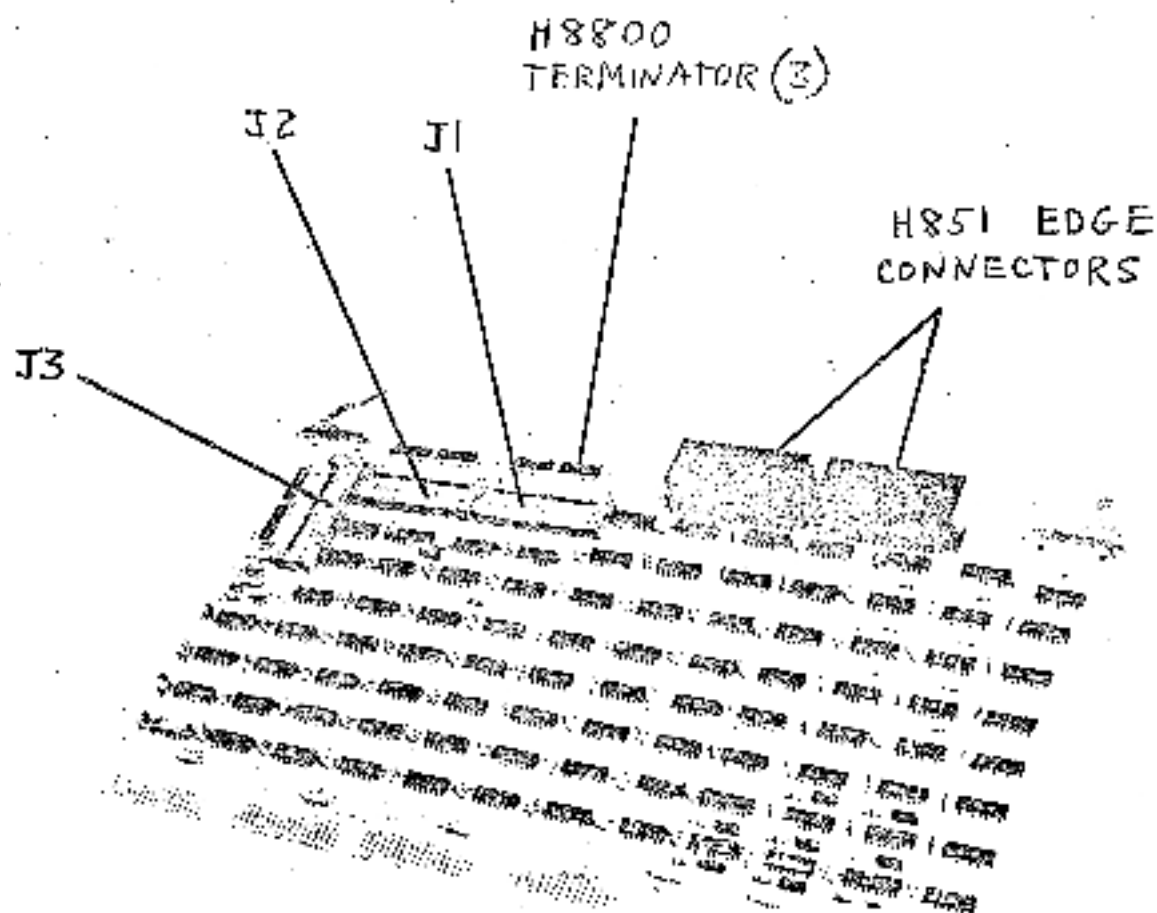


FIG 2-10

M8926 with H851 Edge Connectors and H8800 Terminators

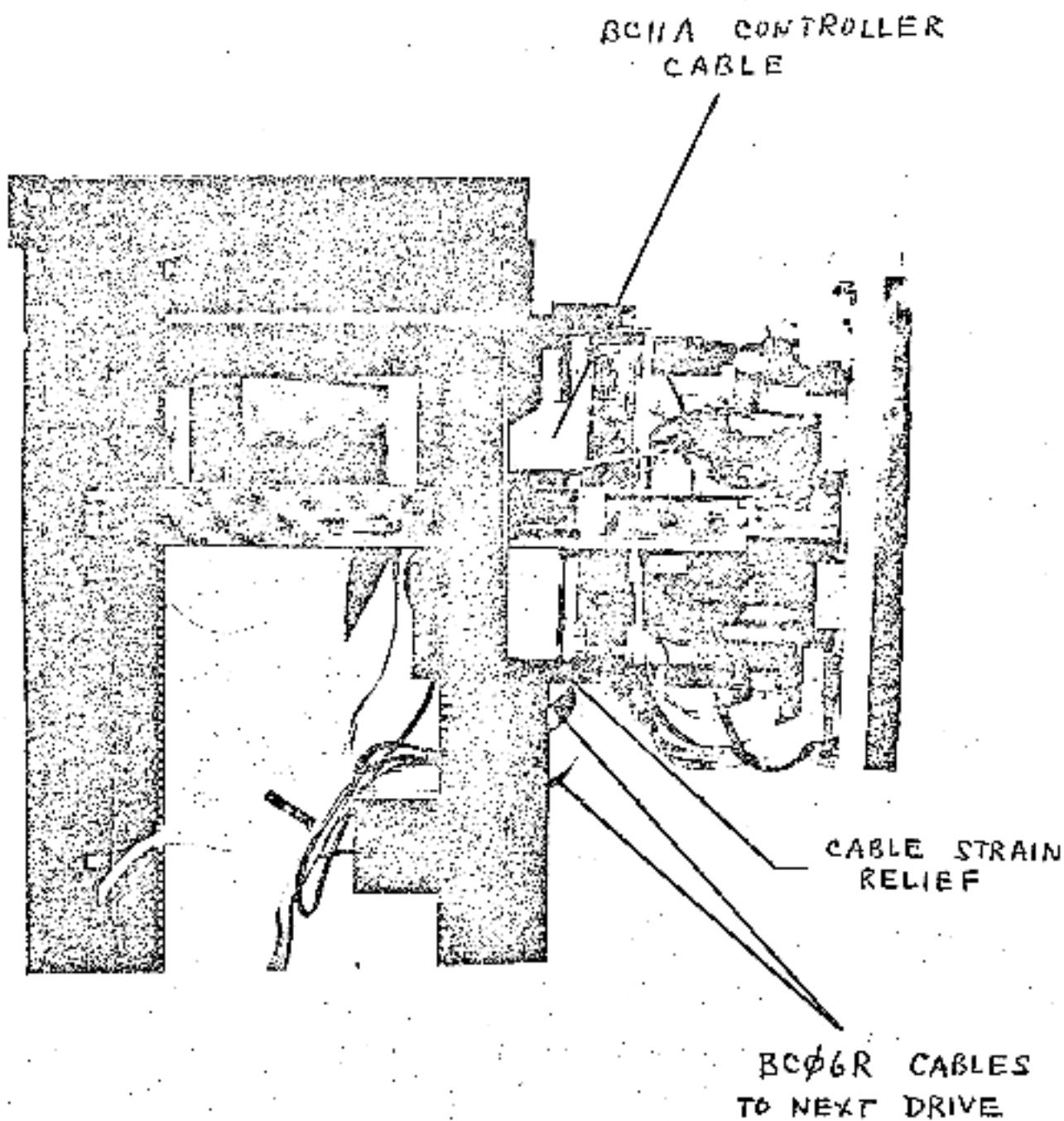


FIG. 2-11

Routing of BC11A and BC06R Cables

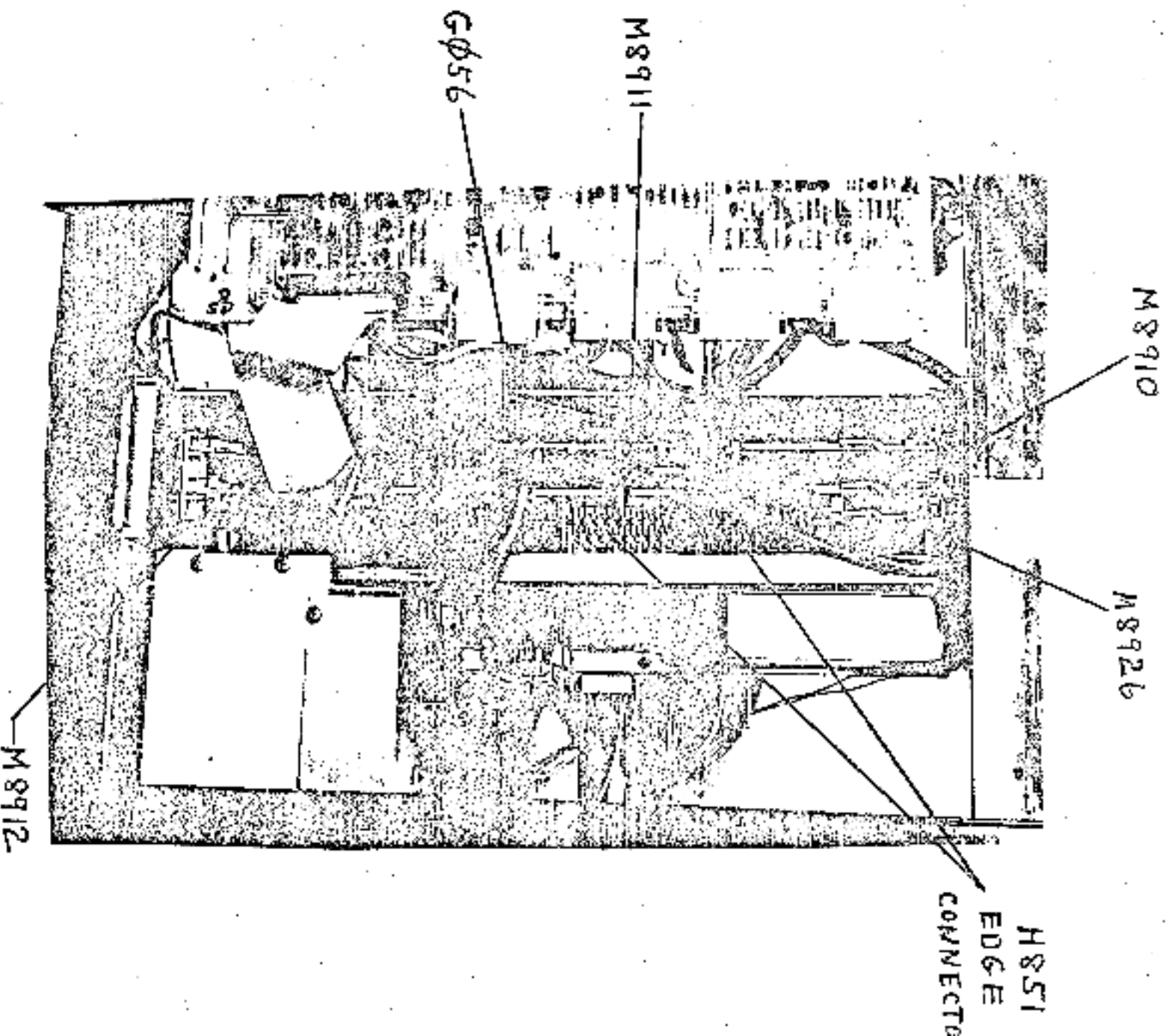


FIG. 2-12

7010W System Unit Modules

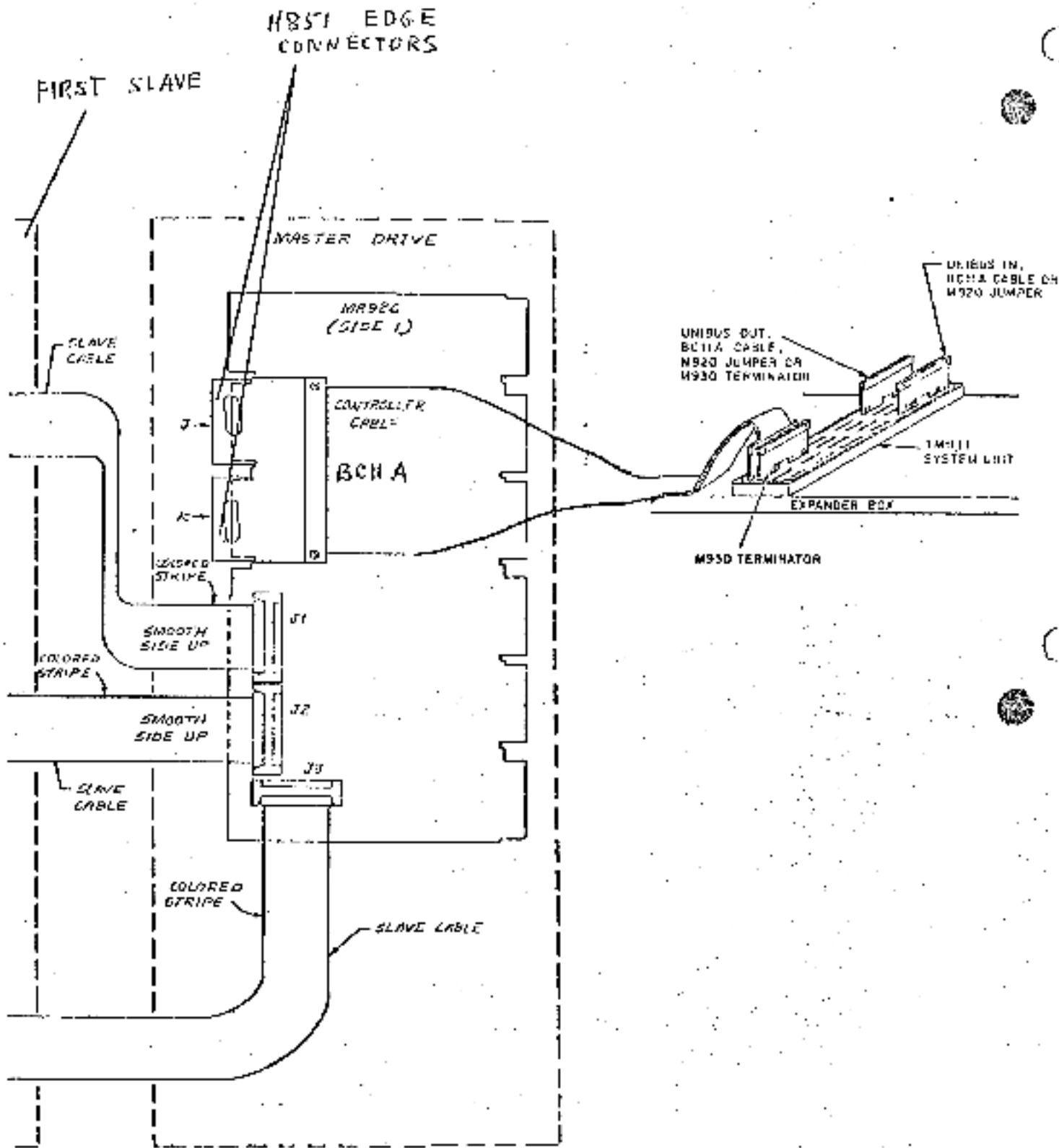
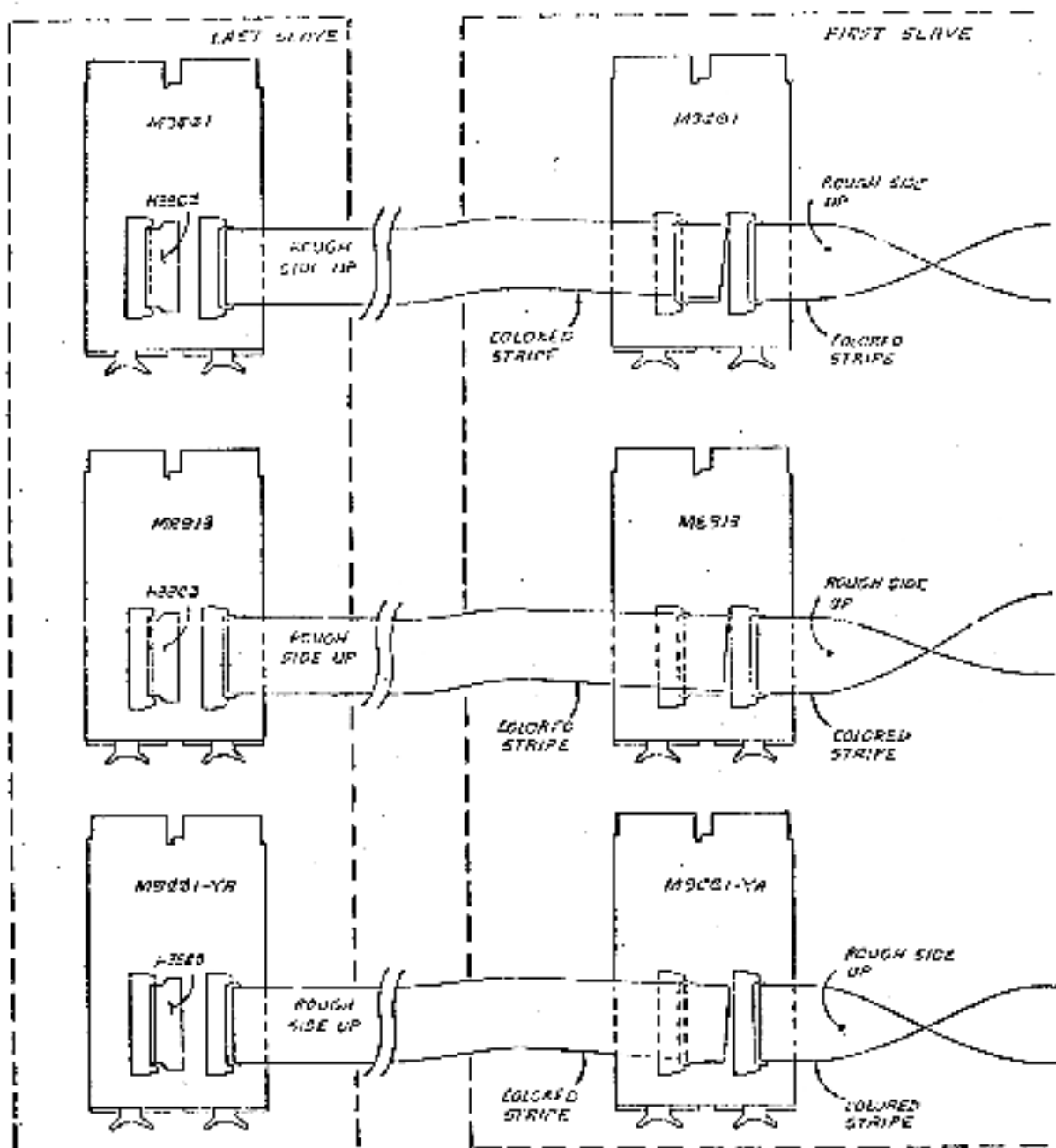


FIG 2-13

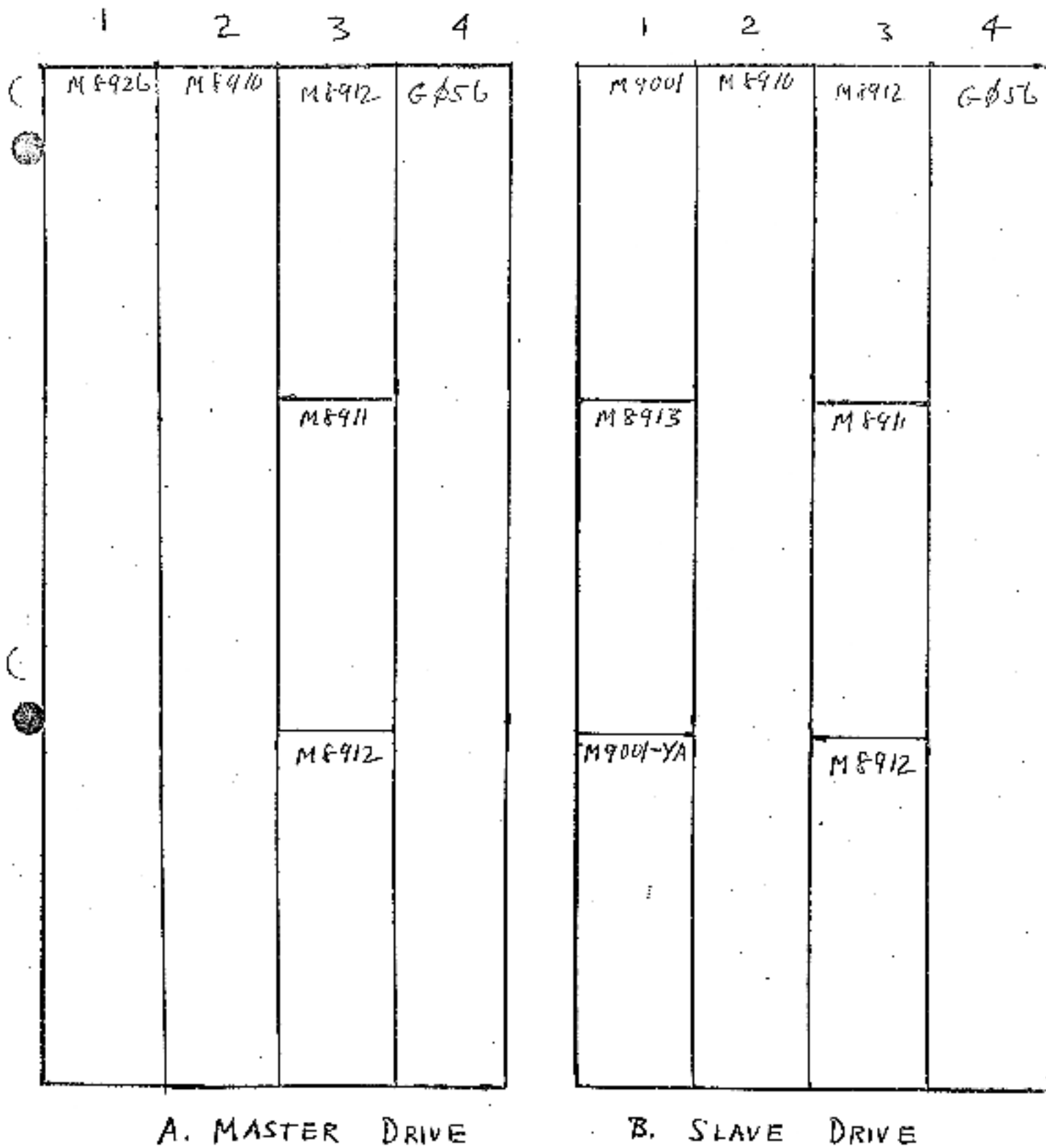
TM-11/TU10W Master/TU10W Slave Cabling Diagram



11. Remove M9001, M8913 and M9001-7A from the slave transport system unit (Figure 2-14).
12. Connect J1 on M8926 to the input jack on cable card M9001. Twist the BC06R one-half turn to obtain the color stripe and smooth side/rough side orientation shown in Figure 2-13.
13. Repeat step 12 for M8926-J2 to cable card M8913, and M8926-J3 to cable card M9001-YA.
14. If this is a two-drive system, install H8800 terminators in the output jacks of M9001, M8913 and M9001-YA. If the system contains more than two drives, install BC06R cables in daisy-chain fashion from one drive to the other observing the colored stripe and smooth side/rough side orientation shown in Figure 2-13. Install H8800 terminators in the M9001, M8913 and M9001-YA output jacks of the last drive in the chain.
15. Plug the 861 power cord into a power receptacle.
16. Set the 861 circuit breaker to the ON position.
17. Slide the TU10W transport(s) back into the cabinet.

2.7 Acceptance Testing

Refer to Acceptance Procedure, Engineering Drawing Nos. A-SP-TU16-0-8 and A-SP-TU10W-0-3 for the acceptance test procedures for the TMB11/TU10W tape drive system.



TU10W System Unit Module Location, Viewed from Backplane

FIG. 2-14

CHAPTER 3

SYSTEM OPERATING INSTRUCTIONS

3.1 Controls and Indicators

The operator control box (Figure 3-1) is located at the left of the file reel. The functions of the control box switches and indicators are listed in Tables 3-1 and 3-2.

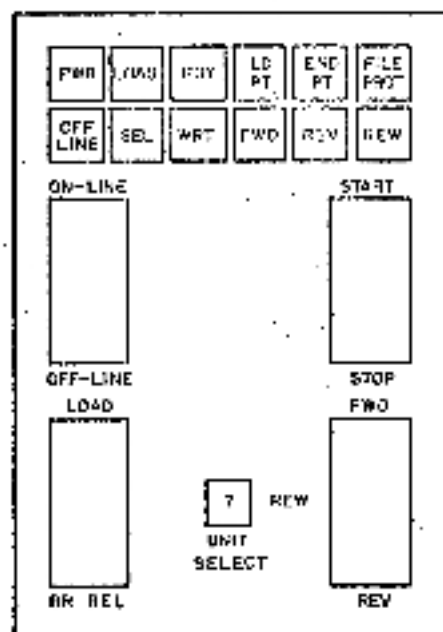
3.2 Operating Procedures

3.2.1 Application of Power

1. If the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch is in the REMOTE ON position, TU10W power is controlled by the processor POWER key switch. This method is used in normal operation.
2. If the processor POWER key switch is not activated, TU10W power may be turned on locally by setting the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON. This method may be used during maintenance.

3.2.2 Loading and Threading Tape--Use the following procedure to mount and thread magnetic tape.

1. Apply power to the transport. Place LOAD/BR REL switch to center position.
2. Place a write enable ring in the tape reel groove if data is to be written on the tape. Ensure that there is no ring in the groove if data on the tape is not to be erased or written over.



10-1747

3-1

Figure 3-1 Operator Control Box

3. Mount the file reel onto the lower hub, with the groove facing toward the back (away from the operator). Ensure that the reel is firmly seated against the flange of the hub and that the reel hub is securely tightened by hand. To tighten the reel hub, turn it clockwise. Do not grip reel by outer flanges. Ensure that brakes are on while tightening the hub.

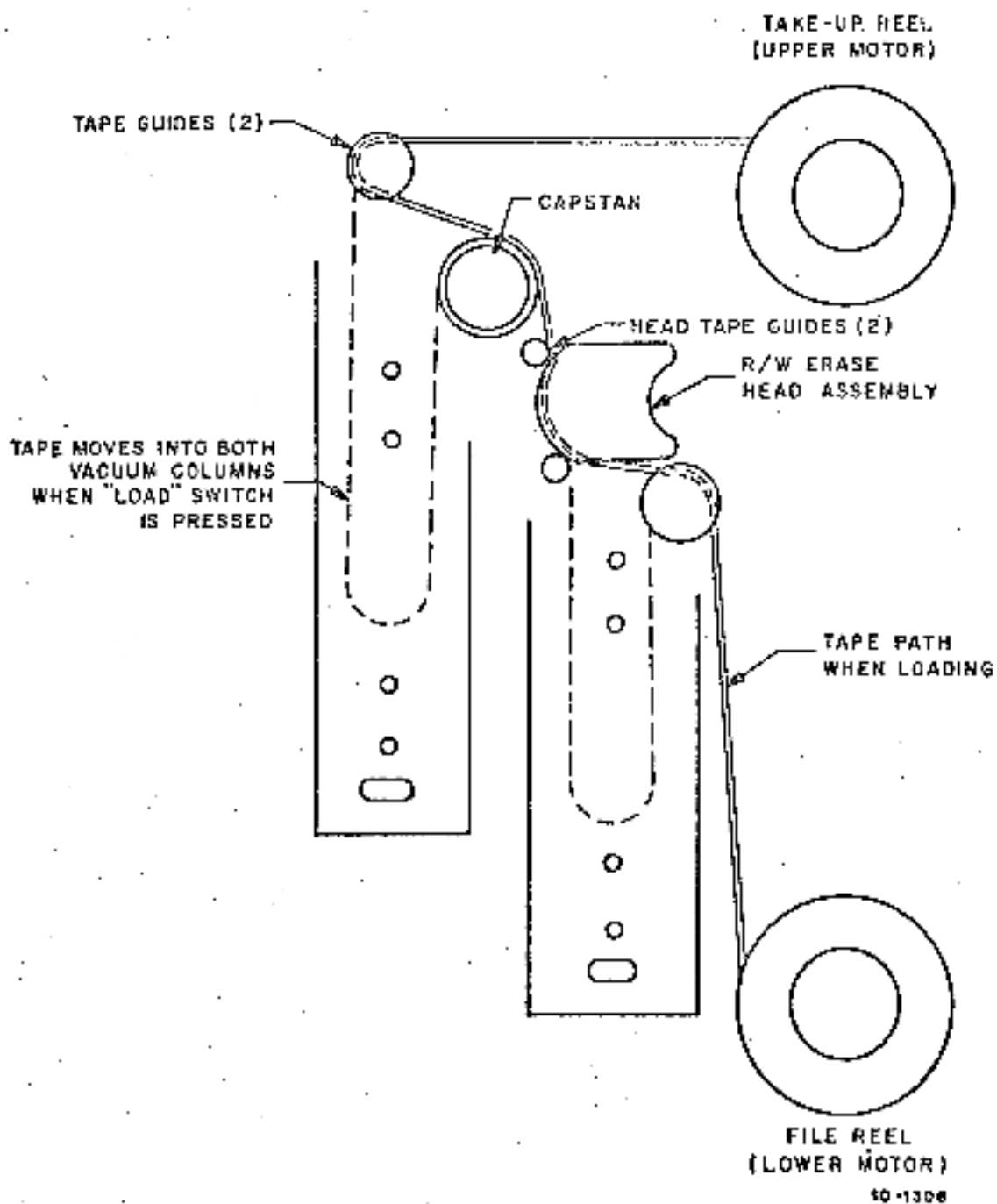
Table 3-1 TU10W Control Box Switches

Switch	Function
LOAD/BR REL LOAD position	Enables vacuum motor, which draws tape into the buffer columns.
Center position	Disables vacuum motor; brakes are full on.
BR REL position	Releases brakes.
ON-LINE/OFF-LINE ON-LINE position	Selects remote operation.
OFF-LINE position	Selects local operation.
FWD/REW/REV FWD position	Selects, but does not initiate, forward tape motion when transport is off-line.
REW position	Selects, but does not initiate, tape rewind when transport is off-line.
REV position	Selects, but does not initiate, reverse tape motion when transport is off-line.
START/STOP START position	Initiates tape motion selected by FWD/REW/REV switch when transport is off-line.
STOP position	Clears any motion commands when transport is off-line.
UNIT SELECT (plug activated)	Selects the tape transport unit by number (0-7); this number is used in the program to address the tape transport (slave address).

Table 3-2
Status Indicators

Indicator	Function
PWR	Indicates power has been applied to the transport.
LOAD	Indicates the vacuum is on and the tape is loaded into the buffer columns.
RDY	Indicates that the tape transport is ready (vacuum on and settle-down delay complete); no tape motion.
LD PT	Indicates that the tape is at load point (beginning of tape--ROT).
END PT	Indicates that the tape is at end point (end of tape --ROT).
FILE PROT	Indicates that write operations are inhibited because the write enable ring is not mounted on the file reel.
CFF-LINE	Indicates local operation by the control box.
SEL	Indicates the tape transport is selected by the controller (program).
WRT	Indicates that a write operation has been initiated.
FWD	Indicates that a forward command has been issued.
REV	Indicates that a reverse command has been issued.
REW	Indicates that a rewind command has been issued.

4. Install the take-up reel (at the top) using the same procedure used in step 3.
5. Place the LOAD/BR REL switch in the BR REL position.
6. Manually unwind tape from the file reel and thread the tape by the tape guides and head assembly as shown in Figure 3-2.
7. Wind about four turns of tape onto the take-up reel. Ensure that the tape is in the guides.



3-2
Figure 3-2 Tape Loading Path

8. Place the LOAD/BR REL switch to the LOAD position to draw tape into the vacuum columns.
9. Select FWD and press START to advance the tape to the load point. When the BOT marker is sensed, tape motion stops, the FWD indicator goes out, and the LD PT indicator comes on.

NOTE

If tape motion continues for more than 10 sec, it is possible that originally too much tape was wound by hand onto the take-up reel, passing the BOT marker. If this happens, press STOP, select REV (reverse), and press START. The tape should move to the BOT marker (load point) and stop.

3.2.3 Unloading Tape--Different procedures are used to unload tapes, depending on whether or not the tape is at BOT.

Unloading Tape at BOT--To unload a tape which is at the BOT marker, perform the following procedure:

1. Place the LOAD/BR REL switch in the BR REL position to release the brakes.
2. Gently hand wind the file reel (lower) in a counterclockwise direction until all of the tape is wound onto the reel.

CAUTION

When winding the tape by hand, do not jerk the reel. This can stretch or compress the tape, which could cause irreparable damage.

3. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.

Unloading Tape Not At BOT--To unload a tape which is not at the BOT marker, perform the following procedure:

1. Place the ON-LINE/OFF-LINE switch in the OFF-LINE position.

2. Press STOP; select REW.
3. Press START. The tape should rewind until the BOT marker is reached.
4. Place the LOAD/BR REL switch in the BR REL position to release the brakes.
5. Gently hand wind the file (lower) reel in a counterclockwise direction until all of the tape is wound onto the reel.

CAUTION

When winding the tape by hand, do not jerk the reel. This can stretch or compress the tape, which could cause irreparable damage.

6. Remove the file reel from the hub assembly. Turn the hub counterclockwise to loosen it.
- 3.2.4 Restart After Power Failure--In the event of a power failure, the TU10W automatically shuts down and tape motion stops without physical damage to the tape. However, if the TU10W was on-line and was either reading or writing at the time of the power failure, the last record was probably lost; refer to system recovery procedures documentation if this happens. To restart the transport, proceed as follows:

NOTE

Return of power is indicated when the PWR indicator lights.

1. set the ON-LINE/OFF-LINE switch to OFF-LINE.
2. Place the LOAD/BR REL switch in the BR REL position to release the brakes.
3. Manually wind the reels to take up any slack in the tape.

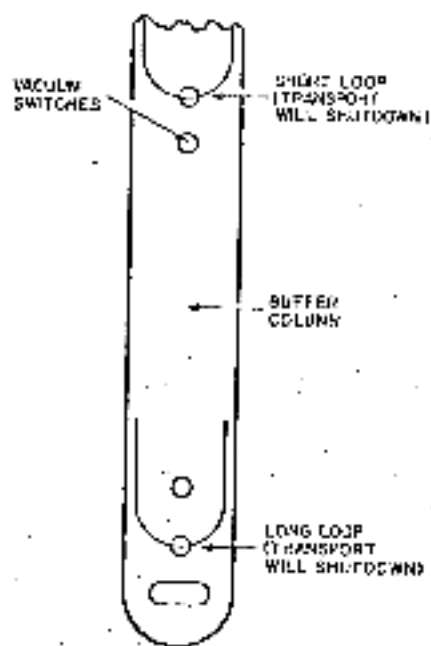
4. Set the LOAD/SR REL switch to the LOAD position to draw tape back into vacuum columns.
5. Set the ON-LINE/OFF-LINE switch to the desired position.

3.2.5 Restart After Fail-Safe--If the tape loop in either buffer column exceeds the limit shown in Figure 3-3, the vacuum system automatically shuts down and tape motion stops without damage to the tape. When this fail-safe condition occurs, the TV10W does not respond to either on-line or off-line commands. To restart the transport, refer to Paragraph 3.2.4.

3.3 Operator Troubleshooting

Before any maintenance personnel are called to correct a problem, the operator can make several checks with minimal effort. These precautions may isolate an easily correctable error:

1. Ensure that the vacuum door (Figure 1-4) is closed and sealed properly.
2. If the tape does not stop at BOT, be certain the tape has a BOT marker.
3. Ensure that the write enable ring is inserted in the tape reel if a write operation is to be performed.
4. Clean the tape path according to the daily (8-hour) preventive maintenance procedures in Chapter 4.



3-3
 Figure 3-3 Fail-Safe Limits

10-1250

4.1 CUSTOMER RESPONSIBILITIES

The customer is directly responsible for:

1. Obtaining operating supplies, including disk cartridges, disk packs and filters, magnetic tape, DECTape, paper tape, cassettes, printer paper, printer ribbons, plotter paper, etc.
2. Supplying accessories, including disk storage racks, DECTape storage racks, carrying cases for disk cartridges and DECTape, cabinetry, tables, and chairs.

NOTE

Users of Digital Equipment Corporation equipment may obtain the proper operating supplies and accessories by contacting:

Digital Equipment Corporation
DEC Supplies Order Processing
146 Main Street
Maynard, Massachusetts 01754
Phone: (617)897-5111, Ext. 5218, 5907
Boston Area: (617)890-0330
TWX: 710-347-0212
Cable: Digital Mayn
Telex: 94-8457

3. Maintaining the required logs and report files consistently and accurately.

4. Making the necessary documentation available in a location convenient to the system.
5. Keeping the exterior of the system and the surrounding area clean.
6. Turning off the teletypewriter and/or line printer when these devices are not in use.
7. Ensuring that ac plugs are securely plugged in each time equipment is used.
8. Performing the specific equipment care operations described in Paragraphs 4.2 and 6.3 at the suggested frequencies or more often if usage and environment warrant.

4.2 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; it is imperative that the tape be kept clean.
2. Always store tape reels inside containers when not in use; keep the empty containers tightly closed to keep out dust and dirt.
3. Never touch the portion of tape between the BOT and EOT markers; oil from fingers attracts dust and dirt.
4. Never use a contaminated reel of tape; this will spread dirt to clean tape reels and could have an adverse affect on tape transport reliability.
5. Always handle tape reels by the hub hole; squeezing the reel flanges could lead to tape edge damage in winding or unwinding tapes.
6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.
7. Do not place magnetic tape near any line printer or other device that produces paper dust.

8. Do not place magnetic tape on top of the tape transport, or in any other location where it might be affected by hot air.

4.3 CUSTOMER PREVENTIVE MAINTENANCE OF T1100 TAPE TRANSPORT

4.3.1 General

Digital Equipment Corporation tape transports are highly reliable precision instruments that will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The following information will assist the customer in caring for his equipment and ensure the highest level of performance and reliability.

4.3.2 Preventive Maintenance

To ensure trouble-free operation, a preventive maintenance schedule should be kept. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport. Therefore, a rigid schedule applying to all machines is difficult to define. Daily cleaning is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Paragraph 4.3.4 contains the cleaning instructions.

Before performing any cleaning operation, remove the supply reel and store it properly. All items in the tape path should be cleaned on a daily basis. In cleaning, it is important to be thorough yet gentle and to avoid certain dangerous practices. It should be remembered that the tape cleaner is a strong cleaning agent and should not come in contact with painted surfaces or plastic.

CAUTION

Do not use acetone or lacquer thinner, rubbing alcohol, or excessive cleaner. Be extremely careful not to allow the cleaner to penetrate ball bearings, tension rollers, and motors.

4.3.3 MAGNETIC TAPE DRIVE CLEANING KIT

A magnetic tape drive cleaning kit has been carefully configured to provide cleaning materials that will not harm tape equipment and will not leave any residue behind to interfere with data reliability. The hints contained in the following few paragraphs will ensure that the very best results possible will be obtained from the kit.

The FREON #TF113 cleaning fluid in this kit is one of the safest and best degreasing agents available. It will not adversely affect any part of DIGITAL's tape equipment. To ready the can of fluid for service, unscrew the top and punch a small hole in the metal seal covering the pour spout.

WARNING

TF113 is a non-restricted, non-hazardous substance. However, when using TF113, avoid excessive skin contact, do not allow TF113 to come in contact with the eyes, and do not swallow it. Use TF113 only in a well-ventilated area.

When cleaning tape equipment, never dip a contaminated cleaning swab or wipe into the can. To transfer fluid onto the swab, pour a little out into the screw cap and dip the swab into the cap. Discard the remaining fluid when the cleaning operation is complete.

*Registered trade mark, Dow Chemical Co.

Always keep the can of fluid tightly closed when not in use, because FREON TF113 evaporates rapidly when exposed to air.

Use the cleaning materials contained in the kit to clean tape heads, guides, reels and any part of the drive where a dirty residue could ultimately come in contact with tape. To clean other parts of the drive, such as the exterior surfaces of doors or the friction pads of brakes, use any reasonably clean, lint-free material with or without cleaning fluid.

NOTE

Should you encounter an unusually stubborn dirt deposit that appears to resist TF113, try a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with TF113 to remove soapy residues.

4.3.4 Cleaning the TU1GW DECmagtape Drive

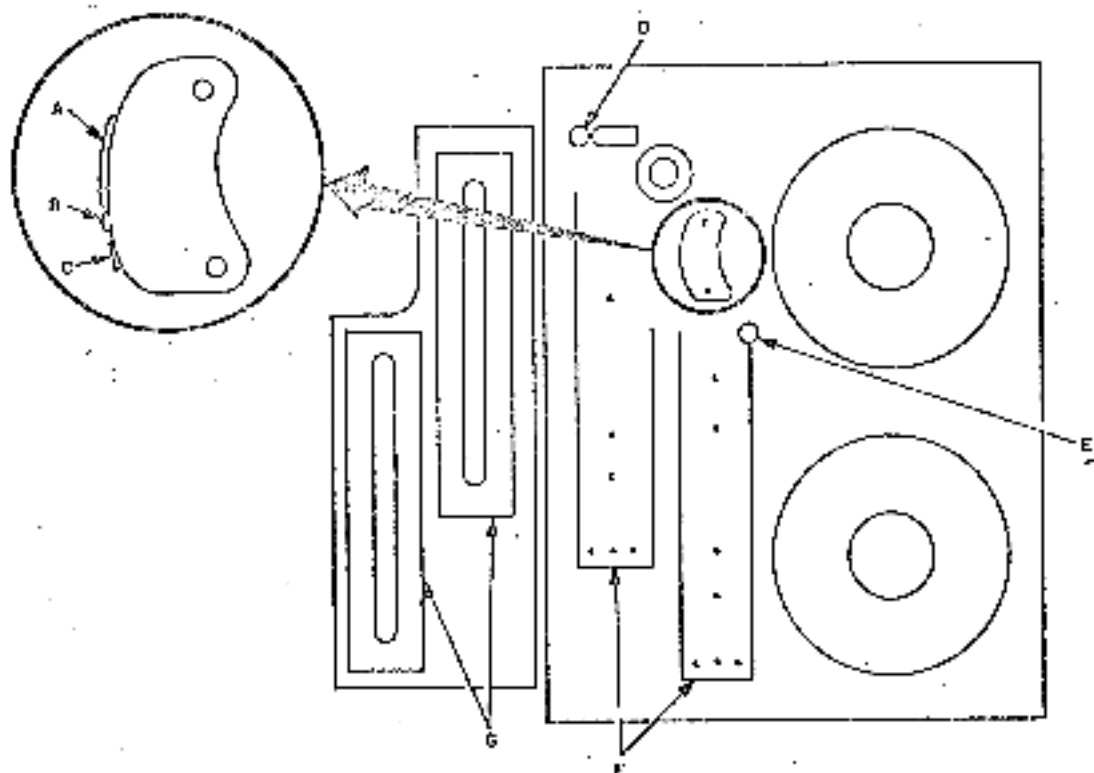
1. Dismount the tape from the unit.
2. Clean the following components of the drive using a foam-tipped swab soaked in cleaning fluid (Figure 4-1).
 - a. Read/write head (Location A)
 - b. Erase head (Location B)
 - c. Tape cleaner (Location C)
 - d. Upper roller guide (Location D)
 - e. Lower roller guide (Location E)

NOTE

Be careful to keep cleaning fluid only on the tape-bearing surface of roller guides to prevent degreasing the roller guide bearings.

3. When cleaning the head area, avoid the spring-loaded ceramic washers on the tape drive assemblies. If it appears necessary to rub the swab over the tape bearing surface of these guides to remove oxide deposits, do so; however, when cleaning is completed, be sure that the washer is pressed snugly up against the tape guide surface and not "hung up" on its shaft (Figure 4-2).

4. Next, clean the vacuum pockets (F) and the inner surface of the vacuum door (G) using a lint-free wipe and cleaning fluid. Pass another lint-free wipe over the head using a polishing action to remove any remaining deposits.



11-3357

Figure 4-1 Location of Read/Write and Erase Heads and Tape Cleaner

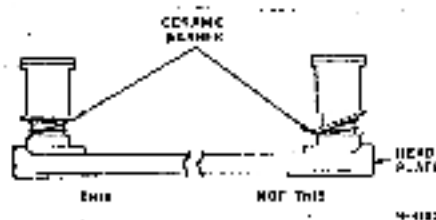


Figure 4-2 Proper Ceramic Washer Positioning

CHAPTER 5

SYSTEM MAINTENANCE

5.1 SCOPE

This chapter provides a complete description of TMB11/TU10W preventive and corrective maintenance procedures.

5.2 TMB11/TU10W MAINTENANCE PHILOSOPHY

The TMB11/TU10W DECmagtape System is highly reliable and will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

The preventive maintenance required on the TMB11 differs from that required on the TU10W transport. The TMB11 controller and the M8926 interface are total solid-state units with no moving parts; therefore, no preventive maintenance is required on these units. The TU10W transport, however, requires daily customer care consisting of head and tape path cleaning (Chapter 4). Otherwise, the transport requires very few adjustments and these should not be performed unless problems are encountered in transport operation. See Paragraph 5.4 for the recommended preventive maintenance procedures.

Corrective maintenance consists of troubleshooting at the system level using system diagnostics and visual observations to localize the failure to a particular unit, whether it be the TMB11 Controller, the M8926 Interface or TU10W transport. Once the faulty unit is identified, unit level troubleshooting can be performed using unit functional block diagrams, engineering flow diagrams, timing diagrams and detail logic diagrams to localize the failure to an electrical module or mechanical part.

Once the faulty module or mechanical part is located, it should be replaced. If the faulty part is a module, it should be returned to the depot for repair; if a mechanical part fails, it should be repaired only if the cost warrants it.

5.3 TEST EQUIPMENT

Test equipment required to maintain the TMB11/TU10W falls into two categories: standard test equipment and special test equipment.

5.3.1 Standard Test Equipment

Maintenance procedures for the TMB11/TU10W require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes.

Table 5-1 Standard Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplet or Simpson	Model 630XA or 260
Oscilloscope	Tektronix	Type 453 or equivalent
X10 Probes (2)	Tektronix	P6008
Diagnostics (MAINDECS)	DIGITAL	MAINDEC-11-D2TMA-*
		MAINDEC-11-D2TMR-*
		MAINDEC-11-D2TME-*
		MAINDEC-11-D2TMF-*
		MAINDEC-11-D2TMG-*

*Revision level

5.3.2 Special Test Equipment

The special test equipment and tools required are listed in Table 5-2. Usage of the special tools and equipment is also given.

Table 5-2

Special Tools and Equipment and Their Use

Item	Part No.	Usage*				
		1	2	3	4	5
1. Skew Tape (800BPI) 1200 ft. or 600 ft.	29-19224	X				X
	29-22020	X				X
2. Reel Hub Tool	29-18611					X
3. Roller Guide Tool	29-18607					X
4. Microscope	29-20273				X	X
5. Magna-see	29-16971				X	X
6. Penlight		X	X	X	X	X
7. Alignment Glass	74-13909					X
8. Depth Micrometer	29-22039					X
9. Shimstock .001 .002 (red) .003 (green) .004 (tan) .005 (blue) .0075 (transparent) .010 (brown)	48-50023-01					X
	48-50023-03					X
	48-50023-04					X
	48-50023-05					X
	48-50023-06					X
	48-50023-07					X
	48-50023-08					X
10. TMB11/TM10W Module Swap Kit		X				
11. Feeler Gauge Set		X		X	X	X
12. Allen Wrench Set		X		X	X	X
13. EOT/BOT Markers (Reflective Strips)					X	X
14. Ground Isolation Plug (Scope Float)		X		X	X	X
15. Vacuum Belt Tension Gauge		X				

*Usage Legend

1. Routine Corrective Maintenance
2. Monthly P.M.
3. Quarterly P.M.
4. Semi-Annual P.M.
5. Major Tape Path Alignment

5.4 Preventive Maintenance

The TMS11 controller and M8926 interface module are all-electronic assemblies requiring no preventive maintenance. Care and preventive maintenance of the TU10W to be performed by the user is given in Chapter 4. TU10W preventive maintenance to be performed by the service technician is contained in Chapter 5 of the TU16/TM02 tape drive system maintenance manual; document No. EK-TU16-MX-002.

5.5 Adjustments

The TMS11 controller and M8926 interface module contain no adjustments. TU10W adjustments and alignment procedures are contained in Chapter 4 of the TU16/TM02 tape drive system maintenance manual; document No. EK-TU16-MX-002.

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance information is provided to guide and aid the maintenance technician when isolating and repairing faults. The information consists of five troubleshooting aids: the TMB11/TU10W diagnostics, the corrective action flow diagram, the functional block diagram, TMB11 troubleshooting, and TU10W Troubleshooting.

5.6.1 TMB11/TU10W Diagnostics

Diagnostics, consisting of a paper tape and documentation, are provided with each system. The documentation includes instructions on loading, running, and interpreting diagnostic printouts. The diagnostics provided with the TMB11/TU10W are listed and described in Table 5-3. Appendix B contains the diagnostic documentation less the program listings.

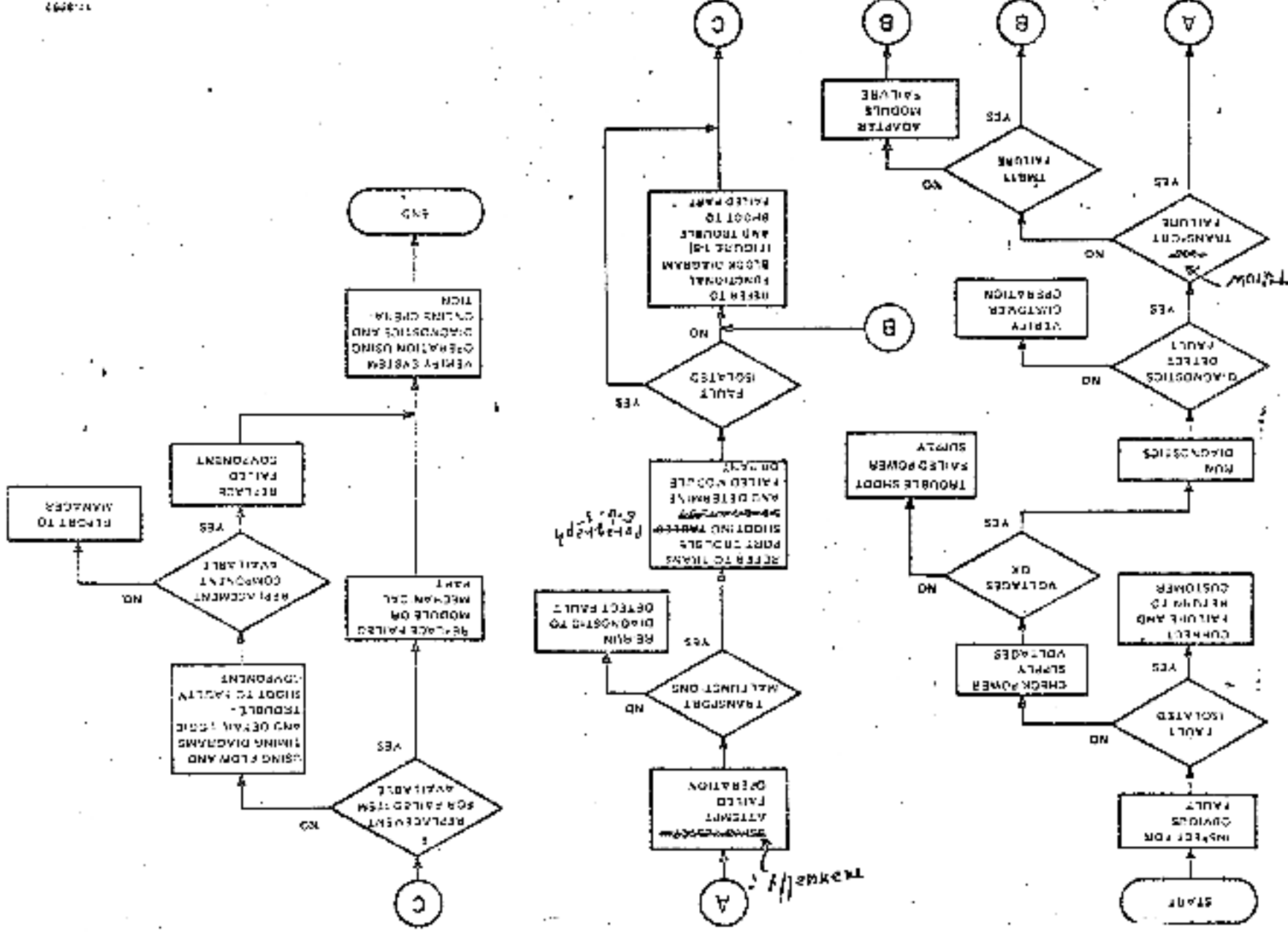
Table 5-3 Diagnostic Descriptions

Number: MAINDEC-11-	Title	Description
DZTMA	TMA-11 Instruction Test	A series of basic tests that checks TMB11 registers for proper operation.
DZTMH	TMA-11 Multidrive Data Reliability Exerciser	Tests all TMB11/TU10W function for evaluation and debugging.
DZTME	TU10W Drive Function Timer	Selected TMB11/TU10W operations are executed, timed, and the times are then printed.
DZTMP	TU10W Supplemental Instruction Test	Four tests that check special data transfers of the TMB11/TU10W.
DZTMG	TU10W Utility Driver	Executes designated operation regardless of errors or result.

5.6.2 Corrective Action Flow Diagram

Figure 5-1 provides sequential procedures for troubleshooting the TMB11/TU10W.

Figure 5-1 TMB11/TR10M Corrective Action Flow Diagram



5.6.3 Functional Block Diagram

Figure 1-6 functionally separates the circuitry comprising the three major units (TMB11, M8926, TU15W) into functional blocks and depicts signal flow between these blocks within each unit; it also depicts interfacing between each unit and interfacing between the TMB11 and the Unibus. The functional block diagram can be used in conjunction with Figure 5-1 for troubleshooting and maintenance.

5.6.4 TMB11 Controller Troubleshooting

The diagnostics listed in Table 5-3 will test and troubleshoot all functions of the TMB11 Controller. By using the diagnostics and the functional block diagram (Figure 1-6), troubles within the controller can be isolated and repaired.

5.6.5 TU15W Transport Troubleshooting

Table 5-4 suggests possible causes when problems are encountered with the TU15W transport. More specific and more detailed troubleshooting procedures are found in Chapter 3 of the TU16/TM02 tape drive system maintenance manual, document No. EX-TU16-MM-002.

5.7 PARTS REPLACEMENT

In most instances, assembly methods for parts replacement are obvious. Electronic parts are nearly all on plug-in modules. Items in the transport tape path may require machine realignment if replaced. If only one item in the transport tape path is replaced at a time, the complete alignment procedure may usually be avoided. Refer to the Removal and Replacement procedures in Chapter 4 of the TU16/TM02 tape drive system maintenance manual, document No. EX-TU16-MM-002.

Table 5-4 TU10W DECmagtape Transport Troubleshooting Hints

Problem	Hints
General	<p>Problems in the TU10W transport can usually be classified as either mechanical or electrical but often the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case the problem should be thoroughly analyzed before adjustments are made.</p> <p>Electronic troubleshooting is greatly facilitated by the modular construction--a new card may be substituted and the effect observed. Most difficult, of course are subtle problems and those of an intermittent nature.</p> <p>Visualizing solution (Magna-See) is useful under certain conditions for troubleshooting. At high densities the data cannot be satisfactorily resolved but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use.</p> <p>If a tape has had visualizing solution applied to it, <u>do not</u> reuse that portion of the tape as it will contaminate the head. Cut the visualized portion off and discard.</p> <p>To use visualizing solution, shake the can thoroughly, remove top, and pass portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using Scotch</p>

tape and applied to a sheet of paper for a permanent record.

High Error
Rate

Usually the more difficult problems involve a higher than permissible error rate for which there is no obvious reason. If operating properly with good tape, the transport should make very few errors in writing and, if rewriting is included in the program, it should make no read errors.

Useful clues are:

1. In what mode (read or write) are many errors occurring?
2. At what point in the block does the error occur?
3. What is the nature of the errors: vertical parity, CRC, LMC?
4. Are the error patterns related?
5. Do errors occur only on certain sets of commands?

The first thing to be done is to inspect the head and other items in the tape path for dirt accumulations.

Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check interface connections for broken wires or bad contacts.

Table 5-4 TU10W DECmagtape Transport Troubleshooting Hints (Cont)

Problem	Hints
Compatibility	<p>The TU10W transport accepts and produces tapes conforming to ANSI standards. Occasionally compatibility problems can arise:</p> <ol style="list-style-type: none"> 1. Tapes written by and acceptable to the TU10W transport are not acceptable to another transport. 2. Foreign tapes cannot be read by the TU10W transport but its own tapes can be read satisfactorily. <p>Four items may be involved: skew, speed, ramp times, and tape path alignment. These should be checked as described in the adjustment procedures.</p>

CHAPTER 6 TMB11 THEORY OF OPERATION

6.1 INTRODUCTION

The TMB11 Controller has three main functions: handling data transfers, issuing control commands, and monitoring operation of the system.

During data transfer functions, the controller assembles the data word from the magnetic tape and places it on the bus (read operation) or assembles it from the bus and loads it into the tape transport read/write heads (write operation) for recording on magnetic tape. The commands necessary to perform the specified operation are generated by the controller under program control.

Normal data word transfers are performed by direct memory access transactions at the NPR level. If the controller is ready to begin a new function or if an error condition exists, it issues an interrupt request so that it can be serviced by the program.

In addition to the commands required for data transfers, the controller may issue other commands governing tape unit selection, direction of tape travel, rewind, space forward, space reverse, write end-of-file mark, etc. The controller also monitors various functions and provides an indication of error conditions. The status of the monitored functions is stored in the status register.

6.2 GENERAL OPERATION

The prime function of the TMB11 Controller is to control transfers of information so that digital data can either be taken from the bus and recorded on magnetic tape (write operation) or read from the magnetic tape and transferred to the bus for use by another device such as memory (read operation). In addition, the controller performs tape transport selection, tape positioning, tape formatting, and system monitoring functions.

The controller contains a command register, which allows the program to specify desired operations by loading control data (transport selection, packing density, function, etc.) into the register. System status information (end-of-tape, errors, tape unit ready, etc.) is loaded into a status register, which can be read from the bus.

Data transfers are controlled by a byte record counter (MTBRC) and a current memory address register (MTCMA). The program loads the byte record counter with the 2's complement of the desired number of data transfers. The counter is incremented before each transfer; therefore, the byte transfer that causes the byte count overflow (MTBRC becomes zero) is the last transfer to take place. The byte counter is also used to count the number of records during space forward and space reverse operations.

The current memory address register is also incremented before each transfer and, therefore, always points to the next higher address than the one most recently accessed. Thus, when the entire record is transferred, the register contains the address plus 1 of the last character in the record. For certain error conditions, the register contains the address of the location in which the failure occurred.

6.2.1 Read

During read operations, the controller assembles bytes from successive characters read from the tape channels. When reading a 7-channel tape, the 6 data bits are assembled in a data buffer register for temporary storage. The parity bit is read but not loaded into memory. Because the PDP-11 uses 3-bit bytes, the remaining 2 bits in the buffer are forced to 0. When the byte is assembled, it is placed on the bus for transfer to memory. If an NPR transfer is used, bytes from the data buffer are alternately stored into the low and high byte portions of memory.

When reading 9-channel tape, operation is identical except that 8 data bits are assembled. It is not necessary to force any bits to 0, because the 8 data bits constitute a complete PDP-11 byte. In the case of both 7-channel and 9-channel tapes, the parity bit can be loaded into the data buffer but is not loaded into memory.

When reading 9-channel tapes, either the CRC character or the LRC character at the end of a record is stored in the data buffer, depending on the state of bit 14 in the MTRD. If this bit is 0, the CRC character is loaded into the data buffer and can be used for error detection. If the bit is 1, then the data buffer contains the LRC character at the end of the record. When reading a 7-channel tape, bit 14 in the MTRD operates in a similar manner. If bit 14 is set, the LRC character is present, and when bit 14 is cleared, the last data character is present in the data buffer.

6.2.2 Write

During write operations, the controller disassembles 8-bit bytes from the bus and distributes the bits so that they can be recorded on successive frames of the tape. The controller selects one of three recording densities (200, 556, or 800 hpi) for 7-channel tapes. All 9-channel tapes are written at a density of 800 hpi. There are three possible write functions: write, write-with-extended-IRG, and write end-of-file (EOF) mark.

When a write function is selected, the program loads the byte record counter with the 2's complement of the number of bytes to be written in the record. Although the parity bit is generated by the master tape transport, the polarity of the bit is determined by the controller so that either odd or even parity can be selected. When the buffer is loaded, the controller transmits the byte to the master tape transport, which places the byte on the read/write heads of the selected slave transport so that data can be written on the magnetic tape.

The write-with-extended-IRG function is identical to the write function except that a 3-in. gap, rather than the normal gap is used between records. When this function is selected, a 3-in. segment of tape is erased before writing begins.

The write end-of-file (EOF) function is used to indicate that a block of records is complete. When this function is selected, a special EOF character is written on the tape followed by an LRC character. In 7-channel mode the EOF and LRC characters are octal 17. In 9-channel mode the EOF character (and the LRC character) are octal 23. These two characters constitute a complete record. This command causes a 3-in. gap to be placed before the EOF mark. The XIRG command must be absent to have this gap written.

6.2.3 System Monitoring

System monitoring functions are performed by the controller status register. The 16 bits in this register retain error and tape status information. Some status data is combined, such as lateral and longitudinal parity errors, or has a combined meaning, such as illegal command, for optimum use of the available bits. The status register only monitors the tape transport selected by the command register; therefore, other units that may be rewinding do not interrupt the system when ready for data.

6.2.4 Interrupts

The TMBII Controller uses NPR or BR interrupts to gain control of the bus in order to perform data transfers or to cause a vectored interrupt, thereby causing a branch to a handling routine. The NPR requests are used for direct memory access whenever it is desired to transfer data between memory and the data buffer register without processor intervention. The BR requests are made when processor servicing is required for completed operations or error conditions.

6.2.4.1 NPR Requests - The controller issues an NPR request whenever it is necessary to transfer data between memory and the data buffer register. During a read operation, the direction of transfer is from the data buffer to the core memory. The RDS pulse (read strobe, from master tape transport to controller), which is used to strobe data from the tape transport into the data buffer register, generates the NPR request. When the request is granted, the controller performs a DATOB bus cycle and transfers information from the data buffer into memory.

During a write (or write-with-extended-IRG) operation, the NPR request is generated by the write strobe (WRS) pulse from the transport. When the request is granted, the controller performs a DATI bus cycle and transfers a byte from core memory into the data buffer register.

During both read and write operations, the address in memory that data is read from or loaded into is determined by the value in the current memory address register (MTCMA).

6.2.4.2 BR Requests - A BR interrupt can occur only if the interrupt enable (INT ENB) bit in the command register is set. With INT ENB set, setting the CU RDY bit in the command register, or completing a rewind operation initiates an interrupt request.

When CU RDY is set, it indicates that the controller is ready to perform another command.

When ERR is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause the program to branch to an error handling routine.

If a function command is issued with the GO bit cleared and INT ENB set, an interrupt is initiated.

If the selected tape unit (as indicated by the SEL bits in the command register) completes the rewind operation before a new command to that unit is received and INT ENB is set, an interrupt is initiated.

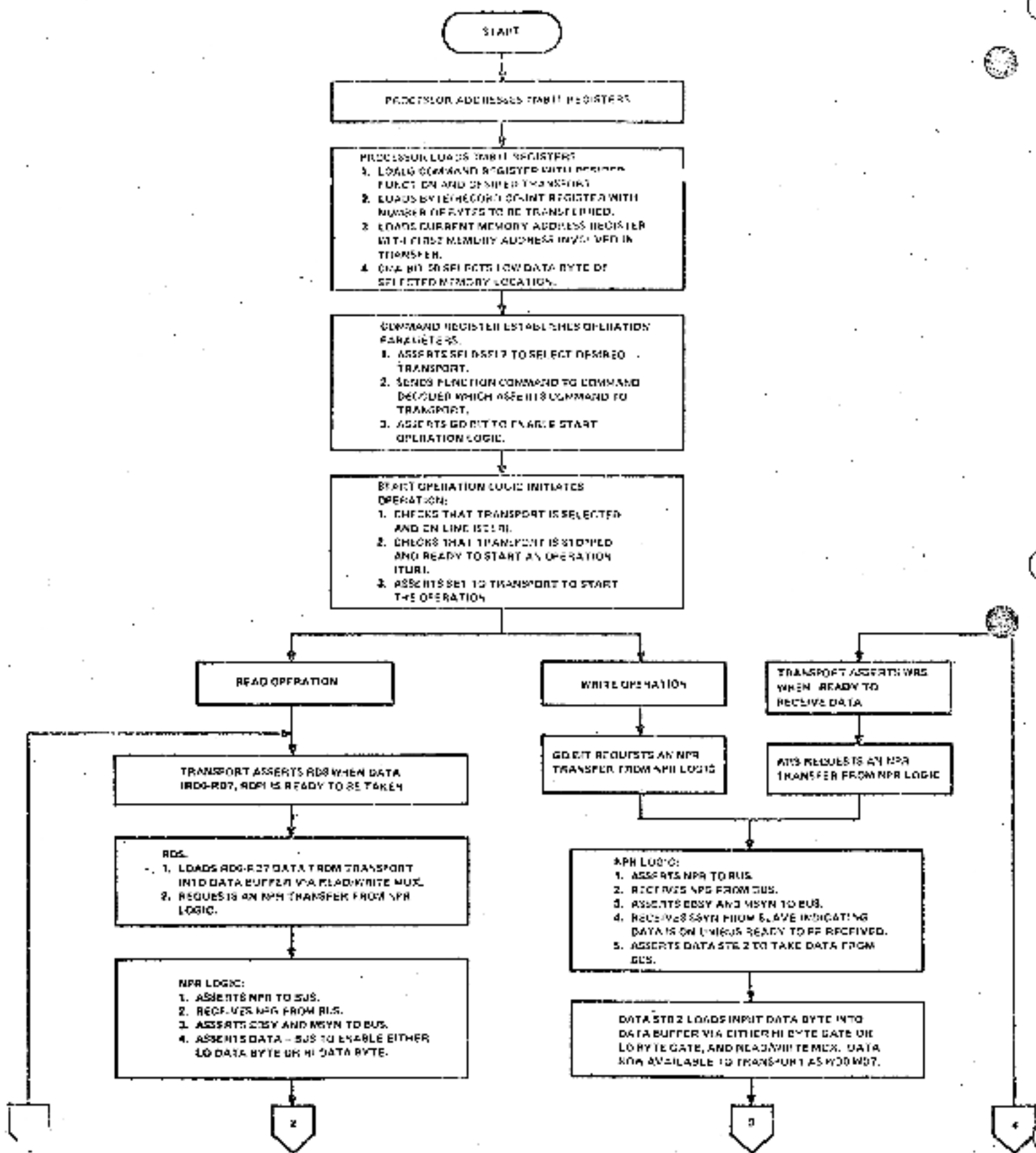
If the interrupt is enabled (INT ENB set) and selection of the tape unit is not changed (as indicated by the SEL bits), then a rewind command causes two interrupts: an interrupt when the rewind function begins and an interrupt when the tape unit completes the rewind function. If, however, the tape unit is already at the BOT marker when rewind is issued, only one interrupt occurs.

6.3 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

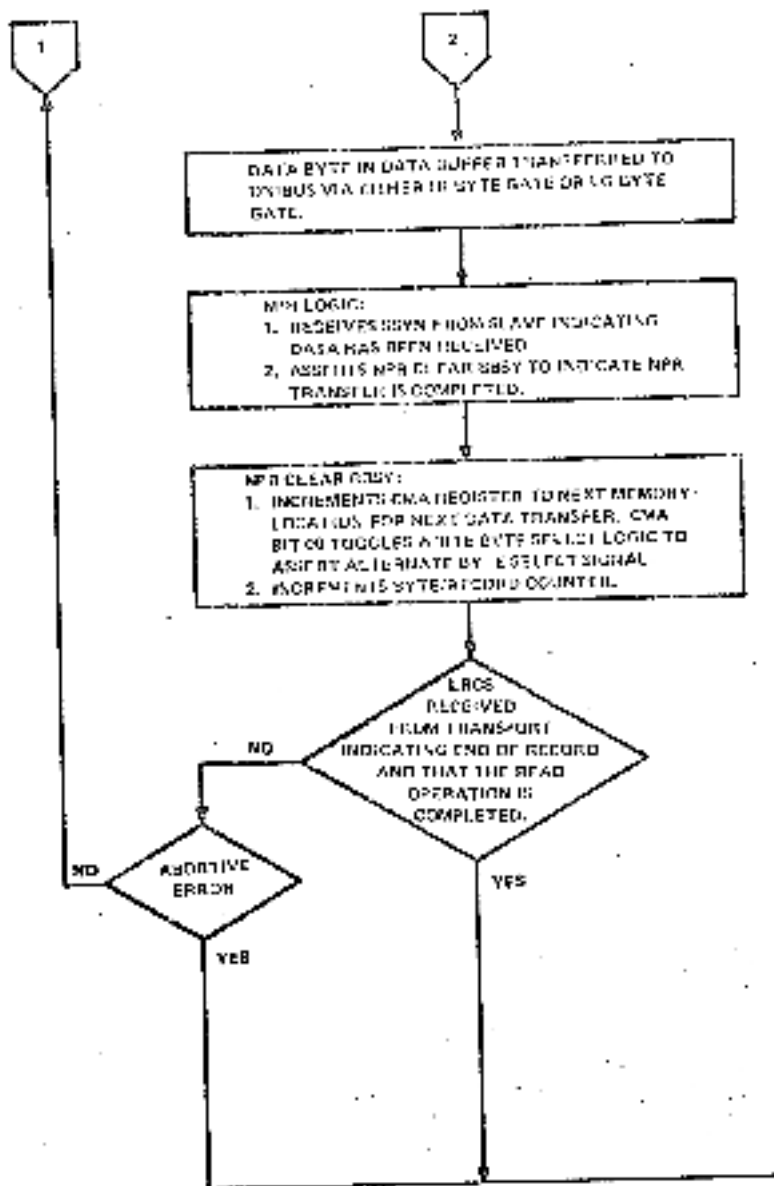
The TMBII flow diagram (Figure 6-1) provides a brief functional description of the controller. This diagram should be read in its entirety while referencing the controller functional block diagram, Figure 6-2.

6.4 TMBII REGISTERS

All software control of the magtape system is performed by means of six device registers within the controller. These registers have been assigned bus addresses and can be read or loaded using any PDP-11 instruction that refers to their address. The six device registers are listed in Table 6-1. The register addresses are determined by jumpers on the M105 address selector module. Any programs that refer to these addresses must be modified accordingly if the jumpers are changed.



TIB11 Flow Diagram (Sheet 1 of 2)



LRCs STORED OR AND LOGIC ASSERTING DO LOGIC.

BUS INTERRUPT L
 1. ASSERTS BUS E
 2. RECEIVES BUS
 3. ASSERTS SBY
 4. ASSERTS VECT INTERVENTION

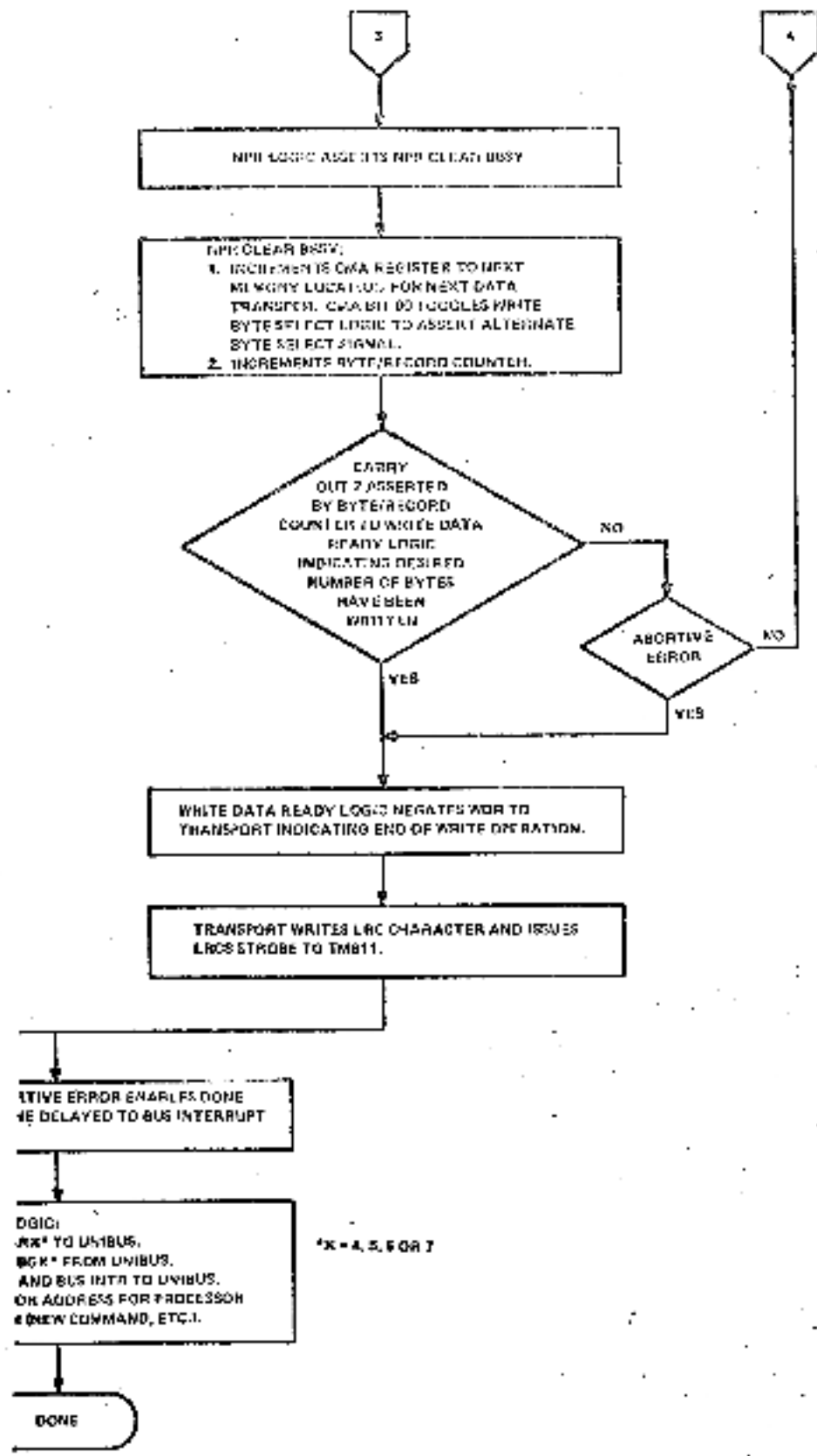
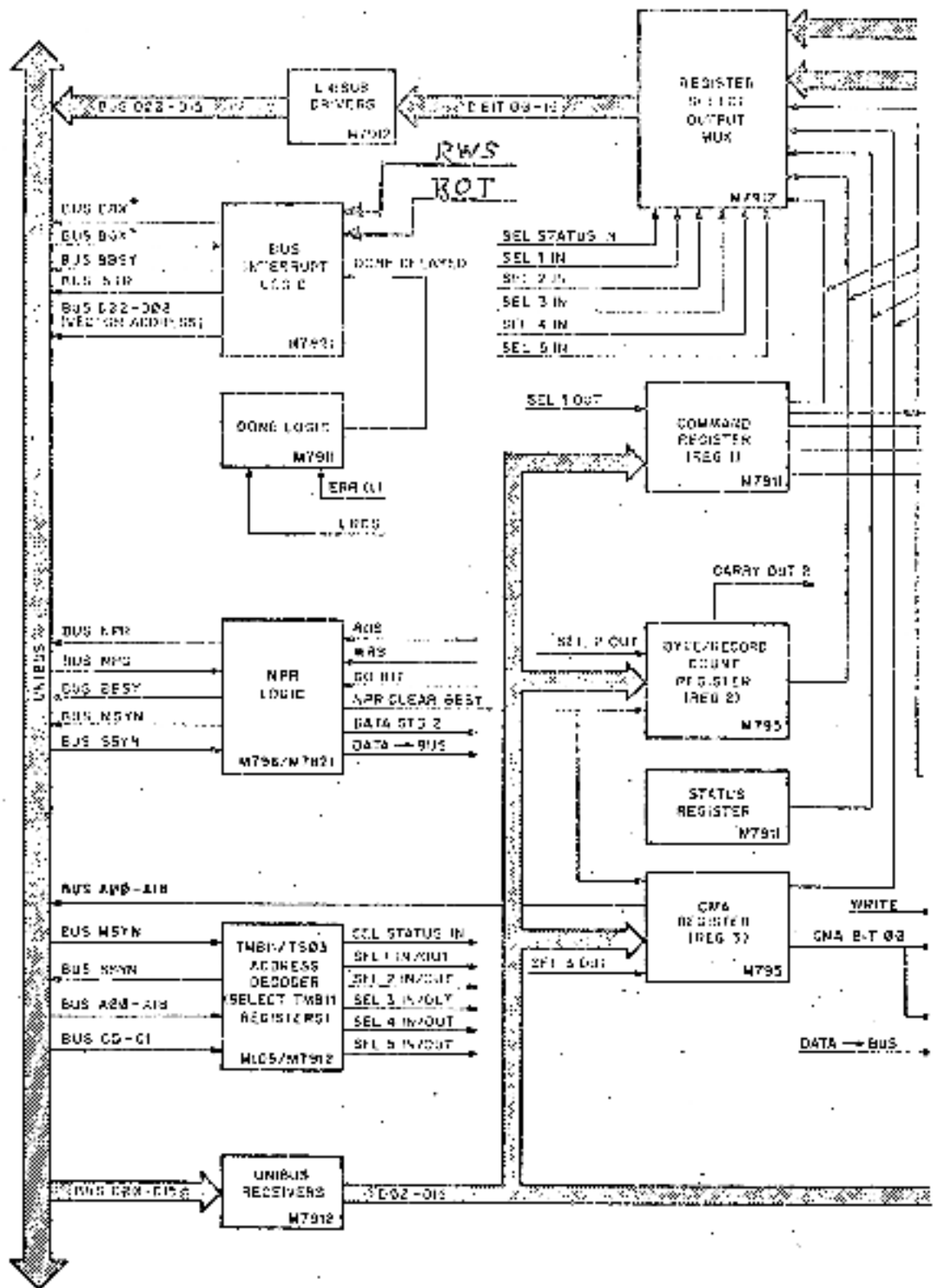


Figure 6-1 TMB11 Flow Diagram (Sheet 1 of 2)

6-5a



6-6

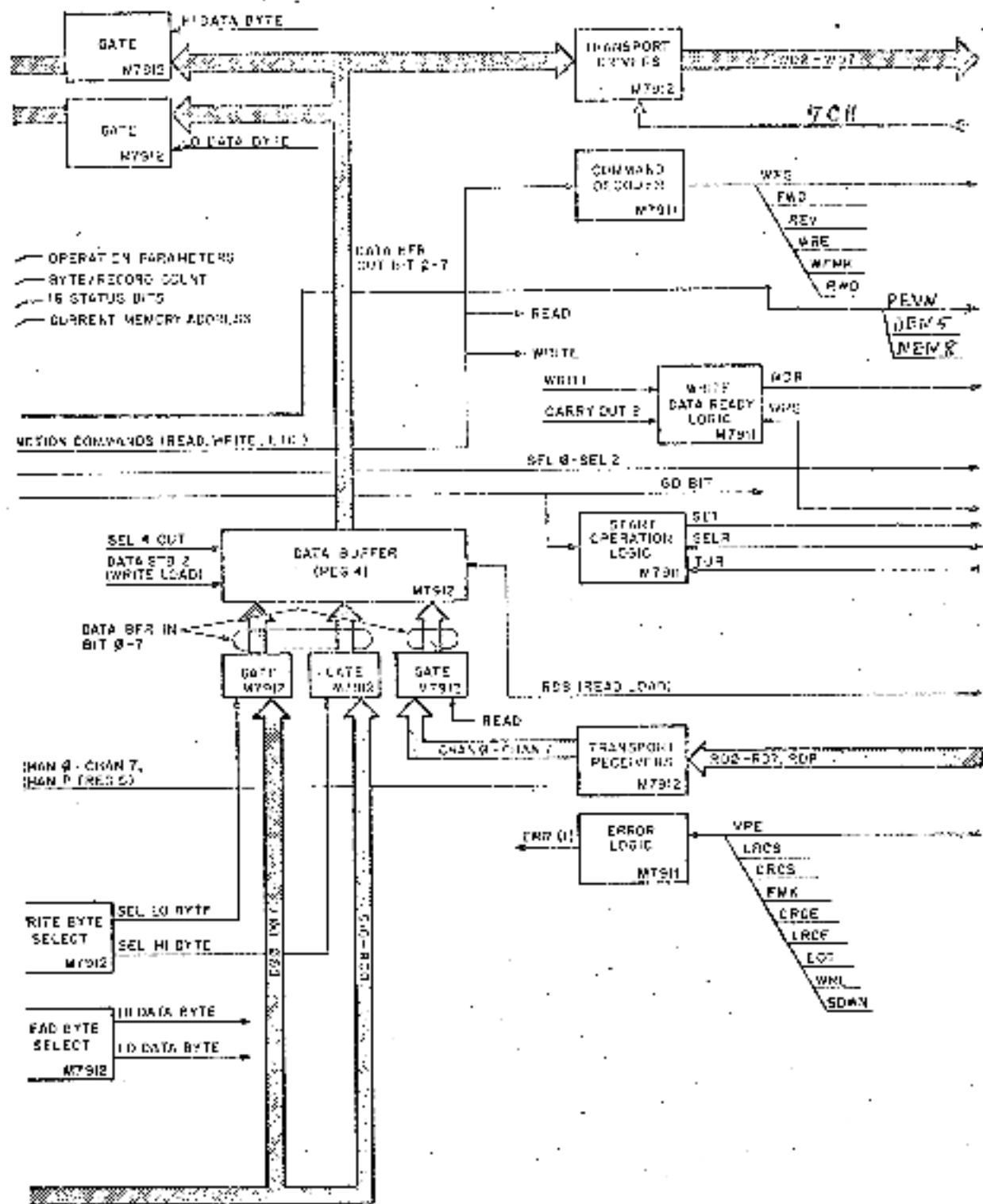


Figure 6-2 TMB11 Functional Block Diagram

6-62

Table 6-1 Device Register Functions

Register	Mnemonic	Function
Status Register	MFS	Provides detailed information on the status of the controller. Such information includes error indications and tape unit status indications.
Command Register	MTC	This is the main control register in the controller. Specifies the operation to be performed on the tape unit, selects the tape bit packing density, and selects the tape unit to be used. Indicates when the controller is ready, when an error condition exists, and when the controller is cleared.
Byte Readout Counter	MTBRC	Provides the two extended address bits for bus addresses. Counts the number of bytes in any write operation, the number of records in a space forward or space reverse operation, and the number of bytes in a read operation. Desired byte count is preset by the program. When the register counts the number of specified bytes, it prevents further transfers.
Current Memory Address Register	MTCMA	Specifies the bus or memory address to or from which data is transferred during read and write operations. After each transfer is completed, the register is automatically incremented by 1 (next byte location). When BGL or NXM errors occur, the register contains the address of the location in which the failure occurred. Note that this register is incremented by 1, and therefore, accesses byte, rather than word, locations.
Data Buffer Register	MTD	Contains the information read from or written on the tape. Serves as a buffer between the tape unit and the memory.
Tape Unit Read Lines	MTRD	Permits storage of data read from the tape transport. A parity bit indicates the occurrence of a parity error and the channel containing the error. A character selector bit is used to select the last character of a record that is to be loaded into the data buffer register. A timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. A BTE/OPI bit is used to set transfer done prematurely in order to provide a bad tape error indication.

Figures 6-3 through 6-9 show the bit assignments within the six device registers. Except in the case of the data buffer register, the "unused" and "load only" bits are always read as 0s. Loading "unused" or "read only" bits has no effect on the bit position.

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or occurrence of a power-up or power-down condition of either the processor power supply or the controller power supply.

The INIT signal clears the entire system; however, the INIT signal produced by a RESET instruction does not clear the processor. Clearing only the controller and the tape units can be accomplished by loading a 1 into bit 12 (POWER CLEAR) of the command register (MTC).

NOTE

INIT and POWER CLEAR deselect the current tape unit and select tape unit 0. Also, a rewind operation in progress continues to the load point.

6.4.1 Status Register (MTS)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILC	ERR	CRL	PAE	ESL	EDT	RLE	RDY/STC	KAM	SELR	MDZ	TCR	SDRN	WRL	HWG	TJR

Figure 6-3 Status Register (MTS) Bit Assignments

Bit	Meaning and Operation
15	<p>ILC - Illegal command bit. Indicates an illegal command. This bit is set whenever one of the following illegal commands occur:</p> <ul style="list-style-type: none"> a. Any DATO or DATOB transfer to the command register (MTC) during tape operation (CU RDY bit clear). The register cannot accept a new command while in the process of executing another command. b. A write, write end-of-file, or write-with-extended-IRG (command register functions 2, 3, and 6, respectively), when the WRL (write lock) bit is set. Writing is inhibited with WRL set, and write commands are illegal. c. Any command to a tape unit that has its SELR bit clear is illegal, because SELR clear indicates that the unit is not on-line. d. Any time the SELR bit becomes 0 during any operation except off-line, it sets the ILC bit, because no command can be issued to a unit that is not on-line.

If any of the illegal commands listed in a through c above occur, the command is loaded into the command register.

In all of the above cases, the ILC bit and the ERR bit (bit 15 in the command register) are set simultaneously.

Cleared by INIT or by the GO pulse to the tape unit.

14

EOF - End-of-file bit, used to indicate that the tape has reached the end of the file. An end-of-file (EOF) character is detected during a read, space forward, or space reverse operation. During the read or space forward operations, the EOF bit is set when the EOF character is read. During a space reverse operation, the EOF bit is set when the LRC character following the EOF character is read. The ERR bit (bit 15 in the command register) is set when the LRC character following the EOF character is detected. It is also set during WRITE EOF command.

The EOF bit is set only by the tape unit logic; it is cleared by INIT or by the GO pulse to the tape unit.

The EOF character is loaded into memory during read operations.

13

CRE - Cyclic redundancy error bit. A cyclic redundancy error can be detected during either a read or write operation. This check compares the CRC character, written on a 9-channel tape during a write or a write-with-extended-IRG operation, with the CRC character generated during a read operation.

If the two CRC characters are not the same, the CRCE from the tape unit becomes a 1, forcing the CRE bit to a 1. The ERR bit in the command register, however, is not set until the LRC character is detected.

Cleared by INIT or by the GO pulse to the tape unit.

12

PAE - Parity error bit. When set, this bit indicates that a parity error exists. The PAE bit is the logical OR of both vertical and longitudinal parity errors.

A vertical parity error is indicated on any character in a record; a longitudinal parity error occurs only after the LRC is detected.

A vertical parity error does not affect the transfer of data. In other words, the entire record is transferred to the tape during a write operation or transferred into memory during a read operation.

Both vertical and longitudinal parity errors are detected during read, write, and write-with-extended-IRG operations. The entire record is checked, including the CRC and LRC characters.

Longitudinal parity occurs when an odd number of 1s is detected on any channel in the record. Vertical parity error occurs when an even number of 1s is detected on any character, provided the PEVN bit (bit 14 in the command register) is clear, or if an odd number of 1s is detected when the PEVN bit is set.

When a parity error occurs, PAE is set, and the ERR bit (bit 15 in the command register) is set after the LRC character has been detected.

Cleared by INIT or by the GO pulse to the tape unit.

Bit**Meaning and Operation**

11

BGL - Bus grant late bit. If the controller issues a request for the bus and does not receive a bus grant before it must issue another bus request for the following tape character, a bus grant late error occurs.

This error condition is tested only for NPRs (non-processor requests). The UGL bit is set if an NPR bus request is not honored before the controller receives a WFS pulse for a write operation or an RDS pulse for a read operation.

The BGL bit and the PRK bit (bit 15 in the MTC) are set simultaneously, halting the operation.

If the BGL error occurred during a write or write-with-extended-IRG operation, the controller does not send the WDR signal to the master tape unit to allow the master tape unit to write data characters on the tape.

Cleared by INIT or by the GO pulse to the tape unit.

10

EOT - End-of-tape bit. The EOT bit is set as soon as the EOT marker is detected, when the tape is moving in the forward direction. It is cleared as soon as the EOT marker is detected, when the tape is moving in the reverse direction.

The EOT is an error condition if the tape is moving forward. Therefore, when EOT is set, ERR bit is also set when the LRC character is read.

Cleared by tape transport head passing over EOT marker when tape is moving in the reverse direction.

09

RLE - Record length error bit. The record length error is tested only during read operations. An error is indicated as soon as the byte record counter (MTBRC) attempts to increment beyond 0.

When a record length error occurs, the RLE bit is set, incrementation of the MTBRC and the current memory address register (MTCMA) ceases, and the ERR bit is set when the LRC character is read.

The CU RDY (bit 07 of the command register) remains cleared until the LRC character is read at which time CU RDY is set.

Cleared by INIT or by the GO pulse to the tape unit.

If the exact record length is desired following the occurrence of a record length error, it can be found by setting the MTBRC to a value so large as not to generate an RLE and re-reading the record. Record length can be derived by subtracting the current value of the MTBRC from its initial setting.

Bit

Meaning and Operation

08 **BTE/OPI** - Bad tape error operation incomplete bit. A bad tape error occurs when a character is detected (RDS pulse) during the gap shutdown or settle down period for any tape function except rewind.

During write, write EOF, or write-with-extended-LRG operations, a bad tape error sets both the BTE/OPI and ERR bits immediately on detecting the error.

During both read and space forward or space reverse operations, the BTE/OPI bit is set immediately on detection of bad tape.

During a read operation, the MTBRC increments continuously and words are read into memory until the MTBRC overflows. During a space operation, the MTBRC stops incrementing as soon as BTE occurs. When BTE is discovered, the tape unit stops, regardless of the state of the MTBRC.

Because it is not possible to artificially generate bad tape, bad tape may be indicated by setting the CU RDY bit prematurely, thereby producing the gap shutdown period while the data is still being read. The CU RDY bit is set by loading a 1 into bit 13 of the MTRD. If bit 13 of the MTRD is set during a record for either a read or write operation, a bad tape error indication occurs.

Any initiated tape operation other than a REWIND or OFF-LINE command that does not detect an LRC character within seven seconds results in setting the BTE/OPI bit. This 7-second time-out is called Operation Incomplete. Any legal size record with a legal size gap results in detection of an LRC character within seven seconds. During a spacing operation, the OPI timer is restarted at each interrecord gap. When the 7-second time-out occurs, the tape unit in operation is RESET by CINIT. The BTE/OPI bit is set and at TUR the CU RDY bit is set.

Cleared by INIT or GO.

07 **NXM** - Nonexistent memory bit. This error condition occurs when the controller is bus master during NPR transfers and does not receive an SSYN response within 20 μ s after asserting MSYN.

The NXM bit and the ERR bit are set simultaneously, halting the operation.

Cleared by INIT or by the GO pulse to the tape unit.

06 **SELR** - Select remote bit. The SELR bit is set when the tape unit has been properly selected. The SELR bit is 0 if the tape unit that is addressed does not exist (UNIT SELECT setting does not correspond to SEL bits), if the selected tape unit is off-line (ON-LINE/OFF-LINE switch set to OFF-LINE), or if the tape unit power is off.

05 **BOT** - Beginning-of-tape bit. The BOT bit is set as soon as the BOT marker is detected. When BOT is set, it has no effect on the ERR bit. The BOT bit remains cleared whenever the BOT marker is not being read.

This bit is set and cleared only by the tape transport.

Bit	Meaning and Operation
04	<p>7CH - 7-channel bit. This bit is cleared or set by the tape transport to indicate whether a 7-channel or 9-channel tape is being used.</p> <p>When 7CH bit is set, it indicates a 7-channel tape; when it is clear, it indicates a 9-channel tape.</p> <p>The 7CH bit is also used in conjunction with the DEN 8 and DEN 5 bits in the command register to cause the core dump mode of operation. When the 7CH, DEN 8, and DEN 5 bits are all set, the core dump mode of operation is used.</p>
03	<p>SDWN - Settle down bit. The settling down period is provided to allow the tape to fully stop prior to starting a new operation. This settling down period sets the SDWN bit. When the tape unit stops, SDWN is cleared, and the tape unit ready (TUR) bit is set.</p> <p>During a tape reverse operation (this does not include rewind operations), the gap shutdown period begins immediately after the first gap encountered after spacing over a record.</p>
02	<p>WRL - Write lock bit. The write lock bit is under control of the tape transport. When set, it prevents the controller from writing information on the tape.</p>
01	<p>RWS - Rewind status bit. This bit is under control of the tape unit. It is set at the start of a rewind operation and clears as soon as the rewind sequence is complete.</p>
00	<p>TUR - Tape unit ready bit. This bit is under control of the tape transport. Whenever the selected tape unit is being used (such as rewind), this bit is cleared. When the tape unit is stopped and ready to receive a new command, the tape transport sets the TUR bit.</p>

NOTE

Status register bits 00 - 05 are cleared or set by the tape transport, not the controller.

6.4.2 Command Register (MTC)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DFN 8	DEN 5	PWR CLA	PEVN	SEL 2	SEL 1	SEL 0	CU MDY	INT ENB	DIRS BIT 17	DIRS BIT 16	FCTN BIT 2	FCTN BIT 1	FCTN BIT 0	CO

II-0434

Figure 6-4 Command Register (MTC) Bit Assignments

Bit

Meaning and Operation

15 **ERR** - Indicates an error condition that is the inclusive OR of all error conditions (bits 15 - 07 in the Status Register, MTS). Causes an interrupt if enabled (see bit 06). The ERR bit is not set for some errors until the longitudinal redundancy check (LRC) character is read, in order to allow the current operation to be completed. Specific error conditions are described in the status register bit assignments (Figure 6-3).

When ERR is set, it sets bit 07 (CU RDY) when the tape unit asserts TUR.

Cleared by INIT or by the next GO command (bit 00).

14 **DEN 8** - This bit, in conjunction with bit 13, selects the bit packing density of the tape. These combinations are shown below. Note that this bit, in conjunction with DEN 5 and 7CH in the MTS, can be used to select the core dump mode for 7-channel tape.

Bit 14 (DEN 8)	Bit 13 (DEN 5)	Density (bpi)	
0	0	200	} 7-channel tape
0	1	556	
1	0	800	
1	1	800	} 9-channel tape/7-channel core dump

13 **DEN 5** - This bit, in conjunction with bit 14, selects the bit packing density of the tape. See bit 14 above for combinations.

12 **PWR CLR** - When a 1 is loaded into this bit position, it clears the controller logic and all tape units. This bit becomes a 1 for 1 μ s during a processor DATO cycle, provided the corresponding bit on the bus is a 1. Always read by processor as a 0.

11 **PEVN** - This is the even parity bit. This bit is set whenever the selected tape unit is to write or read even vertical parity on or from the tape. The bit is 0 whenever the selected tape unit is to write or read odd vertical parity on or from the tape.

A search for parity error is made whenever the tape moves. The controller ignores parity errors during space forward, space reverse, or rewind operations.

Cleared by INIT or by loading with a 0.

10-08 **SEL** - These three unit select bits specify the number of the tape unit that is to function as the unit under program control. These three bits (SEL 2, SEL 1, and SEL 0) are set or cleared to represent an octal code that corresponds to the unit number of the tape unit to be used. The tape unit number is selected by the UNIT SELECT plug on the tape transport.

Cleared by INIT or by loading with a 0.

Bit	Meaning and Operation
07	<p>CU RDY - When set, indicates that the controller is ready to receive a new command. This bit is set at the end of a tape operation (indicating that a new operation can be started) and is cleared at the beginning of a tape operation (indicating that the controller is not ready for new commands).</p>

This bit is also set (indicating CU RDY) whenever ILC (bit 15 of MTS) is set or whenever INIT is generated.

06	<p>INT ENB - Interrupt enable bit. This bit, when set, allows an interrupt to occur, provided either CU RDY (bit 07) or ILC (bit 15 of MTS) is set. With INT ENB set, a REWIND command can cause two interrupts - one at initiation and one at completion.</p>
----	---

An interrupt also occurs whenever an instruction sets the INT ENB bit but does not set the GO bit (bit 00). Interrupts are described in Paragraph 6.2.4.

Cleared by INIT or by loading with a 0.

05	<p>ADRS BIT 17 - Extended bus address bit 17. Used to specify address line 17 in direct memory transfers. Increments with the current memory address register (MTCMA). Cleared by INIT.</p>
----	--

04	<p>ADRS BIT 16 - Extended bus address bit 16. Function is the same as ADRS BIT 17 (bit 05 above).</p>
----	--

03-01	<p>FUNCTION - These bits specify a command to be performed by the selected tape unit. These functions are:</p>
-------	---

Octal No.	Function Bits			Function
	03	02	01	
0	0	0	0	Off-line
1	0	0	1	Read
2	0	1	0	Write
3	0	1	1	Write end-of-file
4	1	0	0	Space forward
5	1	0	1	Space reverse
6	1	1	0	Write-with-extended IRG
7	1	1	1	Rewind

All function bits cleared by INIT.

00	<p>GO - Loaded with a 1 from the bus to initiate the function selected. Clears CU RDY bit.</p>
----	---

Cleared when GO pulse is sent to tape transport. Normal time duration of bit is 1 μ s, but this time may extend to as long as several minutes in the case where the bit is loaded for a tape unit that is in the process of rewinding.

Also cleared by INIT or cleared whenever ILC in the status register is set.

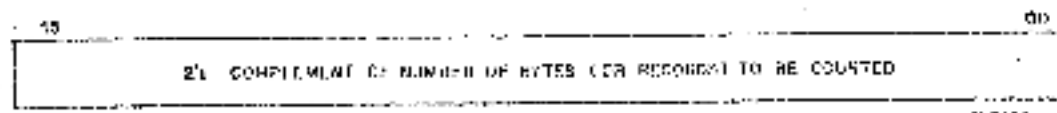


Figure 6-5 Byte/Record Counter (MTBRC) Bit Assignments

Bit	Meaning and Operation
15-00	<p>Contains the 2's complement of the number of bytes or records to be transferred. The desired value is loaded by the program on a processor DATO. Cleared by INIT. Increments by 1 after each memory access.</p> <p>The byte record counter (MTBRC) is a 16-bit binary counter used to count bytes in a read or write operation and used to count records in space forward or reverse operations.</p> <p>When used in a write or write-with-extended-IRG operation, this register is set by the program to the 2's complement of the number of bytes to be written on the tape. After the last byte of the record has been strobed from memory, the MTBRC becomes 0. Thus, when the next write strobe signal is received from the master tape transport, the controller lowers the write data ready line to indicate to the master transport that there are no more data characters in the record.</p> <p>When used in a read operation, the MTBRC is set to a number equal to or greater than the 2's complement of the number of words to be loaded into memory. A record length error, which occurs for long records only, occurs whenever a read pulse is generated after the MTBRC is at 0. Neither the CRC or LRC character is loaded into memory during a read operation, although both characters are checked for parity errors.</p> <p>When used in a space forward or space reverse operation, the MTBRC is loaded with the 2's complement of the number of records to be spaced. The counter is incremented by 1 at LRC time, regardless of tape direction.</p>

6.4.4 Current Memory Address Register (MTCMA)

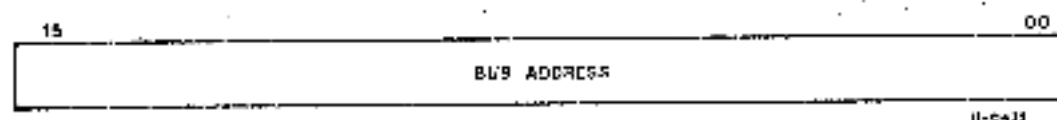


Figure 6-6 Current Memory Address Register (MTCMA) Bit Assignments

Bit

Meaning and Operation

15-01

These bits specify the bus or memory address to or from which data is to be transferred during write or read operations. Only bits 01-15 of the MTCMA are accessible by the program, although bits 00-15 participate in NPR transfers. Bit 00 always starts in the cleared or even byte state because all NPR transfers access even boundaries for a starting byte address. Therefore, MTCMA must be initially loaded with an even address. The MTCMA contains 16 of the possible 18 memory address bits. The remaining two bits (16 and 17) are part of the command register.

Before issuing a command, the program loads the MTCMA with the memory address that is to receive the first byte of data (read operation) or with the memory address from which the first byte is to be taken (write operation). After each memory access (read or write), the MTCMA is immediately incremented by 1 (the next byte boundary). Therefore, at any given time, the MTCMA points to the next memory byte address that is to be accessed. On completion of the record transfer, the MTCMA points to the address plus 1 of the last character in the record.

If a bus grant late (BGL) or nonexistent memory (NXM) error occurs, the MTCMA contains the address of the location in which the failure occurred.

If an 18-bit memory address is required, the program loads the appropriate address into bits 01-15 of the MTCMA and into extended address bits 16 and 17 of the command register. The extended address bits are a logical extension to the MTCMA register and participate in any required incrementation.

6.4.5 Data Buffer Register (MTD)

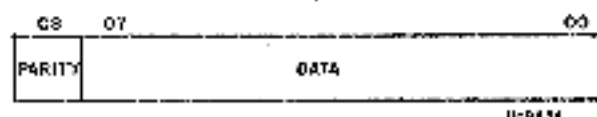


Figure 6-7 Data Buffer Register (MTD) Bit Assignments

Bit

Meaning and Operation

15-09
(not shown)

Correspond to bits 07-01 respectively on a processor DATI cycle.
Example: Bit 15 = bit 7, bit 14 = bit 6, etc.

08

Correspond to the parity bit on the magnetic tape. During a processor read operation, this bit is stored in memory. During NPR operations, this bit is read by the controller but not loaded into memory. During operation of a 9-channel tape unit, this bit is valid only after the CRC character has been read, provided bit 14 of the MTRD is a 1.

NOTE

The parity bit is generated by the master tape transport; it is not generated by the controller. However, the polarity of the parity bit (odd or even) is determined by the PEVN bit in the command register.

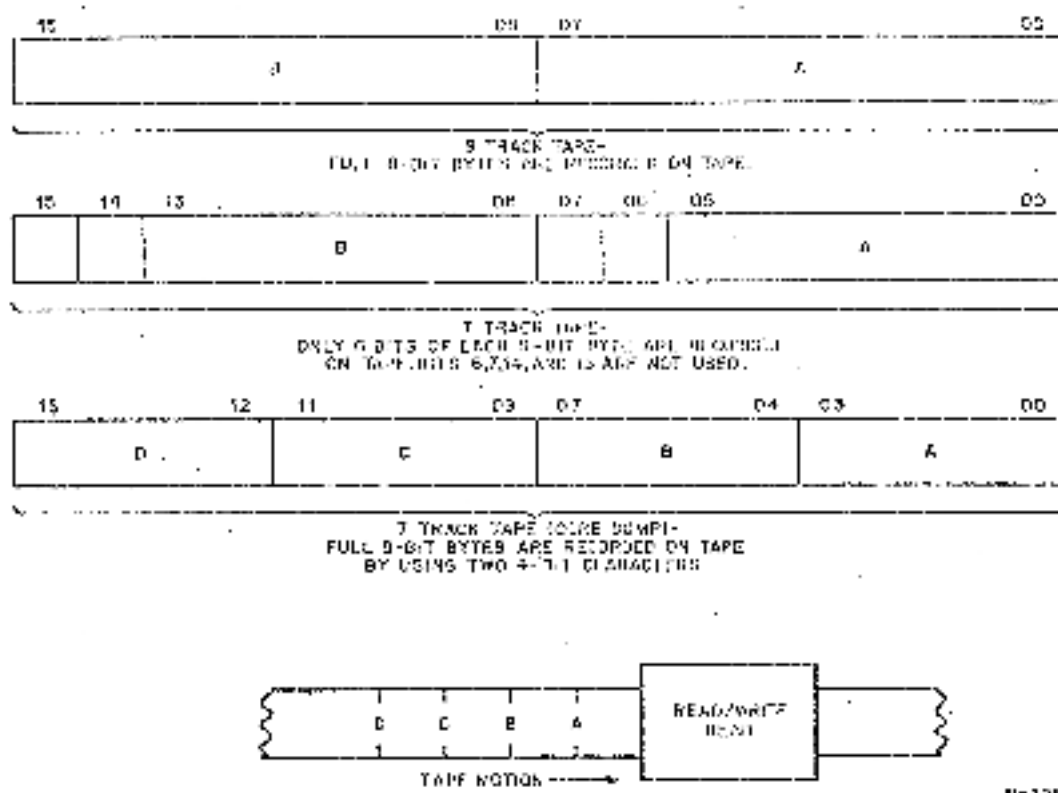


Figure 6-8: Relationship Between Tape Characters and Memory Byte Characters

Bit

Meaning and Operation

07-40

During read operations, these bits are used for temporary storage of characters read from tape prior to loading into memory. During write operations, these bits are used for temporary storage of data from memory before writing on tape.

During read operations, the LRC character enters the data buffer when bit 14 of the address location for the read lines register is a 1; the LRC character is prevented from entering the data buffer when bit 14 is a 0. Thus, after reading a 9-channel tape, the data buffer contains an LRC character (if bit 14 is a 1) or a CRC character (if bit 14 is a 0). After reading a 7-channel tape, the data buffer contains either the LRC character (if bit 14 is a 1) or the last data character (if bit 14 is a 0). After reading an EOF character, the data buffer contains either all 0s (bit 14 is a 1) or the EOF character (bit 14 is a 0).

The data buffer can store only bytes; therefore, two bus cycles are required to transfer a word. During NPR operation the data bits are written into or read from alternate low and high byte positions. The relationship between tape characters and high and low memory byte characters is shown in Figure 6-8.

6.4.6 Read Lines Register (MTRD)

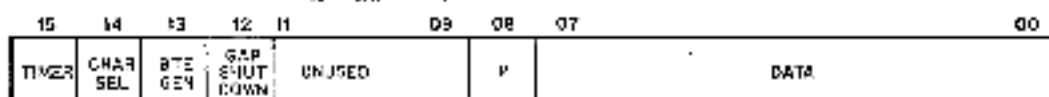


Figure 6-9 Read Line Register (MTRD) Bit Assignments

Meaning and Operation

Bit			
15	TIMER - The timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. The timer signal is a 100 μ s signal with a 50% duty cycle and is generated by the controller. It is read as bit 15 in the memory location reserved for the read data lines register. Read only bit.		
14	CHAR SEL. This bit is used to select the last character of a record that is to be loaded into the data buffer. Read/write bit. Selection is as follows:		
	7-channel	9-channel	
	Set	LRC character	LRC character
	Clear	Last data character	CRC character
13	BTE GEN - Bad tape error generator bit. Actually, bad tape cannot be artificially generated. When set, this bit sets the CU RDY bit. With CU RDY set, a premature gap shutdown is generated, which produces a bad tape error indication when data is read during this period. Write only bit.		
12	GAP SHUTDOWN - Read only bit. When set, indicates a gap shutdown period.		
11-09	Unused.		
08	PARITY - Corresponds to the parity bit read from the tape by the master tape transport. Used in conjunction with bits 07-00 to indicate a longitudinal parity error. After a read or write operation, bits 08-00 should all be 0. If one or more of these bits remains a 1 after the operation is complete, it indicates a longitudinal parity error. The bit position containing the 1 indicates the tape channel containing the error. Read only bit.		
07-00	DATA - These bit positions contain information read from the magnetic tape transport. After these positions are read by the processor, all bit positions clear unless a parity error exists.		
	Bits 07-00 in the read lines register correspond to tape channels 00-07, respectively. Read only bits.		

6.5 PROGRAMMING NOTES

In normal programming practice no attempt should be made to modify one record in the middle of a file. This practice could result in overwriting the boundary of the record and destroying part of the next record. Also, a read operation should never directly follow a write operation without at least one intervening tape move operation. This prevents generating a BTE/OP if the previous operation involved the last record on the tape. If it is desired to read a record that was just written, a space reverse command should be issued before the read command. New commands are issued only when CU RDY is set, which is true after interrupts.

Attempting to write an all zero character with even parity on a 7-track or 9-track tape unit causes the zero character to be converted to a tape character of 20. When reading this character from tape, a 20 is read instead of zero.

ASCII standards provide for a 25-ft trailer following the end-of-tape marker. This allows approximately 18 ft of writing space after passing EOT. Care should be taken when attempting to write past the EOT marker if the operator is not familiar with the tape that he is working with, because after a tape has been used, the reflective markers are often changed, possibly decreasing the length of the standard 25-ft trailer.

Because the physical displacement of the heads differ between 7-channel and 9-channel drives, records written on one cannot be read by the other. However, a tape that is recorded on one can be re-recorded by the other, providing you begin at the load point.

If two drives are sharing one controller, care should be taken not to allow both drives to have the same unit number selected on the unit select plugs. If they are both set to the same number and a command is issued, they will both attempt to respond and data transfers will become totally confused.

The industry-standard packing density for 9-channel drives is 800 bpi. However, 9-channel drives may be recorded at 200, 556, or 600 bpi, providing the data is read back at the same rate.

A SPACE REVERSE or REWIND command issued while the tape is at the load point will cause an immediate interrupt.

6.5.1 Rewind Operation

Assume drive 0 is to be rewound. The command to rewind drive 0 is issued to the controller. At this time the master tape unit asserts bit 1 (RWS) in the status register. If bit 6 (INT ENB) in the command register was set at the start of the rewind operation, an interrupt occurs from the controller as soon as bit 7 (CU RDY) of the command register has been set by RWS. This informs the program that the controller is ready to accept a new command. By testing bit 1 (RWS) in the status register, the program can determine if this interrupt was issued as a result of drive 0 completing its rewind operation or just beginning it.

When the reflective marker, signifying BOT, is sensed, bit 5 (BOT) is asserted in the status register only for the duration of time that the reflective marker is being read. Tape motion does not stop at this time.

Drive 0, still moving in the reverse direction, passes over the reflective marker, reverses its direction, and proceeds in the forward direction back to the load point. Upon sensing the reflective marker while proceeding in the forward direction, drive 0 halts tape motion, asserts bit 3 (SDWN) allowing the tape to fully deskew, and then sets bit 0 (TUR) in the status register.

An interrupt is issued coincident with bit 0 (TUR) being asserted in the status register, providing the following conditions have been met.

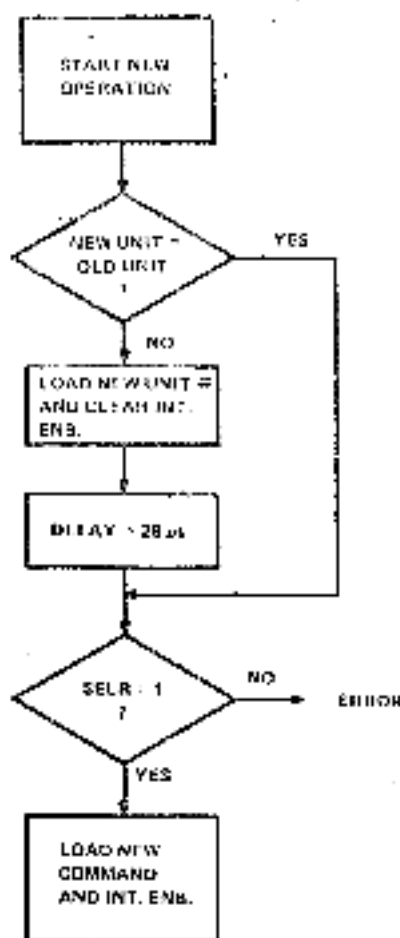
1. Bit 6 (INT ENB) in the command register is set,
2. The drive has not been deselected by changing the status of bits 10-8 in the command register since issuing the REWIND command.

If multiple transports are used, it is not necessary to wait for a REWIND command to be completed on one transport before switching to another. After a REWIND is issued, another transport can be switched to as soon as RWS is set.

When operations on the second transport have been completed, a switch to the rewinding transport can be made as soon as SDWN or TUR is true on the second transport (so the status bits will be from the rewinding unit). Only the unit select bits in the command register have to be changed to the unit that is rewinding to get its status. If the rewind is complete when the unit is selected, TUR is set in the status register. If the RWS bit is still set, the software can either work on another transport or load the next command to be executed in bits 1-3 of the command register where it is buffered until the rewind is completed. If INT ENB is set at this time, the completion of the buffered command causes an interrupt to occur. A REWIND command may take from 3 to 5 minutes to complete.

6.5.2 New Drive Selection

Figure 6-10 is a flowchart for new drive selection.



11-2873

Figure 6-10 New Drive Selection Flowchart

Other programming restrictions occur when using select remote along with tape unit ready. The select remote lines for all tape units that are not addressed are at 0. A tape operation may be performed only on a selected tape unit and one whose SELR line is a 1. Thus, whenever a command is sent to a different tape unit from the one presently indicated by the unit select hits, the SELR line becomes 0 almost immediately (less than one instruction time later) and becomes a 1 from 1 to 28 microseconds later.

6.5.3 Error Handling

6.5.3.1 Write Operations

1. ILC - Illegal Command
 - If SELR (bit 6 of MTS) is not set to a 1, or WRL (bit 2 of MTS) is set to a 1, then operator intervention is required to ensure that the drive to be used is properly selected and is not write locked.
 - If SELR (bit 6 of MTS) is set to a 1 and WRL (bit 2 of MTS) is not set to a 1, then a command has been issued while CU RDY (bit 7 of MTC) was cleared. Try the operation again, ensuring first that CU RDY is set before issuing a new command.
2. EOF - End-of-File N/A
3. CRE - Cyclic Redundancy Error
Backspace and try operation again with extended IRG.
4. PAE - Parity Error
Backspace and try operation again with extended IRG.
5. BGL - Bus Grant Late
Backspace and try operation N times.
6. EOT - End-of-Tape
The reflective marker signifying the end-of-tape has been passed. Operations past this point are not illegal, however, they are not recommended unless the programmer is familiar with the tape being used and is knowledgeable about the length of tape existing past the EOT marker. Conducting any write operations past the EOF marker leaves the programmer open to the possibility of running the tape off of the reel.
7. RLE - Record Length Error N/A
8. BTE/OPI - Bad Tape Error/Operation Incomplete
Regain a known tape position and try the operation again with extended IRG.

NOTE

A known tape position refers to BOT, header records, or EOT marks.

9. NXM - Nonexistent Memory
Resolve the memory discrepancy and try the operation again.

6.5.3.2 Read Operations

1. ILC - Illegal Command
 - If SELR (bit 6 of MTS) is not set, then operator intervention is required to ensure that the drive to be used is properly selected.
 - If SELR (bit 6 of MTS) is set, then a command has been issued while CU RDY (bit 7 of MTC) was cleared. Try the operation again ensuring that CU RDY is set prior to issuing the new command.

2. EOF - End-of-File
The characters signifying the end of a file have been read.
3. CRE - Cyclic Redundancy Error
Backspace and try the operation N times.
4. PAE - Parity Error
Backspace and try the operation N times.
5. BGL - Bus Grant Late
Backspace and try the operation N times.
6. EOT - End-of-Tape
The reflective marker signifying the end-of-tape has been passed. Continue only if it is certain that an EOF mark exists after the EOT marker, or the tape will run off of the reel.
7. RLE - Record Length Error
Reset the MTBRC to a value that is equal to or greater than the number of bytes in the record, backspace, and try the operation again.
8. BTE/OPI - Bad Tape Error/Operation Incomplete
Regain a known tape position and try the operation again. If, after doing so, the condition still persists, the data from the failing point to the next known tape position is lost.
9. NXM - Nonexistent Memory
Resolve the memory location discrepancy and try the operation again.

6.5.3.3 Write End-of-File Operation

BTE/OPI - Bad Tape Error/Operation Incomplete.
Regain a known tape position and try the operation again.

6.5.3.4 Spacing Operations

1. ILC - Illegal Command
Same as read operation.
2. EOF - End-of-File
The characters signifying the end of a file have been read. Detection of the EOF marks stops a spacing operation even if the MTBRC is not equal to zero.
3. EOT - End-of-Tape
Same as read operation.
4. BTE/OPI - Bad Tape Error/Operation Incomplete
Regain a known tape position and try N times.

6.5.3.5 Write-with-Extended-IRG Operation - Same as write operation.

6.5.3.6 Rewind Operation - Once a rewind operation is started, it continues until complete, regardless of errors or unit detection.

6.6 FUNCTIONAL DESCRIPTIONS

The TMB11 Controller may be divided into eight functional areas as follows:

1. Processor Data Transfer - The reading or writing of TMB11 registers by the processor (DATI/DATO).
2. Operation Start - The sequence from setting the GO bit to issuing SET to the transport to start tape motion.
3. NPR Bus Cycle - Acquiring bus mastership for an NPR transfer.
4. NPR Read (DATO) - The transfer of characters from the tape transport to memory.
5. NPR Write (DATI) - The transfer of characters from memory to the tape transport.
6. Operation Done - The terminating sequence of a TMB11 operation.
7. Error Sequence - The system errors detected by the controller and how they occur.
8. Interrupt Bus Cycle - Acquiring bus mastership for a processor interrupt.

These eight functional areas are discussed in the following paragraphs. Block diagrams, flow diagrams, and timing diagrams complement the discussions.

NOTE

The block diagrams that follow use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the controller logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used they are enclosed in parenthesis.

Integrated circuit data sheets are contained in Appendix F.

6.6.1 Processor Data Transfer

6.6.1.1 Processor Out (DATO) Transfer (TMB11 Register Write) (Figures 6-12 and 6-13) - The processor selects the TMB11 for a data transfer by asserting the proper address on BUS A04-A17 to the TMB11 address decoder (address range = 772570 to 772586). When the decoder recognizes the proper address it enables the address MSYN gate which asserts ADDR DEC MSYN when BUS MSYN is received from the processor. ADDR DEC MSYN enables the select in/out logic which looks at BUS A01-A03 to select one of the six controller registers. The control select logic looks at BUS C0-C1 and BUS A00 and asserts OUT HI, OUT LO, or neither according to whether a high byte is to be written, a low byte is to be written, or a processor read operation is to occur. The control select output enables the corresponding portion of the select in/out logic which outputs the loading strobe for the selected register.

When an "out" transfer is commanded, the SEL 1(4,5) OUT HI strobes will load their respective registers, when selected.* The SEL 2 OUT HI, SEL 3 OUT HI, and SEL 4 OUT I/O through SEL 4 OUT I/O strobes are ANDed with SSYN INH to produce corresponding SLCF loading strobes. SSYN INH is produced by inverting ADDR DEC MSYN on the M105 module. A delay occurs with the inversion, thus the loading of registers with SLCF strobes will be later (with respect to BUS MSYN) than the loading of those with SEL strobes.

The information is strobed into the selected register a byte at a time; D00 - D07 = low byte, D08 - D15 = high byte.

SSYN INH becomes BUS SSYN to notify the processor that the information on the data bus has been strobed into the selected register.

The command register contains the type of operation to be performed and the operation parameters. D13 and D14 are the density bits outputting DEN 5 and DEN 8. The processor sets these bits according to the desired mode of operation as shown in Table 6-2.

Table 6-2 Modes of Operation

Mode	DEN 5	DEN 8
200 bpi, 7-track	0	0
556 bpi, 7-track	1	0
800 bpi, 7-track	0	1
800 bpi, 9-track	1	1

The core dump mode is enabled when the program asserts both DEN 5 and DEN 8 while the 7-channel (7CH) signal from the tape transport is true (indicating that a 7-channel tape transport is being used). DEN 5 (1) and DEN 8 (1) are applied to an AND gate that is enabled by the 7CH signal from the transport. The output from this AND gate is CORE DUMP which, when true, inhibits the DEN 5 AND gate thereby negating DEN 5. Thus, an 01 density code is sent to the tape transport indicating an 800 bpi data transfer.

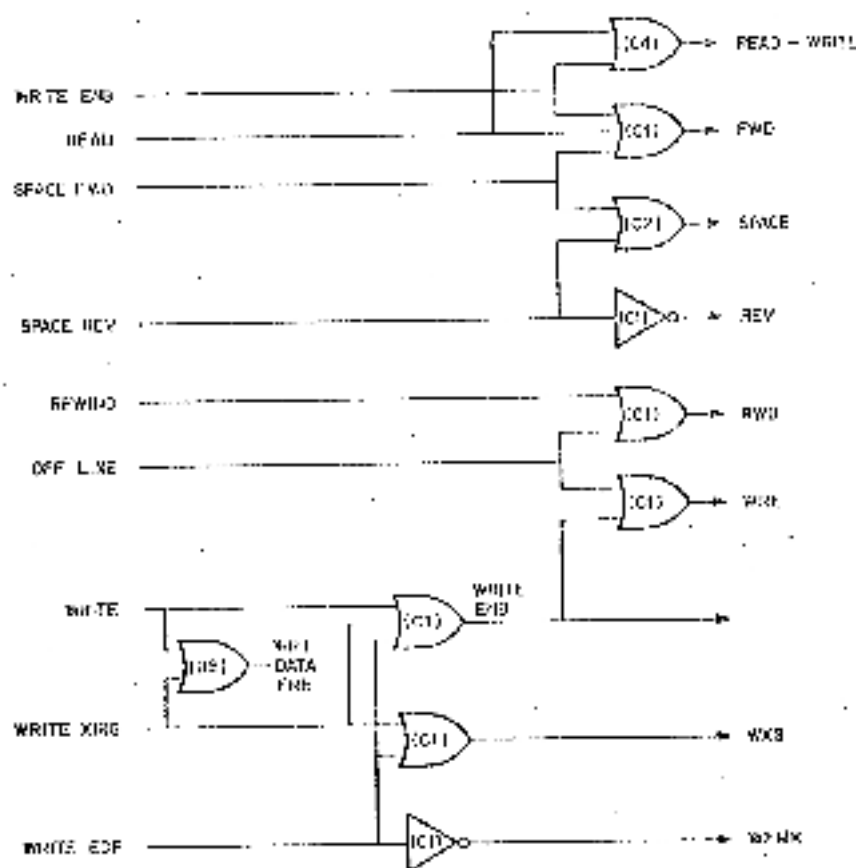
The command register also specifies even or odd parity to the transport (PEVN), selects the desired transport (SEL0-SEL2), enables or inhibits BR cycles (INT ENB), and specifies the function that the transport is to perform via a 3-bit function decoder. In addition, the command register carries 2 memory address bits to extend the current memory address register to 18 bits. Bit 00 of the command register is the GO bit which initiates the commanded operation.

Other registers addressed during a processor out-operation are:

- The current memory address register, which is loaded with the address of the first byte to be transferred
- The byte record counter, which is loaded with the 2's complement of the number of bytes to be transferred
- The LRC ENB (1) bit of the read lines register which, when set, allows the LRC character to be read into the data buffer.

*See Figure 6-27 for processor write of register 4.

6.6.1.2 Command Decoder (Figure 6-11) - The command decoder converts the eight functions generated by the command register function decoder into the six commands required by the tape transport. Figure 6-11 illustrates the functions that make up each of the transport commands. Table 6-3 illustrates the conversion in tabular form.



NOTE:
Designations in parentheses refer to engineering drawings containing corresponding logic.

6-4120

Figure 6-11 Command Decoder Logic Diagram

Table 6-3 Function Decoder Output vs Transport Commands

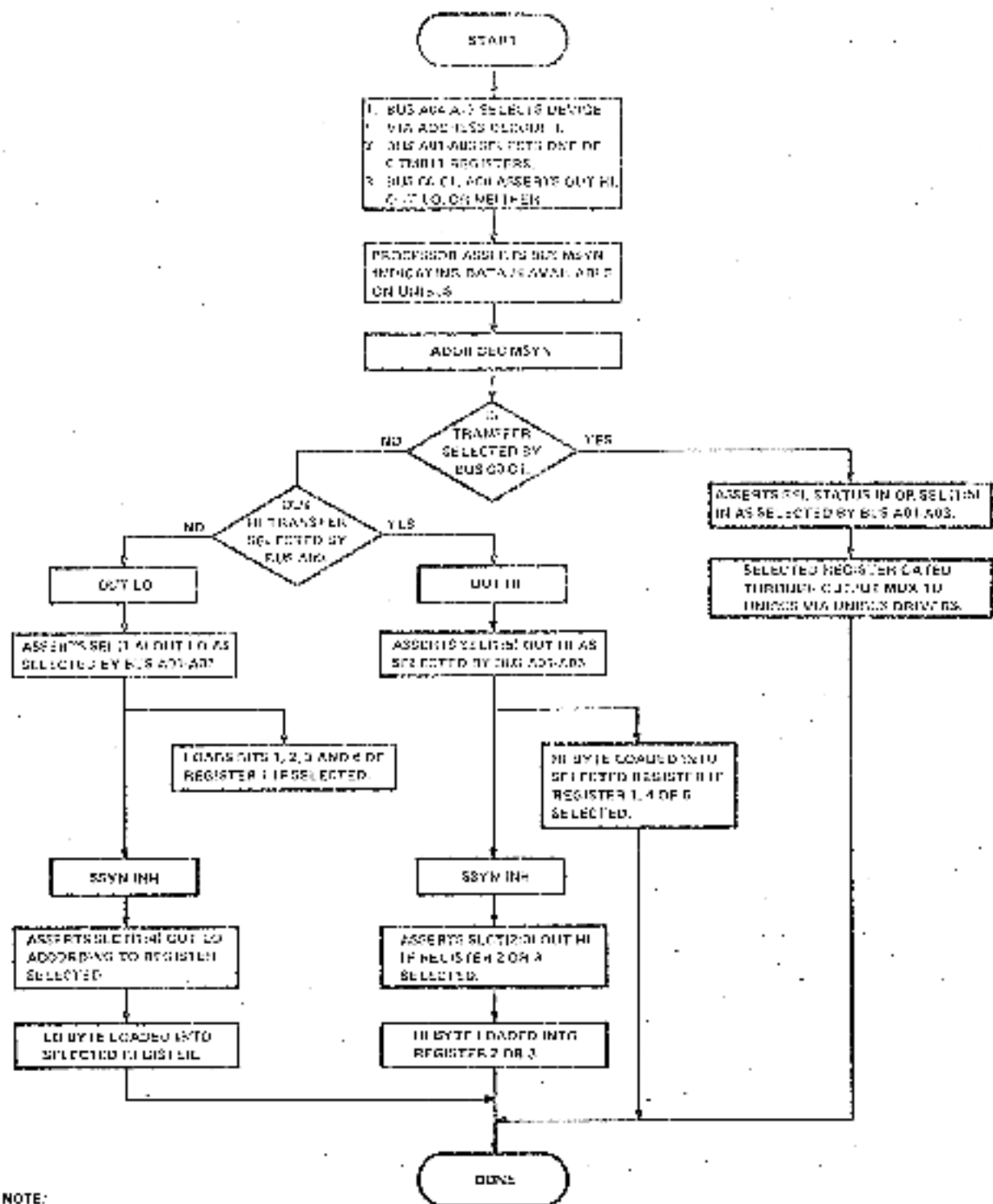
COMMAND DECODER FUNCTIONS	TRANSPORT COMMANDS					
	FWD	REV	RWD	WRE	WXG	WEMK
OFF LINE			X	X		
READ	X					
WRITE	X			X		
WRITE EOF	X			X	X	X
SPACE FWD	X					
SPACE REV		X				
WRITE XIRG	X			X	X	
REWIND			X			

The conversion is mostly ORing and is straightforward except for the OFF LINE function. If the processor orders an OFF LINE function, RWD (rewind) and WRB (write enable) is asserted to the transport. Writing during a rewind is an impossible situation that the transport interprets as an OFF LINE command. Four other signals are generated in the command decoder for use throughout the TMBII. These signals are OR functions of decoder commands as shown in Table 6-4.

Table 6-4 Decoder ORed Functions for TMBII 2

TMBII Signal	ORed Function
WRITE DATA ENB	WRITE WRITE XIRG
WRITE ENB	WRITE WRITE XIRG WRITE EOF
READ + WRITE	WRITE WRITE XIRG WRITE EOF READ
SPACE	SPACE FWD SPACE REV

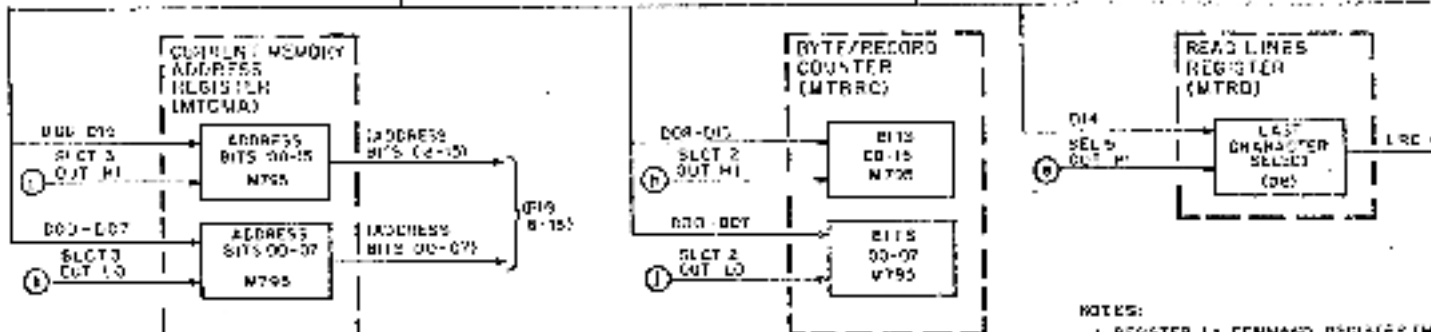
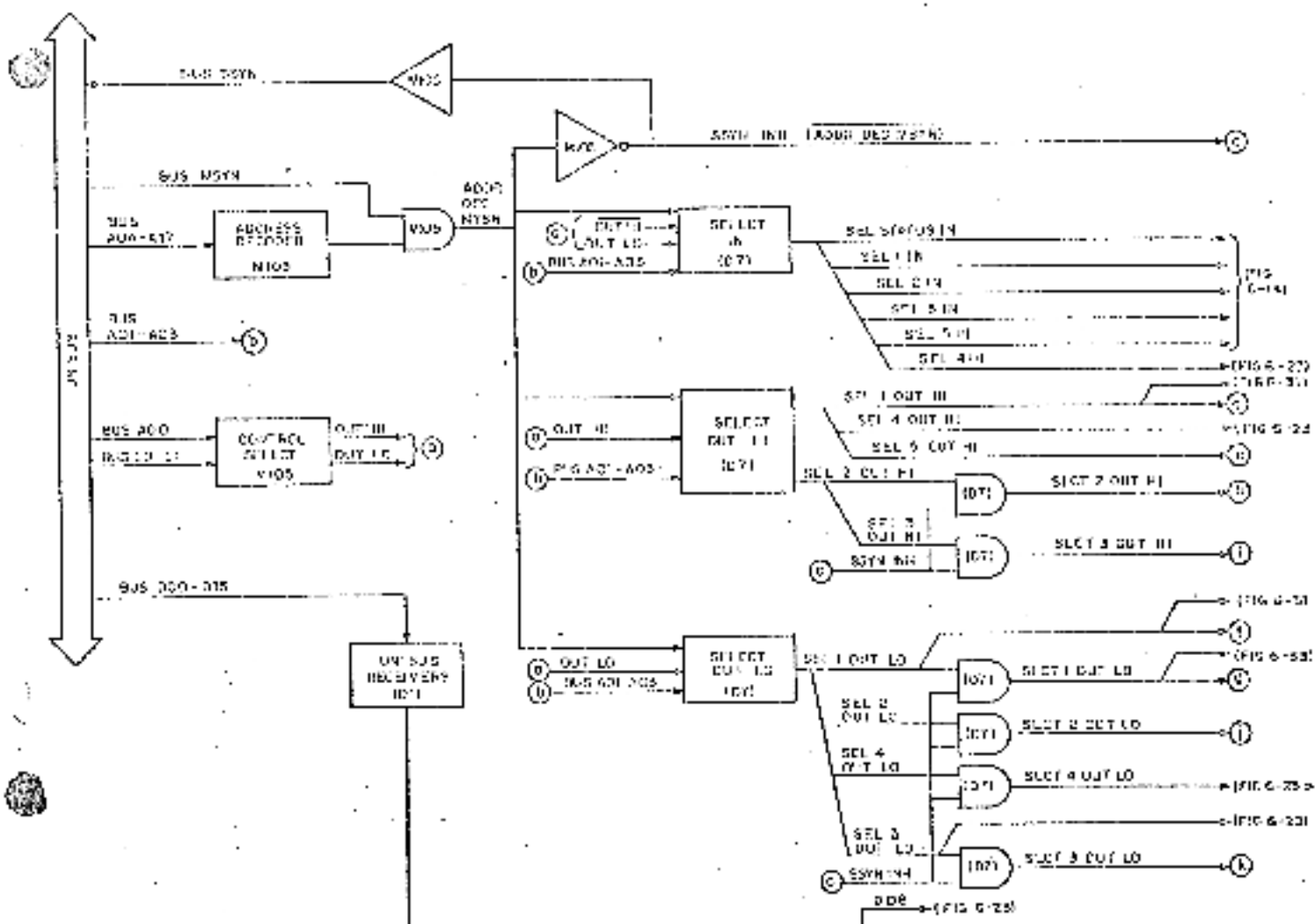
6.6.1.3 Processor In (DATA) Transfer (TMBII register read) (Figures 6-12 and 6-14) - When an "in" transfer is commanded by the processor, OUT HI and OUT LO from the control select logic are negated thereby enabling the select in logic. BUS A01-A03 selects one of the six controller registers and outputs the corresponding SCL IN gating strobe to the output select multiplexer. Accordingly the 16 bits of the status register, register 1, 2, 3, 4, or the 12 bits of register 5 are gated out to the Unibus via the Unibus drivers (see Figure 6-23 for processor read of register 4).



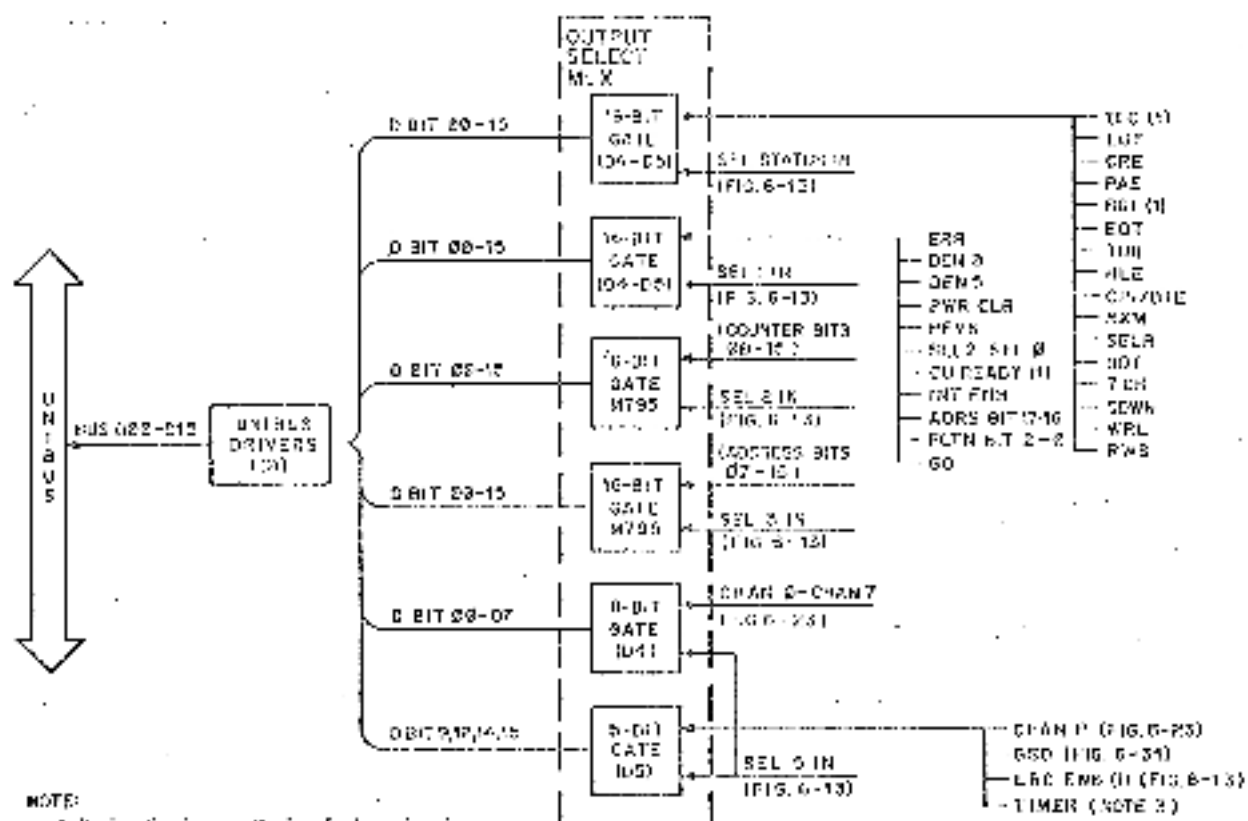
NOTE:
 During processor address of the TM311 an IN transfer is a processor to transfer or a read of the TM311. An OUT transfer is a processor out transfer or a write into the TM311.

11-4143

Figure 6-12 Processor In/Out Flow Diagram (DATI/DATO)



- NOTES:
- REGISTER 1 - COMMAND REGISTER (MTRC)
 - REGISTER 2 - BYTE/RECORD COUNTER (MTRC)
 - REGISTER 3 - CURRENT MEMORY ADDRESS REGISTER (MTRM)
 - REGISTER 4 - DATA BUFFER REGISTER (MTRD)
 - REGISTER 5 - READ LINES REGISTER (MTRD)
2. Designations in parentheses refer to components containing corresponding tag 2.



- NOTE:
1. Designation in parenthesis refer to engineering drawings containing corresponding logic.
 2. See SPR read for processor read of data buffer (register 4).
 3. Maintenance use only.

11-1124

Figure 6-14 Processor In (DATA) Block Diagram

6.6.2 Operation Start (Figure 6-15 and 6-16)

6.6.2.1 Basic Sequence - When the command register CO bit is set by the processor a command start sequence is initiated. GO BIT (1) resets the CU ready bit in the command register indicating that the TMBII is processing a command. If the tape transport is not rewinding and TUR is true, GO BIT (1) triggers the GO strobe 1 one-shot. If the tape transport is rewinding (RWS true) GO BIT (1) will not trigger the one-shot due to the "0" output from the transport rewinding flip-flop. When the rewind is complete, TUR asserts resetting the rewinding flip-flop thereby triggering the GO strobe 1 one-shot. The GO STROBE 1 output of the one-shot resets the request store flip-flop and if SRLR is true, the "0" output of the request store flip-flop triggers the GO strobe 2 one-shot. When GO STROBE 2 (1) asserts, the following occurs:

1. SET is asserted to the tape transport if there is no illegal command and if the function is not REWIND or SPACE REV while the tape transport is at BOT (REV BOT false).
2. The GO flip-flop is reset and the request store flip-flop is set in preparation for another GO command from the processor.
3. The trailing edge of GO STROBE 2 (1) resets the CUR delay flip-flop. CUR DEL (1) is negated indicating to the error logic and the done logic that a transport operation is now in progress.

6.6.2.2 Time Out - If the transport is not selected or is not on-line (SELR false), the output of the request store flip-flop will not trigger the GO strobe 2 one-shot. In this case, GO BIT (1) initiates a 28 μ s delay after which TIME OUT (1) asserts and triggers the GO strobe 2 one-shot. The assertion of GO STROBE 2 (1) while SELR is negated causes the assertion of SET ILC and ILC (Paragraph 6.6.7) which respectively inhibit the assertion of SET to the transport and initiates a done sequence (Paragraph 6.6.6).

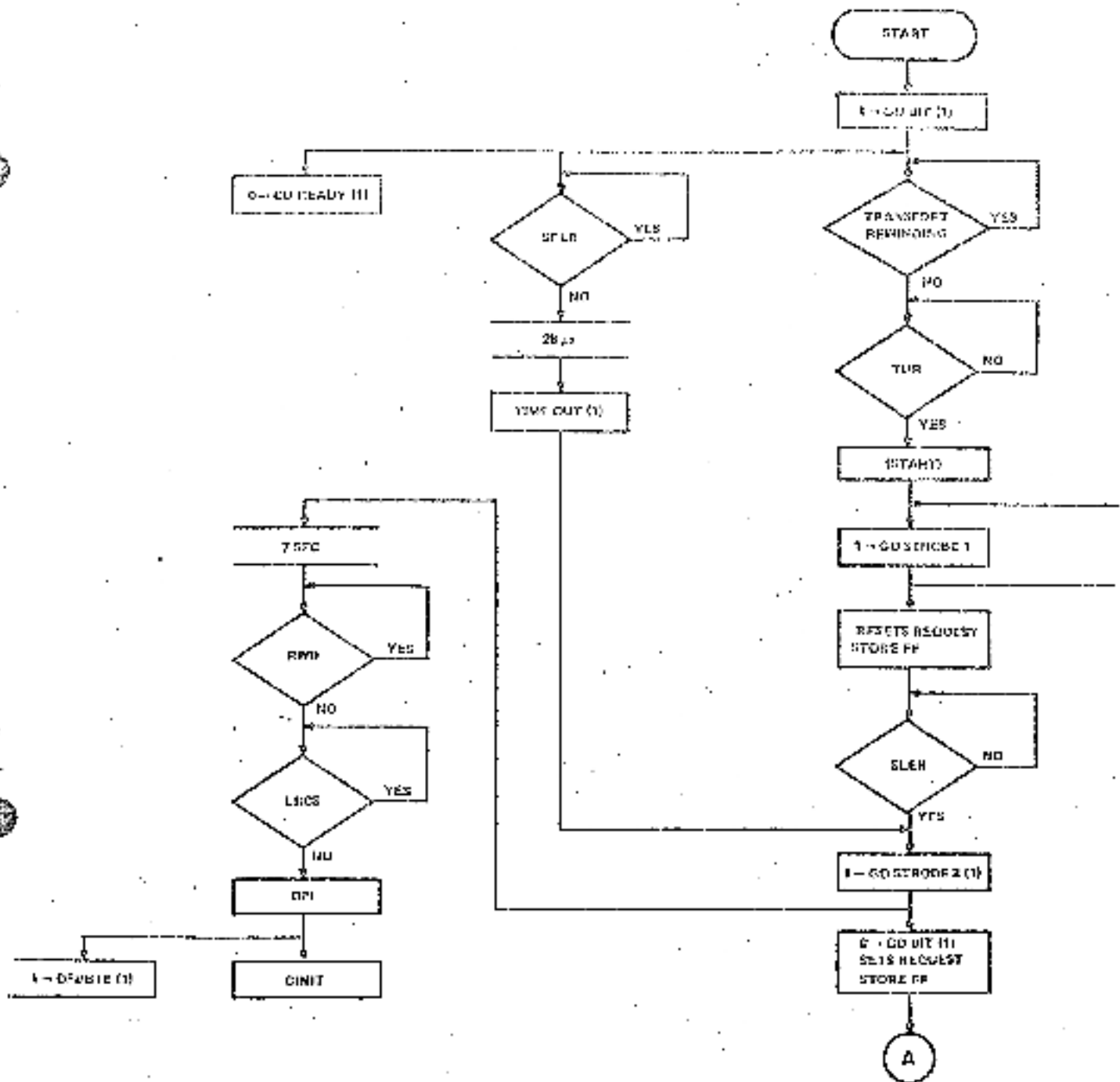
6.6.2.3 Restart - If the system is performing a spacing operation, either forward or reverse, the tape will space through records without coming to a stop at each interrecord gap.

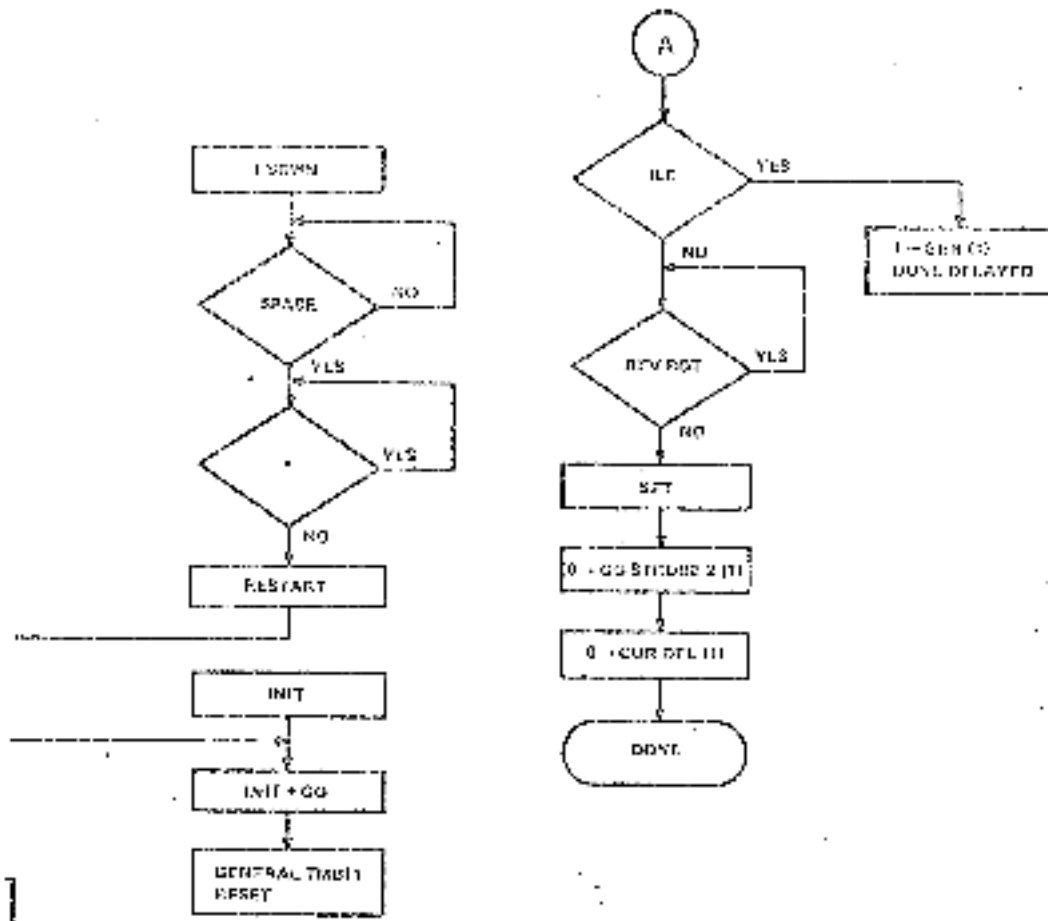
In this case the SET commands required by the transport are generated by RESTART which triggers the GO STROBE 1 one-shot without the necessity of TUR being true. RESTART asserts in the SPACE mode of operation each time SDWN is sensed and the following errors are false: BTE, BCL, NXM, ILC (1), OVERFLOW (1), EOFF (1), and BOT.

6.6.2.4 OPI/BTE - When GO STROBE 2 (1) asserts, a 7-second delay is initiated. If the 7-second time period elapses before an LRCS terminating strobe occurs, OPI is asserted indicating an operation incomplete error. OPI asserts the OPI/BTE bit in the status register and also CINIT to the tape transport resetting the transport logic circuits. The 7-second delay sequence is inhibited during a rewind operation (RWD true) as rewinding the tape could exceed 7 seconds.

6.6.2.5 Initialize - GO STROBE 1 (or an INIT from the processor) asserts INIT + GO which causes a general reset of the TMBII logic circuits. A general reset of the tape transport is caused by CINIT which is asserted by any of the following conditions:

1. The processor asserts INIT.
2. BOT is reached during a space reverse operation.
3. OPI is asserted.



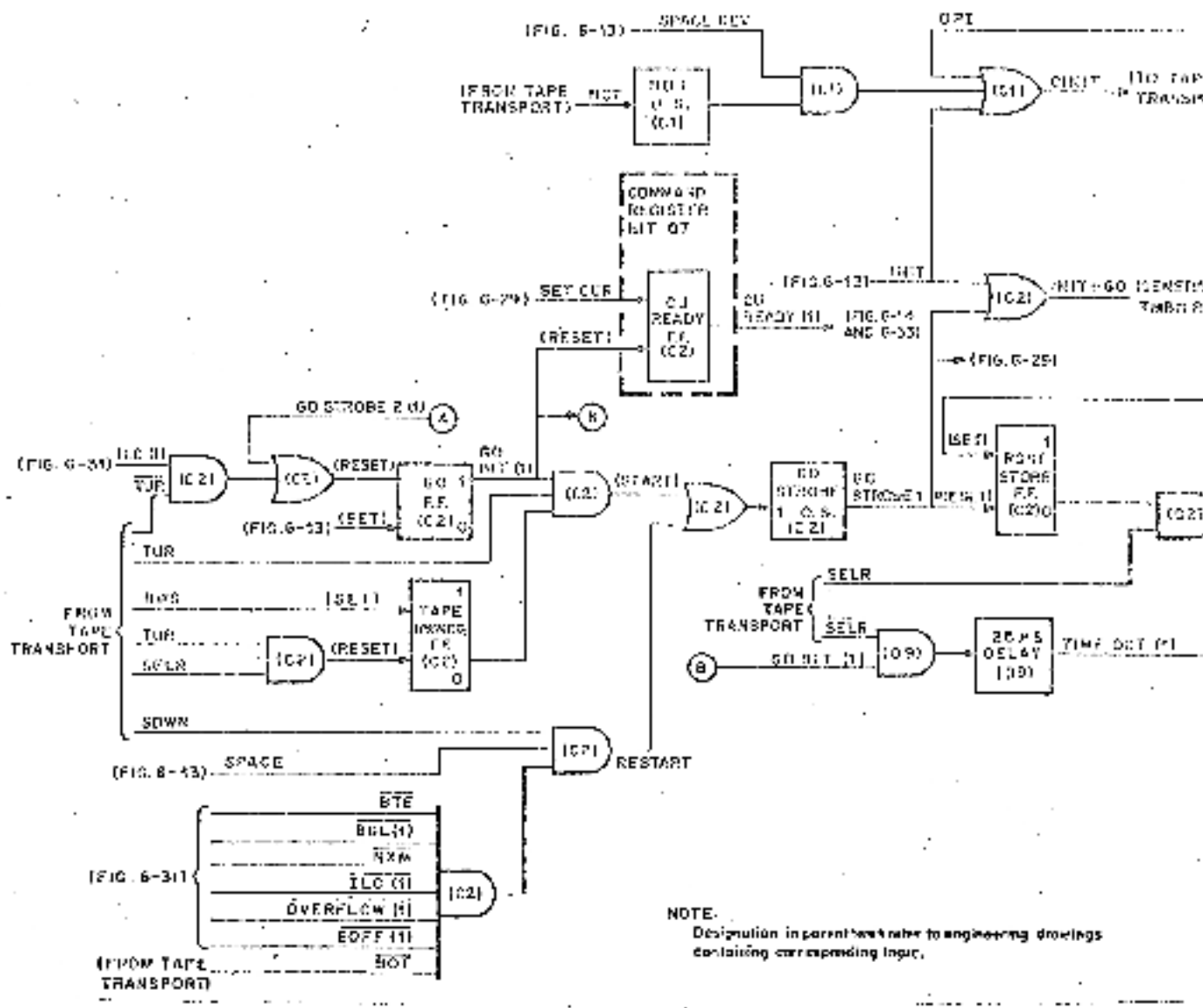


- Any one of the following:
 HTF
 DGL (I)
 N2M
 ILC (I)
 OVERFLOW (I)
 EOFF (I)
 ROT

11-4-59

Figure 6-15 Operation Start Flow Diagram

6-350



6.6.3 NPR Bus Cycle (Figures 6-17 and 6-18)

6.6.3.1 Basic Sequence -- An NPR bus cycle is initiated via the NPR request logic. The request logic generates NPR ENB (1) (2).

1. No inhibiting condition exists.
2. The logic is enabled.
3. NPR SET is asserted.

The request logic is inhibited if OVERFLOW (1) is true (the desired number of data records have already been transferred), BGL or NXM is true from the last NPR request, or CRCS or LRCS are asserted (CRC and LRC characters are not transferred to memory). The request logic is enabled by EVEN CHAR STB which is always high in normal 7-track or 9-track modes but only high during even character transfers in core dump mode. Thus in core dump, two characters are read from (or written onto) tape for each NPR bus cycle.

The request logic is set by read strobes or write strobes (RDS + WRS) from the tape transport. If a write operation is being executed (WRITE DATA ENB true) GO STROBE 2 (1) triggers the first NPR bus cycle as the first write strobe is not generated until the first character is written on tape.

The request logic asserts NPR ENB (1) to the Unibus NPR acquisition logic which requests control of the Unibus by asserting BUS NPR. When the processor responds with BUS NPG IN the acquisition logic asserts BUS SACK and the processor responds by negating BUS NPG IN. The acquisition logic checks for BUS BBSY true (by some other device) and if it finds the bus free asserts BUS BBSY (indicating bus mastership) and NPR MASTER to enable the NPR master logic.

When the NPR master logic is enabled the following actions occur.

1. ADRS → BUS becomes true and gates the address register and the two extended address bits of the command register to the Unibus as BUS A00 - A17.
2. BUS C0 - C1 is gated to the Unibus. If a read operation is to occur, READ is true and BUS C0 - C1 are high. If a write operation is commanded, READ is false and BUS C0 - C1 are low.
3. If the transfer is a read operation, DATA → BUS is asserted and gates the character in the data buffer out to the Unibus.
4. Another output from the master logic undergoes a 150 ns delay (to allow for deskewing on the Unibus address lines) and then sets the MSYN logic circuit.

The MSYN logic asserts BUS MSYN to the slave device which then returns BUS SSYN to the TMB11. BUS SSYN becomes SSYN and is applied to the read and write termination circuits. If a read operation is being performed the read termination circuit asserts an input to the termination OR logic. If a write operation is being performed (READ false) the write termination circuit asserts DATA STB 1 which undergoes a 150 ns delay (for input data deskewing) and then becomes DATA STB 2. DATA STB 2 loads the data buffer with the input character that is to be written on tape. DATA STB 2 also asserts an input to the terminator OR logic. The asserted output of the OR logic is delayed 75 ns (for data deskewing into the data buffer) and then triggers the NPR clear logic.

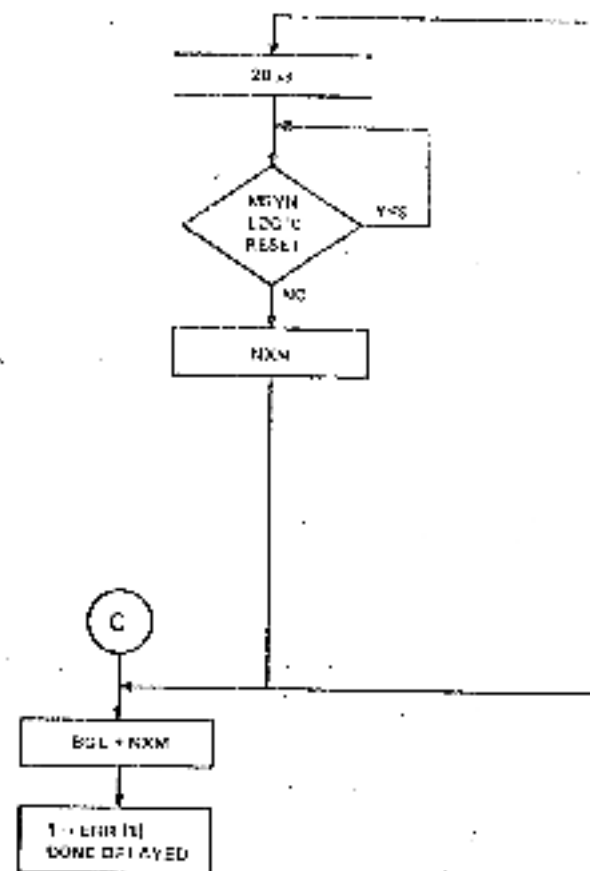
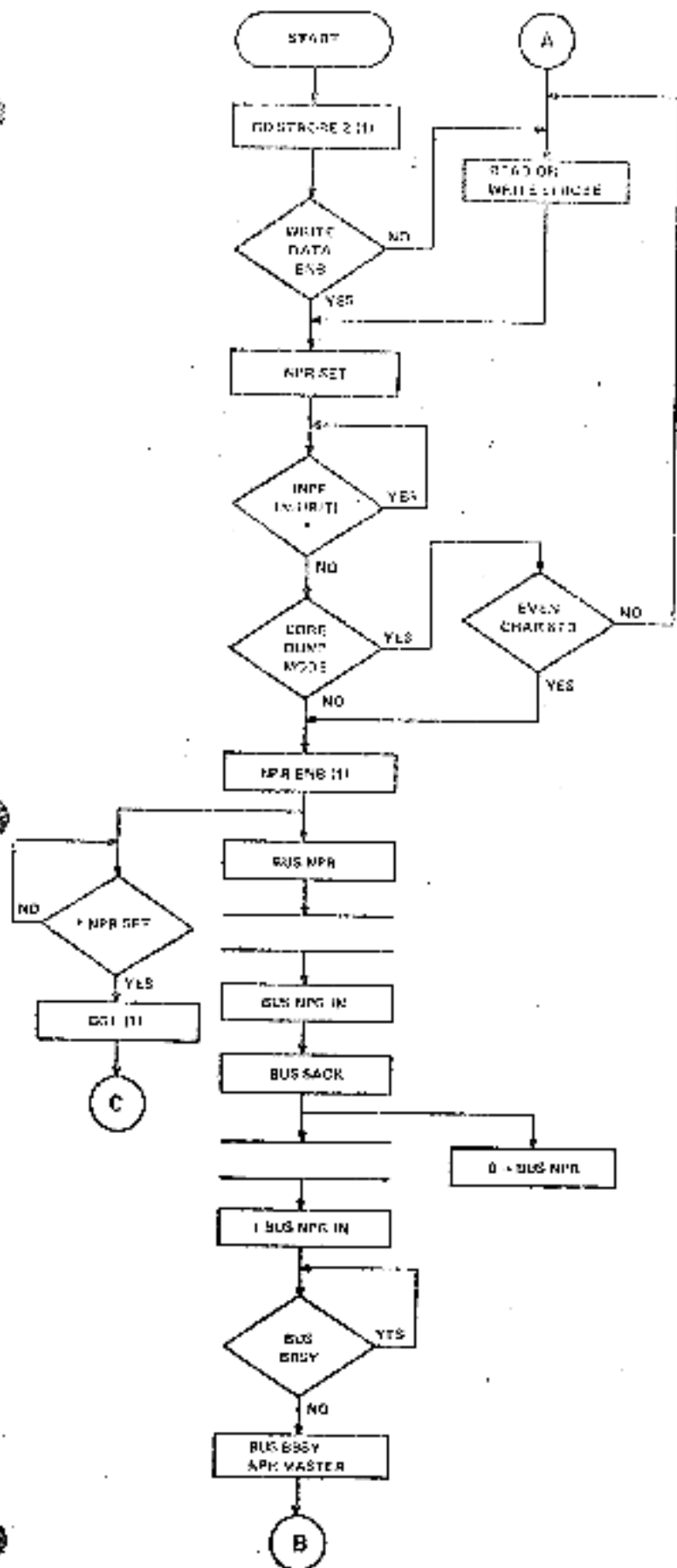
The NPR clear logic asserts NPR CLR BBSY which resets the NPR request logic and increments the bus address register and the byte/record counter for the next character transfer. If a spacing operation is in progress the byte/record counter is incremented by LRCSID and no bus cycle is involved.

6.6.3.2 Bus Grant Late (BGL) and Nonexistent Memory (NXM) - When NPR ENB (1) is asserted the bus grant flip-flop is conditioned to set. If another NPR SE1 is asserted to the NPR request logic before the logic is reset, the bus grant late flip-flop will set asserting BGL (1) which in turn asserts BGL + NXM to the error logic.

If the MSYN logic is not reset within 20 μ s after being set, NXM asserts and terminates the bus cycle by asserting the termination DR logic output, NXM also asserts BGL + NXM to the error logic.

6.6.3.3 BUS NPG OUT - An NPG from the processor is passed from one system device to another in daisy-chain fashion until it reaches the device that issued the BUS NPR. A BUS NPG IN received by the TMB11 is gated back to the Unibus as BUS NPG OUT under either of the following conditions:

1. NPR MASTER is true (TMB11 is presently bus master), or
2. NPR ENB is false (TMB11 did not issue the BUS NPR that caused the BUS NPG IN).



Any one of the following OVERFLOW (1)
 BGL (H)
 NXN
 CHLS
 LRES

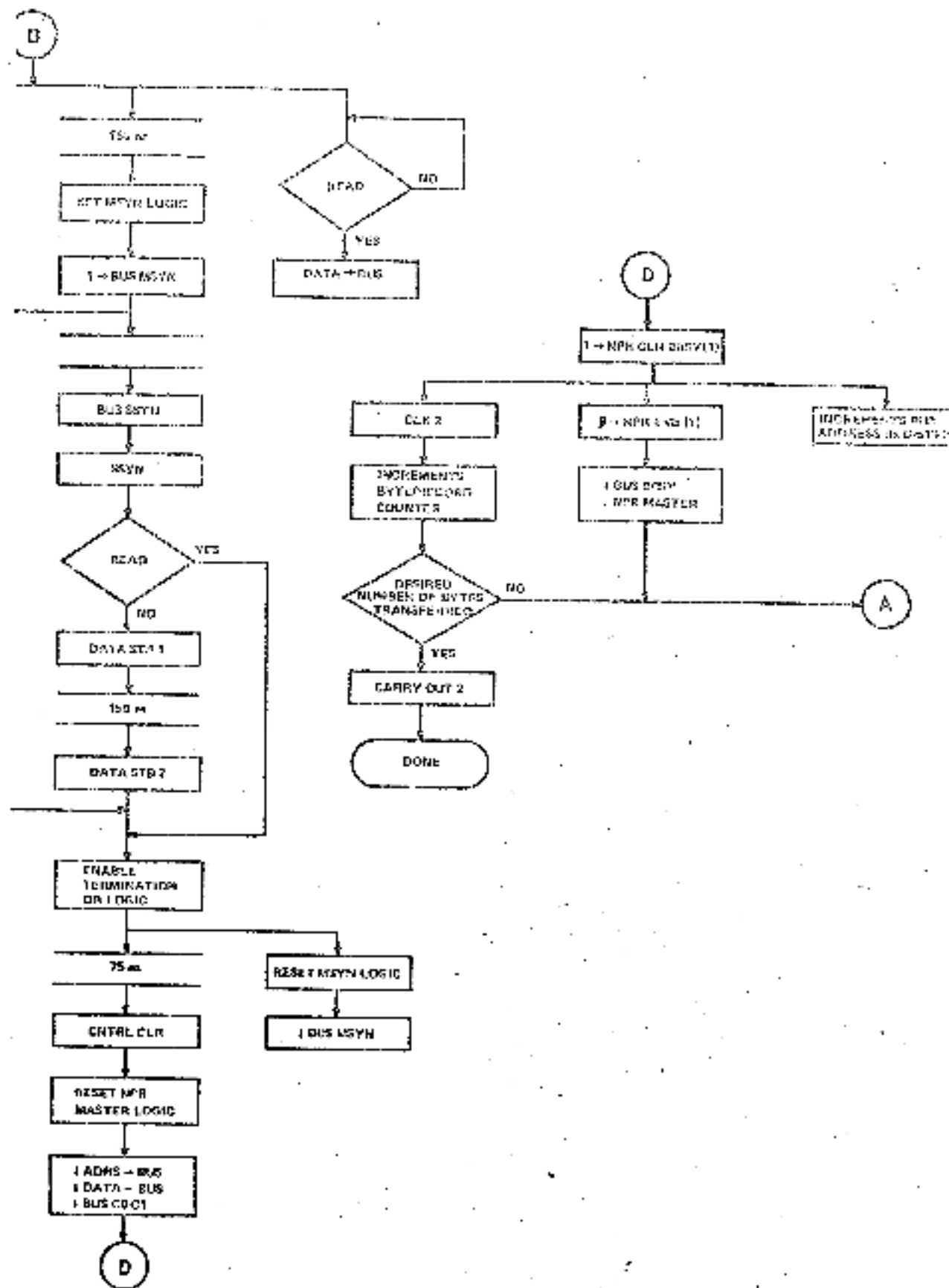
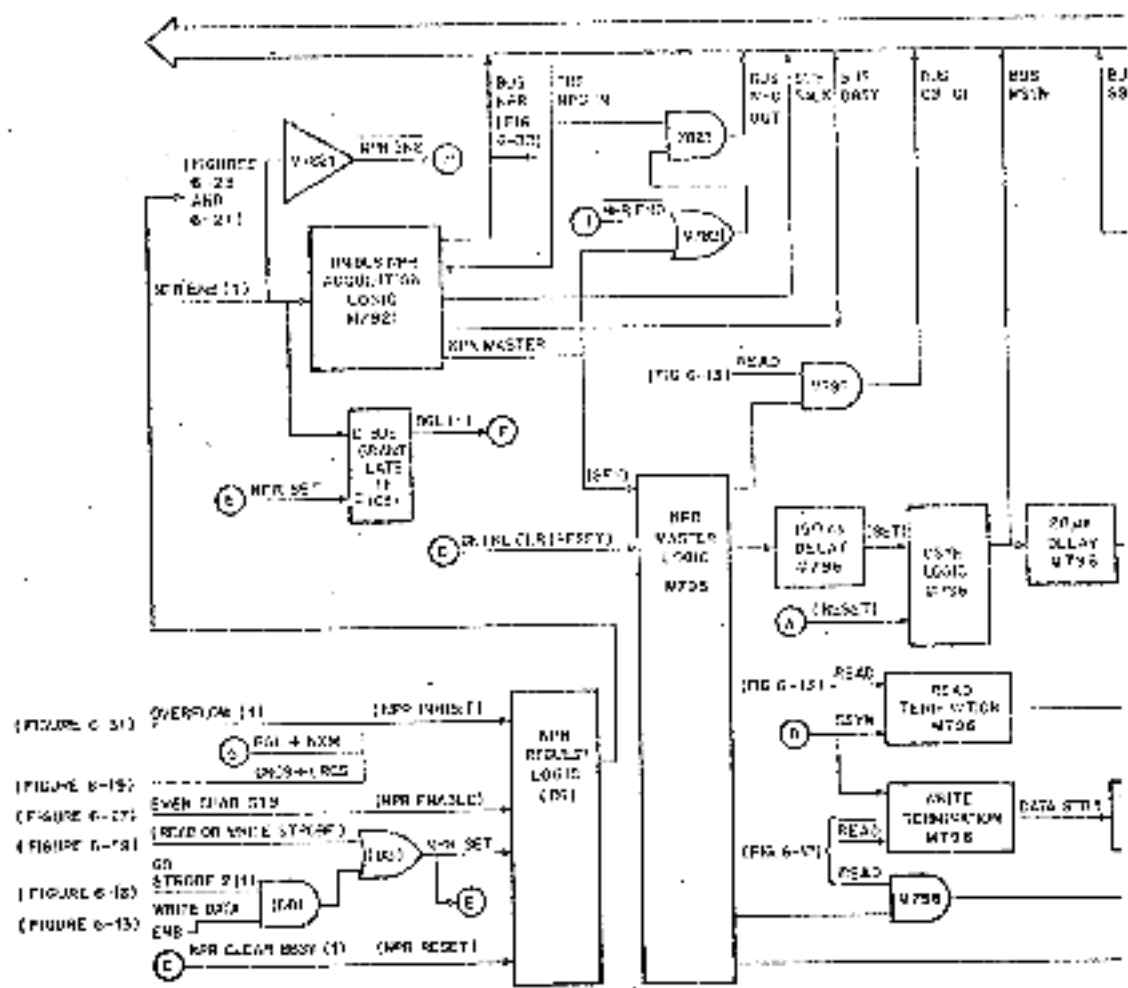


Figure 6-17 NPR Bus Cycle Flow Diagram



The 7-track operation is identical to the 9-track operation, except that the buffer input gate C is inhibited. (See Table 6-5.) Consequently CHAN 6-7 are not loaded into the data buffer and there is no data on buffer output lines DATA BFR OUT BIT 6-7, or on Unibus driver input lines D BIT 06-07 (low data byte) and D BIT 14-15 (high data byte).

Table 6-5 Data Multiplexing in 9-Track, 7-Track Normal, and Core Dump Modes

Mode of Operation	Enabled Gates	Channel Bits From Transport	DATA BFR OUT BITS From Data Buffer	Number of Output Bits per Data Cycle
9-Channel	A B C	CHAN 0-3 CHAN 4-5 CHAN 6-7	0-3 4-5 6-7	8
7-Channel (Normal)	A B	CHAN 0-3 CHAN 4-5	0-3 4-5	6
7-Channel (Core Dump)	First Cycle	CHAN 0-3	0-3	4
	Second Cycle	CHAN 0-3	4-7	4

6.6.4.3 Core Dump Operation (Figures 6-22 and 6-23) - Core dump operation can be implemented only in the 7-track mode, thus both 7 CH and CORE DUMP are true throughout this discussion.

When the first character is received from the transport, READ STB sets the select read flip-flop, SEL READ DATA becomes true, and gates A and D are enabled. CHAN 0-3 are passed through both gates to become DATA BFR IN BIT 0-3 and DATA BFR IN BIT 4-7 into the data buffer. The input READ STB asserts DATA BFR STB 1 (via the even character strobe logic) and DATA BFR STB 2 thereby loading both halves of the data buffer with the same character. The second character received from the transport triggers the same sequence except no read strobe is issued from the even character strobe logic and DATA BFR STB 1 is not asserted. DATA BFR STB 2 is asserted and loads bit 4-7 of the data buffer with the second tape character. (See Table 6-5.) The read strobe associated with the second character initiates an NPR bus cycle causing DATA - BUS to go true and gate the contents of the data buffer out to the Unibus. Thus, NPR bus cycles are initiated after each even numbered character is read from tape thereby allowing the two characters to be assembled into a byte in the data buffer before being gated out to the Unibus.

6.6.4.4 Processor Read (Figure 6-23) - During a processor read of the data buffer SEL 4 IN asserts both HI DATA BYTE and LO DATA BYTE. The latter gates the 7 bits of the data buffer to the Unibus while the former serves to gate D BIT 08 IN to D BIT 08 on the Unibus. During a processor read (NPR ENH false) D BIT 08 IN reflects the state of the parity flip-flop as determined by the parity bit of the LRC character.

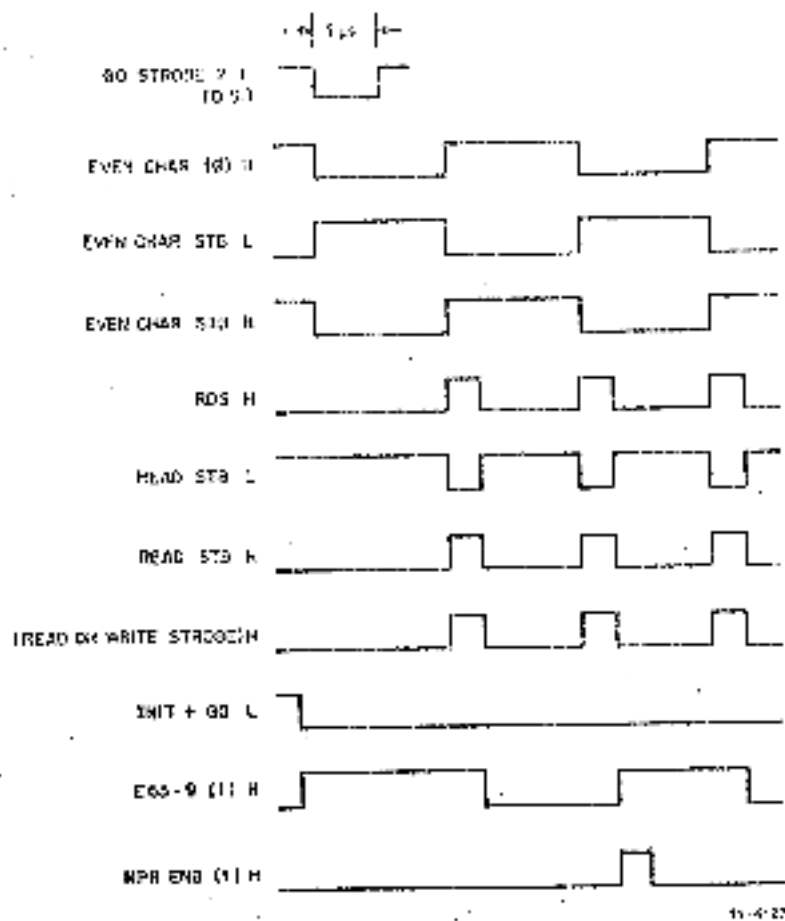
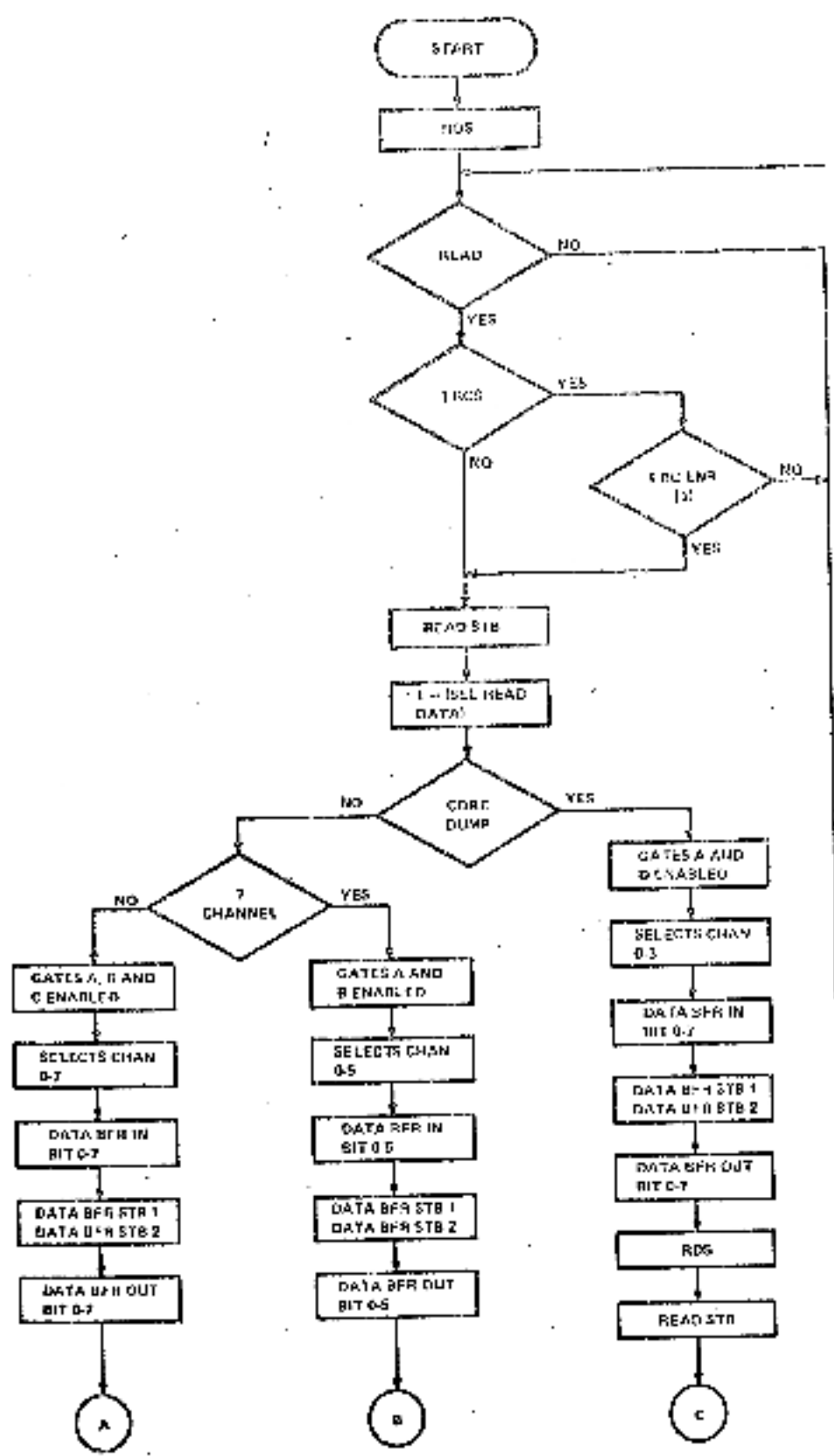
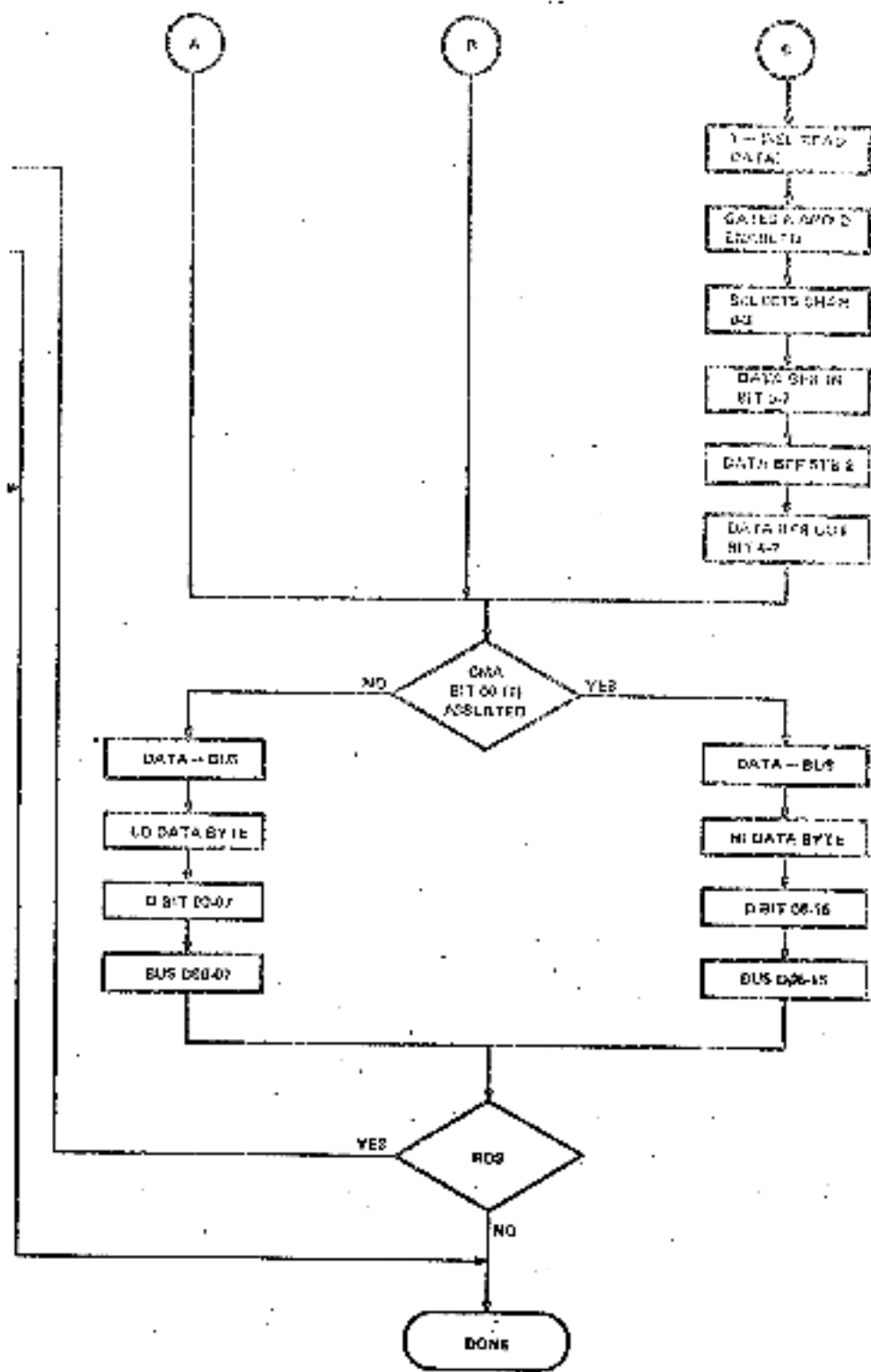


Figure 6-21 Even Character Strobe Timing Diagram



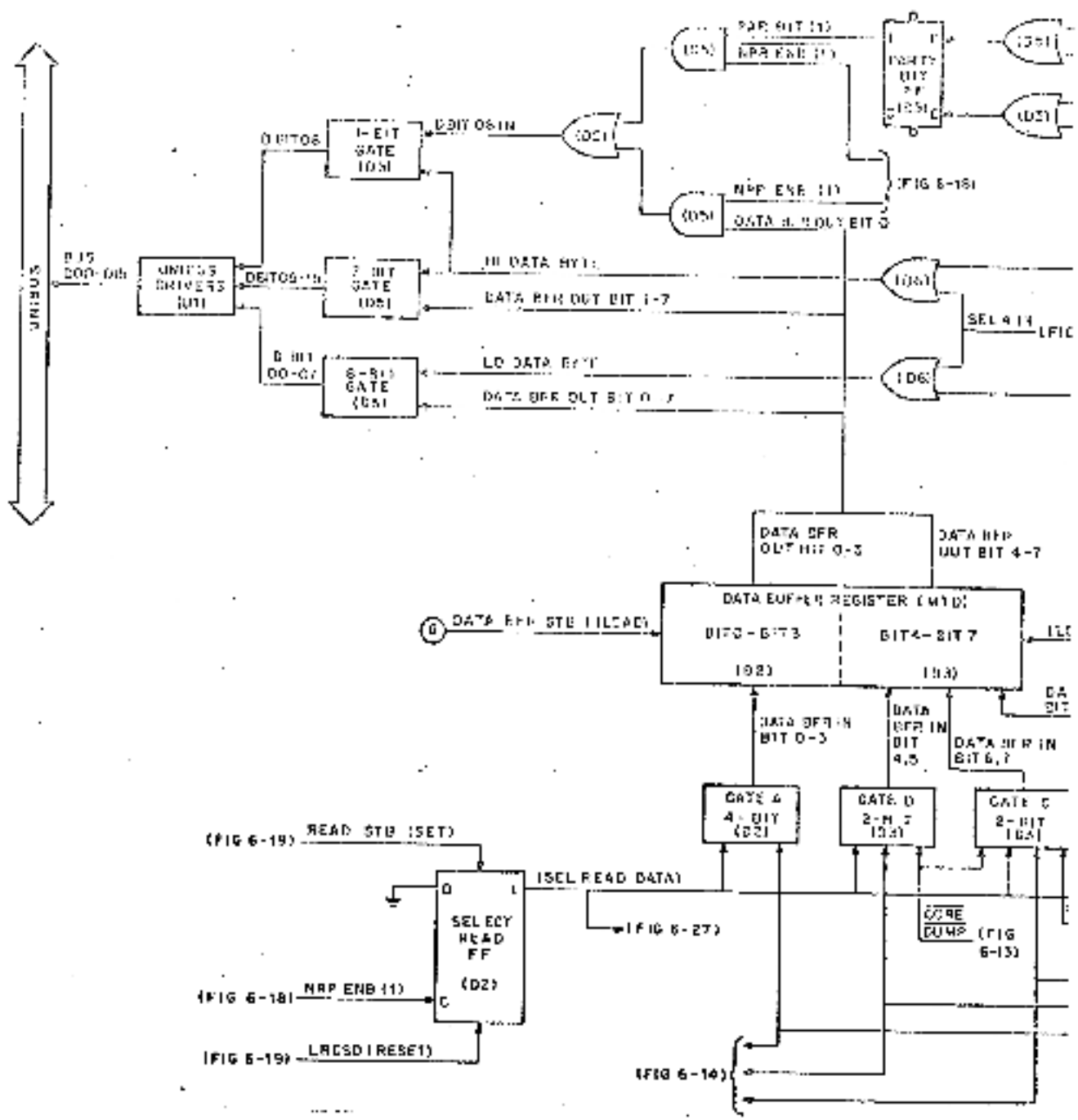
649

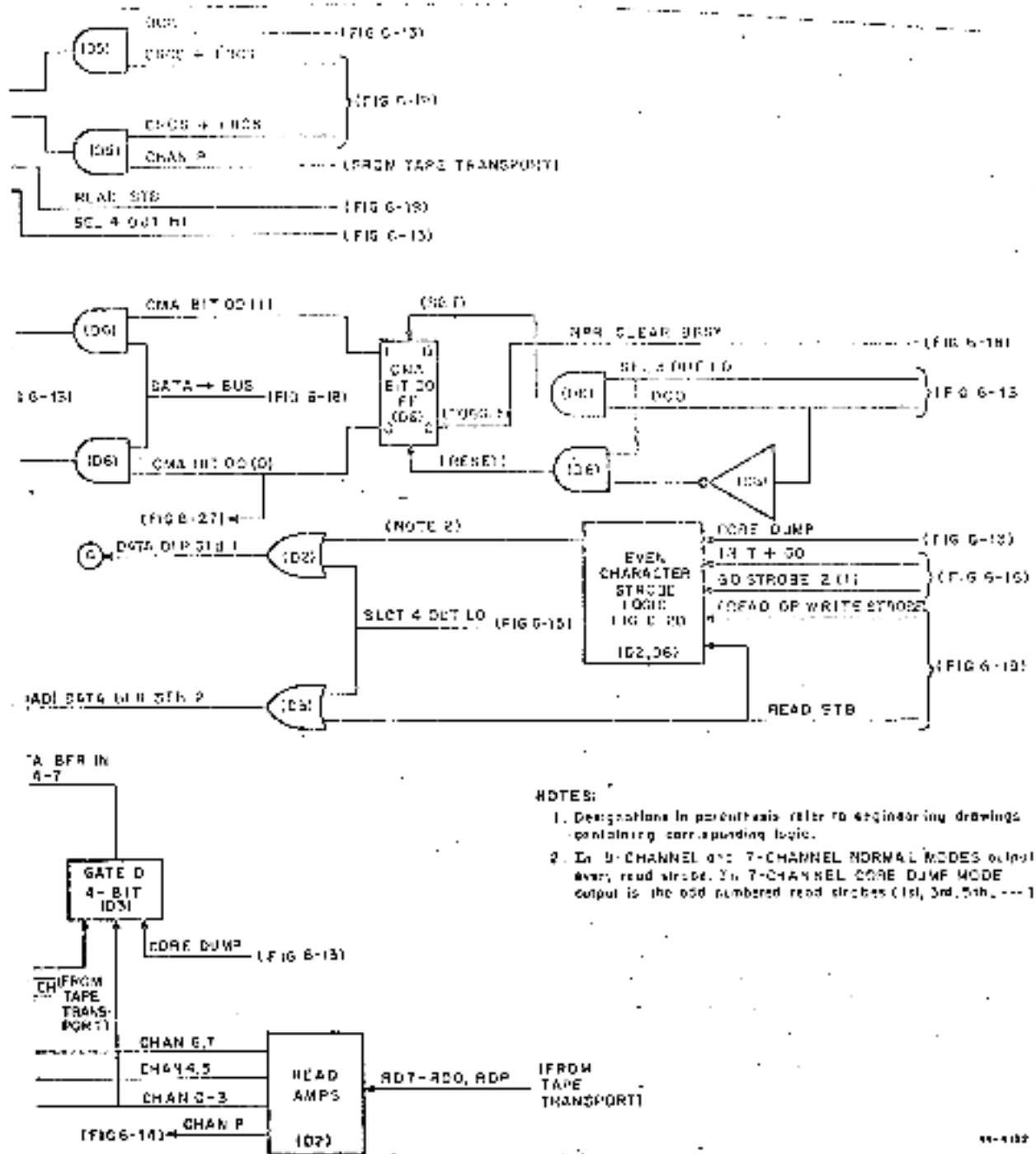


11-4143

Figure 6-22 NPR Read (DATO) Flow Diagram

6-49a





- NOTES:
1. Designations in parenthesis refer to engineering drawings containing corresponding logic.
 2. In 9-CHANNEL and 7-CHANNEL NORMAL MODES output is every read stroke. In 7-CHANNEL CORE DUMP MODE output is the odd numbered read strokes (1st, 3rd, 5th, ...)

Figure 6-23 NPR Read (DATO) Block Diagram

6.6.5 NPR Write (DATA) (Figures 6-26 and 6-27)

6.6.5.1 9-Track and 7-Track Normal Operation An NPR request must be made (NPR ENB true) before a write operation (READ false) can be initiated. With NPR ENB true and READ false either SEL 10 BYTE WRITE DATA or SEL 111 BYTE WRITE DATA asserts to gate respectively D00-D07 or D08-D15 from the Unibus to the input of the data buffer. The state of bit 00 in the current memory address register determines whether the high byte or the low byte is gated to the buffer. During the write NPR bus cycle DATA STB 2 is asserted (Paragraph 6.6.3.1) and asserts DATA BFR STB 1, 2 which loads the data buffer with the selected input byte. DATA BFR OUT BIT 0-7 is now available to gates A, B, C, and D. In 9-track operation gates B, C, and D are enabled gating DATA BFR OUT BIT 0-7 to the tape transport as WD7-WD0. (Note the reversal in the bit/track numbering sequence at the write gate outputs.) The 7-track normal write data sequence is identical to the 9-track sequence except that write gate D is inhibited. Thus DATA BFR OUT BIT 0-5 are gated to the transport as WD7-WD2. Table 6-6 summarizes the gating action for all modes of operation.

Table 6-6 Write Data Gating for 9-Track, 7-Track Normal and Core Dump Modes

Mode	Enabled Write Gates	DATA BFR OUT BITS From Data Buffer	Write Data To Transport Register	Number of Input Bits per Data Cycle
9-Track	B C D	0-3 4-5 6-7	WD7-WD4 WD3-WD2 WD1-WD0	8
7-Track (Normal)	B C	0-3 4-5	WD7-WD4 WD3-WD2	6
7-Track (Core Dump)	First Cycle	B	WD7-WD4	4
	Second Cycle	A	WD7-WD4	4

6.6.5.2 Core Dump Operation - Core dump operation is identical to 9-track and 7-track normal operation with regard to the input gating and loading of the data buffer. The difference is that only write gates A and B are enabled and they are alternated by EVEN CHAR STB so when one gate is on the other is off. With CORE DUMP true, the even character strobe logic is enabled and EVEN CHAR STB is a square wave with its alternations switched by write strobes. (See Paragraph 6.6.4.5.)

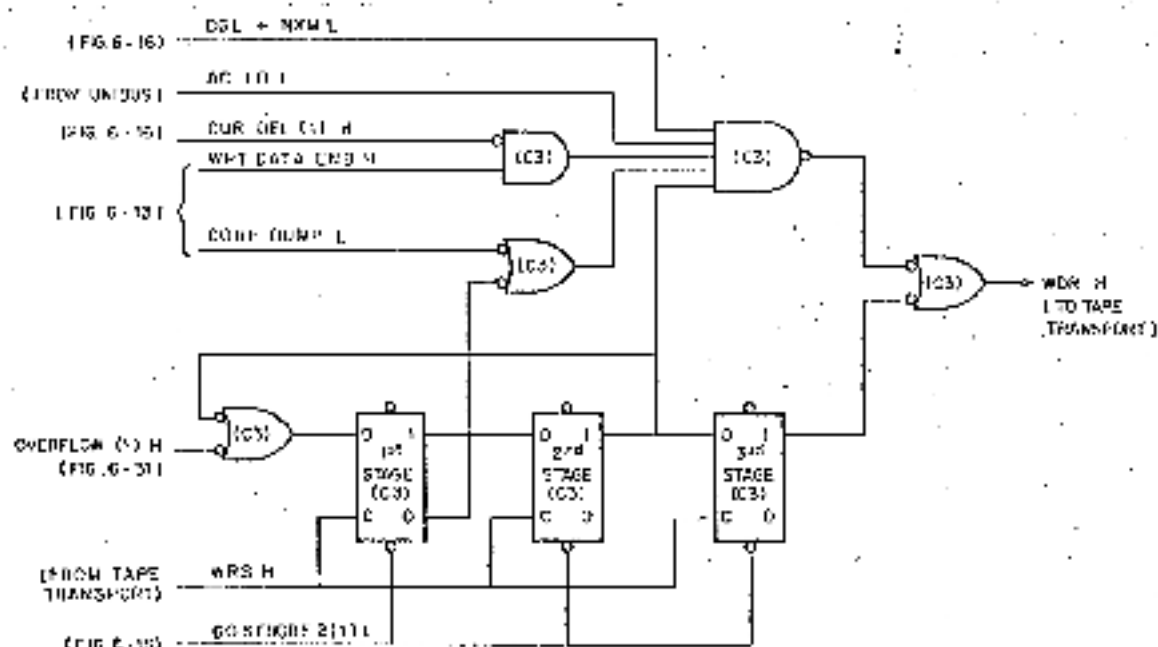
A sequence is started by GO STROBE 2 (1) which sets EVEN CHAR STB to a high level and triggers the first NPR write bus cycle. DATA STB 2 asserts during the bus cycle asserting DATA BFR STB 1, 2 which loads the data byte into the buffer register. DATA BFR OUT BIT 0-3 is gated through gate B and passes into the tape transport as WD7-WD4. The first character is written on tape and the first write strobe is generated. The first write strobe sets EVEN CHAR STB to the low state thereby inhibiting gate B and enabling gate A which gates DATA BFR OUT BIT 4-7 to the transport as WD7-WD4 and the second character is written on tape. The low state of EVEN CHAR STB inhibits another NPR bus cycle. The second write strobe will set EVEN CHAR STB high enabling gate B once again and triggering the second NPR bus cycle. Thus, the even character strobe logic disassembles the input data byte into two 4-bit characters for the tape transport while inhibiting an NPR bus cycle on the odd numbered write strobes.

6.6.5.3 Processor Write - If a processor write is being executed, SEL READ DATA and NPR ENB (1) are false, thereby asserting SEL LO BYTE WRITE DATA and gating the low data byte from the Unibus to the buffer register. SELECT 4 OUT LO then asserts (Paragraph 6.6.1.1) in turn asserting DATA RPR STB 1, 2 which loads the buffer register with the input data.

6.6.5.4 Write Data Ready (Figures 6-24 and 6-25) - WDR to the tape transport must be true to enable the write logic within the transport. The write data ready logic supplies WDR to the transport, under the proper conditions, and assures a minimum record length of three characters in normal operation and four characters in core dump. Also during core dump, when OVERFLOW (1) occurs, indicating that the last character has been transferred to the controller, the logic holds WDR true for one more write strobe to allow the second half of the last data byte to be written on the tape.

WDR is asserted true by the third stage output of a 3-stage counter or by the asserted output of a 5-input AND gate. When a write operation is initiated GO STROBE 2 (1) L is asserted and resets the counter. The third stage output of the counter asserts WDR via the OR gate. OVERFLOW (1) H is false, thereby conditioning the first stage of the counter to set. The first three write strobes set the counter stages in order. The third write strobe sets the third stage causing its output to the OR gate to assert high; however, the AND gate is now enabled and holds WDR true. Note that WDR is held true for three write strobes regardless of the state of OVERFLOW (1) H.

When the desired number of characters have been transferred to tape, OVERFLOW (1) H goes true, conditioning the first stage of the counter to reset. The next WRS strobe resets the first stage inhibiting the AND gate causing WDR to go false. If CORE DUMP L is asserted the AND gate will not be inhibited until the next WRS strobe when the second stage is reset. Thus, in core dump mode WDR is held true for one more write strobe after OVERFLOW (1) H asserts.



NOTE:
Designations in parenthesis refer to engineering drawings containing corresponding logic.

11-4187

Figure 6-24 Write Data Ready Logic Diagram

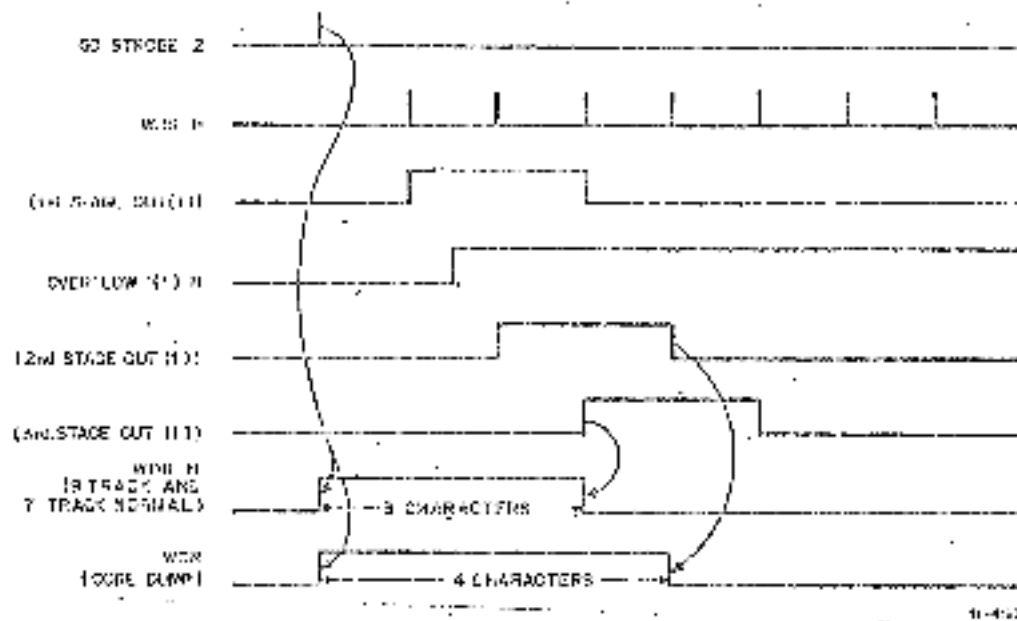
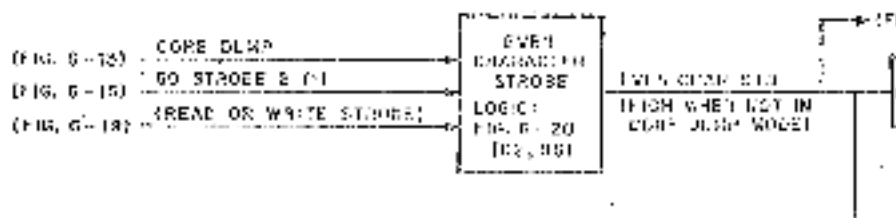
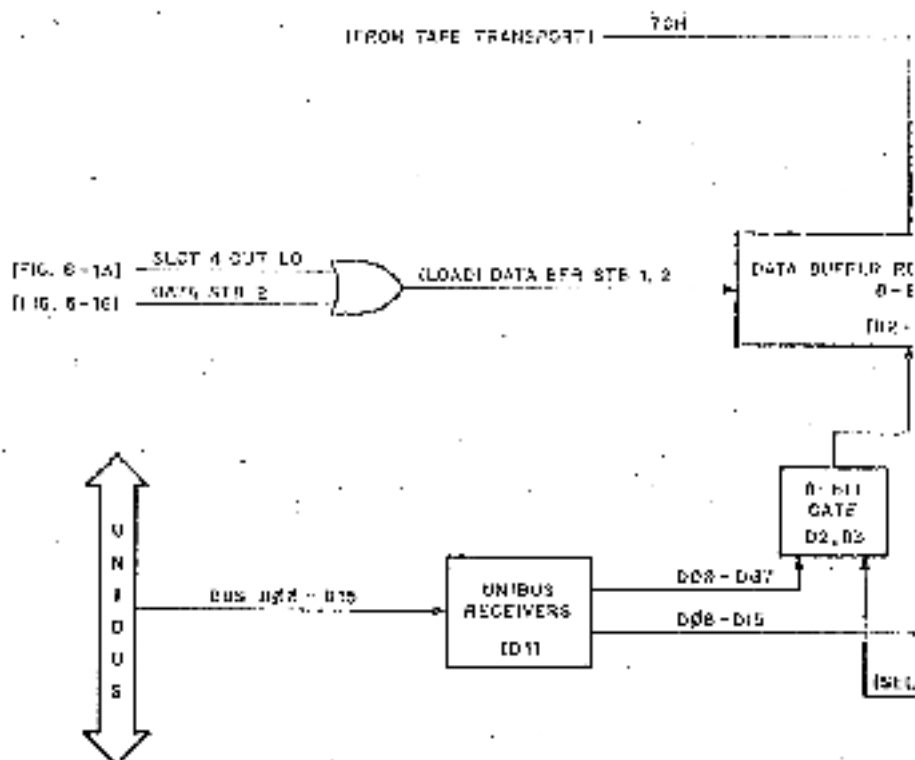


Figure 6-25 Write Data Ready Timing Diagram

Due to feedback from the second counter stage to the first, two write strobes must occur (to set the second stage) before the first stage can be reset. Consider the case where OVERFLOW (1) H asserts after the first or second write strobe (Figure 6-25). The first stage will reset on the third WRS which also sets the third stage. If, in core dump mode, the AND gate holds WDR true until the fourth WRS strobe which resets the second stage thereby negating WDR. Thus at least four write strobes are assured in core dump operation.



(FIGURE 6-13) CORE DUMP



NOTE

Designations in parenthesis refer to engineering drawings containing corresponding logic.

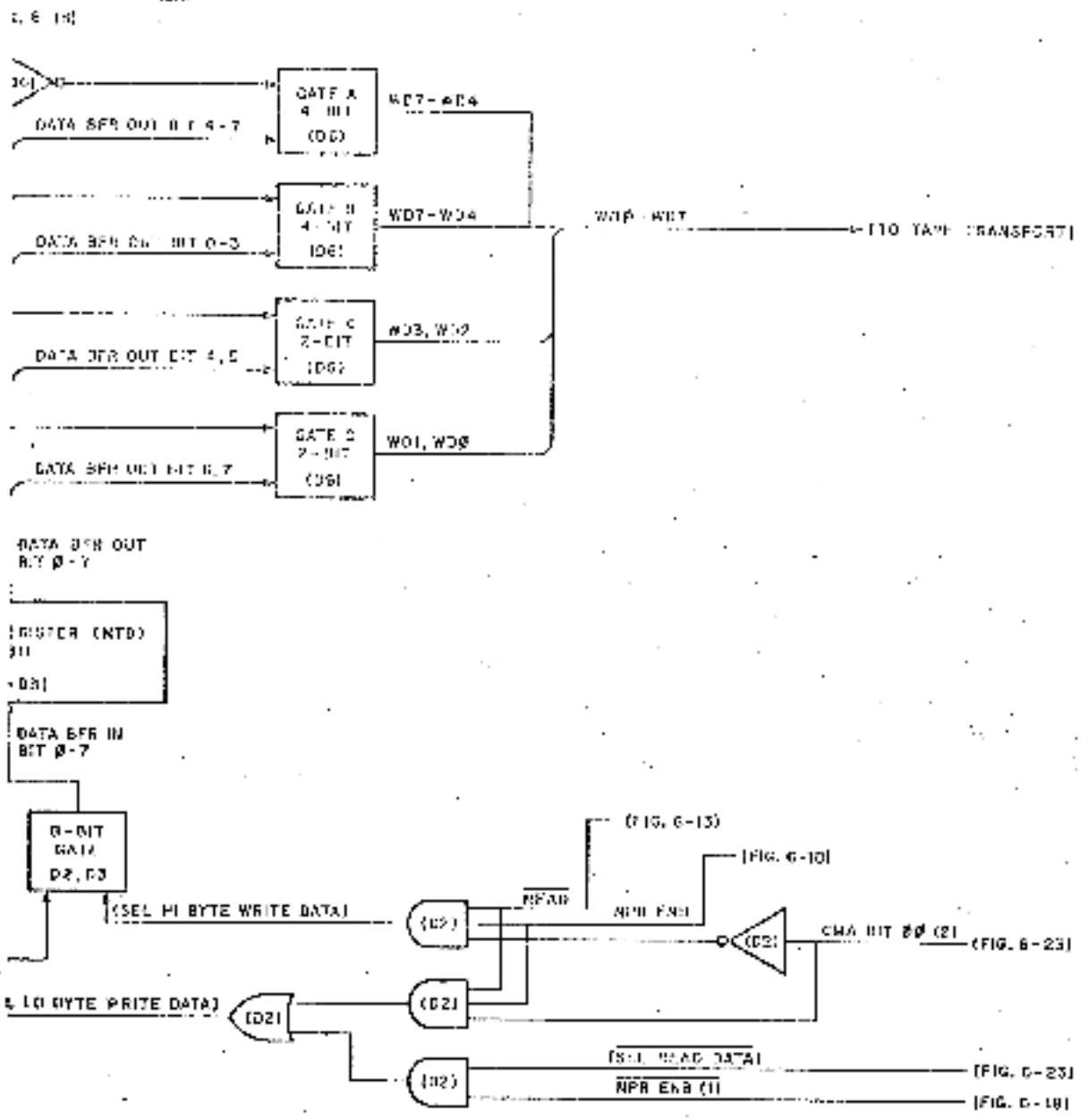


Figure 6-27 NPR Write (DAT)
Block Diagram

6.6.6 Done Logic (Figures 6-28 and 6-29)

The done logic senses the completion of an operation and functions to assert control unit ready (for another command) and issue an interrupt request to the interrupt logic.

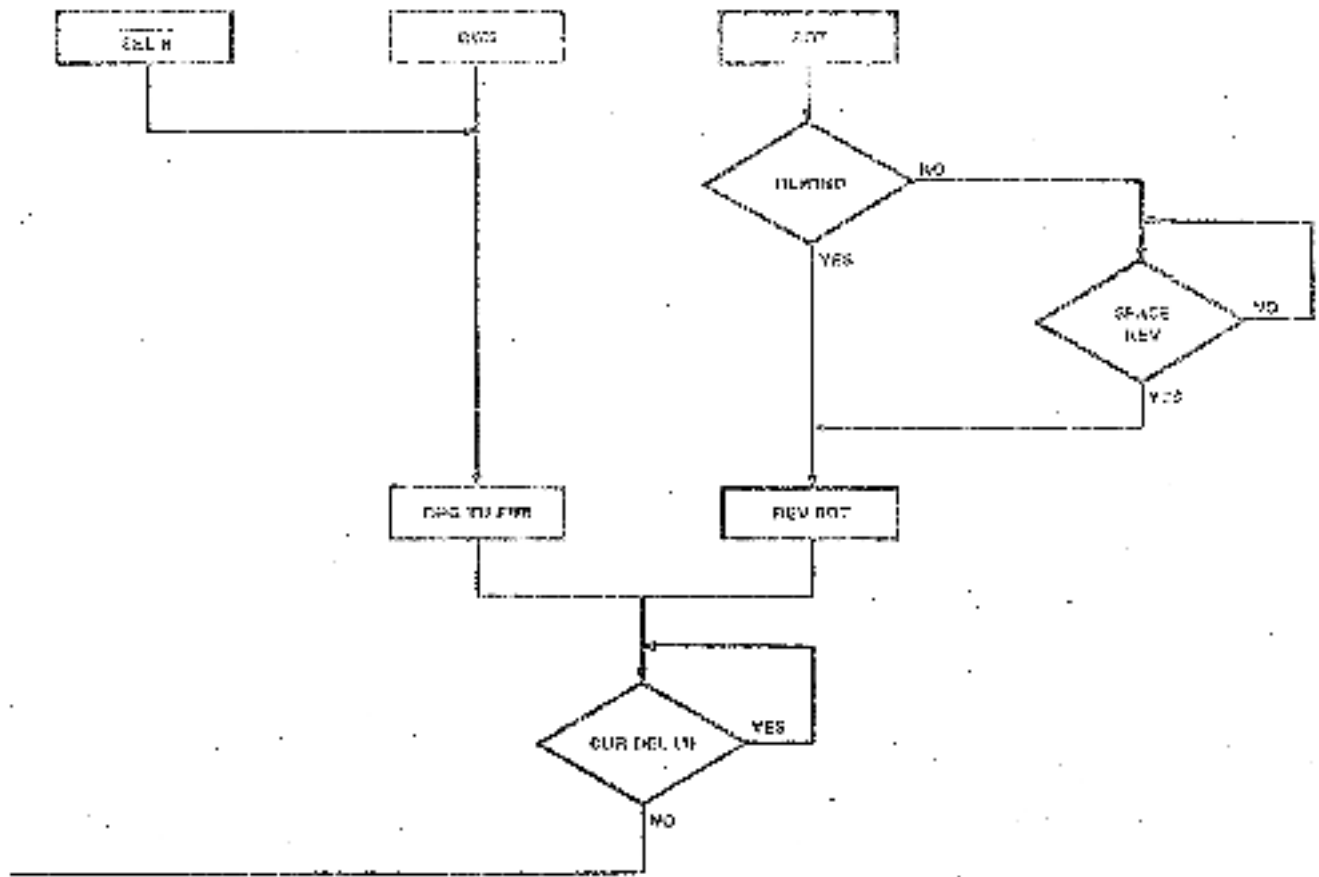
If a spacing operation was being executed CARRY OUT 2 signifies the completion of the operation by asserting when the desired number of records has been spaced over. If a read or write operation was being executed (SPACE false) the assertion of LRCSD signifies the operation is over.

In both cases the done flip-flop is set and DONE (1) is asserted. If ERR (1) asserts during the operation a done sequence will be triggered before the operation is completed. Certain errors will interrupt an operation by asserting ERR (1) as soon as they are detected. Other errors will allow the operation to terminate normally. (See Paragraph 6.6.7.)

When DONE (1) asserts and the tape transport comes to a stop (TUR true) DONE DELAYED (1) asserts in turn asserting (GET NEW CMD) to the bus interrupt logic and SET CUR to the operation start logic.

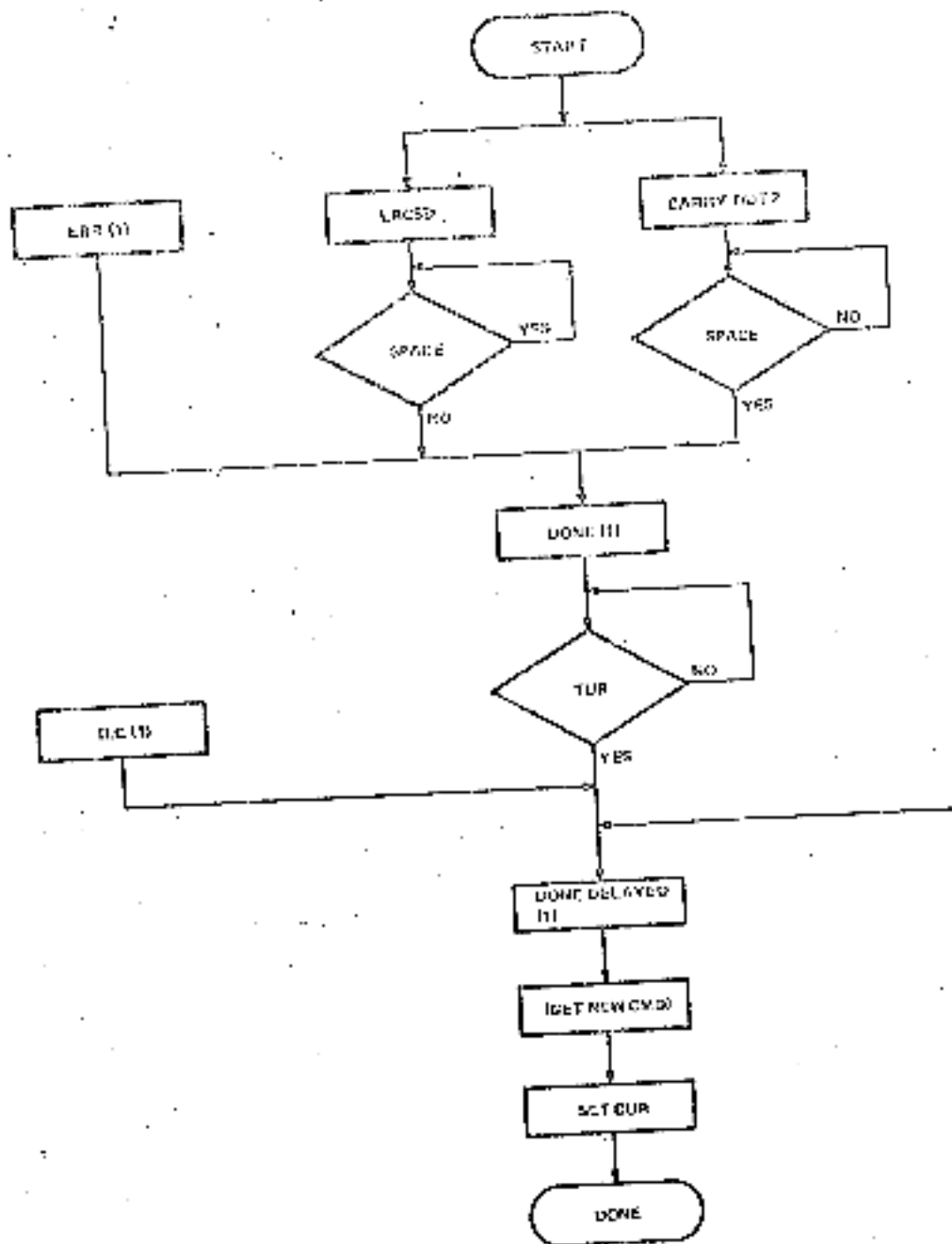
Some conditions that will assert DONE DELAYED (1) without waiting for TUR to come true are:

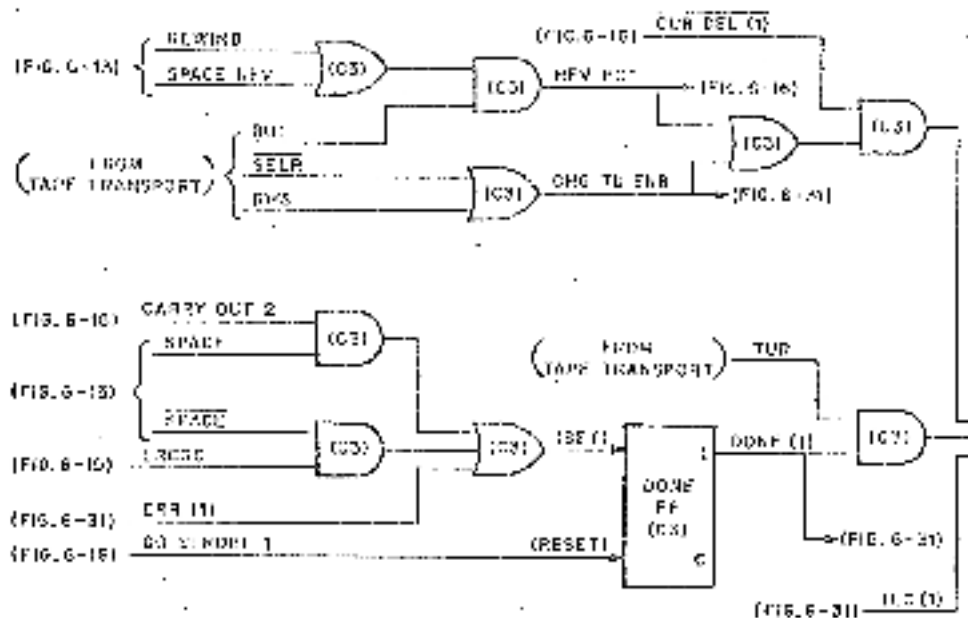
1. An illegal command [ILC (1)]
2. Reaching BOT during a space reverse operation.
3. Reaching BOT during a rewind operation that was commanded by the processor
4. Deselecting the drive
5. When the transport starts a rewind from a local command.



11-4142

Figure 6-28 Operation Done
Flow Diagram

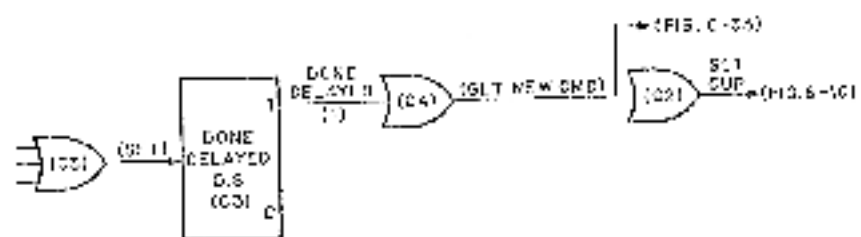




NOTE

Designations in parenthesis refer to engineering drawings containing corresponding logic.

6-65



11-4-23

Figure 6-29 Operation Done Block Diagram

6.6.7 Error Logic (Figures 6-30 and 6-31)

ERR (1) is asserted by any of the error conditions that could arise within the system. When ERR (1) comes true it sets bit 15 in the command register and triggers a done sequence. The error conditions that assert ERR (1) are in two classes: those that assert ERR (1) immediately and abort the current operation, and those that allow the operation to terminate normally. In the latter case ERR (1) will become true with the assertion of LRCS0.

Errors that abort an operation are:

NXM
BGL
ILC
BTE

Errors that allow an operation to terminate normally are:

RLE
CRE
PAE
EOFF
End of Tape Error

NXM and BGL are error conditions that arise from the execution of an NPR bus cycle.

ILC is asserted under the following circumstances:

- When the processor attempts to access the command register while the controller is busy executing a command (SEL 1 OUT asserted while CUR DEL 1 is false).
- When an on-line transport is deselected while an operation is being executed (SELK negates while OFF LINE and CUR DEL 1 are false).
- The controller attempts to initiate an operation on a deselected transport (GO STROBE 2 (1) asserts while SELR is false).
- The controller attempts to initiate a write operation on a write protected transport (GO STROBE 2 (1) asserts while WRITE ENB and WRL are true).

BTE is asserted when a read strobe occurs during the gap shutdown or settle down periods provided no BGL, NXM, or ILC errors exist. (RDS asserts when either SDWN or GSD is true and the following are false: BGL, NXM, ILC.) Gap shutdown is the period between the end of a record and the beginning of the settle down interval (from the assertion of LRCS to the assertion of SDWN).

RLE (1) is asserted when a read strobe occurs after an overflow condition has been sensed except if the read strobe is a CRC or an LRC strobe (READ STB asserts when OVERFLOW (1) is true and CRCS + LRCS is false).

CRE (1) is asserted during a read or a write operation when a read strobe occurs and a CRC error exists. (RDS asserts while CRCE and READ + WRITE are true.)

PAE (1) is asserted during a read or a write operation when a read strobe occurs and either a vertical parity error or a longitudinal redundancy check error exists. (RDS asserts while either VPE or LRCE is true and READ + WRITE is true.)

EOFF (1) is asserted when a file mark (FMK) is received from the tape transport.

An end-of-tape error is asserted when the end-of-tape marker is sensed during a transport operation other than rewind or space reverse (EOE asserts when REWIND and SPACE REV are false).

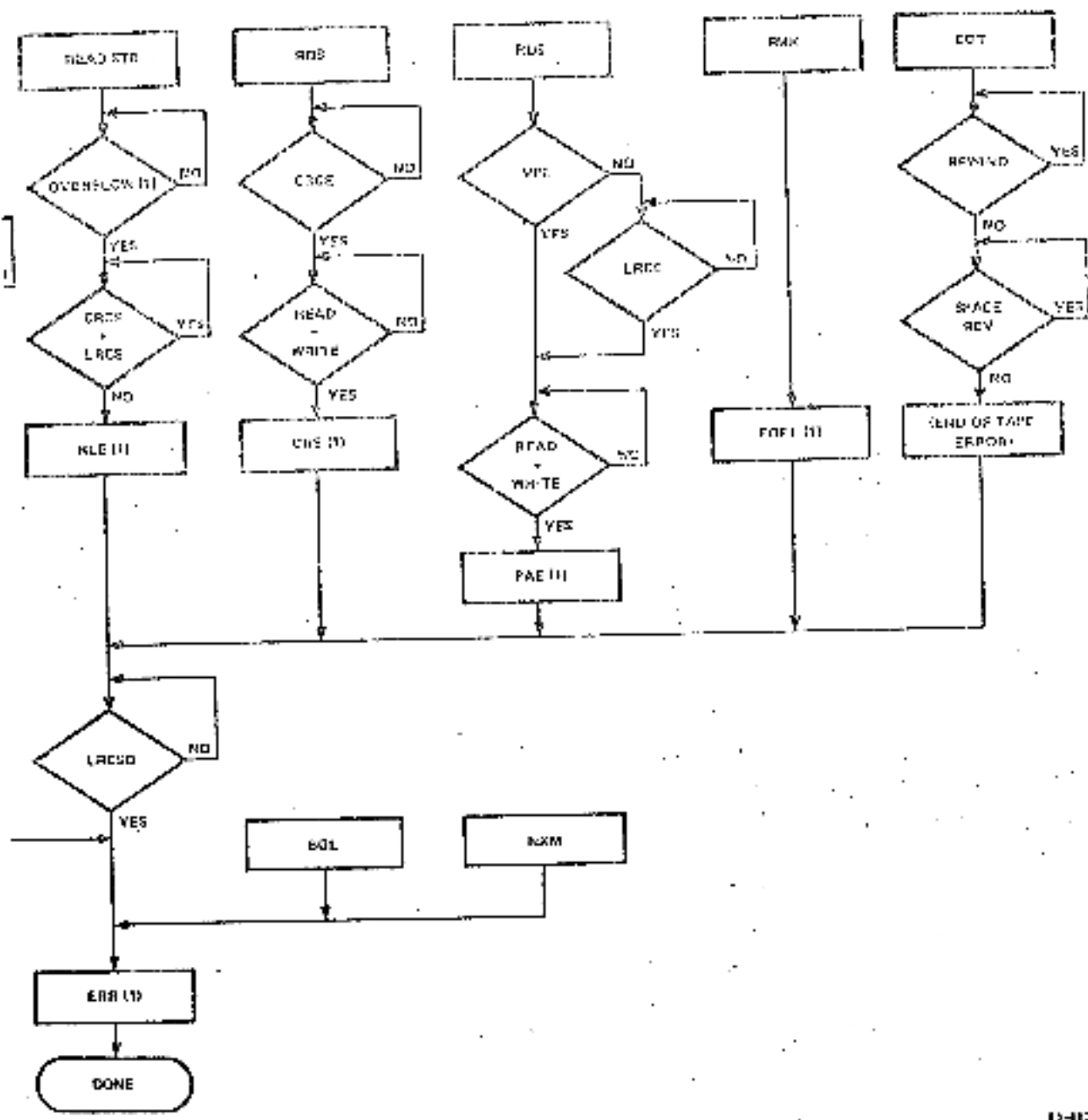


Figure 6-30 Error Sequence Flow Diagram

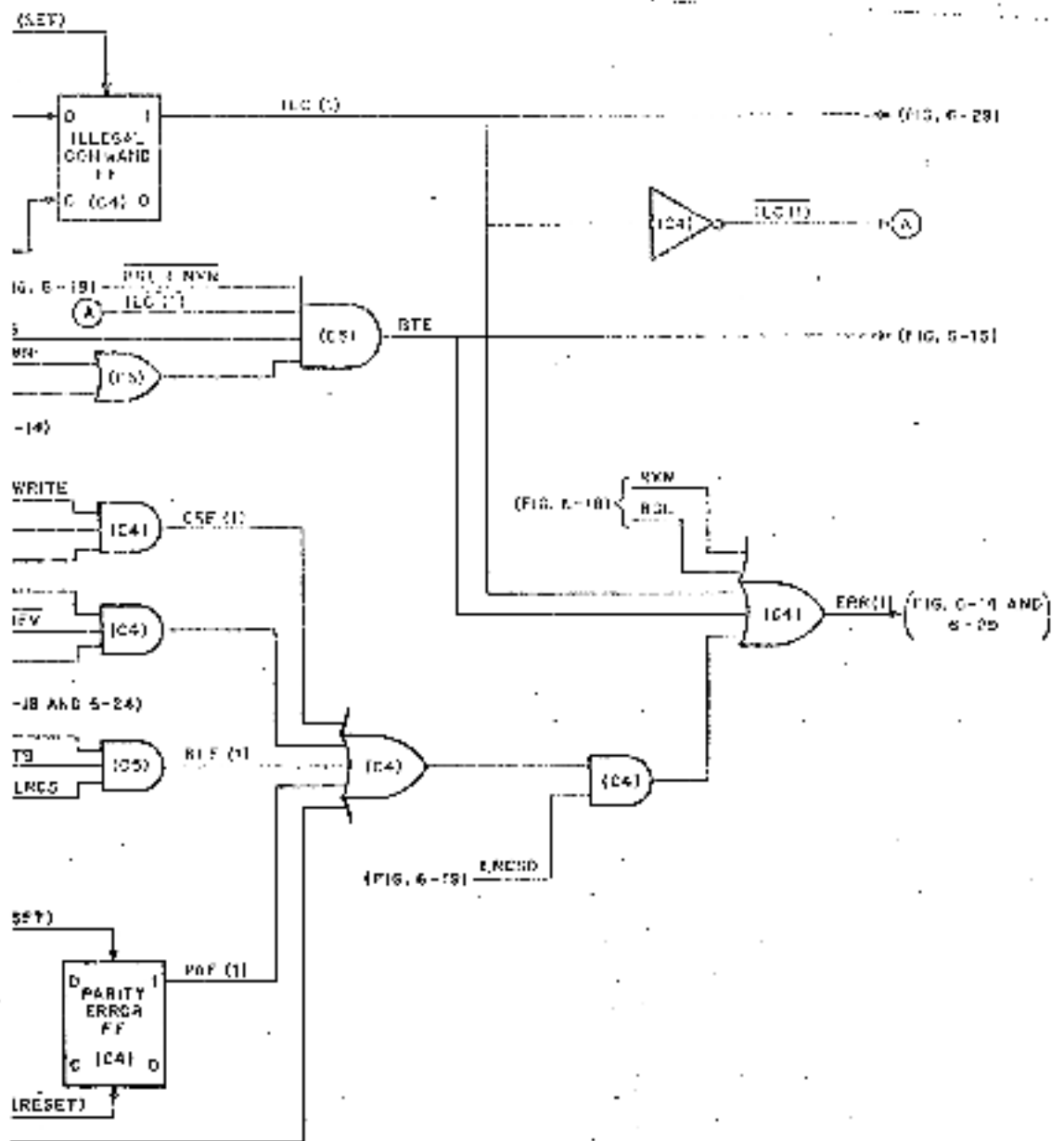


Figure 6-31 Error Sequence Block Diagram

6.6.8 Interrupt Bus Cycle (Figures 6-32 and 6-33)

An interrupt bus cycle is initiated if the interrupt enable bit (bit 05) in the command register is set and any one of the following occurs:

1. GET NEW CMD asserts from the done logic.
2. The tape comes to a stop (TUR asserts) after a rewind operation.
3. The processor requests an interrupt.

The setting of the BR interrupt flip-flop starts the interrupt sequence. The flip-flop is set via a gate enabled by INT ENB (1) from the command register. The other gate input comes from the set interrupt one-shot or from the processor. The set interrupt one-shot is triggered by GET NEW CMD from the done logic (if an interrupt bus cycle is not already in progress) or when the tape transport stops (TUR asserts) after a rewind operation (BOT is reached when CU READY and RWS are true). The processor initiated interrupt is accomplished by the processor asserting SLOTT OUT LO and D00 after it has set the interrupt enable bit in the command register.

NOTE

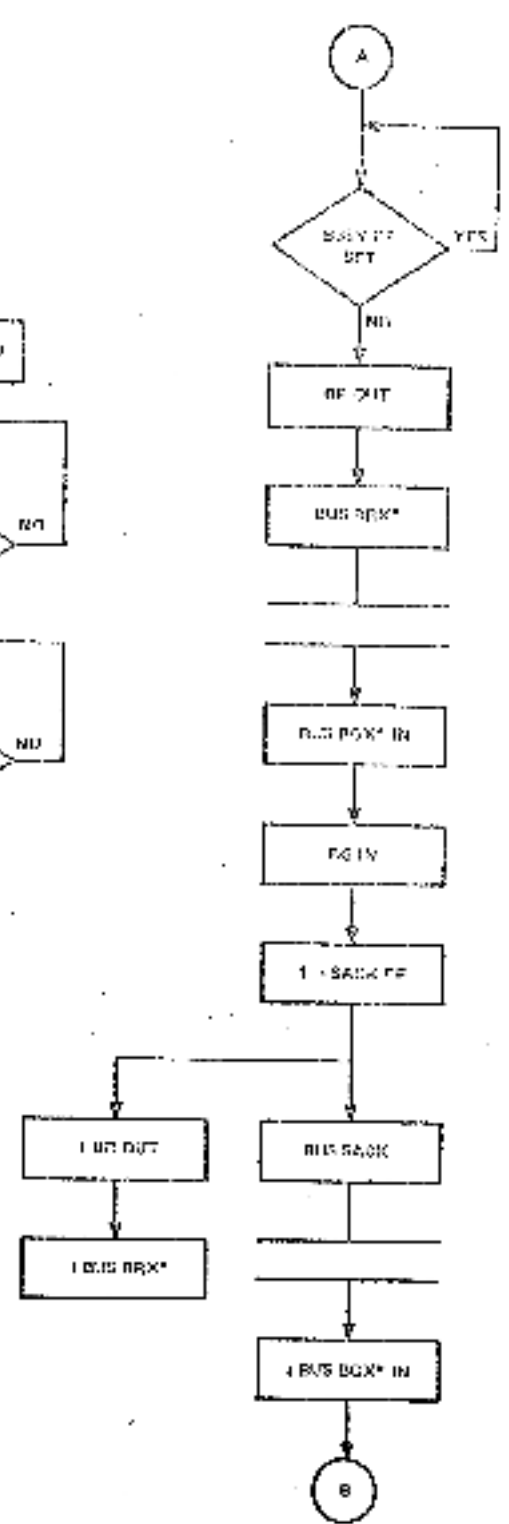
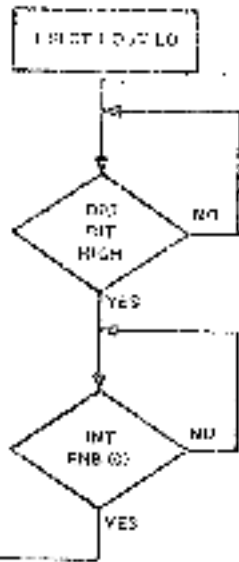
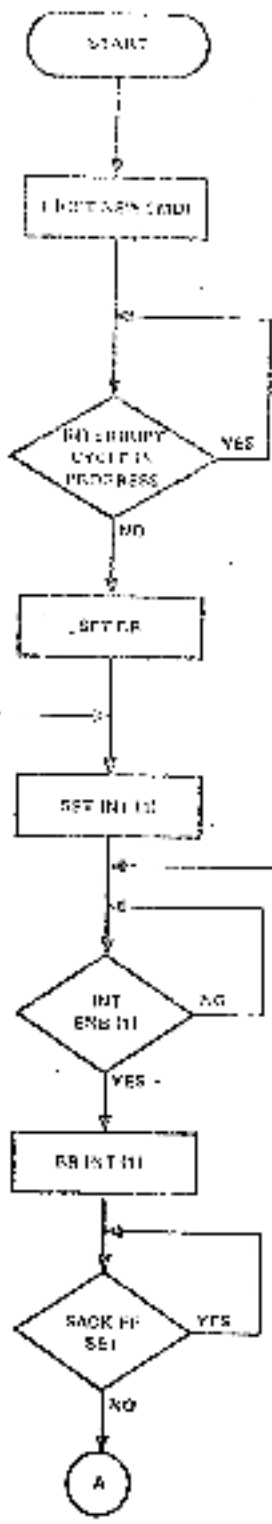
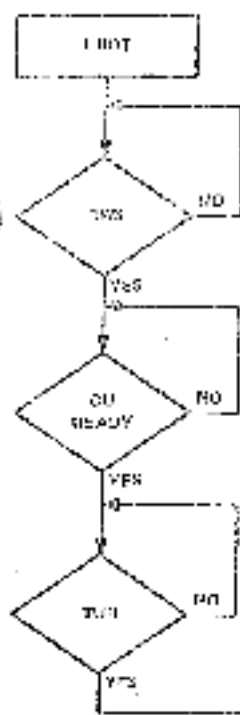
Processor initiation of an interrupt is done for special software purposes and is not a normal occurrence of TMB11/TS03 operation.

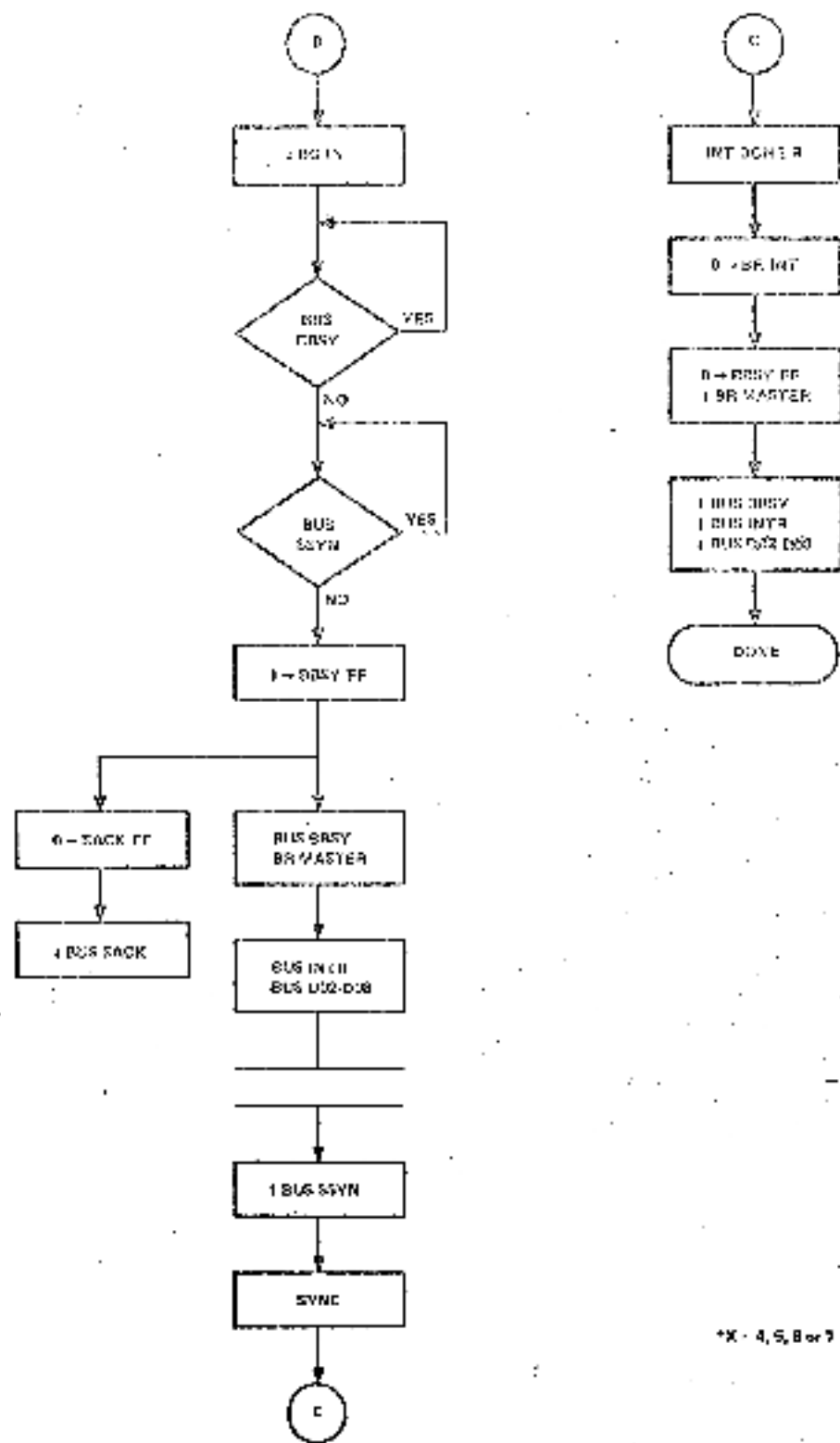
When the BR interrupt flip-flop is set, BR INT (1) asserts enabling the Unibus request logic. The Unibus request logic asserts BR OUT which becomes BUS BRX to the Unibus. The value of X is determined by the priority jumpers and may be 4, 5, 6, or 7 (usually 5). The processor responds to the bus request with BUS BGX IN which becomes BG IN and enables the Unibus acquisition logic. The Unibus acquisition logic asserts BUS SACK to the processor which responds by negating BUS BGX IN. The acquisition logic checks for BUS BBSY (by some other device) and if it finds the bus free asserts BUS BBSY to the Unibus (indicating bus mastership) and BR MASTER to the interrupt circuits. BR MASTER becomes BUS INTR and is placed on the Unibus along with BUS D02-D08, thereby commanding the processor to initiate an interrupt routine starting at the address specified by BUS D02-D08 (address = 224). Processor acceptance of this data is indicated by its assertion of BUS Ssyn to the TMB11. BUS Ssyn becomes Ssyn and triggers the interrupt done logic. The interrupt done logic asserts INT DONE B which completes the interrupt bus cycle by resetting the interrupt flip-flop and acquisition circuits.

6.6.8.1 BUS BGX OUT

A BUS BGX IN from the processor is passed from one system device to another in daisy-chain fashion until it reaches the device that issued the BUS BRX. A BUS BGX IN received by the TMB11 is gated back to the Unibus as BUS BGX OUT if the controller is not making an NPR bus request (BUS NPR false) (NPR requests take priority over all BR requests) and one of the following conditions exist:

1. BR MASTER is true (TMB11 is presently bus master).
2. BR INT (1) is false (TMB11 did not issue the BUS BRX that caused the BUS BGX IN).

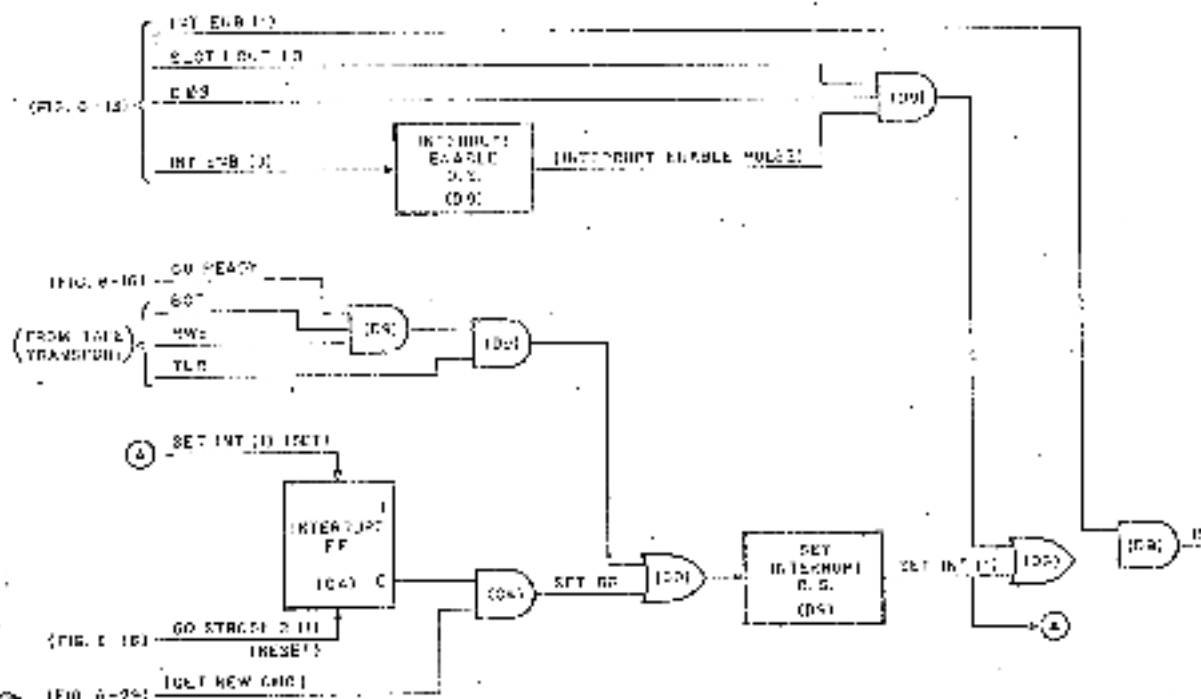




*X - 4, 5, 8 or 7

11 4138

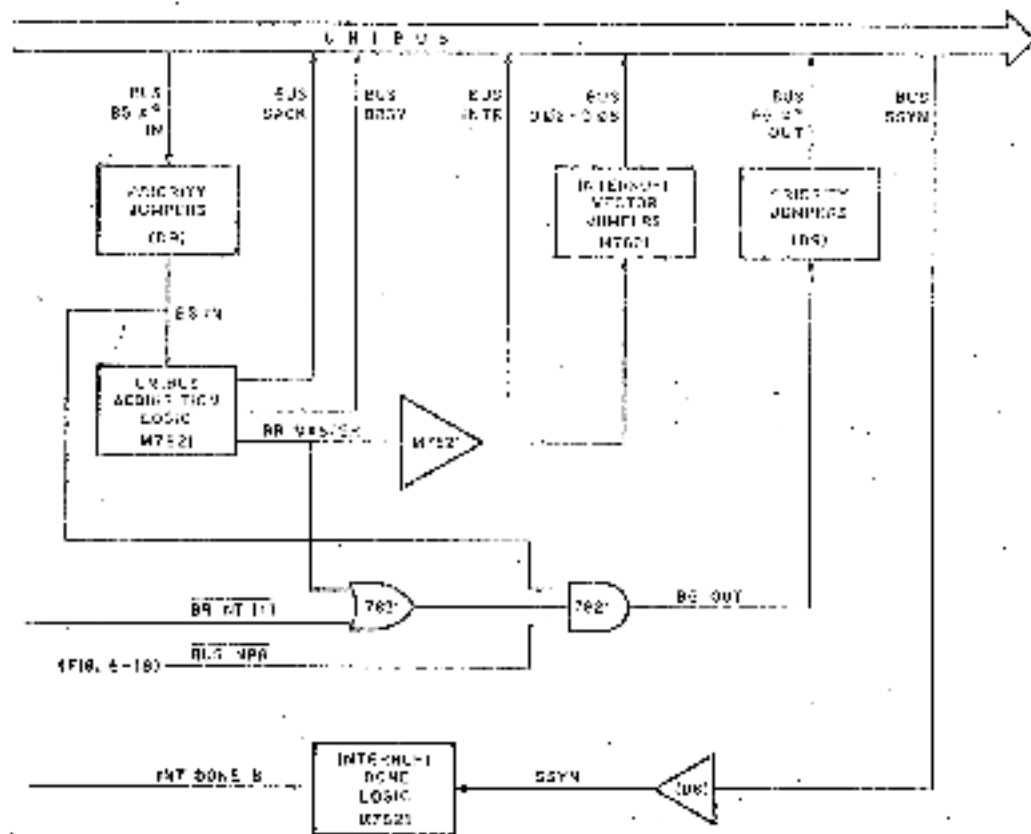
Figure 6-32 Interrupt Bus Cycle Flow Diagram



NOTE

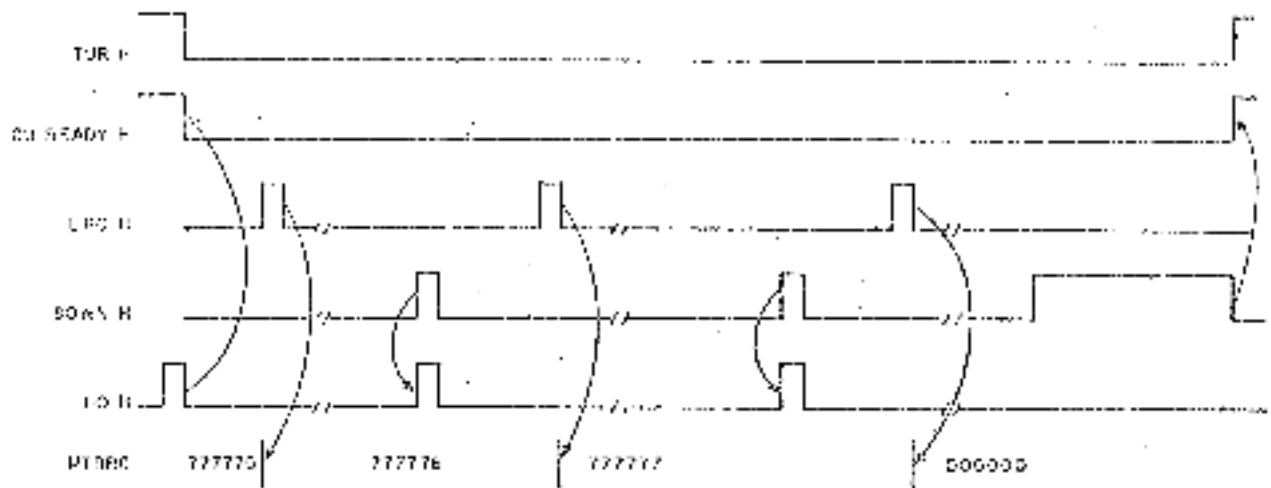
Designations in parenthesis refer to engineering drawings containing corresponding logic.

A: X=4,3,6 or T.



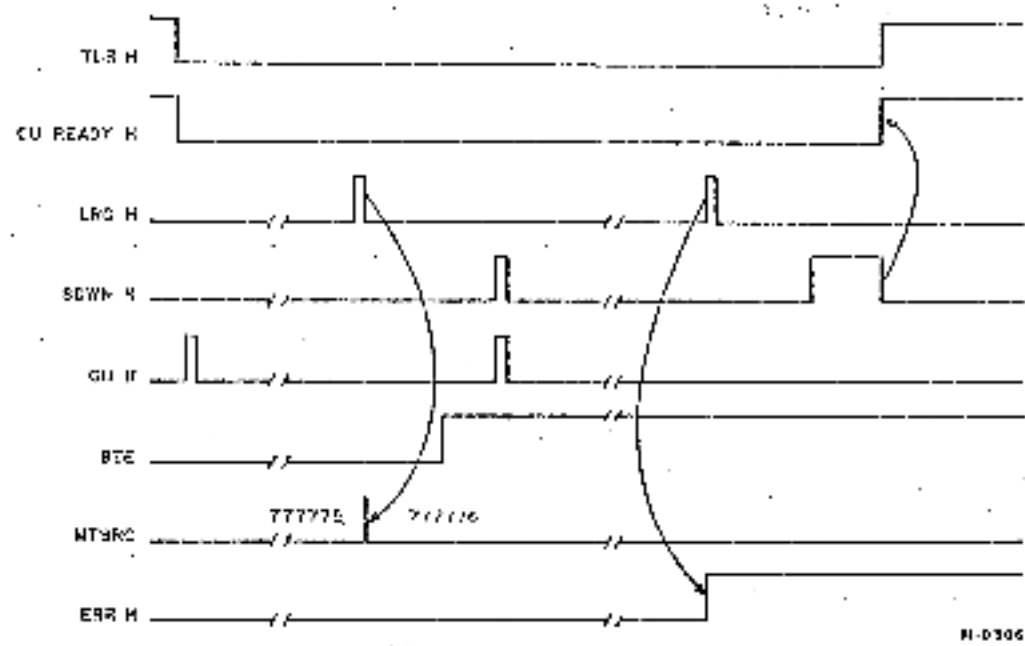
6-78

Figure 6-33 Interrupt Bus Cycle Block Diagram



6-4247

Figure 6-36 Spacing Reverse Three Records



6-0306

Figure 6-37 Spacing Forward Three Records, Bad Tape Error Appearing in First Record

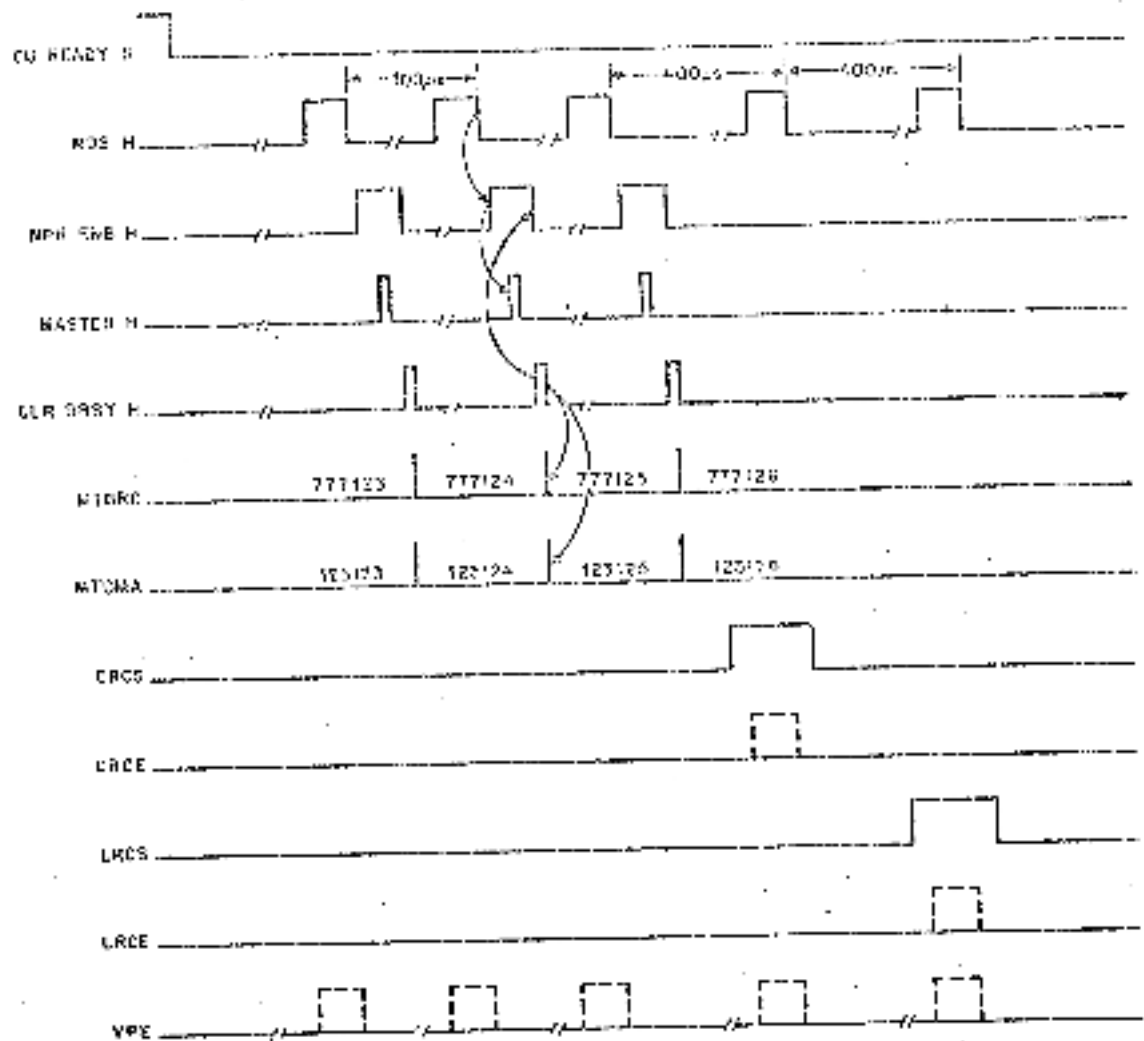


Figure 6-38 Reading Record of Three Data Characters

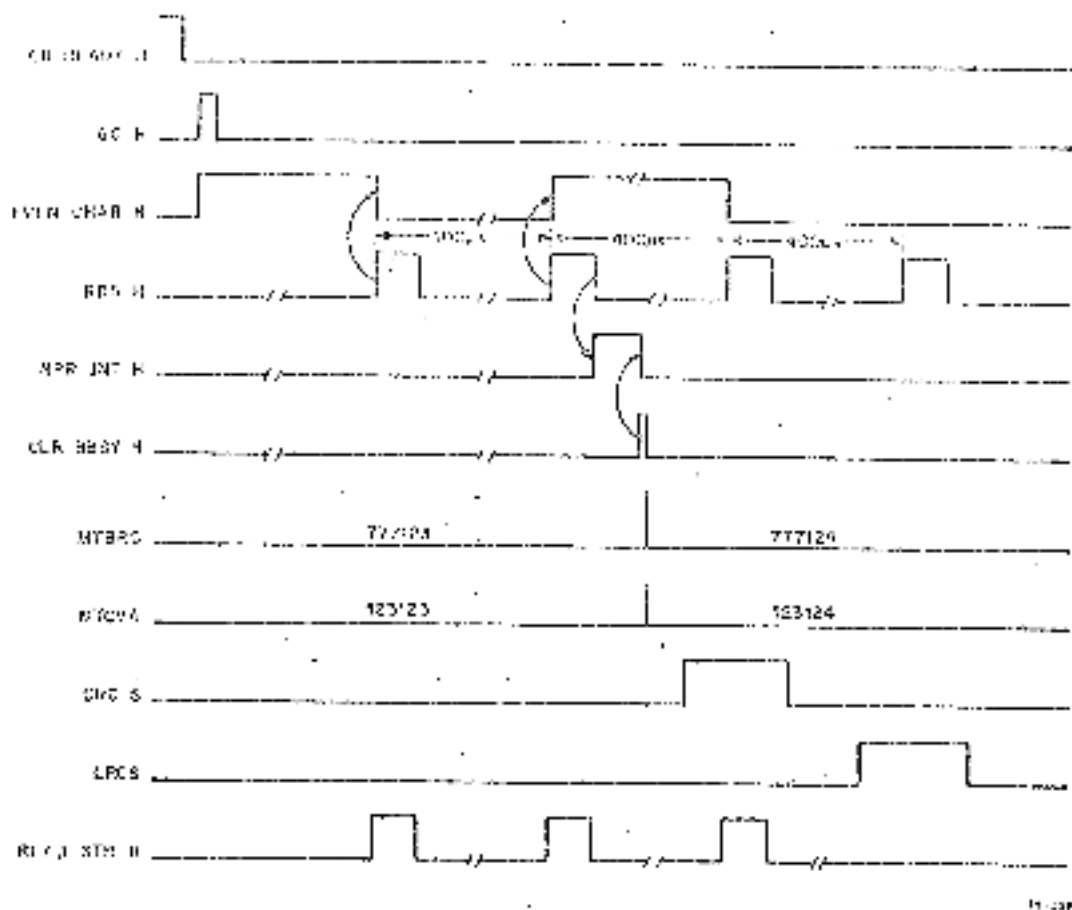


Figure 6-39 Reading Record of Two Tape Characters in Core Dump Mode

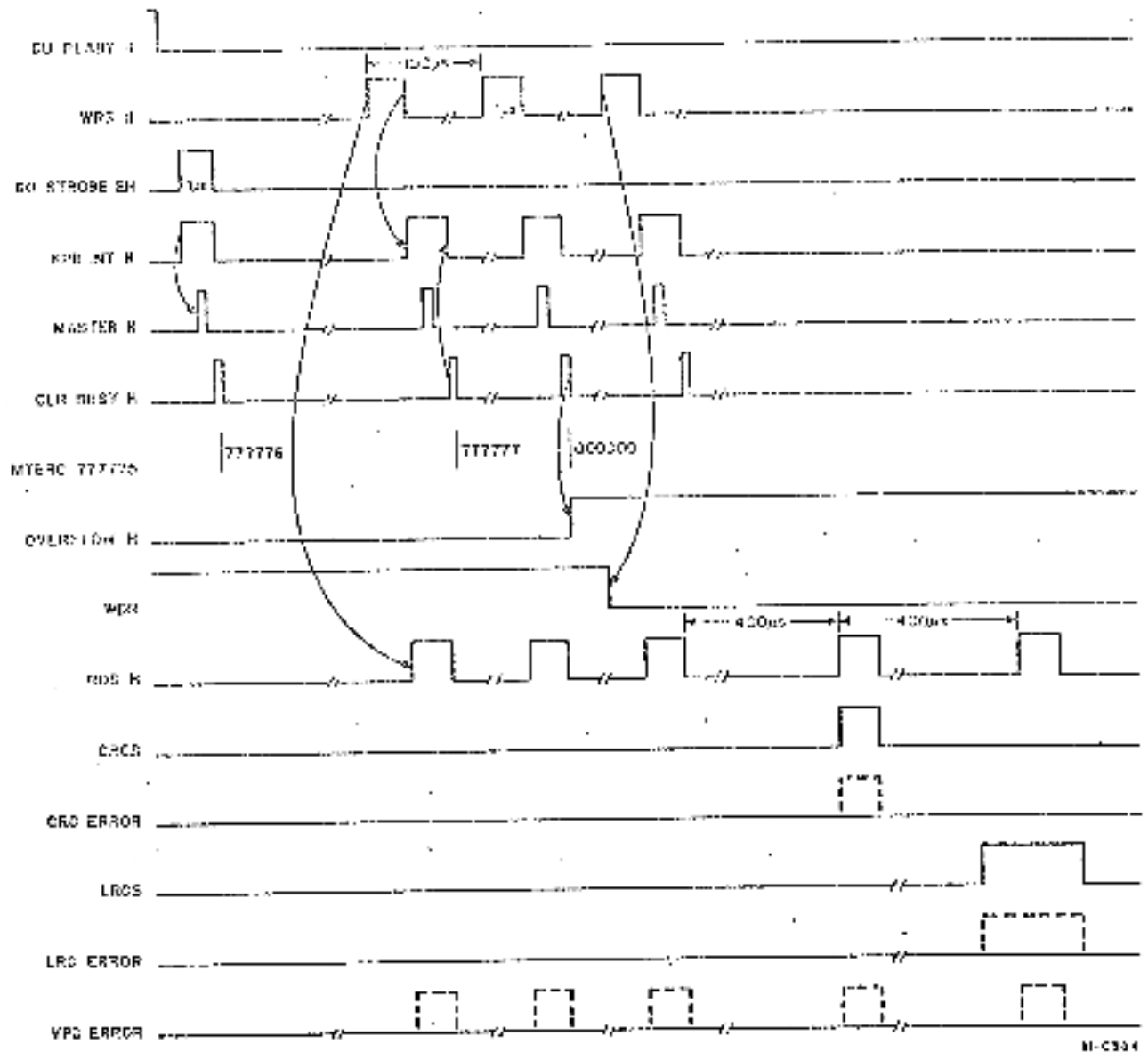
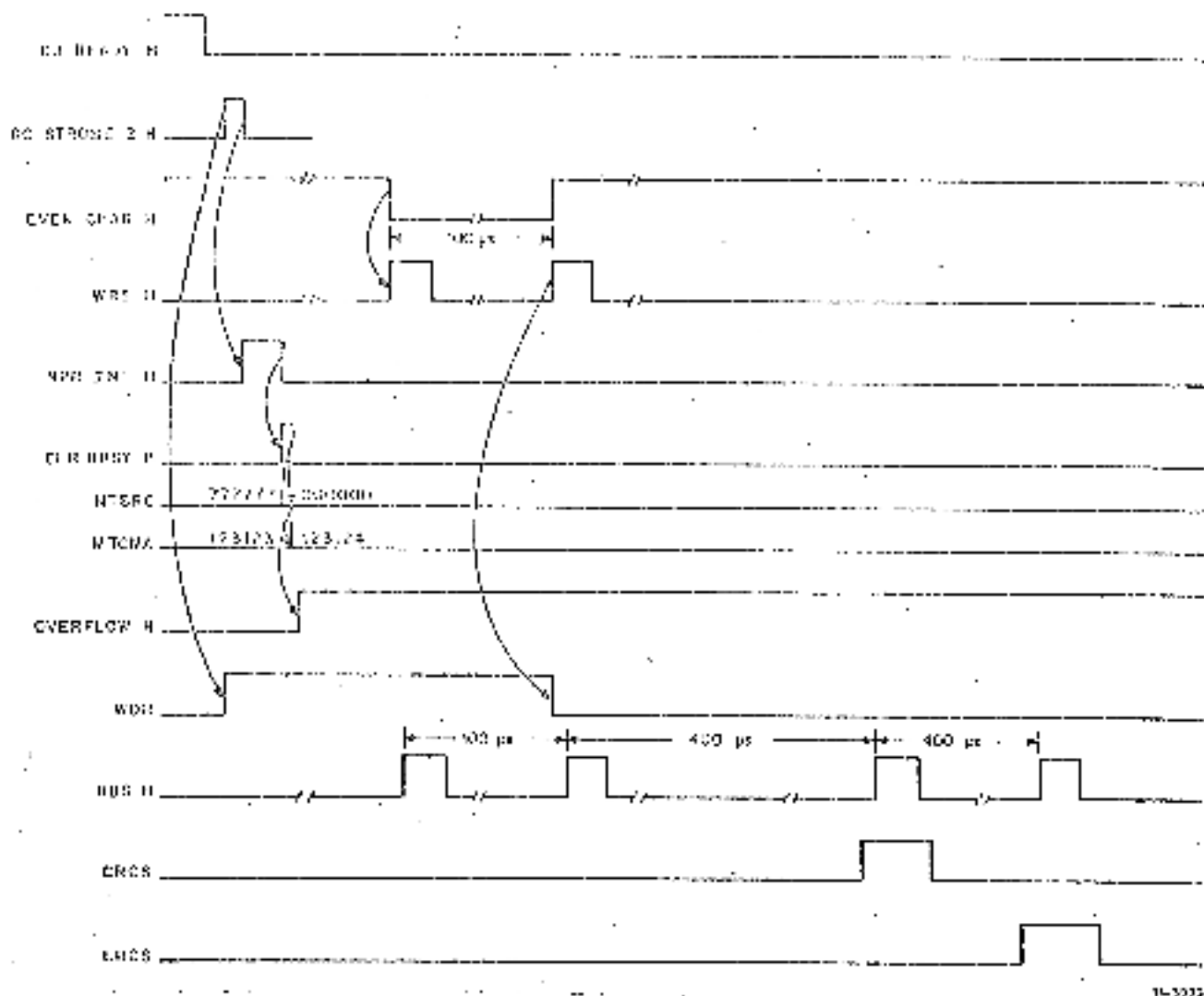


Figure 6-40 Writing Record of Three Data Characters



11-5075

Figure 6-41 Writing Record of Two Tape Characters in Core Dump Mode

CHAPTER 7

M8926 Theory of Operation

7.1 General (Figures 7-1, 7-2 and 7-3)

Figure 7-1 is a simplified flow diagram of the M8926 Interface Board. The CSET command from the controller triggers a drive start-up sequence. The start-up sequence signals the drive to start the drive motor and introduces an 8.9 ms delay for the drive motor to get up to speed (45 ips) before enabling a read or write sequence.

All commands from the controller except rewind, will cause a read sequence to occur. The read sequence transfers data from the drive to the M8926 board. A write command (WRB) must be asserted by the controller to enable a write sequence. If a write command is asserted by the controller, data is transferred from the controller to the drive to be written on tape (write sequence). The data written on tape is immediately read back via the read sequence. This read-after-write feature allows the recorded data to be checked for errors by the M8926 board. The read-after-write data is made available to the controller where it can be accessed by the processor for maintenance purposes. During normal operation read data is not accepted by the controller unless a read command is asserted.

When the read circuits detect the end of the record a drive stop sequence is triggered. The stop sequence signals the drive to stop the drive rotor and initiates another 8.9 ms delay. The delay allows the drive motor to slow down to a stop before the command operation is terminated.

The M8926 detailed flow diagram (Figure 7-2) provides a more detailed functional description of the M8926 interface board. This diagram should be read in its entirety while referencing the functional block diagram, Figure 7-3. Subsequent sections in this chapter treat the M8926 board according to the functional divisions shown in Figures 7-1, 7-2 and 7-3, namely:

1. Status/Command Logic
2. Drive Start Up
3. Write Sequence
4. Read Sequence
5. Drive Stop

It will be helpful to reference Figures 7-2 and 7-3 as an overview while reading through Chapter 7.

NOTE

The block diagrams that follow use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the controller logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used they are enclosed in parenthesis.

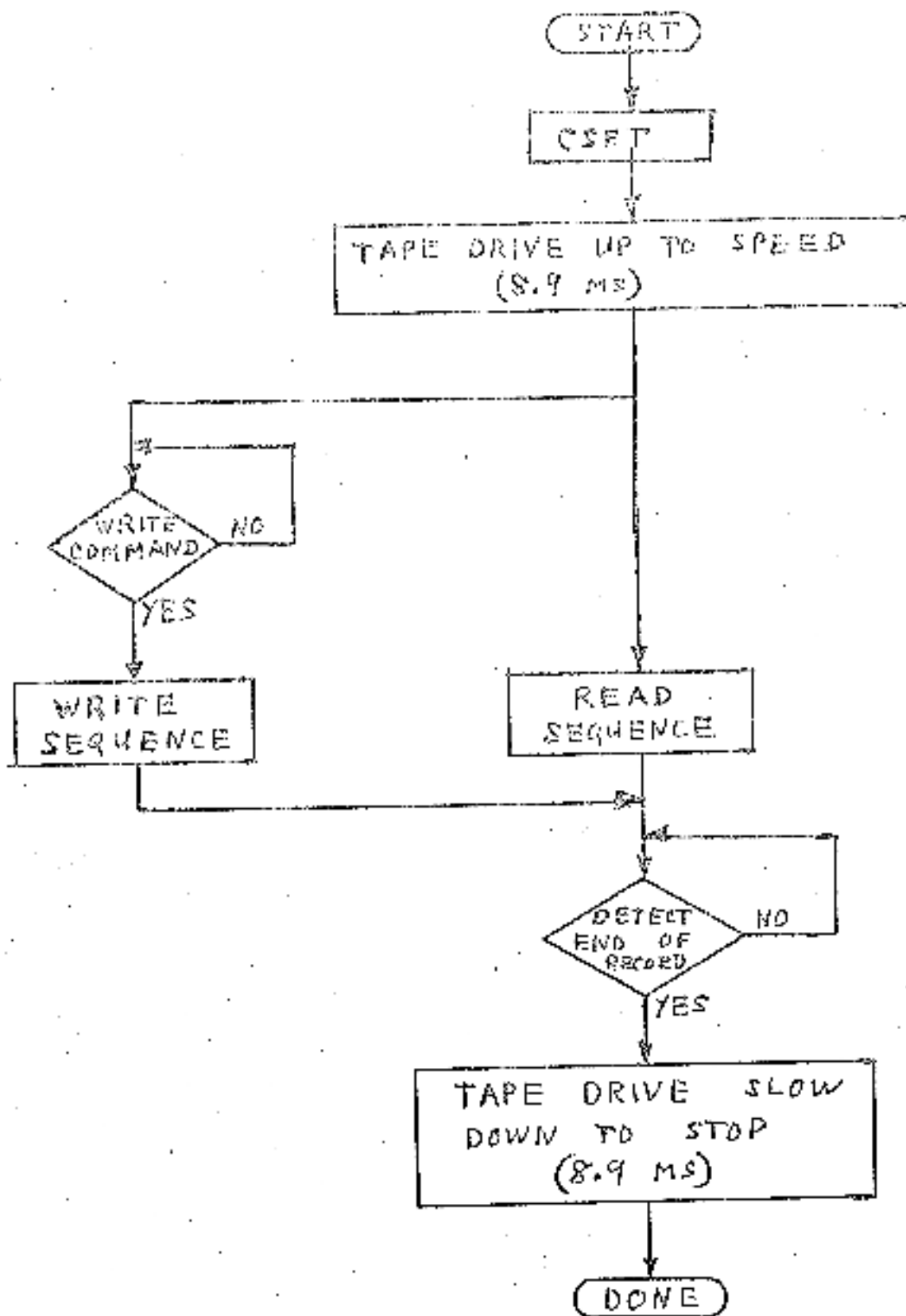


FIG. 7-1 M9926 Simplified Flow Diagram

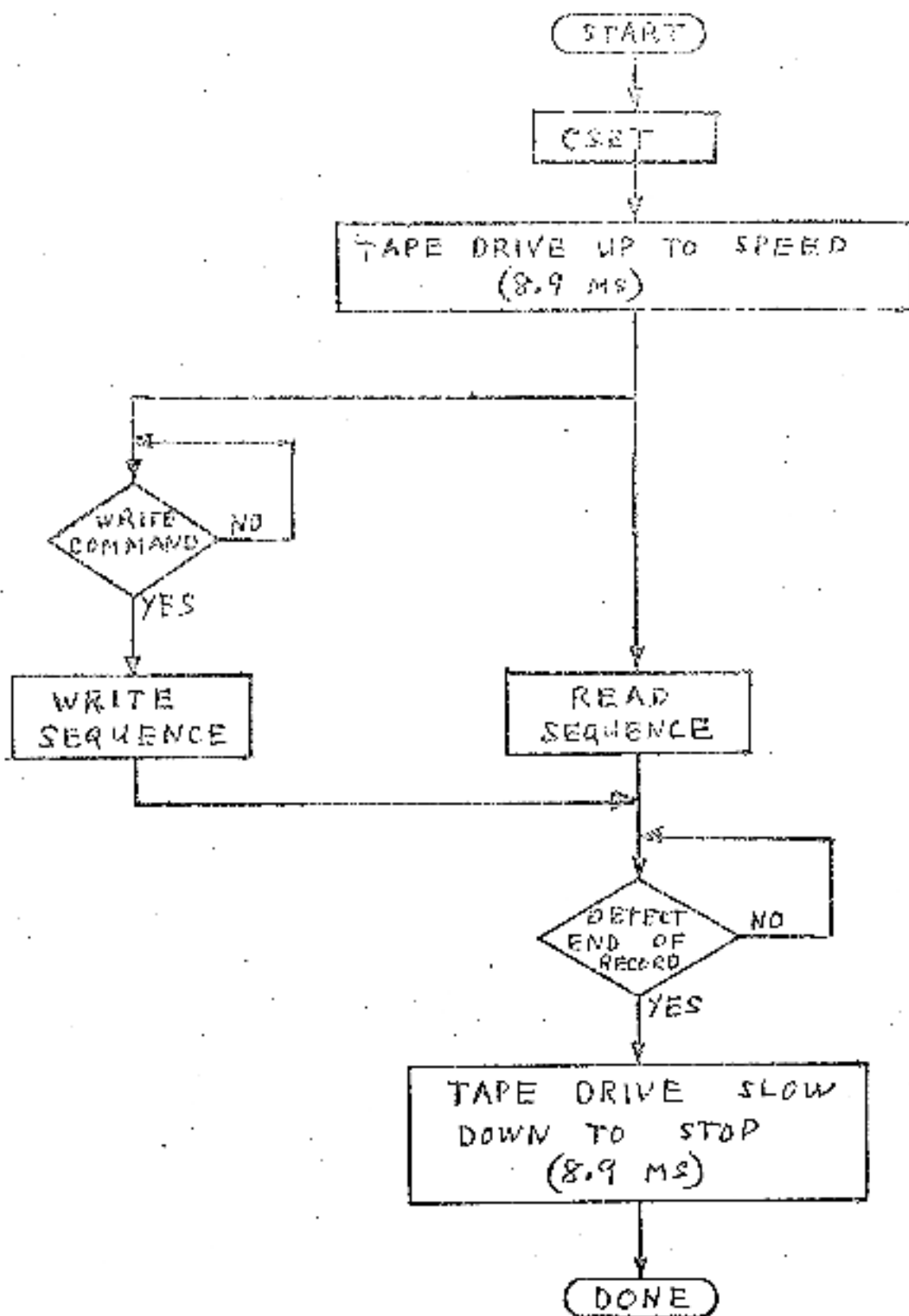
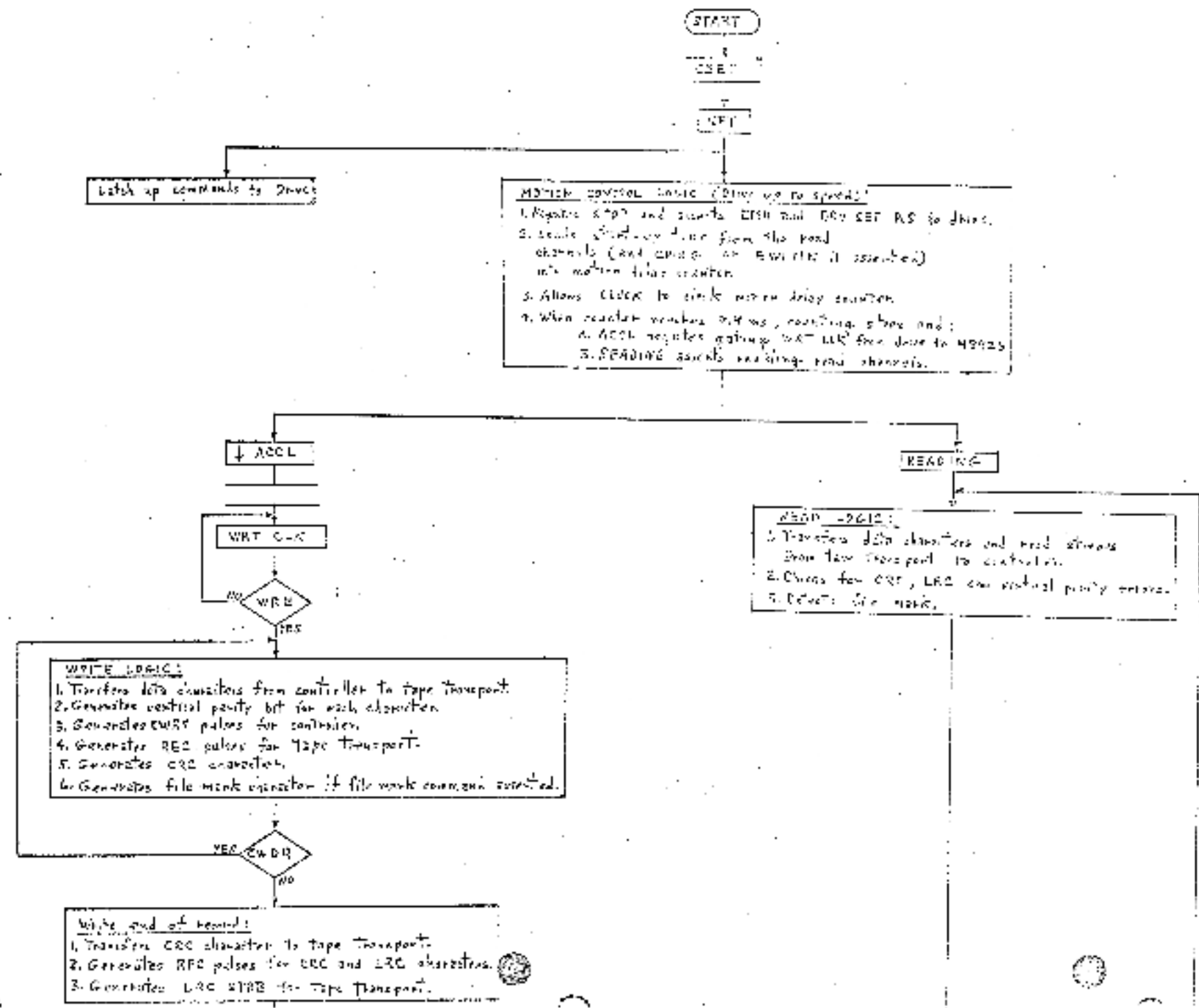


FIG. 7-1 M8926 Simplified Flow Diagram

7-4



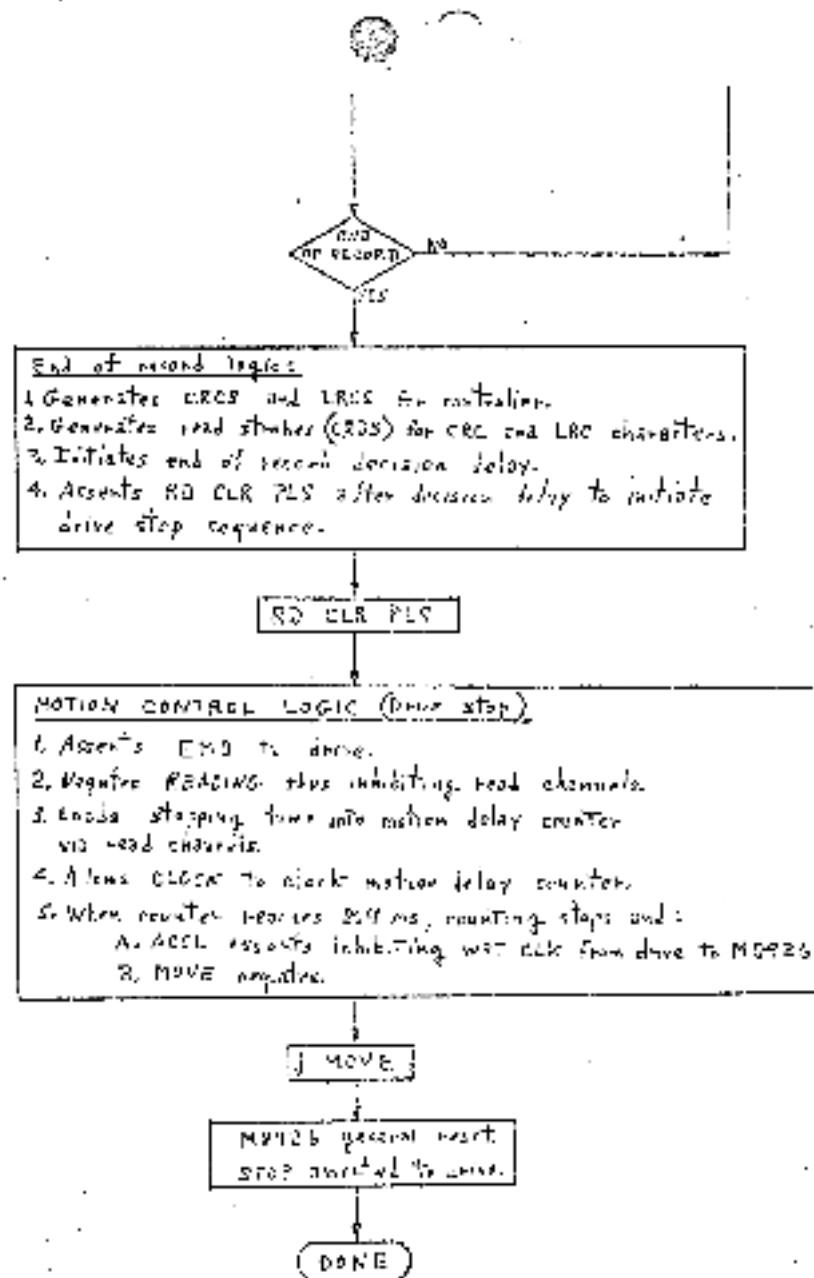


FIG. 7-2 M926 Detailed Flow Diagram

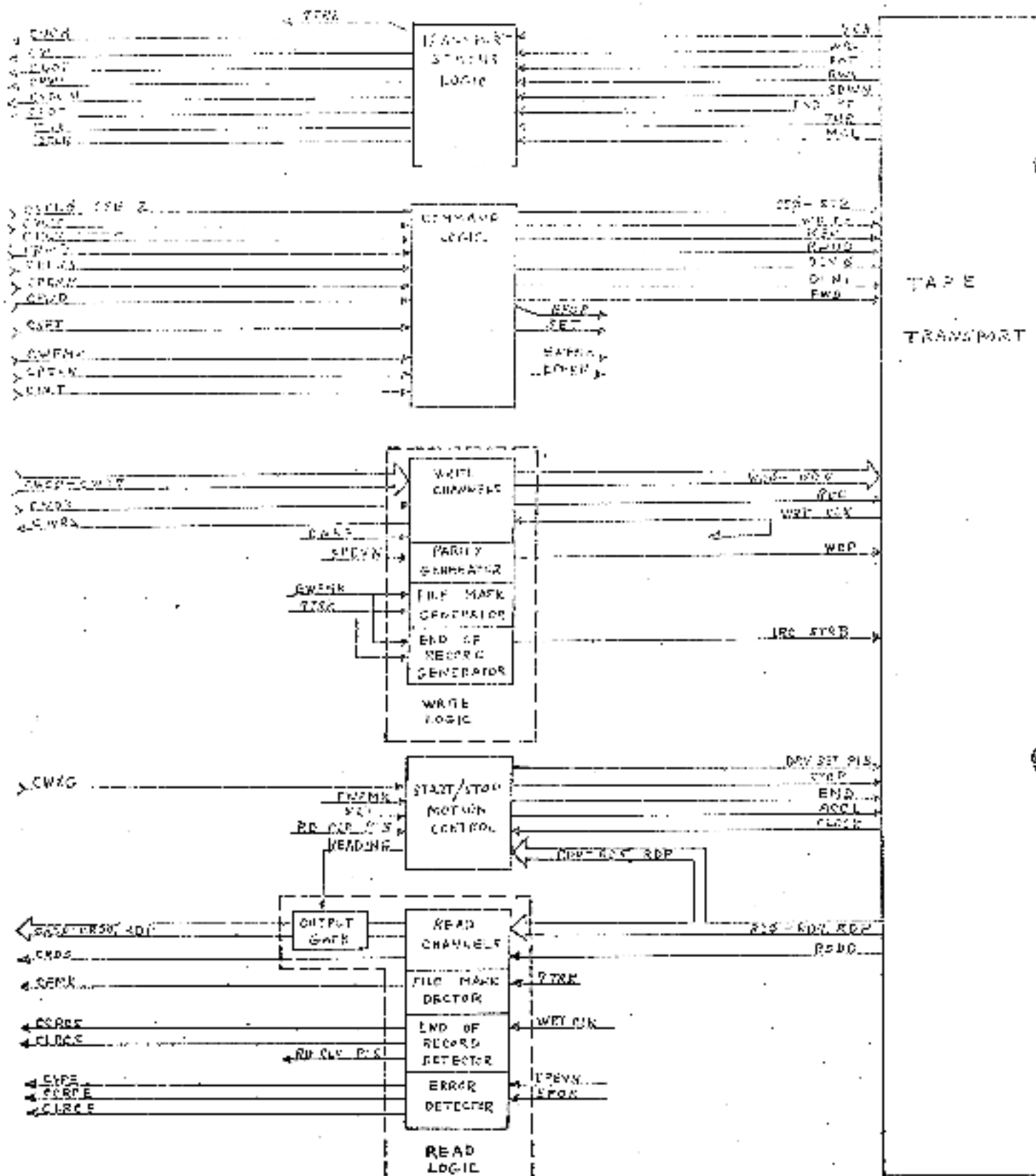


Fig. 7-3 X8926 Block Diagram

7.2 Status/Command Logic (Figures 7-5 and 7-6)

7.2.1 Command Logic

Some operational commands are coupled from the controller to the drive via passive logic circuits. Other commands that must stay asserted during the entire operation, are latched up in flip-flops set by CSST from the controller. Note the conversion of CSFNS to DEFS and CSFNS to DEFI during the latch-up process.

CSSEL0-CSSEL2 selects a slave unit via a 3-bit code. The 3-bit code is latched up in the slave select latch-up flip-flops which output SS0-SS2 to the drive. The input code from the controller is compared to the output code in the slave select comparator. If the two codes do not match the latch-up flip-flops are clocked forcing SS0-SS2 to agree with the select code from the controller. An AND gate must be enabled by MOVE before clocking of the flip-flops occur. MOVE is asserted true during every command operation except rewind. Thus a new slave drive cannot be selected during a data transfer operation. Note that a bit reversal takes place in the latch flip-flops where the CSSEL0, 1 and 2 input bits become bits SS2, 1 and 0 respectively in the output.

7.2.2 Status Logic

Some status signals are directly coupled from the drive to the controller while others such as RWS and MOL undergo conditional gating. Rewind status (RWS) from the drive negates at the end of SDWN simultaneous with the assertion of TOR (see Figure 7-4). A timing requirement within the controller is that RWS negate before TOR asserts.

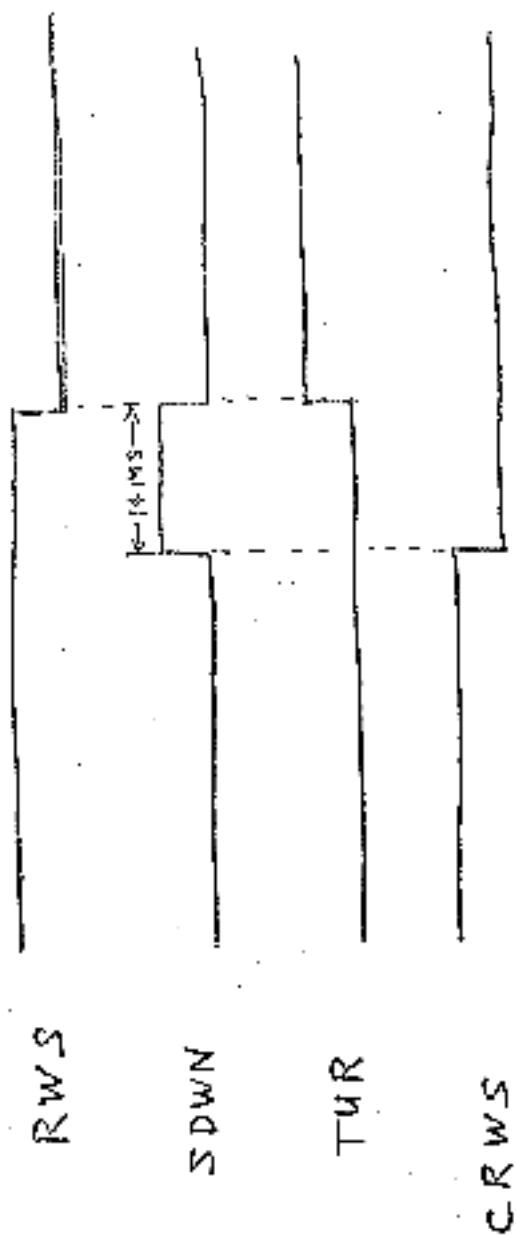


FIG. 7-4 RWS and CRWS Timing Diagram

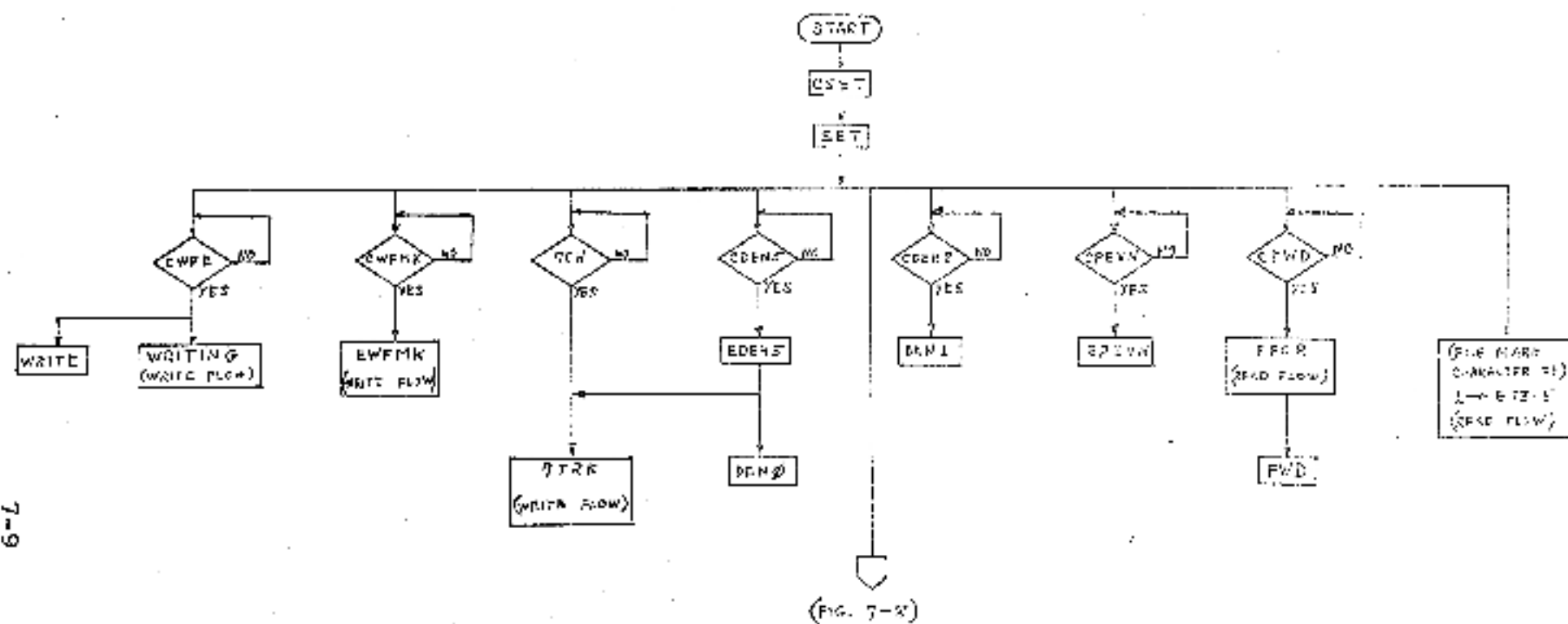
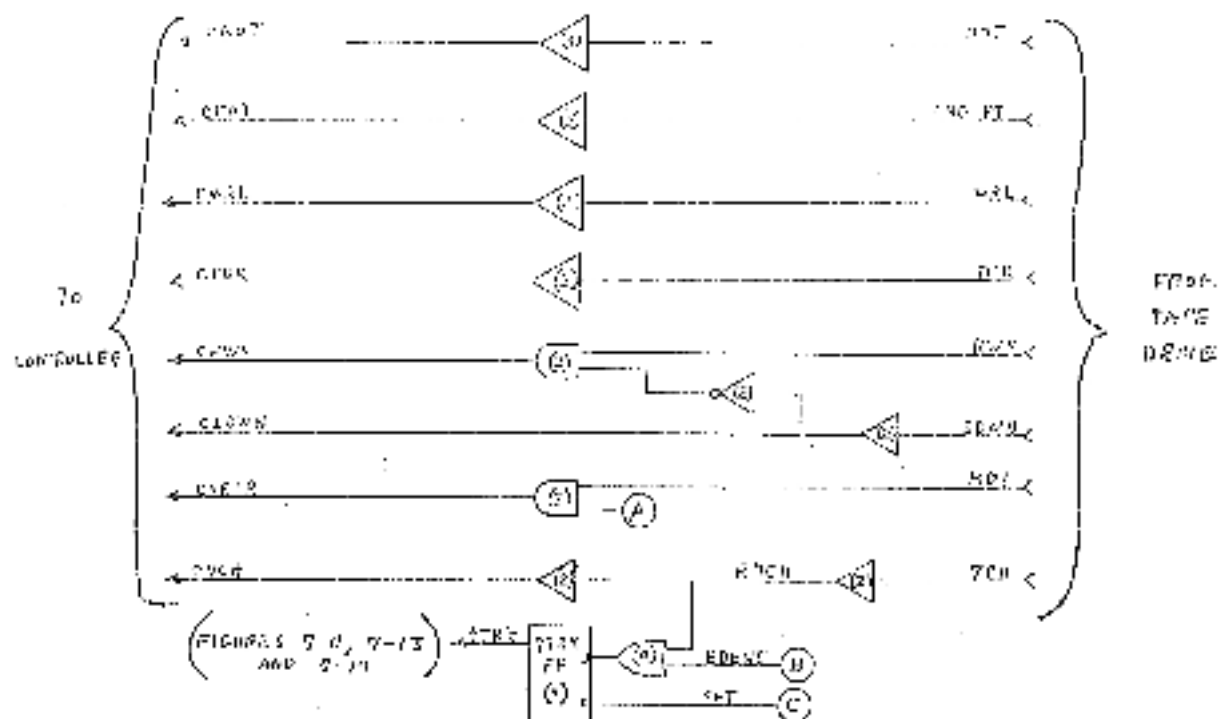
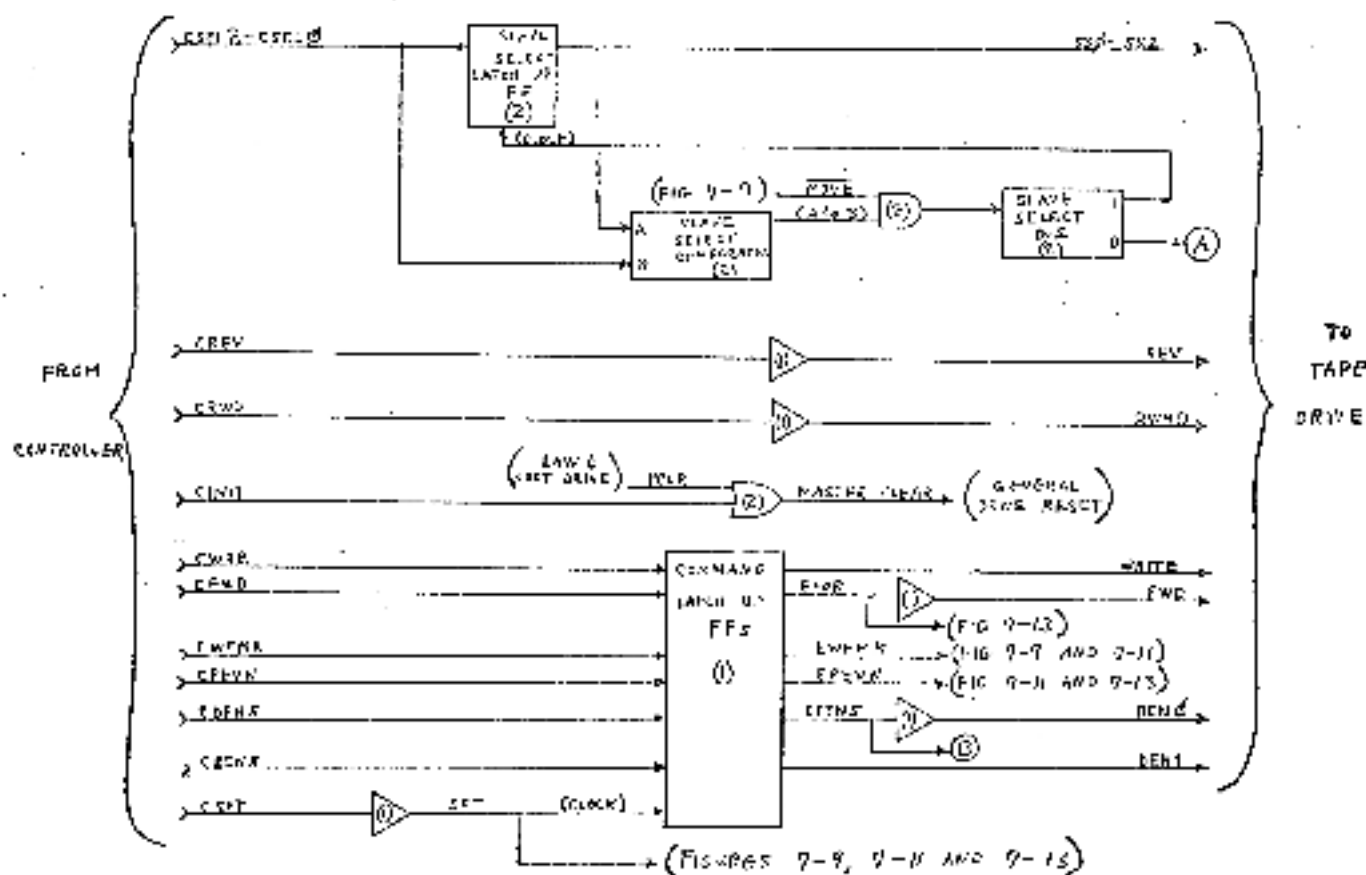


FIG. 7-5 Command Latch Up Flow Diagram



A. STATUS



B. COMMAND

FIG. 7-6

STATUS/COMMAND Block Diagram

This requirement is met by ANDing R03 with SEN5 thus producing the proper CKCS timing as shown in Figure 7-4.

CSELB is negated for 1 us while a new drive is being selected by the slave select logic. This is accomplished by the gating of MCL with the β output of the slave select one-shot. The 1 us delay allows settling of the select code before CSELB is asserted for the new drive.

When a 7 track drive is being used 7CK is asserted from the drive causing the assertion of C7CK to the controller and R7CK to the 7TRK flip-flop. When SET asserts 7TRK becomes true to indicate the presence of a 7 track, slave drive to the MS926 board. Note that the assertion of EDSB5 will also cause 7TRK to become true at SET time. Compatibility between the TU16 and TU10W drives requires that both EDSB5 and R7CK cause the assertion of 7TRK at SET pulse time.

7.3 Drive Start Up (Figures 7-7, 7-8 and 7-9)

7.3.1 Drive Start Signals

The SET pulse starts the command operation in the drive by:

- a. Setting the EMD flip-flop and asserting EMD to the drive
- b. Asserting DRV SET PLS to the drive
- c. Setting the MOVE flip-flop thereby negating STOP to the drive

MOVE remains asserted and holds STOP false during the entire command operation. During a rewind operation the MOVE flip-flop is not set.

In this case DRV SET PLS negates STOP at SET time which is sufficient for the drive to start the rewind sequence.

7.3.2 Start Up Delay

The output of the RMD flip-flop loads the motion delay counter with delay data sent onto read lines RD₀-RD₅, RD₆ by the drive. Bit 13 of the counter is preset to a 1 and gates in the clock pulses. The clock pulses are obtained from a $\div 4$ counter which receives CLOCK pulses from the slave bus. No output from the $\div 4$ counter is obtained after the first 2 CLOCK pulses and every 4 CLOCK pulses thereafter. After 8.9 ms bit 13 of the delay counter is counted down to 0 and bit 14 is asserted. At this time:

- a. Input clock pulses to the delay counter are inhibited.
- b. REMPING is asserted enabling the read sequence.
- c. ACCL is negated to the drive thus getting WAF CLX pulses in from the drive for the write sequence.

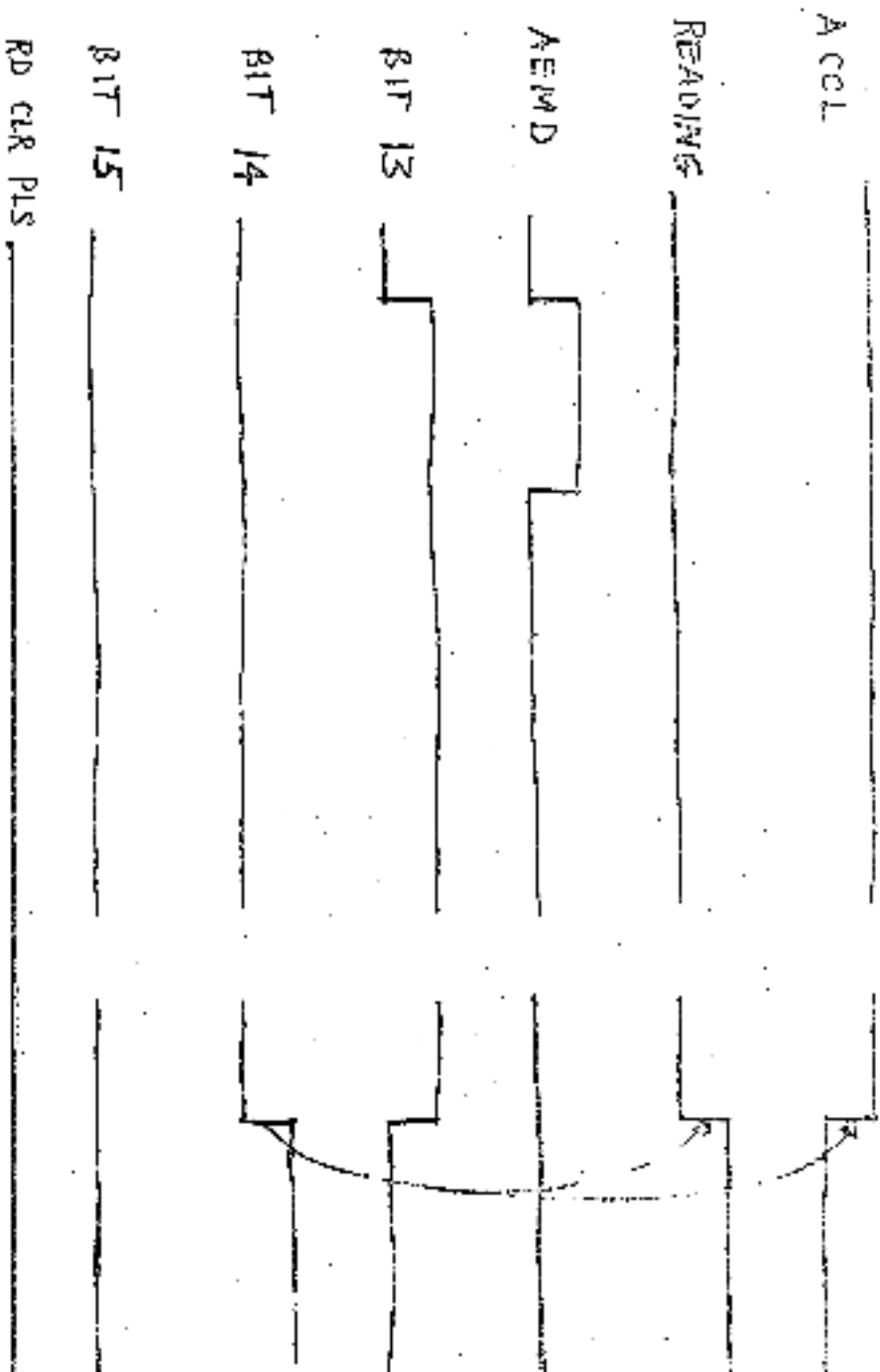
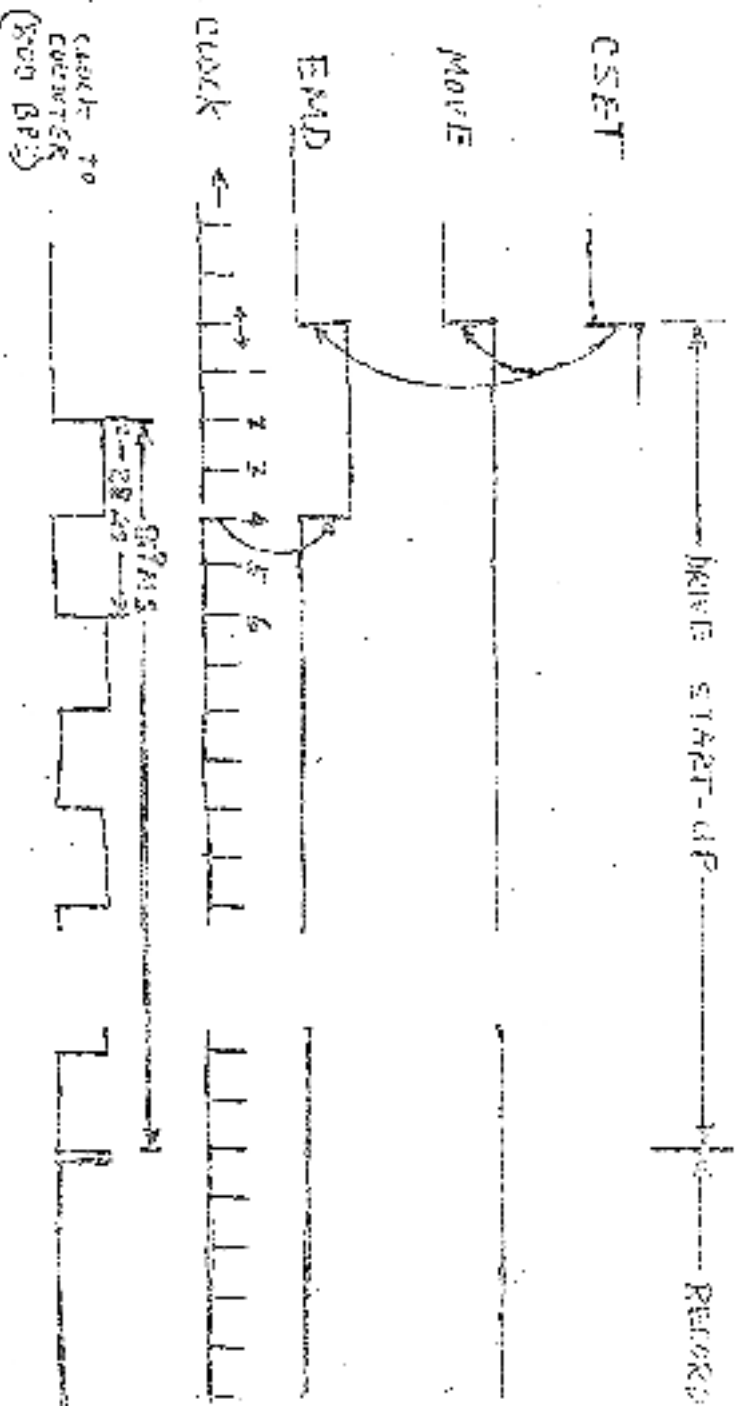
If the command is CWXS or CWFMK an extended interrecord gap is generated prior to writing the record. CWXS or CWFMK, if asserted, input into the delay counter increasing the 8.9 ms delay time and allowing the tape to travel an extra distance before the read and write sequences are enabled. The CWXS and CWFMK inputs to the delay counter are via a gate enabled by ACCL. Thus only the start-up time or gap prior to the record is extended.

7.4 Write Sequence (Figures 7-10 and 7-11)

7.4.1 Nine Track Normal

7.4.1.1 Write Data

If a write command is asserted by the controller, WRF will be true allowing the SET pulse to set the WRITING flip-flop. The assertion



TRANSFER ——— | 200 ——— DRIVE SHUTDOWN ——— | 200 ———

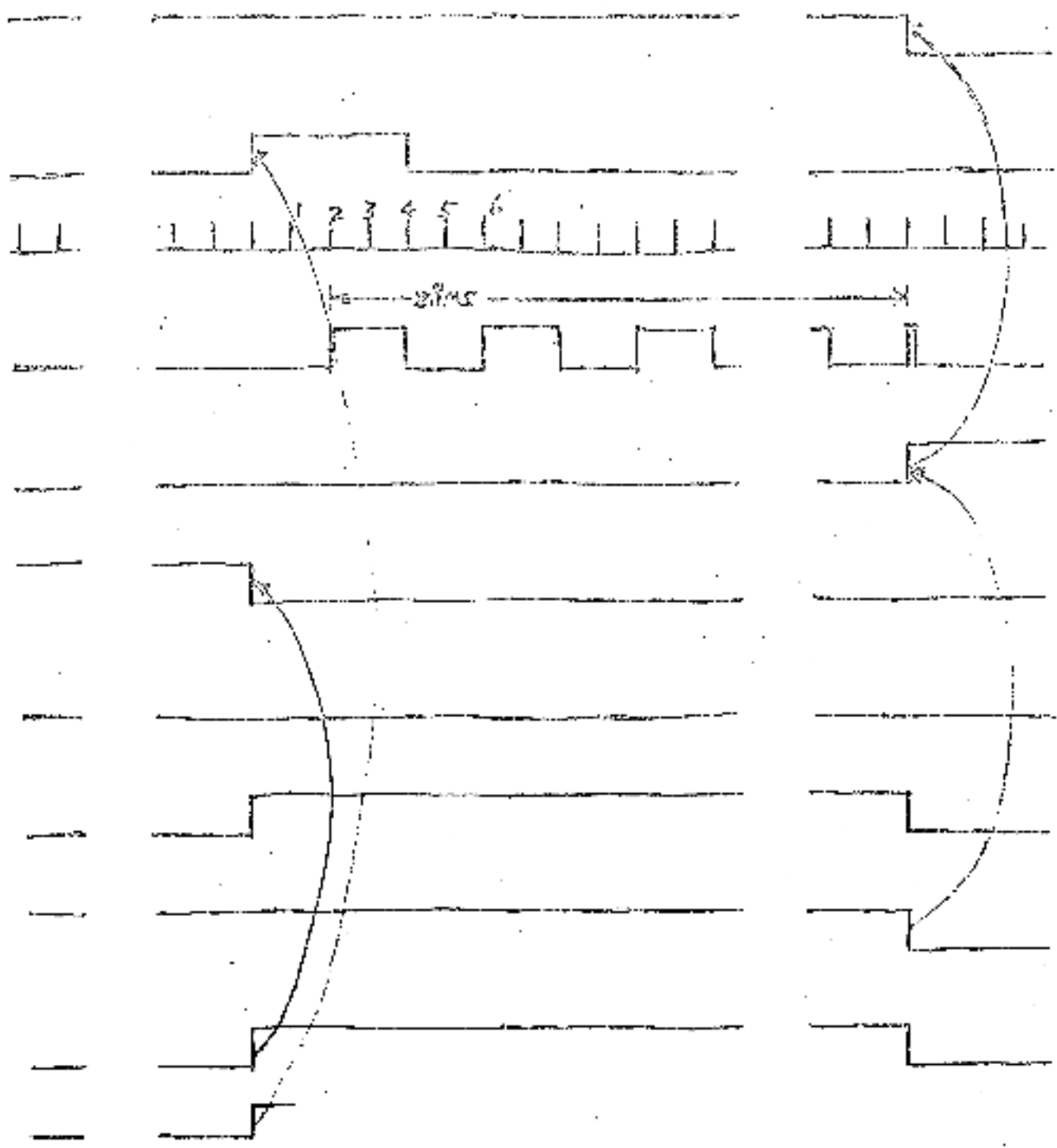
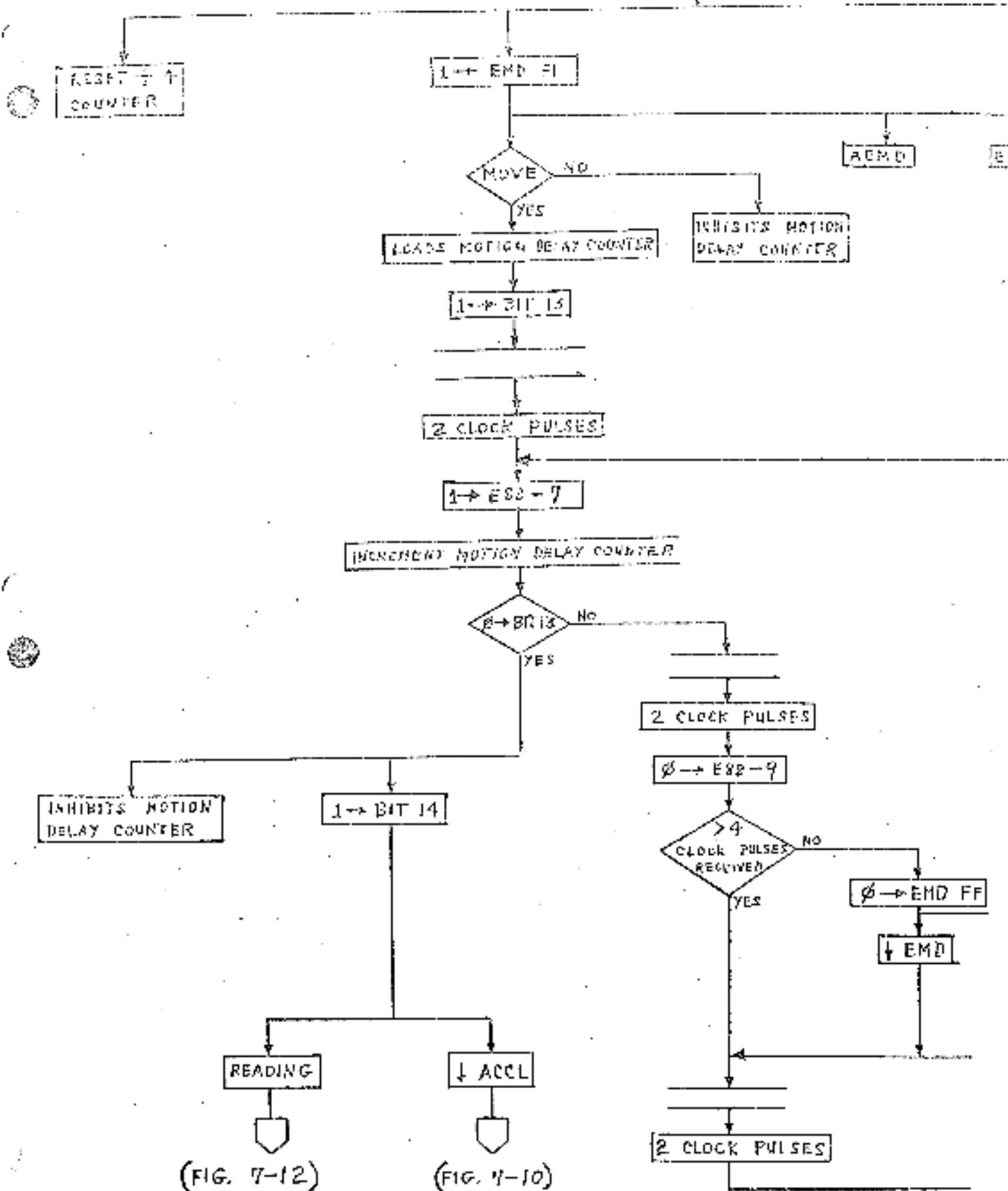


FIG. 7-7 X8926 Timing Diagram

(FIG. 4-5)



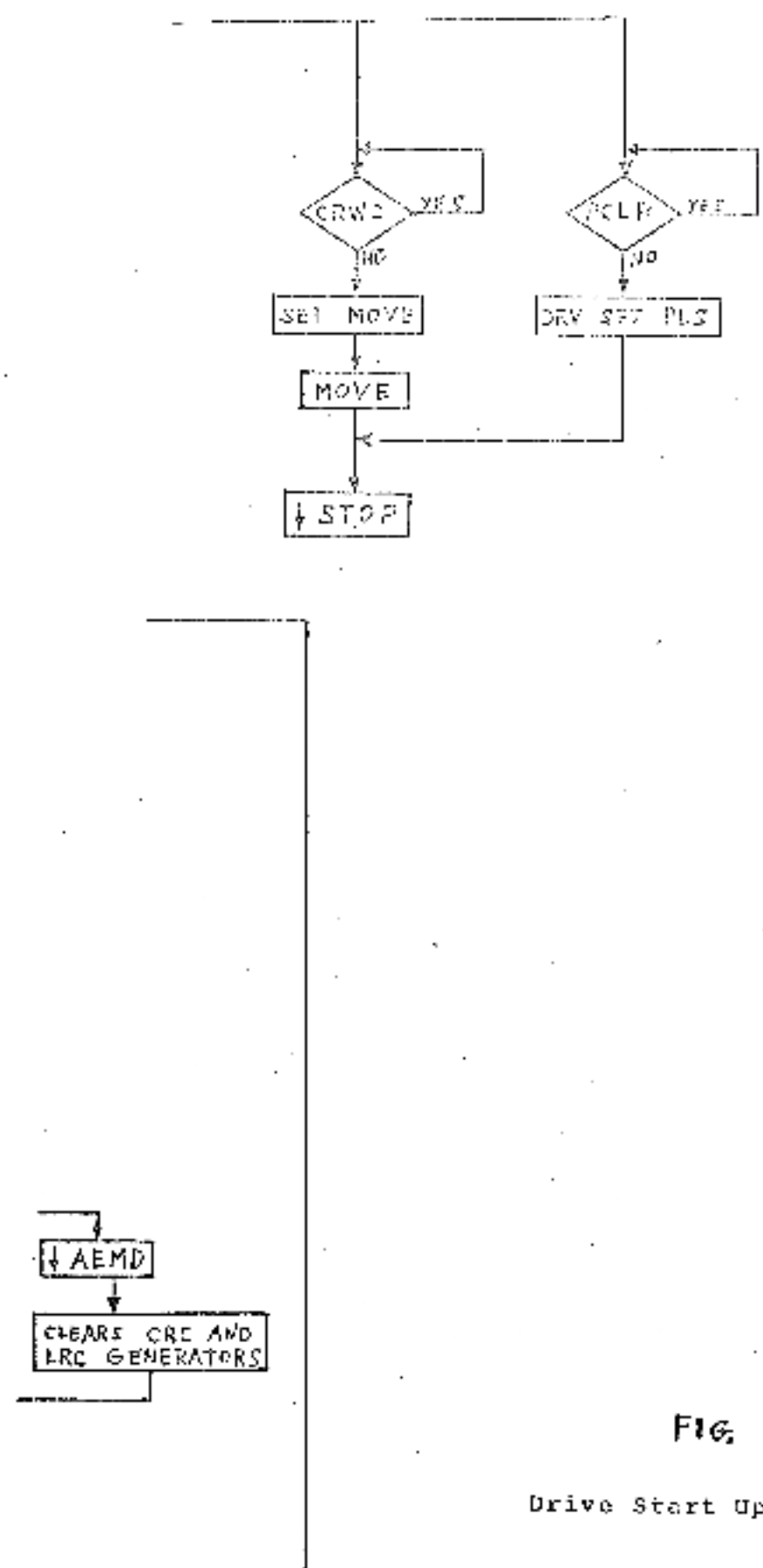
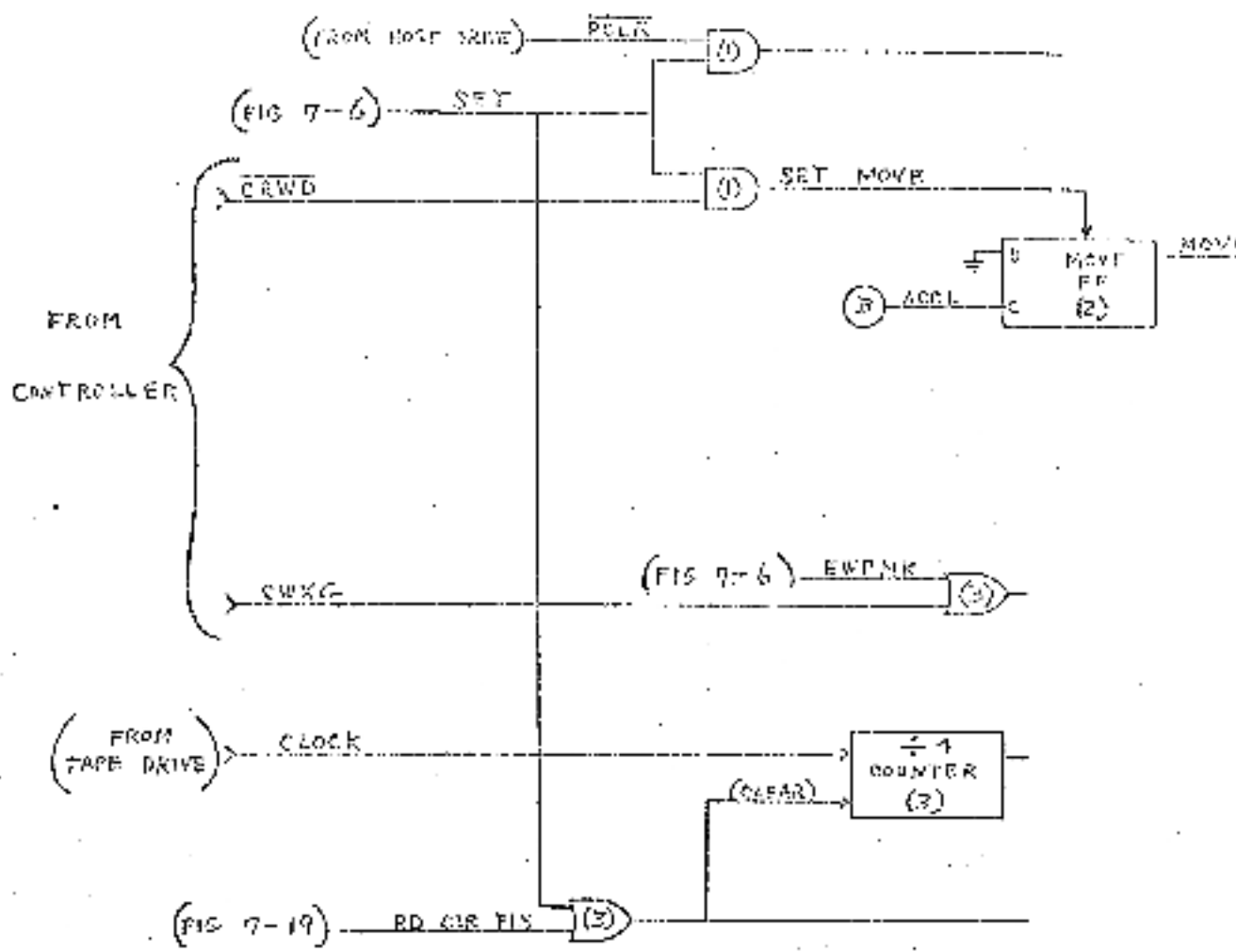


FIG. 7-8

Drive Start Up Flow Diagram



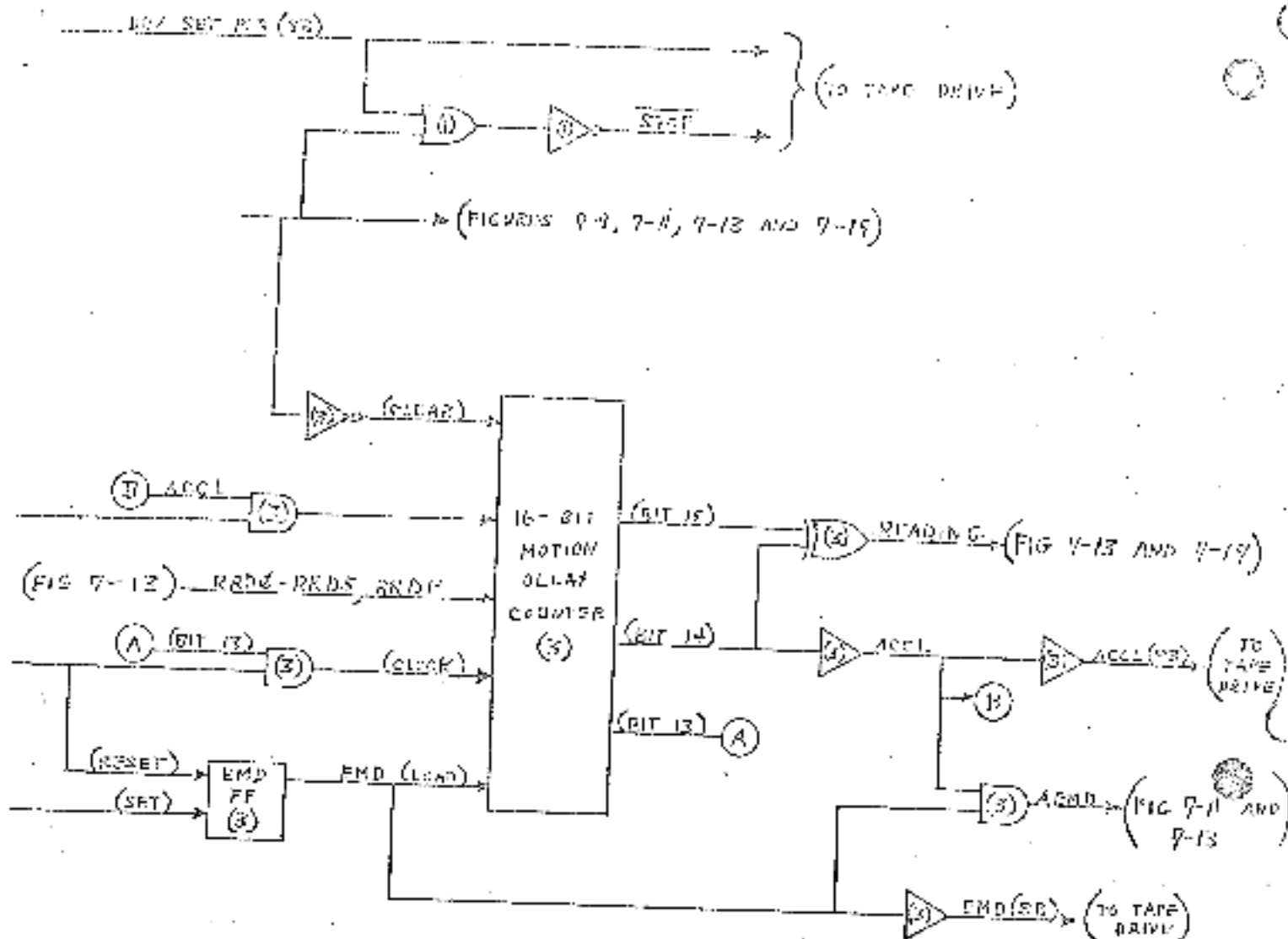


FIG. 7-9 Start/Stop Control Block Diagram

of WRITING loads the end of record counter which is preset to a count of 8. The 8 bit output from the counter gates a WRP CLK pulses from the drive to produce WRITE STROBE pulses. The assertion of each WRITE STROBE pulse will:

- a. latch up write data from the controller making it available to the drive via the output gates
- b. assert CURS to the controller
- c. assert REC to the drive and to the CRC generator.

Vertical parity is produced by a parity generator which monitors the 8 write lines and outputs a true or false parity bit according to the number of 1 bits and whether odd or even parity is specified (EPPVN).

The write logic contains a circuit to detect a zero-character condition when even parity is specified. Such a condition results in a blank space on the tape which can not be sensed by the read logic. Should an attempt be made to write a zero character with even parity the zero character detector output would assert WRXZ thereby generating a 1 bit on the third write channel. A single bit character demands a 1 parity bit when EPPVN is true. The parity bit is also artificially generated via the zero character detector output which asserts WRXP to the parity write channel.

The CRC generator receives each data character from the write channels. REC pulses clock the generator which develops the CRC character during the body of the record.

7.4.1.2 Write End of Record

When the data transfer has been completed the controller negates **WRITE STROBE**. The next **WRITE CLK** pulse produces **WRITE STROBE** which latches up the last data character, and issues a **CHAR STRB** pulse and a **RFC** pulse. The **WRITE CLK** pulse also resets the **WRITING** flip-flop. When **WRITING** negates:

- a. **CHAR STRB** pulses to the controller are inhibited
- b. **RFC** pulses to the drive are inhibited
- c. the end of record counter is enabled

WRITE STROBE pulses clock the end of record counter. When the counter reaches a count of 3, **CHK CHAR STRB** asserts and:

- a. switches the CRC character onto the write lines via the write data/CRC mux
- b. enables the **REC AND** gate

The next **WRITE STROBE** pulse latches up the CRC character and generates a **REC** pulse for the drive to record the CRC character. Three **WRITE STROBES** later the counter is at a count of 7 and again asserts **CHK CHAR STRB** which:

- a. enables the **REC AND** gate
- b. asserts **LRC STROBE** via the enabled **LRC STROBE AND** gate.

LRC STROBE asserts **LRC STRB** to the drive, and resets the write data latch up register setting all the write lines to zero. (The **LRC** character is generated in the drive). The next **WRITE STROBE** asserts **REC** to record the **LRC** character, and resets the end of record counter thereby inhibiting any further **WRITE STROBE** pulses.

7.4.2 Seven Track Normal

Seven track normal operation is identical to nine track normal except for the write end of record sequence. In seven track operation both

the 4 and the 8 bits of the end of record counter are preset to a 1. Thus when the counter reaches a count of 3 the same conditions exist as a count of 7 in nine track operation. The seven track end of record sequence is:

- a. the last data character
- b. three blank spaces
- c. the LRC character
- d. reset end of record counter to terminate the write sequence.

7.4.3 Nine Track File Mark

7.4.3.1 Write Data

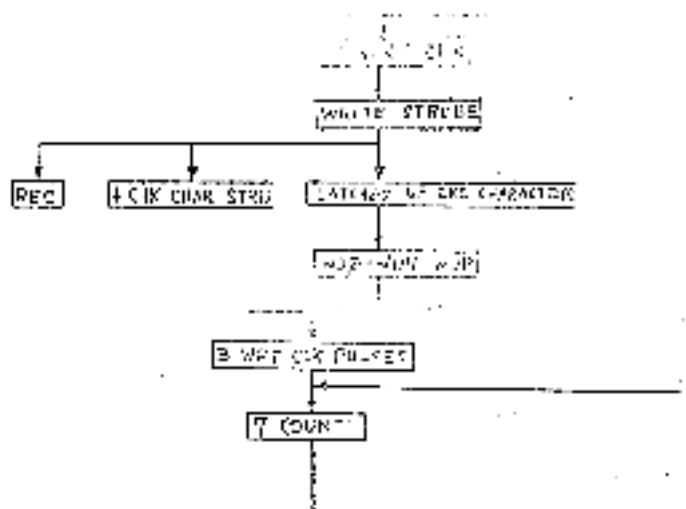
In file mark operation, \overline{EWFMK} is true and forces the write data/CRC mux to output all 1s on the write lines. After the 1s are latched up in the latch up register they are applied to the output gates. \overline{EWFMK} enables gates 3, 1 and 4 thus outputting an octal 23 (nine track file mark) to the drive.

\overline{CWRE} is true and \overline{CWDR} is false for a \overline{CWFMK} command. \overline{CWRE} allows the SET pulse to set the WRITING flip-flop. The first WRT CLK pulse asserts WRITE STROBE but, due to \overline{CWDR} being false, resets the WRITING flip-flop. Thus one WRITE STROBE is issued for the file mark character.

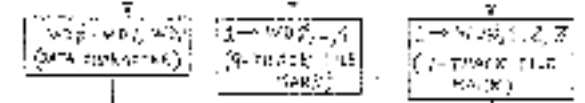
No \overline{CWRE} pulses are returned to the controller in file mark operation.

7.4.3.2 Write End of Record

The write end of record sequence for a nine track file mark is identical to the write end of record sequence for nine track normal except that the CRC character is skipped and only the LRC character is written. The end of record



PAGES ARE
GENERATED



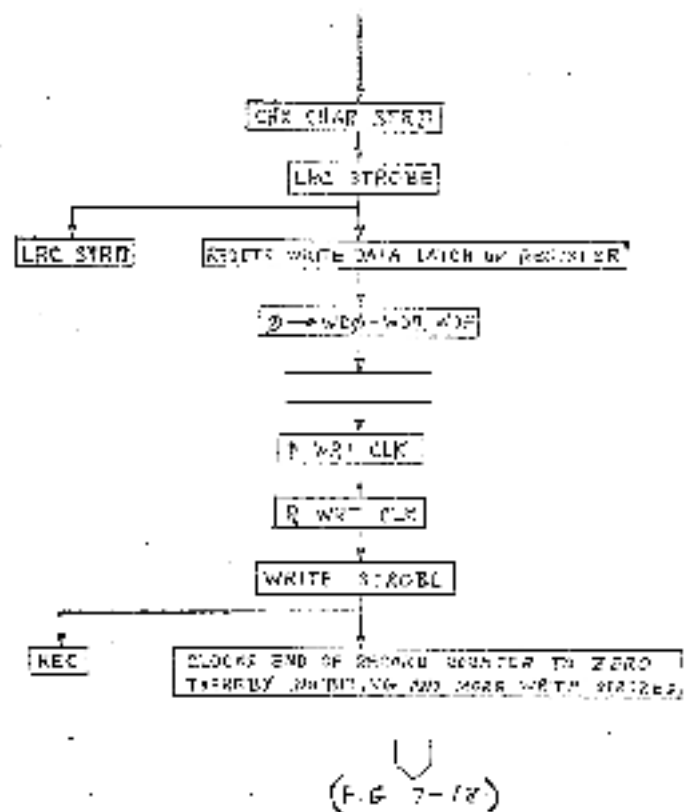
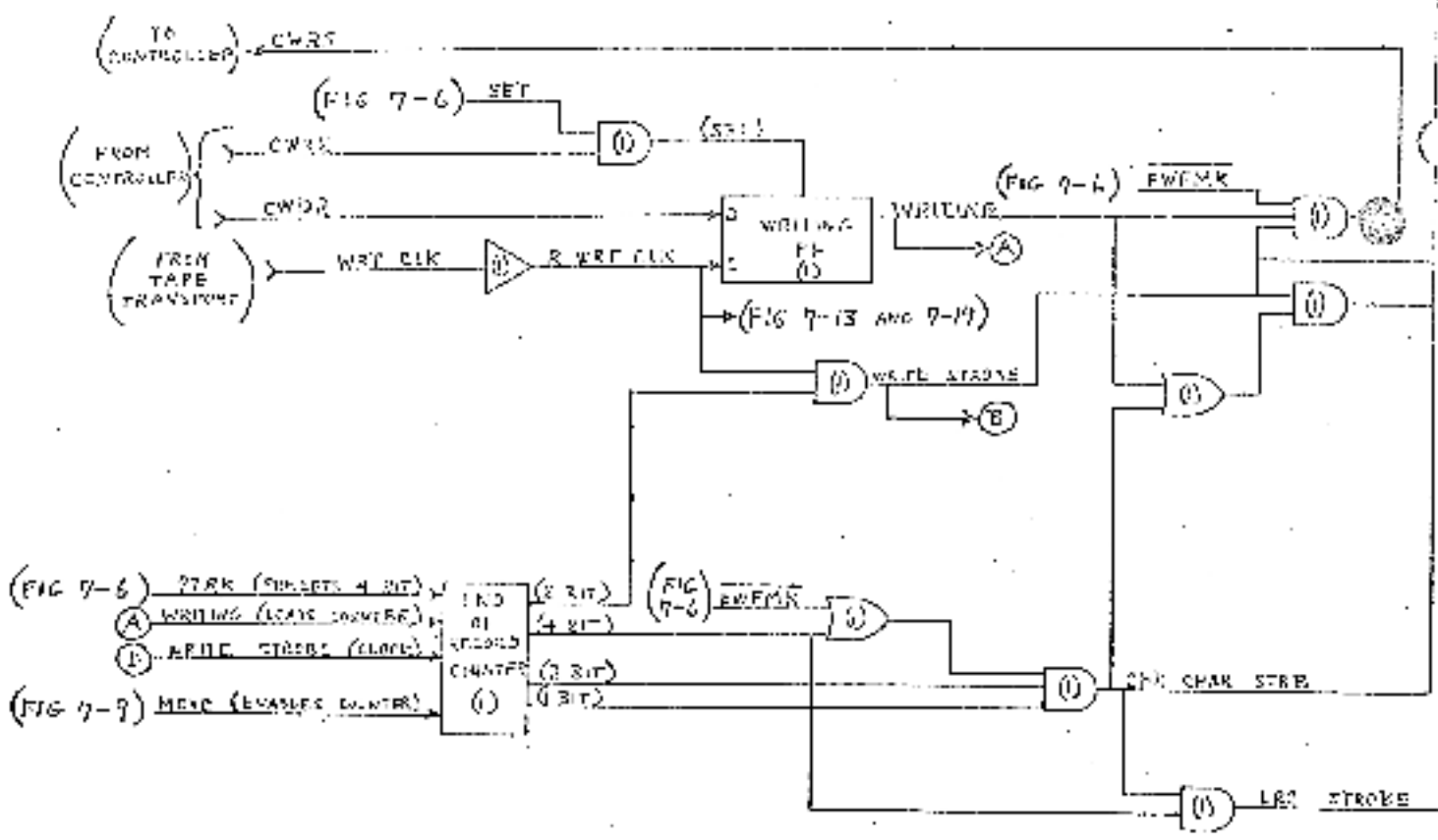
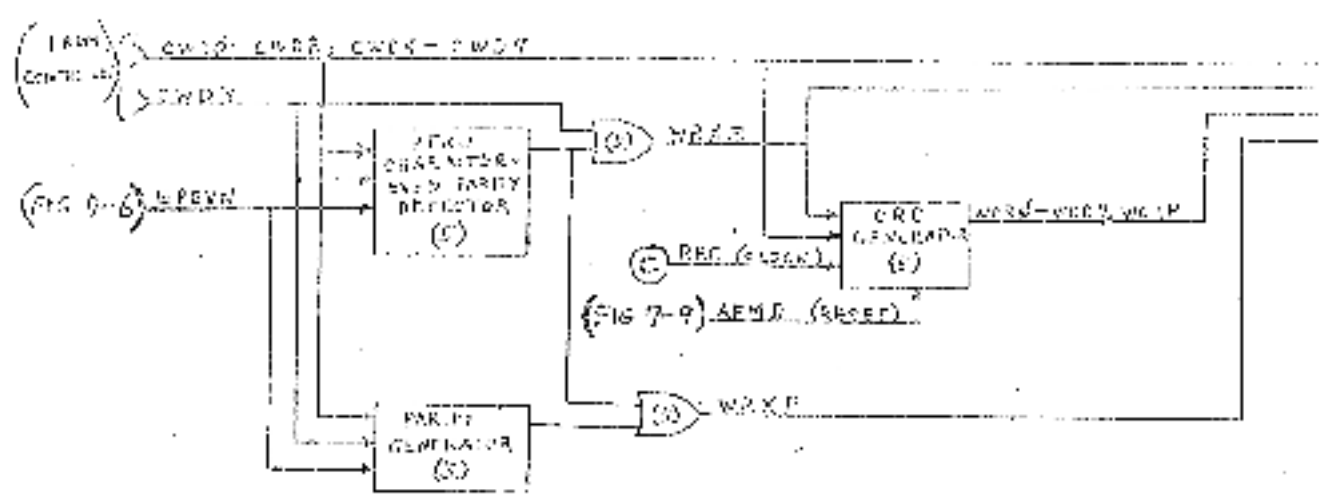


FIG. 7-10 Write Flow Diagram

(FIG 7-6)



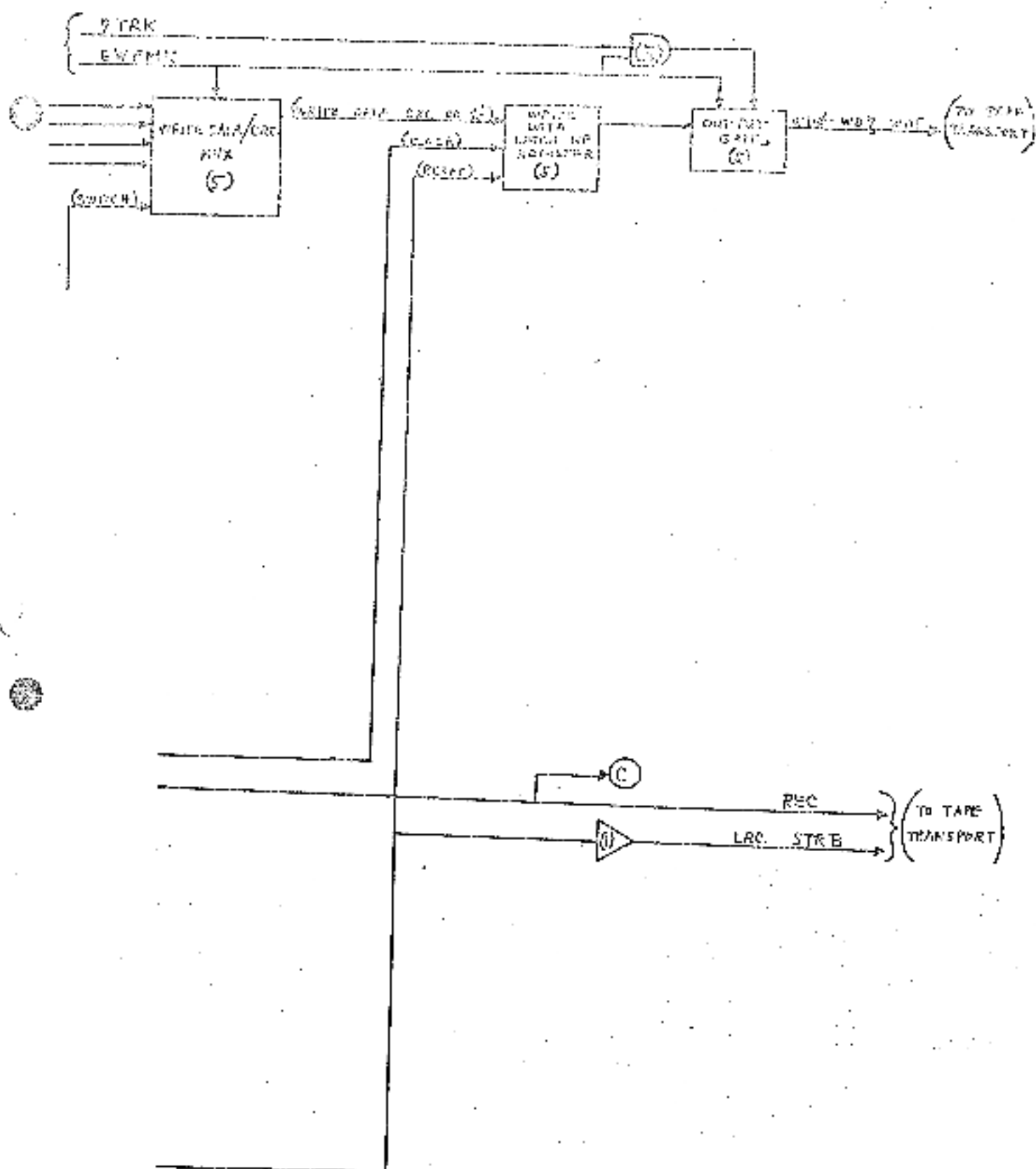


FIG. 7-11 Write Block Diagram

counter must reach a count of 7 before a CNK CRD STRB is asserted. At this point the same conditions exist as in the nine track normal mode; thus the LSC character is recorded and the write sequence is terminated. The nine track file mark end of record sequence is:

- a. the last data character (the file mark character)
- b. seven blank spaces
- c. the LSC character
- d. reset end of record counter to terminate the write sequence

7.4.4 Seven Track File Mark

The write data sequence for the seven track file mark is identical to that for the nine track file mark except that 7TRK is asserted to the output gates via the enabled F7TRK gate.

Output gates now enabled are \bar{g} , 1, 2 and 3 thus outputting an octal 17 (seven track file mark) to the drive.

The end of record sequence for the seven track file mark is identical to that for a seven track normal sequence.

7.5 Read Sequence

7.5.1 Read Data (Figures 7-12 and 7-13)

RSDO pulses from the drive assert COMP RD STRB which:

- a. clocks the read data latch up register
- b. triggers the read strobe one-shot asserting CRDS to the controller
- c. uses a second output from the read strobe one-shot (CHECK REG PLS) to clock the IRC generator (and the LRCS flip-flop in the end of record detection sequence, paragraph 7.5.4).

when the read data latch up register is clocked by COMP RD STRB read data is made available to the controller via the read data output mux. When READING is true the mux selects the data character from the read lines for the controller. When READING is false (not during a normal data transfer) the LRC character is output to the controller for maintenance purposes.

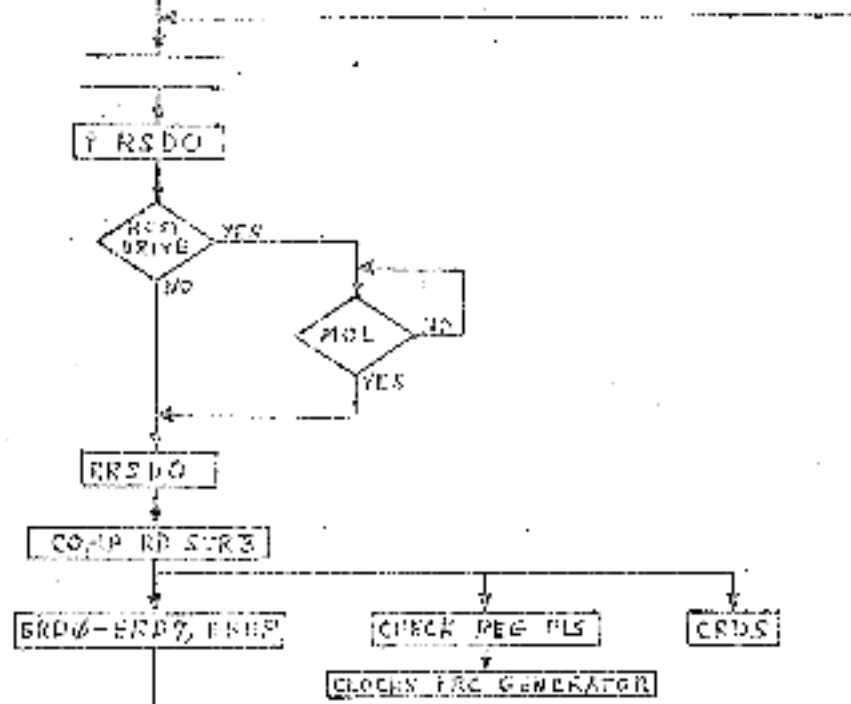
7.5.3 Error Detection (Figures 7-12 and 7-13)

Read data ERD0-ERD7, ERDP is checked for CRC, LRC and vertical parity errors. Each data character is clocked into the CRC and LRC generators by the CRXCK R3C FLS. At the end of the record the CRC character is clocked into the CRC generator causing the CRG-CR7, CRP output to be all zeros. The CRC error detector looks for an all zeros character from the CRC generator at CRCS time. If the CRC generator output is not all zeros when CRCS is true, CCRC is asserted to the controller indicating a CRC error.

In a similar manner, the LRC character is clocked into the LRC generator causing the LRG-LR7, LRP output to be all zeros. The LRC error detector looks for an all zero character from the LRC generator at LRCS time. If the LRC generator output is not all zeros when LRCS is true, CLRC is asserted to the controller indicating an LRC error.

CRC and LRC error outputs are enabled only when the drive is executing a forward motion command. (This is due to the location of the CRC and LRC characters at the end of the record.) Accordingly EFOR must be true for CCRC or CLRC to assert.

(FIG 7-2)



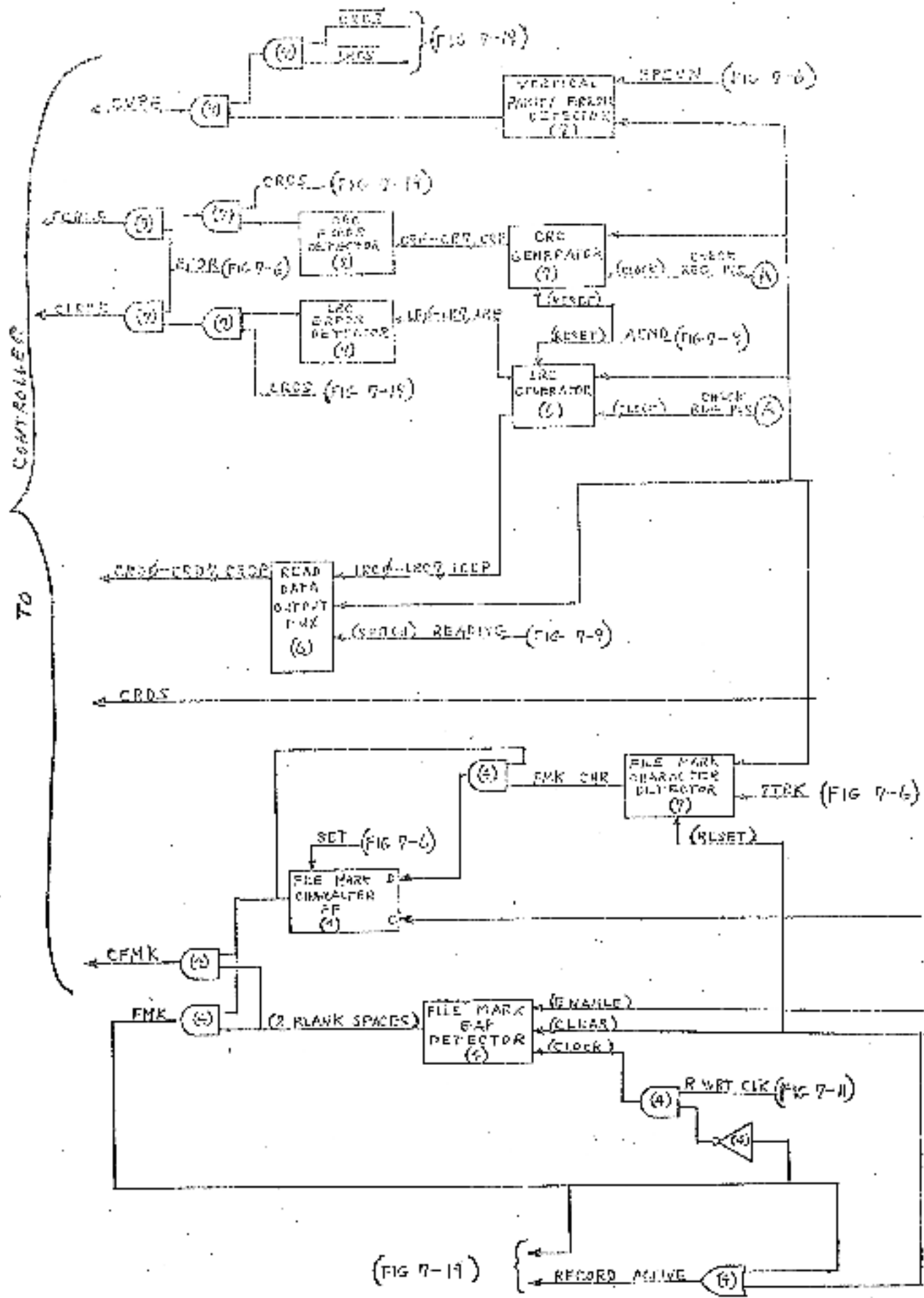
Each data character occurring during the body of a record is checked for vertical parity error by a vertical parity error detector circuit. If a parity error is sensed by the detector CVPE is asserted to the controller. CVPE is inhibited during CRC and LRC lines as no vertical parity check is made on the CRC and LRC characters.

7.5.3 File Mark Detection (Figures 7-12 and 7-13)

The file mark detection logic monitors the read data and outputs CPMK to the controller if a file mark is detected. Three conditions must be met before the record is identified as a file mark. These are:

- a. there must be two characters and only two characters to the record
- b. both characters must be file mark characters
- c. the second file mark character must be followed by eight blank spaces

To meet condition b, read data (ERD₀-FRD₇, ERDP) is examined by the file mark character detector which outputs FMK CHR if a file mark character is sensed. A file mark character flip-flop is set by the SET pulse at the start of the operation and then clocked by ERSD₀ pulses. The flip-flop is conditioned to set by FMK CHR, via an AND gate, such that if the flip-flop is clocked to the reset state it cannot be set again during the current operation. Thus the first two characters read must be file mark characters in order to keep the file mark character flip-flop set.



Conditions 8.000 & are met by means of a file mark gap detector and a read strobe counter. When the read strobe counter reaches a count of two the file mark gap detector is enabled and starts counting R WRT CLK pulses. When the strobe counter reaches a count of three, RSDO₂ asserts and resets the gap detector. If the gap detector reaches a count of eight it outputs 6 BLANK SPACES and CMNK is asserted to the controller via an enabled AND gate. If a third RSDO pulse occurs before the gap detector reaches eight, the detector is cleared and the file mark character flip-flop is reset indicating that the record is not a file mark and a normal record transfer is in progress.

The end of record detection sequence is enabled from the read data channels via a record active OR gate. If a normal record transfer is in progress (RSDO₂ is true) or a file mark has been detected (FMK true), RECORD ACTIVE is asserted and enables (but does not start) the end of record detection sequence.

7.5.4 End of Record Detection (Figures 7-18 and 7-19)

7.5.4.1 Nine track Normal (Figure 7-14)

The end of a record is detected by looking for the three blank spaces that occur between the last data character and the CRC character (LRC character for seven track). The blank spaces are detected by an end of record counter which is clocked by R WRT CLK pulses and effectively reset by COMP RD STRB pulses. (Actually the COMP RD STRB pulses load

the counter with a count of 3.) COMP RD STROB pulses are asserted by RSDO pulses from the drive. The R WRT CLK pulses and the RSDO pulses are not necessarily in sync but they are of the same frequency. Hence the end of record counter is continually being clocked and "reset" during the body of a record. Two R WRT CLK pulses might occur in between two RSDO pulses thereby clocking the counter to a count of two before it is reset, but it should never reach a count higher than two during the body of a record. If the counter does reach a count of three (three R WRT CLK pulses with no RSDO pulse) 3 COUNT is asserted signifying that this is the end of the record and the end of record sequence is started.

The assertion of 3 COUNT clocks the CRCS flip-flop set outputting CRCS to the controller indicating that the next character will be the CRC character. The next RSDO pulse will be the CRC character strobe which will:

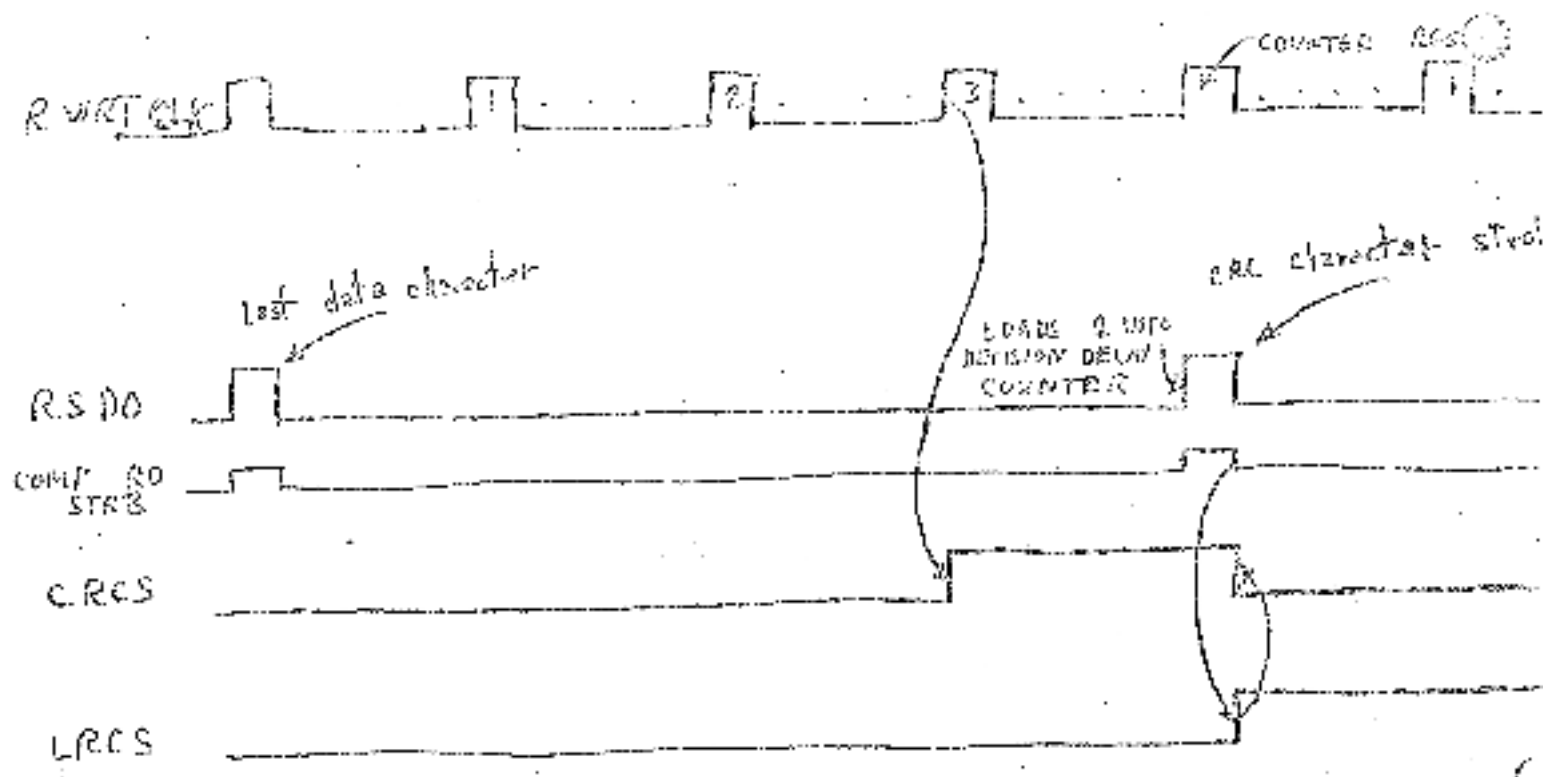
- a. latch up the CRC character in the read data latch up register
- b. "reset" the end of record counter
- c. assert CRDS to the controller
- d. assert CHECK REC PLS which clocks the LRCS flip-flop set

The asserted output of the LRCS flip-flop will reset the CRCS flip-flop and assert CLRCS to the controller indicating that the next character will be the LRC character. The next RSDO pulse will be the LRC character strobe which will:

- a. latch up the LRC character in the read data latch up register
- b. "reset" the end of record counter
- c. assert CRDS to the controller
- d. assert CHECK REC PLS which resets the LRCS flip-flop

The negation of LRS sets the end of record flip-flop asserting END OF RECORD which locks the CRC flip-flop in the read state until the next operation.

When END OF RECORD asserts a decision delay period begins. The decision delay period is a time interval (normally 8 RWT CLK pulses long) between the assertion of END OF RECORD and the assertion of RD CLK PLS. The delay period is a "last chance" look for more RSDO



(END OF RECORD)

RD CLR PLS

1961-11-11

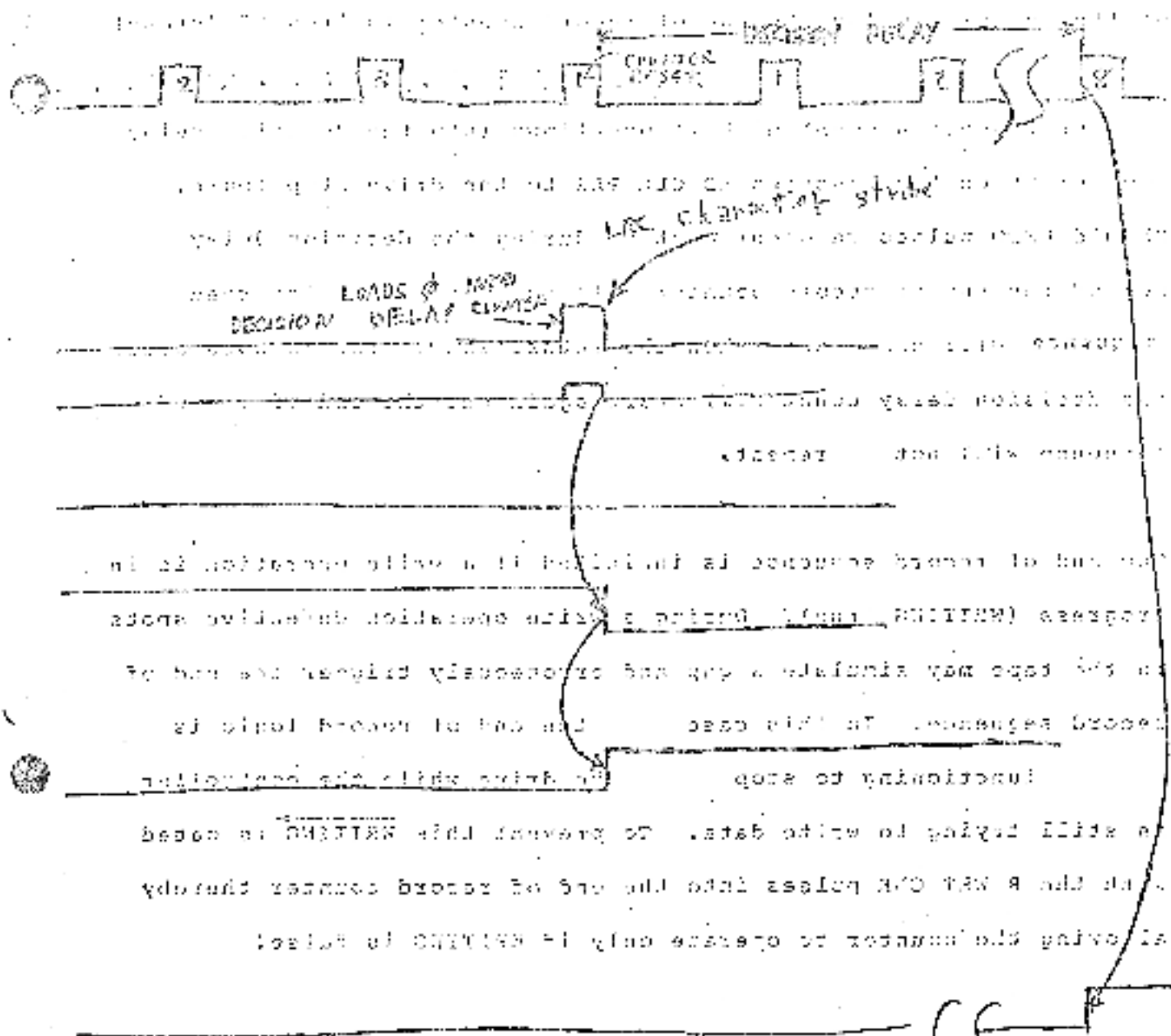


FIG. 7-14 End of Report Timing, Non-zero CRC, and LRC

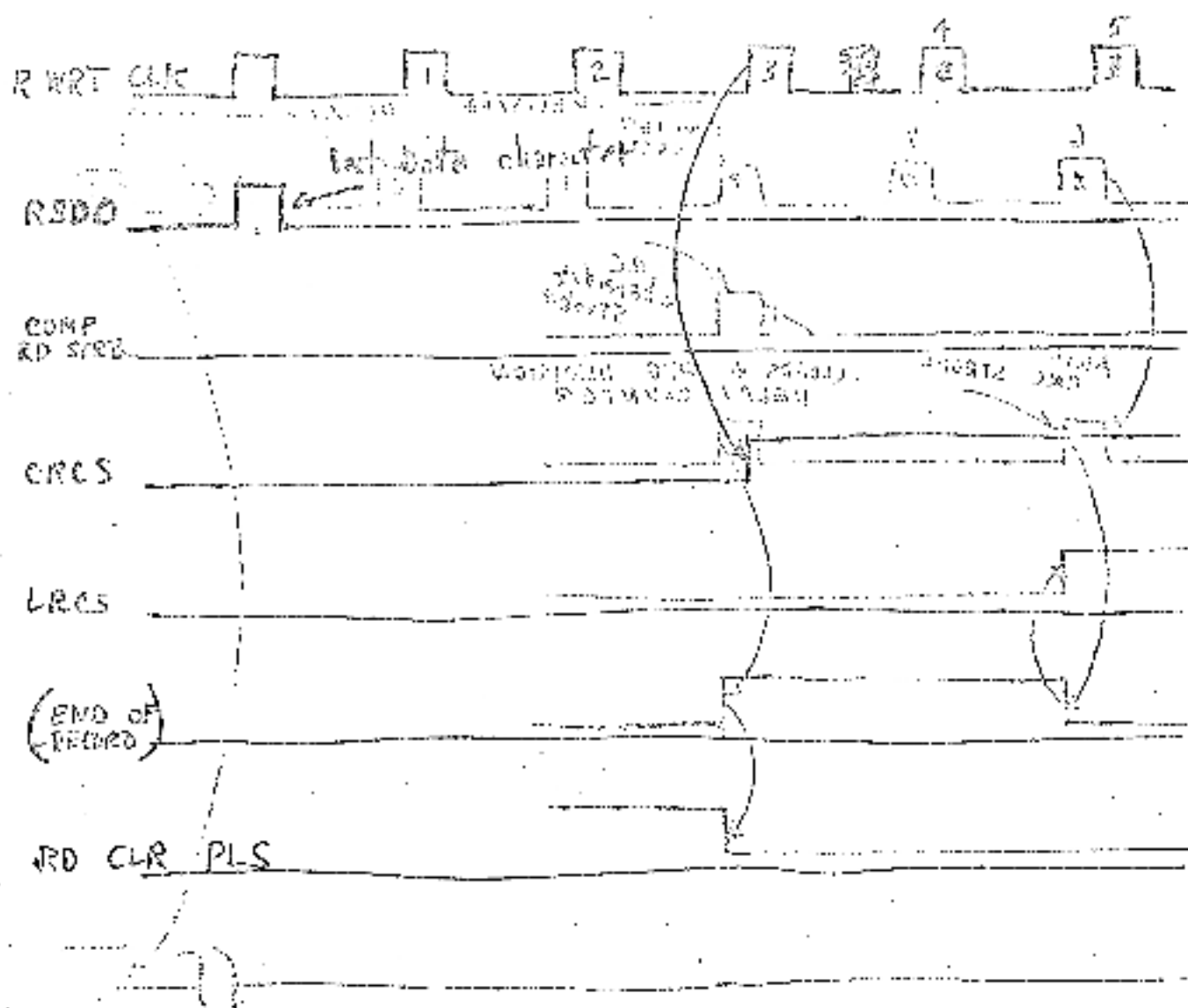
...in possible that the CRC or the LRC character could be a zero character ...
 ...no corresponding CRC value being received from the drive ...
 ...at the end of record sequence ...
 ...received to "report" the end of record sequence ...
 ...at six at which time COMB RD STRT will be asserted ...
 ...provided by COMB or DRCR. Timing 7-13 and 7-14 illustrate respectively ...
 ...the timing sequence for a zero CRC and a zero LRC character.

pulses before triggering the drive stop sequence. At the start of the decision delay the end of record counter is "reset" (reset to a count of 0) and starts counting RSDO pulses. When the counter reaches a count of 6 it overflows into the decision delay counter which then asserts RD CLR PDS to the drive stop logic. Should RSDO pulses re-occur during the decision delay period the end of record counter will be "reset" and the read sequence will continue when the actual end of record does occur. The decision delay count will start again but the end of record sequence will not repeat.

The end of record sequence is inhibited if a write operation is in progress (WRITING true). During a write operation defective spots in the tape may simulate a gap and erroneously trigger the end of record sequence. In this case the end of record logic is functioning to stop the drive while the controller is still trying to write data. To prevent this WRITING is gated with the R WRT CLK pulses into the end of record counter thereby allowing the counter to operate only if WRITING is false.

7.5.4.2 Zero CRC or LRC Characters

It is possible that the CRC or the LRC character could be a zero character resulting in no corresponding RSDO pulse being received from the drive. In this case a COMP RD STRB pulse is generated artificially so clocking of the end of record sequence can continue. If no RSDO pulse is received to "reset" the end of record counter counting will continue up to six at which time COMP RD STRB will be asserted via a gate enabled by CRCS or LRCS. Figures 7-15 and 7-16 illustrate respectively the timing sequence for a zero CRC and a zero LRC character.



File 7-19 of Record Keeping Case 7-39

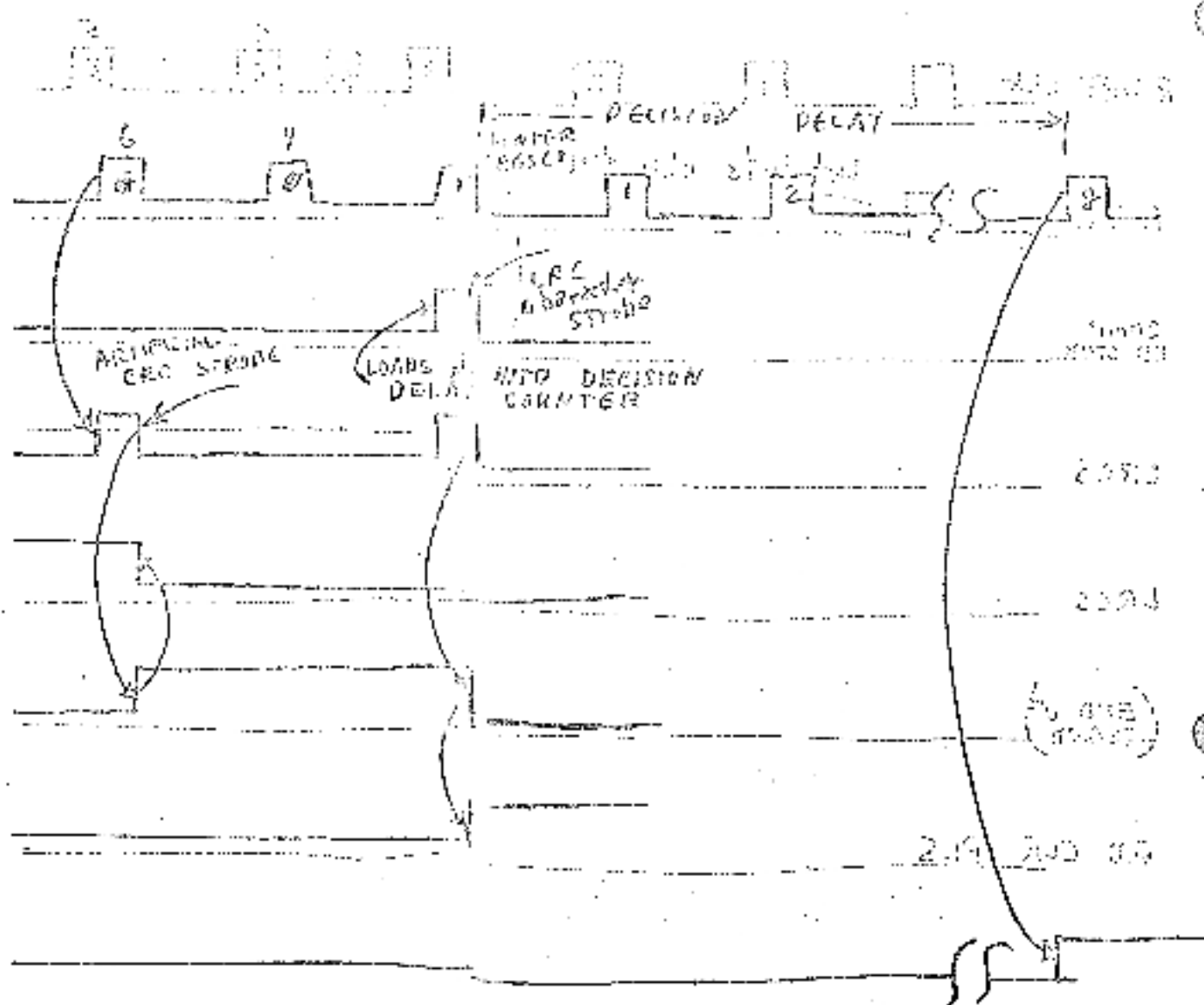
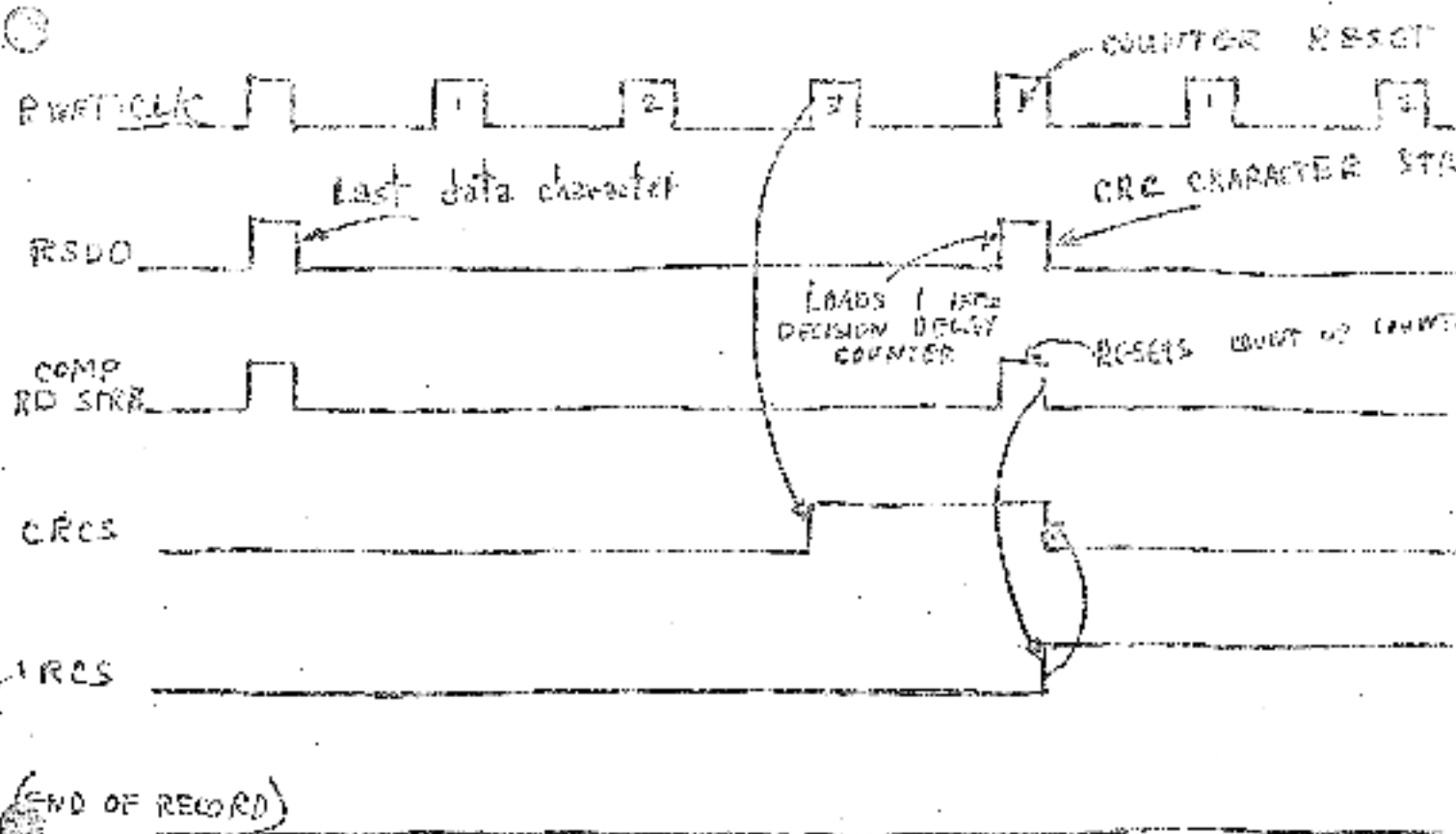


Fig. 7-13 End of Record Timing, Zero CRC



RD CLR PLS

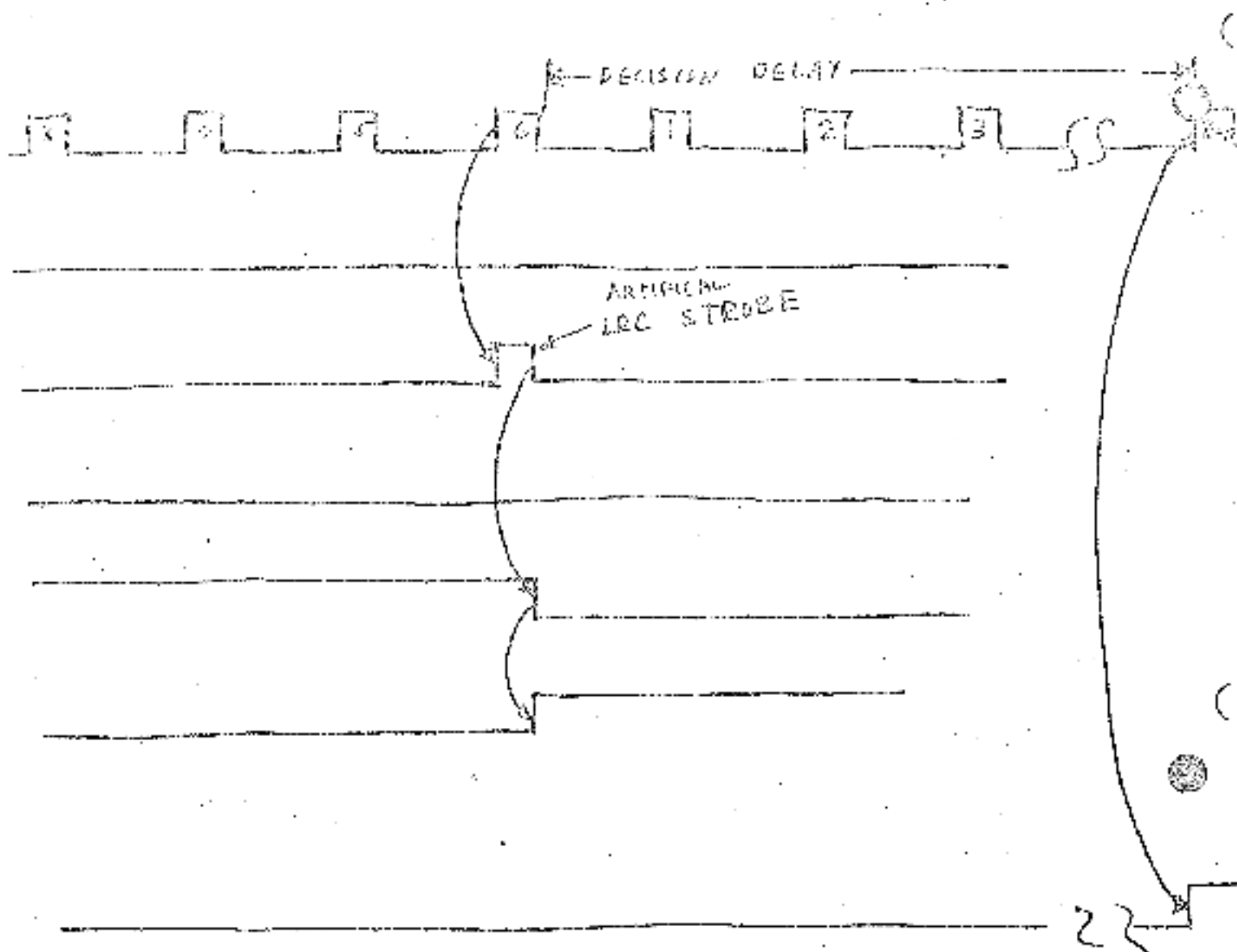


FIG. 7-16 End of Record Timing, Zero LRC

The decision delay is normally eight R WKT CLK pulses long but is extended to 24 pulses if no LRC character is detected. Failure to detect an LRC character may be due to the character being zero but it could also be due to a bad area in the tape. Thus when an LRC character is detected some doubt exists as to whether the end of the record has been reached.

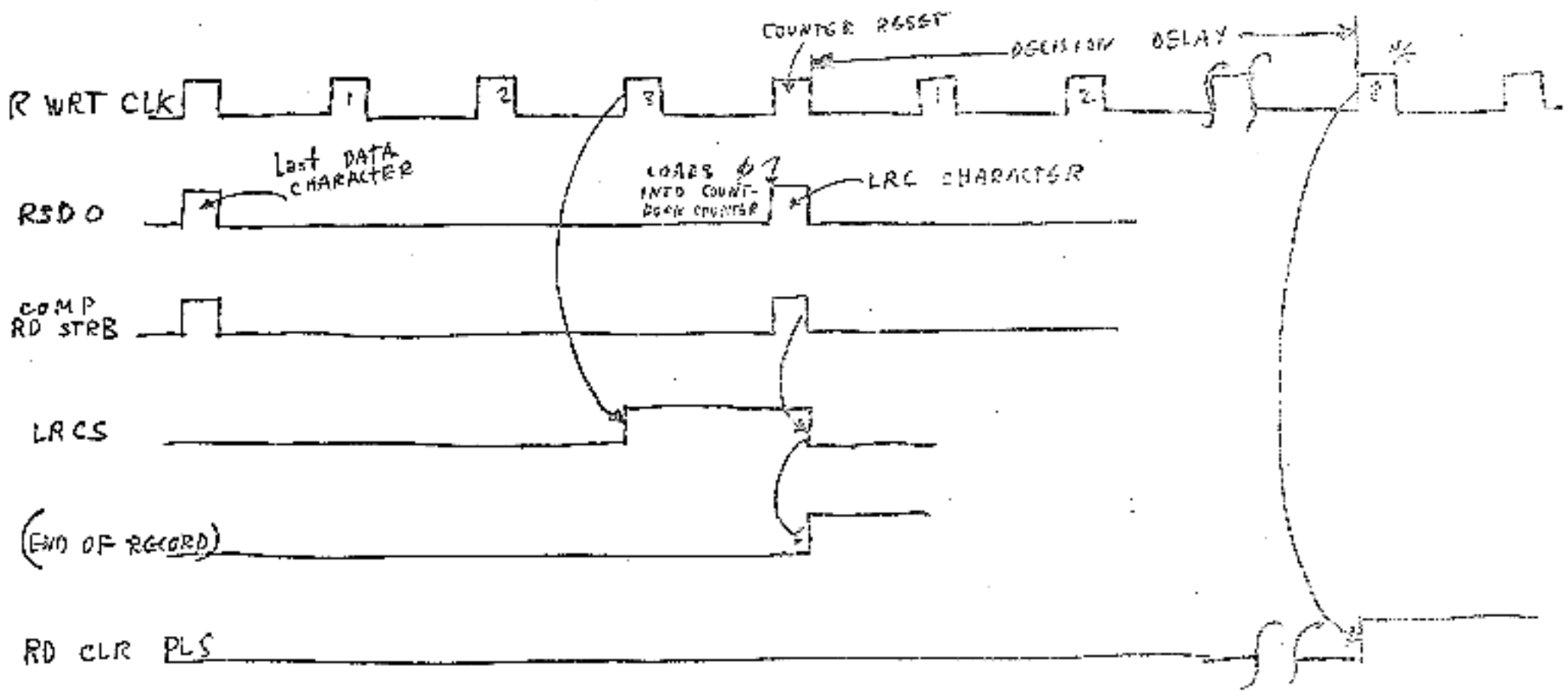
Extending the decision distance to 24 pulses provides extra assurance that the end of the record has been reached. The decision delay counter is a count down counter which is loaded by each RSDO pulse. The counter is loaded with zeros except for the 1 bit which is loaded with \overline{LRCS} . If there is an LRC character then LRCS is true during the last RSDO pulse (Figure 7-14) and the counter is loaded with all zeros. If there is no LRC character then LRCS is false during the last RSDO pulse (Figure 7-16) and the delay counter is loaded with a 1. In this case the end of record counter must count an additional 16 pulses to count down the 1 and assert RD CLR PLS.

7.5.4.3 Seven Track and File Mark (Figure 7-17)

In seven track or file mark operation the end of record sequence is modified to eliminate the CRC character from the sequence. With either FMK or 7TRK true the 3 count output from the end of record counter directly sets the LRCS flip-flop which in turn holds the CRCS flip-flop reset. Also, when in file mark operation, the decision delay is extended to 24 R WKT CLK pulses as there is no RSDO pulse associated with the assertion of LRCS.

7.6 Drive Stop (Figures 7-7, 7-9 and 7-20).

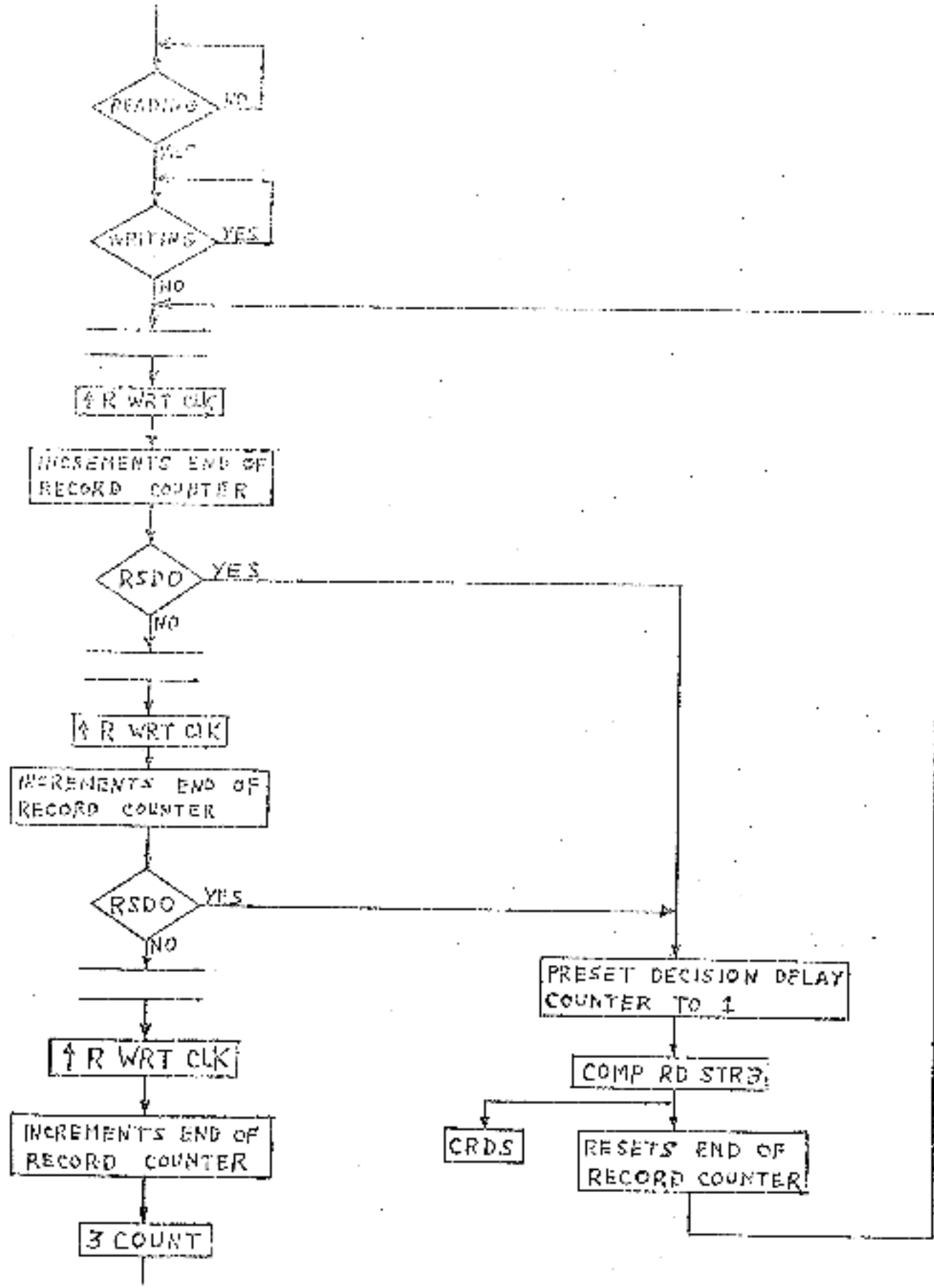
RD CLR PLS triggers the drive stop sequence by setting the EMD flip-flop and asserting EMD to the drive. The output of the EMD

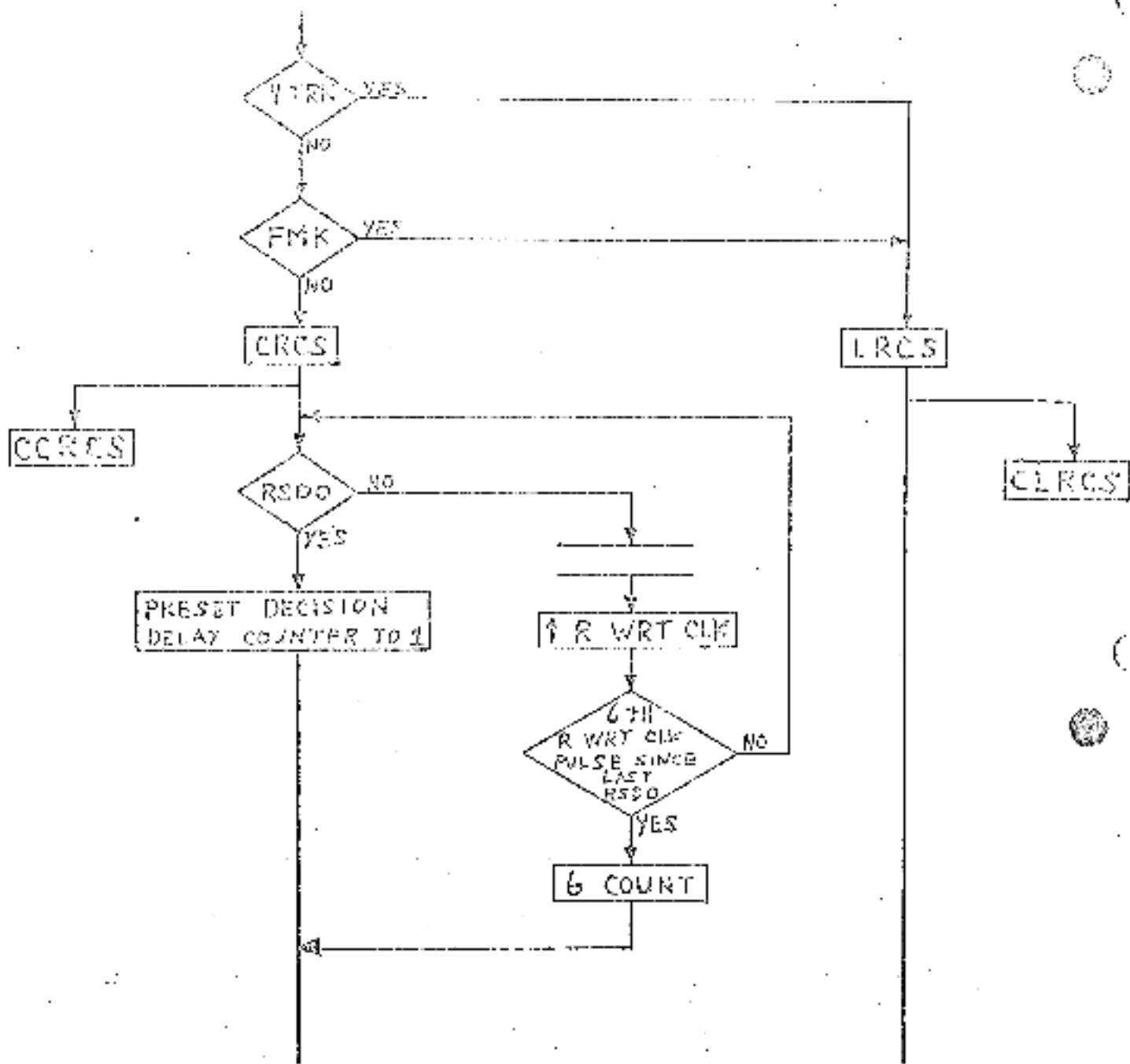


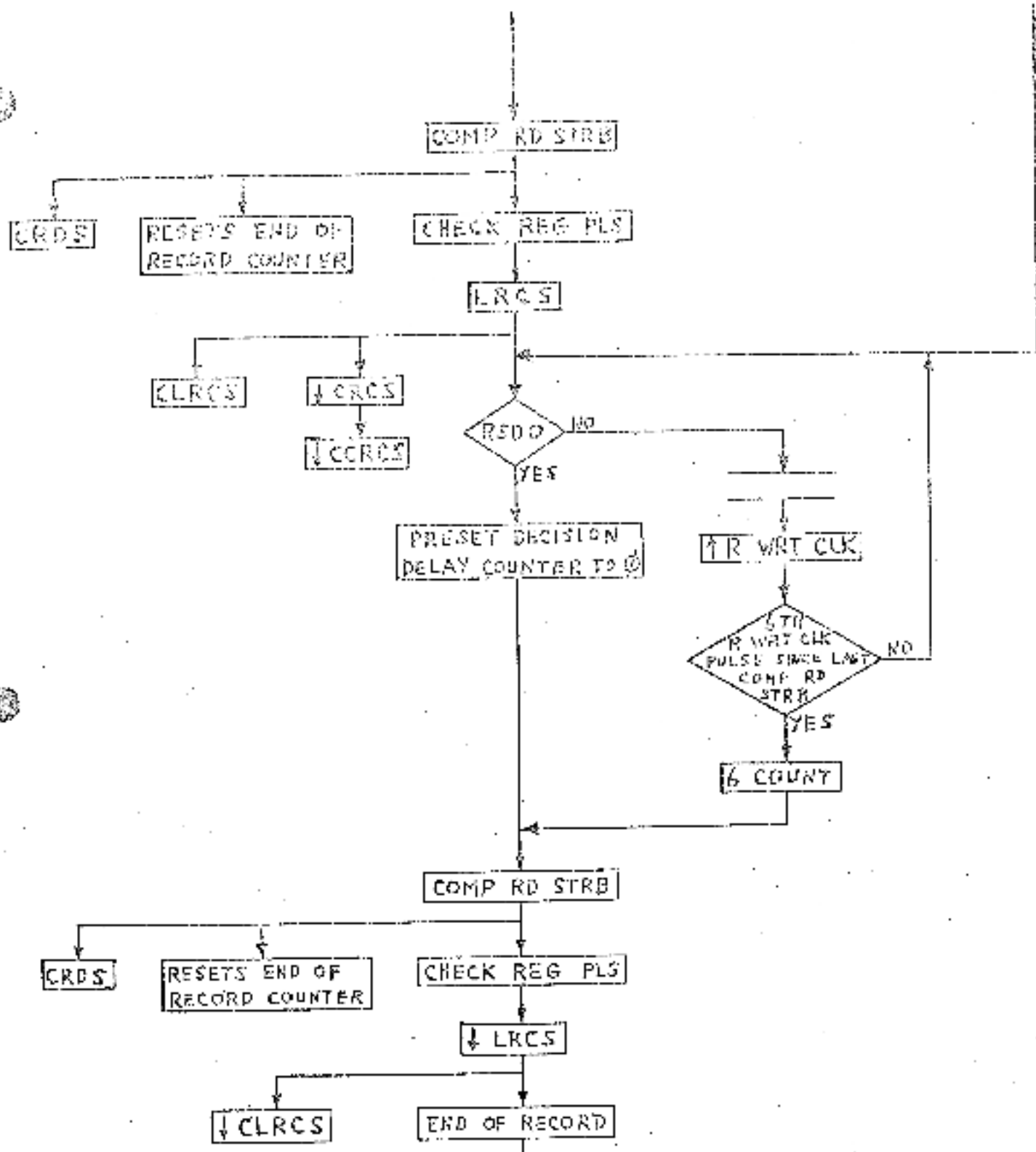
* Decision delay = 24 R WRT CLK pulses in File Mark Mode

FIG. 7-17 End of Record Timing, Seven Track and File Mark

(FIGURES 7-10 AND 7-12)







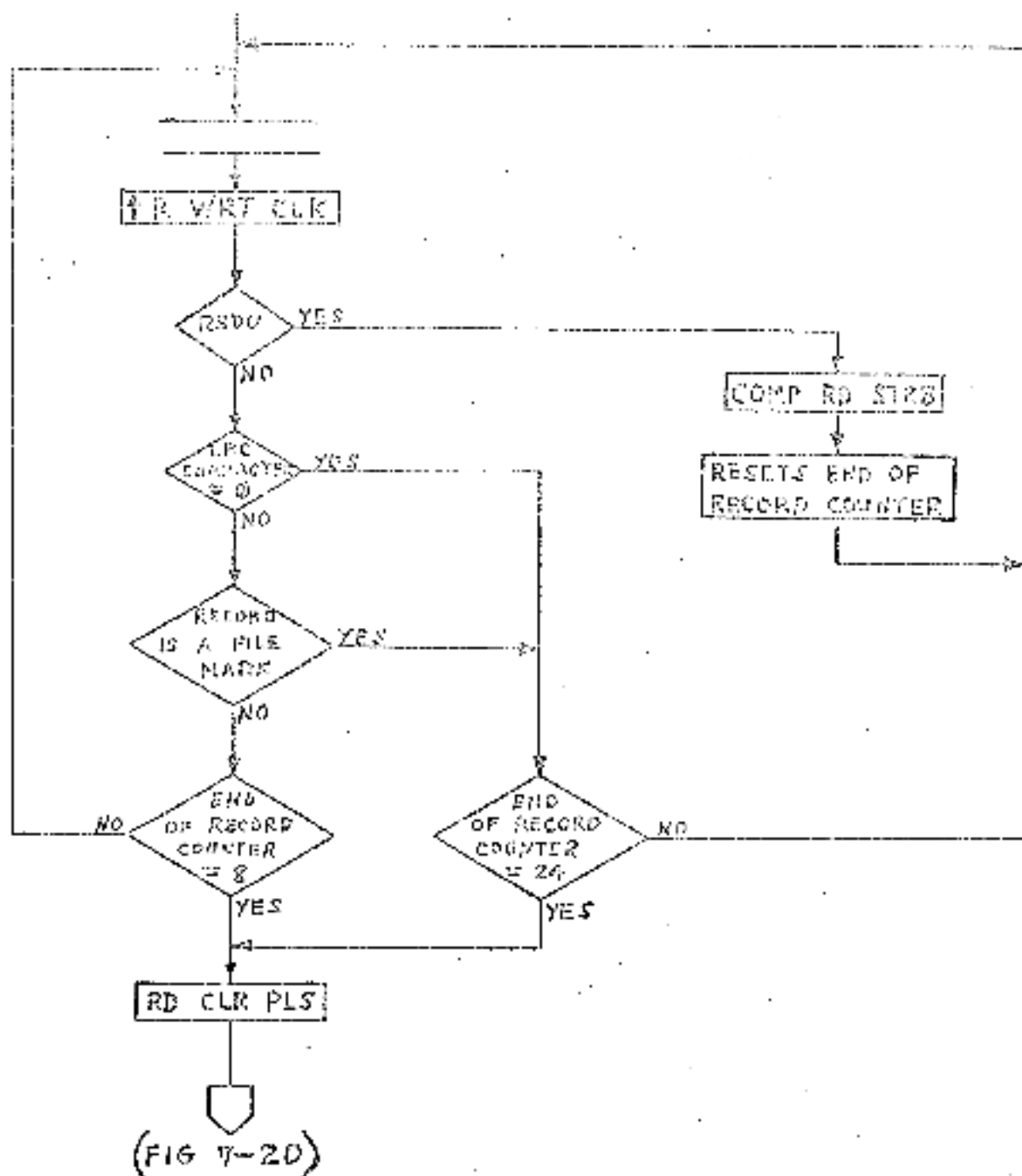


FIG. 7-10 End of Record Flow Diagram

FIG 7-18

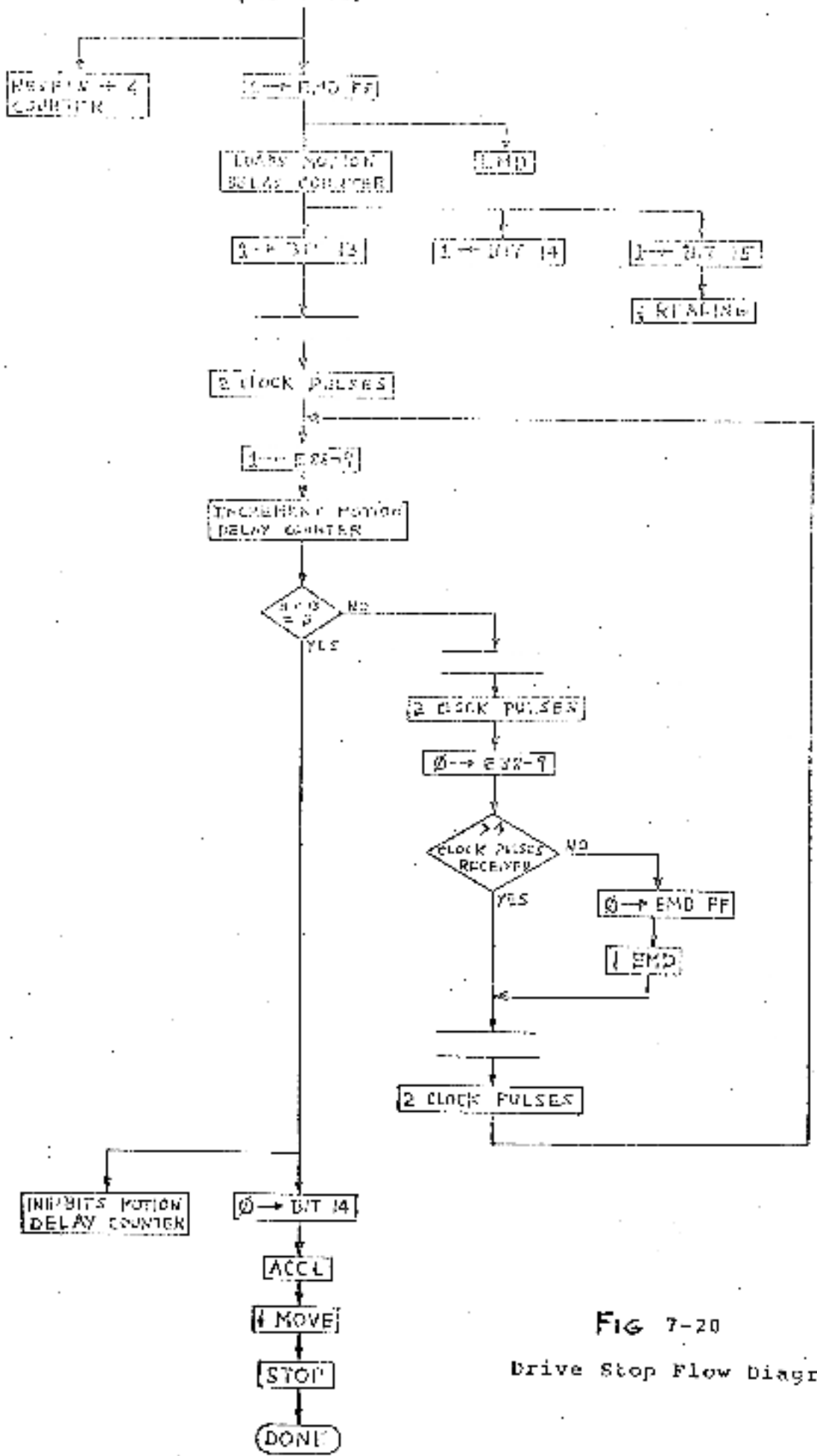


FIG 7-20
Drive Stop Flow Diagram

RDY also loads the motion delay counter with data set onto
lines RDY-RDY, RDY by the Drive. Bit 13 of the counter is
always a 1. The bit 13 output, which has been a 1 all during
the record transfer, is connected to the data input of bits 14 and
15. Thus when RDY loads the counter, output bits 13, 14 and 15
change to 1. READING negates due to exclusive ORing of output bits
14 and 15 while bit 13 gates clock pulses into the counter from the
4 counter. The 4 counter receives CLOCK pulses from the slave bus.
An output from the 4 counter is obtained after the first two
CLOCK pulses and every four CLOCK pulses thereafter. After 5.9 ms
the motion delay counter is clocked reset and:-

- a. input clock pulses to the delay counter are inhibited
(bit 13=0)
- b. ACCL is asserted to the drive (bit 14=0) and inhibits WRT
CLK pulses from the drive.

The assertion of ACCL resets the MOVE flip-flop which negates
MOVE and asserts STOP to the drive thereby terminating the command
operation.

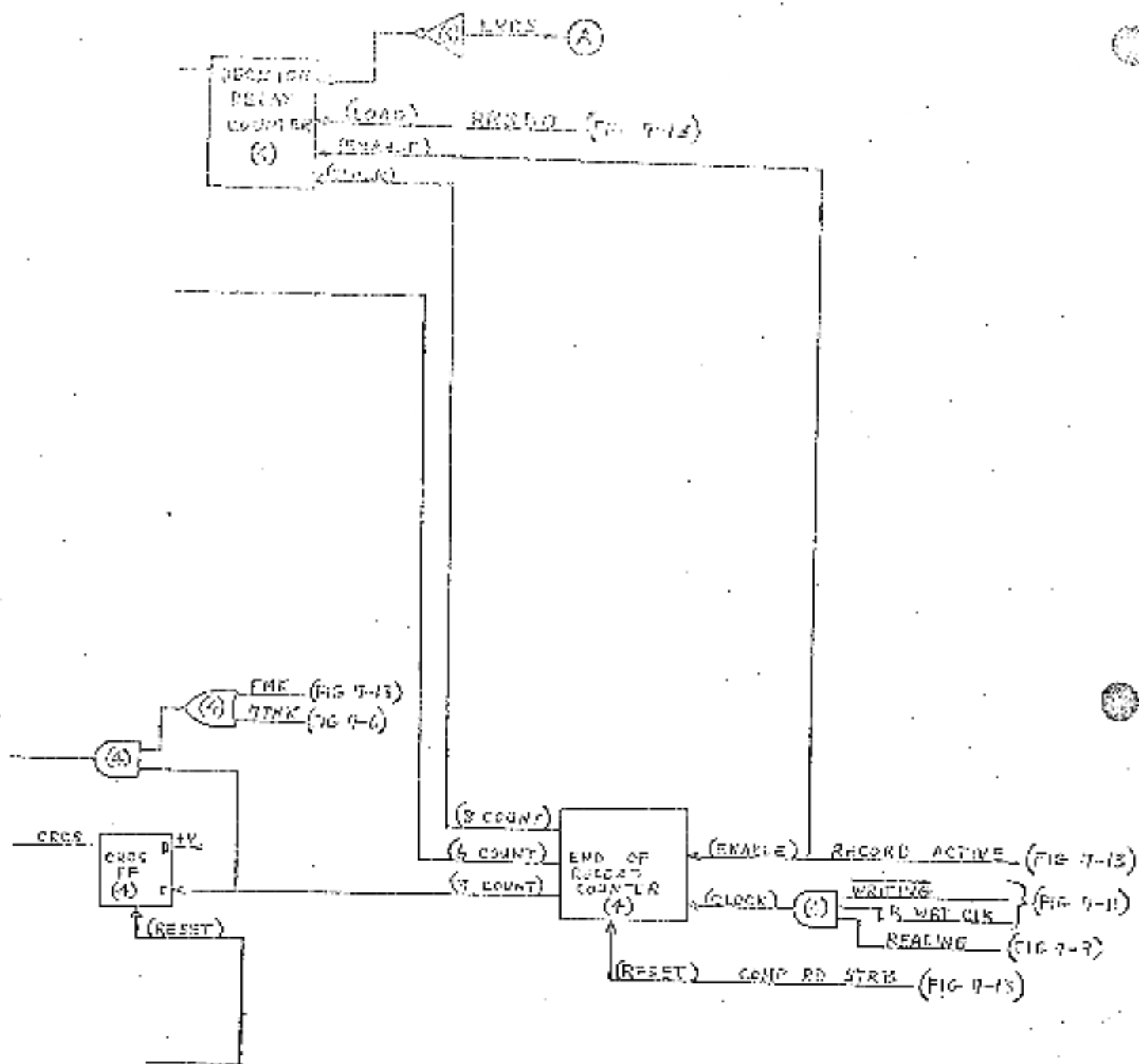


FIG 7-19 End of Record Block Diagram

CHAPTER 8

TU10W Transport Theory of Operation (TU16/TU10W differences)

8.1 General

In many areas the TU10W tape transport is identical to the TU16. Hence the reader is referred to the theory of operation, Chapter 2 of the TU-6/TM02 tape drive system maintenance manual (document No. ER-TU16-XB-002) for a functional description of the TU10W. The reader is also referred to Chapter 3 of the same manual for detailed discussions of the functional areas of the transport.

The paragraphs that follow are concerned with the differences between the TU10W and the TU16. They provide a supplement to the TU16/TM02 manual such that this manual together with the TU16/TM02 manual will provide full coverage of the TU10W tape drive transport. Paragraphs 8.2 through 8.5 cover the differences between the TU10W and TU16 transports. Paragraph 8.5 is an errata for the TU16/TM02 manual. It lists errors that were discovered in the TU16 manual and are being corrected, but will likely still be in the copy used by the reader of this preliminary manual.

8.2 Delete TM02

The TU10W does not contain the TM02 tape controller. Delete all descriptive theory that pertains to the TM02 tape controller.

8.3 Add M8926 Interface Module

The M8926 interface module (covered in Chapter 7 of this manual) is installed in the system unit of the master drive, replacing the M9001, M8913 and M9001-YA modules. (See Figure 2-14.)

3.15.2 Replace +5 Volt Regulator

The TU10 +5 regulator was redesigned to provide a greater output current capability. The new regulator (Figure B-1) supplies the extra power required for the W3926 module. Formerly the +5V regulator had a maximum current output of 4.8 A. The new regulator current output is rated at 6.0A maximum.

To incorporate the new +5V regulator, make the following changes to the information in the TU10/TX63 manual.

- a. Delete paragraph 3.15.2 and substitute the following:

3.15.2 +5VDC Regulator circuit

The +5Vdc regulator circuit is shown in Figure 3.15-3. Raw dc voltage is input to pins 11 and 12 of the 723 voltage regulator. The output voltage from pin 10 is fed to transistors Q6 and Q5, which are series regulators used to increase the current output capabilities of the circuit. Resistors R52 through R56 inclusive sense the output current. R52 is used as a current limit monitor by the 723. As the current increases, the voltage across R52 increases. When the reference voltage is exceeded, the 723 begins to turn off Q6 and Q5, impeding current flow. The current does not stop, but instead decreases to a safer level; this is called current foldback. It assures that the output current never goes over 6.0 A. Refer to Figure 3.15-4 which shows how the current foldback procedure works. As the current surpasses the limit of 6.0 A, the conduction of Q5 and Q6 slows down (toward being shut off) until no voltage is produced (at the short circuit current rating). The output voltage may be regulated. Resistors R58, R59 and R60 divide the actual output voltage.

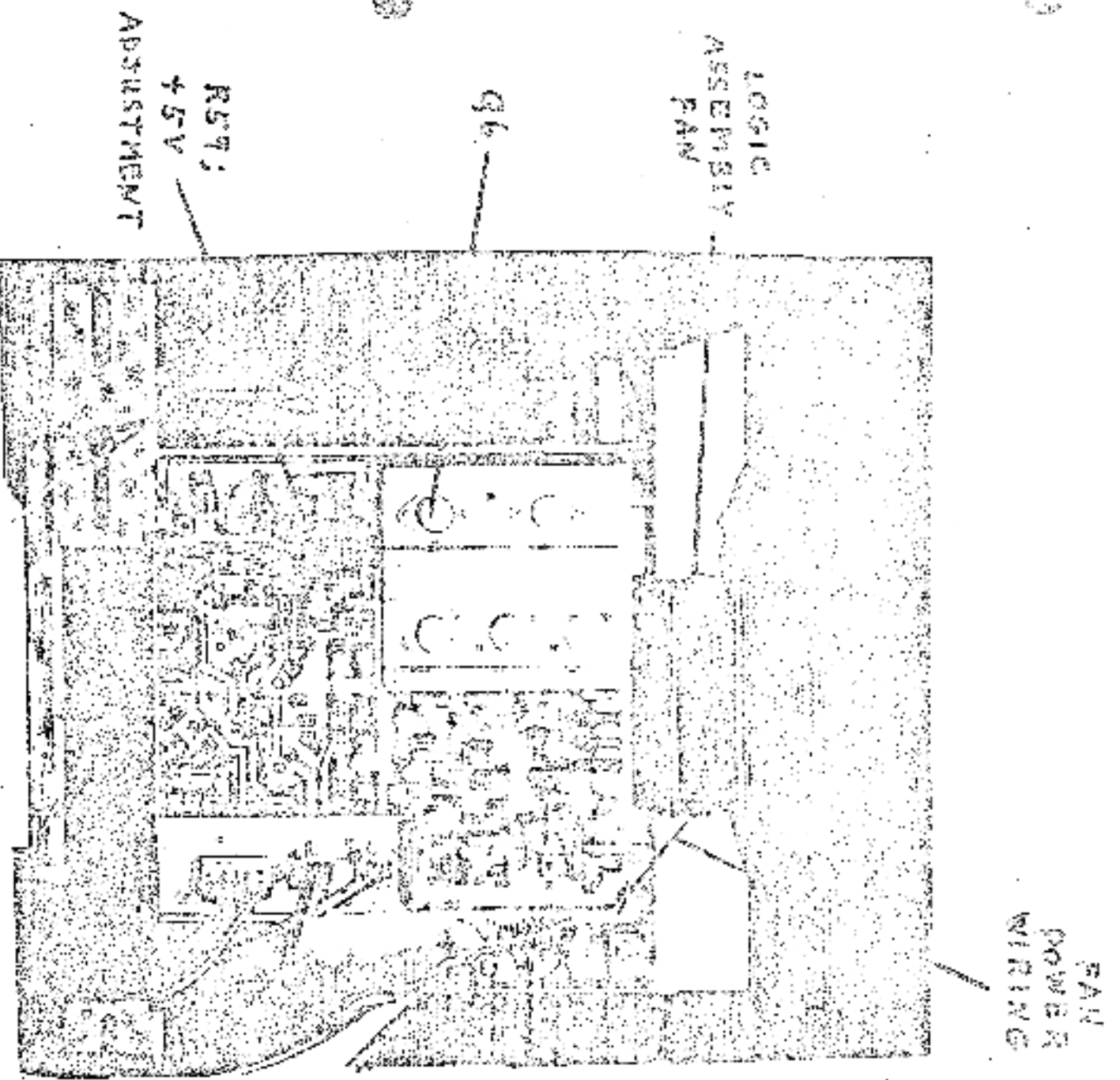


Fig. 8-1 TUIUM Regulator Board and Fan

9.2 Replace +5 Volt Regulator

The TU16 +5 regulator was redesigned to provide a greater output current capability. The new regulator (Figure 8-1) supplies the extra power required for the M8926 module. Formerly the +5V regulator had a maximum current output of 4.8 A. The new regulator current output is rated at 8.0A maximum.

To incorporate the new +5V regulator, make the following changes to the information in the TU16/TM82 Manual.

- a. Delete paragraph 3.15.2 and substitute the following:

3.15.2 +5VDC Regulator circuit

The +5Vdc regulator circuit is shown in Figure 3.15-3. Raw dc voltage is input to pins 11 and 12 of the 723 voltage regulator. The output voltage from pin 10 is fed to transistors Q6 and Q5, which are series regulators used to increase the current output capabilities of the circuit. Resistors R52 through R56 inclusive sense the output current. R52 is used as a current limit monitor by the 723. As the current increases, the voltage across R52 increases. When the reference voltage is exceeded, the 723 begins to turn off Q6 and Q5, impeding current flow. The current does not stop, but instead decreases to a safer level; this is called current foldback. It assures that the output current never goes over 8.0 A. Refer to Figure 3.15-4 which shows how the current foldback procedure works. As the current surpasses the limit of 8.0 A, the conduction of Q5 and Q6 slows down (toward being shut off) until no voltage is produced (at the short circuit current rating). The output voltage may be regulated. Resistors R58, R59 and R60 divide the actual output voltage.

CHAPTER 8

TU10W Transport: Theory of Operation (TU16/TU10W Differences)

8.1 General

In many areas the TU10W tape transport is identical to the TU16. Hence the reader is referred to the theory of operation, Chapter 2 of the TU16/TM02 tape drive system maintenance manual (document No. EK-TU16-MM-002) for a functional description of the TU10W. The reader is also referred to Chapter 2 of the same manual for detailed discussions of the functional areas of the transport.

The paragraphs that follow are concerned with the differences between the TU10W and the TU16. They provide a supplement to the TU16/TM02 manual such that this manual together with the TU16/TM02 manual will provide full coverage of the TU10W tape drive transport. Paragraphs 8.2 through 8.5 cover the differences between the TU10W and TU16 transports. Paragraph 8.6 is an errata for the TU16/TM02 manual. It lists errors that were discovered in the TU16 manual and are being corrected, but will likely still be in the copy used by the reader of this preliminary manual.

8.2 Delete TM02

The TU10W does not contain the TM02 tape controller. Delete all descriptive theory that pertains to the TM02 tape controller.

8.3 Add M926 Interface Module

The M926 interface module (covered in Chapter 7 of this manual) is installed in the system unit of the master drive, replacing the M901, M913 and M901-YA modules. (See Figure 2-14.)

Pin 5 of the 723 accepts the output feedback voltage through R58. The adjustment of R59 regulates the +5V output.

In addition to the current feedback feature, a voltage crowbar circuit is used, offering overvoltage protection. If for some reason Q5 or Q6 become shorted, the overvoltage protection circuit protects any load connected to the power supply. When Q5 or Q6 short circuits, the output voltage starts increasing very rapidly. As the voltage across the D16 zener diode becomes greater than 6.8V, it breaks down and begins conducting; it does not conduct during normal operation. Current now begins to flow through R22. When the voltage at the junction of D16 and R22 becomes greater than approximately 0.7V (at the gate of D15), the SCR fires and begins conducting. This offers a path for current from the output to ground, shunting any load, thus protecting it. The SCR continues conducting until the power supply is turned off or the 15 A fuse is blown.

- b. Delete Figure 3.15-3 and substitute Figure 3-2.
- c. In Table 3.15-2; change the first item in the "Specification" column from: "5A maximum" to " 8A maximum"
- d. In Table 3.15-3 change the +5V adjustment potentiometer from R18 to R59.
- e. In Table 3.15-4; replace the second and third items (" +5V output too low" and " +5V too high") with the following:

+5V output too low	723 bad Q5 or Q6 shorted R64, R65, R66, R59, R59 open
+5V too high	D16 open R59 or R60 open

b. Table 3.15-3: 1016 Power Supply Regulated Voltages: the

"Wire Color Code" column is given as:

RED
YEL
GRN
GRN
GRN

The second and third items should be switched. The

column should read:

RED
GRN
YEL
GRN
GRN

c. Figure 2-2; the ninth signal line down has the following

mnemonic: SLAVE SER PLS L

The signal mnemonic should be: DRV SER PLS L

d. Figure 2-2; the 21st signal line down has the following

mnemonic: BOT L

The signal mnemonic should be: BND PT L

- f. In Table 3.15-5, change fuse F1 type from "5A" to "10A", and fuse F12 type from "5A" to "15A".
- g. In Figure 3.15-1 change the +5 volt adjustment from R16 to R17 and relocate it as shown in figure B-1. Also note the addition of Q5 to the power transistor heat sink.
- h. Change other areas in the TU16 manual, as required, that pertain to the +5V regulator.

8.5 Add Logic Assembly Fan

A fan has been added on top of the logic assembly to supply additional cooling for the new +5V regulator and the M3928 module. The fan and associated wiring are shown in Figure B-1.

8.6 TU16/TM52 Errata

Errors found in the TU16/TM52 maintenance manual are listed in this paragraph. These are not TU16W/TU16 differences but errors in the TU16/TM52 manual that are applicable to both the TU16 and the TU16W.*

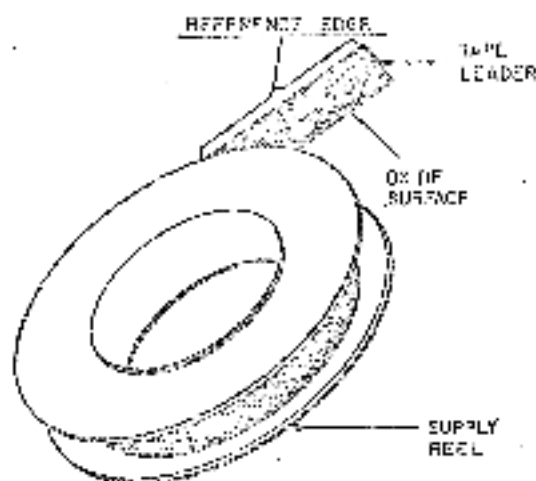
- a. In Figure 3.15-1; TU16 Power Supply Regulator Board:
R44 is designated as (-64)
R44 should be designated as (-6.4).

*These errors are being corrected and will not appear in the next issue of the TU16/TM52 maintenance manual.

APPENDIX A MAGNETIC TAPE FUNDAMENTALS

A.1 MAGNETIC TAPE FUNDAMENTALS - DEFINITIONS

1. Reference Edge - The edge of the tape as defined by Figure A-1. For tape loaded on a tape transport, the reference edge is toward the observer.



10-1205

Figure A-1 Reference Edge of Tape

2. BOT (Beginning-of-Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 ft, ± 1 ft (457 cm, ± 30.5 cm) from the beginning of the tape.
3. EOT (End-of-Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 ft (762 to 914 cm) from the trailing edge of the tape.
4. 9-Channel Recording - Eight tracks of data plus one track of vertical parity. Figure A-2 shows the relationship between track and bit weight for a 9-channel transport.*

*When the track vs bit channel standard was adopted, the outer tracks were more susceptible to bit dropping errors. Consequently, channels containing the least 1s were assigned the outer locations on the tape.

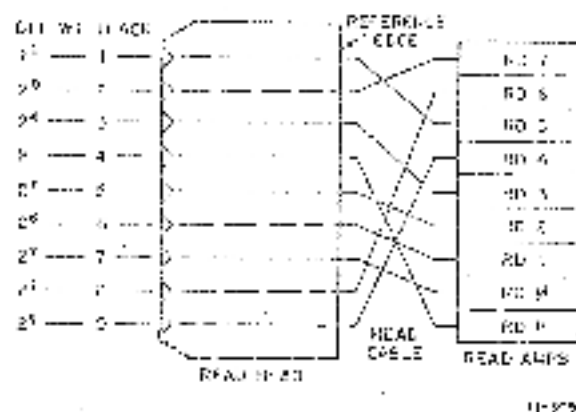


Figure A-2 Track-Bit Weight Relationship for 9-Channel Transport

5. Tape Character - A bit recorded in each of the nine channels.
6. Record - A series of consecutive tape characters.
7. File - An undefined number of records (minimum = zero, no maximum).
8. Interrecord Gap (IRG) - A length of erased tape used to separate records [0.5 in. (1.27 cm) minimum for 9-track; maximum IRG is 25 ft (762 cm)].
9. Extended IRG - A length of erased tape [3 in. (7.62 cm) minimum] optionally used to separate records. It must be used between BOT and the first record.
10. Tape Speed - The speed at which tape moves past the read/write heads; normally stated in inches per second.
11. Tape Density - The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi), which is equivalent to characters per inch.
12. Write Enable Ring - A rubber ring that must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.
13. Tape Mark (TM) - A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK).

A.2 RECORDING METHODS AND DECmagtape FORMATS

The DECmagtape system is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows called characters. Each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program-selected as even or odd. The odd-parity bit guarantees that each character records at least one 1 bit.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even. For example, if odd parity is used and the character contains an even number of 1 bits, the parity bit is generated as a 1 bit and an odd number of 1 bits are recorded; then, if an even number of bits are read back from tape, a vertical parity error is generated to notify the program that the data is in error.

The CRC character is generated during a write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character.

The LRC character is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the tape transport after the CRC character is written. The LRC character resets the write buffer, causing a 1 to be written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.

A.2.3 7-Channel Tape Format

Each character frame in a 7-channel tape (Figure A-5) consists of six character bits (B, A, S, 4, 2, 1) in descending order of significance. The parity bit, or check bit (C), is the seventh bit and is set or cleared by the transport write head. One byte of a data word corresponds to one tape character. However, because one byte contains eight bits and a tape character contains only six data bits, two bits within each byte are not used. During a read operation, the extra bits are forced to 0; during a write operation, the bits remain unchanged. During the core dump mode of operation, one byte corresponds to two tape characters. Thus, all bits within the byte are used; however, the two most significant bits on the tape are not used.

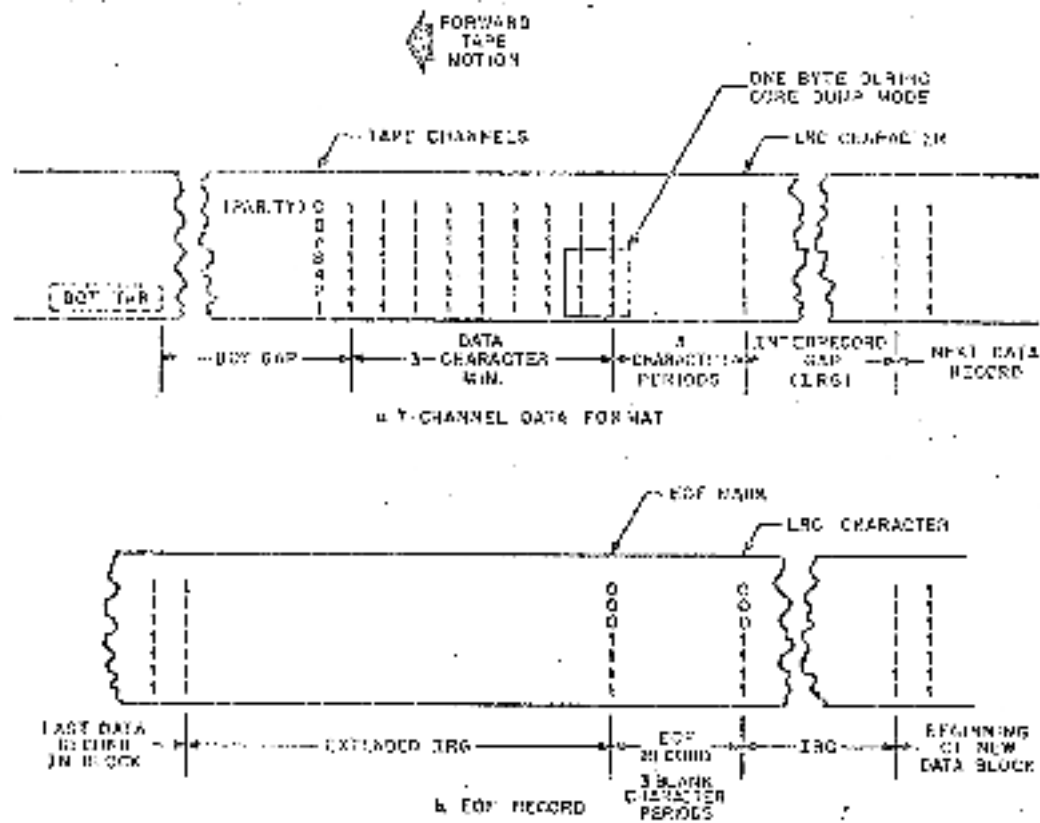


Figure A-5 7-Channel Tape Format

- The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 of the CRC register are inverted if the bit entering CRC 1 is a 1. Data is shown in Table A-1; the resultant CRC character is shown in Table A-2.

Table A-1 Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
7	0	0	1	0	1
6	1	0	0	1	0
5	0	1	0	1	0
4	0	1	0	1	1
3	1	0	1	1	0
2	0	1	1	0	1
1	0	1	0	1	0
0	1	0	0	1	0

Table A-2 CRC Character in Register When Writing

CRC Bits	CRC Register						CRC Character On Tape
	Character 0	Character 1	Character 2	Character 3	Character 4	Final	
CRC7	0	1	0	0	1	0	1
CRC6	0	0	1	1	1	0	1
CRC5	0	0	0	1	1	0	1
CRC4	0	1	0	0	0	1	1
CRC3	0	0	1	0	0	0	1
CRC2	0	0	0	0	0	1	1
CRC1	0	1	0	0	0	0	1
CRC0	0	0	0	1	0	0	1
CRCP	0	0	0	0	1	1	0

- Steps 1 - 3 are repeated for each data character of record.
- At CRC time, all positions of the CRC register, except CRC2 and CRC4, are complemented and the resultant CRC character is written on tape.
- The CRC register is cleared for the next record.

A.4 LONG-TERMINAL-BIT BOUNDARY CHECK (LRC) CHARACTER

The LRC character is written three spaces after the CRC character. The vertical parity bit is always written as the LRC character. The vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC is generated by the LRC register in the following manner:

1. The LRC register is cleared at the beginning of a record.
2. As characters are written on tape, corresponding 1 bits complement the LRC register as the first data is written on tape.
3. At LRC time, the LRC strobe clears the write buffer and its are written on tape in only those channels for which the write buffer is set prior to clearing.
4. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character.

A.5 DATA FILES

As previously stated, a record is a group of characters preceded by an IRG and terminated by three spaces, a CRC character, three more spaces, and an LRC character. A file is a group of records separated by IRGs and terminated by a 3 in. (7.62 cm) gap followed by a file mark. The file mark is a record consisting of a single data character [the end-of-file (EOF) character] followed by seven blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a file mark is a duplicate of the EOF character (23₆).

A.6 TRACK ASSIGNMENTS

The track assignments for read, write, and parity bits are shown in Table A-3.

Table A-3 Track Assignments for Data and Parity

Transport Track Number	Write Data Bits	Read Data Bits	Binary Weight
1 furthest from transport	WD5	RD5	2 ³
2	WD7	RD7	2 ⁰
3	WD3	RD3	2 ⁴
4	WD7	RDP	-
5	WD2	RD2	2 ⁵
6	WD1	RD1	2 ⁶
7	WD0	RD0	2 ⁷
8	WD6	RD6	2 ¹
9, closest to transport	WD4	RD4	2 ²