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TMA11-M
DECmagtape system maintenance manual

digital equipment corporation · maynard, massachusetts

TMA11-M
DECmagtape system maintenance manual

EK-TMA11-MM-PRE

PRELIMINARY

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PREFACE

This manual provides a complete description of the TMA11-M DECmagtape System. Included are installation instructions, operation and programming information, functional block and logic level descriptions, preventive and corrective maintenance procedures, and removal and replacement procedures. The manual is divided into three parts:

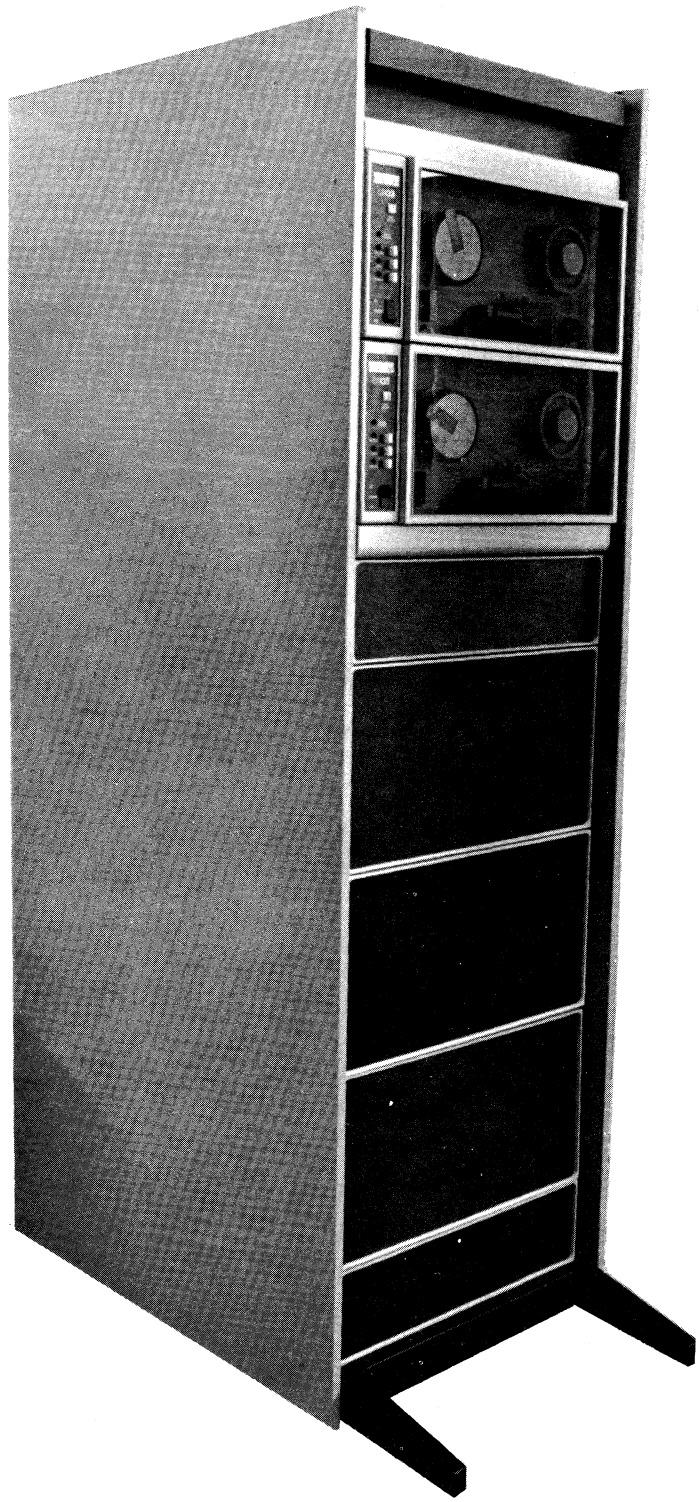
Part I – Contains a general description of the system and complete system installation instructions.

Also contains maintenance information including customer care and operation, preventive maintenance, corrective maintenance, and removal and replacement procedures.

Part II – Contains a complete description of the TMA11 Controller including specifications, programming information, and functional block, logic level, and flow diagram descriptions.

Part III – Contains a complete description of the TS03 DECmagtape Transport including specifications, operation, and functional block, logic level, and flow diagram descriptions.

PART I
SYSTEM INFORMATION



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TMA11-M DECmagtape System

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The TMA11-M DECmagtape System is a magnetic tape storage system that interfaces with the PDP-11 family of processors and peripherals and provides storage for digital information. The system reads and records digital data in parallel in a nine-channel, industry-compatible format.

1.2 SYSTEM CONFIGURATION

The TMA11-M DECmagtape System is composed of the units shown in Figures 1-1 and 1-2 and listed below.

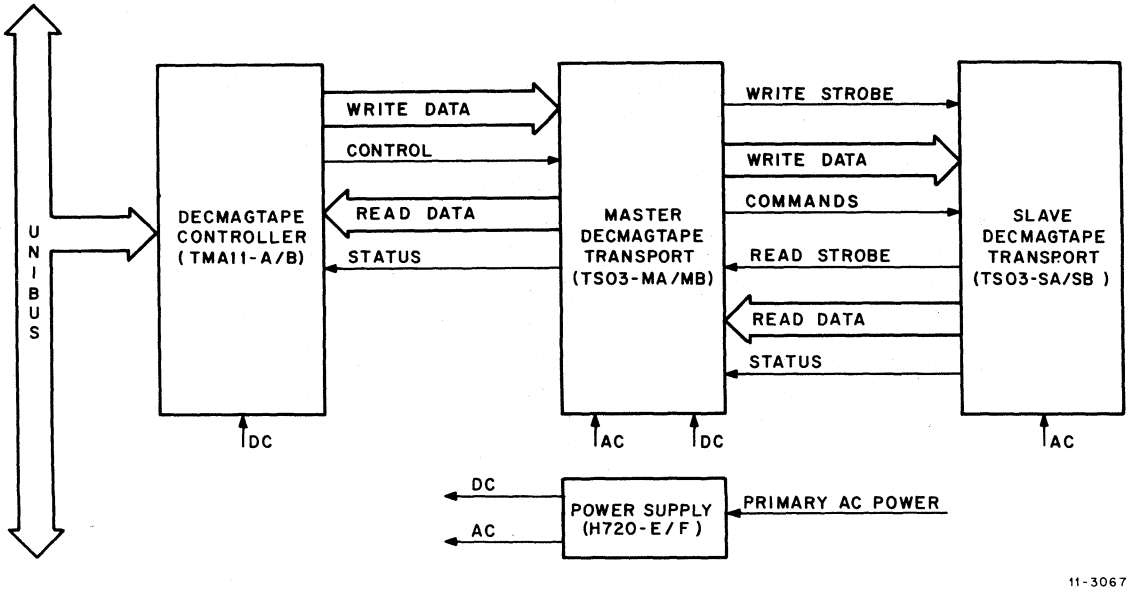


Figure 1-1 TMA11-M System Configuration

1. DECmagtape Controller – The TMA11 interfaces the DECmagtape system to the PDP-11 Unibus. It controls data transfers, issues control commands to the TS03 master, and monitors system operation. Each TMA11 can control two TS03 transports: a master and a slave.

2. Slave DECmagtape Transport – The TS03-S consists of a tape transport only. In response to inputs from the adapter, it controls tape motion and records and reads data on magnetic tape. The TS03-SA requires 115 V, 60 Hz primary power and the TS03-SB requires 230 V, 50 Hz primary power.

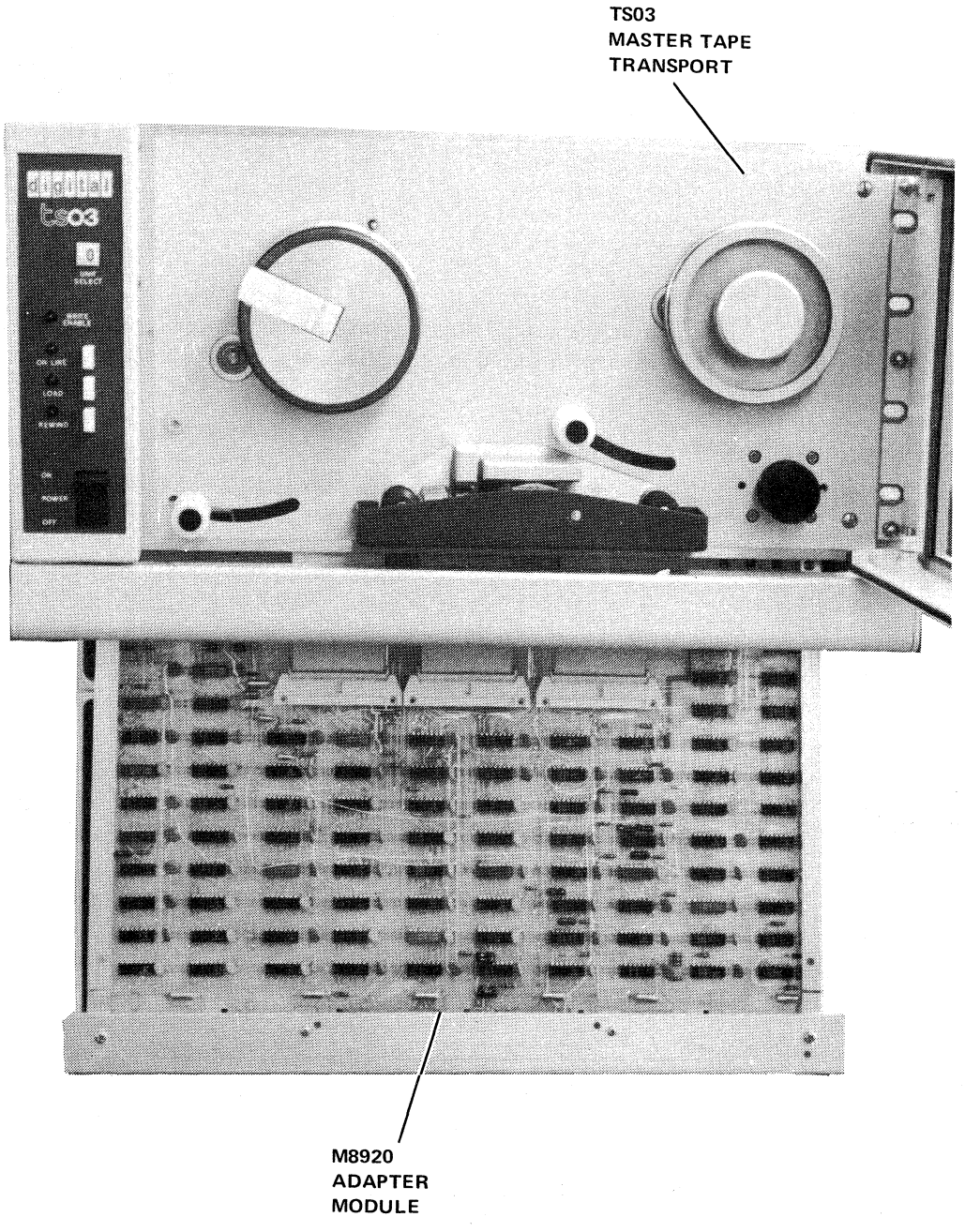


Figure 1-2 Major Assemblies (Sheet 1 of 2)

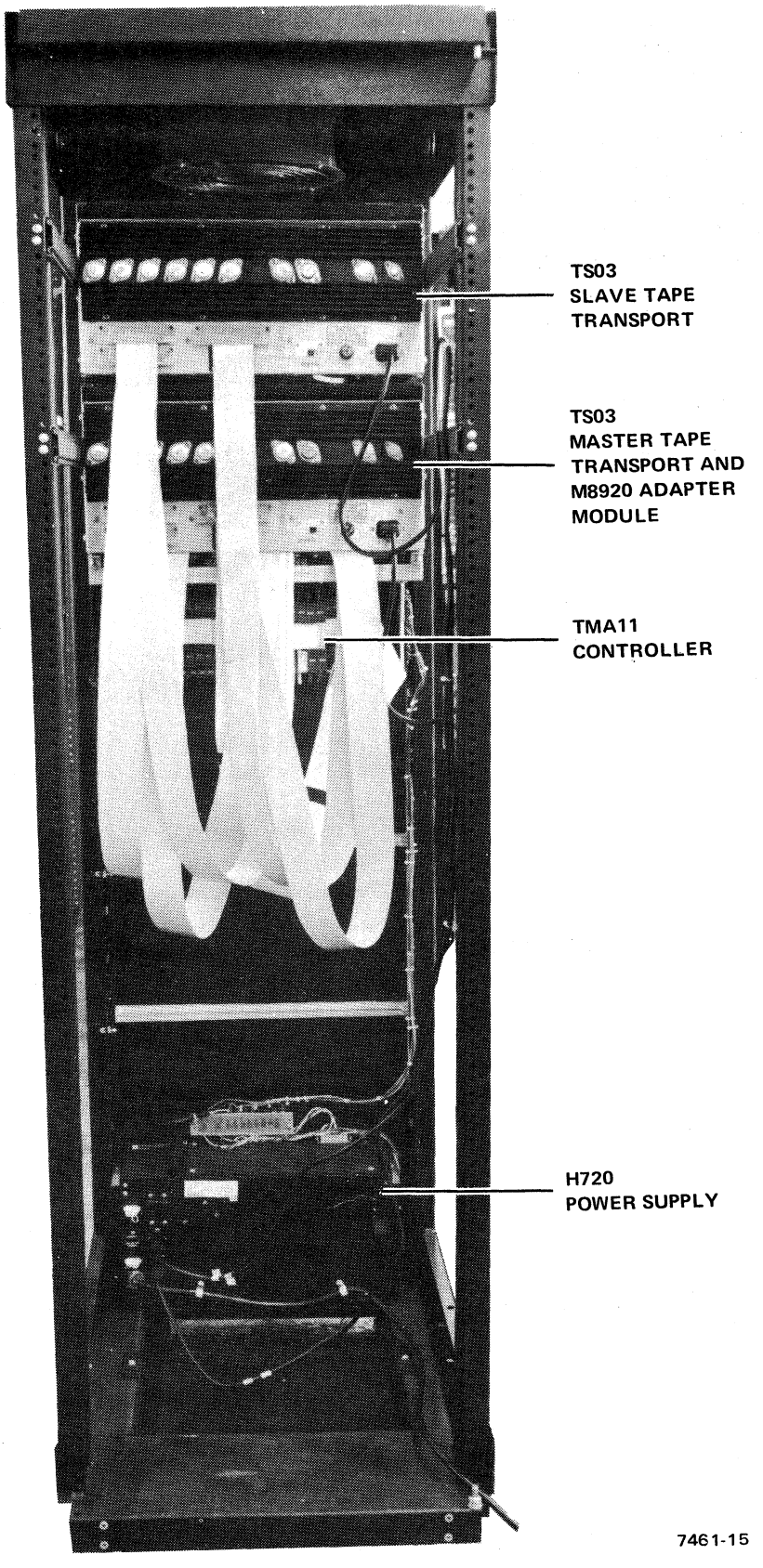


Figure 1-2 Major Assemblies (Sheet 2 of 2)

3. Power Supply – The H720 provides switched ac and dc operating power for the TMA11-M system. Two models of the power supply are available: the H720-E, which requires 115 V primary power and the H720-F, which requires 230 V primary power.

4. Master DECmagtape Transport – The TS03-M consists of an M8920 adapter module and a tape transport. The M8920 processes commands from the controller and issues motion and read/write commands to the master and slave transports; the M8920 also monitors status lines from the master and slave transports. Any status changes at the selected transport are reported immediately to the controller. In response to inputs from the adapter, the tape transport controls tape motion and records and reads data on magnetic tape. Two models of the master DECmagtape transport are available: the TS03-MA, which requires 115 V, 60 Hz primary power and the TS03-MB, which requires 230 V, 50 Hz primary power.

1.3 APPLICABLE DOCUMENTS

Table 1-1 lists PDP-11 documents that are applicable to the TMA11-M DECmagtape System.

Table 1-1
Applicable Documents

Title	Number	Description
H720 Power Supply and Mounting Box Manual	EK-H720-TM-003	A theory manual that provides a functional and detailed circuit description of the H720 power supply.
PDP-11 Processor and Systems Manuals	*	A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 system.
PDP-11 Processor Handbook	†	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
PDP-11 Peripherals Handbook	112-00973-2908	A handbook devoted to a discussion of the various peripherals used with PDP-11 systems. It also provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
DIGITAL Logic Handbook, 1973-74 Edition		Presents functions and specifications of the M-series logic modules, accessories, and connectors used in the TMA11 Controller and the TS03 DECmagtape Transport. Includes other types of logic produced by DEC but not used with PDP-11 devices.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

*Applicable manuals are furnished with the system at time of installation. The document number depends upon the specific PDP-11 family processor.

†Use the processor handbook unique to the actual CPU.

1.4 MAGNETIC TAPE FUNDAMENTALS – DEFINITIONS

1. Reference Edge – The edge of the tape as defined by Figure 1-3. For tape loaded on a TS03, the reference edge is toward the observer.

2. BOT (Beginning-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 ft (±1 ft) from the beginning of the tape.

3. EOT (End-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 ft from the trailing edge of the tape.

4. Nine-Channel Recording – Eight tracks of data plus one track of vertical parity. Figure 1-4 shows the relationship between track and bit weight for a nine-channel transport.

5. Tape Character – A bit recorded in each of the nine channels.

6. Record – A series of consecutive tape characters.

7. File – An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) – A length of erased tape used to separate records (0.5 in. minimum for nine-track; maximum IRG is 25 ft).

9. Extended IRG – A length of erased tape (3 in. minimum) optionally used to separate records. It must be used between BOT and the first record.

10. Tape Speed – The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density – The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi), which is equivalent to characters per inch.

12. Write Enable Ring – A rubber ring which must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

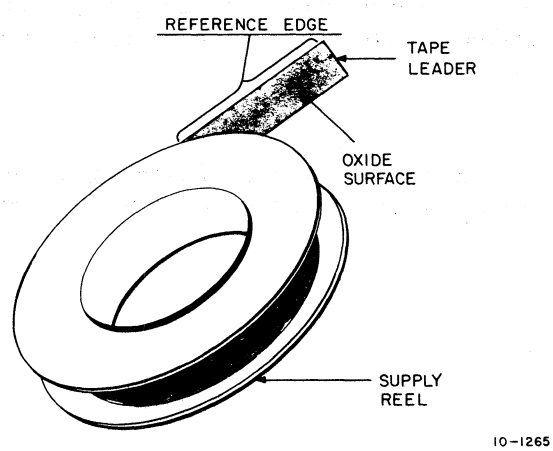


Figure 1-3 Reference Edge of Tape

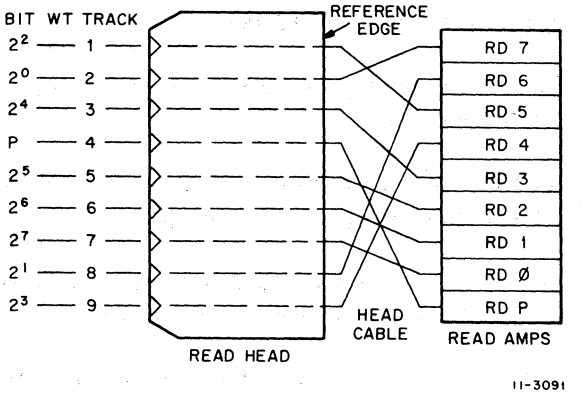


Figure 1-4 Track-Bit Weight Relationship for Nine-Channel Transport

13. Tape Mark (TM) – A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK). *In the TMA11-M, the tape mark is always preceded by an extended IRG.*

1.5 RECORDING METHODS AND DECmagtape FORMATS

The DECmagtape system is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows, termed characters. Each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program-selected as even or odd. The odd parity bit guarantees that each character records at least one 1 bit.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even. For example, if odd parity is used and the character contains an even number of 1 bits, the parity bit is generated as a 1 bit and an odd number of 1 bits are recorded; then, if an even number of bits are read back from tape, a vertical parity error is generated to notify the program that the data is in error.

The data characters are recorded in blocks of characters, termed records (Figure 1-5). Each record contains a specified number of characters determined by the word count. The minimum record length is 3 characters; the minimum word count is the 2's complement of 3 or 7775_8. If a write operation is attempted for a record with less than 3 characters, the controller will force a minimum of three characters to be written.

Records are separated by interrecord gaps (IRGs). The IRG is 0.5 in. (approximately 0.6 in. in normal operation) minimum, but may be extended to 3 in. by performing an extended gap operation. Tape IRGs (unrecorded areas) provide areas on the tape for the transport to start or stop and also separate data records.

1.5.1 NRZI Recording Method

The TS03 employs the NRZI (non-return-to-zero change on one) recording method. In the NRZI method, a 1 bit is represented by a reversal in the direction of tape magnetization on a track; a 0 bit is represented by no change in tape magnetization.

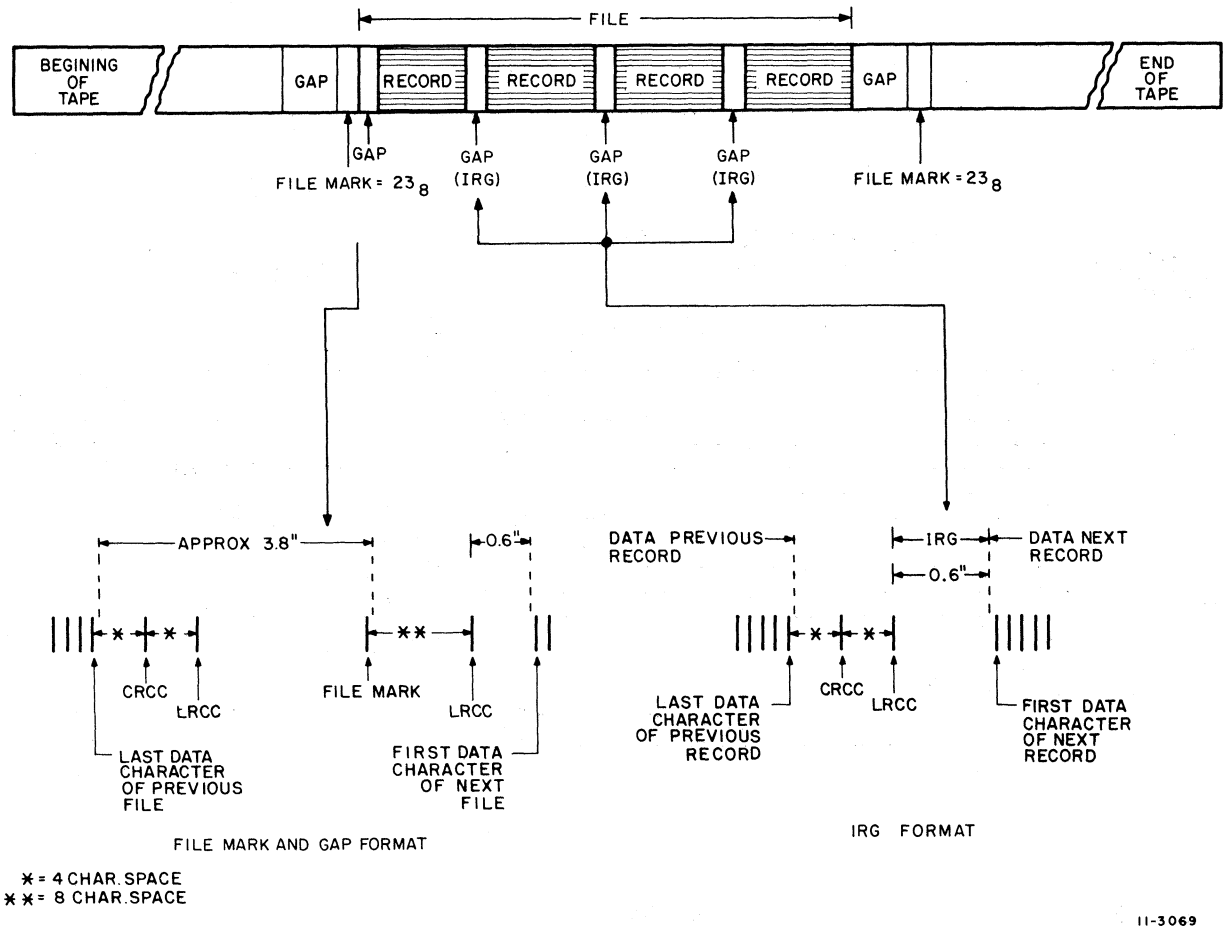


Figure 1-5 Data Recording Scheme

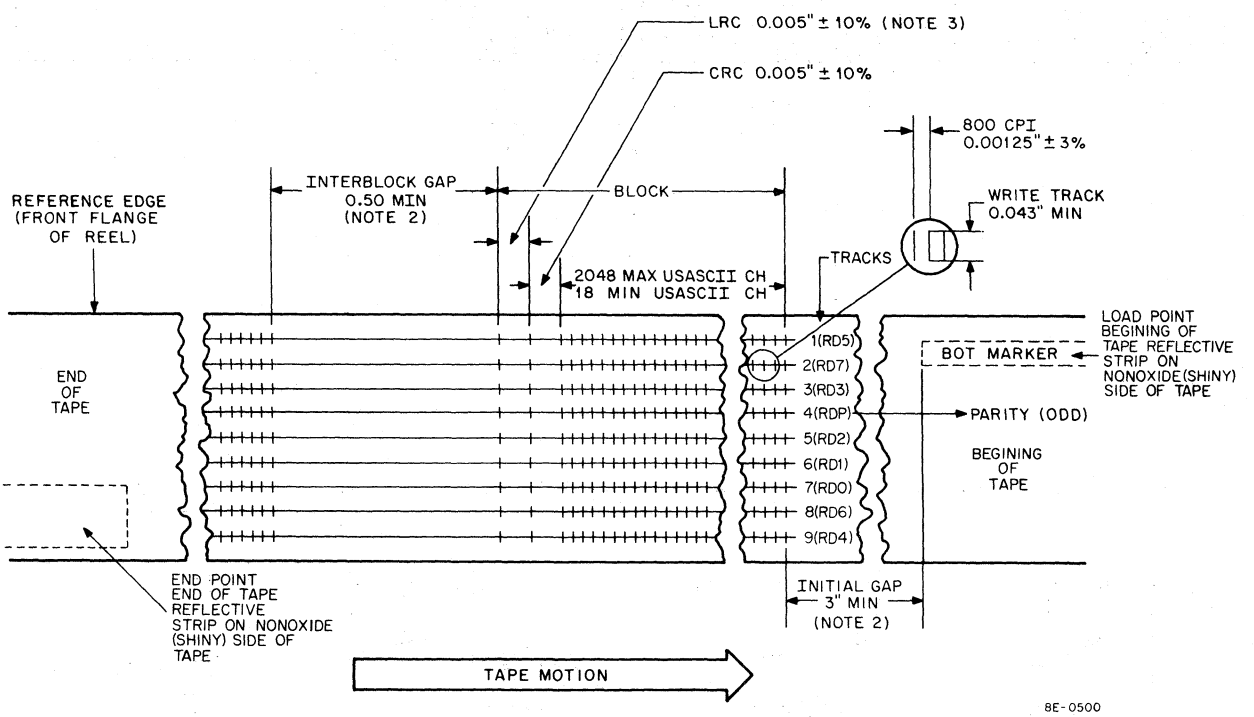
1.5.2 Tape Format

The format (Figure 1-6) is composed of from 18* to 2048 nine-bit characters spaced 1/800 in. apart, followed by 4 character spaces, a CRC character, 4 more spaces, and an LRC character. This unit of data is called a record. At 800 characters per inch, the record is between 1/32 in. (minimum) and 5 in. (maximum). Between each record is a gap of at least 1/2 in. The tape structure consists of a number of records followed by a file mark (Figure 1-5). Since data is recorded and read at high speed, IRGs are used to provide space for starting and stopping the TS03 transports. The TS03 transport accelerates from standstill to full speed in approximately 0.2 in. of tape and decelerates from full speed to standstill in 0.2 in. of tape; thus, the 0.5 in. IRG provides adequate space for starting and stopping the tape transport.

The CRC character (Paragraph 1.5.3) is generated in the TS03 during a write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character.

The LRC is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the tape transport after the CRC character is written. The LRC strobe resets the write buffer, causing a 1 to be written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.

*USASCII program standards, not a hardware limit.



LEGEND

BPI	Tape Bits per Inch
BOT	Beginning of Tape
LRC	Longitudinal Redundancy Check
CRC	Cyclic Redundancy Check

NOTES:

1. Tape is shown with oxide side up, read/write head on same side as oxide. Tape shown representing 1 bits in all NRZI recording; 1 bit produced by reversal of flux polarity, tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the interrecord gap and the initial gap.
3. An LRC bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the LRC character.
4. CRC – Parity of CRC character is odd if an even number of data characters are written, and even if an odd number of characters are written.

Figure 1-6 Tape Format

1.5.3 Cyclic Redundancy Check (CRC) Characters

The CRC character provides a method of error detection and correction on TS03 DECmagtape Transports. The code has nine check bits that form a check character at the end of each record. To perform a correction, a record in which an error has been detected must be reread into memory with the LRC and CRC characters for program evaluation. Errors involving more than one track can be detected but not corrected.

The CRC character is generated as follows:

1. The CRC register, located in the TS03, is cleared at the beginning of each record. As each data bit is written on tape, it is exclusively-ORed with its corresponding bit in the CRC register.

2. The CRC register is shifted one position to the right after the exclusive-OR operation has taken place.

3. The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 of the CRC register are inverted if the bit entering CRCP is a 1. Data is shown in Table 1-2; the resultant CRC character is shown in Table 1-3.

Table 1-2
Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
P	0	0	1	0	1
0	1	0	0	1	0
1	0	1	0	1	0
2	0	1	0	1	1
3	1	0	1	1	0
4	0	1	1	0	1
5	0	1	1	0	1
6	1	0	1	0	1
7	0	1	0	1	0

Table 1-3
CRCC In Register When Writing

CRC Bits	CRC Cleared	CRC Register				Final CRC	CRCC On Tape
		Character 1	Character 2	Character 3	Character 4		
CRCP	0	0	0	0	1	1	0
CRC0	0	0	0	1	0	0	1
CRC1	0	1	0	0	0	0	1
CRC2	0	0	0	0	0	1	1
CRC3	0	0	1	0	0	0	1
CRC4	0	1	0	0	0	1	1
CRC5	0	0	0	1	1	0	1
CRC6	0	0	1	1	1	0	1
CRC7	0	1	0	0	1	0	1

4. Steps 1–3 are repeated for each data character of record.

5. At CRC time, all positions of the CRC register, except CRC 2 and CRC 4, are complemented and the resultant CRC character is written on tape.

6. The CRC register is cleared for the next record.

1.5.4 Longitudinal Redundancy Check (LRC) Character

The LRC character is written four spaces after the CRC character. The vertical parity bit is always written on the LRC character; the vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC is generated in the TS03 by the LRC register in the following manner:

1. The LRC register is cleared at the beginning of a record.

2. As characters are written on tape, corresponding 1 bits complement the LRC register at the time data is written on tape.

3. At LRC time, the LRC strobe clears the write buffer and 1s are written on tape in only those channels for which the write buffer is set prior to clearing.

4. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character.

1.5.5 Data Files

As previously stated, a record is a group of characters preceded by an IRG and terminated by four spaces and an LRC character. A file is a group of records separated by IRGs and terminated by a 3 in. gap followed by a file mark. The file mark is a record consisting of a single data character [the end-of-file (EOF) character] followed by seven blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a file mark is a duplicate of the EOF character (23_8).

1.5.6 Track Assignments

The track assignments for read, write, and parity bits are shown in Table 1-4.

Table 1-4
TS03 Track Assignments for Data and Parity

Transport Track Number	Write Data Bits	Read Data Bits
1 (inside)	WD5	RD5
2	WD7	RD7
3	WD3	RD3
4	WDP	RDP
5	WD2	RD2
6	WD1	RD1
7	WD0	RD0
8	WD6	RD6
9 (outside)	WD4	RD4

CHAPTER 2
INSTALLATION

2.1 SITE PLANNING AND CONSIDERATIONS

2.1.1 Space Requirements

Figure 2-1 illustrates the space and service clearances required. Adequate space must be provided to slide the equipment out of the rack for servicing and to open the front door on the TS03 DECmagtape Transport.

2.1.2 Power Requirements

The TMA11-M DECmagtape System can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained to within 10 percent of the nominal value and the frequency should not vary more than 3 Hz. Ensure that primary power is compatible with the H720 power supply.

2.1.3 Environmental Requirements

The operating environment should have cool, well filtered, humidified air, a temperature range of 15° to 27° C, and relative humidity of 40 to 60 percent.

2.2 UNPACKING

The TMA11-M may be shipped in two different configurations: with the system installed in an equipment rack or with each device packaged separately.

2.2.1 Cabinet Unpacking Instructions

To unpack the cabinet, proceed as follows:

1. Remove outer shipping container.

NOTE

The container may be either heavy corrugated cardboard or plywood. In either case, remove all metal straps first, then remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter.

2. Remove the polyethylene cover from the cabinet.

3. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting side rails, and are exposed by opening the access door(s). Remove the bolts.

4. Raise the leveling feet above the level of the roll-around casters.

5. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

6. Roll the system to the proper location for installation.

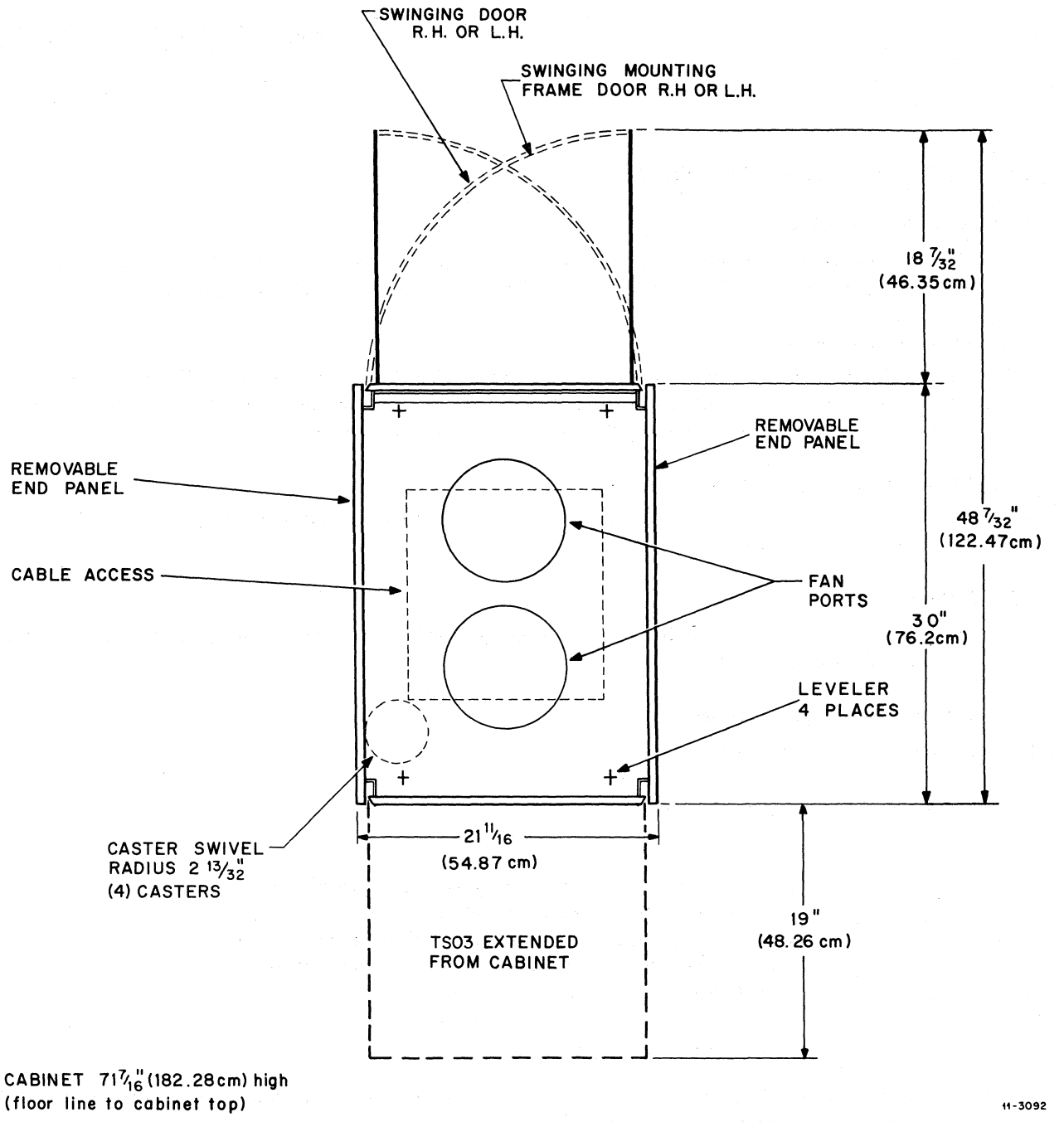


Figure 2-1 Space and Service Clearance

2.2.2 Device Unpacking Instructions

Before unpacking the equipment, check the shipping list to ensure that the correct number of packages have been received. Then carefully remove each device from its shipping carton. Note that the side mounts are already attached to the TS03 transport(s) and the mounting hardware is packed in a bag in each shipping carton.

2.3 INSPECTION

After removing the equipment from its container(s), inspect it and report any damage to the responsible shipper and the local DEC Sales Office. Inspect as follows:

1. Inspect all switches, indicators, and panels for damage.
2. Remove equipment covers where necessary and inspect for loose or broken modules, blower or fan damage, cable damage, and loose nuts, bolts, screws, etc.
3. Inspect wiring side of logic panels for bent pins, broken wires, loose external components, and foreign material.
4. Check TS03 transport(s) for any foreign material that may have lodged in the tension arm, reel hubs, and other moving parts.
5. Check power supply for proper seating of fuses and power connectors.

2.4 INSTALLATION

2.4.1 Cabinet Installation

If the equipment is already mounted in the cabinet, proceed as follows:

1. Lower the leveling feet so that the cabinet is resting on the floor, not on the roll-around casters.
2. Use a spirit level to level the cabinet; ensure that all leveling feet are firmly on the floor.
3. Remove the shipping screws which secure the equipment to the cabinet.
4. Plug the H720 power supply ac power cord into a receptacle having the correct voltage and frequency.

2.4.2 Device Installation

The equipment should be mounted in a 19 in. by 20 in. equipment bay. Figure 2-2 shows a recommended cabinet layout. The equipment should be mounted from the top down.

2.4.2.1 TS03 Mounting Instructions – To mount the TS03, proceed as follows.

NOTE

If two TS03 transports (master and slave) are to be installed, the slave (the unit without the M8920 adapter module) is installed at the uppermost position.

1. Remove the outer portions of the guides from the TS03 chassis by actuating the slide releases and mount the guides to the cabinet in the 19th hole from the top of the cabinet using the eight screws provided. Ensure that the guides are level and parallel to each other.

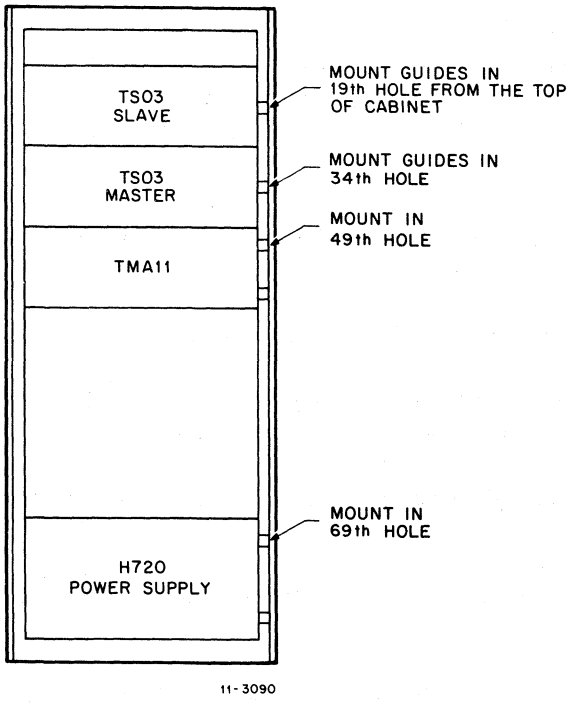


Figure 2-2 Cabinet Installation

2. Lift the TS03 up and slide it carefully into the guides until the slide releases lock.

3. Carefully lift the slide releases and push the transport fully into the cabinet.

4. If a second TS03 transport is to be installed, repeat steps 1 through 3 above, but mount the guides in the 34th hole.

2.4.2.2 TMA11 Controller Mounting Instructions – Using the hardware provided, mount the TMA11 in the cabinet at the 49th hole position.

2.4.2.3 H720 Power Supply Mounting Instructions – Using the hardware provided, mount the H720 power supply in the cabinet at the 69th hole position.

2.4.3 I/O Cable Connections

To install the I/O cables, proceed as follows (Figure 2-3).

1. Install one end of the BC11A cable assembly into slot 03 of the TMA11 backpanel and install the other end into the M8920 adapter board edge connectors.

2. Install 7010570 master/slave cables between the M8920 adapter board connectors J1–J6 and the TS03 master and slave transport connectors as listed in Table 2-1 and illustrated in Figure 2-3.

3. Install one end of the remaining BC11A cable assembly into slot 01 of the TMA11 backpanel and install the other into the PDP-11 Unibus.

4. Install either a Unibus terminator module or a second BC11A cable assembly into slot 02 of the TMA11 backpanel.

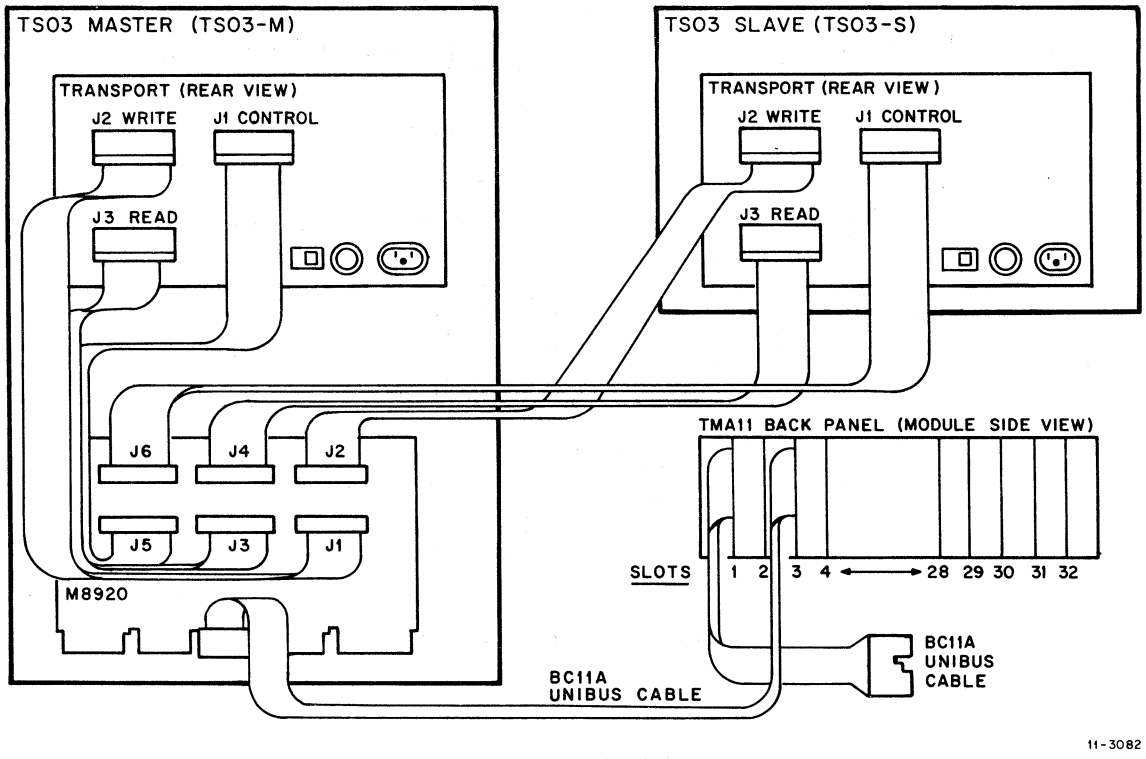


Figure 2-3 I/O Cable Connection Diagram

Table 2-1
BC08A-10 Cable Connections

From M8920 Adapter Board Connector	To TS03 Master Connector	TS03 Slave Connector
J1	J2	
J3	J3	
J5	J1	
J2		J2
J4		J3
J6		J1

2.4.4 Power Connections

To make power connections, proceed as follows:

1. Install the power harness (7009742) between the H720 power supply and the TMA11 power end assembly panel in accordance with color coding listed in Table 2-2 (Figure 2-4).

2. Install the power harness (70-10832) between the H720 power supply and the M8920 adapter module.

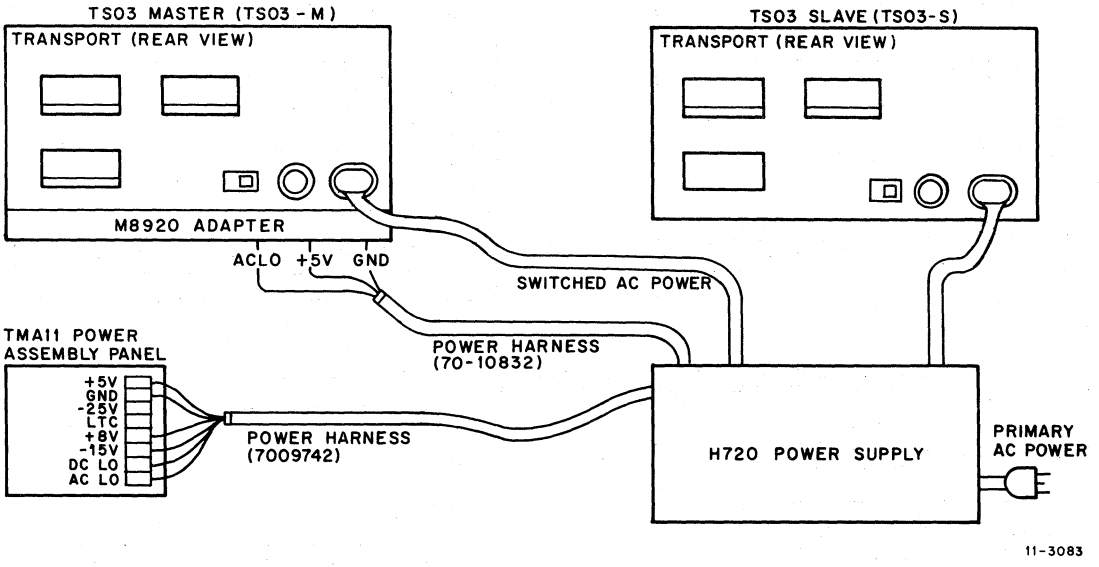


Figure 2-4 Power Connection Diagram

Table 2-2
Power Harness Color Coding

DC Voltage/Signal	Wire Color
+5 V	Red
Gnd	Black
-15 V	Blue
DC LO	Violet
AC LO	Yellow

3. Plug the TS03 master and slave transport ac power cords into the H720 power supply switched receptacles.

4. Plug the H720 power supply power cord into the site's primary ac power outlet having the proper ac voltage and frequency. Check the label on H720 power supply for power requirements.

5. Using tie wraps, neatly dress all cables and harnesses. Leave service loops so TS03 drives can be extended from the cabinet and the M8920 adapter can be swung down on its hinges.

CHAPTER 3
SYSTEM OPERATING INSTRUCTIONS

3.1 SCOPE

This chapter covers operation of the TMA11-M, including a description of controls and indicators and all operating procedures.

3.2 CONTROLS AND INDICATORS

Figure 3-1 describes the controls and indicators.

3.3 OPERATING PROCEDURES

3.3.1 Tape Threading

To thread the tape on the transport, proceed as follows:

1. Raise the latch of the quick-release hub and place the tape file reel to be used on the supply hub (Figure 3-2) with the write enable ring side next to the transport deck.

2. Hold the reel flush against the hub flange and secure it by pressing the hub latch down.

3. Thread the tape along the path as shown in the threading diagram (Figure 3-2).

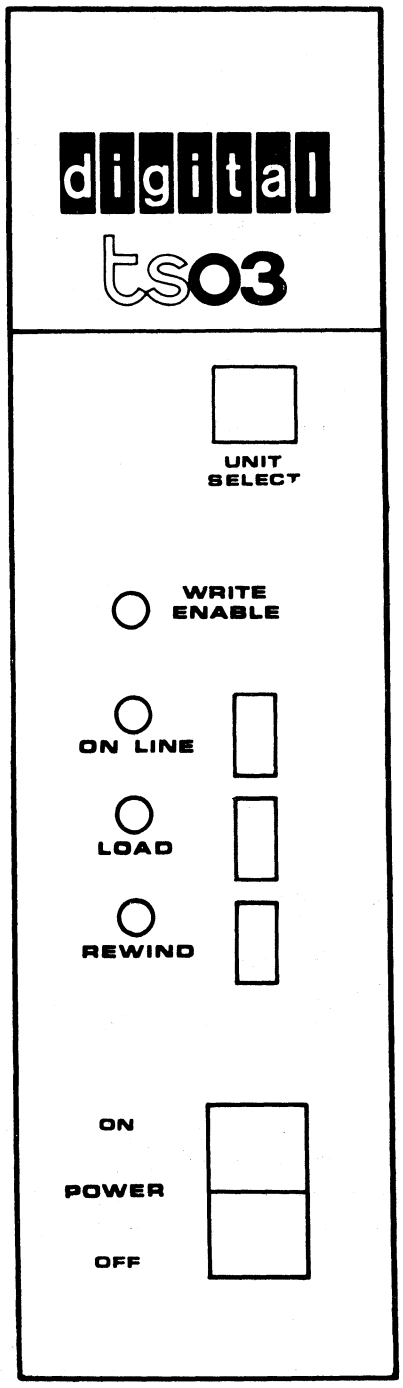
4. Holding the end of the tape with a finger, wrap a few turns counterclockwise around the takeup hub.

3.3.2 Tape Loading

Pressing the LOAD pushbutton energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops. If for some reason the load point marker is already past the sensor (as, for example, in restoring power after a shutdown), tape will continue to move. Under these conditions, press LOAD and then REWIND and the tape will rewind to the load point. Once pressed, the LOAD switch is illuminated and is inactive until power has been turned off or tape is removed from the machine.

3.3.3 Placing Tape Unit On-Line

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and check that the ON LINE indicator illuminates. (The REWIND pushbutton is disabled when the tape unit is on-line.) On-line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.



UNIT SELECT Plug – One of two plugs can be inserted, designating unit as 0 or 1.

NOTE

In a single drive system, the drive is always designated as drive 0. In a dual drive system, either drive can be designated as drive 0.

WRITE ENABLE Indicator – Illuminated whenever a reel with a write enable ring is mounted on the supply hub.

ON LINE Pushbutton/Indicator – A momentary push-button, which functions as alternate action. When first activated, the tape unit is placed in an on-line condition; when the tape unit is on-line, it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the unit off-line. The indicator is illuminated in the on-line condition. The load function must be performed before the unit will go on-line.

LOAD Pushbutton/Indicator – The momentary push-button activates the reel servos (tensions tape) and starts the load sequence. The indicator is illuminated when the reel servos are activated and tape is tensioned.

REWIND Pushbutton/Indicator – The momentary push-button activates a rewind operation. This control is enabled only when tape is tensioned and the unit is off-line. The indicator is illuminated during either a local or a remote rewind operation.

POWER Switch – The ON/OFF switch applies ac power to the tape transport.

Figure 3-1 Controls and Indicators

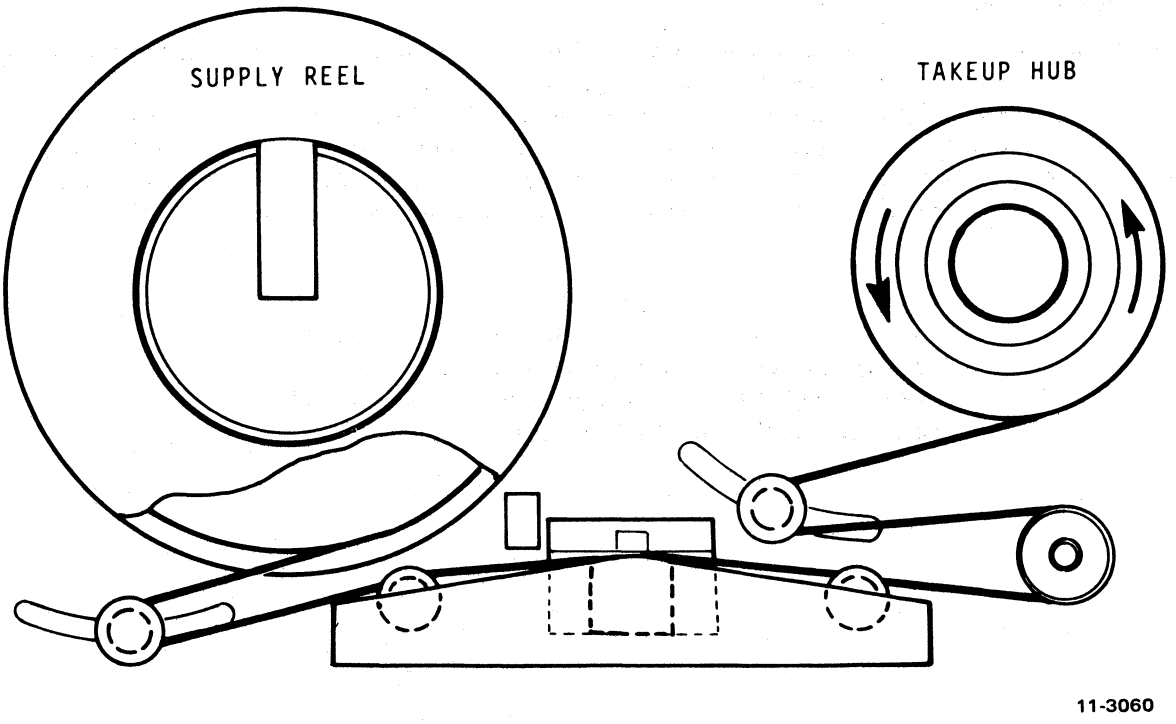


Figure 3-2 Tape Threading Diagram

3.3.4 Tape Unloading and Rewind

Provision is made in the TS03 transport for rewinding a tape to the load point under remote control. However, this operation may also be performed manually. Proceed as follows.

1. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. Check that the indicator extinguishes when pressure is removed.

2. Press the REWIND pushbutton. The tape will now rewind to the load point marker.

3. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to rewind the tape past the load point to the physical beginning of the tape.

NOTE

The rewind sequence cannot be stopped until the tape has rewound either to the load point or until tension is lost at the physical beginning of the tape.

3.3.5 Power Shutdown

A tape transport should not be turned off when tape is loaded and is past the load point marker. The TS03 transport is designed to prevent physical damage to the tape in the event of power failure, and to minimize operator error which could destroy recorded data. In the event of power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton, then the REWIND pushbutton. This will rewind the tape to the load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred by initiating the appropriate control commands.

CAUTION

In dual drive systems, when one drive is on-line and running, *do not* turn power off at the unused drive, i.e., do not set the TS03 POWER ON/OFF switch to OFF. To do so can result in data errors on the drive that is running.

CHAPTER 4
CUSTOMER EQUIPMENT CARE AND OPERATION

4.1 SCOPE

The information contained in this chapter will assist the customer in caring for his equipment and ensure the highest level of performance and reliability.

4.2 REQUIREMENTS

The customer is directly responsible for:

1. Obtaining operating supplies, including disk cartridges, disk packs and filters, magnetic tape, DECtape, paper tape, cassettes, printer paper, printer ribbons, plotter paper, etc.

2. Supplying accessories, including disk storage racks, DECtape storage racks, carrying cases for disk cartridges and DECtape, cabinetry, tables and chairs.

NOTE

Users of Digital Equipment Corporation equipment may obtain the proper operating supplies and accessories by contacting:

Digital Equipment Corporation
DEC Supplies Order Processing
146 Main Street
Maynard, Massachusetts 01754
Phone: (617)897-5111, Ext. 5218, 5907
Boston Area: (617)890-0330
TWX: 710-347-0212
Cable: Digital Mayn
Telex: 94-8457

3. Maintaining the required logs and report files consistently and accurately.

4. Making the necessary documentation available in a location convenient to the system.

5. Keeping the exterior of the system and the surrounding area clean.

6. Turning off the teletypewriter and/or line printer when these devices are not in use.

7. Performing the specific equipment care operations described for the various devices at the suggested frequencies, or more often if usage and environment warrant.

8. Ensuring that ac plugs are securely plugged in each time equipment care operations are performed.

4.3 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; it is imperative that the tape be kept clean.

2. Always store tape reels inside containers when not in use; keep the empty containers tightly closed to keep out dust and dirt.

3. Never touch the portion of tape between the BOT and EOT markers; oil from fingers attracts dust and dirt.

4. Never use a contaminated reel of tape; this will spread dirt to clean tape reels, and could have an adverse effect on tape transport reliability.

5. Always handle tape reels by the hub hole; squeezing the reel flanges could lead to tape edge damage in winding or unwinding tapes.

6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.

7. Do not place magnetic tape near any line printer or other device that produces paper dust.

8. Do not place magnetic tape on top of the tape transport, or in any other location where it might be affected by hot air.

4.4 CARE OF TS03 TAPE TRANSPORT

4.4.1 General

Digital Equipment Corporation tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

4.4.2 Preventive Maintenance

To ensure continuing trouble-free operation, a preventive maintenance schedule should be kept. Only a few items are involved, but they are very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

Before performing any cleaning operation (Table 4-1), remove the supply reel and store it properly. All items in the tape path must be cleaned on a per-shift basis. In cleaning, it is important to be thorough yet gentle and to avoid certain dangerous practices. It should be remembered that the tape cleaner is a strong cleaning agent and should not come in contact with painted surfaces or plastic.

CAUTION

Do not use: **acetone or lacquer thinner; aerosol spray cans; rubbing alcohol; excessive cleaner. Be extremely careful *not* to allow the cleaner to penetrate ball bearings, tension rollers, and motors.**

4.4.3 Materials Required

1. DECmagtape system and magtape cleaning kit
2. Lint-free wipers

Table 4-1
Customer Equipment Care Operations

Device: TS03 DECmagtape Transport

Freq	Operation
Once per Shift	1. Clean tape path according to the following procedure. (Time required = 5 min.) a. Remove tape from transport. b. Using head cleaner and lint-free cloth, clean the following (Figure 4-1): Head and head shield Load point/end-of-tape sensor Missing tape sensor Both tape guides Tape cleaner Tape tension roller (not shown) Capstan (not shown) c. Using a clean, dry, lint-free cloth or wipe, once again go over each surface listed above to dry and remove any residue. **NOTE** **Do not use any cloth or wipe that has come in contact with the tape path as it is probably contaminated.** d. Using a clean, lint-free cloth or wipe, dust the inside and outside of the plexiglass door. If dirt and dust have accumulated, a mild soap and water solution or antistatic cleaner may be used. Ensure that the door is dry before returning the tape transport to service.

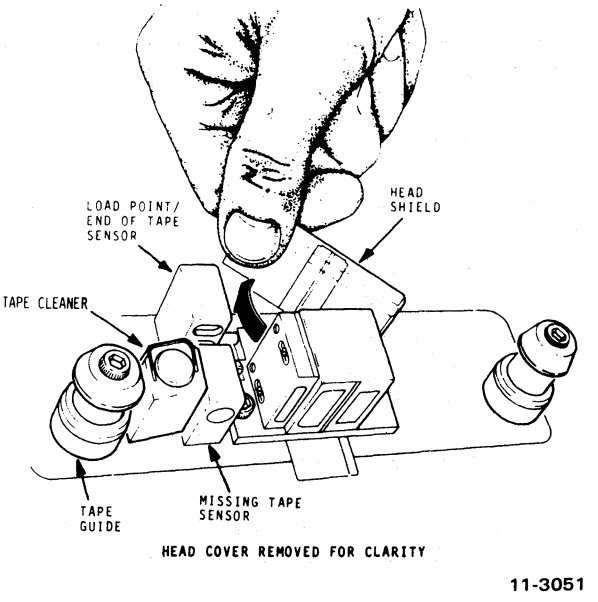


Figure 4-1 Opening Head Shield

CHAPTER 5
SYSTEM MAINTENANCE

5.1 SCOPE

The chapter provides a complete description of TMA11-M preventive and corrective maintenance procedures.

5.2 MAINTENANCE PHILOSOPHY

The TMA11-M DECmagtape System is highly reliable and will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

The preventive maintenance required on each unit differs in accordance with its design. The TMA11 Controller, M8920 adapter, and H720 power supply are total solid state units with no moving parts; therefore, no preventive maintenance is required on these units. The TS03 transport, however, requires daily customer care consisting of head and tape path cleaning (Chapter 4). Otherwise, the transport requires very few adjustments and these should not be performed unless problems are encountered in transport operation. See Table 5-3 for the recommended preventive maintenance procedure.

Corrective maintenance consists of troubleshooting at the system level using system diagnostics and visual observations to localize the failure to a particular unit, whether it be the TMA11 Controller, the M8920 adapter, the TS03 transport, or the H720 power supply. Once the faulty unit is determined, unit level troubleshooting will be performed using unit functional block diagrams, engineering flow diagrams, timing diagrams, and detail logic diagrams to localize the failure to an electrical module or mechanical part.

NOTE

In the case of the TS03 transport, troubleshooting tables are provided (see Tables 5-5 and 5-6) listing the symptoms, possible causes, indications, and recommended actions.

Once the faulty module or mechanical part is located, it should be replaced. If the faulty part is a module, it should be returned to the depot for repair; if a mechanical part fails, it should be replaced and repaired only if the cost warrants it.

5.3 TEST EQUIPMENT

Test equipment required to maintain the TMA11-M falls into two categories: standard test equipment and special test equipment.

5.3.1 Standard Test Equipment

Maintenance procedures for the TMA11-M require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes.

Table 5-1
Standard Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630NA or 260
Oscilloscope	Tektronix	Type 453 or equivalent
X10 Probes (2)	Tektronix	P6008
Diagnostics (MAINDECS)	Digital	See Paragraph 5.9.1

5.3.2 Special Test Equipment

The special test equipment and tools required are listed in Table 5-2.

Table 5-2
Special Test Equipment and Tools

Equipment	Manufacturer	Designation
Test Panel	Digital	29-21922
General Tape Kit (Paragraph 5.3.3)	Digital	–
Tape Path Tool	Digital	29-21904
Transport Module Extender	Digital	29-21925

5.3.3 General Tape Kit

The kit consists of:

Item	Part No.
Skew tape (7 in. reel)	29-19224
Head cleaner	–
Capstan cleaner	–
Magna-See® (also renew solution)	29-16871
Magnifying glass	29-20273
Reflective tape marker	90-91777
Write ring	–
Lint-free cloth (Kimwipes)	
Scotch tape	

5.4 PREVENTIVE MAINTENANCE

At 6-month intervals, it is advisable to peak-up and check the TS03 operating parameters. This is done to ensure that progressive degradation will not cause customer outage. The PM procedures (Table 5-3) should be performed in the sequence listed for maximum efficiency and to reduce the interaction of adjustments.

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Table 5-3
TS03 Preventive Maintenance Procedure

Device TS03 DECmagtape Transport **Sheet** 1 of 7

Freq	Operation
	1. Clean the reel hubs according to the following procedure (time required = 5 min): a. Remove O-ring from the hub. b. Clean with a mild solvent. Ensure that there is no residue from the solvent. c. Lubricate the O-ring with Dow Corning 4 compound or equivalent silicone grease. Wipe off as thoroughly as possible, leaving a thin film. d. Replace the O-ring on the hub.
	2. Align the tape path according to the following procedure (time required = 10 min): **NOTE** **For proper transport operation, the items in the tape path must be accurately aligned. Tapes in the area of the head are not shimmed or adjusted. The tension roller guides must be set to two criteria: they must be aligned to the tape guides and they must have their axes at right angles to the tape. These two steps are necessary to ensure that the tape passes over the head correctly.** a. Turn transport power off. b. Remove the head cover. c. Remove both tape guides (keep each assembly together) (Figure 5-1).

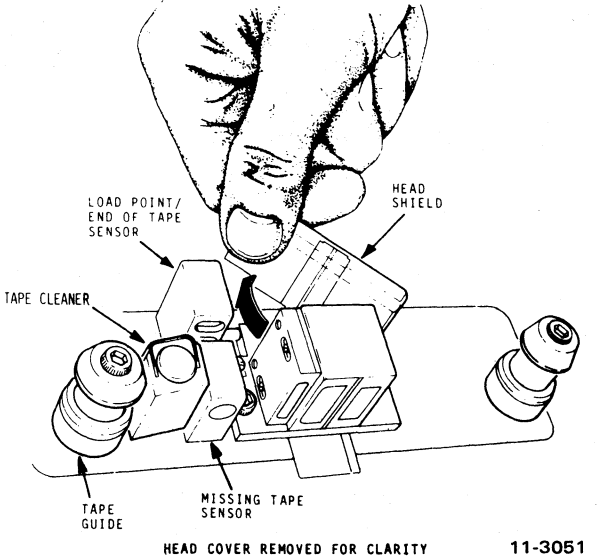


Figure 5-1 Opening Head Shield

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

System TS03 DECmagtape Transport **Device** _____ **Sheet** 2 of 7

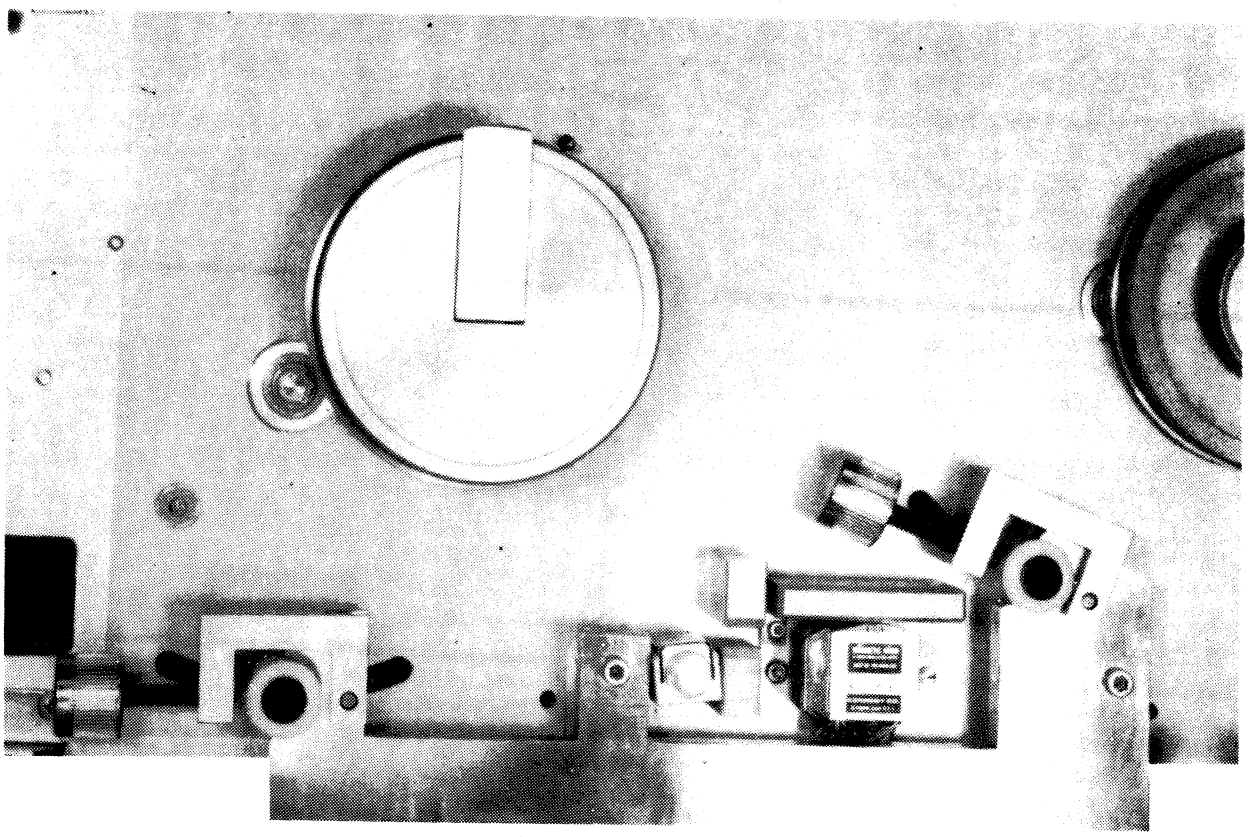
Freq	Operation
	d. Remove the operator control panel.
	e. Mount the tape path alignment tool on the deck per Figure 5-2.
	NOTE **The screws need only be finger-tight.**
	
	Figure 5-2 Use of Alignment Tool
	f. Pull each tape tension arm into the notch provided on the ends of the tape path alignment tool. Check that the roller guide is parallel to the tool and that the reference edge of the roller guide (outside edge) fits snugly against the outer edge of the tape path alignment tool. If the roller guides do not require adjustment, skip to step 3; otherwise, proceed to step g.
	g. Loosely clamp the roller guide in the tape path alignment tool (Figure 5-2).
	h. Loosen the roller guide split clamp screw (item C in Figure 5-3) and remove the roller shaft from the tension arm. Do not loosen the adjustment lockscrew (item A, Figure 5-3).

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

Device TS03 DECmagtape Transport **Sheet** 3 of 7

Freq	Operation

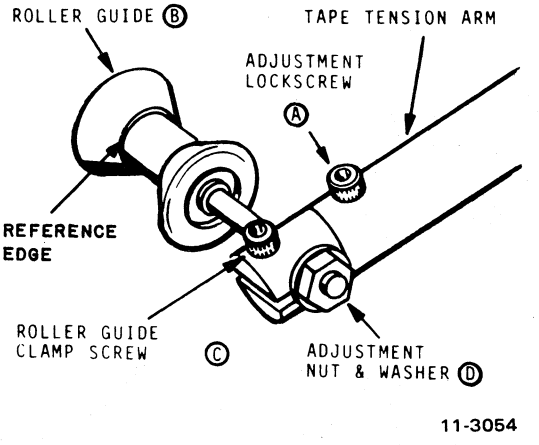


Figure 5-3 Roller Guide Adjustment

i. The shaft end is threaded to allow use of a nut for fine adjustment. The thread does not enter the clamp area. Place several No. 10 flat washers over the threaded end and install a 10-32 nut as shown in Figure 5-3.

j. Push the shaft so that the roller is too far forward. Tighten the nut lightly.

k. Tighten the adjustment nut until the reference edge of the roller guide just touches the tape path alignment tool.

l. Parallelism can now be set by loosening the adjustment lockscrew (item A, Figure 5-3) and retightening after the adjustment is made.

NOTE
Ensure that the reference edge of the roller guide is still set per step k.

m. Remove the adjustment nut and washer (item D, Figure 5-3).

3. Check the magpot (Figure 5-4) according to the following procedure (time required = 5 min):

a. Release the left tape tension arm from the clamp on the tape path alignment tool.

b. Place a short strip of magnetic tape on the head to disable the tape broken sensor.

c. Remount the operator control panel, power up the transport, and press the LOAD switch.

d. With the tape tension arm relaxed (pulled to the left), the supply reel should be turning counterclockwise.

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

Device TS03 DECmagtape Transport **Sheet** 4 of 7

Freq	Operation

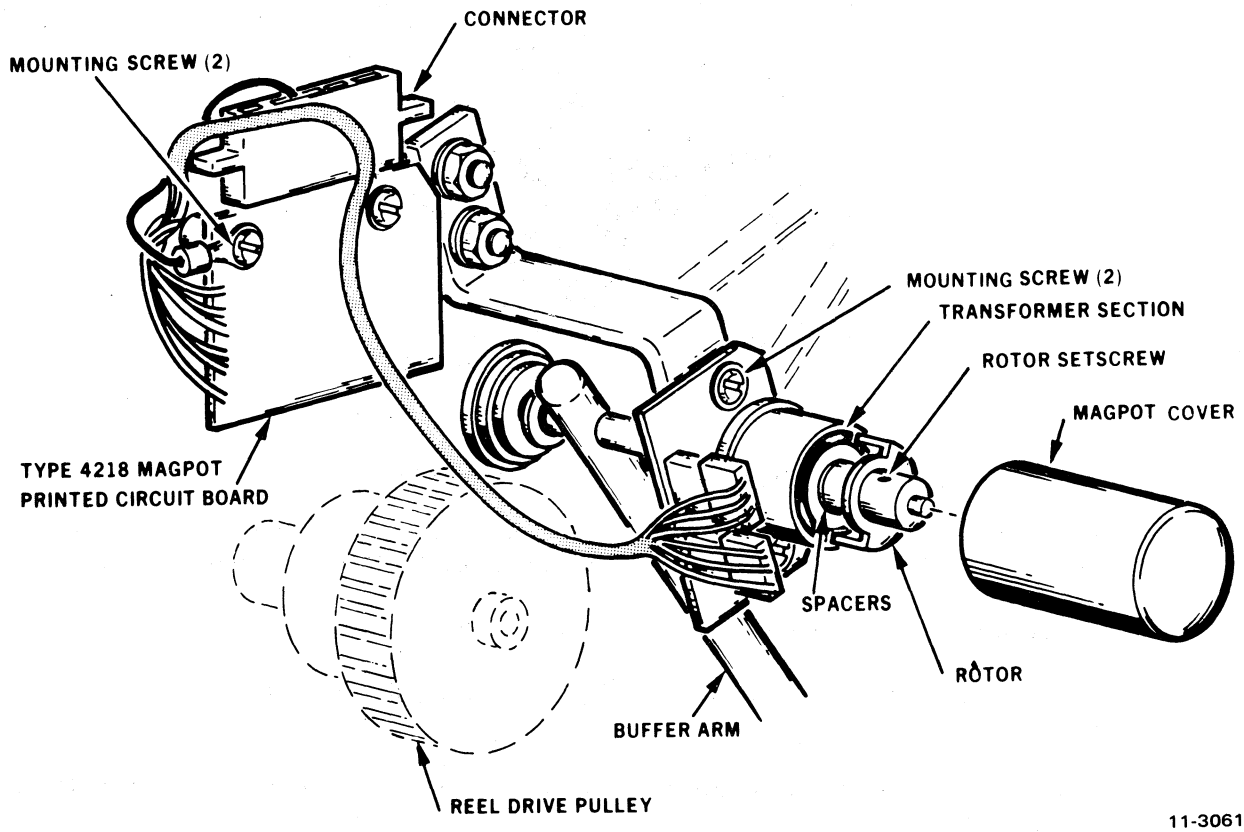


Figure 5-4 Magpot Position Sensor Assembly

e. Pull the arm into the V provided in the tape path alignment tool. The motor should now be null (no rotation). If the reel rotates in either direction, go to step i.

f. Release the right tape tension arm from the clamp on the tape path alignment tool.

g. With the tape tension arm relaxed (pulled to the left), the takeup reel should be turning counterclockwise.

h. Pull the tension arm back into the V provided in the tape path alignment tool. The reel motor should be null. If the reel motor rotates in either direction, go to step i; otherwise, proceed to step k.

NOTE
The following procedure is for the reel motors that continue to rotate while in the V-groove of the tape path alignment tool.

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

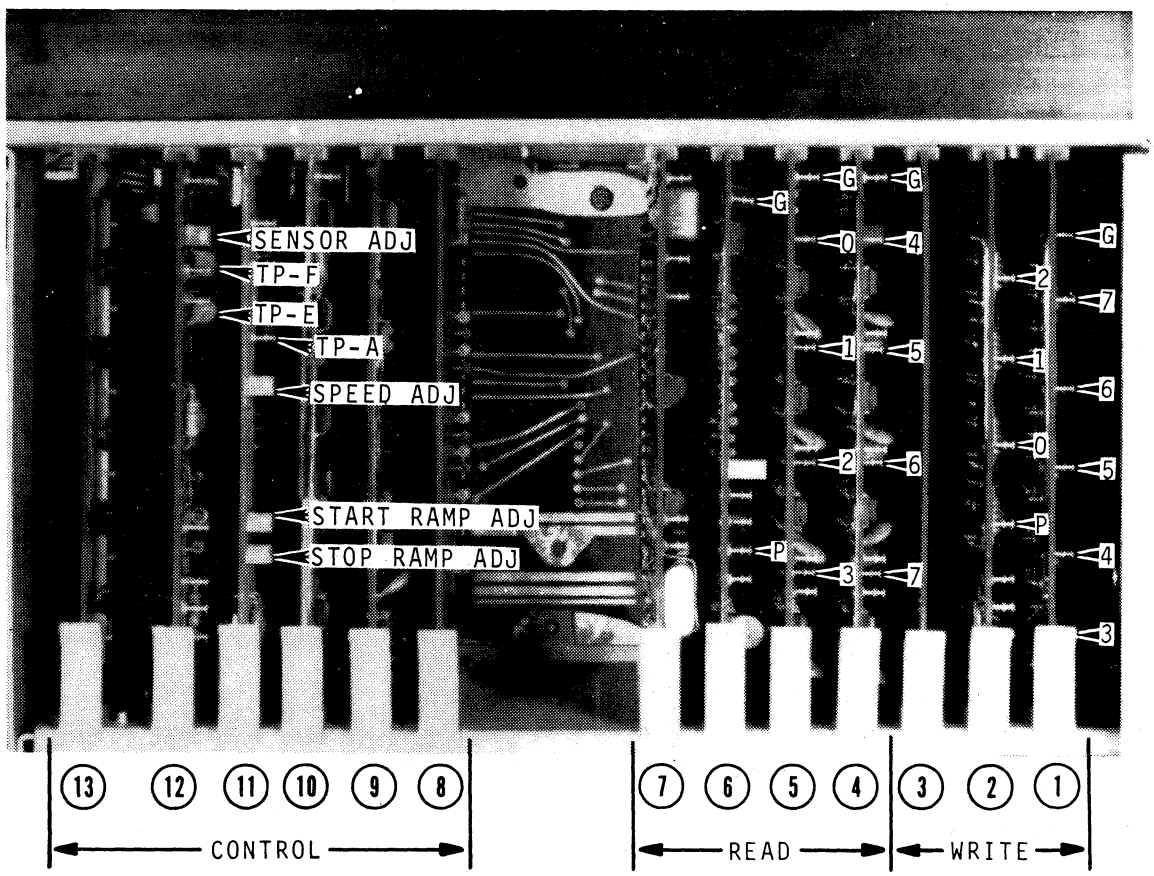
Device TS03 DECmagtape Transport **Sheet** 5 of 7

Freq	Operation
	i. Hold the tape tension arm in the V provided in the tape path alignment tool. Loosen the set screw holding the armature on the pivot shaft. Rotate the armature until the reel stops rotating or has minimum rotation. j. Press the armature firmly against the transformer section and tighten the rotor set screw. k. Turn off the transport. l. Remove the tape path alignment tool. m. Restore the tape guides and head cover.
	4. Adjust the photosensor in accordance with the following procedure (time required = 5 min): a. Connect a dc voltmeter between test points E and F of the sensor amplifier driver in slot 11 (Figure 5-5). **NOTE** **If a scope is to be used, it must not be grounded. The probe may now be used on a test point and the ground lead for the probe on the other test point.** b. Adjust the sensor adjustment potentiometer (R16) for 0 V.
	5. Check the capstan per the following procedure (time required = 5 min): a. Turn transport power off. b. Mount the servo preamplifier in slot 13 on the extender board. c. Connect a scope to test point A of the servo preamplifier. **NOTE** **Test point A is accessible only while the module is on the extender.** d. Turn transport power on and load a scratch tape. e. Adjust potentiometer R56 for 0 V. **NOTE** **The capstan must remain stable and not rotate at all.** f. Turn transport power off. Remove the extender board and reinsert the servo preamplifier in slot 13.

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

Device TS03 DECmagtape Transport **Sheet** 6 of 7

Freq	Operation



13	4306-002	SERVO PREAMPLIFIER	7	4845-001	TIMING DELAY
12	3844-001	SENSOR AMPLIFIER/DRIVER	6	4179-004	P CHANNEL/CLIPPING
11	3645-002	RAMP GENERATOR	5	4178-004	QUAD READ AMPLIFIER
10	3843-001	PUSHBUTTON CONTROL	4	4178-004	QUAD READ AMPLIFIER
9	3842-001	INTERFACE CONTROL	3	3860-001	DATA TERMINATOR
8	3841-001	CONTROL TERMINATOR	2	3848-001	4 CHANNEL HEAD DRIVER
			1	3849-001	5 CHANNEL HEAD DRIVER

Figure 5-5 Plug-In Module and Test Point Locations

Table 5-3 (Cont)
TS03 Preventive Maintenance Procedure

Device TS03 DECmagtape Transport **Sheet** 7 of 7

Freq	Operation
	6. Using the instructions included in Appendices A, B, C, and D, run the TMA11 Instruction Test (MAINDEC-11-DZTMA-E), the TS03 Supplemental Test (MAINDEC-11-DZTSF-A), the TS03 Drive Function Timer (MAINDEC-11-DZTSE-A), and the TMA11 Multidrive Data Reliability Exerciser (MAINDEC-11-DZTMH-A) (time required = 25 min).
	7. Return the tape subsystem to operational status for customer use (time required = 5 min).

5.5 TS03 DECmagtape TRANSPORT ADJUSTMENTS

Figure 5-6 illustrates the recommended sequence for performing all adjustments on the TS03 DECmagtape Transport. References are made to paragraphs describing the adjustments.

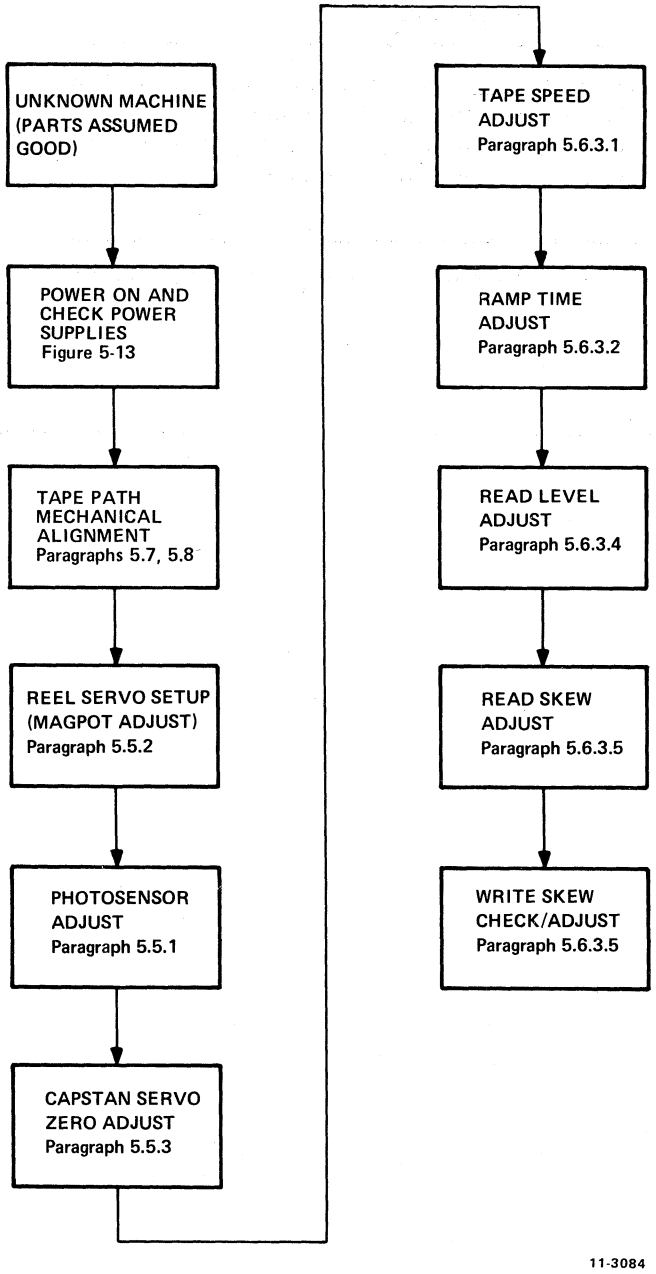


Figure 5-6 Adjustment Sequence

5.5.1 Photosensor Adjustment (Figure 5-5)

Photosensor elements used to detect the load point and EOT are cadmium sulfide photoresistive cells. Their characteristics sometimes vary with time and light history. An adjustment is provided to ensure their proper operation. Need for adjustment will be indicated if the load point or EOT is not observed by the sensors. To adjust:

1. Verify that both lamps at the photosensor are illuminated.

2. Connect a dc voltmeter from test point E to test point F on the sensor amplifier/driver module.

NOTE
These points are both off ground. If a scope is used instead of a voltmeter, it must be isolated from ground or the two inputs added with one channel inverted.

3. Adjust potentiometer R16 so that there is 0 V between test points E and F.

5.5.2 Magpot Adjustment (Figure 5-5)

Magpots that provide position feedback to the reel servos should not require adjustment since only passive components and their geometry determine their zero settings. If one is moved by severe damage to the machine or if replacement is necessary, refer to the detailed circuit description in Chapter 3 of Part III for adjustment details.

5.5.3 Capstan Zero Adjustment (Figure 5-5)

The capstan must not move, even slightly, when at zero speed setting. A zero adjustment is provided on the servo preamplifier to remove effects of component tolerances. To determine if adjustment is required, observe the following:

1. If the capstan rotates slowly when it should be standing still, grasp the capstan with tape loaded and turn first clockwise and then counterclockwise. The capstan will show a reluctance to turn. If turned gently, a small dead zone can be detected. This dead zone should be approximately the same for both directions of motion. If adjustment is required, connect a volt-ohmmeter or scope probe to test point A of the servo preamplifier module.

2. Extend the Type 4306 Servo Preamplifier module.

3. Load tape to the load point.

4. Rotate zero adjustment potentiometer R56 to bring the measured voltage to zero.

5.6 TEST PANEL USE

The test panel is packaged in a box and supplied as Model 9900 for use with TS03 transports (Figure 5-7). The controls and indicators, together with brief descriptions of their purpose, are shown in Figure 5-8. Note that the box allows tape to be moved in either direction at normal or fast speed. Motion is interlocked to prevent running off reels at either end. Additionally, the 9900 allows writing an all-1s pattern on the tape and provides indicators for skew, data, load point, and EOT.

The test panel is intended to be used in checking the TS03 transport when off-line or when completely isolated from the operating system. The controls provided are useful under these circumstances but under normal operation they would be confusing and invite possible operator error.

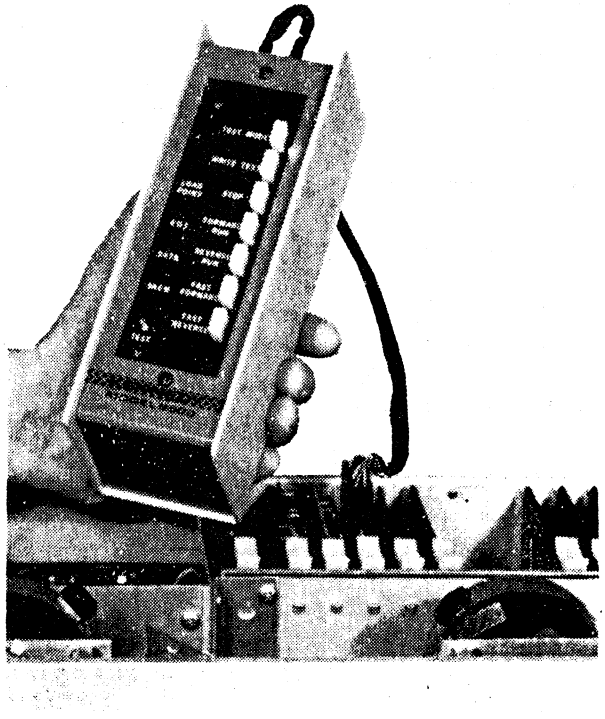


Figure 5-7 Test Panel Installation

5.6.1 Operations

The test panel becomes operational only in test mode, selected by pressing the alternate action TEST MODE pushbutton. For the TEST MODE button to be operational, the machine must be off-line and STOP must be depressed. Test mode is terminated by either pressing the alternate action TEST MODE button or pressing the ON LINE pushbutton.

A characteristic of transport electronics is that when LOAD is pressed, the machine feeds forward to the load point. If tape is already wound on the machine and the load point marker has been passed, the search will continue to the end-of-tape unless REWIND is pressed. This characteristic is sometimes troublesome when servicing the machine. Under these circumstances pressing TEST MODE will terminate search and induce an ON TAPE status in the control electronics. If ON LINE is subsequently pressed, the ON TAPE status is retained. This feature can be adapted to allow power turn-off while tape is loaded.

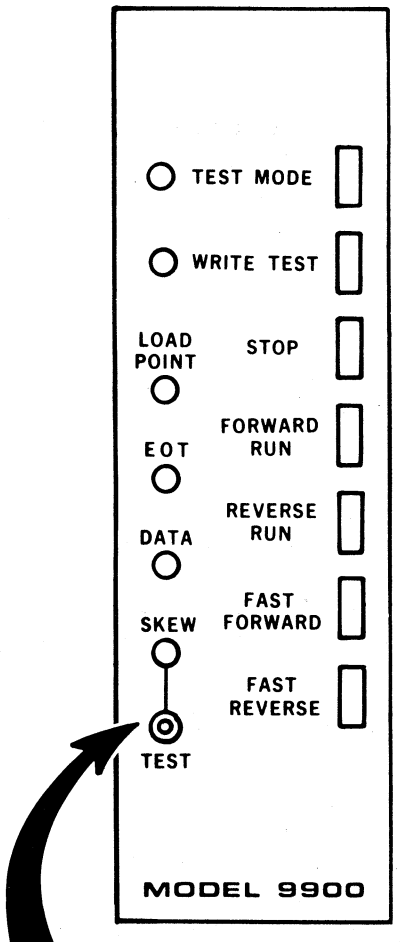
When using tape motion pushbuttons, the STOP button should be pressed between changes in speed or direction. No harm will result if this is not done, but on occasion switch bounce will cause the command to be unrecognized and the last motion signaled will be retained.

5.6.2 Indicators

5.6.2.1 SKEW Indicator – This is an LED indicator which flashes if skew is being encountered. Logic in the data section detects skew to two different criteria and lights the indicator. The skew gate in the NRZI read electronics is normally open for 50 percent of one character time. If pulses fall outside the skew gate, they trigger the indicator. In test mode, the skew gate is narrowed to 5/32 of a character time. An all-1s pattern on a properly adjusted machine should fall inside the shortened gate. A tape with random data suffers from pulse crowding effects and will not, in general, fall inside the gate. Thus in test mode the SKEW light indicator is valid for an all-1s data pattern only.

NOTE

Tape transport must be off-line and STOP pushbutton depressed before test panel can become functional.



TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates the test panel. When the indicator (LED) is illuminated, the test panel is active. (Tape unit must be off-line and the STOP pushbutton depressed before the test panel will function.)

WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1s to be written on all channels to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator remains illuminated while the unit is in this mode.

STOP pushbutton. An interlocked pushbutton switch that terminates all tape motion.

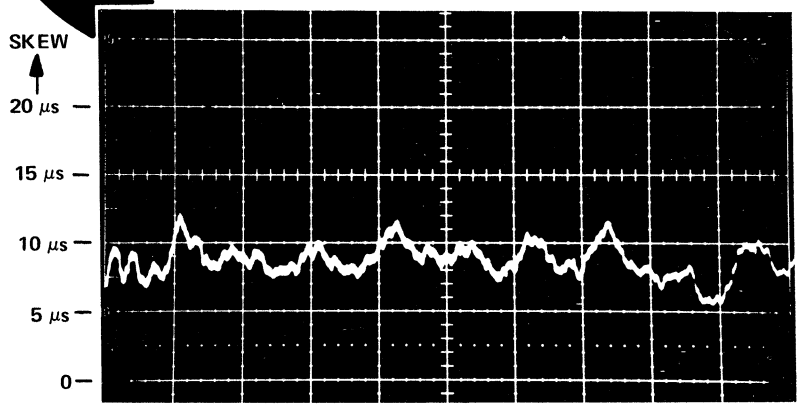
FORWARD RUN pushbutton. An interlocked pushbutton switch that allows the tape unit to proceed forward at normal speed. Depressing the STOP pushbutton or an EOT marker terminates this operation.

REVERSE RUN pushbutton. An interlocked pushbutton switch that allows the tape unit to run in reverse at normal speed. Deprssing the STOP pushbutton or a load point marker terminates this operation.

FAST FORWARD pushbutton. An interlocked pushbutton switch that allows the tape unit to run forward at fast speed. Depressing the STOP pushbutton or an EOT marker terminates this operation.

FAST REVERSE pushbutton. An interlocked pushbutton switch that allows the tape unit to run in reverse at fast speed. Depressing the STOP pushbutton or a load point marker terminates this operation.

SKEW TEST point. The SKEW TEST point measures total character skew of all nine tracks by means of a sample-and-hold circuit. The calibration of this test point is 10 μs of character skew per 1 V of output. To measure skew, set the scope for 0.5 V/div vertical and 100 ms/div horizontal and observe skew waveform as shown.



Dynamic Character Skew

Figure 5-8 Model 9900 Test Panel

5.6.2.2 DATA Indicator – The DATA indicator is illuminated when the tape being read has data written on it at a level sufficient to activate the read electronics. It blinks when reading gapped data.

5.6.2.3 LOAD POINT Indicator – This LED lights when the load point is sensed.

5.6.2.4 EOT Indicator – EOT is indicated when the end-of-tape marker is sensed in the forward direction and remains true until it is passed in the reverse direction.

NOTE
All indicators operate whether or not TEST MODE is selected.

5.6.3 Utilization Procedures

5.6.3.1 Speed Adjustment – Normal speed of the unit is determined by the setting of R14 on the ramp generator card. This control is set at the factory and does not normally require adjustment. To check speed:

1. Mount a skew master tape on the machine as in the read skew adjustment (Paragraph 5.6.3.5).

2. Observe the waveform at one preamplifier test point.

3. Set the time for one complete sine wave cycle (two bits) at 200 μs by adjusting R14. Note that the waveform will not be entirely stationary on the scope due to small, rapid speed variations. These should be visually averaged.

4. If a speed adjustment was made, check the read preamplifier gain settings (Paragraph 5.6.3.4).

5.6.3.2 Ramp Time Adjustment – Tape is brought up to speed at constant acceleration. To control tape velocity, a ramp voltage is generated by the ramp generator which rises linearly to the required running speed and falls linearly to zero at stop (Figure 5-9). Ramp time should accelerate the tape to running speed in 0.19 in. of travel. This timing is of utmost importance in gap generation on tape and must be accurately set. Ramp time is 15 ms at 25 in./sec and varies inversely with speed. Thus, at 12.5 in./sec it is 30 ms and at 37.5 in./sec it is 10 ms. This voltage may be observed at test point A of the ramp generator card.

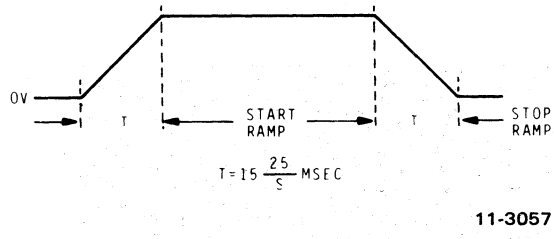


Figure 5-9 Ramp Time Adjustment

The test panel may be used to make ramp time measurements by starting and stopping the machine via the FORWARD RUN and REVERSE RUN pushbuttons. This is difficult, however, because the buttons must be pushed as the scope is observed. Measurement under rapid start/stop commands fed to the synchronous forward input is much easier. In reverse operation, timing is the same as in forward but the polarity is reversed – the ramp is negative-going. To adjust ramp time:

1. Establish rapid start/stop motion.

2. Observe waveforms at ramp generator test point A. Synchronize on run command; be sure time is long enough to produce a flat area between ramps.

3. Set the start rise time at the proper value using R3 on the ramp generator module.

4. Set the stop fall time using R4 on the ramp generator module.

5.6.3.3 Rewind Speed – Rewind speed is not adjustable. It is determined by fixed values on the ramp generator card.

5.6.3.4 Read Level Adjustment – This adjustment sets the gain of the read preamplifiers to the correct level. Too much gain will introduce noise and too little will aggravate dropouts.

1. Load a reel of scratch tape on the transport with the write enable ring in place.

2. Press TEST MODE.

3. Press WRITE TEST and FORWARD RUN.

4. Observe waveforms at the test point for each channel on the read preamplifier.

5. The signal observed should appear as an approximate sine wave. Noise introduced by crosstalk from the write head will be present but the waveform should not be badly distorted by this.

6. Measure peak-to-peak amplitude and set for 9 ± 0.5 V using the channel gain control on the read preamplifier. Repeat for each channel. Note that the read level is about 10 percent higher when the machine is operating in the read-after-write mode than when in the read mode. This effect is caused by small, unavoidable magnetic remanence in the write head and the erase head. Skew master tapes should *not* be used as amplitude reference for this reason.

5.6.3.5 Skew Adjustment – Skew is one of the most important parameters in reading NRZI data. Since, in a read-after-write head, data is read with one gap and written with a second gap, read and write skew are, in general, different and must be compensated separately. The machine is deskewed only when both are properly set. In TS03 transports, the read gap is deskewed mechanically while digitally controlled delays are used to deskew the write gap.

Read Skew Adjustment – In deskewing the read gap, the head is mechanically tilted to have its gap at an exact right angle to the tape. This is accomplished using a skew master tape (Paragraph 5.3.3).

a. Load a skew master tape on the transport. Be sure the write enable ring is removed.

b. Press TEST MODE.

c. Press FORWARD RUN.

d. Observe the SKEW indicator and adjust the skew-adjustment screw on the head mounting plate (Figure 5-10) until the indicator does not come on.

For greater precision, a scope probe may be connected to the TEST terminal on the test panel. At this point, the pattern will be a grouping of nine pulses as each channel "reports in." The optimum skew setting is the one at which these pulses occupy the minimum spread.

If the test panel is not available, this signal is available at pin 8 of the test panel connector on the pushbutton control module.

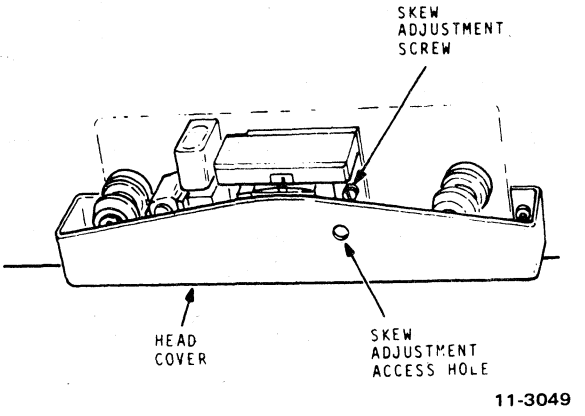


Figure 5-10 Head Skew Adjustment

Write Skew Adjustment – TS03 transports feature a unique digital deskewing arrangement for deskewing the write head. Since write-read skew is a function of head geometry and does not change, write deskewing delays are determined at the factory and each head has a deskewing chart showing the appropriate write amplifier deskew switch settings for that head. All channels are referenced to the P channel.

If for some reason it is necessary to deskew the write head in the field, the procedure is as follows:

1. Proceed as in a read level adjustment (Paragraph 5.6.3.4).

2. Connect dual channel scope channel 1 to the P channel test point on the read preamplifier. Set alternate sweep and trigger channel 1 internal.

3. Connect scope channel 2 to the test point for tape channel 5 and observe the pattern (Figure 5-11). Set the sweep to display 1/2 sine wave cycle.

4. Observe separation of peaks displayed. Note that because of small variations in speed and skew, the pattern will not be entirely stationary.

5. Set the skew switch for channel 5 for minimum peak separation.

6. Repeat for each of the remaining seven channels.

5.7 TAPE PATH ALIGNMENT

For proper transport operation, the items in the tape path must be accurately aligned. Tape guides are fixed in location and are not shimmed or adjusted in any way. The tension roller guides must be set to two criteria:

1. Roller guides must be aligned with tape guides.

2. Roller guides must have their axes at an exact right angle to the tape.

The more convenient and accurate technique for alignment uses a special alignment tool, Part No. 154-0035-001, shown in Figure 5-2.

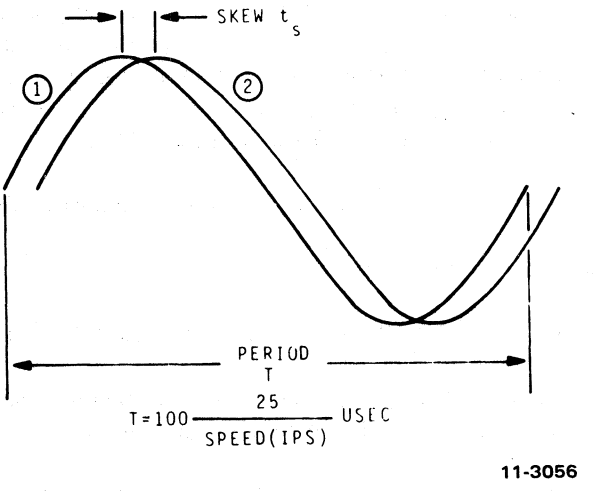


Figure 5-11 Skew Adjustment Waveforms

5.7.1 Alignment Procedure

1. Loosen the roller guide clamp screw (both rollers) (item C in Figure 5-3).
2. Loosen the roller guide adjustment lockscrew (both rollers) (item A in Figure 5-3).
3. Remove the tape guides by removing the mounting screws (keep together as sets).
4. Remove the head cover and control panel.
5. Using the guide mounting screws, mount the alignment tool. Tighten the mounting screws finger-tight.
6. Clamp the roller guides to the alignment tool with the guide portion approximately centered in Vee.
7. Tighten the adjustment lockscrews and snug roller guide clamp screws. This sets the angularity of the roller guide axes.
8. Loosen the tool clamp screws one at a time.
9. Holding the roller guide against Vee, press the roller guide toward the panel until the outer edge of its guide area reference edge touches the tool's outer surface. This sets the roller guide height.
10. Tighten the roller guide clamp screw.
11. Remove the tape path alignment tool and replace the tape guides.

With roller guides aligned as described above, only one critical item remains in the tape path – the drive capstan. Its surface must lie accurately at a right angle to the tape surface. The capstan motor can be tilted slightly by the action of two set screws in the front panel. To determine if adjustment is required, run the tape forward and reverse about 1 ft each way and observe whether the tape maintains the same position on the capstan for each direction. If the tape moves more than 1/32 in., adjustment is required. To adjust (Figure 5-12):

1. Loosen slightly outboard motor mounting screws I and IV, and loosen inboard screws II and III.

2. Run tape forward and reverse, observing motion on the capstan.

3. Tighten left-hand set screw A slightly. If motion decreases, adjust for minimum motion.

4. If motion increases, loosen set screw A, tighten inboard mounting screws II and III snugly, loosen outboard mounting screws I and IV, and repeat using right-hand set screw B.

5. When minimum motion has been found, tighten all four mounting screws.

6. If set screw A has been used, tighten mounting screws I and IV first, then II and III. If set screw B has been used, tighten mounting screws II and III first, then I and IV.

7. Observe tape motion through the tape guides. When properly aligned, tape will have a slight tendency to follow the spring loaded (inside) guide edge when it is depressed manually. If tape runs hard against either guide, surface alignment is not correct.

8. Observe and adjust skew using a skew master tape. (See Skew Adjustment, Paragraph 5.6.3.5.) Skew should be about the same forward and reverse.

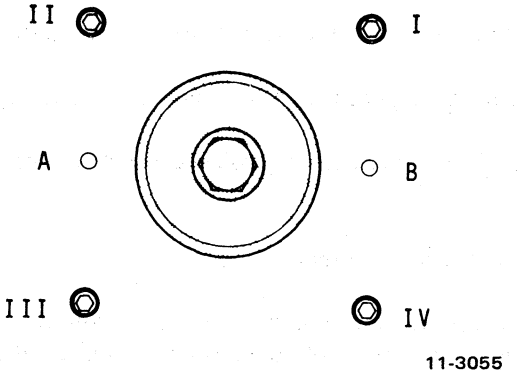


Figure 5-12 Capstan Parallelism Adjustment

5.7.2 Tape Path Alignment Without Use of Alignment Tool

It is possible though somewhat tedious to adjust the tape path without using alignment tools. Most difficult is setting squareness of the roller guides. A procedure is:

1. Remove the roller guide to be aligned and replace it with a length (4 in. approximately) of 0.1875 in. stainless steel ground stock. Clamp in place.

2. Loosen the roller guide lockscrew slightly so that the moderate pressure rod can be rotated.

3. Thread tape over the rod.

4. While holding the rod, run tape forward. Tilt the rod back and forth until a position is found at which tape runs with equal tension on the inside and outside and tape enters the tape guides correctly, or in the case of the takeup roller guides, winds correctly on the center of the takeup reel.

5. When the position is found, tighten the lockscrew securely.

6. Replace the roller guide and adjust height (Paragraph 5.10.1).

7. Check alignment as described above and revise if required.

5.8 HEAD FACE SHIELD ADJUSTMENT

A shield is located over the magnetic head surface to reduce write-read crosstalk. Its spacing, determined by a spring stop, is important. The spring stop is adjustable as follows:

1. Loosen the stop screw with tape removed from the machine.

2. Insert three thicknesses of tape (0.006 in.) between the shield surface and the top surface of the head. Do not use feeler gauges, since they may scratch the head surface.

3. Press the shield against the tape firmly and tighten the stop screw.

4. Remove the tape pieces by lifting the shield.

5.9 CORRECTIVE MAINTENANCE

Corrective maintenance information is provided to guide and aid the maintenance technician in isolating and repairing faults. The information consists of five troubleshooting aids: the TMA11-M diagnostics, the corrective action flow diagram, the maintenance block diagram, TS03 transport troubleshooting hints, and TS03 transport troubleshooting tables.

5.9.1 TMA11-M Diagnostics

Diagnostics, consisting of a paper tape and documentation, are provided with each system. The documentation includes instructions on loading, running, and interpreting diagnostic printouts. The diagnostics provided with the TMA11-M are listed below:

TMA11 Instruction Test	MAINDEC-11-DZTMA-E-D/PB
TMA11 Data Reliability	MAINDEC-11-DZTMB-B-D/PB
TMA11 Multidrive Data Reliability Exerciser	MAINDEC-11-DZTMH-A-D/PB
TS03 Drive Function Timer	MAINDEC-11-DZTSE-A-D/PB
TS03 Supplemental Instruction Test	MAINDEC-11-DZTSF-A-D/PB
TS03 Utility Driver	MAINDEC-11-DZTSG-A-D/PB

5.9.2 Corrective Action Flow Diagram

Figure 5-13 provides sequential procedures for troubleshooting the TMA11-M.

5.9.3 Maintenance Block Diagram

Figure 5-14 functionally separates the circuitry comprising the four major units (TMA11, M8920, TS03, and H720) into functional blocks and depicts signal flow between those blocks within each unit; it also depicts interfacing between each unit and interfacing between the TMA11 and the Unibus.

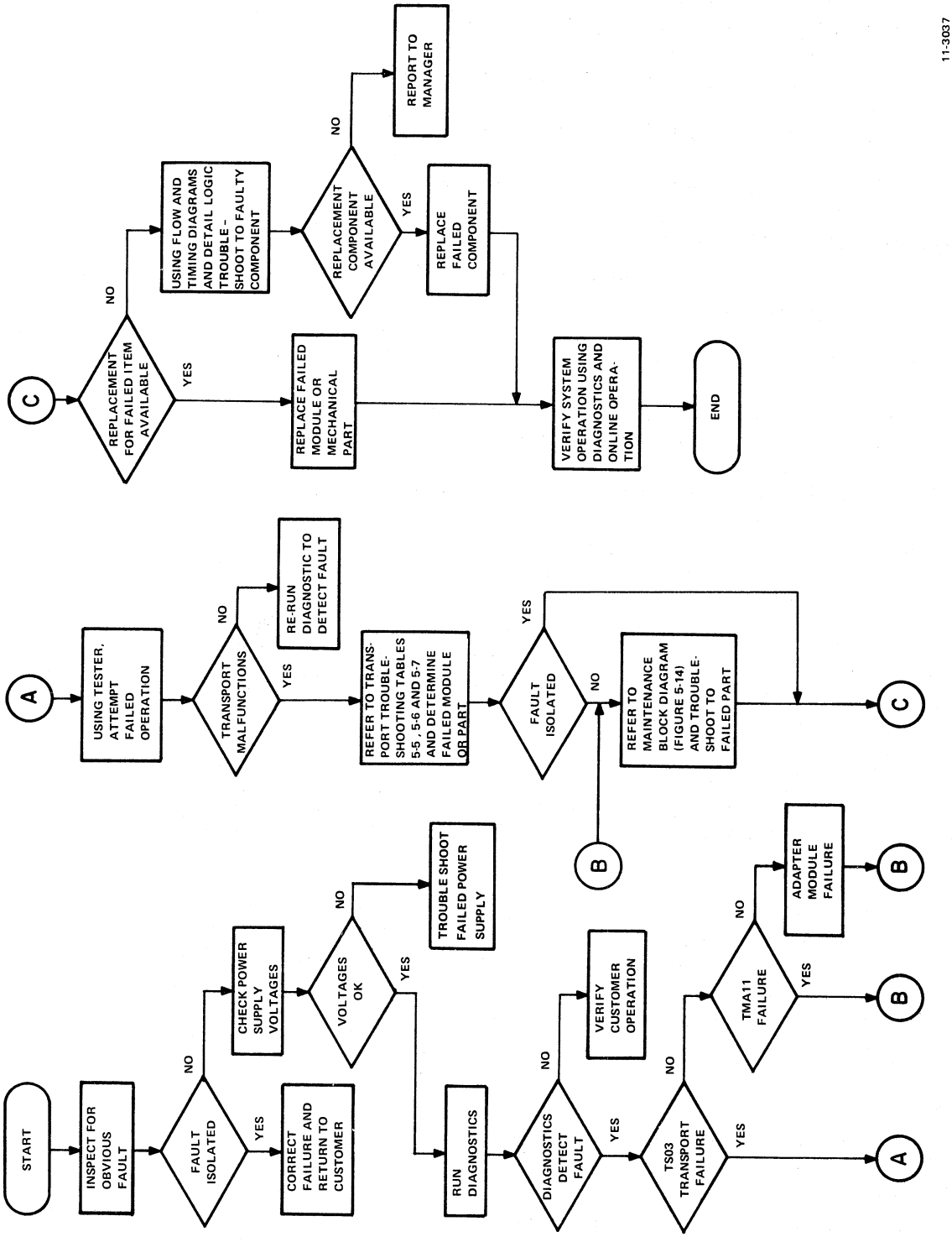


Figure 5-13 TMA11-M Corrective Action Flow Diagram

To Be Supplied

Figure 5-14 TMA11-M Maintenance Block Diagram

5.9.4 TMA11 Controller Troubleshooting Hints

If problems are encountered with the TMA11 50 μs clock, it may need adjustment. To adjust, proceed as follows:

1. Scope pin A31H2 on the TMA11 backpanel.
2. Set the scope for sync positive slope, internal trigger, and 10 μs/cm sweep rate.
3. Adjust the bottom potentiometer on the M307 module in slot A31 for 50 μs wide positive pulse.

5.9.5 TS03 Transport Troubleshooting Hints

Table 5-4 suggests possible causes when problems are encountered with the transport.

5.9.6 TS03 Transport Troubleshooting Tables

Tables 5-5 and 5-6 list transport symptoms versus possible causes, indications, and corrective actions.

5.9.7 Troubleshooting Procedure

When problems are encountered in system operation, the technician should

1. Discuss the symptoms with operation personnel to determine the exact nature of the failure.
2. Refer to the corrective action flow diagram (Figure 5-13) and proceed as directed.

Table 5-4
TS03 DECmagtape Transport Troubleshooting Hints

Problem	Hints
General	Problems in the TS03 transport can usually be classified as either mechanical or electrical but often the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case the problem should be thoroughly analyzed before adjustments are made. Electronic troubleshooting is greatly facilitated by the modular construction – a new card may be substituted and the effect observed. Most difficult, of course, are subtle problems and those of an intermittent nature. Visualizing solution (Magna-See) is useful under certain conditions for troubleshooting. At high densities the data cannot be satisfactorily resolved but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use. If a tape has had visualizing solution applied to it, *do not* reuse that portion of the tape as it will contaminate the head. Cut the visualized portion off and discard. To use visualizing solution, shake the can thoroughly, remove top, and pass portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using Scotch tape and applied to a sheet of paper for a permanent record.

Table 5-4 (Cont)
TS03 DECmagtape Transport Troubleshooting Hints

Problem	Hints
High Error Rate	Usually the more difficult problems involve a higher than permissible error rate for which there is no obvious reason. If operating properly with good tape, the transport should make very few errors in writing and, if rewriting is included in the program, it should make no read errors. Useful clues are: 1. In what mode (read or write) are many errors occurring? 2. At what point in the block does the error occur? 3. What is the nature of the error: VRC, CRC, LRC? 4. Are the errors pattern related? 5. Do errors occur only on certain sets of commands? The first thing to be done is to inspect the head and other items in the tape path for dirt accumulations. Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check interface connections for broken wires or bad contacts. Table 5-5 is a troubleshooting chart concerned with high error rate.
Compatibility	The TS03 transport accepts and produces tapes conforming to the ANSI standards. Occasionally compatibility problems can arise: 1. Tapes written by and acceptable to the TS03 transport are not acceptable to another transport. 2. Foreign tapes cannot be read by the TS03 transport but its own tapes can be. Three items may be involved: skew, speed, ramp times. These should be checked as described in the adjustment procedures.
Other Malfunctions	Normal troubleshooting procedures are involved in finding electronic malfunctions. The first things to check are the supply voltages: ±24 V nominal unregulated will normally be about ±26 V under light load. ±10 V ± 0.5 V +5 V ± 0.25 V

Table 5-4 (Cont)
TS03 DECmagtape Transport Troubleshooting Hints

Problem	Hints
Other Malfunctions (Cont)	Convenient test points for measuring supply voltages are: +24 V – Case of Q9 (MJ802) on heat sink -24 V – Case of Q10 (MJ4502) on heat sink +10 V – Sensor amplifier/driver TPA -10 V – Sensor amplifier/driver TPB +5 V – Sensor amplifier/driver TPC Voltages are measured to chassis (ground). **NOTE** **Turn power off when removing or inserting cards.** If the voltages are not correct, the trouble is in the power supply or the malfunction is loading the supply excessively. Pulling cards from their sockets can help isolate an overloaded condition. The power supply is short-circuit protected on the regulated voltages. A short circuit on +24 V should blow the fuse. Assuming the voltages are correct, Table 5-6 should help in isolating malfunctions.

5.10 PARTS REPLACEMENT

In most instances, assembly methods for parts replacement are obvious. Electronic parts are nearly all on plug-in modules. Items in the transport tape path may require machine realignment if replaced. If only one item in the transport tape path is replaced at a time, the complete alignment procedure may usually be avoided. Examples of transport parts replacement follow.

5.10.1 Supply Tension Arm Roller Guide

If an alignment tool is available, follow the procedure given in tape path alignment (Paragraph 5.7). If not available, the following procedure will generally suffice.

1. Loosen the roller guide split clamp screw (C) and remove the roller shaft from the tension arm. Do not loosen the adjustment lockscrew (A).

2. Insert a new roller guide shaft and clamp lightly by tightening the split clamp screw (C).

3. The shaft end is threaded to allow use of a nut for fine adjustment. The thread does not enter the clamp area. Place several No. 10 flat washers over the threaded end and install a 10-32 nut as shown in Figure 5-3.

4. Push the shaft so that the roller is too far forward. Tighten the nut up lightly.

5. Load tape on the transport and feed it forward.

6. Tighten the nut pulling the shaft back in the clamp until the tape runs just inside the outer guide surface with the spring-loaded side manually pushed in.

7. Tighten the split clamp screw.

8. Remove the adjusting nut and washers.

Table 5-5
High Error Rate Troubleshooting

Symptom	Possible Cause	Indication	Action	Reference
Continuous errors, every block (read mode).	Broken connection to interface or internally.	Continuity.	Correct connection.	
	Bad preamplifier channel.	No output at test point on write test.	Replace preamplifier.	
	Bad quad read amplifier channel.	No data at test point.	Replace quad read amplifier.	
	Tape speed grossly wrong.	Visual or skew master.	Adjust speed.	5.6.3.1
	Bad head channel.	No output at preamplifier test point on write test.	Replace head.	5.10.7
Continuous errors, write mode only.	Broken connection on write data or WDS lines.	Continuity.	Correct connection.	
	Bad write amplifier channel.	Wrong or no signal at write amplifier test point in write test mode.	Replace write amplifier.	
Frequent write errors, few or no read errors.	Write-read crosstalk.	Noisy signal at preamplifier test point.	Check preamplifier gain. Check face shield spacing.	5.6.3.4 5.8
Frequent CRC and LRC errors, no VRC errors.	Wrong CRC generation in interface.	Wrong data at input.	Correct interface.	
Read or write errors only at start of block.	Ramp time wrong.	Read signals appear before ramp is complete.	Adjust ramp time.	5.6.3.2
Read errors on long blocks only.	Tape path misaligned.	Tape bears heavily on one guide surface.	Mechanical alignment.	5.7
Pattern related errors.	Write-read crosstalk.	Noisy signal at preamplifier test point.	Check preamplifier gain. Check face shield spacing.	5.6.3.4

Table 5-6
Control Malfunctions Troubleshooting

Symptom	Possible Cause	Location	Action	Reference
LOAD pushbutton activates servos when pressed but does not hold.	Broken tape signal clears load flip-flop.			
	Sensor amplifier driver module	Card cage	Replace module.	
	Pushbutton control module	Card cage	Replace module.	
	Photosensor (BKN) malfunction	Deck	Replace sensor.	5.10.8
After load, tape runs and does not stop.	Tape feeds forward after load point marker is sensed.			
	Marker strip missing from tape.	Tape	Apply reflective strip.	
	Misadjustment of photosensor on sensor amplifier driver module.	Card cage	Adjust photosensor.	5.5.1
No EOT signal.	Same as load point above but for EOT.			5.5.1
REWIND pushbutton inoperative.	Logic malfunction, pushbutton control module.	Card cage	Replace module.	
Rewind does not stop at LP but continues until tape is wound off reel.	Same as above.			
	Photosensor adjustment wrong on sensor amplifier driver module.	Card cage	Adjust photosensor	5.5.1
Reels rotate uncontrolled when power is turned on	Servo preamplifier malfunction.	Card cage	Remove preamplifier. If reels stop, replace preamplifier module.	
	Servo power amplifier (bad power transistors).	Heat sink	Replace heat sink assembly or locate and replace bad power transistors.	
Arms badly off center of arc at rest.	Magpot adjustment.	Deck	Adjust magpot setting.	5.5.2

Table 5-6 (Cont)
Control Malfunctions Troubleshooting

Symptom	Possible Cause	Location	Action	Reference
Arms bottom when starting or stopping. Weak reel torque, otherwise normal.	Servo preamplifier malfunction. Magpot adjustment (spacing). Bad reel motor.	Card cage Deck Deck	Replace module. Check adjustment. Replace reel motor.	5.5.2
Tape moves erratically, slips on capstan.	Head face shield touching tape. Defective tension roller.	Deck Deck	Adjust face shield setting. Replace roller.	5.8 5.10.1
Capstan turns slowly when it should be stopped.	Capstan zero adjustment on servo preamplifier module.	Card cage	Adjust zero.	5.5.3

5.10.2 Takeup Roller Guide

The takeup roller guide is adjusted in the same way as the supply roller except for steps 5 and 6, which are:

5. Load tape and cause forward and reverse tape motion – about 1 ft each.

6. Tighten the adjusting nut until tape feeds to the center of the takeup reel. Then apply fine adjustment until tape moves only slightly or not at all on the capstan surface on reversal.

5.10.3 Tension Arm Replacement

Tension arms are replaced by removing roller guides and disassembling. Do not attempt to remove the pin holding the arm to its shaft; replacement assemblies are supplied pinned. Reassemble the arm mechanism.

It will be necessary, if tension arms are replaced, to perform the complete tape path alignment procedure (Paragraph 5.7).

5.10.4 Reel Motor or Belt Replacement

1. Unplug the motor and remove the motor and mounting plate.

2. Remove the motor from mounting plate. Replace with a new motor.

3. Hook the drive belt on the motor pulley and replace the screws holding the motor mounting plate to the deck assembly.

4. Hold tension against the belt and tighten the mounting screws.

5. Check belt tension by squeezing between thumb and forefinger. The belt should deflect about 1/4 in. If not, loosen the screws and move the motor.

6. Plug in the motor.

5.10.5 Capstan Motor Replacement

1. Remove the capstan lockscrew.

2. Remove the capstan. The capstan fits a taper on the motor shaft so it may be readily removed once loosened. It may require considerable force to break loose, however. Pullers are available for this use but a screwdriver properly protected to prevent marring may be used to pry against the panel.

3. Remove the four capstan motor mounting screws. Unplug and remove the motor.

4. Install a new motor. Note if a red dot is present on the motor housing. If a dot is present, the motor should be oriented to place the dot as near as possible to the outside end of the deck.

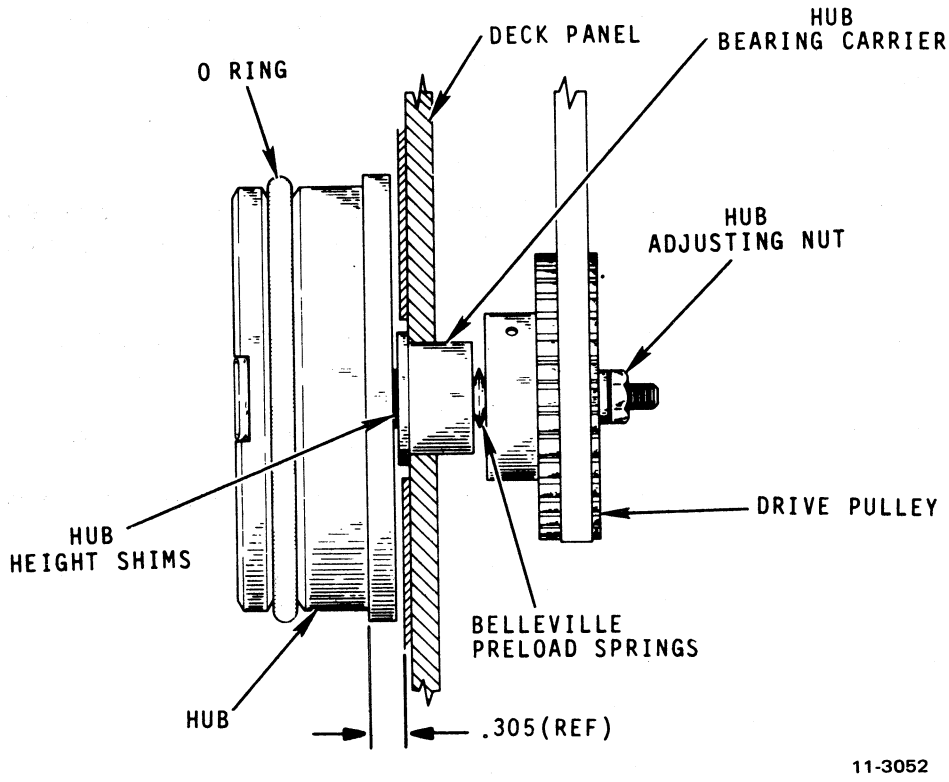
5. Adjust by procedure given under tape path alignment, Paragraph 5.7.

5.10.6 Supply Hub Replacement

After long use, components in the quick-locking mechanism may become worn to the point that adjustment of locking pressure cannot securely hold the tape reel. It is not necessary to replace the hub in its entirety; a hub repair kit is included.

Repair kits consist of a replacement lock lever, thrust washer, and O ring. (See Replaceable Parts List, Part III, Chapter 4.) To install:

1. Remove the lock adjusting nut.
2. Pull the lock lever out.
3. Remove the thrust washer.
4. Replace the thrust washer.
5. Install a new lock lever and replace the adjusting nut.
6. Install a new O ring.
7. Adjust the hub for proper holding force. Verify using several different reels. Refer to Figure 5-15 for more detailed adjustment procedures.



NOTES:
1. Loosen hub adjustment nut.
2. Open hub, install tape reel.
3. Close hub. Tighten hub adjusting nut until O ring presses firmly against reel.
4. Check for slippage under torque by holding hub or drive pulley. Reel should not slip on hub.
5. Open and close several times and recheck for slippage.
6. Try several reels, checking for slippage.

Figure 5-15 Reel Hub Adjustment

5.10.7 Magnetic Head Replacement

Replacement heads are supplied as complete assemblies together with mounting plate and face shield. A write deskewing chart is supplied with each head.

1. Unplug the head connectors.
2. Remove the head mounting screw and remove the head, passing connectors through the panel hole provided.
3. Be sure the adjusting screw on the replacement head is almost completely unscrewed.
4. Mount a new head with the mounting screw fairly loose. Screw in adjusting screw until point protrudes enough to engage its conical locating hole. Tighten the mounting screw.
5. Plug in the head.
6. Deskew the read head as described in the deskew adjustment procedure (Paragraph 5.6.3.5).
7. Set the deskewing switches on the write amplifiers to correspond to the chart supplied.
8. Place the chart over the old chart to record switch settings.

5.10.8 Photosensor Replacement

1. Remove the photosensor assembly by unplugging and removing the mounting screws. Since it will not pass through the hole provided, the connector must be removed by cutting the cable. Retain the connector.
2. Replacement sensors are provided with connector pins crimped to wires but with no connector shell installed.
3. Replace the assembly, passing the wires through the hole provided. Replace the screws.
4. Snap pins into the connector shell in the same color sequence as in the shell just removed; plug in the assembly.
5. Adjust as described in adjustment procedure.

5.10.9 Magpot Replacement (Figure 5-4)

1. Unplug the magpot assembly from its cable.
2. Remove the rotor by loosening the set screw.
3. Remove the screws holding the magpot PC board and remove the assembly.
4. Install a replacement unit.
5. Consult the magpot circuit description (Part III, Chapter 3) for realignment procedures.

5.10.10 Tape Cleaner Replacement

1. Remove the circular snap-in plug cover.
2. Remove the mounting screw and tape cleaner.
3. Mount a new cleaner assembly with the mounting screw finger-tight.
4. Adjust the cleaner surface so that it just touches the tape and is parallel to the tape surface.
5. Tighten the mounting screw and install a snap-in plug cover.

APPENDIX A
TMA11 INSTRUCTION TEST
(MAINDEC-11-DZTMA-E)

ABSTRACT

THE TM11 INSTRUCTION TEST CONTAINS A SERIES OF BASIC TESTS THAT CHECK TM11 REGISTERS FOR PROPER OPERATION WHILE NOT INVOLVING TAPE MOTION, ALL TAPE MOTION FUNCTIONS, DATA TRANSFERS, EXTENDED MEMORY, AND MANUAL INTERVENTION TESTS OF THE TU10 TRANSPORT SWITCHES.

2, REQUIREMENTS

2,1 EQUIPMENT

PDP-11 WITH TM11 CONTROL UNIT AND 1 TU10 TAPE UNIT,

2,2 STORAGE

2,2,1 PROGRAM STORAGE

THE ROUTINE REQUIRES 4K OF MEMORY,

3, LOADING PROCEDURE

3,1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED,

1, ABSOLUTE LOADER MUST BE IN MEMORY,
2, PLACE BINARY TAPE IN READER,
3, LOAD ADDRESS #7500 (* DETERMINED BY LOCATION OF LOADER)
4, PRESS "START" (PROGRAM WILL LOAD),

4, STARTING PROCEDURE

4,1 CONTROL SWITCH SETTINGS

STARTING AT SA 200 ALL SWITCHES SHOULD BE DOWN OR ZERO,

4,2 STARTING ADDRESS

200

4,3 PROGRAM AND/OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY,
PLACE ONE TU10 TAPE UNIT, ON-LINE, AT LOAD POINT (BOT), UNIT 0 SELECT
SET SWITCH REGISTER TO STARTING ADDRESS,
LOAD ADDRESS,
PRESS START,
PROGRAM WILL TYPE "SET SW0=1 IF 7 CHANNEL",
IF APPROPRIATE SET SW0 AND THEN PRESS CONTINUE,
THE PROGRAM WILL BEGIN TESTING,

5, OPERATING PROCEDURE

5,1 OPERATIONAL SWITCH SETTINGS

5,1,1 WITH ALL SWITCHES DOWN THE PROGRAM WILL PRINT OUT ON ERRORS AND CONTINUE IN TEST, (BELL WILL RING AT COMPLETION OF A PASS),

5,1,2 SWITCH SETTINGS ARE:

```
SW15 = 1 OR UP ,., HALT ON ERROR
SW14 = 1 OR UP ,., SCOPE LOOP
SW13 = 1 OR UP ,., INHIBIT PRINTOUT,
SW12 = 1 OR UP ,., INHIBIT SUB-TEST INTERATION,
SW10 = 1 OR UP ,., INHIBIT MANUAL INTERVENTION TEST
SW0  = 1 OR UP ,., TEST 7 CHANNEL TAPE UNIT,
```

5,1,3 MANUAL INTERVENTION TEST

THIS TEST WILL REQUIRE THE OPERATOR TO PERFORM CERTAIN OPERATIONS WITH THE TU10 TRANSPORT AS DIRECTED BY MESSAGES PRINTED ON THE TELETYPE,

5,2 SUBROUTINE ABSTRACTS

5,2,1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUB-TEST IN THE INSTRUCTION SECTION, IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT I' BEING ENTERED, IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUB-TEST THAT THE SCOPE LOOP IS REQUESTING,

5,2,2 HLT

THIS SUBROUTINE CALL PRINTS THE ADDRESS THAT TAGS THE FAILING SUBTEST AND THE CONTENTS OF ALL THE TM11 REGISTERS,

6.0 ERRORS

6.1 ERROR PRINTOUT FORMAT

WITH SW13=0 (OR DOWN) THE FOLLOWING PRINTOUT WILL APPEAR ON AN ERROR:

PC	STATUS	COMAND	BYTE	CA	DATA B	READ L	TEMP	CRC CAL
XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

PC	=	ADDRESS OF TEST WHERE ERROR OCCURED
STATUS	=	CONTENTS OF STATUS REGISTER AT TIME OF ERROR
COMAND	=	CONTENTS OF COMMAND REGISTER AT TIME OF ERROR
BYTE	=	CONTENTS OF BYTE COUNTER AT TIME OF ERROR
CA	=	CONTENTS OF CURRENT MEMORY ADDRESS AT TIME OF ERROR
DATA B	=	CONTENTS OF DATA BUFFER AT TIME OF ERROR
READ L	=	CONTENTS OF READ LINES AT TIME OF ERROR
TEMP	=	CONTENTS OF ADDRESS "TEMP" USED BY SOME TESTS
CRC CAL	=	CRC CHARACTER CALCULATED (USEFUL ONLY FOR CRC TEST)

NOTE THAT NOT ALL OF THE INFORMATION PRINTED IS INTENDED TO BE USEFUL FOR EVERY TYPE OF ERROR. THIS IS SIMPLY A STANDARD ERROR REPORT FOR ALL ERRORS. THE OPERATOR MUST REFER TO THE PROGRAM LISTING AT THE ADDRESS OF THE ERROR FOR A DESCRIPTION OF THE CAUSE OF THE ERROR. IT IS THEN UP TO HIM TO DETERMINE WHICH OF THE INFORMATION IS USEFUL.

6.2 ERROR RECOVERY

WITH SW15=1 OR UP THE PROGRAM WILL HALT ON AN ERROR. DEPRESS CONTINUE SWITCH TO RESTART TEST.

7, RESTRICTIONS

7,1 STARTING RESTRICTION

BEFORE STARTING PROGRAM THE OPERATOR MUST MAKE CERTAIN THAT THE TU10 TRANSPORT HAS DRIVE 0 SELECTED, IS "ON-LINE", AND AT "LOAD POINT".

7,2 OPERATIONAL RESTRICTIONS

MANUAL INTERVENTION TEST MUST BE PERFORMED ON EACH PASS THRU THE PROGRAM UNLESS INHIBITED WITH SW10=1 (OR UP).

8,0 MISCELLANEOUS

8,1 EXECUTION TIME

WITH MANUAL INTERVENTION TEST INHIBITED IT TAKES 1 MINUTE FOR ONE PASS THRU PROGRAM, MANUAL INTERVENTION TEST IS OPERATOR DEPENDENT BUT SHOULD TAKE APPROXIMATELY 2 MINUTES.

9,0 PROGRAM DESCRIPTION

10,0 LISTING

APPENDIX B
TS03 SUPPLEMENTAL INSTRUCTION TEST (MAINDEC-11-DZTSF-A)

1. ABSTRACT

THIS PROGRAM IS INTENDED TO BE USED IN ADDITION TO THE TM11/TU10 INSTRUCTION TEST (MAINDEC-11-DZTMA-C) TO COMPLETE TESTING OF THE TS03 MAGTAPE SYSTEM. THE PROGRAM CONSISTS OF ONLY FOUR (4) TESTS WHICH CHECK THE TMA-11 FEATURES OF DATA TRANSFER AT ODD BYTE STARTING ADDRESS AND OPERATION INCOMPLETE TIME OUT.

2. REQUIREMENTS

A. ANY PDP-11 PROCESSOR
B. 4K OF CORE
C. CONSOLE TTY
D. TMA-11 TAPE CONTROLLER
E. 1 OR 2 TAPE TRANSPORTS

3. LOADING PROCEDURE

USE STANDARD PROCEDURE FOR LOADING BINARY PAPER TAPE

4. STARTING PROCEDURE

THERE ARE TWO (2) STARTING ADDRESSES THAT MAY BE USED; 200(8) AND 210(8).

A. 200(8): STARTING AT THIS ADDRESS WILL CAUSE A PROGRAM IDENTIFICATION HEADER TO BE PRINTED, A REQUEST FOR UNIBUS ADDRESS AND VECTOR AND A REQUEST FOR ENTRY OF THE UNIT NUMBER (TAPE TRANSPORT SELECT). THE DEFAULT SELECTION OF UNIT ZERO (0) IS DISPLAYED, AND MAY BE CHANGED TO ANY NUMBER (0-7) OR UNCHANGED BY TYPING THE DESIRED NUMBER OR A CARRIAGE RETURN. IF THE SELECTED UNIT IS NOT AVAILABLE, A MESSAGE WILL BE PRINTED SO STATING, AND THE UNIT SELECT REQUEST REPEATED.

B. 210(8): STARTING AT THIS ADDRESS WILL NOT PRINT THE HEADER OR THE UNIT SELECT REQUEST AND IS INTENDED AS A RESTART ADDRESS ONLY.

5. CONSOLE SWITCH SETTING

ALL SWITCHES EXCEPT 3-9 ARE USED AND THE NORMAL, OR DEFAULT, RUN IS DONE WITH ALL SWITCHES SET TO ZERO (Ø).
ALL SWITCHES ARE DYNAMIC AND MAY BE CHANGED AT ANY TIME.

```
SW15:   1=HALT ON ERROR
        Ø=CONTINUE
SW14:   1=LOOP ON ERROR (SCOPE)
        Ø=CONTINUE
SW13:   1=INHIBIT ERROR TIME OUT
        Ø=PRINT ALL ERRORS
SW12:   1=INHIBIT ITERATION
        Ø=ITERATE EACH TEST ITS ASSIGNED AMOUNT
SW11:   1=CONTINUOUS CYCLE
        Ø=HALT AT END OF PASS
SW1Ø:   1=HALT AT END OF CURRENT TEST
        Ø=CONTINUE
SW9-3:  NOT USED
SW2-Ø:  SELECT INDIVIDUAL TEST (1-4)** ØØ = DO ALL TESTS
```

6. ERROR PRINTOUTS

THERE ARE THREE (3) TYPES OF ERROR PRINTOUTS WHICH MAY APPEAR: STATUS ERROR, DATA ERROR, POSITION ERROR.

A. STATUS ERROR: ANY READ, WRITE, OR SPACE OPERATION WHICH RESULTS IN SOME BAD STATUS (BIT 15 OF MTC), OR UNEXPECTED BUS ADDRESS, OR INCORRECT BYTE COUNT, WILL BE PRINTED.

B. DATA ERROR: ANY READ OPERATION WHICH RESULTS IN UNEXPECTED DATA WILL BE PRINTED.

C. POSITION ERROR: ANY SPACE OR REWIND OPERATION RESULTING IN UNEXPECTED STATUS WILL BE PRINTED.

EXAMPLES***

1. THE FOLLOWING EXAMPLE SHOWS A TYPICAL STATUS ERROR,

```
TEST1: WRITE FROM ODD BYTE
WRITE ERROR                 THIS PRINT SHOWS THAT WHILE EXECUTING
MTS: 1Ø1Ø1                  TEST 1 ON UNIT 2 AT 8ØØ BPI, A WRITE
MTC: 161204                 PARITY ERROR OCCURED.  THE BYTE COUNT
MTBC: Ø                     IS ZERO AS IT SHOULD BE AND THE CURRENT
MTCA: 6ØØ3 6ØØ3             ADDRESS IS AS EXPECTED.
```

2. THE FOLLOWING EXAMPLE SHOWS A TYPICAL DATA ERROR.

```
TEST 2: READ TO ODD BYTE
DATA ERROR                  THIS PRINT SHOWS THAT A SINGLE BIT WAS
CN: 0                       PICKED UP IN BOTH CHARACTER NUMBER ZERO
G: 00000000                 (0) AND CHARACTER NUMBER THREE (3).
B: 01000000
CN: 3
G: 00000011
B: 01000011
```

3. THE FOLLOWING EXAMPLE SHOWS AN ERROR DURING A REWIND OPERATION.

```
TEST4: OPI TOO LONG
REWIND ERROR: NO BOT
```

7. OPERATION

THE PROCEDURES FOR OPERATING THIS PROGRAM ARE QUITE SIMPLE AND REQUIRE ONLY A FEW STEPS:

1. LOAD ADDRESS 200 OR 210
2. SET SWICHES FOR DESIRED TEST SEQUENCE
3. PRESS START

ALL CONSOLE SWITCHES ARE DYNAMIC AND MAY BE CHANGED AT ANY TIME. THE NORMAL OPERATING SEQUENCE IS ALL SWITCHES DOWN (0). THE PROGRAM WILL TAKE APPROXIMATELY 1.25 MINUTES TO RUN; HOWEVER, IF ITERATIONS ARE INHIBITED (SW11=1), THE PROGRAM WILL RUN IN ABOUT .75 MINUTES. THE END OF PASS IS NOTED BY A PRINTOUT STATING END OF PASS AND THE NUMBER OF THAT PASS.

SINGLE TEST SELECTION: (SW0-SW3)

WHEN SW0-3 ARE SET TO ZERO (0), THE SCHEDULAR WILL EXECUTE ALL TESTS (1-4) IN SEQUENCE AS A SINGLE PASS, IF SW0-3 ARE SET TO SOME NUMBER BETWEEN 1 AND 4, THEN THAT PARTICULAR TEST WILL BE EXECUTED CONTINUOUSLY. THE PROGRAM MAY BE STOPPED AT THE END OF THE CURRENT TEST (EITHER IN SEQUENCE OR SINGLE TEST MODE) BY SETTING SWITCH TEN (SW10) TO A ONE (1). YOU MAY SELECT TEST NUMBERS IN ANY ORDER (UP OR DOWN) BECAUSE EACH TEST IS SELF CONTAINED.

8. TEST DESCRIPTION

TEST1: WRITE FROM ODD BYTE

THE PURROSE OF THIS TEST IS TO ASSURE THAT DATA MAY BE TRANSFERRED FROM MEMORY TO TAPE STARTING FROM AN ODD BYTE ADDRESS. THE TEST WILL WRITE A SIX (6) BYTE RECORD FROM AN ODD ADDRESS (WDATA+1) AND READ THAT RECORD BACK INTO AN EVEN ADDRESS (RDATA). NO STATUS ERROR SHOULD OCCUR, AND THE READ DATA SHOULD BE POSITIONED PROPERLY. THE RECORD IS SIX BYES LONG, EACH BYTE IS ITS NUMBER (Ø,1,2,3,4,5)

TEST2: READ TO ODD BYTE

THE PURPOSE OF THIS TEST IS TO ASSURE THAT DATA MAY BE TRANSFERRED FROM TAPE TO MEMORY STARTING AT AN ODD BYTE ADDRESS. THE PROCEDURE IS THE SAME AS IN TEST ONE (1), EXCEPT THAT THE WRITE IS FROM AN EVEN ADDRESS (WDATA) AND THE READ IS TO AN ODD ADDRESS (RDATA+1).

TEST3: OPI TOO LONG (OPI = BIT 8 OF MTS)

THE PURROSE OF THIS TEST IS TO ASSURE THAT THE OPI TIMER WILL SHUTDOWN THE DRIVE BEFORE TEN POINT FIVE FEET OF BLANK TAPE IS PASSED. THE PROCEDURE IS TO PERFORM A WRITE WITH IRG, BACKSPACE, WRITE WITH IRG 32(1Ø) TIMES IN ORDER TO ERASE 1Ø.5 FEET OF TAPE. AFTER REWIND, ISSUE A READ COMMAND AND OPI SHOULD TIME OUT BEFORE THE FIRST RECORD (1Ø,5 FEET DOWN TAPE) IS FOUND. THE NOMINAL VALUE FOR OPI IS SEVEN SECONDS (7SEC) OR ABOUT SEVEN POINT FIVE FEET (7,5 FT) OF TAPE. TEN POINT FIVE FEET OF TAPE REFLECTS THE MAXIMUM TOLERANCE FOR OPI.

TEST4: OPI TOO SHORT (OPI = BIT 8 OF MTS)

THE PURROSE OF THIS TEST IS TO ASSURE THAT THE OPI TIMER WILL NOT SHUTDOWN THE DRIVE BEFORE FOUR FEET (4 FT) OF BLANK TAPE IS PASSED. THE PROCEDURE IS THE SAME AS IN TEST THREE (3), HOWEVER OPI IS NOT EXPECTED BEFORE THE FIRST RECORD IS FOUND (4 FEET DOWN TAPE). THE FOUR FEET OF TAPE RELECTS THE MINIMUM TOLERANCE FOR OPI.

APPENDIX C
TS03 DRIVE FUNCTION TIMER
(MAINDEC-11-DZTSE-A)

1. ABSTRACT

THE TSØ3 DRIVE FUNCTION TIMER ASSISTS IN THE TESTING OF THE TMA-11 CONTROL UNIT AND TSØ3 TAPE UNIT. SELECTED OPERATIONS ARE EXECUTED, TIMED, AND THE TIMES ARE THEN PRINTED (IN MILLISECONDS). THERE IS NO LIMIT OR ERROR TESTING FACILITIES IN THE PROGRAM, THE DECISION ON THE VALIDITY OF TIMES MEASURED MUST BE MADE BY THE OPERATOR, EITHER 1 OR 2 TSØ3 UNITS MAY BE SELECTED.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11 WITH TMA-11 CONTROL UNIT AND 1 OR 2 TSØ3 TAPE UNITS.

2.2 STORAGE

2.2.1 PROGRAM STORAGE

THE PROGRAM REQUIRES 4K OF MEMORY.

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED

1. ABSOLUTE LOADER MUST BE IN MEMORY.
2. PLACE BINARY TAPE IN READER.
3. LOAD ADDRESS #75ØØ (# DETERMINED BY LOCATION OF LOADER).
4. PRESS "START" (PROGRAM WILL LOAD).

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS: NONE

4.2 STARTING ADDRESS

2ØØ

4.3 PROGRAM AND/OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY.
SET DESIRED TSØ3 TAPE UNITS ON-LINE.
SET SWITCH REGISTER TO STARTING ADDRESS.
LOAD ADDRESS.
PRESS START.
ENTER STARTING REGISTER ADDRESS.
THE PROGRAM WILL AUTOMATICLY FIND THE AVAILABLE
TSØ3 TAPE UNITS TO BE TESTED.
THE PROGRAM WILL BEGIN TIMING FUNCTIONS.
ON COMPLETION OF ALL TESTS "END OF TIMING" WILL BE PRINTED AND
THE PROCESSOR WILL HALT.
TO REPEAT TEST; PRESS CONTINUE.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

NONE

6. ERRORS

THE PROGRAM HAS NO INTERNAL ERROR DETECTION FACILITIES AND,
THEREFORE, NO ACTUAL ERROR TYPEOUTS. THE VALIDITY OF THE
TIMES MEASURED MUST BE DETERMINED BY THE OPERATOR.

6.1 TIME RELATIONSHIPS

A. "READ SHUTDOWN" MUST BE < "WRITE SHUTDOWN".
B. GAPS MUST = 8>7>6>5>4>3, 3=2=1 (+OR- 5.Ø).
C. "WRITE EOF" SHOULD BE SLIGHTLY > "WRITE XIRG".

6.2 TIME LIMITS AND PRINTOUT FORMAT EXAMPLE
*****(ALL TIMES ARE IN MILLISECONDS)*****

FUNCTION	UNIT Ø	UNIT 1	RANGE MAX - MIN
WRITE FROM BOT	565.Ø	SAME	593.Ø - 537,Ø
WRITE SHUTDOWN	15,6	"	17,6 - 13,6
WRITE START	35,8	"	37,5 - 33,9
SETTLE DOWN DELAY	33,Ø	"	33,6 - 30,4
WRITE TO ERASE HEAD	69,Ø	"	74,Ø - 6Ø,Ø
BACKSPACE SHUTDOWN	7,Ø	"	7,2 - 6,4
READ SHUTDOWN	7,Ø	"	7,2 - 6,4
GAPS SHOULD=8>7>6>5>4>3,	3=2=1	(+OR- 5,Ø)	
GAP 1	5Ø,Ø	"	
GAP 2	5Ø,Ø	"	
GAP 3	5Ø,2	"	
GAP 4	53,6	"	
GAP 5	67,1	"	
GAP 6	9Ø,4	"	
GAP 7	1Ø3,7	"	
GAP 8	117,4	"	
WRITE START	35,9	"	37,5 - 33,9
WRITE XIRG	333,1	"	349,8 - 315,8
READ FROM BOT	235,Ø	"	24Ø,4 - 22Ø,4
WRITE EOF	385,Ø	"	4ØØ,Ø - 36Ø,Ø
EOR TO EOF S TIME	36Ø,Ø	"	368,Ø - 328,Ø
SPACE SHUTDOWN	6,9	"	7,2 - 6,4
ONE INCH DATA TIME	81,Ø	"	83,9 - 75,9

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

AT LEAST ONE TSØ3 TAPE UNIT MUST BE "ON-LINE".
ALSO MAKE CERTAIN THAT EACH TSØ3 THAT IS "ON-LINE"
HAS A UNIQUE UNIT NUMBER SELECTED.

7.2 OPERATING RESTRICTIONS

TMA-11 INSTRUCTION TEST MUST RUN WITHOUT ERRORS BEFORE ATTEMPTING
TO OPERATE THIS PROGRAM.

8. MISCELLANEOUS

8.1 EXECUTION TIME

NOT APPLICABLE

9.Ø PROGRAM DESCRIPTION

9.1 WRITE FROM BOT DELAY

WRITE FROM BOT DELAY IS THE TIME NECESSARY TO MOVE THE BEGINNING
OF TAPE (BOT) MARKER APPROXIMATELY 6 INCHES PAST THE WRITE HEAD.
THE FIRST RECORD ON TAPE MUST BE WRITTEN AT LEAST 3 INCHES AWAY
FROM THE BOT MARKER.

PROCEDURE TO MEASURE TIME:

A. IF TSØ3 IS NOT AT BOT IT IS REWOUND TO BOT.
B. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
C. ISSUE WRITE FUNCTION, 8ØØ BPI, SET "GO".
D. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN 2ND BYTE IS OUTPUT.
E. THE TIME FROM "GO" UNTIL 2ND BYTE IS OUTPUT IS APPROXIMATELY EQUAL TO "WRITE FROM BOT DELAY".

9.2 WRITE SHUTDOWN

WRITE SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE
MOVING TAPE AFTER A RECORD IS WRITTEN SO THAT THE PROPER
INTERRECORD GAP WILL EXIST BETWEEN RECORDS.

PROCEDURE TO MEASURE TIME:

A. THE PROGRAM USES THE SAME RECORD THAT WAS WRITTEN TO TIME "WRITE FROM BOT DELAY".
B. AFTER THE LAST BYTE (BC=Ø), INDICATING THE END OF THE RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
C. THE TIME FROM "BC=Ø" UNTIL "SETTLEDOWN" IS "WRITE SHUTDOWN".

9.3 WRITE START

WRITE START IS THE TIME NECESSARY FOR TAPE TO ACCELERATE TO FULL SPEED AND GUARANTEE A 1/2 INCH INTERRECORD GAP.

PROCEDURE TO MEASURE TIME:

SAME AS "WRITE FROM BOT" EXCEPT NOW WE ARE NOT AT BOT.

A. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
B. ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
C. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN 2ND BYTE IS OUTPUT.
D. THE TIME FROM "GO" UNTIL 2ND BYTE IS OUTPUT IS APPROXIMATELY EQUAL TO "WRITE START".

9.4 SETTLEDOWN DELAY

TAPE DOES NOT ACTUALLY COME TO A COMPLETE STOP UNTIL SOME PERIOD OF TIME AFTER SHUTDOWN HAS ENDED. ALSO, AFTER TAPE HAS FULLY STOPPED, AN ADDITIONAL PERIOD OF TIME IS NECESSARY FOR THE TAPE AND HARDWARE TO "SETTLEDOWN" AND BECOME STABLE. THE "SETTLEDOWN DELAY" IS THE PERIOD OF TIME NECESSARY FOR THE TAPE AND MECHANICAL CHARACTERISTICS OF THE TS03 TO BECOME STABLE, SO THAT THE UNIT CANNOT BE OPERATED, START/STOP, AT A FREQUENCY WHERE IT IS MECHANICALLY RESONANT.

PROCEDURE TO MEASURE TIME:

A. THE PROGRAM USES THE SAME RECORD THAT WAS WRITTEN TO TIME "WRITE START"
B. AFTER "SETTLEDOWN" BECOMES A 1, INDICATING THE START OF SETTLEDOWN, MONITOR "TU READY" UNTIL IT BECOMES A 1.
C. THE TIME FROM "SETTLEDOWN" UNTIL "TU READY" IS "SETTLEDOWN".

9.5 WRITE TO ERASE HEAD

THE PURPOSE OF THE ERASE HEAD IS TO INSURE THAT THE TAPE IS IN THE SAME FLUX STATE AS THE WRITE HEADS. THIS IS NECESSARY FOR SEVERAL REASONS.

1. START/STOP CHARACTERISTICS VARY AMONG TAPE UNITS AND IT WOULD BE POSSIBLE TO LEAVE OLD DATA IN THE INTERRECORD GAPS WHEN USING A TAPE ON MORE THAN ONE UNIT.
2. A TAPE PREVIOUSLY USED AT ONE RECORDING DENSITY COULD NOT BE USED LATER AT ANOTHER DENSITY.
3. TRACK ALIGNMENT AND HEAD WIDTH VARY FROM TAPE UNIT TO TAPE UNIT AND IT WOULD BE POSSIBLE FOR DATA TO BE LEFT ON THE TRACK EDGES FROM OLD RECORDS.

THE "WRITE TO ERASE HEAD" TEST INSURES THAT THE TAPE IN FRONT OF THE WRITE HEAD IS ERASED DURING A WRITE OPERATION.

PROCEDURE TO MEASURE TIME:

A. A LONG RECORD HAS BEEN WRITTEN FROM BOT, SAME RECORD THAT WAS USED TO TIME "WRITE FROM BOT DELAY".
B. TAPE IS REWOUND TO BOT.
C. BYTE RECORD COUNTER IS INITIALIZED FOR A 3 BYTE RECORD AND CURRENT MEMORY ADDRESS REGISTER IS INITIALIZED.
D. ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
E. AWAIT CUR AT END OF CURRENT WRITE.
F. ISSUE A 2 BYTE READ.
G. TIME FROM GO UNTIL CUR OF THE READ IS WRITE TO ERASE HEAD TIME.
H. IF TIME IS TOO SHORT, ERASE HEAD IS INOPERATIVE.

9.6 BACKSPACE SHUTDOWN

"BACKSPACE SHUTDOWN" IS THE LENGTH OF TIME NECESSARY TO GUARANTEE THAT IF A WRITE OPERATION FOLLOWS A BACKSPACE THE TAPE WILL BE POSITIONED SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE WRITE AND ERASE HEADS AND WILL BE ERASED. "BACKSPACE SHUTDOWN" MUST BE LESS THAN "WRITE START" SO THAT INTERRECORD GAPS WILL INCREASE IF A BACKSPACE/REWRITE OPERATION IS INITIATED.

PROCEDURE TO MEASURE TIME:

A. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
B. ISSUE WRITE EOF FUNCTION, 800 BPI, SET "GO"
C. AFTER EOF RECORD IS WRITTEN WAIT FOR "TU READY".
D. SET BYTE RECORD COUNTER TO BACKSPACE 1 RECORD.
E. ISSUE BACKSRACE FUNCTION, SET "GO".
F. AFTER "EOF" BECOMES A 1, INDICATING THE RECOGNITION OF THE "EOF" RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
G. THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "BACKSPACE SHUTDOWN".

9.7 READ SHUTDOWN

READ SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE MOVING TAPE AFTER A RECORD IS READ SO THAT THERE IS ENOUGH GAP FOR TAPE TO BE FULLY ACCELERATED IF A READ IS FOLLOWED BY A BACKSPACE. "READ SHUTDOWN" MUST ALSO BE LESS THAN "WRITE SHUTDOWN" TO GUARANTEE THAT THE WRITE AND ERASE HEADS WILL BE POSITIONED SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE HEADS AND WILL BE ERASED IF A WRITE FOLLOWS A READ. IN ADDITION, WHEN A WRITE FOLLOWS A READ THE INTERRECORD GAP MUST STILL BE AT LEAST 1/2 OF AN INCH.

PROCEDURE TO MEASURE TIME:

A. RECORD PREVIOUSLY USED IN "BACKSPACE SHUTDOWN" IS READ.
B. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER
C. ISSUE READ FUNCTION, 800 BPI, SET "GO".
D. AFTER "EOF" BECOMES A 1, INDICATING THE END OF THE RECORD, MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
E. THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "READ SHUTDOWN"

9.8 GAP CONSISTENCY

FOR PROPER OPERATION, THE INTERRECORD GAPS ON TAPE MUST ALWAYS BE AT LEAST 1/2 OF AN INCH. THIS WILL ALLOW DATA WRITTEN USING ONE TAPE UNIT TO BE READ ON ANOTHER TAPE UNIT WHEN THE START/STOP CHARACTERISTICS OF EACH UNIT ARE DIFFERENT. THE MINIMUM GAP SIZE OF 1/2 INCH IS GENERATED WHEN A WRITE FOLLOWS A READ. ALL OTHER GAPS SHOULD BE LARGER DEPENDING ON HOW THEY WERE WRITTEN.

PROCEDURE TO MEASURE TIME:

A. A TOTAL OF NINE RECORDS ARE WRITTEN ON TAPE (FROM BOT) UTILIZING DIFFERENT SEQUENCES TO GENERATE THE INTERRECORD GAPS.
B. THE TAPE IS REWOUND TO BOT.
C. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
D. ISSUE READ FUNCTION, 800 BPI, SET "GO".
E. WAIT FOR "CU READY" TO BECOME A 1, THEN REPEAT STEP C AND RESET "GO" TO CONTINUE.
F. MONITOR CURRENT MEMORY ADDRESS TO DETERMINE WHEN 2ND BYTE IS INPUT.
G. THE TIME FROM WHEN "GO" IS RESET UNTIL THE 2ND BYTE IS INPUT WILL REFLECT THE SIZE OF THE GAP.
H. STEPS E, F ARE REPEATED UNTIL ALL 8 GAPS ARE MEASURED.

PROGRAM SEQUENCE FOR EACH GAP:

GAP 1 — WRITE FOLLOWED BY A WRITE (START/STOP).

GAP 2 — WRITE FOLLOWED BY A WRITE (START/STOP).

GAP 3 — READ FOLLOWED BY A WRITE (START/STOP).

GAP 4 — WRITE-BACKSPACE FOLLOWED BY A WRITE (START/STOP).

GAP 5 — SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 2 TIMES.

GAP 6 — SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 3 TIMES.

GAP 7 — SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 4 TIMES.

GAP 8 — SAME AS GAP 4 EXCEPT WRITE-BACKSPACE REPEATED 5 TIMES.

GAP LENGTHS SHOULD REFLECT THE FOLLOWING RELATIONSHIP:

8>7>6>5>4>3, 3=2=1 (+OR- 5,0).

9.9 WRITE START

THIS IS A REPEAT OF THE "WRITE START" TEST PREVIOUSLY COMPLETED (REFERENCE 9.3). IT'S PURPOSE IS TO DETERMINE IF TAPE WILL DRIFT BACKWARDS TO BOT IF A "POWER CLEAR" IS ISSUED AS SOON AS BOT DISAPPEARS WHEN MOVING FORWARD FROM BOT. TIME SHOULD EQUAL "WRITE START" AS MEASURED IN 9.3.

9.10 WRITE XIRG

WRITE WITH AN EXTENDED INTERRECORD GAP IS A FUNCTION THAT CAUSES THE GENERATION OF AN INTERRECORD GAP THAT IS AT LEAST 3 INCHS LONG AS COMPARED WITH THE NORMAL 3/4 INCH GAP. THE PURPOSE IS TO ELIMINATE WRITE ERRORS THAT MAY BE CAUSED BY A DEFECTIVE AREA ON TAPE. NORMALLY ONE REWRITE WITH XIRG WOULD BE SUFFICIENT TO MOVE PAST THE BAD SPOT, HOWEVER IF IT ISN'T, THE PROCEDURE WOULD BE TO REPEAT THE "BACKSPACE-REWRITE WITH XIRG" SEQUENCE UNTIL A RECORD IS WRITTEN WITHOUT ERRORS. EACH SUCCESSIVE REWRITE WOULD ADD 3 INCHES TO THE INTERRECORD GAP UNTIL "GOOD" TAPE WAS REACHED.

PROCEDURE TO MEASURE TIME:

A. TAPE IS NOT AT BOT
B. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
C. ISSUE WRITE WITH XIRG FUNCTION, 800 BPI, SET "GO",
D. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN 2ND BYTE IS OUTPUT,
E. THE TIME FROM "GO" UNIT 2ND BYTE IS OUTPUT IS "WRITE WITH XIRG".

9.11 READ FROM BOT

THE FIRST RECORD WRITTEN ON TAPE IS SUPPOSED TO BE AT LEAST 6 INCHES FROM THE BOT MARKER. IN THE EVENT THAT THIS CONDITION WASN'T MET IT IS STILL DESIREABLE TO READ THE RECORD. READ FROM BOT IS THE TIME FROM WHEN A READ FUNCTION IS ISSUED UNTIL THE 2ND BYTE IS INPUT.

PROCEDURE TO MEASURE TIME:

A. THE RECORD THAT WAS WRITTEN JUST OFF BOT DURING "WRITE START" (REFERENCE 9.10) IS USED.
B. TAPE IS REWOUND TO BOT
C. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
D. ISSUE READ FUNCTION, 800 BPI, SET "GO",
E. MONITOR CURRENT MEMORY ADDRESS REGISTER TO DETERMINE WHEN 2ND BYTE IS INPUT,
F. THE TIME FROM "GO" UNTIL 2ND BYTE IS INPUT IS "READ FROM BOT".

9.12 WRITE EOF.

TO WRITE AN END OF FILE MARK IT IS NECESSARY FOR TAPE TO MOVE 3 INCHES BEFORE WRITING. IN THAT RESPECT IT IS SIMILAR TO WRITING A RECORD WITH EXTENDED INTERRECORD GAP, HOWEVER, AN EOF MARK CORRESPONDS TO A 1 BYTE RECORD. THE TIME SHOULD BE SLIGHTLY LARGER THAN "WRITE XIRG".

PROCEDURE TO MEASURE TIME:

A. TAPE UNIT IS REWOUND TO BOT.
B. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS REGISTER.
C. ISSUE WRITE FUNCTION, 800 BPI, SET "GO".
D. WAIT FOR "CU READY" AND THEN "TU READY" TO BECOME A 1.
E. ISSUE WRITE EOF FUNCTION, 800 BPI, SET "GO".
F. WAIT FOR "CU READY" TO BECOME A 1.
G. THE TIME FROM "GO" UNTIL "CU READY" IS "WRITE EOF".

9.13 EOR TO EOF SPACE TIME

EOR TO EOF SPACE TIME IS THE TIME NEEDED TO MOVE TAPE FROM THE END OF A RECORD TO AN END OF FILE MARK WRITTEN AFTER IT. THE PROCEDURE USED TURNS OUT TO BE A TEST OF THE WRITE AND ERASE HEAD POLARITIES. IF THE TIME PRINTED IS EQUAL TO ZERO IT IS AN INDICATION THAT THE EOF WAS NOT FOUND WHEN "CU READY" BECAME A 1.

THIS COULD INDICATE ONE OR MORE OF THE FOLLOWING PROBLEMS:

1. ERASE HEAD POLARITY REVERSED.
2. ERASE HEAD CURRENT NOT SUFFICIENT TO FULLY SATURATE TAPE.
3. ONE OR MORE OF WRITE HEAD TRACKS POLARITY REVERSED.
4. ONE OR MORE SENSITIVE READ AMPLIFIERS.
5. WRITE EOF FUNCTION DIDN'T REALLY WRITE AN EOF MARK, OTHERWISE "EOR TO EOF SPACE TIME" SHOULD BE SLIGHTLY LARGER THAN "WRITE EOF".

PROCEDURE TO MEASURE TIME:

A. A RECORD AND EOF WAS PREVIOUSLY WRITTEN FROM BOT FOR "WRITE EOF" (REFERENCE 9.12).
B. TAPE IS REWOUND TO BOT.
C. REWRITE RECORD OVER PREVIOUSLY WRITTEN RECORD.
D. BACKSPACE OVER RECORD JUST WRITTEN.
E. SET BYTE RECORD COUNTER TO SPACE 2 RECORDS.
F. ISSUE SPACE FORWARD FUNCTION, SET "GO".
G. WAIT FOR BYTE RECORD COUNTER TO INDICATE THAT 1ST RECORD HAS BEEN SPACED OVER THEN MONITOR "CU READY" UNTIL IT BECOMES A 1. AFTER "CU READY" CHECK TO SEE IF "EOF" IS A 1 IN STATUS REGISTER. IF "EOF" NOT SET THEN ZERO TIME COUNTER.
H. TIME FROM BYTE RECORD COUNTER =-1 UNTIL "CU READY" IS "EOR TO EOF SPACE TIME".

9.14 SPACE SHUTDOWN

SPACE SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE MOVING TAPE AFTER A RECORD IS SPACED OVER IN THE FORWARD DIRECTION FOR THE SAME REASONS AS "READ SHUTDOWN" .

PROCEDURE TO MEASURE TIME:

A. SPACE FORWARD FUNCTION USED TO TIME "EOR TO EOF SPACE TIME" IS USED.
B. AFTER "EOF" BECOMES A 1, INDICATING THE END OF THE RECORD (EOF), MONITOR "SETTLEDOWN" UNTIL IT BECOMES A 1.
C. THE TIME FROM "EOF" UNTIL "SETTLEDOWN" IS "SPACE SHUTDOWN".

9.15 ONE INCH DATA TIME

ONE INCH OF DATA, 800 BPI IS WRITTEN AND TIMED TO DETERMINE IF TAPE IS MOVING AT PROPER SPEED.

PROCEDURE TO MEASURE TIME:

A. INITIALIZE BYTE RECORD COUNTER AND CURRENT MEMORY ADDRESS.

B. ISSUE WRITE FUNCTION, 800 BPI, SET "GO".

C. WAIT FOR CURRENT MEMORY ADDRESS REGISTER TO INDICATE 2ND BYTE IS OUTPUT AND THEN MONITOR BYTE RECORD COUNTER UNTIL EQUAL TO ZERO.

D. TIME FROM 2ND BYTE OUTPUT UNTIL BYTE RECORD COUNTER = 0 IS "ONE INCH DATA TIME"

10. STATUS AND COMMAND REGISTER BIT ASSIGNMENTS (TMA-11)

COMMAND REGISTER

15	ERROR		
14	DEN 8	00 = 200 BPI 7 TRACK	10 = 800 BPI 7 TRACK
13	DEN 5	01 = 556 BPI 7 TRACK	11 = 800 BPI 9 TRACK
12	POWER CLEAR		
11	PARITY	0 = ODD 1 = EVEN	
10	UNIT SEL. BIT 2		
9	UNIT SEL. BIT 1		
8	UNIT SEL. BIT 0		
7	CONTROL UNIT READY		
6	INTERRUPT ENABLE		
5	ADDRESS BIT 17		
4	ADDRESS BIT 16		
3	FUNCTION BIT 2	000 = OFF LINE	100 = SPACE FORWARD
		001 = READ	101 = SPACE REVERSE
2	FUNCTION BIT 1	010 = WRITE	110 = WRITE XIRG
1	FUNCTION BIT 0	011 = WRITE EOF	111 = REWIND
0	GO		

STATUS REGISTER

```
15      ILLEGAL COMMAND (ILC)

14      END OF FILE (EOF)
13      CYCLICAL REDUNDANCY ERROR (CRE)
12      PARITY ERROR (PAE)

11      BUS GRANT LATE (BGL)
10      END OF TAPE (EOT)
9       RECORD LENGTH ERROR (RLE)

8       BAD TAPE ERROR (BTE)
7       NON EXISTENT MEMORY (NXM)
6       SELECT REMOTE (SELR)

5       BEGINNING OF TAPE (BOT)
4       7 CHANNEL (7CH)
3       SETTLE DOWN (SDWN)

2       WRITE LOCK (WRL)
1       REWIND STATUS (RWS)
0       TAPE UNIT READY (TUR)
        .ENDR
```

APPENDIX D
TMA11 MULTIDRIVE DATA RELIABILITY EXERCISER (MAINDEC-11-DZTMH-A)

1. ABSTRACT

THIS PROGRAM IS DESIGNED TO BE USED BY AN EXPERIENCED ENGINEER /TECHNICIAN FOR EVALUATION AND DEBUGGING OF MAG TAPE DRIVES. THE PROGRAM IS CAPABLE OF EXERCISING ANY TAPE DRIVE THAT CAN BE OPERATED ON A UNIBUS PDP-11 SYSTEM THROUGH THE TMA-11 MAG TAPE CONTROLLER. ANY TYPE OF TAPE DRIVE; 7 OR 9 TRACK MAY BE USED. ANY NUMBER OF DRIVES, SINGLE OR MULTIDRIVE SYSTEMS, UP TO EIGHT (8), MAY BE TESTED BY A SINGLE EXECUTION OF THE PROGRAM. THIS FLEXIBILITY IS POSSIBLE BECAUSE THE PROGRAM HAS NO FIXED PARAMETERS OR TESTING SEQUENCE. THE ENTIRE TEST PLAN, INCLUDING PARAMETERS AND OPERATING SEQUENCE, IS DETERMINED BY THE OPERATOR THROUGH RESPONSES TO TELETYPE REQUESTS AND SETTING OF CONSOLE SWITCHES.

THE PROGRAM PROVIDES FOR TESTING OF ALL TAPE DRIVE FUNCTIONS SUCH AS WRITING,READING,REWINDING,TAPE POSITIONING,EOT - BOT SENSING AND ASSUMES A GOOD TMA-11 CONTROLLER.

HOWEVER; THE TMA-11 CONTROLLER IS TESTED SOMEWHAT INTRINSICALLY DURING THE TEST CYCLE IN ORDER TO PROVIDE FULL INFORMATION ABOUT ANY ERROR CONDITIONS DETECTED.

DURING A TEST CYCLE, CHECKS ARE MADE FOR STATUS ERRORS,DATA ERRORS, POSITION ERRORS,WORD COUNT AND CURRENT MEMORY ADDRESS ERRORS WHEREVER APPLICABLE.

2. REQUIREMENTS (HARDWARE)

A. ANY PDP-11 PROCESSER
B. 8K OF CORE
C. TELETYPE
D. TMA-11 TAPE CONTROLLER
E. 1 TO 8 MAG TAPE DRIVES

3. LOADING PROCEDURE

USE STANDARD PROCEDURE FOR LOADING BINARY TAPES

4. STARTING PROCEDURE

THERE ARE FOUR (4) STARTING ADDRESSES THAT MAY BE USED; 200(8), 204(8), 210(8), AND 240(8):

A. 200(8): THIS ADDRESS MUST BE USED ON INITIAL START FROM LOAD AS ALL PARAMETERS ARE ENTERED FROM HERE. REQUESTS ARE PRINTED ON THE TELETYPE FOR ENTRY OF TMA-11'S REGISTER STARTING ADDRESS, VECTOR ADDRESS, UNIT NUMBER, DENSITY,PARITY,RECORD COUNT,CHARACTER COUNT,PATTERN NUMBER, TAPE MARK (EOF) OPTION,AND STALL FOR READ, WRITE, AND TURNAROUND. ALL REPONSES SHOULD BE MADE IN OCTAL AND WITHIN THE LIMITS OF THE PARAMETER. A QUESTION MARK (?) WILL BE TYPED IF ANY CHARACTER ENTERED IS NOT BETWEEN 0 THRU 7 (OCTAL). THE CHARACTER MAY BE RETYPED FOLLOWING THE QUESTION MARK. IF THE RESPONSE IS NOT WITHIN ITS LIMITS, A QUESTION MARK (?) IS TYPED AND THE ENTIRE RESPONSE MAY BE RENTERED. SOME RESPONSES REQUIRE MORE THAN ONE (1) CHARACTER, BUT NONE REQUIRES MORE THAN SIX (6). RESPONSES NEED NOT HAVE LEADING ZEROS AND SHOULD BE TERMINATED BY A CARRIAGE RETURN IF LESS THAN THE MAXIMUM NUMBER OF CHARACTERS IS INPUT.

B. 204(8): THIS ADDRESS SHOULD BE USED ANYTIME A RESTART OF THE PROGRAM IS NECESSARY AND THE PARAMETERS ENTERED AT THE INITIAL START OF 200(8) NEED NOT BE CHANGED. ALSO NOTE THAT ANY DATA PATTERN WHICH HAD BEEN GENERATED BY SETTING THE RANDOM DATA SWITCH (CONSOLE SWITCH EIGHT) WILL NOT BE OVERWRITTEN AND THERFORE IS HELD IN CORE FOR USE UNTIL CONSOLE SWITCH EIGHT(8) IS AGAIN SET.

C. 210(8): THIS ADDRESS IS THE SAME AS USING 204(8) IN THAT THE PREVIOUSLY SET PARAMETERS ARE USED; HOWEVER, THE DATA PATTERN IS RETURNED TO THE FIXED PATTERN ORIGINALLY CALLED FOR AT THE 200(8) START. ALSO ALL STATISTICS PREVIOUSLY GATHERED WILL BE CLEARED.

D. 240(8): THIS IS A SPECIAL ADDRESS WHICH WILL CAUSE THE PROGRAM TO EXECUTE A PREDETERMINED TEST PLAN ON ALL AVAILABLE UNITS. THE ONLY INPUT REQUIRED BY THE OPERATOR IS A RESPONSE TO REQUESTS FOR THE TMA-11 ADDRESS, VECTOR ADDRESS, AND CONTINUOUS OPERATION OF THE SEQUENCE.

SEE ITEM 11, (PAGE 22) FOR FULL DETAILS.

THE FOLLOWING IS AN EXPLANATION OF THE INITIAL START (200 OCTAL) REQUESTS AND RESPONSES:

REGISTER START: THE RESPONSE REQUIRED FOR THIS REQUEST IS TO ENTER THE ADDRESS OF THE FIRST TMA-11 REGISTER (MTS) AS A SIX DIGIT UNIBUS ADDRESS.

VECTOR ADDRESS: THE RESPONSE FOR THIS REQUEST IS TO ENTER THE INTERRUPT VECTOR ADDRESS USED BY THE TMA-11 AS A THREE (3) DIGIT ADDRESS.

UNIT NUMBER: THE UNIT NUMBER IS ENTERED AS ONE (1) OCTAL CHARACTER AND MUST BE WITHIN THE LIMITS OF 0 THROUGH 7. WHEN THE UNIT NUMBER HAS BEEN ENTERED AND IS LEGAL, THE PROGRAM TESTS FOR THE PRESENCE OF A UNIT OF THAT NUMBER. IF THE UNIT IS AVAILABLE A PRINTOUT OF 7 CHANNEL OR 9 CHANNEL WILL BE MADE TO ASSIST THE OPERATOR IN SETTING DENSITY AND PARITY. IF THE UNIT IS NOT AVAILABLE, A MESSAGE STATING SO WILL BE PRINTED AND A NEW UNIT NUMBER REQUEST WILL BE ISSUED. WHEN A GOOD UNIT NUMBER HAS BEEN ENTERED, REQUESTS FOR OPERATING DENSITY AND PARITY ARE MADE FOR THAT UNIT AND SHOULD BE RESPONDED TO ACCORDING TO THAT PARTICULAR UNIT'S NEEDS. AS MANY AS EIGHT (8) UNIT NUMBER REQUESTS MAY BE USED, HOWEVER, AT LEAST ONE MUST BE USED. THE UNIT NUMBER AND THEIR RESPECTIVE DENSITY AND PARITY MAY BE ENTERED IN ANY ORDER. THE INFORMATION FOR EACH UNIT ENTERED IS LOADED INTO A TABLE FOR REFERENCE IN TESTING. IF LESS THAN EIGHT(8) UNITS ARE REQUIRED, THEN RESPONDING TO THE UNIT NUMBER REQUEST WITH A CARRIAGE RETURN WILL TERMINATE THE UNIT ENTRIES AND CONTINUE TO THE NEXT PARAMETER. IT SHOULD BE REMEMBERED THAT AT LEAST ONE UNIT NUMBER REQUEST MUST BE ENTERED. IF THE FIRST REQUEST IS RESPONDED TO BY A CARRIAGE RETURN, THEN THE REQUEST WILL BE REPEATED.

DENSITY: THE DENSITY REQUEST IS RESPONDED TO BY ONE (1) OCTAL CHARACTER AND MUST BE WITHIN THE LIMITS OF 0 THRU 3. AS EACH UNIT NUMBER IS ENTERED, A REQUEST FOR THE OPERATING DENSITY FOR THAT UNIT IS TYPED. THE RESPONSE MEANINGS ARE AS FOLLOWING:

A. 0 = 200BPI, 7 CHANNEL NRZ1
B. 1 = 556BPI, 7 CHANNEL NRZI
C. 2 = 800BPI, 7 CHANNEL NRZI
D. 3 = 800BPI, 9 CHANNEL NRZI

PARITY: THE PARITY REQUEST IS RESPONDED TO BY ONE (1) OCTAL CHARACTER AND MUST BE EITHER Ø OR 1.

A. 1 = EVEN PARITY
B. Ø = ODD PARITY

RECORD COUNT: THIS REQUEST IS RESPONDED TO BY A SIX (6) CHARACTER OCTAL NUMBER FROM 1 TO 177777. REMEMBER LEADING ZEROS ARE NOT REQUIRED AND IF LESS THAN SIX CHARACTERS ARE ENTERED, A CARRIAGE RETURN WILL TERMINATE THE RESPONSE. THE RECORD COUNT IS USED IN CONJUCTION WITH THE CHARACTER COUNT TO ESTABLISH A BLOCKING FACTOR FOR USE IN READ OR WRITE CYCLES.

CHARACTER COUNT: THIS RESPONSE IS ENTERED AS FOUR (4) OCTAL CHARACTERS WITHIN THE LIMITS OF 4 THRU 4000. AGAIN LEADING ZEROS ARE NOT REQUIRED AND A CARRIAGE RETURN TERMINATES A LESS THAN FOUR (4) CHARACTER RESPONSE. THE CHARACTER COUNT IN CONJUNCTION WITH THE RECORD COUNT IS USED TO ESTABLISH THE BLOCK SIZE (CHARACTERS PER RECORD, AND RECORDS PER BLOCK) USED IN READ AND WRITE CYCLES THE SAME BLOCKING IS USED ON ALL AVAILABLE UNITS.

PATTERN NUMBER: THIS RESPONSE IS A TWO (2) CHARACTER OCTAL NUMBER WITHIN THE LIMITS OF Ø THRU 20(8). THE NUMBER ENTERED WILL CAUSE A SPECIFIC DATA PATTERN TO BE USED FOR ALL READING AND WRITING. THIS DATA PATTERN IS NOT CHANGED UNLESS RANDOM DATA IS REQUESTED BY SETTING CONSOLE SWITCH EIGHT (8) TO A ONE. RESETTING OF THE RANDOM DATA SWITCH DOES NOT CAUSE REVERSION TO THE FIXED PATTERN, BUT WILL HOLD THE LAST GENERATED PATTERN UNTIL A RESTART IS DONE FROM LOCATION 210(8) OR 200(8). THE SELECTION OF DATA PATTERN ZERO (Ø) HAS A SPECIAL USE. PATTERN NUMBER ZERO (Ø) WILL CAUSE TO BE READ IN AT THE HIGH SPEED PAPER TAPE READER ANY DATA PATTERN DESIRED. THE EXTERNAL INPUT DATA THOUGH THE READER IS DONE BY PREPARING A PAPER TAPE WITH A PROGRAM CALLED DTC. (MAINDEC-11-DZTMA-A-D) ANY CONFIGURATION OF BITS AND CHARACTERS MAY BE USED AND A LIMIT OF 377(8) CHARATERS IS IMPOSED. WHEN EXTERNAL DATA IS INPUT, THE ENTIRE WRITE BUFFER IN CORE IS FILLED WITH THE PATTERN SO THAT ANY SIZE RECORD MAY BE USED. DATA PATTERN ZERO (Ø) EXTERNAL PAPER TAPE NEED ONLY BE READ ONCE AT INITIAL START OF 200(8), AND NEED NOT BE READ AGAIN UNLESS OVERWRITTEN BY RANDOM DATA. BE SURE TO LOAD THE READER BEFORE PRESSING START.

SEE ITEM 5, (PAGE 7) FOR A DESCRIPTION OF THE DATA PATTERNS.

TAPE MARK: THE TAPE MARK REQUEST IS USED TO DETERMINE IF THE OPERATOR WISHES TO HAVE EACH DATA BLOCK SEPARATED BY A TAPE MARK (OFTEN CALLED EOF FOR END OF FILE). IF RESPONDED TO BY A ONE(1) THE TAPE MARK WILL BE WRITTEN AND WHEN READING WILL BE EXPECTED AT THE END OF EACH DATA BLOCK. A ZERO(Ø) RESPONSE WILL DISALLOW THE TAPE MARK OPTION. PLEASE NOTE THAT THE TAPE MARK RECORD INCREASES THE BLOCK SIZE BY ONE(1) RECORD; IN OTHER WORDS, A BLOCK OF 100 RECORDS WILL HAVE THE TAPE MARK AS RECORD 101.

STALLS: THE STALL REQUESTS ARE RESPONDED TO BY A SIX (6) CHARACTER OCTAL NUMBER WITHIN THE LIMITS OF 1 THRU 177777. LEADING ZEROS ARE NOT REQUIRED AND AN ENTRY OF LESS THAN SIX (6) CHARACTERS SHOULD BE TERMINATED BY A CARRIAGE RETURN. EACH INCREMENT OF THE VALUE ADDS ABOUT 2.6 MICSEC TO THE DELAY.

READ: THE TIME DELAY BETWEEN EACH RECORD READ

WRITE: THE TIME DELAY BETWEEN EACH RECORD WRITTEN

TURN AROUND: TIME DELAY BETWEEN CHANGES OF TAPE DIRECTION (FORWARD,TO REVERSE,ETC.) AND BETWEEN BLOCKS.

FIXED PARAMETERS: IT SHOULD BE NOTED THAT ALL PARAMETERS EXCEPT FOR THE UNIT DESCRIPTION VALUES (UNIT NUMBER, DENSITY, AND PARITY) HAVE NUMINAL VALUES ALREADY STORED IN THE PROGRAM. AS EACH PARAMETER REQUEST (PATTERN NUMBER, RECORD COUNT, CHARACTER COUNT, AND STALLS) IS TYPED. ITS PRESENT STORED VALUE IS ALSO PRINTED. IF THESE VALUES NEED NOT BE CHANGED, SIMPLY TYPE A CARRIAGE RETURN AS RESPONSE AND NO CHANGE WILL BE MADE. EACH START OF THE PROGRAM AT 200(8) WILL SHOW THE CURRENT VALUES OF THESE PARAMETERS AS PER THE LAST ENTRY. WHEN A FRESH LOAD OF THE PAPER TAPE IS DONE. THE PARAMETERS WILL REFLECT THE FIXED VALUES STORED IN THE PROGRAM.

A. RECORD COUNT = 100
B. CHARACTER COUNT = 201
C. PATTERN NUMBER = 1
D. READ STALL = 1
E. WRITE = 1
F. TURN AROUND = 1

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SAMPLE START AT 200(8):

        THE FOLLOWING IS A SAMPLE OF THE
        PRINTED REQUESTS AND THEIR RESPONSES.
        RESPONSES ARE ENCLOSED IN PARENS FOR
        CLARITY ONLY AND (CR) MEANS CARRIAGE RETURN

LOAD ADDRESS 200(8), SET CONSOLE SWITCHES, PRESS START SWITCH:

        TMA-11 TAPE DRIVE TEST
        ENTER CONDITIONS IN OCTAL
        REGISTER START = 172520 (CR)
        VECTOR ADDRESS = 224 (CR)
        UNIT NUMBER=(5) 9 CHAN
        DENSITY=(3)
        PARITY=(0)
        UNIT NUMBER=(2) 7 CHAN
        DENSITY=(2)
        PARITY=(1)
        UNIT NUMBER=(CR)
        RECORD COUNT=100 (500)(CR)
        CHARACTER COUNT=201 (38)?(7)(CR)
        PATTERN NUMBER=1 (22)
        ?
        (6)(CR)
        TAPE MARK = 0 (1)(CR)

        ENTER STALLS
        READ=1 (CR)
        WRITE=1 (CR)
        TURN AROUND=1 (3000)(CR)

THE PROGRAM WILL NOW PERFORM THE TEST CYCLE SET IN
THE CONSOLE SWITCHES ON UNIT FIVE (5) THEN TWO (2),
ONE BLOCK ON EACH UNIT PER CYCLE, USING DATA PATTERN
NUMBER SIX (6) WITH A BLOCKING FACTOR OF 37 CHARACTERS
PER RECORD AND 500 RECORDS PER BLOCK.  THE DELAYS ARE SET
FOR MINIMUM ON READ AND WRITE, AND APPROXIMATELY .75
SECONDS ON TURN AROUND.
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5. DATA PATTERNS

THERE ARE TWENTY DATA PATTERN GENERATORS STORED IN CORE AND ANY ONE OF THESE MAY BE SELECTED. THE ONE UNIQUE CASE IS PATTERN ZERO(Ø); SELECTION OF PATTERN ZERO(Ø) REQUIRES THAT A PREVIOUSLY PREPARED PAPER TAPE BE ENTERED AT THE HIGH SPEED READER. THIS TAPE CONTAINS A DATA PATTERN OF NO MORE THAN 377 OCTAL CHARACTERS. THE FIRST CHARACTER READ IN IS THE NUMBER OF ACTUAL DATA CHARACTERS THAT ARE CONTAINED ON THE TAPE. EACH DATA CHARACTER MAY BE ANY COMBINATION OF BITS AND WILL BE LOADED INTO CORE AS THEY APPEAR ON THE TAPE. NO MATTER HOW MANY CHARACTERS ARE ON TAPE, THE ENTIRE WRITE BUFFER (2ØØØ CHARACTERS) WILL BE FILLED WITH THE PATTERN ENTERED SO THAT ANY SIZE RECORD CAN BE USED.

THE FOLLOWING IS A LIST OF THE DATA PATTERNS AVAILABLE:

DATAØ: EXTERNAL INPUT THRU HIGH SPEED READER
(SEE DTC; MAINDEC-11-DZTUF-A)

DATA1: ALL ONE BITS IN ALL CHARACTERS
DATA2: ALL ZERO BITS IN ALL CHARACTERS
DATA3: A ONE BIT WALKING FROM RIGHT TO LEFT IN A FIELD OF ZEROS
DATA4: A ZERO BIT WALKING FROM RIGHT TO LEFT IN A FIELD OF ONES.
DATA5: ALTERNATING ONE AND ZERO BITS IN EACH CHARACTER
DATA6: ALTERNATING ZERO AND ONE BITS IN EACH CHARACTER
DATA7: SAME AS DATA5 BUT WITH EVERY OTHER CHARACTER COMPLEMENTED
DATA1Ø: SAME AS DATA6 BUT WITH EVERY OTHER CHARACTER COMPLEMENTED
DATA11: INCREMENTING CHARACTERS (ØØØ-377)
DATA12: DECREMENTING CHARACTERS (377-ØØØ)
DATA13: ALTERNATING CHARACTERS OF ALL ZERO AND ALL ONE BITS
DATA14: ALTERNATING CHARACTERS OF ALL ONE AND ALL ZERO BITS
DATA15: SPECIAL PATTERN OF A WALKING ZERO BIT REPEATED 4 TIMES
DATA16: IBM COMPAT PATTERN 1: RIPPLE
DATA17: IBM COMPAT PATTERN 2: FIXED (ABCDEF)
DATA2Ø: IBM COMPAT PATTERN 3: FIXED (J)

6. RANDOMIZATION

THERE ARE THREE (3) VALUES THAT MAY BE GENERATED RANDOMLY; DATA, CHARACTER COUNT, AND RECORD COUNT. THESE ARE NORMALLY SET TO SOME FIXED VALUE BUT MAY BE RANDOMIZED BY SETTING THE APPROPRIATE CONSOLE SWITCHES.

A. RANDOM DATA: (CONSOLE SWITCH 8)
GENERATES AN ENTIRE BUFFER, CHARACTER BY CHARACTER, OF RANDOM DATA WHEN SWITCH 8 IS SET TO A ONE. ONCE SET, THE RESETTING OF SWITCH 8 CAUSES THE LAST GENERATED PATTERN TO BE RETAINED IN CORE. A RESTART AT LOCATION 200(8) OR 210(8) WILL CAUSE REVERSION OF THE DATA TO THE FIXED PATTERN REQUESTED INITIALLY. A RESTART AT LOCATION 204(8) WILL HOLD THE LAST GENERATED PATTERN IN CORE UNTIL SWITCH 8 IS AGAIN SET.
ALTHOUGH THE DATA IS GENERATED AS RANDOM, THE PROGRESSION OF RANDOM CHARACTERS IS ALWAYS THE SAME FROM THE OUTSET OF RANDOMIZATION. THEREFORE IT IS POSSIBLE TO GENERATE ONE TAPE REEL OF RANDOM DATA ON ONE UNIT, RELOAD THE PROGRAM TO RE-ESTABLISH THE OUTSET POINT, AND READ THE RANDOM TAPE REEL ON ANOTHER UNIT FOR COMPATABILITY TESTING. NOTE THAT MERELY RESTARTING THE PROGRAM WILL NOT RE-ESTABLISH THE OUTSET POINT FOR RANDOMIZATION, BUT THE PROGRAM MUST BE FULLY LOADED THEN RESTARTED IN ORDER TO GENERATE THE SAME PROGRESSION OF RANDOMIZATION! IN MULTIDRIVE SYSTEMS THE SAME BLOCK OF DATA, WHETHER RANDOM OR FIXED, IS WRITTEN OR READ ON EACH AVAILABLE UNIT IN THE ORDER THAT THEY WERE ENTERED, BEFORE BEING CHANGED.

B. RANDOM CHARACTER COUNT: (CONSOLE SWITCH 7)
GENERATES A DIFFERENT NUMBER OF CHARACTERS PER RECORD TO BE WRITTEN ON EACH BLOCK CYCLE. THE SAME NUMBER OF CHARACTERS PER RECORD IS WRITTEN OR READ ON EACH AVAILABLE UNIT BEFORE BEING CHANGED. RESETTING SWITCH 7 HOLDS THE LAST VALUE GENERATED.

C. RANDOM RECORD COUNT: (CONSOLE SWITCH 6)
GENERATES A DIFFERENT NUMBER OF RECORDS FOR EACH BLOCK OF DATA WRITTEN OR READ ON EACH BLOCK CYCLE. THE SAME NUMBER OF RECORDS IS WRITTEN OR READ ON EACH AVAILABLE UNIT BEFORE BEING CHANGED. RESETTING SWITCH 6 HOLDS LAST VALUE GENERATED.

7. DYNAMIC PARAMETERS:

THE THREE (3) STALL VALUES ARE CONSIDERED TO BE DYNAMIC PARAMETERS AS THEY MAY BE CHANGED WHILE THE PROGRAM IS RUNNING BY TYPING A CONTROL C CHARACTER AT THE TELETYPE. AS SOON AS THE BUS IS RELEASED BY THE MAG TAPE OPERATION IN PROGRESS, THE PROGRAM WILL RESPOND TO THE CONTROL C INPUT BY TYPING A REQUEST FOR NEW STALL PARAMETERS. THE LAST VALUES THAT WERE ENTERED WILL BE PRINTED AS THE STORED VALUES AND MAY BE CHANGED BY ENTERING NEW VALUES OR LEFT UNCHANGED BY TYPING A CARRIAGE RETURN.

8. CONSOLE SWITCH SETTINGS

THE CONSOLE SWITCHES ARE USED TO SET UP THE TEST CYCLE DESIRED, TO GENERATE RANDOM VALUES, AND TO CONTROL ERROR RESPONSES. THE SWITCHES SHOULD BE SET IN THE DESIRED MANNER BEFORE PRESSING THE START SWITCH BECAUSE THEY ARE ALL DYNAMIC AND WILL RUN THE PROGRAM IN ANY CONFIGURATION. ALL SWITCHES SET TO ZERO(0) IS NORMAL.

SW15: 1=STOP ON ERROR
0=CONTINUE ON ERROR

SW14: 1=YOZZLE ON CURRENT BLOCK
0=DO NOT YOZZLE ON BLOCK

SW13: 1=DO NOT CHECK DATA ERRORS
0=CHECK DATA ERRORS

SW12: 1=DO NOT CHECK WRITE STATUS ERRORS
0=CHECK WRITE STATUS ERRORS

SW11: 1=DO NOT CHECK READ STATUS ERRORS
0=CHECK READ STATUS ERRORS

SW10: 1=DO NOT PRINT ANY ERRORS
0=PRINT ALL ERRORS

SW9: 1=REWIND ALL AVAILABLE TAPES
0=DO NOT REWIND

SW8: 1=GENERATE RANDOM DATA
0=USED FIXED DATA

SW7: 1=GENERATE RANDOM CHARACTER COUNT
0=USE FIXED CHARACTER COUNT

SW6: 1=GENERATE RANDOM RECORD COUNT
0=USED FIXED RECORD COUNT

SW5: 1=YOZZLE ON CURRENT RECORD
0=DO NOT YOZZLE ON RECORD

SW4: 1=PRINT STATISTICS
0=DO NOT PRINT STATISTICS

SW3: 1=DO NOT READ
0=READ

SW2: NOT USED

SW1: 1=DISABLE WRITE AND READ RETRY OPTION
0=ENABLE WRITE AND READ RETRY OPTION

SW0: 1=DO NOT WRITE
0=WRITE

SWITCH EXPLANATION AND EXAMPLES:

SW0+SW3: THESE SWITCHES ARE USED TO CONTROL THE SEQUENCE OF MAG TAPE OPERATIONS PREFORMED ON EACH AVAILABLE UNIT. THE BLOCK OF DATA DESCRIBED THROUGH THE RESPONSES TO TELETYPE REQUESTS AT INITIAL START WILL BE EITHER WRITTEN OR READ FROM EACH AVAILABLE UNIT IN THE ORDER THAT THEY WERE ENTERED. THE SEQUENCE OF OPERATIONS IS CALLED A CYCLE, AND WILL BE PERFORMED CONTINUOUSLY UNTIL STOPPED BY THE OPERATOR. WHEN END OF TAPE IS REACHED, THE UNIT WILL BE REWOUND AND FLAGGED AS UNAVAILABLE FOR TEST UNTIL ALL UNITS HAVE REACHED EOT, AT WHICH TIME TESTING IS RESUMED ON ALL AVAILABLE UNITS.

EXAMPLES: SW0+SW3

A. SW0=0,SW3=1
WRITE ONLY X RECORDS OF Y CHARACTERS

B. SW0=1,SW3=0
READ ONLY X RECORDS OF Y CHARACTERS

C. SW0=0,SW3=0
WRITE THEN BACKSPACE AND READ X RECORDS

SW1: SWITCH ONE(1), WHEN SET TO A ZERO (0), WILL CAUSE ANY DATA RELATED WRITE ERROR TO BE RETRIED. THE RETRY SCHEME CONSISTS OF REWRITING THE RECORD IN THE SAME SPOT ON THE TAPE FOUR (4) TIMES. IF ALL FOUR (4) REPEATS ARE SUCCESSFUL, THE RECORD IS CONSIDERED RECOVERED, AND A TAPE WRITE ERROR IS LOGGED. IF ANY OF THE FOUR (4) REPEATS IS UNSUCCESSFUL, A WRITE WITH EXTENDED INTERECORD GAP IS DONE, A SUSPECTED BAD TAPE SPOT LOGGED AT THIS BLOCK AND RECORD NUMBER, AND A SECOND RETRY OF FOUR REPEATS IS DONE. IF AFTER FOUR (4) RETRIES, THE RECORD CANNOT BE RECOVERED A NOTIFICATION IS PRINTED, AND TESTING IS RESUMED ON THE NEXT RECORD. IF 20(8) BAD TAPE SPOTS ARE FOUND, THE UNIT WILL BE REWOUND AND REMOVED FROM TESTING WITH AN APPROPRIATE MESSAGE PRINTED.

SWITCH ONE (1), WHEN SET TO A ZERO (0), WILL ALSO CAUSE ANY DATA RELATED READ ERROR TO BE RETRIED. THE RETRY SCHEME CONSISTS OF REREADING THE RECORD A MAXIMUM OF FOUR (4) TIMES. IF THE RECORD IS SUCCESSFULLY RECOVERED ON ANY OF THE REREADS IT IS CONSIDERED FOR STATISTICS PURPOSES TO BE A SOFT READ ERROR AND TESTING CONTINUES IF THE REREADS FAIL TO RECOVER THE RECORD, THE ERROR IS LOGGED AS A HARD READ ERROR.

SW4: SWITCH FOUR (4) WHEN SET WILL PRINT THE STATISTICS GATHERED FOR EACH UNIT. THE NUMBER WILL BE PRINTED AT THE END OF A BLOCK CYCLE.

SEE ITEM 10, PAGE 20 FOR FULL DETAILS.

SW5: SWITCH FIVE (5) WHEN SET DURING A READ OPERATION WILL CAUSE THE PROGRAM TO CONTINUOUSLY READ THE CURRENT RECORD BY SPACING REVERSE OVER THE RECORD AND REREADING THAT RECORD. THIS TAPE MOVEMENT IS CALLED YOZZLING. THERE IS A SOFTWARE DELAY EXECUTED BETWEEN EACH SPACE/READ OF THE RECORD AND IT MAY BE VARIED BY TYPING CONTROL C ON THE TELETYPE DURING THE EXECUTION OF THE YOZZLE AND RESPONDING TO THE PRINTED REQUEST WITH A SIX (6) DIGIT VALUE. THE YOZZLE STALL IS PRESET TO A VALUE OF 1000 IN THE PROGRAM TO PREVENT EXCESSIVE TAPE WEAR, BUT MAY BE SET TO ANY VALUE THROUGH THE TELETYPE.

SW6-8: THESE THREE (3) SWITCHES CONTROL THE RANDOMIZATION OF DATA AND BLOCK SIZE AND MAY BE SET AND RESET AT ANY TIME. THE ACTUAL CHANGE WILL TAKE PLACE BETWEEN BLOCK CYCLES.

SW9: SWITCH NINE (9) WHEN SET WILL CAUSE ALL AVAILABLE TAPE UNITS TO BE REWOUND AT THE END OF THE CURRENT BLOCK CYCLE. TESTING WILL BE RESUMED AT A BLOCK COUNT OF ONE (1) WHEN ALL UNITS HAVE REACHED BOT.

SW10-13: THESE SWITCHES ARE USED TO CONTROL THE ERROR HANDLING TO BE DONE ON THE TAPE OPERATION DESCRIBED BY SWITCHES 0+3.

A. SWITCH TEN (10) WHEN SET TO A ONE WILL DISALLOW ANY ERROR PRINTOUTS MADE ON THE OPERATION IN PROGRESS. CATASTROPHIC FAILURES AND INFORMATION PRINTOUTS WILL STILL OCCUR. IE: UNIT NOT AVAILABLE, ILLEGAL BOT, DROP OR PICK OVERFLOW, AND EOT REWIND.

B. SWITCH ELEVEN (11) WHEN SET TO A ONE WILL DISALLOW THE CHECKING FOR STATUS ERRORS ON READ OPERATIONS.

C. SWITCH TWELVE (12) WHEN SET TO A ONE WILL DISALLOW THE CHECKING FOR STATUS ERRORS ON WRITE OPERATIONS.

D. SWITCH THIRTEEN (13) WHEN SET TO A ONE WILL DISALLOW THE CHECKING OF READ DATA. THIS SWITCH HAS NO EFFECT ON STATUS CHECKING.

Sw14: SWITCH FOURTEEN (14) IS USED DURING A READ ONLY OPERATION; WHEN SET, THE BLOCK OF DATA BEING READ WILL CONTINUOUSLY BE READ AND SPACED OVER SO THAT TAPE WILL REMAIN AT THE SAME BLOCK. WHEN RESET, THE TAPE WILL BE ALLOWED TO MOVE FORWARD AND DATA BLOCKS WILL BE READ PROGRESSIVELY.
THIS IS A BLOCK YOZZLE.

Sw15: SWITCH FIFTEEN (15) WHEN SET TO A ONE, WILL CAUSE THE PROGRAM TO HALT ON ANY ERROR DETECTED BY THE OPERATION IN PROGRESS.
IF BOTH SWITCH TEN (10) AND FIFTEEN (15) ARE SET, THE ACTUAL ERROR DETECTED WILL NOT BE PRINTED BUT WILL CAUSE A HALT.
IF SWITCH TEN (10) IS RESET BEFORE PRESSING CONTINUE, THE ERROR WHICH CAUSED THE HALT WILL BE PRINTED BEFORE TESTING IS RESUMED.

9. ERROR PRINTOUTS

THERE ARE THREE TYPES OF ERROR PRINTOUTS MADE BY THE PROGRAM; OPERATION ERRORS, DATA ERRORS, AND CONDITION ERRORS. EACH ERROR MESSAGE PRINTED IS PRECEDED BY A HEADER WHICH CONTAINS THE UNIT NUMBER, BLOCK COUNT NUMBER, BAD RECORD NUMBER PLUS TOTAL NUMBER OF RECORDS, SIZE OF RECORD, AND TYPE OF OPERATION WHICH CAUSED ERROR.

A. OPERATION ERRORS:

THESE ARE ERRORS WHICH CAN OCCUR AS A DIRECT RESULT OF A TAPE OPERATION.

1. READ/WRITE STATUS ERRORS:

   THESE ARE INDICATED BY THE ERROR BIT (BIT 15) OF THE TAPE COMMAND REGISTER BEING SET TO A ONE.

2. RECORD LENGTH ERRORS:

   THESE ARE INDICATED BY A BYTE COUNT OTHER THAN ZERO (0) OR AN INCORRECT CURRENT MEMORY ADDRESS OR BOTH

3. TAPE POSITIONING ERRORS:

   THESE ARE INDICATED BY A SPACE COUNT OTHER THAN ZERO (0), NO BOT FOUND FROM A REWIND, OR NO TAPE UNIT READY AT THE END OF REWIND.

B. DATA ERRORS:

DATA ERRORS WILL OCCUR WHEN TAPE IS BEING READ AND THE DATA DOES NOT MATCH THE EXPECTED DATA.

BECAUSE DATA RECORDS CAN BE UP TO TWO THOUSAND CHARACTERS LONG, AN ERROR CONDITION WHICH WILL CAUSE THE ENTIRE RECORD TO READ INCORRECTLY COULD CAUSE A VERY LENGTHY PRINTOUT. THEREFORE, A COUNTER OF SUCCESSIVE BAD CHARACTERS IS EMPLOYED. IF TEN (10) CHARACTERS IN SUCCESSION ARE BAD, A NOTIFICATION IS PRINTED (BLOOD BATH) AND THE NEXT TWENTY (20) CHARACTERS ARE SKIPPED BEFORE CHECKING IS RESUMED. IF THE BLOOD BATH CONDITION OCCURS THREE (3) TIMES IN ONE RECORD, THE REST OF THE RECORD IS SKIPPED, DOWN TO THE LAST TEN (10) CHARACTERS, WHICH WILL BE CHECKED. THE SKIPPING AND RESUMPTION OF CHECKING WILL ONLY BE DONE ON RECORDS WHICH ARE LONG ENOUGH TO ALLOW IT.

C. CONDITION ERRORS:

THESE ERRORS REFLECT THE STATE OF THE TAPE SYSTEM BEFORE AND AFTER AN OPERATION.

1. EOT: WHEN AN EOT (END OF TAPE) IS ENCOUNTERED DURING EITHER A READ OR A WRITE, THAT UNIT IS FLAGGED AS UNAVAILABLE FOR TESTING AND IS REWOUND UNTIL ALL AVAILABLE UNITS HAVE REACHED EOT. AT WHICH TIME TESTING IS RESUMED ON ALL AVAILABLE UNITS.

2. ILLEGAL BOT: WHEN A UNIT ENCOUNTERS BEGINNING OF TAPE (BOT) DURING A READ OR WRITE OPERATION THE ERROR IS PRINTED AND THE PROGRAM STOPPED. THIS IS A CATASTROPHIC ERROR. TESTING MAY BE RESUMED BY PRESSING THE CONTINUE SWITCH.

3. UNIT NOT AVAILABLE: THIS CAN OCCUR WHEN THE SELECTED UNIT HAS BECOME UNAVAILABLE. THIS IS A CATASTROPHIC ERROR AND WILL CAUSE A HALT. TESTING MAY BE RESUMED BY PRESSING THE CONTINUE SWITCH.

4. CONTROLLER NOT READY: BEFORE ANY OPERATION IS ATTEMPTED THE CONTROLLER IS CHECKED FOR READY. IF IT IS NOT READY, AN ERROR WILL BE PRINTED.

5. NO INTERRUPT RETURNED: EACH TAPE OPERATION SHOULD BE TERMINATED BY SETTING AN INTERRUPT IN THE CPU. IF NO INTERRUPT IS RETURNED WITHIN THE APPROPIATE TIME, AN ERROR IS PRINTED.

E. EXAMPLES:

GLOSSARY:

BN = BLOCK NUMBER
RN = RECORD NUMBER (X) OF A TOTAL OF (Y)
RS = RECORD SIZE IN CHARACTERS PER RECORD
WE = WRITE ERROR
RE = READ ERROR
SE = SPACE ERROR
F = FORWARD
CR = COMMAND REGISTER
CS = STATUS REGISTER
WC = BYTE COUNTER
CA = CURRENT MEMORY ADDRESS POINTER AND EXPECTED VALUE
CN = CHARACTER NUMBER
G = GOOD DATA (SHOWN IN BIT FORMAT AS IN CORE)
B = BAD DATA (SHOWN IN BIT FORMAT AS IN CORE)
ERR AMT = NUMBER LEFT TO SPACE
TM = TAPE MARK (OFTEN CALLED EOF FOR END OF FILE)
LPC = LONGITUDINAL PARITY CHECK (RECEIVED - EXPECTED)
PATTRN = DATA PATTERN (R=RANDOM)

```
        EXAMPLE 1
        ---------

EXAMPLE 1: IN THIS EXAMPLE A TAPE VERTICAL PARITY ERROR
        WAS DETECTED DURING A WRITE OPERATION OF THE
        TWELVTH (12) RECORD OF THE BLOCK.  THE WORD
        COUNT AND CURRENT MEMORY ADDRESS ARE CORRECT.
        THE RETRY OPTION WAS DISABLED.

UNIT NO. 3 *PATTRN 1
BN 406*RN 12-200*RS 2000*WE
COMD 1010001111000100
STAT 0001000001000001
WC 0
CA 14436-14436

        EXAMPLE 2
        ---------

EXAMPLE 2: IN THIS EXAMPLE A RECORD LENGTH ERROR WAS
        DETECTED WHILE READING THE FIRST  RECORD OF
        THE BLOCK.  THE RETRY OPTION WAS DISABLED.  THE
        WORD COUNT SHOWS A COUNT OF 20 CHARACTERS
        LEFT TO BE TRANSFERRED.  THE CURRENT MEMORY
        ADDRESS REFLECTS THAT A SHORTAGE OF 20
        CHARACTERS TRANSFERRED HAD OCCURRED.  IN
        THIS EXAMPLE THE STATUS AND COMMAND
        REGISTERS DO NOT SHOW ANY ERROR, BUT
        THE LPC IS SHOWN TO BE INCORRECT.

UNIT NO. 7  *PATTRN  6
BN 10*RN 1-100*RS 50*RE  F***
CR 0100011111000100
CS 0000000001000001
WC 20
CA 12466-12506
LPC 337 -147

        EXAMPLE 3
        ---------

EXAMPLE 3: IN THIS EXAMPLE THE TAPE UNIT WAS TRYING
        TO SPACE OVER THE 15 RECORDS IN
        THE BLOCK IN ORDER TO ESTABLISH PROPER
        POSITION TO BEGIN READING.
        THE OPERATION WAS TERMINATED
        BEFORE THE ENTIRE 15 RECORDS WERE TRAVERSED
        AND AN ERROR SHOWN BECAUSE THE TAPE IS
        NOT IN PROPER POSITION TO BEGIN READING.

UNIT NO. 0 *PATTRN R
BN 2*RN 15-15*RS 23 *SE
ERR AMT 4
```

```
        EXAMPLE 4
        ---------

EXAMPLE 4: IN THIS EXAMPLE UNIT NUMBER ONE (1) HAD BEEN
        REWOUND VIA CONSOLE SWITCH NINE (9) AND AT THE
        COMPLETION OF THE OPERATION BOT WAS NOT SET IN
        THE STATUS REGISTER.

UNIT NO. 1  *PATTRN R
BN 3002*RN 65-65*RS 10
NO BOT ON REWIND-HALT

        EXAMPLE 5
        ---------

EXAMPLE 5: IN THIS EXAMPLE TWO BAD CHARACTERS WERE
        READ FROM TAPE IN THE FORWARD DIRECTION.
        THE FIRST (0) AND THE THIRTEENTH (13) CHARACTERS
        OF THE TOTAL NUMBER OF SIXTEEN (16) CHARACTERS
        IN THE BLOCK ARE BAD.  CHARACTER NUMBER
        ZERO (0) HAS DROPPED BIT NUMBER FIVE (5) AND
        CHARACTER NUMBER TWELVE (12) HAS PICKED UP
        BIT NUMBER SEVEN (7).

UNIT NO. 5  *PATTRN 5
BN 12*RN 3-10*RS 15*DE-F**
CN 0
G; 10101010
B; 10001010
CN 12
G; 01010101
B; 11010101
```

```
        EXAMPLE 6
        ---------

EXAMPLE 6: IN THIS EXAMPLE UNIT NUMBER SIX (6) HAS
        REACHED END OF TAPE (EOT) FOR THE 1ST TIME AND WILL BE REWOUND.
        TESTING WILL RESTART ON UNIT NUMBER SIX (6)
        WHEN ALL UNITS HAVE REACHED EOT.

UNIT NO. 6  *PATTRN  R
BN 677 *RN 25-600*RS 1566
EOT  NO. 1
UNIT WILL REWIND AND BE
RESTARTED ON BLOCK ONE
WHEN ALL AVAIL UNITS REACH EOT

        EXAMPLE 7
        ---------

EXAMPLE 7: IN THIS EXAMPLE UNIT NUMBER TWO (2) HAS
        ENCOUNTERED BEGINNING OF TAPE (BOT) AND
        THE PROGRAM WILL BE HALTED,  TESTING MAY
        BE RESUMED BY PRESSING THE CONTINUE SWITCH.

UNIT NO. 2  *PATTRN 2
BN 56*RN 2-4*RS 1200
ILLEGAL BOT-HALT

        EXAMPLE 8
        ---------

EXAMPLE 8: IN THIS EXAMPLE THE SELECTED UNIT (NUMBER 3)
        HAS BECOME UNAVAILABLE.  THE PROGRAM WILL
        HALT TO ALLOW OPERATOR CORRECTION AND MAY
        BE RESUMED BY PRESSING THE CONTINUE SWITCH.

UNIT NO. 3  *PATTRN 4
BN 1*RN 0-200*RS 66
NOT AVAILABLE

        EXAMPLE 9
        ---------

EXAMPLE 9: IN THIS EXAMPLE THE WRITE OPERATION EXECUTED ON
        UNIT NUMBER SIX (6) WAS NOT COMPLETED AND NO
        INTERRUPT WAS RETURNED.

UNIT NO. 6  *PATTRN R
BN 12*RN 3-4*RS 100*WE
NO INTERRUPT RETURNED
```

```
        EXAMPLE 10
        ----------

EXAMPLE: 10  THIS EXAMPLE SHOWS A READ ERROR WHICH
         RECOVERED ON THE SECOND RETRY.  THIS
         ERROR WILL BE LOGGED AS A RDERR BUT WILL BE
         CATEGORIZED AS A SOFT ERROR.  THE REGISTERS
         SHOW A PARITY ERROR WAS THE CAUSE OF THE ERROR.

UNIT NO. 1  *PATTRN R
*BN 10 *RN 2-100 *RS 1117 *RE  F***
COMD 1110100110000010
STAT 0011000001000001
WC 0
LPC 337-147
***ORIGINAL ERROR***


UNIT NO. 1  *PATTRN R
*BN 10 *RN 2-100 *RS 1117 *RE  F***
COMD 1110100110000010
STAT 0011000001000001
WC 0
LPC 337-147
READ FAILED--RETRY: 1
REREAD SUCCESSFUL--RETRY: 2

        EXAMPLE 11
        ----------

EXAMPLE 11:  THIS EXAMPLE SHOWS A WRITE ERROR WHICH
         WAS NOT RECOVERED BY SUCCESSFULLY REWRITTING
         THE RECORD FOUR TIMES AT THAT LOCATION.  THE
         RECORD WAS SUCCESSFULLY WRITTEN AFTER 3
         INCHES OF TAPE WAS ERASED.  THIS ERROR
         WILL BE LOGGED AS A BAD TAPE SPOT.

UNIT NO. 0 *PATTRN R
*BN 2 *RN 370 -461 *RS 2407 *WE
COMD 1110000010000100
STAT 0011000001000001
WC 0
CA 25613 -25613
***ORIGINAL ERROR***

UNIT NO. 0 *PATTRN R
*BN 2 *RN 370 -461 *RS 2407 *WE
COMD 1110000010000100
STAT 0011000001000001
WC 0
CA 25613 -25613
SUSPECT BAD TAPE
RETRY: 0
REPEAT: 0
RECOVERED
RETRY: 1
```

10. STATISTICS PRINTOUT

THE PROGRAM GATHERS A VARIETY OF STATISTICS DURING THE COURSE OF ITS TESTING. THE STATISTICS ARE KEPT ON A UNIT BY UNIT BASIS AND ARE SUMMARIZED IN A STATISTICS PRINTOUT. STATISTIC PRINTOUTS CAN BE PRINTED AT THE END OF EACH BLOCK CYCLE BY SETTING SWITCH FOUR (4) TO 1. A STATISTIC PRINTOUT IS AUTOMATICALLY PRINTED WHEN A UNIT REACHES EOT AND IS REWOUND.

HERE IS AN EXPLANATION OF THE STATISTIC SUMMARY.

DROPS: THE NUMBER OF BITS DROPPED ON A PER TRACK BASIS. DROPS ARE COLLECTED DURING THE DATA CHECK ROUTINE.

PICKS: THE NUMBER OF BITS PICKED ON A PER TRACK BASIS. DROPS ARE COLLECTED DURING THE DATA CHECK ROUTINE.

WTERR: THE NUMBER OF RECORDS IN WHICH A WRITE ERROR OCCURRED. IF WRITE RETRY WAS ENABLED, WTERR WILL CONTAIN ONLY THOSE RECORDS WHICH WERE NOT RECOVERED AFTER ONE RETRY.

RTRY: THE NUMBER OF RETRIES INITIATED UNDER THE WRITE RETRY OPTION. (SEE ITEM 8., SW1:)

RDERR: THE TOTAL NUMBER OF RECORDS IN WHICH A READ ERROR OCCURRED.

SOFT: THE NUMBER OF READ ERRORS WHICH WERE RECOVERED WITHIN A MAXIMUM OF FOUR REREADS OF A RECORD UNDER THE READ RETRY OPTION. (SEE ITEM 8., SW1:)
**NOTE: SOFT READ ERRORS ARE ONLY CATEGORIZED FOR THOSE READ ERRORS OCCURRING WHEN CONSOLE SWITCH 1 IS SET TO ZERO.

HARD: THE NUMBER OF READ ERRORS WHICH REMAINED UNRECOVERED UNDER THE READ RETRY SCHEME. (SEE ITEM 8., SW1:)
**NOTE: HARD READ ERRORS ARE ONLY CATEGORIZED FOR THOSE READ ERRORS OCCURRING WHEN CONSOLE SWITCH 1 IS SET TO ZERO.

DTERR: THE NUMBER OF DATA ERRORS FOUND FOR THIS UNIT.
**NOTE: DATA ERRORS ARE ONLY FOUND FOR THOSE RECORDS WHICH WERE READ WITH SWITCH 11 RESET TO ZERO.

```
BAD TAPE SPOTS:  A COUNT OF THE NUMBER OF TAPE SPOTS
        WHERE A RECORD COULD NOT BE REWRITTEN SUCCESSFULLY
        UNDER THE WRITE RETRY OPTION (SEE ITEM8,, SW1:)
        FOLLOWING THE COUNT IS A LIST OF THE BAD TAPE
        LOCATIONS IDENTIFIED BY THE BLOCK AND RECORD NUMBER
        WHEN THE BAD TAPE SPOT WAS LOGGED.

        EXAMPLE
        -------
DROPS:  0 0 0 0 7 0 0 0
PICKS:  0 0 0 2 0 0 0 0
WTERR:  3
 RTRY:  4
RDERR:  6
 SOFT:  1
 HARD:  5
DTERR:  10
1  BAD TAPE SPOTS
0 *BN 16 *RN 41
```

11. AUTO SEQUENCE

THE AUTO SEQUENCE (START AT ADDRESS 240) WILL EXECUTE A PREDETERMINED TEST PLAN ON ALL AVAILABLE UNITS. THE ONLY OPERATOR RESPONSE REQUIRED IS TO THE TYPED REQUESTS FOR THE TMA-11'S ADDRESS AND VECTOR AND CONTINUOUS OR SINGLE CYCLE. ALL SWITCHES REMAIN ACTIVE AND MAY BE USED NORMALLY; HOWEVER, THE INTENT IS TO LEAVE ALL SWITCHES DOWN AND ALLOW FULL EXECUTION OF THE TEST PLAN FOR SYSTEM CHECKOUT.

SAMPLE START AT 240(8): AUTO SEQUENCE

LOAD ADDRESS 240(8), SET SWITCHES TO ZERO, PRESS START:

```
        TMA-11 AUTO SEQUENCE TEST
        ENTER RESPONSES IN OCTAL

        REGISTER START = 172520 (CR)
        VECTOR = 224 (CR)
        AUTO CONT: 0 (1)
```

THIS EXAMPLE SHOWS AN AUTO SEQUENCE START WITH THE TMA-11 AT BUS ADDRESS 172520 AND A VECTOR OR 224. ALL AVAILABLE UNITS WILL BE TESTED CONTINUOUSLY.

AS EACH PASS IS COMPLETED A DIVIDER LINE OF ASTERISKS WILL BE PRINTED FOLLOWED BY AN END OF PASS MESSAGE INDICATING HOW MANY PASSES HAVE BEEN COMPLETED SINCE THE AUTO SEQUENCE WAS BEGUN. AT THE START OF EACH PASS THE UNITS BEING TESTED ARE PRINTED.

AUTO SEQUENCE TEST PLAN:

THE AUTO SEQUENCER WILL EXECUTE A PASS CONSISTING OF THE WRITING, READING, AND CHECKING OF SEVERAL DIFFERENT DATA PATTERNS. EACH PASS WILL START AT BOT AND PROCESS AN ENTIRE MAG TAPE BEFORE REWINDING

THE UNITS WILL BE SET UP TO WRITE 800 BPI IN NINE TRACK FORMAT. ODD PARITY WILL BE USED AND NO TAPE MARKS WILL BE WRITTEN.

THE DATA PATTERNS WILL BE AS FOLLOWS:

THREE FIXED DATA PATTERNS:

EACH PATTERN WILL BE USED FOR SIX BLOCKS.
EACH BLOCK CONSISTS OF (100) 4000 CHARACTER RECORDS.

```
PATTERN 3:      WALKING ONE BIT
PATTERN 7:      ALTERNATING ONE AND ZERO BITS
PATTERN 11:     INCREMENTING CHARACTERS (000-377)
```

RANDOM DATA:

FOLLOWING THE FIXED DATA PATTERNS, RANDOM
DATA WILL BE WRITTEN IN THE SAME BLOCK STRUCTURE
UNTIL EOT IS REACHED.
IT IS IMPORTANT THAT THE TAPE USED FOR THE TEST
BE OF SUFFICIENT LENGTH TO ACCOMODATE ALL OF
THE FIXED DATA PATTERNS AND AT LEAST ONE
RECORD OF RANDOM DATA; OTHERWISE, THE TAPE WILL
BE REWOUND UNTIL ALL OF THE DATA PATTERNS
HAVE BEEN TESTED.

12. TESTING PROCEDURES

AS PREVIOUSLY STATED THIS PROGRAM CONTAINS NO FIXED TESTS. THE ENTIRE TEST CYCLE TO BE EXECUTED IS DESCRIBED BY THE OPERATOR THOUGH RESPONSES TO TELETYPE REQUESTS FOR PARAMETERS AND CONSOLE SWITCH SETTINGS FOR OPERATION. THE OPERATION SELECTED WILL BE EXECUTED WITH THE PARAMETERS ENTERED CONTINUOUSLY ON EACH AVAILABLE UNIT, ONE BLOCK AT A TIME, UNTIL STOPPED BY THE OPERATOR. THE OPERATION MAY BE CHANGED DYNAMICALLY BY CHANGING THE CONSOLE SWITCHES AT ANY TIME. THE PROGRAM WILL ATTEMPT TO PERFORM ANY OPERATION SET AND THEREFORE CAUTION SHOULD BE TAKEN TO ASSURE THAT THE UNIT IS CAPABLE OF PERFORMING AS REQUESTED. FOR INSTANCE, ONE SHOULD NOT ATTEMPT TO PERFORM READ OPERATIONS ON A TAPE WHICH HAS NOT BEEN WRITTEN AS THE DATA, IF ANY, IS UNPREDICTABLE. HOWEVER, IF A TAPE HAS BEEN WRITTEN WITH THIS PROGRAM, IT CAN BE READ AS OFTEN AS DESIRED WITHOUT BEING REWRITTEN. THIS IS A GOOD PROCEDURE TO USE FOR TESTING TAPE COMPATABILITY. SCOPING OF TAPE UNITS BECOMES SIMPLE; BY SETTING THE DESIRED OPERATION AND ITS PARAMETER, A UNIT MAY BE CONTINUOUSLY EXERCISED IN ANY MANNER DESIRED. BY USING THE VARIOUS ERROR CONTROL SWITCHES AND ENTERING THE NEEDED STALL, ANY FUNCTION CAN BE SCOPED RATHER EASILY. RELIABILITY TESTING CAN BE PREFORMED BY USE OF THE RANDOMIZATION CAPABILITY. PERHAPS A CYCLE OF RANDOM TESTING MIGHT BE SET UP AND ALLOWED TO RUN FOR SOME PERIOD OF TIME, THE STATISTICAL COLLECTION OF DROPS AND PICKS IS THEN SIGNIFICANT. INTERMITTANT PROBLEMS CAN BE FOUND BY SETTING THE DESIRED OPERATION IN MOTION AND DISALLOWING ERROR PRINTOUTS WHILE ALLOWING A HALT ON ERROR. THE ERROR THAT CAUSED THE HALT CAN BE PRINTED BY RESETTING CONSOLE SWITCH TEN AND PRESSING CONTINUE. IF SOME PARTICULAR DATA PATTERN SHOULD BE CAUSING DATA ERROR, USE OF THE YOZZLE SWITCH AND ITS ASSOCIATED STALL CAN BE USED TO ALLOW SCOPING OF THIS PARTICULAR RECORD.

AS YOU SEE, THERE ARE MYRIAD TESTING PROCEDURES WHICH COULD BE PERFORMED. THE PARAMETERS, TAPE OPERATIONS, ERROR EXAMINATION AND REPORTING ARE ALL AT YOUR DISCRETION.

TRY IT, YOU'LL LIKE IT.

13. LISTING

PART II
TMA11 CONTROLLER

CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The TMA11 Controller is the interface between the TS03 DECmagtape Transport and the Unibus. Thus, it controls command and data transfers between the tape transport and any device connected to the bus, such as the processor or memory. One controller can handle two TS03 DECmagtape Transports.

Basically, the controller consists of six major registers that have been assigned standard bus addresses and can be loaded or read by any PDP-11 instruction referring to that address. Four of the registers can be loaded or read from the bus; the remaining two registers can only be read from the bus.

The controller has three main functions: handling data transfers, issuing control commands, and monitoring operation of the system.

During data transfer functions, the controller assembles the data word from the magentic tape and places it on the bus (read operation), or assembles it from the bus and loads it into the tape transport read/write heads (write operation) for recording on magnetic tape. The commands necessary to perform the specified operation are generated by the controller under program control.

Normal data word transfers are performed by direct memory access transactions at the NPR level. If the controller is ready to begin a new function or if an error condition exists, it issues an interrupt request so that it can be serviced by the program.

In addition to the commands required for data transfers, the controller may issue other commands governing tape unit selection, direction of tape travel, rewind, space forward, space reverse, write end-of-file mark, etc. The controller also monitors various functions and provides an indication of error conditions. The status of the monitored functions is stored in one of the controller registers.

1.2 PHYSICAL DESCRIPTION

The TMA11 consists of the following:

Logic Assembly
H720 Power Supply*
Two BC11A Cable Assemblies
Power Harness
Priority Jumper Level No. 5

One BC11A cable assembly is used to connect the TMA11 to the TS03 DECmagtape Transport. DC operating power for the TMA11 is provided by H720 power supply via the power harness.

*For a detailed description of the H720 power supply, refer to the *H720 Power Supply and Mounting Box Manual,* EK-H720-TM-003.

1.3 SPECIFICATIONS

Environmental

Ambient Temperature	40° to 110° F
Relative Humidity	20% to 95% (without condensation)

Electrical

AC Input Power to H720 Power Supply

TMA11-A	115 Vac, 50/60 Hz at 6 A, single phase
TMA11-B	230 Vac, 50/60 Hz at 3 A, single phase

DC Voltage Requirements of TMA11 Controller	+5 V at 16 A -15 V at 10 A } Provided by H720 power supply
Electrical Characteristics	Electrical characteristics of controller meet PDP-11 Unibus interface specifications.

Physical

Size

TMA11	5-1/4 in. high, 19 in. wide
H720 Power Supply	8-1/2 in. high, 16-1/2 in. wide, 5-1/2 in. deep

Mounting

TMA11 H720 Power Supply	Mounts in standard 19 in. rack

CHAPTER 2
PROGRAMMING INFORMATION

2.1 SCOPE

This chapter presents general programming information for software control of the TMA11 Controller. Although a typical program example is included in this chapter, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook,* DEC-11-XPTSA-A-D.

This chapter of the manual is divided into four major portions: device registers, interrupts, programming note, and program example.

2.2 DEVICE REGISTERS

All software control of the TMA11 Controller is performed by means of six device registers within the controller. These registers have been assigned bus addresses and can be read or loaded using any PDP-11 instruction that refers to their address. The six device registers and associated addresses are listed in Table 2-1. Note that these addresses can be changed by altering the jumpers on the M105 Address Selector module. However, any DEC programs that refer to these addresses must also be modified accordingly if the jumpers are changed.

Figures 2-1 through 2-7 show the bit assignments within the six device registers. Except in the case of the data buffer register, the unused and load-only bits are always read as 0s. Loading unused or read-only bits has no effect on the bit position.

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by: issuing a programmed RESET instruction; depressing the START switch on the processor console; or occurrence of a power-up or power-down condition of the processor power supply.

The INIT signal clears the entire system; however, the INIT signal produced by a RESET instruction does not clear the processor. Clearing only the TMA11 Controller and the TS03 tape units can be accomplished by loading a 1 into bit 12 (Power Clear) of the command register (MTC).

NOTE

INIT and Power Clear deselect the current tape unit and select tape unit 0. Also, a rewind operation in progress continues to the load point.

Table 2-1
Standard Device Register Assignments

Register	Mnemonic*	Address
Status Register	MTS	772520
Command Register	MTC	772522
Byte Record Counter	MTBRC	772524
Current Memory Address Register	MTCMA	772526
Data Buffer Register	MTD	772530
TS03 Read Lines	MTRD	772532

*First two letters of mnemonic (MT) refer to magnetic tape control; the remaining letters represent the mnemonic of a specific register.

2.2.1 Status Register (MTS)

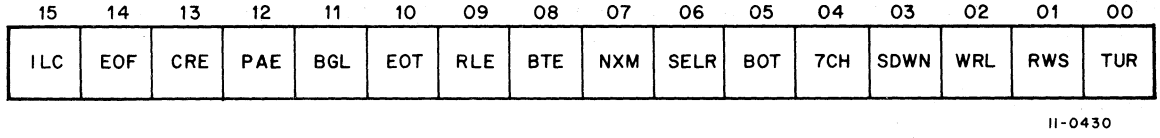

Figure 2-1 Status Register (MTS) Bit Assignments

Bit	Meaning and Operation
15	**ILC** – Illegal command bit. This bit is set whenever one of the following illegal commands occur:

1. Any DATO or DATOB transfer to the command register (MTC) during tape operation (CU RDY bit clear). The register cannot accept a new command while in the process of executing a previous command.

2. A write, write end-of-file, or write-with-extended-interrecord-gap (command register functions 2, 3, and 6, respectively), when the WRL (write lock) bit is set. Writing is inhibited with WRL set, and write commands are illegal.

3. Any command to a tape unit that has its SELR bit clear, because SELR clear indicates that the unit is not on-line.

4. Any time the SELR bit becomes 0 during any operation except off-line, it sets the ILC bit, because no command can be issued to a unit that is not on-line.

If any of the illegal commands listed in 1. through 3. above occur, the command is loaded into the command register.

In all of the above cases, the ILC bit and the ERR bit (bit 15 in the command register) are set simultaneously.

Cleared by INIT or by the GO pulse to the tape unit.

Bit	Meaning and Operation
14	**EOF** – End-of-file bit. An end-of-file (EOF) character is detected during a read, space forward, or space reverse operation. During the read or space forward operations, the EOF bit is set after the EOF and LRC characters are read. During a space reverse operation, the EOF bit is set after the LRC and EOF characters are read. The ERR bit (bit 15 in the command register) is set when the LRC character following the EOF character is detected. It is also set during WRITE EOF command. The EOF bit is set only by the TS03 logic; it is cleared by INIT or by the GO pulse to the tape unit. The EOF character is loaded into memory during read operations.
13	**CRE** – Cyclic redundancy error bit. A cyclic redundancy error can be detected during either a read or write operation. This check compares the CRC character written during a write or a write-with-extended-IRG operation with the CRC character generated during a read operation. If the two CRC characters are not the same, the CRCE from the tape unit becomes a 1, forcing the CRE bit to a 1. The ERR bit in the command register, however, is not set until the LRC character is detected. Cleared by INIT or by the GO pulse to the tape unit.
12	**PAE** – Parity error bit. When set, this bit indicates that a parity error exists. The PAE bit is the logical OR of both vertical and longitudinal parity errors. A vertical parity error is indicated on any character in a record; a longitudinal parity error occurs only after the LRC character is detected. A vertical parity error does not affect the transfer of data. In other words, the entire record is transferred to the tape during a write operation or transferred into memory during a read operation. Both vertical and longitudinal parity errors are detected during read, write, and write-with-extended-IRG operations. The longitudinal parity check is made on the entire record, including the CRC and LRC characters. A longitudinal parity error occurs when an odd number of 1s is detected on any channel in the record. A vertical parity error occurs when an even number of 1s is detected on any character, provided the PEVN bit (bit 11 in the command register) is clear, or if an odd number of 1s is detected when the PEVN bit is set. When a parity error occurs, PAE is set, and the ERR bit (bit 15 in the command register) is set after the LRC character has been detected. Cleared by INIT or by the GO pulse to the tape unit.

Bit	Meaning and Operation
11	**BGL** – Bus grant late bit. If the controller issues a request for the bus and does not receive a bus grant before it must issue another bus request for the following tape character, a bus grant late error occurs. This error condition is tested only for NPRs (non-processor requests). The BGL bit is set if an NPR bus request is not honored before the controller receives a WRS pulse for a write operation or an RDS pulse for a read operation. The BGL bit and the ERR bit (bit 15 in the MTC) are set simultaneously, halting the operation. If the BGL error occurred during a write or write-with-extended-IRG operation, the controller negates the WDR signal to the master tape unit, inhibiting the write operation. Cleared by INIT or by the GO pulse to the tape unit.
10	**EOT** – End-of-tape bit. The EOT bit is set as soon as the EOT marker is detected when the tape is moving in the forward direction. It is cleared as soon as the EOT marker is detected when the tape is moving in the reverse direction. The EOT is an error condition if the tape is moving forward. Therefore, when EOT is set, the ERR bit is also set when the LRC character is read. Cleared by tape transport head passing over EOT marker when tape is moving in the reverse direction.
09	**RLE** – Record length error bit. The record length error is tested only during read operations. An error is indicated as soon as the byte record counter (MTBRC) attempts to increment beyond 0. When a record length error occurs, the RLE bit is set, incrementation of the MTBRC and the current memory address register (MTCMA) ceases, and the ERR bit is set when the LRC character is read. The CU RDY (bit 07 of the command register) remains cleared until TUR (tape unit ready) asserts, at which time CU RDY is set. Cleared by INIT or by the GO pulse to the tape unit. If the exact record length is desired after the occurrence of a record length error, it can be found by setting the MTBRC to a value so large that an RLE is not generated and then re-reading the record. Record length can be derived by subtracting the current value of the MTBRC from its initial setting.

Bit	Meaning and Operation
08	**BTE/OPI** – Bad tape error/operation incomplete bit. A bad tape error occurs when a character is detected (RDS pulse) during a gap shutdown or settle down period for any tape function except rewind. During write, write EOF, or write-with-extended-IRG operation, a bad tape error sets both the BTE/OPI and ERR bits immediately on detecting the error. During both read and space forward or space reverse operations, the BTE/OPI bit is set immediately on detection of bad tape. During a read operation, the MTBRC increments continuously, and words are read into memory until the MTBRC overflows. During a space operation, the MTBRC stops incrementing as soon as BTE occurs. When BTE is discovered, the tape unit stops, regardless of the state of the MTBRC. Because it is not possible to artifically generate bad tape, bad tape may be indicated by setting the CU RDY bit prematurely, thereby producing the gap shutdown period while the data is still being read. The CU RDY bit is set by loading a 1 into bit 13 of the MTRD. If bit 13 of the MTRD is set during a record for either a read or write operation, a bad tape error indication occurs. Any initiated tape operation, other than a REWIND or OFF-LINE command, that does not detect an LRC character within 7 seconds results in setting the BTE/OPI bit. This 7-second time-out is called Operation Incomplete. Any legal size record with a legal size gap results in detection of an LRC character within 7 seconds. During a spacing operation, the OPI timer is restarted at each interrecord gap. When the 7-second time-out occurs, the tape unit in operation is RESET by CINIT. The BTE/OPI bit is set and, at TUR, the CU RDY bit is set. Cleared by INIT or GO.
07	**NXM** – Non-existent memory bit. This error condition occurs when the controller is bus master during NPR transfers and does not receive an SSYN response within 10 μs after asserting MSYN. The NXM bit and the ERR bit are set simultaneously, halting the operation. Cleared by INIT or by the GO pulse to the tape unit.
06	**SELR** – Select remote bit. The SELR bit is set when the tape unit has been properly selected. The SELR bit is 0 if the tape unit that is addressed does not exist (UNIT SELECT setting does not correspond to SEL bits), if the selected tape unit is off-line (ON LINE indicator extinguished), or if the tape unit power is off.
05	**BOT** – Beginning-of-tape bit. The BOT bit is set as soon as the BOT marker is detected. When BOT is set, it has no effect on the ERR bit. The BOT bit remains cleared whenever the BOT marker is not being read. This bit is set and cleared only by the TS03.

Bit	Meaning and Operation
04	**7CH** – 7-channel bit. This bit is always cleared because the TS03 is a 9-channel unit.
03	**SDWN** – Settle down bit. The settling down period is provided to allow the tape to fully stop prior to starting a new operation. This settling down period sets the SDWN bit. When the tape unit stops, SDWN is cleared and the tape unit ready (TUR) bit is set. During a tape reverse operation (this does not include rewind operations), the gap shutdown period begins immediately after the first gap encountered after spacing over a record.
02	**WRL** – Write lock bit. The write lock bit is under control of the tape transport. When set, it prevents the controller from writing information on the tape.
01	**RWS** – Rewind status bit. This bit is under control of the tape unit. It is set at the start of a rewind operation and clears as soon as the rewind sequence is complete.
00	**TUR** – Tape unit ready bit. This bit is under control of the tape transport. Whenever the selected tape unit is being used (such as rewind), this bit is cleared. When the tape unit is stopped and ready to receive a new command, the tape transport sets the TUR bit.

NOTE
Status register bits 00-03 and 05 are cleared or set by the tape transport, not the controller.

2.2.2 Command Register (MTC)

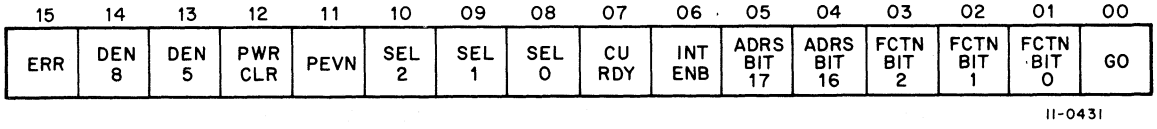

Figure 2-2 Command Register (MTC) Bit Assignments

Bit	Meaning and Operation
15	**ERR** – Error bit. Indicates an error condition that is the inclusive OR of all error conditions (bits 15 – 07 in the status register, MTS). Causes an interrupt if enabled (see bit 06). The ERR bit is not set for some errors until the longitudinal redundancy check (LRC) character is read, in order to allow the current operation to be completed. Specific error conditions are described in the status register bit assignments (Figure 2-1). When ERR is set, it sets bit 07 (CU RDY) when the tape unit asserts TUR. Cleared by INIT or by the next GO command (bit 00).

Bit	Meaning and Operation

14 **DEN 8** – Density bit. This bit, in conjunction with bit 13, selects the bit packing density of the tape. These combinations are shown below.

Bit 14 (DEN 8)	Bit 13 (DEN 5)	Density (bits/inch)	
0	0	200	7-channel tape (See Note)
0	1	556	
1	0	800	
1	1	800	9-channel tape (TS03)

NOTE

TS03 ignores bits 14 and 13; it always operates at 800 bpi, 9-channel.

13 **DEN 5** – Density bit. This bit, in conjunction with bit 14, selects the bit packing density of the tape. See bit 14 for combinations.

12 **PWR CLR** – Power clear bit. When a 1 is loaded into this bit position, it clears the controller logic and all tape units. This bit becomes a 1 for μs during a processor DATO cycle, provided the corresponding bit on the bus is a 1. Always read by processor as a 0.

11 **PEVN** – Even parity bit. This bit is set whenever the selected tape unit is to write or read even vertical parity on or from the tape. The bit is 0 whenever the selected tape unit is to write or read odd vertical parity on or from the tape.

A search for a parity error is made whenever the tape moves. The controller ignores parity errors during space forward, space reverse, or rewind operations.

Cleared by INIT or by loading with a 0.

10–08 **SEL** – Tape unit select bits. These three unit select bits specify the number of the tape unit that is to function as the unit under program control. These three bits (SEL 2, SEL 1, and SEL 0) are set or cleared to represent an octal code that corresponds to the unit number of the tape unit to be used. The TS03 master tape transport recognizes octal codes 000 and 001 only.

Cleared by INIT or by loading with a 0.

07 **CU RDY** – Controller ready bit. When set, indicates that the TMA11 Controller is ready to receive a new command. This bit is set at the end of a tape operation (indicating that a new operation can be started) and is cleared at the beginning of a tape operation (indicating that the controller is not ready for new commands). Refer to Paragraph 2.4.1 for CU RDY operation during a rewind sequence.

This bit is also set (indicating CU RDY) whenever ILC (bit 15 of MTS) is set or whenever INIT is generated.

Bit	Meaning and Operation
06	**INT ENB** – Interrupt enable bit. This bit, when set, allows an interrupt to occur, provided either CU RDY (bit 07) or ILC (bit 15 of MTS) is set. With INT ENB set, a REWIND command can cause two interrupts – one at initiation and one at completion. An interrupt also occurs whenever an instruction sets the INT ENB bit but does not set the GO bit (bit 00). Interrupts are described in Paragraph 2.3. Cleared by INIT or by loading with a 0.
05	**ADRS BIT 17** – Extended bus address bit 17. Used to specify address line 17 in direct memory transfers. Increments with the current memory address register (MTCMA). Cleared by INIT.
04	**ADRS BIT 16** – Extended bus address bit 16. Function is the same as ADRS BIT 17 (bit 05 above).
03–01	**FUNCTION** – These bits specify a command to be performed by the selected tape unit. These functions are:

	Function Bits			
Octal No.	03	02	01	Function
0	0	0	0	Off-line
1	0	0	1	Read
2	0	1	0	Write
3	0	1	1	Write end-of-file
4	1	0	0	Space forward
5	1	0	1	Space reverse
6	1	1	0	Write-with-extended-IRG
7	1	1	1	Rewind

All function bits cleared by INIT. Table 3-1 describes each function.

00	**GO** – Loaded with a 1 from the bus to initiate the function selected. Clears CU RDY bit. Cleared when GO pulse is sent to tape transport. Normal time duration of bit is 1 μs, but this time may extend to as long as several minutes when the bit is loaded for a tape unit in the process of rewinding. Also cleared by INIT or whenever ILC in the status register is set.

2.2.3 Byte Record Counter (MTBRC)

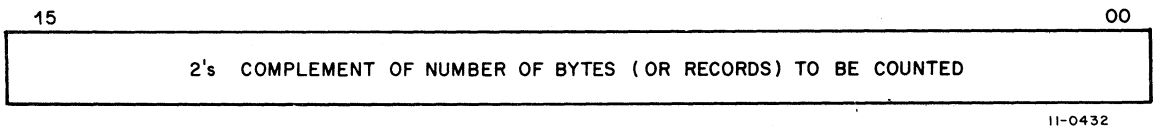

Figure 2-3 Byte Record Counter (MTBRC) Bit Assignments

Bit	Meaning and Operation
15–00	Contains the 2's complement of the number of bytes or records to be transferred. The desired value is loaded by the program on a processor DATO. Cleared by INIT. Increment by 1 after each memory access.

The byte record counter (MTBRC) is a 16-bit binary counter used to count bytes in a read or write operation and used to count records in space forward or reverse operations.

When used in a write or write-with-extended-IRG operation, this register is set by the program to the 2's complement of the number of bytes to be written on the tape. After the last byte of the record has been strobed from memory, the MTBRC becomes 0. Thus, when the next write strobe signal is received from the master tape transport, the controller lowers the write data ready line to indicate to the master transport that there are no more data characters in the record.

When used in a read operation, the MTBRC is set to a number equal to or greater than the 2's complement of the number of words to be loaded into memory. A record length error, which occurs for long records only, occurs whenever a read pulse is generated after the MTBRC is at 0. Neither the CRC or LRC character is loaded into memory during a read operation, although both characters are checked for parity errors.

When used in a space forward or space reverse operation, the MTBRC is loaded with the 2's complement of the number of *records* to be spaced. The counter is incremented by 1 at LRC time, regardless of tape direction.

2.2.4 Current Memory Address Register (MTCMA)

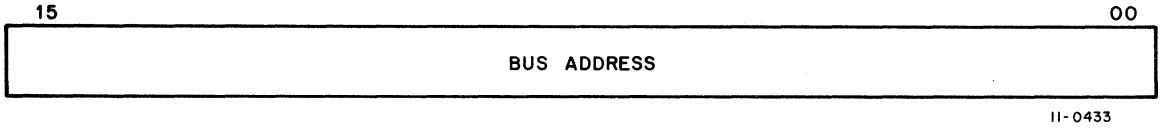

Figure 2-4 Current Memory Address Register (MTCMA) Bit Assignments

Bit	Meaning and Operation
15–01	These bits specify the bus or memory address to or from which data is to be transferred during write or read operations. Only bits 01–15 of the MTCMA are accessible by the program, although bits 00–15 participate in NPR transfers. The MTCMA contains 16 of the possible 18 memory address bits. The remaining two bits (16 and 17) are part of the command register.

Before issuing a command, the program loads the MTCMA with the memory address that is to receive the first byte of data (read operation) or with the memory address from which the first byte is to be taken (write operation). After each memory access (read or write), the MTCMA is immediately incremented by 1 (the next byte boundary). Therefore, at any given time, the MTCMA points to the next memory byte address that is to be accessed. On completion of the record transfer, the MTCMA points to the address plus 1 of the last character in the record.

Bit	Meaning and Operation
15–01 (Cont)	If a bus grant late (BGL) or non-existent memory (NXM) error occurs, the MTCMA contains the address of the location in which the failure occurred. If an 18-bit memory address is required, the program loads the appropriate address into bits 01–15 of the MTCMA and into extended address bits 16 and 17 of the command register. The extended address bits are a logical extension to the MTCMA register and participate in any required incrementation.

2.2.5 Data Buffer Register (MTD)

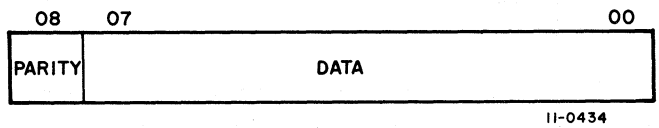

Figure 2-5 Data Buffer Register (MTD) Bit Assignments

Bit	Meaning and Operation
15–09 (not shown)	Correspond to bits 07–01 respectively on a processor DATI cycle (e.g., bit 15 = bit 7, bit 14 = bit 6).
08	Corresponds to the parity bit on the magnetic tape. During a processor read operation, this bit is stored in memory; during NPR operations, this bit is read by the controller but not loaded into memory. During operation of a nine-channel tape unit, this bit is valid only after the CRC character has been read, provided bit 14 of the MTRD is a 1. **NOTE** **The parity bit is generated by the TS03 master tape transport, not by the controller. However, the polarity of the parity bit (odd or even) is determined by the PEVN bit in the command register.**
07–00	During read operations, these bits are used for temporary storage of characters read from tape prior to loading into memory. During write operations, these bits are used for temporary storage of data from memory before writing on tape. During read operations, the LRC character enters the data buffer when bit 14 of the address location for the TS03 read lines is a 1; the LRC character is prevented from entering the data buffer when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains an LRC character (if bit 14 is a 1) or a CRC character (if bit 14 is a 0). After reading an EOF character, the data buffer contains either all 0s (bit 14 is a 1) or the EOF character (bit 14 is a 0). The data buffer can store only bytes; therefore, two bus cycles are required to transfer a word. During NPR operation, the data bits are written into or read from alternate low and high byte positions. The relationship between tape characters and high and low memory byte characters is shown in Figure 2-6.

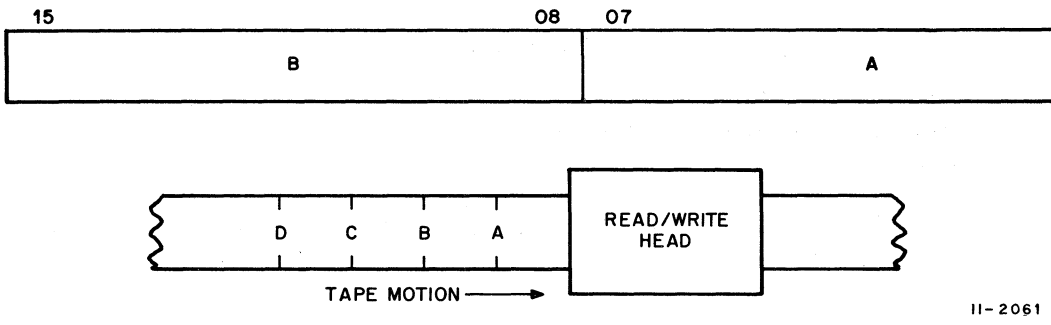

Figure 2-6 Relationship Between Tape Characters and Memory Byte Characters

2.2.6 TS03 Read Lines (MTRD)

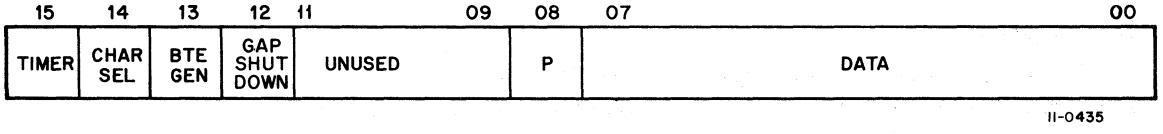

Figure 2-7 TS03 Read Line (MTRD) Bit Assignments

Bit	Meaning and Operation
15	**TIMER** – The timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. The timer signal is a 100 μs signal with a 50 percent duty cycle and is generated by the controller. It is read as bit 15 in the memory location reserved for the TS03 read data lines. This is a read-only bit. See Paragraph 5.9.4 in Part I of this manual for the timer adjustment procedure.
14	**CHAR SEL** – This bit is used to select the last character of a record that is to be loaded into the data buffer. This is a read/write bit. Selection is as follows: Set – LRC character Clear – CRC character
13	**BTE GEN** – Bad tape error generator bit. Bad tape cannot be artifically generated. When set, this bit sets the CU RDY bit. With CU RDY set, a premature gap shutdown is generated, which produces a bad tape error indication when data is read during this period. This is a write-only bit.
12	**GAP SHUTDOWN** – When set, indicates a gap shutdown period. This is a read-only bit.
11–09	Unused.
08	**PARITY** – Corresponds to the parity bit read from the tape by the TS03 tape transport. Used in conjunction with bits 07–00 to indicate a longitudinal parity error. After a read or write operation, bits 08–00 should all be 0. If one or more of these bits remains a 1 after the operation is complete, it indicates a longitudinal parity error. The bit position containing the 1 indicates the tape channel containing the error. This is a read-only bit.

Bit	Meaning and Operation
07–00	**DATA** – These bit positions contain information read from the magnetic tape transport. After these positions are read by the processor, all bit positions clear unless a parity error exists. Bits 07–00 in the read lines correspond to tape channels 00–07, respectively. These are read-only bits.

2.3 INTERRUPTS

The TMA11 Controller uses NPR or BR interrupts to gain control of the bus in order to perform data transfers or to cause a vectored interrupt, thereby causing a branch to a handling routine. The NPR requests are used for direct memory access whenever it is desired to transfer data between memory and the data buffer register without processor intervention. The BR requests are made when processor servicing is required for completed operations or error conditions.

2.3.1 NPR Requests

The TMA11 Controller issues an NPR request whenever it is necessary to transfer data between memory and the data buffer register. During a read operation, the direction of transfer is from the data buffer to the core memory. The RDS pulse (read strobe from master tape transport to controller), which is used to strobe data from the tape transport into the data buffer register, generates the NPR request. When the request is granted, the TMA11 Controller performs a DATOB bus cycle and transfers information from the data buffer into memory.

During a write (or write-with-extended-IRG) operation, the NPR request is generated by the write strobe (WRS) pulse from the transport. When the request is granted, the controller performs a DATI bus cycle and transfers a byte from core memory into the data buffer register.

During both read and write operations, the address in memory that data is read from or loaded into is determined by the value in the current memory address register (MTCMA).

2.3.2 BR Requests

A BR interrupt can occur only if the interrupt enable (INT ENB) bit in the command register is set. With INT ENB set, setting the CU RDY bit in the command register or completing a rewind operation initiates an interrupt request. When CU RDY is set, it indicates that the controller is ready to perform another command.

When ERR is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause the program to branch to an error handling routine.

If a function command is issued with the GO bit cleared and INT ENB set, an interrupt is initiated.

If the selected tape unit (as indicated by the SEL bits in the command register) completes the rewind operation before a new command to that unit is received and INT ENB is set, an interrupt is initiated.

If the interrupt is enabled (INT ENB set) and selection of the tape unit is not changed (as indicated by the SEL bits), then a rewind command causes two interrupts: an interrupt when the rewind function begins, and an interrupt when the tape unit completes the rewind function. If, however, the tape unit is already at the BOT marker when rewind is issued, only one interrupt occurs.

The interrupt priority level is BR5, and the interrupt vector address is 224. Note that the priority level can be changed by the priority chip on the G736 module, and the vector address can be changed by jumpers on the M7821 Interrupt Control. However, any DEC programs or other software referring to the standard level or address must also be changed if the jumpers are changed.

2.4 PROGRAMMING NOTES

In normal programming practice, no attempt should be made to modify one record in the middle of a file. This practice could result in overwriting the boundary of the record and destroying part of the next record. Also, a read operation should never directly follow a write operation without at least one intervening tape move operation. This prevents generating a BTE/OPI if the previous operation involved the last record on the tape. If it is desired to read a record that was just written, a space reverse command should be issued before the read command. New commands are issued only when CU RDY is set, which is true after interrupts.

Attempting to write an all-0 character with even parity causes the 0 character to be converted to a tape character of 20. When reading this character from tape, a 20 is read instead of a 0.

ASCII standards provide for a 25-ft trailer following the end-of-tape marker. This allows approximately 10 ft of writing space after passing EOT. Care should be taken when attempting to write past the EOT marker if the operator is not familiar with the tape that he is working with, because after a tape has been used, the reflective markers are often changed, possibly decreasing the length of the standard 25-ft trailer.

A backspace or REWIND command issued while the tape is at the load point will cause an immediate interrupt provided the INT ENB bit is set.

2.4.1 Rewind Operation

Assume transport 0 is to be rewound. The command to rewind transport 0 is issued to the controller. At this time, the master tape unit asserts bit 01 (RWS) in the status register. If bit 06 (INT ENB) in the command register was set at the start of the rewind operation, an interrupt occurs from the TMA11 Controller as soon as bit 07 (CU RDY) of the command register has been set by RWS. This informs the program that the controller is ready to accept a new command. By testing bit 01 (RWS) in the status register, the program can determine if this interrupt was issued as a result of transport 0 completing its rewind operation or just beginning it.

Transport 0, still moving in the reverse direction, passes over the reflective marker, reverses its direction, and proceeds in the forward direction to the load point. Upon sensing the reflective marker while proceeding in the forward direction, transport 0 halts tape motion, asserts bit 03 (SDWN), allowing the tape to fully stop, and then sets bit 00 (TUR) in the status register.

An interrupt is issued coincident with bit 00 (TUR) being asserted in the status register, providing the following conditions have been met.

1. Bit 06 (INT ENB) in the command register is set.

2. The drive has not been deselected by changing the status of bits 10–08 in the command register since issuing the REWIND command.

If multiple transports are used, it is not necessary to wait for a REWIND command to be completed on one transport before switching to another. After a REWIND is issued, another transport can be switched to as soon as RWS is set.

When operations on the second transport have been completed, a switch to the rewinding transport can be made as soon as SDWN or TUR is true on the second transport (so the status bits will be from the rewinding unit). Only the unit select bits in the command register have to be changed to the unit that is rewinding to get its status. If the rewind is complete when the unit is selected, TUR is set in the status register. If the RWS bit is still set, the software can either work on another transport or wait until the rewind is completed. A REWIND command may take from 3 to 5 minutes to complete.

2.4.2 New Drive Selection

Figure 2-8 is a flowchart for new drive selection.

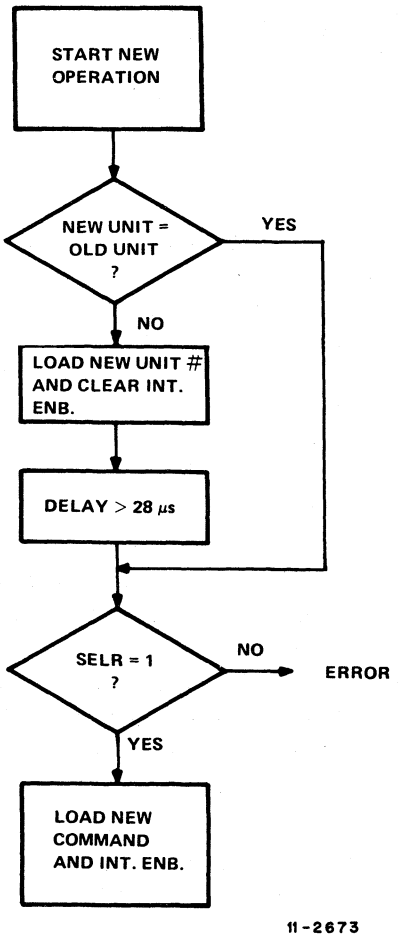

Figure 2-8 New Drive Selection Flowchart

2.4.3 Error Handling

2.4.3.1 Write Operations

Mnemonic	Error	Correction
ILC	Illegal command	1. If SELR (bit 06 of MTS) is not set to a 1 or WRL (bit 02 of MTS) is set to a 1, then operator intervention is required to ensure that the drive to be used is properly selected and is not write locked. 2. If SELR (bit 06 of MTS) is set to a 1 and WRL (bit 02 of MTS) is not set to a 1, then a command has been issued while CU RDY (bit 07 of MTC) was cleared. Try the operation again, ensuring that CU RDY is set before issuing a new command.
EOF	End-of-file	N/A
CRE	Cyclic redundancy error	Backspace and try operation again with extended IRG.
PAE	Parity error	Backspace and try operation again with extended IRG.
BGL	Bus grant late	Backspace and try operation N times.
EOT	End-of-tape	The reflective marker signifying the end of tape has been passed. Operations past this point are not illegal; however, they are not recommended unless the programmer is familiar with the tape being used and is knowledgable about the length of tape existing past the EOT marker. Conducting any write operations past the EOT marker leaves the programmer open to the possibility of running the tape off of the reel.
RLE	Record length error	N/A
BTE	Bad tape error/operation incomplete	Regain a known tape position and try the operation again with extended IRG. **NOTE** **A known tape position refers to BOT, header records, or EOF marks.**
NXM	Non-existent memory	Resolve the memory discrepancy and try the operation again.

2.4.3.2 Read Operations

Mnemonic	Error	Correction
ILC	Illegal command	1. If SELR (bit 06 of MTS) is not set, then operator intervention is required to ensure that the drive to be used is properly selected. 2. If SELR (bit 06 of MTS) is set, then a command has been issued while CU RDY (bit 07 of MTC) was cleared. Try the operation again ensuring that CU RDY is set prior to issuing the new command.
EOF	End-of-file	The characters signifying the end of a file have been read.
CRE	Cyclic redundancy error	Backspace and try the operation N times.
PAE	Parity error	Backspace and try the operation N times.
BGL	Bus grant late	Backspace and try the operation N times.
EOT	End of tape	The reflective marker signifying the end of tape has been passed. Continue only if it is certain that an EOF mark exists after the EOT marker, or the tape will run off of the reel.
RLE	Record length error	Reset the MTBRC to a value that is equal to or greater than the number of bytes in the record, backspace, and try the operation again.
BTE/OPI	Bad tape error/operation incomplete	Regain a known tape position and try the operation again. If, after doing so, the condition still persists, the data from the failing point to the next known tape position is lost.
NXM	Non-existent memory	Resolve the memory location discrepancy and try the operation again.

2.4.3.3 Write End-of-File Operation

Mnemonic	Error	Correction
BTE/OPI	Bad tape error/operation incomplete	Regain a known tape position and try the operation again.

2.4.3.4 Spacing Operations

Mnemonic	Error	Correction
ILC	Illegal command	Same as read operation.
EOF	End of file	The characters signifying the end of a file have been read. Detection of the EOF marks stops a spacing operation even if the MTBRC is not equal to zero.
EOT	End of tape	Same as read operation.
BTE/OPI	Bad tape error/operation incomplete	Regain a known tape position and try N times.

2.4.3.5 Write-With-Extended-IRG Operation – Same as write operation.

2.4.3.6 Rewind Operation – Once a rewind operation is started, it continues until complete, regardless of errors or unit deselection.

2.5 PROGRAM EXAMPLE

The following program example is used to write a 1000-byte record, backspace, read the record, and compare data.

```
        172520                  MTS=172520                      ;STATUS REGISTER
        172522                  MTC=172522                      ;COMMAND REGISTER
        172524                  MTBRC=172524                    ;BYTE RECORD COUNTER
        172526                  MTCMA=172526                    ;CURRENT MEMORY ADDRESS REGISTER

        001000                          .=1000
                                ;WRITE RECORD
001000  005067  171516                  CLR     MTC             ;CLEAR COMMAND REGISTER, ALSO SELECTS UNIT #0
001004  105767  171512                  TSTB    MTC             ;IS CONTROL UNIT READY?
001010  100375                          BPL     .-4             ;NO, WAIT
001012  006067  171502                  ROR     MTS             ;IS TAPE UNIT READY?
001016  103375                          BCC     .-4             ;NO, WAIT
001020  012767  001152  171520          MOV     #WBUF,MTCMA     ;INITIALIZE MTCMA WITH BUFFER AREA TO BE WRITTEN
001026  012767  176030  171470          MOV     #-1000.,MTBRC   ;INITIALIZE BYTE COUNT
001034  012767  060005  171460          MOV     #60005,MTC      ;SELECT UNIT #0, 800 BPI, WRITE, ISSUE GO
001042  105767  171454                  TSTB    MTC             ;IS CONTROL UNIT READY, INDICATING COMPLETION OF WRITE?
001046  100375                          BPL     .-4             ;NO, WAIT
                                ;RECORD WRITTEN, NOW BACKSPACE
001050  012767  177777  171446          MOV     #-1,MTBRC       ;INITIALIZE BYTE COUNT TO BACKSPACE 1 RECORD
001056  012767  060013  171436          MOV     #60013,MTC      ;ISSUE BACKSPACE COMMAND
001064  105767  171432                  TSTB    MTC             ;IS CONTROL UNIT READY, INDICATING COMPLETION OF BACKSPACE?
001070  100375                          BPL     .-4             ;NO, WAIT
                                ;NOW READ RECORD
001072  012767  003120  171426          MOV     #RBUF,MTCMA     ;INITIALIZE MTCMA WITH BUFFER AREA TO BE READ INTO
001100  012767  176030  171416          MOV     #-1000.,MTBRC   ;INITIALIZE BYTE COUNT
001106  012767  060003  171406          MOV     #60003,MTC      ;SELECT UNIT #0, 800 BPI, READ, ISSUE GO
001114  105767  171402                  TSTB    MTC             ;IS CONTROL UNIT READY, INDICATING COMPLETION OF READ?
001120  100375                          BPL     .-4             ;NO, WAIT
                                ;COMPARE DATA READ WITH DATA WRITTEN
001122  012700  001152                  MOV     #WBUF,%0        ;USE REGISTERS 0,1 AS BUFFER POINTERS FOR COMPARISON
001126  012701  003120                  MOV     #RBUF,%1
001132  022021                  C1:     CMP     (0)+,(1)+       ;IS DATA WRITTEN = DATA READ?
001134  001421                          BEQ     .+4             ;YES
001136  000000                          HALT                    ;NO, HAVE DATA ERROR
001140  020027  003120                  CMP     %3,#WBUF+1000.  ;FINISHED COMPARISON OF BUFFER?
001144  002772                          BLT     C1              ;NO
001146  000000                          HALT                    ;YES, EXAMPLE COMPLETED
001150  000000                  WBUF:   0                       ;WRITE BUFFER BEGINS HERE
        003120                          .=WBUF+1000.
003120  000000                  RBUF:   0                       ;READ BUFFER BEGINS HERE
        000001                                  .END
```

CHAPTER 3
THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a detailed description of the TMA11 Controller and consists of three major parts: functional description of overall controller operation, block diagram description of major components, and detailed description covering controller logic circuits. The discussions in this chapter are supported by a complete set of engineering drawings located in a companion volume entitled *TMA11 DECmagtape System, Engineering Drawings.*

The TMA11 Controller may be divided into six functional areas: selection logic, bus control logic, register logic, tape control logic, read/write logic, and error logic. Parity logic is part of the Master Tape Transport and is, therefore, only covered in general in subsequent discussions. The purpose of each of the controller functional units is as follows:

Selection Logic — Determines if the controller has been selected as a bus slave device, and what type of operation (read or write) has been selected. Permits selection of one of six internal registers for use and determines if the register is to perform an input or output operation.

Bus Control Logic — Permits the controller to gain bus control either by means of an NPR for transferring data or by means of a programmed interrupt to request service by the program because an error condition exists, because the controller is ready to perform a new operation, or because the controller is ready to make a direct memory access transfer (NPR transfer).

Register Logic — Six internal registers, addressable by the program, provide data transfer functions, command and control functions, and status monitoring functions for the TMA11 Controller.

Tape Control Logic — Controls selection of tape unit, direction of tape travel (forward, reverse), and function to be performed such as rewind, write, read, space forward, and space reverse.

Read/Write Logic — Controls assembly, disassembly, and transfer of data between the magnetic tape and the Unibus. Counts number of words in transfer and keeps track of current bus address.

Error Logic — Monitors controller operation and provides an indication of any error condition that arises. Stops the operation and issues an interrupt request for most error conditions.

3.2 FUNCTIONAL DESCRIPTION

The prime function of the TMA11 Controller is to control transfers of information so that digital data can either be taken from the bus and recorded on magnetic tape (write operation) or read from the magnetic tape and transferred to the bus for use by another device such as memory (read operation). In addition, the controller performs tape transport selection, tape positioning, tape formatting, and system monitoring functions.

The controller contains a command register, which allows the program to specify desired operations by loading control data (transport selection, packing density, function, etc.) into the register. System status information (end-of-tape, errors, tape unit ready, etc.) is loaded into a status register, which can be read from the bus.

The TMA11 Controller controls two magnetic tape transports. Although both tape units may be simultaneously rewinding, data transfers may take place with only one transport at any given time. The basic functions performed by the controller are: off-line, read, write, write EOF, space forward, space reverse, write-with-extended-IRG, and rewind. Each of these functions is briefly described in Table 3-1.

Table 3-1
Controller Functions

Number	Function	Description
0	Off-Line	The off-line function is used when it is desired to return control to the tape transport so that tape can be rewound, reels changed, etc. without using processor time. The off-line function places the selected tape transport in the off-line (local) mode and causes it to begin a rewind operation. The TMA11 Controller cannot write on or read from the magnetic tape when the off-line function is used.
1	Read	This function permits reading from the magnetic tape. During the read operation, the data portion of the record is loaded into the controller data buffer for transfer to the memory. The LRC and CRC characters are read but not transferred into memory.
2	Write	This function permits writing on the magnetic tape. During the write operation, data from the bus is loaded into the controller data buffer register. The controller then transfers the data to the tape transport write heads. The necessary LRC and CRC characters are generated by the master transport and written on the tape following the data. The write function advances the tape forward one record.
3	Write EOF	This function writes an end-of-file (EOF) mark on the tape. When selected, this function erases a 3-in. segment of tape prior to writing the first character. The EOF mark and the associated LRC character are considered one record.

Table 3-1 (Cont)
Controller Functions

Number	Function	Description
4	Space Forward	This function is used to skip over a number of records to find a specific record on the tape. When selected, the space forward function causes the tape transport to advance forward a specified number of records. The number of records is determined by the value in the byte record counter. This value is loaded into the byte record counter by the program. Space forward is used for tape positioning only and, therefore, does not affect information stored on the tape or in memory.
5	Space Reverse	This function is identical to the space forward function except the tape moves in the reverse rather than in the forward direction.
6	Write-with-Extended-IRG	This function is identical to the write function except that a 3-in. segment of tape is erased before writing the first character.
7	Rewind	This function is used for rewinding the tape on the feed reel so that the tape can either be unloaded from the transport or operation can start at the beginning of the tape. When this function is used, the tape moves in the reverse direction, at a much higher speed (150 in./sec) than for other functions, until the beginning-of-tape (BOT) marker is detected. Rewind is used for tape positioning only and has no effect on information stored on the tape or in the memory.

Data transfers are controlled by a byte record counter (MTBRC) and a current memory address register (MTCMA). The program loads the byte record counter with the 2's complement of the desired number of data transfers. The counter is incremented before each transfer; therefore, the byte transfer that causes the byte count overflow (MTBRC becomes zero) is the last transfer to take place. The byte counter is also used to count the number of records during space forward and space reverse operations.

The current memory address register is also incremented before each transfer and, therefore, always points to the next higher address than the one most recently accessed. Thus, when the entire record is transferred, the register contains the address plus 1 of the last character in the record. For certain error conditions, the register contains the address of the location in which the failure occurred.

During read operations, the controller assembles bytes from successive characters read from the tape channels. The eight data bits are assembled in a data buffer register for temporary storage. The parity bit is read but not loaded into memory. When the byte is assembled, it is placed on the bus for transfer to memory. If an NPR transfer is used, bytes from the data buffer are alternately stored into the low and high byte portions of memory.

Either the CRC character or the LRC character at the end of a record is stored in the data buffer, depending on the state of bit 14 in the MTRD. If this bit is 0, the CRC character is loaded into the data buffer and can be used for error detection. If the bit is 1, then the data buffer contains the LRC character at the end of the record.

During write operations, the controller disassembles eight-bit bytes from the bus and distributes the bits so that they can be recorded on successive frames of the tape. All tapes are written at a density of 800 bpi. There are three possible write functions: write, write-with-extended-IRG, and write end-of-file (EOF) mark.

When a write function is selected, the program loads the byte record counter with the 2's complement of the number of bytes to be written in the record. Although the parity bit, which is also loaded into the buffer, is generated by the master tape transport, the polarity of the bit is determined by the controller so that either odd binary or even BCD parity can be selected. When parity is generated and the buffer is loaded, the controller transmits the byte to the master tape transport, which places the byte on the read/write heads of the selected slave transport so that data can be written on the magnetic tape.

The write-with-extended-IRG function is identical to the write function except that a 3-in. gap, rather than the normal gap, is used between records. When this function is selected, a 3-in. segment of tape is erased before writing begins.

The write end-of-file (EOF) function is used to indicate that a block of records is complete. When this function is selected, a special EOF character is written on the tape followed by an LRC character. These two characters constitute a complete record. This command causes a 3-in. gap to be placed before the EOF mark. The XIRG command must be absent to have this gap written.

System monitoring functions are performed by the controller status register. The 16 bits in this register retain error and tape status information. Some status data is combined, such as vertical and longitudinal parity errors, or has a combined meaning, such as illegal command, for optimum use of the available bits. The status register only monitors the tape transport selected by the command register; therefore, other units that may be rewinding do not interrupt the system when ready for data.

The following paragraphs discuss parity, gap shutdown, and function commands.

3.2.1 Parity

All parity characters are generated and read by the logic in the master tape transport rather than the controller. However, a brief description of parity is included in this chapter, because an understanding of the parity function is necessary for proper understanding of controller operation.

Whenever any command is issued that moves the tape forward, the master tape transport transmits a CRC strobe (CRCS) pulse and an LRCS at the end of each record.

During any write operation, the controller sends a write data ready (WDR) level to the master tape unit for each character in the record to indicate that the controller is ready to transmit data to the transport. The master tape transport then issues a write strobe (WRS) pulse that strobes the character from the controller data buffer register into the selected tape unit for writing on the tape.

When the last WRS pulse causes the BYTE RECORD COUNTER register to overflow, the controller lowers the WDR level and the master tape transport writes the CRC character and then the LRC character on the tape.

Whenever a slave tape transport is handling the magnetic tape being read or written, the control signals are still generated by the master tape transport, and the necessary characters transferred from the master to the slave at the appropriate time.

The parity bit can be written in even or odd parity. If the master tape transport is writing even parity, then the parity bit is set or cleared so that the total number of ones in the character is even. If odd parity is used, then the parity bit is set or cleared so that the total number of ones in a character is odd. The type of parity to be used (odd or even) is determined by the PEVN bit in the controller command register.

A longitudinal redundancy check (LRC) is also performed. The master tape transport writes an LRC character at the end of each data record. The bits in this character may be either 1s or 0s. The character is written in such a manner that the total number of bits in a channel (including the LRC character) is even.

In addition to vertical and longitudinal parity checks, the tape format includes a cyclic redundancy check (CRC), which checks the total number of data characters within a record or block. The vertical parity of the CRC character is odd if the number of data characters within the block is even, and is even if the number of data characters is odd.

The CRC character is generated by a nine-bit register in the master tape transport. All bits in a data character are exclusive-ORed into this register, which shifts one position between each character transfer. If shifting causes a 1 in the register bit corresponding to tape channel P, then the bits representing tape channels 2, 3, 4, and 5 are inverted. After the last data character is read, the register shifts a final time. At this point, all bit positions except those representing tape channels 2 and 4 are inverted. The register now contains the CRC character, which is written on the tape.

The values described above are related to the physical location of the read/write heads as shown below.

		Most Significant Bit							**Least Significant Bit**
Value of CRC Register Bit	P	0	1	2	3	4	5	6	7
Track No.	4	7	6	5	3	9	1	8	2

3.2.2 Gap Shutdown

The master tape transport employs a gap shutdown period to ensure a blank gap of tape between records. As soon as the master transport reads the LRC character, it times through the gap shutdown period and then sends a stop command to the selected slave transport.

On receiving a stop command, the selected transport enters a settling down (SDWN) period, which is the time between the stop command and the actual stopping of the tape. When the transport stops, it enters an idle period at which time the tape unit ready (TUR) bit is set to indicate that the transport is now ready to accept a function command.

3.2.3 Function Commands

The program selects the specific function to be performed by setting or clearing appropriate function bits in the command register. When the program sets the GO bit in the command register, the operation defined by the selected function occurs. Both the control unit ready (CU RDY) and tape unit ready (TUR) bits are cleared to indicate that the controller and selected tape transport are currently engaged in an operation and cannot accept a new command until the current operation is completed.

When the off-line function is selected, the tape unit goes off-line and then rewinds to the beginning-of-tape (BOT) marker. As soon as the off-line command is given, both the CU RDY and TUR bits are cleared, thereby preventing the controller and transport from accepting a new command. The master tape transport then clears the select remote (SELR) bit in the status register, indicating to the program that the selected transport is now off-line.

When a tape reverse operation (not rewind) is selected, the master tape transport enters the gap shutdown period immediately after reading the first data character.

During a write function (write, write EOF, and write-with-extended-IRG), the CU RDY bit is set when TUR asserts. For write EOF and write-with-extended-IRG functions, a 3-in. gap is erased prior to writing the required data characters.

A write EOF function causes a character that indicates a block of data is complete to be written on the tape. This function writes an EOF character followed by an LRC character. These two characters constitute one record. In an EOF record (Figure 3-1), the EOF character and the LRC character are identical. The EOF character is an octal 23.

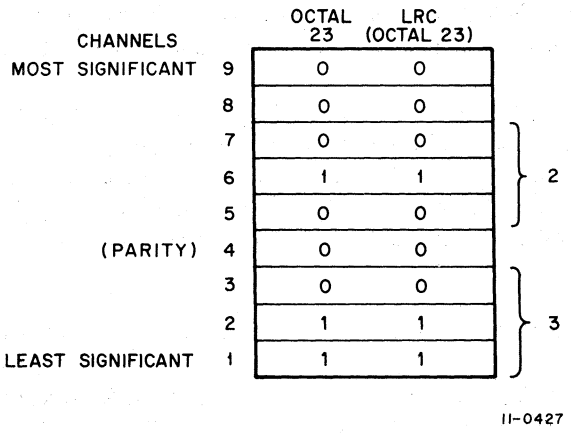

Figure 3-1 EOF Record

3.3 SYSTEM RELATIONSHIP

Figure 3-2 is a simplified block diagram of the TMA11-M DECmagtape System, showing the relationship of the TMA11 Controller to the TS03 Transports and to PDP-11 system components. Note that all communication between the controller and the transports is handled by the master tape transport. Communication between the controller and other PDP-11 devices is by means of the Unibus.

3.4 ADDRESS SELECTION

The TMA11 Controller selection logic decodes the address on the bus lines to determine if the controller has been selected for use. Unique addresses are assigned to each of the six registers in the controller and manipulation of these registers determines whether information is to be written on or read from the tape, or if some other control function is to be performed.

The TMA11 Controller consists basically of six registers (or bus addresses). In addition to decoding the incoming address, the selection logic controls the information flow between the Unibus and the controller registers. The logic produces SELECT line and gating IN or OUT signals, which determine the register to be used and the function to be performed (i.e., input or output).

The selection logic consists of an M105 Address Selector module and register select logic (M797 module).

3.4.1 Address Selector Module

The M105 Address Selector module (Drawing TMA11-0-19) decodes the address information from the bus to provide the gating and select line signals that activate appropriate TMA11 Controller logic circuits for the selected register. The M105 module jumpers are arranged so that the module responds only to the standard device register addresses 772520 through 772532. Although these addresses have been selected by DEC as the standard assignments for the TMA11 Controller, the user may change the jumpers to any address desired. However, any MAINDEC program (or other software) that references the TMA11 standard address assignments must be modified if other than the standard assignments are used.

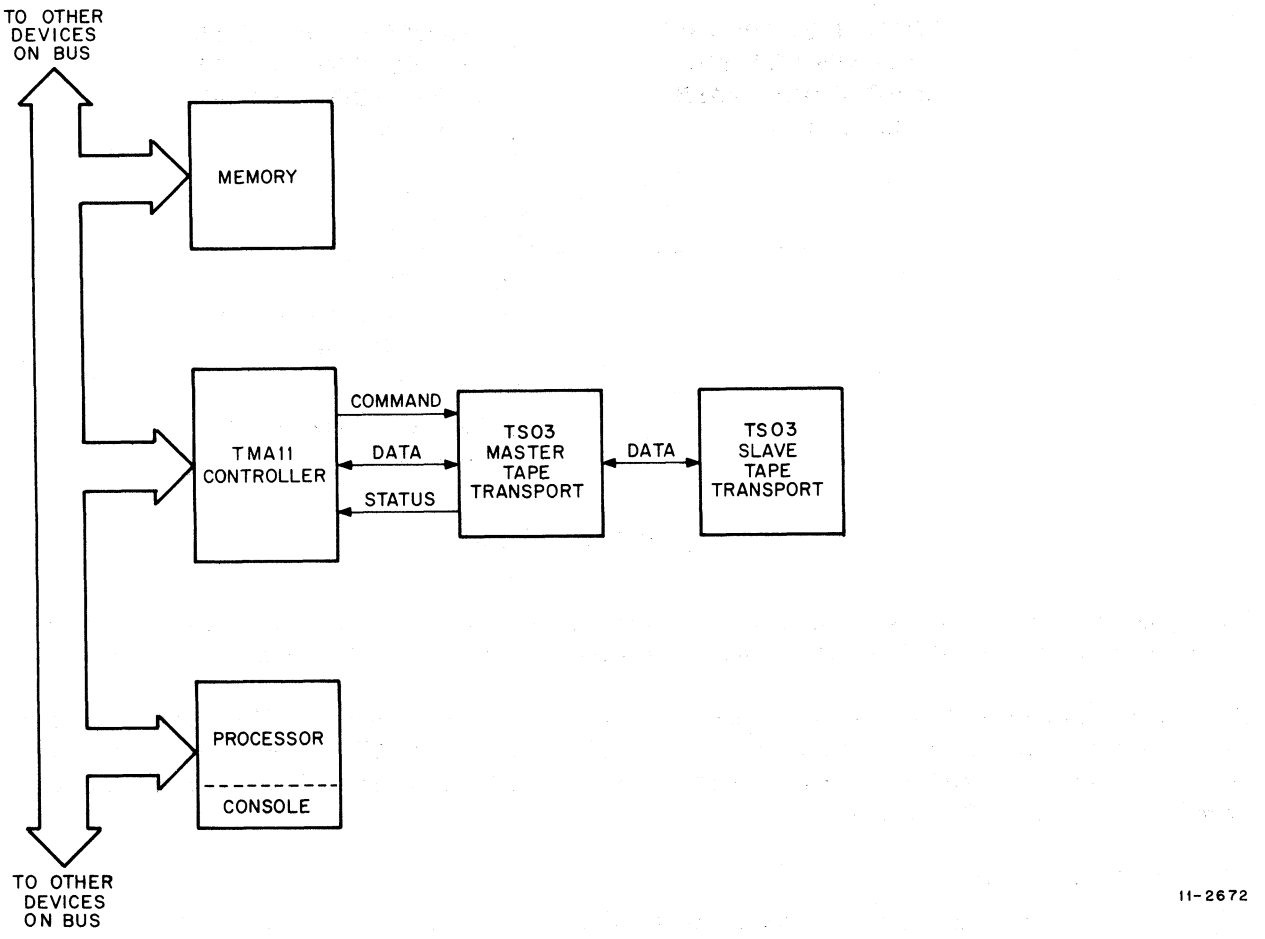

Figure 3-2 TMA11-M System – Simplified Block Diagram

A standard M105 module provides only four select line signals and, therefore, can reference only four registers. Because the TMA11 Controller contains six registers, the M105 is used in conjunction with register select logic (M797 module) to provide the six required select lines. This necessitates wiring the M105 in a manner somewhat different from the standard wiring.

Rather than decode the entire incoming address, as is the normal method, the M105 in the TMA11 Controller decodes all but the four least significant bits. These bits are then decoded by the register select module (M797 module), provided the other bits are part of a valid address.

Address line A00, which is the least significant bit of the address, is decoded by the M105 to determine if a byte or word operation is required. Address lines A01, A02, and A03 are grounded and are the only address bits that cannot be decoded by the M105. Thus, the M105 decodes all but the four least significant bits of the incoming address as shown in Figure 3-3. If the first portion of the address is valid (77252 or 77253), then the address selector generates an ADRS DEC MSYN L (address decoded, master sync valid) signal that clears the decoders in the register select logic (Paragraph 3.4.2).

The M105 Address Selector also decodes the bus C01 and C00 mode control signals to generate the IN, OUT LO, and OUT HI signals that determine whether the selected register is reading or writing (performing an input or output function).

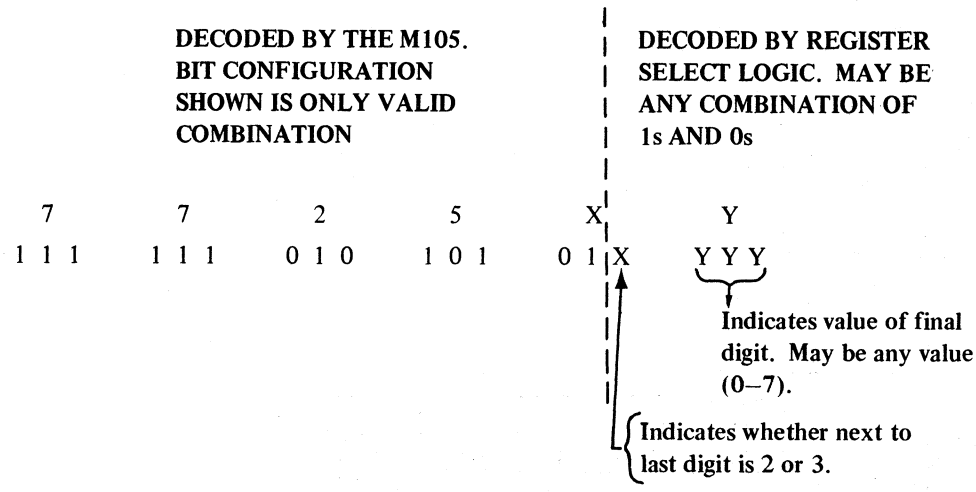

Figure 3-3 M105 Address Decoding

It is beyond the scope of this discussion to cover operation of the M105 Address Selector; detailed descriptions of this module are covered in DIGITAL's *1973–74 Logic Handbook* and in the *PDP-11 Peripherals Handbook.*

There are only two prime differences between normal use of the M105 and the use in the TMA11 Controller. Pin L2 is normally a test point, but in the TMA11 it is used to provide the ADRS DEC MSYN L signal for the register select logic. Address lines A01, A02, and A03 are normally decoded by the M105, but in the TMA11 they are decoded by the register select logic (M797 module).

3.4.2 Register Select Logic

The gating signal lines from the M105 Address Selector and address lines A01, A02, and A03 from the bus are connected to the M797 Register Select module (Drawing TMA11-0-20). This module decodes the address lines and provides the pulses that select the appropriate register and determine whether the register is to be read or loaded.

The ADRS DEC MSYN L signal from the M105 module is applied to the register select module when valid addresses up to the least significant octal digit have been decoded. The ADRS DEC MSYN L signal gates the appropriate gating signal (IN, OUT LO, OUT HI) to enable one of three decoders. If the M105 has provided an IN gating signal, then the first decoder (E2) is enabled, and one of the six outputs is selected by address lines A01, A02, and A03. The IN gate indicates that data is being transferred into the bus master device, and the decoder output selects the register from which the data is to be taken. Note that the decoder is actually enabled by the absence of the two OUT signals rather than the presence of the IN signal (Table 3-2).

Table 3-2
M797 Decoder Selection

Input Signal	Function Selected	Decoder Enabled	Output Signals	Remarks
IN (~OUT LO ~OUT HI)	Load	E2	6	One for each register.
OUT LO	Load even byte	E6	4	Only four of the six registers can be loaded.
OUT HI	Load odd byte	E9	4	

If the OUT LO signal is supplied by the M105, the second decoder (E6) in the M797 module is enabled, and the address lines select one of five decoder outputs. The OUT signal indicates a load operation (data from bus to master device). The first four outputs are used for the four registers that can be loaded from the bus. Note that OUT LO loads only the low-order (even) byte in these registers. The fifth output is used to load bits 13 and 14 in the TS03 read lines.

If the OUT HI signal is received from the M105, the third decoder (E9) is enabled, and the address lines select one of four decoder outputs to load the high-order (odd) byte of the selected register.

Table 3-3 indicates the functions selected by the various select line and gating signal combinations.

Table 3-3
Gating and Select Line Signals

Select Line	Gating Signal	Function	Register	Bus Cycle
Status	IN	Status to bus	MTS	DATI or DATIP
1	IN	Command to bus	MTC	DATI or DATIP
2	IN	Byte record count to bus	MTBRC	DATI or DATIP
3	IN	Current memory address to bus	MTCMA	DATI or DATIP
4	IN	Data buffer to bus	MTD	DATI or DATIP
5	IN	TS03 read lines to bus	MTRD	DATI or DATIP
1	OUT	Bus to command register	MTC	DATO or DATOB
2	OUT	Bus to byte record counter	MTBRC	DATO or DATOB
3	OUT	Bus to current memory address register	MTCMA	DATO or DATOB
4	OUT	Bus to data buffer register	MTD	DATO or DATOB
5	OUT	Bus to bits 13 and 14 of TS03 read lines	MTRD	DATO or DATOB

NOTES:

1. IN and OUT refer to information transfer with relation to the bus master device.
2. Status register and TS03 read lines can be read by the processor but cannot be loaded by the processor except for bit 14 of the TS03 read lines, which is the CRC/LRC character selector bit, and bit 13 which is the BTE/OPI generator bit.
3. The OUT gating signal actually can be OUT LO or OUT HI. OUT LO loads the low-order (even) byte; OUT HI loads the high-order (odd) byte.
4. The IN gating signal is actually (~OUT LO·~OUT HI).

3.5 BUS CONTROL

The TMA11 Controller is interfaced to all other components of a PDP-11 system by the Unibus. All control instructions and data transfers that take place between the TMA11 Controller and PDP-11 components, such as the processor and memory, must pass through this bus.

The bus control logic performs three main functions: NPR transfers, interrupts, and slave response. Each of these functions is briefly explained in Table 3-4 and discussed in detail in the following paragraphs.

Table 3-4
Bus Control Functions

Function	Controller Status	Bus Cycle	Description
NPR Transfer	Bus Master	DATOB	The bus control logic requests control of the bus for NPR data transfers whenever the controller is ready to *send* data from the data buffer through the bus to memory (read function). Transfers one byte at a time.
		DATI	The bus control logic requests control of the bus for NPR data transfers whenever the controller is ready to *receive* data from the memory (write function). Transfers one byte at a time.
Interrupt Request	Bus Master	INTR	The bus control logic issues an interrupt request if the controller requires servicing by the program, because it is ready to transfer data, is ready to begin a new operation, is awaiting a command, or because an error condition exists. INT ENB in the command register must be set.
Slave Response	Bus Slave	DATO DATOB DATI DATIP	Whenever the TMA11 Controller is selected for use, it must respond with SSYN in order for the command instructions to be supplied by the processor or other bus master. This logic provides the proper slave response.

3.5.1 NPR Transfers

The NPR control logic circuits are shown on Drawing TMA11-0-19. The main portion of the control logic consists of an M796 NPR Control module. This module is used to control transfers of data to and from any slave device on the bus when the controller is functioning as bus master. The transfers are performed independently of processor control and are often referred to as "direct memory access."

The logic necessary to gain control of the bus is provided by the M7821 Interrupt Control module (Drawing TMA11-0-19), which generates the non-processor request (NPR). When the proper responses are received from the processor, the M7821 asserts BUS BBSY to indicate bus control. On becoming bus master, the controller is free to conduct a data transfer. A DATI cycle is performed if the controller needs data from a bus address; a DATO or DATOB cycle is performed if the controller transmits data to memory or some other device. Basically, a DATI is used during write operations; a DATO or DATOB is used during read operations.

The bit that controls selection of a DATI or DATO is function bit 02 (Drawing TMA11-0-07). This bit is always clear for a read operation (octal number 01) and is always set for write operations (octal numbers 02, 03, and 06). Therefore, by using this bit for bus cycle selection, the proper cycle is used for the selected function (read = DATO, write = DATI). The resultant read and write signals are applied to the NPR input logic (Drawing TMA11-0-11).

Whenever a read strobe (RDS) or write strobe (WRS) pulse from the master tape transport is sent to the controller or whenever the WRITE DATA ENB and GO STROBE pulses are present in the controller, a series of gates is qualified to produce a signal that sets the NPR enable flip-flop, provided there is no non-existent memory, bus grant late or overflow error condition present, or no CRCS or LRCS pulse present. This flip-flop produces the NPR ENB H level, which initiates the NPR sequence.

The NPR ENB H level activates the Master Control A portion of the M7821 Interrupt Control module (Drawing TMA11-0-19), which generates a request on the BUS NPR line. When the processor has completed its current bus cycle and all higher priority device requests have been satisfied, the processor issues a grant on BUS NPG IN. The M7821 module responds with BUS SACK and, when BUS SSYN, BUS BBSY, and BUS NPG are negated (indicating that the bus is free), the M7821 claims bus control by asserting BUS BBSY.

At this time, the M7821 Interrupt Control module produces an NPR MASTER signal, which activates the M796 NPR Control module (Drawing TMA11-0-19). This NPR MASTER signal produces an internal start signal in the M796. Detailed descriptions of both the M7821 Interrupt Control and the M796 NPR Control modules are provided in the *PDP-11 Peripherals Handbook.* Note, however, that in the Peripherals Handbook, the M796 is referred to as the Unibus Master Control module.

Regardless of the bus cycle selected, a bus address must be used to indicate where the controller is to send or receive data. The M796 module produces the ADRS → BUS L signal, which enables the address line drivers in the current memory address register (MTCMA) so that the data transfer is made with the location specified by the MTCMA.

When a read operation is performed, the controller receives data read from the tape by the transport, assembles the data in the data buffer register (MTD) and, when the data is properly assembled, sends the data to the bus. This is a DATOB operation, because only one character is read from the tape at a time and the character corresponds to a PDP-11 byte.

When a DATOB bus cycle is selected by the M796 module, the module produces the DATA → BUS signal which, together with a flip-flop and AND gates, produces alternate HI DATA BYTE L and LO DATA BYTE L signals (Drawing TMA11-0-15) that enable data buffer output gating logic (Drawing TMA11-0-14); thus, the information stored in the data buffer register is gated onto the bus for storage in alternate memory byte locations. After the necessary Unibus time delays, BUS MSYN is asserted and, thus, a slave device is selected. When the slave device responds with SSYN, MSYN is dropped, and the bus cycle is complete.

When a write operation is to be performed, the controller receives the data from the Unibus, holds it temporarily in the data buffer, and then transmits it through the read/write lines to the master tape transport electronics for writing on the magnetic tape.

When a DATI is selected by the M796 module, the module first produces the ADRS → BUS signal as usual but, rather than produce a DATA → BUS signal, the M796 waits for the slave to respond and then produces two sequential pulses: DATA STB 1 and DATA STB 2. The DATA STB 1 pulse allows time for the data on the Unibus to deskew and settle. The pulse is also used internally (Drawing TMA11-0-16) to produce DATA BFR STB 1 and DATA BFR STB 2, which clear the data buffer register (MTD).

The trailing edge of DATA STB 2 is tied back into the M796 module to produce an internal signal, indicating that the data has been accepted. As a result of this signal, MSYN is dropped, and the bus cycle is complete.

On completion of either a DATI or DATOB bus cycle, the NPR CLR BBSY signal is generated. This signal is used to increment the current memory address register (MTCMA). The NPR CLR BBSY signal also produces the CLK 2 pulse (Drawing TMA11-0-19), which increments the byte record counter (MTBRC). The trailing edge of NPR CLR BBSY direct clears the request bus flip-flop (Drawing TMA11-0-11), which drops at the input to the M7821 Interrupt Control which, in turn, drops BUS BBSY.

A time-out flip-flop, referred to as NXM (non-existent memory), in the M796 module is set if an SSYN response from the slave device does not occur within 10 μs after BUS MSYN is asserted by the controller. When this flip-flop is set, the bus cycle is not performed, and the NXM error bit in the status register is set by the error logic circuits. In this case, the current memory address register is not incremented and, therefore, the register contains the address of the erroneous location.

3.5.2 Interrupt Request

An interrupt request is generated when the controller is ready to send or receive data to or from the bus. Interrupt requests are controlled by the BR (bus request) input logic (Drawing TMA11-0-11) and by the M7821 Interrupt Control module.

The BR interrupt flip-flop is used to generate the BR INT pulse, which activates the M7821 Interrupt Control. Note that this flip-flop can be set only if the INT ENB bit is set.

When a read, write, write IRG, write file mark, space forward, or space reverse operation completes, the transfer done flip-flop is set (TMA11-0-06). An operation that results in setting the ERR bit also sets the transfer done flip-flop. Transfer done is ANDed with TUR from the drive performing the operation which generates SET CUR L and SET BR L. Execution of a rewind, a reverse motion at BOT, or some action that results in an ILC causes the generation of SET CUR L and SET BR L (TMA11-0-06).

If a function command is issued but the GO bit remains cleared and INT ENB is set, an interrupt is initiated. If the selected tape transport (as indicated by the SEL bits in the command register) completes the rewind operation before a new command to that unit is received, then an interrupt is initiated. This logic is covered in Paragraph 3.8.

The M7821 module provides the logic necessary to make bus requests and gain control of the bus (become bus master). The module also includes the circuits necessary for generating an interrupt. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus control. The following paragraphs provide a brief description of both channels. A detailed description of the M7821 module, including circuit schematics, is contained in the *PDP-11 Peripherals Handbook.*

Channel A (master control A) is used only for NPR requests and is activated when the bus request flip-flop is set, as described in Paragraph 3.5.1. The BR MASTER L signal from channel A activates the NPR control logic so that an NPR DATI or DATOB bus cycle can be performed. No vector address is used with this channel.

Channel B (master control B) is used to generate interrupts (Drawing TMA11-0-19). This channel is activated by the BR INT pulse described previously.

The jumpers on the M7821 module are wired for a standard vector address of 224 and a bus request level of BR5. Note that the priority level can be changed by the priority chip on the G736 module, and the vector address can be changed by jumpers on the M7821 Interrupt Control. However, any programs referring to that level or vector address must also be changed if the jumpers are changed. All DEC software references the above standard jumpers.

3.5.3 Slave Response

When the TMA11 Controller is to participate in a data transfer as a bus slave device, the slave response logic provides the necessary acknowledgement signals required by the bus master. This slave response logic is part of the M105 Address Selector and the M797 Register Select modules.

For a DATO, the master device places the address of the TMA11 Controller on the bus A lines, data to be transferred on the bus D lines, and signals on the bus C lines to select the appropriate register and function to be performed.

The master device waits 150 ns (75 ns to allow for worst case signal skew and 75 ns for address decoding) and then asserts BUS MSYN, provided the bus is clear (SSYN is clear).

When the controller decodes the address, it produces the ADRS DEC MSYN L signal at the time MSYN is received. The BUS MSYN L signal is gated through the M105 to produce the BUS SSYN response. There is a 300-ns time delay between MSYN and generation of SSYN.

The master device receives SSYN and clears MSYN (which clears ADRS DEC MSYN L). Clearing ADRS DEC MSYN L negates BUS SSYN to signify the end of the bus transaction.

3.6 BUS DRIVERS AND RECEIVERS

The bus drivers and receivers provide the signal levels required for compatibility with the Unibus. The M798 Transmitter module contains bus drivers for interfacing controller outputs to the bus. The M784 Receiver module contains inverting circuits that provide buffered bus signal outputs, which are used as inputs to the controller. The M785 Transceiver module contains both drivers and receivers that are used for bidirectional interfacing to the bus.

The bus receivers are used primarily on the input lines to the various controller registers; the bus transmitters are used on the output lines. The transceivers are used on the current memory register lines for bits 01, 02, 03, 16, and 17.

The M784, M785, and M798 modules are described in the *PDP-11 Peripherals Handbook.*

3.7 REGISTERS

All software control of the TMA11 Controller is performed by means of six device registers. These registers are assigned Unibus addresses and can be read or loaded with any PDP-11 instruction that refers to their address. Note, however, that the status register and the TS03 read lines (with the exception of bits 13 and 14 in the read lines) can be read but cannot be loaded from the bus. Bits 13 and 14 of the read lines can be loaded from the bus. In addition, bit 13 is always read as a 0. Table 3-5 lists the six registers and the function of each.

The register select logic provides the pulses that activate a specific register for use. This selection is described in Paragraph 3.4.2.

Paragraph 3.7.1 describes the initialize (INIT) logic, which is common to all registers. Subsequent paragraphs discuss each of the registers from a hardware standpoint. A discussion of the registers from a programming standpoint is presented in Chapter 2.

Table 3-5
Device Register Functions

Register	Mnemonic	Function
Status Register	MTS	Provides detailed information on the status of the TMA11 Controller. Such information includes error indications and tape unit status indications.
Command Register	MTC	This is the main control register in the TMA11 Controller. Specifies the operation to be performed on the tape unit, selects the tape bit packing density, and selects the tape unit to be used. Indicates when TMA11 Controller is ready, when an error condition exists, and when the controller is cleared. Provides the two extended address bits for bus addresses.

Table 3-5 (Cont)
Device Register Functions

Register	Mnemonic	Function
Byte Record Counter	MTBRC	Counts the number of bytes in any write operation, the number of records in a space forward or space reverse operation, and the number of bytes in a read operation. Desired byte count is preset by the program. When the register counts the number of specified bytes, it prevents further transfers.
Current Memory Address Register	MTCMA	Specifies the bus or memory address to or from which data is transferred during read and write operations. After each transfer is completed, the register is automatically incremented by 1 (next byte location). When BGL or NXM errors occur, the register contains the address of the location in which the failure occurred. Note that this register is incremented by 1 and, therefore, accesses byte, rather than word, locations.
Data Buffer Register	MTD	Contains the information read from or written on the tape. Serves as a buffer between the tape unit and the memory.
TU10 Read Lines	MTRD	Permits storage of data read from the tape transport. A parity bit indicates the occurrence of a parity error and the channel containing the error. A character selector bit is used to select the last character of a record that is to be loaded into the data buffer register. A timer bit is used for diagnostic purposes by measuring the time duration of the tape operations. A BTE/OPI bit is used to set transfer done prematurely in order to provide a bad tape error indication.

3.7.1 Initialize Logic

The TMA11 Controller logic can be initialized by one of the following methods:

1. Loading a 1 into bit 12 (Power Clear) of the command register.
2. Issuing a programmed RESET instruction.
3. Depressing the START switch on the PDP-11 processor console.
4. Occurrence of a power fail by either the processor power supply or the controller power supply.

The controller initialization logic is shown on Drawing TMA11-0-17.

When a 1 is loaded into bit 12 of the command register, an AND gate is qualified by D12 H and SEL 1 OUT HI H. When the AND gate is qualified, the INIT H and INIT L signals are produced as before.

The remaining three methods of initialization (programmed RESET, processor START, power fail) all use external logic to provide a BUS INIT signal input to the controller. This signal becomes INIT REC H and produces the INIT H and INIT L signals as before.

3.7.2 Command Register (MTC)

The command register is the main control register in the system and specifies the operation to be performed. Each of the bits is discussed separately below, beginning with the most significant bit.

3.7.2.1 Error Bit (15) – The error bit (bit 15) in the command register is the inclusive-OR of all error conditions in the status register. Thus, if any error bit in the status register is set, it sets the error bit in the command register. When any error condition occurs, it sets the appropriate flip-flop in the status register. The appropriate level from the flip-flop passes through a series of OR gates (Drawing TMA11-0-18) and sets the command register error flip-flop, which produces the ERR H signal. The ERR H signal is then applied through a series of AND gates (Drawing TMA11-0-13) so that the bit can be read from the bus.

Because of gating shown on Drawing TMA11-0-18, the ERR flip-flop may or may not be set simultaneously with the detection of an error condition. In the case of BGL (bus grant late), NXM (non-existent memory), ILC (illegal command), and BTE (bad tape error) errors, the resultant error signal passes through OR gates and sets the error flip-flop simultaneously with detection of the error.

If RLE (record length error), CRE (cyclical redundancy error), PAE (parity error), or EOF (end-of-file) occurs, the appropriate status register flip-flop is set, and the resultant error signal is ANDed with the LRCSD signal, which occurs only when the LRC character is detected. Thus, the command register error flip-flop is not set until the LRC character has been read, in order to give the controller time to complete the current operation.

When the EOT (end-of-tape) marker is detected, it represents an error condition only if the tape is moving in the forward direction. The EOT signal is ANDed with SPACE REV L, REWIND L, and LRSCD. This AND gate, therefore, is qualified only if the end-of-tape marker has been detected (EOT), the tape is not moving in the reverse direction (SPACE REV L), the tape is not being rewound (REWIND L), and the LRC character has been detected (LRCSD). If these conditions are met, the gate is qualified, and the resultant output sets the error flip-flop in the command register.

When the error bit is set, it sets the transfer done flip-flop as shown on Drawing TMA11-0-06. The transfer done signal is ANDed with TUR to produce the SET CUR L signal that direct sets the control unit ready (CU RDY) flip-flop.

The output of the interrupt flip-flop (BR INT H) is applied to the Master Control B section of the M7821 Interrupt Control module, and the TMA11 Controller initiates an interrupt routine. Thus, an error condition causes an interrupt, provided the INT ENB bit is set.

A selection error is an illegal command and, therefore, also causes an error condition.

The error conditions can be cleared by INIT (refer to Paragraph 3.7.1) or by the next GO command.

3.7.2.2 Density Bits (14 and 13) – The DEN 8 and DEN 5 bits are used together to determine the bit packing density of the tape. Only 800 bpi can be used. The program selects the density by loading the appropriate value into these bit positions, according to the following table:

DEN 8 (BIT 14)	DEN 5 (Bit 13)	Selected bpi	
0	0	200	7-channel tape (See Note)
0	1	556	
1	0	800	
1	1	800	9-channel (TS03)

NOTE
TS03 ignores bits 14 and 13; it always operates at 800 bpi, 9-channel.

These signals are applied to the master tape transport by the controller but are ignored as the TS03 only operates at 800 bpi. The controller logic is used primarily to feed appropriate bits to the master tape transport and to select the core dump mode of operation. Controller logic is shown on Drawing TMA11-0-08.

When a 1 is loaded into bit 13 (DEN 5), it is applied to the D-input of a flip-flop. The clock input is the SEL 1 OUT HI H signal that indicates the bus is loading the command register. These two inputs set the flip-flop. The low side of the flip-flop qualifies an AND gate, provided the core dump mode is not being used. The output of the AND gate is the DEN 5 signal (representing binary 1) that is applied through the BC11A interconnecting cable to the master tape transport.

If a 0 is loaded into this bit position, the flip-flop is not set, the AND gate is disqualified, and the AND gate output is a low level representing binary 0.

The DEN 8 (bit 14) signal is produced in an identical manner to the DEN 5 signal.

3.7.2.3 Power Clear Bit (12) – When the program loads a 1 into this bit position, an initialize signal is provided to clear the TMA11 Controller, the master tape transport, and the slave transport. This initialize signal does not clear the processor or any other device on the bus. The initialize signal is generated by the controller logic as descirbed in Paragraph 3.7.1. The INIT signal passes through a gate and becomes the CINIT signal, which is applied to the master tape transport logic to clear all transports.

3.7.2.4 Parity Bit (11) – The parity bit (bit 11) specifies whether odd or even vertical parity is to be read from or written on the magnetic tape. Although parity is generated by the master tape transport, the parity bit in the controller command register is used to select the polarity. The parity bit is referred to as the PEVN (parity even) bit, because it denotes even parity when set.

The parity flip-flop is shown on Drawing TMA11-0-08. The flip-flop is set by SEL 1 OUT HI H (indicating that the command register has been selected for loading from the bus) and by D11 H (indicating that a 1 has been loaded into bit 11 of the command register). With the flip-flop set, the low side passes through a gate and becomes the PEVN signal, which is applied to the master tape unit to indicate that even parity is to be used.

The parity flip-flop is cleared by loading a 0 into bit 11 (the D11 H input becomes low) or by an INIT signal, which direct clears the flip-flop. When the flip-flop is clear, the resultant PEVN signal is low, indicating to the master tape transport that odd parity is to be used.

3.7.2.5 Unit Select Bits (10, 09, 08) – The three unit select bits (bits 10 through 08) specify the tape transport that is to be used for a particular operation. The states of these three bits represent an octal code corresponding to the number of the transport, as set by the UNIT SELECT switch on the individual transport.

The three unit select bits are shown on Drawing TMA11-0-10. These three bits (UNIT SEL BIT 2, UNIT SEL BIT 1, and UNIT SEL BIT 0) are set or cleared by loading 1s or 0s from bus lines 10, 09, and 08, respectively. These bits are loaded whenever the high byte of the MTC is addressed (SEL 1 OUT HI H). This results in SEL 2, SEL 1, and SEL 0 signals (representing the appropriate octal code loaded from the bus), which are applied to the master tape transport logic.

The master tape transport only recognizes octal codes 000 and 001. Any other code places both transports in the deselect mode.

Another instance of improper selection would be selecting a tape transport that is off-line. Improper selection is an illegal command (ILC) error, which, in turn, causes an ERR indication.

The unit select logic also produces UNIT SEL BIT TM H and L signals, which are used by the tape motion control logic described in Paragraph 3.8.

3.7.2.6 Control Unit Ready Bit (07) – The control unit ready bit (bit 07) indicates that the controller is ready to receive a new command. It is set (indicating ready) whenever the previous command operation is completed, an initialize signal is given, or an error condition exists. It is cleared at the beginning of a tape operation when the GO command (bit 00) is issued.

The control unit ready flip-flop is shown on Drawing TMA11-0-06. A series of gates is connected to the direct-set input of the flip-flop. If the INIT signal goes high (indicating initialize), the output of the OR gate goes low and direct sets the control unit ready flip-flop, producing CU RDY H.

The gating also direct sets the CU RDY bit when an operation sets the transfer done bit which is ANDed with TUR; when a rewind operation has started; when the unit goes off-line during an operation; and when the BOT is sensed during a rewind or space reverse operation.

The control unit ready flip-flop is cleared by the GO BIT H signal, which occurs whenever the GO bit is loaded from the bus.

3.7.2.7 Interrupt Enable Bit (06) – The interrupt enable (INT ENB) bit, when set, allows an interrupt to occur provided CU RDY (bit 07) becomes set. It also permits an interrupt whenever a tape unit in the rewind mode reaches the BOT marker at the time CU RDY is a 1, or whenever an instruction sets the INT ENB bit but does not set the GO bit (bit 00).

The interrupt enable flip-flop is shown on Drawing TMA11-0-08. It is set by SEL 1 OUT LO H (bus loading command register) and D06 H (a 1 in the bit position). The high output of the flip-flop (INT ENB H) qualifies one side of an AND gate, tied to the input of the bus request flip-flop (Drawing TMA11-0-11). The other input to the AND gate is produced by a series of gates corresponding to the conditions mentioned above. Thus, when a condition exists that results in a SET BR L pulse, or when a tape unit has completed its rewind operation (indicated by RWS H and BOT H), or when an instruction sets the INT ENB bit but does not set the GO bit (indicated by INT ENB L, D00 L, and SEL 1 OUT LO H), the AND gate is qualified, thereby setting the BR INT flip-flop.

The INT ENB bit is direct cleared by the INIT L signal or is cleared by loading with a 0 (input D06 H becomes low).

3.7.2.8 Extended Bus Address Bits (05 and 04) – The extended bus address bits 05 and 04 represent bus address bits A17 and A16, respectively. These bits are used to specify 18-bit addresses when required, because the current memory address register (MTCMA) is only 16 bits long. Although functionally part of the MTCMA, these bits are loaded by a SEL 1 OUT LO H signal, which indicates that the command register has been selected for use. The current memory address register is incremented after each data transfer, and this incrementation also affects the two extended address bits. These bits are cleared by INIT, as shown on Drawing TMA11-0-20.

3.7.2.9 Function Bits (03, 02, 01) – The three function bits are set or cleared to provide an octal code that selects any one of eight commands that control operation of the tape system. These commands are used for reading data from or writing data on the tape and for controlling tape motion.

The three function bits are shown on Drawing TMA11-0-07. The appropriate 1 or 0 on the associated bus data line (D03, D02, and D01) is loaded into the associated function flip-flop by means of a load pulse, which is SEL 1 OUT LO H (command register selected for loading from the bus).

The FUNCTION BIT H line from each of the three flip-flops is tied to the input of an M163 binary-to-octal decoder, which decodes the state of the three bits and provides the selected function output signal. The selected function signal is then applied to other controller logic to institute the function. Other logic that uses the function signals includes: ready control logic, motion control logic, start control logic, error logic, and tape interface logic.

3.7.2.10 GO Bit (00) – The GO bit is set by loading with a 1 from the bus and is used to initiate operation of the function selected by the function bits.

The GO flip-flop (TMA11-0-05) is set by the SEL 1 OUT LO L signal (command register selected to receive data from bus) and the D00 H signal (1 loaded into bus data line 00). Note that the output of the flip-flop, when set, passes through a series of gates to produce three derivatives of the GO signal. These derivatives (shown in Figure 3-4) are: GO STROBE 1, GO STROBE 2, and SET. The SET signal is effectively the GO pulse to the master tape transport and must be present before any tape operation can be initiated.

The GO flip-flop is cleared by INIT or by the GO STROBE 2 pulse. GO STROBE 2 is simultaneously applied to an OR gate, the output of which direct clears the GO flip-flop, and to an AND gate which, when qualified, asserts the SET pulse (GO command to transport).

During normal operation, the GO pulse is 1 μs in duration. However, in some instances this duration may be considerably longer, depending on the status of the selected tape transport.

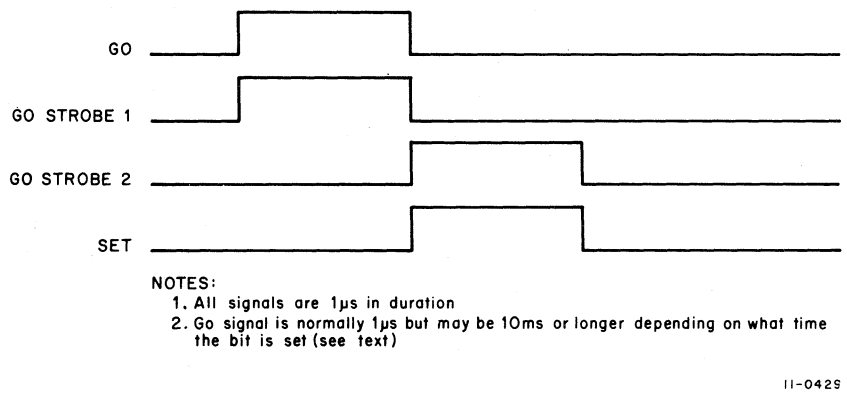

Figure 3-4 Derivatives of GO Signal

As mentioned previously, the GO pulse cannot go low until the GO STROBE 2 pulse is generated. Before GO STROBE 2 can be generated, these conditions are needed: GO BIT H (GO flip-flop) set, selected unit not performing a rewind instruction, and the selected transport is ready (TUR). If any one of these conditions is not true, the GO pulse remains high until the required condition becomes true.

If the selected tape unit is not ready (note that this condition also exists during rewind, because RWS direct sets the flip-flop, providing one of the AND gate inputs), the GO bit duration could be as long as several minutes as would be the case when the selected tape unit is in the process of rewinding.

The GO BIT H signal is also applied to the control unit ready (CU RDY) flip-flop (Drawing TMA11-0-06) to clear the CU RDY bit. This is necessary because whenever the GO bit is present, it indicates the controller is performing an operation and is not ready to accept a new command.

3.7.3 Status Register (MTS)

The status register is used primarily to provide indications of error conditions. It also indicates the status of certain system functions such as write lock, settling down period, tape unit ready, and beginning of tape.

The status register error logic is shown on Drawing TMA11-0-18. Whenever one of the specific error signals is present, it passes through an OR gate, which is the inclusive OR of all error conditions. The resultant flip-flop output signal(ERR L) sets transfer done which is ANDed with TUR, then passes through a pulser and two OR gates in the ready control logic (Drawing TMA11-0-06) and direct sets the control unit ready (CU RDY) flip-flop. This allows the controller to issue an interrupt request whenever an error exists (Paragraph 3.5.2).

All error bits (15 through 06) in the status register are read-only bits. They can be read (tested) by the program to determine if a specific error exists or not, but they cannot be loaded by the program. All error bits are cleared by INIT or by the GO (GO STROBE 1) pulse to the tape unit.

The remaining bits (05 through 00) indicate system status and are set or cleared by the master tape transport. These bits can also be read by the program.

Each individual bit in the status register is discussed separately in the following paragraphs.

3.7.3.1 Illegal Command (15) – The illegal command (ILC) error bit indicates a conflict in commands. The ILC error logic (Drawing TMA11-0-17) consists of a series of gates and a flip-flop. The first series of gates is used to direct set the ILC flip-flop. Any time that a DATO or DATOB transfer is made to the command register (SEL 1 OUT LO H or SEL 1 OUT HI H) during a current tape operation (CUR DEL L), gating is qualified to set the ILC flip-flop, because the command register cannot accept a new command while in the process of executing another command.

When the SELR bit becomes 0 (SELR H) during any operation (CUR DEL L) except an off-line command, gating is qualified to direct set the ILC flip-flop, because no command can be issued to a tape transport that is not on-line.

The remaining gates in the ILC error logic are used to produce SET ILC H, which sets the ILC flip-flop when the GO pulse is present (GO STROBE 2 L). There are two illegal commands that can produce SET ILC H. The first command is any command to a tape transport that has its SELR bit clear (SELR H), because when SELR is clear it indicates the transport is off-line

The second illegal command is any write, write end-of-file, or write-with-extended-IRG command (WRITE ENB H) that is issued when the write lock bit is set (WRL H). Writing is inhibited with WRL set, and all write commands are, therefore, illegal.

When an illegal command produces the ILC H pulse, the pulse is applied to the gating logic for the error flip-flop in the command register (Drawing TMA11-0-18); thus, the command register ERR bit is set simultaneously with the status register ILC bit. The ILC bit asserts SET CUR L and SET BR L immediately (TMA11-0-06).

The ILC error bit is cleared by INIT or by occurrence of the GO pulse. When the GO pulse occurs, the GO STROBE 1 pulse occurs immediately preceding the GO STROBE 2 pulse and is used to direct clear the ILC flip-flop.

3.7.3.2 End-of-File Bit (14) – Bit 14 is used to indicate that the tape has reached the end of the file. The EOF flip-flop (Drawing TMA11-0-18) is set by the master tape transport and cleared by INIT or a GO pulse. The input to the flip-flop is the FMK (file mark) signal from the master tape transport. This signal, when present, indicates that the transport has detected the end-of-file mark on the tape. The signal sets the EOF flip-flop to produce the EOFF H signal.

3.7.3.3 Cyclic Redundancy Error Bit (13) – The cyclic redundancy error (CRE) bit in the status register indicates that the cyclic redundancy check has detected a parity error. This check compares the CRC character written during a write or write-with-extended-IRG operation with the CRC character generated during a read operation.

The comparison of the two CRC characters is performed by logic within the master tape transport. If the two characters are not identical, then the CRCE from the tape unit becomes a 1 and is applied to gating logic in the controller error circuits (Drawing TMA11-0-18). The gating logic sets the CRE flip-flop to produce CRE H.

The CRE output of the flip-flop is applied to gating logic associated with the command register ERR flip-flop. Note, however, that the AND gate is not qualified until both CRE and LRCSD H are present. The latter signal indicates that the LRC character has been detected. Thus, when a CRC error is detected, the CRE bit in the status register is set immediately, but the ERR bit in the command register is not set until the LRC is detected. This gives the controller time to complete the current operation before branching to an error routine by means of the interrupt.

3.7.3.4 Parity Error Bit (12) – The parity error (PAE) bit in the status register indicates that a parity error exists in the data. The error may be in either vertical or longitudinal parity. A vertical parity error is indicated for any character in a record; a longitudinal parity error indicates an error in a specific channel.

The parity error circuits are shown on Drawing TMA11-0-18. An AND gate output is used to set the PAE flip-flop; this AND gate is qualified by three inputs. The first input is RDS H from the master tape transport, which is used to sample parity. The second input is either WRITE ENB or READ, because parity is checked during both read and write operations. The third input is either the BPE (vertical parity error) or LRCE (longitudinal redundancy check error) signal from the transport. Thus, both vertical and longitudinal parity errors are detected during read, write, write EOF, and write-with-extended-IRG operations. The entire record is checked, including the CRC and LRC characters.

Note that longitudinal parity occurs when an odd number of 1s is present in any channel in the record; vertical parity errors may be even or odd, depending on the setting of the PEVN bit in the command register.

The PAE output of the parity error flip-flop is applied to command register gating logic in the same manner as the CRE output, as explained previously. In the case of PAE, the PAE bit in the status register is set immediately, but the command register ERR flip-flop is not set until detection of the LRC character.

3.7.3.5 Bus Grant Late Error Bit (11) – During normal operation, the controller makes an NPR request to gain control of the bus and initiate a data transfer (either a read or a write). If the controller is still engaged in the NPR transfer when another NPR request is initiated, a BGL error condition occurs.

The BGL flip-flop is shown on Drawing TMA11-0-18. It is set (indicating an error) when both the NPR ENB and NPR SET inputs are high. These inputs are received from the NPR input logic (Drawing TMA11-0-11).

If the controller receives either a WRS or RDS pulse from the master tape transport, the NPR logic circuits produce the NPR SET H pulse. This pulse is gated through an AND gate and sets the NPR request flip-flop on its trailing edge.

If, however, the NPR transfer is still occurring when the next NPR SET H pulse occurs, the BGL flip-flop is set to indicate an error. The NPR request flip-flop is cleared at the end of an NPR transaction by the NPR CLEAR BBSY H signal.

The BGL error signal disqualifies the AND gate on the input of the NPR request flip-flop, thereby preventing any further NPR requests until the error condition is corrected. In addition, the BGL signal is applied through gates in the error logic (Drawing TMA11-0-18) to set the ERR flip-flop in the command register.

3.7.3.6 End-of-Tape Bit (10) – The end-of-tape (EOT) bit is set when the EOT marker is detected when the tape is moving in the forward direction; it is cleared by the trailing edge of the EOT marker when the tape is moving in the reverse direction. Note that the EOT bit is an error condition only when the tape is moving forward.

The EOT bit is controlled by the master tape transport. The transport logic detects the EOT and sends the appropriate signal to the status register to set or clear the bit. When the EOT marker is detected by the transport, the EOT H signal is applied to error logic in the controller (Drawing TMA11-0-18). An AND gate is qualified if EOT is high, and both SPACE REV L and REWIND L are true (indicating the tape is not moving in the reverse direction). The output of the AND gate is ANDed with the LRCSD H signal (indicating that the LRC character has been detected) and used to set the ERR flip-flop in the command register.

Thus, the EOT bit in the status register is set or cleared as soon as the EOT marker is detected, but the ERR bit in the command regsiter is not set until the LRC character has been read in order to allow completion of the current operation prior to initiating an interrupt.

3.7.3.7 Record Length Error Bit (09) – During read operations, the record length error (RLE) bit is set if the master tape transport attempts to load another character into the controller after the number of bytes specified by the byte record counter has already been transferred to memory. This error bit is used for long records only and is set as soon as the byte record counter increments beyond 0.

The byte record counter (MTBRC) is used to keep track of the number of data bytes loaded into memory from a tape record. Initially, the MTBRC is loaded with the 2's complement of the number of bytes to be loaded. Each time the master tape transport reads a character, it loads it into the data buffer register. After a byte is transferred to memory, the MTBRC is incremented by 1. When the last byte is transferred to memory, incrementing the MTBRC by 1 sets it to 0.

As soon as the byte record counter goes to 0, it produces a CARRY OUT 2 L signal, which sets the overflow flip-flop (Drawing TMA11-0-18). This flip-flop had been reset because of the INIT or GO L signal. Therefore, it is now set and produces an OVERFLOW H pulse.

This overflow pulse is applied to one leg of a 3-input AND gate. Because the RLE error can only occur during a read operation, the AND gate is not qualified unless a read operation is being performed as indicated by a read strobe signal (READ STB H) and the absence of a CRCS or LRCS pulse (CRCS L or LRCS L). When the AND gate is qualified, its output changes the state of the RLE flip-flop, thereby setting it to provide an indication of record length error in status register bit position 09.

When the RLE flip-flop is set, the RLE L output qualifies an OR gate in the error logic circuits. The signal from the OR gate qualifies an AND gate when the LRC character is read (LRCSD H), thereby setting the ERR flip-flop. Thus, when a record length error occurs, the RLE bit is immediately set, and the ERR bit in the command register is set after the current operation is completed.

3.7.3.8 Bad Tape Error/Operation Incomplete Bit (08) – A bad tape error occurs when a character is detected (RDS pulse) during the gap shutdown or settling down period for all tape functions except rewind and off-line.

The BTE/OPI flip-flop (Drawing TMA11-0-17) is normally in the clear state. It is set by the output of a four-input NAND gate. One input of this NAND gate is the RDS H pulse, which indicates that a character has been detected. The second input to the NAND gate comes from a series of gates that are qualified if the tape unit is in either the gap shutdown (GSD L) or settling down (SDWN L) period. The third input is in the INH BTE signal (BGL, NXM, or ILC is true). Issuing a new GO command or an INIT pulse causes the BTE/OPI flip-flop to clear so that it can be ready for another bad tape error.

When the BTE/OPI flip-flop is set, it also qualifies one leg of an OR gate shown on Drawing TMA11-0-18. The output of this gate sets the ERR flip-flop as soon as the error occurs.

An operation Incomplete occurs when any operation, other than a REWIND or OFF-LINE command, fails to encounter an LRC character within 7 seconds after GO STROBE 2. Each GO STROBE 2 starts the 7-second timer. The timer (TMA11-0-17) is stopped (reset) by LRCS, RWD or INIT + GO. The BTE/OPI bit is a fatal error requiring the tape to be repositioned to a known point (FMK or BOT).

3.7.3.9 Non-Existent Memory Bit (07) – The non-existent memory (NXM) error flip-flop, when set, indicates that the controller was bus master during NPR operations but did not receive an SSYN response from the slave device within 10 μs after the controller issued the MSYN signal. The ERR bit is set simultaneously with the NXM bit, thus terminating all operation. If the NXM error occurs during a write or write-with-extended-IEG operation, the controller does not send the WDR signal to the master tape transport; however, the master transport writes the CRC character (if required) and the LRC character onto the tape.

The NXM error flip-flop is part of the NPR control circuits on the M796 module and is described in Paragraph 3.5.1.

3.7.3.10 Select Remote Bit (06) – The select remote (SELR) bit, when set, indicates that the selected transport has been selected and is on-line. When this bit is 0, it indicates that the tape transport addressed does not exist (no transport UNIT SELECT switch set to the number specified by the program), is off-line (transport ON-LINE/ OFF-LINE switch set to OFF-LINE), or that the selected transport has its power turned off.

The select remote logic is within the master tape transport, which supplies the appropriate signal to the status register for monitoring.

3.7.3.11 Beginning-of-Tape Bit (05) – The beginning-of-tape (BOT) bit in the status register indicates when the BOT marker on the magnetic tape is read. As long as this bit remains 0, it indicates that the BOT marker has not been sensed. When the bit is a 1, it indicates that the marker has been sensed, and the beginning of the tape has been reached. The ERR bit is not set when the BOT bit is sensed, because sensing of the BOT marker does not indicate an error condition.

The beginning-of-tape logic is within the master tape transport, which supplies the appropriate signal to the status register to set or clear the BOT bit.

3.7.3.12 7-Channel Bit (04) – This bit is always cleared by the master tape transport as the TS03 is a 9-channel unit.

3.7.3.13 Settle Down Bit (03) – A settling down period is provided to allow the tape to fully stop prior to stopping or starting a new operation. This settling down period sets the SDWN bit in the status register. When the tape unit stops, SDWN is cleared, and the tape unit ready bit is set.

The settle down logic is within the master tape transport, which supplies the appropriate signal to set or clear the SDWN bit in the status register. A description of the SDWN bit is contained in Paragraph 2.2.

3.7.3.14 Write Lock Bit (02) – The write lock (WRL) bit is under control of the master tape transport. When set, it prevents the controller from writing information on the magnetic tape. If the write lock signal is supplied from the master tape transport (WRL H) and the controller attempts to write on the tape (WRITE ENB H), then an AND gate is qualified (Drawing TMA11-0-17) that sets the illegal command (ILC) flip-flop, thereby setting the ERR flip-flop and preventing the write operation from being executed.

3.7.3.15 Rewind Status Bit (01) – The rewind status (RWS) bit is under control of the master tape transport, which supplies the signal to set or clear the RWS bit in the status register. The RWS bit is set at the start of a rewind operation, and becomes a 0 as soon as the BOT marker is detected while the tape is moving in the forward direction. Thus, when the bit is set, it indicates the tape is rewinding; when it is clear, it indicates the rewind operation is complete. The RWS signal from the master tape transport is also used in the tape control ready logic described in Paragraph 3.8.3.

3.7.3.16 Tape Unit Ready Bit (00) – The tape unit ready (TUR) bit is under control of the master tape unit, which supplies the signal to set or clear the TUR bit in the status register. Whenever the selected tape unit is being used (such as rewind), this bit is cleared. When the tape unit is stopped and ready to receive a new command, this bit is set. The TUR signal from the master tape transport is used in the tape start control logic.

3.7.4 Byte Record Counter (MTBRC)

The byte record counter (MTBRC) is a 16-bit binary counter used to count bytes in a read or write operation and used to count records in space forward and space reverse operations. This register and the current memory address register constitute the M795 module shown on Drawing TMA11-0-19. A detailed schematic and associated description of this module are presented in the *PDP-11 Peripherals Handbook.*

When used in a write or write-with-extended-IRG operation, the register is set by the program to the 2's complement of the number of bytes to be written on the tape. Each time a write operation is performed, the register increments by 1. After the last byte has been strobed from memory, the register increments to 0 and produces a CARRY OUT 2 signal. This signal sets the overflow flip-flop (Drawing TMA11-0-18), which produces the OVERFLOW signal. When the next write strobe (WRS) signal occurs, the OVERFLOW signal clears the write data ready (WDR) line (Drawing TMA11-0-07); thus, the controller lowers the write data ready line to indicate to master tape transport that there are no more data characters in the record.

When used in a read operation, the byte record counter is set to a number equal to or greater than the 2's complement of the number of tape characters to be loaded into memory. A record length error (RLE), which occurs for long records only, occurs whenever a read pulse is generated after the MTBRC is at 0. The RLE error is shown on Drawing TMA11-0-18. The RLE flip-flop is set by the output of an AND gate that is qualified if the MTBRC has incremented to 0 (OVERFLOW H), a read pulse is generated (READ STB H), and there is no CRCS or LRCS pulse (~CRCS + LRCS).

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of *records* to be spaced. The counter is incremented by 1 at LRC time, regardless of direction of tape motion. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not yet at 0. This logic is shown on Drawing TMA11-0-05. Either direction (SPACE FWD or SPACE REV) qualifies an OR gate to produce SPACE H, which is one leg of an AND gate. The other leg of the gate is qualified if the MTBRC is not at 0 (OVERFLOW L), and there is no end-of-file mark (EOF F L). The output of this AND gate qualifies another AND gate, provided settle down is present (SDWN H). When this gate is qualified, it triggers the logic that produces the GO pulse.

When the last record is reached, the byte record counter increments to 0 and produces the CARRY OUT 2 pulse. This pulse is ANDed with SPACE H (Drawing TMA11-0-06), passes through an OR gate, and direct sets the Transfer done flip-flop. The transfer done flip-flop output, DONE (1) H, is then ANDed with TUR H and applied to the ready control logic to direct set the control unit ready (CU RDY) flip-flop. Setting the CU RDY flip-flop indicates that the controller is ready to receive a new command, because the space operation is now complete.

3.7.5 Current Memory Address Register (MTCMA)

The current memory address register specifies the bus or memory address to or from which data is to be transferred during write or read operations. The current memory address register (MTCMA) and the byte record counter (MTBRC) constitute the M795 module shown on Drawing TMA11-0-19. A detailed schematic and associated description of this module are presented in the *PDP-11 Peripheral Handbook.*

Before issuing a command, the program loads the MTCMA with the memory address that is to receive the first byte of data (read operation) or the memory address from which the first byte is to be taken (write operation). After each memory access (read or write), the MTCMA is immediately incremented by 1. This incrementation is caused by the NPR CLR BBSY signal, which indicates the bus transfer is completed.

The logic shown on Drawing TMA11-0-20 is used to carry the bus address register incrementation to extended address bits 16 and 17 in the status register. When incrementation of the MTCMA causes the register to contain all 1s, the next clock pulse sets the current memory address register to all 0s and produces a CARRY OUT 3 pulse, which sets extended address bit 16. The MTCMA then continues incrementing until another CARRY OUT 3 pulse is produced, which sets extended address bit 17.

The logic shown on Drawing TMA11-0-15 is used to select the low- or high-order byte of the data register. This is necessary because the MTCMA increments by 1 (byte addresses). Each time a byte transfer is completed, the CMA BIT 00 flip-flop is clocked by the NPR CLEAR BBSY signal. The CMA BIT 00 flip-flop initial condition (set or reset) is determined by D00 when the MTCMA is loaded. The state of the CMA BIT 00 flip-flop determines which byte is transferred by producing alternate LO DATA BYTE and HI DATA BYTE signals to the data register until the desired data transfer function is complete. When the function is complete, the controller CU RDY bit indicates that the controller is ready to accept a new command.

3.7.6 Data Buffer Register (MTD)

The data buffer register is used as a temporary storage device during read and write operations. During read operations, it stores characters from the tape prior to loading them into memory; during write operations, it stores data prior to writing on the magnetic tape. A functional description of the data buffer register is given in Paragraph 2.2.

The inputs to the data buffer are shown on Drawing TMA11-0-16. If a read operation is being performed, data is loaded into the buffer from the tape transport data channels. Each channel is connected to one leg of an AND/OR gate. The other leg to the gate is controlled by a flip-flop. The read operation (indicated by READ STB L) sets this flip-flop. The high (1) side of the flip-flop qualifies four of the AND/OR gates to produce the DATA BFR IN BIT H signals for bits 00 through 03. The low (0) side of the flip-flop produces the signals for bits 4 through 7. Thus, during a read operation, the data from the tape channels is gated through to the input of the buffer register and strobed into the register by the DATA BFR STB signals. As shown on the data buffer drawing (TMA11-0-20), the first four bits are strobed in by the DATA BFR STB 1 signal; the second four bits are strobed in by the DATA BFR STB 2 H signal.

During write operations, data from the bus is strobed into the data buffer register. The low byte is applied to one series of gates, the high byte to another series of gates (Drawing TMA11-0-16). Each bus line is applied to one input of a two-input AND/OR gate. The other leg is qualified only if the appropriate byte has been selected. This selection is determined by two AND gates. One is qualified if the current memory address is even (CMA 00 L), which indicates a low byte. The other is qualified if the current memory address is odd (CMA 00 H), which indicates a high byte. The data from the bus lines is then strobed into the register in the same manner as before.

The data buffer output logic is shown on Drawings TMA11-0-14 and TMA11-0-09. The logic shown on Drawing TMA11-0-14 is used when the output of the data buffer is to be applied to the bus. Each output of the data buffer is applied to one leg of a two-input AND gate. The other leg is qualified by either the HI DATA BYTE L or LO DATA BYTE L signal, depending on which byte has been selected.

The logic shown on Drawing TMA11-0-09 is used when the output of the data buffer is to be applied to the tape unit for writing. When the core dump mode *is not used*, one byte in memory corresponds to *one* tape character. In this instance, the output of the data buffer is gated through to the tape transport write lines. Data buffer bits 07 through 00 correspond to lines WD0 through WD7, respectively.

When the core dump mode *is used,* one byte in memory corresponds to *two* tape characters. When the write strobe (WRS) is issued, it sets the even character flip-flop (Drawing TMA11-0-11). This clears the EVEN CHAR L pulse, which gates data buffer bits 00 through 03 to write lines WD7 through WD4 (Drawing TMA11-0-11). The flip-flop then clears, and asserts EVEN CHAR L which gates bits 04 through 07 to lines WD7 through WD4, respectively.

During normal read operations, all six tape data channels are read and gated through the data buffer input logic for loading into the data buffer register. When the core dump mode is used, however, the logic operates in a different manner because one byte consists of two 4-bit characters. It is therefore necessary to read tape channels 0–3 twice, loading the first tape character into the low part of the buffer register and the second tape character into the high part of the buffer. This is accomplished by the logic shown on Drawing TMA11-0-16.

When the first tape character is read, the AND/NOR gates having channels 0–7 as inputs are all qualified by the output of the READ STB flip-flop, and the data from the tape is gated through to become DATA BFR IN BITS 0–7. These bits are strobed into the data buffer register by DATA BFR STB 1 and 2 as shown on Drawing TMA11-0-20. Up to this time, data has been read from the tape in a normal manner.

When the next tape character is read, the first set of AND/NOR gates is still qualified and produces DATA BFR IN BITS 0–3. However, these bits are not loaded into the buffer register, because the required strobe signal is no longer present. The low part of the buffer, thus, contains data read from channels 0–3 of the previous tape character.

The second series of AND/NOR gates, which normally receives inputs from tape channels 4–7, are now inhibited due to the CORE DUMP L signal. The other AND inputs to these gates, which receive data from tape channels 0–3, are now qualified by an enabling AND gate having CORE DUMP L as an input. As a result, this series of gates causes the data from tape channels 0–3 to become DATA BFR IN BITS 4–7. These bits are strobed into the high part of the buffer and override the data previously stored in this part of the buffer. Thus, the two 4-bit characters are now in the buffer as a single 8-bit byte.

3.7.7 TS03 Read Lines (MTRD)

The TS03 read lines are assigned a standard bus address and are activated by the address select logic. When these lines are selected for use, data from the lines is gated to appropriate data bits on the bus, as shown on Drawing TMA11-0-14. The 16 bits that constitute the read lines are read-only bits with the exception of the character select (CHAR SEL) and bad tape error generator (BTE GEN) bits (bits 14 and 13, respectively). Bits 15 through 13 are described below; bits 11 through 09 are unused; and the remaining bits are described in Paragraph 2.2.

Bit 15 is the timer bit, which is used for diagnostic purposes by measuring the time duration of the tape operations. The timer logic is shown on Drawing TMA11-0-06. This logic produces the timer signal (TIMER H), which is a 100-μs signal with a 50 percent duty cycle.

Bit 14 is the character select bit, which is used to select the last character of a record that is to be loaded into the data buffer. When this bit is loaded with a 1, the last character loaded into the buffer is the LRC character. When this bit is loaded with a 0, the last character loaded in the buffer is the CRC character.

Bit 13 is the bad tape error generator, which is used to check the bad tape error logic. When loaded with a 1, this bit sets the CU READY flip-flop, thereby causing a premature gap shutdown period. When this portion of the tape is then read, it produces a bad tape error indication.

Bit 12 is the gap shutdown bit. It is a read-only bit and indicates a gap shutdown period when it is a 1.

Data on the TS03 read lines is gated to the bus by the logic shown on Drawing TMA11-0-14. When the read lines are selected for use (SEL 5 IN L), an inverter output qualifies one leg of a series of gates. The other leg of each gate is connected to one of the channels in the tape transport. The output of these gates are then fed through drivers to the bus.

3.8 TAPE CONTROL

The TMA11 Controller performs four tape control functions: unit selection, function control, ready control, and start control.

3.8.1 Unit Selection

The unit selection logic determines which tape transport is to be used to perform the designated operation. Although two tape transports may be handled by one controller, only one transport may be selected at any given time. The tape transport selected is determined by bits 10 through 08 of the command register as shown on Drawing TMA11-0-10. These bits are set or reset in accordance with program inputs on bus data lines D10, D09, and D08 each time the register flip-flops are clocked by SEL 1 OUT HI. The register outputs are then applied to decoder logic in the master tape transport via select lines SEL 2, SEL 1, and SEL 0. Because only two transports can be connected to each TMA11, the master tape transport decoder logic only accepts two octal codes as legal unit select line inputs. Octal code 000 selects transport number 0; octal code 001 selects transport number 1. Any other octal codes place both transports in the deselect mode so that no tape operations can be performed.

3.8.2 Function Control

The function control logic specifies which of eight functions is to be performed by the selected tape transport. A description of each of the eight functions is given in Table 3-1. The function selected is determined by bits 03 through 01 of the command register as shown in Drawing TMA11-0-07. These bits are set or reset in accordance with program inputs on bus data line D03, D02, and D01 each time register flip-flops are clocked by SEL 1 OUT LO. The flip-flop outputs are applied to a binary-to-octal decoder which decodes the eight functions. The selected function line is then asserted to the master tape transport.

3.8.3 Ready and Start Control

The TMA11 ready and start control circuits basically consist of the logic associated with two bits in the command register. The ready logic is controlled by the CU RDY bit (bit 07) and is described in detail in Paragraph 3.7.2.6. The start control logic is the GO bit (bit 00) and is described in Paragraph 3.7.2.10.

3.9 TIMING DIAGRAMS

Timing diagrams of various tape operations are shown in Figures 3-5 through 3-10. These diagrams portray specific tape operations such as reading a record of three data characters, etc. The purpose of these diagrams is to illustrate overall TMA11 operation as described in previous paragraphs.

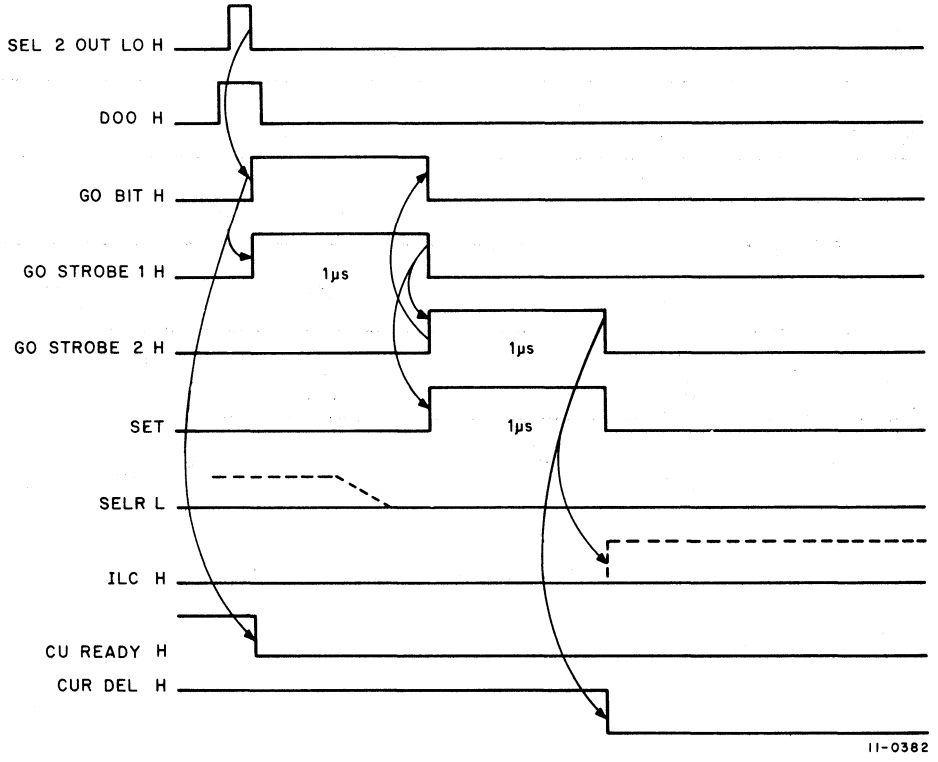

Figure 3-5 Start of Tape Operation

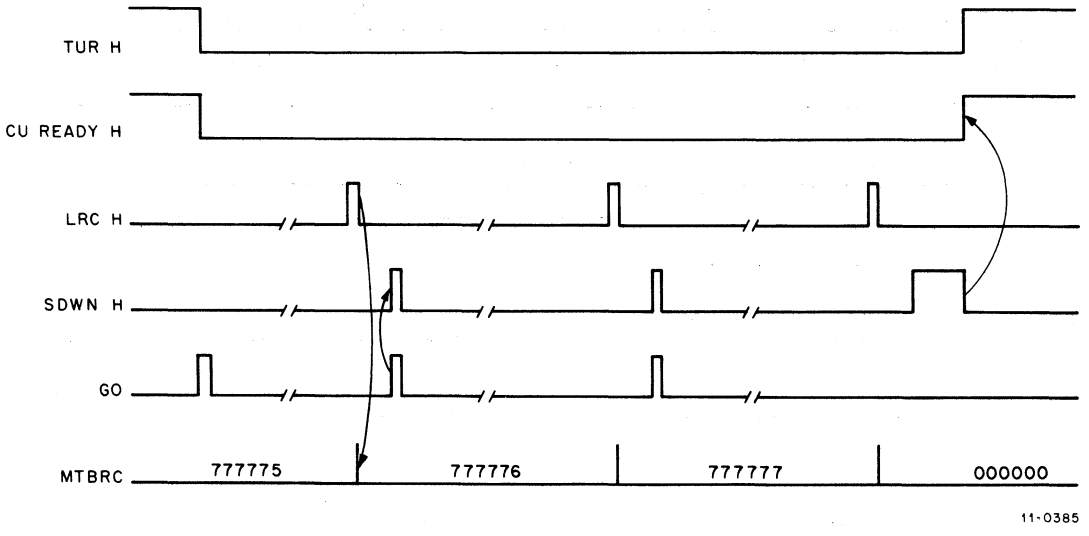

Figure 3-6 Spacing Forward Three Records

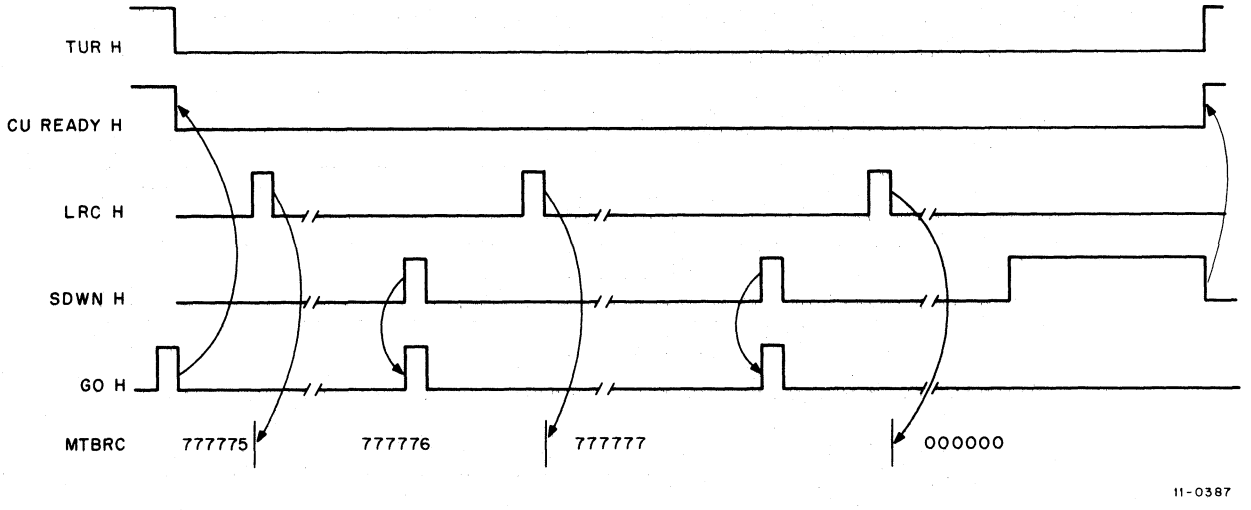

Figure 3-7 Spacing Reverse Three Records

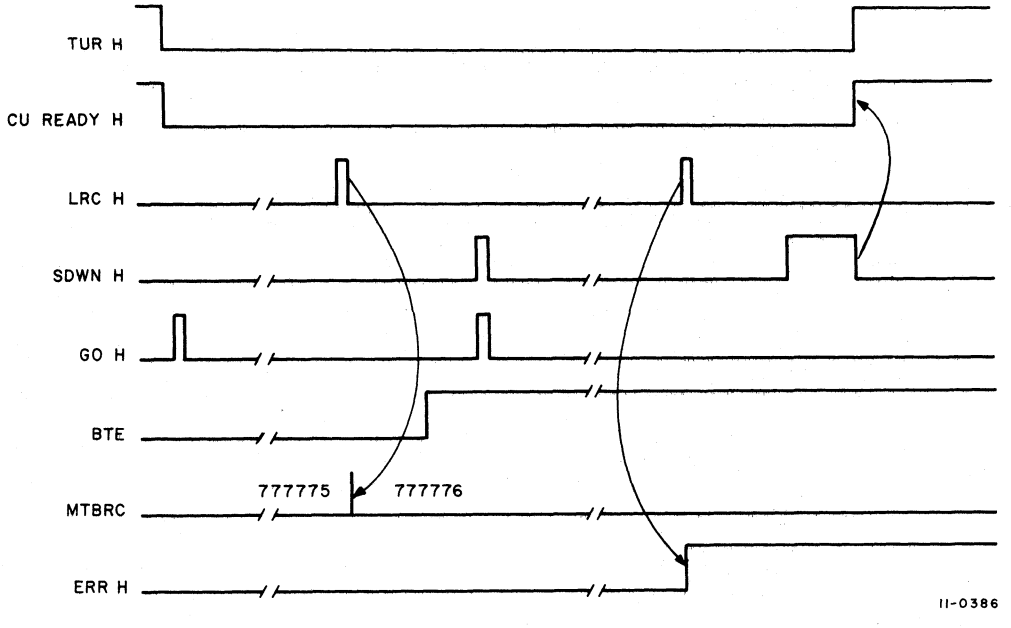

Figure 3-8 Spacing Forward Three Records, Bad Tape Error Appearing in First Record

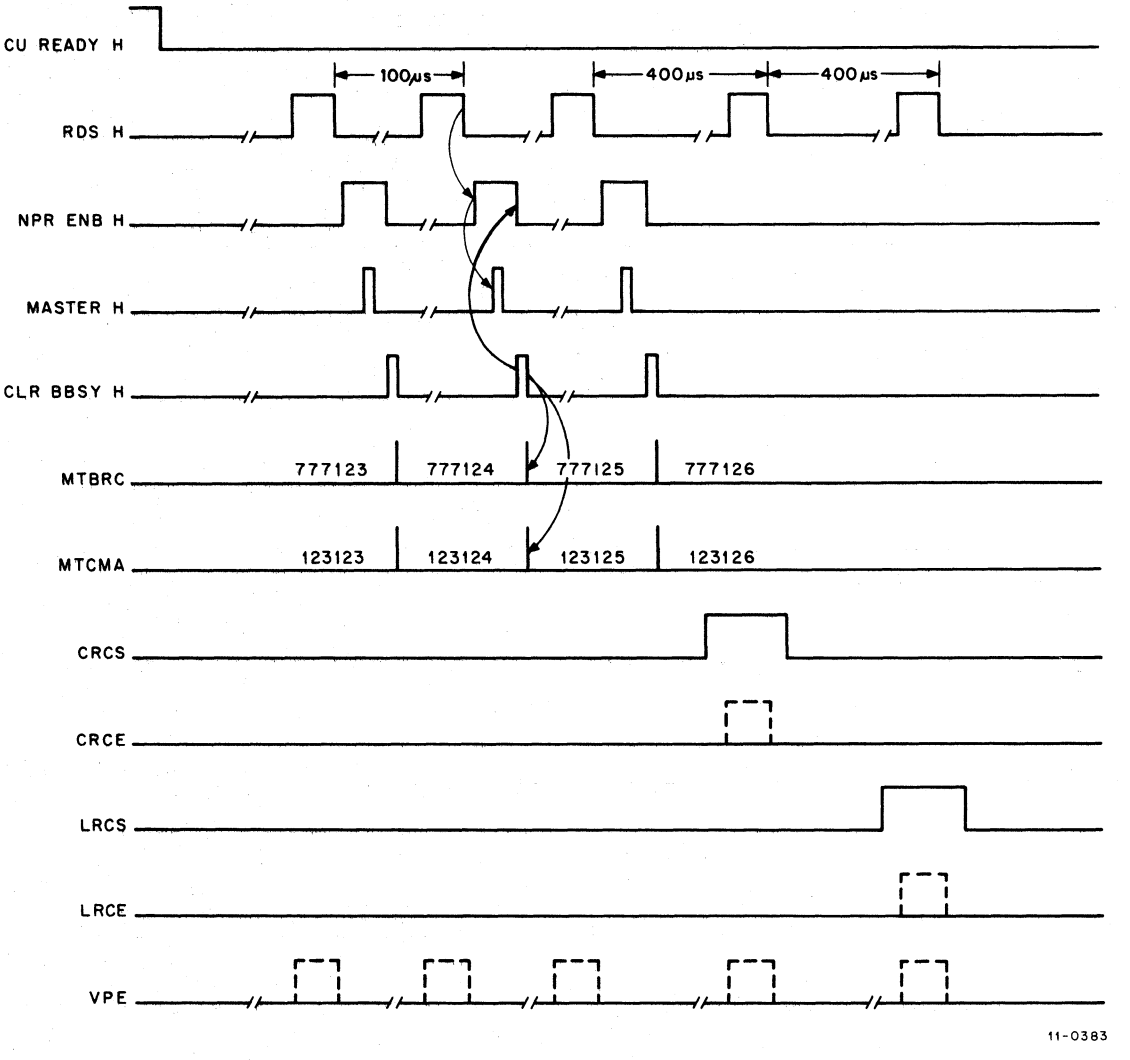

Figure 3-9 Reading Record of Three Data Characters

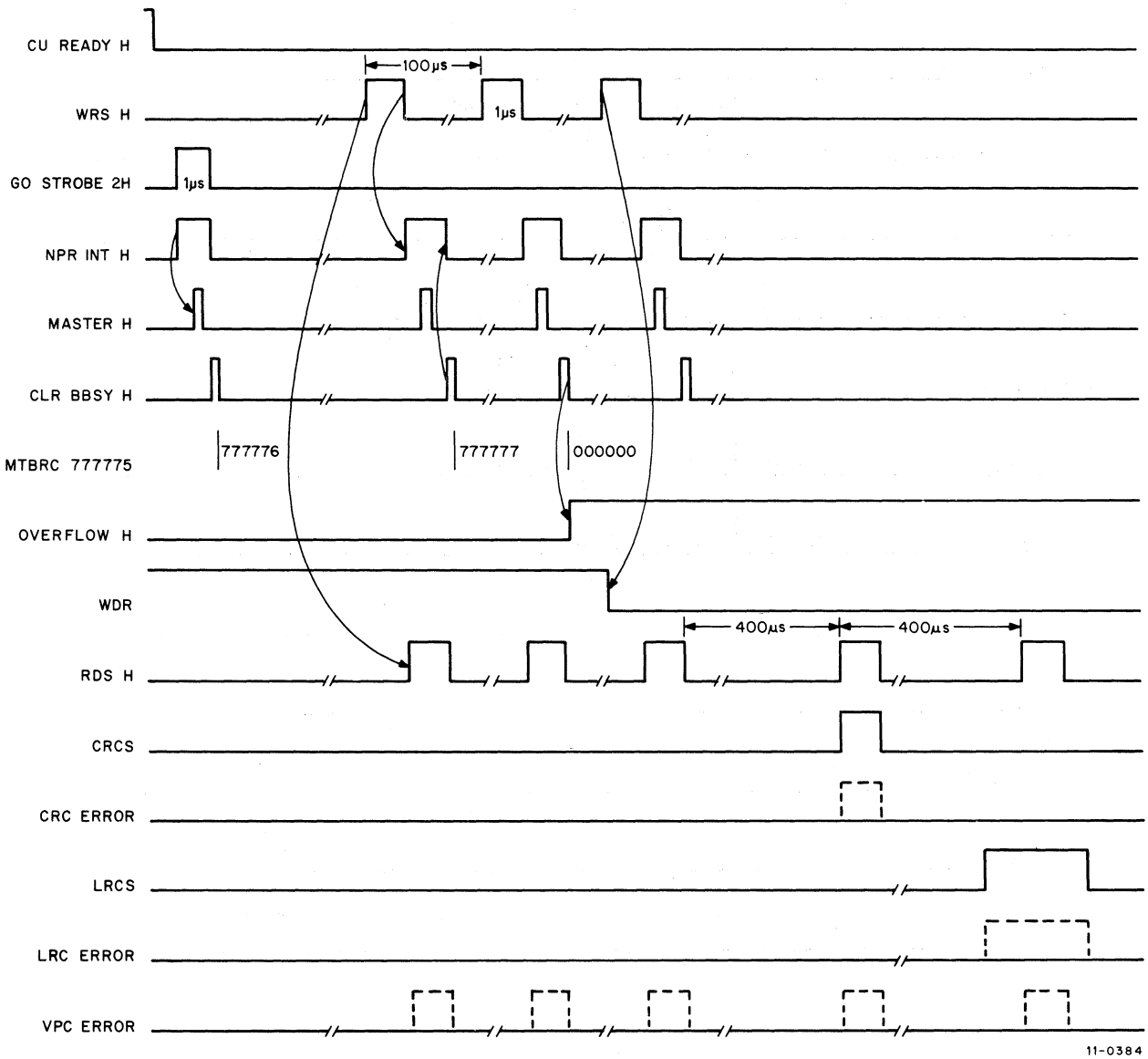

Figure 3-10 Writing Record of Three Data Characters

CHAPTER 4
MODULE DESCRIPTION

4.1 INTRODUCTION

This chapter provides information on the logic modules used in the TMA11 DECmagtape Controller. The position of the modules within the mounting box is shown on Drawing TMA11-0-02.

A list of all TMA11 Controller modules is presented in Table 4-1. This table lists the modules in numerical order, the quantity of each type used in the system, and the name of the module. The last column indicates the DEC document containing the detailed description of that particular module.

Note that it is beyond the scope of this manual to provide information on any of the modules used in the master tape transport logic.

4.2 DEC LOGIC

Except for cable and jumper modules, all of the modules used in the TMA11 Controller are M-series logic modules. The M-series are high-speed, monolithic integrated circuit modules, employing TTL logic (transistor-transistor logic). These circuits provide high-speed, high-fanout, large-capacitance drive capability, and excellent noise margins.

A general description of DEC logic and detailed circuit descriptions of TTL logic gates are provided in DIGITAL's *1973-74 Logic Handbook.*

4.3 MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gated pulse amplifier of the series under test and with the output loaded with gates of the same series. Percentages are assigned as follows: 0 percent is the initial steady-state level, 100 percent is the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately. Rise time and fall time is measured from 10 percent to 90 percent of waveform change, rising or falling.

4.4 LOADING

Input loading and output driving are specified in *unit loads,* where one unit load is 1.6 mA by definition. The inputs to low-speed gates usually draw one unit load. High-speed gates draw 1-1/4 unit loads, or 2 mA.

Table 4-1
Module Utilization

Module Number	Quantity Used	Title	Reference
M105	1	Address Selector	1
M111	5	Inverter	2
M112	3	NOR Gate	2
M113	7	Ten 2-input NAND Gates	2
M115	2	Eight 3-input NAND Gates	2
M117	1	Six 4-input NAND Gates	2
M121	2	AND/NOR Gate	2
M127	3	2-2-2-3 AND/NOR Gate	–
M149	4	9x2 NAND Wired OR Matrix	–
M163	1	Dual Binary-to-Octal Decoder	–
M203	1	Eight Reset/Set Flip-Flops	2
M205	2	Five "D" Flip-Flops	2
M216	5	Six Flip-Flops	–
M239	1	Three 4-bit Counter Registers	–
M304	2	Four One-Shot Delays	–
M307	1	Integrating One-Shot	–
M627	3	NAND Power Amplifier	2
G736	1	Jumper Module	1
M7821	1	Interrupt Control	1
M784	1	Unibus Receiver	1
M785	1	Unibus Transceiver	1
M7854	1	OPI Module	1
M795	1	Word Count and Bus Address Register	1
M796	1	Unibus Master Control	1
M797	1	Register Selection	1
M798	1	Unibus Drivers	1

REFERENCES

1. *PDP-11 Peripherals Handbook*
2. *DIGITAL's 1973-1974 Logic Handbook*

APPENDIX A
MASTER TAPE TRANSPORT SIGNALS

A.1 SIGNALS FROM TS03 TO TMA11 CONTROLLER

Mnemonic	Name
RD0 – RD7	Read data signals.
RDP	Read parity bit.
SDWN	Tape settle down. This is the time between a stop command and the actual stopping of the tape.
TUR	Tape unit ready. This signal is true when the selected tape unit is stopped and SELR is true.
SELR	Select remote. This is true when unit is selected and is on-line.
RWS	Rewind status. This is true when selected unit is rewinding.
7CH	7-channel. Always false.
WRL	Write lock. Prevents writing on tape.
BOT	Beginning of tape.
EOT	End of tape.
WRS	Write strobe. Requests a character for writing.
RDS	Read strobe. Present for both read and write operations.
FMK	File mark.
CRCS	CRC strobe. Appears with CRC character.
LRCS	LRC strobe. Appears with LRC character.
VPE	Vertical parity check error. Sampled with RDS.
LRCE	Longitudinal redundancy check error. Sampled with LRCS.
CRCE	Cyclic redundancy check error. Sampled with RDS.

A.2 SIGNALS FROM TMA11 CONTROLLER TO TS03

Mnemonic	Name
WD0 – WD7	Write data lines.
SET	Required to start any tape operation (derivative of GO command).
FWD	Tape forward.
REV	Tape reverse.
RWD	Tape rewind
WRE	Write enable.
PEVN	Even parity.
DEN 8	Density bit. True for 800 bpi 9-channel. } See Note
DEN 5	Density bit. True for 800 bpi 9-channel. } See Note
WFMK	Write file mark.
WXG	Write-extended-IRG. True for both write-extended-IRG and WFMK functions.
SEL 0 SEL 1 SEL 2	Tape unit select.
WDR	Write data ready.
CINIT	Initialize.

NOTE

TS03 ignores DEN 8/5 input signals; it always operates at 800 bpi, 9-channel.

PART III
TS03 DECmagtape TRANSPORT

CHAPTER 1
GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The TS03 DECmagtape Transport is a synchronous digital tape unit capable of reading and writing industry-compatible tapes and read-after-write operation. The unit is designed for applications requiring high reliability at moderate tape speeds. Typical applications include operation with minicomputers, high-speed data collection systems, and computer peripherals.

The TS03 contains all the electronics necessary to accept, format, and record data and to retrieve, check, and output data. To accomplish this, the TS03 performs the following functions:

Tape motion control
Tape formatting
Parity generation
Cyclic redundancy check (CRC) character generation
Longitudinal redundancy check (LRC) character generation
Interrecord gap control
Even parity zero character conversion
Status monitoring
Parity, CRC character, and LRC character error detection
File protection

The TS03 is a 9-track, 800 bpi unit with a standard tape speed of 12.5 in. per second and a data transfer rate of 10 kHz.

1.2 PHYSICAL DESCRIPTION

The transport portion of the TS03 is completely housed in a 19 in. wide by 17 in. deep by 9 in. high chassis; the adapter portion is contained on a hex height module which mounts just below the chassis in a special mounting bracket. The transport (Figure 1-1) contains the read/write and motion control electronics. The adapter module (Figure 1-1) contains the formatting, parity, CRC, gap control, and error detection electronics.

1.3 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Tape (Computer Grade)	
Width	0.5 in. (1.27 cm)
Thickness	1.5 mils (0.038 mm)
Tension	8.0 oz (227 g)
Reel Diameter	To 7.0 in. (17.78 cm)
Capacity	600 ft (182.40 m)
Reel Hub	3.69 in. (9.37 cm) dia. (per industry standards)

Reel Braking	Dynamic
Recording Mode (Industry-Compatible)	NRZI
Tape Drive	Single capstan
Tape Speed	12.5 in./sec
Instantaneous Speed Variation	±3%
Long-term Speed Variation	±1%
Start/Stop Displacement	0.1875 in. (0.476 cm)
Start/Stop Time at 12.5 in./sec	30 ms
Rewind Speed	75 in./sec (190.5 cm)
Magnetic Head Assembly (Write to Read Gap Displacement)	
Dual Gap Nine-Track Read After Write	0.15 in. (0.38 cm)
Interchannel Displacement Error (Measured with Master Skew Tape)	
Write	150 μin. (3.8 μm) maximum
Read	150 μin. (3.8 μm) maximum
Erase Head	Full width
Load Point and End-of-Tape Reflective Strip Detection (Industry-Compatible)	Photoelectric
Broken Tape Detection	Photoelectric
Dimensions (Figure 1-2)	
Transport Mounting (Horizontal)	Standard 19 in. (48.26 cm) RETMA rack
Height	8.72 in. (22.14 cm)
Width	19.00 in. (48.26 cm)
Depth (From Mounting Surface)	14.38 in. (36.53 cm)
Depth (Overall)	16.88 in. (42.88 cm)
Weight	35 lb (15.85 kg)
Shipping Weight	45 lb (20.38 kg)
Operating Environment	
Ambient Temperature	+2° to +50° C
Relative Humidity (Noncondensing)	15% to 95%
Altitude	To 30,000 ft (9120 m)
Power Requirements	115/230 Vac, 50 to 500 Hz, single phase 200 VA nominal; 300 VA maximum

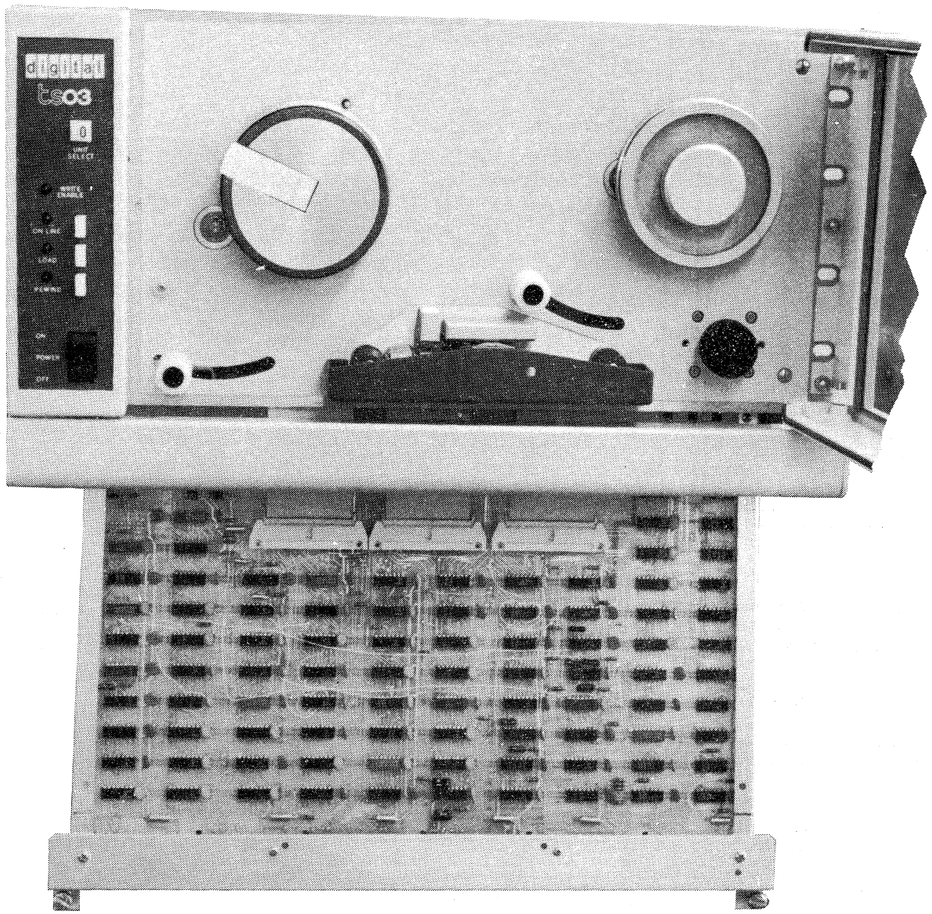

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Figure 1-1 TS03 Transport and TS03 Adapter Module (M8920)

NOTE: DIMENSIONS FIRST SHOWN ARE IN INCHES.
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS.

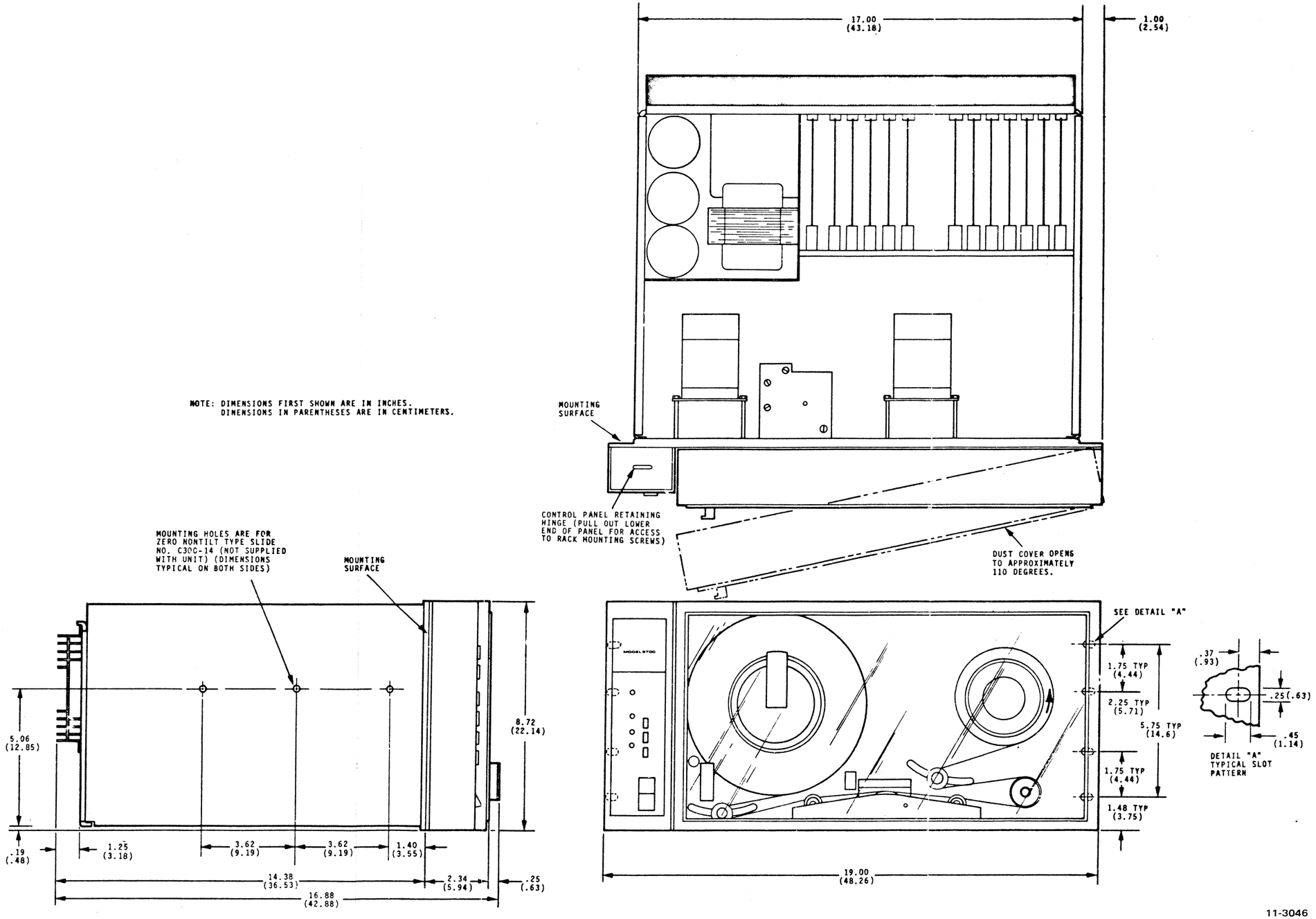


Figure 1-2 TS03 Transport
Physical Dimensions

CHAPTER 2
THEORY OF OPERATION

2.1 INTRODUCTION

This chapter provides a complete description of the TS03 to the functional block level. Functionally, the TS03 can be divided into four major blocks (see Figure 2-1):

Adapter Logic
Transport Control Logic
Servo System
Data Section

The adapter logic interfaces the TS03 transport to the controller. In response to commands from the controller, the adapter:

1. Formats the data on the tape.
2. Generates motion signals to start and stop the tape drive, to move the tape forward or backward, and to move the tape at normal read/write speed or at a higher speed during a rewind operation.
3. Generates strobes to write data and CRC, LRC, and file mark characters on tape.
4. Generates write strobes to notify the controller to send the next write character.
5. Transmits read strobes received from the tape transport out to the controller.
6. Generates parity and the CRC characters for recording on the tape.
7. Performs parity, CRC, and LRC error checks on all read data.
8. Detects file mark records on the tape and notifies the controller.

The control logic:

1. Controls ramp voltage to the servo, thereby controlling direction and speed of tape movement.
2. Generates control signals to the data section which enable and disable the read and write amplifiers.
3. Controls the erase head.

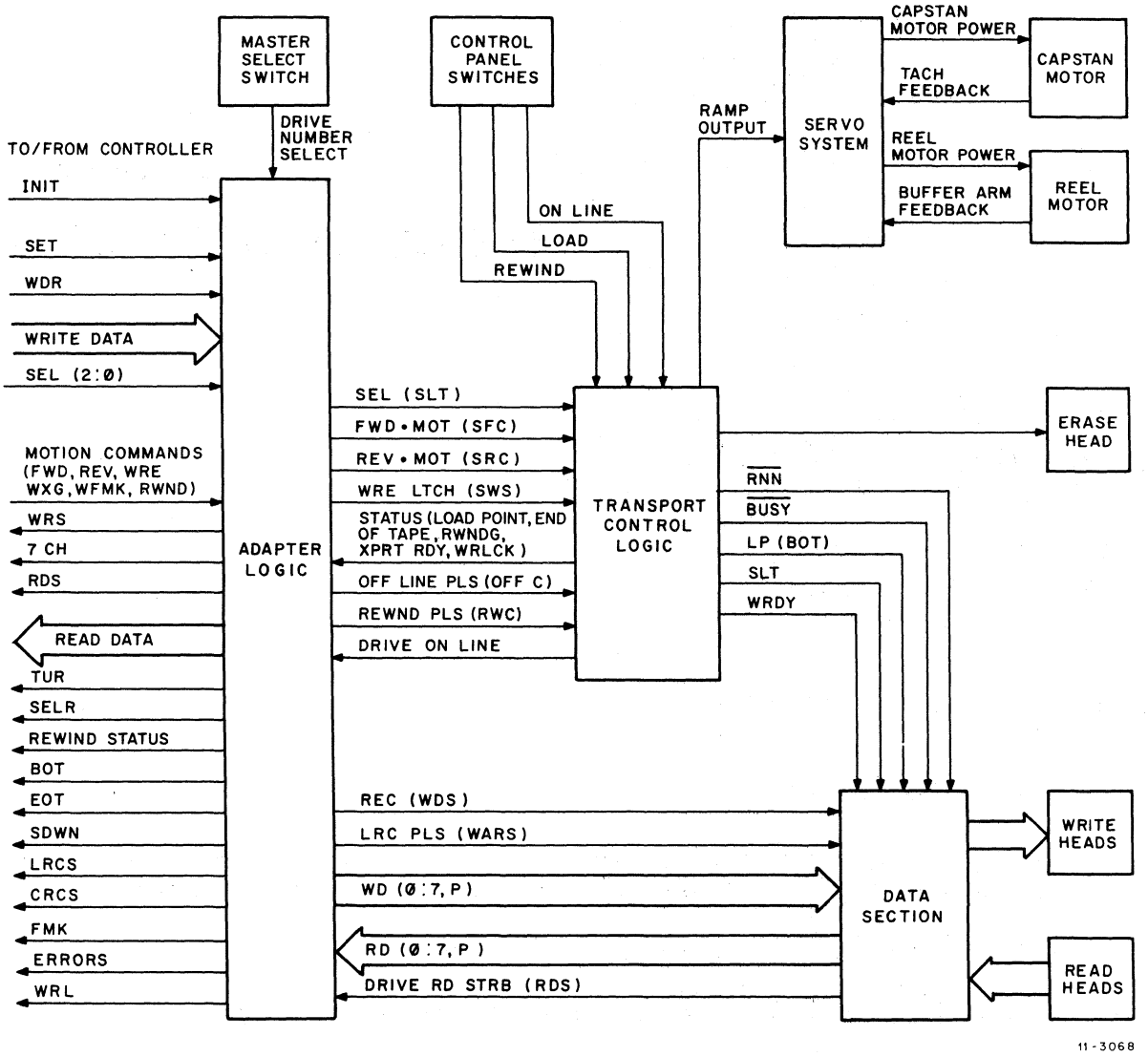


Figure 2-1 TS03 Block Diagram

The servo system consists of the electronics and electromechanical components that are required to advance the tape past the magnetic heads at accurately controlled speeds while maintaining constant tape tension. The servo system is composed of two subsystems: the capstan subsystem, which drives the tape at accurately controlled speeds, and the reel servo subsystem, which maintains constant tape tension.

The data section consists of read and write amplifiers, output drivers, and timing and control logic. The data section controls the read/write heads and generates a read data strobe that is used by the adapter logic to transfer data out to the controller.

2.2 TRANSPORT OPERATIONS

The TS03 performs three basic types of operations: write, read and rewind; all other operations are simply variations. The following paragraphs explain how these operations are performed (Figure 2-1).

Once the controller initializes the adapter logic by asserting INIT, the controller must select the transport (drive 0 or 1) and parity sense (odd or even) before any operations can be performed.

When the controller selects a transport via the SEL lines, the adapter asserts SEL (select) to the selected transport and, if the transport is on-line (ON LINE indicator illuminated), DRIVE ON-LINE is asserted to the adapter and the adapter asserts SELR (select remote) back to the controller. If the selected transport is ready [i.e., tape is loaded and is not rewinding or advancing to the load point (BOT marker)], the transport also asserts XPRT RDY (transport ready) to the adapter, causing the adapter to assert TUR (tape unit ready) to the controller. With these conditions satisfied, the controller can now raise the command lines required to perform a given operation and asserts SET to initiate that operation.

2.2.1 Write Operation

To perform a write operation, the controller raises WRE (write enable) and FWD (forward) and asserts SET. The adapter logic responds by asserting FWD•MOT (forward motion) and WRE LTCH (write enable latch) to the transport control logic, begins to count off a delay, and clears TUR to the controller. The transport logic responds by asserting WRDY (write ready) and SLT (select) to the data section and a ramp-up, forward motion voltage to the servo system. Hence the servo system starts moving the tape forward at normal speed and the data section is enabled. The adapter then completes the delay count. (The delay allows the tape to accelerate to normal operating speed and ensures that the heads have moved well past the BOT marker when starting from a BOT position.) Assuming the controller will have placed a character on the write data lines and asserted WDR (write data ready) to the adapter when the delay expires, the adapter immediately generates a parity bit and a write strobe (REC) to load the data character with parity into the data section. The data section immediately records the character, reads it back, and places it on the read data lines to the adapter along with a read strobe. The adapter then checks the read character for parity errors and outputs the character back to the controller, along with a read strobe (RDS). The adapter then asserts a write strobe (WRS) to the controller to request the next character. The controller then places the next character on the write data lines. This process is repeated over and over until the last character is recorded and the controller clears WDR.

When WDR clears, the adapter generates two more write strobes to properly terminate the record. REC is asserted along with the CRC character to the data section for recording. Then the LRC PLS is generated to the data section to generate the LRC character, which is then recorded. The adapter reads the two check characters, outputs them to the controller, along with the CRC and LRC strobes (CRCS and LRCS), and checks for CRC and LRC errors. If a CRC or LRC error is detected, the respective error line is also asserted to the controller.

Next, the adapter terminates the write operation by clearing FWD•MOT to the transport control logic, asserting SDWN (settle down) to the controller and counting off deceleration delay. When FWD•MOT clears, the transport control logic applies a ramp-down voltage to the servo system and clears the WRDY and SLT lines to the data section. Hence the servo system stops the tape and the data section stops writing and reading data.

When the deceleration delay expires, the adapter asserts TUR and clears SDWN to the controller. Thus the TS03 is ready to perform the next operation.

2.2.2 Read Operation

To perform a read operation, the controller raises FWD and asserts SET. The adapter logic responds by asserting FWD•MOT to the transport control logic, starting the delay count and clearing TUR. The transport control responds by asserting SLT to the data section and a ramp-up voltage to the servo system. The servo system then begins to move the tape forward, and the read portion of the data section is enabled. The adapter completes the delay count and begins to accept read data, along with read strobes from the data section. Each character read is checked for a parity error and output to the controller, along with a read strobe. Upon reading the final two characters (normally a CRC and LRC character) and checking for errors, the adapter clears FWD•MOT, asserts SDWN to the controller, and begins to count off a deceleration delay. When FWD•MOT clears, the transport control logic applies a ramp-down voltage to the servo system to stop tape motion and clears the SLT line to the data section to stop reading.

When the deceleration delay expires, the adapter asserts TUR and clears SDWN to the controller.

2.2.3 Rewind Operation

To perform a rewind operation, the controller asserts RWND (rewind) and SET. The adapter logic responds by asserting REWND PLS to the transport control logic. The transport control logic responds by clearing XPRT RDY, asserting RWNDG to the adapter and applying a high-speed reverse, ramp-up voltage to the servo system. The adapter asserts RWS (rewind status) to the controller while the servo system rewinds the tape past the load point. The transport control logic then applies a forward motion ramp-up voltage to the servo system, which moves the tape forward to the load point and stops the tape. The transport control logic then clears RWNDG and asserts LOAD POINT and XPRT RDY to the adapter. The adapter clears RWS and asserts TUR to the controller.

2.3 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

2.3.1 Adapter Logic

Figure 2-2 is a block diagram of the adapter logic. The diagram separates the adapter logic into six areas and shows adapter data and signal flow.

As stated previously, the adapter logic enables software control of the TS03 DECmagtape Transport. Referring to Figure 2-2, note that the control logic responds to inputs from the controller by generating control signals for the write logic and the read logic as well as control signals for the tape transport. These control signals control the reading and writing of data, tape motion, and interrecord gaps. In addition, the control logic provides clock signals (TIME PLS 1,0) for the adapter logic, monitors transport status lines, and initializes the adapter logic whenever INIT is asserted by the controller.

In response to inputs from the control logic and the controller, the write logic and read logic transfer data to and from the tape transport. The write logic accepts write data from the controller and monitors the controller C WDR (write data ready) line. If the C WDR line is true, the write logic generates parity, write strobes (REC), CRC characters, LRC strobes (LRC PLS), and the file mark character and outputs this information to the tape transport via the transport drivers for recording. The read logic accepts read data from the transport and monitors the RD STRB line. Using RD STRB and the read data, the read logic detects data records and file mark records. In addition, checks are made for parity, CRC, and LRC errors.

2.3.1.1 Control Logic – The control logic can be divided into nine logic sections (Figure 2-3). Each section performs a specific function in performing the eight different operations the control logic is capable of. Table 2-1 lists those operations and indicates the commands that must be issued by the controller to initiate them.

To prepare the control logic to receive commands, the controller asserts C INIT. Asserting C INIT generates SYSTEM RESET, which clears the command status register and resets the motion flip-flop in the read/write control logic.

The controller then issues the commands by asserting the command lines and generating a C SET pulse. The command processing sequence that results is illustrated in Figure 2-4. Note that different operations require that different delays be generated by the delay counter (Table 2-2). These delays are incorporated for the following reasons:

1. To allow time for the tape to accelerate to normal operating speed from a stopped condition.
2. To allow time for the tape to decelerate from normal operating speed to a stopped condition.
3. To allow time for the transport to move the tape BOT marker well past the read/write heads when starting from the BOT position.
4. To enable the writing of industry-compatible extended interrecord gaps and file marks.

Note that the rewind operation does not require a delay.

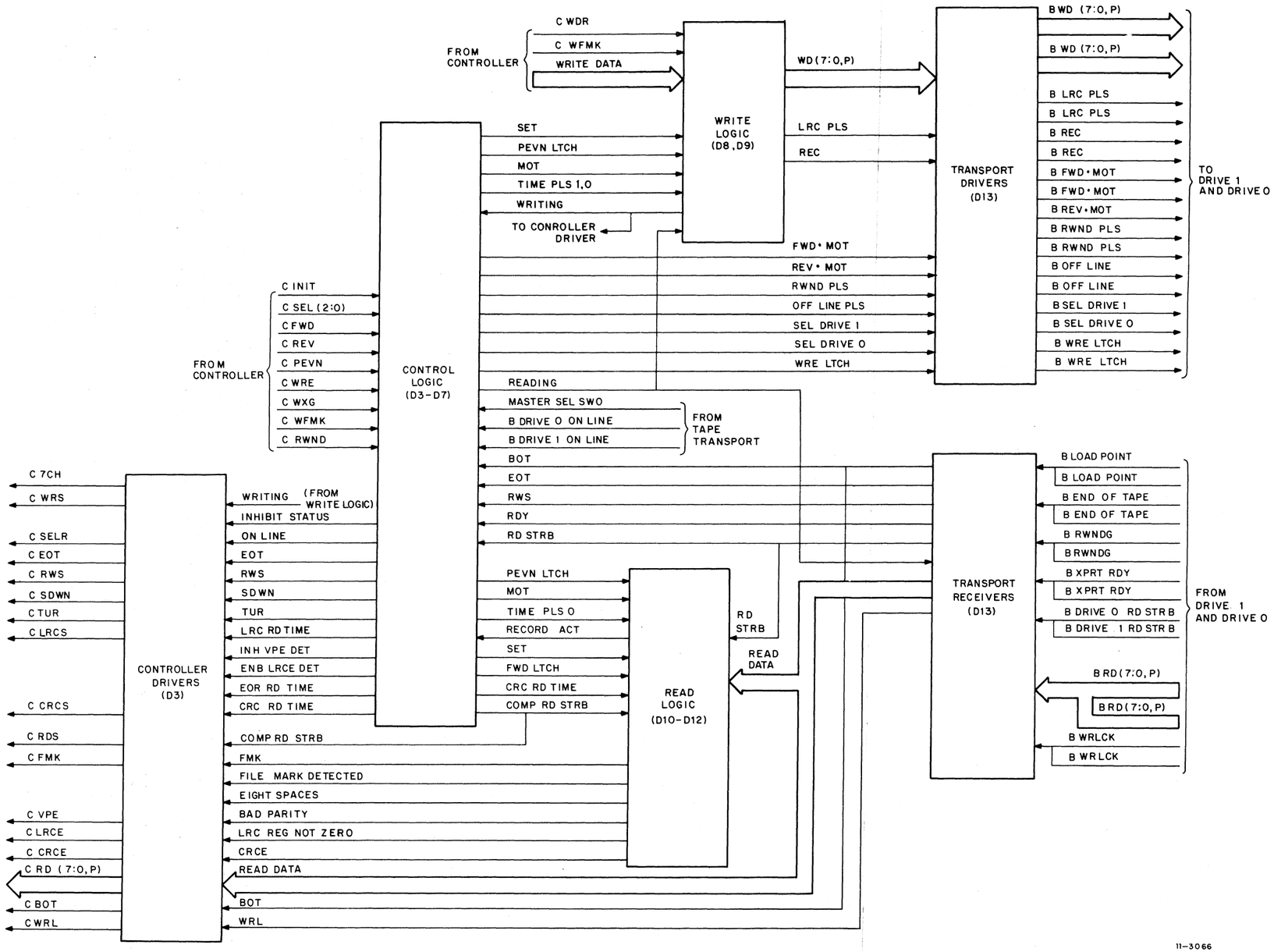


Figure 2-2 Adapter Block Diagram

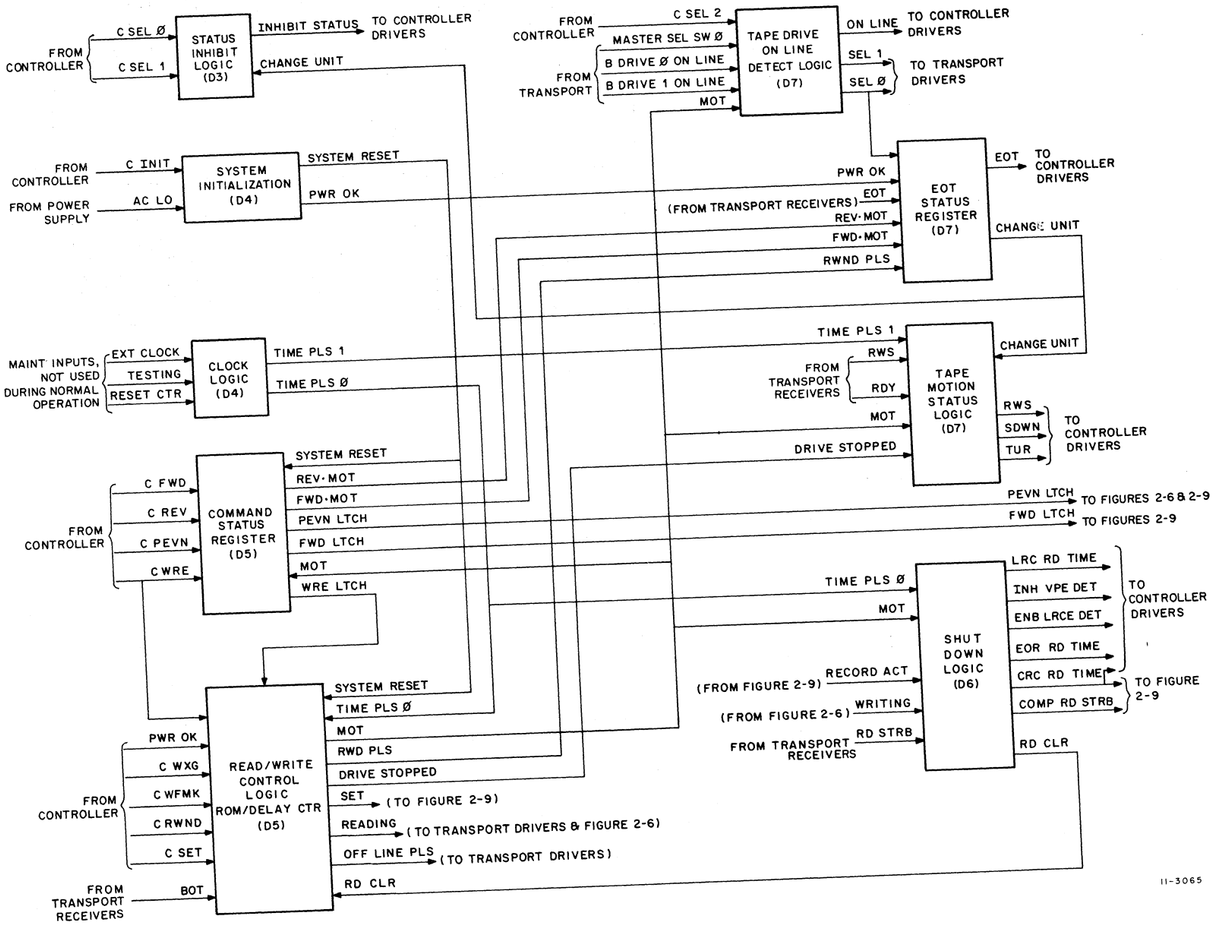


Figure 2-3 Control Logic Functional Block Diagram

Table 2-1
Operations Versus Commands Required

Operations	Controller Commands Required					
	Write Extended Gap (WXG)	Write File Mark (WFMK)	Write Enable (WRE)	Forward (FWD)	Reverse (REV)	Rewind (RWND)
Rewind, Off-Line			X			X
Rewind						X
Write			X	X		
Write-with-extended Interrecord-Gap	X		X	X		
Write File Mark		X	X	X		
Read				X		
Space Forward				X		
Space Reverse					X	

Table 2-2
Commands and Corresponding Delays

Commands	ROM Address	2s Complement of Delay	Delay (ms)	Delay (in.)
(WTMK + WXG)•BOT	14_8	20000	819.2	10.05
WRE•FWD•BOT	16_8	25000	563.2	6.85
(WTMK + WXG)•$\overline{\text{BOT}}$	4_8	31400	332.8	3.97
FWD•BOT	12_8	33400	256.0	3.01
WRE•FWD•$\overline{\text{BOT}}$	6_8	37230	35.7	0.256
FWD•$\overline{\text{BOT}}$	2_8	37423	23.7	0.117
STOP•WRE	24_8, 26_8	37754	2.0	0.025
STOP•$\overline{\text{WRE}}$	20_8, 22_8	37777	0.1	0.001

Due to the similarities of the eight operations performed by the control logic, the following paragraphs will first explain a write operation and then point out the differences between a write operation and the other operations.

Write Operation (Figure 2-5) – To initiate a write operation, the controller must raise the C WRE and C FWD lines and issue the C SET pulse. Assuming the tape is positioned at the BOT marker, the control logic responds to these inputs by presetting the delay counter to 25000 and then asserting MOT, WRE LTCH, and FWD•MOT and clearing TUR. When FWD•MOT asserts, the transport begins to move the tape forward while the delay counter counts off the delay period. The transport actually moves the tape forward 6.85 in. before the delay period expires. This distance ensures that the tape has reached operating speed and is well past the BOT marker and that start-up transients and noise have subsided. When the delay period expires (counter equals 40000), the READING line asserts, enabling the read and write logic. When the controller raises the C WDR (write data ready) line a write strobe (REC) is generated and the data is actually written on the tape. A write strobe (C WRS) is sent to the controller

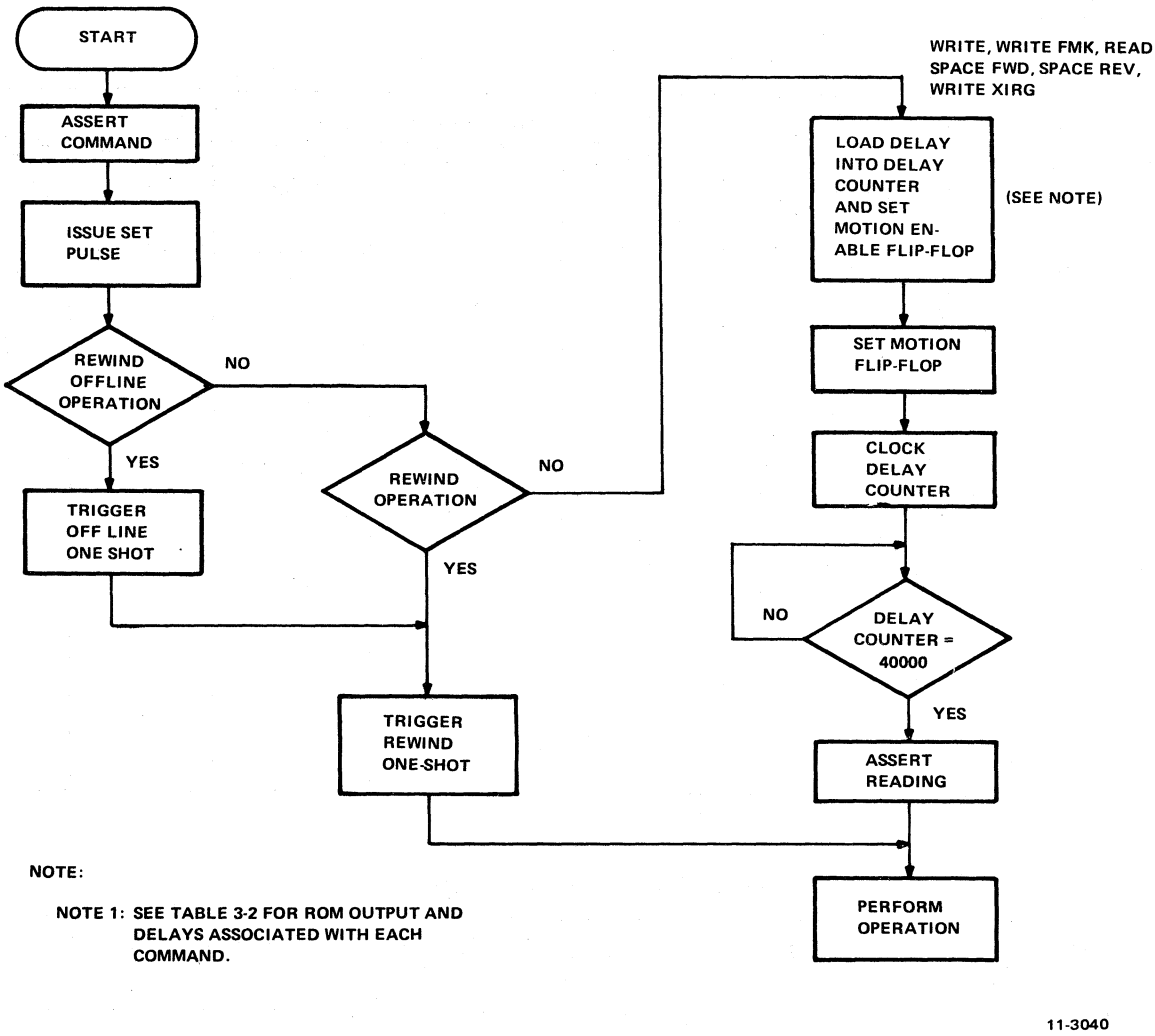


Figure 2-4 Commands Processing Sequence Flow Diagram

50 μs later, requesting the next character. While the write head records the data, the read head reads the data back. Each time the read head detects a character, a RD STRB (read strobe) is sent back to the read logic. Upon receiving three read strobes (minimum record length), the read logic asserts RECORD ACT to the shutdown logic. The recording operation then continues until all the data is recorded and the controller clears the C WDR line. When C WDR is cleared, WRITING (which is controlled by the write logic, Figure 2-6) clears and the shutdown logic is enabled.

When the shutdown logic detects a gap three character times long between successive read strobes, CRC RD TIME is asserted to the read logic and the controller drivers. If the record was recorded correctly, the next two characters detected by the read head should be the CRC character and the LRC character in that order. The read strobe resulting from the CRC character clears CRC RD TIME and asserts LRC RD TIME to the controller drivers. The read strobe resulting from the LRC character clears LRC RD TIME and eight character times later the shutdown logic asserts RD CLR. If the CRC and LRC characters are not detected by the read head, the RD STRB will be generated internally by the shutdown logic; however, the shutdown will wait 56 character times instead of the normal 8 before asserting RD CLR. The extra delay is provided to ensure that the read head has passed the end of the record before the tape stops in the event of a bad tape spot or a write circuitry malfunction.

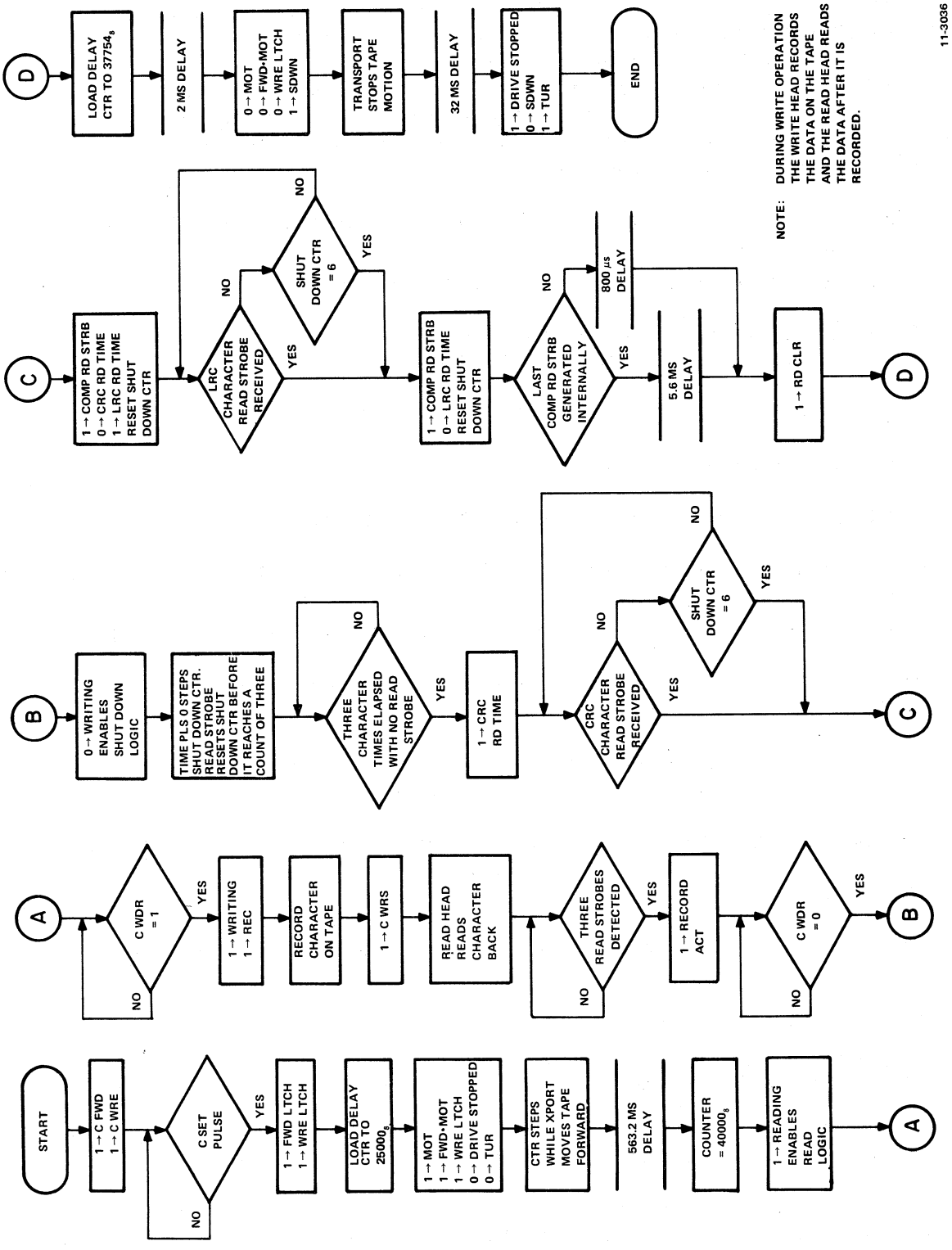


Figure 2-5 Control Logic BOT Write Operation Flow Diagram

The assertion of RD CLR loads the delay counter for a delay and clears READING. In this case, because it was a write operation, the counter is set for a delay of 2 ms. In the case of read operations, the counter is set for a 0.1 ms delay. A smaller delay is used during a read operation to ensure that any unwanted data that may be written on the tape by the write heads while turning off is erased. When the delay expires, the read/write control logic clears MOT, WRE LTCH, and FWD•MOT. When MOT is cleared, the tape motion status logic asserts SDWN (settle down) to the controller drivers to indicate that the transport is in the process of stopping. Clearing WRE LTCH and FWD•MOT actually causes the transport to stop the tape. The read/write control logic delay counter then counts off a 32 ms deceleration delay (which allows time for the tape to stop) and asserts DRIVE STOPPED to the tape motion status logic. The tape motion status logic then clears SDWN and asserts TUR (tape unit ready) to the controller drivers, indicating that another operation may be performed.

Read and Space Forward Operations – The differences between a BOT write operation and a BOT read operation or BOT space forward are as follows:

1. The controller asserts C FWD but does not assert C WRE and C WDR.

2. The read/write control logic delay counter is preset to 33400 and the tape is only advanced 3.01 in. instead of 6.85 in. before the delay expires and READING is asserted.

3. C WRE is not asserted so the transport write logic is disabled.

4. C WDR is not asserted so the adapter write logic is disabled.

5. The delay counter counts off a 0.1 ms delay before clearing MOT and FWD•MOT.

Write File Mark Operation – The differences between a BOT write operation and BOT write file mark operation are as follows:

1. In addition to CFWD and C WRE, the controller asserts C WFMK but does not assert C WDR.

2. The read/write control logic delay counter is preset to 20000 and the tape is advanced 10.05 in. before the delay expires and READING is asserted.

3. C WFMK enables the adapter write logic to write the file mark character and to generate the LRC PLS which causes the transport data section to write the LRC character.

Write Extended Interrecord Gap Operation – The only difference between a BOT write operation and a BOT write-with-extended-interrecord-gap is that the tape is advanced 10.05 in. instead of 6.85 in. before the delay expires and READING is asserted.

Space Reverse Operation – The differences between a BOT write operation and a space reverse operation are as follows:

1. The controller asserts the C REV line only.

2. The read/write control logic delay counter is preset to 37423 and the tape is moved backward only 0.117 in. before the delay expires and reading is asserted.

3. C WDR is not asserted so the adapter write logic is disabled.

4. Because there are no CRC and LRC characters at the beginning of a record, two COMP RD STRB pulses must be generated internally by the shutdown logic and the shutdown counter counts off 5.6 ms before asserting RD CLR.

5. The read/write control logic deceleration delay is 0.1 ms.

Rewind Operations – The differences between a BOT write operation and a rewind off-line operation are as follows:

1. The controller asserts C WRE and C RWND but does not assert C FWD and C WDR; thus OFF-LINE PLS and RWND PLS are generated and sent to the tape transport, initiating a high-speed rewind operation and extinguishing the transport ON LINE indicator.

2. The read/write control logic delay counter is preset for no delay and the motion flip-flop is held in a reset condition; therefore, DRIVE STOPPED is asserted immediately to the tape motion status logic.

3. At the tape motion status logic, RWS (rewind status) asserts and RDY clears, causing TUR to clear and RWS to assert to the controller. If the transport is still selected when the rewind is completed, RWS clears and RDY asserts, causing RWS to clear and TUR to assert.

The rewind operation differs from the rewind off-line operation in that C WRE is not asserted by the controller; therefore, RWND OFF-LINE PLS is not generated and the transport ON LINE indicator remains illuminated.

The only control logic functional blocks not fully discussed in the preceding paragraphs are listed below and discussed in the following paragraphs.

Tape Motion Status Logic
Tape Drive On-Line Detect Logic
EOT Status Register Logic
Status Inhibit Logic

Tape Motion Status Logic – This logic determines the tape motion status and generates outputs to the controller drivers to notify the controller. The logic monitors MOT and DRIVE STOPPED from the read/write control logic and the RWS and RDY inputs from the tape transport. If the transport is on-line with tape loaded and is not rewinding or advancing to the load point, the transport asserts RDY as soon as it is selected by the adapter (BSEL DRIVE asserted). When RDY is asserted by the transport, the tape motion status logic asserts TUR to the controller drivers.

The tape motion logic essentially operates in two modes: the rewind mode and the nonrewind mode. If the controller issues a nonrewind command (for example, a write command), the MOT input is asserted and DRIVE STOPPED is cleared, causing the TUR output to clear. When the operation is completed, the MOT input clears and SDWN asserts. DRIVE STOPPED asserts 32 ms later, SDWN clears, and TUR asserts. If the controller issues a rewind command, the transport clears RDY and asserts RWS; MOT and DRIVE STOPPED remain unchanged, i.e., cleared and asserted, respectively. In response, the tape motion status logic clears TUR and asserts RWS. The transport then rewinds the tape past the BOT marker, clears RWS, advances the tape forward to the BOT marker, and asserts RDY and BOT. The tape motion status then clears RWS and asserts TUR.

The CHANGE UNIT input to the tape motion status logic merely serves to reset the logic each time a new drive is selected by the controller.

Tape Drive On-Line Detect Logic – This logic monitors C SEL 2 from the controller, MOT from the read/write control logic, and DRIVE (1:0) ON-LINE and MASTER SEL SW 0 from the master and slave tape transports.

The MASTER SEL SW 0 input determines which transport is drive 0 and which transport is drive 1 as addressed by the controller. The unit select switches located on the master and slave transport front panels control this input. If an even number switch is installed in the master tape transport, it is addressed as drive 0. If an odd switch is installed in the master transport and an even switch in the slave, the master is addressed as drive 1. If no switch is installed in the slave transport, the master is addressed as drive 0. If the master is the only transport in the system, it is addressed as drive 0.

In accordance with the controller input, the tape drive on-line detect logic selects either the master or slave tape transports by asserting SEL 1 or SEL 0 provided the motion flip-flop is reset. If the transport selected is on-line (ON LINE indicator illuminated) the ON-LINE output is asserted to the controller drivers and C SEL R is asserted, notifying the controller that the designated transport is on-line and has been selected. If, for example, the master transport is drive 0, the controller must clear C SEL 2 to select the master transport. Note that the tape drive on-line logic will not select a new transport while the motion flip-flop is set.

EOT Status Register Logic – The EOT status register logic monitors the EOT input from the tape transport and the SEL 0 line from the tape drive on-line detect logic and stores the EOT status of each transport in a register. If drive 0 is selected and EOT asserts while FWD LTCH is asserted, EOT is asserted to the controller drivers. If drive 1 is then selected, the EOT status of drive 0 is stored and EOT is cleared. The REV•MOT and RWND PLS inputs serve to reset the portion of the EOT status register relating to the drive currently in use. The PWR OK input clears the entire register.

Status Inhibit Logic – This logic inhibits status outputs to the controller when the controller selects a drive other than 0 or 1 and whenever a new drive is selected. If the controller asserts C SEL 0 or C SEL 1, INHIBIT STATUS asserts to the controller drivers and inhibits all status outputs until both inputs are cleared. Whenever the controller clears or asserts C SEL 2, the EOT status register asserts CHANGE UNIT (250 ns pulse), which also causes the status inhibit logic to assert INHIBIT STATUS but for only 250 ns. This prevents the transfer of erroneous status during the drive select operation. Thus, status outputs to the controller are inhibited as long as an illegal drive unit is selected and each time the controller selects drive 0 or drive 1.

2.3.1.2 Write Logic – The write logic generates the strobes necessary to write data, the CRC character, and the file mark character (Figure 2-6). In addition, the write logic generates parity and the CRC and file mark characters and converts all zero characters to 20_8 when even parity (PEVN LTCH asserted) is selected.

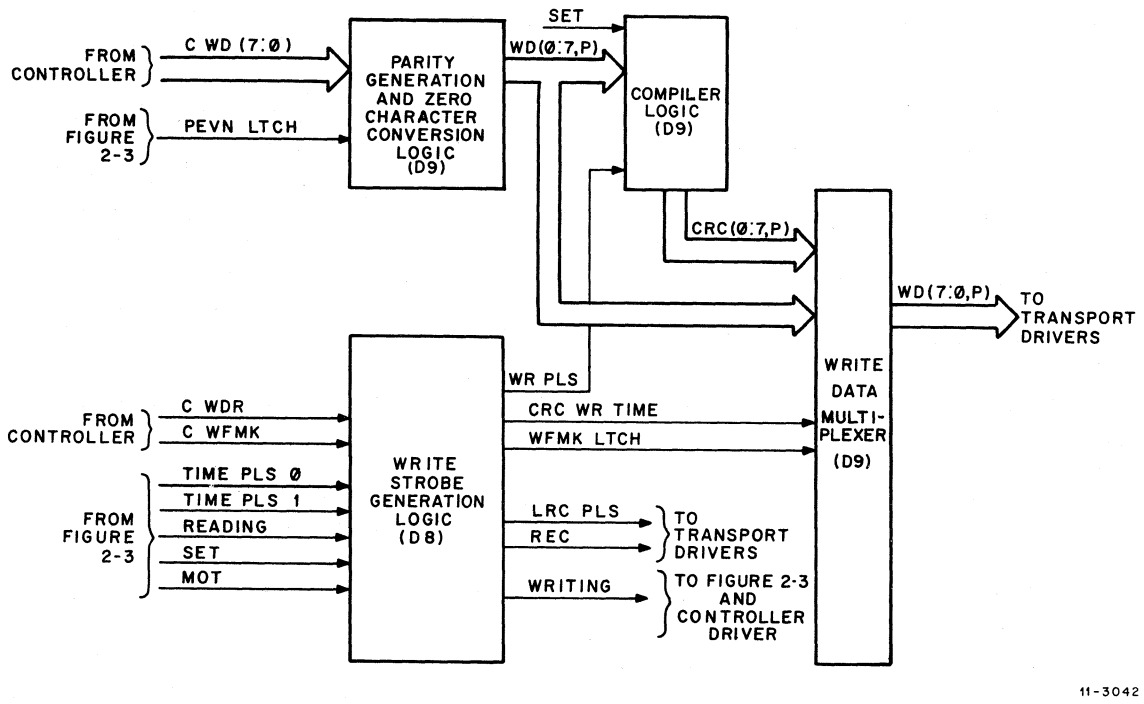


Figure 2-6 Write Logic Functional Block Diagram

The write strobe generation logic is enabled by READING and either C WDR or C WFMK. If READING and C WDR assert, a normal write operation is performed. If READING and C WFMK assert, a write file mark operation is performed. See Figures 2-7 and 2-8 for write operation and write file mark operation flow and timing diagrams.

2.3.1.3 **Read Logic** – The read logic (Figure 2-9) monitors the read data and RD STRB inputs to determine whether a data record or a file mark record is being read and also checks for parity, CRC, or LRC errors.

The record and file mark detection logic decodes the characters read and generates outputs accordingly. The clearing of MOT at the end of the previous operation and the assertion of SET at the beginning of the current operation serve to initialize the logic and assert FMK.

The logic decodes characters read as well as the format in which they are recorded. If a file mark record is detected (a file mark character followed by eight blank character frames and an LRC character), all four outputs are asserted, indicating that a record has been detected and that record was a file mark. The three outputs to the controller drivers serve to notify the controller that a file mark record has been detected. The RECORD ACT output enables the shutdown counter in the control logic. If a data record is detected (three or more data characters followed by a CRC and an LRC), FMK is cleared, RECORD ACT is asserted, and FILE MARK DETECTED and EIGHT SPACES remain cleared.

The parity error detection logic uses the simple generate-and-compare technique to check for parity errors. The logic uses the character read to generate the parity bit as selected by the PEVN LTCH input, then compares the parity bit generated to the parity bit read. If they do not match, BAD PARITY is asserted to the controller drivers.

The LRC error detection logic uses a flip-flop register and a compare network to check the number of 1 bits recorded on each channel of a record, including the CRC and LRC characters. If the number of ones recorded is odd, LRC REG NOT ZERO asserts to the controller drivers, causing LRCE to be asserted to the controller. Note that LRC REG NOT ZERO may assert several times during a particular record; however, the controller driver is only enabled during LRC read time while the tape is moving forward. The CRC error detection logic uses the data characters in each record to compile the CRC character; it then compares the character compiled to the CRC character recorded. If they do not compare, CRCE is asserted to the controller drivers. Note that the CRCE output from the CRC error detection logic is only enabled when CRC RD TIME and FWD LTCH are asserted. At the controller drivers, the C CRCE output is disabled whenever a file mark record is detected.

2.3.2 Transport Control Logic

The control logic section of the tape transport generates the appropriate internal tape motion commands in response to input commands from the adapter, the front panel and the test panel. The control logic receives these commands and generates transport motion if all internal interlocks are satisfied. In addition, the control logic returns the transport status outputs to the adapter and illuminates the respective indicators on the front panel and the test panel. Because the transport uses different signal names than the adapter, a signal name cross-reference is provided in Table 2-3.

2.3.2.1 **Functional Operation** – Five plug-in circuit cards constitute the control section logic (Figure 2-10): Control Terminator Type 3841 (not shown), Interface Control Type 3842, Pushbutton Control Type 3843, Ramp Generator Type 3645, and Sensor Amplifier/Driver Type 3844. The modules are housed in the card cage assembly and plug into the master board. Figure 2-10 is a simplified block diagram of the control logic, showing the signal flow between the control modules. The input signals from the adapter are supplied, after being terminated on the control terminator module, to the control interface module, where these signals are acknowledged if certain interlocks are satisfied. The motion commands are then supplied to the pushbutton control module. This card also includes the interlocks for the front panel pushbuttons and for the test panel pushbuttons. If the interlocks are satisfied, the pushbutton control module encodes all tape motion commands onto three command lines: RNN1 (run normal), RNF1 (run fast), and RVS1 (reverse select). The three command lines are then supplied to the ramp generator module, which produces accurate analog voltage output. The voltage output of the ramp generator is then supplied to the capstan servo amplifier module in the servo system. The voltage output of the ramp generator in

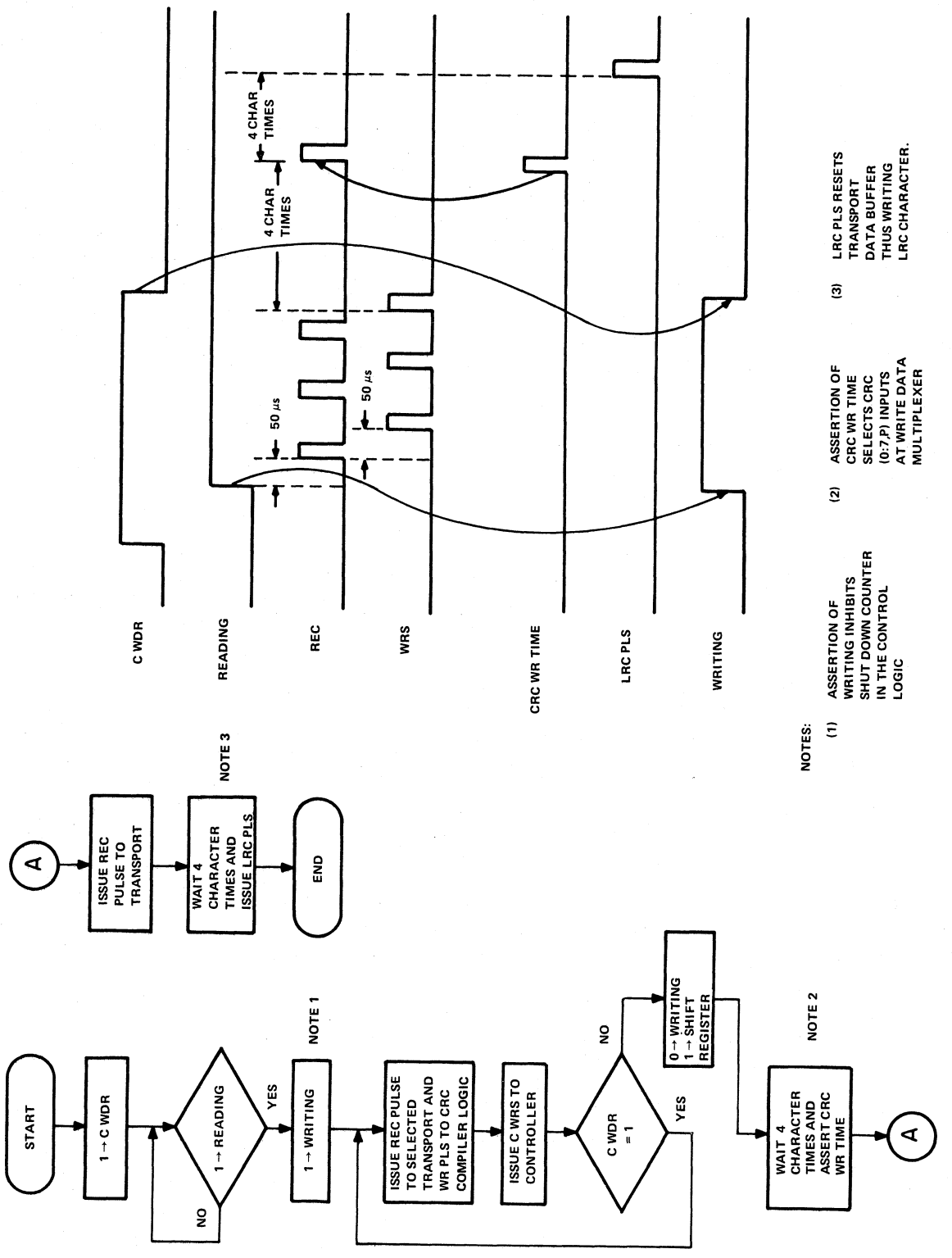


Figure 2-7 Write Operation Flow and Timing Diagram

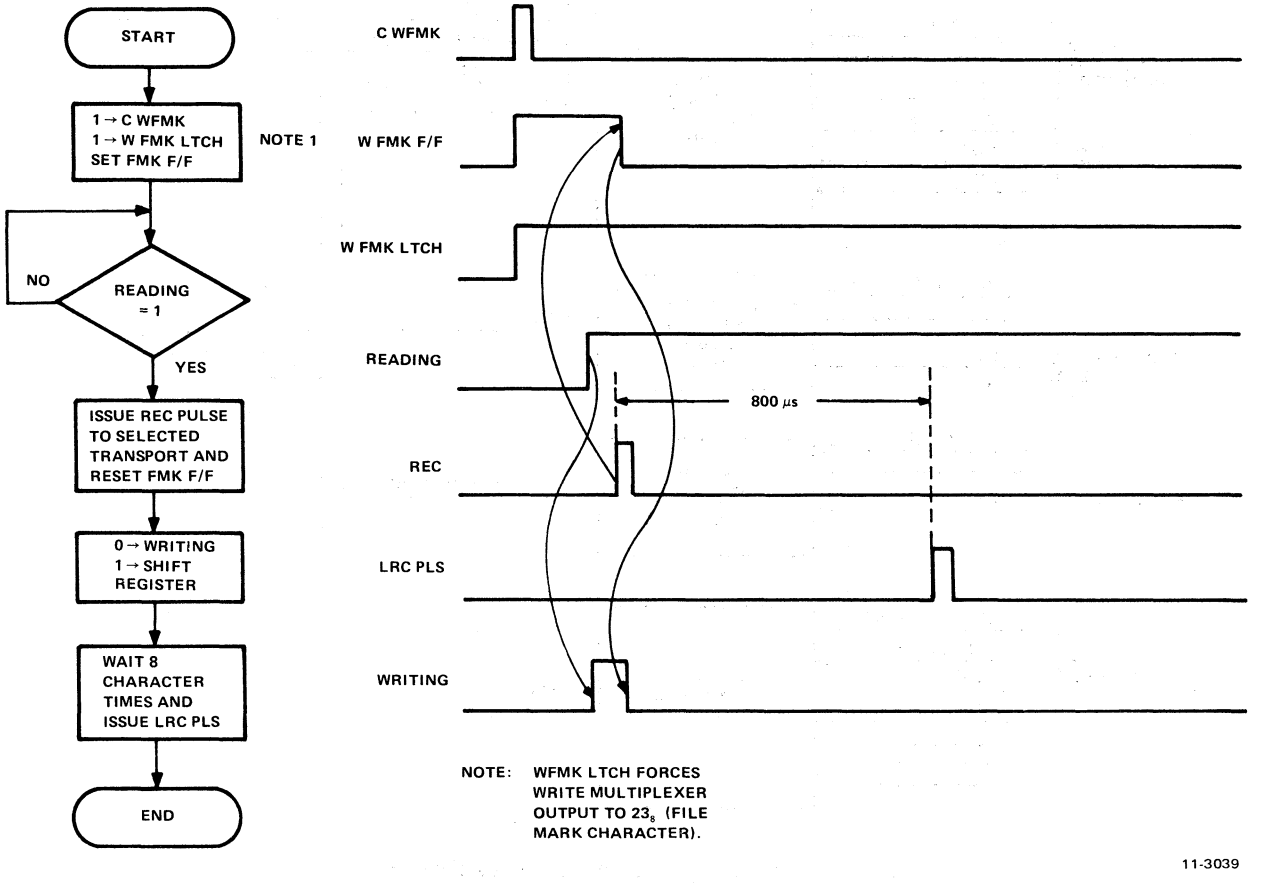


Figure 2-8 Write File Mark Operation Flow and Timing Diagram

conjunction with the feedback from the capstan tachometer is used to energize the capstan motor and to advance the tape in the desired direction at the proper speed. The ramp generator provides linear ramp-ups to speed and linear ramp-downs to standstill in order to minimize the stress on the tape and maintain accurate speeds.

The sensor amplifier driver module receives the inputs from the file protect switch, the load point sensor, end-of-tape sensor, and broken tape sensor. These signals are amplified and supplied to the other modules in the control section where they provide the inputs to the interlocks. The sensor amplifier driver module also contains the drivers for the front panel indicators, the driver for the file protect solenoid, and the write and erase head drivers.

2.3.2.2 **Transport Control Logic Operation During a Write Sequence** – A write operation will be used as an example to demonstrate the interaction of the different components of the control logic. The whole operation is described, showing the flow of commands and the required control interlocks.

The front panel is used to prepare the transport for operation. After the power is turned on and the tape is properly threaded, the front panel LOAD pushbutton is pressed. This sets the load flip-flop on the pushbutton control modules, generating RNN1 true to the ramp generator card. The ramp generator outputs a linear ramp voltage to the capstan servo amplifier card, initiating forward tape motion at normal running speed. The ramp generator also supplies TRNG (tape running) status true through the interface control card to the adapter logic. When the load point reflector marker is detected by the respective photocell, the signal is amplified by the sensor amplifier/driver card and is supplied as LP (load point detect) true to the pushbutton control module. LP true sets the ON TAPE flip-flop to the true condition, terminating the synchronous forward motion by setting RNN1 false. The tape is

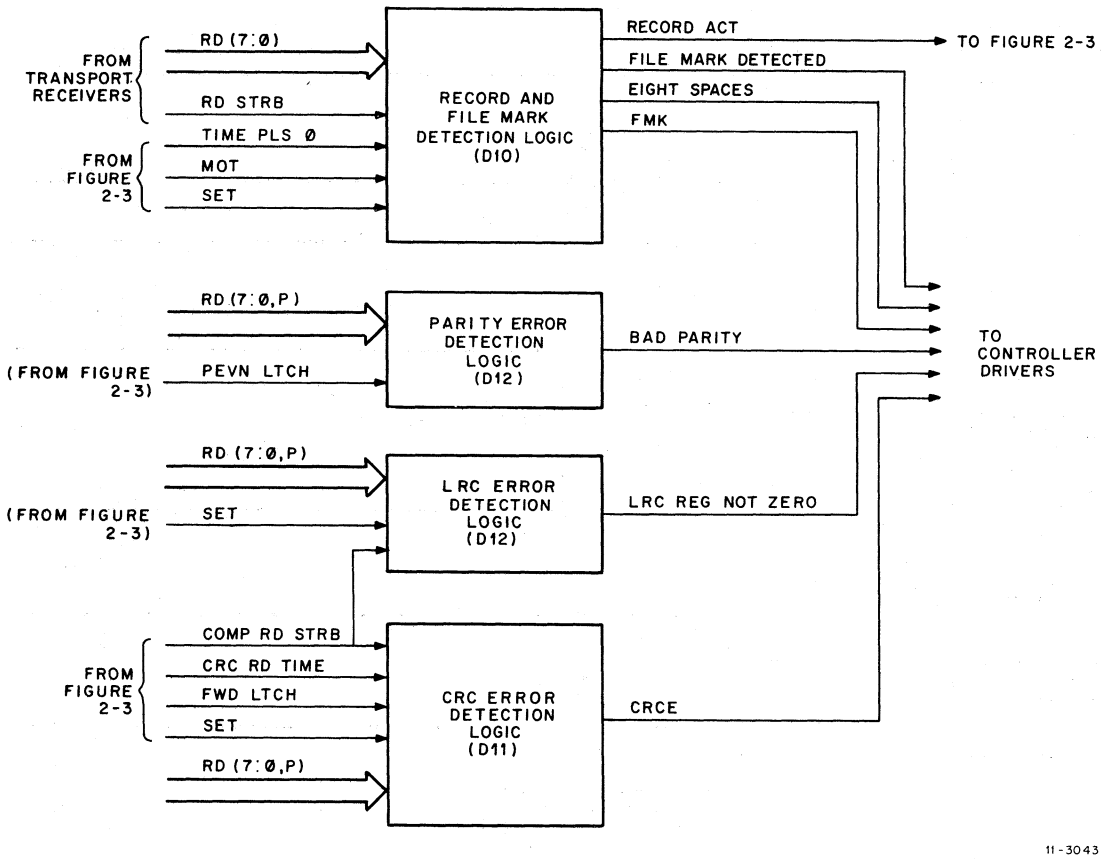


Figure 2-9 Read Logic Functional Block Diagram

Table 2-3
Adapter To Transport Signal Name Cross Reference

Signal Name	
At Adapter	**At Tape Transport**
B FWD•MOT	SFC
B REV•MOT	SRC
B OFF-LINE PLS	OFF C
B RWND PLS	RWC
B WRE LTCH	SWS
B SEL DRIVE (1:0)	SLT
B DRIVE ONLINE	ONL
B WD (0:7, P)	WD (0:7, P)
B XPRT RDY	RDY
B RD (0:7, P)	READ CHAN (0:7, P)
B WRLCK	FPT
B RWNDG	RWD
B LOAD POINT	LDP
B END OF TAPE	EOT
REC	WDS
LRC PLS	WARS
B DRIVE (1:0) RD STRB	RDS

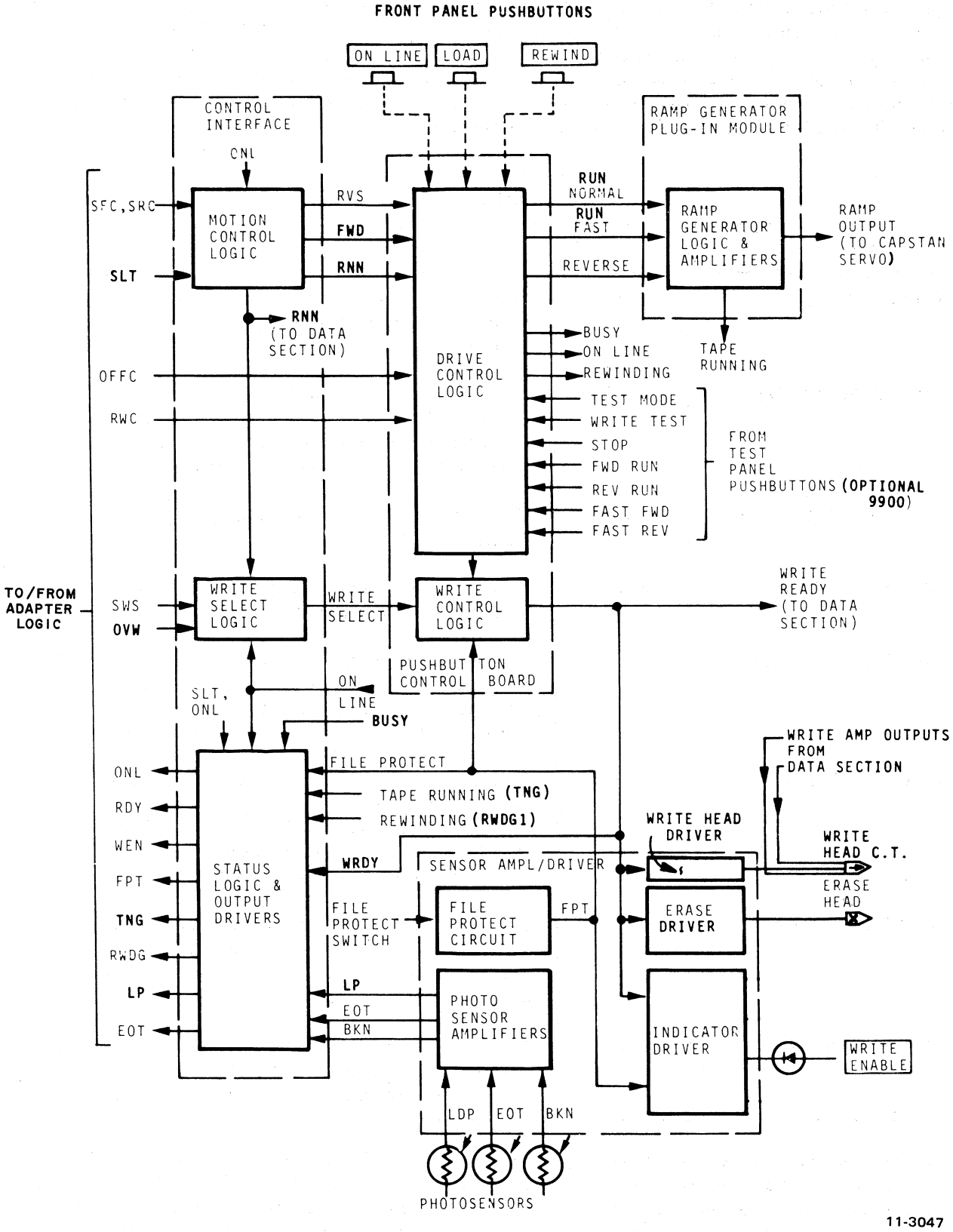


Figure 2-10 Control Logic Block Diagram

stopped at the load point and is properly loaded. Pressing the front panel ON LINE pushbutton now places the transport on-line, preparing the transport to respond to adapter commands once it is selected by the adapter. When the transport is selected (input line select going true), the transport can accept commands from the adapter and return the transport status outputs back to the adapter. At this time, the transport status lines would be in the states shown in Table 2-4. In addition to the status lines, the front panel ON LINE and SELECT indicators are illuminated, as is the WRITE ENABLE indicator if the supply reel contains a write enable ring.

Table 2-4
Transport Status

Status Line	State	Point of Origin
ON-LINE (ONL)	True	Supplied from the load point flip-flop on the pushbutton control module, routed through the interface control module.
TRANSPORT READY	True	This signal, generated on the interface control module, combines BUSY false (meaning the transport is loaded and not rewinding or searching for load point) and SLT1 true (meaning the transport is on-line and SLT is true).
TAPE RUNNING (TNG)	False	This signal goes true on the ramp generator when tape motion is initiated.
REWINDING (RWDG)	False	At this time, the rewind flip-flop on the pushbutton control module is in the cleared state.
FILE PROTECT (FPT)		This signal is true if the reel of tape mounted on the supply hub does not contain a write enable ring. It is false if the reel does contain the ring and is available for writing. The signal originates on the sensor amplifier/driver module.
LOAD POINT (LP)	True	Since the tape is at load point, the sensor amplifier/driver supplies this signal true. When LDP is true, the transport does not acknowledge a REWIND command or an SRC from the interface, but must be taken off-line and rewound off tape by using the front panel pushbutton.
WRITE ENABLE (WEN)		This signal is equivalent to the inverse of the FPT signal and is true whenever the other is false, e.g., whenever the supply reel contains a write enable ring. The signal originates on the interface control module.
END OF TAPE (EOT)	False	This signal goes true only when the end-of-tape reflective marker is detected by the respective photosensor. The signal is supplied to the sensor amplifier/driver module.

If the write operation is to be initiated, the adapter logic now supplies SWS (set write status) level true and then an SFC (synchronous forward command). The SWS level is sampled on the leading edge of SFC. If the level is true, a flip-flop on the interface control module is set, which generates WSEL (write select) true. WSEL is supplied to the pushbutton control module where it generates WRDY (write ready) true provided FPT (file protect) is false (supplied from the sensor amplifier/driver module), BUSY is false (this signal is generated on the pushbutton control

and is true whenever the transport is searching for load point and is rewinding), and a forward motion command is given. These interlocks ensure that the transport writes data on tape only when the tape is properly loaded, the reel has a write enable ring, and the tape is moving forward at normal running speed. WRDY true is supplied to the sensor amplifier/driver module where it turns on write and erase head current drivers. WRDY and SLT1 (select 1) (combining ON-LINE true and SLT true) are also supplied to the data electronics card cage where they enable the write and read amplifier stages.

If WRDY does go true, the adapter logic supplies the properly formatted data to be written on tape. The write operation can be interrupted in case of broken tape; when the BKN (broken tape) signal is supplied from the sensor amplifier/driver module, all servos are disabled immediately. Note that an EOT indication does not terminate a write operation, but leaves it up to the adapter to do so. When the write operation is terminated by the adapter, the tape is rewound to the load point when the adapter issues a REWIND command. Note that the tape cannot be rewound past the load point by a command from the adapter In order to rewind the tape off the takeup reel, the transport must be taken off-line, either through an adapter command or by pressing the front panel ON LINE pushbutton again. Once the transport is off-line, the front panel REWIND pushbutton can be activated to rewind the tape completely off the takeup reel.

2.3.2.3 **Test Panel** – The test panel provides a means of exercising, testing, and adjusting the tape transport while it is off-line, eliminating the need for a separate test fixture or for the use of valuable computer time. The test panel can initiate forward and reverse tape motions at either normal or high tape speeds. It can also initiate a write test, generating a crystal-controlled all-1s test pattern on tape. The test panel also provides indicators for load point, end-of-tape, and data.

An additional indicator monitors excessive skew, and is used in the aligning of the read/write head when using an 800 character/in. skew master tape. When the head is properly aligned and the data is written on tape properly, the SKEW indicator is extinguished.

The controls and interlocks for the test panel are located on the pushbutton control card. The skew detect network is located on the delay timing module in the read logic section of the transport. The test panel becomes operational only when the transport is off-line, with the test panel STOP pushbutton depressed. If these conditions are satisfied, the test panel pushbuttons are enabled when the TEST MODE pushbutton is pressed.

2.3.3 Servo System

The servo system includes two subsystems: the capstan servo subsystem, which drives the tape at accurately controlled speed, and the reel servo system, which maintains constant tape tension.

2.3.3.1 **Reel Servos** – Two identical reel servos are employed for the supply and the takeup reels. A simplified block diagram is shown in Figure 2-11. Each reel servo includes a spring-loaded buffer arm, a magnetic position sensor coupled to the buffer arm shaft, a servo amplifier (located on the Servo Preamplifier Type 4306 module), power transistors (located on the chassis heat sink), and a high power dc motor.

The tape tension is maintained by the interaction of the spring-loaded buffer arms, the capstan, and the respective reel motors. The magnetic position sensors, called magpots, produce a corrective voltage whenever the buffer arms swing away from the center of their arcs. The magpots are rotary differential transformers with oscillator and phase detector circuitry. The output of the magpot circuitry provides a bipolar dc voltage which has a linear relationship to the tension arm position and a null at the center position. The magpot output is summed with a signal from the capstan tachometer in the higher speed versions of the machine. The effect of the tachometer component is to speed up the response of the reel servos.

As shown in Figure 2-11, the corrective voltage approaches 0 V in the rest position where the torque of the motor is balanced against the buffer arm spring tension near the center of the tension arm swing. When capstan motion pulls the tape, the buffer arm moves, causing a change in the magpot output. This is amplified in the servo preamplifier whose signal drives power transistors that control the dc motor current to provide a change in torque until the

torque matches the buffer arm spring tension at the null position again. Since the system is bipolar, seeking a null which is controlled by a magnetic core position, the adjustments are mechanical and will not drift with temperature or component degradation.

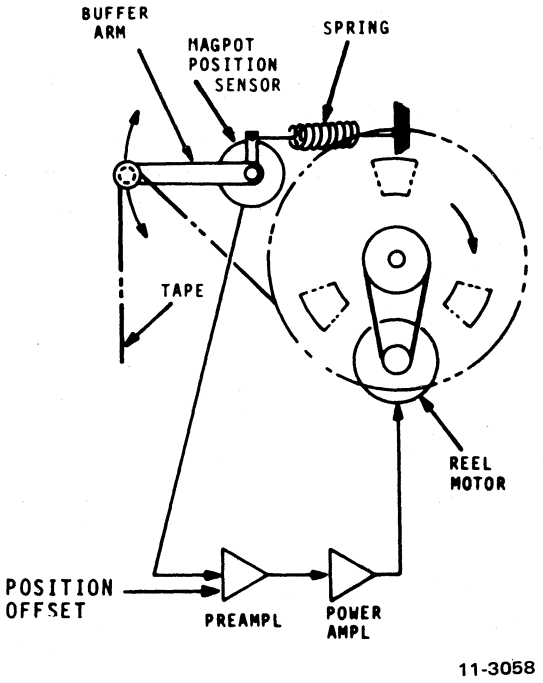


Figure 2-11 Reel Servo System

2.3.3.2 **Capstan Servo** – The single capstan drive motor is part of a high performance velocity servo system. In addition to the motor, the capstan servo system includes a dc tachometer, coupled to the capstan motor shaft, and the capstan amplifier, located on the servo preamplifier module. The linear analog ramp voltage produced by the ramp generator card (in the control logic section) is supplied to the servo preamplifier module where it is compared with the feedback supplied from the capstan tachometer. Any resulting difference is amplified and is supplied to the capstan power transistors, located on the chassis heat sink. The output of the power transistors energizes the capstan motor, advancing tape at accurately controlled speeds.

2.3.4 Data Section

The data section includes read and write amplifiers and interface cards providing output drivers and timing controls. Block diagrams are shown in Figures 2-12 and 2-13.

The data section consists of eight circuit cards that plug into the master board. These include a timing delay module, a read amplifier/clipping control card, a pair of quad read amplifier modules, a four-channel write amplifier card, a five-channel write amplifier card, and a data terminator card.

2.3.4.1 **Write Electronics** – A write amplifier channel is provided for each tape channel. Four such channels and the circuitry common to all write amplifiers are contained on Write Amplifier Type 3848, and the five remaining write amplifier stages are located on Write Amplifier Type 3849. These cards plug into the master board, from which the necessary head connections are made.

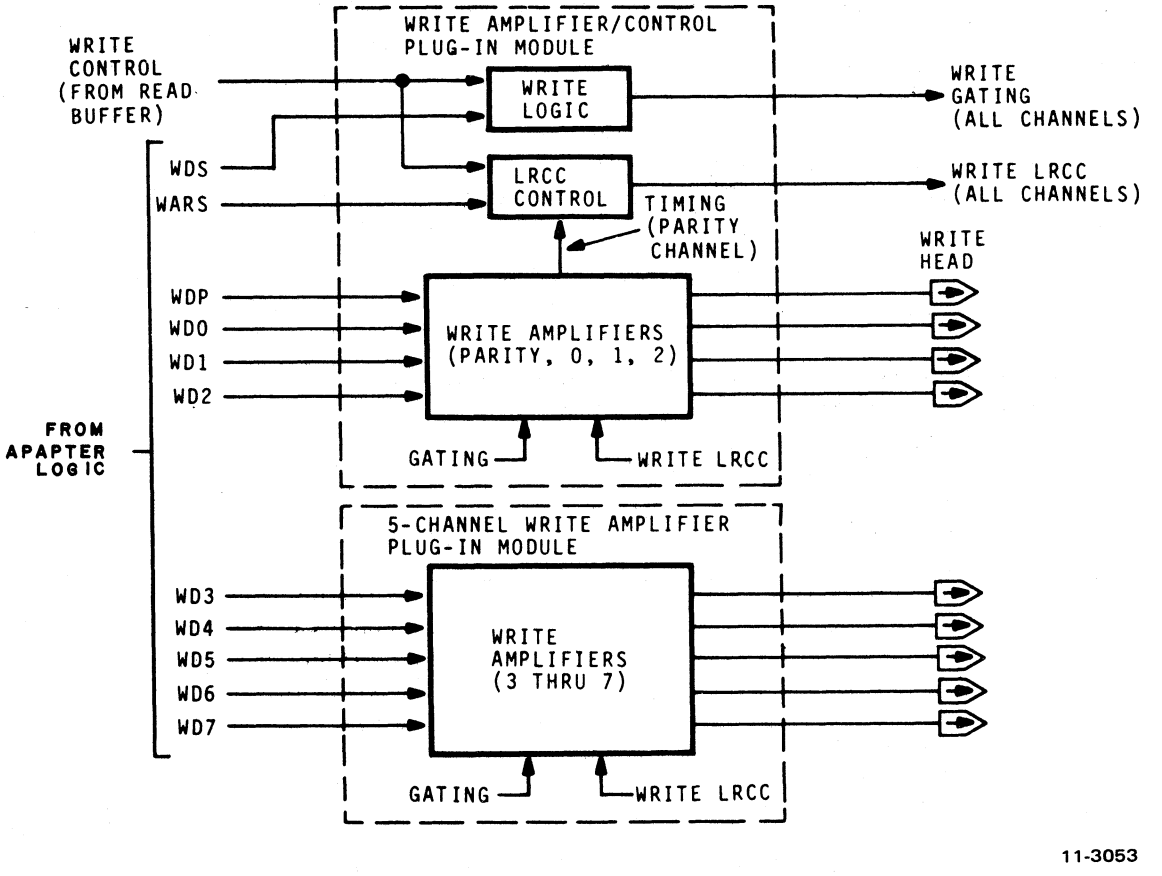


Figure 2-12 Write Data Section

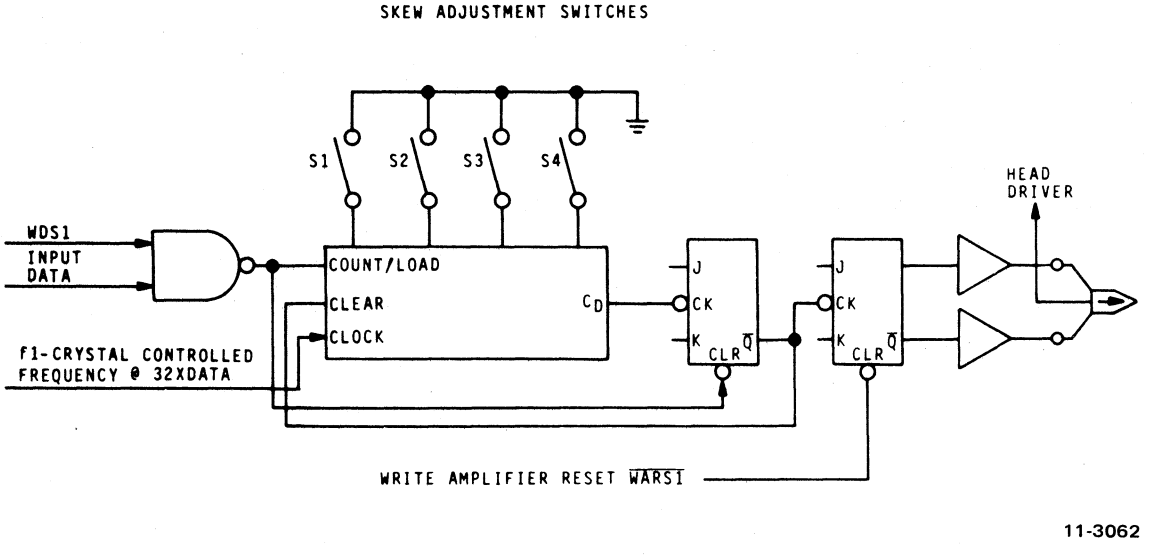
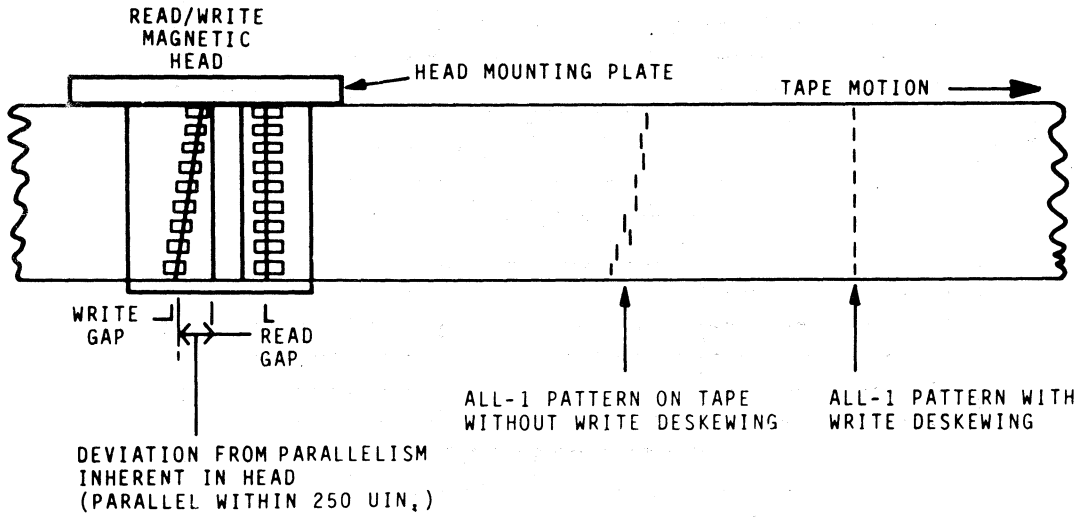


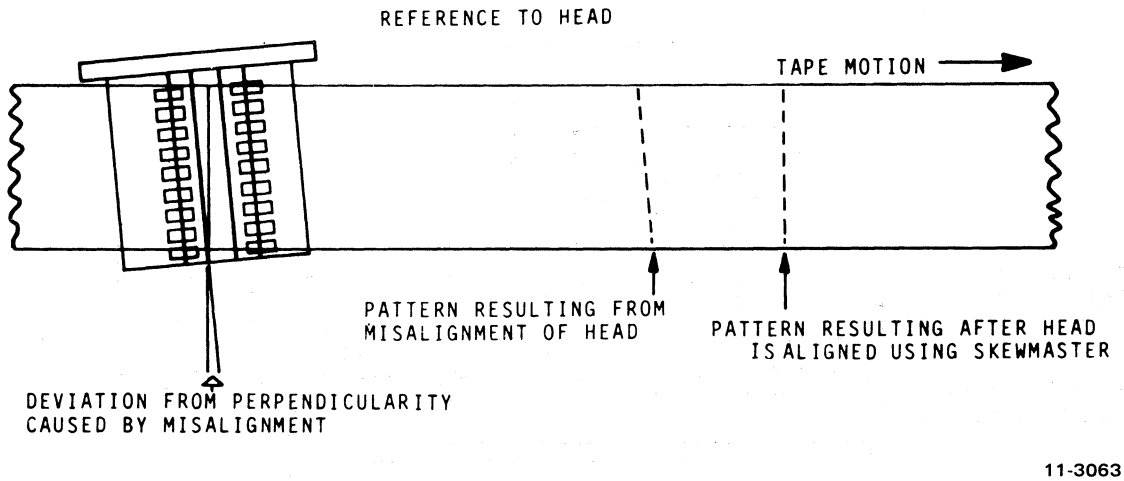
Figure 2-13 Typical Write Amplifier Channel (0–7), Fixed Channel P Delay

Each write amplifier channel consists of an input buffer, a digitally adjustable deskewing circuit, a clocked flip-flop, and a pair of head drivers, as shown in Figure 2-13. Digital write deskewing and its advantages are explained in the following paragraphs.

Manufacturing tolerances in the production of magnetic heads cause deviations in the parallelism between the write gap and the read gap of the magnetic heads, as shown in Figure 2-14. While the magnetic heads are manufactured so that this deviation does not exceed 250 microinches, it is important to correct for it; otherwise the skew across the bits of a character may cause errors during the reading of the data on compatible systems.



a. Skew Caused by Physical Characteristics of Head



b. Skew Caused by Misalignment of Head

Figure 2-14 Skew Characteristics

The skew caused by the physical characteristics of the head should not be confused with azimuth or with the skew caused by the misalignment of the whole magnetic head with respect to the tape path, shown in Figure 2-14. Azimuth can be corrected by aligning the read head to be perpendicular to the tape path using a skew master tape – a tape written by a special machine equipped with a full-width write head set perfectly perpendicular to the tape. The head aligning procedure is made particularly simple by the use of the optional test panel, as described in Part I, Chapter 5 of this manual.

While azimuth can be corrected by manually adjusting the position of the read head, the skew caused by the parallelism tolerance between the write head and read head must be corrected electronically. This is done by delaying the channels with respect to a fixed reference so that all the bits of the character are read simultaneously.

Conventional skew correction methods employ adjustable delays supplied by analog circuitry in the read circuits. While these methods compensate for the skew of the character written on tape by the same machine, they do not correct the character itself as it is written on tape; consequently when the tape is read on a different machine, the skew is uncorrected. Also the delays generated by analog circuits are subject to drift and may require periodical readjustment.

In this tape unit, the skew correction problems are overcome by write deskewing circuits, shown in Figure 2-13. The main component of the deskewing circuit is a divide-by-16 counter clocked by a crystal-derived frequency F_1 at 32 times the data rate (generated on the delay timing module). The counter of channel P is preset to the count of eight, supplying a fixed 1/4 character delay. The parallel inputs of the counters of the other eight channels are adjustable using a set of four switches for each counter, varying the skew delay of each channel in 1/32 character increments. Each head is pretested and the switch positions are determined to compensate for any deviation from parallelism between the write and the read gaps, using channel P as a reference. Once the head is installed on a machine and the write amplifier switches are set, the switch positions should not be changed for the life of the magnetic head. These switch positions are displayed on a tape inside the machine. If the magnetic head is replaced, the replacement head is pretested in the factory and is supplied with a new tag showing the switch positions required to compensate for the characteristics of the new head.

The digital write deskewing method ensures that the character written on tape has minimum skew, increasing the compatibility of tapes between different tape transports. Using digital circuitry with a crystal-controlled reference frequency provides for a high degree of precision and stability for all skew adjustments.

The write electronics section also includes the write data strobe buffer which clocks the write amplifier flip-flops, and a write amplifier reset circuit to clear all write amplifier flip-flops. The write amplifier reset is used to write the LRC character. During a write test mode, initiated by the test panel with the recorder off-line, the write electronics generates an all 1s test pattern on tape derived from a crystal-controlled reference frequency (F_R), supplied from the delay timing module in the read electronics. The test pattern can be used to test the write deskewing, as well as the other functions of the data electronics.

2.3.4.2 **Read Electronics** – The function of the read electronics is to convert the data recovered from the tape into digitized waveforms, deskew it, and supply it to the adapter logic with its respective read strobe. The read electronics also detect the interrecord gap and excessive skew. The components comprising the read section include the magnetic read head, the Read Preamplifier Type 3631 module, Delay Timing Type 3845 module, Read Amplifier/Clipping Control Type 4179 module, and a pair of Quad Read Amplifier Type 4178 modules. Figure 2-15 is a functional block diagram of the read section, showing the general signal flow between the cards.

The low level analog signals, on the order of tens of millivolts, are supplied from the read head to the read preamplifier module where they are linearly amplified to an output voltage (adjusted by a potentiometer for each read preamplifier stage) of approximately 9 V peak to peak in 800 character/in NRZI read operation. The amplified analog signals are then supplied to the nine read amplifier stages, eight of which are located on the quad read amplifier modules while that of channel P is located on the read amplifier/clipping control module. Each read amplifier stage includes a peak detection circuit, a filtering network, an output data register, and a pulse generator.

The analog signals from the preamplifier are detected only when they exceed the positive or negative clipping levels provided by the read amplifier/clipping control module. They are then rectified and peak detected, with the resulting digitized waveforms containing negative-going transitions corresponding to the peaks of the input analog signals, e.g., 1 bits in the NRZI code. The digitized waveforms are supplied to a filtering network which eliminates spurious pulses between transitions. The data of each channel is then stored in a register and generates a PULSE OUT to the delay timing module. Following the skew delay, the delay timing card supplies a DATA TRANSFER output to clock the data registers of all nine channels simultaneously, supplying the data character and read clock to the interface.

When an error is detected and the transport is commanded by the adapter logic to reread a block, the read amplifier clipping levels are switched automatically by the read amplifier/clipping control module to maximize the recoverability of marginally recorded data. The clipping levels are kept normal on the first reread; on the second reread they are switched to lower levels in order to recover possible partial dropouts. If the block is still in error and a third reread is commanded, the clipping levels are switched to higher levels to eliminate possible baseline spikes. During read-after-write operations, higher clipping levels are used.

The delay timing module contains circuitry common to all nine channels. It includes a crystal-controlled oscillator and divider network which produce the synchronous clocks used in the skew delay network, the data strobe generation, the gap detect network, and are also supplied to the Write Amplifier Type 3848 module to generate the write test pattern. The crystal-controlled clocks ensure high precision in the performance of all data synchronized functions.

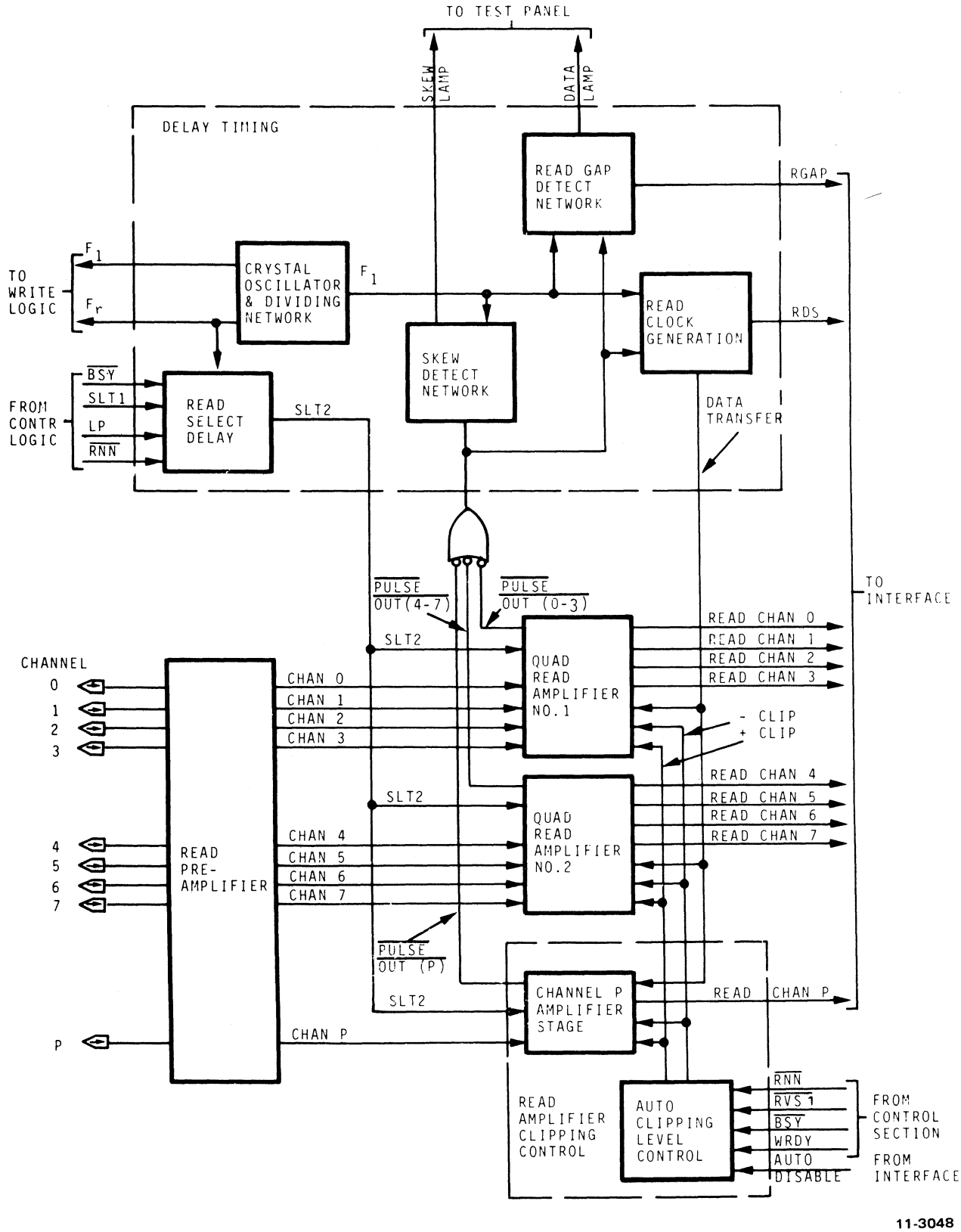


Figure 2-15 Read Data Section

CHAPTER 3
DETAILED LOGIC DESCRIPTIONS

3.1 INTRODUCTION

This chapter contains circuit descriptions of the individual circuit cards comprising the TS03 DECmagtape Transport. Module layout drawings are provided with each description. (See engineering drawing for module schematics.) The descriptions are arranged by functional group as listed below.

Functional Group	Module Name and Type
Adapter Logic	M8920 Adapter
Overall	Model 9700 Power Supply
Control Electronics	Type 3842 Interface Control
	Type 3843 Tape Motion Controls including Pushbutton Control, Main Control Panel, and Test Panel
	Type 3645 Ramp Generator
	Type 3844 Sensor Amplifier/Driver
	Type 4013 Connector Board
Servo System	Type 4306 Servo Preamplifier
	Type 4218 Magpot
Read Electronics	Type 3860 Data Terminator
	Type 3631 Read Preamplifier
	Type 3845 Read Control Logic including Delay Timing
	Type 4178 Quad Read Amplifier
	Type 4179 Read Amplifier/Clipping Control
Write Electronics	Type 3848 Write Amplifier

NOTES TO TRANSPORT SCHEMATIC DIAGRAMS

ain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified, the resistor may be either 1/4 or 1/2 W.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens, they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5 V) and 7 (ground) for 14-pin packages, and 16 (+5 V) and 8 (ground) for 16-pin packages. Some ICs (7476, 7492, 7493, for example) have power connections on pin 5 (+5 V) and pin 10 (ground). Operational amplifiers in the 8-pin package have power connections on pin 4 (−Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. Abbreviations used in from and to designations are as follows:

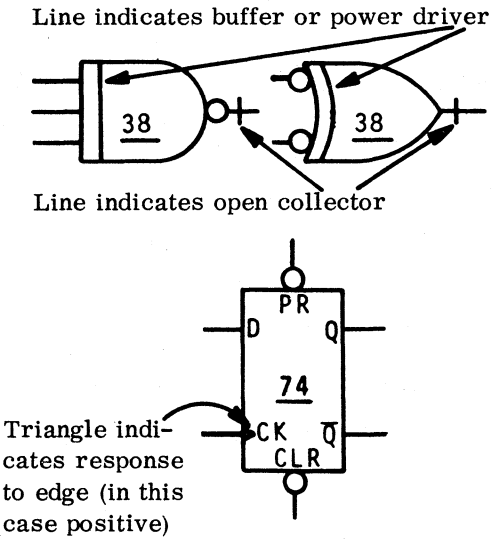
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four-Channel Write Amplifier
WA2	Five-Channel Write Amplifier

8. Positive logic is shown for all *internal* connections. Interface connections are zero true but the bar is omitted.

9. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a *00* designation indicates a 7400 quad two-input NAND gate. Texas Instruments' complete part number is SN7400N. In multifunctional units in close proximity, the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

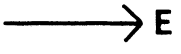
   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.



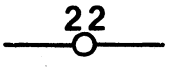
10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

11. Unless otherwise specified, light-emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as



where no further connection is shown on the schematic, and as

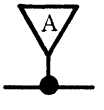


when there is a connection shown.

13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown, their destinations may not be shown.

14. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case, all the connections to the element may not be shown in the interest of clarity.

15. The following symbol designates a test point provided on the module. Letters proceed from the top to the bottom of the card with the ground test point, if present, as the bottom-most terminal.



16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double-sided socket is used. These are the designations on the socket. When a single-sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22-pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

3.3 TYPE M8920 ADAPTER CIRCUIT DESCRIPTION

The following paragraphs provide detailed circuit descriptions on those portions of the adapter logic which perform unique or complex operation. Each description covers a functional block on the control logic, write logic, and read logic functional block diagrams and is titled accordingly. The circuits described are listed as follows:

Functional Area	Circuit	Engineering Drawing Reference
Control Logic	Clock Logic	D4
Control Logic	Read/Write Control Logic (ROM/Delay Counter)	D5
Control Logic	Shutdown Logic	D6
Write Logic	Write Strobe Generation	D8
Read Logic	Record and Tape Mark Detection Logic	D10

3.3.1 Clock Logic

The clock logic generates two 10 kHz pulse trains which are 180 degrees out of phase. See the timing diagram for logic operation and timing specifications (Figure 3-1).

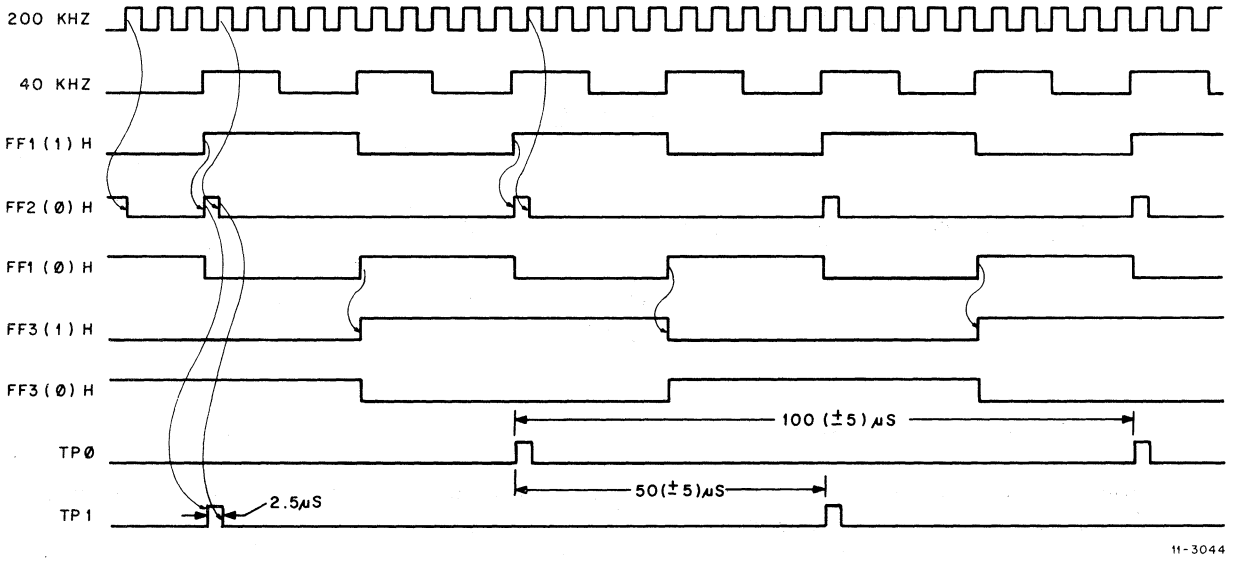


Figure 3-1 Clock Logic Timing

3.3.2 Read/Write Control Logic (ROM/Delay Counter)

The following paragraphs describe the read/write control logic relative to two different operations: a write operation and a rewind off-line operation (engineering drawing D5).

3.3.2.1 Write Operation – To initiate a write operation, C WRE H and C FWD H must be asserted by the controller. When SET L asserts, the following operations occur at the read/write control logic:

1. The ROM is addressed and the proper count is output to the delay counter. The count varies in accordance with the tape position relative to the BOT. If the tape is positioned at the BOT (BOT H asserted), the delay counter is set to 25000_8.

2. The motion enable flip-flop is set.

3. The load delay counter one-shot (E27-5) is triggered and LOAD DELAY CTR L asserts.

Assuming the tape is positioned at BOT, the assertion of LOAD DELAY CTR L loads the delay counter to a count of 25000_8 using the output from the ROM and RWND L. Note that zeros are loaded into the first and second most significant bits (R3 and R2) of Part D of the delay counter due to the assertion of SET L. The load delay counter one-shot then resets and sets the motion flip-flop, asserting MOT H. Thus READING H remains cleared. TIME PLS 0 then clocks the delay counter for 563.2 ms, the second most significant bit of Part D of the delay counter sets, and READING H asserts. The read/write control logic remains in this state until RD CLEAR (1) H is asserted by the shutdown logic.

The assertion of RD CLR (1) H loads the delay counter with a deceleration delay using the ROM output RWND L. In this case, because a write operation is being performed, the delay counter is set to 37754_8. RD CLR (1) H also sets the two most significant bits (R2 and R3) of Part D of the delay counter because SET L is cleared. TIME PLS 0 L then clocks the delay for 2 ms, the most significant bit (R3) is reset, and the motion enable flip-flop (E25-3) is reset. Resetting the motion enable flip-flop asserts CLEAR MOT L, which resets the motion flip-flop, thereby clearing MOT H and the FWD•MOT H output to the tape transport. The transport begins to stop the tape. TIME PLS 0 L then clocks the delay counter for 32 ms (allowing time for the transport to stop the tape), and INHIBIT DELAY COUNT L asserts, inhibiting the clock input to the delay counter and asserting DRIVE STOPPED L. Assertion of DRIVE STOPPED L notifies the tape motion status logic that tape deceleration delay has expired.

3.3.2.2 Rewind Off-Line Operation – To initiate a rewind off-line operation, C RWND H and C WRE H must be asserted by the controller. When C SET H asserts, the following operations occur:

1. The ROM is addressed and a stop count is output to the delay counter.

2. The motion enable flip-flop is set.

3. The off-line one-shot (E33-13) is triggered, asserting OFF-LINE PLS H to the tape transport.

4. The rewind pulse one-shot (E27-13) is triggered, asserting RWND PLS H to the tape transport.

5. The load delay counter one-shot (E27-5) is triggered, asserting LOAD DELAY CTR L.

The assertion of LOAD DELAY CTR L loads the delay counter with a stop count, i.e., the counter is set so that DRIVE STOPPED L asserts. When the load delay counter one-shot resets, the motion flip-flop is held in the reset state by RWND PLS H. Thus MOTION H remains cleared, DRIVE STOPPED L remains asserted, and the tape is rewound to the BOT.

3.3.3 Shutdown Logic (Engineering Drawing D6)

The shutdown logic is enabled when RECORD ACTIVE H asserts and WRITING L clears. With those conditions established, TIME PLS 0 H clocks the shutdown counter. However, the counter is prevented from counting past a count of 2 initially by COMP RD STRB L (composite read strobe), which is generated each time RD STRB H (read strobe) is received. After the last data character is read, there is a gap of four character times before the CRC character is read. During that time, the shutdown counter reaches a count of 3, the CRC flip-flop (E61-5) is set, and

CRC RD TIME (1) H asserts. A read strobe is then received due to the CRC character and COMP RD STRB L asserts and clears the shutdown counter again. When COMP RD STRB L returns high, the CRC flip-flop is reset and the LRC flip-flop (E45-5) is set, asserting LRC RD TIME (1) H. The counter then counts to 3 again, but this time LRC RD TIME (1) H holds the CRC flip-flop in the reset state. Another read strobe is then received due to the LRC character, and COMP RD STRB L asserts again, clearing the shutdown counter. When COMP RD STRB L clears, the LRC flip-flop is reset and the EOR flip-flop (E45-9) is set. Note that the read strobe resulting from the LRC character is also ANDed with LRC RD TIME (1) H to load the shutdown counter with a binary count of 56 (0111000). The shutdown counter is then clocked by TIME PLS 0 and, at a binary count of 64, the read clear one-shot is triggered, the counter is disabled, and RD CLEAR (1) H asserts to the read/write control logic.

The EOR one-shot (E28-5) is provided to ensure that the shutdown process is completed when the CRC and LRC characters are not detected at the end of a record. This is always the case when the tape is moving backward, and might occur when the tape is moving forward if there is a bad spot in the tape or the write circuitry malfunctions. Note that when the last data character read strobe is received, the shutdown counter counts to 3 and sets the CRC flip-flop, thus asserting CHK CHAR RD TIME H. If the CRC read strobe is not received, the shutdown counter counts to 5, placing a low on the EOR one-shot. At a count of 6, the EOR one-shot is triggered, asserting EOR H and thereby generating COMP RD STRB H. Thus the counter is cleared, the LCR flip-flop is set, and the CRC flip-flop is reset. The counter then counts up again and if the LRC read strobe is not received, the same operation is repeated. The shutdown counter then starts its final count cycle; however, in this case the counter starts from a count of 8 instead of a binary 56, due to the absence of the LRC read strobe. Therefore the final count cycle is 56 counts long instead of the normal 8. In the event a bad tape spot is encountered or the write circuitry malfunctions, this extended count cycle ensures that the tape moves past the end of the record before stopping.

3.3.4 Write Strobe Generation Logic

The following circuit description will cover the two modes in which the write logic can operate: write data and write tape mark (engineering drawing D8).

3.3.4.1 Write Data Circuit – When the C WDR H and READING H inputs are asserted, the write data mode is enabled and WRITING L and WRITING H assert. WRITING H enables the clock pulse (TIME PLS 1 H) to generate write strobes to the transport (REC H) and is also output to the controller driver where it enables the clock pulse (TIME PLS 0 H) to generate the write strobe (C WRS L), thus notifying the controller that a character has been recorded and requesting the next character. When the last data character has been strobed to the transport, the controller clears the C WDR H input, causing WRITING L to go high, inhibiting the strobe outputs, and setting the writing done flip-flop (E47-6). Setting the writing done flip-flop places a high on the input to the shift register and the next assertion of TIME PLS 0 loads a 1. The shift register output then resets the writing done flip-flop so that no more ones will be loaded into the shift register. TIME PLS 0 then shifts the 1 bit through the shift register and, at bit position 3, CRC WR TIME H asserts, enabling another write strobe (REC H) to the transport to record the CRC character. The 1 bit is then shifted to bit position 7 and LRC PLS H is generated and sent to the transport to record the LRC character. Thus the CRC and LRC characters are recorded at the end of each record.

3.3.4.2 Write File Mark Circuit – To write a file mark, the controller asserts C WFMK H and C WRE H, places a file character on the write data lines, and issues a SET H pulse, thereby setting the file mark flip-flop (E44-5) and FM LTCH flip-flop (E44-9). After the acceleration delay expires, READING H asserts, WRITING L asserts, and the clock pulse generates REC H. The same clock pulse that generates REC H also generates WR PLS L, which resets the file mark flip-flop on its trailing edge, thereby clearing WRITING L. Thus only one write strobe is generated to record the file mark character. Clearing WRITING L sets the writing done flip-flop and the shift register is loaded and shifted up. However, when CRC WR TIME H asserts, REC H is inhibited by WFMK LTCH (0) H. Therefore, the CRC character is not written. When the 1 is shifted to bit position 7, LRC PLS H is generated the same as in the normal write data mode. Thus the file mark record consists of only two characters.

3.3.5 Record and File Mark Detection Logic

This logic detects data records and file marks (engineering drawing D10). File marks are detected by decoding the characters read; two octal 23 characters at the beginning of a record followed by at least eight blank character frames constitute a file mark record. Data records are detected by counting read strobes; three read strobes constitute a data record.

The MOT H and SET L inputs preset the record and file mark detection logic before the first character (of a current record) and accompanying read strobe is detected. SET L asserts at the beginning of each operation and sets the file mark flip-flop (E47-9), thereby asserting FMK (1) H. MOT H is cleared at the end of each operation and serves to preset the read strobe counter to a count of 1.

3.3.5.1 File Mark Record Detection – When a file mark character (23_8) is the first character read, FMK CHAR L asserts. The assertion of FMK CHAR L is ANDed with the set condition of the file mark flip-flop, placing a high on the D input. Thus the assertion of RD STRB H leaves the flip-flop unchanged and steps the read strobe counter to a count of 2. Now assuming the octal 23 character detected was in fact the first character of a file mark record, the next and final character detected will be the LRC character which is also an octal 23. Therefore when the next character is read, FMK CHAR L remains asserted, the file mark flip-flop remains set, and the read strobe counter is stepped to a count of 3. At a count of 3, ENB FMK CTR H (enable file mark counter) asserts and enables the file mark counter. The file mark counter is then clocked to a count of 8 by TIME PLS 0 L and EIGHT SPACES H asserts, which inhibits the counter and asserts RECORD ACT H. EIGHT SPACES H is ANDed with FMK (1) H to assert FILE MARK DETECTED L.

Note that if another read strobe is received before the file mark counter reaches a count of 8, ENB FMK CTR H clears and RD STRB CTR = 4 (1) H asserts. Thus the file mark counter is cleared and disabled, the read strobe counter is disabled, and RECORD ACT H is asserted. In this case, the two successive octal 23 characters do not constitute a file mark record because data does not follow a file mark record that closely.

3.3.5.2 Data Record Detection – When a character other than an octal 23 is the first character read, FMK CHAR L remains cleared and a low is applied to the file mark flip-flop. Thus the accompanying read strobe resets the file mark flip-flop and steps the read strobe counter to 2. Now, regardless of what the next character is, the file mark flip-flop remains cleared and the read strobe counter is stepped to 3. As previously stated, a count of 3 enables the file mark counter; however, the file mark detection logic was disabled by resetting the file mark flip-flop. Upon the receipt of the next character, the read strobe counter is stepped to a count of 4, RECORD ACT H asserts, and the read strobe counter is disabled.

3.4 MODEL 9700 POWER SUPPLY CIRCUIT DESCRIPTION

The power supply in model 9700 produces the unregulated and regulated voltages required by motors and electronics.

3.4.1 Primary Power

Primary power is switchable to allow either 115 V or 220 V mains. Frequency is not critical and may be from 48 Hz to 500 Hz. These voltages were selected because 220 V mains predominate in Europe. A simple modification allows 230 V operation if required. For 115 V operation, the two 115 V primary windings of T_1 are connected in parallel by S2. For 220 V operation, a 105 V tap on primary winding 2 is connected in series with primary 1. Modification for 230 V operation requires removal of the violet wire and installation of a jumper from S2-6 to S2-3.

3.4.2 Secondary Power

Transformer secondary voltages are rectified to produce nominal unregulated voltages of ±24 V (±26 V under light load) and +8 V. A voltage of ±24 V regulated is supplied to motor drive circuits and provides sources from which ±10 V regulated is produced. A voltage of +8 V is the source for a high efficiency +5 V regulator.

3.4.3 +10 Volt Regulator

Pass transistor Q3 is fed from +24 V and its base is driven by monolithic regulator IC2. Voltage output is determined by R8 and R9. Q7 and Q8 control power supply tracking when powering down. As +24 V drops due to the discharge of C1, Q8 cuts off at approximately 13 V on the +24 V line. When this happens, Q7 is turned on, shorting out R9 and dropping the regulator reference voltage to zero. The +10 V output is cut off and drops to zero. Since +10 V is the reference for −10 V, −10 V also drops to zero. This action occurs before the +5 V supply has dropped sufficiently to cause indeterminate logic states; turn-off transient motions are prevented.

3.4.4 −10 Volt Regulator

The −10 V supply is regulated by pass transistor Q4 driven by Q6. Its reference is +10 V as determined by R13, R14. In this way, the two regulated voltages are made to track or retain a constant relationship to each other.

3.4.5 +5 Volt Regulator

Integrated Circuit regulator IC1 controls +5 V output in conjunction with pass transistor Q1 and driver Q2. Output voltage is set by R4, R5. An inset on the schematic shows the internal circuitry of IC1, IC2. It will be noted that it consists of a differential amplifier with built-in zener reference together with facilities for short-circuit protection. Q2 assures that sufficient base drive is available for Q1.

3.4.6 Short-Circuit Protection

Drop-through series resistors (e.g., R10 in the −10 V supply), provide short-circuit protection. If the drop across R10 exceeds approximately 0.6 V, Q5 is turned on, connecting Q4 base to emitter and cutting off Q4. This corresponds to approximately 1.5 A under short-circuit conditions. Similar circuits are provided in IC1 and IC2.

3.5 TYPE 3842 ADAPTER CONTROL CIRCUIT DESCRIPTION

This module contains a set of receivers for the adapter control commands:

Synchronous Forward (SFC)
Synchronous Reverse (SRC)
Overwrite (OVW)
Rewind (RWC)
Select (SLT)
Set Write Status (SWS)
Off-Line (OFFC)

It also contains drivers that return the recorder status outputs to the interface:

On-Line (ONL)
Rewinding (RWDG)
File Protect (FPT)
Load Point (LP)
Write Enable (WEN)
Ready (RDY)
End of Tape (EOT)
Tape Running (TNG)

Certain controls and delays are also provided to ensure proper tape motion and transport operation.

3.5.1 Tape Motion Controls

The motion control commands from the adapter, SFC and SRC, are translated on this card into the internal motion commands of the transport: run normal ($\overline{RNN}$), forward ($\overline{FWD}$), and reverse ($\overline{RVS}$). These internal motion commands are supplied to the pushbutton control module, where they are combined with commands supplied from the transport pushbuttons and internal interlocks to generate the commands that initiate actual tape motion on the ramp generator module.

On this module, SFC and SRC are supplied to an interlocking network that ensures that the tape comes to a stop before its direction of motion is reversed. The interlocking network includes flip-flop IC1-3, edge circuits IC2-6 and IC2-8, NAND gate IC3-6, and interlocking flip-flop IC3-10. Whenever flip-flop IC1 changes states due to a change in the direction of motion (e.g., from SRC to SFC), its output generates a pulse through the edge circuits consisting of inverters IC2 and the associated capacitors. The pulse is gated through IC3-6 to the set input of interlocking flip-flop IC3-10. The flip-flop can be set only if $\overline{TNG}$ is true, indicating that the tape is still moving. In this case, $\overline{TNG}$ low at input pin W is inverted by IC18-12 and supplies a high input to the clear of IC3. The flip-flop can then be set by the pulse on its set input, its 0 output going low. The 0 output of IC3 then inhibits run normal gate IC15 at pin 2, setting $\overline{RNN}$ false. After the tape has ramped down to a stop, $\overline{TNG}$ goes false, clearing interlocking flip-flop IC3, whose output then enables the run normal gate. $\overline{RNN}$ then goes true if the following conditions are satisfied: SLT1 is true, indicating that the transport is on-line and selected by the adapter; $\overline{BSY}$ is false, indicating that the transport is not rewind or searching for the load point; and an SRC command is not given at the load point. (This would activate NAND gate IC15-8 and would disable the run normal gate at IC15-1.) If the above conditions are satisfied, $\overline{RNN}$ goes true at output pin V, and is supplied to the pushbutton control module where it initiates tape motion at the normal running speed. The direction of motion is determined by the state of flip-flop IC1. If a forward command (SFC) has been given, the flip-flop is set and its 1-output enables NAND gate IC14-8, provided that SLT1 is true and $\overline{BSY}$ is false. This generates $\overline{FWD}$ (forward) true at output pin U. If a reverse command (SRC) has been given, flip-flop IC1 is cleared and enables NAND gate IC14-6, generating $\overline{RVS}$ (reverse) true, providing SLT1 is true, BSY is false, and LP is false. No adapter reverse command is acknowledged by the transport when the load point is detected.

3.5.2 Write Select

During a write operation, the adapter supplies SWS (set write status) true at pin K; SWS is inverted by IC9-4 and is supplied to the D input of flip-flop IC7. The flip-flop is toggled provided that the transport is selected and on-line, after NOR gate IC1-11 is activated by a synchronous motion command. This would activate NAND gate IC1-8 and trigger one-shot IC4-1, generating a 2 μs pulse. On the trailing edge of the pulse, the $\overline{Q}$ output of the one-shot toggles IC7-3, causing the Q output of the flip-flop to go high and activating NAND gate IC10-11, generating WSEL (write select) true at output pin H. During an overwrite operation, OVW true is inverted by IC18-8 and sets the D input of flip-flop IC7-12 high. On the trailing edge of the pulse generated by one-shot IC4-4, the flip-flop is set and enables NAND gate IC8-12. One-shot IC4-4 also direct-sets flip-flop IC11, whose Q output enables the overwrite gate at IC8-9. If write status is true, the gate is enabled at IC8-13 and is kept activated as long as a synchronous motion command is activating NAND gate IC1-8. IC8-8 then goes low and supplies $\overline{WSEL}$ for the duration of the motion command only. When a WRITE AMPLIFIER RESET pulse is given at pin P, it toggles flip-flop IC11 to the cleared state and disables the overwrite gate.

3.5.3 Rewind Flip-Flop

When a RWC (rewind command) is given by the adapter, it sets the rewind flip-flop IC5-3, provided that the transport is selected, on-line, and not at the load point. The 1-output of the flip-flop then goes high, generating RWDG true to the adapter and $\overline{RWC1}$ through an edge circuit consisting of inverter IC6-6, NAND gate IC6-8, and capacitor C5. $\overline{RWC1}$ is supplied to the pushbutton control module. The flip-flop is cleared when the tape returns to and stops at the load point, or when BKN (broken tape) is detected.

3.5.4 End-of-Tape

An end-of-tape indication is set when the EOT marker is encountered in the forward direction and remains set until the marker is passed in the reverse direction.

A true EOT signal at pin Z if machine status is $\overline{\text{RWDG}}$ (IC10-5,8) and $\overline{\text{RVS}}$ (IC14-6) causes IC11 to be preset by IC19-8. An EOT status is then signaled at the interface by IC16-3.

Upon passing the EOT marker in the reverse direction, IC13-3 is high and the EOT signal clocks IC11 clear on the trailing edge of the EOT signal, dropping the EOT signal at the interface. IC11 is preset to the clear state by BKN at pin X.

3.5.5 Output Status

The status gates on this module are all preconditioned by select and on-line being true; consequently, the transport returns status indications only when it is selected and on-line. The READY status is generated when $\overline{\text{BSY}}$ supplied from the pushbutton control module is false and the transport is not rewinding. The LP output is also preconditioned by the rewinding status being false.

3.6 MODEL 9000 TAPE MOTION CONTROLS CIRCUIT DESCRIPTION

The circuitry used to carry out the motion commands issued by the adapter or by the pushbutton panels (both the main control panel and the test panel), is located on Pushbutton Control Card Type 3843 module. This module generates the motion command lines run normal (RNN1), run fast (RNF1), and reverse (RVS1), which are supplied to the ramp generator module to initiate actual tape motion.

3.6.1 Front Panel Pushbutton Controls

The LOAD, ON LINE, and REWIND pushbuttons, located on the main control panel, are connected to respective flip-flops on Pushbutton Control Card Type 3843. When the LOAD pushbutton is activated, it grounds the input to inverter IC12-1, setting the load flip-flop which consists of NOR gate IC13-6 and inverter IC12-1. Once the load flip-flop is set, IC13-6 goes low, is inverted by IC12-4, and removes the direct-clear from on-line flip-flop IC10-3. Thus the on-line flip-flop can be set only after the transport has been loaded. When the ON LINE pushbutton is activated the first time, it toggles IC10-1 to the set, or on-line, position and the outputs of the flip-flops generate ONL and $\overline{\text{ONL}}$ true. Inverters IC12-8 and IC12-10 are connected as a protective flip-flop on the clock input to IC10-1. Once the on-line flip-flop has been set, ONL true is inverted twice by IC9, setting the common of the REWIND pushbutton on the control panel high, disabling that pushbutton. The on-line flip-flop can be cleared by pressing the front panel pushbutton a second time, or by an adapter off-line command (OFFC1), supplied from the adapter control module.

The REWIND pushbutton can be activated only when the transport is off-line. When activated, the REWIND pushbutton sets the flip-flop that consists of gates IC8-8 and IC8-6, provided that the transport is loaded at the time (LOAD true at IC8-13) and test mode is not selected (IC7-8 high). Consequently the transport cannot be rewound by the pushbutton during test mode, when on-line, or when LOAD is false. When the transport is on-line, the rewind flip-flop can be alternately set by $\overline{\text{RWC1}}$, supplied from the adapter control module. The output of the rewind flip-flop, rewinding ($\overline{\text{RWDG1}}$), activates NOR gates IC15-8 and IC14-6, generating RNF1 and RVS1 true to the ramp generator module, initiating a fast reverse motion to the load point. When the load point is detected, the photosensor amp driver module supplies the load point pulse at input pin H of the pushbutton control module, clearing the rewind flip-flop.

An additional flip-flop, IC10-6, is used to locate the tape position. Before the tape is loaded, the flip-flop is cleared by LOAD false at IC10-8. When the transport is loaded, the direct-clear is removed and NAND gate IC14-11 is enabled. Since the on-tape flip-flop is still cleared, its $\overline{\text{Q}}$ output high activates NAND gate IC14-8, generating RNN1 at output pin Y, advancing the tape to the load point. When the load point marker is detected, LP true at input pin 21 from the photosensor module is gated through IC16-3 and direct-sets flip-flop IC10-7 to the on-tape state, terminating the tape motion. Similarly, when the load point is detected during reverse tape motion, the on-tape flip-flop is toggled by NAND gate IC16-11 to the clear state, initiating forward tape motion back to the load point.

3.6.2 Busy

This module generates a BUSY output when the tape is not loaded, when it is advancing to the load point, or when the transport is off-line and not in test mode. In any of these cases, NOR gate IC4-8 is activated and supplies $\overline{BSY}$ true to the adapter control module.

3.6.3 Write Ready

WRDY (write ready) true is generated in two different cases: when the adapter supplies WRITE SELECT true and the transport is not in test mode ($\overline{TM}$ false), or when the transport is in the write test mode and flip-flop IC6-14 is set. In either case, NOR gate IC1-8 is activated, enabling NAND gate IC4-5. The gate is activated provided that $\overline{BSY}$ is false, $\overline{FPT}$ (file protect) is false, and the transport is not in reverse motion (RVS1 is false). IC4-3 then goes low, is inverted by IC5-12, and generates WRDY true at output pin J to Write Amplifier Type 3848.

3.6.4 Test Panel Control

In order to activate the test panel, the transport must be off-line and the test panel STOP pushbutton must be depressed. In that case, the TEST MODE pushbutton on the test panel can be activated, setting the flip-flop that consists of inverters IC11-8 and IC11-10, which in turn toggles the test mode flip-flop IC6-6 to the test mode state, generating TM and $\overline{TM}$ true. The test mode flip-flop is direct-cleared when the transport is placed on-line or when the TEST MODE pushbutton is activated a second time. After the test mode flip-flop has been set, the other test panel pushbuttons are enabled. The WRITE TEST pushbutton may then be activated, setting the protective flip-flop consisting of inverters IC11-4 and IC11-6, which in turn toggles write test flip-flop IC6-1 to the write test mode, provided that forward motion is selected. The Q output of the write test flip-flop then activates NOR gate IC1-8, in turn activating write ready gate IC5-3, provided that FPT, RVS1, and $\overline{BSY}$ are all false. In that case, WRDY true is generated at output pin J to the write amplifier module, where it enables the write data strobe circuitry. During the write test, the write amplifiers generate consectuive all-1s characters which may be used to adjust the skew.

Additional test panel pushbuttons are FORWARD RUN, a normal forward run button, FAST FORWARD, a high-speed forward button, REVERSE, and FAST REVERSE buttons. The reverse motion buttons can be activated only if on-tape flip-flop IC10 is set and the tape is not at the load point, activating NAND gate IC3-3, which in turn activates NAND gate IC7-6 (when the test mode flip-flop is set) and setting the common of the reverse buttons low. The forward motion commands are terminated when either the STOP pushbutton is activated, clearing the test mode flip-flop, or the end of tape is detected, in which case EOT 1 true is inverted by IC17-4, disabling NAND gate IC7-3 and setting the common of both forward motion buttons high. Similarly, the reverse motion can be terminated by activating the STOP pushbutton, which terminates all test mode operations, or when the load point is detected, in which case LP true is inverted by IC17-3 and disables NAND gates IC3-3 and IC7-6, setting the common of the reverse buttons high. The pushbutton control module also drives the test panel indicators, lighting the data lamp when any data is being processed by the write/read electronics, illuminating the skew indicator when the skew is out of adjustment, illuminating the EOT indicator when the transport is at the end of tape, and illuminating the LOAD POINT indicator when the transport is at the beginning of tape.

3.7 TYPE 3194/3645 RAMP GENERATOR CIRCUIT DESCRIPTION

The ramp generator produces the proper analog signal inputs to the capstan servo system to control the direction and velocity of tape motion. The outputs are voltages that rise and fall linearly at controlled rates to highly stable levels. These analog signals are controlled by digital logic outputs from the control section. Waveforms produced are shown with the schematic.

Two similar ramp generator circuits are provided: one for normal speed operation and one for high speed operation. IC4 is an operational amplifier in the run normal speed circuit. The amplifier output is normally saturated in the negative direction. When its positive input at pin 5 is high, the output saturates at +10 V. This occurs when the run normal input sets flip-flop IC7. IC4 feeds FETs Q1, Q2 which are connected in a constant-current circuit. The magnitude of current flow in the circuit is controlled by R3 and R4. R3 controls current in the positive-going direction, or start ramp, while R4 controls the negative-going stop ramp.

Since C1 is charged by a constant current, its voltage rises linearly until clamped by CR1 to a value one diode drop below +5 V. Q3 is an emitter follower whose output rises to a value of +5 V, since the emitter can rise one diode drop higher than the base. When the input from IC7 to IC4 drops, the voltage fed to Q1, Q2 goes to -10 V and C1 is discharged linearly until clamped by the base-collector diode of Q3. Since Q3 base goes one diode drop negative, and the emitter is at zero, a positive-going ramp has been generated.

The ramp voltage output from Q3 is fed to FET switches Q4 and Q5. If forward direction has been selected, Q4 is on and Q5 is off. The ramp is then amplified by unity gain operational amplifier IC3, without inversion, and appears as a positive-going ramp at test point A. If reverse is selected, Q5 is on and Q4 is off. The ramp is then fed to the inverting input of IC3 and appears as a negative-going ramp at test point A. Forward/reverse selection is controlled by flip-flop IC6 and Q9, Q10.

Ramp amplitude and, therefore, tape speed is controlled by normal speed control R14 and output summing resistor R15. The fast forward and reverse ramps are produced by a similar circuit involving amplifiers IC1 and IC2. However, since rewind speed and ramp time need not be precisely controlled, resistors are used instead of FETs to charge and discharge C4 and produce an approximate 0.5 second rise/fall time. CR9 and CR10 isolate the ramp output from any small offsets that may be present in IC2. Rewind speed is controlled by summing resistor R16. Operational amplifier IC5 at zero ramp output has a slight bias produced by R37 and R38, keeping its output negative. When the ramp rises above the bias, IC5 switches to positive output, indicating that the tape is running. This output is used to gate off the input circuits through IC10 and IC9. Flip-flops IC7 and IC8 may be reset by run normal or run fast inputs going false, but cannot be set again until the tape comes to a stop. This prevents damage from illegal commands and reduces timing requirements.

Type 3645 Ramp Generator includes an additional flip-flop, IC11-8, whose function is to enable consecutive run normal commands to be received without requiring the tape to ramp down to a stop following each normal speed operation. Following a run fast command, however, flip-flop IC11 is set by IC8, inhibiting any run normal commands until the tape comes to a stop, at which point IC9-6 clears IC11-9, and the 0 output at IC11-8 enables IC7-2.

3.7.1 Adjustment Procedure

The start/stop time adjustment is as follows:

1. Arrange input signals to the tape transport to start and stop the machine. The rate must allow full ramp time.

2. Adjust the start ramp (R3) for the required time, observing with an oscilloscope at test point A.

3. Adjust the stop ramp (R4) for the required time. Time is measured from maximum volts to 0 V.

The speed adjustment is as follows:

1. Using a master skew tape, drive the transport in a forward direction at normal speed.

2. Observe the data rate at read amplifiers and adjust R14 for correct timing.

3.8 TYPE 3844 SENSOR AMPLIFIER DRIVER CIRCUIT DESCRIPTION

This module responds to signals from photoresistive cells which sense load point and end-of-tape reflective strips, and broken tape. In addition, this module contains the file protect circuitry and the write and the erase head drives.

3.8.1 BOT, EOT, and BKN Sensor Amplifiers

The load point sensor amplifier and the end-of-tape sensor amplifier operate interdependently to detect the load point and the end-of-tape markers. The active components in detecting EOT and load point are two operational amplifiers, IC6 and IC8, and two transistors, Q1 and Q2, in conjunction with associated components. Transistors Q1 and Q2 act as current sources; potentiometer R16 is used to adjust the transistor base currents to equalize the voltage at the inputs of IC8, the load point sensor amplifier, and IC6, the end-of-tape sensor amplifier. Resistors R18, R19, R20, and R21 are used to bias the amplifiers' inputs when plain tape is in front of the photo sensors. When either the load point marker or the end-of-tape marker is detected, the resistance of the respective photoresistive cell is lowered by approximately 60 percent of its unilluminated value. Each cell is returned to +10 V, and a 30 percent change in its resistance, causing a 30 percent change in the input potential, will be sufficient to switch the output of the respective operational amplifier. Resistors R17 and R22 serve as feedback loops for noise protection. Thus when load point is detected, the load point sensor output at input pin Y of this module saturates IC8, causing its output to go high, and is inverted twice by IC7 to generate LDP (load point) true at output pin 19 to the pushbutton control module. The output of inverter IC7-8 is also supplied to an edge circuit which produces a 1 μs pulse on the trailing edge of LDP. This pulse is output at pin 8 to the pushbutton control module. The EOT sensor amplifier operates in the same manner, generating a high output when the EOT marker is detected, and supplying EOT true at output pin X to the pushbutton control and control adapter modules.

When the broken tape photoresistive cell is illuminated, the resistance of the cell is reduced enough for the +10 V to turn on transistor Q3. The collector of the transistor goes to ground, generating BKN (broken tape) true at output pin 18. When $\overline{\text{LOAD}}$ is high at input pin U, the output of IC4-8 is low. This causes the collector of Q3 to be low through the diode CR3 and the BKN output will be true at output pin 18. Also, when power is initially turned on, capacitor C9 will cause the BKN output to be high, which presets the load flip-flop on the adapter control module.

3.8.2 File Protect Circuits

The file protect switch output is supplied to this module at input pin T. When a reel is loaded without a write enable ring, the switch contact remains grounded; the switch input at pin T is inverted by IC2-6 and enables NAND gate IC4-13. The gate is activated when BKN is true before the transport is loaded. Whenever the LOAD pushbutton has not been energized, IC4-8 low grounds the clear input of flip-flop IC4-1 through diode CR14. IC4-2 then issues $\overline{\text{FPT}}$ (file protect) true at output pin 9 to the adapter control card, while the 0 output of IC4 high is inverted by IC2-8 to turn off transistor Q5, disabling the file protect solenoid output at pin P.

When a reel with a write enable ring is used, the file protect switch is opened, setting input pin T high and enabling NAND gate IC2-13. Again the gate can be activated only when BKN is high, before the transport is loaded. The output of the gate then goes low to set flip-flop IC4-5; the flip-flop can be set only after $\overline{\text{LOAD}}$ has gone false. This provision is made to ensure that the write mode can be selected only at the time tape is first loaded. Once flip-flop IC4 is set, its 1 output issues $\overline{\text{FPT}}$ false, and, after being inverted by IC1-10, lights the WRITE ENABLE lamp through output pin H. The 0 output of the flip-flop low is inverted by IC2-8 and turns on transistor Q5, activating the file protect solenoid through pin P. The file protect solenoid then draws in the switch pin, and the transport is ready for the write operation.

3.8.3 Write, Erase Drives

When the file protect switch is grounded, it also turns off transistor Q7, in turn shutting off the current at the base of Q8. This cuts off the write head and erase head drive currents supplied by transistor Q8. In order for the write and erase drives to be turned on, the file protect switch must be opened and WRITE READY must be true at input pin 2. This will activate NAND gate IC2-3, causing op amp IC3 to turn off transistor Q9, in turn enabling transistor Q8 to turn on and supply the write and erase head drives at pins 22 and J.

The zener diode into the base of Q7 detects when power is being dropped. This turns off Q7 early enough in the power-down sequence to turn on Q9 and remove the head voltage supplied by Q8. This avoids putting unwanted remnants on tape during a power failure.

3.9 TYPE 4306 SERVO PREAMPLIFIER CIRCUIT DESCRIPTION

This module contains the capstan servo and reel servo amplifier stages. The following paragraphs describe their operation.

3.9.1 Capstan Servo Amplifier Stage

The capstan servo amplifier portion of this module is a part of a velocity servo system which produces accurately controlled capstan speeds with linear ramp-ups and ramp-downs. The analog linear signal supplied from the ramp generator module is input at pin N of this module and is summed with the output of the dc tachometer coupled to the capstan motor shaft, supplied at pin P of this module. Any difference between the two voltages is amplified by operational amplifier IC5. The amplification of IC5 is controlled by two negative feedback loops, one supplied directly from the output of IC5 through resistors R39, R40 and capacitor C9, and the other loop from the capstan motor through resistor R71. The zero offset of the amplifier is adjusted by potentiometer R56 to eliminate capstan creep during standstill, as described below.

The output of amplifier IC5 is supplied to a pair of complementary driver stages, including transistors Q11, Q12, Q17, and Q18. The output of these stages is supplied to a pair of power transistors located on the heat sink servo power assembly, which is on the rear of the unit. The power transistors' output then energizes the capstan motor, advancing tape at accurately controlled speeds.

3.9.2 Reel Servo Amplifiers

Takeup and supply reel servos are provided to maintain tape tension at a constant value. Three main components are included: magpot position sensor, reel servo amplifier, and reel motor.

The magpot position sensor measures tape tension by the position of a spring-loaded buffer arm. At the approximate center of the arc, sensor output is zero. As the buffer arm moves off center, a positive or negative voltage is produced which is proportional to the error.

The output of the reel servo amplifier on this module is supplied to a pair of power transistors located on the servo power assembly on the heat sink on the rear of the unit. The output of the power transistors then energizes the respective reel motor, returning the buffer arms to their proper locations.

3.9.3 Servo Adjustments

The adjustment given below becomes necessary when a capstan creep is detected during standstill.

1. Connect an oscilloscope probe to monitor the voltage at output pin X, measuring the output of the capstan servo amplifier stage.

2. With the transport on-line and loaded but in a stopped condition, adjust potentiometer R56 so that a straight-line trace is produced. Use the 0.5 V/cm scale on scope.

3. Observe that the capstan does not rotate.

3.10 TYPE 3631 READ PREAMPLIFIER CIRCUIT DESCRIPTION

Read Preamplifier Type 3631 includes nine identical amplifier stages which accept the analog signals from the read head winding and supply the amplified outputs to the read amplifier modules.

The channel 0 amplifier stage is shown in the schematic; the other channels are identical. The amplifier stage consists of high-gain operational amplifier IC1 and negative feedback including resistors R2, R3, R4, R5, and capacitor C2. The input head signal is filtered by resistor R1 and capacitor C1, and is supplied to the noninverting input of IC1. The negative feedback network controls the output amplitude and response.

In NRZ-only tape units, potentiometer R4, located in the feedback network, is adjusted so that the amplified analog output at test point A is 9 V peak-to-peak while writing 800 flux reversals per inch.

3.11 TYPE 4218 MAGPOT TENSION ARM POSITION SENSOR CIRCUIT DESCRIPTION

In the reel servo system it is necessary to produce an analog signal representing tension arm position. The signal must be zero at the nominal resting position of the tension arms and should linearly represent angular deviations from the center of arm travel by positive and negative voltages. A common method utilizes lamps, photocells, and a shutter to produce the required voltage. This method suffers from the mortality of lamps and the relatively slow response of photocells.

The magpot operates as a differential transformer, an example of which is shown in Figure 3-2.

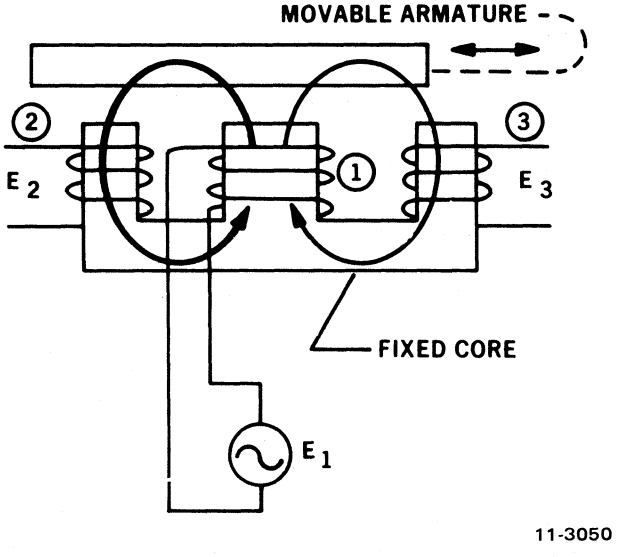


Figure 3-2 Differential Transformer

Magnetic flux produced by current in winding 1 will produce voltages E_2 and E_3 in the other windings. If the armature is symmetrically located with respect to 2 and 3, flux in the two windings will be equal, and since they have the same number of turns, $E_2 = E_3$. If the armature is displaced as shown, $E_2 > E_3$ since the flux coupling E_3 has been reduced. Displacement in the opposite direction produces $E_3 > E_2$. Displacement from center then is represented by $E_0 = E_2 - E_3$. In the configuration shown in Figure 3-2, this relation is linear only for very small displacements because area relations are not linear.

The magpot is an adaptation of the above scheme in that there are three windings on a magnetic core. The core in this case is a ferrite pot core while the armature is half a pot core. Windings 2 and 3 are around legs of the pot core while 1 is around the center portion common to the two legs. Winding 1 is energized by a high-frequency oscillator (approximately 200 kHz). The magpot is in balance and $E_2 = E_3$ when the armature couples equally to the two legs. As the armature is rotated, the area available for magnetic flux increases linearly for one leg and decreases linearly for the other leg. Thus the difference in induced voltages is a linear representation of angular movement.

The 200 kHz oscillator is a Hartley circuit comprising Q1, C1, C2, R1, R2. It produces a 40 V peak-to-peak sine wave across the primary winding.

The two secondary windings are connected in series and their voltages are rectified by CR1, CR2. The two rectified voltages are subtracted and referenced to ground. Thus the input to IC1 operational amplifier is a dc voltage equal to $E_1 - E_3$. This voltage is null when $E_2 = E_3$ and is positive or negative depending upon which is larger. Secondary voltages induced are at all times large enough to overcome the diode drops in CR1, CR2.

DC output of the rectifier circuit is amplified by IC1 and fed from the output to the appropriate reel servo amplifier.

Voltage output for a given angular deflection depends upon coupling between the fixed core and armature at that setting. The gain relations are such that a spacing of 0.030 in. between core and armature results in ±5 V output for full arm travel. Spacing is established by two 0.015-in. thick plastic spacer washers on the shaft.

If adjustment is required:

1. Remove tape from the machine.
2. Place a short length of tape in front of the broken tape sensor.
3. Turn power on and press LOAD. The reels will rotate.
4. Hold the tension arm in approximately the center of the arc. Reel rotation should stop.
5. If the reel continues to rotate, loosen the set screw holding the armature to the tension arm shaft.
6. Rotate the armature until reel hub motion ceases. Press firmly against the fixed core to maintain core to armature spacing.
7. Tighten the set screw.
8. Move the arm to its limits of travel and observe directions of reel hub rotation. There are two null positions 180 degrees apart. The sense of the output is reversed for one null, causing hub rotation to be wrong. If this null has been chosen, loosen the set screw, rotate the armature 180 degrees, and repeat.
9. Check the output at pin 4 using a voltmeter. Total output swing should be between 10 and 12 V (±5 V nominal).

3.12 TYPE 4845 DELAY TIMING CIRCUIT DESCRIPTION

Crystal oscillator, dividers, and timing circuits associated with read electronics comprise Type 4845 Delay Timing. Use of this circuitry eliminates the need for analog delays in forming the read skew gate, detecting gaps, etc. Since the delays required vary with tape speed, switches are provided to select appropriate delays. Delays required are fractions or multiples of character times; therefore it is only necessary to change the division ratio to modify all required. Crystal-controlled pulses generated are also supplied to write electronics in the test mode to allow writing an all 1s test pattern.

3.12.1 Crystal Oscillator Divider

IC5 together with several discrete components is connected as a crystal oscillator. The two inverter sections are biased into the linear region by R1, R2, and R3. Positive feedback through Y1 causes the circuit to oscillate at the crystal frequency. A series of dividers IC2 (÷ 2,6) IC1, IC4 (÷ 16) are selectable by S1–S7 to produce two output frequencies: f_r, which is the repetition frequency of the data to be read (20 kHz at 25 in./sec) and f_1 which is $32 \times f_r$ and divides the bit cell into 32 increments. These are fed to counter circuits which determine delays.

3.12.2 Skew Gate Generation

Skew gate length has three values depending upon operating mode: 1/2 of one bit cell for read, 3/8 for write, and 5/32 for test mode. The write skew gate is shortened to provide a more stringent skew criterion to reveal incipient skew problems.

Pulse outputs from the nine read amplifiers are wire-ORed and appear at pin R. IC3 buffers the pulse input and feeds out to the test panel for service use.

The first pulse to appear clears IC14 and counter IC15 begins to count f_1 pulses. IC15 has been preset clear by low levels on inputs ABCD. At the count of 16, representing 1/2 character time, IC15 Q_D has been high and goes low, setting IC14 and stopping the count. With IC14 set, IC11, a four-stage shift register, starts shifting right. A 1 has been preset in position A and 0s are shifted in, causing the 1 to progress to the right. Shift frequency is f_1. At the time IC14 is set, a 1 is in Q_A and IC12 produces a data transfer pulse to the read amplifiers, causing the data to appear at their outputs. At the next count Q_B goes high, triggering one-shot IC10 (2 μs) and producing a read data strobe (RDS) at the output. At the third count Q_C goes high as a delay, and on the fourth count Q_D goes high. If strap ST1 is installed, a second data transfer pulse is produced, returning the read amplifier output to zero. After the fourth shift pulse, the circuit remains quiescent until the next peak pulse.

3.12.3 Skew Lamp

At a time just after the skew gate (at RDS time), output from IC14 is inspected by one-shot IC10. If the skew delay circuit has been retriggered by a skewed input, IC10 is triggered, producing a relatively long pulse to the SKEW indicator lamp.

3.12.4 Write Mode

If write is selected, WRDY is high, causing counter IC15 to be preset with a count of 4 by IC12. Operation is otherwise identical to read operation but delay is reduced from 16 to 12 counts or 3/8 of one bit cell.

3.12.5 Test Mode

In test mode, delay is further reduced to provide a marginal skew check. The counter is preset by the test mode input (pin U) to 11 and delay is five counts or 5/32 of one bit cell. At 25 in./sec this is 7.8 μs. An all 1s pattern on a properly deskewed machine should fall within this time; however, due to bit crowding on tape, random data generally will not.

3.12.6 Gap Detection

Type 4845 detects the space between the last data character and the CRC and clears read amplifier outputs. The read amplifier outputs are again cleared after the CRC (if not all zeros) and once again after the LRC, leaving all outputs cleared in the IRG. Whenever IC14 is set (between bits), counter chain IC6, IC7 counts f_1; it is cleared by IC14 if a peak pulse is detected. Should the counter reach a count of 32, indicating a missing bit, IC7 is set which in turn sets IC8. The next f_1 pulse, through IC8 pin 3, clears IC7, leaving IC8 set and the counter held clear by IC8 pins 8, 12. IC9 produces a $\overline{\text{RESET}}$ pulse at pin K, clearing the read amplifier. At the next peak pulse, input IC8 is cleared and the cycle is free to repeat. This peak pulse may result from the CRC, LRC, or the first character of the succeeding block.

3.12.7 Start Delay

When tape is stopped (as indicated by RNN) or if BSY or SLT1, or at LP, RDS outputs are gated off by IC19, IC9 and read amplifiers are held reset by IC9.

Upon receipt of an $\overline{\text{RNN}}$, input counter chain IC17, IC18 is enabled for a count of 128 f_r pulses. This corresponds to 0.16 in. of tape movement. During this time, outputs remain disabled.

3.12.8 Data Lamp

Drive for the test panel data lamp comes from IC6 through IC8 pin 6, which is low whenever IC4 is set (between characters). An inverter on the PCB module actually drives the LED indicator.

3.12.9 Adjustments

No adjustments are required on type 4845. However, the proper setting of the speed select switches is essential. A chart is given on the schematic showing crystal frequency and switch settings for a variety of speeds.

3.13 TYPE 3848 WRITE AMPLIFIERS CIRCUIT DESCRIPTION

This module generates the internal write data strobe and contains the write amplifier stages for four of the data channels, channel P through channel 2. These are explained in detail below.

3.13.1 Write Data Strobe Generation

The WDS (write data strobe) is input from the adapter at pin N and is supplied to an edge circuit consisting of inverters IC5 and IC6, capacitor C8, and NAND gate IC6-8. If WRDY (write ready) and SLT1 (select) are true at input pins 12 and 13 of IC6, the gate transmits a short pulse on the leading edge of each input WDS. The pulse is gated through NOR gate IC5-6 and triggers one-shot IC1-1 on its trailing edge. The Q output of the one-shot supplies a positive 0.5 μs pulse which is gated through NAND gate IC7-3, provided that the transport is not in a test mode. The pulse then enables write NAND gates IC11 and IC15, gating the input write data to the write amplifier stages. It is also supplied as WDS1 to Type 3849 Write Amplifier module. When IC1-13 generates the write strobe, its Q output triggers the second IC1 one-shot, which in turn inhibits IC6 for a 3.5 μs duration, inhibiting any pulses during that time.

If the transport is in test mode, TM true at pin K enables NAND gates IC5-2 and IC7-10, 12 while disabling NAND gate IC7-2. If WRDY is true, crystal-controlled data frequency f_r, supplied from the delay timing module, is gated through NAND gate IC5-12 and NOR gate IC5-6 to generate the test mode strobes. These are gated through the two IC7 NAND gates and direct-clear the write amplifier flip-flops on this module and on the other write amplifier module, writing the all-1s characters of the test mode.

3.13.2 Write Amplifier Stages

The data inputs are supplied from the data terminator card at pins R, S, T, and U, are inverted, and then strobed through NAND gates IC11 and IC15 by the WDS1, generated at test point B. The write channels are then supplied to the amplifier stages, each consisting of a divide-by-16 counter, a pair of flip-flops, and a pair of drivers. The amplifier stages are digitally deskewable, where the delay of channels 0 through 7 is adjusted to coincide with that of the reference channel, channel P, when read back.

The delay of channel P is permanently set to the count of eight, equivalent to 1/4 character delay, by counter IC8. Whenever the input data is 1, the WDS pulse is gated through IC11-8 and direct-clears flip-flop IC9-13. The Q output of the flip-flop goes high, removing the direct-clear from the IC8 counter. The counter is then clocked by f_1 at 32 times the data frequency until the count of eight, at which point the Q_d output of the counter goes low and toggles the IC9 flip-flop to the set state. The $\overline{Q}$ output of IC9 then goes low, locking the counter and toggling the output flip-flop IC9-9. During the next 1 character, the same process is repeated with output flip-flop IC9-9 toggling to the opposite state. When a 0 is input, the input NAND gate IC11-8 does not transmit the write data strobe, and consequently the write amplifier flip-flops are not toggled. The outputs of flip-flop IC9-5, 6 are then supplied to a pair of drivers IC10 which energize the write head, reversing the flux for each 1 while remaining unchanged for each 0, as required for NRZI.

The operation of the amplifier stages of the eight other channels is identical to that of channel P, except that their delay is digitally adjustable. Four switches are connected to the parallel inputs of the skew delay counters of the eight channels, as shown for data channel 0. The skew of each channel can be measured and adjusted during the write test mode, which writes all-1s characters, by observing the analog outputs at the Type 3631 Read Preamplifier module.

Trigger channel 1 of a dual trace oscilloscope on the P channel so that one peak is easily observed. With channel 2 of the oscilloscope, observe the preamplifier channel that is to be checked or adjusted. Set the switches on the write amplifier channel so that the peaks of the two observed channels coincide. A small amount of jitter will be seen on the channel being adjusted due to tape recorder dynamics. Repeat the observations for all eight channels leaving the P channel as the reference.

Opening the switches reduces the count while closing them increases it. Thus when the switches are all opened the counter is direct-set to 16, gating the data character to the output without any delay. When the switches are all closed, the skew counter is set at 0 and the character will be delayed 16 counts, or 1/4 character time behind channel P.

3.13.3 Write Amplifier Reset

$\overline{\text{WARS}}$ (write amplifier reset) pulse is input at pin P from the data terminator card, and is gated through NAND gate IC2-3, provided that select 1 is true, to set flip-flop IC2-12. The 1 output of the flip-flop goes high, removing the direct-clear from shift register IC3. The register is then clocked by f_1 at 32 times the data frequency. On the seventh pulse, the Q_g output of the register goes high and is inverted by IC4-8 to issue $\overline{\text{WARS1}}$, resetting the write amplifier flip-flops on this module. $\overline{\text{WARS1}}$ is also output at pin H to the Type 3849 Write Amplifier where it resets the flip-flops of the other amplifier stages. On the eighth pulse to the register, the Q_h output goes high and is inverted by IC4-11, clearing flip-flop IC2 and locking itself until the next $\overline{\text{WARS}}$ is issued by the interface.

3.14 TYPE 4178 QUAD READ AMPLIFIER CIRCUIT DESCRIPTION

Quad Read Amplifier Type 4178 accepts amplified head signals from the head preamplifier module and supplies decoded and deskewed data outputs to the adapter. Each module contains four amplifier stages, and each recorder contains two of these modules. The channel P amplifier stage is located on the read amplifier/clipping control module. The operation of the channel A amplifier stage is explained in the following paragraphs. The other amplifier stages operate identically.

The amplified analog signal is supplied from the read preamplifier at input pin E. The signal is filtered through R1, C1; the negative half-waves are routed through diode CR1 while the positive half-waves are routed through CR2. CR1 and CR2 are back biased by the negative and positive clipping levels, respectively, supplied from the read amplifier/clipping control module, to eliminate spurious baseline pulses. The negative half-waves are then differentiated by C4 and R6 and are input at the inverting input of operational amplifier IC1. At the leading edge of the negative analog half-wave, the differentiated output of C4 and R6 swings negative, crossing zero at the peak of the analog signal and then going positive until the trailing edge of the analog signal. Normally the op amp output is low, since the noninverting input of IC1 is negatively biased through R7 and R9. When the leading edge of the differentiated signal exceeds the input threshold, the output of the amplifier swings positive. The amplifier output returns to 0 V at the zero crossover of the differentiated signal, corresponding to the peak of the input analog signal. A similar transition occurs for the positive half-wave, since it is input at the noninverting input of the amplifier. Consequently the amplifier output goes high and returns low for each 1 character, with the negative-going transition occurring at the analog peak. The output of the amplifier is limited by diodes CR3 and CR4 and is inverted by NAND gate IC2-3. IC2-3 output is supplied to a filtering network, consisting of C6, R11, R12, and CR5, whose output is in turn supplied to the Schmitt trigger input of one-shot IC3. The output of IC2-3 is normally high, and the voltage at the input of IC3-5 is at 3.3 V. When the output of IC1 swings positive, IC2-3 goes low and capacitor C6 discharges through R12 with a slow time constant, approximately 5 μs at 25 in./sec. The voltage is clamped at 0 V by diode CR5. When the output of IC1 goes low again at the peak of the analog input, IC2-3 goes high and C6 charges with a much faster time constant, approximately 300 ns. When C6 charges up to 1.8 V, one-shot IC3 triggers, generating a 300 ns pulse. The Q output of the one-shot is connected back to IC2-2, disabling the gate and preventing the one-shot from being retriggered by spurious pulses on the input.

The positive pulse generated by the Q output of IC3 is inverted by IC2-11 and is output as $\overline{\text{PULSE OUT}}$ at pin V. The pulses of all the amplifier stages are wire-ORed and supplied to the delay timing module where they are used for read deskewing and read data strobe generation. The Q output of one-shot IC3 direct-sets flip-flop IC4-4, the data

3.7.3.2 End-of-File Bit (14) – Bit 14 is used to indicate that the tape has reached the end of the file. The EOF flip-flop (Drawing TMA11-0-18) is set by the master tape transport and cleared by INIT or a GO pulse. The input to the flip-flop is the FMK (file mark) signal from the master tape transport. This signal, when present, indicates that the transport has detected the end-of-file mark on the tape. The signal sets the EOF flip-flop to produce the EOFF H signal.

3.7.3.3 Cyclic Redundancy Error Bit (13) – The cyclic redundancy error (CRE) bit in the status register indicates that the cyclic redundancy check has detected a parity error. This check compares the CRC character written during a write or write-with-extended-IRG operation with the CRC character generated during a read operation.

The comparison of the two CRC characters is performed by logic within the master tape transport. If the two characters are not identical, then the CRCE from the tape unit becomes a 1 and is applied to gating logic in the controller error circuits (Drawing TMA11-0-18). The gating logic sets the CRE flip-flop to produce CRE H.

The CRE output of the flip-flop is applied to gating logic associated with the command register ERR flip-flop. Note, however, that the AND gate is not qualified until both CRE and LRCSD H are present. The latter signal indicates that the LRC character has been detected. Thus, when a CRC error is detected, the CRE bit in the status register is set immediately, but the ERR bit in the command register is not set until the LRC is detected. This gives the controller time to complete the current operation before branching to an error routine by means of the interrupt.

3.7.3.4 Parity Error Bit (12) – The parity error (PAE) bit in the status register indicates that a parity error exists in the data. The error may be in either vertical or longitudinal parity. A vertical parity error is indicated for any character in a record; a longitudinal parity error indicates an error in a specific channel.

The parity error circuits are shown on Drawing TMA11-0-18. An AND gate output is used to set the PAE flip-flop; this AND gate is qualified by three inputs. The first input is RDS H from the master tape transport, which is used to sample parity. The second input is either WRITE ENB or READ, because parity is checked during both read and write operations. The third input is either the BPE (vertical parity error) or LRCE (longitudinal redundancy check error) signal from the transport. Thus, both vertical and longitudinal parity errors are detected during read, write, write EOF, and write-with-extended-IRG operations. The entire record is checked, including the CRC and LRC characters.

Note that longitudinal parity occurs when an odd number of 1s is present in any channel in the record; vertical parity errors may be even or odd, depending on the setting of the PEVN bit in the command register.

The PAE output of the parity error flip-flop is applied to command register gating logic in the same manner as the CRE output, as explained previously. In the case of PAE, the PAE bit in the status register is set immediately, but the command register ERR flip-flop is not set until detection of the LRC character.

3.7.3.5 Bus Grant Late Error Bit (11) – During normal operation, the controller makes an NPR request to gain control of the bus and initiate a data transfer (either a read or a write). If the controller is still engaged in the NPR transfer when another NPR request is initiated, a BGL error condition occurs.

The BGL flip-flop is shown on Drawing TMA11-0-18. It is set (indicating an error) when both the NPR ENB and NPR SET inputs are high. These inputs are received from the NPR input logic (Drawing TMA11-0-11).

If the controller receives either a WRS or RDS pulse from the master tape transport, the NPR logic circuits produce the NPR SET H pulse. This pulse is gated through an AND gate and sets the NPR request flip-flop on its trailing edge.

If, however, the NPR transfer is still occurring when the next NPR SET H pulse occurs, the BGL flip-flop is set to indicate an error. The NPR request flip-flop is cleared at the end of an NPR transaction by the NPR CLEAR BBSY H signal.

During a read-after-write operation, WRDY at input pin J is inverted by IC7-12 and disables the automatic clipping level control by direct-setting the IC10 flip-flops, keeping the IC11 counter direct-cleared. At the same time, WRDY true activates NOR gate IC13-4, enabling the higher clipping level, while the Q output of IC11-5 low enables the normal clipping level. Thus the normal and high clipping levels are combined to generate a still higher clipping level used during read-after-write only.

The automatic clipping level control is also disabled when the adapter supplies AUTO DISABLE true at input pin N, or when $\overline{\text{BSY}}$ is true at input pin Y of the module. In either case, NOR gate IC7-6 is high, and direct-sets the IC10 flip-flops which in turn keep the reread counter IC11 cleared.

Operational amplifier IC6 is connected with negative feedback through R26, establishing its gain at a value determined by the ratio of the input resistance to +10 V switched by IC13 to the value of R26 (22K).

Capacitor C10 acts as an integrator, slowing the response of IC6 to a change in input, which avoids coupling enough signal through C4 and C5 into IC1 to cause a spurious output. IC5 is connected as an inverter, outputting an equal but opposite polarity voltage to that voltage at IC6-10. The negative clipping level voltage (TPD) and positive clipping level voltage (TPC) are then applied to each read amplifier through a resistor dividing network to backbias diodes CR1 and CR2. This establishes the amplitude of analog input from the read preamplifier required for IC1 to switch and thus detect data.

CHAPTER 4
PARTS IDENTIFICATION

Figures 4-1 through 4-3 and Tables 4-1 through 4-3 show the location and identify parts comprising the TS03 DECmagtape Transport. Table 4-4 lists replaceable/spare parts.

NOTE

See the engineering drawing set for parts information on the M8920 adapter module.

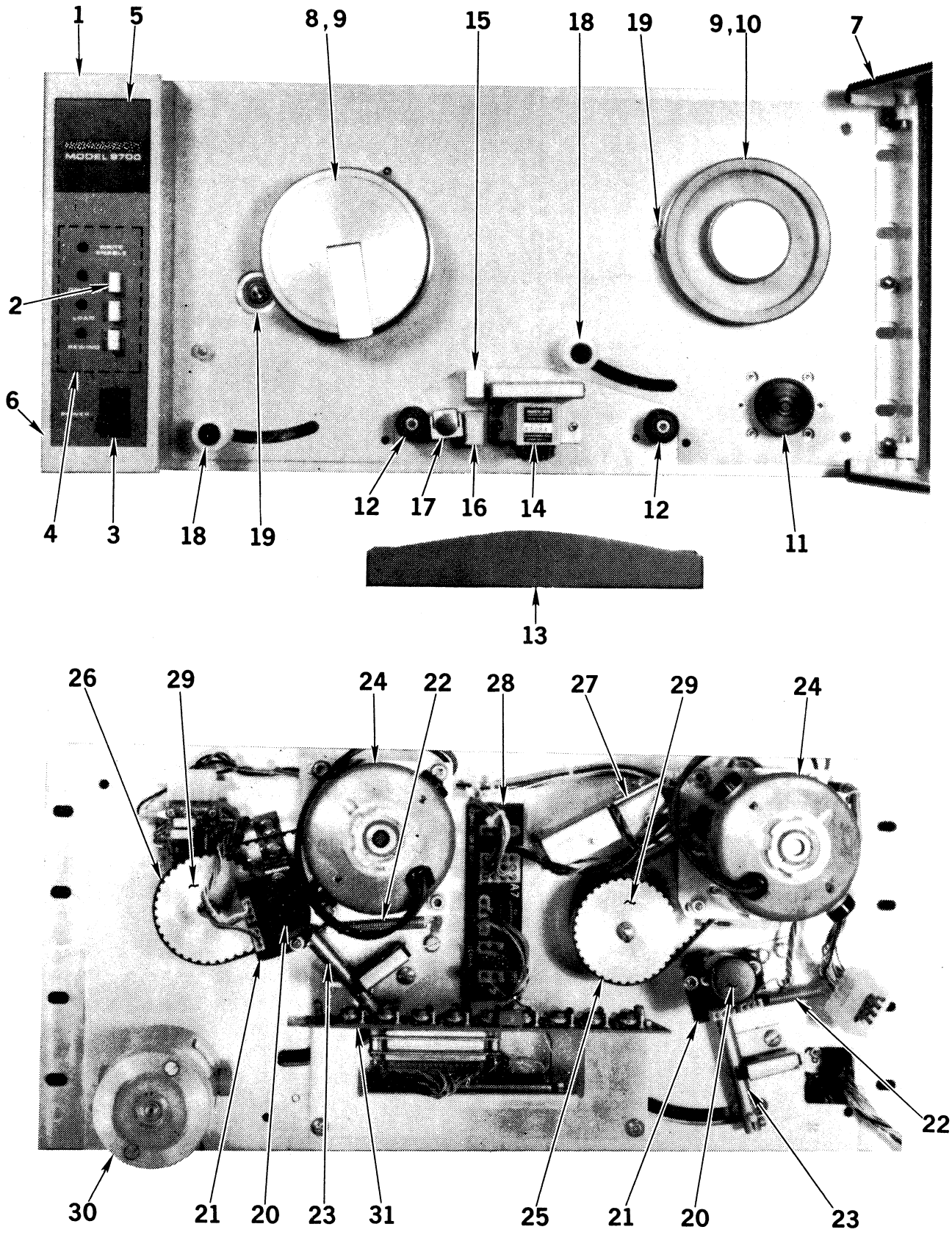


Figure 4-1 Front Panel Parts Identification

Table 4-1
Illustrated Parts Breakdown for Figure 4-1

Item	Part No.	Description
1-1	*	Control Panel Assembly (Note 1)
1-2	151-0057-001	Pushbutton Switch Assembly
1-3	151-0038-001	Power Switch
1-4	190-4448-001	LED Display, PC Board Assembly
1-5	291-3922-xxx	Switch Cover (Note 1)
1-6	391-4440-xxx	Control Panel (Note 1)
1-7	*	Dust Cover Assembly
1-8	190-2744-001	Hub, Quick Release (Note 2)
1-9	198-0011-001	Hub Bearing Assembly
1-10	190-2772-001	Takeup Hub
1-11	*	Capstan Wheel
1-12	*	Tape Guide Assembly
1-13	291-1509-001	Head Cover (Note 1)
1-14	*	Head Assembly
1-15	*	Photosensor Assembly, Load Point, EOT
1-16	*	Photosensor Assembly, Broken Tape
1-17	*	Tape Cleaner
1-18	*	Tension Roller Guide Assembly
1-19	190-4554-001	Tension Arm Bearing Assembly
1-20	*	Magpot Tension Sensor Assembly
1-21	*	Magpot Circuit Module
1-22	*	Spring, Tension
1-23	*	Tension Arm Assembly
1-24	*	Reel Motor Assembly
1-25	*	Belt, Supply Drive
1-26	*	Belt, Takeup Drive
1-27	*	File Protect Switch Assembly
1-28	190-4013-001	Connector PC Board Assembly
1-29	191-0805-001	Pulley, Reel Drive
1-30	*	Capstan Motor/Tachometer Assembly
1-31	*	Read Preamplifier PC Board Assembly

NOTES
1. Specify logo and paint color if different from standard.
2. Order repair kit 198-0100-001 as spare (Table 4-4).

*Indicates replaceable part. For part number, see Replaceable Parts List (Table 4-4).

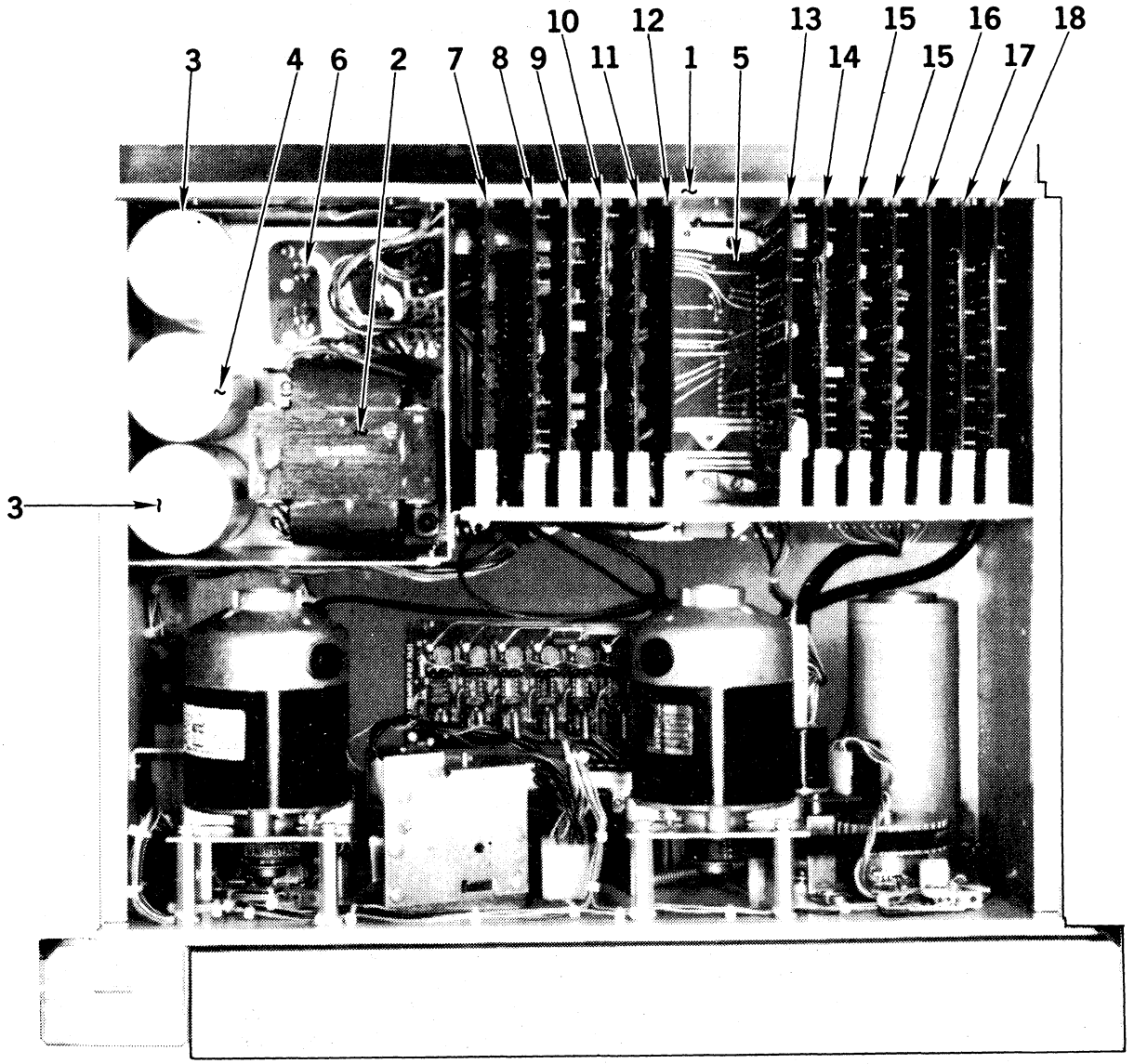


Figure 4-2 Tape Transport Parts Identification (Top View)

Table 4-2
Illustrated Parts Breakdown for Figure 4-2

Item	Part No.	Description
2-1	190-4442-001	Power Supply/Card Cage Assembly
2-2	*	Transformer Assembly
2-3	*	Capacitor, 18,000 mF/25 V
2-4	*	Capacitor, 39,000 mF/10 V
2-5	190-4206-001	Motherboard Assembly
2-6	*	Rectifier
2-7	*	Servo Preamplifier Module
2-8	*	Sensor Amplifier/Driver Module
2-9	*	Ramp Generator Module
2-10	*	Pushbutton Control Module
2-11	*	Control Interface Module
2-12	190-3841-001	Control Terminator Module
2-13	*	Delay Timing Module
2-14	*	Read Amplifier/Clipping Control Module
2-15	*	Quad Read Amplifier Module
2-16	190-3860-001	Data Terminator Module
2-17	*	Four-Channel Write Amplifier Module
2-18	*	Five-Channel Write Amplifier Module

*Indicates replaceable part. For part number, see Table 4-4.

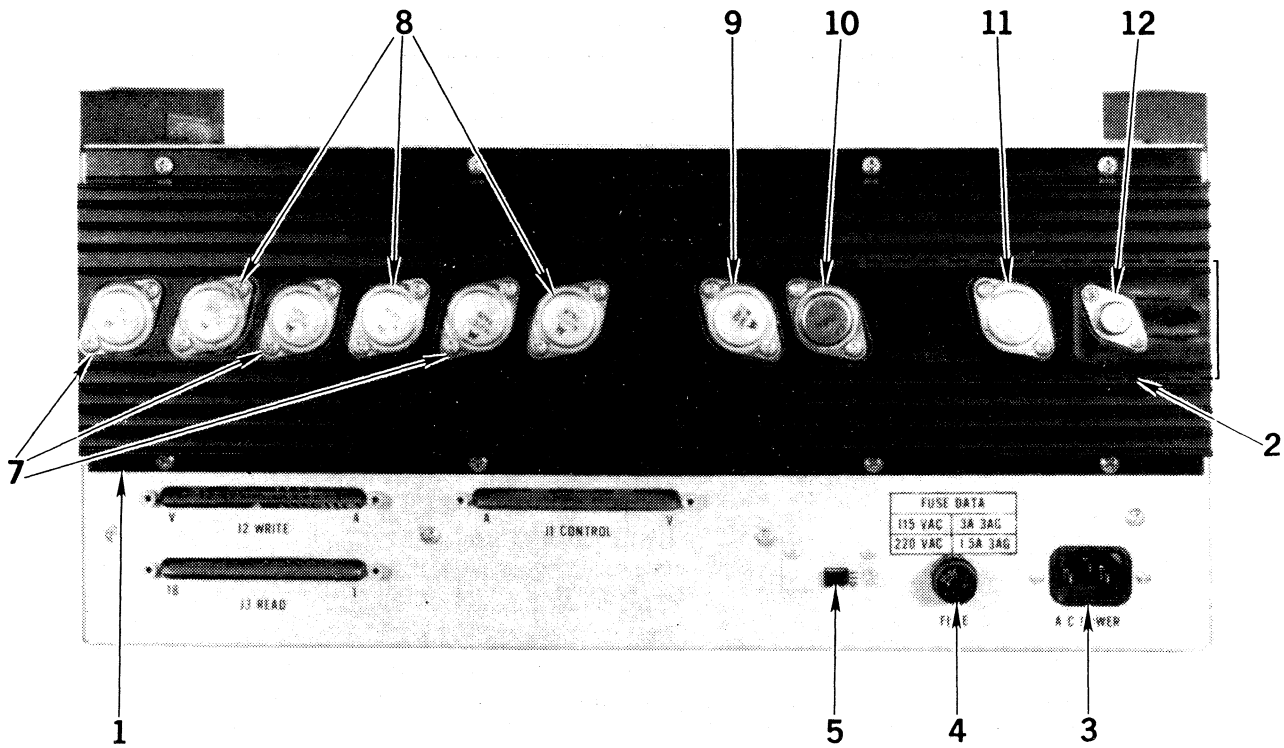


Figure 4-3 Tape Transport Parts Identification (Rear View)

Table 4-3
Illustrated Parts Breakdown for Figure 4-3

Item	Part No.	Description
3-1	*	Voltage Regulator/Servo Power Assembly
3-2	190-4352-001	Voltage Regulator PC Board Assembly (Note 1)
3-3	127-0003-001	Power Receptacle
3-4	*	Fuseholder
3-4	*	Fuse, 3AG, 3 A (115 V operation)
3-4	*	Fuse, 3AG, 1.5 A (220/230 V operation)
3-5	*	Switch, 115/220 V
3-6	*	Power Cord (not shown)
3-7	148-0122-001	Power Transistor Type MJ802 Motorola (Note 1)
3-8	148-0121-001	Power Transistor Type MJ4502 Motorola (Note 1)
3-9	148-0102-003	Power Transistor Type MJ900 Motorola (Note 1)
3-10	148-0102-004	Power Transistor Type MJ1000 Motorola (Note 1)
3-11	148-0053-001	Power Transistor Type 2N3055 (Note 1)
3-12	148-0075-001	Power Transistor Type 2N4910 (Note 1)

NOTES

1. Normally voltage regulator/servo power assembly is replaced as a module. These parts are listed for reference purposes.

*Indicates replaceable part. For part number, see Table 4-4.

Table 4-4
Replaceable/Spare Parts

Item	Part No.	Description	Qty Spare	Note
1-1	198-4439-001	Control Panel Assembly	1	1
1-7	198-2771-xxx	Dust Cover Assembly		1
1-11	198-2605-001	Capstan Wheel	1	
1-12	198-1509-001	Tape Guide Assembly	2	
1-14	198-2399-010	Head Assembly, Nine-Track	1	2
1-14	198-2399-003	Head Assembly, Seven-Track	1	2
1-15	198-1138-001	Photosensor Assembly, Load Point/EOT	1	
1-16	198-1139-001	Photosensor Assembly, Broken Tape	1	
1-17	198-2747-001	Tape Cleaner Assembly	1	
1-18	198-2647-002	Roller Guide Assembly	1	
1-20	198-0013-001	Magpot Tension Sensor Assembly (includes Magpot Circuit Module)	1	
1-22	198-0017-002	Spring, Tension (package of 2)	1	
1-23	198-2827-001	Tension Arm Assembly		
1-24	198-4438-001	Reel Motor Assembly	1	
1-25/ 1-26	198-0101-001	Belt Kit (1 each supply/takeup)		
1-27	198-2641-001	File Protect Switch Assembly		
1-30	198-2484-001	Capstan Motor Assembly	1	3
1-31	198-3631-xxx	Read Preamplifier Printed Circuit Board Assembly	1	3
2-2	198-4474-601	Transformer Assembly		

NOTES

1. Unless specified, control panels and dust covers will be shipped with standard paint colors. If special paint or logo is required, please specify.

2. Head is supplied on mounting plate and with face shield and connector. Specify number of tracks. All heads are read after write with side mounted erase. Deskew chart is furnished with each head.

3. Capstan motor/tachometer assembly is supplied with capstan wheel in case of damage to capstan in removal.

4. Assembly varies with speed of machine. Please specify when ordering.

5. Delay timing module version varies with machine specifications. Consult card identification strip or schematic section for module type required.

6. Heat sink assembly includes regulation module 190-4352-001. This module is not readily replaceable without replacing heat sink.

7. Repair kit contains those items subject to wear.

Table 4-4 (Cont)
Replaceable/Spare Parts

Item	Part No.	Description	Qty Spare	Note
2-3	198-3625-199	Capacitor, Electrolytic, 18,000 mF, 25 V min		
2-4	198-3610-449	Capacitor, Electrolytic, 39,000 mF, 10 V min		
2-6	198-0108-001	Rectifier, MR751, Motorola (package of 6)		
2-7	198-4306-xxx	Servo Preamplifier Module	1	4
2-8	198-3844-001	Sensor Amplifier/Driver Module	1	
2-9	198-3194-xxx	Ramp Generator Module	1	4
2-10	198-3843-001	Pushbutton Control Module	1	
2-11	198-3842-001	Control Interface Module	1	
2-13	198-3845-xxx	Delay Timing Module (9-track, 800 characters/in. standard)	1	4,5
	198-4118-xxx	Delay Timing Module (7-track)	1	4, 5
	198-4845-xxx	Delay Timing Module (9-track, special)	1	4, 5
2-14	198-4179-xxx	Read Amplifier/Clipping Level Module	1	4
2-15	198-4178-xxx	Quad Read Amplifier Module	1	4
2-17	198-3848-001	Four-Channel Write Amplifier Module	1	
2-18	198-3849-001	Five-Channel Write Amplifier Module	1	
3-1	198-4441-001	Voltage Regulator/Servo Power Assembly	1	6
3-4	198-0802-001	Fuse Holder		
	198-0133-030	Fuse 3AG, 3 A (115 V) (box of 5)	1	
	198-0133-015	Fuse 3AG, 1.5 A (230 V) (box of 5)	1	
3-5	198-5001-103	Switch, 115/220 V		
3-6	198-0068-001	Power Cord		
	198-0100-001	Hub Repair Kit	1	7
	198-0102-001	Brush Replacement Kit, Reel Motor (4 brushes)	1	
	198-0103-001	Brush Replacement Kit, Capstan Motor (2 brushes)	1	

APPENDIX A
TRANSPORT SIGNAL DESCRIPTIONS AND INTERFACE INFORMATION

A.1 INPUT SIGNALS

All commands from and to the input/output connector are preconditioned by loading the machine and placing it on-line using the front panel controls. The next commands set up the recorder.

A.1.1 Setup Commands

Signal	Pin No.	Description
Transport Select (SLT)	P1-J	A level that when true enables all the adapter drivers and receivers in the transport, thus connecting the transport to the controller. The transport must also be on-line, and SLT must be true for the entire write sequence (until tape motion stops). The SLT level may be removed to disconnect the machine from the system. The machine will remain in the last condition established by SWS.
Data Density Select (DDS) (Dual Density Only)	P1-D	Used when the TRANSPORT DENSITY SELECT switch is in the remote position. When true, this level selects the high read density (dual density).

A.1.2 Tape Motion Commands

Signal	Pin No.	Description
Overwrite (OVW) (Optional)	P1-B	A level that when true conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the write mode of operation to utilize the OVW feature.
Synchronous Forward Command (SFC)	P1-C	A level that when true, with the transport ready and on-line, causes tape to move forward at the specified speed. When the level goes false, tape motion ramps down and ceases.
Synchronous Reverse Command (SRC)	P1-E	A level that when true, with the transport ready and on-line, causes tape to move in a reverse direction at the specified speed. When the level goes false, tape motion ceases. If the load point marker is detected during an SRC, the SRC will be terminated. If an SRC is given when the tape is at the load point, it will be ignored.

Signal	Pin No.	Description
Rewind Command (RWC)	P1-H	A pulse input will rewind the tape past the load point and stop. The transport will then initiate a load forward sequence and return the tape to the load point marker. This input will be accepted only if the load point output is false. The transport may be taken off-line while rewind is still in process. Rewind will continue normally.

A.1.3 Write Commands

Signal	Pin No.	Description
Set Write Status (SWS)	P1-K	A level that must be true at the leading edge of an SFC (or RUN and FWD) when the write mode of operation is required, and must remain true for a minimum of 10 μs after the leading edge of the SFC (or RUN and FWD). SWS is sampled at the leading edge of the SFC or SRC (or RUN and FWD), toggling the read/write flip-flop to the appropriate state. Internal interlocks in the 9800/9700 will prevent writing in the reverse direction, when the write enable ring is missing, when the tape unit is off-line, when loading to a load point, and during a rewind.
Write Data Inputs		These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Data inputs must have settled 0.5 μs before the leading edge of the WDS pulse and must remain quiescent 0.5 μs beyond the trailing edge of the WDS pulse. The CRCC is written by providing the correct data character together with a WDS four character times after the last data character of the record.
WDP	P2-L	
WD0	P2-M	
WD1	P2-N	
WD2	P2-P	
WD3	P2-R	
WD4	P2-S	
WD5	P2-T	
WD6	P2-U	The LRCC is written using the WARS signal. The LRCC can also be written by providing the correct data character together with a WDS. If the LRCC is written (DATA-WDS) in this manner, a WARS should be given one character time after the LRCC to ensure proper IRG erasure in case of data input error.
WD7	P2-V	
Write Data Strobe (WDS)	P2-A	A pulse of 2 μs nominal width for each character to be written. Writing occurs on the leading edge of the WDS. WDS may be a 1 μs minimum, 3 μs maximum pulse. Data inputs must have settled for at least 0.5 μs before the leading edge of WDS and remain quiescent for at least 0.5 μs beyond the trailing edge.
Write Amplifier Reset (WARS)	P2-C	A pulse of 2 μs nominal width that, when true, resets the write amplifier circuits on the leading edge. The purpose of this line is to enable writing of the longitudinal redundancy check character (LRCC) at the end of a record. This ensures that all tracks are properly erased in an interrecord gap (IRG). In a nine-track system, the leading edge of the WARS pulse should be eight character times after the leading edge of the WDS associated with the last data character in the block (four character times after the CRCC is written).

A.1.4 Read Commands

A read-after-write machine will always have read selected. When write is selected (SWS), the data just written will be read back using a high threshold level on the read amplifiers. When SWS is false, the normal threshold is applied to the read amplifiers.

Signal	Pin No.	Description
Automatic Clipping Level Disable (ACLD)	P3-6	When true, this level overrides the automatic clipping level electronics and holds the read electronics in the normal clipping level.

A.1.5 Shutdown Commands

The use of a given magnetic tape unit may be terminated by an off-line command. Once this command is given, the tape unit may be returned to an adapter command only by operating the front panel ON LINE switch.

Signal	Pin No.	Description
Off-Line Command (OFFC)	P1-L	A level or pulse (minimum width 2 μs) that resets the on-line flip-flop to the zero state, placing the transport under manual control. It is gated only by SELECT in the transport logic, allowing an OFFC to be given while a rewind is in progress. An OFFC should be separated from a rewind command by at least 2 μs.

A.2 INTERFACE OUTPUT SIGNALS

All output signals are enabled only when the tape transport is on-line and selected.

A.2.1 Status Outputs

Signal	Pin No.	Description
On-Line (ONL)	P1-M	A level that is true when the on-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.
Transport Ready (RDY)	P1-T	A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.
High Density Indicator (HDI) (Dual Density Only)	P1-F	A level that is true only when the high-density mode of operation is selected.
File Protect (FPT)	P1-P	A level that is true when a reel of tape without a write enable ring is mounted on the transport supply (or file) hub.
Write Enable (WEN)	P1-S	A level that is true when a reel of tape with a write enable ring is mounted on the transport supply (or file) hub. Opposite of file protect.

Signal	Pin No.	Description
Load Point (LDP)	P1-R	A level that is true when the load point marker is under the photosensor and the transport is not rewinding. After receipt of an SFC, the signal will remain true until the load point marker leaves the photosense area. (Circuitry using this output should not use the transitions to and from the true state.)
Tape Running (RNG)	P1-V	This is a level that is true when tape is being moved under capstan control and remains true until tape motion has ceased. (Includes forward, reverse, and rewind tape motion.)
End-of-Tape (EOT)	P1-U	A level that is true for the duration of the EOT marker. (Circuitry using this output should not use the transitions to and from the true state.)
Rewinding (RWD)	P1-N	A level that is true only when the transport is engaged in a rewind operation or returning to the load point. (Goes true approximately 5 μs after a rewind command is given.)

A.2.2 Read Outputs

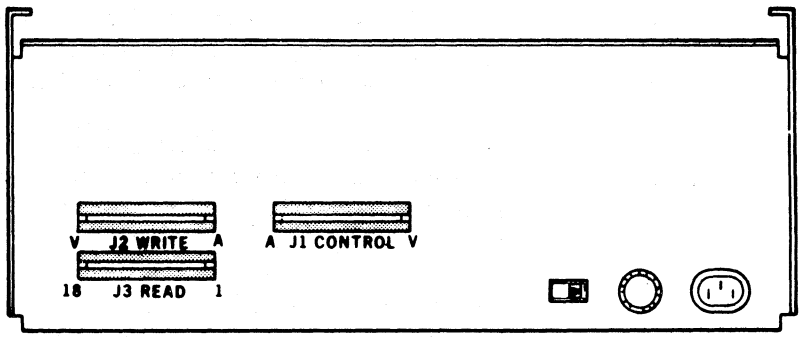
Read outputs are present at all times in tape units when a dual gap head is used (read after write). The high threshold level is selected internally when SWS is selected. In a read/write tape unit (single-gap head), read outputs are inhibited when SWS is true.

Signal	Pin No.	Description
Read Data Strobe (RDS)	P3-B	A pulse of 2 μs minimum width for each data character read from tape. Although the average time between two read data strobes is τ_1 (sec) = [1/s•d)] where s = tape speed in inches per second d = density characters per inch the minimum time between consecutive read data strobes is less than this figure due to skew and bit crowding effects. A guaranteed safe value for the minimum time is $1/2\ \tau_1$.
Read Gap Detect (RGAP)	P3-N	A level that is true approximately nine character spacings after the last data byte, and remains true until the first data byte of the subsequent data block. **NOTE** **This level will be true whenever tape motion is at rest.**

Signal	Pin No.	Description
Read Data Level		Nine staticisers are provided, which act as a one-stage read deskewing buffer. Each output is a level that changes to the appropriate state approximately 1 μs before the read data strobe and remains in that state until 1 μs before the next read data strobe. Data lines return to false condition in the IRG when tape motion stops, regardless of the last character read.
RDP	P3-1	
RD0	P3-3	
RD1	P3-4	
RD2	P3-8	
RD3	P3-9	
RD4	P3-1	
RD5	P3-1	It is recommended that read data strobes and the read gap detect be ignored during the first read or write operation from load point for τ_2 ms after the load point output goes false, where τ_2 = 1000/s (s = speed of tape unit).
RD6	P3-1	
RD7	P3-1	The read gap in a read-after-write tape unit is downstream from the write gap. Thus when the write gap is initially energized, the read gap may detect a flux change depending on the initial state of magnetism on the tape.

A.3 SUMMARY OF INTERFACE CHARACTERISTICS

Figure A-1 shows the location of connectors and pin numbers with signal names.



11-3059

→ INPUT
← OUTPUT

WRITE CONNECTOR J2

Active	Ground		Signal	Mnemonic
A	1	←	Write Data Strobe	WDS
B	2		N. C.	
C	3	←	Write Amplifier Reset	WARS
D	4		Not Used	
E	5		Not Used	
F	6		Not Used	
H	7		Not Used	
J	8		Not Used	
K	9		Not Used	
L	10	←	Write Data Channel P	WDP
M	11	←	Write Data Channel 0	WD0
N	12	←	Write Data Channel 1	WD1
P	13	←	Write Data Channel 2	WD2
R	14	←	Write Data Channel 3	WD3
S	15	←	Write Data Channel 4	WD4
T	16	←	Write Data Channel 5	WD5
U	17	←	Write Data Channel 6	WD6
V	18	←	Write Data Channel 7	WD7

CONTROL CONNECTOR J1

A	1		Spare	
B	2	←	Overwrite	OVW
C	3	←	Synchronous Forward	SFC
D	4	←	Data Density Select	DDS
E	5	←	Synchronous Reverse	SRC
F	6	→	Data Density Indicator	DDI
H	7	←	Rewind Command	RWC
J	8	←	Select	SLT
K	9	←	Set Write Status	SWS

CONTROL CONNECTOR J1 (Cont)

Active	Ground		Signal	Mnemonic
L	10	←	Off-Line Command	OFFC
M	11	→	On-Line Command	ONL
N	12	→	Rewinding	RWD
P	13	→	File Protect	FPT
R	14	→	Load Point	LDP
S	15	→	Write Enable	WEN
T	16	→	Transport Ready	RDY
U	17	→	End-of-Tape	EOT
V	18	→	Tape Running	RNG

READ CONNECTOR J3

1	A	→	Read Data Channel P	RDP
2	B	→	Read Data Strobe	RDS
3	C	→	Read Data Channel 0	RD0
4	D	→	Read Data Channel 1	RD1
5	E		Not Used	
6	F	→	Auto Disable	
7	H		Not Used	
8	J	→	Read Data Channel 2	RD2
9	K	→	Read Data Channel 3	RD3
10	L		Not Used	
11	M		Not Used	
12	N	→	Gap Detect	
13	P		Not Used	
14	R	→	Read Data Channel 4	RD4
15	S	→	Read Data Channel 5	RD5
16	T		Not Used	
17	U	→	Read Data Channel 6	RD6
18	V	→	Read Data Channel 7	RD7

Figure A-1 Summary of Adapter Characteristics

APPENDIX B
DEC/VENDOR TS03 TRANSPORT PART NUMBERS

Vendor Number	DEC Number	Description
154-0035-001	29-21904	Tape Path Alignment Tool
190-1509-001	29-21905	Tape Guide
190-2399-010	29-21906	Head Assembly
190-2641-001	29-21907	File Protect Assembly
190-2747-001	29-21908	Tape Cleaner Assembly
190-3631-005	29-21909	Read Preamplifier Module
190-3645-002	29-21910	Ramp Generator Module
190-3842-001	29-21911	Interface Control Module
190-3843-001	29-21912	Tape Motion Control
190-3844-001	29-21913	Sense Amplifier/Driver Module
190-3848-001	29-21914	Write Amplifier (4-Channel) Module
190-3849-001	29-21915	Write Amplifier (5-Channel) Module
190-4178-004	29-21916	Quad Read Amplifier Module
190-4179-004	29-21917	Read Amplifier/Clip Control Module
190-4220-001	29-21918	Mag Pot PLB
190-4306-001	29-21919	Servo Preamplifier Module
190-4352-001	29-21920	Voltage Regulator PCB.
190-4845-001	29-21921	Timing Delay Module
192-9900-001	29-21922	Test Panel
190-4448-001	29-21923	LED Display
190-4441-001	29-21924	Voltage Regulator/Servo Power Amplifier
190-3468-001	29-21925	Module Extender
190-2647-002	29-21926	Tension Roller
190-2484-001	29-21927	Capstan Motor
128-0091-001	29-21928	Spring
125-0030-006	29-21929	O-Ring
190-4218-001	29-21930	Mag Pot
190-4438-001	29-21931	Reel Motor
151-0057-001	29-21932	Switch
190-1139-001	29-21933	Broken Tape Sensor
190-1138-001	29-21934	Tape Photo Sensor
151-0038-001	29-21935	Switch
125-0006-001	29-21936	Reel Drive Belt (Supply)
125-0015-001	29-21937	Reel Drive Belt (Take-Up)
125-0008-103	29-21938	Bearing
125-0040-001	29-21939	Bearing
154-0001-001	29-21940	Capstan Puller

Vendor Number	DEC Number	Description
190-4474-601	29-21941	Transformer
148-0114-001	29-21942	LED Fairchild FLV-102
148-0108-001	29-21943	Diode MR751
148-0122-001	29-21944	Power Transistor MJ802
151-0802-002	29-21945	Fuse Holder
115-3625-199	29-21946	Capacitor (18K MFD or larger)
115-3610-449	29-21947	Capacitor (40K MFD or larger)
198-0100-001	29-21964	Hub Repair Kit
148-0121-001	29-10334	Power Transistor MJ4502
148-0075-001	29-19037	Transistor 2N4910
148-0053-001	15-10008	Transistor 2N3055A
148-0102-003	15-10712	Transistor MJ-900
148-0102-004	15-10853	Transistor MJ-1000
198-0133-030	90-07217	Fuse 3 A–3 AG (115 V)
198-0133-015	90-08388	Fuse 1.5 A–3 AG (230 V)

Reader's Comments

TMA11-M DECMAGTAPE SYSTEM
MAINTENANCE MANUAL
EK-TMA11-MM-PRE

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