EK-RQDX1-UG-001

RQDX1 Controller Module User's Guide

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RQDX1 Controller Module User's Guide

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CONTENTS

CONTENTS (Cont)

FIGURES

TABLES

PREFACE

This user's guide provides information on the configuration, installation, and operation of the RQDX1 disk drive controller module, the associated disks (the RD51 Winchester fixed disk drive and the RX50 diskette drive), and the RQDX1-E extender module option.

Chapter 1 provides environmental and functional specifications for the RQDX1 controller module, the RD51 fixed disk drive, the RX50 diskette drive, and the RQDX1-E extender module option.

Chapter 2 gives a functional description of the RQDX1 controller module.

Chapter 3 presents configuration and installation information for the RQDX1 controller module and the RQDX1-E extender module option.

Chapter 4 describes the programmable registers that are LSI-11 bus addressable on the RQDX1 controller module. Mass storage control protocol (MSCP) and diagnostics and utilities protocol (DUP) are also briefly described.

Chapter 5 provides testing and error detection information.

Chapter 6 presents installation and operation information for the RD51 fixed disk drive and the RX50 diskette drive.

RELATED DOCUMENTATION

The following documents provide additional information and may be of interest to RQDX1 controller module users.

Document Title	Document Number
RQDX1 Field Maintenance Print Set	MP-01731-01
UDA50 Programmer's Documentation Kit	QP-905-GZ

In addition, users may refer to documentation for the specific system in which the RQDX1 controller module is installed.

CHAPTER 1
INTRODUCTION

1.1 DESCRIPTION

The RQDX1 disk drive controller module interfaces the RD51 disk and/or RX50 diskette drives to any quad- or hex-size backplane that uses a 16-, 18-, or 22-bit LSI-11 bus. The backplane must be in a mounting box (such as a BA23) that provides a control panel and a signal distribution panel. A single RQDX1 module controls any one of the configurations listed in Table 1-1.

Table 1-1 RQDX1 Controller Module Configurations

Configuration	Physical Disk Drives	Logical Disk Drive Numbers
1	One RD51, one RX50	Unit 0 = RD51 Unit 1, 2 = RX50
2	Two RX50s	Unit 0, 1 = RX50 Unit 2, 3 = RX50
3*	Two RD51s One RX50	Unit 0 = RD51 Unit 1 = RD51 Unit 2, 3 = RX50
4*	Two RD51s	Unit 0 = RD51 Unit 1 = RD51
5	One RX50	Unit 0, 1 = RX50
6	One RD51	Unit 0 = RD51

* These configurations require the use of the optional RQDX1-E extender module. Refer to Paragraph 3.7 for additional RQDX1-E information.

The RD51 disk drive is a random access storage device, which uses two nonremovable 133.4 mm (5.25 inch) disks as storage media. The RD51 disk drive has a total formatted storage capacity of 11 megabytes.

The RX50 diskette drive is a random access storage device, which uses two single-sided 133.4 mm (5.25 inch) RX50K diskettes. The total storage capacity of the RX50 diskette drive is 800 kilobytes of formatted data.

The RQDX1-E extender module option provides cable connection to a single disk or diskette that is mounted externally from the MICRO/PDP-11 (BA23) mounting box.

1.2 FEATURES

The RQDX1 controller module has the following features.

- Single quad-size module.
- Supports DMA data transfers in 16-, 18-, or 22-bit addressing modes.
- Supports block mode transfers with MSV11-P memories.
- Supports 22-bit addressing on an LSI-11 bus.
- Memory parity error abort feature for use with memories that have a parity option.
- Requires no jumper/switch reconfiguration when adding or removing RD51 or RX50 drives.

1.3 SPECIFICATIONS

1.3.1 RQDX1 Disk Controller Module

Module	1 quad-size module, M8639
Size	Height: 26.56 cm (10.46 in) Width: 1.27 cm (0.5 in) Length: 22.70 cm (8.94 in)
Power Requirements	+5 Vdc ±5% at 6.4 A (typical) 8.0 A (maximum) +12 Vdc ±5% at 7.3 mA (typical) 10 mA (maximum)
Bus Loads	
AC Bus Loads	2.5
DC Bus Loads	1
Addressing Modes	16-, 18-, and 22-bit (determined by user)
Limitations	The RQDX1 will not fit in the dual-height LSI-11 mini-series H9281 backplane.
Drives Per Controller	Up to four logical units, no more than two RD51 disk drives
LSI-11 Bus-Addressable Registers	2

Base Device Address (Standard)

Addressing Mode	Address (Octal)
16-bit	172150
18-bit	772150
22-bit	17772150

Vector	Software selectable (Normally set at 154)
Data Transfer Rate	800 ns/word (peak) controller to host
Environmental Specifications	
Temperature	
Storage Operating	−40°C to 66°C (−40°F to 150°F) 5°C to 50°C (41°F to 122°F)
Relative Humidity	
Storage Operating	10% to 95%, noncondensing 10% to 95%, noncondensing
Altitude	
Storage Operating	9.1 km (30,000 ft) maximum 2.4 km (8,000 ft) maximum
Airflow	
Operating up to 50°C	Maximum temperature rise across module must not exceed 20°C (68°F) input to output.

1.3.2 RD51 Disk Drive

Storage Type	
Medium	Winchester fixed disk
Recording Surfaces	4 data surfaces
Magnetic Heads	4 read/write heads
Recording Method	Modified frequency modulation (MFM)
Performance Specifications	
Recording Capacity (Formatted)	
Bytes Per Sector	512 bytes
Sectors Per Track	18 sectors (track size) Each sector has a logical block number (LBN)
Tracks Per Group	4 tracks (group size)

Groups Per Cylinder	3 groups (cylinder size)
Cylinders Per Unit	100 cylinders
Total Cylinders Per Unit	102 cylinders*
Total Bytes Per Unit	11.059 M bytes
Transfer Rate	5,000,000 bits/s (625 K bytes/s)
Access Time (Buffered Seek, Including Settling)	
Average	85 ms
Maximum	205 ms
Average Latency	8.33 ms
Functional Specifications	
Rotational Speed	3,600 r/min (±1%)
Recording Density	9,074 bits/in (maximum)
Track Density	345 tracks/in
Environmental Specifications	
Ambient Temperature	10°C to 50°C (50°F to 122°F)
Relative Humidity	20% to 80% noncondensing
Maximum Wet Bulb	25.6°C (78°F)

1.3.3 RX50 Diskette Drive

Storage Type	
Medium	Diskette
Recording Surfaces	2 data surfaces
Magnetic Heads	2 read/write heads
Recording Method	Modified frequency modulation (MFM)

* Cylinders 100 and 101 are assigned as follows.

Cylinder 100, Group 0:	Replacement and caching table (RCT) Format control table (FCT)
Cylinder 100, Groups 1, 2:	Replacement block numbers (RBNs)
Cylinder 101, Groups 0, 1:	Diagnostic block numbers (DBNs)
Cylinder 101, Group 2:	Reserved

Performance Specifications

Recording Capacity (Formatted)

Bytes Per Sector	512 bytes
Sectors Per Track	10 sectors (track size) Each sector has a logical block number (LBN).
Tracks Per Group	5 tracks (group size)
Groups Per Cylinder	16 groups (cylinder size)
Cylinders Per Surface	1 cylinder
Bytes Per Surface	404,480 bytes
Surfaces Per Unit	2 surfaces (2 diskettes)
Bytes Per Unit	808,960 bytes
Transfer Rate	250,000 bits/s (31.25 K bytes/s)

Access Time	Minimum	Typical	Maximum
Track to Track	6 ms	–	–
Head Settling Time	–	–	30 ms
Head Load Time	–	–	30 ms
Rotational Latency	–	100 ms	200 ms
Random Access	–	264 ms	–
Drive Motor Start	–	–	250 ms

Functional Specifications

Rotational Speed	300 r/min (±1.5%)
Recording Density	5,576 bits/in (maximum)
Track Density	96 tracks/in

Environmental Specifications

Ambient Temperature	15°C to 32°C (59°F to 90°F)
Relative Humidity	20% to 80% noncondensing
Maximum Wet Bulb	25°C (78°F)

1.3.4 RQDX1-E Extender Module Option

Module	1 dual-size module, M7512
Size	Height: 13.2 cm (5.2 in) Width: 1.27 cm (0.5 in) Length: 22.8 cm (8.9 in)
Power Requirements	+5 Vdc at 0.5 A (typical) 0.6 A (maximum)
Bus Loads	
AC Bus Loads	0
DC Bus Loads	0
Limitations	Provides signal distribution to a single disk or diskette drive Cannot be used on the PDP-11/23 Plus
Environmental Specifications	
Temperature	
Storage	−40°C to 66°C (−40°F to 150°F)
Operating	5°C to 60°C (41°F to 140°F)
Relative Humidity	
Storage	10% to 95%, noncondensing
Operating	10% to 95%, noncondensing
Altitude	
Storage	9.1 km (30,000 ft) maximum
Operating	2.4 km (8,000 ft) maximum
Airflow	
Operating up to 50°C	Maximum temperature rise across module must not exceed 20°C (68°F) input to output.

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The RQDX1 controller module interfaces the RD51 disk drive and/or RX50 diskette drives to a 16-, 18-, or 22-bit LSI-11 bus. One RQDX1 controller module can support up to four logical units in any combination of RD51 and RX50 drives (up to two RD51 drives per RQDX1 controller module). The RQDX1 controller module (M8639) has the LSI-11 bus transceivers and decoders, programmable registers, controller timing and sequence logic, and the data formatting circuits necessary to read and write on the RD51 disk media and/or the RX50 diskette media.

2.2 BLOCK DIAGRAM DESCRIPTION

The main functional subsections of the RQDX1 module are shown on the block diagram in Figure 2-1. The block diagram illustrates the basic architecture and the data path relationships of the major subsections. The RQDX1 controller module is a bus-oriented system controlled by a system control function shared by the T-11 chip and the main high-speed controller.

The major subsections of the RQDX1 are as follows.

- Shuffle step oscillator
- Phase locked loop
- Data recovery
- Sync mark detector
- Serializer/deserializer
- MFM encoder/precomp generator
- Interrupt vector register
- SA read/write registers, IP register
- QBus transceivers and handshake controller
- RQDX1 control logic: T-11 chip and main high-speed controller
- Memory address counter/register
- 2 K × 16 RAM
- Disk drive control register and status buffer
- T-11 RAM address pointer and arithmetic logic unit (ALU)
- Bidirectional byte multiplexer
- 8 K × 16 PROM
- QBus DMA pointer and ALU

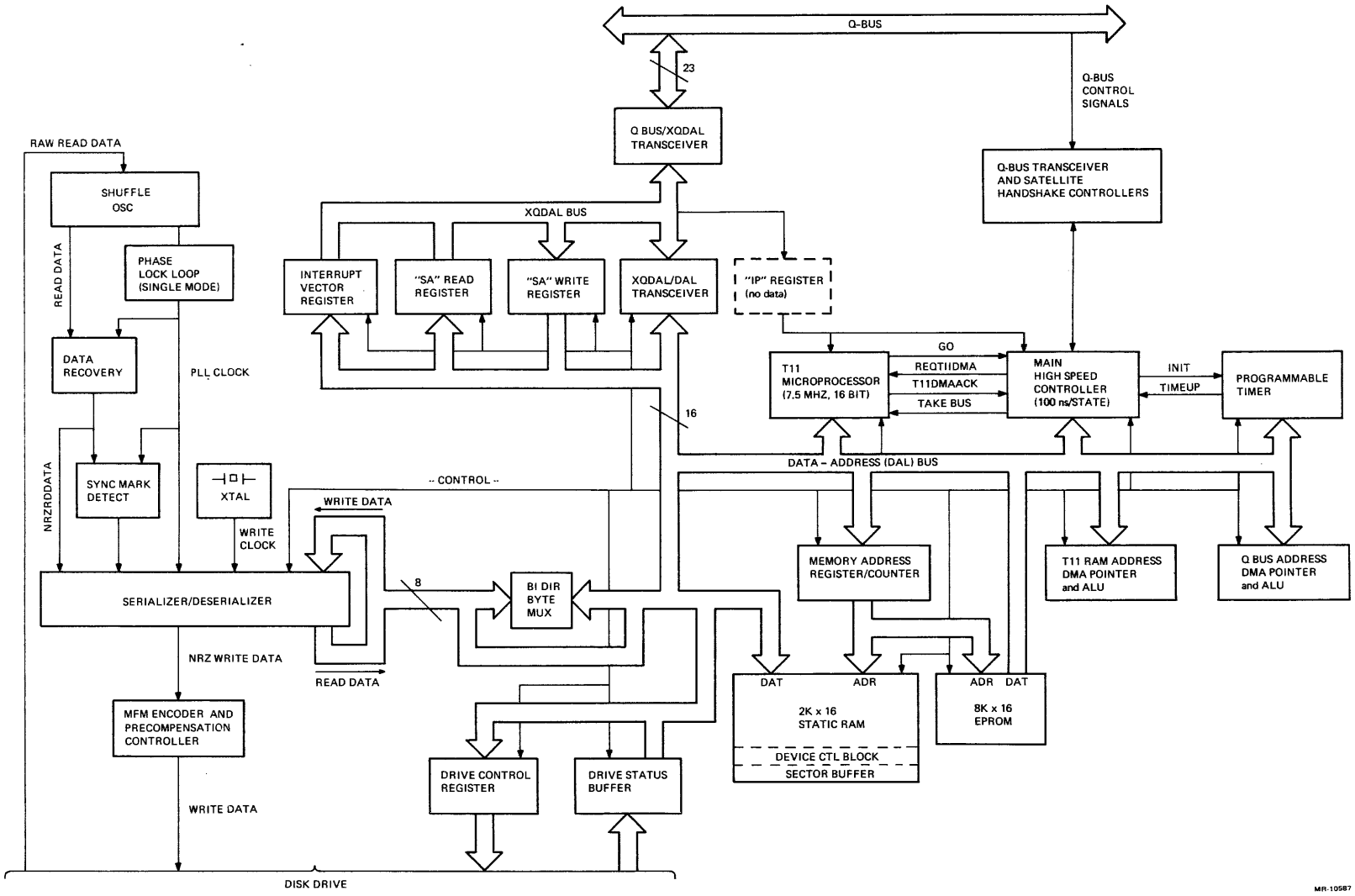


Figure 2-1 RQDX1 Controller Module Functional Block Diagram

2.3 SHUFFLE STEP OSCILLATOR

The shuffle step oscillator (Figure 2-2) is a system of two matched 10 MHz oscillators, a small asynchronous oscillator controller, and a read data delay equalizer. When one of the oscillators is generating a raw read clock signal for the phase locked loop (PLL), the other oscillator is in stand-by. At each raw read data pulse, the active oscillator is commanded to turn off and the stand-by oscillator is commanded to become active. This causes the oscillators to "shuffle" to keep in step with the RAW read data. The read data delay equalizer section delays the RAW read data to compensate for the short amount of time that it takes to shuffle the oscillators.

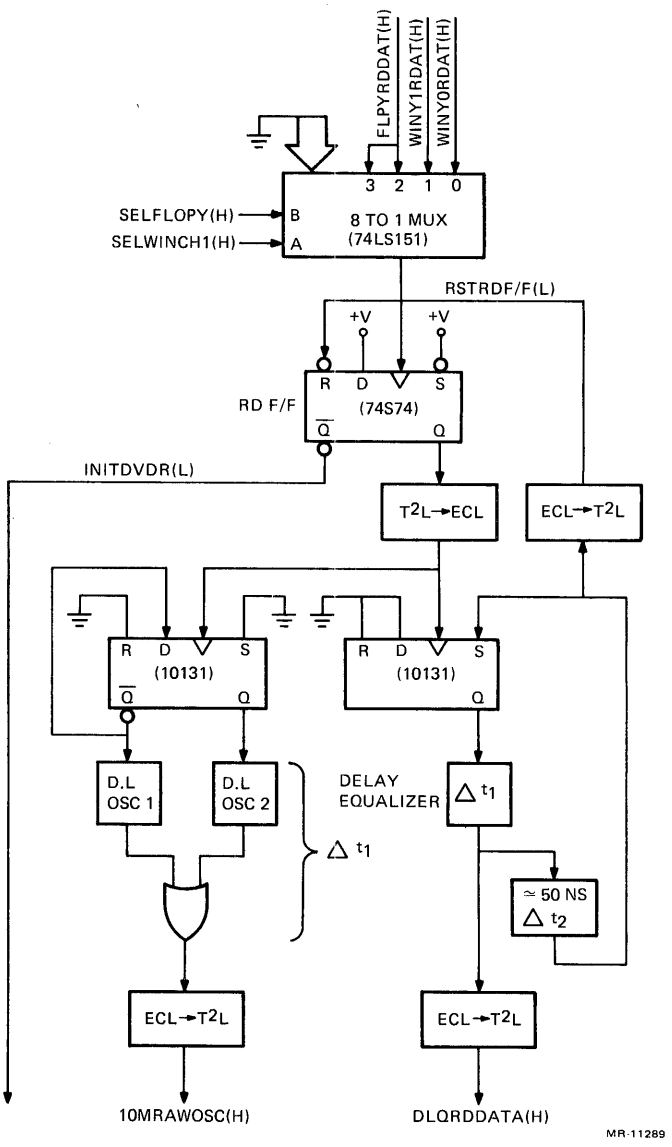


Figure 2-2 Shuffle Step Oscillator

2.4 PHASE LOCKED LOOP

The phase locked loop (PLL) logic is shown in Figure 2-3. The PLL is a dual-channel, single-mode system. Dual channel provides one channel for the RX50 diskette drive(s) and one channel for the RD51 disk drive(s). The function of the PLL logic is to provide the "flywheel" effect for the shuffle step oscillator output, thus integrating the effects of the "pulse drift" in the RAW read data. The output of the PLL is fed into a counter which generates two data recovery window signals. These "windows" are generated in a way to center the read data pulses. (At any given time the data will be framed by one of these windows.) The proper data framing window is selected automatically by the sync mark detector.

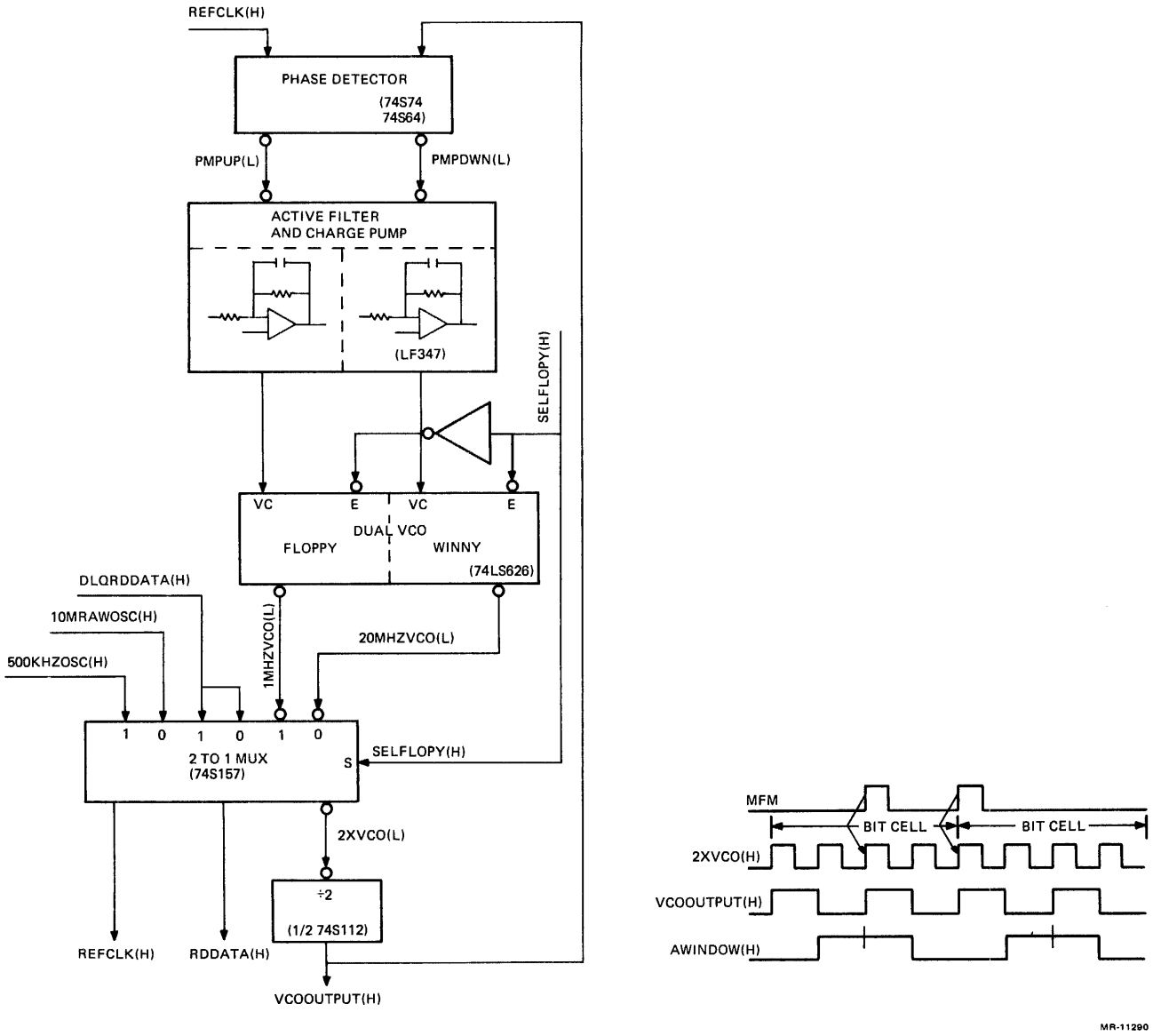


Figure 2-3 Phase Locked Loop Logic

2.5 DATA RECOVERY

The data recovery logic (Figure 2-4) consists of two single-bit, edge-triggered, double-buffered registers. The registers are cross-coupled in order to capture the read data occurring anywhere within either data framing window. Together with the phase locked loop output, an NRZ read data stream is produced.

2.6 SYNC MARK DETECTOR

The sync mark detector logic (Figure 2-4) provides two functions. One, it detects the sync mark, and, two, it selects the proper stream from the data recovery logic. Both data recovery bit streams are analyzed to find the sync mark. Upon detection of the sync mark in either stream, the serializer/deserializer logic receives the desired data stream.

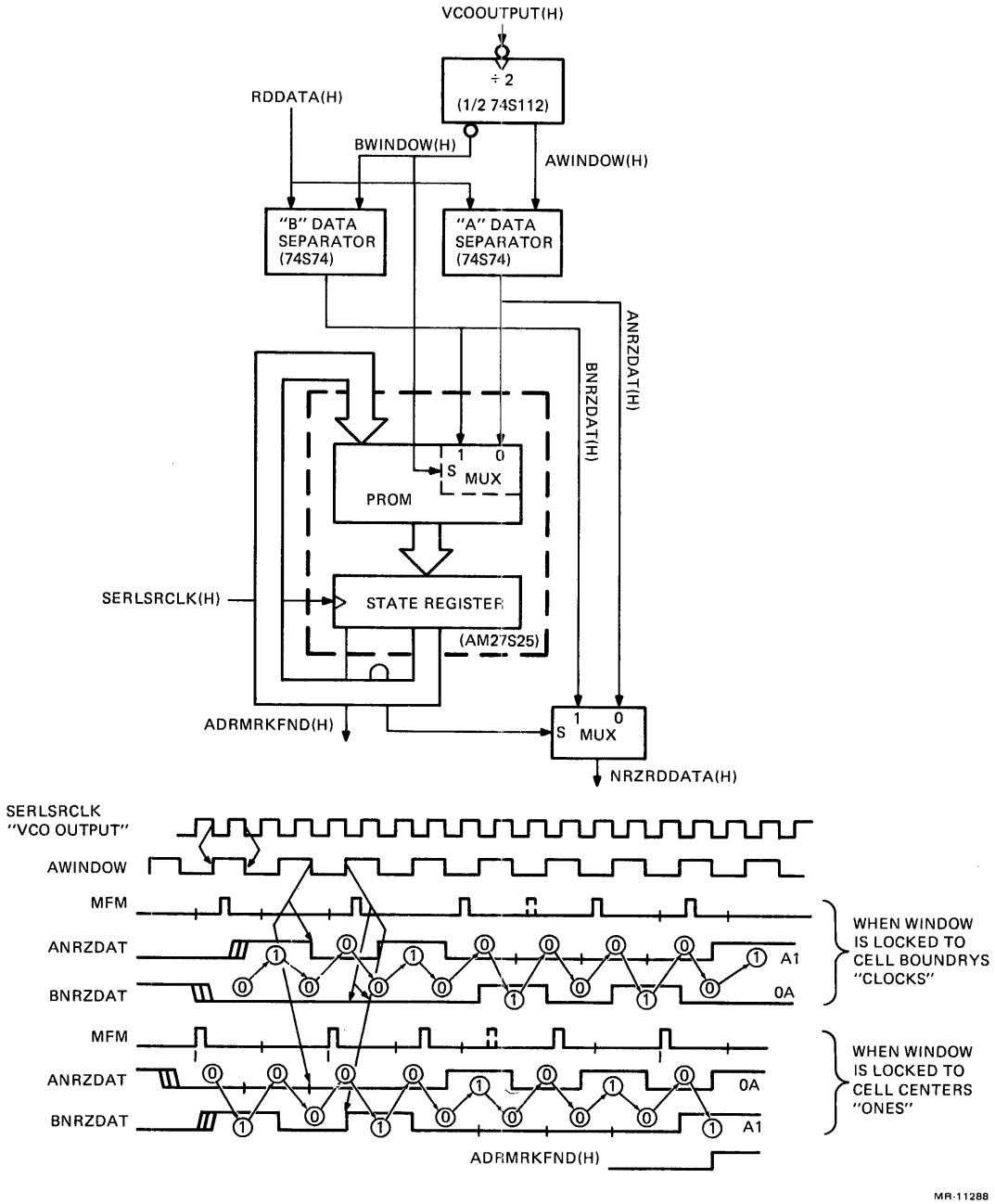


Figure 2-4 Data Recovery and Sync Mark Detector Logic

2.7 SERIALIZER/DESERIALIZER

The serializer/deserializer is shown in Figure 2-5 and consists of the following four parts.

- A double-buffered serial in/parallel out register
- A double-buffered parallel in/serial out register
- A CRC generator/checker
- A high-speed finite state machine controller

The serial in/parallel out (SIPO) logic shifts the serial read data through the CRC generator and forms an 8-bit parallel byte. The byte is buffered for data transfer.

The parallel in/serial out (PISO) logic receives the parallel write data, buffers it, and shifts this data serially through the CRC generator to the MFM encoder and precomp generator. This serial data becomes the write data to be sent to the disk.

Both the SIPO and the PISO logic are controlled by the high-speed machine controller.

2.8 MFM ENCODER/PRECOMP GENERATOR

The MFM encoder/precomp generator logic (Figure 2-5) receives the serial data to be written to the disk and performs the following operations.

1. It generates a modified frequency modulation (MFM) data bit stream.

2. It precompensates the MFM bit stream (for both the RD51 disk drive and the RX50 diskette drive).

3. It generates the sync mark bit sequence on command.

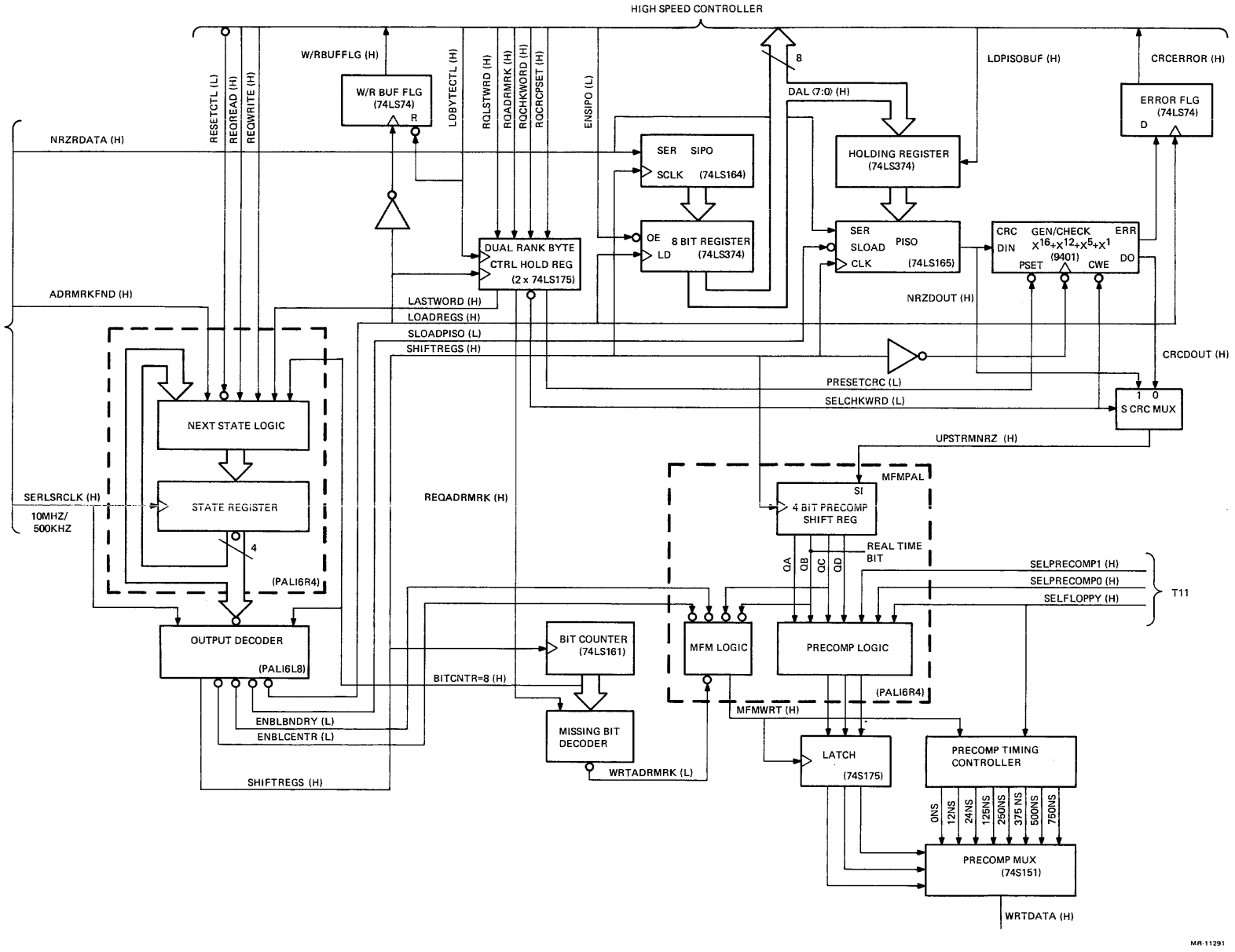


Figure 2-5 Serializer/Deserializer and MFM Encoder/Precomp Generator Logic

2.9 INTERRUPT VECTOR REGISTER

During an interrupt sequence, the contents of the interrupt vector register (Figure 2-6) are gated to the QBus to be used as the vector. The MSCP initialization function supplies the T-11 chip on the RQDX1 controller module with the vector number. The T-11 chip loads this number into the interrupt vector register.

2.10 SA READ REGISTER, SA WRITE REGISTER, IP REGISTER

The status and address registers (SA) shown in Figure 2-6 are used by the T-11 chip and the QBus processor for the MSCP port initialization sequence. Both SA registers occupy the same QBus I/O page address.

The SA read register is written into by the T-11 chip and read from by the host QBus processor. This register is used to pass initialization status to the QBus processor.

The SA write register is written into by the QBus processor and read from by the T-11 chip. This register is used during the initial sequence to pass the MSCP command buffer address and interrupt vector to the T-11 chip.

The IP register is used to begin the initialization sequence when this register is written into by the QBus processor. When the host QBus processor reads from the IP register, the RQDX1 controller module initiates a polling routine.

2.11 QBUS TRANSCEIVERS AND HANDSHAKE CONTROLLERS

The RQDX1 controller module interfaces to the QBus through QBus drivers, QBus receivers, and control circuits. The control circuits, shown in Figure 2-6, provide the handshake signals necessary to interrupt the QBus, obtain control of the QBus for DMA, and interface the programmed SA and IP registers to the QBus.

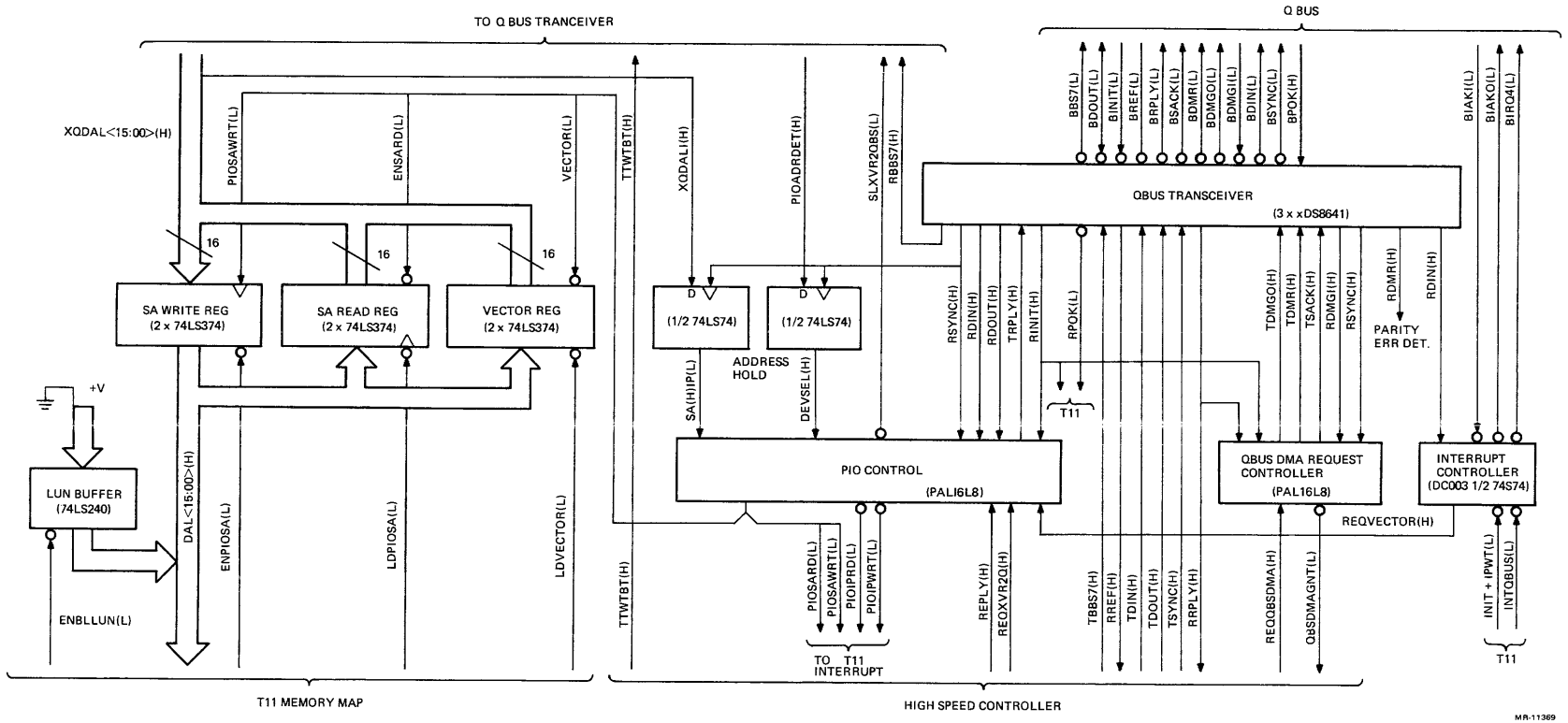


Figure 2-6 Interrupt Vector Register, SA Registers and QBus Interface Logic

2.12 RQDX1 CONTROL LOGIC

The supervisory control of the complete RQDX1 controller module is a shared function between the T-11 chip and the main high-speed controller. These two devices share the internal data address bus (DAL bus). (Refer to Figure 2-1)

The T-11 chip has control over all housekeeping functions that are considered to be slow or those that require data processing. The T-11 chip is configured into the 16-bit static mode driven by a 7.5 MHz clock. The T-11 logic, along with the RAM and ROM memories, is shown in Figure 2-7.

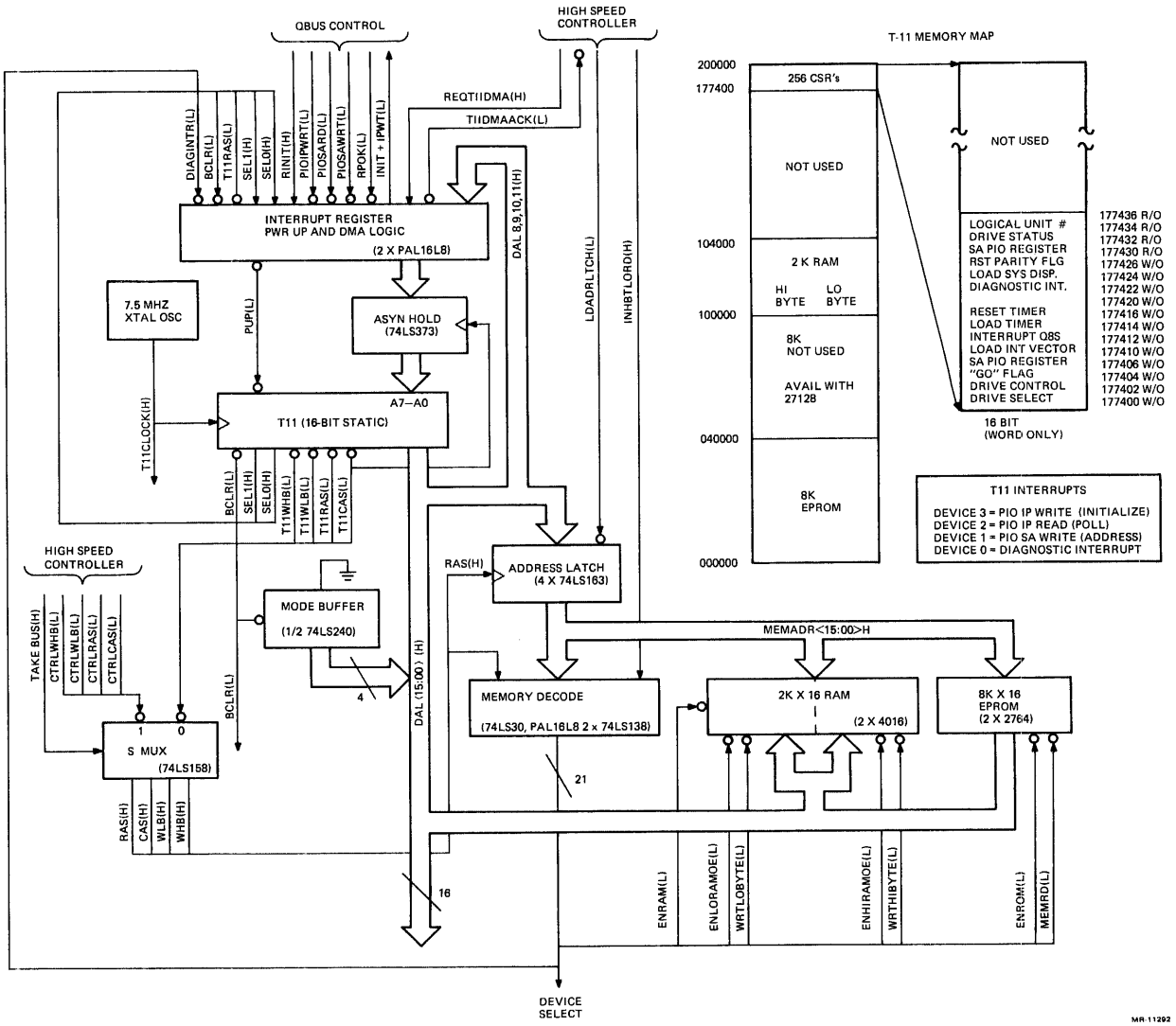


Figure 2-7 T-11, RAM and ROM Logic

The main high-speed controller controls the high-speed read, write, and DMA functions to or from host memory. This controller is configured as a microprogrammed multibranch controller operating at 10 MHz. The main high-speed controller architecture is shown in Figure 2-8.

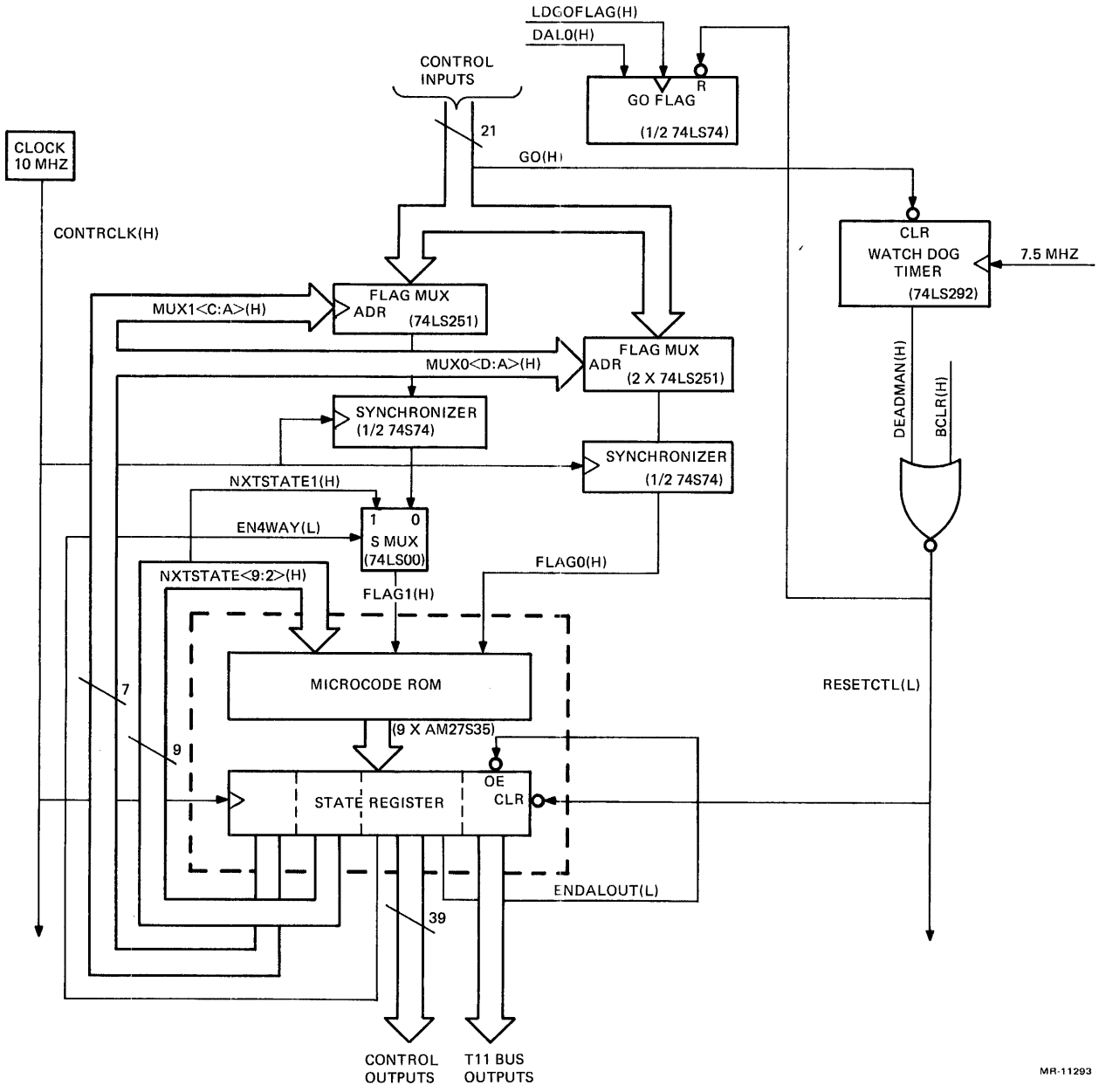


Figure 2-8 Main High-Speed Controller Architecture

The T-11 chip sets up all disk drive control signals, initializes the timer, clears the parity error flag, and resets the shuffle step oscillator. The T-11 chip then sets up the device control block (DCB) with parameters for the high-speed controller, initializes the response word with 1s, and then sets the GO flag in the I/O map. The high-speed controller, upon receipt of the GO signal, requests direct memory access to the DAL bus from the T-11 chip. Upon receipt of the T11DMAACK signal, the controller takes control of the DAL bus and begins the operation specified in the function code. Upon completion, various parameters are placed in T-11 RAM, the controller response word is filled in (in the DCB), the GO bit is cleared, and control is returned to the T-11 chip. All high-speed controller operations must be completed within 1 second or the timer logic will terminate controller operation.

2.13 MEMORY ADDRESS COUNTER/REGISTER

The memory address counter/register (shown in Figure 2-7) is used to latch the T-11 memory address during the address phase of the bus cycle. The counter function of the address register is used by the high-speed controller to form a RAM pointer which can be incremented.

2.14 2 K × 16 RAM

As shown in Figure 2-7, the 2 K × 16 RAM is divided into the following three major sections.

- T-11 work space
- Device control block
- Sector buffer

This RAM can be accessed by both the T-11 chip and the high-speed controller.

2.15 DISK DRIVE CONTROL REGISTER AND STATUS BUFFER

The disk drive control register and status buffer are shown in Figure 2-9. Under T-11 control, the disk drive control register provides drive selection and head control, including cylinder seeks on the selected drive. This register also contains static control information for the PLL and serializer. The drive status buffer is designed to interface the selected drive status to the DAL bus so that it can be interrogated by either the T-11 chip or the high-speed controller.

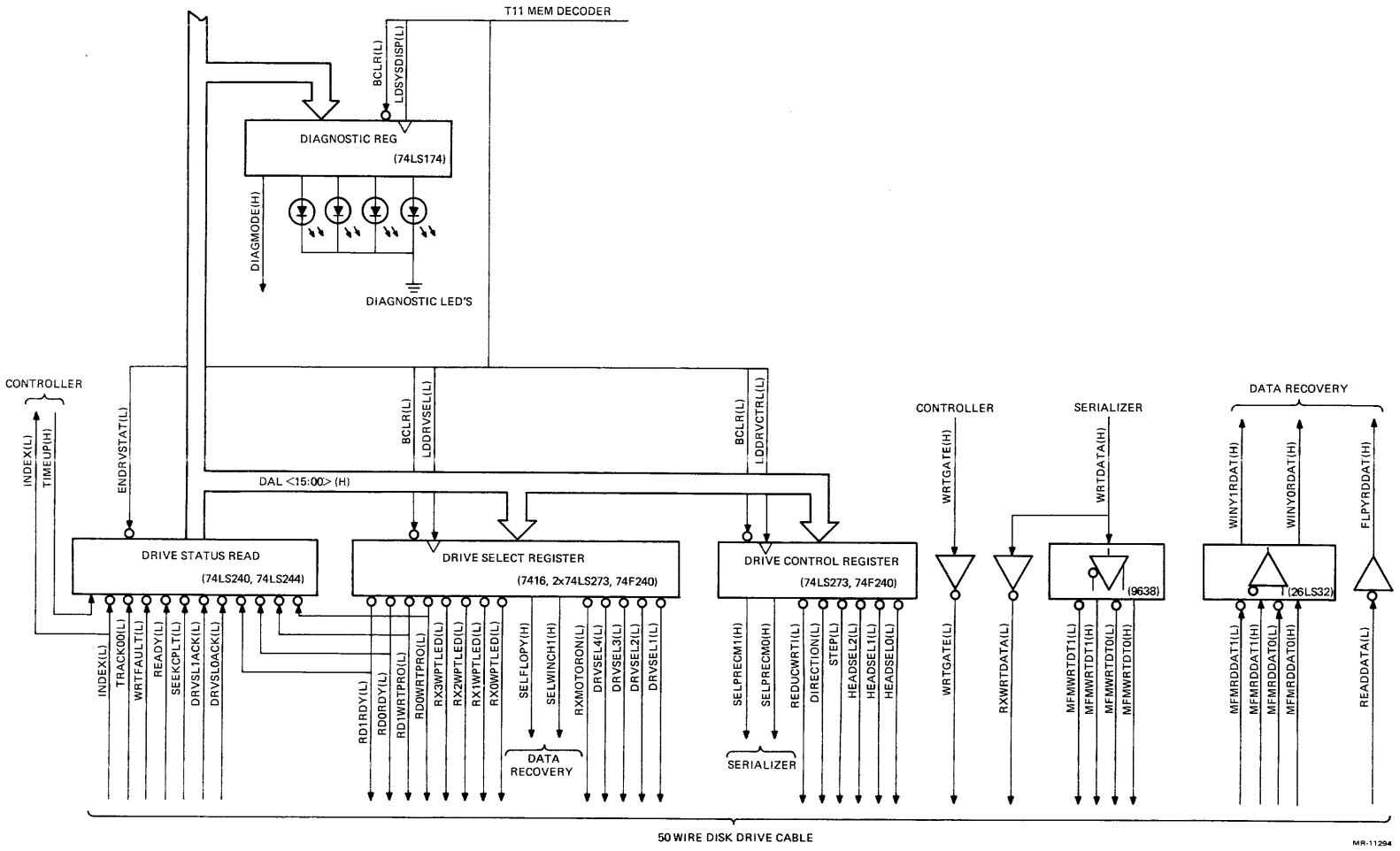


Figure 2-9 Disk Drive Control Register and Status Buffer

2.16 T-11 RAM ADDRESS POINTER AND ALU

The T-11 RAM pointer logic consists of an address counter and an ALU. The high-speed controller logic loads the beginning and ending T-11 RAM addresses into the registers within the address counter. The controller then uses these pointers to specify the locations in the T-11 RAM where data is to be transferred during QBus DMA and disk data transfers. The high-speed controller increments the pointers and monitors the ALU to determine when the ending address has been reached.

2.17 BIDIRECTIONAL BYTE MULTIPLEXER

The bidirectional byte multiplexer is used to interface the 8-bit input/output of the serializer/deserializer to the 16-bit RAM via the DAL bus.

During the read operation, the byte multiplexer causes the 8-bit byte from the serializer/deserializer to appear on both high and low bytes of the 16-bit DAL bus. The high-speed controller can then selectively write the byte into either the high or low byte section of the 2 K × 16 RAM.

During a write operation, the bidirectional byte multiplexer, again under control of the high-speed controller, can be used to place the high byte into the low byte position of the DAL bus. The low byte output of the RAM is disabled at this time.

2.18 8 K × 16 PROM

The 8 K × 16 PROM is used solely to store the T-11 instructions.

2.19 QBUS DMA POINTER AND ALU

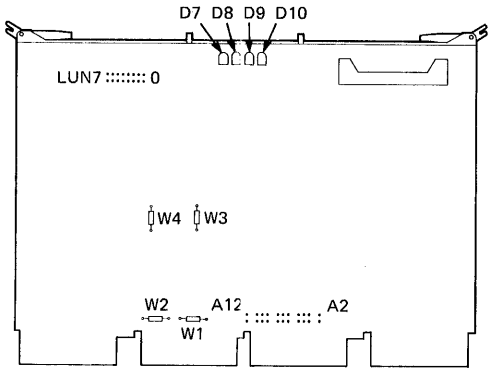
The QBus DMA pointer logic consists of an address counter and an ALU. This logic is controlled by the high-speed controller and is used to hold the QBus address during a DMA process.

This logic is also used as a byte comparator. The high-speed controller utilizes this compare function to perform sector seek functions during read/write operations.

CHAPTER 3
CONFIGURATION AND INSTALLATION

3.1 INTRODUCTION

The RQDX1 controller module must be mounted in the last occupied slot of the backplane due to the DMA and interrupt structure of the LSI-11 bus. The module's device address and logical unit number may be changed by reconfiguring jumpers on the module. Figure 3-1 shows the RQDX1 controller module jumper and diagnostic LED locations.



NOTES:
1. ADDRESS SELECTION (A12 THROUGH A2) AND LOGICAL UNIT NUMBER SELECTION (LUN7 THROUGH LUN0) IS MADE BY ATTACHING TWO POSITION JUMPER CLIPS (PART NO. 12-18783-00). THIS ELIMINATES THE NEED TO WIRE WRAP JUMPERS ONTO THE ADDRESS OR LOGICAL UNIT NUMBER STAKES.
2. JUMPERS W1 AND W2 ARE IN FOR Q/Q AND Q22/Q22 MACHINES AND ARE OUT FOR Q/CD AND Q22/CD MACHINES. THEY PROVIDE GRANT CONTINUITY.

MR-9915

Figure 3-1 RQDX1 Controller Module Jumper and LED Locations

3.2 DEVICE ADDRESS SELECTION

The location of the RQDX1 controller module address jumpers is shown in Figure 3-1. Table 3-1 lists the jumper configuration for the standard module address (772150). To configure the module for an address other than 772150, use the format shown in Figure 3-2 to determine the appropriate jumper configuration.

Table 3-1 RQDX1 Standard Address Jumper Configuration

Jumper	State	
A2	Out	Address selection (772150)
A3	In	
A4	Out	
A5	In	
A6	In	
A7	Out	
A8	Out	
A9	Out	
A10	In	
A11	Out	
A12	In	

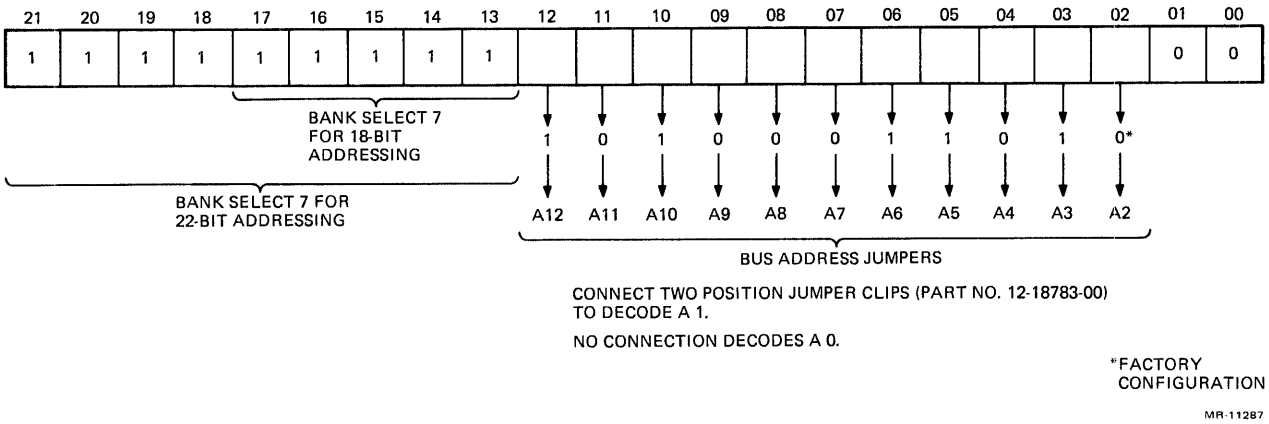


Figure 3-2 RQDX1 Address Selection Jumper Format

3.3 LOGICAL UNIT NUMBER SELECTION

The location of the RQDX1 controller module logical unit number jumpers is shown in Figure 3-1. These jumpers are set to the lowest logical unit number assigned to any disk/diskette drive controlled by the module. The controller module automatically sizes the logical unit configuration during initialization to determine how many (of the four possible units) are actually present. This automatic sizing eliminates the need for reconfiguration of jumpers when units (RD51 or RX50 drives) are added to or removed from the controller module. The standard configuration for the logical unit number jumpers (selecting logical unit number 0) is listed in Table 3-2. To configure the module for logical unit numbers beginning with other than unit number 0, use the format shown in Figure 3-3 to determine the appropriate jumper configuration.

Table 3-2 RQDX1 Standard Logical Unit Number Jumper Configuration

Jumper	State	
LUN1	Out	Logical unit number (0)*
LUN2	Out	
LUN3	Out	
LUN4	Out	
LUN5	Out	
LUN6	Out	
LUN7	Out	
LUN8	Out	

* This indicates that logical unit numbers 0–3 are assigned to this controller module. The controller will automatically determine if less than four logical units are present.

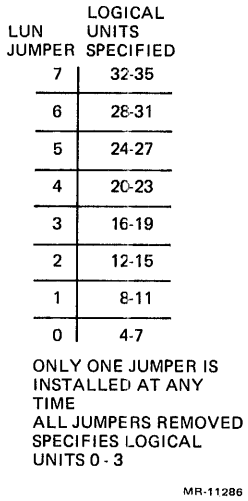


Figure 3-3 RQDX1 Logical Unit Number Jumper Format

3.4 INTERRUPT VECTOR

The interrupt vector has a range of 0 to 774 and is software selectable. (A vector selected by software must be greater than 0.) The normal interrupt vector used by the RQDX1 controller module is 154.

3.5 INTERRUPT REQUEST LEVEL

The RQDX1 controller module interrupts at priority level 4 determined by E3, a DC003 chip.

3.6 RQDX1 CONTROLLER MODULE INSTALLATION

The RQDX1 module (M8639) is typically installed in the last occupied slot of the backplane. If empty slots are left between the other modules and the M8639 module, install grant cards (part number G7272) in those empty slots to accommodate the interrupt and direct memory access structure of the backplane.

Before installing the module, make sure that the address and logical unit number jumpers are properly configured.

Install the 50-conductor signal cable (part number BC02D-1D) to the J1 connector on the M8639 module. This cable must be connected to a signal distribution panel that will connect the appropriate signals to the RD51 and/or RX50 drives. An example of the MICRO/PDP-11 signal distribution panel connecting the M8639 module to an RD51 disk drive and an RX50 diskette drive is shown in Figure 3-4. The RD51 disk drive requires two signal cable connections. One is a 20-conductor cable (part number 17-00282-00), the other is a 34-conductor cable (part number 17-00286-00). The RX50 diskette drive requires a single 34-conductor signal cable (part number 17-00285-02).

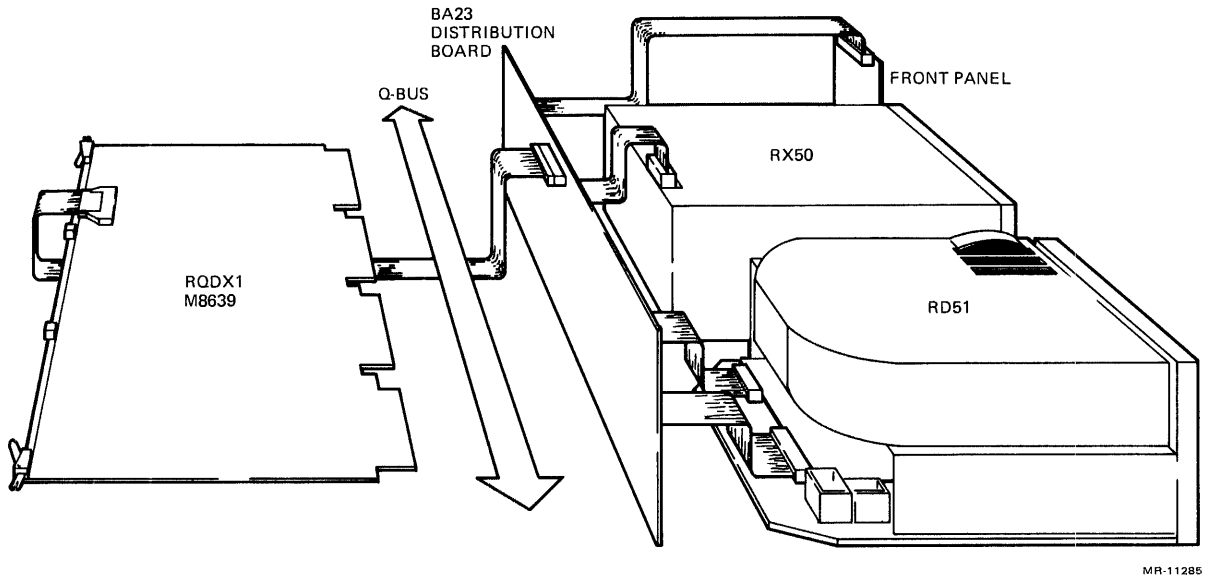


Figure 3-4 RQDX1 MICRO/PDP-11 Signal Distribution Connections

3.7 RQDX1-E EXTENDER MODULE OPTION

Typically (in the MICRO/PDP-11), the RQDX1 controller module is located in the same mounting box as the disk and/or diskette drives that it controls. However, if the system mounting box cannot accommodate all of these drives, the optional RQDX1-E extender module may be used to connect the RQDX1 controller module signals to any drive that is external from the system mounting box.

3.7.1 RQDX1-E Extender Module Jumper Configuration

As shown in Figure 3-5, the RQDX1-E extender module is a dual-height module that provides signal connectors and requires appropriate jumper configurations. The J2 connector receives signals from the RQDX1 controller module. The other connectors (J1 and J3) distribute these signals to the disk and diskette drives. Jumper functions for the RQDX1-E extender module, as well as the jumpers installed in the factory configuration, are listed in Table 3-3.

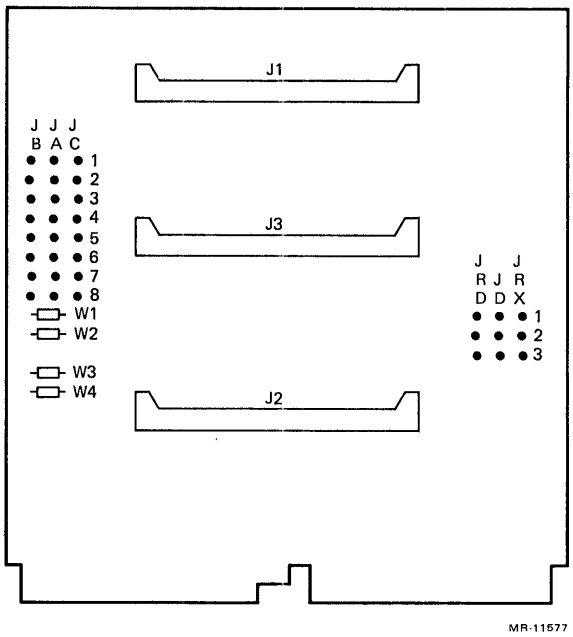


Figure 3-5 RQDX1-E Extender Module Jumper Locations

Table 3-3 RQDX1-E Extender Module Jumper Configuration

Jumpers	Functions	Factory Configuration*
W1 through W4	Must be installed (Manufacturing use only)	W1 through W4
JRD1 through JRD3 JD1 through JD3 JRX1 through JRX3	Select the external drive to be connected to the J3 connector	JD1 to JRD1 JD2 to JRD2 JD3 to JRD3
JB1 through JB8 JA1 through JA8 JC1 through JC8	Determine which connector (J2 or J3) the RD read/write will connect to	JA1 to JC1 JA2 to JC2 JA3 to JB3 JA4 to JB4 JA5 to JB5 JA6 to JB6 JA7 to JC7 JA8 to JC8

* Factory configuration is set to connect an external RD51 disk drive to connector J3. To configure the module for an external RX50 (connected to J3), jumpers JD1 through JD3 are connected to JRX1 through JRX3, jumpers JA1 through JA8 are connected to JB1 through JB8.

NOTE

Jumper selection (for configurations listed in Table 3-3) is made by attaching two-position jumper clips (part number 12-18783-00).

3.7.2 RQDX1-E Extender Module Installation

Figure 3-6 shows the installation of the RQDX1-E extender module option in the MICRO/PDP-11 system (BA23 mounting box). The M7512 dual-height module is installed in the backplane slot directly below the M8639 (RQDX1) module, in connectors A and B. A cable (part number BC02D-0K) connects the RQDX1 controller module to the RQDX1-E extender module through the J2 connector. Another cable (part number 70-18652-01) attached to the J3 connector connects the RQDX1-E extender module to a mounting plate (part number 74-2866-01) that is mounted to the system's patch and filter panel assembly. (The entire cable and mounting plate assembly may be ordered as part number 70-20691-01.) This external plate provides the signals to be sent to the external drive. A third cable (part number BC02D-1D – attached to the J1 connector on the RQDX1-E extender module) is connected to the signal distribution panel in the mounting box, providing signals to the disk or diskette drives that are installed in the system mounting box.

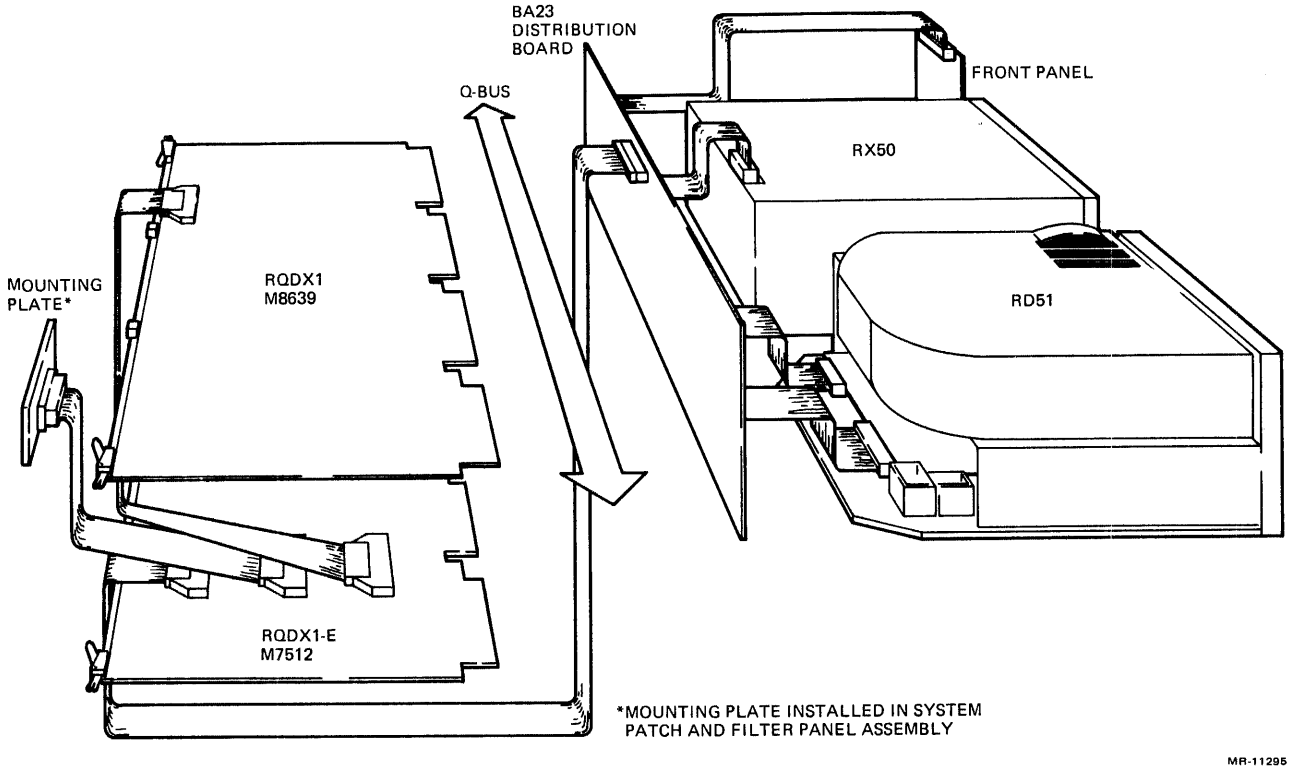


Figure 3-6 RQDX1-E Extender Module Connections

CHAPTER 4
REGISTERS AND COMMANDS

4.1 INTRODUCTION

The RQDX1 controller module contains two registers that can be accessed by a QBus address. A number of other registers reside on the module, but these are accessible only to the T-11 logic within the module.

The module uses mass storage control protocol (MSCP) to communicate with the host QBus processor. Detailed information regarding MSCP is available in the UDA50 Programmer's Documentation Kit (document number QP-905-GZ).

4.2 REGISTERS

The programmable registers contained on the RQDX1 controller module are the initialize and poll register (IP) and the status and address register (SA).

These registers can be addressed like any memory location.

4.2.1 Initialize and Poll Register (IP)

The initialize and poll register (IP) has a standard LSI-11 bus address of 772150. This address is determined by the address selection jumpers on the RQDX1 module. (Refer to Paragraph 3.2 for jumper selection information.)

The host begins the initialization sequence by either issuing a bus initialize or by using the IP initialize operation. The IP register is not an actual register, but is simply a circuit that checks for a write operation at the IP address. Any write to that address will cause an initialize operation to take place.

4.2.2 Status and Address Register (SA)

The status and address register (SA) has a standard LSI-11 bus address of 772152. This address is determined by the address selection jumpers on the RQDX1 module.

The SA register consists of a set of two registers, the SA read register and the SA write register. These are named according to their function in relation to the QBus host processor.

The SA read register is written into by the RQDX1 module's T-11 and read from by the QBus. This register is used to pass initialization status to the QBus processor.

The SA write register is written into by the QBus processor and read from by the T-11. This register is used during the initialization process to pass the mass storage control protocol (MSCP) command buffer address and interrupt vector to the T-11 chip.

4.3 MASS STORAGE CONTROL PROTOCOL (MSCP)

Mass storage control protocol (MSCP) is the message-oriented set of rules by which the RQDX1 controller module communicates with the host system. MSCP provides the protocol that allows the host to send a command message and the controller module to send a response message. The host designates an area of memory to be used as a *communications area*, and provides the location of this area to the controller module. The size of the communications area is variable and is determined by the host software. Its organization is shown in Figure 4-1. For additional information regarding MSCP, refer to the UDA50 Programmer's Documentation Kit (document number QP-905-GZ).

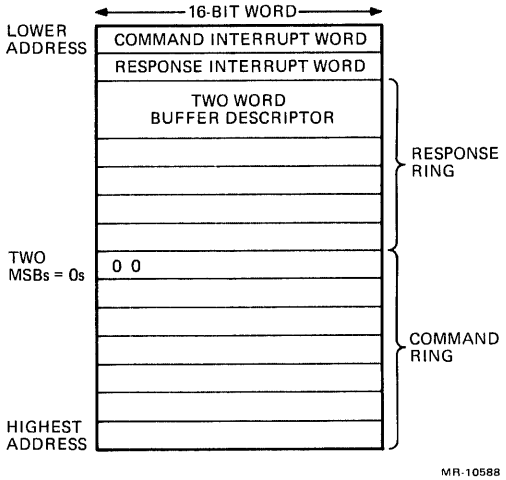


Figure 4-1 Memory "Communications Area" Organization

4.3.1 MSCP Commands

Table 4-1 lists MSCP commands and their functions that are supported by the RQDX1 controller module.

Table 4-1 MSCP Commands

Command	Function
Access	Reads data from the specified unit.
Abort	Guarantees that referenced MSCP command will complete within the controller timeout period.
Available	If specified unit is on-line, returns it to the unit-available state. If specified unit is currently in the unit-available state, this command is essentially a no-operation. (The RQDX1 cannot spin down a unit.)
Compare Host Data	Reads data from the disk and compares it with the data in the host buffer.
Erase	Writes zeros to the specified logical blocks on the unit. (No data is accessed from the host.)
Get Command Status	Reports on the status of a specified command by returning a number that reflects the command's progress.
Get Unit Status	Reports on the status of a specified unit.
On Line	Places the specified unit on line, if possible.
Read	Reads data starting from the specified logical block on the disk into host memory.
Set Controller Characteristics	Sets host-settable controller characteristics.
Set Unit Characteristics	Sets host-settable unit characteristics.
Write	Writes data starting at the specified logical block on the disk from the host memory.

4.3.2 MSCP Status Codes

The RQDX1 controller module provides MSCP status code response messages listed in Table 4-2.

Table 4-2 MSCP Status Code Messages

Message	Meaning
Command Aborted	The current command was aborted before it could be completed normally.
Compare Error	While performing a Compare command, a discrepancy was found while comparing the disk data to the host data.
Controller Error	The RQDX1 controller module detected an internal error, but is able to continue processing its outstanding commands.
Data Error	Data could not be read or written due to CRC errors, "header not found", or due to a sector being read whose forced error bit was set.
Drive Error	A drive-related error was detected (such as a seek failure).
Media Format Error	Indicates the the media mounted on the unit was incorrectly formatted.
Host Buffer Access Error	Reports bus timeouts and parity errors during data transfers. (Applies only to the data portion of an MSCP command.)
Invalid Command	The RQDX1 controller module found some field in the command to be in error.
Success	The command was successfully completed.
Unit Available	The RQDX1 controller module is not on line, but it can accept an On Line command from the host.
Unit Offline	The RQDX1 controller module is not on line, and it cannot be brought on line.
Write Protected	A write or erase command was attempted to a unit that is either physically or logically write-protected.

4.4 DIAGNOSTICS AND UTILITIES PROTOCOL (DUP)

The diagnostics and utilities protocol (DUP) provides a diagnostic mode of communication between the host QBus processor program and the diagnostic and utilities server task (DUST). This protocol allows the host program to request that the DUST load a diagnostic or utility program and execute it. Some diagnostic programs access the diagnostic blocks on the RD51 disk. This allows the diagnostic to test reading/writing on the disk without accessing or affecting customer software.

During execution of the diagnostic or utility program, the host program can make inquiries to the DUST about the progress of the program being executed, or abort the program if there are unexpected results.

The diagnostic and utility programs executed by DUP commands (see Table 4-3) may require the host program to specify certain parameters (such as starting host buffer addresses, byte count, block count, etc.).

For additional information regarding DUP, refer to the UDA50 Programmer's Documentation Kit (document number QP-905-GZ).

Table 4-3 DUP Programs

Program	Function
Write DBN (RD51 only)	Writes and transfers a diagnostic block with a data pattern.
Read DBN (RD51 only)	Reads a diagnostic block.
Format (RD51 only)	Formats the entire disk, verifies the disk, and implements bad block revectoring.
Read Sector (RD51 or RX50)	Reads a physical sector. The data is not transferred to the host, but drive problems will be detected.
Restore (RD51 or RX50)	Moves the read/write head of the drive to the home position.
Self Test	Verifies that certain RQDX1 controller module logic is functioning properly. Self Test results are reported in the diagnostic LEDs (refer to Paragraph 5.2). Self Test is always executed on power up or Bus INIT.

4.4.1 DUP Commands

The following commands are available to DUP and are supported by the RQDX1 controller module.

- Get DUST Status
- Execute Supplied Program
- Execute Local Program (Diagnostic or Utility)
- Send Data
- Receive Data
- Abort Program

4.4.2 DUP Responses

The following responses are available to DUP and are supported by the RQDX1 controller module.

- Success
- Illegal Command

In the case of an Execute Supplied Program command, the following responses are also available.

- No Region Available
- No Region Suitable

In the case of an Execute Local Program command, the following responses are also available.

- No Region Available
- No Region Suitable
- Program Not Known
- Load Failure
- Standalone

CHAPTER 5
ERROR DETECTION

5.1 INTRODUCTION

Each time that the RQDX1 controller module is powered up, the module executes a selftest that verifies the operation of the T-11 chip and the ROM and RAM memory chips. Successful completion of the selftest takes approximately five seconds. The RQDX1 controller module provides a set of four diagnostic LEDs that display a code corresponding to the functional block of the selftest currently being executed or the type of failure that occurred. The diagnostic LEDs and error codes are described in Paragraph 5.2.

Diagnostic programs determine whether or not the RQDX1 controller module, the RD51 disk drive, and/or the RX50 diskette drive are working properly. If they are not, they isolate the failing component. Diagnostic programs are used exclusively for maintenance purposes and play no part in normal system operation. The programs are provided on the XXDP+ diagnostic software system available from Digital Equipment Corporation. The diagnostic programs that test the RQDX1 controller module, the RD51 disk drive, and the RX50 diskette drive are described in Paragraph 5.3.

5.2 DIAGNOSTIC LED ERROR DISPLAYS

The diagnostic LEDs provided on the RQDX1 controller module indicate faults during the selftest. On power up, all of the LEDs are lit and then immediately cleared as the RQDX1 module enters the selftest. The LEDs indicate (in a binary sequence) the functional block of the selftest or the type of failure that has occurred. All four LEDs are off after successful completion of the selftest. Figure 5-1 shows the diagnostic LED locations on the RQDX1 module. Table 5-1 lists the diagnostic LED codes and the corresponding failure description.

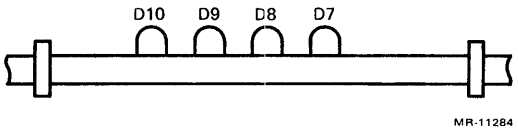


Figure 5-1 Diagnostic LED Locations

Table 5-1 Diagnostic LED Error Displays

Display LED Octal	MSD D10 Bit 3	LSD D9 Bit 2	D8 Bit 1	D7 Bit 0	Type of Error
00	Off	Off	Off	Off	No error Exit from selftest
01	Off	Off	Off	On	T-11 failure
02	Off	Off	On	Off	T-11 2942 failure
03	Off	Off	On	On	QBus 2942 failure
04	Off	On	Off	Off	Serializer deserializer failure
05	Off	On	Off	On	CRC failure
06	Off	On	On	Off	Microcode version
07	Off	On	On	On	Diagnostic interrupt failure
10	On	Off	Off	Off	Shuffle oscillator failure
11	On	Off	Off	On	RQDX1 ROM checksum failure
12	On	Off	On	Off	RQDX1 RAM failure
13	On	Off	On	On	Undefined
14	On	On	Off	Off	Undefined
15	On	On	Off	On	Undefined
16	On	On	On	Off	Undefined
17	On	On	On	On	Power up of the RQDX1 or reception of Bus INIT

5.3 DIAGNOSTIC SOFTWARE

The XXDP+ diagnostic software system provides the diagnostic programs necessary to test the RQDX1 controller module, as well as any RD51 disk drives and/or RX50 diskette drives that are connected to the RQDX1. Table 5-2 lists the appropriate XXDP+ diagnostic programs and the testing function performed by each program. The individual program listings may be used to further isolate component failures.

Table 5-2 XXDP+ Diagnostic Programs

XXDP+ Program Name	Title
ZRQA??.BIN*	RDRX Performance Exerciser
ZRQB??.BIN	RDRX Formatter†

* ?? indicates any revision of the program.

† This program formats the RD51 disk. The procedure is described in Paragraph 6.2.2.

CHAPTER 6
DISK DRIVES

6.1 INTRODUCTION

The RQDX1 controller module is used to interface an RD51 disk drive(s) and/or an RX50 diskette drive(s) to the extended LSI-11 bus.

The RD51 disk drive is a random access storage device which uses two nonremovable 133.4 mm (5.25 inch) disks as storage media. The total formatted capacity of the RD51 disk drive is 11 megabytes.

The RX50 diskette drive is a random access dual diskette storage device which uses two single-sided 133.4 mm (5.25 inch) RX50K diskettes. The total drive capacity is 800 K bytes of formatted data.

6.2 RD51 DISK DRIVE

The RD51 disk drive, shown in Figure 6-1, is a field replaceable unit (FRU) that is installed in a system mounting box. The RD51 drive is connected to the controller module (via the distribution panel) by two signal cables (J1 and J2). A third cable (J3) provides power supply connections to the RD51 drive. The connector pin assignments for each of the three cables is provided in Appendix C.

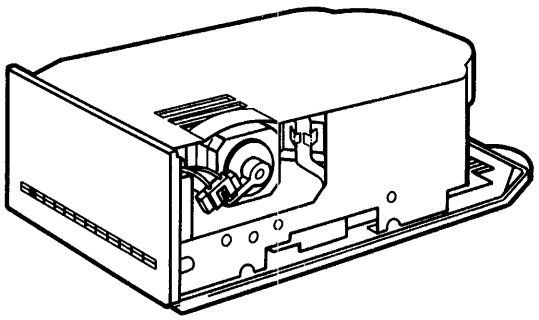


Figure 6-1 RD51 Disk Drive

The RD51 disk drive capacity is 11 megabytes on two nonremovable 133.4 mm (5.25 inch) disks. Each disk surface uses one movable head to service 306 data tracks. The head and disk technology used allows the heads, which normally fly over the disk surface, to land when the drive is powered off. This technology, termed Winchester, utilizes lubricated media and lightly loaded read/write heads.

High bit densities on the media are achieved by flying the heads at a height of 20 microinches. This flying height requires a clean air environment which is achieved by manufacturing and sealing the head and disk assembly (HDA) in a clean room environment.

6.2.1 RD51 Disk Drive Installation

Installation of the RD51 disk drive requires proper configuration of the dual in-line package (DIP) shunt jumper pack located on the RD51 read/write printed circuit board. Location of the shunt is shown in Figure 6-2. The proper jumper configuration (required for the RD51 drive to be used with the RQDX1 controller module) is listed in Table 6-1.

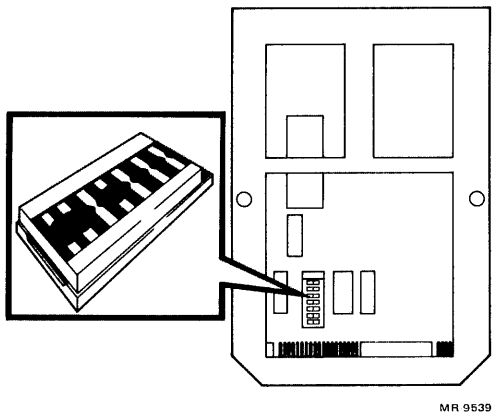


Figure 6-2 RD51 Disk Drive Read/Write Printed Circuit Board

Table 6-1 DIP Shunt Jumper Configuration

Pin Numbers	Pin Connection
1 to 16	Not used*
2 to 15	In
3 to 14	In
4 to 13	In
5 to 12	Out
6 to 11	In
7 to 10	Out
8 to 9	Out

* The 14-pin DIP jumper pack is offset into a 16-pin socket toward the contact pins on the read/write printed circuit board. If the DIP shunt (jumpers) need to be replaced, a new DIP shunt can be ordered (part number 29-24115).

NOTE

Any replacement RD51 disk drive must be formatted using the ZRQB??.BIN program to be compatible with the RQDX1 controller module. (Refer to Paragraph 6.2.2 for the formatting procedure.)

WARNING

When sliding the RD51 disk drive in or out of a system chassis, do not hold the drive by its front right side. Doing so will cause the head positioner flag to rotate, resulting in damage to the drive. Figure 6-3 shows the head positioner flag location on the disk drive.

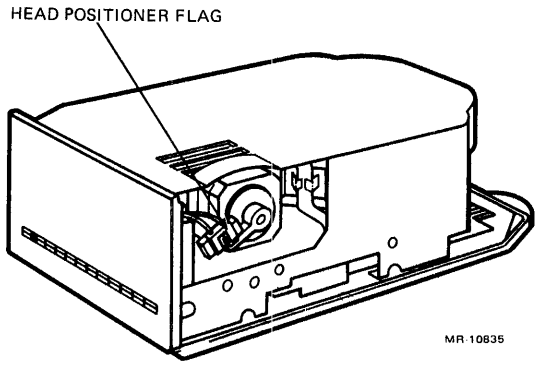


Figure 6-3 RD51 Disk Drive Head Positioner Flag

6.2.2 Formatting the RD51 Disk Drive

The ZRQB?? (any revision) program, provided by the XXDP+ diagnostic software system, is used to format the RD51 disk drive. The procedure for formatting is as follows.

In response to the XXDP+ . (period) prompt, type R ZRQB??

```
.R ZRQB?? <CR>
```

(The question marks will allow any revision of the program to be used.) A response similar to the following appears on the console terminal.

```
DRSD0
RDRX -X-X  (where -X-X is the current revision information)
RD51 DISK FORMATTER
UNIT IS RQDX1 DISK DRIVE SUBSYSTEM
RSTRT ADR AAAAAA  (where AAAAAA specifies a restart address)
DR>
```

You must respond to this prompt with a command to run the program. For example:

```
DR>START  (default will cause the program to run one pass)
```

You are then asked the following.

```
CHANGE HW (L) ? N

CHANGE SW (L) ? N

ENTER UNIT TO BE FORMATTED (D) ? X  (where X is the unit number assigned to the drive
                                     to be formatted)

USE EXISTING BAD BLOCK INFORMATION (L) N ? N

USE DOWN LINE LOAD (L) N ? N

CONTINUE IF BAD BLOCK INFORMATION IS INACCURATE (L) N ? Y

ENTER 8 CHARACTER SERIAL NUMBER (A) ?
```

The 8-character serial number is a unique serial number assigned to each RD51 disk drive. It is labeled on the left side of the disk drive (refer to Figure 6-4).

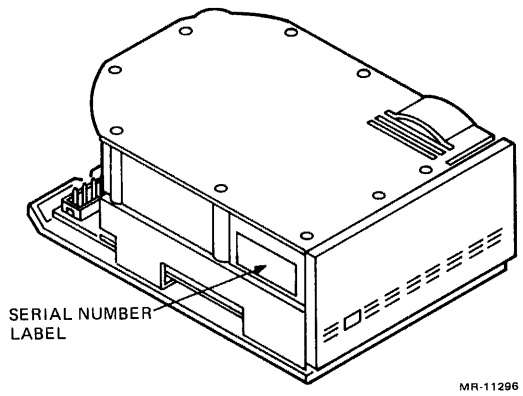


Figure 6-4 RD51 Serial Number Label Location

```
ENTER DATE IN MM-DD-YY FORMAT (A) ?
```

As shown above, the current date should be entered.

The format routine takes approximately 11 minutes to complete, and its successful completion results in a message similar to the following.

```
FORMAT COMPLETED, X REVECTORED LBNS
RDRX EOP 1
  0 TOTAL ERRS
```

The RQDX1 controller module automatically revectors any bad sectors and prints the total number of revectored sectors in the format completed message. The maximum number of sectors that will be revectored is 144.

If the formatting process is not successful, an error message appears on the terminal. Refer to the individual program listing to use this message (if necessary) to isolate the failure or to determine which FRU to replace.

6.3 RX50 DISKETTE DRIVE

The RX50 diskette drive is shown in Figure 6-5. The RX50 diskette drive is a field replaceable unit (FRU) that is installed in a system mounting box. One cable connects the RX50 to the RQDX1 controller module (via the distribution panel), another cable connects the drive to the power supply. There are no field alignment procedures for the RX50 diskette drive, since it is adjusted and aligned at the time of manufacture.

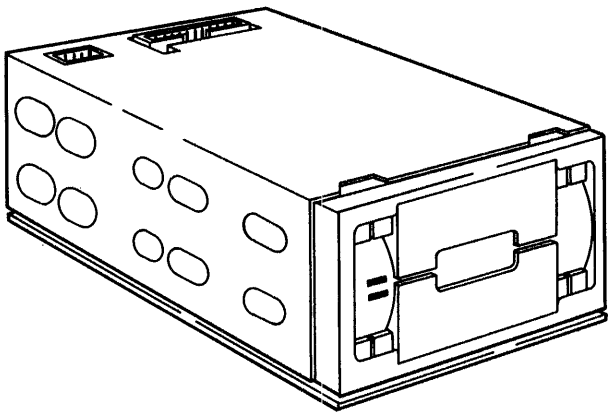


Figure 6-5 RX50 Diskette Drive

The RX50 diskette drive is a random access, dual-diskette storage device. It has two access doors and slots for diskette insertion and removal. An active drive light for each diskette slot informs you when that drive is busy. The RX50 diskette drive capacity is 800 K bytes of formatted data on two single-sided diskettes. This is accomplished by utilizing a 133.4 mm (5.25 inch) RX50K diskette that contains 80 tracks, 10 sectors per track, and 512 bytes per sector of modified frequency modulation (MFM) data. The average access time, including latency, is 264 ms.

APPENDIX A
RQDX1 CONTROLLER MODULE BACKPLANE PIN ASSIGNMENTS

Digital Equipment Corporation's plug-in modules, including the RQDX1 controller module, all use the same contact (pin) identification system. Figure A-1 shows the contact finger identification for a typical quad-height module. Each connector contains 36 lines (18 lines on each side of the printed circuit board). Table A-1 lists the backplane pin assignments for the RQDX1 controller module.

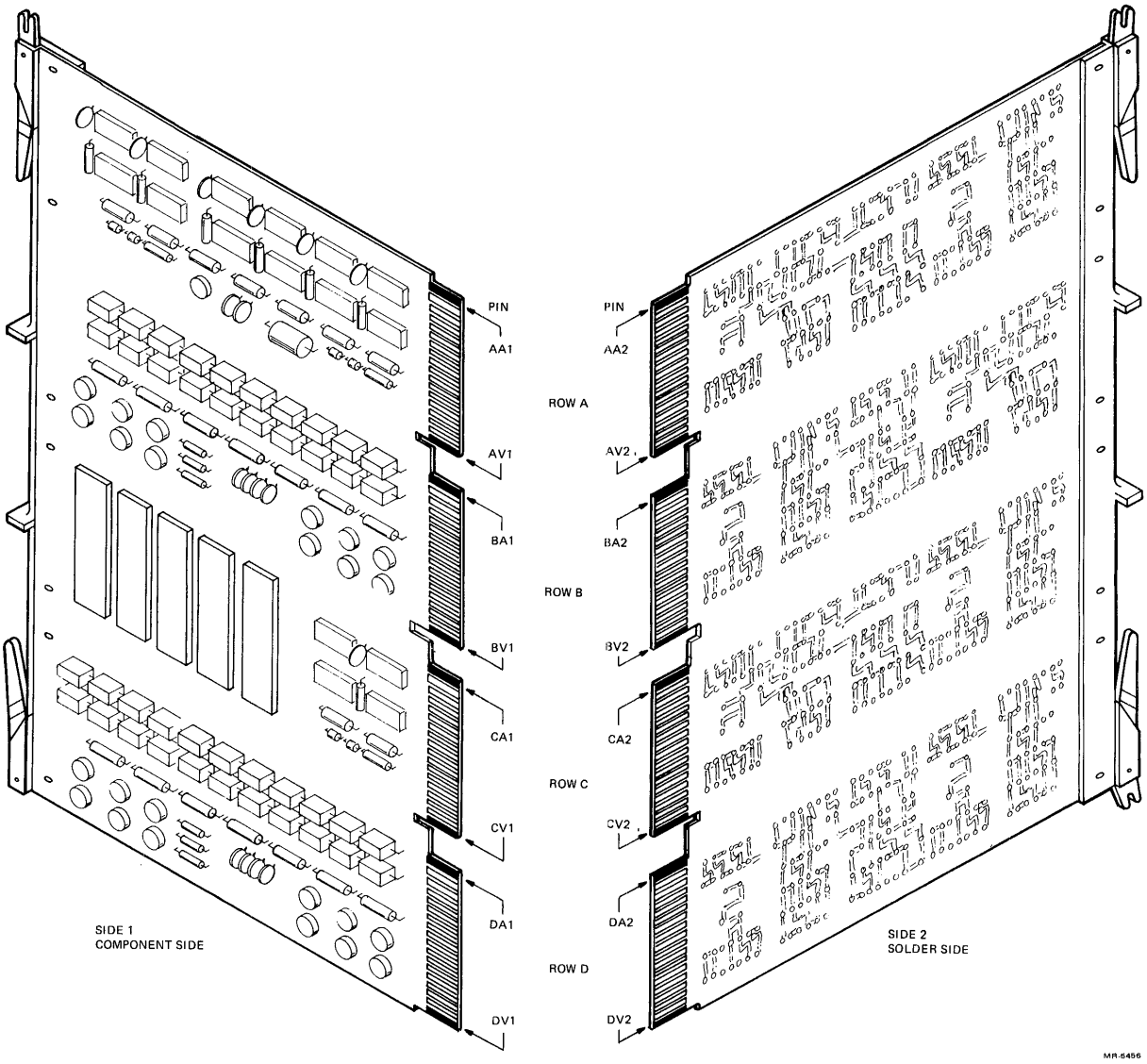


Figure A-1 Quad Module Contact Finger Identification

Table A-1 RQDX1 Controller Module Backplane Pin Assignments

Pin	Signal Name	Pin	Signal Name
AA1	(BIRQ5 L)	AA2	+5V
AB1	(BIRQ6 L)	AB2	(−12V)
AC1	BDAL16 L	AC2	GND
AD1	BDAL17 L	AD2	(+12V)
AE1	(SSPARE1 or +5B)	AE2	BDOUT L
AF1	(SSPARE2)	AF2	BRPLY L
AH1	(SSPARE3)	AH2	BDIN L
AJ1	GND	AJ2	BSYNC L
AK1	(MSPAREA)	AK2	BWTBT L
AL1	(MSPAREB)	AL2	BIRQ4 L
AM1	GND	AM2	BIAKI L
AN1	BDMR L	AN2	BIAKO L
AP1	(BHALT L)	AP2	BBS7 L
AR1	BREF L	AR2	BDMGI L
AS1	(+12B or +5B)	AS2	BDMGO L
AT1	GND	AT2	BINIT L
AU1	(PSPARE1)	AU2	BDAL0 L
AV1	(+5B)	AV2	BDAL1 L
BA1	(BDCOK H)	BA2	+5V
BB1	BPOK H	BB2	(−12V)
BC1	BDAL18 L	BC2	GND
BD1	BDAL19 L	BD2	+12V
BE1	BDAL20 L	BE2	BDAL2 L
BF1	BDAL21 L	BF2	BDAL3 L
BH1	(SSPARE8)	BH2	BDAL4 L
BJ1	GND	BJ2	BDAL5 L
BK1	(MSPAREB)	BK2	BDAL6 L
BL1	(MSPAREB)	BL2	BDAL7 L
BM1	GND	BM2	BDAL8 L
BN1	BSACK L	BN2	BDAL9 L
BP1	(BIRQ7 L)	BP2	BDAL10 L
BR1	(BEVNT L)	BR2	BDAL11 L
BS1	(+12B)	BS2	BDAL12 L
BT1	GND	BT2	BDAL13 L
BU1	(PSPARE2)	BU2	BDAL14 L
BV1	+5V	BV2	BDAL15 L

Table A-1 RQDX1 Controller Module Backplane Pin Assignments (Cont)

Pin	Signal Name	Pin	Signal Name
CA1	(Unused)	CA2	+5V
CB1	(Unused)	CB2	(Unused)
CC1	(Unused)	CC2	GND
CD1	(Unused)	CD2	(Unused)
CE1	(Unused)	CE2	(Unused)
CF1	(Unused)	CF2	(Unused)
CH1	(Unused)	CH2	(Unused)
CJ1	GND	CJ2	(Unused)
CK1	(Unused)	CK2	(Unused)
CL1	(Unused)	CL2	(Unused)
CM1	GND	CM2	CIAKI L
CN1	(Unused)	CN2	CIAKO L
CP1	(Unused)	CP2	(Unused)
CR1	(Unused)	CR2	CDMGI L
CS1	(Unused)	CS2	CDMGO L
CT1	GND	CT2	(Unused)
CU1	(Unused)	CU2	(Unused)
CV1	(Unused)	CV2	(Unused)
DA1	(Unused)	DA2	+5V
DB1	(Unused)	DB2	(Unused)
DC1	(Unused)	DC2	GND
DD1	(Unused)	DD2	(Unused)
DE1	(Unused)	DE2	(Unused)
DF1	(Unused)	DF2	(Unused)
DH1	(Unused)	DH2	(Unused)
DJ1	GND	DJ2	(Unused)
DK1	(Unused)	DK2	(Unused)
DL1	(Unused)	DL2	(Unused)
DM1	GND	DM2	(Unused)
DN1	(Unused)	DN2	(Unused)
DP1	(Unused)	DP2	(Unused)
DR1	(Unused)	DR2	(Unused)
DS1	(Unused)	DS2	(Unused)
DT1	GND	DT2	(Unused)
DU1	(Unused)	DU2	(Unused)
DV1	(Unused)	DV2	(Unused)

APPENDIX B
RQDX1 CONTROLLER MODULE CABLE SIGNALS

Table B-1 lists the RQDX1 controller module signals on the J1 connector.

Table B-1 J1 Connector Signals

J1 Pin	Signal Name
1	MFMWRTDT1 (H) (RD51 only signal)
2	MFMWRTDT1 (L) (RD51 only signal)
3	GROUND
4	HEAD SEL 2 (L) (RDXX only signal)*
5	GROUND
6	SEEKCPLT (L) (RD51 only signal)
7	RD1 RDY (H) (RD51 only signal)
8	WRT FAULT (L)
9	DRVBUSOE (L)
10	HEAD SEL 1 (L) (RD51 only signal)
11	RX0WPTLED (L) (RX50 only signal)
12	RD0 RDY (H) (RD51 only signal)
13	RX1WPTLED (L) (RX50 only signal)
14	DRVSL0ACK (L) (RD51 only signal)
15	MFMRDDAT0 (H) (RD51 only signal)
16	MFMRDDAT0 (L) (RD51 only signal)
17	MFMWRTDT0 (H) (RD51 only signal)
18	MFMWRTDT0 (L) (RD51 only signal)
19	MFMRDDAT1 (H) (RD51 only signal)
20	MFMRDDAT1 (L) (RD51 only signal)
21	GROUND
22	REDUCWRTI (L)
23	RD0WRTPRO (L) (RD51 only signal)
24	DRV SEL 4 (L)
25	GROUND
26	INDEX (L)
27	RD1WRTPRO (L) (RD51 only signal)
28	DRV SEL 1 (L)
29	DRV SEL 2 (L)

* Reserved for future use.

Table B-1 J1 Connector Signals (Cont)

J1 Pin	Signal Name
30	DRV SEL 3 (L)
31	RX2WPTLED (L) (RX50 only signal)
32	RXMOTORON (L) (RX50 only signal)
33	GROUND
34	DIRECTION (L)
35	GROUND
36	STEP (L)
37	GROUND
38	RXWRTDATA (L) (RX50 only signal)
39	GROUND
40	WRT GATE (L)
41	GROUND
42	TRACK 00 (L)
43	RX3WPTLED (L) (RX50 only signal)
44	DRVSL1ACK (L) (RD51 only signal)
45	GROUND
46	READ DATA (L) (RX50 only signal)
47	GROUND
48	HEAD SEL 0 (L)
49	GROUND
50	READY (L)

* Reserved for future use.

APPENDIX C
DISK DRIVE CABLE CONNECTOR PIN ASSIGNMENTS

C.1 RD51 DISK DRIVE CONNECTOR PIN ASSIGNMENTS

The connector pin assignments for the RD51 disk drive signal and power cables are listed in Tables C-1 through C-3.

Table C-1 RD51 Disk Drive J1 Signal Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
1	2	Reserved
3	4	Head Select 2
5	6	Write Gate
7	8	Seek Complete
9	10	Track 0
11	12	Write Fault
13	14	Head Select 0
15	16	Reserved (to J2 pin 7)
17	18	Head Select 1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction In

Table C-2 RD51 Disk Drive J2 Signal Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	Drive Selected
4	3	Reserved
6	5	Reserved
8	7	Reserved (to J1 pin 16)
	9, 10	Reserved
12	11	GND
	13	+MFM Write Data
	14	−MFM Write Data
16	15	GND
	17	+MFM Read Data
	18	−MFM Read Data
20	19	GND

Table C-3 RD51 Disk Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

C.2 RX50 DISKETTE DRIVE CONNECTOR PIN ASSIGNMENTS

The connector pin assignments for the RX50 diskette drive signal and power cables are listed in Tables C-4 and C-5.

Table C-4 RX50 Diskette Drive J1 Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
1	2	TK43L (controls write current level)
3	4	Reserved
5	6	Drive Select 3 L
7	8	Index L
9	10	Drive Select 0 L
11	12	Drive Select 1 L
13	14	Drive Select 2 L
15	16	Motor On L
17	18	Direction (head movement direction)
19	20	Step L (head movement distance)
21	22	Write Data L
23	24	Write Gate L
25	26	Track 0 L
27	28	Write Protect L
29	30	Read Data L
31	32	Reserved
33	34	Ready L

Table C-5 RX50 Diskette Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

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