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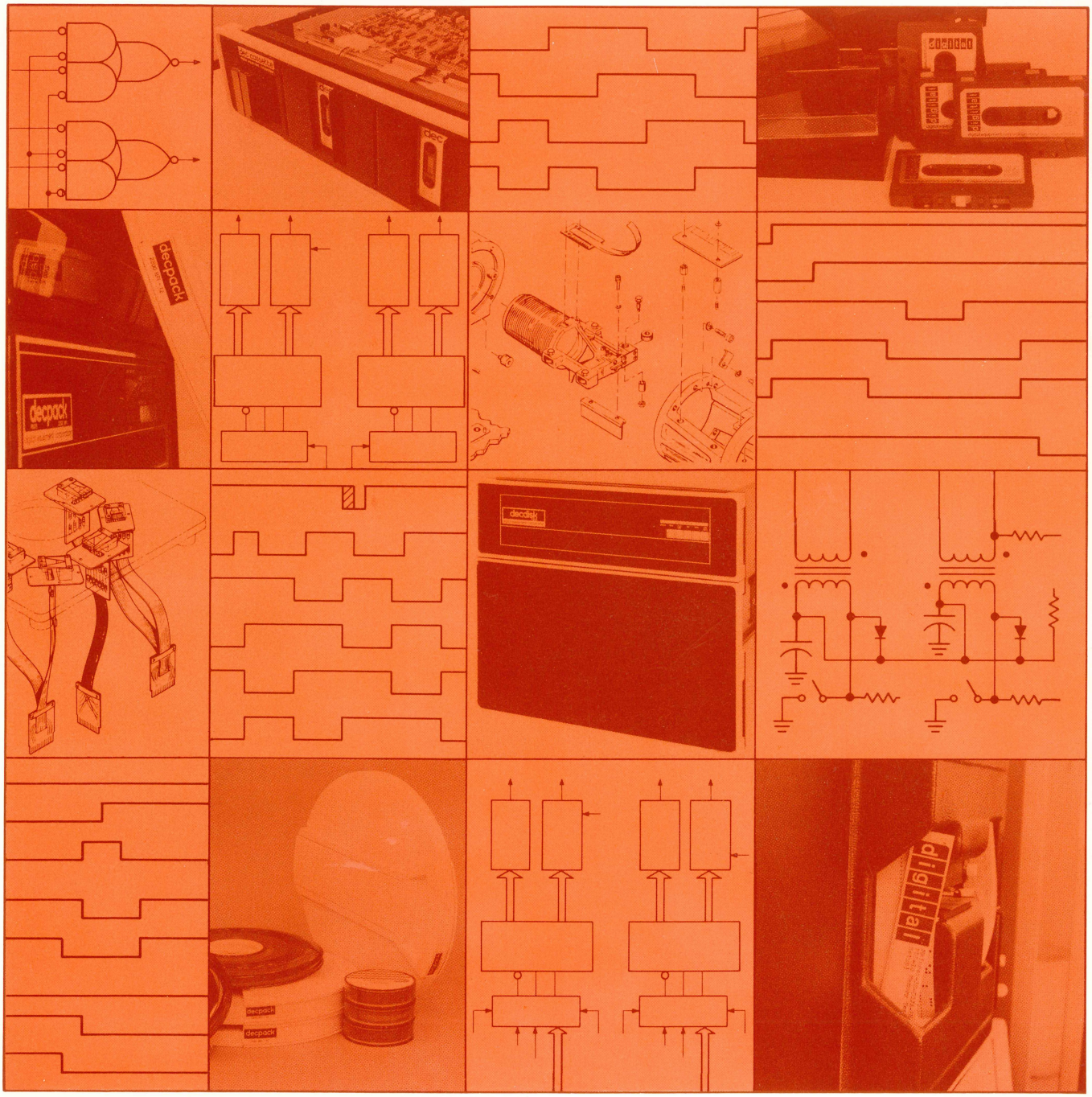
RP04 device control logic maintenance manual



digital equipment corporation · maynard, massachusetts

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EK-RP04-MM-001

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Preliminary, June 1974
1st Edition, November 1974
2nd Printing, January 1975

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual describes the Device Control Logic (DCL) incorporated in the RP04 Disk Drive. The RP04 is divided into two major functional parts (Figure 1-1):

1. The DCL which houses the necessary logic circuits to interpret and implement all commands executable by the RP04 and allows for access by two different controllers.

2. The DEC 733 Disk Storage Drive which houses the circuits for: rotating the disk pack, positioning the read/write heads at the addressed cylinder track and sector; and writing/reading bits on the disk pack surface.

1.1.1 System Compatibility

The DCL is capable of handling data transfers in either 16 or 18-bit format making the RP04 compatible with the PDP-11, PDP-15 and DECsystem-10. Each system has its own specialized controller that interfaces the RP04 with the related processor.

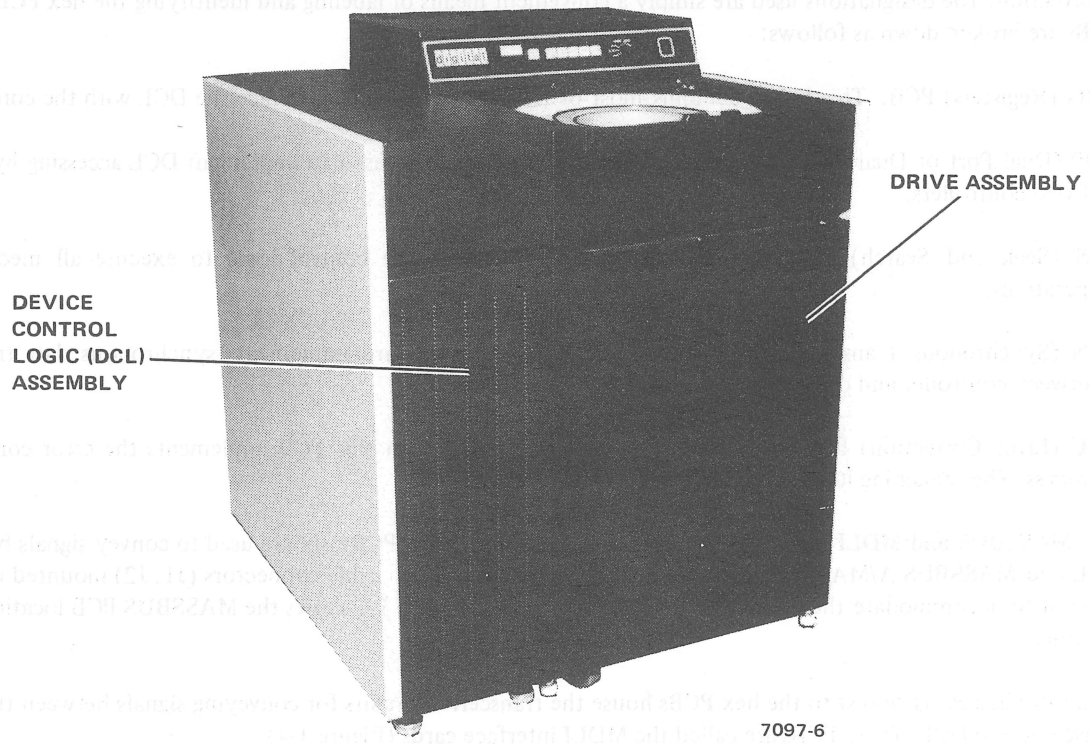


Figure 1-1 RP04 Drive and DCL Assemblies

1.2 PHYSICAL DESCRIPTION

The DCL itself is a 9-inch wide by 32-inch deep by 35-inch high unit that attaches at the left of the Drive assembly when the RP04 is viewed from the front (Figure 1-1). The DCL assembly is attached to the drive assembly by four 2-inch long 1/4 X 20 bolts. The DCL assembly also has its own casters for easy roll-away when disconnected from the Drive assembly. Levelers are attached to provide stability when the DCL is permanently installed.

Physically, the DCL is comprised of three main subassemblies: The Card Nest and Cable Assembly, the Power Supply, and the Power Monitor (Figures 1-2 and 1-3).

1.2.1 Card Nest and Cable Assembly

The card nest and cable assembly is accessible through the rear of the unit by lifting the entire rear cover panel and drawing it free of the assembly. This exposes the two fasteners that are used to hold the card nest and cable assembly (Figure 1-2) in an upright position. Then access to the printed circuit cards is gained by:

1. Loosening the two fastener screws and carefully swinging the assembly outboard until it rests in a horizontal position.

2. Loosening the two fastener screws (Figure 1-3) on the air flow cover and swinging the cover to the vertical position. This exposes the hex and interface printed circuit boards (PCB's).

All control logic circuits are housed on the hex PCBs that extend the full length of the card nest and cable assembly. The PCBs that interface with the drive assembly and the two controllers are the smaller PCBs situated to the left of the assembly when viewed from the top. Figure 1-4 shows the layout of the PCBs within the card nest and cable assembly.

1.2.1.1 Hex Printed Circuit Boards – There are five hex PCBs. Designations for these cards are based on the principal control circuits housed on a particular PCB. For example, the Error Correction (EC) PCB is so designated because there are more ICs used for this function than for any other control function on this particular board. This does not mean, however, that other ICs on this same PCB are not used for control functions completely unrelated to error correction. The designations used are simply a convenient means of labeling and identifying the hex PCB's. The hex PCBs are broken down as follows:

RG (Registers) PCB: This board contains most of the registers used to interface the DCL with the controller.

DP (Dual Port or Dual Controller) PCB: This card contains logic used to implement DCL accessing by either of two controllers.

SS (Seek and Search) PCB: This board primarily includes the control logic to execute all mechanical operations.

SN (Synchronous Transfer) PCB: Much of the logic on this board implements synchronous data transfers between controller and disk pack.

EC (Error Correction) PCB: Approximately half of the logic on this PCB implements the error correction process. The remaining logic is used for error registers and timing.

1.2.1.2 MASSBUS and MDLI Interface PCBs – Of the eight interface PCBs, six are used to convey signals between the DCL and MASSBUS A/MASSBUS B. Each of these six PCBs has two cable connectors (J1, J2) mounted directly on the card to accommodate the appropriate MASSBUS cables. Figure 1-4 shows the MASSBUS PCB locations and designations.

The two interface cards closest to the hex PCBs house the transceiver circuits for conveying signals between the DEC 733 Drive and the DCL. These PCBs are called the MDLI interface cards (Figure 1-4).

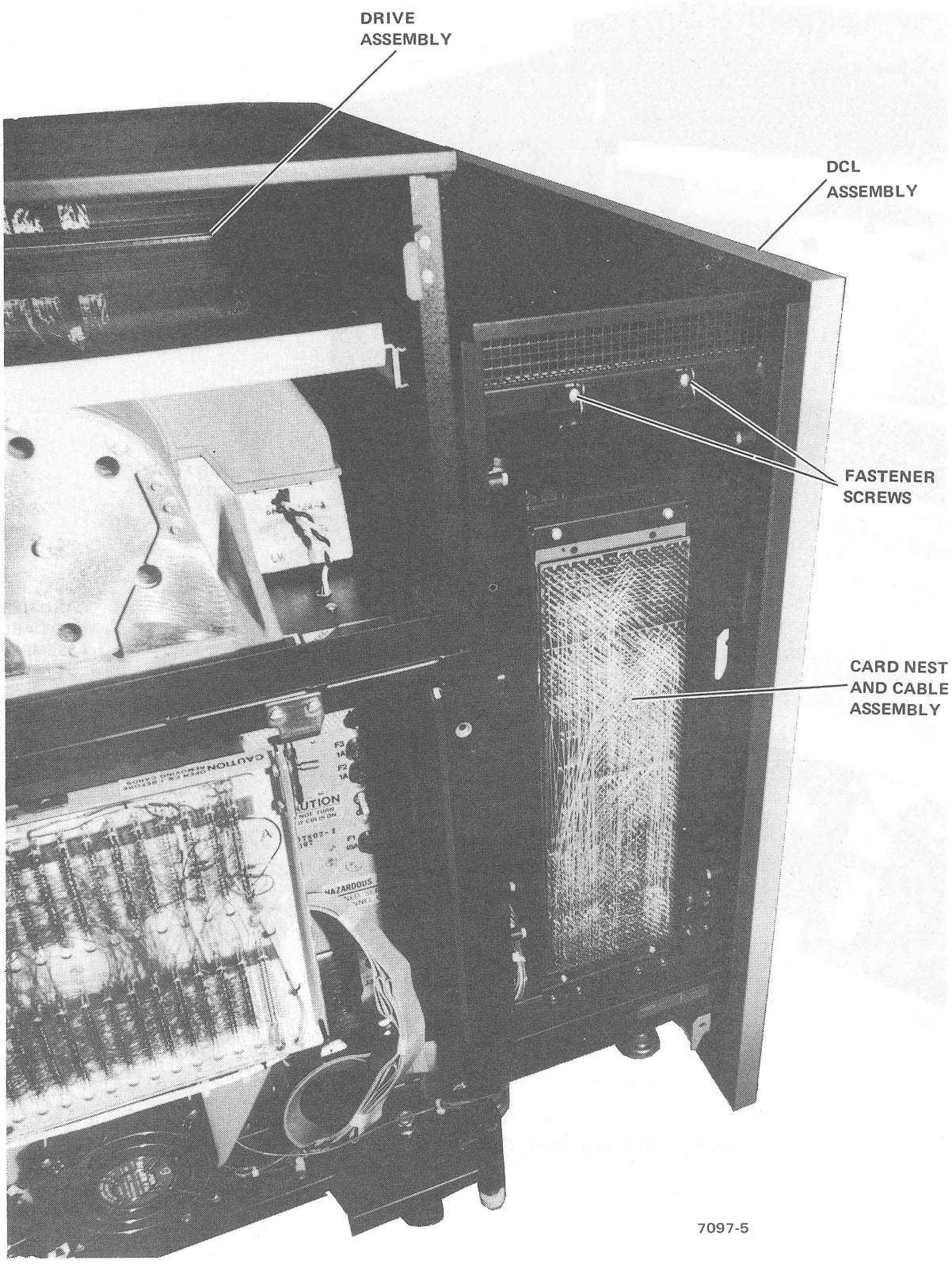


Figure 1-2 RP04 Drive and DCL Assemblies Back View, Rear Panels Removed

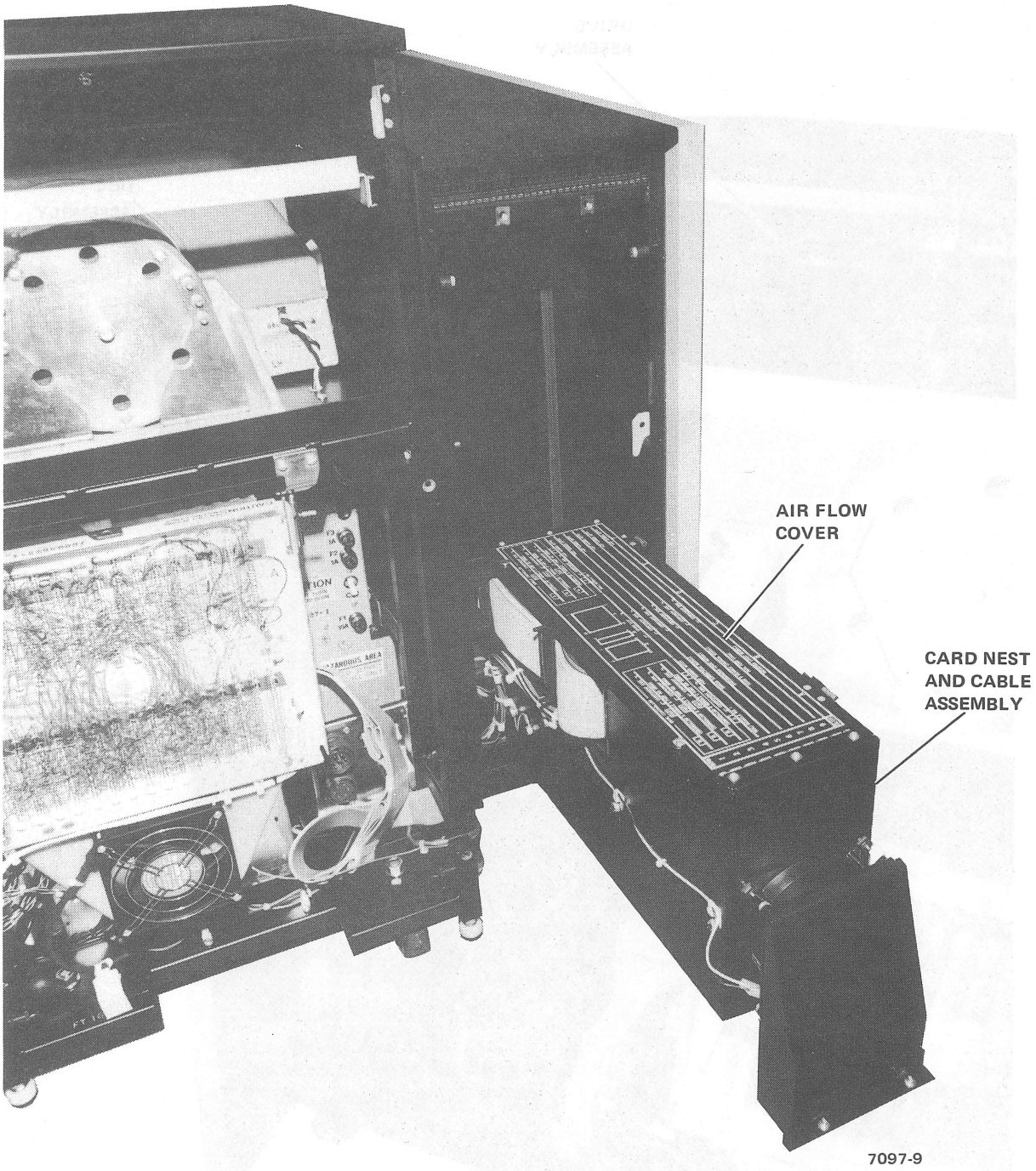


Figure 1-3 DCL Rear View, Card Nest and Cable Assembly Extended

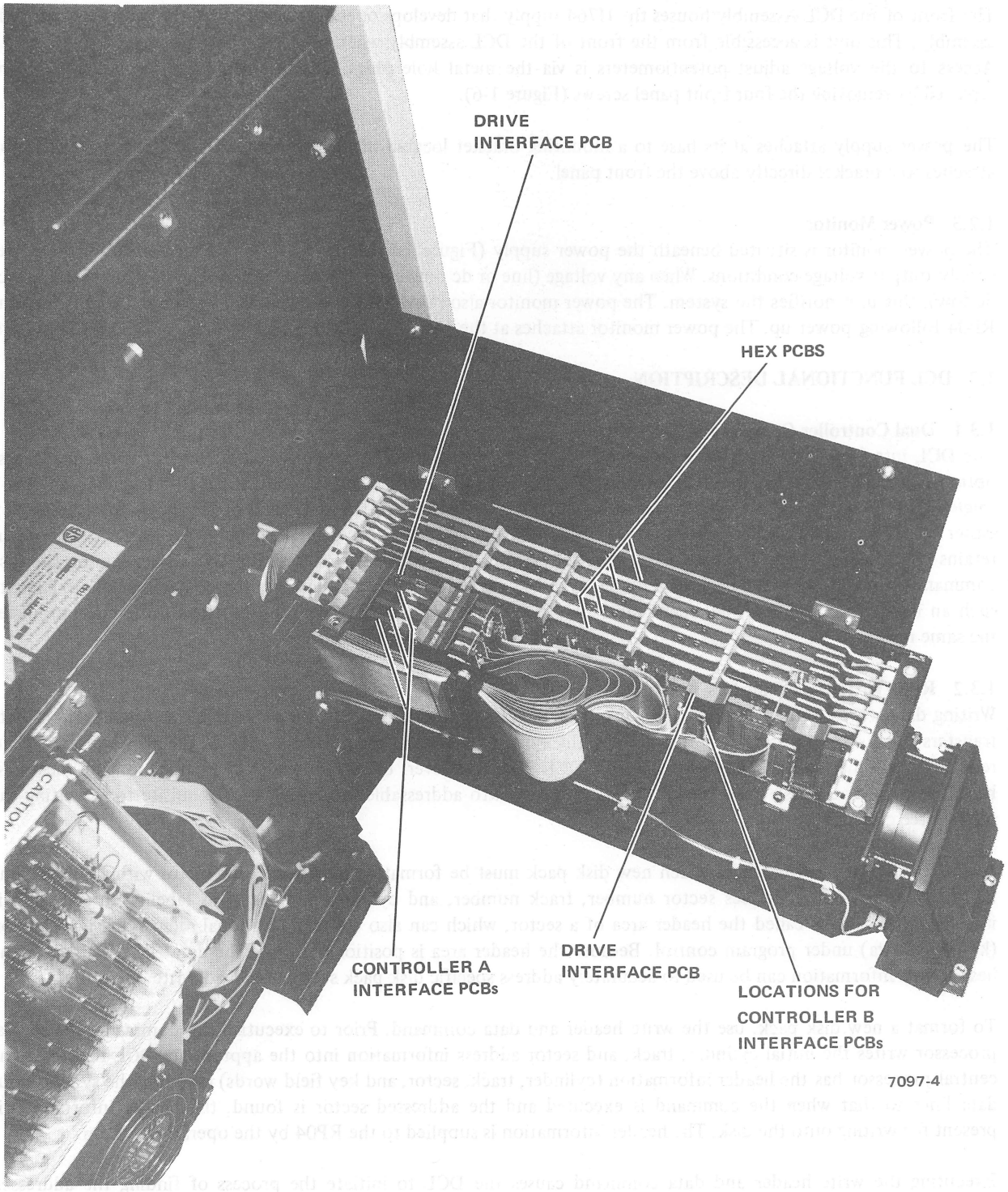


Figure 1-4 Card Nest and Cable Assembly PCB Layout

1.2.2 Power Supply

The front of the DCL Assembly houses the H764 supply that develops operating voltages for the card nest and cable assembly. This unit is accessible from the front of the DCL assembly when the front panel is removed (Figure 1-5). Access to the voltage adjust potentiometers is via the metal hole plugs. The power supply components can be replaced by removing the four front panel screws (Figure 1-6).

The power supply attaches at its base to a mounting bracket located in the center of the DCL assembly. The top attaches to a bracket directly above the front panel.

1.2.3 Power Monitor

The power monitor is situated beneath the power supply (Figure 1-5) and provides a constant check of the power supply output voltage conditions. When any voltage (line or dc output) strays from the required tolerance (ac low or dc low), this unit notifies the system. The power monitor also provides the "power OK" signal used to initialize the RP04 following power up. The power monitor attaches at the base of the DCL assembly with four mounting screws.

1.3 DCL FUNCTIONAL DESCRIPTION

1.3.1 Dual Controller Operation

The DCL interface logic is designed to permit access by two different controllers (i.e., provided that the dual access option is installed). The setting of the CONTROLLER SELECT switch on the control panel determines whether a single or both controllers are allowed to access the RP04. When set to the A/B position, it allows for accessing by either controller on a "first-come, first-serve" basis. Once a controller has gained access in the dual access mode, it retains control until it has completed its operation. Normally, a controller releases the DCL by executing a release command to place the RP04 back in a device available status. However, if the accessing controller fails to execute such an instruction within a one-second time span (i.e., following the last operation), a timeout function produces the same result.

1.3.2 Read/Write Data Transfers

Writing data words onto the RP04 disk pack or reading data words from the disk pack are termed synchronous data transfers since such transfers are effected over the synchronous data bus portion of the MASSBUS interface. Four read/write commands are implemented by the DCL logic. However, the write header and data command must first be used to format a disk pack (divide the disk surface into addressable sectors) as a prerequisite to executing the other three commands.

1.3.2.1 Disk Pack Formatting – Each new disk pack must be formatted to provide each sector with an identifying indicator or label that defines sector number, track number, and cylinder number. This labeling information is inserted into what is called the header area of a sector, which can also contain additional identifying information (key field data) under program control. Because the header area is positioned before the data field of a sector, the header area information can be used to accurately address specific disk pack sectors for read/write operation.

To format a new disk pack, use the write header and data command. Prior to executing this command, the central processor writes the initial cylinder, track, and sector address information into the appropriate DCL registers. The central processor has the header information (cylinder, track, sector, and key field words) ready on the synchronous data lines so that when the command is executed and the addressed sector is found, the header information is present for writing onto the disk. The header information is supplied to the RP04 by the operating system.

Executing the write header and data command causes the DCL to initiate the process of finding the addressed cylinder, track, and sector. When all are found, the DCL informs the controller to send the header information. At this time, the DCL also initiates the sequence for serially writing each header word onto the disk surface. In this way, header information is introduced onto an addressed sector.

The write header and data command also allows for writing data words beginning at a fixed time following the header. The area where data words are written is called the data field.

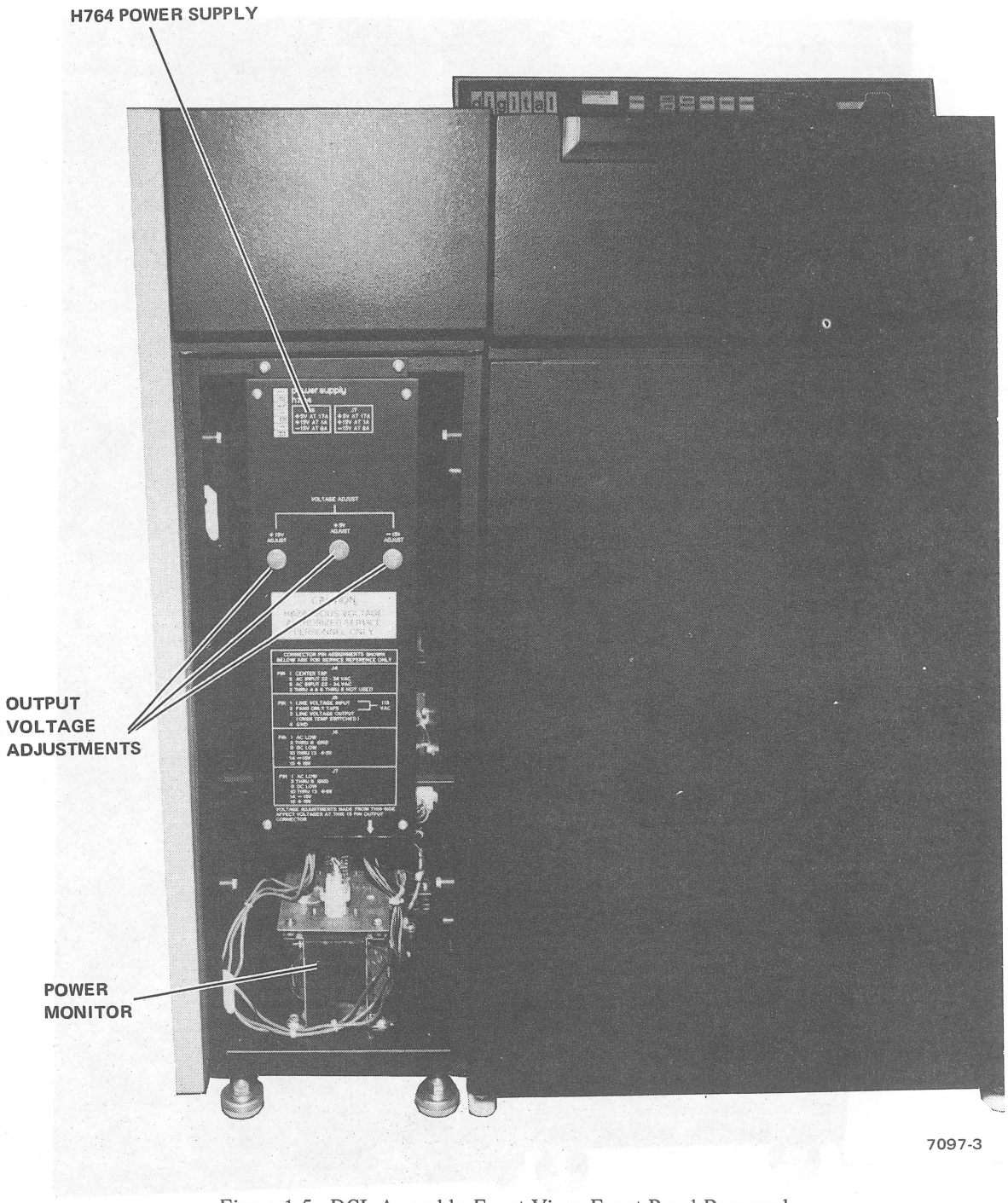


Figure 1-5 DCL Assembly Front View, Front Panel Removed

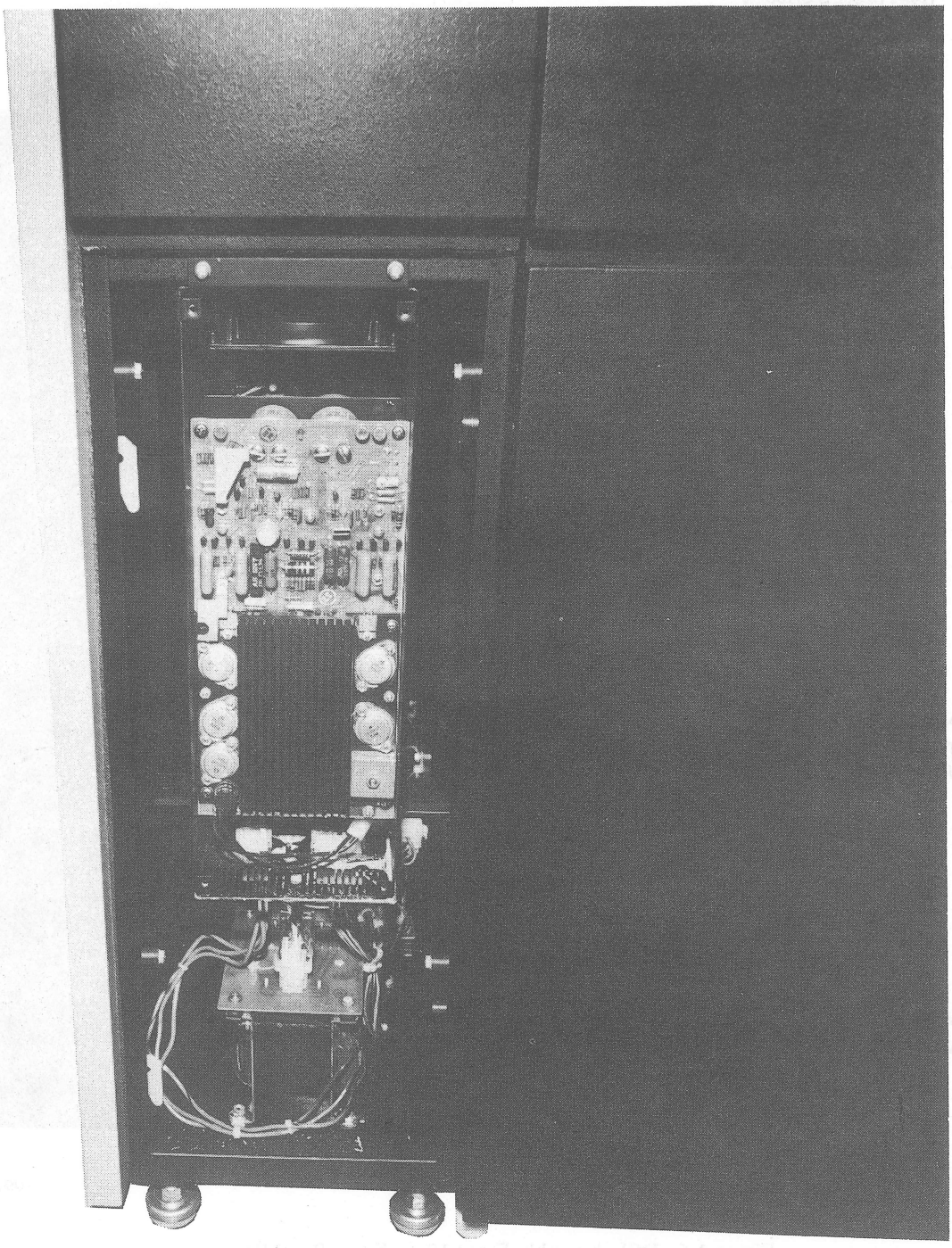


Figure 1-6 DCL Assembly Power Supply, Front Panel Removed

1.3.2.2 Other Read/Write Commands – The DCL interprets and executes three other commands to effect read/write data transfers. For each of these commands, the DCL makes proper identification of the header prior to initiating the transfer process. The technique for header identification is to compare the cylinder, sector, and track addresses of the header against those supplied prior to the read/write command initiation. Failure to detect a matchup in all three addresses results in the DCL setting a header compare error bit that is eventually sampled by the central processor.

A breakdown of the remaining read/write commands and their functions is given below:

Write data command: This command is used to write data words into the data field of an addressed sector. The DCL executes this command by first finding and identifying the addressed sector and then initiating the write transfer into the data field of that sector. The command can be used for an extended (multi-sector) write operation in that the DCL continues to write into the data fields of successive sectors for as long as the RUN line from the controller is asserted.

Read Header and Data Command: This command reads the header and data fields of an addressed sector and sends both to the central processor via the controller. Reading the header information may prove useful in analyzing faults after the DCL has indicated a header compare error on a particular sector. By reading the header information (cylinder, track and sector address) and comparing it against that supplied with the read header and data command, the CPU is able to determine exactly what header (format) information is in error.

Read Command: This command is used to read the data field of an addressed sector. As is the case with all read/write commands, the CPU must load the desired cylinder address and desired sector/track registers prior to executing the command. Once the addressed sector has been found, the DCL reads consecutive sectors for as long as the RUN line from the controller is asserted.

1.3.3 Disk Addressing Techniques and Related Commands

The DCL executes two commands that are used solely to locate addressed areas of the disk pack – seek and search. The functions carried out by these commands are broken down as follows:

Seek Command: This causes the drive read/write heads to be positioned over the addressed cylinder. Cylinder and track information is supplied from the central processor prior to executing the command. When the heads are correctly positioned, the drive informs the DCL which in turn asserts the ATTENTION line to the controller.

Read/Write commands may also require positioning the read/write heads at the addressed cylinder. This activity is referred to as an "implied seek", since the seek command is not used and the ATTENTION line is not asserted.

Search Command: The search command is used as a method of optimizing the pack revolution time. When the DCL detects the addressed sector, it asserts the ATTENTION line to the controller.

1.3.4 DCL Interface Registers

The DCL has 16 interface registers that can be accessed by the controller; they fall into the following general categories:

Control – The control register receives the command (read, write, seek, etc.) codes from the controller. The DCL control logic samples the content of this register and initiates the appropriate execution sequence.

Status – The bits of this register supply the central processor with DCL and Drive status information.

Maintenance – The maintenance register is used by diagnostic programs to initiate various maintenance functions.

Error Information – Three registers are provided to indicate error status within both the DCL and the Drive.

Address Data – These are five registers that are associated with disk addressing:

- Desired Cylinder Address Register
- Current Cylinder Address Register
- Desired Sector/Track Register
- Offset Register, used to offset the disk read/write heads in fixed increments.
- Look Ahead Register, can be used to subdivide the data field of a sector.

System Housekeeping – There are two registers used for system housekeeping, i.e., a drive type register and a serial number register.

Attention Summary Pseudo Register – This is a one bit register used to indicate that the RP04 requires the attention of the system. In one sense it can be considered an interrupt line.

Error Correction – There are two registers used to convey error correction information to the central processor.

1.3.5 Error Correction Capability

The DCL is equipped with error correction logic, which (provided it is not inhibited by the system) becomes operative whenever an error is detected during a read operation. Once activated, the error correction circuits proceed to locate the area in the sector data field where the error occurred. When this area is detected, the DCL makes available the following information to the operating system:

1. Error correction code burst pattern.
2. Position with the data field where the error occurred.

Given this information, the software can determine the exact bits in error and correct them.

1.4 APPLICABLE INSTRUCTION MANUALS

Instruction manuals bearing upon use of the RP04 depends on whether the device is configured in a PDP-11 or PDP-10 system environment (or both). When used with the PDP-11, applicable instruction manuals are:

- RP04 Disk Drive Installation Manual
- Model 733 DEC Disk Storage Drive Operation, Service and Diagrams Manual
- RJP04 Moving Head Disk Drive Maintenance Manual
- RH11 Controller Instruction Manual
- RP04 DCL Print Set

When the RP04 is used with the PDP-10 system, related handbooks are:

- RP04 Disk Drive Installation Manual
- Model 733 DEC Disk Storage Drive Operation, Service and Diagrams Manual

- RH10 Controller Instruction Manual
- RP04 DCL Print Set

1.5 SPECIFICATIONS

Data Format Option:

20 sectors per data track (256 18-bit words per sector data field).
22 sectors per data track (256 16-bit words per sector data field).

Error Handling:

Error Detection and Correction Capability.

Interface Characteristics:

MASSBUS Controller to device interface Dual Controller capability.

System Compatibility:

Can be used in PDP-11 or PDP-10 system configuration.

Data Transfer Modes:

Single sector or multisector (spiral or extended read/write) transfers.

Operating Temp. Ranges:

15° C minimum to 32° C maximum.

Humidity Range:

20% minimum to 80% maximum.

Dimensions:

9-in. wide by 35-in. high by 32-in. deep.

Weight (DCL only):

100 lb (approx).

Operating Voltages DCL only:

+5 Vdc
-15 Vdc
+15 Vdc

CHAPTER 2
THEORY OF OPERATION

2.1 DEVICE CONTROL LOGIC, SIMPLIFIED BLOCK DIAGRAM DISCUSSION

Figure 2-1 is a simplified block diagram of the DCL indicating the major functional areas involved in accessing the RP04 (asynchronous operation) and the implementation of synchronous data transfers. This diagram also shows the duality of the Massbus interface (the DCL can be accessed by either of two controllers).

2.1.1 Asynchronous Transfers and Control Command Execution

2.1.1.1 Dual Control Operation – Asynchronous transfers between DCL and controller take place over the Massbus control lines and occur when the controller writes or reads a register within the DCL. Between controllers, access to the DCL registers is on a first-come-first-serve basis. Once the DCL is selected by a controller, the enabling signals (indicated in Figure 2-1 as CONTROLLER SELECT) permit transfers only to/from that controller.

2.1.1.2 Register Select Decoding and Registers – Register addressing is also an integral part of the asynchronous transfer process. The address of the register to be accessed is sent over the Massbus register select lines and multiplexed in the same manner as the control line signals. The output of the register select multiplexer is applied to register select decode logic which decodes the five bit address and then generates an enabling signal to the proper register for the register read or register write operation.

The DCL has 16 Massbus drive registers, all of which are readable by the controller. About half can also be written into. The DCL registers fall into the following categories:

Control Register – This read/write register receives all command codes from the controller and stores the command for the duration required to execute the command.

Status Register – This read only register provides status information to the controller regarding the state of the drive and regarding conditions within the DCL itself.

Error Registers – The DCL has three read/write error registers to convey Drive and DCL error information to the controller.

Maintenance Register – A read/write maintenance register that can be used for diagnostic purposes is provided.

Attention Summary Pseudo Register – There are two of these read/write registers (one for each controller) if the dual controller configuration is used.

Disk Addressing Registers – The DCL has five registers that are involved in accessing data from the disk. Three are read/write; two are read only.

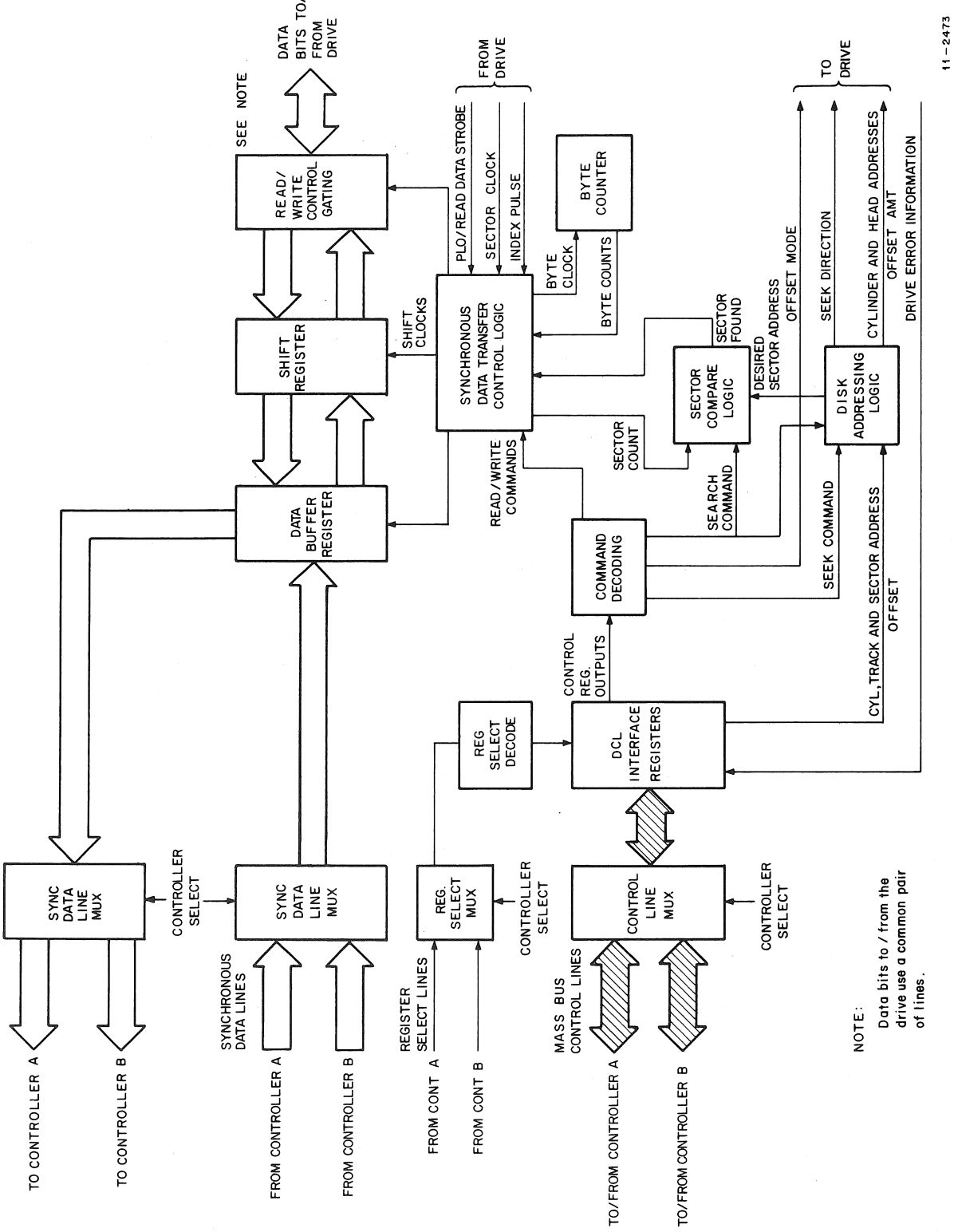


Figure 2-1 Device Control Logic, Simplified Block Diagram

Serial No. and Drive Type Registers – These two read only registers are used for system housekeeping.

ECC Position and Pattern Registers – These two read only registers are used for error correction code handling.

2.1.1.3 **Command Decoding** – The command decoding logic interprets the outputs of the control register to determine which of the 17 possible commands is to be executed. Among these commands are the read/write commands (discussed later) that initiate synchronous data transfers. The seek command (Figure 2-1) is used to move the disk read/write heads between cylinders.

The offset mode is used to offset the read/write heads from the track centerline. The search command can be used to detect a particular sector of a track. A more comprehensive breakdown of the command repertoire is given later in this section.

2.1.2 Synchronous Data Transfers

Once the RP04 has been connected to a controller and a read/write command has been decoded, synchronous data transfers are implemented via the four blocks shown at the top of Figure 2-1. Controller A or B (having earlier accessed the DCL and therefore having control) transmits or receives data via the following circuit groups:

Massbus Synchronous Data Line Multiplexer – This logic steers 16/18-bit data words (refer to format bit in offset register) to or from the controller having access to the DCL. Once a controller has gained access, enabling signals (indicated here as CONTROLLER SELECT) are generated that permit transfers to/from only that controller.

Data Buffer Register – This register buffers 16/18-bit data words in one of two ways depending on transfer mode (write/read):

- During write operations this register accepts the data words from the multiplexer and presents them to the shift register.

- During read operations this register accepts data words from the shift register and presents them to the Massbus.

The time at which the data buffer register accepts a word is governed by the synchronous data transfer control logic. This logic takes into account such factors as the number of shift clocks required to empty/load the shift register before loading a new word into the data buffer register.

Shift Register – The shift register fulfills the parallel-to-serial conversion requirement during write operations and the serial-to-parallel conversion requirement during read operations. These conversions are accomplished as follows:

- Write operation: In this case, the shift register accepts 16/18-bit words in parallel from the data buffer register; then transfers the word a-bit-at-a-time (via the least significant bit position) until all 16/18 bits have been emptied from the shift register and written onto the disk. At this point the next data word is parallel loaded into the shift register.

- Read operation: In this case, the shift register accepts data words a-bit-at-a-time from the disk for application at the most significant bit position. When 16/18 shifts have been accomplished on the incoming data, a complete word is contained in the shift register. It is then presented in parallel to the data buffer register.

The shift pulses used to clock bits to/from the shift register are supplied from the synchronous data transfer control logic. The number of shift clocks supplied to fully shift a word depends on whether 16- or 18-bit words are being transferred.

Read/Write Gating Control Logic – This logic simply gates data from/to the disk depending on whether it is a read or a write operation. It also governs the length of the registers for 16- or 18-bit mode operation. If the DCL is in the 18-bit mode, two high order stages of the buffer and shift registers are enabled.

2.1.2.1 Synchronous Data Transfer Commands – The DCL interprets six basic read/write commands for transferring data words via the synchronous data path. These commands, *and only these commands,* activate the synchronous data transfer control logic to implement the data transfers. The six commands are:

Write Header and Data – Used for formatting each sector on the disk. Formatting consists of dividing each sector into fields to insert gaps of all zeros, control words (header), and data words (data field). This is necessary so that the DCL can address specific sectors of a track when using the other data transfer commands. The makeup and structure of the sector format are discussed in a later paragraph of this chapter.

Write Data – Used to write data into the data field of a sector. The address information is specified prior to executing the write command. The DCL uses this address information to find the correct sector and then initiates the write data transfer.

Read Header and Data – Executed to retrieve the header information as well as the contents of the data field of a sector. Address information must be supplied prior to executing the command so that the DCL can locate the proper sector and implement the read transfer.

Read Data Command – Similar to the read header and data command except that only the contents of the data field are sent to the controller. Again, proper header identification must be made prior to reading the data field words from the disk.

Write Check Header and Data.

Write Check Data.

2.1.2.2 Synchronous Data Transfer Control Logic – This logic carries out all control operations inherent in executing the read/write commands for transferring data from/to the disk. The paragraphs that follow describe some of the more salient control operations and the reasons for them.

- Read/Write Command Interpretation – The synchronous data transfer control logic must recognize the type of read/write command being executed to initiate the proper control sequence. That is, the control sequence employed when formatting a disk through use of the write header and data command is altogether different from that used when executing a read data command. Also, the clock signal used to develop shift clock pulses differs for the write and read modes. Furthermore, the proper control signals must be sent to the read/write control gating in keeping with the type of operation in progress.

- Clock (PLO/Read Data Strobe) Sector Clock and Index Pulses – The DCL synchronous data transfer control logic receives clock, sector, and index pulses from the drive. The clock pulse is derived from one of two source signals depending on read/write mode. When reading, the read data strobe signal is used to develop the shift clock. In write operations, the phase locked oscillator (PLO) signal is used to develop the shift clock.

  The sector clock is used to keep track of and to update the sector count as the disk revolves beneath the read/write heads. The sector count is important to the sector addressing technique employed by the DCL. There can be either 20 or 22 sectors per track depending on word length (i.e., 18-bit or 16-bit).

The index pulse is used to signify the beginning of each revolution.

- Shift Clock Pulse Uses – Since each shift clock pulse represents a serial bit transfer time, it is used for counting as well as shifting data bits. The four uses of the shift clock pulse are listed below.

  1. Clocks bit serially to/from the shift register for DCL to disk transfers.

  2. Counts the number of bits shifted to determine when the shift register has been emptied or filled. This is necessary to inform the controller when to take or send a word.

  3. Generates a byte clock so that the DCL is aware of what byte and word of a sector is passing beneath the disk read/write heads.

  4. Serves as a clocking source in cyclic redundancy checking.

- Byte Count Development – The synchronous data transfer control logic employs a byte counter to keep track of what part of a sector is being accessed. As stated earlier, each sector is broken up into fields during the formatting process. Each field must contain the same number of bytes when comparing one sector against another. Also, each field must begin at the proper byte count with respect to the sector pulse which defines the start of a sector. The synchronous data transfer control logic uses the count from the byte counter to determine when to read/write sync bytes, header words, and the data words that make up the data field of a sector.

- Sync Clock Generation – The synchronous data transfer control logic also generates the sync clock signals to the controller that must be issued to effect each word transfer. During a write operation, the DCL issues the sync clock (telling the controller to send another word) after the shift register has been emptied and a word is parallel loaded into the shift register. During read operations, the DCL issues the sync clock (telling the controller to take another word) after the shift register has been filled and the word is loaded into the data buffer register.

2.1.3 Disk Addressing Logic

The disk addressing logic actually includes a number of the registers within the register block on Figure 2-1. However, the disk addressing logic and sector compare logic are shown as separate blocks on the diagram to distinguish them as functions and to indicate their relationship to the seek and search commands respectively.

2.1.3.1 Cylinder/Track Addressing (Seek) – To select an addressed cylinder, the DCL and Drive must execute a seek, which means that the disk read/write heads must be mechanically moved to the desired cylinder address. The DCL employs a desired cylinder register (9 bits) to store the new cylinder address and a current cylinder address register (9 bits) to store the current position of the read/write heads. When the contents of both these registers is the same, no positioning of the read/write head (seek action) is required. Any change in the contents of the desired cylinder address register initiates a subtraction process that results in the DCL sending direction and magnitude information to the Drive. This information is, in turn, used by the Drive to carry out a seek operation. At the conclusion of a seek (meaning that the heads have been positioned at the desired cylinder), the desired cylinder address (now the current address) is entered into the current cylinder address register. At this time, both registers contain the same address. Following this, any updating or change of the contents of the desired cylinder address register results in the DCL and Drive executing a new seek. Updating the contents of desired cylinder address register can occur in any of the following ways:

- The controller executes a seek command. In this case, the desired cylinder address is loaded with the new desired cylinder address before the seek command code is loaded into the control register.

- The controller executes a read/write command having previously loaded a new cylinder address into the desired cylinder address register. This type of seek is called an "implied seek", because a seek command is not being executed, yet a seek operation must take place before the data transfer can start.

- The desired cylinder address is incremented following the last track of a cylinder when the DCL is executing an extended read/write operation. This is called a "mid-transfer" seek.

- A search command is executed and the previously loaded desired cylinder address differs from the current cylinder address.

The DCL disk addressing circuits employ subtraction logic using the outputs of both the desired cylinder address (DCA) register and current cylinder address (CCA) register to develop difference for the Drive. The cylinder difference (magnitude) of seek is generated by subtracting the contents of the CCA from the contents of the DCA. The disk addressing logic also supplies a seek direction signal to the Drive, informing it as to which way the read/write heads must be moved for the new cylinder address.

Track addressing is effective via a five bit portion of the desired sector/track address register and selects the desired read/write head of the drive.

2.1.3.2 Sector Addressing – New sector addresses accompanying operating system commands are inserted into a five bit portion of the desired sector/track register. This may be done when the operating system executes a search or any read/write command.

The DCL employs a sector counter (part of the synchronous data transfer control logic) to maintain synchronization between the DCL sector timing and the actual disk revolution in relation to the read/write heads. When the sector count matches the contents of the five bit sector address (in the desired sector/track register), the sector found condition occurs.

All read/write commands have desired sector addresses accompanying them. When the sector found condition occurs, it means that the synchronous data transfer control logic can initiate the control sequence for the read/write transfer.

Clearing the sector counter occurs once each revolution on assertion of the index signal from the Drive.

2.2 MASSBUS AND MDLI (DRIVE) INTERFACE SIGNALS

The interface signals conveying control signals and data words from the DCL to the Massbus and from the DCL to the Drive are shown on Figure 2-2. These signals and their purposes are described in subsequent paragraphs.

2.2.1 Massbus Interface Signals

Individual Massbus signal lines and signal group lines connecting the controller and DCL are described below:

1. SYNCHRONOUS DATA AND PARITY (19) LINES – These lines convey 16-bit or 18-bit data and an associated parity bit. The synchronous data lines are bidirectional and employ odd parity. Data is transmitted synchronously using the sync clock signal supplied from the DCL and the write clock signal generated by the controller.

2. SYNC CLOCK – Developed by the DCL during read/write data transfers to inform the controller to:

    - Accept the data on the synchronous data lines during read operations. The controller accepts the data on the negation of the SYNC CLOCK signal and the DCL changes the data on the assertion of the SYNC CLOCK signal.

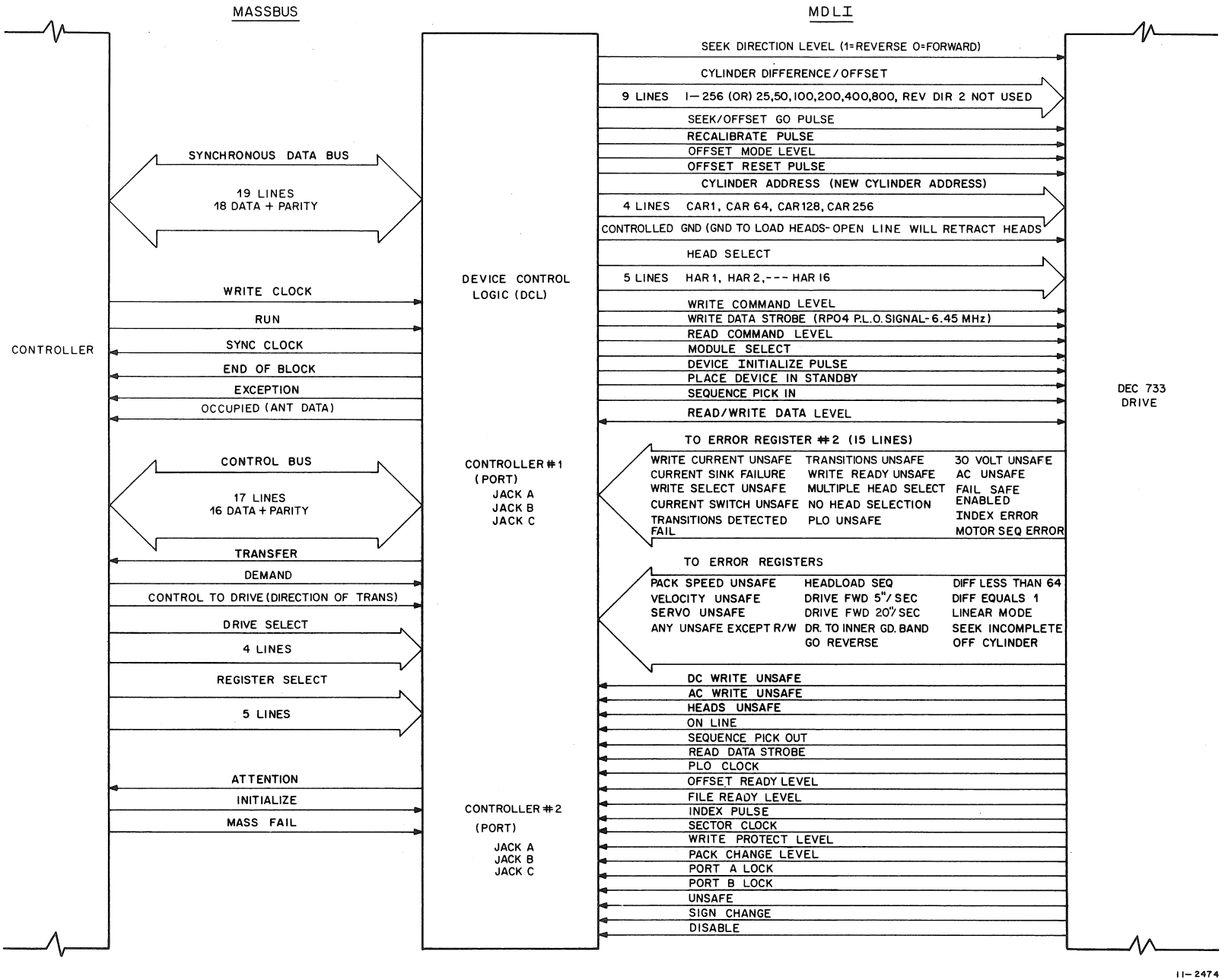


Figure 2-2 Massbus and MDLI (Drive) Interface Signal

- Send the WRITE CLOCK during write operations. This informs the DCL to take the data word on the synchronous data bus lines.

3. WRITE CLOCK – This signal is echoed by the controller in response to the SYNC CLOCK during write operations. On the assertion of the WRITE CLOCK the DCL accepts the data word. On the negation of this signal, the controller changes the data on the data bus lines.

4. RUN LINE – After a data transfer command has been written into the control register of the DCL, the DCL connects to the synchronous data bus. The controller then asserts the RUN line to initiate the function. At the end of each sector, on the trailing edge of the EBL (end-of-block) pulse, RUN is sampled by the DCL. If it is still asserted, the function continues for the next sector; if it is negated, the function is terminated.

5. END-OF-BLOCK (EBL) – This signal is asserted by the DCL at the end of each sector (after the last sync clock/pulse and the two ECC words). For certain error conditions where it is necessary to terminate operations immediately, EBL is asserted prior to the normal time for the last SYNC CLOCK. The data transfer is terminated prior to the end of the sector in this case.

6. EXCEPTION (EXC) – This signal is asserted when an abnormal condition occurs in the DCL. The DCL asserts this signal to indicate an error during a data transfer command. EXCEPTION is asserted at or prior to assertion of EBL and is negated at the negation of EBL.

7. CONTROL BUS – The parallel control and status path consists of a 16-bit parallel data path and an associated parity bit. The control and status lines are bidirectional and employ odd parity.

8. DRIVE SELECT – These four lines transmit a 4-bit binary code from the controller to select a particular DCL/Drive. The DCL responds when the (unit) select number in the DCL corresponds to the transmitted binary code.

9. CONTROLLER-TO-DRIVE – This signal is generated by the controller and indicates the direction in which control and status information is to be transferred. For a controller-to-Drive transfer, the controller asserts this signal. For a Drive-to-controller transfer, this signal is negated by the controller.

10. REGISTER SELECT – These five lines transmit a 5-bit binary code from the controller to the DCL. The binary code selects one of the DCL registers.

11. DEMAND – This signal is asserted by the controller to indicate that a transfer is to take place on the control bus. For a controller-to-DCL transfer, DEMAND is asserted by the controller when control line information is present and settled on the control bus. For a DCL-to-controller transfer, DEMAND is asserted by the controller to request data and is negated when the data has been strobed off the control bus.

12. TRANSFER – This signal is asserted by the DCL in response to DEMAND. For a controller-to-DCL transfer, TRANSFER is asserted when the data is strobed off of the control lines and is negated when DEMAND is negated. For a DCL-to-controller transfer, TRANSFER is asserted after the data is asserted on the control bus and negated when the negation of DEMAND is received.

13. ATTENTION – This line is shared by all eight DCL's attached to a controller; it may be asserted by any DCL as a result of an abnormal condition or status change in the DCL. An ATA status bit in each DCL is set whenever that Drive is asserting the ATTN line.

This signal may be asserted for any of these reasons:

- An error, while no command is being executed (asserted immediately).
- At the completion of a command if an error occurred during execution of the command.
- Completion of a non-data transfer command (such as SEARCH).

The ATTENTION bit in a DCL may be cleared by the following actions:

- Asserting INITIALIZE on the Massbus (affects all eight Drives).
- Writing a 1 into the Attention Summary register (in the bit position corresponding to the address of the asserting Drive). This clears the ATTENTION bit; however, it does not clear the error.
- Writing a valid command (with the GO bit set) into the DCL Control register when no composite error is preset. Note that clearing the ATTENTION bit of one DCL does not always cause the ATTN line to be negated because other DCLs may also be asserting the line.

14. INITIALIZE – This signal is asserted by the controller to perform a system reset of all DCLs. When a DCL receives the INITIALIZE pulse, it immediately aborts the execution of any current command.

15. MASS FAIL – When asserted, this signal indicates that a power-fail condition has occurred in the controller.

2.2.2 MDLI (DRIVE) Interface Signals

Control and data lines used to transfer signals between the DCL and Drive are also on Figure 2-2. These signals are described in the handbook for the Drive. Some of the more fundamental signals are shown on Figure 2-1 and described in the paragraphs covering this illustration.

2.3 COMMAND REPERTOIRE

The subsequent paragraphs describe the reaction of the DCL to control commands, as well as the range and type of commands executable within the DCL itself.

2.3.1 Control Commands

Execution of a control command by the controller causes transfer of control/status information over the 17 control bus lines (Figure 2-2).

Execution of a control command by the controller always results in the reading or writing of an addressed DCL register. Consequently, a register select code, supplied over the five register select lines, must always be present when the controller executes a command code. Further, the DCL device code must also be supplied over the drive select lines. When the register selected is the control register and the controller writes into this register (i.e., with the low order bit, called the GO bit, set), one of the 17 commands executable by the DCL is initiated.

A summary of the 16 registers that can be sampled and written into by the controller is listed as follows.

Register Name	Register Select Code (Octal)	Unibus Address** (Octal)
Control*	00	776700
Status*	01	776720
Error Register No. 1*	02	776714
Maintenance*	03	776724
Attention Summary*	04	776716
Desired Sector/Track Address*	05	776706
Look Ahead	07	776720
Drive Type	06	776726
Serial No.	14	776730
Offset*	11	776732
Desired Cylinder Address*	12	776734
Current Cylinder Address	13	776736
Error Register No. 2*	10	776740
Error Register No. 3*	15	776742
ECC Position	16	776744
ECC Pattern	17	776746

*Indicates register can also be written.

**Code conversion of two low order octal digits is accomplished by related controller.

2.3.2 Data Transfer Commands

The DCL executes the following data transfer commands when the related command code is written into the control register:

1. Write header and data (formatting), 63_8
2. Write data, 61_8
3. Read header and data, 73_8
4. Read data, 71_8
5. Write check header and data, 53_8. The decode of this command is ORed with that of the read header and data. As such the DCL executes the same control sequence.

6. Write check data 51_8. The decode of this command is ORed with that of the read command. Hence, the DCL treats it as a read command.

7. Search. The search command does not actually transfer data. However, it does inform the controller that the desired sector has been found, and consequently, the software can go ahead and initiate a data transfer. Its principal uses are in disk use optimization and rotational position sensing.

A brief description of the activities carried out by the DCL for each of these commands is given below:

- When formatting (write header and data command), the DCL writes all fields of a sector (including header field and data field) onto the disk and inserts each field in its proper position with respect to the sector pulse. (The sector pulse defines the start of a sector.)

- Write data. This command is used to write the 256-word data field of a sector. The DCL makes proper identification of the addressed cylinder track and sector by reading and verifying the header before beginning the write operation.

- Read Header and Data. When executing this command, both the header and data fields of a sector are sent to the controller. Proper identification of the sector only is required before the transfer is initiated.

- Read Data. In this case, the DCL sends only the data field of a sector. Again, proper header identification is made before beginning the transfer.

  Data transfer commands may include an implied seek if the desired cylinder address (accompanying the command) does not match the current cylinder address. When there is a difference between the desired cylinder address and the current cylinder address on execution of a data transfer command, the DCL executes a seek to position the disk read/write heads at the addressed cylinder. The DCL then searches the disk (on the addressed track) for the desired sector and when found, initiates the data transfer.

2.3.3 Housekeeping Commands

The housekeeping commands used by the DCL and their individual purposes are as follows:

1. NO-OP. This command does nothing and is used as a filler command by the software.

2. DRIVE CLEAR. The following registers and conditions within the DCL are cleared by this command.

   - Status Register (ATA and ERR status bits)
   - All three Error Registers
   - Attention Summary Register
   - ECC Position and Pattern Registers
   - The Diagnostic Mode Bit

3. INITIALIZE SIGNAL. This MASSBUS interface signal performs the same functions as the DRIVE CLEAR command, but does not require that the Drive be ready (i.e., it bypasses the control register).

4. PACK ACKNOWLEDGE. This command sets the volume valid bit for the commanding controller. This command must be issued before any data transfer or positioning commands can be given if the drive has gone off-line and then on-line. It is primarily intended to avoid unknown disk pack changes.

5. READ-IN PRESET. This command sets the VV (volume valid) bit, clears the desired sector/track address register, clears the desired cylinder address register, and clears the FMT, HCI, and ECI bits in the offset register. It is used to bootstrap the device.

6. RELEASE. This command performs a drive clear function and releases the Drive for use by the other controller.

2.3.4 Mechanical Movement Commands

All of the below commands require movement of the Drive read/write heads as part of their execution sequence.

1. SEEK. This command causes the heads to be moved over the desired cylinder. Once the heads are positioned, the desired cylinder address becomes the current cylinder address since they are now the same.

2. OFFSET. This command is executed as a "micro" seek. It allows the read/write heads to be moved off the track center line. This command is used as part of the error recovery process and requires 10 ms to execute, regardless of the offset value.

3. RETURN TO CENTER LINE. This command is used to return the read/write heads to the track center line after an offset operation.

4. RECALIBRATE. This command positions the read/write heads over cylinder zero, and resets the current cylinder address register to zero. This command takes a maximum of 500 ms to complete.

5. UNLOAD. This command is used to place the drive in the STANDBY state. The heads are retracted, the spindle powered down, and the STANDBY light lit. This command completes when the Drive is brought back on-line (up to speed and heads loaded).

2.4 DETAILED BLOCK DIAGRAM DISCUSSION

2.4.1 Massbus Control Signal Routing and DCL Interface Registers

A block diagram showing the circuits used to route control line data from/to the controller and all interface control registers within the DCL is illustrated in Figure 2-3. The command decoding logic used to interpret the contents of the control register is also shown on this illustration.

Since the DCL can be accessed by either of two controllers, enabling signals that permit transfer to/from one particular controller at any given time must be generated. A controller gains access to the DCL when it asserts its DEMAND line at a time when the DCL is free (i.e., at a time when the other controller has not pre-empted the DCL through an earlier access).

2.4.1.1 Control Line Enabling Signals – The enabling signals (allowing transfer over the control lines) generated following access by a controller are defined below:

1. Controller A has access and is writing a DCL register. Signal DP3 REC CONT EN A H enables the related receivers to apply the 16-bit control line information to the control bus input multiplexer. Only the receivers are enabled since the Control-to-Drive (CTOD) signal is asserted when transferring to the DCL (Figure 2-3).

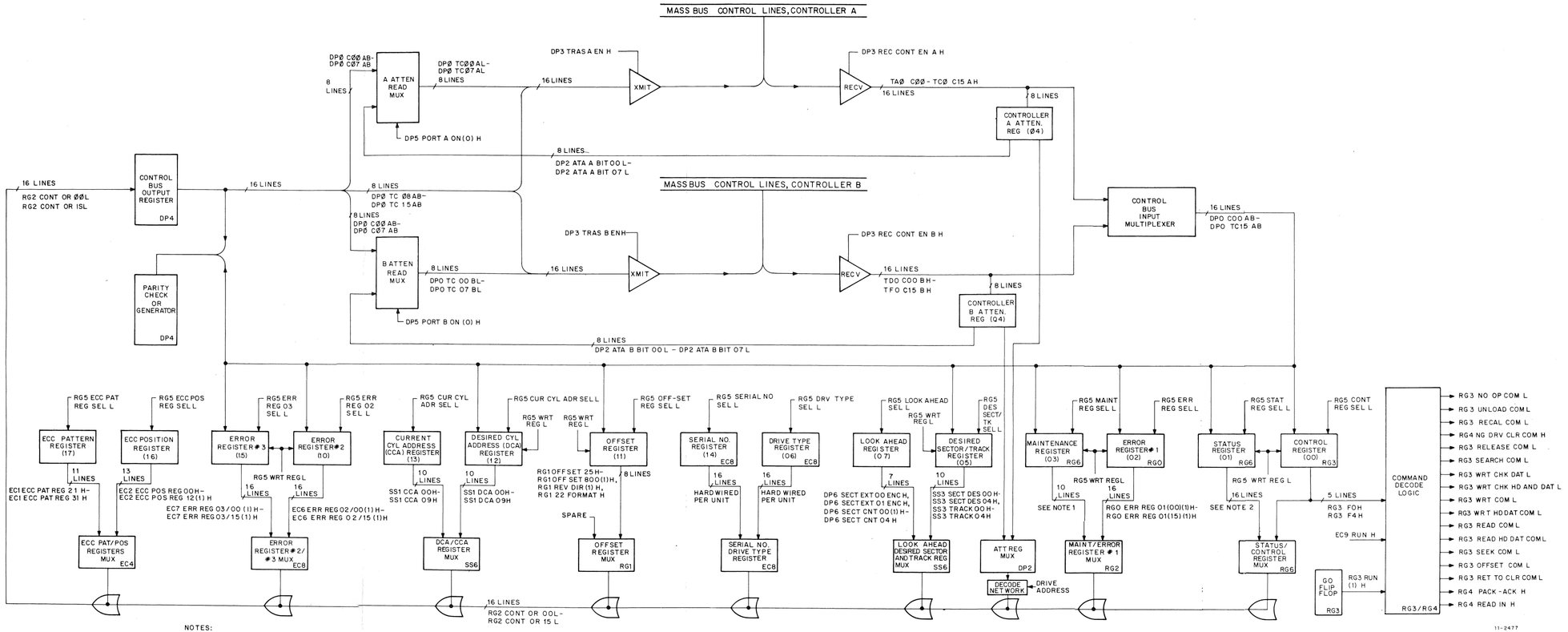


Figure 2-3 DCL Interface Registers and Massbus Control Signal Routing Block Diagram

2. Controller A has access and is reading one of the DCL registers. In this case, signal DP3 TRAS A EN H is asserted to enable the transmitters to send the outputs of the control bus output register/A attention read multiplexer to the controller.

NOTE

The eight low order bits from the control bus output register are taken through a multiplexer that also receives the outputs of the controller A attention register. This arrangement permits controller A to sample the status of the attention register at times when it does not have control of the DCL. This feature is discussed in a later paragraph.

Because controller A has access in this instance, signal DP5 PORT A ON (0) H is not asserted. This allows the multiplexer to pass on the low order byte from the control bus output register and not the output of the controller A Attention Register.

3. Controller B has access and is sending 16-bit information over the control bus. In this case, signal DP3 REC CONT EN B H is asserted in the same way as described for Controller A.

4. Controller B has access and is sampling the contents of the DCL register. In this case, signal DP3 TRAS B EN H is asserted in the same way as described for Controller A.

When a controller is sending information over the control bus, it is to write the control information into one of the DCL registers. The transfer path in this situation involves the receivers, control bus input multiplexer, and the addressed (selected) register.

To write control data into any register, signal RG5 WRT REG L must be asserted (this signal is generated only when the control-to-drive, CTOD, signal is asserted to indicate that the direction of transfer is to the DCL).

When a register is being sampled by a controller, the routing path is through an associated multiplexer. (In all but one case, one multiplexer serves two registers.) The signals are then applied to the control bus output register for transfer to the controller via the related read multiplexer and transmitter circuits.

All multiplexer circuits feeding the control bus output register have their outputs wire ORed. The multiplexer enabling signals that select the outputs of one register rather than another are the same as the signals used to select a particular register. The register selection signals are listed in the following table:

Register Name	Selection Signal
Control	RG5 CONT REG SEL L
Status	RG5 STAT REG SEL L
Error Reg No. 1	RG5 ERR REG 01 SEL L
Maintenance	RG5 MAINT REG SEL L
Attention Summary	DP2 ATA REG SEL A/B H
Desired Cylinder Address	RG5 DES CYL ADR SEL L

Register Name	Selection Signal
Current Cylinder Address	RG5 CUR CYL ADR SEL L
Error Reg 02	RG5 ERR REG 02 SEL L
Error Reg 03	RG5 ERR REG 03 SEL L
ECC Position	RG5 ECC POS REG SEL L
ECC Pattern	RG5 ECC PAT REG SEL L

2.4.1.2 Attention Summary Register Access – The manner and path in which an attention summary register is sampled by a controller depends on whether the DCL is free for access or currently engaged by one of the two controllers. For example, assume that the DCL is not currently engaged and it raises the ATTENTION interface line. Assume further that controller A is the first of the two controllers to sample the attention summary register to determine which Drive unit raised the ATTENTION line. In such a situation, controller A gains access to the DCL and samples the attention register via the following path: attention register multiplexer, Drive address decode network, control bus output register, A attention register read multiplexer, and the controller A transmitter circuits. If it is further assumed in this example that controller B attempts to read the attention summary register (after controller A has already gained access), it too can sample the register but the transfer now takes place over a different path. The transfer path to controller B is directly through the B attention read multiplexer. From Figure 2-7, it can be seen that this in no way affects paths to controller A which currently has access to the DCL. When controller B attempts to access the status register after accessing the attention summary register, it is supplied with an all zeros status, meaning that controller A has control.

2.4.1.3 DCL Interface Registers – The subsequent paragraphs describe the interface registers within the DCL.

- Control Register (00) and Command Decoding – The control register is addressed (selected) by the controller when the five Register Select lines convey all zeros. The control register is used to store the command code as shown below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
–	–	–	–	DVA	–	–	–	–	–	F5	F4	F3	F2	F1	GO

DVA – Device Available (For status sampling)

F1–F5 – Function Code

GO – GO bit

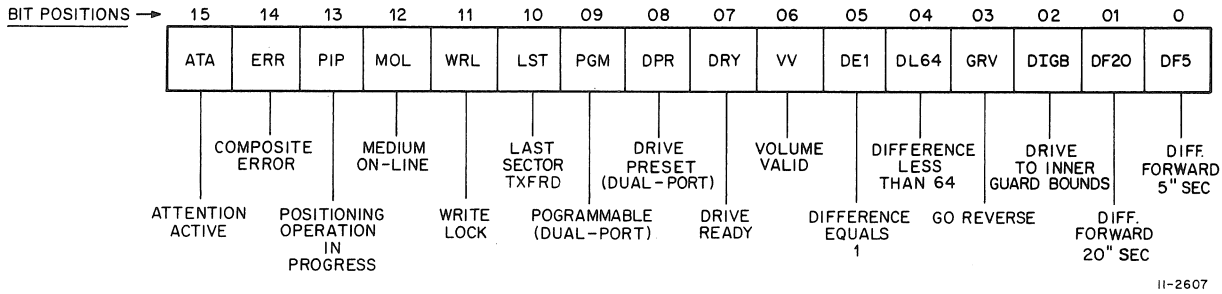
Control Register Format

The GO bit can be considered an extension of the function code since it must be set (and also the RUN line must be high) for the DCL to execute the specified command. The five bit function (F1–F5) specifies the type of command to be executed. The Function Code and related commands are listed below.

Function Code					Command
F5	F4	F3	F2	F1	
0	0	0	0	0	No operation
0	0	0	0	1	Unload (stand-by)
0	0	0	1	1	Recalibrate
0	0	1	0	0	Drive Clear
0	0	1	0	1	Release (dual-port operation)
0	1	1	0	0	Search Command
1	0	1	0	0	Write Check Data
1	0	1	0	1	Write Check Header and Data
1	1	0	0	0	Write Data
1	1	0	0	1	Write Header and Data
1	1	1	0	0	Read Data
1	1	1	0	1	Read Header and Data
0	0	0	1	0	Seek Command
0	0	1	1	0	Offset Command
0	0	1	1	1	Return to Centerline
0	1	0	0	1	Pack Acknowledge
0	1	0	0	0	Read-In Preset
1	1	0	1	0	Illegal Functions
		Through			
1	1	1	1	1	

The device available (DVA) bit is used for controller status sampling. This bit is set if sampled by the controller that has gained control of the DCL. It is reset (meaning that the device is not available) to the controller that does not have control.

- Status Register – The status register informs the controller of various conditions within the DCL and the Drive. The format and the meaning for each bit position are shown below.



Bits 0–5 are used to monitor the drive read/write head loading sequence. Following a successful head loading sequence, these bits are always cleared. On an unsuccessful head loading, the particular bits that are set inform the operating/diagnostic system of the type of fault. A detailed breakdown of all bit meanings is given below:

1. Bit 0: Drive Forward 5 in./sec (DF5) – The DCL has detected the drive forward 5 in./sec signal while in the head load mode after a start pulse was recognized. This bit is reset by the File Ready signal at the completion of a head load sequence.

2. Bit 1: Drive Forward 20 in./sec (DF20) – The DCL has detected the drive forward 20 in./sec signal during a head load sequence. This bit is reset by File Ready at the completion of a head load sequence.

3. Bit 2: Drive to Inner Guard Band (DIGB) – The DCL has detected the drive to inner guard band signal during a head load sequence. This bit is reset by a File Ready at the completion of the head load sequence.

4. Bit 3: Go Reverse (GRV) – The DCL has detected the GO Reverse signal during a head load sequence. This bit is reset by File Ready at the completion of a head load sequence.

5. Bit 4: Difference Less than 64 (DL64) – The DCL has detected a value less than 64 in the difference counter during the reverse seek of the head load sequence. This bit is reset by a File Ready at the completion of a head load sequence.

6. Bit 5: Difference Equals 1 (DE1) – The DCL has detected a value equal to 1 in the difference counter during a head load sequence. The bit is reset by a File Ready at the completion of a head load sequence.

7. Bit 6: Volume Valid (VV) – The "Volume Valid" status bit indicates when a disk pack may have been changed, and therefore the program should not assume anything about the identity of the pack. Even though only one VV bit exists in the dual-controller application, VV-A is accessible only to controller A and VV-B is accessible only to controller B. The VV status bit is reset by the DCL whenever the drive cycles up (from the off state). The "Pack Acknowledge" command or "Read in Preset" command, when received from either controller, causes the VV bit to set for that controller.

8. Bit 7: Drive Ready (DRY) – At the completion of every command, data handling or mechanical motion, the DCL sets this bit. The controller should not attempt to issue another command if this bit is reset. This bit indicates the readiness of the RP04 DCL to accept a new command. The (DRY) bit is associated with the following conditions:

   - If the command is read or write type, the setting of the DRY bit indicates normal termination. If an error was made during data transfer, the appropriate error bits are set as well.

   - If the command is mechanical movement command, both the ATA bit and the DRY bit are set at the completion of the command. If an error was committed during the command, the appropriate error bits are also set.

     The DRY bit status during the various stages of the DCL operation is shown in Table 2-1. The ATA bit associated with the DRY bit functions is shown in the table only if no error conditions exist (normal termination). At the completion of the operation, the DRY bit is set.

Table 2-1
DRY/PIP/ATA Status During DCL Operation

Operation	DRY	PIP	ATA at End? (No Error)
No Operation	1	0	No
Unload (Stand-by)	0	1	Yes
Recalibrate	0	1	Yes
Drive Clear	1	0	No
Release	0	0	No
Search Command	0	1	Yes
Implied Search	0	0	No
Seek	0	1	Yes
Offset	0	1	Yes
Write Check	0	0	No
Write Data	0	0	No
Write Header and Data	0	0	No
Read Data	0	0	No
Read Header and Data	0	0	No
Implied Seek	0	0	No
Mid-Transfer Seek	0	0	No
Return to Centerline	0	1	Yes
Pack Acknowledge	1	0	No
Read-In Preset	1	0	No

9. Bit 8: Drive Preset (DPR) – On a single-controller type operation this bit is always set. On dual-controller type operation, this bit will be reset if the DCL is busy from the other controller.

   The DPR bit is set again when the RP04 switches from the other controller to this one.

   In general, setting the DPR bit indicates that the DCL is connected to the asynchronous control bus of this controller.

10. Bit 9: Programmable (PGM) – This bit is set when the CONTROLLER SELECT switch is in the neutral (A/B) position upon power up, indicating that the device is accessible from either controller A or B. When the CONTROLLER SELECT switch is in either A or B position upon power up this bit is cleared.

11. Bit 10: Last Sector Transferred (LST) – This bit is set by the RP04 when the last addressable sector on the disk pack has been read or written. It is cleared by the initialize signal.

12. Bit 11: Write Lock (WRL) – This bit reflects the status of the WRITE/PROTECT switch on the RP04 control panel. When this switch is activated, no write operation can be executed.

13. Bit 12: Medium On-Line (MOL) – This bit is set by the RP04 at the successful completion of the start-up cycle as follows:

    - Mount Pack
    - Start Spindle Motor

- Brush Cycle
- Motor Up to Speed
- Load Heads
- Recalibrate

With the positioner in recalibrate state (addressing cylinder 0), the device generates a "File-Ready" condition which is active only if the positioner is settled in recalibrate state. Upon recognizing this condition, the RP04 device sets the MOL bit.

The MOL bit is reset when:

- The spindle is powered down.
- The device is switched off-line (with the spindle still up to speed) for diagnostic purposes.

NOTE

Whenever the MOL bit changes states (set or reset), the ATA bit is also set (except in the unload operation case).

14. Bit 13: Positioning Operation in Progress (PIP) – Set by the RP04 when a positioning function command is accepted. This bit is reset when the function is complete.

    The PIP bit is set during seek, offset, return to centerline, recalibrate, unload, and search commands. The PIP bit is not set during implied-seeks or mid-transfer seeks.

    Table 2-1 shows the conditioning of PIP in relation to the type of operation being performed. At the completion of the moving operation, the PIP bit is reset and both the DRY and ATA bits are set (normal termination).

15. Bit 14: Composite Error (ERR) – This bit is set when any bit in the error registers 01, 02, or 03 becomes set. This bit summarizes all the errors in the DCL/Drive that are considered important to the operation.

    This bit is reset as follows:

    - The controller issues a "Drive Clear" command.
    - The controller asserts the initialize (INIT) line.

16. Bit 15: Attention Active (ATA) – The attention active bit in the status register is the indicator of the attention condition for the RP04.

    The ATA bit can be set only by the DCL. In addition to setting this bit on the status register, the same conditions control the interface line (ATTENTION) belonging to the attention summary register.

    The conditions for setting the ATA bit and asserting the ATTENTION line are as follows:

    - Any error in the error register causes the ATA Bit/ATTENTION Line to set (except during data transfers).
    - A positioning operation is completed (Table 2-1).

- Start-up cycle completion (with MOL Bit set).
- Dual-Controller operation. Indicates present drive availability (drive was requested before, but was not available).

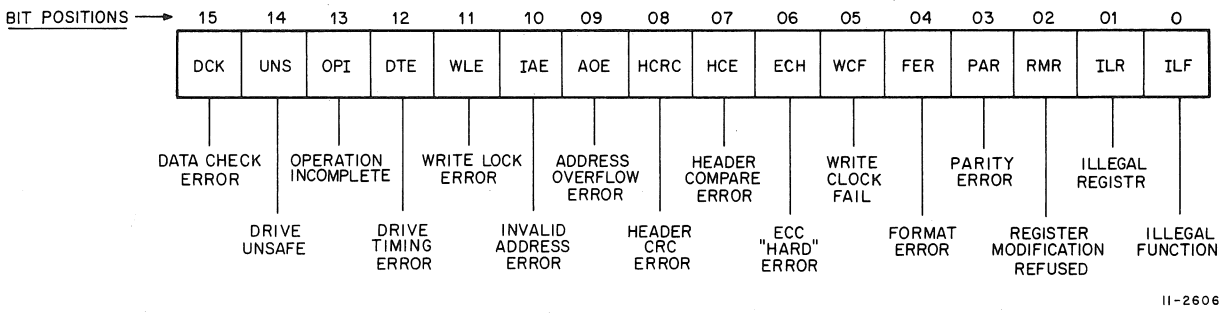
NOTE

The ATA bit is not set if the drive is switched from a neutral position.

The conditions for resetting the ATA bit and negating the ATTENTION line are as follows:

- The controller issues a "Drive Clear" command.
- The controller writes a ONE into the attention summary pseudo register bit position corresponding to this drive.
- The controller asserts the initialize (init) line on the interface.

- Error Register No. 1 – This register informs the controller of specific DCL error conditions. The register can also be written by the controller for diagnostic purposes. Setting any bit in this register sets the composite error bit in the status register. The format of this register is shown below.



The meanings of the individual bits are as follows:

1. Bit 0: Illegal Function (ILF) – This bit is set when the function code in the control register does not correspond to an implemented command. This bit is reset when a "Drive Clear" command is issued or an initialize (INIT) pulse is received.

2. Bit 1: Illegal Register (ILR) – This bit is set when the DCL decodes a nonexisting register address on the register select lines.

NOTE

Attempting to write into a read only register does not cause the (ILR) bit to set. The bits received are ignored and no other error condition is flagged.

This bit is reset when a Drive Clear command is issued or an initialize (INIT) pulse is received.

3. Bit 2: Register Modification Refused (RMR) – This bit is set when a "Write" is attempted into any register (except for the Attention Summary Register) during an operation.

During an operation only two registers can be written into:

- Maintenance Register
- Attention Summary Register

When the RMR bit is set, the DCL continues to execute the command in progress. This bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

4. Bit 3: Parity Error (PAR) – This bit becomes set under the two conditions given below.

   - When a parity error is detected during data transmission over the synchronous or asynchronous data lines (odd parity) during a "Write" operation. The detection of a parity error causes the DCL to set the "Exception" line and set the PAR bit in the error register. The DCL continues accepting data as if nothing happened until the end of the sector. At the trailing edge of (EBL), the RP04 samples the RUN line and takes the following actions:

     If the RUN-line is high, the DCL maintains the PAR bit and EXCEPTION line set and continues writing on the next sector as if nothing happened. At the end of transfer the ATA bit is set.

     If the RUN-line is low, the "Write" command will be terminated with the ATA bit and EXCEPTION line set, in addition to the PAR error bit.

     In either of the foregoing cases, the EXCEPTION line is reset at the trailing edge of the EBL pulse.

   - When a parity error is detected on the asynchronous control bus while writing a register.

5. Bit 4: Format Error (FER) – This bit is set during header verification when bit 12 of the first header word fails to match bit 12 of the offset register. This error bit usually indicates the case where the wrong pack is mounted on the RP04 device. If the error is detected, all synchronous commands except read header and data will abort. This bit is cleared by a Drive Clear command or the initialization signal.

6. Bit 5: Write Clock Fail (WCF) – This bit is set if (during a write operation), no write clock signal from the controller is detected. Upon recognizing this error condition, the RP04 device aborts the command. This bit is cleared when a "Drive Clear" command or an initialize (INIT) pulse is received.

7. Bit 6: ECC Hard Error (ECH) – This bit is set when the outcome of the error correction procedure is such that the error is ECC noncorrectable. This bit is cleared when a "Drive Clear" command or an initialize (INIT) pulse is received.

8. Bit 7: Header Compare Error (HCE) – This bit is set by the DCL when the header information read from the addressed sector fails to match the desired address information (cylinder, sector, and track addresses) accompanying a read/write command. If the DCL sets this bit, no transfer takes place except in the case of read header and data command when headers are transferred to the controller even though header errors are detected. This bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

9. Bit 8: Header Cyclic Redundancy Check Error (HCRC) – This bit is used to indicate a CRC error in the header field. It is possible for the cylinder address and sector/track address words of the header to compare successfully (no HCE), but because of an error in the key field words (or the CRC word itself), the HCRC bit can become set. With this bit set, the DCL does not make any data transfer. In the event of a CRC error during a "Read Header and Data" command, the header words are transferred to the controller. This bit is reset when a Drive Clear command or an initialize (INIT) pulse is received.

10. Bit 9: Address Overflow Error (AOE) – This bit is set during any synchronous transfer after the last addressable sector has been transferred and the RUN line is still asserted. Once set, the DCL terminates the operation. The AOE bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

11. Bit 10: Invalid Address Error (IAE) – This bit is set when a seek/search operation is initiated and the address in the desired cylinder address register or desired sector/track address register is invalid. The DCL format allows for 20 sectors per data track (18-bit word data fields) or 22 sectors per data track (16-bit word data fields). The DCL distinguishes between the two formats and sets the IAE bit if a sector greater than 19 is requested from a 20-sector disk pack (18-bit word data fields). A similar action occurs if the cylinder and track addresses exceed the RP04 device capability.

NOTE

When this error bit is set, any intended operation will not take place.

The IAE bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

12. Bit 11: Write Lock Error (WLE) – A manual WRITE PROTECT switch can place the Drive in "Write Lock" during normal operation. If the Drive is in the "Write Lock" mode and the operating system attempts to issue a write command, the "Write Lock Error" (WLE) bit is set. The WLE bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

13. Bit 12: Drive Timing Error (DTE) – This bit is set when a failure has occurred in the clocking or timing circuits of the DCL. A failure in the clocking or timing circuits cannot guarantee the logic remaining in the proper sequence. Consequently, in both the read or write operation, the DCL aborts the command as soon as this error is detected. In the "Write" case, the software should try to regenerate the sector where the error occurred. Setting the DTE error bit includes those cases where the rise of a sector pulse is encountered before the data transmission is finished. This bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

14. Bit 13: Operation Incomplete (OPI) – This error bit can only be set when the Drive is not positioning the read/write heads and is set under the following conditions:

    - A read or write command, involving header search, has not begun transmitting data (sync clocks) within three index pulses.

    - During a "Search" operation, and in the case where a "Sector Count" match is not made, the OPI bit is set after a maximum of three index pulses have been encountered.

    The DCL continues retrying for as long as the software wishes. This bit resets when a "Drive Clear" command or an initialize (INIT) pulse is received.

NOTE

In general, the OPI bit is used to indicate every case where, following a command initiation, there is inactivity for a period of three index pulses.

With the OPI bit set, the GO-bit is cleared and the RP04 is returned to the ready state (the RDY bit is set).

15. Bit 14: Drive Unsafe (UNS) – This bit is set when the drive recognizes a condition that prevents the Drive from operating. Usually this bit being set reflects an "emergency" situation where the heads are automatically retracted and/or the drive is cycled down. One example of a "drive unsafe" case is the drive error conditions that cause the RP04 to go into the "Write Lock" mode. If executing a "Drive Clear" does not cause the UNS condition to disappear, the RP04 must be powered and cycled-up again to assure clearing all the errors including the UNS bit. With the UNS bit set, the DCL cannot guarantee correct results of any of the operations. In most cases, clearing the UNS bit requires field service intervention.

16. Bit 15: Data Check Error (DCK) – This bit is set during a "Read" operation when the ECC hardware has detected an ECC error after the ECC bytes have been monitored. The DCK bit is handled as follows:

    - If "Error Correction Code/Inhibit" (ECI) Bit is OFF, the DCL enters into the error correction process. The DCK bit remains set during the error correction procedure. This bit is cleared when a "Drive Clear" command or an initialize (INIT) pulse is received.

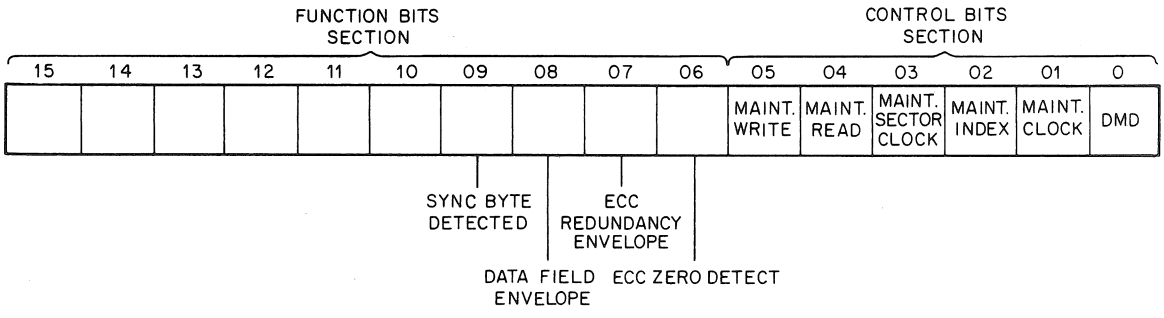
    - If "Error Correction Code/Inhibit" (ECI) Bit is ON, even though an ECC error is detected at the end of data transmission, the error correction is inhibited.

    With the DCK bit set, the data transfer on the present sector terminates normally and if the RUN-line remains high at the fall of the EBL Pulse, the command continues on the next sector. This bit is reset when a "Drive Clear" command or an initialize (INIT) pulse is received.

NOTE

The EXCEPTION line is asserted at the completion of the error correction process and lasts for the duration of EBL.

- Maintenance Register – This register implements maintenance and diagnostic functions within the DCL. All bits can be read or written. The format for this register is shown below.



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The Diagnostic Mode (DMD) bit must be set before the DCL can be placed in a diagnostic mode. With this bit set, the device handles the same command repertoire as it normally does.

The maintenance register provides wrap-around capability within the DCL. By using a program controlled clock the data is shifted through various registers and brought back to memory without being written on the disk. The wrap-around capability does not check the read/write electronics, but goes as far as the shift register. The wrap-around capability operates only under the diagnostic mode.

- Attention Summary Register – This register can be considered a pseudo register because it appears as an 8-bit register from a system standpoint, but is implemented as a single bit (in a different bit position however) in each Drive. Also all eight Drives in a system respond when this register is accessed. By looking at which bit positions are set, the operating system can determine which Drive(s) require servicing. From a system standpoint, the physical Drives and related bit positions (on the Massbus control lines) are broken down as follows:

Prime No.	Bit	Massbus Control Line
0	$00\ (ATA00)_8$	0
1	$01\ (ATA01)_8$	1
2	$02\ (ATA02)_8$	2
.	.	.
.	.	.
.	.	.
.	.	.
7	$07\ (ATA07)_8$	7

Hence the single attention register for drive zero is used to indicate the attention active condition for drive zero etc.

The controller normally requests "Attention Summary" status from all drives simultaneously by indicating a "read from Register-04" on the register select lines on the Massbus interface. When "Register-04" is selected, each device places the output of its "attention active" (ATA) flip-flop on its assigned bit position on the asynchronous control bus.

A particular attention register flip-flop is cleared when the controller writes a one on the related control line. The operating system normally clears the attention register when the controller accesses a drive, i.e., immediately after recognizing that an attention line has been raised. In dual controller operation, the attention bit for both controllers is set under the following special conditions:

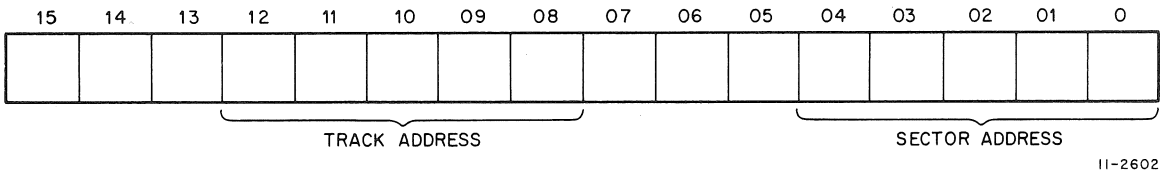
1. Upon powering up the Drive from the off-state, attention active goes to both controllers.

2. Upon powering up the Drive from the standby state, attention active goes to both controllers (even if the device is seized by one of the controllers).

3. In case of a persistent error, the Drive is forced to the neutral state. Unless it has already been requested by the other controller, no attention active is generated until a request comes through.

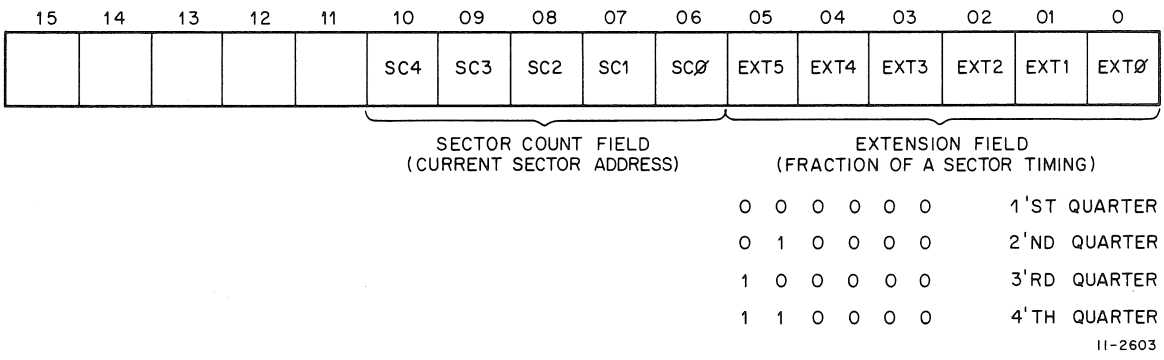
   When a controller clears the attention register on accessing the DCL/Drive, it clears only the related flip-flop. That is, controller A clears only the flip-flop associated with controller A and controller B clears only its related flip-flop.

- Desired Sector/Track Register – One register is used for sector and track addressing since only five dedicated bits are required to address the 22 possible sectors or 19 possible tracks. The format of this register is shown below:



Invalid address errors are generated by the DCL if the address information supplied by the controller exceeds the maximum number of accessible sectors/tracks.

- Look Ahead Register – This register is incorporated to provide the software with a means of optimizing the disk access time by minimizing rotational delays. The format of this register is shown below.



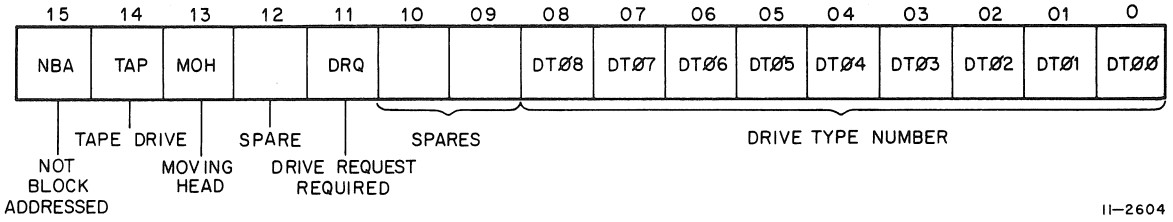
The two fields of the register are described below.

a. Extension Field. This 6-bit field is essentially a counter that develops the internal timing within a sector. The counter is always cleared to zero state at the rise of each sector pulse. The counter divides the sector roughly into fourths (=200 μs) since only the two high order bits are currently used for counting.

b. Sector Count Field. The purpose of this field is to address the required sector on the data track, through an exclusive OR arrangement, with the "desired sector/track address" register. The sector count field is always being updated. Each time the index pulse is encountered, the sector count field resets to zero, at the rise of the index pulse. The maximum count of the sector counter is:

   0 through 21 if 16-bit word/data field format.
   0 through 19 if 18-bit word/data field format.

- Drive Type Register – This is a jumper rather than flip-flop type register and is cut at installation to provide proper coding information. This register permits the controller/software to distinguish between different classes of drives. The format is below.



Bits 0–8 are used to identify the device type so that the system can distinguish between types of disk drives, tape drives etc.

Bit 11 is the Drive request required (DRQ) bit and is hardwired to always indicate a "1" when the drive is to be operated in a dual port environment.

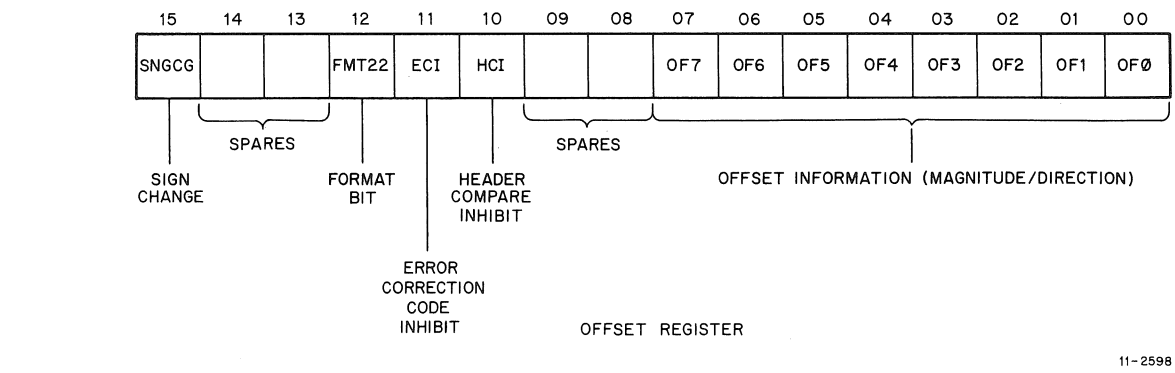
Bit 13 is used to indicate that the Drive is a moving head (MOH) device. Since the RP04 falls in the category, this bit is hardwired to the set state.

Bit 14 and 15 are always zero for the RP04 device since it is not a tape drive and it is block (sector) addressed.

- Serial Number Register – Like the drive type register, this register also employs jumpers. Its purpose is to allow identification of the Drive unit to distinguish it from other Drives, possibly of the same type, attached to a single controller.

  It differs from the "drive type" number in that the "drive type" refers to different types of Drives, such as RP04's or RS04's with major options of RP04's purchased from a different vendor.

- Offset Register – This register is used for data recovery purposes. Its format is shown below.



Bit 0–7 contain offset information which dictates how far (in microinches) from the centerline the read/write heads are to be positioned to implement the data recovery operation.

NOTE

Normally the offset register is used only when data recovery is unattainable through use of ECC processing.

The selectable read/write head position offsets are given as follows:

Position	Code Word OF0 – OF7								Value/Direction
	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0	(Microinches)
1st Offset	0	0	0	1	0	0	0	0	+400
2nd Offset	1	0	0	1	0	0	0	0	-400
3rd Offset	0	0	1	0	0	0	0	0	+800
4th Offset	1	0	1	0	0	0	0	0	-800
5th Offset	0	0	1	1	0	0	0	0	+1200
6th Offset	1	0	1	1	0	0	0	0	-1200
Return to Track Centerline									

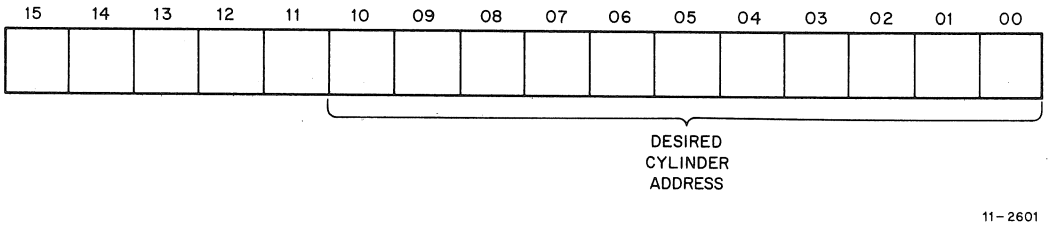
Bit 11 is used for the header compare inhibit function. The software operating system has the option of inhibiting header comparison technique used for sector identification. The RP04, upon recognizing this bit high, ignores the header compare logic and CRC correction.

With the HCI bit set, the DCL depends only on the sector count desired sector address for sector identification. If the sector count happens to be out of sequence, the wrong sector may be accessed.

Bit 11 provides the error correction inhibit function. By setting this bit, the software can disable the error correction code handling logic. When this bit is cleared during a read data transfer and an error is detected at the end of a transmission, the DCL immediately enters the ECC correction process. At this time, the DCL also sets the data check error (DCK) bit in error register 01.

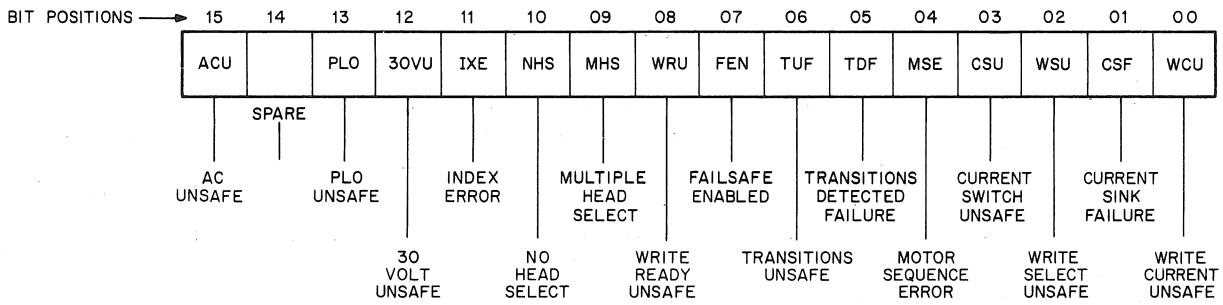
When the results of ECC processing are available, the DCL places the error pattern and the location of the error pattern (within the data field) in the appropriate ECC registers. If the error is ECC non-correctable, the DCL also sets the "ECC Hard Error" (ECH) bit. If the ECI bit is set, the ECC correction process is inhibited. However, the DCK bit is still set on detection of an error.

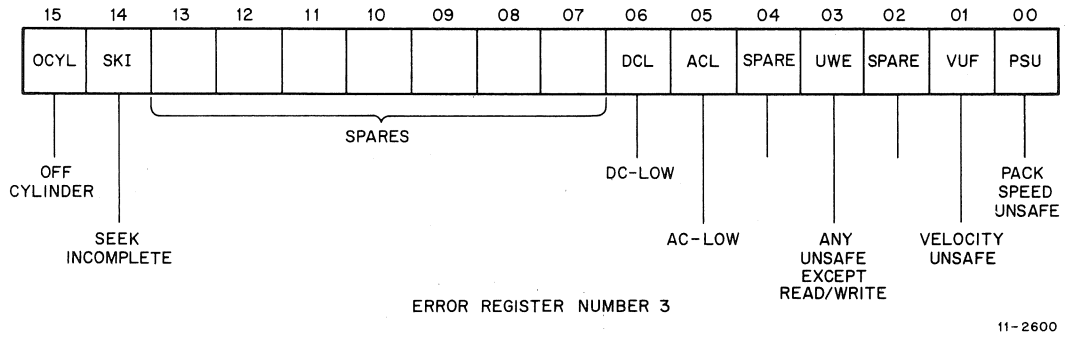
- Desired Cylinder Address Register – The format of this register is shown below. Its function and use are described in the subsection covering the disk addressing logic. Only 10 bits are used since this is more than enough to address the 411 cylinders in a disk.



- Current Cylinder Address Register – This register always stores the actual cylinder address where the disk read/write heads are now positioned. Its format is the same as the described cylinder address register and is more fully discussed in the subsection on the Disk Addressing Logic.

- Error Register Numbers 2 and 3 – These registers are used to receive the error bits supplied from the drive via the MDLI interface lines (Figure 2-2). The formats for both registers are shown as follows.





- ECC Position Register – Following the completion of the error correction procedure, this register contains the exact location of the error burst within the data field.

  Upon completion of the ECC process, the DCL loads this register with the necessary information for processor software examination and analysis.

- ECC Pattern Register – This register contains the actual error burst which becomes available at the completion of the DCL error correction process.

  The processor software uses the contents of the ECC position register to find the actual location of the error burst in the data field. Then the error burst itself determines the bits in error within the 11 bit field.

2.4.2 Synchronous Data Flow

Figure 2-4 shows a block diagram of the circuits used to implement data word (synchronous) transfers between controller and disk. The data path for both 16 and 18-bit transfers is the same with only minor differences in handling techniques required.

NOTES:

1. THE 18 DATA LINES FROM THESE PCBs ARE: TA0 DI00AH–TA0 DI05AH, BIT 00 THROUGH 05
   TB0 DI05AH–TB0 DI11AH, BIT 06 THROUGH 11
   TC0 DI12AH–TC0 DI17AH, BIT 12 THROUGH 17
2. THE 18 DATA LINES FROM THESE PCBs ARE: TD0 DI00BH–TD0 DI05BH, BIT 00 THROUGH 05
   TE0 DI06BH–TE0 DI11BH, BIT 06 THROUGH 11
   TF0 DI12BH–TF0 DI17BH, BIT 12 THROUGH 17
3. DESIGNATOR IN BOX (▭) INDICATES CORRESPONDING PRINT SET DRAWING
4. BITS 00–07 (SN3 BUF00H – SN3 BUF07H) ARE TAKEN THROUGH THE SYNC CHARACTER MULTIPLEXER FOR APPLICATION TO THE I/O DATA SHIFT REGISTER

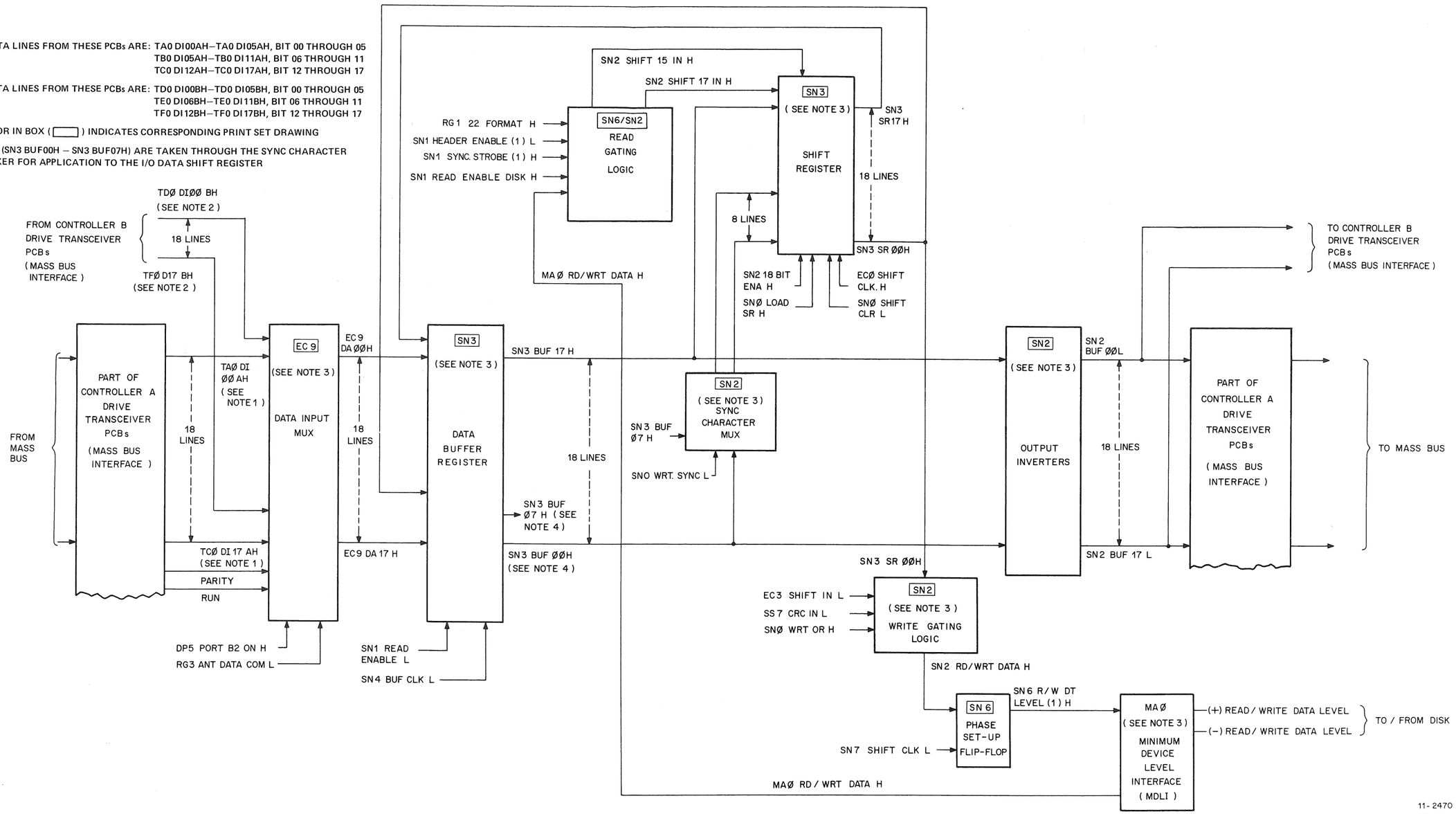


Figure 2-4 Synchronous Data Transfer Path Block Diagram

2.4.2.1 Write Operation (Massbus-to-Disk Transfer) – Data words placed on the Massbus for transfer to the disk travel through the following circuits before being sent to the disk circuitry:

1. Controller A/controller B Drive transceiver PCB modules.
2. Data input multiplexer logic.
3. Data buffer register.
4. Data shift register. All transfers up to this point are made in parallel – that is, 16 or 18 bits at a time. Conversion from parallel to serial transfer is effected here in the shift register.
5. Write gating logic.
6. Phase set up flip-flop.
7. Minimum device level interface (MDLI) circuits.

Data words supplied over either Massbus are taken through respective Drive transceiver modules for application to the data input multiplexer circuits on the error correction module. The level of signal DP5 PORT B2 ON H governs whether the data word is accepted from Massbus A or Massbus B. When asserted, indicating that controller B has access to the disk, only data words from Massbus B are accepted by the data input multiplexing logic. When this signal is negated, Massbus A has access and only words from it are accepted. Signals PARITY and RUN are also received into the data input multiplexing circuits from which they are sent to the parity check and control logic respectively.

The data buffer register is used to temporarily store data in both read and write operations. Since a write operation is being performed, signal SN1 READ ENABLE L is not asserted, meaning that the data buffer register accepts data words from the data input multiplexer rather than the shift register.

For both write and read operations, signal SN4 BUF CLK L strobes each data word into the data buffer register. For a write operation, this signal is developed as follows:

- When the DCL is ready to load the data buffer register, it issues the Bus Sync Clock to the controller.
- In response to the Bus Sync Clock, the controller echoes back a write clock signal which the DCL uses to develop signal SN4 BUF CLK L.

From the data buffer register, the 18/16-bit word is entered (in parallel) into the shift register.

NOTE

The 8 low order bits are taken through a sync character multiplexer circuit for application to the shift register. At times, it is necessary to write sync bytes as part of the sector format (see discussion on sector format).

The SN0 WRITE SYNC L signal is used to enable transfer of sync characters through the sync character multiplexer for application at the 8 low order bit positions of the shift register.

Signal SN0 LOAD SR H is used to allow transfer of data words being parallel loaded into the shift register. Since the RP04 is capable of writing both 16 and 18-bit words onto the disk, the time that loading occurs depends on the word length. In other words, if an 18-bit word is being written, 18 shift pulses must occur (for writing each bit onto the disk) before an SN0 LOAD SR H signal is issued. For 16-bit words, only 16 shift pulses need occur before SN0 LOAD SR H is asserted. Once a word is loaded, it is shifted out (one-bit at a time) via the least significant bit line (SN3 SR 00 H). Shifting is affected by the ECO SHFT CLK H signal which is derived from the PLO clock supplied from the disk. Two additional signals are used by I/O data shift register during write operations are:

1. SN2 18 BIT ENA H. This is used to enable the two high order bits of the register that are only operative during 18-bit transfers.

2. SN0 SHFT CLR L. This is used to clear out the register (at the start of each sector and at other times) when it is necessary to write zeros onto the disk. See discussion on sector format.

Each bit shifted out of the shift register is taken through the write gating logic for application to the phase setup flip-flop. Since a write operation is being performed, signal SN0 WRITE OR H is asserted to allow each bit from the shift register to pass through the write gating logic. The purposes of the two remaining signals applied here are:

1. SS7 CRC IN L. This is used to write the CRC word produced as part of the header format. (See sector format discussion.)

2. EC3 SHIFT IN L. This is used to write the ECC field following the data field. (See sector format discussion.)

The phase setup flip-flop is set/reset consistent with each ONE/ZERO supplied from the write gating logic. This flip-flop is clocked by the SN7 SHIFT CLK L signal which ensures that setting/resetting (and eventual flux reversal on the disk surface) occurs during the middle of the bit transfer time.

From the phase setup flip-flop, the signal (SN6 R/WDT LEVEL (1) H) is taken to a differential line driver in the MDLI circuits. In turn, the signal is issued over the read/write data level lines to the disk circuitry.

2.4.2.2 **Read Operation (Disk-to-Massbus Transfers)** – Data words coming from the disk travel through the following circuits before being sent over the Massbus:

1. MDLI circuits

2. Read gating logic

3. Shift register

4. Data buffer register

5. Output inverters

6. Controller A/controller B drive transceivers PCB's

Data bits read from the disk are first taken through a differential line receiver in the MDLI circuits and applied to the read gating circuits as signal MA0 RD/WRT DATA H. Since a read operation is in process, signal SN1 READ ENABLE DSK H is asserted. This allows data read from the disk to be shifted serially to the shift register. Application of the received data to the shift register can be over one of two lines, SN2 SHIFT 15 H or SN2 SHIFT 17 H. The former is used when receiving 16-bit words and the latter when receiving 18-bit words. Certain control signals are applied to the read gating logic to govern the time, at which a particular output line is selected. These signals and their uses are:

1. RG1 22 FORMAT H. This signal is asserted as long as bit 12 of the offset register is set. It means that the device control logic is operating in the 16-bit mode and causes selection of the SN2 SHIFT 15 H line as the input to the shift register.

2. SN1 HEADER ENABLE. Regardless of operating mode (16 or 18-bit) the header is always in 16-bit format. This signal enables transfer of 16-bit header information over the SN2 SHIFT 15 IN H line when the device control logic is being operated in the 18-bit mode.

3. SN1 SYNC STROBE H. As mentioned earlier, the sync byte is always positioned in the low order character position of a 16-bit word. Consequently, when the sync byte is being read it must be inserted in the register over the SN2 SHFT 15 IN H line and then shifted into position for detection.

If the device control logic is in the 18-bit mode, signal SN2 18 BIT ENA H is asserted. Essentially, this signal extends the I/O data shift register two more bits. The most significant bit position of the shift register receives the SN2 SHIFT 17 IN H signal from the read gating logic. After 18 shift pulses the word is properly positioned for transfer to the data buffer register. Transfer is over the lines designated SN3 SR 00 H through SN3 SR 17 H.

Since a read operation is in process, signal SN1 READ ENABLE L is asserted, allowing the data buffer register to accept the inputs from the shift register rather than the data input multiplexer. Strobing of the word into this register is affected by SN4 BUF CLK L. After a word is completely assembled in the shift register, signal SN4 BUF CLL L (produced as a result of the number of shift pulses required, i.e., 16/18) is asserted to parallel load the data buffer register.

Output signals SN3 BUF 001 L through SN3 BUF 17 H from the data buffer register are taken through a set of output inverters for application to the Massbus interface circuits.

2.4.3 Basic Clock and Index Pulse Distribution

Numerous control operations within the DCL are governed in one way or another by the clock and index signals supplied from the drive. Figure 2-5 shows the distribution and key uses made of these signals within the DCL.

2.4.3.1 Basic Clock Signals – Two basic clock signals are supplied from the drive logic:

1. PLO CLOCK – The phase locked oscillator (PLO) signal is taken through a line receiver in the MDLI interface logic and applied to a three level synchronization network on the error correction PCB. Here it is used to implement and synchronize all control sequences required during all operations other than read activities.

2. READ DATA STROBE – This signal is also taken through the MDLI interface logic and applied to the three level synchronization logic. It is used to implement the control and transfer sequence during read operations (read header and data, read data and the header handling portion of the write data operation).

Each of these clock signals is used within the three level synchronization network to generate ECO SHFT CLK H. Signal SN1 READ ENABLE H (supplied from the synchronous logic and asserted during read operations) is used to select MB1 READ STROBE H as the source signal to produce ECO SHFT CLK H. When SN1 READ ENABLE H is not asserted, meaning no read operations are in process, then MB1 PLO CLK H is selected as the clock source signal.

The ECO WRITE STROBE H signal (generated by dividing the PLO clock signal in half) is used by the Drive to write the data bits onto the disk. One purpose of the ECO SHFT CLK H signal during write operations is that it shifts bits serially out of the shift register for transfer to the Drive. Therefore both shifting of the data bits and the accompanying write strobes are under control of the MB1 PLO CLK H signal.

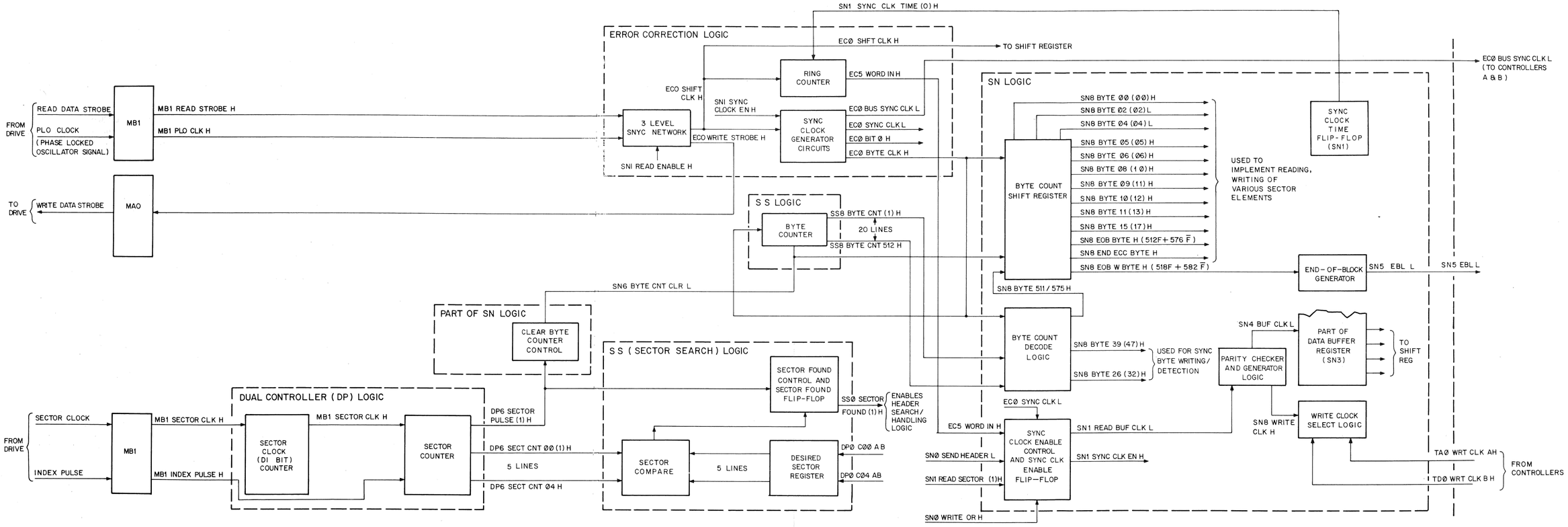


Figure 2-5 Basic Clock and Index Pulse Distribution Block Diagram

2.4.3.2 Sync Clock Generator Circuits – The sync clock generator circuits consist of a shift register and an end-around counter both of which are clocked by the EC0 SHFT CLK H signal. The shift register is used primarily for developing the sync clock signals used in synchronous data transfers while the end-around counter serves chiefly to count bits to develop a byte clock. Four output signals are produced by the sync clock generator circuits. These signals and their system uses are described in the paragraphs below.

- Signal EC0 BUS SYNC CLK L – This signal is shipped to the controller for each synchronous word transfer between controller and DCL, i.e., whether it be a header word or data word. Signal SN1 SYNC CLK EN H controls the times at which the EC0 BUS SYNC CLK L signal is sent to the controller. By asserting SN1 SYNC CLK EN H (supplied from the SYNC CLK ENABLE flip-flop in the SN logic) four times during each header field transfer and 256 times during each data field transfer, the number of SYNC CLOCKs required for a complete sector transfer are developed.

- Signal EC0 SYNC CLK L – This signal switches high at the trailing edge of EC0 BUS SYNC CLK L and is used to clear the SYNC CLK ENABLE flip-flop. Since the data word (for both read and write operation) is now in the data buffer register, the SYNC CLK ENABLE flip-flop is cleared until it is time to generate the sync clock for the next header/data word.

NOTE

Setting the SYNC CLK ENABLE flip-flop is under control of the ring counter which is clocked by the EC0 SHIFT CLK H pulse. By counting the number of shift pulses necessary to shift a word out of the shift register (write) or into the shift register (read), the ring counter determines when the DCL is ready to receive/send another word. At the appropriate time, then, the ring counter asserts EC5 WORD IN H to set the SYNC CLK ENABLE flip-flop.

- Signal EC0 BIT 0 H – This signal is used in the SN logic to insert the header gap sync character into the shift register.

- Signal EC0 BYTE CLK H – This signal is used to clock the byte counter and to provide the shift pulses for the byte count shift register. Both of these circuits are used to implement the various control functions during read/write operations. This signal is also used to develop a decode strobe within the byte count decode logic.

2.4.3.3 Ring Counter – The ring counter is clocked by the same signal used to clock the sync clock generator (EC0 SHIFT CLK H) and to shift bits through the shift register (Figure 2-4). This counter is enabled only for the span of time when sync clock signals are to be issued to the controller; that is, for header and data fields (see discussion of sector format). The times at which this counter is enabled are governed by the "sync clock time" flip-flop in the SN logic. That is, signal SN1 SYNC CLK TIME (0) L must be asserted. When enabled, the ring counter counts the number of bits shifted out of the shift register (write) or into the shift register (read). By asserting signal EC5 WORD IN H when a word is fully assembled in the shift register, the ring counter determines when it is time to send/receive a new word. Signal EC5 WORD IN H is used to set the "sync clk enable" flip-flop in the SN logic. The latter circuit enables generation of the sync clock to the controller as described earlier.

2.4.3.4 **Byte Counter and Byte Count Shift Register** – The byte counter and byte count shift register keep track of the synchronous timing throughout the entire sector. In doing so, they provide the necessary timing signals for reading and writing bytes/words as demanded by the various sector fields (see sector format discussion). Both circuits are cleared at the start of each sector by SN6 BYTE CNT CLR L. They are also cleared at other times during a sector such as at the start of the header and data fields.

NOTE

By presetting the least significant bit of the byte count shift register to a one count and then shifting it through higher order bit positions (on each EC0 BYTE CLK), the result is effectively the same as counting bytes. Use of the byte count shift register minimizes the amount of logic required for decoding byte counts if the byte counter was used alone.

All outputs necessary for writing/reading the various sector elements are supplied from the byte count shift register and byte count decoder. The byte count decode logic is used to detect certain specific byte counts of the byte counter. Two of these are:

1. Signal SN8 BYTE 30 (36) H and SN8 BYTE 39 (47) H are used in writing/detection of the sector sync bytes. (See sector format discussion.)

2. Signal SN8 BYTE 511/575 H is decoded to detect the end of the data field.

The latter signal is applied to the byte count shift register and after being shifted seven times, it produces SN8 EOB W BYTE H. This is used to generate the end-of-block signal to the controller.

2.4.3.5 **Sync Clock Enable Control and Sync Clock Enable Flip-Flop** – As mentioned in the discussion of the sync clock generator circuits, the sync clk enable flip-flop controls the times at which the EC0 BUS SYNC CLK L signal is gated out to the controller. This flip-flop is preset by EC5 WORD IN H from the ring counter and clocked reset by EC0 SYNC CLK L occurring at the trailing edge of the sync clock signal sent to the controller. However, the sync clk enable flip-flop can only be set at certain times as governed by the following signals:

1. SN0 WRITE OR H – This allows the sync clk enable flip-flop to be clocked set at the following times:

   a. During the first four words of the header field when executing a write header and data command (formatting).

   b. During each word of the data field of both the write header and data command and the write data command.

2. SN1 READ SECTOR – This allows the sync clk enable flip-flop to be clocked set for each data field word during both the read header and data command and the read command.

3. SN0 SEND HEADER L – This allows the sync clk enable flip-flop to be preset during all commands requiring reading of the header. However, additional gating in the sync clock generator circuits inhibits issuance of EC0 BUS SYNC CLK L during the header field except when the write header and data and read-header and data command are being executed.

2.4.3.6 Sector Clock Counter and Sector Counter – The DCL employs a special counter to develop sector pulses because the disk can operate with formats of 20 or 22 sectors. To develop the sector pulse at the proper time (i.e., consistent with the number of sectors involved), the sector clock counter counts a fixed number of di-bits (issued from the disk itself and applied as MB1 SECTOR CLK H) before issuing the sector pulse (DP6 FUNC SECT CLK H). If the 22 sector format is being used, the sector clock counter counts 609 di-bit pulses before issuing the sector pulse. In the 20 sector format, it counts 672.

The sector counter itself provides two basic outputs:

1. DP6 SECTOR PULSE (1) H – This is issued every sector and is used to clear out the byte counter/byte counter shift register and to clock the sector found flip-flop.

2. DP6 SECT CNT 00 (1) H through DP6 SECT CNT 04 H – These five lines convey the current sector count to the sector compare logic.

2.4.3.7 Sector Compare Logic and Desired Sector Register – The sector compare logic detects a match between the current sector and the desired sector addressed by the controller. Detection of this matchup means that the particular sector addressed by the controller has been found. The sector compare circuit compares inputs from the sector counter (current sector count) and the desired sector register (sector addressed by controller). When the count from the sector counter matches that from the desired sector register, signal SS5 SECTOR COMP H is issued.

2.4.3.8 Sector Found Control and Sector Found Flip-Flop – These circuits detect the sector found condition when the sector matchup occurs. At this time, the sector found flip-flop issues signal SS0 SECTOR FOUND (1) H to enable the header handling logic for the header compare process.

2.4.4 Sector Format and Related Control/Synchronization Requirements

Figure 2-6 shows the component elements that make up an entire sector in the 16-bit format. It is important to understand the positioning and structure of the various format byte/word elements, since such understanding provides insight into the control sequence and synching requirements necessary for the type of operation being performed. When a disk is being formatted through use of the write header and data command, the elements shown in Figure 2-6 must be written onto the disk. When simply writing data onto or reading from the disk, detection of sync bytes, cylinder address, and verification of the header information must precede the actual data field transfer.

The entire sector consists of 609 8-bit bytes in the 16-bit format. Even when the data field contains 18-bit word (in cases where the RP04 is used with the DECsystem-10) all words preceding and after the data field are in 16-bit format.

The following breakdown describes the makeup of each sector beginning with the pre-header/sync field occurring immediately after the sector pulse:

1. Pre-header/sync field. This is a 20 word/40 byte field. It has 39 bytes of zeros followed by a sync byte ($1001\ 1000_2$). The latter defines the start of valid information.

2. Header Field. This consists of five words whose content is described below:

   Word 1 – Cylinder address and format bit used to specify any one of 411 addressable cylinders on the disk. A format bit may be set (under software control) to specify the 16-bit format.

   Word 2 – Sector/Track Address used to specify any one of 19 tracks per cylinder and any one of 20/22 sector per track depending on format. Bits 0–4 of the low order byte specify sector address while bits 8–12 of the upper byte indicate track address.

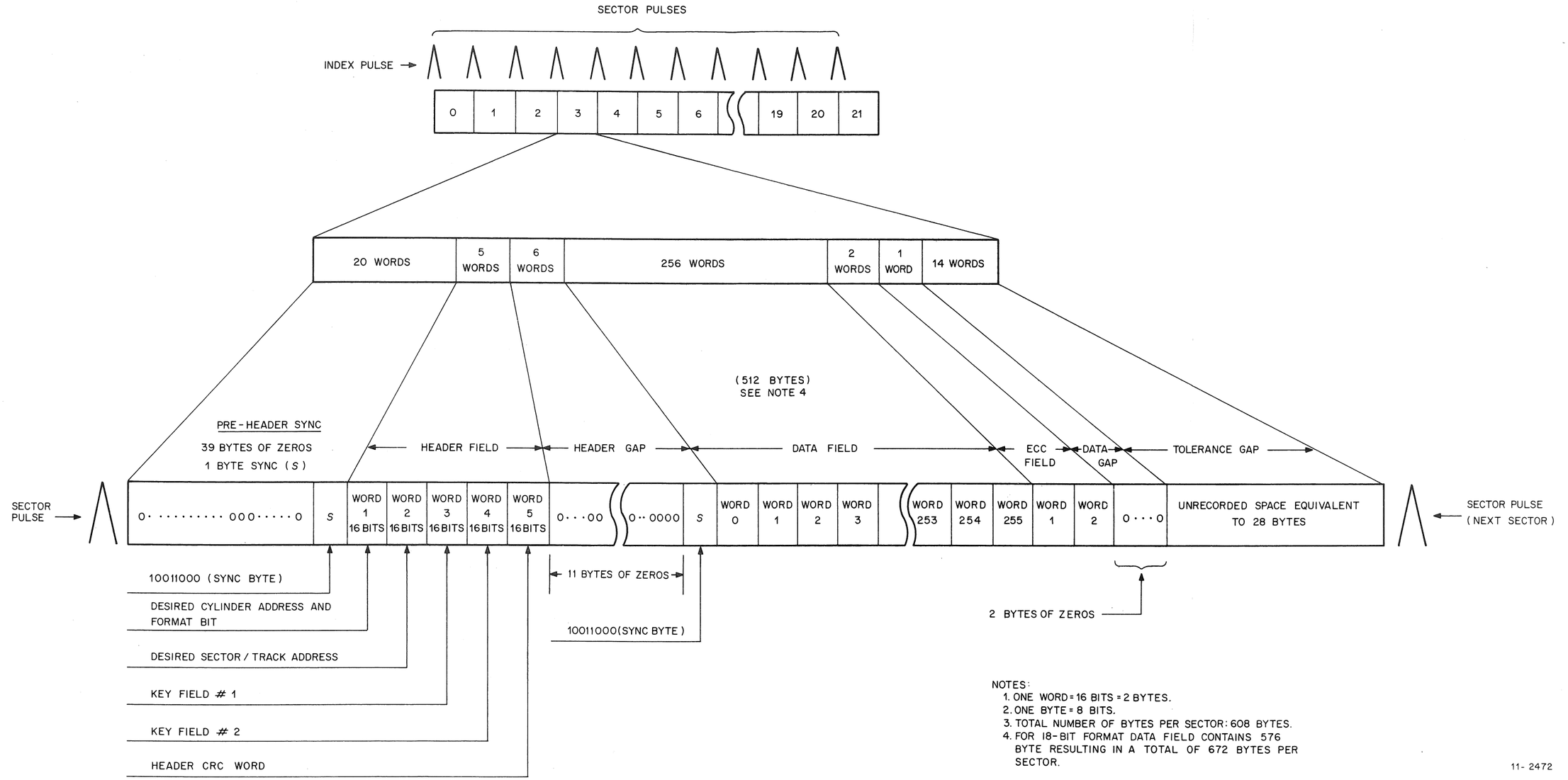


Figure 2-6 Sector Format (16 Bit Mode) Diagram

Words 3 and 4 – Key field 1 and 2 respectively are available for programming use and have no bearing on control operations within the DCL.

Word 5 – Cyclic Redundancy Check (CRC) word for header. This is generated by the DCL and then written onto the disk when formatting. It is checked by the DCL when reading from the disk to establish the accuracy of the header field content.

3. Header Gap is a 6 word/12 byte field that consists of 11 bytes of zeros followed by a sync byte. This allows time for CRC checking and to determine that a sector identification has been made when reading from the disk. The sync byte is inserted, as before, to define the start of valid information.

4. Data Field allows for writing up to 256 words of data. This is true in either 16-bit or 18-bit format. The additional space consumed in the 18-bit mode results from the fact that there are only 20 addressable sectors per track as opposed to the 22 sectors available in the 16-bit mode.

5. Error Correction Code (ECC) Field. Two words of error correction code are required due to the length of the polynomial used in the error correction process. These are generated during write operations, and are read and checked during read operations.

6. Data Gap. Two bytes of zeros are inserted after the ECC field to ensure a clean break between ECC data and the tolerance gap and to compensate for the timing differences between the DCL and the Drive.

7. Tolerance Gap consists of 14 words (28 bytes) equivalent to 34.72 microseconds. It is inserted here to compensate for mechanical tolerances.

For each element (field) making up the format, certain control sequences are required. Moreover, the control sequence implemented in the DCL can vary depending on whether the operation called for involves formatting, writing, or reading data. Table 2-2 attempts to point out some of the more salient sync and control requirements implemented during each field, consistent with the type of operation being performed; that is, formatting (write header and data), writing data only, reading header and data, and reading data only.

2.4.5 Disk Addressing Logic, Block Diagram Discussion

Figure 2-7 is a block diagram of the DCL circuits used to address and compare cylinders, tracks, and sectors on the RP04 disk. Cylinder addressing is effected when: the controller executes a seek command; the implied seek condition occurs as a result of the controller executing any read/write command; or the cylinder address is updated during an extended read/write.

Sector/track addressing is effected as part of any read/write or search command. Even though no mechanical movement of the read/write heads may be required (heads already positioned) sector/track address information is essential to the header formatting or header identification process.

Sector addressing may also be effected on execution of the search command by the controller; that is, under conditions where the operating system is cognizant that the proper cylinder (seek complete) and track have already been selected and need only be informed when the addressed sector passes under the heads.

2.4.5.1 Cylinder Addressing – Cylinder addressing begins with loading the desired cylinder address (DCA) register prior to executing the instruction (seek or read/write) that asserts the SEEK/OFFSET GO PULSE to the Drive. The cylinder address register is a 10-bit register (one bit reserved for expansion) capable of addressing any of the 411 cylinders comprised in the disk.

The cylinder address is supplied to the desired cylinder address register from the dual controller (DP) logic via the lines designated DP0 C00 AB.

Table 2-2
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
Sector Pulse	Clocks sector counter to current sector address	Clocks sector counter to current sector address		
	Clear data shift register to ensure writing of ZEROs onto disk. Clear Byte Counter prior to beginning byte count.	Provides sector compare at addressed sector	Same as write data	Same as write data
	Sets sector-found and format command flip-flops meaning that the sector to be formatted has been found.	Clears shift register		
		Clears Byte counter prior to beginning byte counter		
		Sets the sector found flip-flop (when sector count equals desired sector address) as pre-condition to initiating the header compare process.	Same as write data	Same as write data
Pre-Header Field	Sync clock signal (EC0 BUS SYNC CLK L) is sent to Controller informing it that DCL is ready to accept 1st header word.	Byte Count of 30 sets read enable flip-flop (SNIREAD ENABLE H) and sync strobe flip-flop to prepare DCL logic for sync byte detection and to enable reading of header words from disk.	Same as write data	Same as write data
	Controller responds with write clock (TA0 WRT CLK A H) to indicate that the first header word is on the data lines. First header word is strobed into the data buffer register.	Detection of sync byte indicates that DCL is now looking at header field (SSO HEADER AREA (1) H flip-flop is set)	Same as write data	Same as write data
	Zeros are written onto disk until byte counter counts to 39. At this time sync byte multiplexer is enabled to insert sync byte into shift register for writing onto disk. DCL is now prepared to accept header from controller.	Detection of sync byte also clears byte counter.	Same as write data	Same as write data
	Loading of sync byte in shift register also clears byte counter.			
	During byte count of 39, DCL initiates the following.			
	1. DCL produces SN4 BUF CLK L signal to enter first header word into data buffer register.			

Table 2-2 (Cont)
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
(Cont)	2. Sync byte is shifted out of shift regular and written onto disk in the byte 39 position. 3. After sync byte is shifted out of shift register, first header word is loaded into shift register by SN0 LOAD SR H			
Header Field 1. Cyl. Addr.	Sync clock signal is generated to controller which in turn responds with write clock to enter second header word into data buffer register. Cylinder address is shifted out of shift register and written onto disk as first header word.	First header word (current cylinder address) is read from disk into shift register and then clocked into data buffer register. First header word (current cylinder address) and desired cylinder address are compared at byte count of 02. If match exists, SS0 CYL MATCH L signal is asserted.	Same as write data except that sync clock (EC0 BUS SYNC CLK L) is asserted to send each of the four header words to controller.	Same as write data
2. Sect/Trk Addr	Sync Clock signal is generated to controller which responds with write clock to enter third header word into data buffer register (see discussion under pre-header field). Sector/track address is shifted out of shift register and written onto disk as second header word.	Second header word (sector/track address) is read from disk into shift register and then clocked into data buffer register. Second header word (current sector/track address) is compared with desired sector/track address at byte count of 04. If match exists, signal SS0 ALL MATCH L is asserted.		
3,4 Key Field words	Sync clock signal is sent to controller to initiate process for entering fourth header word into data buffer register. Third header word (now in shift register) is shifted out and written onto disk after which the 4th header word is strobed into shift register and then shifted out for writing onto disk.	Key fields are successively read from disk for entry into shift register followed by entry into data buffer register. However they are not sampled and acted upon by DCL logic.		Same as write data

Table 2-2 (Cont)
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
(cont) 5. CRC word	CRC word (generated during the 1st four words of the header field) is now written onto disk as fifth header word (this word does not go through the shift register).	CRC word from disk is clocked into CRC logic for CRC check. If error, HCRC bit in error register 01 is set. If no error header found flip-flop (SS0 HEADER FOUND (1) H) is set.	Same as write data except header found flip-flop is set at byte count of 10 even though CRC error occurs.	Same as write data
Header Gap: Byte Count 10		Clears read eanble flip-flop (SN1 READ ENABLE H) since the header identification has been made and no further word need be read from the disk as part of the write command operation.	Clears the read enable flip-flop but only temporarily as this flip-flop is again set later on in the header gap.	Same as read header and data
Byte Count 11	Clears shift register so that zeros are written onto disk for remainder of header gap (SN0 SHFT CLR L). First byte clock pulse after trailing edge of SN8 BYTE 11 (13) H signal clears and presets byte counter shift register (this is done in anticipation of writing the sync byte at the end of the header gap). Sync clock signal is sent to controller informing it to send first data field word. Controller responds with write clock which enters first data word in data buffer register.	Resets header area flip-flop since all header words have now been read from disk (signal SS0 SEARCH RESET L clocks SS0 HEADER AREA (1) H flip-flop reset). Clears SN1 HEADER ENABLE (1) H flip-flop. First byte clock pulse after trailing edge of SN8 BYTE 11 (13) H signal clears and presets byte count shift register. This is done in anticipation of writing sync byte at end of header gap.	Same as write data	Same as write data
Byte Count 15*			Clears header enable flip-flop (SN1 HEADER ENABLE (1) H since all header information has already been sampled for both read commands. Sets read enable flip-flop	Same as read header and data

*Used during read operations only.

Table 2-2 (Cont)
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
(Cont)			Sets read sector flip-flop (SN1 READ SECTOR (1) H.	Same as read header and data
			Jam presets sync strobe flip-flop (SN1 SYNC STROBE (1) H) in anticipation of detecting sync byte at end of header gap.	Same as read header and data
Byte Count 09* (Byte Count 21)	Sync byte multiplexer is enabled to insert sync into 8 low order bits of shift register (SN0 WRITE SYNC L)	Same as write header and data	Sync byte is read into shift register and detected indicating that the DCL is now ready to receive the data field.	Same as read header and data
	Sync byte is written onto disk.	Same as write header and data		
	Data envelope flip-flop is set to indicate data field and to initiate generation of the error correction code.	Same as write header and data	Data envelope flip-flop is set to indicate data field and to initiate generation of the error correction code.	Same as read header and data
	First data word is entered into shift register for writing onto disk.	Same as write header and data	Byte counter and byte count shift register are cleared	Same as read header and data
DATA FIELD Word 1	First data word is shifted out of shift register for writing onto disk.	Same as write header and data	First data word is shifted into shift register and when fully assembled in the shift register (EC5 OWRD IN H) the word is strobed into data buffer register. The DCL now generates the sync clock (EC0 BUS SYNC CLK L) to the controller informing it to take the word in the data buffer register.	Same as read header
	Sync clock signal is sent to controller informing it to send next word etc.		Once the first data word is strobed into data buffer register, the second data word is shifted into shift register etc.	

*Since the byte count shift register was cleared and preset at byte 11 time (i.e., at a time that defines the twelfth byte following the first header word) the byte count of 09 occurs after byte count 15 and for write operations defines the time that the sync byte is to be written on the disk.
a

Table 2-2 (Cont)
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
DATA FIELD (Cont) Word 256	Last data field word is shifted out of shift register for writing onto disk.	Same as write header and data		
	Last byte of data field (byte 512, EOB byte) is detected by byte count decoder.	Same as write header and data	Last data word is shifted into shift register and clocked into data buffer register. DCL then asserts sync clock to controller informing it to take last word.	Same as read header and data
	Data envelope flip-flop is now reset (SN7 DATA ENVELOPE (1) H) and ECC envelope flip-flop is set (ECC ENVELOPE (1) H).	Same as write header and data	Last byte of data field (byte 512, EOB byte is detected by byte count decoder.	Same as read header and data
	SYNC CLK TIME (1) H flip-flop is cleared since no more sync clock pulses are to be sent to the controller (SN8 EOB BYTE H).	Same as write header and data	Data envelope flip-flop is reset and ECC envelope flip-flop is set.	Same as read header and data
ECC Field	The two ECC residue words are taken from the error correction logic and written into the disk.	Same as write header and data	The two ECC words are checked to detect any error condition.	Same as read header and data
	Signal SN8 END ECC BYTE H is now generated to clear the ECC envelope flip-flop.	Same as write header and data	Signal SN8 END ECC BYTE H is now generated to clear the ECC envelope flip-flop.	
Data Gap	At the end of the data gap, signal SN8 EOB W BYTE H is generated to effect the following 1. Reset the write sector flip-flop (SN0 WRITE SECTOR (1) H 2. Trigger the end-of-block one shot multivibrator that issues the end-of-block signal to the controller (SN5 EBL (1) H).	Same as write header and data	At the end of the ECC field, the byte count shift register produces SN8 EOB W BYTE H to effect the following 1. Develop signal SN5 END ECC GTL to clear the read sector flip-flop (SN1 READ SECTOR (1) H) 2. Triggers the end-of-block one shot multivibrator that issues the end	Same as read header and data

Table 2-2 (Cont)
SECTOR FORMAT PROCESSING FOR READ/WRITE COMMANDS

SECTOR FORMAT ELEMENT	WRITE HEADER AND DATA, 63_8 (FORMATTING)	WRITE DATA, 61_8	READ HEADER AND DATA, 73_8	READ DATA, 71_8
Data Gap (Cont)	3. Clears sector area flip-flop (SN5 SECTOR AREA (1) H).		of block signal to the countroller (SN5 EBL (1) H). 3. Clears sector area flip-flop (SN5 SECTOR AREA (1) H).	
Tolerance Gap (14 words)	No action	No action	No action	No action

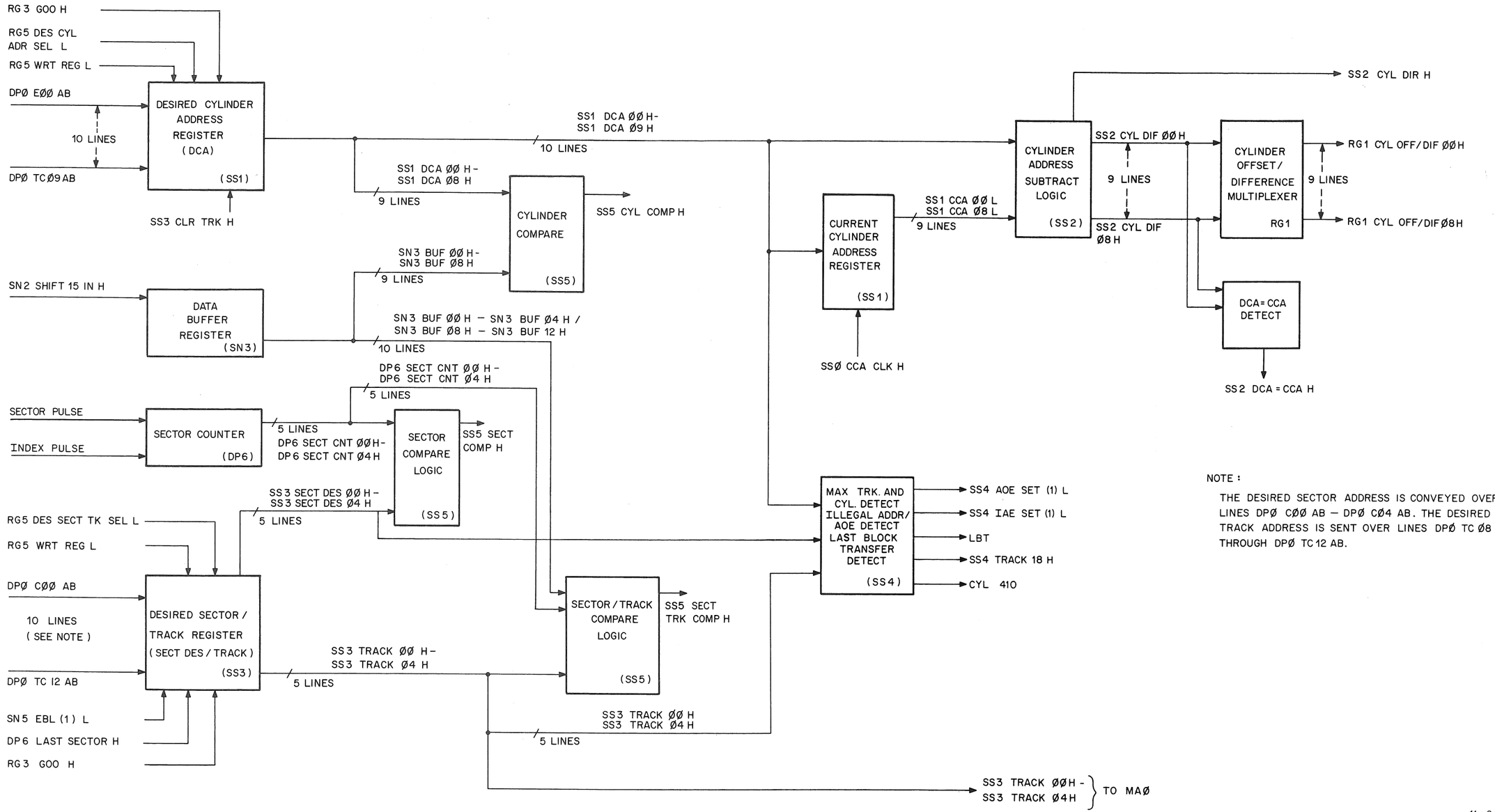


Figure 2-7 Disk Addressing Logic Block Diagram

Signal RG5 DES CYL ADR SEL L together with RG5 WRT REG L effect parallel loading of the address into the DCA register provided that RG3 G00 H is not asserted.

Once loaded, the desired cylinder address (DCA) is applied to the cylinder address subtract logic whose outputs determine the magnitude and direction of the head movement. The cylinder address subtract logic develops its outputs by subtracting the current cylinder address (CCA supplied from SS1) from the desired cylinder address (DCA) resulting in three possible computational actions:

1. If (DCA) – (CCA) is greater than zero, no borrow is generated by the cylinder address subtract logic and the direction of the head movement is forward. (In this case, signal SS2 CYL DIR H is not asserted.) The magnitude of head movement is determined by the contents of the 9 output lines, SS2 CYL DIF 00 H through SS2 CYL DIF 08 H.

2. If (DCA) – (CCA) is less than a zero, a borrow is generated by subtraction logic and the direction of drive head movement is reverse. (In this case, signal SS2 CYL DIR H is asserted.) Again, the magnitude of head movement is defined by the content of the nine difference lines.

3. If (DCA) – (CCA) is equal to zero, the output of the cylinder address subtract logic is equal to zero and no movement of the heads is initiated.

Signals SS2 CYL DIF 00 H through SS2 CYL DIF 08 H are multiplexed with the outputs of the offset register in the register logic (RG1) before being sent to the drive via the MDLI interface. These signals are also sent to the DCA = CCA detect logic, which determines if the DCA and CCA are equal. If all nine difference lines are zero, it indicates that a seek operation need not be initiated or that a seek operation has just been completed. An all zeros condition asserts signal SS2 DCA = CCA H to enable clocking the sector found flip-flop (in the SS0 logic) now that it has been determined that the heads are properly positioned.

- Substituting the Desired Cylinder Address for the Current Cylinder Address – When the outputs of the cylinder address subtract logic are received by the Drive, the Drive drops the FILE READY line and keeps it low until the head positioning process is complete. Reassertion of the FILE READY signal informs the DCL logic that the read/write heads are now positioned over the desired cylinder. The contents of the current cylinder address register must now be updated by inserting the contents of the desired cylinder address register into the current cylinder address register. The DCL logic does this by generating SS0 CCA CLK H as a high at the reassertion of the FILE READY signal. Once the substitution is completed, the desired cylinder address becomes the current cylinder address because this is where the read/write heads are now positioned. When the substitution occurs, signal SS2 DCA = CCA H is asserted.

- Cylinder Address Updating (Mid Transfer Seek) – During extended read/write operation, (e.g., when data block overlays two or more cylinders) the desired cylinder address register is incremented when transfer is complete, or when the last track of the cylinder address has been read from/written on. Clocking to update the cylinder address is provided by signal SS3 CLR TRK H.

  Updating the cylinder address means that a difference exists again between the contents of the desired cylinder address register and the current cylinder address register. As a result, the following occurs:

  1. The cylinder address subtract logic issues new outputs that are fed into the Drive over the SEEK DIRECTION LEVEL and CYLINDER DIFFERENCE OFFSET lines.

  2. A seek/offset GO signal is sent to the Drive.

  3. The Drive lowers the FILE READY line until the process of moving the heads to the newly addressed (next) cylinder is completed.

4. The drive reasserts the FILE READY line causing substitution of the desired cylinder address for the current cylinder address, etc., as described in the preceding paragraphs.

In this way, a new seek is carried out each time the contents of the desired cylinder address register are updated.

- Cylinder Overflow Detection and Invalid Cylinder Address – The DCL logic contains circuits for detecting when the cylinder address exceeds the 411 (0–410) cylinders contained in the disk. If, during an extended read/write operation, the desired cylinder address register is updated to a count exceeding 410, then the address overflow error flip-flop is set to produce signal SS4 AOE SET (1) L.

  If the operating system loads the desired cylinder address register with an invalid address (i.e., exceeding 410_{10}), then the invalid address error flip-flop is set to generate signal SS4 IAE SET (1) L.

- Cylinder Compare Logic – The contents of the desired cylinder address register are also applied to the cylinder compare logic and compared with the cylinder address read from the disk during header verification. When the cylinder address (word 1 of sector header field) read from the disk matches that contained in the desired cylinder address register, the cylinder compare logic asserts signal SS5 CYL COMP H to indicate a valid matchup. Signal SS5 CYL COMP H is used by the header handling logic as one factor in the header identification/verification process.

2.4.5.2 Track Addressing – Since all Drive read/write heads are positioned during the cylinder addressing process, no mechanical movement is necessary for track addressing. Hence track selection is effected by simply supplying the address over the five head select lines going to the drive.

The track address supplied from the controller is loaded into the desired sector/track register prior to executing the read/write command. Signal RG5 DES SECT TK SEL L (register select) ANDed with signal RG5 WRT REG L (write register) clocks the track address into the desired sector/track register. Signals SS3 TRACK 00 H through SS3 TRACK 04 H at the output of the registers convey the track address to the Drive via the interface logic. Then the Drive selects the addressed head for the read/write operation.

- Updating the Track Address – When all sectors on a particular track (20 or 22 depending on format) have been read/written during an extended read/write (e.g., transfers conveying 2 or more tracks), the track address must be updated to select the next read/write head for continuing the operation. With a read/write operation in progress, the GO bit is set and signal RG3 G00 H is asserted. This allows incrementing the track address when the transfer is complete or on transfer of the last sector of the track.

  During extended read/write operations the track address can be incremented from 0 to a maximum count of 18 (19 tracks). When a count equal to track 18 is detected in the desired sector/track register, signal SS4 TRACK 18 H is asserted. At the completion of the track 18 transfer, this signal is eventually used to clear the track bits and thereby address the first track (track no. 0) of the next cylinder.

- Sector/Track Compare Logic – When reading sector headers from the disk for header identification purposes, the contents of the second header word are compared against the track bits of the desired sector/track register (the sector bits are also compared against the output of the sector counter). This comparison occurs in the sector/track compare logic which looks at the data buffer register (contains second header word from disk) and the desired sector/track register to determine the match up. (This compare logic also receives sector count information from the sector counter.) When a match occurs, signal SS5 SECT TRK COMP H is asserted to inform the header handling logic that a valid comparison has been made.

2.4.5.3 Sector Addressing – Sector addressing occurs when the sector address is written into the sector field of the desired sector/track register. This is performed before the controller executes the read/write command. The sector field from the desired sector/track register is compared with the sector count from the sector counter. When a match occurs between the addressed sector and the count from the sector counter, signal SS5 SECT COMP H is asserted. This is important to the search logic because it initiates header comparison.

The sector field of the desired sector/track register is also updated at the completion of each sector transfer when a read/write operation is in progress. Incrementing the count is accomplished by signal SN5 EBL (1) L, which is asserted at the end of each sector after transfer is complete. Signal DP6 LAST SECTOR H (asserted to indicate last sector of a track) is used to clear the sector/track register following the transfer of last sector on a track.

2.4.6 Error Correction Code Logic Block Diagram Discussion

Figure 2-8 is a block diagram of the circuits used to implement error correction processing within the DCL. The circuits on this diagram can be looked at as performing three separate functions, all related to error correction code processing.

1. Generation of a 32-bit ECC redundancy code during write operations. This information is written serially on the disk immediately following the 256 word data field (Figure 2-6).

2. Checkout of the ECC redundancy field during read operations to detect the possible presence of a data check error. The check is made by ORing together the low order 21 bits of the ECC register and looking for a zero status.

3. Entry into the error correction process on detection of a data check error indicated by the fact that the low order 21 bits of the ECC register are not zeros. This has two immediate effects with respect to the Massbus Control Interface lines:

   - The end-of-block (EBL) signal normally inserted at the end of a sector is inhibited or delayed until completing error correction processing.

   - The datacheck error (DCK) bit in Error Register 1 is set causing the setting of the composite error bit in the status register and subsequently raising of the ATTENTION line.

Following the error correction process, the DCL detects one of two conditions:

1. Detects the 11-bit error burst and its position (physical location within the data field). The burst pattern and position information are supplied to the software operating system via the appropriate registers.

2. Determines that the error is non-correctable and sets the error correction hard (ECH) error bit in Error Register 1.

2.4.6.1 Generating and Writing the ECC Field (Write Operation) – Generating and writing the ECC redundancy code in the ECC field (Figure 2-6) occurs when the DCL executes either of the write commands. The code is formed within the ECC register during the time that the data field is written onto the disk. Each bit shifted from the shift register (for transfer to the disk) is also entered into the ECC register. This is accomplished as follows:

a. Signal SN1 WRITE COM OR H (applied to the ECC register feedback control logic) is asserted since a write operation is in progress.

b. At the start of the data field, signal SN7 DATA ENVELOPE (1) H asserts. This in turn causes signal EC3 ECC REG FDBKCTRL H to switch high and enable the ECC register feedback gating.

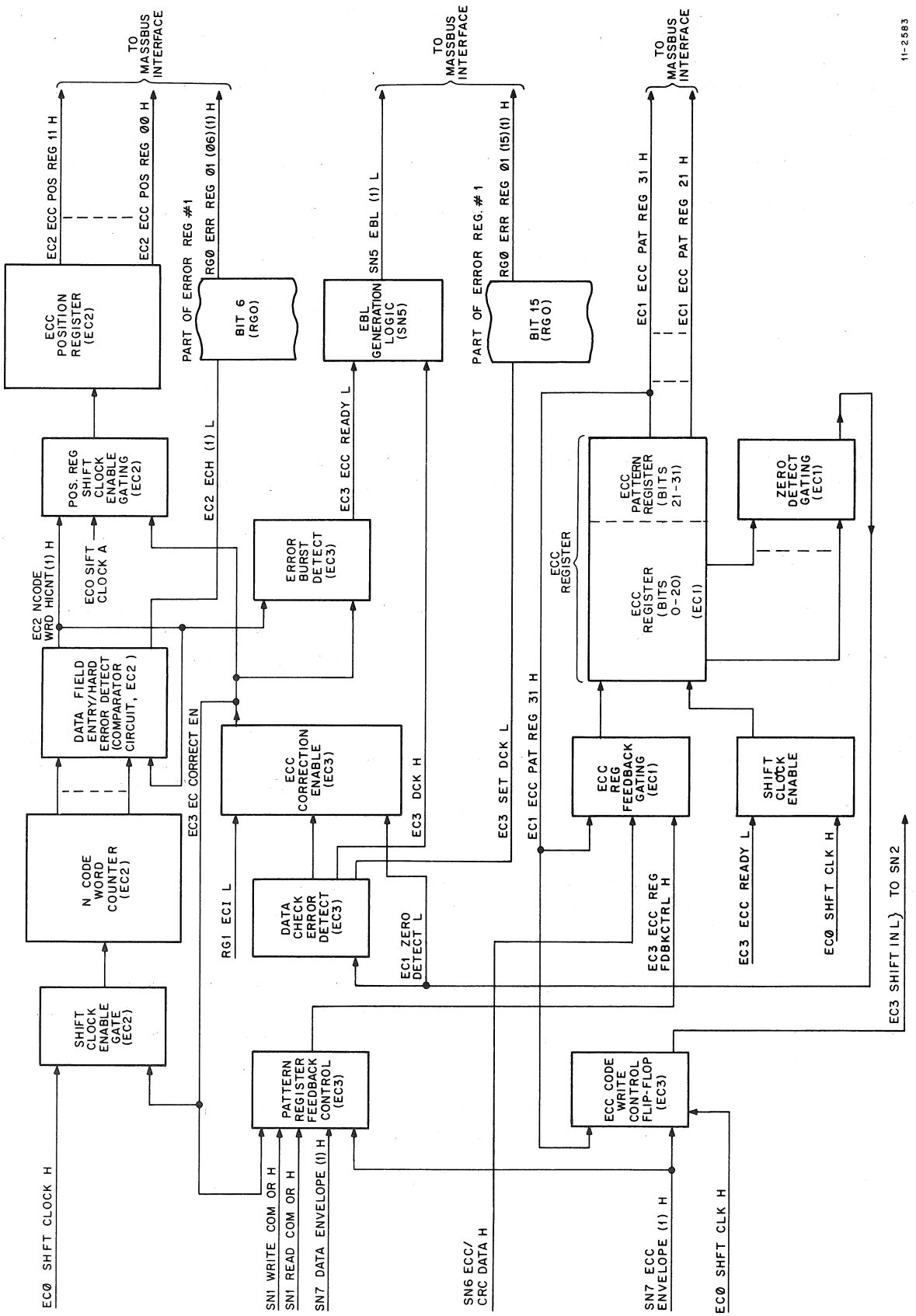


Figure 2-8 Error Correction Logic Block Diagram

ONEs and ZEROs coming from the shift register (signal SN6 ECC/CRC DATA H) now enter the ECC register throughout the data field transfer. In this way, the ECC redundancy code (to be written onto the disk following the data field) is formed. At the end of the data field, signal SN7 ECC ENVELOPE (1) H asserts because it is now time to write the ECC field associated with the data just written. The latter signal is applied to the ECC code write control flip-flop as an enabling level. Also applied to the flip-flop is the output of the ECC register (ECI ECC PAT REG 31 H). The ECC code write control flip-flop is now set/reset (consistent with the bits coming out of the ECC register) to form serial pulse train EC3 SHIFT IN L. This pulse train is written onto the disk as the ECC field.

2.4.6.2 Checkout of the ECC Redundancy Code (Read Operation) – During read operations, the ECC redundancy code is formed again by applying each data field bit read from the disk to the ECC register. When reading from the disk, the enabling of the ECC register feedback gating is effected in the following way:

a. With a read operation undertaken, signal SN1 READ COM OR H (applied to the ECC register feedback control logic) is asserted.

b. At the end of the header gap, signal SN7 DATA ENVELOPE (1) H asserts to define the start of the data field.

c. Signal EC3 ECC REG FDBKCTRL H now asserts to enable the ECC register feedback gating and thereby allows each bit coming from the disk (SN6 ECC/CRC DATA H) to enter the ECC register.

Applying each bit read from the disk to the ECC register (with the feedback loop enabled) reconstructs the same code that was attached to the ECC field when the data was written.

When the end of the data field is reached, signal SN7 DATA ENVELOPE (1) H negates; however, signal SN7 ECC ENVELOPE (1) H immediately switches high to maintain signal EC3 ECC REG FDBKCTRL H at the asserted level allowing the ECC field bits coming from the disk (SN6 ECC/CRC DATA H) to enter the ECC register while the feedback loops are still enabled.

When the ECC redundancy code read from the disk and clocked into the ECC register matches that developed (in the ECC register) at the close of reading the ECC field, then the 21 low order bits of the ECC register all contain zeros. This means that the data field has checked out OK. As a result, signal EC ZERO DETECT L asserts and sector processing is terminated normally by raising the EBL signal to the controller.

NOTE

The 21 low order bits of the ECC pattern register are inverted and then wire ORed together. When all bits are zeros, signal EC1 ZERO DETECT L asserts.

When the 21 low order bits of the ECC register fail to contain all zeros, it means that there is an error in the data read from the disk. The actual location and the nature (soft or hard) of that error is not known at this time. The DCL now enters the error correction process (provided it is not inhibited from doing so) as described in the subsequent paragraphs.

2.4.6.3 Error Correction Processing – When signal EC1 ZERO DETECT L fails to assert at the end of the ECC envelope, the data check error detect logic issues three outputs that are used as follows:

1. Signal EC3 SET DCK L asserts to set bit 15 (data check error, DCK) in Error Register 1.

2. Signal EC3 DCK H asserts. This is used in the synchronous logic to inhibit generation of the end-of-block (EBL) signal.

NOTE

If the Error Correction Inhibit (ECI) bit in the offset register is set, an EBL signal is sent to the controller even though signal EC3 DCK H asserts. The error correction process in this case, is inhibited.

3. EC3 DCK H is applied to clock the ECC correction enable logic. The latter circuit now asserts EC3 EC CORRECT EN provided that the error correction inhibit signal (RG1 ECI L) is negated.

Assertion of EC3 EC CORRECT EN begins the error correction process and has two immediate effects:

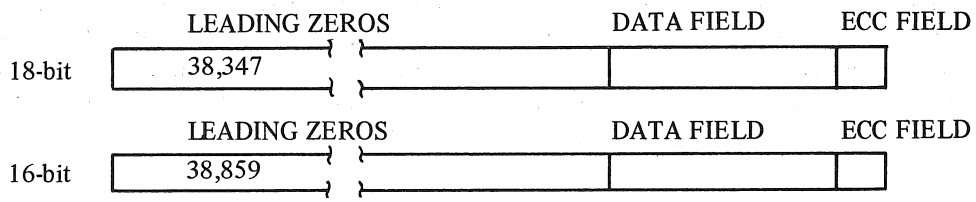
1. It asserts signal EC3 ECC REG FDBKCTRL H via the ECC register feedback control logic to enable the ECC register feedback paths. (This is essential for the error correction process.)

2. Enables clocking of the N Code word counter to maintain a count of each bit serially shifted within the ECC register.

NOTE

The polynomial used for the error correction process is capable of accommodating a data field much larger than the 256 word data field of each sector. For this reason, the DCL goes through a process of shifting leading zeros within the ECC register and feedback paths. The N Code word counter maintains a count of the leading zeros. This is done so the time at which error correction code processing enters the data field can be decoded and the task of detecting the 11-bit error burst can begin.

The number of leading zeros shifted within the pattern register depends on whether the 18-bit or 16-bit format is being used. The leading zero values are as shown below:



When the applicable number of leading zeros has been counted, the data field entry detect logic asserts signal EC2 N CODE WRD HICNT (1) H. This acts as an enabling signal to the position register shift clock enable gating. The position register keeps a count of data field bits shifted (in the ECC register) until such time as the 11-bit error burst is located. A second use of signal EC2 N CODE WRD HICNT (1) H is its application to the error burst detect circuits. Here it acts as an enabling signal, (i.e., in an anticipation of detecting the 11-bit error burst) because the shifting of bits is now within the data field.

Conditions are now set up for detecting the presence of the error burst in the 11 high order bits of the ECC register. That portion of the ECC register is also called the "ECC pattern" register. Design is such that the location of the 11 bit error burst is detected as being identified when the 21 low order bits all contain zeros (i.e., as a result of the continuous shifting/feedback process). An all zero condition is sampled in the zero detect gating and asserts signal EC1 ZERO DETECT L. On application to the ECC correction enable logic, signal EC1 ZERO DETECT L immediately negates EC3 ECC CORRECT EN to produce the following results:

a. Inhibits the position register shift clock enable gating to stop the count of the position register at that point in the data field (or ECC field). The count stored in the "ECC position" register identifies the physical location, within the data field, of the first bit of the 11-bit error burst.

b. Causes the error burst detect logic to assert signal EC3 ECC READY L. This, in turn, has a double effect:

   1. Inhibits the ECC register shift clock enable gating so that no further shifting of bits occurs in the ECC register. This is necessary because the 11 high order bits ("ECC pattern" containing the error burst) must now be sent to the central processor.

   2. Forces the EBL generation logic to send an end-of-block signal to the controller. This is done to indicate that error correction processing is complete and that the CPU may now take the contents of the ECC position and pattern registers.

c. Inhibits further counting by the N Code word counter.

This completes DCL error correction processing for those cases where the location of the error burst is detected within the data field and the error is correctable. If the error correction logic fails to detect an error burst within the data (or ECC) field, the DCL notifies the CPU of a "hard error" condition. This condition is indicated to the logic by the fact that the N Code word counter has exceeded the maximum size of the entire ECC code length without having found an all zeros condition in the low order 21 flip-flops of the ECC register.

NOTE

By definition, "hard error" means that the DCL failed to detect a correctable error burst within the data or ECC fields.

The error correction logic keeps a count of the bits being shifted in the pattern register after the shifting process enters the data field. Consequently, when the N Code word counter reaches a value of 4128_{10} bits* (following entry into the data field) it means that no error burst has been detected and the ECH bit in Error Register 1 must be set. This occurs when the data field entry/hard error detect logic determines that the count from the N Code word counter has gone past the ECC field and asserts signal EC2 ECH (1) L.

*16-bit mode. The value of 4128_{10} represents 256 words times 16 bits plus 32 bits of ECC field. In the 18-bit mode, the value for detecting a hard error is 4640_{10} (256 words times 18 bits plus 32 bits of ECC field).

CHAPTER 3
SERVICE INFORMATION

3.1 GENERAL

Because no adjustment procedures are necessary when servicing the DCL, this chapter consists entirely of detailed theory covering flow diagrams, timing diagrams, and logic diagrams within the print set. Discussions here center primarily on the flow diagrams that illustrate the step-by-step sequences used to implement DCL control operations. Certain circuit groups such as those implementing the header compare process and those involved in byte counting are also described here in greater depth.

3.2 DCL POWER SUPPLY AND POWER MONITOR

The power source for the DCL is a digital standard H764 supply located behind the hex printed circuit board nest. This power supply develops three different dc output voltages that are distributed within the DCL in the following ways:

1. +5 Vdc supplies the integrated circuit chips on all hex PCBs in the DCL. This supply also feeds logic circuits on the MDLI PCBs.

2. -15 Vdc is used in the MDLI MA0 PCB.

3. +15 V is fed to the power monitor.

The H764 power supply is turned on by throwing circuit breaker CBI at the base of the drive. When this circuit breaker is activated and power is applied to the DCL, certain control flip-flops are cleared as part of the power up process. These flip-flops are:

1. Composite error

2. Port A/Port B request flip-flops

3. Port A/Port B lock flip-flops

4. Offset mode flip-flop.

The pins, over which power is applied to each PCB, are indicated on the first page of PCB subsets making up the complete drawing set.

The power monitor unit provides a constant check of DCL voltage conditions. As long as line and dc power voltages remain within tolerance, the POWER OK signal is asserted. When the line and dc voltages fail, the AC POWER and DC POWER signals (in sequence) are raised to set error flags. The negating of the CONTROL GROUND signal occurring on a power loss informs the Drive that the DCL has lost power.

3.3 ASYNCHRONOUS DATA TRANSFER (HANDSHAKE)

3.3.1 Writing a Register

The asynchronous data transfer – write register – sequence loads one of the interface registers with data from the control bus to prepare for a command sequence (see drawing number RP04-0-28). The interface registers that can be loaded during a write register sequence are:

1. Desired Cylinder Register
2. Desired Sector/Track Register
3. Offset Register
4. Error Register 01
5. Error Register 02
6. Error Register 03
7. Maintenance Register
8. Attention Register
9. Control Register

Prior to the start of the write register sequence, the Drive unit is addressed, the register to be written is selected, and a write register sequence is specified. The Drive unit is addressed by comparing TC0 DRV SEL A with DP2 DISPLAY (1,2,4). If they match, DP2 MACH SELED A asserts, indicating that this Drive has been selected. DP2 DISPLAY (1,2,4) is the Drive unit number, in binary, as determined by the position of the three topmost Drive address switches on the DP printed circuit board. TB0 REG SEL A (00:02) and TA0 REG SEL A (03:04) decode to select the register to be written; the assertion of TA0 CTOD A specifies a write register sequence.

The write register sequence is initiated by the assertion of MASSDEM on the MASSBUS which causes DP3 REC CONT EN A to assert enabling the control bus receivers to gate the 16 control lines and parity line into the DCL. A parity check is performed and DP4 ODD PARITY asserts if the check is good.

MASSDEM also asserts DP3 SEL DEM A enabling the handshake time generator and end around counter that develops time intervals DP3 SYNC EN A, DP3 HS TIM 2 A, DP3 HS TIM 3 A, and DP3 TRANSFER A (drawing number RP04-0-29).

At time DP3 HS TIM 3 A, the selected register is written. If the attention register is selected, the Drive unit device code selects one of the first eight control lines of the control bus. If the selected line is true, DP2 CLR ATTENTION A will assert and reset the attention bit.

Writing the attention register is effected to clear the attention bit. The bit is set by any of seven conditions shown in the various command flow diagrams. The conditions are listed below along with the flow diagram in which they are shown:

1. A controller being released while a port request exists. Drawing number RP04-0-32.
2. Completion of any of the five positioning commands. Drawing number RP04-0-3,4,5,6,7.

3. Issuing of a seek command, but a seek operation is not performed. Drawing number RP04-0-3.

4. Completion of a search command. Drawing number RP04-0-8.

5. A composite error exists but no command sequence is in operation. Drawing number RP04-0-34.

6. A composite error exists and an interface register is about to be written. Drawing number RP04-0-28.

7. Whenever the Drive unit goes off line or comes on-line.

If the maintenance register is selected, RG5 ASY WRT gates the data into the register. If any of the remaining registers are selected, RG5 WRT REG gates the data into the register, but only if a command sequence is not already in progress.

When the control register is selected, bits (01:05) of the control bus assert RG3 F (0:4), which is the coded command to be executed. Bit 00 is the GO bit and asserts RG3 STO GO to enable the GO FF.

After time DP3 HS TIM 3 A, DP3 TRANSFER A asserts and is placed on the MASSBUS signifying that the control bus data has been written into the interface register. The controller responds with the negation of MASSDEM, which negates DP3 TRANSFER A to end the write register sequence. If the GO bit in the control register is set, RG3 GO asserts upon the negation of DP5 SEL DEM AB. This initiates the command sequence contained in the control register.

3.3.2 Reading a Register

The asynchronous data transfer-read-register sequence (drawing number RP04-0-30) reads one of the interface registers by accessing the register and making its contents available on the control bus. Any of the sixteen interface registers can be read during a read register sequence.

Prior to the start of the read register sequence, a read sequence is specified, the Drive unit is addressed and the desired register is selected. The negation of MASSCTOD specifies a read register sequence. The Drive unit is addressed by comparing TC0 DRV SEL A with DP2 DISPLAY (1,2,4). If they match, DP2 MACH SELED A asserts, indicating that this Drive has been selected. DP2 DISPLAY (1,2,4) is the Drive unit number, in binary, as determined by the position of the Drive address switches.

TB0 REG SEL A (00:02) and TA0 REG SEL A (03:04) asserts DP5 REG SEL AB (00:04), which decodes to select the register to be read. The desired register is selected by enabling a multiplexer which gates the register contents to the RG2 CONT OR (00:15) lines.

If the attention register is selected, an RG2 CONT OR (00:07) rendezvous is enabled. The DP2 DISPLAY (1,2,4) drive address selects one of the first eight control OR lines, if the attention bit DP2 ATA A is set, the selected line will be true.

A similar rendezvous asserts one of eight DP2 ATA A BIT (00:07) lines. However, the eight ATA A BIT lines are not gated to the MASSBUS while DP5 PORT A ON is true. If controller B had acquired the Drive, DP5 PORT A ON would be negated and the attention A bit would be gated to the control bus [MASS C (00:07)]. Thus the controller, not having control of the Drive (in this case controller B), can still read its attention register.

Controller B can access the B attention bit by asserting DP2 ATA REG SEL B even though the Drive is acquired by controller A. DP3 TRAS B EN asserts to gate out the attention bit when controller B raises MASSDEM on the B Massbus.

The read register sequence is initiated by asserting MASSDEM, which causes DP3 TRAS A EN and DP3 PARITY EN A to assert. These latter signals enable the control bus transmitters to gate the DCL to the 16 control lines and the parity line on the MASSBUS.

MASSDEM also asserts DP3 SEL DEM A, enabling the handshake timing generator that develops time intervals DP3 SYNC EN A, DP3 HS TIM 2 A, DP3 HS TIM 3 A, and DP3 TRANSFER A (drawing number RP04-0-29).

At time DP3 HS TIM 3 A, the selected register (except the attention register) is read out to the control bus. RH5 ASY READ clocks the control OR lines into the control output register asserting DP0 TC (00:07) A and DP0 TC (08:15) AB to the MASSBUS. The first eight bits of the control word route to the MASSBUS via a port A/port B multiplexer. While DP0 TC (00:07) A is routed to MASSC (00:07) of MASSBUS A, the multiplexer is routing the B attention bit to MASSC (00:07) of MASSBUS B.

After time DP3 HS TIM 3 A, DP3 TRANSFER A asserts and is placed on the MASSBUS signifying that the contents of the selected register are now on the control bus. The controller responds with the negation of MASSDEM, which negates DP3 TRANSFER A to end the read register sequence.

3.3.3 Dual Control

3.3.3.1 Port Acquisition (drawing number RP04-0-31, 33A) – If the Drive unit is in the neutral state, controller A can acquire control of the Drive by addressing it and asserting MASSDEM. If the controller requests a read register, MASSDEM holds the Drive for the HANDSHAKE read register sequence. When MASSDEM negates, the Drive returns to the neutral state. If the register selected is the control register, or the controller requested a write register sequence, a port A request latch is set during the handshake. When MASSDEM negates, the port request latch continues to hold the Drive until a port release command is issued or a one second time-out elapses, whichever comes first.

If controller B has control of the Drive when controller A makes its request, the port A request latch is still set. When controller B releases the Drive, the port A latch causes controller A to automatically acquire control of the Drive.

The Drive unit is addressed by comparing TC0 DRV SEL A (00:02) with DP2 DISPLAY (1,2,4). If they match, DP2 MACH SELED A asserts, signifying that this Drive has been selected. DP2 DISPLAY (1,2,4) is the binary representation of the Drive unit number as determined by the position of the three topmost drive address switches on the DP printed circuit board.

Port Acquisition is initiated by the assertion of MASSDEM. DP3 SEL DEM A asserts and enables the handshake timing generator – and end-around counter that develops time intervals DP3 SYNC EN A, DP3 HS TIM 2 A, and DP3 HS TIM 3 A (drawing number RP04-0-29). At time DP3 SYNC EN A, if DP5 PORT B ON is negated, controller A acquires the Drive in sync with handshake clock A and asserts DP5 PORT A ON.

DP3 SYNC EN A also asserts DP3 INHIBIT A SET, which inhibits controller acquisition during the latter part of the handshake cycle. The asynchronous transmitters and receivers are not enabled until DP5 PORT A ON is true. They must be enabled early in the handshake cycle to gate the control bus to the DCL and allow time for the interface register to be accessed.

At time DP3 HS TIM 2 A, a port request is made if controller A requests a write register sequence or requests to read the control register when controller B does not have control of the Drive (neutral state). Once DP5 PORT A REQ is asserted, the request state is held until controller B releases control and DP5 PORT B ON is negated. When this occurs, controller A acquires the Drive and DP5 PORT A ON asserts. A port request is made at time DP3 HS TIM 3 A if the attention bit has cleared (DP2 CLR ATTENTION A asserted).

3.3.3.2 **Port Release (drawing number RP04-0-32, 33B)** – In the referenced port release flow diagram, a condition is assumed to controller A having control of the Drive unit with DP5 PORT A ON asserted.

One means of releasing port control is via a release command sequence. When the GO FF is set, RG3 RELEASE COM asserts and sets the DP5 RELEASE A FF. This resets the DP5 PORT A REQ FF and two handshake clock cycles later, DP5 PORT A ON is negated. If a port B request exists, controller B acquires the Drive and DP5 PORT B ON asserts in sync with handshake clock B (50 ns later).

A port release also occurs if DP5 SEL DEM AB is asserted longer than one second under conditions where no command sequence is in progress. In this case, the DP5 RELEASE A FF sets and the release sequence just described occurs.

3.3.3.3 **Simultaneous Controller A and Controller B Demands (drawing number RP04-0-33, C)** – The referenced diagram illustrates the condition where MASSDEM is asserted simultaneously by controllers A and B. Noting that handshake clocks A and B are 180-degrees out-of-phase, the diagram shows that the controller whose clock has the next rising edge (following the assertion of DEMAND) seizes the control. The acquisition sequence is as shown in drawing number RP04-0-31. Drawing number RP04-0-33, C shows those time periods when simultaneous demands would seize controller A and the alternate periods when controller B would be seized.

3.4 MECHANICAL MOVEMENT

3.4.1 Seek

The seek sequence positions the Drive unit heads over the cylinder whose address is contained in the desired cylinder address register. When a seek command is to be executed, the contents of the desired cylinder address (DCA) register and the current cylinder address (CCA) register are compared. If a difference exists, a seek is performed to reduce the difference to zero. If a sector search or any synchronous data transfer command is issued, the desired cylinder address and current cylinder address registers are examined. If DCA $\neq$ CCA, an implied seek is performed before the command is executed.

3.4.1.1 **Seek Flow (drawing number RP04-0-3, 12)** – The GO FF is set, asserting RG3 GO and starting the seek command sequence. RG3 SEEK COM is decoded from the function code in the control register. If DCA = CCA, a seek is not required; the command is terminated by resetting the GO FF and setting the attention bit.

A bad address (SS4 BAD ADDR) also inhibits the SEEK sequence and causes a command termination. SS4 BAD ADDR asserts if the desired cylinder address is greater than 410, the track address is greater than 18, or the desired sector is greater than 19 (18-bit mode, 21 in the 16-bit mode).

The RP04 does not execute a SEEK while in the offset mode. If the RP04 is in the offset mode and a seek command is issued, SS0 SS RTC is asserted and the flow branches into a return to centerline process. This causes return of the heads to track centerline and takes the RP04 out of the offset mode. Exit from the return-to-centerline process occurs on the negation of RG5 OFFSET MD.

RG5 MOV COM is asserted by SS0 SEEK GO and enables an end-around counter. The counter is clocked by DP6 FUNC SECT CLK and develops move timing gate RG5 MOV TIM 1, RG5 MOV TIM 2, and RG5 MOV TIM 3. After the three timing gates have been developed, the counter resets to its initial state until another RG5 MOV COM is issued (Figure 3-1).

RG5 MOV TIM 2 asserts RG5 SEEK/OFFSET GO which triggers the seek operation within the Drive unit. When the Drive has completed the seek operation and the heads are positioned over the desired cylinder MB0 FILE READY is asserted. MB0 FILE READY terminates the command by resetting the GO FF and setting the attention bit. SS0 CCA CLK is asserted and transfers DCA into the current cylinder register making DCA = CCA.

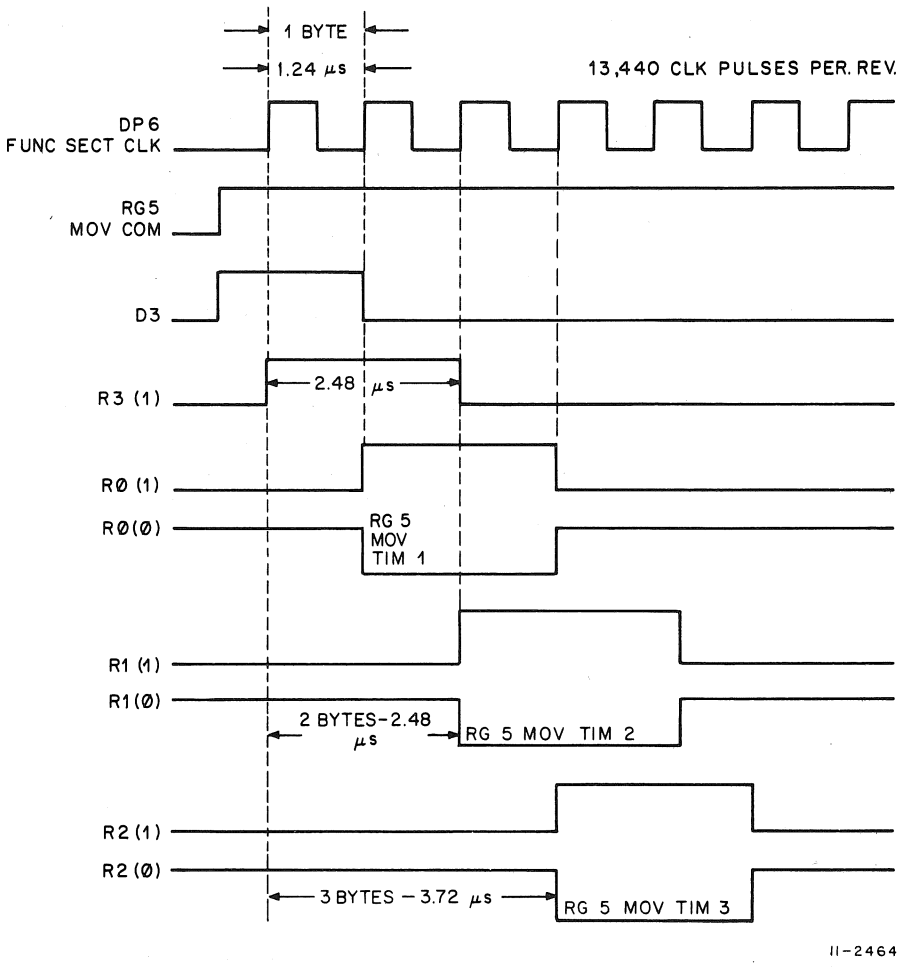


Figure 3-1 Move Timing Diagram

3.4.1.2 Implied Seek (Figure 3-2) – The seek flow (RP04-0-3) can be entered from a sector search flow. When a sector search sequence (or read/write operation sequence) is initiated and DCA ≠ CCA, the sequence is held up until an implied seek is performed and DCA = CCA. After SS0 CCA CLK sets DCA = CCA, the implied seek process is complete. Command termination (setting attention bit and resetting the GO FF) does not occur because a positioning command does not exist.

3.4.1.3 Mid-Transfer Seek – During a spiral read or write operation, when the last sector of the last track of a given cylinder has been read (or written), a seek is needed to move the heads to the next cylinder. SS4 TRACK 18 HOLD, SS3 EBL, and DP6 LAST SECTOR assert SS1 DCA CLK to increment the desired cylinder address register causing a difference of 1 between DCA and CCA. The next read (or write) sequence asserts SS0 SEEK OR (via a sector search sequence) to initiate an implied seek sequence. After the heads have moved to the next cylinder, DCA again equals CCA and the read (or write) operation can continue.

3.4.2 Offset

The offset sequence displaces the heads slightly off of track centerline by a specified amount and in a specified direction by the data contained in the offset register. The heads remain offset until a return to centerline command (issued directly or implied) is issued.

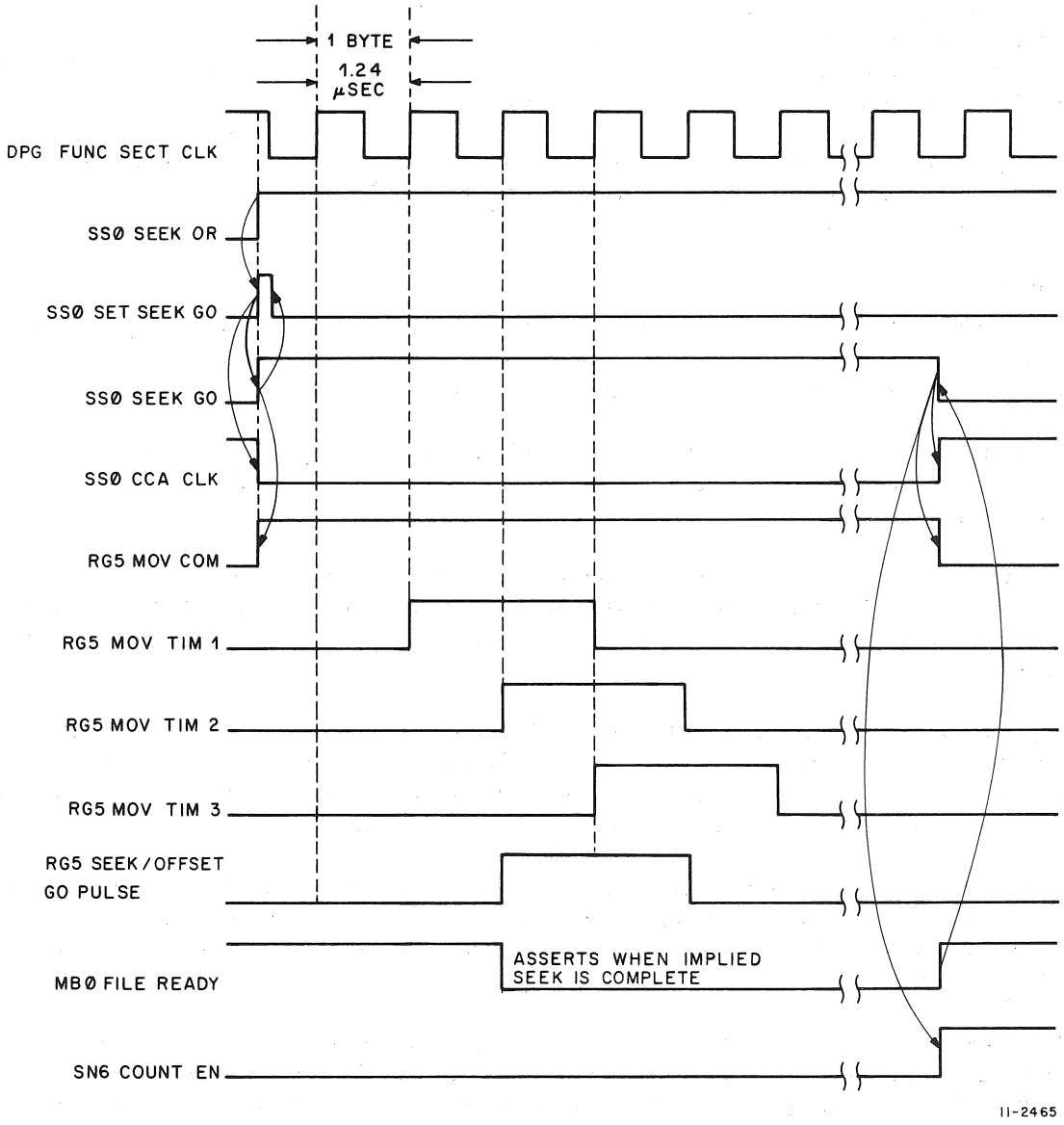


Figure 3-2 Implied Seek Timing Diagram

3.4.2.1 Offset Flow (drawing number RP04-0-4, 13) – The GO FF is set, asserting RG3 GO and starting the offset command sequence. RG3 OFFSET COM is decoded from the function code in the control register. RG5 OFFSET MODE and RG5 OFFSET MD assert and remain asserted for as long as the heads are in an offset position.

RG5 MOV COM is asserted by RG3 OFFSET COM and enables the end-around counter. The counter is clocked by DP6 FUNC SECT CLK and develops move timing frames RG5 MOV TIM 1, RG5 MOV TIM 2, and RG5 MOV TIM 3. After the three timing signals have been developed, the counter resets to its initial state until another RG5 MOV COM is issued.

RG5 MOV TIM 2 asserts RG5 SEEK/OFFSET GO which triggers the offset operation within the Drive unit. When the Drive has completed the offset sequence and the heads are offset from centerline by the desired amount, MB0 OFFSET READY is asserted by the Drive. MB0 OFFSET READY terminates the command sequence by resetting the GO FF and setting the attention bit.

The sequence shown in drawing number RP04-0-4 offsets the heads by the amount specified in the offset register. If the heads are to be offset a different amount, or in the other direction, the new OFFSET value is placed into the offset register (in a handshake operation). Then the OFFSET command is issued and the sequence of drawing number RP04-0-4 is repeated. The sequence is completed when the heads are over the new offset position.

While moving the heads to the new offset position, the offset mode FF remains set and RG5 OFFSET MODE and RG5 OFFSET MD remain asserted. They are negated only when an offset reset pulse is asserted and the Drive executes a return to centerline sequence.

3.4.3 Return-to-Centerline

Execution of a return to centerline sequence returns the Drive heads from an offset position to track centerline. The sequence can be initiated by a return-to-centerline command in the control register or an implied return to centerline derived from a seek command or either of the synchronous write commands.

3.4.3.1 Return to Centerline Flow (drawing number RP04-0-5, 14) – The GO FF is set, asserting RG3 GO and starting the return-to-centerline command sequence. RG3 RET TO CL COM is decoded from the function code in the control register.

RG5 MOV COM is asserted by RG3 RET TO CL COM and enables an end-around counter. The counter is clocked by DP6 FUNC SECT CLK and develops move timing signals RG5 MOV TIM 1, RG5 MOV TIM 2 and RG5 MOV TIM 3. After the three timing signals have been developed, the counter resets to its initial state until another RG5 MOV COM is issued.

During RG5 MOV TIM 1, RG5 OFFSET RES PULSE is asserted and initiates the return to centerline operation within the Drive. When the Drive has completed the RETURN-TO-CENTERLINE operation and the heads are positioned over the track centerline, the MB0 OFFSET READY signal is asserted by the Drive. MB0 OFFSET READY terminates the sequence by resetting the GO FF and setting the attention bit.

3.4.3.2 Implied Return to Centerline (Figure 3-3) – The return to centerline flow process can be entered from a seek flow or from either of the write flows. The respective flow will assert SN1 RTC and a return to centerline sequence will be carried out. When the sequence is completed, RG5 OFFSET MD is negated and a return is made to the SEEK or the WRITE flows.

Note that in Figure 3-3, signal RG5 OFFSET MODE is negated at MOV TIM 3 while RG5 OFFSET MD is held true until MB0 OFFSET READY is asserted. The negation of RG5 OFFSET MODE at MOV TIM 3 causes the negation of RG5 MOV COM early in the sequence. If the implied RETURN TO CENTERLINE originated from a SEEK flow, the SEEK command is waiting for the negation of RG5 OFFSET MD to assert RG5 MOV COM for the SEEK sequence timing. The early negation of RG5 MOV COM ensures that it will have settled in the negated state when the SEEK command asserts it for the SEEK timing.

3.4.4 Recalibrate

The recalibrate command sequence is intended to position the Drive heads over cylinder 000 while clearing current cylinder address register.

3.4.4.1 Recalibrate Flow (drawing number RP04-0-6, 15) – The GO FF is set, asserting RG3 GO and starting the recalibrate command sequence. RG3 RECAL COM asserts from the function code in the control register.

RG5 MOV COM is asserted by RG3 RECAL COM and enables an end-around counter. The counter is clocked by DP6 FUNC SECT CLK and develops move timing signals RG5 MOV TIM 1, RG5 MOV TIM 2, and RG5 MOV TIM 3. After the three timing signals have been developed, the counter resets to its initial state until another RG5 MOV COM is issued.

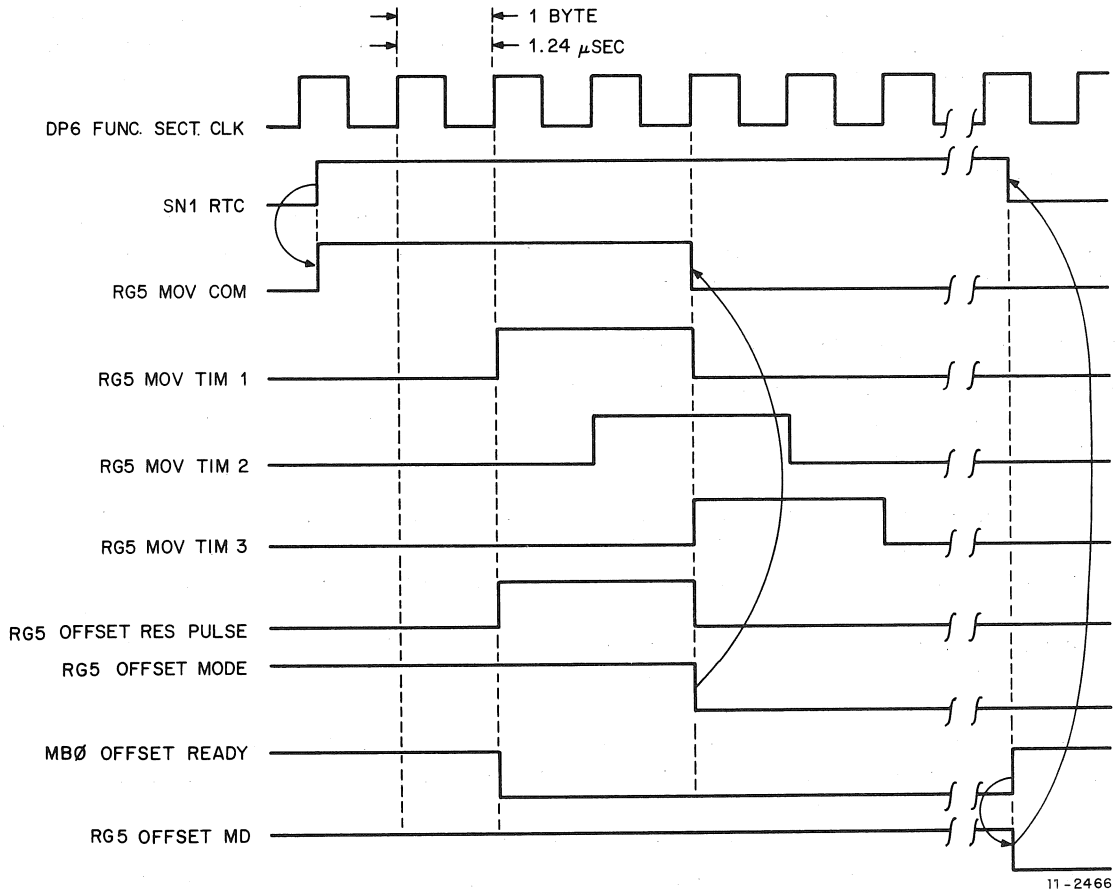


Figure 3-3 Implied Return to Centerline Timing Diagram

RG5 MOV TIM 1 asserts RG5 RECAL PULSE which starts the RECALIBRATION operation within the Drive unit. The latter signal also clears the current cylinder address register (CCA). When the Drive has completed the recalibrate operation and the heads are centered over cylinder 000, the MB0 FILE READY is asserted by the Drive. MB0 FILE READY terminates the command sequence by resetting the GO FF and setting the attention bit.

3.4.5 Unload

An unload command causes the Drive unit to retract the heads and the spindle to cycle down. When the STNDBY button is pressed the spindle will cycle up to speed and the heads will load completing the unload sequence.

3.4.5.1 Unload Flow (drawing number RP04-0-7, 16) – The GO FF is set, asserting RG3 GO and starting the unload command sequence. RG3 UNLOAD COM is decoded from the function code in the control register.

RG3 UNLOAD COM asserts DP4 DEV IN STNBY, which initiates the Drive unit cycle down process. Cycling down the Drive unit causes the heads to retract and the STANDBY light to illuminate. MB1 ON LINE now negates indicating that the disk pack is unavailable.

Operator intervention is required to finish the command sequence. Pushing the STANDBY button initiates the cycle-up process. After the heads are loaded and the spindle has come up to speed, signals MB1 ON LINE and MB0 FILE READY are asserted. MB0 FILE READY terminates the sequence by resetting the GO FF and setting the attention bit.

3.5 SECTOR SEARCH

The sector search sequence functions to locate the desired sector loaded into the desired sector/track address register. A sector timing circuit produces a count of the sectors as the disk rotates. The count is compared to the desired sector, and if they match, a sector found signal is asserted.

3.5.1 Sector Timing (drawing number RP04-0-11, 17)

A multiplexer selects the index pulse and sector clock either from the Drive unit or from the diagnostic circuitry. At the beginning of a disk revolution, DP6 FUNC INDEX PULSE will set the sector pulse FF and reset the sector clock counter and the sector pulse counter.

The sector clock counter starts a count of sector clocks and outputs the count to the sector clock decoder. The decoder looks for a binary count of 608* or 671* (depending on the format) signifying that the sector is completed. When this occurs the clock counter is reset and a sector pulse is generated to start the next sector.

The sector pulses are counted and decoded for a sector pulse count of 19 or 21 (depending on the format) as the last sector signifying that the disk has completed a revolution.

During the last sector, the sector pulse FF is inhibited from setting through normal clocking. On occurrence of the index pulse, the sector counter is cleared and the sector pulse flip-flop is set to assert sector pulse No. 0.

3.5.2 Sector Search Flow (drawing number RP04-0-8 and Figure 3-4)

The GO FF is set, asserting RG3 GO and starting the SEARCH command sequence. RG3 SEARCH COM asserts from the function code in the control register. If an illegal address is decoded in either the DCA register or the sector/track register, the illegal address error (IAE) bit is set and the command is aborted. If the addresses are legal but DCA $\neq$ CCA, an implied seek is executed. The implied seek process is entered by asserting SS0 SEEK OR but does not progress any further unless DCA $\neq$ CCA. When the implied seek has been executed and DCA = CCA, the flow exits back to the sector search flow.

At the leading edge of each sector pulse, the sector counter is incremented. If the output of the sector counter matches the desired sector address, signal SS5 SECTOR COMP H is asserted. At the trailing edge of the same sector pulse, the SS0 SECTOR FOUND flip-flop is set. Signal SS0 SEARCH COMP is the asserted sequence by resetting the GO flip-flop and asserts the attention bit.

3.5.3 Implied Search

If any of the four synchronous data transfer commands are initiated, an implied search is executed. RG3 READ COM, RG3 READ HD DT COM, or RG3 WRITE COM asserts SN1 HEADER ENABLE while RG3 WRT HD DAT COM asserts SN0 SECTOR SEARCH. Both header enable and sector search initiate a search sequence. Exit for both of the implied search flows is SS0 SECTOR FOUND.

3.6 WRITE HEADER AND DATA FLOW DIAGRAM DISCUSSION

Drawing RP04-0-26 shows the flow sequence for the write-header-and-data operation (used to format the disk) from the time command setup occurs until the desired number of sectors have been formatted. A timing diagram, showing principal control pulses occurring within a sector, is also provided in drawing RP04-0-24.

*Since a count of zero is given significance, the actual count is one greater than that decoded; i.e., 609 or 672.

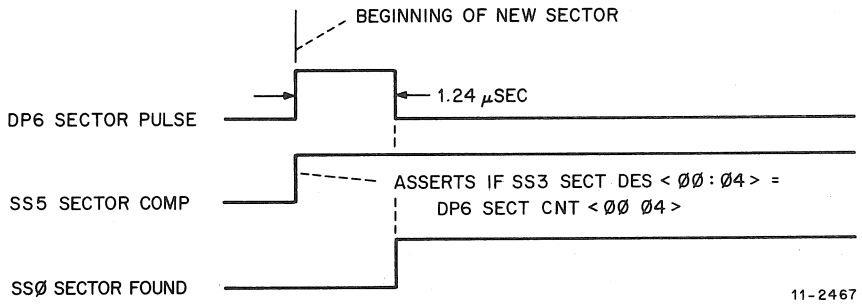


Figure 3-4 Sector Search Timing Diagram

3.6.1 Command Setup

The write header and data command is initiated when the control register is loaded with a function code of (63_8). This sets the RG3 GO FF allowing the function code decoder to assert RG3 WRT HD & DAT. The setting of the GO FF also asserts RG3 G00 which is sent over to the Drive as MODULE SELECT to indicate that this particular Drive has been selected by the controller. The RG3 COM ENA FF is set when the controller raises the RUN line (EC 9 RUN). This causes assertion of RG3 WRT HD DAT COM which, in turn, produces the following:

1. Asserts signal SN1 WRITE COM OR H. This is used later (during the sector header gap) to set the write sector FF.

2. Generates signal SN0 WRT HD EN to set the SN0 SECTOR SEARCH FF. With the sector search flip-flop set, the process of detecting the addressed sector begins now.

3.6.2 Sector Search/Sector Found

If at this time, the contents of DCA are not equal to CCA, an implied seek operation is executed before returning to the flow process shown on RP04-0-26. If signal SS0 DCA = CCA is already asserted (which results when the implied seek is completed), detection of the desired sector is initiated. Signal SS0 SECTOR COMP asserts at the leading edge of the sector pulse if the sector count matches the desired sector address. At the trailing edge of the same sector pulse, the sector found flip-flop is set.

3.6.3 Pre-Header Field

Setting the sector found flip-flop initiates pre-header field processing as follows:

1. The sector search flip-flop is cleared triggering a one shot to generate signal SN0 GT LD SYNC CLK. This signal forces the first EC0 BUS SYNC CLK which (following receipt of the write clock) results in loading the first header word into the data buffer register.

2. The SN0 FORMAT COM FF is set, asserting signal SN0 WRITE OR. This enables the write gating logic, and also asserts signal MA0 WRITE COMMAND LEVEL to inform the Drive that a write operation is to begin.

3. As a result of the sector pulse, the byte counter is reset to a count of zero, while the data shift register is cleared. As the byte counter counts up from this time on, a pre-header gap of 39 bytes of zeros is allowed to pass through the shift register and onto the disk.

3.6.3.1 Writing the Sync Byte – At byte 39 time, signals SN0 WRITE SYNC and SN0 LOAD SR are asserted to load the sync byte into the shift register. At this time, the process of serially shifting the sync byte onto the disk is begun.

3.6.4 Header Setup Operations and Writing the Header

As the sync byte is being shifted serially onto the disk, various timing operations are being set up to strobe the header words from the controller into the DCL and then onto the Drive. These are as follows:

1. SN1 SYNC CLK TIME flip-flop is set to enable the ring (word-in) counter and the SN1 SYNC CLK EN flip-flop. In general, this signal envelopes a period when sync clocks are to be generated.

2. EC5 WORD IN (produced by the ring counter) will assert four times during the header area. Each assertion loads a header word from the data buffer register into the shift register through generation of SN0 LOAD SR. The loading occurs when a complete word has been shifted out of the shift register.

3. While the serial shifting is in process, the data buffer register is parallel loaded with the next header word received from the controller. Signal EC0 BUS SYNC CLK is asserted three more times. (The first assertion occurred earlier in the pre-header area.) Each assertion results in a SN8 WRITE CLK signal and then a SN4 BUF CLK signal. The latter signal parallel loads a word from the controller into the buffer register.

4. At byte 5 time (when all header information has been obtained from the controller), the SN8 SYN CLK STOP flip-flop is set to inhibit further generation of sync clocks.

5. At byte 8 time after the second key word has been recorded onto the disk, the SN7 CRC WORD flip-flop is set to allow the CRC word to be written. Signal SS7 CRC IN represents the CRC word in serial form. The cyclic redundancy check (CRC) word is the last header information written onto the disk.

   Also at byte 8 time, SN0 FORM SYNC TIME CLR asserts to reset the SN1 SYNC CLK TIME FF, clearing the ring counter and the SN1 SYNC CLK EN flip-flop.

6. At byte 10 time, all header information has been recorded and the SN7 CRC WORD flip-flop is reset. A header gap of bytes of zeros follows.

3.6.5 Header Gap

A header gap of bytes of zeros separates the header field and the data field sync byte. The byte counter is allowed to continue the header field count up to byte 11. At this point, SN0 WRITE COM SET asserts to produce the following:

1. The byte counter is reset by SN0 BYTE CNT SYNC CLR and allowed to count up to byte 9 for a total of 21 bytes before the data field sync byte is to be written.

2. The SN0 WRITE SECTOR flip-flop is set to maintain the assertion of SN0 WRITE ENABLE and MA0 WRITE COMMAND LEVEL. At this point, SN0 FORMAT COM flip-flop is cleared.

3. Signal SN0 WRITE COM SET also triggers a one shot to assert signal SN0 GT LD SYNC CLK. This in turn forces a EC0 BUS SYNC CLK to the controller. As a result, the first data word is loaded from the controller into the data buffer register.

3.6.5.1 Data Field Sync Byte – At byte 9 time the data field sync byte is being written. Immediately following the sync byte is the 256-word data block. The synchronous clocking is almost identical to that described in Paragraphs 3.6.3.1 and 3.6.4. Assertion of SN0 WRITE SYNC at byte 9 time enables the sync byte to be written onto the disk.

3.6.6 Data Field

After the sync byte is written, a total of 255 more EC0 BUS SYNC CLK signals are generated. After the last data word has been loaded into the buffer register from the controller, the SN7 SYNC CLK STOP flip-flop is set to

inhibit sync clock generation. After the complete data block has been transferred (at byte count 512), SN8 EOB BYTE is asserted to reset SN0 SYNC CLK TIME flip-flop, disabling the ring counter and SN0 SYNC CLK EN flip-flop. The SN7 DATA ENVELOPE flip-flop is set at the beginning of the data block and is reset at the end of the data block. This signal enables the generation of the two ECC words that follow the data block.

3.6.7 Error Correction Code (ECC) Field

At the end of the data block, when SN8 EOB BYTE resets SN7 DATA ENVELOPE flip-flop, it also sets the SN7 ECC ENVELOPE flip-flop. As a result, EC3 SHIFT IN, which is the serial representation of the two ECC words, is asserted. This signal is written onto the disk as the ECC field before the SN7 ENVELOPE flip-flop is reset by SN8 END ECC BYTE.

3.6.8 Data Gap

A data gap of two bytes of zeros is written following the ECC Field. This occurs before the complete write control logic is reset by the assertion of SN8 EOB W BYTE. At the assertion of this signal, the SN0 WRITE SECTOR flip-flop is reset disabling SN0 WRITE ENABLE and MA0 WRITE COMMAND LEVEL; at the same time, SN5 END COM triggers the SN5 EBL one-shot signaling that the sector transfer is completed. Then EC9 RUN is sampled to determine if the transfer is to continue. If EC9 RUN is asserted, SN5 COM CONT sets the SN0 SECTOR SEARCH flip-flop and re-initiates the complete process. If EC9 RUN is not asserted, signal SN5 RESET GO resets the GO FF and terminates the command.

3.7 HEADER COMPARE PROCESS (drawing number RP04-0-9, 19 and Figure 3-5)

The header compare process is entered from any synchronous data transfer command flow except write header and data. The purpose of this process is to compare and verify the header read from the disk against the desired cylinder, desired sector, desired track and the format bit. A CRC check is also performed on the header data. If the desired cylinder, sector, and track address match the header address, and the CRC check is good, SS0 HEADER FOUND is asserted which returns the flow back to the basic command.

The process is initiated by SN1 HEADER ENABLE which asserts from RG3 WRITE COM, RG3 READ COM, or RG3 READ HD DT COM.

Before a header compare can take place, the desired sector must be found. The sector search process locates the desired sector and asserts SS0 SECTOR FOUND at the trailing edge of the sector pulse. The sector pulse resets the byte counter which starts a byte count of the pre-header field.

When byte 30 of the pre-header field is reached, SN1 READ ENABLE enables the DCL read logic circuits. At this time, SN1 SYNC STROBE is asserted to allow the sync byte to be detected by the sync byte decoder. When the logic recognizes the sync byte, signal SN7 SYNC CLR is asserted to clear the CRC logic before the header words are shifted in. SN7 SYNC CLR resets the byte counter to begin a byte count of the header. It also enables the ring (word in) counter to count serial data bits and assert EC5 WORD IN to load a complete 16-bit word from the shift register into the data buffer. Each time a word is loaded, a sync clock is developed. The bus sync clocks are sent to the controller only during the read header and data command. The first header word loaded into the data buffer by EC5 WORD IN contains the format bit and the cylinder address. (If the format bit, bit 12, does not match the format bit contained in the offset register, SS0 FMT ERR SET will assert.) If the cylinder address matches the desired cylinder address contained in the desired cylinder address register, SS0 CYL MATCH asserts.

The second header word strobed by EC5 WORD IN is the header sector/track address. If these match the desired sector and track addresses (in the desired sector/track address register), signal SS0 SECT TRK MATCH asserts.

The third and fourth header words are key words and are not verified by hardware. After the key words are read, if either SS0 CYL MATCH or SS0 SECT TRK MATCH has not been asserted, SS0 HCE (header compare error) is asserted.

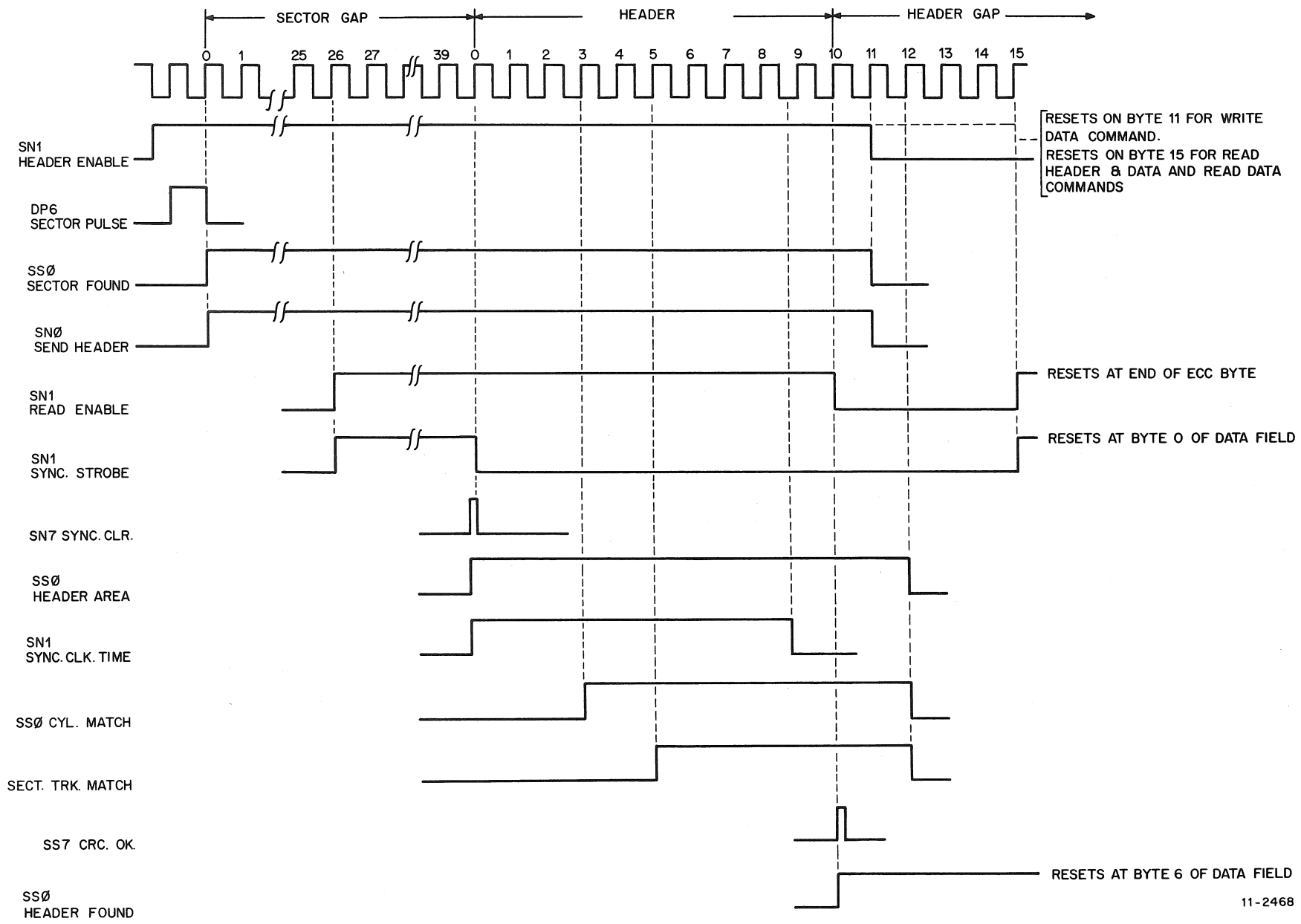


Figure 3-5 Header Compare Timing Diagram

If no HCE is detected, the CRC word (fifth header word) is shifted serially into the CRC logic for the check. A byte 10 of the header field, SS7 CRC OK, asserts if the CRC checked out properly. Then SS0 HEADER FOUND asserts and an exit is made from the header compare flow. If a CRC error is detected, SS0 HCRC set is asserted.

3.8 WRITE DATA FLOW DIAGRAM DISCUSSION

Illustrations of the write header command flow and timing are given in drawings RP04-0-27 and RP04-0-25 respectively.

3.8.1 Command Setup

The write data command is initiated when the control register is loaded with a function code of (61_8). This sets the RG3 GO FF, allowing the function code decoder to assert RG3 WRT DAT. Setting the GO FF also asserts RG3 G00, which is sent over to the Drive as MODULE SELECT to indicate the particular Drive that has been selected. RG3 COM ENA FF is asserted when the controller raises the RUN line (EC9 RUN). This results in the assertion of RG3 WRT COM and SN1 WRITE COM EN which clock sets SN0 HEADER ENABLE flip-flop to enter the header search flow.

3.8.2 Pre-Header Field and Header Field

The header search flow begins at the setting of SN0 HEADER ENABLE flip-flop and ends at the setting of SS0 HEADER FOUND flip-flop which indicates a successful header verification. Detail descriptions are given in Paragraph 3.7 and drawings RP04-0-9, and 19.

3.8.3 Header Gap

A header gap of zeros follows the header verification before the sync byte and data field are written. The byte counter continues counting from the header field to byte 11. By then, all read control logic and header handling logic are reset to produce the following:

1. The SN0 WRITE SECTOR flip-flop is set by clearing the SN0 HEADER ENABLE flip-flop. From this point on, all write control logic begins to function.

2. As the SN0 HEADER ENABLE flip-flop is reset, it triggers a one-shot to assert SN0 GT LD SYNC CLK. This signal forces the assertion of EC0 BUS SYNC CLK which (on receipt of the write clock) loads the first data word from the controller into the buffer register.

3. The byte counter is cleared and then renews its count to byte 9. At this point, the write logic is initiated to write the sync byte and data field.

3.8.4 Data Field Sync Byte and Data Field

From the time SN0 WRITE SYNC is asserted at byte 9, all control functions are identical to those described in Paragraphs 3.6.5.1 and 3.6.6.

In short, SN0 SYNC CLK TIME FF is set to enable the ring counter and the sync clock generation. SN7 DATA ENVELOPE is raised. After a total transfer of 256 words from the controller, the sync clocks are terminated. After the complete data block is recorded onto disk 10, ECC field follows.

3.8.5 ECC Field

Here again, control timing is identical to that described in Paragraph 3.6.7. The SN7 ECC ENVELOPE flip-flop is set to allow the two ECC words to be recorded.

3.8.6 Data Gap

The termination of the sector transfer (or command) is identical to that outlined in Paragraph 3.6.8 with one exception: if the transfer is to continue, SN5 COM CONT is asserted to set the SN0 HEADER ENABLE flip-flop. The write operation is repeated beginning with the header search process.

3.9 READ DATA COMMAND/READ HEADER AND DATA COMMAND FLOW DIAGRAM DISCUSSION (drawing number RP04-0-10, 18 and Figure 3-6)

These two commands resemble each other functionally to the extent that they both transfer data off the disk and over to the controller. Their major differences, on the other hand, are:

1. Header information is transferred to the controller during the read header and data command. During read data command the header is verified internally within the DCL.

2. Header errors are flagged, but transfer continues during a read header and data command. During read data command, header errors abort the command. (See Error Handling subsection.)

Both commands are initiated when the proper command codes (accompanied by the GO bit) are loaded into the control register. These codes and the related control signals they assert are:

1. Read data (61_8) asserts RG3 READ COM.

2. Read header and data (63_8) assert RG3 RD HD & DAT COM.

Both signals set the SN1 HEADER ENABLE flip-flop to initiate the header search process. When this process concludes, SS0 HEADER FOUND asserts to indicate a successful header verification.

NOTE

When the read header and data command is being executed, the sector search process produces four EC0 BUS SYNC clocks to the controller; that is, one for each header word transferred.

When byte 15 in the header gap is counted, SN1 SYNC STROBE is asserted. The DCL is now set up to detect the sync byte from the sync byte decoder. In the interim, SN1 READ ENABLE enables serial shifting of data from the disk into the shift register. When the logic recognizes the sync byte, the signal SN7 SYNC CLR is asserted.

SN7 SYNC CLR resets the byte counter to initiate a byte count of the data field. It also enables the ring (word in) counter to count serial data bits and assert EC5 WORD IN after a complete word has been shifted into the shift register. Each time a word is shifted in, a sync clock is developed for the controller. During the data field a total of 256 sync clocks are generated.

SN7 SYNC CLR also asserts SN7 DATA ENVELOPE to allow the ECC logic to accept the data field. The data envelope signal remains asserted throughout the entire data block transfer; SN8 EOB BYTE negates it, and asserts SN7 ECC ENVELOPE. Under the ECC envelope the two ECC words are read off the disk to complete the ECC check. Four bytes later SN8 END ECC BYTE negates the ECC envelope.

If the ECC check of the 256 word data field is good, SN5 EBL is asserted by SN8 EOB W BYTE. If the ECC check shows that a data error exists, EC3 DCK asserts to indicate a data check error and the error correction process can be entered if the software so desires.

If no data check error is present, SN5 EBL asserts to signal the end of a sector transfer. Then EC9 RUN is sampled to determine if the transfer is to continue. If the RUN line remains asserted, SN5 COM CONT sets off the header search subroutine again. If EC9 RUN is not asserted, signal SN5 RESET GO resets the GO FF and terminates the command.

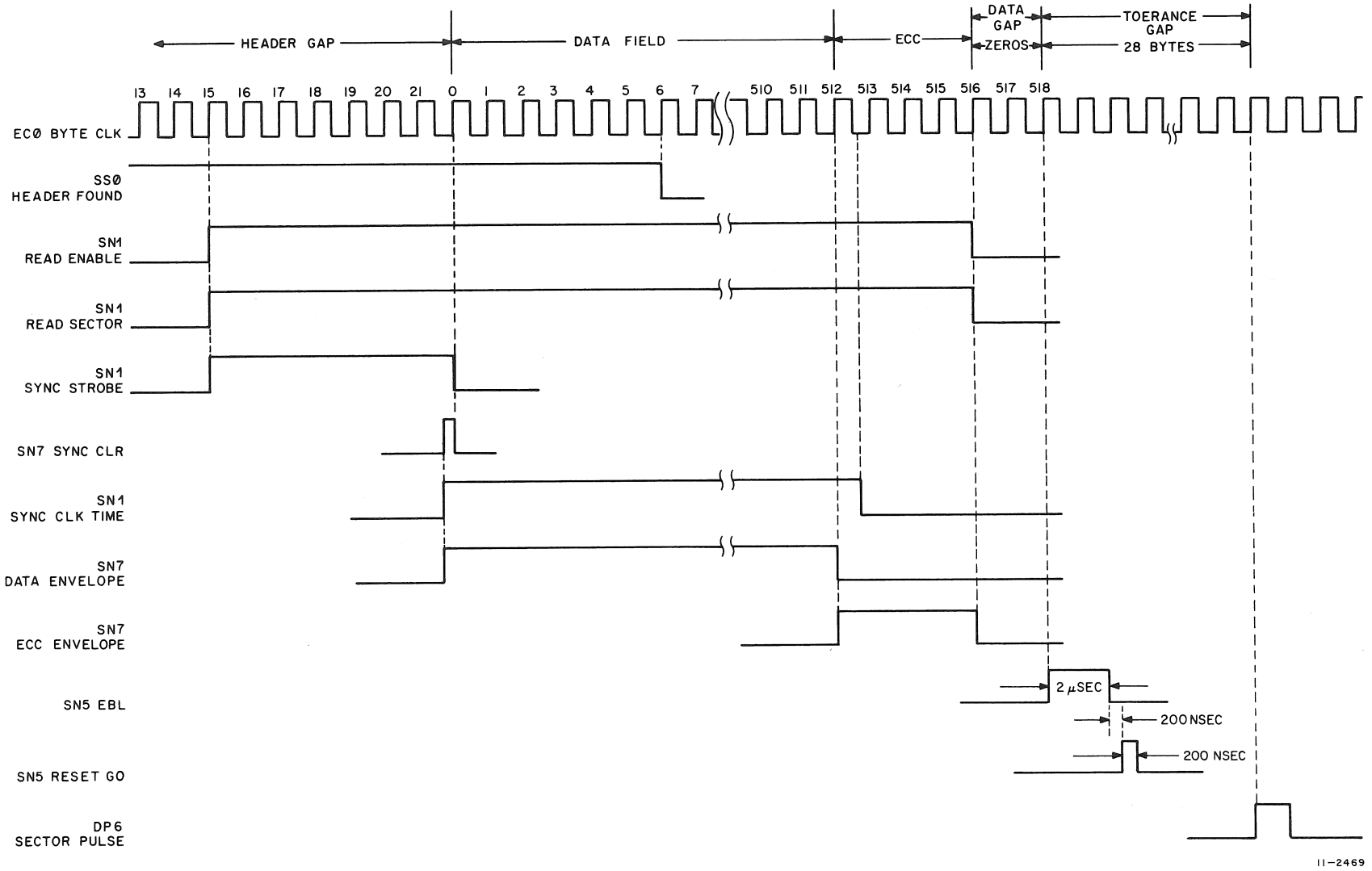


Figure 3-6 Data Field Timing – Read Data and Read Header and Data

3.10 HOUSEKEEPING COMMANDS

3.10.1 No Operation (No-Op) (drawing number RP04-0-21)

The no-op command does nothing within the DCL. When the GO FF is set, the RG3 NO OP command is decoded from the data in the control register. When RG3 NO OP asserts, the GO FF is reset to terminate the command sequence.

3.10.2 Read In (drawing number RP04-0-20)

The read in command sets the VV (volume valid) bit, clears the desired sector/track address register, clears the desired cylinder address register, and clears the FMT, HCI, and ECI bits in the offset register. When the ST0 GO FF is set, the RG4 READ IN command is decoded from the data in the control register. The command performs these functions and also resets the ST0 GO FF to terminate the command sequence.

3.10.3 Pack Acknowledge (drawing number RP04-0-20)

The only function of the pack acknowledge command is to set the VV (volume valid) bit. When the ST0 GO FF is set, the RG4 PCK ACK is decoded from the data in the control register. It asserts RG4 READ ACK RESET which sets the VV bit and terminates the command by resetting the ST0 GO FF.

3.10.4 NG Drive Clear (drawing number RP04-0-21)

The NG drive clear command clears the two ECC registers and asserts the master reset pulse. The master reset pulse (RG4 MAS RES) does the following:

1. Clears all three error registers.
2. Clears the ATA and COMP ERR bits in the status register.
3. Clears the diagnostic mode bit in the maintainability register.

When the ST0 GO FF is set, the RG4 NG DRV CLR COM is decoded from the data in the control register. When the command is asserted, the ECC register is reset and RG4 MAS RES asserts to perform the functions previously listed. The master reset pulse asserts RG0 CLEAR GO which resets the ST0 GO FF to terminate the command sequence.

3.11 BYTE COUNTER OPERATION (drawing number RP04-0-22)

The purpose of the byte counter is to count the bytes within each sector and provide outputs at specific byte counts. The outputs are used to time fields/gaps that make up each sector. The byte counter clock is derived from the shift clock. The source of the shift clock is determined by the mode of operation and the command being executed.

3.11.1 Shift Clock Select

EC0 SHFT CLK is the bit clock used to clock the data word register, the ring (word in) counter, the CRC circuit, the ECC circuit and the sync clock/byte clock generator. The clock is selected from one of three sources: the diagnostic clock, the read strobe from the Drive unit, or the phase locked oscillator (PLO) from the Drive unit. If, in the diagnostic mode, the diagnostic clock is used, then read strobe and the PLO are inhibited. If a read operation is in process, SN1 READ ENABLE selects the read strobe for the shift clock and inhibits the PLO. If a write operation is in process, the PLO is used as the shift clock. The PLO frequency is cut in half by the three level synchronization and frequency divider network (12.9 MHz to 6.45 MHz). The 6.45 MHz clock also serves as the WRITE DATA STROBE used by the Drive unit to clock data into the Drive during a write operation.

3.11.2 Byte Count Development

EC0 SHFT CLK clocks the byte clock generator. The generator is an end-around counter connected to recycle every eight counts. Outputs from the generator are shown in drawing number RP04-0-23.

The byte counter is a synchronous binary counter clocked by EC0 BYTE CLK. The outputs of the counter are decoded to generate SN8 BYTE 30, SN8 BYTE 39, SN8 BYTE 511/575, and other counts. SN8 BYTE 0 through SN8 BYTE 15 are generated separately in the byte count shift register. A second, high order-shift register (when enabled by SN8 BYTE 511/575) produces the EOB, END ECC, and EOB W bytes. The two shift registers are clocked by EC0 BYTE CLK in synchronism with byte counter.

The byte counter is reset several times during a sector and these times vary according to the command being executed. The counter is reset by SN6 BYTE CNT CLR and by SN0 BYTE CNT SYNC CLR.

SN6 COUNT EN enables the byte counter if one of the synchronous data commands or a sector command is in progress, provided an implied or a mid-transfer seek is not being performed.

The counter is also enabled by SS0 TRACK LD EN which asserts when the desired sector/track address register is loaded. After the counter reaches byte 30, SS0 TRACK LD EN is negated and the counter must be enabled by the proper command.

3.12 ERROR HANDLING AND ECC HANDLING

3.12.1 Error Handling (drawing number RP04-0-34)

The error handling flow diagram illustrates how the errors are classified and what action is taken for each class of errors. There are three classes of errors: Class B, Exception, and Composite. Class B errors (RG0 CLASS B ERR) include most of the errors in error register 01 and any error in error registers 02 or 03. Errors in error registers 02 and 03 are caused within the Drive unit.

The following is a summary of the effects of the three error classes.

A Composite Error:

1. Asserts ATTENTION except during a command sequence.
2. Inhibits setting of GO FF.
3. Negates RG3 GT STO GO.
4. Inhibits the setting of RG3 ATA MAS RES by RG3 CONT REG WRT.
5. Sets error bit (14) in the status register.

An Exception Error will:

1. Do everything a Composite error does.
2. Assert EXCEPTION to the MASSBUS.

A Class B Error will:

1. Do everything an Exception error does.
2. Abort any synchronous data transfer by asserting SN5 CLASS B ABORT.

When the controller asserts Exception on the MASSBUS, SN5 EXC is asserted and immediately aborts the command sequence. The EBL FF is also set terminating the command sequence.

3.12.2 ECC Handling (drawing number RP04-0-35)

The ECC subroutine is entered when an error is detected in a sector data field and error correction inhibit (ECI) is negated. A detected error is indicated by asserting EC3 DCK. (See Read Data and Read Header and Data Flow Drawing, number RP04-0-10.) Drawing number RP04-0-35 shows the flow sequence leading to the assertion or negation of EC3 DCK.

The serial data read from the Drive unit (MA0 RD/WRT DATA) is shifted into the ECC shift register. The register is enabled for the duration of the data envelope and the ECC envelope by EC3 ECC REG FDBKCTRL.

With EC3 ECC CORRECT ENA negated, the ECC register zero detect circuit is examined at the end of the ECC envelope when EC3 DCK SPIKE ELIM asserts. If an EC1 ZERO DETECT exists, EC3 DCK is negated signifying that the sector data field is free of error. If an EC1 ZERO DEFECT is not obtained, EC3 DCK is asserted indicating the presence of an error in the data field. If RG1 EC1 is negated, the error correction process is entered by asserting EC3 ECC CORRECT EN.

EC3 ECC CORRECT EN keeps the ECC shift register enabled and starts the N-Code counter. The error correction code requires that the ECC shift register clocked 38,347 times for the 18-bit mode (38,859 for the 16-bit mode) before the actual data field begins within the register.

When the N-Code counter reaches this value, EC2 N CODE WRD HICNT is asserted and enables the ECC position register which counts bits of the data field.

With EC3 ECC CORRECT ENA asserted, the ECC shift register zero detect circuit looks for an EC1 ZERO DETECT again. If the error is correctable (error bits confined to an 11-bit area), a zero detect is sensed when the first error bit is reached in the ECC shift register. EC3 ECC CORRECT ENA is then negated, stopping both the position register and the pattern register. The position register contains the position of the first error bit in the data field and the pattern register contains the pattern of the next 11 bits.

If the error is noncorrectable (error bits separated by more than 11 bits), no zero detect is obtained as the ECC shift register reaches the end of the data field. The end of the data field is indicated by a count of 42,987 from the N-Code counter. In this case, EC2 ECH is asserted indicating a noncorrectable error. The exit from the subroutine occurs by asserting EC3 ECC READY.

CHAPTER 4
REPLACEMENT PROCEDURES

4.1 GENERAL

The only special replacement procedures required for the Device Control Logic involves the DP hex printed circuit board. When replacing this board, care must be taken to ensure that the dual-in-line rocker switches are set for the same device address as that of the removed DP board. No other special replacement procedures are necessary.

CHAPTER 5
MAINTENANCE

5.1 GENERAL

Preventive and corrective maintenance procedures for the DCL are carried out by using diagnostic programs. Individual diagnostic tests, the circuits they exercise, and related test objectives are described fully in the following instruction manuals: For PDP-11 system diagnostics, refer to the *RJP04 Moving Head Disk Subsystem Maintenance Manual.* For DECsystem-10 diagnostics, refer to *RH10 Controller Maintenance Manual* (EK-RH10-MM-002).

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTION

A.1 INTRODUCTION

This appendix contains descriptions of some of the integrated circuits used in the RH11. Where applicable, logic diagrams, schematics, and pin connection diagrams are shown.

A.2 3341 64-WORD X 4-BIT SERIAL MEMORY (SILO)

The 3341 Silo Memory operates in a first in/first out mode (FIFO). The output rate is independent of the input rate and asynchronous or synchronous operation can be achieved.

The four data inputs (D0 through D3) are transferred to the first memory location if both the Input Ready (IR) and Shift In (SI) signals are asserted high (see Silo Memory Block Diagram). After 250 ns to allow the data to stabilize, IR goes low. However, data remains in the first memory location until both IR and SI are brought low. At this point, the data propagates to the next memory location, if the location is empty. When the data is transferred, IR goes high, indicating that the device is ready to accept new data. If the memory is full, the IR signal remains unasserted (low).

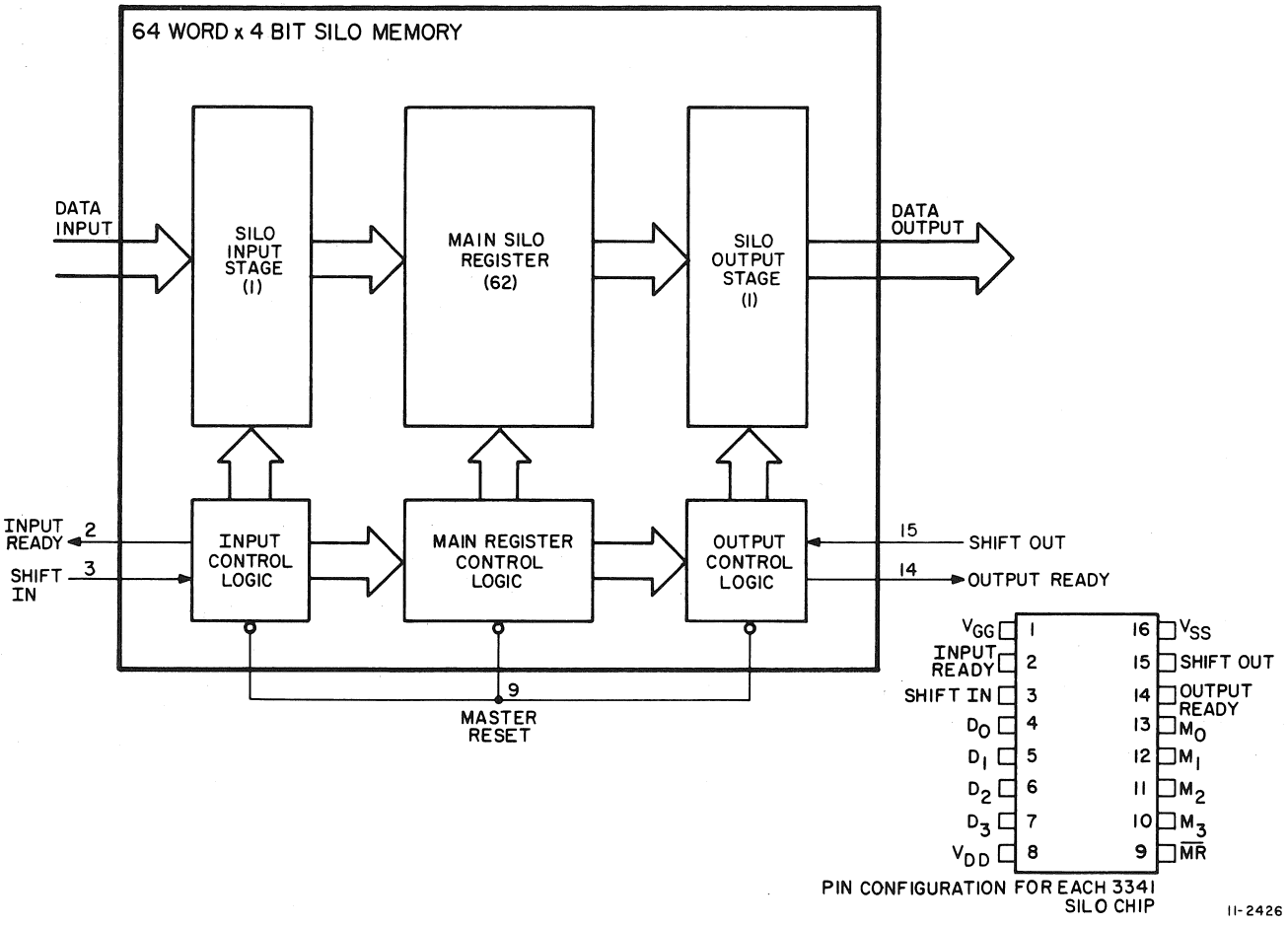
When data enters the second cell, the transfer of any data word from a full cell to the next empty cell is automatic and is activated by an on-chip control. Consequently, data stacks up at the output to the memory while empty locations "bubble" to the input of the memory. The throughput time from input to output of the Silo is from 0 to 32 μs (16 μs typical).

When data has transferred to the last cell in the Silo, OUTPUT READY (OR) is asserted high, indicating that valid data is present at the output pins (M0 through M3 on each chip). Data is not shifted out of the Silo, however, until the OUTPUT READY and SHIFT OUT signals to the Silo are both asserted high. When the data is shifted out, OUTPUT READY goes low. The output data is maintained until both OUTPUT READY and SHIFT OUT go low. At this point, the contents of the previous memory cell (if it is full) are transferred to the output cell, causing OUTPUT READY to be asserted high again. When the Silo memory is emptied, OUTPUT READY stays low.

Table A-1 lists the minimum, typical, and maximum times for the above mentioned signals at 0° C and at 70° C.

Table A-1
Control Signal Timing Specifications

Signal	0°			70°		
	MIN	TYP	MAX	MIN	TYP	MAX
Input Ready High Time	90	300	–	155	300	450
Input Ready Low Time	138	400	–	–	400	520
Data Input Stabilizing Time	–	250	–	–	250	400
Data Output Stabilizing Time	–	250	–	–	250	400
Output Ready High Time	90	250	–	155	250	350
Output Ready Low Time	170	450	–	–	450	650


64 WORD x 4 BIT SILO MEMORY
DATA INPUT
SILO INPUT STAGE (1)
MAIN SILO REGISTER (62)
SILO OUTPUT STAGE (1)
DATA OUTPUT
INPUT READY 2
SHIFT IN 3
INPUT CONTROL LOGIC
MAIN REGISTER CONTROL LOGIC
OUTPUT CONTROL LOGIC
15 SHIFT OUT
14 OUTPUT READY
9 MASTER RESET
VGG 1
INPUT READY 2
SHIFT IN 3
D0 4
D1 5
D2 6
D3 7
VDD 8
16 VSS
15 SHIFT OUT
14 OUTPUT READY
13 M0
12 M1
11 M2
10 M3
9 MR
PIN CONFIGURATION FOR EACH 3341 SILO CHIP
11-2426

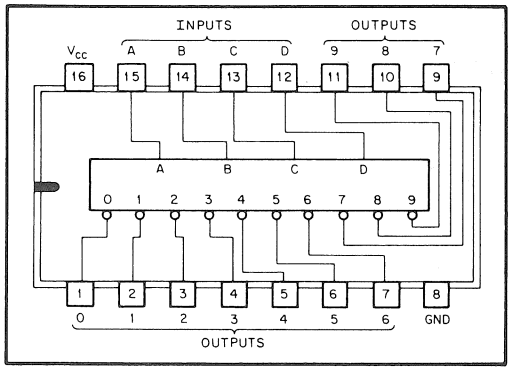
A.3 7442 4-LINE-TO-10-LINE DECODERS (1-of-10)

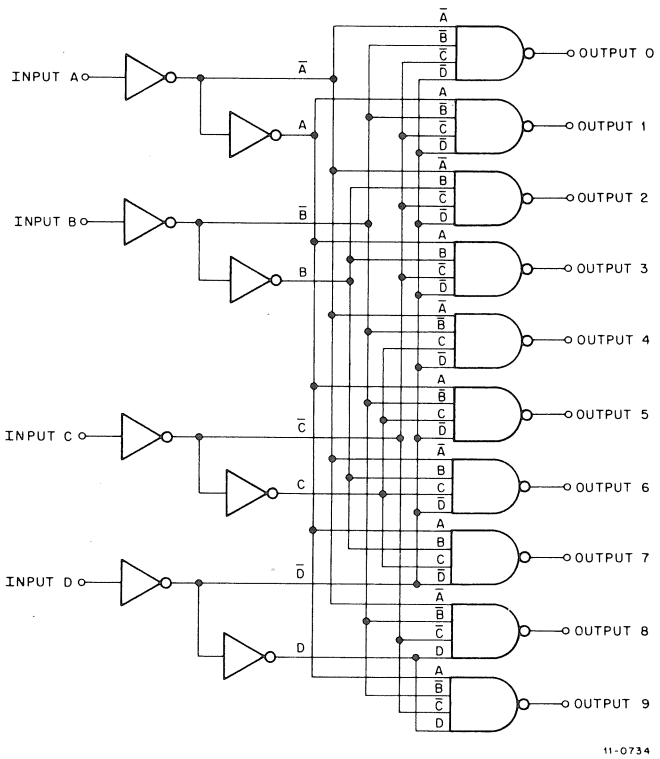
These monolithic decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The 7442 BCD-to-decimal decoder features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs that are compatible for use with other TTL and DTL circuits.

TRUTH TABLES

BCD Input				Decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1





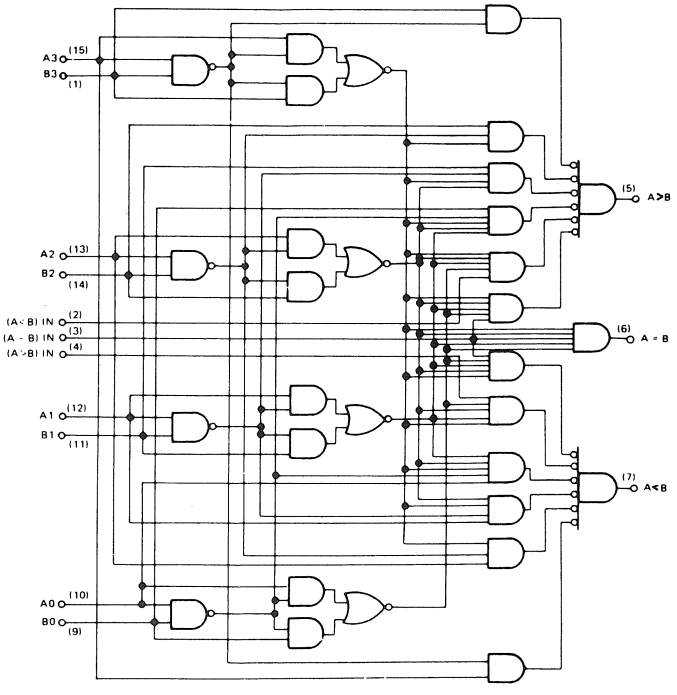
A.4 7485 4-BIT MAGNITUDE COMPARATORS

The 7485 performs magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

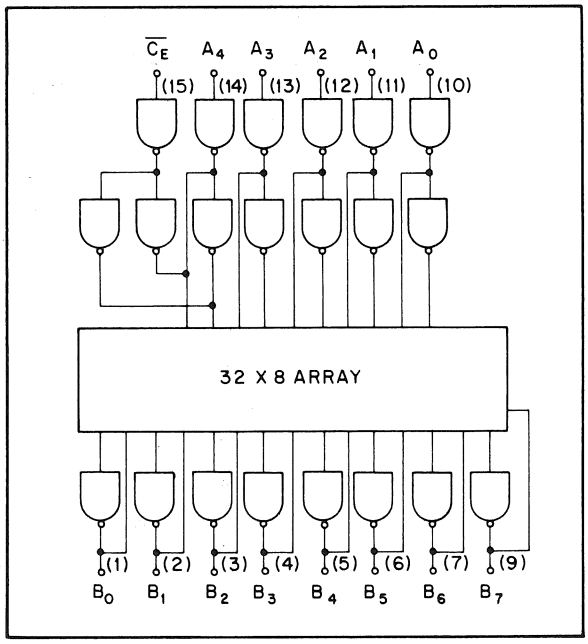
NOTE: H = high level, L = low level, X = irrelevant



Pin (16) = V_{CC}, Pin (8) = GND

A.5 8223 256-BIT BIPOLAR FIELD-PROGRAMMABLE ROM (32 X 8 PROM)

The 8223 is a TTL 256-bit read only memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

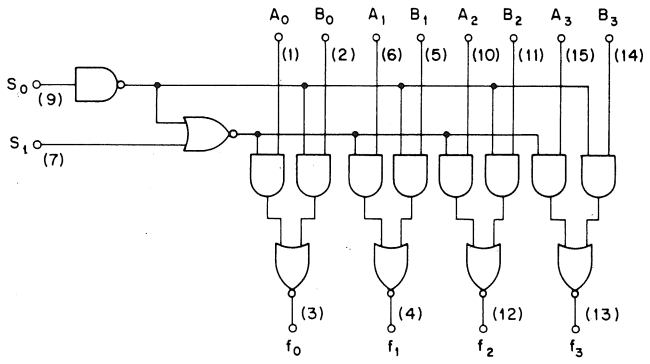


V_{CC} = (16)
GND=(8)
( ) = DENOTES PIN NUMBERS

11-2382

A.6 8234 2-INPUT 4-BIT DIGITAL MULTIPLEXER

This device is a 2-input, 4-bit digital multiplexer designed for general purpose, data selection applications. The 8234 features inverting data paths. The 8234 design has open-collector outputs which permit direct wiring to other open-collector outputs (collector logic).



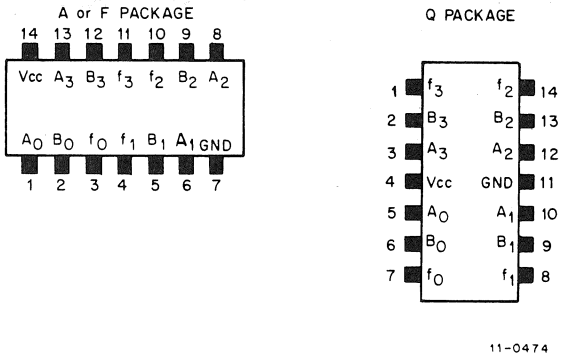
S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

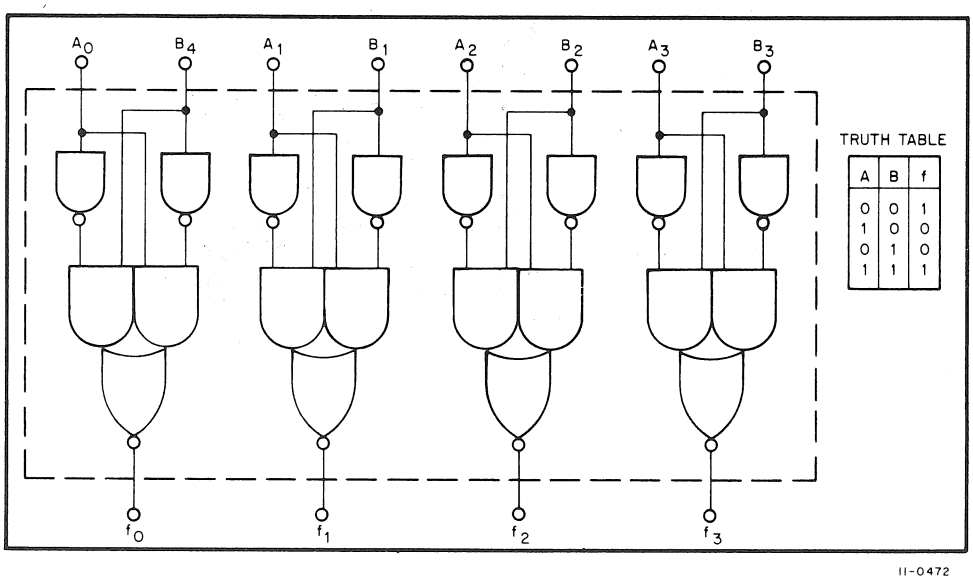
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

11-2383

A.7 8242 EXCLUSIVE-NOR 4-BIT DIGITAL COMPARATOR

The 8242 digital comparator circuit consists of four independent Exclusive-NOR gates with each gate structure having an open-collector output to permit multiple bit comparisons. A 4-bit comparator network is formed by connecting the independent outputs; such a network is easily expanded by cascading the outputs.



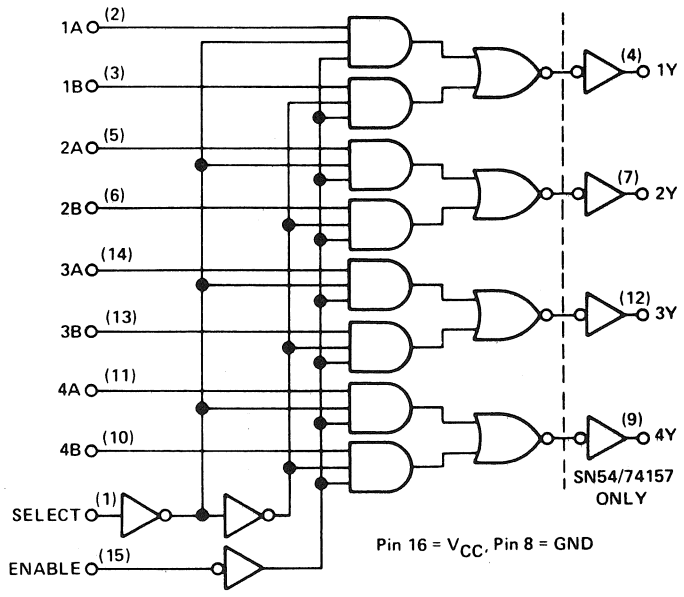


A.8 74157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER

The 74157 quadruple 2-line to 1-line multiplexer features buffered inputs and outputs. All outputs are low when disabled (enable high). The truth table and logic diagram are shown below.

INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	SN54/74157, SN54S/74S157	SN54S/74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H = high level, L = low level, X = irrelevant



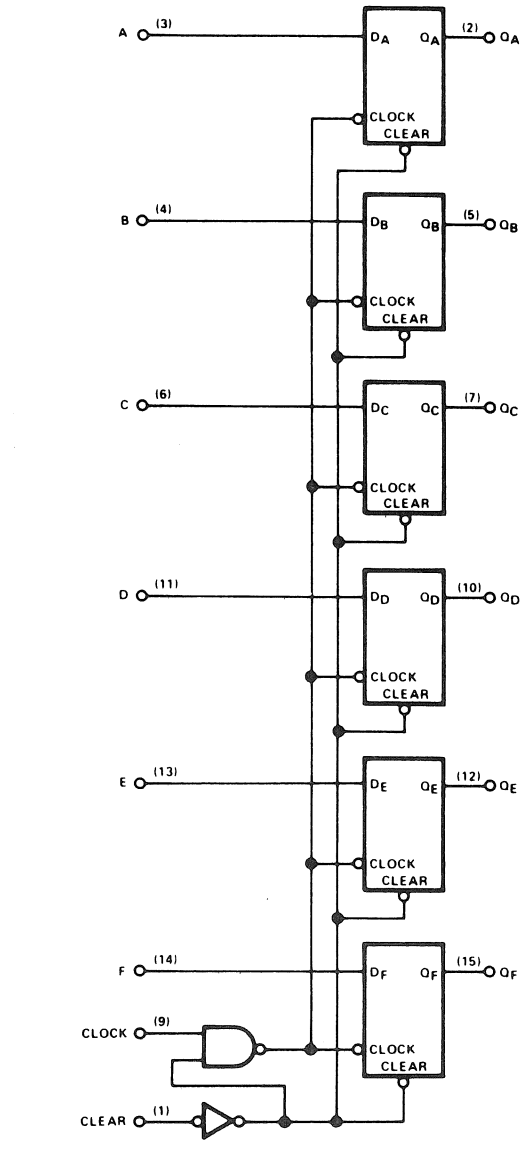
Pin (16) = V_{CC}, Pin (8) = GND

A.9 74174 HEX D-TYPE FLIP-FLOPS

The 74174 contains six flip-flops with single outputs. The flip-flops contain direct clear inputs and buffered clock inputs.

INPUT t_n	OUTPUTS t_n+1	
D	Q	$\overline{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

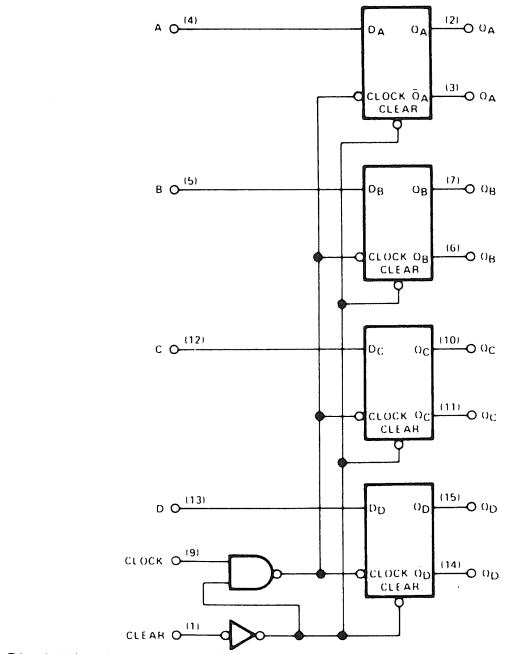
A.10 74175 QUAD D-TYPE FLIP-FLOPS

The 74175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct clear and buffered clock inputs.

INPUT t_n	OUTPUTS t_n+1	
D	Q	$\bar{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.

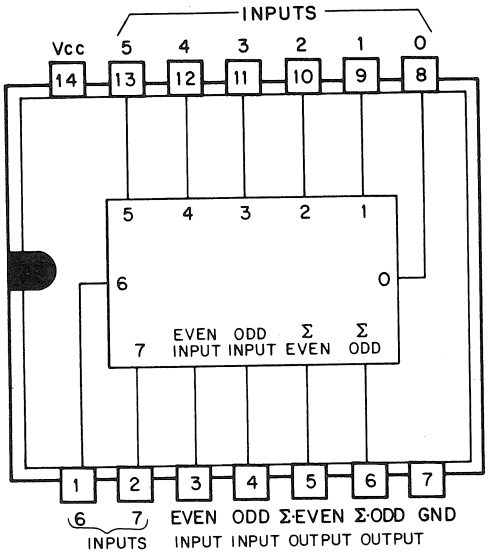
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

A.11 74180 PARITY CONTROL GENERATOR/ CHECKER

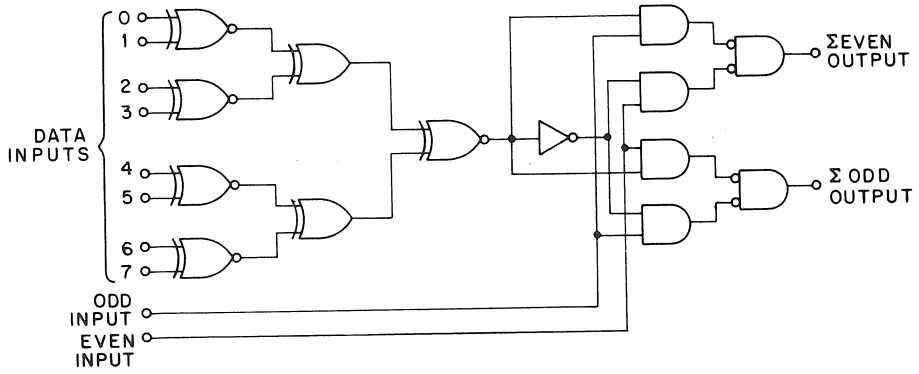
The 74180 is an 8-bit parity generator/checker featuring odd and even outputs and control inputs to provide odd or even parity operation. Word length is expandable by cascading. The truth table, pin connection diagram, and functional block diagram are shown below.



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= IRRELEVANT



11-2384

A.12 74193 4-BIT BINARY COUNTER

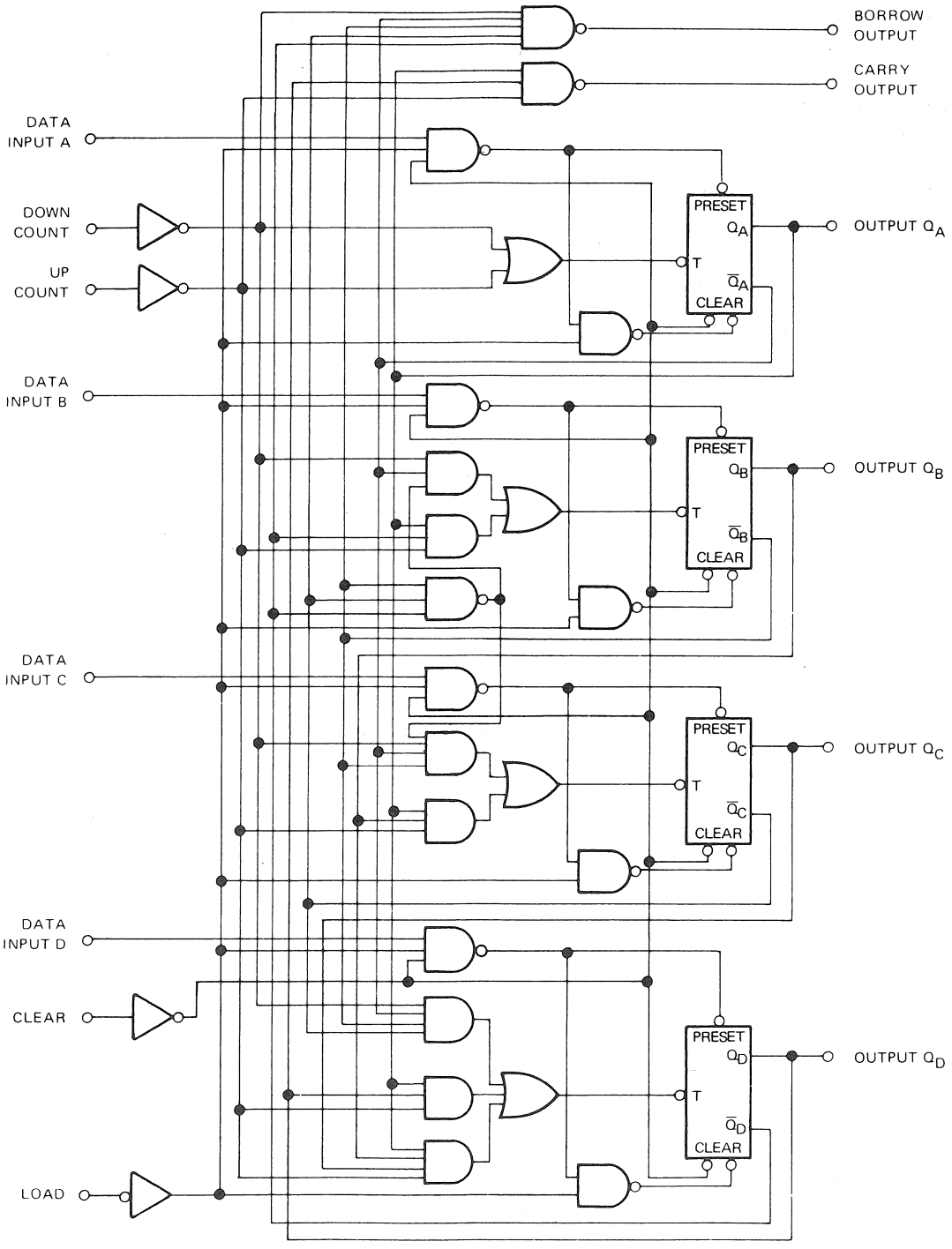
The 74193 binary counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.

COUNT UP	COUNT DOWN	LOAD	MODE
X	X	L	Parallel Load
CLOCK	H	H	Count Up
H	CLOCK	H	Count Down

H = high level, L = low level, X = irrelevant

Signal/Pin Designation

Signal Name	Pin Designation
DATA INPUT A	15
DATA INPUT B	1
DATA INPUT C	10
DATA INPUT D	9
CLEAR	14
LOAD	11
DOWN COUNT	4
BORROW OUTPUT	13
CARRY OUTPUT	12
UP COUNT	5
OUTPUT Q_A	3
OUTPUT Q_B	2
OUTPUT Q_C	6
OUTPUT Q_D	7


BORROW OUTPUT
CARRY OUTPUT
DATA INPUT A
DOWN COUNT
UP COUNT
DATA INPUT B
DATA INPUT C
DATA INPUT D
CLEAR
LOAD
PRESET
Q_A
T
$\overline{Q}_A$
CLEAR
OUTPUT Q_A
PRESET
Q_B
T
$\overline{Q}_B$
CLEAR
OUTPUT Q_B
PRESET
Q_C
T
$\overline{Q}_C$
CLEAR
OUTPUT Q_C
PRESET
Q_D
T
$\overline{Q}_D$
CLEAR
OUTPUT Q_D

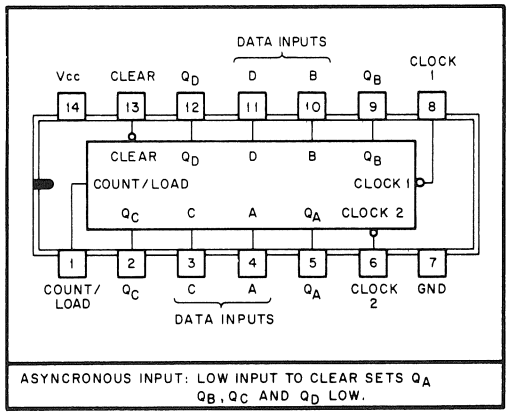
A.13 74197 50 MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

This high-speed monolithic counter consists of four dc coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter. The counter is fully programmable; i.e., the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. It features a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



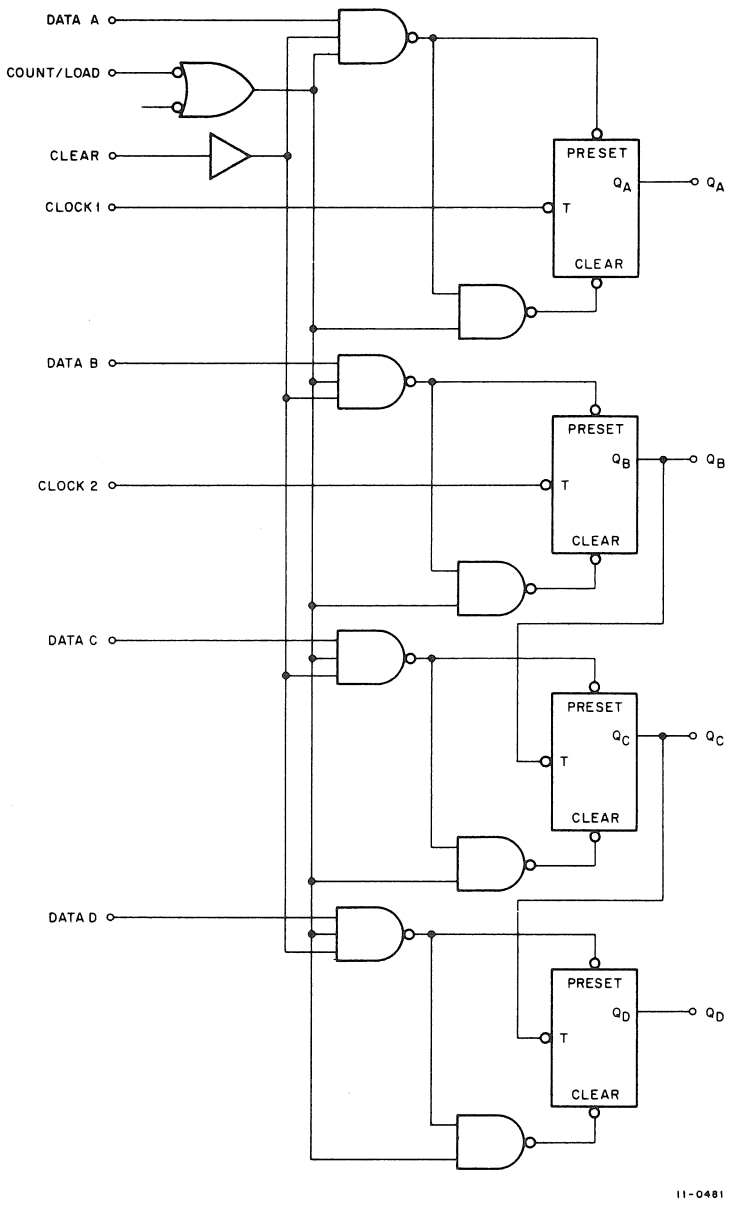
*Pin assignments for these circuits are the same for all packages.

11-0482

SN74197 TRUTH TABLE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.


DATA A
COUNT/LOAD
CLEAR
CLOCK 1
PRESET
Q_A
T
CLEAR
Q_A
DATA B
CLOCK 2
PRESET
Q_B
T
CLEAR
Q_B
DATA C
PRESET
Q_C
T
CLEAR
Q_C
DATA D
PRESET
Q_D
T
CLEAR
Q_D
11-0481

RP04 Device Control Logic
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printed in U.S.A.