EK-MSV1Q-UG-002

MSV11-Q

MOS Memory

User's Guide

digital™

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CHARACTERISTICS AND SPECIFICATIONS 1

1.1 INTRODUCTION

This manual describes the MSV11-Q memory module. The module contains metal oxide semiconducters (MOS) random access memory (RAM). It is used with the LSI-11 bus and provides 1024K byte to 4096K byte storage for 18-bit words (16 data bits and 2 parity bits). It also contains parity control circuitry and a control and status register (CSR).

There are four variations of the MSV11-Q module.

- MSV11-QA (etch revision A) – 64K RAMs fully populated; cannot be configured for battery backup
- MSV11-QA (etch revision C or later) – 64K RAMs fully populated; can be configured for battery backup
- MSV11-QB – 256K RAMs half populated; can be configured for battery backup
- MSV11-QC – 256K RAMs fully populated; can be configured for battery backup

The MSV11-QA (etch revision A) is indicated as shown in Figure 1-1A. Differences between the MSV11-QA, etch revision A, and the other variations will be pointed out as they occur.

The MSV11-QA (etch revision C), MSV11-QB, and MSV11-QC all use the same etch (refer to Figure 1-1B).

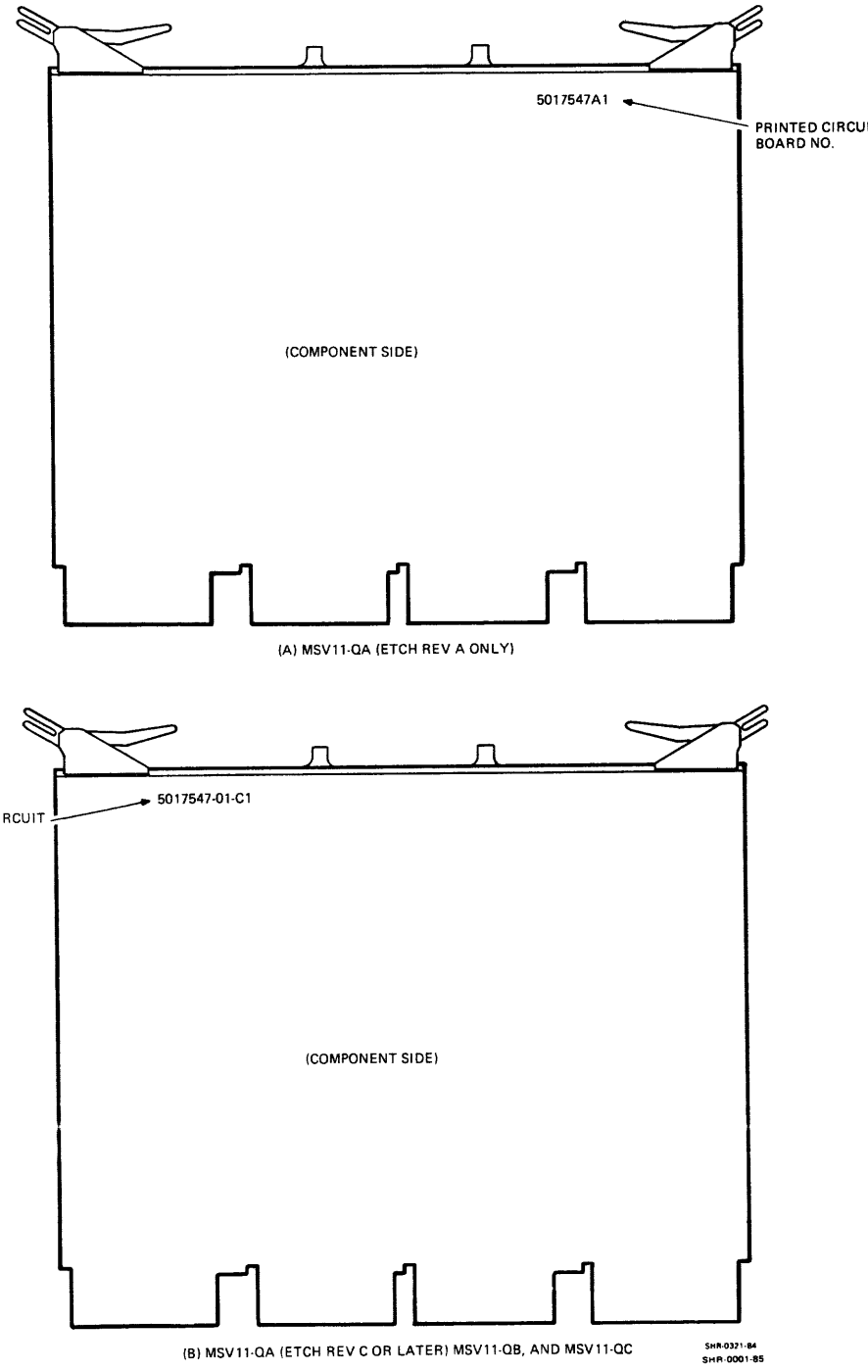

Figure 1-1 Module Identification

The major features of the MSV11-Q are:

- 1 megabyte of MOS memory on a single quad module (MSV11-QA).
  2 megabyte of MOS memory on a single quad module (MSV11-QB).
  4 megabyte of MOS memory on a single quad module (MSV11-QC).
- 22-bit addressing standard.
- Parity is generated and checked for each byte for data integrity.
- Self-contained Control and Status Register (CSR) for full parity implementation.
- Full parity control enables the CPU to trap on a parity error with LED display for parity status.
- Completely LSI hardware and software compatible.
- Switch selectable starting address in 128K byte increments.
- 16 jumper selectable CSR addresses (17772100 through 17772136).
- Single +5 V power. MSV11-QA (etch revision A) does not support battery backup.
- Supports Block-Mode for efficient multiple DMA transfer.

1.2 GENERAL DESCRIPTION

The MSV11-Q memory module consists of a single, quad-height module (M7551) that contains the LSI-11 bus interface, timing and control logic, refresh circuitry, and a MOS storage array. The module also contains circuitry to generate and check parity, and a control and status register. The MSV11-Q memory uses +5 V from the backplane.

The memory module's starting address can be set on any 128 KB boundary within the 4096 KB LSI-11 address space or 256 KB LSI-11 address space. The MSV11-Q allows the top 4K of the LSI-11 address space to be reserved for the I/O peripheral page. There is no address interleaving with the MSV11-Q.

The memory storage elements for the MSV11-QA are 65,536 by 1 bit MOS dynamic RAM devices. The storage elements for the MSV11-QB and MSV11-QC are 262,144 by 1 bit MOS dynamic RAM devices. The MOS storage array for the MSV11-QA and MSV11-QC has 8 rows with each row containing 18 devices for a total of 1024K bytes on the MSV11-QA and 4 megabytes on the MSV11-QC. The MSV11-QB is half populated and therefore contains 4 rows for a total of 2 megabytes of memory. The read operation for MOS storage devices is non-destructive. The MOS storage devices must be refreshed every 12.0 μs so that the data remains valid.

The control and status register in the MSV11-Q contains bits used to store the parity error address bits. You can force wrong parity by setting a bit in the CSR. This is a useful diagnostic tool for checking out the parity logic. The CSR has its own address in the top 4K of memory. Bus masters can read or write to the CSR.

The parity control circuitry in the MSV11-Q generates parity bits based on data being written into memory during a DATO or DATOB bus cycle. One parity bit is assigned to each data byte and is stored with the data in the MOS storage array. When data is retrieved from memory during DATI or DATIO bus cycles, the parity of the data is determined. If parity is good, the data is assumed correct. If the parity bits do not correspond, the data is assumed unreliable and memory initiates the following action.

1. If a parity error occurs, CSR bit 15 is set and a red LED on the module lights.

   In the case of MSV11-QA (etch revision C or later), MSV11-QB and MSV11-QC, the memory asserts BDAL 16 and 17 if bit 0 in the CSR is set. This warns the processor that a parity error has occurred. For this to occur in the MSV11-QA (etch revision A), jumper H must be connected (refer to Paragraph 2.2.7).

2. Part of the address of the faulty data is recorded in the CSR.

1.3 SPECIFICATIONS

This section gives functional, electrical, and environmental specifications and backplane pin utilization information. The specifications in this section are applicable to all variations of the MSV11-Q memory except where differences are noted.

1.3.1 Functional Specifications

Table 1-1 provides access and cycle time specifications for the MSV11-QA (etch revision A) memory. Table 1-2 provides access and cycle times for the other MSV11-Q variations.

Table 1-1 MSV11-QA (etch revision A) Access and Cycle Times

	T_{acc}(ns)			T_{cyc}(ns)		
	Meas Typ	Max	Notes	Meas Typ	Max	Notes
Parity-CSR Configurations (Notes 1,8,9)						
DATI	320	358	2	520	578	4
DATO(B)	350	376	2	550	597	5
DATIO(B)	1000	1045	3	1220	1255	6
DATBI	320	358	2	–	–	N/A
	20	31	10	–	–	N/A
	320	376	11,12	–	–	N/A
	–	–	N/A	520	569	15
DATBO	350	387	2	–	–	N/A
	20	31	10	–	–	N/A
	280	668	13,14	–	–	N/A
	–	–	N/A	500	547	16

Table 1-2 MSV11-QA (Etch Revision C or Later), MSV11-QB, and MSV11-QC Access and Cycle Times

	T_{acc}(ns)			T_{cyc}(ns)		
	Meas Typ	Max	Notes	Typ	Max	Meas Notes
Parity-CSR Configurations (Notes 1,8,9)						
DATI	320	358	2	510	563	4
DATO(B)	160	189	2	550	592	5
DATIO(B)	780	847	3	1220	1250	6
DATBI	320	358	2	–	–	N/A
	20	31	10	–	–	N/A
	340	363	11,12	–	–	N/A
	–	–	N/A	518	569	15
DATBO	160	189	2	–	–	N/A
	20	31	10	–	–	N/A
	250	292	13,14	–	–	N/A
	–	–	N/A	655	695	16

The following notes (1 through 16) refer to Tables 1-1 and 1-2.

Notes for DATI, DATO(B), DATIO(B) Cycles:

1. *Assuming memory not busy and no arbitration.*

2. *SYNCH to RPLYH with minimum times (25/50 ns) from SYNCH to (DINH/DOUTH). The DATO(B) access and cycle times assume a minimum of 50 ns from SYNCH to DOUTH inside memory receivers. For actual LSI-11 bus measurements, a constant (K-50 ns) where K = 200 ns should be added to DATI(B) times, i.e. acc (Typ) = 100 + (200 - 50) = 250 ns.*

3. *SYNCH to RPLYH DATIO(B), with minimum time (25 ns) from SYNCH to DINH and minimum 350 ns from RPLYH (DATI) asserted to DOUT asserted.*

4. *SYNCH to MBSY L negated.*

5. *SYNCH to MBSY L negated with minimum time (50 ns) from SYNCH to DOUTH.*

6. *SYNCH to MBSY L (DATIO(B)) with minimum times (25 ns) from SYNCH to DINH and minimum 350 ns from RPLYH (DATI) asserted to DOUT asserted.*

7. *REF REQ L to MBSY L negated.*

8. *The MSV11-Q Module does not lose any time due to refresh arbitration.*

9. *REFRESH conflict adds 250 ns Typical and 542 ns maximum to access and cycle time.*

Notes for DATBI AND DATBO Cycles:

10. *DIN/DOUT negation to MRPLY negation*

11. *DIN negation to TRPLY assertion*

12. *DIN remains asserted for 200 ns minimum after TRPLY with 150 ns minimum from TRPLY negation to assertion of next DIN.*

13. *DOUT remains asserted for 150 ns minimum after TRPLY with 150 ns minimum from TRPLY negation to assertion of next DOUT.*

14. *DOUT assertion to TRPLY assertion.*

15. *DIN negation to MBSY L negation after first DIN cycle. Use DATI cycle time for first DIN/TRPLY cycle in block mode ready cycle.*

16. *DOUT assertion to MBSY L negation after first DOUT cycle. Use DATO(B) cycle time for first DOUT/TRPLY cycle in block mode write cycle.*

1.3.2 Electrical Specifications

The electrical specifications state the voltage and power requirements for the MSV11-Q.

1.3.2.1 Voltages – Single voltage MOS RAMs require only +5 V. Voltage margins for +5 V are ±5 percent (Tables 1-3 and 1-4).

1.3.2.2 Power Requirements – Power requirements are provided in Tables 1-5, 1-6 and 1-7.

Table 1-3 Voltage Pins (MSV11-QA, Etch Revision A)

Voltage	Pins	Service
+5 V	AA2, BA2, BV1, CA2, DA2	Single voltage MOS RAMs*

Table 1-4 Voltage Pins [MSV11-QA (Etch Revision C or Later,) MSV11-QB, and MSV11-QC]

Voltage	Backplane Pins	
+5 V	AA2,BA2,BV1,CA2, and DA2	Single voltage MOS RAMs
+5 V BBU	AV1, and AE1*	

* Check backplane voltages to ensure proper configurations.

Table 1-5 MSV11-QA Power (All Etch Revisions)

MSV11-QA With 64K RAMs Fully Populated

	Current (Amps)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	1.0	1.32	1.0	1.32
+5 V BBU total	1.28	2.33	1.4	2.67
Module total	2.28	3.65	2.4	3.99

	Power (Watts)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	5.0	6.93	5.0	6.93
+5 V BBU total	6.4	12.23	7.0	14.02
Module total	11.4	19.16	12.0	20.95

Table 1-6 MSV11-QB Power

MSV11-QB With 256K RAMs Half Populated

	Current (Amps)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	1.0	1.32	1.00	1.32
+5 V BBU total	1.18	1.66	1.30	2.27
Module total	2.18	2.98	2.30	3.59

	Power (Watts)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	5.0	6.93	5.0	6.93
+5 V BBU total	5.90	8.72	6.50	11.92
Module total	10.90	15.65	11.50	18.85

Table 1-7 MSV11-QC Power

MSV11-QC With 256K RAMs Fully Populated

	Current (Amps)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	1.0	1.32	1.0	1.32
+5 V BBU total	1.34	2.37	1.50	2.98
Module total	2.34	3.69	2.50	4.30

	Power (Watts)			
	Standby		Active	
	Typ Measured	Max	Typ Measured	Max
+5 V total	5.00	6.93	5.00	6.93
+5 V BBU total	6.70	12.44	7.50	15.65
Module total	11.70	19.37	12.50	22.58

1.3.3 Environmental Specifications

Environmental specifications cover storage and operating temperature, relative humidity, altitude, and air flow specifications.

1.3.3.1 Temperature – Temperature is separated into the following two groups.

1. Operating Temperature Range – The operating temperature range is +5°C to +60°C. Lower the maximum operating temperature by 1°C for every 1000 feet of altitude above 8000 feet.

2. Storage Temperature Range – The storage temperature range is –40°C to +66°C. Do not operate a module that has been stored outside the operating temperature range before bringing the module to an environment within the operating range and allowing at least five minutes for the module to stabilize.

1.3.3.2 Relative Humidity – The relative humidity for the MSV11-QA memory modules must be 10% to 90 percent noncondensing for storage or operating conditions.

1.3.3.3 Operating Airflow – Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module to 5°C when the inlet temperature is +60°C. For operation below +55°C, airflow must be provided to limit the inlet to outlet temperature rise across the module to 10°C maximum.

1.3.3.4 Altitude – The module resists mechanical or electrical damage at altitudes up to 50,000 feet (90 MM mercury) under storage or operating conditions.

NOTE: Lower the maximum operating temperature by 1°C for every 1000 feet of altitude above 8000 feet.

1.3.4 Refresh

The MSV11-Q memory module uses a self-contained refresh oscillator, with rate that is typically 535 ns every 12,000 ns. The refresh overhead maximum is 542 ns/12,500 ns or 4.3 percent.

1.3.5 Diagnostics

The diagnostics are CVMSAA for 22-bit systems and EHXMS for MicroVAX.

1.3.6 Backplane Pin Utilization

Backplane pin utilization for the MSV11-QA (etch revision A) is shown in Table 1-8. Backplane pin utilization for the MSV11-QA (etch revision C or later), MSV11-QB and MSV11-QC is shown in Table 1-9. Blank spaces indicate pins not used.

Table 1-8 Backplane Pin Utilization (MSV11-QA, Etch Revision A)

	A Connector		B Connector		C Connector		D Connector	
Pin	**Side 1**	**Side 2**	**Side 1**	**Side 2**	**Side 1**	**Side 2**	**Side 1**	**Side 2**
A	—	+5 V	BDCOK H	+5 V		+5 V		+5 V
B	—	—	—	—		—		—
C	BDAL 16L	GND	BDAL 18L	GND		GND		GND
D	BDAL 17L	—	BDAL 19L	—		—		
*E	+5 V BB	BDOUT L	BDAL 20L	BDAL 02L		—		
F	—	BRPLY L	BDAL 21L	BDAL 03L		—		
H	—	BDIN L	—	BDAL 04L	B	—	B	B
J	GND	BSYNC L	GND	BDAL 05L	L	—	L	L
K	REFKILL	BWTBT L	—	BDAL 06L	A	—	A	A
L	—	—	—	BDAL 07L	N	—	N	N
M	GND	*BIAKIL	GND	BDAL 08L	K	*BIAKIL	K	K
N	—	*BIAKOL	—	BDAL 09L		*BIAKOL		
P	—	BBS7L	—	BDAL 10L		—		
R	BREF L	*BDMGIL	—	BDAL 11L		*BDMGIL		
S	—	*BDMGOL	—	BDAL 12L		*BDMGOL		
T	GND	BINIT L	GND	BDAL 13L	GND	—	GND	
U	—	BDALOO L	—	BDAL 14L	—	—	—	
*V	+5 V BB	BDALO1 L	+5 V	BDAL 15L	—	—	—	

* Hardwired via etch on module. If a system uses the pin for anything but power, user must cut gold finger AE1 on the board.

Table 1-9 Backplane Pin Utilization (MSV11-QA, Etch Revision C or Later, MSV11-QB, MSV11-QC)

	A Connector		B Connector		C Connector		D Connector	
Pin	Side 1	Side 2	Side 1	Side 2	Side 1	Side 2	Side 1	Side 2
A	—	+5 V	BDCOK H	+5 V		+5 V		+5 V
B	—	—	—	—		—		—
C	BDAL 16L	GND	BDAL 18L	GND		GND		GND
D	BDAL 17L	—	BDAL 19L	—		—		
E	+5 V BB	BDOUT L	BDAL 20L	BDAL 02L		—		
F	—	BRPLY L	BDAL 21L	BDAL 03L		—		
H	—	BDIN L	—	BDAL 04L	B	—	B	B
J	GND	BSYNC L	GND	BDAL 05L	L	—	L	L
K	REFKILL	BWTBT L	—	BDAL 06L	A	—	A	A
L	—	—	—	BDAL 07L	N	—	N	N
M	GND	*BIAKIL	GND	BDAL 08L	K	*BIAKIL	K	K
N	—	*BIAKOL	—	BDAL 09L		*BIAKOL		
P	—	BBS7L	—	BDAL 10L		—		
R	BREF L	*BDMGIL	—	BDAL 11L		*BDMGIL		
S	—	*BDMGOL	—	BDAL 12L		*BDMGOL		
T	GND	BINIT L	GND	BDAL 13L	GND	—	GND	
U	—	BDALOO L	—	BDAL 14L	—	—	—	
V	+5 V BB	BDALO1 L	+5 V	BDAL 15L	—	—	—	

* Hardwired via etch on module.

NOTE: If you are using AE1 (sspare 1) for anything other than battery backup voltage (+5 V BB), jumper W1 must not be installed. However, Digital Equipment Corporation recommends backpanel pin <AE1> be used as +5.0 V battery backup power in this application. Refer to Paragraph 3.2.3 for additional information.

1.3.7 Electrical Specifications

1.3.7.1 Power Supply Requirements – The module operates on +5 V only.

1.3.8 Bus Loading

MSV11-QA (etch revision A)

AC load units = 1.9
DC load units = 0.5

MSV11-QA (etch revision C)

AC load units = 2.4
DC load units = 0.5

1.4 RELATED DOCUMENTS

Refer to the following documents for more information.

- MSV11-QA, MSV11-QB, and MSV11-QC (all etch revisions) Field Maintenance Printset (MP01931)
- Microcomputer and Memory Handbook (EB-18451-20)
- Microcomputer Interface Handbook (EB-20175-20)
- LSI-11 System Service Manual (EK-LSI-FS-SV)*
- MicroVAX I Owner's Manual (EK-KD32A-OM) (For Diagnostics Section)

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

ATTN: Communications Services (NR2/M15)
Customer Services Section

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* Field Service Use Only

CONFIGURATION (MSV11-QA, ETCH REVISION A) 2

2.1 GENERAL

This chapter contains information for configuring the MSV11-QA memory module (etch revision A). Jumper and address switch settings are included.

NOTE: Configuration and installation for the MSV11-QA (etch revision C or later), and the MSV11-QB and MSV11-QC are provided in Chapter 3.

2.2 CONFIGURING THE MSV11-QA (Etch Revision A)

The MSV11-QA (etch revision A) has one red LED to indicate parity errors. The module contains the following jumpers (Figure 2-1).

- Test jumper (W5, W6)
- CSR register selection jumpers (R, P, N, M)
- Enable/disable CSR selection jumper (A, B)
- Enable/disable block mode jumper (W1, W2)
- Enable extended error address jumper (K, L)
- Test jumper (C, D)
- Enable parity error detection jumper (J, H)
- +5 V/+5 VB

The MSV11-QA has two DIP (dual in-line package) switch packs. Each DIP switch pack consists of six switches. The two DIP switch packs are used to set:

- Starting address.
- Ending address.

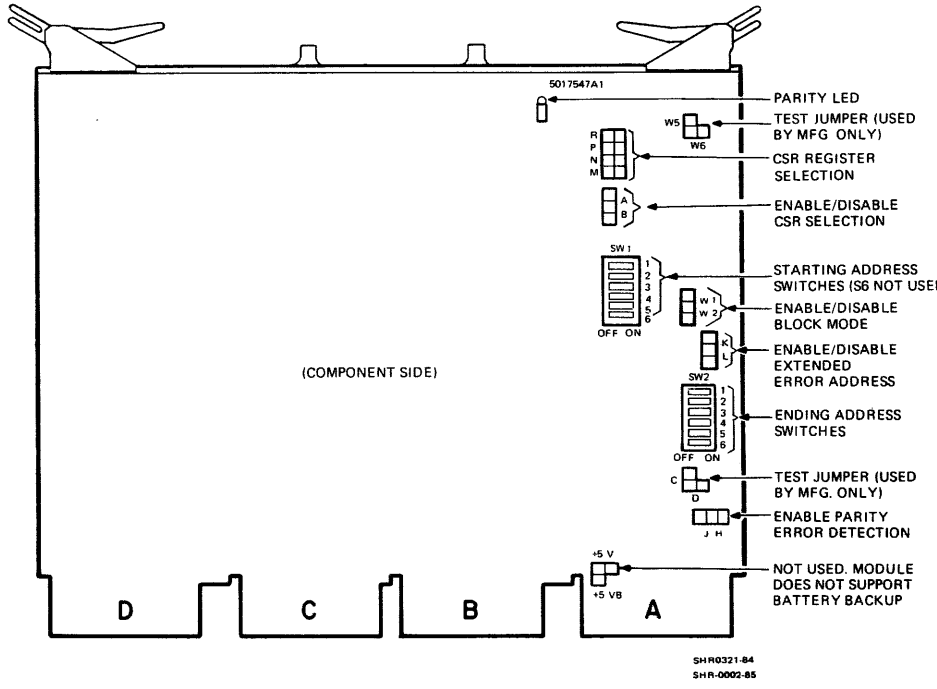
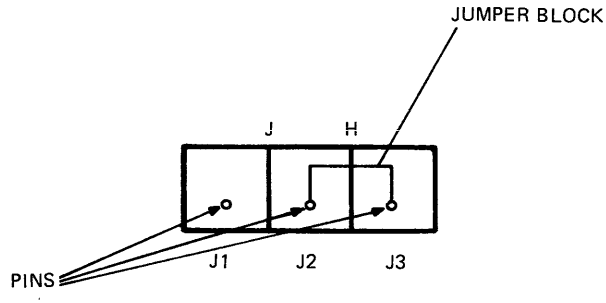
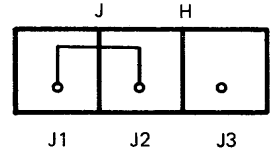


Figure 2-1 Jumper and Switch Locations MSV11-QA (Etch Revision A)

Figure 2-1 shows the physical location of the jumpers and switches. The jumpers and switches are described in the following paragraphs. To jumper two pins, a 0 ohm connector block is used. For example, to enable parity error detection, jumper H (Figure 2-2) is connected (pin J2 to J3) and to disable parity error detection, jumper J is connected (pin J1 to J2). Factory configuration has parity error detection enabled.



a. PARITY ERROR DETECTION ENABLED



b. PARITY ERROR DETECTION DISABLED

SHR-0322-84

Figure 2-2 Jumper Block Example

2.2.1 Test Jumper (W5, W6)

This test jumper is used by manufacturing and should not be changed. W6 should be jumpered and W5 should be open.

2.2.2 CSR Register Selection (R, P, N, M) Jumpers

The MSV11-QA can provide up to 16 CSR register address selections when the user installs or removes appropriate jumper blocks (Figure 2-2). For example, in Figure 2-2, the parity error detection jumper block is shown. Table 2-1 shows the jumper positions and the corresponding CSR register addresses. Figure 2-3 shows the jumper settings for a CSR register address of 17772100.

Table 2-1 CSR Register Selection

Number CSR Memory	Jumper Position R	P	N	M	CSR Register Address
1st	in	in	in	in	17772100
2nd	out	in	in	in	17772102
3rd	in	out	in	in	17772104
4th	out	out	in	in	17772106
5th	in	in	out	in	17772110
6th	out	in	out	in	17772112
7th	in	out	out	in	17772114
8th	out	out	out	in	17772116
9th	in	in	in	out	17772120
10th	out	in	in	out	17772122
11th	in	out	in	out	17772124
12th	out	out	in	out	17772126
13th	in	in	out	out	17772130
14th	out	in	out	out	17772132
15th	in	out	out	out	17772134
16th	out	out	out	out	17772136

If more than one CSR parity type of memory is installed in the system, use care to ensure that no two modules have the same address.

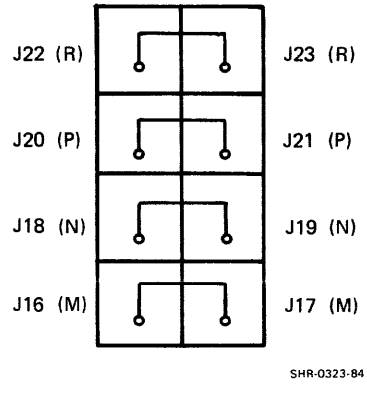


Figure 2-3 Jumper Settings for CSR Address of 17772100

2.2.3 Enable/Disable CSR Selection Jumper (Figure 2-4)

This jumper disables CSR selection when non-parity memory is used. Since the MSV11-QA is a parity memory, this jumper should be set for "enable CSR selection" (jumper B connected).

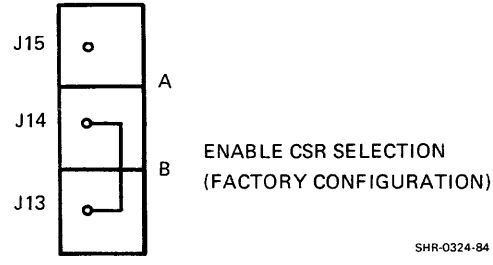


Figure 2-4 Enable/Disable CSR Selection

2.2.4 Enable/Disable Block Mode Jumper (Figure 2-5)

This jumper enables or disables block mode operation. The jumper should be set for "enable block mode" (jumper W1 connected).

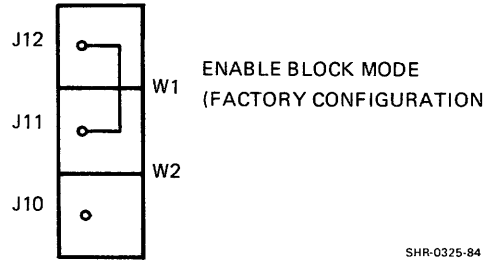


Figure 2-5 Enable/Disable Block Mode

2.2.5 Enable/Disable Extended Error Address Jumper (Figure 2-6)

This jumper selects 18- or 22-bit addressing. The jumper should be set for "enable extended error address" (jumper L connected).

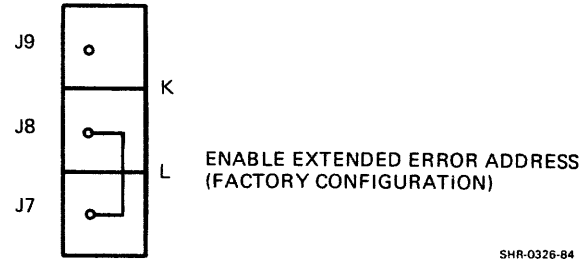


Figure 2-6 Enable/Disable Extended Error Address

2.2.6 Test Jumper C, D (Figure 2-7)

This jumper is a test jumper for use by manufacturing. Jumper C should be connected and jumper D should be open.

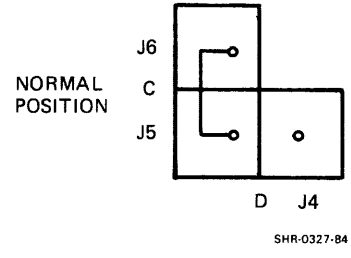


Figure 2-7 Test Jumper

2.2.7 Enable Parity Error Detection Jumper (Figure 2-8)

This jumper enables or disables parity error detection. The jumper should be set for "enable parity error detection" (jumper H connected).

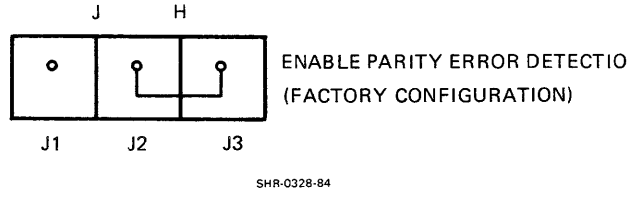


Figure 2-8 Enable/Disable Parity Error Detection

2.2.8 Battery Backup (Figure 2-9)

Not used or supported in etch revision A of MSV11-QA.

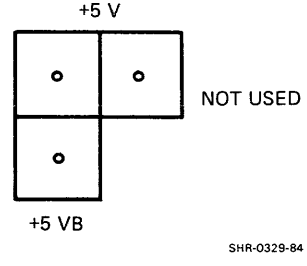


Figure 2-9 Battery Backup

2.2.9 Address Switches

There are two DIP (dual-in-line package) switch packs on the MSV11-QA module. DIP switch pack SW1, containing six switches, selects the starting address. DIP switch pack SW2, containing six switches, selects the ending address. The starting address is set first and then the ending address is set to a number greater than the starting address. Table 2-2 shows the switch settings for the starting addresses and ending addresses. Switch 6 of SW1 is not used. Switch 6 of SW2 is turned on or enabled (0) for a starting address of all 0's and is turned off or disabled (1) for all other starting addresses.

Table 2-2 Starting and Ending Address Selection

Desired Starting Address	SW 1 Switch Position	SW 2 Switch Position	Desired Ending Address	SW 2 Switch Position
In Kbyte	1 2 3 4 5	6	In Kbyte	1 2 3 4 5
0	0 0 0 0 0	0	128	1 1 1 1 1
128	1 1 1 1 1	1	256	0 1 1 1 1
256	0 1 1 1 1	1	384	1 0 1 1 1
384	1 0 1 1 1	1	512	0 0 1 1 1
512	0 0 1 1 1	1	640	1 1 0 1 1
640	1 1 0 1 1	1	768	0 1 0 1 1
768	0 1 0 1 1	1	896	1 0 0 1 1
896	1 0 0 1 1	1	1024 (1 MB)	0 0 0 1 1
1024 (1 MB)	0 0 0 1 1	1	1152	1 1 1 0 1
1152	1 1 1 0 1	1	1280	0 1 1 0 1
1280	0 1 1 0 1	1	1408	1 0 1 0 1
1408	1 0 1 0 1	1	1536	0 0 1 0 1
1536	0 0 1 0 1	1	1664	1 1 0 0 1
1664	1 1 0 0 1	1	1792	0 1 0 0 1
1792	0 1 0 0 1	1	1920	1 0 0 0 1
1920	1 0 0 0 1	1	2048 (2 MB)	0 0 0 0 1
2048 (2 MB)	0 0 0 0 1	1	2176	1 1 1 1 0
2176	1 1 1 1 0	1	2304	0 1 1 1 0
2304	0 1 1 1 0	1	2432	1 0 1 1 0
2432	1 0 1 1 0	1	2560	0 0 1 1 0

Table 2-2 Starting and Ending Address Selection (Cont)

Desired Starting Address In Kbyte	SW 1 Switch Position 1 2 3 4 5	SW 2 Switch Position 6	Desired Ending Address In Kbyte	SW 2 Switch Position 1 2 3 4 5
2560	0 0 1 1 0	1	2688	1 1 0 1 0
2688	1 1 0 1 0	1	2816	0 1 0 1 0
2816	0 1 0 1 0	1	2944	1 0 0 1 0
2944	1 0 0 1 0	1	3072 (3 MB)	0 0 0 1 0
3072 (3 MB)	0 0 0 1 0	1	3200	1 1 1 0 0
3200	1 1 1 0 0	1	3328	0 1 1 0 0
3328	0 1 1 0 0	1	3456	1 0 1 0 0
3456	1 0 1 0 0	1	3584	0 0 1 0 0
3584	0 0 1 0 0	1	3712	1 1 0 0 0
3712	1 1 0 0 0	1	3840	0 1 0 0 0
3840	0 1 0 0 0	1	3968	1 0 0 0 0
3968	1 0 0 0 0	1	4096 (4MB)	0 0 0 0 0

1 = Off Position
0 = On Position

NOTES: Switch S6 of SW1 is not used. For a memory starting address of 0, switch S6 of SW2 should be set to 0 (on). For all other starting addresses, switch S6 of SW2 should be off (1).

CONFIGURATION (MSV11-QA ETCH REVISION C OR LATER, MSV11-QB AND MSV11-QC) 3

3.1 GENERAL

This chapter contains information for configuring and installing the MSV11-QA (etch revision C or later), the MSV11-QB and the MSV11-QC memory module. Jumper and address switch setups are included. Hereafter, in this chapter these variations will be referred to as the MSV11-Q.

NOTE: Configuration and installation for the MSV11-QA (etch revision A) is provided in Chapter 2 of this manual.

3.2 CONFIGURING THE MSV11-Q

The MSV11-Q has one red LED to indicate parity errors. The module contains the following jumpers (Figure 3-1).

- CSR register selection (jumpers J4 through J11)
- Test jumpers used by manufacturing (J1 through J3) (do not remove)
- Battery backup (W1, W2, W3, W4)
- Test jumpers (chip select) used by manufacturing (jumpers J12 through J17) (do not remove)

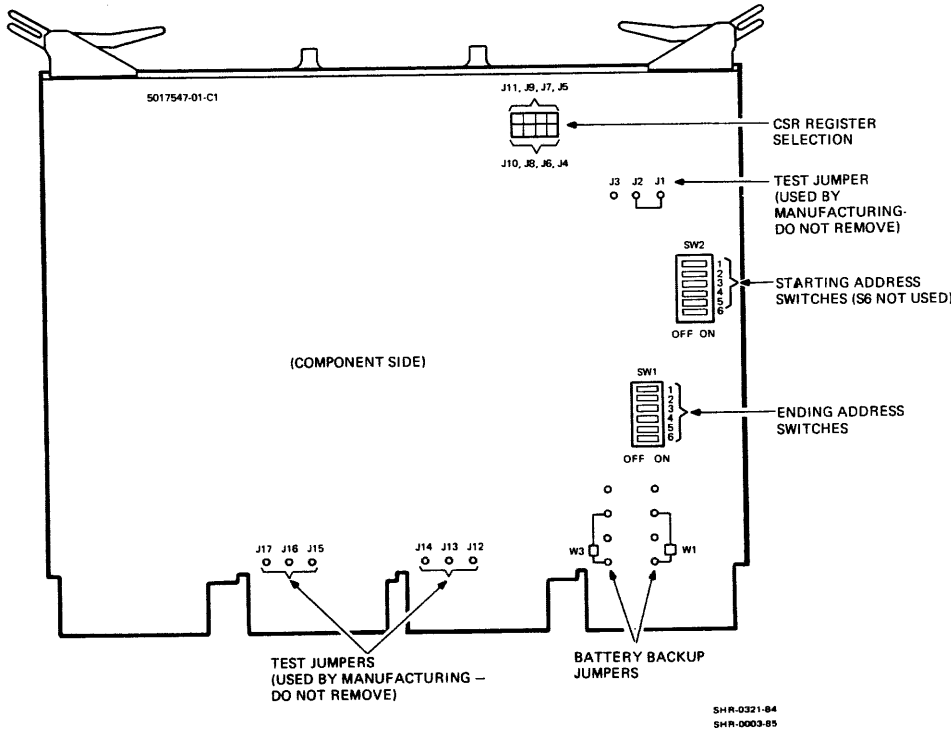


Figure 3-1 MSV11-Q Jumpers and Switches

The MSV11-Q has two DIP (dual in-line package) switch packs. Each DIP switch pack consists of six switches. The two switch packs are used to set:

- Starting address.
- Ending address.

Figure 3-1 shows the physical location of the jumpers and switches. The jumpers and switches are described in the following paragraphs.

3.2.1 CSR Register Selection (Jumpers J4 through J11)

The MSV11-Q can provide up to 16 CSR register address selections when the user installs or removes appropriate jumper blocks (Figure 3-2). Table 3-1 shows the jumper positions and the corresponding CSR register addresses. Figure 3-2 shows the jumper settings for a CSR register address of 17772102 representing a second MSV11-Q installed.

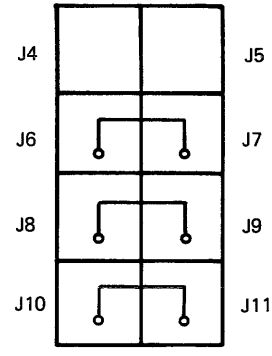


Figure 3-2 Jumper Settings for CSR Address of 17772102

Table 3-1 CSR Register Selection

Number CSR Memory	Jumper Connections J4 to J5	J6 to J7	J8 to J9	J10 to J11	CSR Register Address
1st	in	in	in	in	17772100
2nd	out	in	in	in	17772102
3rd	in	out	in	in	17772104
4th	out	out	in	in	17772106
5th	in	in	out	in	17772110
6th	out	in	out	in	17772112
7th	in	out	out	in	17772114
8th	out	out	out	in	17772116
9th	in	in	in	out	17772120
10th	out	in	in	out	17772122
11th	in	out	in	out	17772124
12th	out	out	in	out	17772126
13th	in	in	out	out	17772130
14th	out	in	out	out	17772132
15th	in	out	out	out	17772134
16th	out	out	out	out	17772136

If more than one CSR parity type of memory is installed in the system, use care to ensure that no two modules have the same address.

3.2.2 Test Jumpers J1 through J3

Test jumpers on J1 through J3 are used by manufacturing and should not be removed by the user (Figure 3-3). Jumper J1 is always connected to J2.

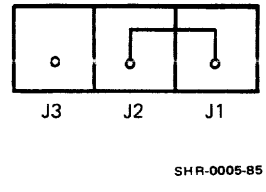


Figure 3-3 Manufacturing Test Jumpers

3.2.3 Battery Backup

The battery backup jumpers are shown in Figure 3-4. Figure 3-4A shows 0 ohm jumpers W2 and W4 connected in a non-battery backed up configuration. Figure 3-4B shows 0 ohm jumpers W1 and W3 connected for the battery backup configuration. These are the only two valid combinations; for example, jumpers W1 and W2 cannot be connected in the circuit at the same time. Other illegal jumper configurations are W1 and W4; W2 and W1; and W2 and W3.

NOTE: On systems using backpanel pin <AE1> sspare 1 for signals other than +5.0 V BBU, jumper W1 may be omitted when module is strapped for battery backup operation. However, Digital Equipment Corporation recommends backpanel pin <AE1> be used as +5.0 V battery backup power in this application. Refer to Paragraph 3.2.3 for additional information.

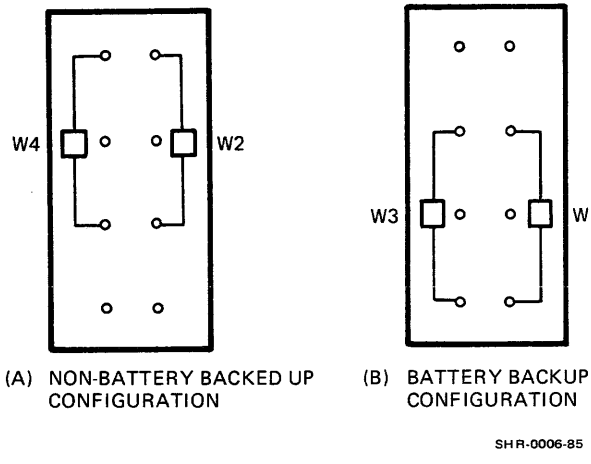
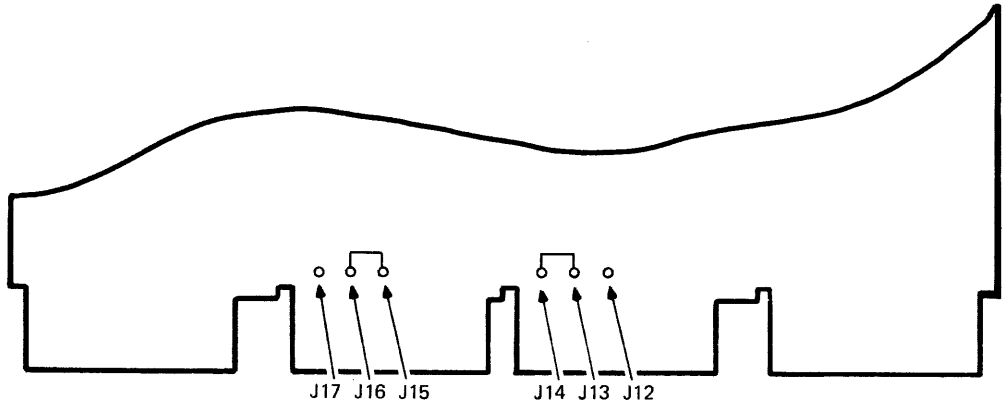


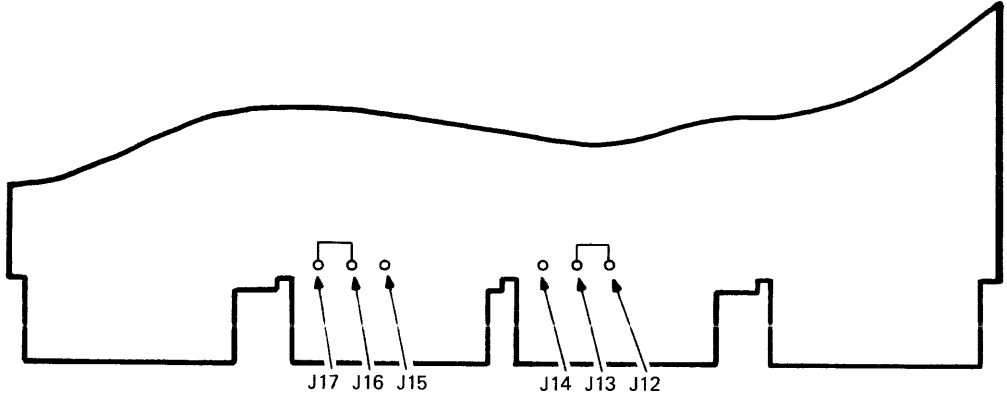
Figure 3-4 Battery Backup

3.2.4 Chip Select Jumpers

The chip select jumpers are J12 through J17 (see Figure 3-5). To select 64K RAMs used in the MSV11-QA (etch revision C or later) memory module, jumper J16 must be connected to J15 and jumper J14 must be connected to J13. To select 256K RAMs used in the MSV11-QB and MSV11-QC memory modules, jumper J17 must be connected to J16 and jumper J13 must be connected to J12. All other jumper combinations are illegal and should not be attempted by the user.



A. MSV11-QA SELECT (64K RAMS)



B. MSV11-QB/MSV11-QC SELECT (256K RAMS)

SHR-0007-85

Figure 3-5 Chip Select Jumpers

3.2.5 Address Switches

There are two DIP switch packs, each containing six switches. DIP switch SW2 selects the starting address of the MSV11-Q. DIP switch SW1 selects the ending address. Table 3-2 shows the switch settings for the starting addresses and ending addresses. Switch 6 of SW2 (starting address) is not used. Switch 6 of SW1 (ending address) is turned on or enabled (0) for a starting address of all 0's and is turned off or disabled (1) for all other starting addresses.

Table 3-2 Starting and Ending Address Selection

Desired Starting Address	SW 2 Switch Position	SW 1 Switch Position	Desired Ending Address	SW 1 Switch Position
In Kbyte	1 2 3 4 5	6	In Kbyte	1 2 3 4 5
0	0 0 0 0 0	0	128	1 1 1 1 1
128	1 1 1 1 1	1	256	0 1 1 1 1
256	0 1 1 1 1	1	384	1 0 1 1 1
384	1 0 1 1 1	1	512	0 0 1 1 1
512	0 0 1 1 1	1	640	1 1 0 1 1
640	1 1 0 1 1	1	768	0 1 0 1 1
768	0 1 0 1 1	1	896	1 0 0 1 1
896	1 0 0 1 1	1	1024 (1 MB)	0 0 0 1 1
1024 (1 MB)	0 0 0 1 1	1	1152	1 1 1 0 1
1152	1 1 1 0 1	1	1280	0 1 1 0 1
1280	0 1 1 0 1	1	1408	1 0 1 0 1
1408	1 0 1 0 1	1	1536	0 0 1 0 1
1536	0 0 1 0 1	1	1664	1 1 0 0 1
1664	1 1 0 0 1	1	1792	0 1 0 0 1
1792	0 1 0 0 1	1	1920	1 0 0 0 1
1920	1 0 0 0 1	1	2048 (2 MB)	0 0 0 0 1
2048 (2 MB)	0 0 0 0 1	1	2176	1 1 1 1 0
2176	1 1 1 1 0	1	2304	0 1 1 1 0
2304	0 1 1 1 0	1	2432	1 0 1 1 0
2432	1 0 1 1 0	1	2560	0 0 1 1 0
2560	0 0 1 1 0	1	2688	1 1 0 1 0
2688	1 1 0 1 0	1	2816	0 1 0 1 0
2816	0 1 0 1 0	1	2944	1 0 0 1 0
2944	1 0 0 1 0	1	3072 (3 MB)	0 0 0 1 0
3072 (3 MB)	0 0 0 1 0	1	3200	1 1 1 0 0

Table 3-2 Starting and Ending Address Selection (Cont)

Desired Starting Address	SW 2 Switch Position	SW 1 Switch Position	Desired Ending Address	SW 1 Switch Position
In Kbyte	1 2 3 4 5	6	In Kbyte	1 2 3 4 5
3200	1 1 1 0 0	1	3328	0 1 1 0 0
3328	0 1 1 0 0	1	3456	1 0 1 0 0
3456	1 0 1 0 0	1	3584	0 0 1 0 0
3584	0 0 1 0 0	1	3712	1 1 0 0 0
3712	1 1 0 0 0	1	3840	0 1 0 0 0
3840	0 1 0 0 0	1	3968	1 0 0 0 0
3968	1 0 0 0 0	1	4096 (4 MB)	0 0 0 0 0

1 = Off Position
0 = On Position

NOTES: Switch S6 of SW2 is not used. For a memory starting address of 0, switch S6 of SW1 should be set to 0 (on). For all other starting addresses, switch S6 of SW1 should be off (1).

UNPACKING AND INSTALLATION 4

4.1 GENERAL

This chapter describes unpacking, pre-installation, and installation procedures for verifying proper system configuration for all variations of the MSV11-Q.

NOTE: This memory is static sensitive. Electro-static Discharge (ESD) precautions must be taken when handling this module outside of its protective container. Use Velostat Kit 29-11762 when handling the module.

4.1.1 Unpacking and Inspection

The MSV11-Q is shipped in special packing cartons to protect the boards from excessive mechanical shock, electrical shock, and vibration, and to give the boards maximum protection during shipment. To unpack the memory, remove any packing materials and visually inspect the memory board for physical damage. Check all hardware attached to the board.

4.1.2 Pre-installation

CAUTION:

1. *You must remove dc power from the backplane during module insertion or removal.*

2. *Be careful when replacing the memory module. Make sure that the component side of the module faces in the same direction as the other modules on the system. The memory module, backplane, or both can be damaged if the module is inserted backwards.*

Before installing any MSV11-Q variation make sure the system is correctly configured.

The pre-installation procedure is given in the following checklist.

1. Check if system power is hooked up correctly and make sure all cables are securely attached.

2. Verify proper system operation.

3. Check if other memory is present and check the addressing range of the memory.

4. Check the CSR address setting of the existing memory, and make necessary CSR jumper settings on the MSV11-Q module according to Table 2-1 for MSV11-QA (etch revision A), or Table 3-1 for MSV11-QA (etch revision C or later), MSV11-QB and MSV11-QC. If no other memory exists in the system, the memory module is factory set at the first CSR address location.

5. If no other memory is present, set the starting address of the MSV11-Q to 0. If other memory is present, set the module starting and ending address accordingly. (See Table 2-2 for MSV11-QA, etch revision A or Table 3-2 for MSV11-QA (etch revision C or later), MSV11-QB and MSV11-QC.)

6. Verify that your system (CPU, peripherals, backplane, and software) is capable of supporting 22-bit addressing.

4.1.3 Installation

The MSV11-Q (all variations) is designed to install in backplanes that are wired for LSI-11/23, PDP-11/23, PDP-11/23 Plus, Micro/PDP-11 computer systems, and MicroVAX I.

After verifying that the appropriate jumpers and switch settings are correct, insert the MSV11-Q memory board into its designated slot.

CAUTION: Do not try to install or remove memory modules with dc power applied to the backplane. Damage to the memory board may occur.

4.1.4 Module Checkout

When memory modules are installed, apply dc power and verify memory operation by running the system diagnostics; in particular, those that test the memory. (Refer to Chapter 6.)

FUNCTIONAL DESCRIPTION 5

5.1 INTRODUCTION

The MSV11-Q memory modules (all variations) interface with the LSI-11 bus. The CPU and DMA devices can become bus master of the LSI-11 bus to transfer or obtain data from memory. The memory is always a slave to whatever device becomes bus master. Figure 5-1 shows the CPU and DMA devices connected to memory via the LSI-11 bus.

Devices that are ready to use the LSI-11 bus must gain control of the bus through the arbitration that takes place in the CPU. The device that wins the arbitration is able to use the bus as soon as bus signals BSYNC and BRPLY are negated. This device is now bus master and can initiate a bus cycle. The types of bus cycles that can be performed are shown in Table 5-1.

All bus cycles are divided into three sequential events.

- Address cycle
- Data cycle
- Bus cycle termination

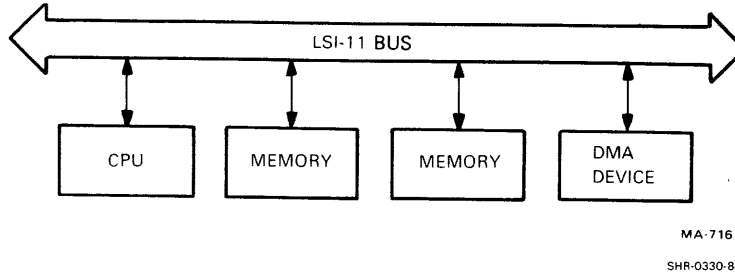


Figure 5-1 Typical System

Table 5-1 Summary of Bus Cycles

Bus Cycle Mnemonics	Description	Function with Respect to Bus Master
DATI	Data word input	Read word
DATO	Data word ouput	Write word
DATOB	Data Byte output	Write byte
DATIO	Data word input/output	Read word, modify, write word
DATIOB	Data word input/byte output	Read word, modify, write byte
DATBI	Data word block mode input	Block mode read
DATBO	Data word block mode output	Block mode write

5.2 LSI-11 BUS SIGNALS AND DEFINITIONS

To transfer data, the bus master must generate the signals shown in Figure 5-2. The slave device (memory) receives the signals and initiates BRPLY. This starts a chain reaction to terminate the bus cycle. Table 5-2 gives the signal names and definitions of the bus signals.

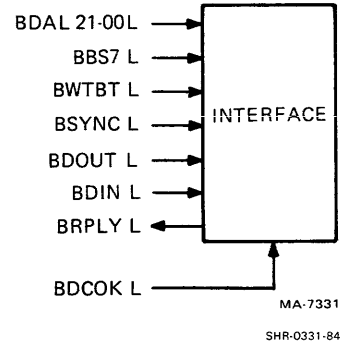


Figure 5-2 MSV11-Q Memory Interface

Table 5-2 Bus Signals

Bus Pin	Mnemonics	Description
AA1	BIRQ5 L	Interrupt request priority level 5
AB1	BIRQ6 L	Interrupt request priority level 6
AC1	BDAL16 L	Extended address bit during addressing protocol; memory error data line during data transfer protocol.
AD1	BDAL17 L	Extended address bit during addressing protocol; memory error logic enable during data transfer protocol.
AE1	SSPARE1 (Alternate +5 B)	On the MSV11-QA (etch revision A), this pin is directly shorted to AV1 and is used for +5 V battery backup power to keep critical circuits alive during power failures.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AF1	SSPARE2 SRUN simultaneously	Special Spare – not assigned or bused in Digital cable or backplane assemblies; available for user interconnection. In the highest-priority device slot, the processor may use this pin for a signal to indicate its RUN state.
AH1	SSPARE3 SRUN simultaneously	Special Spare – not assigned or bused in Digital cable or backplane assemblies; available for user interconnection. An alternate SRUN signal may be connected in the highest-priority set.
AJ1	GND	Ground – System signal ground and dc return.
AK1	MSPAREA	Maintenance Spare – Normally connected together on the backplane at each option location (not bused connection).
AL1	MSPAREB	Maintenance Spare – Normally connected together on the backplane at each option location (not bused connection).
AM1	GND	Ground – System signal ground and dc return.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AN1	BDMR L	Direct Memory Access (DMA) Request – A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt – When BHALT L is asserted for at least 25 μs, the processor services the halt interrupt and responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts in LSI-11 are enabled if W4 on M7264 and M7264-YA processor modules is removed and DMA request/grant sequences are enabled. The processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF L	Memory Refresh – Asserted by a DMA device. This signal forces all dynamic MOS memory units requiring bus refresh signals to be activated for each BSYNC L/BDIN L bus transaction. *CAUTION: The user must avoid multiple DMA data transfers (burst or "hog" mode) that could delay refresh operation. Complete refresh cycles must occur once every 1.6 msec if required.*

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AS1	+12 B or +5 B	+12 Vdc or +5 V battery backup power to keep critical circuits alive during power failures.* This signal is not bused to BS1 in all Digital backplanes. A jumper is required on all LSI-11 Bus options to open (disconnect) the backup circuit from the bus in systems that use this line at the alternate voltage.
AT1	GND	Ground – System signal ground and dc return.
AU1	PSPARE 1	Spare (Not assigned. Customer usage not recommended.) Prevents damage when modules are inserted upside down.
AV1	+5 B	+5V Battery Power* – This pin is directly shorted to AE1 on the MSV11-QA (etch revision A only), and is a secondary +5 V power connection.
BA1	BDCOK H	DC Power OK – Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK – Asserted by the power supply 70 ms after BDCOK negated when ac power drops below the value required to sustain power (about 75 percent of nominal). When negated during processor operation, a power-fail trap sequence is initiated.
BC1	SSPARE4 BDAL 18L (on Q22 only)	On the Q22 Bus, SSPARE4 is bused address line BDAL 18 and is currently not used during data time.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
BD1	SSPARE5 BDAL 19L (on Q22 only)	On the Q22 Bus, SSPARE5 is bused address line BDAL 19 and is currently not used during data time.
BE1	SSPARE6 BDAL 20L	On the Q22 Bus, SSPARE6 is bused address line BDAL 20 and is currently not used during data time.
BF1	SSPARE7 BDAL 21L	On the Q22 Bus, SSPARE7 is bused address line BDAL 21 and is currently not used during data time.
BH1	SSPARE8	Special Spare – Not assigned or bused in DIGITAL cable and backplane assemblies; available for user interconnection.
BJ1	GND	Ground – System signal ground and dc return.
BK1 BL1	MSPAREB MSPAREB	Maintenance Spare – Normally together on the backplane at each option location (not a bused connection).
BM1	GND	Ground – System signal ground and dc return.
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BIRQ7 L	Interrupt request priority level 7
BR1	BEVNT L	External Event Interrupt Request – When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100_8. A typical use of this signal is a line time clock interrupt.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
BS1	+12B	+12 Vdc battery backup power (not bused to AS1 in all Digital backplanes).*
BT1	GND	Ground – System signal ground and dc return.
BU1	PSPARE2	Power Spare 2 (not assigned a function, not recommended for use). If a module is using –12 V (on pin AB2) and if the module is accidentally inserted upside down in the backplane, –12 Vdc appears on pin BU1.
BV1	+5	+5 V Power – Normal +5 Vdc system power.
AA2	+5	+5 V Power – Normal +5 Vdc system power.
AB2	–12	–12 V Power* – –12 Vdc (optional) power for devices requiring this voltage.

NOTE: LSI-11 modules that require negative voltages have an inverter circuit (on each module) that generates the required voltage(s). Hence, - 12 V power is not required with Digital-supplied options.

* Voltages normally not supplied by DIGITAL.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AC2	GND	Ground – System signal ground and dc return.
AD2	+12	+12 V Power – 12 Vdc system power.
AE2	BDOUT L	Data Output – BDOUT, when asserted, implies that valid data is available on BDAL <0:15) L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transactions. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AH2	BDIN L	Data Input - BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize - BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL <21:0> L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte - BWTBT L is used in two ways to control a bus cycle: 1. It is asserted at the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AL2	BIRQ4 L	Interrupt Request Priority Level 4 – A level 4 device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge – In accordance with interrupt protocol, the processor asserts BIAKO L to acknowledge receipt of an interrupt. The bus transmits this to BIAKI L of the device electrically closest to the processor. This device accepts the interrupt acknowledge under two conditions: 1. The device requested the bus by asserting BIRQx L. 2. The device has the highest-priority interrupt request on the bus at that time. If these conditions are not met, the device asserts BIAKO L to the next device on the bus. This process continues in a daisy-chain fashion until the device with the highest-interrupt priority receives the interrupt acknowledge signal.
AP2	BBS7 L	Bank 7 Select – The bus master asserts this signal to reference the I/O page (including that portion of the I/O page reserved for nonexistent memory). The address in BDAL <0:12> L when BBS7 L is asserted is the address within the I/O page.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
AR2 AS2	BDMGI L BDMGO L	Direct Memory Access Grant - The bus arbitrator asserts this signal to grant bus mastership to a requesting device, according to bus mastership protocol. The signal is passed in a daisy-chain from the arbitrator (as BDMGO L) through the bus to BDMGI L of the next priority device (electrically closest device on the bus). This device accepts the grant only if it requested to be bus master (by a BDMR L). If not, the device passes the grant (asserts BDMGO L) to the next device on the bus. This process continues until the requesting device acknowledges the grant. *CAUTION: DMA device transfers must not interfere with the memory refresh cycle.*
AT2	BINIT L	Initialize - This signal is used for system reset. All devices on the bus are to return to a known, initial state; i.e., registers are reset to zero, and logic is reset to state 0. Exceptions should be completely documented in programming and engineering specifications for the device.
AU2 AV2	BDALO L BDAL1 L	Data/Address Lines - These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.

Table 5-2 Bus Signals (Cont)

Bus Pin	Mnemonics	Description
BA2	+5	+5 V Power – Normal +5 Vdc system power.
BB2	–12	–12 V Power* – –12 Vdc (optional) power for devices requiring this voltage.
BC2	GND	Ground – System signal ground and dc return.
BD2	+12	+12 V Power – +12 V system power.
BE2	BDAL2 L	Data/Address Lines – These 14 lines are part of the 16-line data/address bus previously described.
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

SPARES

Nomenclature	Pin Assignment
SSpare1	AE1
SSpare3	AH1
SSpare8	BH1
SSpare2	AF1
MSpareA	AK1
MSpareB	AL1
MSpareB	BK1
MSpareB	BL1
PSpare1	AU1
ASpare2	BU1

5.2.1 LSI-11 Bus Dialogues

The MSV11-Q memory module (all variations) responds to these dialogues: DATI, DATO(B), DATIO(B), DATBO and DATBI. Table 5-3 explains which figure to use with each dialogue.

Table 5-3 Dialogues to Perform Memory Data Transfers

Dialogue	Figure
DATO(B)	5-3
DATI	5-4
DATIO(B)	5-5
DATBO	5-6
DATBI	5-7

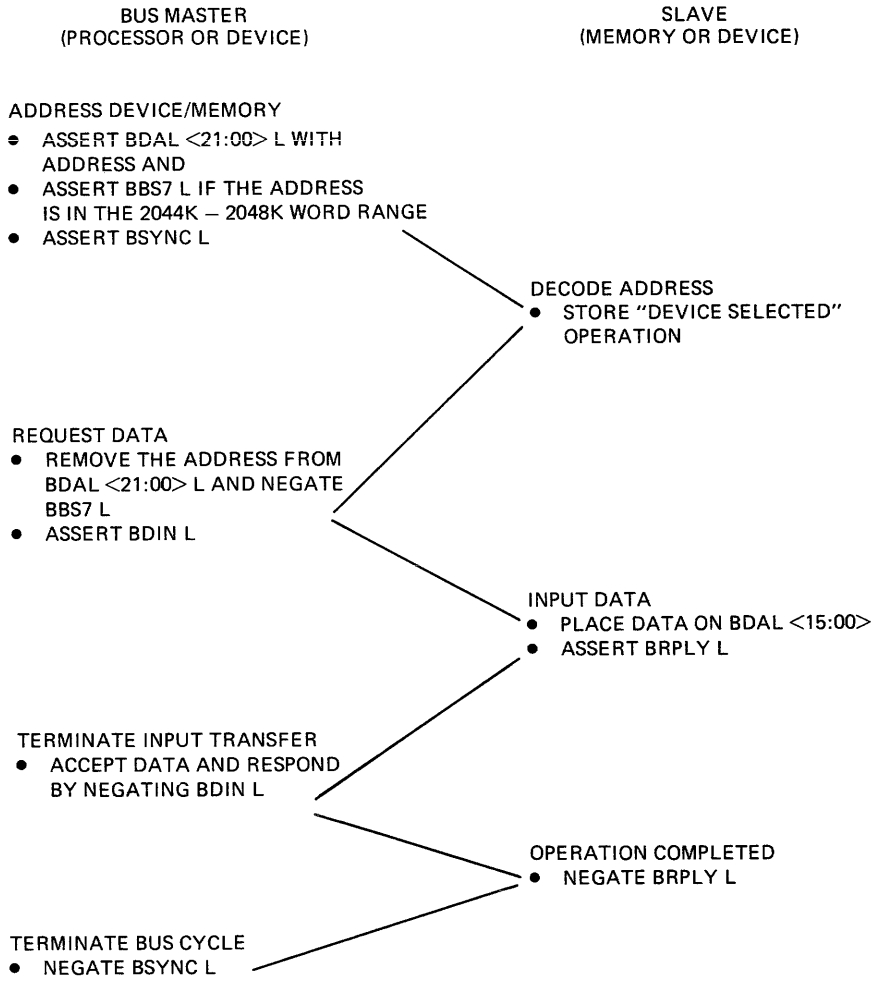


Figure 5-3 DATO or DATOB Bus Cycle

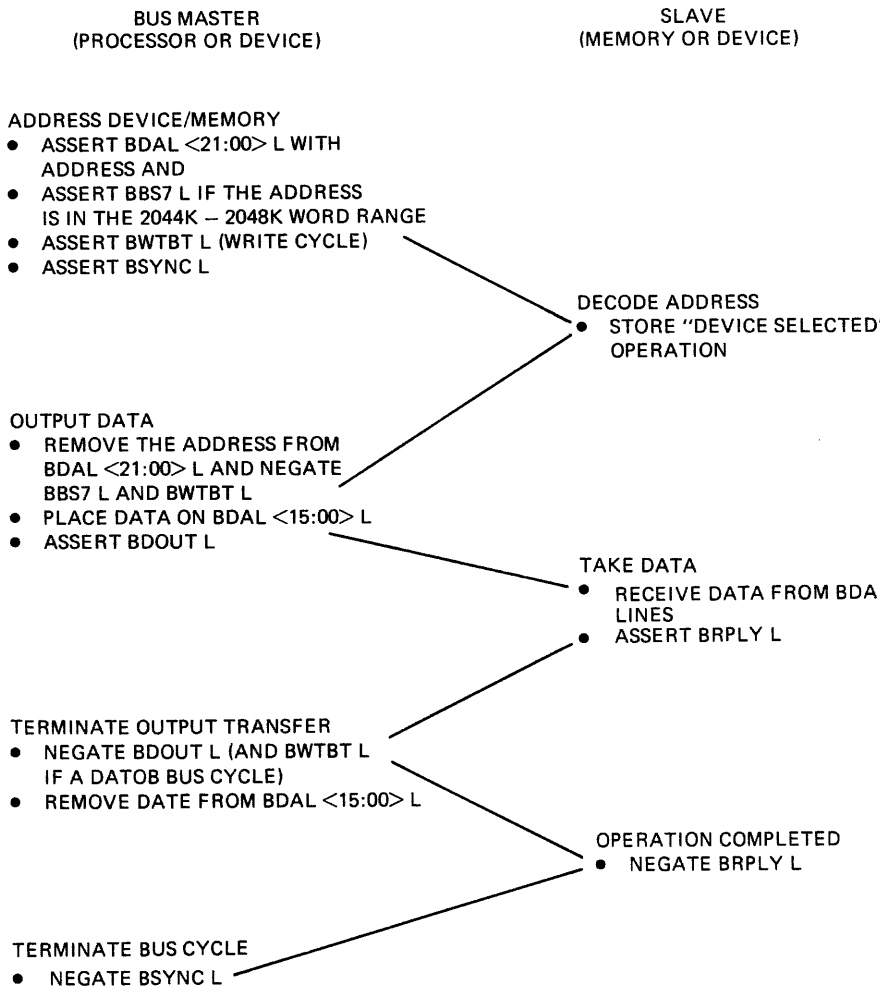


Figure 5-4 DATI Bus Cycle

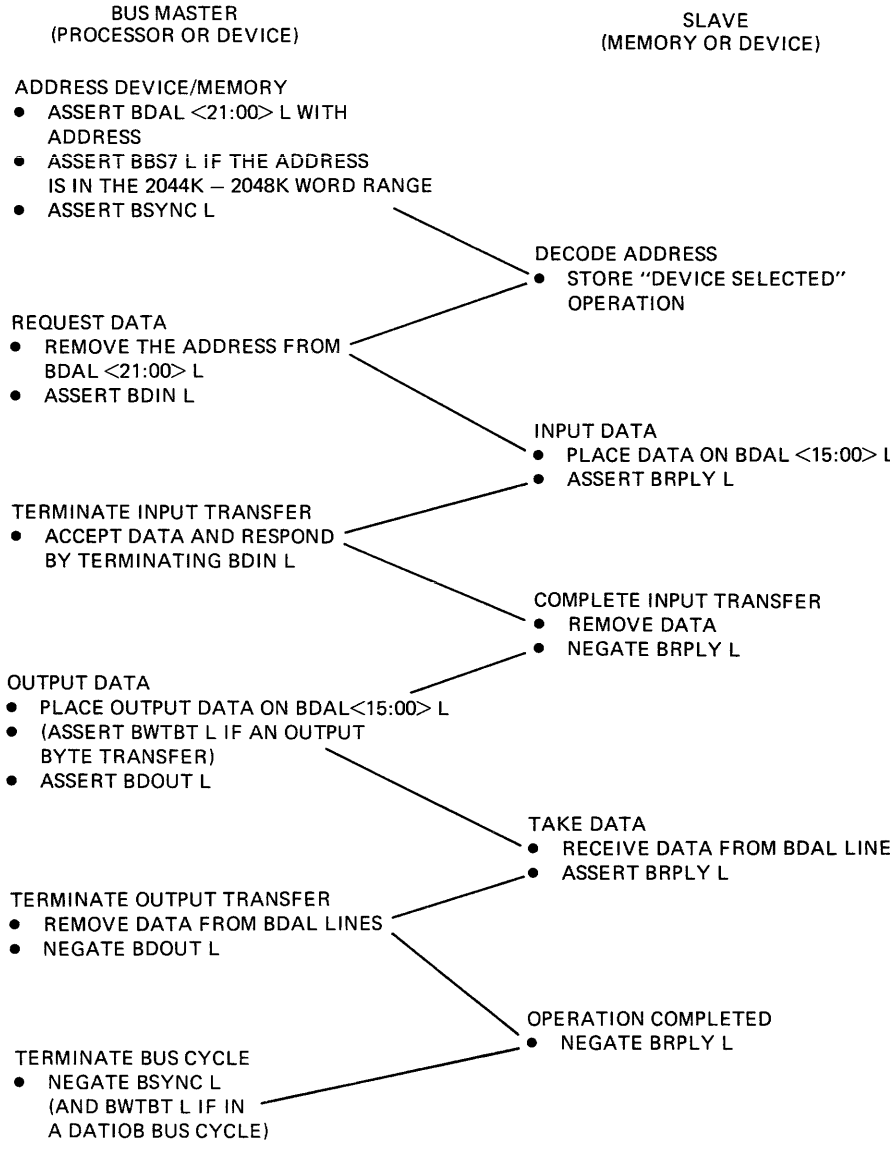


Figure 5-5 DATI or DATIOB Bus Cycle

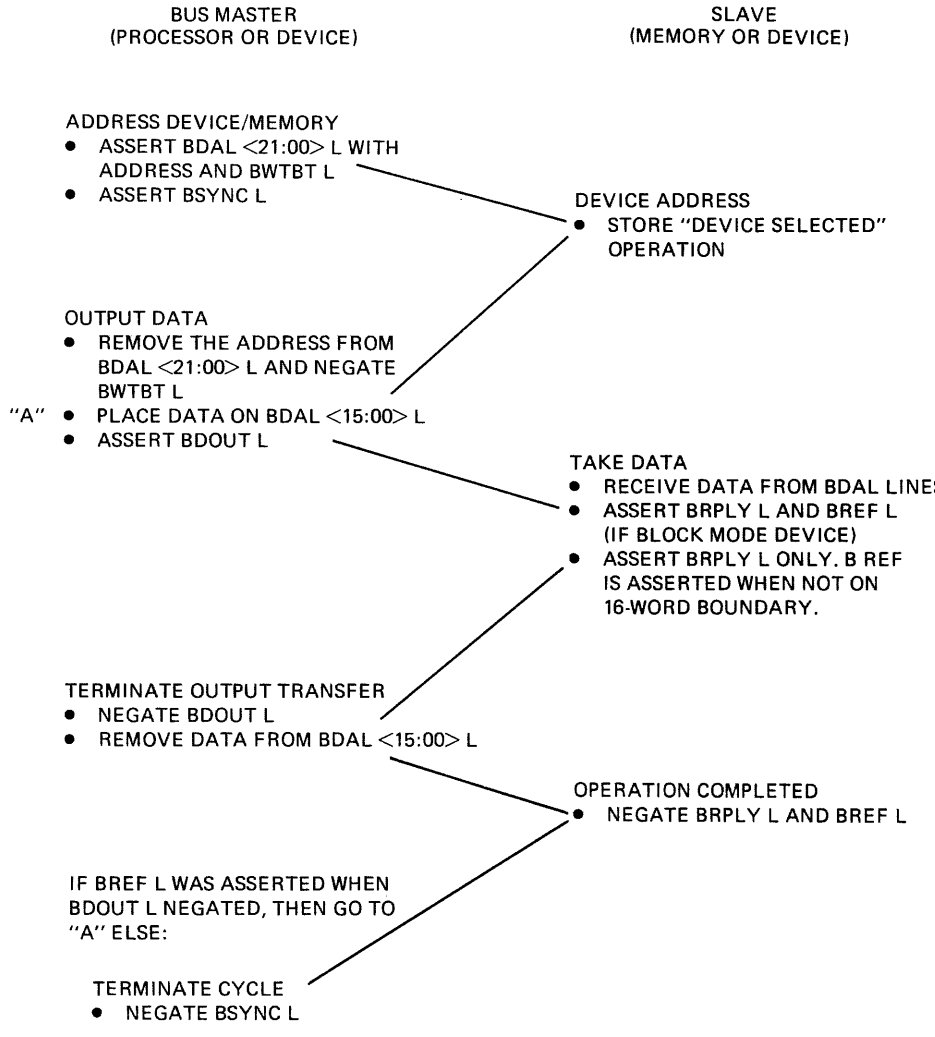


Figure 5-6 DATBO Bus Cycle

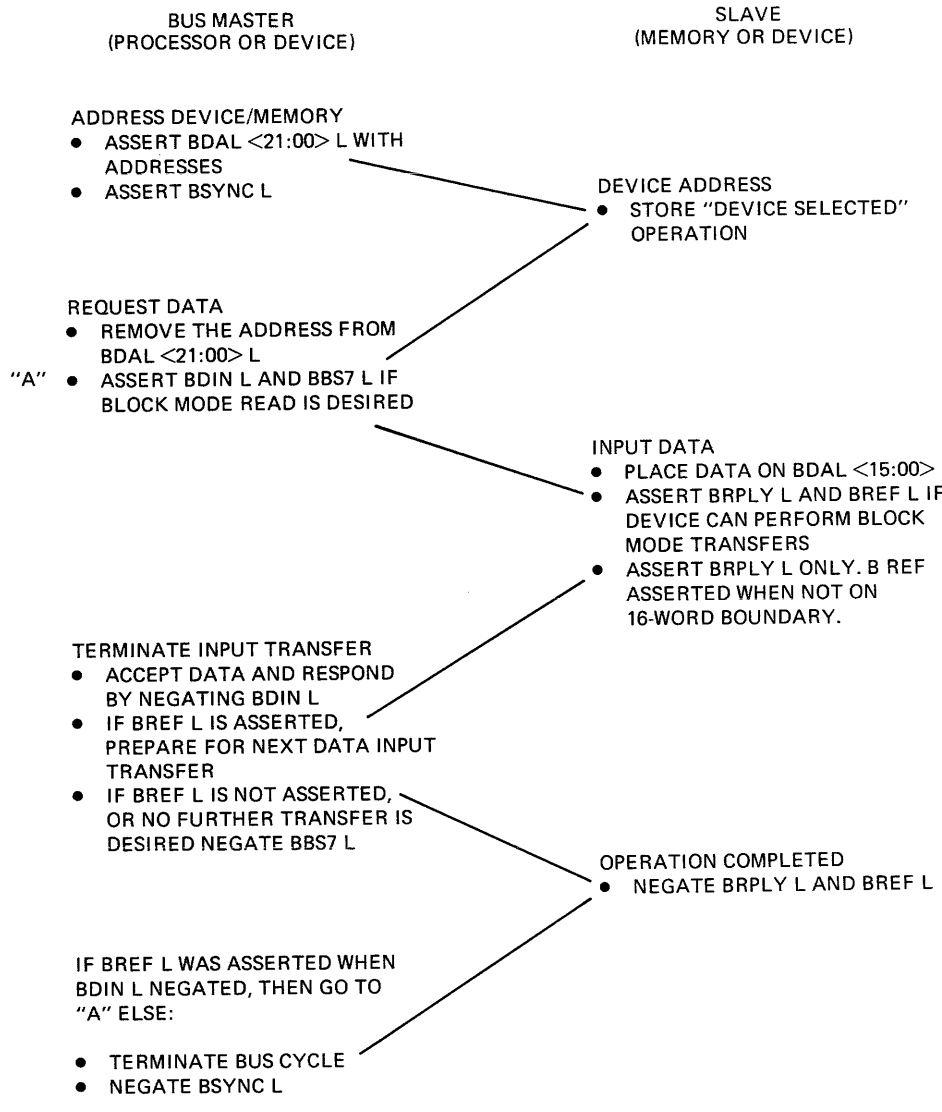


Figure 5-7 DATBI Bus Cycle

5.3 FUNCTIONAL DESCRIPTION OF MEMORY MODULE

Figure 5-8 is a functional block diagram of the MSV11-Q memory module. The following paragraphs describe the basic functions.

5.3.1 Xcvrs (Transmit - Receive)

The Xcvrs are an interface between the Q-bus and the memory array and allow memory to transmit or receive:

Address,
Data, and
Control signals.

In addition, they also provide parity checking and generation, and output data storage.

5.3.2 Address Logic

The memory module contains starting address and ending address switches to set the starting and ending memory addresses. Both starting and ending address switches must be set; otherwise, false accesses above the memory range of addresses may occur. For example, on the MSV11-QA module, if the starting address is set to 0, and only half of the memory array is used, the ending address switch should be set to 0.5 Mb. A set of four CSR jumpers provide for selection of 1 of 16 possible CSR addresses.

5.3.3 Control Signal Xcvrs

The control signal Xcvrs receive and transmit all control signals from the Q-bus. The memory module decodes the control signals to determine what type of access is to occur. The signals entering and leaving the control signal Xcvrs are the normal Q-bus protocol signals previously described.

5.3.4 Address Select Logic

The address select logic detects whether the MSV11-Q is addressed via the Q-bus. If the address select logic decides that the Q-bus address corresponds to the MSV11-Q, a module select (BDSEL) signal is generated. This signal is applied to the cycle arbitration logic to arbitrate the type of cycle.

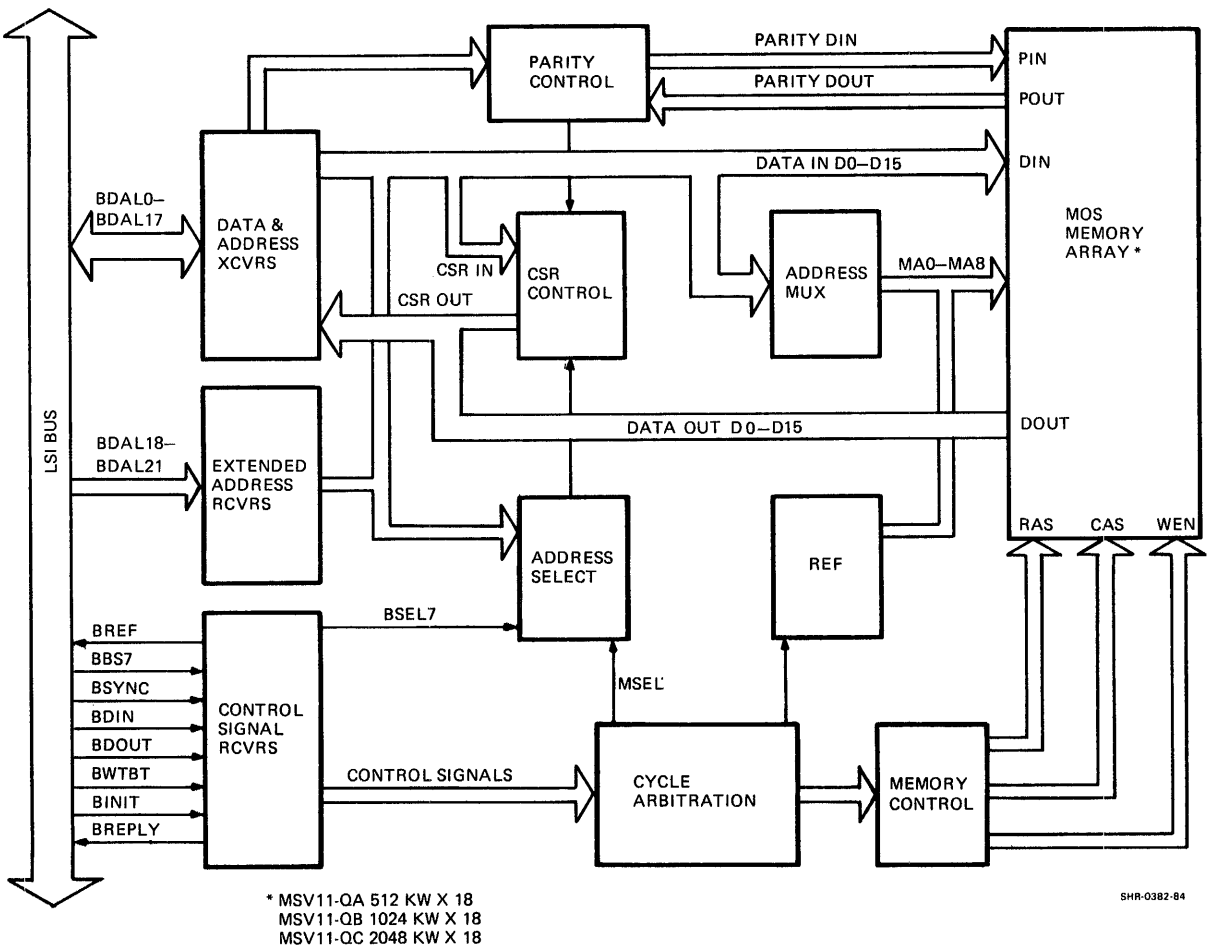


Figure 5-8 MSV11-Q Functional Block Diagram

5.3.5 Cycle Arbitration

Control signals are supplied to the cycle arbitration logic which arbitrate between a CSR access, a memory access, or refresh cycle. If the access is a CSR access, appropriate timing signals are generated to read or write the CSR. If the cycle is a memory access (read, write, write byte, or block mode), RAS (row address strobe) and CAS (column address strobe) signals are generated to enable the row and column address to occur. If the access is a refresh cycle, only RAS is generated. The refresh logic consists of a timer which requests that a memory refresh be performed every 12 μs. The refresh logic also generates a refresh address defining the rows to be refreshed. This occurs asynchronously. All RAMs are refreshed at the same time. Eight RAS pulses are generated to allow one row in each bank of RAMs to be refreshed at the same time. Then the refresh address is incremented and the next row in each bank is refreshed on the next REF REQ until all rows are refreshed. There are 128 rows to be refreshed on the MSV11-QA. There are 256 rows to be refreshed on the MSV11-QB and MSV11-QC. The total refresh time is 535 nanoseconds for each refresh cycle.

5.3.6 Memory Access

During a memory cycle, the Q-bus address is compared with the address space defined by the address switches on board the module. If the addresses match, the address is then transferred to the RAM array via the address multiplexer. First, the row address is latched and the required RAS signal is asserted. Then, the memory control logic switches to provide the column address and CAS is asserted.

During block mode, the address is incremented at the end of each memory cycle. The cycle is restarted, and a new address is supplied to the RAMs. Up to 16 words can be transferred in rapid succession in this mode.

5.3.7 Parity

During a write cycle, parity is generated on each byte written to the memory array; consequently, two parity bits are generated for each memory word (one parity bit for upper byte and one for lower byte). During a read cycle (DATI) parity is checked in the parity control logic. If a parity error occurs, a red LED on the board turns on and the error address is strobed into the CSR. Bits 11 through 21 of the address containing the parity error are stored in the CSR in bit locations 5 through 11, as described below (Figure 5-9).

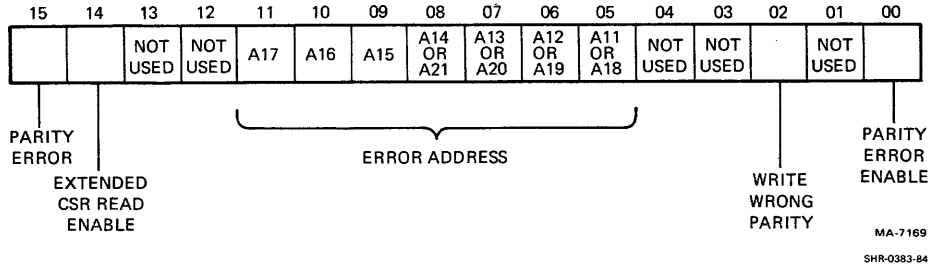


Figure 5-9 CSR Bit Allocation

To determine the failed address, perform the following:

1. Read the CSR. This provides bits 11 through 17 of the failed address.

2. Set bit 14 of the CSR (extended CSR read enable).

3. Read the CSR. CSR bit locations 5 through 8 store bits 18 through 21 of the failed address. These bits are referred to as extended error address bits.

4. Reset bit 14.

5.4 CONTROL AND STATUS REGISTER (CSR) BIT ASSIGNMENT

The control and status register (CSR) in the MSV11-Q allows program control of certain parity functions, and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared by assertion of BUS INIT L. This signal is asserted for a short time by the processor after system power has come up, or in response to a reset instruction. Figure 5-9 shows the CSR bits. They are described in the following paragraph.

Bits 1, 3, 4, 12, and 13	These bits are not used and are always read as logical zeros. Writing into these bits has no effect on the CSR.
Bit 0	Parity Error Enable – If a parity error occurs on a DATI or DATIO(B) cycle to memory, and bit 0 is set (1), then BDAL 16 L and BDAL 17 L are asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power up or BUS INIT.
Bit 2 Maintenance Only	Write Wrong Parity – If this bit is set (1) and a DATO or DATOB cycle to memory occurs, wrong parity data is written into the parity MOS RAMs. This bit can be used to check the parity error logic as well as failed address information in the CSR. • Bit 2 is a read/write bit reset to zero on power up or BUS INIT.
Bits 3, 4	Not used.

Bits 05 through 11

Error Address Bits – If a parity error occurs on a DATI or DATIO(B) cycle, then A11 through A17 are stored in CSR bits 5 through 11 and bits A18 through A21 are latched. The 128K word machines (18-bit address) require only one read of the CSR register to obtain the failed address bits. CSR bit 14 = 0 allows the logic to pass A11 through A17 to the LSI-11 bus. A 2048K word machine (22-bit address) requires two reads. The first read (CSR bit 14 = 0) sends contents of CSR bits 5 through 11. Then the program must set CSR bit 14 (1). This enables A18 through A21 to be read from CSR bits 05 through 08.

The parity error addresses locate the parity error to a 1K segment of memory. These bits are read/write and are not reset to zero via power up or BUS INIT. If a second parity error is found the new failed address is stored in the CSR.

Bit 14

Extended CSR Read Enable – The use of this bit was explained in the error address description.

Bit 14 = 0, always for 128K word machine

Bit 14 = 0, first read on 2048K word machine

Bit 14 = 1, second read on 2048K word machine

Bit 14 is a read/write bit reset to 0 on power up or BUS INIT.

Bit 15	Parity Error – This bit, when set, indicates that a parity error has occurred. The bit then turns on a red parity LED on the module. This provides visual indication of a parity error. Bit 15 is a read/write bit. It is reset to zero via power up or BUS INIT and remains set unless rewritten or initialized.

MAINTENANCE 6

6.1 GENERAL

The maintenance procedures in this chapter apply to the MSV11-Q memory module. To perform corrective maintenance on this module, the user must understand basic operation of the MSV11-Q memory module as described in the previous chapters. This knowledge, together with diagnostic testing knowledge, will help the user isolate MSV11-Q malfunctions.

CAUTION: ALL power must be off before installing or removing modules. Always be sure the component side of the memory faces in the same direction as the other modules within the LSI system.

NOTE: This memory is static sensitive. ESD (electro static discharge) precautions must be taken when handling the module outside of the protective container. Use Velostat kit 29-11762 when handling the module.

6.2 PREVENTIVE MAINTENANCE

Preventive maintenance pertains to specific tasks, performed at intervals, to detect conditions that may lead to performance deterioration or malfunction. The following tasks can be performed along with other preventive maintenance procedures for the LSI computer system, but are not mandatory on a scheduled basis.

1. Visual inspection
2. Voltage measurements
3. Diagnostic testing

6.2.1 Visual Inspection

Inspect the modules and backplane for broken wires, connectors, or other obvious defects.

6.2.2 Power Voltage Check

Once primary power has been turned on, check the dc power voltage at the backplane. Refer to Table 1-3 for MSV11-QA, (etch revision A). Refer to Table 1-4 for MSV11-QA (etch revision C or later), MSV11-QB, and MSV11-QC.

6.3 DIAGNOSTIC TESTING

Memory diagnostic programs to test the MSV11-Q memory modules are available from Digital.

For MicroVAX systems, the memory test (EHXMS) is part of MicroVAX Diagnostics I contained on the diagnostic diskette.

For fault isolation in other 22-bit systems and 18-bit systems use the MAINDEC-11 CVMSA (22-bit system) diagnostic.

Detailed operating instructions and program listings are included with each diagnostic software kit.

6.3.1 MicroVAX Memory Diagnostic 1 (EHXMS)

The MicroVAX Memory diagnostic 1 (BL-T856C-DE) verifies the correct functioning of MSV11-Q memory modules. The lowest acceptable revision for EHXMS is Version 1.3.

WARNING: This diagnostic will eliminate the current contents of system memory.

Each MSV11-QA memory module has 1 megabyte of MOS memory using 64K memory chips.

Each MSV11-QB memory module has 2 megabytes of memory using 256K memory chips (half-populated). Each MSV11-QC memory module has 4 megabytes of memory using 256K memory chips (full populated).

This diagnostic identifies a memory board that failed. Run this diagnostic when the operating system detects memory errors or when intermittent program failures suggests a problem in the memory subsystem.

Run this diagnostic after first running the CPU diagnostic to verify that the CPU is functioning correctly.

The Memory diagnostic (EHXMS) is distributed on the diskette labeled "MicroVAX Diagnostics 1." The diagnostic requires 30 kilobytes of memory to run. It takes approximately 48 minutes to run the diagnostic with parity test enabled. Without parity test enabled, run time is 28 minutes. The default occurs with parity enabled. To disable parity, use EHXMS>DISABLE PARITY.

6.3.1.1 Bootstrapping Procedure – The memory diagnostic is a standalone diagnostic and is bootstrapped by inserting the diskette into the RX50 diskette drive n and typing:

```
>>>B/100 DUAn (where n = 0 through 7)
Bootfile:  [SYS0.SYSMAINT]EHXMS.EXE
```

6.3.1.2 Operation – Once the diagnostic is bootstrapped, it produces a header message that contains the Memory diagnostic version number. You are then prompted to issue commands that control the diagnostic.

6.3.1.3 Command Syntax – You may issue commands either in upper- or lowercase. They are displayed in uppercase. Before ending a line with a Carriage Return, you may enter any of the editing characters shown in Table 6-1. The convention ^U or ^R means that you hold down the CTRL (Control) key and press the U or R key at the same time.

Commands and option keywords may be abbreviated to the first letter. The commands are summarized in Table 6-2 and then fully described.

Table 6-1 Control Keys

Key	Function
Delete	Backspaces one character and deletes it. A backslash (\) is printed, followed by the deleted character and another backslash.
^U	You may use ^U instead of Delete to delete an entire line. The text you have typed on the current line is ignored and a Carriage Return is performed. You may then reenter the line.
^R	Performs a Carriage Return and redisplays the current line. The cursor is left at the end of the line so that you can continue typing input. Use ^R when you have deleted a lot of characters on the line and cannot easily read its contents.

Table 6-2 Command Summary

Command	Function
DISABLE	Disables a feature selected with the ENABLE command.
ENABLE	Selects a test feature.
HELP	Produces information about using the memory diagnostic commands.
MEMORY_SIZE	Specifies the amount of available memory.
START	Starts the test sequence.
VIEW	Lists the status of all ENABLE and DISABLE command options.

6.3.1.4 Using the Commands – Commands may be issued in any order, but the START command must be the last command issued. No testing occurs until the START command is issued.

All commands are optional except the MEMORY_SIZE and START commands. An informational message is issued if you specify a START command without first specifying the size of memory. The most common way to use this diagnostic is to issue a MEMORY_SIZE command followed by a START command. This begins run of the full diagnostic with all of the default ENABLE and DISABLE options.

When a START or START 0 command is issued, the diagnostic begins testing at the first test and continues until all tests run or an error is found. If test 2 (Memory Configuration Test) is run, and a memory map is requested, a short pictorial map is output on the console terminal. This map may be used to detect installation errors and is also used to map a failing address to the appropriate MSV11-Q memory module. At the end of the last test, the diagnostic relocates itself in memory (if the RELOCATE option is enabled) and the test sequence is repeated on the memory that the diagnostic occupied. After this second test sequence, the diagnostic is moved back to the memory it previously occupied. Figure 6-1 shows this concept.

At the end of the test pass, a message is output indicating that testing is completed and the entire test is then repeated.

If a test number is specified with the START command, testing starts at the specified test, and continues executing that test (looping) until you stop it.

Typing ^C (CTRL/C) any time during the test process causes the diagnostic to halt testing (software halt) and return the command prompt. The ENABLE and DISABLE command options and the memory size are saved. You may rerun the same test sequence by issuing a START command on its own, or you may change the commands to run the test in a different way. The HALT pushbutton on the system unit front control panel provides a hardware halt. This action is not recommended unless the user understands the diagnostic and the various implications.

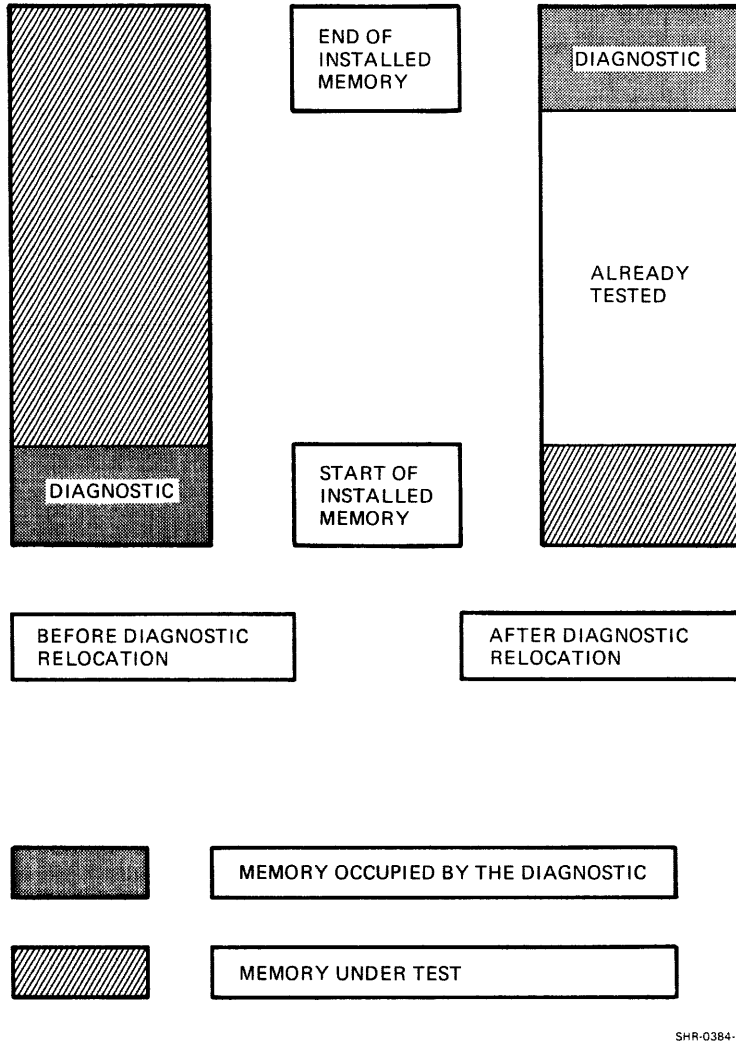


Figure 6-1 Memory Diagnostic Relocation

Figure 6-2 shows a sample diagnostic run. The test system has 2 megabytes (2048 kilobytes) of memory (one MSV11-QA configured to start at physical address 0, and one MSV11-PL configured to start at physical address 00100000 and one MSV11-PL configured to start at physical address 00180000) (hex notation).

6.3.1.5 Test Procedure – Memory must be contiguous in the physical address space and the first memory module installed must be jumpered to start at physical address 0. The diagnostic produces an optional memory map that provides a picture of how memory modules have been installed. This map correlates a failing memory location to a particular memory module. The map is a matrix of 256 elements, one element for each possible 16 kilobyte memory element in the 22-bit memory address space. The map is organized in four rows of 64 columns; each row represents 1 megabyte of memory. The row and column headings may be used to form the starting physical address of the 16 kilobyte element in memory. The row headings provide the most significant 2 bits of the 22-bit physical address. They are represented as 32-bit hexadecimal numbers in the actual map output, with five placeholding X's for the 20 least significant bits (five hexadecimal digits) of the memory address.

The five least significant hexadecimal digits may be read down vertically as the column headings.

For example, the physical base address of the memory described by the intersection of row two and column four is 0010C000 (001X X000 + 0C000). The address range is from the base address for 16 kilobytes, or from 0010C000 to 0010FFFF inclusive.

In each memory element of the matrix there is a flag describing the status of memory at that location. The entry is any of the following.

A blank – signifying that no memory is installed at that address.

A hexadecimal digit – containing the memory controller number associated with that memory.

A ? – signifying that more than one memory controller is specified (this indicates a configuration error).

An * – signifying that non-MSV11-QA memory, such as MRV11-D PROM, is in the bank.

```
EHXMS>STA
Testing started.

Memory Map:   !0000111122223333444455556666777 78889999AAAABBBBCCCCDDDDEEEEFFFF!
              !048C048C048C048C048C048C048C048C 048C048C048C048C048C048C048C048C!

              +--------------------------------+--------------------------------+
000X X000     !00000000000000000000000000000000!00000000000000000000000000000000!
              +--------------------------------+--------------------------------+
001X X000     !11111111111111111111111111111111!22222222222222222222222222222222!
              +--------------------------------+--------------------------------+
002X X000     !                                !                                !
              +--------------------------------+--------------------------------+
003X X000     !                                !                                !
              +--------------------------------+--------------------------------+

                    Key: <SPACE>   No memory responds in this 16 Kb bank.
                           0-F     Memory controller number
                            ?      Error - more than one memory controller.
                            *      Non-MSV11 memory in this bank.

Memory module 0 is an MSV11-Q and contains 00000000 to 00100000 (CSR = 772100)
Memory module 1 is an MSV11-PL and contains 00100000 to 00180000 (CSR = 772102)
Memory module 2 is an MSV11-PL and contains 00180000 to 00200000 (CSR = 772104)

Each complete pass of this diagnostic takes about 96 minutes.
Disabling parity testing (via DISABLE PARITY) reduces this to 56 minutes.
End of test pass 1, no errors detected.
End of test pass 2, no errors detected.
End of test pass 3, no errors detected.
End of test pass 4, no errors detected.
End of test pass 5, no errors detected.
End of test pass 6, no errors detected.
End of test pass 7, no errors detected.
End of test pass 8, no errors detected.
End of test pass 9, no errors detected.
End of test pass 10, no errors detected.
End of test pass 11, no errors detected.
```

Figure 6-2 Sample Diagnostic Run for MSV11-QA/MSV-11P

For example, in the example map output, the entry for 00190000 is 2, signifying that memory is contained on the third memory card (controller 2) on the system.

At the end of the map, a summary is printed. This summary shows which memory modules control which memory ranges, and the type of memory used.

6.3.1.6 Error Messages – Whenever the diagnostic finds an error it produces an error message. The format of the error message depends on whether the error is caused by an invalid command entered by you, or an error in the memory under test.

Error messages produced as a result of incorrect input have the format:

EHXMS – [text]

The message test can be:

EHXMS – Command [command name] is unknown. Try HELP for some information.

EHXMS – The [command name] command takes no arguments. Excess user input [input] ignored.

EHXMS – The [command name] command accepts an optional decimal number. [text] is not decimal.

EHXMS – The [command name] command requires an argument.

EHXMS – [command name] is not a valid DISABLE or ENABLE option keyword. Try HELP for help information.

EHXMS – Test number [number] is incorrect. Test numbers range from 1 to 12.

EHXMS – The memory size specified is incorrect; valid memory sizes range from 256 kilobytes to 4096 kilobytes.

EHXMS – The memory size specified is incorrect; valid memory sizes are multiples of 256 kilobytes.

Error messages produced as a result of an error in the memory under test are listed if the MESSAGE option is specified with the ENABLE command.

NOTE: The default is to have messages enabled. The messages have the format:

EHXMS – Error during test [number] subtest [number] [testname], [subtestname] [test]

The first line of the error message identifies the test and subtest numbers of the test item that failed.

The second line of text supplies the test and subtest names.

The third line of the error message is a description of the error detected. The message text can be:

Data error at location [location]; expected [data], received [data]

Memory Parity error detected testing location [location]

Memory Timeout error detected testing location [location]

Memory does not respond from [location] to [location]

Memory module [module] did not respond to any memory addresses

Memory module with CSR at [address] is misconfigured; CSRs must be contiguous.

Memory size incorrect; expected [number] kilobytes, actually found [number] kilobytes

Memory size of [number] kilobyte is not a multiple of 256 kilobytes

There are addressing conflicts present; see map for more details

Unexpected Machine Check (reason = [number]) testing location [location]

First 256 kilobytes of memory not present

Interrupt/exception/trap via SCB offset [offset] testing location [location]

The following error message requires that you run the CPU diagnostic, recheck the memory and replace any faulty memory modules. If the fault persists you may need to replace the CPU.

Unexpected trap or exception or interrupt
Via SCB vector [vector]
Return PC would be [number]

6.3.2 MSV11-Q DIAGNOSTIC (LSI-11 BUS)

The CVMSAA diagnostic tests the MSV11-Q memory on the LSI-11 bus. This program has the ability to test memory from address 000000 to address 17757777. It does so using:

1. Unique addressing techniques.
2. Worse case noise patterns, and
3. Instruction execution throughout memory.

6.3.2.1 Hardware Requirements – The following hardware is needed to run CVMSAA.

LSI-11/2,
LSI-11/23 bus family processors
Minimum of 32 kilobytes of memory.

Optional Hardware

Any parity memory control module
KTF11 memory management

6.3.2.2 Software Requirements – The smallest unit of memory this program recognizes is 16 kilobytes. If any address in a 16 kilobyte bank causes a time out trap, the program ignores that entire bank of memory. The program tests memory in 16 kilobyte banks, unless it is the last 8 kilobytes before the I/O page or last 12 kilobytes in a 60 kilobyte system.

The program exercises the vector portion of memory (locations 0 – 776) in exactly the same manner as the rest of memory.

This means that the results are unpredictable if:

- Memory management is not available or is disabled (SW12=1)
- Program is relocated out of bank 0
- Locations 0 – 776 are selected for test
- Unexpected hardware trap occurs

6.3.2.3 Hardware Restrictions – It is recommended *not* to mix 18-bit memories with 22-bit memories.

6.3.2.4 Related Documents and Standards – Refer to these documents as needed.

Programming Practices – Document Number 175-003-009-01
PDP-11 MainDEC Sysmac Package – MainDEC-11-DZQAC-C5-D
Applicable Memory System Maintenance Manual
Applicable Circuit Schematics

6.3.2.5 Diagnostic Hierarchy Prerequisites – Before running this program, run a CPU diagnostic to verify the functionality of the processor and PDP-11 instruction set. For LSI-11/23:CJKDB Diag (latest revision); for LSI-11/2:CVKAA Diag (latest revision)

If memory management is to be used, then also run the KTF11 diagnostic CJKDA.

6.3.2.6 Assumptions – This program assumes correct operation of the CPU and the memory management option (if used).

6.3.2.7 Loading the Program – Load the program using XXDP or any standard absolute loader. At starting address 200: Normal program execution proceeds. At starting address 204: Program is restarted using previously selected parameters.

6.3.2.8 Special Environments – If the program is run in automatic mode under ACT11 or APT11 the program is done after the first pass. Also, the program does not relocate to test the lower 16 kilobytes of memory after the first pass.

6.3.2.9. Program Options – The software switch register (location 176) is used for all operational switch settings. The user can type CTRL G (^G) to allow switch register changes during program execution.

SW15 = 1 or up..... HALT ON ERROR
SW14 = 1 or up..... LOOP ON TEST
SW13 = 1 or up..... INHIBIT ERROR TYPEOUT
SW12 = 1 or up..... INHIBIT MEMORY MANAGEMENT (INITIAL START ONLY)
SW11 = 1 or up..... INHIBIT SUBTEST ITERATION (NOT USED)
SW10 = 1 or up..... RING BELL ON ERROR
SW9 = 1 or up..... LOOP ON ERROR
SW8 = 1 or up..... LOOP ON TEST IN SWR<4:0>
SW7 = 1 or up..... INHIBIT PROGRAM RELOCATION
SW6 = 1 or up..... INHIBIT PARITY ERROR DETECTION
SW5 = 1 or up..... INHIBIT EXERCISING VECTOR AREA LOCATIONS (0-1000)

6.3.2.10 Execution Times – Execution time is dependent on type of memory and amount of memory. The following are worse case run times with MOS memories.

For Parity Memory

Full Pass:	Approximately 40 minutes for 1024 kilobytes

6.3.2.11 Error Reporting – There are a total of 31 (octal) types of error reports generated by the program. The following describes some of the key column heading mnemonics for clarity.

PC =	Program counter of error detection code (V/PC=P/PC)
V/PC =	Virtual program counter. This is where the error detection code can be found in the program listing.
P/PC =	Physical program counter. This is where the error detection code is actually located in memory.
TRP/PC =	Physical program counter of the code which caused a trap.
MA =	Memory address
REG =	Parity register address
PS =	Processor status word
IUT =	Instruction under test
S/B =	What contents should be
WAS =	What contents were (was)

6.3.2.12 Error Halts – With the 'Halt on Error' switch (SW15) not set, there are several programmed 'Halts' in the program.

1. In the error trap service routine for unexpected traps to vector 4, one occurs if a second trap to 4 occurs before the error report for the first has had a chance to print out.

2. In the relocation routine, if the program is relocated back to the first 16 kilobytes of memory and the program code was not able to be transferred properly.

3. In the case of error reporting and there is no terminal to allow the information transfer.

4. In the power fail routine, if the power up sequence was started before the power down sequence had a chance to complete itself.

5. Failures to find a meaningful map in the memory mapping routine or any of the address control routines.

6.3.2.13 Sub-test Summaries – The following briefly describes the tests.

Section 1: Address Tests
These tests verify the uniqueness of every memory address.

Test 1 writes and reads the value of each memory word address into that memory location. After all memory has been written, all locations are checked again.

Test 2 writes the byte value of each address into that byte location and checks it.

Test 3 writes the complement of each word address into that location and checks it.

Test 4 writes the 8K bank number into each byte of that bank and checks it.

Test 5 writes the complement of the bank number into each byte of that bank and checks it.

Section 2: Worst Case Noise Tests
These tests apply maximum stress to the various types of PDP-11 MOS memories.

Test 6 and 7 allow the operator to select a single word data pattern (SA=204) and scope on either the writing (DATO) in test 6 or the reading (DATI) in Test 7 of that data.

Location: .CONST:0 should be changed if a different single word data pattern is considered.

Test 10 writes and then checks a series of single word patterns designed to stress parity memory.

Test 11 writes all memory with 1's in every bit and then "ripples" a "0" through it.

Test 12 writes all memory with 0's in every bit and then "ripples" a "1" through it.

Test 13 writes wrong parity in each byte of memory and checks that the parity detection logic works. This test is skipped for non-parity memory.

Test 14 writes "random" program code through memory and checks it.

Section 3: Instruction Execution Tests
This group of tests places instructions in the memory under test, then executes the instructions, and finally, checks that they are executed correctly.

Test 15 executes an instruction which does a DATI and a DATO on the memory under test.

Test 16 executes an instruction which does a DATI and a DATOB on the low byte of memory under test.

Test 17 executes an instruction which does a DATI and a DATOB on the high byte.

Test 20 executes an instruction which does a DATIO and a DATO.

Test 21 executes an instruction which does a DATIO and a DATOB on the low byte.

Test 22 executes an instruction which does a DATIO and a DATOB on the high byte.

Section 4: MOS Tests

Test 23 writes a pattern of 000377 through memory, then complements it addressing downward, complements the new pattern addressing upward, complements the third pattern addressing upward and finally complements this new AB patterns addressing downward.

Tests 24 and 25 write a checkerboard through memory, stall for 2 seconds, and then verify that no data has changed.

6.3.2.14 Toggle-In-Program 1 – The following is a Toggle-In-Memory Address Test. This test is useful when an address selection failure is suspected involving the first 16 kilobytes of memory. This program writes the value of each address into itself starting with the lower limit (200) and continuing to the upper limit. After all addresses have been written, each address is checked for the correct contents, starting with the upper limit and continuing to the lower limit.

	Location	Contents	Mnemonic	Comment
	10	012700	MOV #200,R0	;GET FIRST ADDRESS
	12	000200		;TO TEST ;(EXAMPLE START ADDRESS)
	14	010001	MOV R0,R1	;SAVE IN R1
	16	020037	1$: CMP R0,@#SWR	;CHECK UPPER LIMIT
	20	000176		;(IN SOFTWARE SWITCH REGISTER)
	22	001403	BEQ 2$	;BRANCH IF AT UPPER LIMIT
	24	010010	MOV R0,(R0)	;LOAD VALUE INTO ADDRESS
	26	005720	TST (R0)+	;STEP TO NEXT ADDRESS
	30	000772	BR 1$	;LOOP UNTIL DONE
	32	010004	2$: MOV R0,R4	;SAVE UPPER LIMIT
	34	020001	3$: CMP R0, R1	;CHECK IF AT LOWER LIMIT
*	36	001767	BEQ 1$	;BRANCH IF DONE
	40	024000	CMP –(R0),R0	;CHECK DATA WRITTEN
	42	001774	BEQ 3$	;BRANCH IF OK
	44	000000	HALT	;ERROR
	46	000772	BR 3$	;LOOP BACK

6.3.2.15 Toggle-In-Program 2 – The following is also a Toggle-In-Program and is used with Toggle-In-Program 1 for more complete address testing. This program writes the complement value of each address into itself starting with the upper limit and continuing to the lower limit. After all addresses have been written, each address is checked for the correct contents, starting with the lower limit address and continuing to the upper limit. Toggle in the following patches to the program above.

This is the patch to Toggle-In-Program 1.

Location	Contents	Mnemonic	Comment
36	001404	BEQ 4$	;BRANCH TO PROGRAM #2

These are the additions to Toggle-In-Program 1.

Location	Contents	Mnemonic	Comment
50	010402	4$: MOV R4,R2	;GET UPPER LIMIT
52	005142	5$: COM –(R2)	;COMPLEMENT ADDRESS
54	020201	CMP R2,R1	;CHECK IF AT LOWER LIMIT
56	001375	BNE 5$	;LOOP UNTIL DONE
60	020204	6$: CMP R2,R4	;CHECK IF AT UPPER LIMIT
62	001755	BEQ 1$	;GO TO PROGRAM 1 IF DONE
64	010203	MOV R2,R3	;GET VALUE OF ADDRESS
66	005103	COM R3	;COMPLEMENT VALUE
70	020322	CMP R3,(R2)+	;CHECK ADDRESS
72	001772	BEQ 6$	;BRANCH IF OK
74	000000	HALT	;ERROR
76	000770	BR 6$	;GO CHECK NEXT ADDRESS

6.4 DIGITAL'S SERVICES

Maintenance can be performed by the user or by Digital. Digital's maintenance and on-site services are described in Chapter 1 of the *Microcomputer Processor Handbook* (EB-18451-20).

6.4.1 Digital Repair Service

Digital Field Service offers a range of flexible service plans.

ON SITE SERVICE offers the convenience of service at your site and insurance against unplanned repair bills. For a small monthly fee you receive personal service from our Service Specialist. Within a few hours the specialist is dispatched to your site with equipment and parts to give you fast and dependable maintenance.

BASIC SERVICE offers full coverage from 8 a.m. to 5 p.m., Monday through Friday. Options are available to extend your coverage to 12-, 16-, or 24-hour days, and to Saturdays, Sundays, and holidays.

DECservice offers a premium on-site service that guarantees extra-fast response and nonstop remedial maintenance. We don't leave until the problem is solved, which makes this service contract ideal for those who need uninterrupted operations.

Under Basic Service and DECservice all parts, materials, and labor are covered in full.

CARRY-IN SERVICE offers fast, personalized response, and the ability to plan your maintenance costs for a smaller monthly fee than On-Site Service. When you bring your unit to one of 160 Digital Servicenters worldwide, factory-trained personnel repair your unit within two days (usually 24 hours). This service is available on selected terminals and systems. Contact your local Digital Field Service Office to see if this service is available for your unit.

Digital Servicenters are open during normal business hours, Monday through Friday.

DECmailer offers expert repair at a per use charge. This service is for users who have the technical resources to troubleshoot, identify, and isolate the module causing the problem. Mail the faulty module to our Customer Returns Center where the module is repaired and mailed back to you within five days.

PER CALL SERVICE offers a maintenance program on a noncontractual, time-and-materials-cost basis. This service is available with either On-Site or Carry-In service. It is appropriate for customers who have the expertise to perform first-line maintenance, but may occasionally need in-depth support from Field Service.

Per Call Service is also offered as a supplementary program for Basic Service customers who need maintenance beyond their contracted coverage hours. There is no materials charge in this case.

On-Site Per Call Service is provided on a best effort basis, with a normal response time of two to three days. It is available 24 hours a day, seven days a week.

Carry-In Per Call Service is available during normal business hours, with a two to three day turnaround.

For more information on these Digital service plans, prices, and special rates for volume customers, call one of the following numbers for the location of the Digital Field Service office nearest you.

Digital International Field Service Information Numbers

U.S.A.	1-(800)-554-3333	Denmark	430-1005
Canada	(800)-267-5251	Spain	91-7334370
United Kingdom	(0256)-57122	Finland	90-423332
Belgium	(02)-242-6790	Holland	(01820)-34144
West Germany	(089)-9591-6644	Switzerland	01-8105184
Italy	(02)-617-5381/2	Sweden	08-987350
Japan	(03)-989-7161	Norway	2-256422
France	1-6873152		

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