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MS11-E–J MOS memory user's manual

digital

EK-MS11E-OP-001

MS11-E–J MOS memory
user's manual

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CHAPTER 1
INTRODUCTION

The MS11-E – MS11-J (referred to herein as MS11) memories comprise a group of MOS semi-conductor, random-access memories that are designed to be used with the PDP-11 Unibus. Each memory assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The group provides storage for 16- or 18-bit data words (two parity bits are included in the 18-bit word), with capacity ranging from 4096 (4K) words to 16,384 (16K) words in 4K blocks. An MS11 memory can be assigned adjacent 4K blocks of addresses anywhere within the 124K Unibus address space. A special feature of the 16K MS11 allows the assignment of part of the I/O page to memory, although this can be done only for processors without memory management. Table 1-1 lists the significant specifications of an MS11 system.

The logic components of an MS11 memory are mounted on a single hex printed circuit board; the module has DEC designation M7847. The storage elements are 4096 × 1-bit, N-channel, MOS memory devices. A row of 18 of these devices is mounted on a module for each 4K block of addresses that is assigned to the memory; e.g., a 16K memory has 4 rows of 18 devices, an 8K memory has but 2 rows of devices. Table 1-2 lists the available MS11 options and the respective bit and word capacities.

The use of MOS memory circuits provides advantages (both economical and operational) not available with core memory systems. The cost-per-bit for MOS memories is low and, unlike core memory, this cost remains approximately constant with size.

Unlike core, MOS memory provides non-destructive readouts; consequently, the write-after-read cycle time associated with core memory is eliminated. Furthermore, with dynamic MOS devices such as those used in the MS11, power consumption is much lower than with core memory. The disadvantage of MOS storage volatility (i.e., data is not retained when power is lost) is compensated for by the availability of battery-supported power supplies that enable data retention for as long as several hours. The MS11 is designed for a special low-power mode to maximize the effectiveness of battery-powered operation.

Because the data storage element is a capacitor in the MOS storage device, all memory locations in the MOS memory must be periodically refreshed so that the data remains valid. The controller on the memory module includes the logic and timing circuits to carry out the periodic refreshing operation.

Table 1-1
Significant System Specifications

Characteristic	Specification	
Storage Capacity	4096 (4K) to 16,384 (16K) words, in 4K blocks	
Data Word Length	16 data bits, 2 parity bits	
Maximum Access Time (ns)		
Normal Operation	550	
Refresh Conflict*	1250	
Maximum Cycle Time (ns)		
Normal Operation	700	
Refresh Conflict*	1400	
Refresh Cycle Rate	One cycle every 25 μs (typical); maximum of one cycle every 22.5 μs	
Maximum Power Consumption (watts)	Idle	700 ns Cycle
MS11-E	12.3	23.5
MS11-F	13.0	24.3
MS11-H	13.8	25.0
MS11-J	14.5	25.8
Maximum Current Drain (mA)	Idle	700 ns Cycle
MS11-E		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	50	800
-15 Vdc	100	100
MS11-F		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	100	850
-15 Vdc	100	100
MS11-H		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	150	900
-15 Vdc	100	100
MS11-J		
+5 Vdc	1500	1500
BB+5 Vdc	500	500
+15 Vdc	200	950
-15 Vdc	100	100

*A characteristic of dynamic MOS memory devices is that they must be cycled periodically to ensure data validity. These cycles are known as refresh cycles and the controller on these memory modules has all the logic and timing circuits necessary to ensure that these cycles are performed. Should a processor or NPR request (MSYN) come during a refresh cycle, it is held up until the refresh cycle is completed and then processed. The Refresh Conflict time is the maximum amount of time that a normal cycle may be held up by a refresh cycle. The amount of time lost to bus masters because of refresh is dependent on the bus activity. For a system that uses the bus at a maximum rate (700 ns cycles) the loss of memory availability is less than 3 percent. For a system with an average bus cycle every 1.4 μs, the loss of availability is typically less than 3/4 percent.

Table 1-2
MS11 Options

Option Designation	Word Bit Length	Data Word Capacity
MS11-E	16	4K
MS11-EP	18	4K
MS11-F	16	8K
MS11-FP	18	8K
MS11-H	16	12K
MS11-HP	18	12K
MS11-J	16	16K
MS11-JP	18	16K

NOTE
18-bit words include two parity bits; an M7850 Parity Control module must be used with the parity options.

CHAPTER 2
INSTALLATION

2.1 GENERAL

Installation of the MS11 is relatively simple. First, the user should verify that factory-installed jumper wires relating to the number of memory chip banks are in place. Next, certain switches must be arranged to assign Unibus address space to the MS11. The backplane should then be checked to ensure that the required dc voltages are available. Finally, the module is inserted into the backplane and a diagnostic check is carried out to assure correct operation. These procedures are discussed more fully in following paragraphs.

Figure 2-1 shows the MS11 module (an 8K memory is illustrated). The array of chips is located in the upper-right quarter of the board. At the left-center of the board are eyelets W1 – W6, into which appropriate jumpers are inserted. To the lower-right of the eyelets is the DIP switch (E111) which is configured according to the MS11 address assignment. E111 has eight individual contacts that may be identified by numbers or letters on the switch; however, the contacts are identified by etched letters A – J on the printed circuit board (this notation is followed throughout the text and in the logic drawings).

2.2 JUMPER VERIFICATION

The MS11 Memory is shipped with factory installed jumpers appropriate for the memory size. The user should check the module to ensure that the correct jumpers are in place. Table 2-1 lists the memories by size and indicates the jumpers that are installed for each. A 16K memory will normally operate with switch H closed, in addition to the installed jumpers; however, a 16K memory installed in a 32K PDP-11 requires special consideration.*

2.3 SWITCH ARRANGEMENT

The MS11 Memory is assigned Unibus address space by the arrangement of switches A – E. *The switches must be arranged by the user before the memory is installed.**

2.4 VOLTAGE CHECK

Before the module is inserted in the backplane, check the backplane to ensure that the required dc voltages are present and within tolerance. The dc voltages are listed in Table 2-2; Table 2-3 lists the MS11 pin-outs.

All four dc voltages must be supplied for system operation. If data retention is desired when the ac power is removed, the +5 Vdc supply can be powered down and the other supplies maintained.

Table 2-1
Module Jumper Installation

Memory Designation	Memory Size	Eyelet Pairs Connected by Jumpers		
		W3-W4	W1-W2	W5-W6
MS11-E/EP	4K	X		
MS11-F/FP	8K	X	X	
MS11-H/HP	12K	X	X	X
MS11-J/JP	16K	X	X	X

Table 2-2
MS11 DC Voltage Tolerances

DC Voltage	Minimum	Maximum
+5	4.75	5.25
+15	14.50	16.50
-15	-16.50	-13.50
BB+5	4.75	5.25

*Refer to Paragraph 4.2 of MS11-E-J MOS Memory Maintenance Manual (EK-MS11E-MM-001).

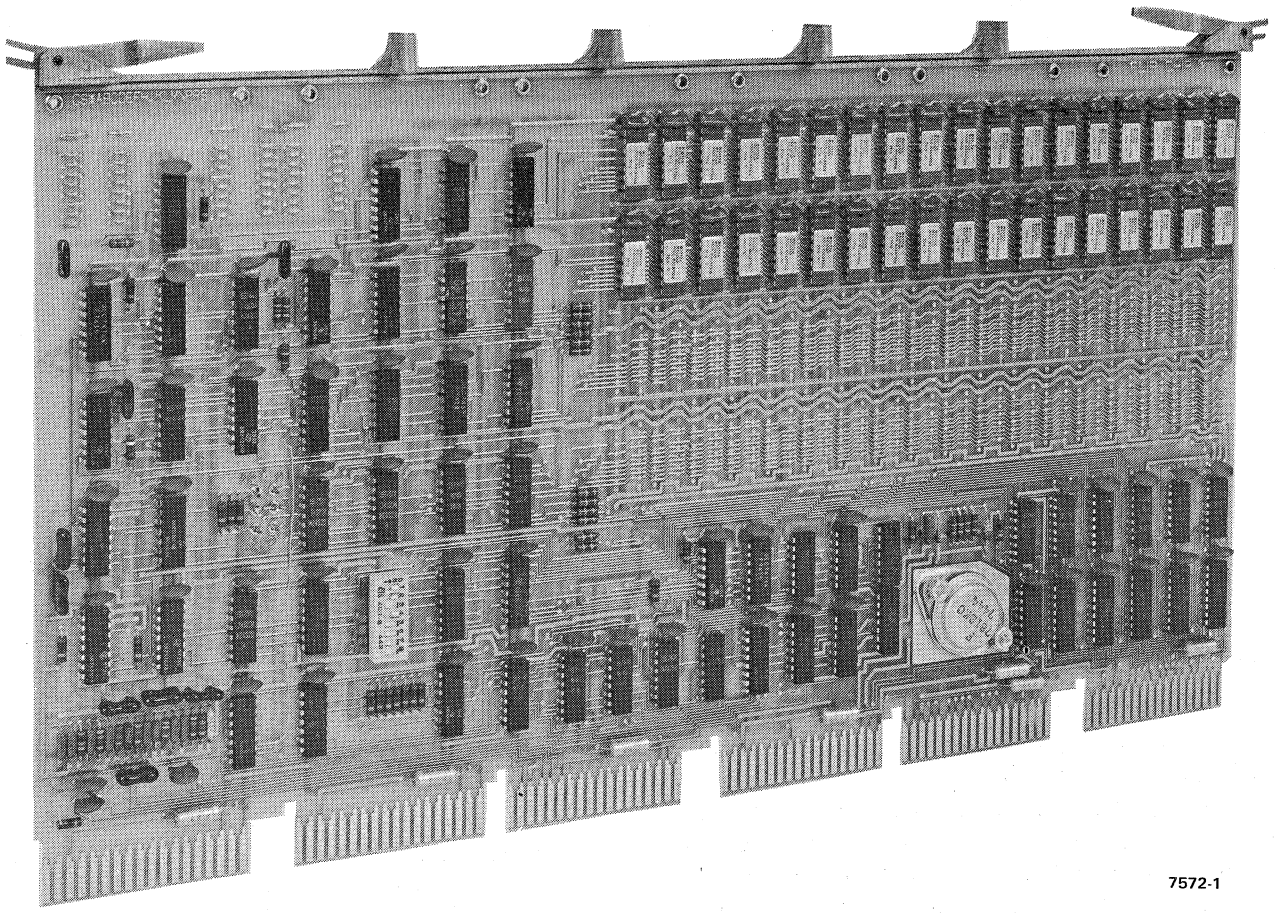

Figure 2-1 MS11-F Module

Table 2-3
MS11 Memory Pinouts

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A		+5		+5	*]	+5	TP	+5		+5		+5
B		TP		TP	]		TP					
C	D00	GND		GND		GND		GND		GND		GND
D	D02	D01	BB+5									
E	D04	D03	INT SSYN	PAR DET	TP							
F	D06	D05		DC LO	TP							
H	D08	D07	A01	A00								
J	D10	D09	A03	A02								
K	D12	D11	A05	A04	TP			*]				
L	D14	D13	A07	A06				]				
M		D15	A09	A08	TP			*]				
N	P1		A11	A10				]				
P	P0		A13	A12			TP	*]				
R	+15		A15	A14			TP	]				
S	-15		A17	A16			TP	*]				
T	GND		GND	C1	GND		GND	]	GND		GND	
U			SSYN	C0			TP					
V			MSYN									

*Points marked by] are tied together to provide grant continuity on backplane.

2.5 BACKPLANE INSTALLATION

When the dc voltages have been verified, insert the MS11 into the Unibus backplane. Presently, three backplanes can be used with the MS11, although other backplanes may become available; these three are DD11-C, DD11-D, and DD11-P. The DD11-C is a 4-slot backplane; the MS11 can be inserted into slot 2 or slot 3. The DD11-D is a 9-slot backplane; slots 2 – 8 can be used for the MS11. The DD11-P is another 9-slot backplane, which is used with the PDP-11/04 or PDP-11/34. If an M7850 Parity Control module is to be used with the MS11, it must be installed in the same backplane; the M7850 can occupy any of the backplane slots that are available to the MS11.

2.6 DIAGNOSTIC CHECK

When the memory is connected to the Unibus, run the MS11 diagnostic program to verify that the memory is operable. If a problem arises, follow the instructions in the diagnostic.

APPENDIX A
MS11 SWITCH SETTINGS

Table A-1 first lists the 31 addresses that can be assigned as the starting address on the MS11 module. Listed next is the number of Unibus addresses below the MS11 starting address; e.g., there are 8096 (8K) Unibus addresses below starting address 040000_8. Finally, the third column lists the switch settings that will produce the desired address assignment. The MS11 ending address is automatically determined by the starting address and the memory size. Table A-2 shows how switches H, J, and F must be arranged for normal operation and when I/O page space is assigned to the MS11.

Table A-1
Switch Settings for MS11 Starting Addresses

MS11 Starting Address (Octal)	Unibus Addresses Below Starting Address	Switch Selection (Switch OFF = Logic 1)				
		A	B	C	D	E
000000	0K	1	1	1	0	0
020000	4K	1	1	0	1	1
040000	8K	1	1	0	1	0
060000	12K	1	1	0	0	1
100000	16K	1	1	0	0	0
120000	20K	1	0	1	1	1
140000	24K	1	0	1	1	0
160000	28K	1	0	1	0	1
200000	32K	1	0	1	0	0
220000	36K	1	0	0	1	1
240000	40K	1	0	0	1	0
260000	44K	1	0	0	0	1
300000	48K	1	0	0	0	0
320000	52K	0	1	1	1	1
340000	56K	0	1	1	1	0
360000	60K	0	1	1	0	1
400000	64K	0	1	1	0	0
420000	68K	0	1	0	1	1
440000	72K	0	1	0	1	0
460000	76K	0	1	0	0	1
500000	80K	0	1	0	0	0
520000	84K	0	0	1	1	1
540000	88K	0	0	1	1	0
560000	92K	0	0	1	0	1
600000	96K	0	0	1	0	0
620000	100K	0	0	0	1	1
640000	104K	0	0	0	1	0
660000	108K	0	0	0	0	1
700000	112K	0	0	0	0	0
720000	116K	1	1	1	1	1
740000	120K	1	1	1	1	0

NOTE
Switch contacts are open when switch is in OFF position

Table A-2
Switch Settings for I/O Page Operation
Memory Size Determination

Memory Option	Switch		
	F	H	J
MS11-E/EP, MS11-F/FP, MS11-H/HP	OFF	OFF	OFF
MS11-J/JP, Normal Use	OFF	ON	OFF
MS11-J/JP, Lower 2K of I/O page assigned to memory*	OFF	OFF	ON
MS11-J/JP, Lower 3K of I/O page assigned to memory*	ON	OFF	ON

*Set switches A through E for a starting address of 100000_8.

NOTE
Switch contacts are open when switch is in OFF position.

MS11-E–J MOS MEMORY
USER'S MANUAL
EK-MS11E-OP-001

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