EK-LSIFS-SV-005

# LSI-11 Systems Service Manual

## Volume III

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# LAV11 PRINTER INTERFACE

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 0.5 | 0 | 1.8 | 1.0 | BC11S (for LA180)<br>7009087 (for Centronics line printer™ models 101, 101A, 101D, 102A, and 303) |

## Standard Addresses

LACS 177514
LADB 177516

## Vectors

200

## Diagnostic Program

Refer to Appendix A.

## Related Documentation

*LAV11 User's Manual* (EK-LAV11-OP-001)
Field Maintenance Print Set (MP00306)
*LA180 DECprinter I Maintenance Manual* (EK-LA180-MM)
Microcomputer Interfaces Handbook (EB-20175-20)

## CAUTIONS

1. Switching – Switching the LA180 off-line while the operating system is running a program may result in the computer hanging and crashing the program. If this occurs, type P to continue. This problem does not occur if the LPV11 is used in place of the LAV11.

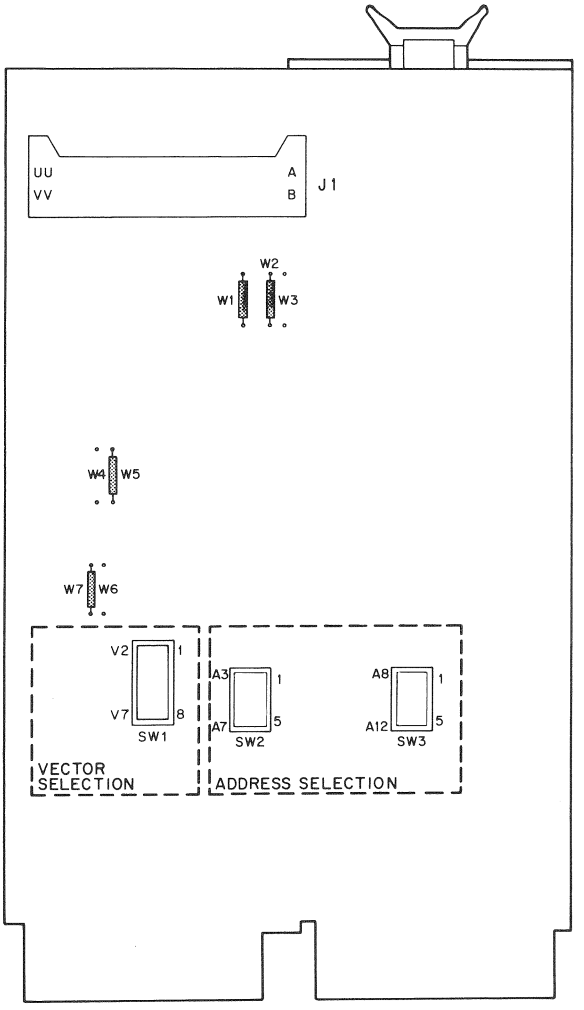
2. LA180 to LAV11 Cable – The only acceptable cable for use between the LA180 and the LAV11 is the BC11S. The end labeled P2 must attach to the LA180. The end labeled P1 must be attached to the LAV11.

3. LA180 Modifications – On the LA180 logic board (54-11023), jumper W6 must be inserted. This ensures +5 Vdc sense will read the LAV11. Failure to do so will result in a continued error condition in the LAV11 LACS buffer. W6 is located between J2 and J3 on the 54-11023 module.

4. Miscellaneous Jumpers – For an LA180, the following jumper configuration must be maintained.

| Jumper | Condition | Function if Inserted |
|---|---|---|
| W1 | I | Transmit parity on line |
| W2 | I | +5 Vdc sense from LA180 |
| W3 | R | +5 Vdc sense from LAV11 |
| W4 | R | DEMAND is asserted low |
| W5 | I | DEMAND is asserted high |
| W6 | R | P STROBE is asserted low |
| W7 | I | P STROBE is asserted high |

5. The field replacement for the LAV11 (M7949) is the LPV11 (M8027).




STANDARD CONFIGURATION

| | | |
|---|---|---|
| ADDRESS | | |
| SW3 | 1 | OFF |
| | 2 | OFF |
| | 3 | OFF |
| | 4 | OFF |
| | 5 | OFF |
| SW2 | 1 | OFF |
| | 2 | ON |
| | 3 | ON |
| | 4 | OFF |
| | 5 | ON |
| VECTOR | | |
| SW1 | 1 | ON |
| | 2 | ON |
| | 3 | ON |
| | 4 | ON |
| | 5 | ON |
| | 6 | OFF |
| | 7 | ON |
| | 8 | N.A. |

STANDARD ADDRESS = 17751X

VECTOR = 200

| JUMPER | LA180 | CENTRONICS |
|---|---|---|
| W1 | I | I |
| W2 | I | R |
| W3 | R | I |
| W4 | R | R |
| W5 | I | I |
| W6 | R | R |
| W7 | I | I |

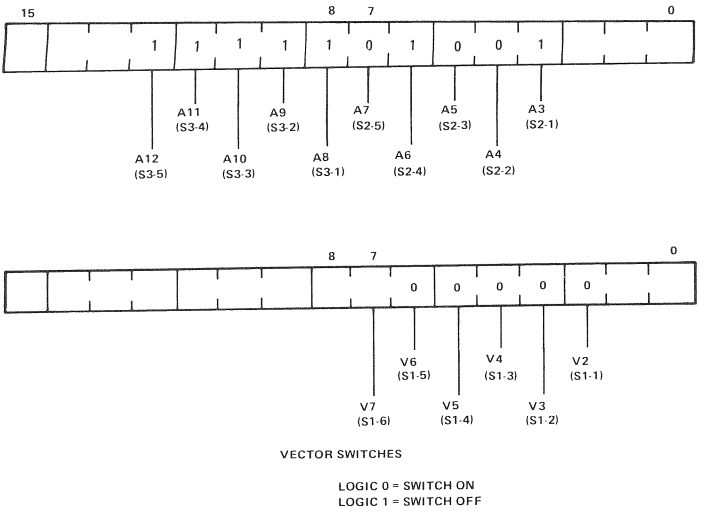
KEY:

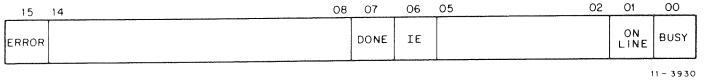
I = INSERT

R = REMOVE

11-4146

LAV11 Jumpers



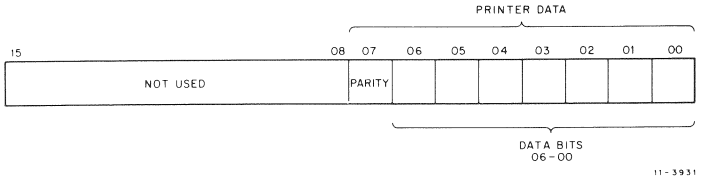

LAV11 Control/Status Register (LACS)

**LACS Bit Definitions**

| Bit | Function |
|---|---|
| 15 | Error - The error bit is asserted (1) when an error condition (i.e., torn or no paper) exists in the line printer. This is a read-only bit, which is reset only by manual correction of the error condition. |
| 14-08 | Unused. |
| 07 | Done - The done bit is asserted (1) when the printer is ready to accept another character. This is a read-only bit set by INIT. The done bit is cleared by loading the LADB register. An interrupt sequence is started if IE (interrupt enable, bit 06) is also set. |

**LACS Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 06 | IE - The interrupt enable bit is set or cleared (read or write bit) under program control. It is cleared by the INIT (initialize) signal on the LSI-11 bus.<br><br>(INIT is caused by programmed RESET instruction, console start function, or a power-up or power-down condition.) When IE is set, an interrupt sequence is started if either error or done is also set. |
| 05-02 | Unused. |
| 01 | On Line - The on line bit is asserted (1) when the LA180 printer (only) is on-line. Read only. |
| 00 | Busy - The busy bit is asserted (1) when the LA180 printer (only) is performing a print or paper advance operation. |




LAV11 Data Buffer Register (LADB)

**LADB Bit Definitions**

| Bit | Function |
|---|---|
| 15-08 | Unused. |
| 07 | Parity - The parity bit is loaded with the data word if the parity jumper is installed. Write only. |
| 06-00 | Data - The data comprises seven bits, with bit 06 being the most significant. This buffered 7-bit character will be transferred to the printer. These are all write-only bits. |

# LPV11 LP05/LA180 INTERFACE MODULE

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 0.8 | 0 | 1.4 | 1 | BC11S-25 for LA180<br>70-11212-25 for LP05 |

### Standard Addresses

| | |
|---|---|
| LPCS | 177514 |
| LPDB | 177516 |

### Standard Vector

Done or error interrupt 200

### Diagnostic Programs

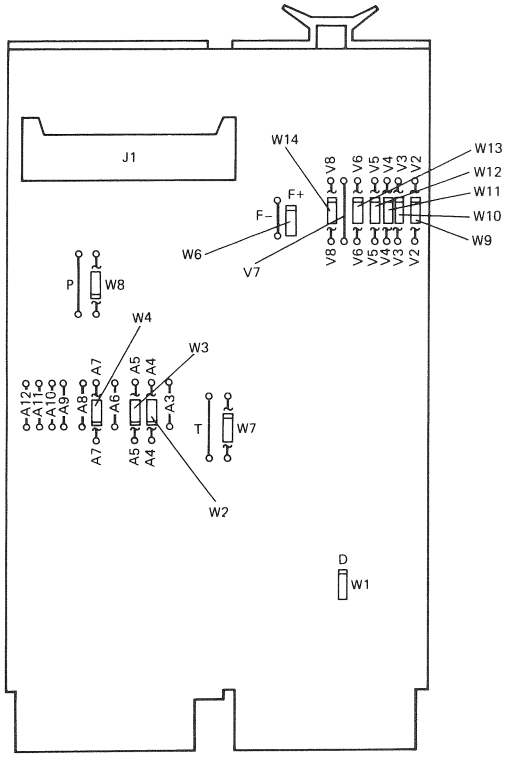
Refer to Appendix A.

### Related Documentation

*LP25 Line Printer Maintenance Guide* (ER-OLP25-5V)
*LPV11 Printer User's Manual* (EK-LPV11-OP)
*LA180 DECprinter I User's Manual* (EK-LA180-OP)
LA180 Field Maintenance Print Set (MP-LA180-00)
*LA180 DECprinter I Maintenance Manual* (EK-LA180-MM)
*LP05 Technical Manual, Model 2230 Line Printer* (Dataproducts Corporation)
LPV11-V Field Maintenance Print Set (MP00467)
*Microcomputer Interfaces Handbook* (EB-20175-20)

**NOTE**

**The LPV11 (M8027) is a direct replacement for the LAV11 (M7949).**



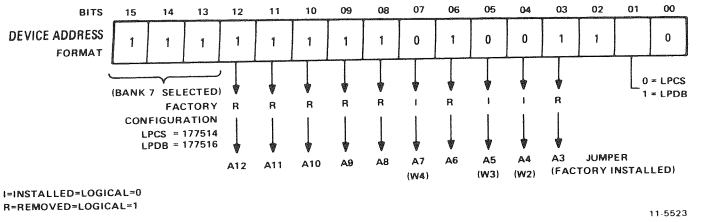

NOTE:

=JUMPERS BROKEN FOR CLARITY ON THIS FIGURE. THESE WIRE-WRAP JUMPERS WOULD NORMALLY BE USED TO REPLACE PREVIOUSLY REMOVED FACTORY INSTALLED (W) JUMPERS (SHOWN INSTALLED).

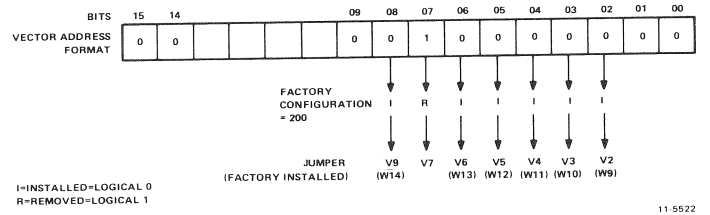
o =WIRE WRAP PIN.

MR-0863

LPV11 Jumpers




LPV11 Interrupt Device Address Format and Jumpers




LPV11 Vector Address Format and Jumpers

**LPV11 Jumper Definitions**

| Jumper Designation | Configuration When Shipped | Function |
|---|---|---|
| A12 | R | Jumper wires W2, W3, and W4 are factory installed to negate address bits 4, 5, and 7, respectively. |
| A11 | R | |
| A10 | R | |
| A9 | R | |
| A8 | R | This sets 177514 as the base address. |
| A7 | I | |
| A6 | R | |
| A5 | I | |
| A4 | I | |
| A3 | R | |
| V8 | I | Jumper wires W9 through W14 are factory installed to negate vector bits 2, 3, 4, 5, 6, and 8. |
| V7 | R | |
| V6 | I | |
| V5 | I | |
| V4 | I | This sets 200 as the interrupt vector. |
| V3 | I | |
| V2 | I | |

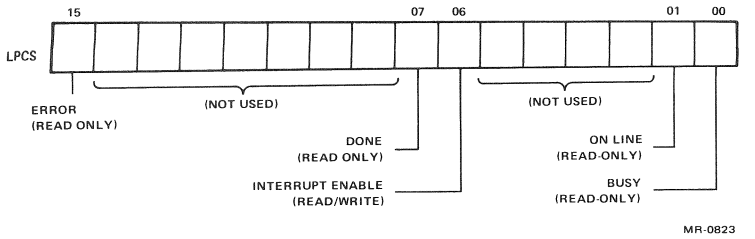
**LPV11 Jumper Definitions (Cont)**

| Jumper Designation | Configuration When Shipped | Function |
|---|---|---|
| D | I | W1 installed to delay BRPLY L. |
| T<br>W7 | R<br>I | Supports both uppercase and lowercase printing. For uppercase only, remove W7 and install T.<br><br>Do not configure the module with both jumpers W7 and T installed. |
| P<br>W8 | R<br>I | Configured to transmit parity (bit 07) to printer.<br><br>**Parity Option / Jumper W8 / Jumper P**<br>Normal parity bit — Installed — Removed<br>No parity, bit 07 low — Removed — Removed<br>No parity, bit 07 high — Removed — Installed<br><br>Do not configure the module with both jumpers W8 and P installed. |

**NOTE**

**If the LPV11 interface module is used with an LP05 printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W8. The LP05 interface module does not support the DAVFU Function.**

| | | |
|---|---|---|
| F−<br>F+ | R<br>O | W6 is installed at F+ to enable error filter operation with the LP05.<br><br>For operation without the error filter, remove W6 and install a jumper at F−.<br><br>Do not configure the module with jumpers installed at both F+ and F−.<br><br>The LA180 automatically enables the error filter circuit regardless of the jumper configuration. |



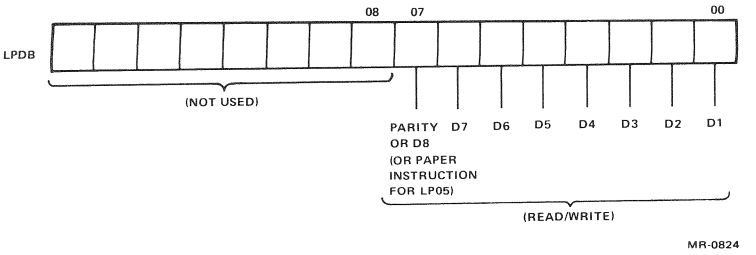

LPV11 Control/Status Register (LPCS)

**LPCS Register Bit Functions**

| Bit | Function |
|---|---|
| 15 | Error - Asserted (1) whenever an error condition exists in the line printer. Error conditions include the following.<br><br>LP05 errors:<br><br>• Power off<br>• No paper<br>• Printer drum gate open<br>• Over-temperature alarm<br>• PRINT INHIBIT switch off<br>• Printer off-line<br>• Torn paper<br><br>LA180 errors:<br><br>• Fault (paper fault)<br>• ON-LINE switch (in OFF position)<br><br>Reset by manual correction of error condition if LPCS bit 06 is not set. If bit 06 is set, bit 15 is reset by manual correction of the error and (1) reading the interrupt vector if the interface is "ready," or (2) after reading the LPCS if the interface is "not ready." Read only. |
| 14-08 | Not used. Read as 0s. |

**LPCS Register Bit Functions (Cont)**

| Bit | Function |
|---|---|
| 07 | Done LP05 - Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit is set by the LSI-11 processor asserting BINIT L; if bit 06 is also set, an interrupt sequence is initiated. Also set by the printer when on-line and ready to accept a character. Cleared by loading (writing into) the LPDB register. Inhibited when bit 15 is set. Read only.<br><br>LA180 - Asserted (1) when the printer is ready to accept another character. Done is set by the LSI-11 processor asserting BINIT L and is cleared by loading (output transfer to) the LPDB register. If the interrupt enable bit is set, setting done will initiate an interrupt request. |
| 06 | Interrupt Enable - Set or cleared by the program. Also cleared by the LSI-11 processor asserting BINIT L. When set, an interrupt sequence is initiated if either the error or done bit is set. |
| 05-02 | Not used. Read as 0s. |
| 01 | On-Line - Not supported and not required by DEC software. |
| 00 | Busy - Not supported and not required by DEC software. The following information is for reference only.<br><br>LA180 - Set when the LA180 prints a line or advances paper.<br><br>LP05 - Not used. Read as 0. |




LPV11 Data Buffer Register (LPDB)

**LPDB Register Bit Functions**

| Bit | Function |
|---|---|
| 15-08 | Not used. Read as 0s. Data written into these bits is lost. |
| 07 | Parity or D8 - Optional use. Read as 0.<br><br>LA180 - Optional parity bit.<br><br>LP05 - Optional paper instruction bit. Not supported by the LPV11 (read as 0). |
| 06-00 | Data - Seven-bit ASCII character register. Characters are sequentially output to the printer buffer via this register. Read as all 0s. |

# LSI-11/2 PROCESSOR MODULE DESIGNATIONS

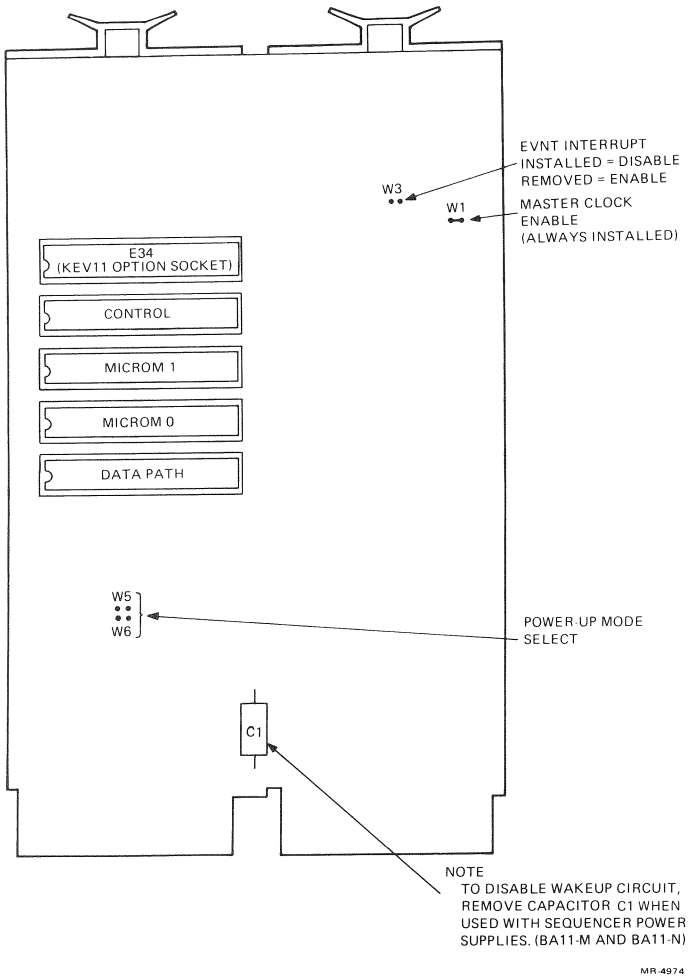
| | | |
|---|---|---|
| KD11-HA | Dual-height LSI-11 processor without memory | |
| KD11-HB | KD11-HA + MSV11-DB 8K word memory | |
| KD11-HC | KD11-HA + MSV11-DC 16K word memory | |
| KD11-HD | KD11-HA + MSV11-DD 32K word memory | |
| KD11-HF | KD11-HA + MSV11-DA 4K word memory | |
| KD11-HJ | KD11-HA + MMV11-A 4K word core memory | |
| KD11-HU | KD11-HA + MRV11-BA | |
| KD11-XA | KD11-HA, 2 MSV11-ED 64K word memory | (Heathkit) |
| KD11-XB | KD11-HA, 4 MSV11-ED 128K word memory | (Heathkit) |
| KD11-XC | KD11-HA, 9 MSV11-ED 288K word memory | (Heathkit) |
| KD11-XD | KD11-HA, 3 MSV11-DD | (Heathkit) |
| KD11-XH | KD11-HA, 3 MSV11-DC | (Heathkit) |
| KD11-XJ | KD11-HA, 3 MSV11-DB | (Heathkit) |

### M7270 Specifications

| | |
|---|---|
| Size: | Double-height module |
| Dimensions: | 13.34 cm (5.25 in) × 22.8 cm (8.9 in) |
| Power: | +5 Vdc ±5%, 1 A<br>+ 12 Vdc ± 5%, .22 A |
| Bus Loads: | AC - 1.7 unit loads<br>DC - 1 unit load |

### Related Documentation

*Microcomputer Processor Handbook* (EB-18451-20)
KD11-HA Print Set (MP-00495)
LSI-11 Maintenance Card (EK-LSI11-MC)




M7270 Jumpers and Socket Locations

**Jumper**

W1 Always installed - master clock enabled.

W3 Removed - external event interrupt (line clock) enabled.
Installed - external event interrupt disabled.

| W6 | W5 | Mode Selected |
|---|---|---|
| R* | R | PC at 24 and PS at 26, or halt mode (mode 0). |
| R | I | ODT microcode (mode 1). |
| I | R | PC at 173000 for user bootstrap (mode 2). |
| I | I | Special processor microcode; not implemented (mode 3). |

**Diagnostic Programs**
The following diagnostic programs are for use with LSI-11 processors except for the limitations noted.

VKAA?? LSI-11 basic instruction test.

VKAB?? LSI-11 Extended Instruction Set (EIS) test. This program can be run only on LSI-11 CPUs with the KEV11 (EIS/FIS) or KEV11-CA (DIBOL instruction set) options installed.

VKAC?? LSI-11 Floating Point Instruction (FIS) test. This runs only on LSI-11 CPUs that have the KEV11 (EIS/FIS) option (23-003B5).

VKAD?? LSI-11 traps test. This diagnostic auto-sizes for the EIS, FIS, and DIBOL options.

a. Older versions (Rev B1 and below) require the setting of a bit in the software switch register if EIS, FIS, or DIBOL is present.

b. Rev A diagnostics will not run on D322 or D324 systems because of the DIS instructions.

**NOTE**
**See Appendix A for XXDP+ multimedia assignments.**

VKAH?? Basic system exerciser. Tests serial line unit, memory, processor, EIS/FIS, clock, and both floppy disks under various conditions. Software switch register must be set for options.

*R = jumper removed; I = jumper installed.

| Chip | Vendor Number | DEC Number | $V_{BB}$ | Comments |
|---|---|---|---|---|
| DATA | CP 1611 B-39 | 21-11549-01 | −3.9 | |
| | | 21-15579-00 | −3.5 | With ECO 6 |
| CONTROL | CP 1621 B-173 | 23-002C4 | −3.9 | 2007 pattern |
| MICROM-0 | CP 1631 B-103 | 23-001B5 | −3.9 | |
| MICROM-1 | CP 1631 B-073 | 23-002B5 | −3.9 | |
| EIS/FIS (if present) KEV11-A | CP 1631 B-135 | 23-003B5 | −3.9 | |

**ECOs for Etch Rev E**

| CS Rev | ECO No. | Change |
|---|---|---|
| A | 1 | 1. Remove blanking pulse.<br>2. Generate clock driver $V_{cc}$ from +12 V.<br>3. Move K1 MSTB L from E34-3 to E34-4.<br>4. Relayout board. |
| B | 2 | Change C31 and C32 from 10-12312-01 to 10- 10279-0. |
| C | 3 | Change Augat socket to Burndy socket. |
| F | 3A | Allow customer to remove C81. |
| H | 4 | Change R18 from 13-10317 to 13-10522. |
| J | 5 | Alternate part 19-14282-01 may be used to replace E37. |
| K | 6 | Change part E30 from 21-11549-01 to 21-15579-00. |

# MCV11-D CMOS READ/WRITE MEMORY

## GENERAL

**MCV11-D Modules**

| Model | Memory Capacity | MOS Chips | Module | Number of Chips |
|---|---|---|---|---|
| MCV11-DA | 8K bytes | 2K × 8 | M8631-A | 4 |
| MCV11-DC | 32K bytes | 2K × 8 | M8631-C | 16 |

### Diagnostic Programs

Refer to Appendix A.

### Related Documentation

*MCV11-D User's Guide* (EK-MCV1D-UG)
MCV11-D Reference Card (EK-MCV1D-RC)
Field Maintenance Print Set (MP-DDM8631)

MCV11-D Power

| MCV11-DC (32K byte) | | | | |
|---|---|---|---|---|
| Current and Power | | Active Mode | Standby Mode | Data Retention Mode |
| Current | +5 V (Typ)* | 1.23 A | 1.22 A | 0 |
| | +5 V (Max)* | 2.16 A | 2.15 A | 0 |
| | +5 V BBU (Typ)† | 1 mA | 1 mA | 9 mA |
| | +5 V BBU (Max)† | 2 mA | 2 mA | 14 mA |
| Power | +5 V (Typ) | 6.20 W | 6.10 W | .045 W |
| | +5 V (Max) | 11.34 W | 11.29 W | .073 W |
| **MCV11-DA (8K byte)** | | | | |
| Current | +5 V (Typ)† | 1.20 A | 1.19 A | 0 |
| | +5 V (Max)* | 2.09 A | 2.08 A | 0 |
| | +5 V BBU (Typ)† | 1 mA | 1 mA | 9 mA |
| | +5 V BBU (Max)† | 2 mA | 2 mA | 14 mA |
| Power | +5 V Typ | 6.00 W | 5.95 W | .045 W |
| | +5 V Max | 10.97 W | 10.92 W | .073 W |

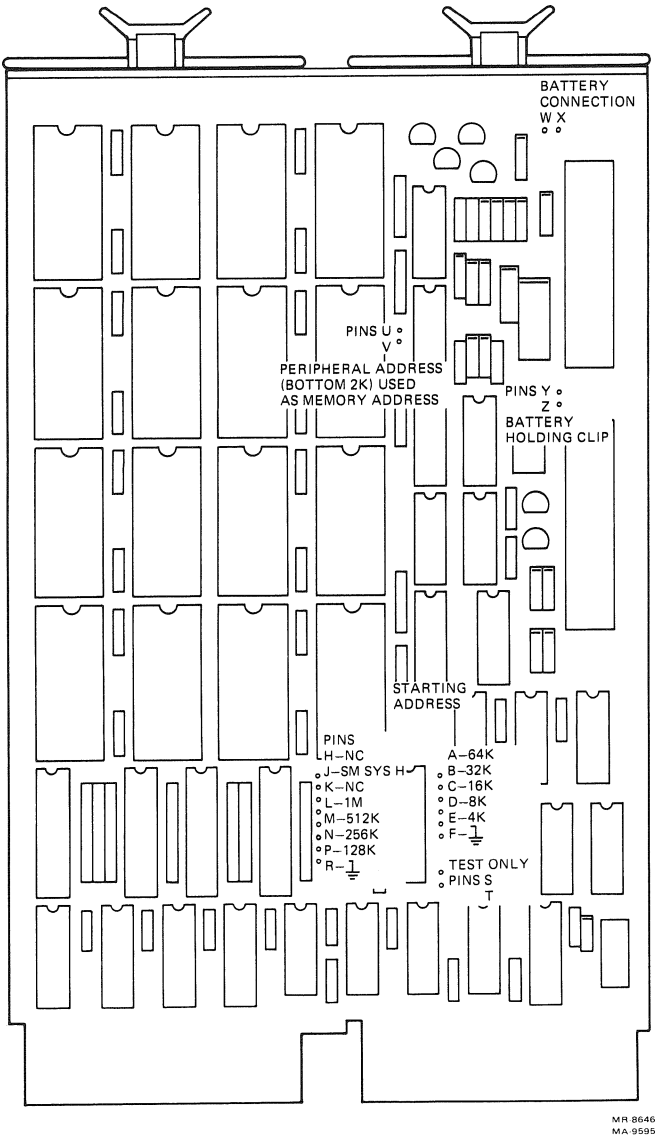
* The +5 V current is recorded with no +5 V BBU supply connected.

† The +5 V BBU current assumes +5 V = 4.75 V and +5 V BBU = 5.25 V. In the active and standby mode, a majority of current comes from the +5 V supply, so it appears as though very little current is required by the +5 V BBU supply. In the data retention mode, the +5 V supply is assumed to be at 0 V. The current supplied by +5 V BBU is used to trickle charge the batteries. If the batteries were disconnected, +5 V BBU would be typically 20 μA.

## CONFIGURING THE MCV11-D MEMORY MODULE

There are five groups of MCV11-D memory module jumpers.

1. Module starting address jumpers
2. System selection jumper
3. Manufacturing test jumper
4. Memory I/O page address jumper
5. Memory module battery backup jumper




MCV11-D Module Layout

**Module Starting Address (MSA) Jumpers**

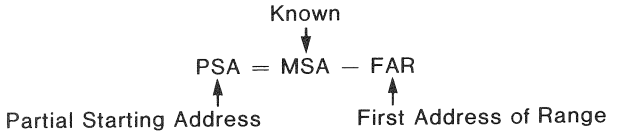
To configure the MSA jumpers, you need the module starting address. From the module starting address you can obtain the necessary data to configure the jumpers.

The first address of range (FAR) selects the first address of the 128K range the starting address falls in.

The partial starting address (PSA) selects which 4K boundary within a specific 128K range the starting address falls in.

You can find the memory module starting address (MSA) by determining how much memory the system has in decimal K words. This word value is the MSA.

To jumper the module starting address (MSA), proceed as follows.




**First Address of Range (FAR)**

| Decimal (K) | Octal | Jumpers In (X) to Ground (R) L | M | N | P |
|---|---|---|---|---|---|
| 000-124 | 00000000-00760000 | | | | |
| 128-252 | 01000000-01760000 | | | | X |
| 256-380 | 02000000-02760000 | | | X | |
| 384-508 | 03000000-03760000 | | | X | X |
| 512-636 | 04000000-04760000 | | X | | |
| 640-784 | 05000000-05760000 | | X | | X |
| 768-892 | 06000000-06760000 | | X | X | |
| 896-1020 | 07000000-07760000 | | X | X | X |
| 1024-1148 | 10000000-10760000 | X | | | |
| 1152-1276 | 11000000-11760000 | X | | | X |
| 1280-1404 | 12000000-12760000 | X | | X | |
| 1408-1532 | 13000000-13760000 | X | | X | X |
| 1536-1660 | 14000000-14760000 | X | X | | |
| 1664-1788 | 15000000-15760000 | X | X | | X |
| 1792-1916 | 16000000-16760000 | X | X | X | |
| 1920-2044 | 17000000-17760000 | X | X | X | X |

## Partial Starting Address (PSA)

| Decimal (K) | Octal | Jumpers in (X) To Ground (F) A | B | C | D | E |
|---|---|---|---|---|---|---|
| 0 | 00000000 | | | | | |
| 4 | 00020000 | | | | | X |
| 8 | 00040000 | | | | X | |
| 12 | 00060000 | | | | X | X |
| 16 | 00100000 | | | X | | |
| 20 | 00120000 | | | X | | X |
| 24 | 00140000 | | | X | X | |
| 28 | 00160000 | | | X | X | X |
| 32 | 00200000 | | X | | | |
| 36 | 00220000 | | X | | | X |
| 40 | 00240000 | | X | | X | |
| 44 | 00260000 | | X | | X | X |
| 48 | 00300000 | | X | X | | |
| 52 | 00320000 | | X | X | | X |
| 56 | 00340000 | | X | X | X | |
| 60 | 00360000 | | X | X | X | X |
| 64 | 00400000 | X | | | | |
| 68 | 00420000 | X | | | | X |
| 72 | 00440000 | X | | | X | |
| 76 | 00460000 | X | | | X | X |
| 80 | 00500000 | X | | X | | |
| 84 | 00520000 | X | | X | | X |
| 88 | 00540000 | X | | X | X | |
| 92 | 00560000 | X | | X | X | X |
| 96 | 00600000 | X | X | | | |
| 100 | 00620000 | X | X | | | X |
| 104 | 00640000 | X | X | | X | |
| 108 | 00660000 | X | X | | X | X |
| 112 | 00700000 | X | X | X | | |
| 116 | 00720000 | X | X | X | | |
| 120 | 00740000 | X | X | X | X | |
| 124 | 00760000 | X | X | X | X | X |

## Module Starting Address (Example – 352K Words)

| Names | First Address of Range (FAR) | | | | Partial Starting Address (PSA) | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Decimal k words Binary address | 1Meg | 512K | 256K | 128K | 64K | 32K | 16K | 8K | 4K |
| Values BDAL | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 |
| BDAL bits | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| Jumper pin names | L | M | N | P | A | B | C | D | E |
| Jumper pins | N to R | | | | A to B, B to F | | | | |

**System Selection Jumper**
Small/large system selection is set by the condition of jumper pin J. Small systems use 16- or 18-bit addressing, with pin J open. Large systems use 22-bit addressing, with pin J wrapped to pin R.

**Manufacturing Test Jumper**
This jumper, when installed (pin T to pin S), allows addresses to start at 128K. The jumper is installed during manufacturing test. When the modules leave manufacturing test, the jumper is removed.

**Memory I/O Page Address Jumper**
When a customer wants to use the bottom 2K of the I/O space as a memory address, jumper U to V.

**Memory Module Battery Backup Jumper**
When you receive an MCV11-D memory, there will be two 1.2 V rechargeable nicad batteries. Pins Y and Z are the clip carrier pins (no electronic function); they should have a clip across them. Remove the clip and connect it across pins W and X. This installs module battery backup.

# MRV11-AA READ-ONLY MEMORY

A PROM/ROM module will accept up to 16 customer-supplied erasable UVPROMs, fusible link PROMs, or masked ROM devices.

| Amps | | | Bus Loads | | Cables |
|---|---|---|---|---|---|
| | +5 | −12 | AC | DC | |
| W/O PROMs (0.6 max.) | 0.4 | 0 | 1.84 | 1.0 | none |
| With PROMs (4.1 max.) | 2.8 | 0 | | | |

### Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 addresses (0-1777).

### Vectors, Diagnostic Program, Exerciser Program

None

### Related Documentation

Field Maintenance Print Set (MP00066)
*Microcomputer Processor Handbook* (EB-18451-20)

### NOTES

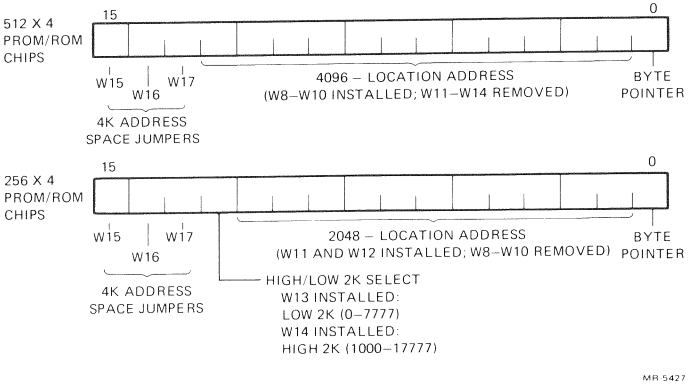
1. **Jumpers W8–W14 select chip set types (512 or 256).**
2. **Any row not populated with PROMs must have the BRPLY L jumper (W0–W7) removed.**

**MRV11-AA Address Word Formats**

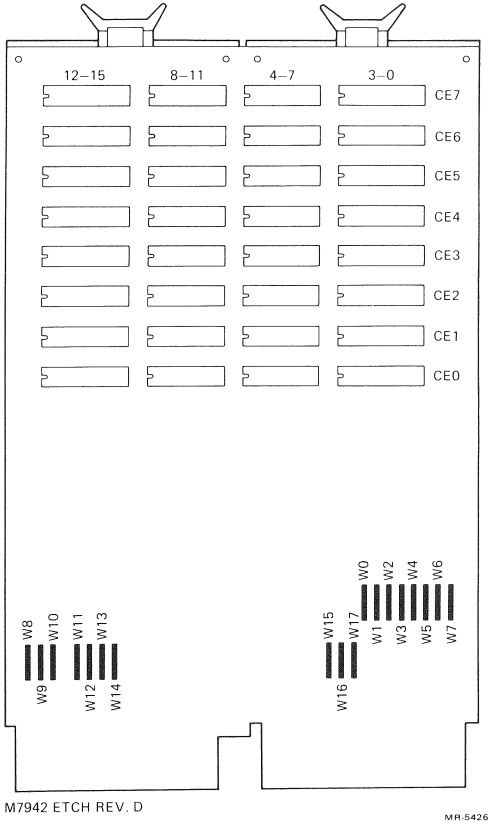
| Bank | Bank Select W15 | W16 | W17 |
|---|---|---|---|
| 0 | I | I | I |
| 1 | I | I | R |
| 2 | I | R | I |
| 3 | I | R | R |
| 4 | R | I | I |
| 5 | R | I | R |
| 6 | R | R | I |
| 7 | R | R | R |

**NOTE**

**Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.**




MRV11-A Address Word Format




M7942 Etch Rev D

**512 by 4-Bit PROM Addresses**

| Bank Address Jumpers | | | Word/Byte Address | Physical Row | BRPLY L Jumper |
|---|---|---|---|---|---|
| W15 | W16 | W17 | | | |
| I | I | I | 0-1777 | CE0 | W0 |
| I | I | R | 2000-3777 | CE1 | W1 |
| I | R | I | 4000-5777 | CE2 | W2 |
| I | R | R | 6000-7777 | CE3 | W3 |
| R | I | I | 10000-11777 | CE4 | W4 |
| R | I | R | 12000-13777 | CE5 | W5 |
| R | R | I | 14000-15777 | CE6 | W6 |
| R | R | R | 16000-17777 | CE7 | W7 |

**256 by 4-Bit ROM Addresses**

| Bank Address Jumpers | | | Word/Byte Address | | Physical Row | BRPLY L Jumper |
|---|---|---|---|---|---|---|
| W15 | W16 | W17 | W13 Installed W14 Removed | W13 Removed W14 Installed | | |
| I | I | I | 0-7776 | 100000-107776 | CE0 | W0 |
| I | I | R | 10000-17776 | 110000-117776 | CE2 | W2 |
| I | R | I | 20000-27776 | 120000-127776 | CE4 | W4 |
| I | R | R | 30000-37776 | 130000-137776 | CE6 | W6 |
| R | I | I | 40000-47776 | 140000-147776 | CE1 | W1 |
| R | I | R | 50000-57776 | 150000-157776 | CE3 | W3 |
| R | R | I | 60000-67776 | 160000-167776 | CE5 | 25 |
| R | R | R | 70000-77776 | 170000-177776 | CE7 | W7 |

**BRPLYL Select**

| Empty Row | Remove Jumper |
|---|---|
| CE0 | W0 |
| CE1 | W1 |
| CE2 | W2 |
| CE3 | W3 |
| CE4 | W4 |
| CE5 | W5 |
| CE6 | W6 |
| CE7 | W7 |

## MRV11-BA ULTRAVIOLET PROM-RAM

The MRV11-BA is a high density multifunction module with two independently configurable, asynchronous serial lines which are compatible with RS232-C and RS-423.

| | Amps | | Bus Loads | | Cables |
|---|---|---|---|---|---|
| | +5 | +12 | AC | DC | |
| W/O PROM | 0.58<br>(0.67 max.) | 0.34 | 2.8<br>(0.41 max.) | 1.0 | None |
| With PROMs | 0.62<br>(0.744 max.) | 0.5 | (0.6 max.) | | |

### Standard Addresses

| | |
|---|---|
| RAMs | 20000-20777 |
| PROMs | 140000-157777 |

### Standard Vectors

None

### Diagnostic Programs

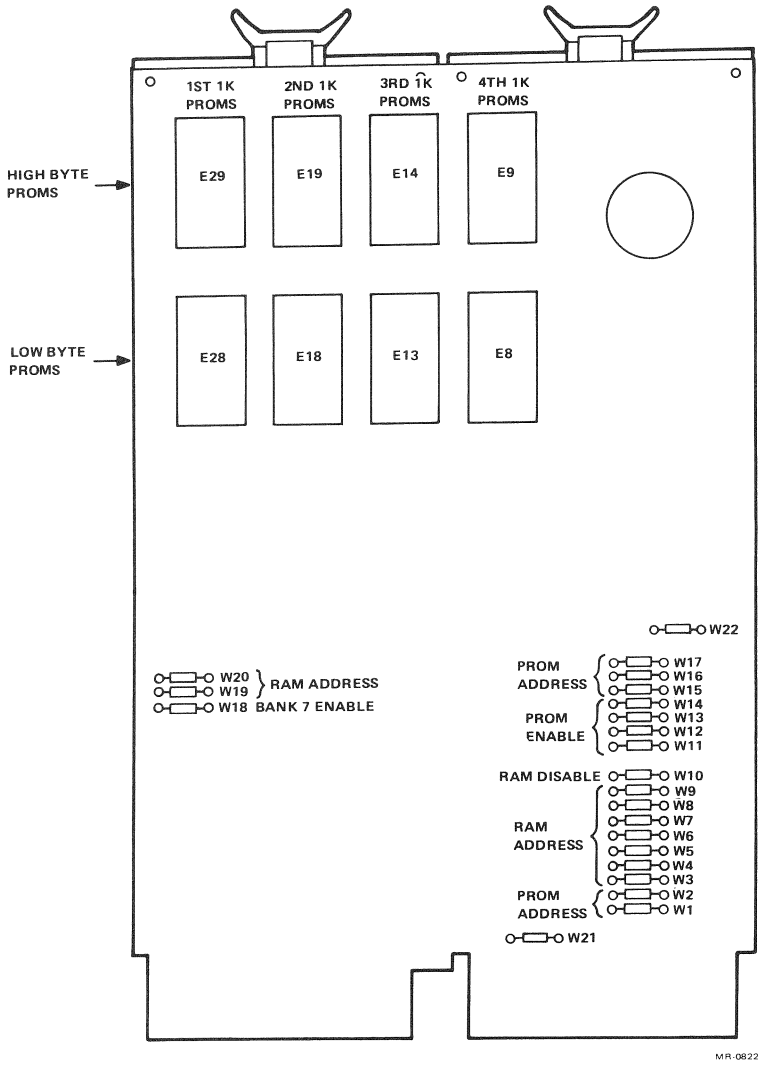
Refer to Appendix A.

### Related Documentation

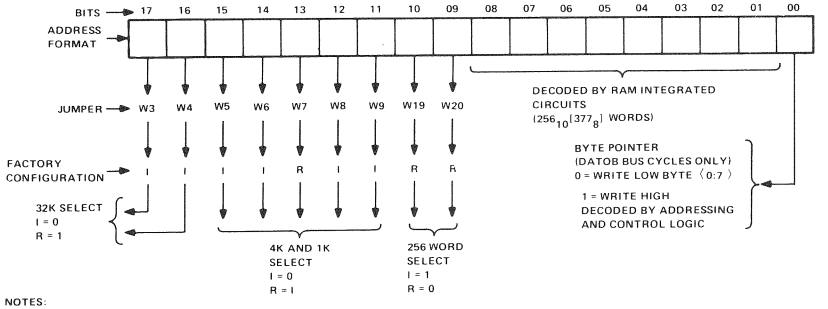
*MRV11-BA LSI-11 UV PROM-RAM User's Manual* (EK-MRV11-TM)
Field Maintenance Print Set (MP00354)
*Microcomputer Processor Handbook* (EB-18451-20)

### Recommended PROM Types

| | |
|---|---|
| DEC MRV11-BC Intel 2708<br>(DEC PN 23-00087-01) | 1024 × 8-bit, MOS, tri-state, erasable, ultraviolet (24-pin DIP) |




MRV11-BA RAM Addressing

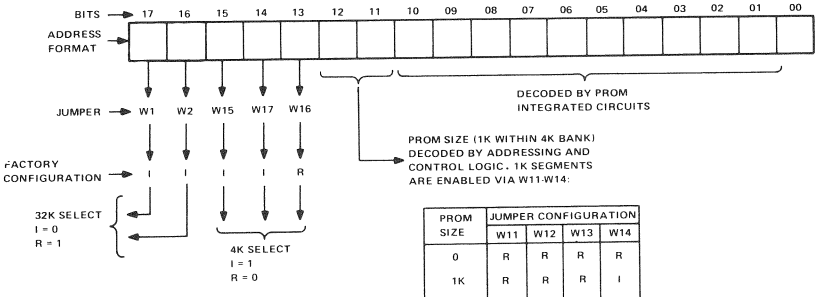



NOTES:

1. Factory configured address range = 20000 – 20377
2. I = Jumper installed; R = Jumper removed
3. W10 removed = RAM ENABLE
   W10 installed = RAM DISABLE

MR-5536

MRV11-BA RAM Addressing




| PROM SIZE | JUMPER CONFIGURATION | | | |
|---|---|---|---|---|
| | W11 | W12 | W13 | W14 |
| 0 | R | R | R | R |
| 1K | R | R | R | I |
| 2K | R | R | I | I |
| 3K | R | I | I | I |
| 4K | I | I | I | I |

NOTES:

1. Factory configured address range = 140000-157777
2. I = Jumper installed R = Jumper removed

MR-5537

MRV11-BA PROM Addressing

## RAM Addressing Summary

| Address Range (Octal) | Memory Jumper Configuration (I=Installed; R=Removed) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Bank | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W19 | W20 |
| 000000-000777 | 0 | I | I | I | I | I | I | I | R | R |
| 001000-001777 | 0 | I | I | I | I | I | I | I | R | I |
| 002000-002777 | 0 | I | I | I | I | I | I | I | I | R |
| 003000-003777 | 0 | I | I | I | I | I | I | I | I | I |
| 004000-004777 | 0 | I | I | I | I | I | I | R | R | R |
| 005000-005777 | 0 | I | I | I | I | I | I | R | R | I |
| 006000-006777 | 0 | I | I | I | I | I | I | R | I | R |
| 007000-007777 | 0 | I | I | I | I | I | I | R | I | I |
| 010000-010777 | 0 | I | I | I | I | I | R | I | R | R |
| 011000-011777 | 0 | I | I | I | I | I | R | I | R | I |
| 012000-012777 | 0 | I | I | I | I | I | R | I | I | R |
| 013000-013777 | 0 | I | I | I | I | I | R | I | I | I |
| 014000-014777 | 0 | I | I | I | I | I | R | R | R | R |
| 015000-015777 | 0 | I | I | I | I | I | R | R | R | I |
| 016000-016777 | 0 | I | I | I | I | I | R | R | I | R |
| 017000-017777 | 0 | I | I | I | I | I | R | R | I | I |
| 020000-020777 | 1 | I | I | I | I | R | I | I | R | R |
| 021000-021777 | 1 | I | I | I | I | R | I | I | R | I |
| 022000-022777 | 1 | I | I | I | I | R | I | I | I | R |
| 023000-023777 | 1 | I | I | I | I | R | I | I | I | I |
| 024000-024777 | 1 | I | I | I | I | R | I | R | R | R |
| 025000-025777 | 1 | I | I | I | I | R | I | R | R | I |
| 026000-026777 | 1 | I | I | I | I | R | I | R | I | R |
| 027000-027777 | 1 | I | I | I | I | R | I | R | I | I |
| 030000-030777 | 1 | I | I | I | I | R | R | I | R | R |
| 031000-031777 | 1 | I | I | I | I | R | R | I | R | I |
| 032000-032777 | 1 | I | I | I | I | R | R | I | I | R |
| 033000-033777 | 1 | I | I | I | I | R | R | I | I | I |
| 034000-034777 | 1 | I | I | I | I | R | R | R | R | R |
| 035000-035777 | 1 | I | I | I | I | R | R | R | R | I |
| 036000-036777 | 1 | I | I | I | I | R | R | R | I | R |
| 037000-037777 | 1 | I | I | I | I | R | R | R | I | I |
| 040000-040777 | 2 | I | I | I | R | I | I | I | R | R |
| 041000-041777 | 2 | I | I | I | R | I | I | I | R | I |
| 042000-042777 | 2 | I | I | I | R | I | I | I | I | R |
| 043000-043777 | 2 | I | I | I | R | I | I | I | I | I |
| 044000-044777 | 2 | I | I | I | R | I | I | R | R | R |
| 045000-045777 | 2 | I | I | I | R | I | I | R | R | I |
| 046000-046777 | 2 | I | I | I | R | I | I | R | I | R |
| 047000-047777 | 2 | I | I | I | R | I | I | R | I | R |

RAM Addressing Summary (Cont)

| Address Range (Octal) | Memory Jumper Configuration (I=Installed; R=Removed) Bank | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W19 | W20 |
|---|---|---|---|---|---|---|---|---|---|---|
| 050000-050777 | 2 | I | I | I | R | I | R | I | R | R |
| 051000-051777 | 2 | I | I | I | R | I | R | I | R | I |
| 052000-052777 | 2 | I | I | I | R | I | R | I | I | R |
| 053000-053777 | 2 | I | I | I | R | I | R | I | I | I |
| 054000-054777 | 2 | I | I | I | R | I | R | R | R | R |
| 055000-055777 | 2 | I | I | I | R | I | R | R | R | I |
| 056000-056777 | 2 | I | I | I | R | I | R | R | I | R |
| 057000-057777 | 2 | I | I | I | R | I | R | R | I | I |
| 060000-060777 | 3 | I | I | I | I | R | I | I | R | R |
| 061000-061777 | 3 | I | I | I | I | R | I | I | R | I |
| 062000-062777 | 3 | I | I | I | I | R | I | I | I | R |
| 063000-063777 | 3 | I | I | I | I | R | I | I | I | I |
| 064000-064777 | 3 | I | I | I | I | R | I | R | R | R |
| 065000-065777 | 3 | I | I | I | I | R | I | R | R | I |
| 066000-066777 | 3 | I | I | I | I | R | I | R | I | R |
| 067000-067777 | 3 | I | I | I | I | R | I | R | I | I |
| 070000-070777 | 3 | I | I | I | I | R | R | I | R | R |
| 071000-071777 | 3 | I | I | I | I | R | R | I | R | I |
| 072000-072777 | 3 | I | I | I | I | R | R | I | I | R |
| 073000-073777 | 3 | I | I | I | I | R | R | I | I | I |
| 074000-074777 | 3 | I | I | I | I | R | R | R | R | R |
| 075000-075777 | 3 | I | I | I | I | R | R | R | R | I |
| 076000-076777 | 3 | I | I | I | I | R | R | R | I | R |
| 077000-077777 | 3 | I | I | I | I | R | R | R | I | I |
| 100000-100777 | 4 | I | I | R | I | I | I | I | R | R |
| 101000-101777 | 4 | I | I | R | I | I | I | I | R | I |
| 102000-102777 | 4 | I | I | R | I | I | I | I | I | R |
| 103000-103777 | 4 | I | I | R | I | I | I | I | I | I |
| 104000-104777 | 4 | I | I | R | I | I | I | R | R | R |
| 105000-105777 | 4 | I | I | R | I | I | I | R | R | I |
| 106000-106777 | 4 | I | I | R | I | I | I | R | I | R |
| 107000-107777 | 4 | I | I | R | I | I | I | R | I | I |
| 110000-110777 | 4 | I | I | R | I | I | R | I | R | R |
| 111000-111777 | 4 | I | I | R | I | I | R | I | R | I |
| 112000-112777 | 4 | I | I | R | I | I | R | I | I | R |
| 113000-113777 | 4 | I | I | R | I | I | R | I | I | I |
| 114000-114777 | 4 | I | I | R | I | I | R | R | R | R |
| 115000-115777 | 4 | I | I | R | I | I | R | R | R | I |
| 116000-116777 | 4 | I | I | R | I | I | R | R | I | R |
| 117000-117777 | 4 | I | I | R | I | I | R | R | I | I |

RAM Addressing Summary (Cont)

| Address Range (Octal) | Memory Jumper Configuration (I=Installed; R=Removed) Bank | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W19 | W20 |
|---|---|---|---|---|---|---|---|---|---|---|
| 120000-120777 | 5 | I | I | R | I | R | I | I | R | R |
| 121000-121777 | 5 | I | I | R | I | R | I | I | R | I |
| 122000-122777 | 5 | I | I | R | I | R | I | I | I | R |
| 123000-123777 | 5 | I | I | R | I | R | I | I | I | I |
| 124000-124777 | 5 | I | I | R | I | R | I | R | R | R |
| 125000-125777 | 5 | I | I | R | I | R | I | R | R | I |
| 126000-126777 | 5 | I | I | R | I | R | I | R | I | R |
| 127000-127777 | 5 | I | I | R | I | R | I | R | I | I |
| 130000-130777 | 5 | I | I | R | I | R | R | I | R | R |
| 131000-131777 | 5 | I | I | R | I | R | R | I | R | I |
| 132000-132777 | 5 | I | I | R | I | R | R | I | I | R |
| 133000-133777 | 5 | I | I | R | I | R | R | I | I | I |
| 134000-134777 | 5 | I | I | R | I | R | R | R | R | R |
| 135000-135777 | 5 | I | I | R | I | R | R | R | R | I |
| 136000-136777 | 5 | I | I | R | I | R | R | R | I | R |
| 137000-137777 | 5 | I | I | R | I | R | R | R | I | I |
| 140000-140777 | 6 | I | I | R | R | I | I | I | R | R |
| 141000-141777 | 6 | I | I | R | R | I | I | I | R | I |
| 142000-142777 | 6 | I | I | R | R | I | I | I | I | R |
| 143000-143777 | 6 | I | I | R | R | I | I | I | I | I |
| 144000-144777 | 6 | I | I | R | R | I | I | R | R | R |
| 145000-145777 | 6 | I | I | R | R | I | I | R | R | I |
| 146000-146777 | 6 | I | I | R | R | I | I | R | I | R |
| 147000-147777 | 6 | I | I | R | R | I | I | R | I | I |
| 150000-150777 | 6 | I | I | R | R | I | R | I | R | R |
| 151000-151777 | 6 | I | I | R | R | I | R | I | R | I |
| 152000-152777 | 6 | I | I | R | R | I | R | I | I | R |
| 153000-153777 | 6 | I | I | R | R | I | R | I | I | I |
| 154000-154777 | 6 | I | I | R | R | I | R | R | R | R |
| 155000-155777 | 6 | I | I | R | R | I | R | R | R | I |
| 156000-156777 | 6 | I | I | R | R | I | R | R | I | R |
| 157000-157777 | 6 | I | I | R | R | I | R | R | I | I |
| 160000-160777 | 7* | I | I | R | R | R | I | I | R | R |
| 161000-161777 | 7* | I | I | R | R | R | I | I | R | I |
| 162000-162777 | 7* | I | I | R | R | R | I | I | I | R |
| 163000-163777 | 7* | I | I | R | R | R | I | I | I | I |
| 164000-164777 | 7* | I | I | R | R | R | I | R | R | R |
| 165000-165777 | 7* | I | I | R | R | R | I | R | R | I |
| 166000-166777 | 7* | I | I | R | R | R | I | R | I | R |

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

**RAM Addressing Summary (Cont)**

| Address Range (Octal) | Memory Jumper Configuration (I=Installed; R=Removed) Bank | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W19 | W20 |
|---|---|---|---|---|---|---|---|---|---|---|
| 167000-167777 | 7* | I | I | R | R | R | I | R | I | I |
| 170000-170777 | 7* | I | I | R | R | R | R | I | R | R |
| 171000-171777 | 7* | I | I | R | R | R | R | I | R | I |
| 172000-172777 | 7* | I | I | R | R | R | R | I | I | R |
| 173000-173777 | 7* | I | I | R | R | R | R | I | I | I |
| 174000-174777 | 7* | I | I | R | R | R | R | R | R | R |
| 175000-175777 | 7* | I | I | R | R | R | R | R | R | I |
| 176000-176777 | 7* | I | I | R | R | R | R | R | I | R |
| 177000-177777 | 7* | I | I | R | R | R | R | R | I | I |

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

**NOTE**

**The following jumper configurations illustrate configuring the address range in banks above bank 7 (not implemented in present LSI-11 system configurations). W8, W9, W19, and W20 can be configured as shown in the preceding pages to select the desired segment within the bank.**

| Address Range (Octal) | Memory Jumper Configuration (I=Installed; R=Removed) Bank | W3 | W4 | W5 | W6 | W7 |
|---|---|---|---|---|---|---|
| 200000-217777 | 10 | I | R | I | I | I |
| 220000-237777 | 11 | I | R | I | I | R |
| 240000-257777 | 12 | I | R | I | R | I |
| 260000-277777 | 13 | I | R | I | R | R |
| 300000-317777 | 14 | I | R | R | I | I |
| 320000-337777 | 15 | I | R | R | I | R |
| 340000-357777 | 16 | I | R | R | R | I |
| 360000-377777 | 17 | I | R | R | R | R |
| 400000-417777 | 20 | R | I | I | I | I |
| 420000-437777 | 21 | R | I | I | I | R |
| 440000-457777 | 22 | R | I | I | R | I |
| 460000-477777 | 23 | R | I | I | R | R |
| 500000-517777 | 24 | R | I | R | I | I |
| 520000-537777 | 25 | R | I | R | I | R |
| 540000-557777 | 26 | R | I | R | R | I |
| 560000-577777 | 27 | R | I | R | R | R |
| 600000-617777 | 30 | R | R | I | I | I |
| 620000-637777 | 31 | R | R | I | I | R |
| 640000-657777 | 32 | R | R | I | R | I |
| 660000-677777 | 33 | R | R | I | R | R |
| 700000-717777 | 34 | R | R | R | I | I |
| 720000-737777 | 35 | R | R | R | I | R |
| 740000-757777 | 36 | R | R | R | R | I |
| 760000-777777 | 37 | R | R | R | R | R |

## PROM Addressing Summary

| Address Range (Octal) | Memory Jumper Configuration (I = Installed; R = Removed) | | | | | |
|---|---|---|---|---|---|---|
| | Bank | W1 | W2 | W15 | W17 | W16 |
| 000000-017777 | 0 | I | I | R | R | R |
| 020000-037777 | 1 | I | I | R | R | I |
| 040000-057777 | 2 | I | I | R | I | R |
| 060000-077777 | 3 | I | I | R | I | I |
| 100000-117777 | 4 | I | I | I | R | R |
| 120000-137777 | 5 | I | I | I | R | I |
| 140000-157777 | 6 | I | I | I | I | R |
| 160000-177777 | 7* | I | I | I | I | I |
| 200000-217777 | 10 | I | R | R | R | R |
| 220000-237777 | 11 | I | R | R | R | I |
| 240000-257777 | 12 | I | R | R | I | R |
| 260000-277777 | 13 | I | R | R | I | I |
| 300000-317777 | 14 | I | R | I | R | R |
| 320000-337777 | 15 | I | R | I | R | I |
| 340000-357777 | 16 | I | R | I | I | R |
| 360000-377777 | 17 | I | R | I | I | I |
| 400000-417777 | 20 | R | I | R | R | R |
| 420000-437777 | 21 | R | I | R | R | I |
| 440000-457777 | 22 | R | I | R | I | R |
| 460000-477777 | 23 | R | I | R | I | I |
| 500000-517777 | 24 | R | I | I | R | R |
| 520000-537777 | 25 | R | I | I | R | I |
| 540000-557777 | 26 | R | I | I | I | R |
| 560000-577777 | 27 | R | I | I | I | I |
| 600000-617777 | 30 | R | R | R | R | R |
| 620000-637777 | 31 | R | R | R | R | I |
| 640000-657777 | 32 | R | R | R | I | R |
| 660000-677777 | 33 | R | R | R | I | I |
| 700000-717777 | 34 | R | R | I | R | R |
| 720000-737777 | 35 | R | R | I | R | I |
| 740000-757777 | 36 | R | R | I | I | R |
| 760000-777777 | 37 | R | R | I | I | I |

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

## PROM Addressing

| Address* Octal | Binary | 10 09 08 07 06 05 04 03 02 01 | Address Bits PROM Pins |
|---|---|---|---|
| | | 22 23 1 2 3 4 5 6 7 8 | |
| 0 | 00000000000 | L L L L L L L L L L | |
| 2 | 00000000010 | L L L L L L L L L H | |
| 4 | 00000000100 | L L L L L L L L H L | Actual Logic |
| 6 | 00000000110 | L L L L L L L L H H | Levels Required |
| 10 | 00000001000 | L L L L L L L H L L | ($1024_{10}$ |
| 12 | 00000001010 | L L L L L L L H L H | Locations) |
| 14 | | | |
| . | | | |
| . | | | |
| . | | | |
| 3776 | 11111111110 | H H H H H H H H H H | |

*Bus address bit 0 is not used. Therefore, only even-numbered addresses are shown.

# MRV11-C READ-ONLY MEMORY MODULE

The MRV11-C is a flexible, high-density ROM module used with the LSI-11 bus. The module contains 129 wirewrap pins and 16 24-pin ROM chip sockets that use a variety of user-supplied ROM chips. Masked ROMs, fusible link ROMs and ultraviolet erasable PROMs are acceptable to use. The MRV11-C is shipped without jumpers installed.

Using 4K × 8 ROM chips, the total capacity of one M8048 module can be 64K bytes, accessible either by direct access or window mapping.

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | None |
| 0.8 | | 2 | 1 | |

(plus ROM chip power)

### Standard Addresses

Recommended window starting address 760000
Bootstrap starting address: 16-bit system 173000; 18-bit system 773000

Technical detailed information is beyond the scope of this manual. Additional information can be found in the *Microcomputer Processor Handbook*, EB-18451-20.

### Related Documentation

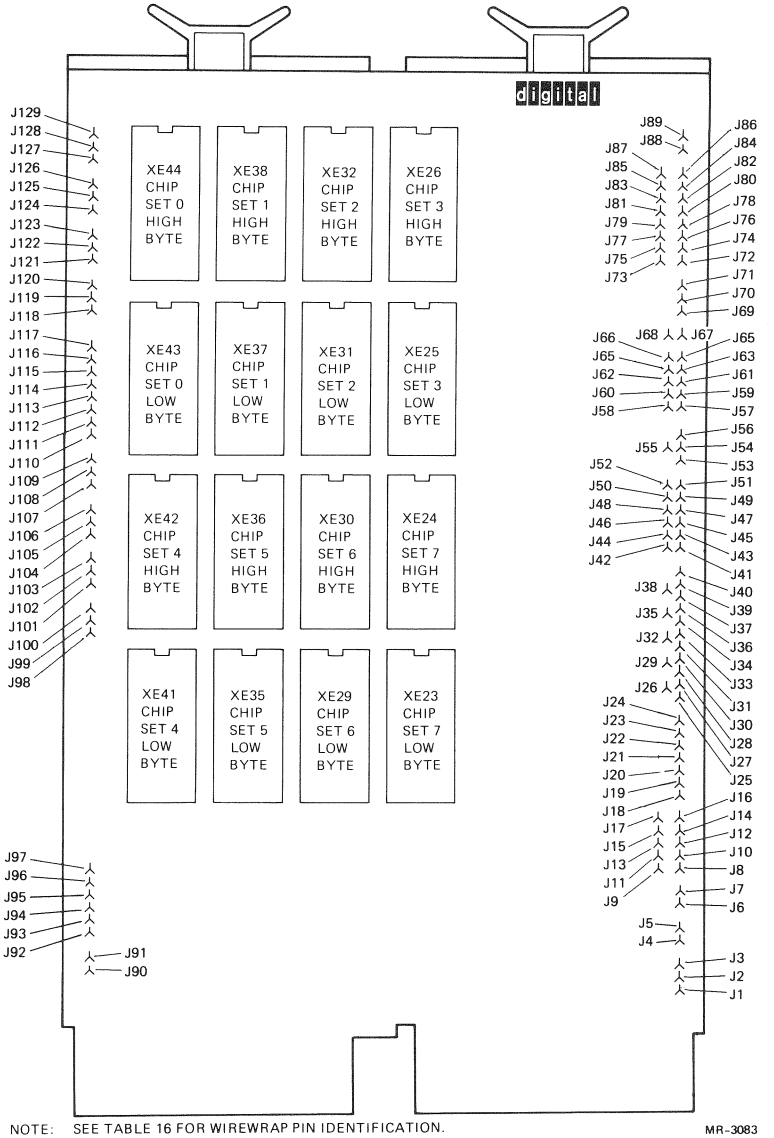
*MRV11-D Universal PROM Module User Guide* (EK-MRV1D-UG-001)
Field Maintenance Print Set (MP-00871)

**Compatible UV PROMs (Ultraviolet)**

| UV PROMs | Chip Array Size | Maximum Memory Size |
|---|---|---|
| Intel 2758 | 1K × 8 | 16K bytes |
| Intel 2716 | 2K × 8 | 32K bytes |
| Intel 2732 | 4K × 8 | 64K bytes |
| Mostek MK2716 | 2K × 8 | 32K bytes |
| T.I. TMS 2516 | 2K × 8 | 32K bytes |
| T.I. TMS 2532 | 4K × 8 | 64K bytes |

**Compatible PROMs**

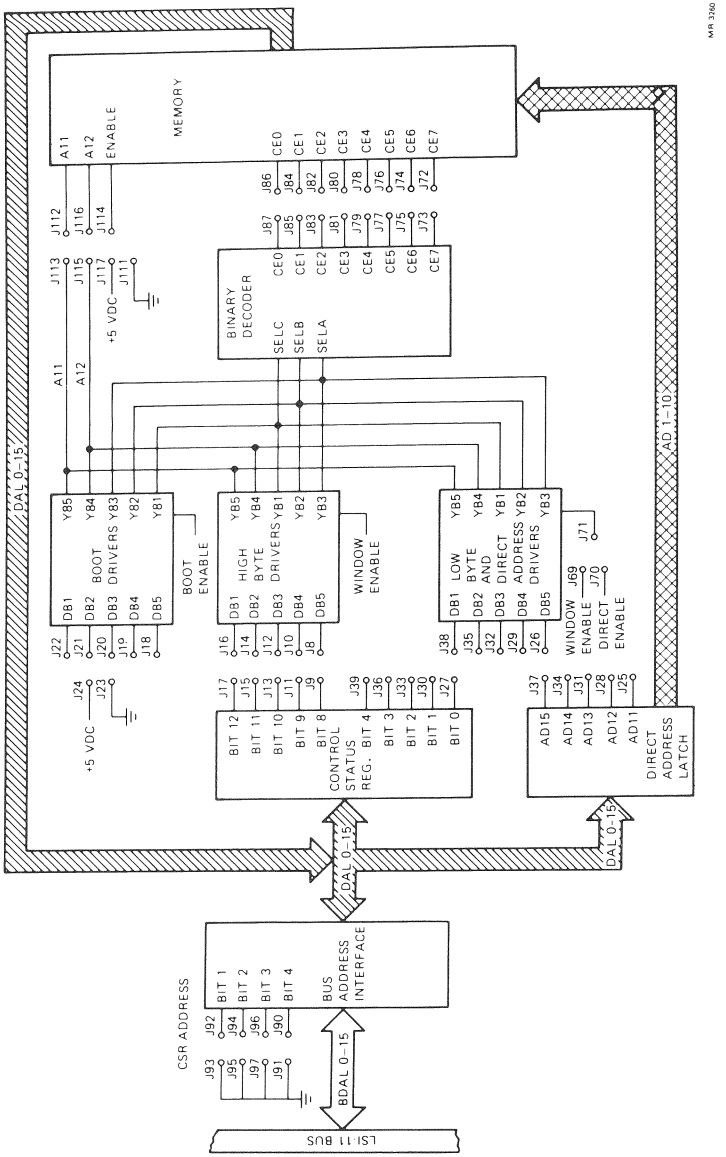
| PROM | Chip Array Size | Maximum Memory Size |
|---|---|---|
| Intel 3628 | 1K × 8 | 16K bytes |
| Signetics 82S 2708 | 1K × 8 | 16K bytes |
| Signetics 82S 181 | 1K × 8 | 16K bytes |
| Signetics 82S 191 | 2K × 8 | 32K bytes |



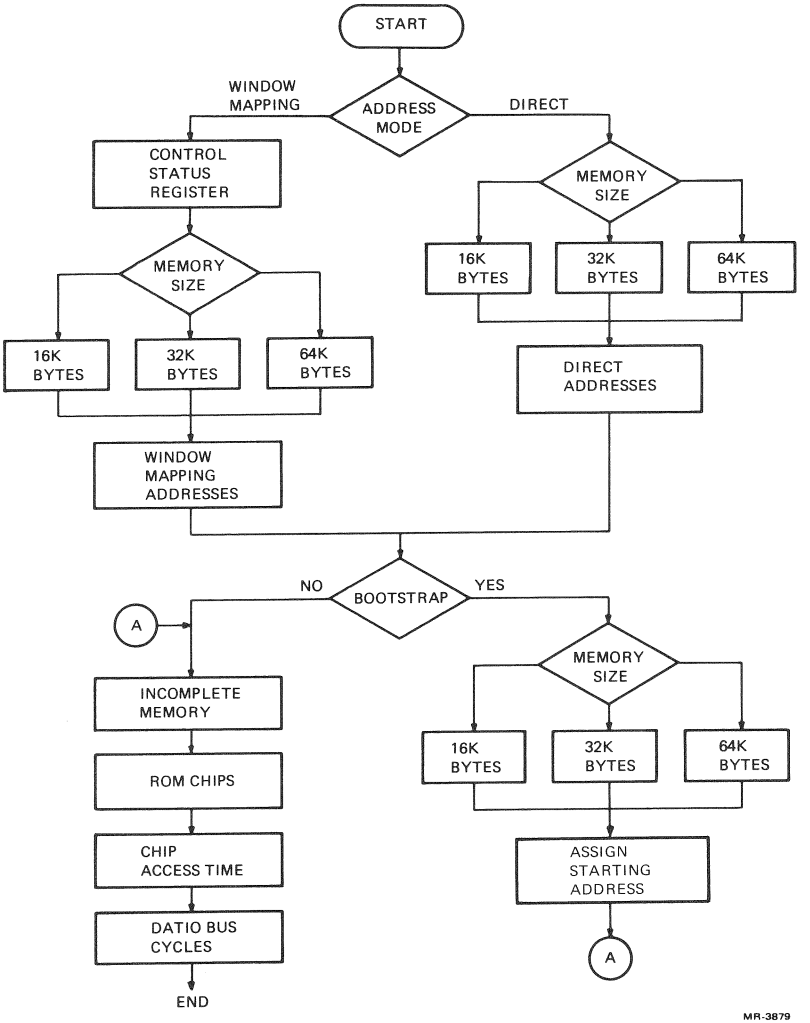

NOTE: SEE TABLE 16 FOR WIREWRAP PIN IDENTIFICATION.

MR-3083

MRV11-C Wirewrap Pin Locations




MRV11-C Configuration Interconnections




Configuration Procedure

**Wirewrap Pin Identification**

| Wirewrap Pin Designation | Function |
|---|---|
| J1 | RXCX pull-up resistor |
| J2 | RXCX optional capacitor |
| J3 | RXCX signal |
| J4 | LMATCH input for BDOUT control |
| J5 | LMATCH for BDOUT control |
| J6 | Window address enable ground |
| J7 | Window address enable |
| J8 | High byte chip enable bit A11 |
| J9 | CSR high byte bit 8 chip enable output |
| J10 | High byte chip enable bit A12 |
| J11 | CSR high byte bit 9 chip enable output |
| J12 | High byte chip enable least significant bit |
| J13 | CSR high byte bit 10 chip enable output |
| J14 | High byte chip enable intermediate bit |
| J15 | CSR high byte bit 11 chip enable output |
| J16 | High byte chip enable most significant bit |
| J17 | CSR high byte bit 12 chip enable output |
| J18 | Boot address chip enable bit A11 |
| J19 | Boot address chip enable bit A12 |
| J20 | Boot address chip enable least significant bit |
| J21 | Boot address chip enable intermediate bit |
| J22 | Boot address chip enable most significant bit |
| J23 | Boot address chip enable ground reference |
| J24 | Boot address chip enable 5 V reference |
| J25 | Direct address bit 11 chip enable output |
| J26 | Low byte chip enable A11 bit |
| J27 | CSR low byte bit 0 chip enable output |
| J28 | Direct address bit 12 chip enable output |
| J29 | Low byte chip enable A12 bit |
| J30 | CSR low byte bit 1 chip enable output |
| J31 | Direct address bit 13 chip enable output |
| J32 | Low byte chip enable least significant bit |
| J33 | CSR low byte bit 2 chip enable output |
| J34 | Direct address bit 14 chip enable output |
| J35 | Low byte chip enable intermediate bit |
| J36 | CSR low byte bit 3 chip enable output |
| J37 | Direct address bit 15 chip enable output |
| J38 | Low byte chip enable most significant bit |
| J39 | CSR low byte bit 4 chip enable output |
| J40 | Reserved for future DIGITAL use. |
| J41 | Window address bit 15 compare ground |
| J42 | Window address bit 13 compare input |
| J43 | Window address bit 12 compare ground |

**Wirewrap Pin Identification (Cont)**

| Wirewrap Pin Designation | Function |
|---|---|
| J44 | Window address bit 14 compare input |
| J45 | Window address bit 14 compare ground |
| J46 | Window address bit 15 compare input |
| J47 | Window address bit 16 compare ground |
| J48 | Window address bit 16 compare input |
| J49 | Window address bit 13 compare ground |
| J50 | Window address bit 17 compare input |
| J51 | Window address bit 17 compare ground |
| J52 | Window address bit 12 compare input |
| J53 | Direct address 32K memory limit output |
| J54 | Direct address 16K memory limit output |
| J55 | Direct address memory limit input |
| J56 | Direct address 8K memory limit output |
| J57 | Direct address bit 17 compare ground |
| J58 | Direct address bit 16 compare input |
| J59 | Direct address bit 16 compare ground |
| J60 | Direct address bit 17 compare input |
| J61 | Direct address bit 15 compare ground |
| J62 | Direct address bit 15 compare input |
| J63 | Direct address bit 14 compare ground |
| J64 | Direct address bit 14 compare input |
| J65 | Direct address bit 13 compare ground |
| J66 | Direct address bit 13 compare input |
| J67 | CSR high byte bit 15 enable ground |
| J68 | CSR high byte bit 15 enable input |
| J69 | High byte chip enable window address function |
| J70 | High byte chip enable direct address function |
| J71 | High byte chip enable function select drivers |
| J72 | Bit 7 chip select enable input |
| J73 | Bit 7 chip enable decoder output |
| J74 | Bit 6 chip select enable input |
| J75 | Bit 6 chip enable decoder output |
| J76 | Bit 5 chip select enable input |
| J77 | Bit 5 chip enable decoder output |
| J78 | Bit 4 chip select enable input |
| J79 | Bit 4 chip enable decoder output |
| J80 | Bit 3 chip select enable input |
| J81 | Bit 3 chip enable decoder output |
| J82 | Bit 2 chip select enable input |
| J83 | Bit 2 chip enable decoder output |
| J84 | Bit 1 chip select enable input |
| J85 | Bit 1 chip enable decoder output |
| J86 | Bit 0 chip select enable input |

Wirewrap Pin Identification (Cont)

| Wirewrap Pin Designation | Function |
|---|---|
| J87 | Bit 0 chip enable decoder output |
| J88 | Boot address enable ground |
| J89 | Boot address enable |
| J90 | DAL 4 CSR address select signal |
| J91 | DAL 4 CSR address select ground |
| J92 | DAL 1 CSR address select signal |
| J93 | DAL 1 CSR address select ground |
| J94 | DAL 2 CSR address select signal |
| J95 | DAL 2 CSR address select ground |
| J96 | DAL 3 CSR address select signal |
| J97 | DAL 3 CSR address select ground |
| J98 | Pin 18 input for chip set 5 |
| J99 | Chip wirewrap interconnection for chip set 5 |
| J100 | Pin 20 input for chip set 5 (chip enable 5) |
| J101 | Pin 18 input for chip set 4 |
| J102 | Chip wirewrap interconnection for chip set 4 |
| J103 | Pin 20 input for chip set 4 (chip enable 4) |
| J104 | Pin 18 input for chip set 6 |
| J105 | Chip wirewrap interconnection for chip set 6 |
| J106 | Pin 20 input for chip set 6 (chip enable 6) |
| J107 | Pin 18 input for chip set 7 |
| J108 | Chip wirewrap interconnection for chip set 7 |
| J109 | Pin 20 input for chip set 7 (chip enable 7) |
| J110 | Reserved for future DIGITAL use. |
| J111 | ROM interconnection, ground reference |
| J112 | Chip enable bit bus input |
| J113 | Address bit A11, used as chip input A10 |
| J114 | Chip interconnection loop (to wirewrap pins) |
| J115 | Address bit A12, used as chip input A11 |
| J116 | Chip interconnection loop for chip pin 21 |
| J117 | ROM interconnection +5 Vdc voltage reference |
| J118 | Pin 18 input for chip set 0 |
| J119 | Chip wirewrap interconnection for chip set 0 |
| J120 | Pin 20 input for chip set 0 (chip enable 0) |
| J121 | Pin 18 input for chip set 1 |
| J122 | Chip wirewrap interconnection for chip set 1 |
| J123 | Pin 20 input for chip set 1 (chip enable 1) |
| J124 | Pin 18 input for chip set 2 |
| J125 | Chip wirewrap interconnection for chip set 2 |
| J126 | Pin 20 input for chip set 2 (chip enable 2) |
| J127 | Pin 18 input for chip set 3 |
| J128 | Chip wirewrap interconnection for chip set 3 |
| J129 | Pin 20 input for chip set 3 (chip enable 3) |

### Control and Status Register

Each MRV11-C board uses one 16-bit control and status register located in the system I/O page to determine mapping of ROM segments into windows in the window mapped mode. The default address for this CSR is 177000 (777000 in the PDP-11/23 system). The valid address range for CSRs is 177000 to 177036 (777000 to 777036 on PDP-11/23s).

The CSR contains a 5-bit read/write field for each window. The number stored in this field (0 to $31_{10}$) selects the desired 2Kb region from the MRV11-C board to be associated with the window in question. CSR bits 0 through 4 control the mapping of the low address window, window 0. The low five bits of the upper byte (bits 8 through 12) control the mapping of window 1.

The MRV11-C optionally provides a window enable/disable capability. When this option is selected, bit 15 of the CSR is used to enable or disable window response under program control. When bit 15 is a 0, the board will respond to references to the CSR or DATI or DATIO references to either of the windows. When bit 15 is a 1, only the CSR will respond. If the enable/disable option is not selected, bit 15 of the CSR will be read only and will always be 0. The enable/disable bit has no effect on direct mode addressing or the bootstrap window capability. If enable/disable option is used, bit 15 on system initializes, disabling the board.

**Control and Status Register Addresses**

| CSR Address | Bit 4 J90 to J91 | Bit 3 J96 to J97 | Bit 2 J94 to J95 | Bit 1 J92 to J93 |
|---|---|---|---|---|
| 177000* | R | R | R | R |
| 177002 | R | R | R | I |
| 177004 | R | R | I | R |
| 177006 | R | R | I | I |
| 177010 | R | I | R | R |
| 177012 | R | I | R | I |
| 177014 | R | I | I | R |
| 177016 | R | I | I | I |
| 177020 | I | R | R | R |
| 177022 | I | R | R | I |
| 177024 | I | R | I | R |
| 177026 | I | R | I | I |
| 177030 | I | I | R | R |
| 177032 | I | I | R | I |
| 177034 | I | I | I | R |
| 177036 | I | I | I | I |

R = jumper removed. I = jumper installed.

*Default address

**NOTE**

**Install J67 to J68 to allow the use of bit 15 of the CSR.**

MRV11-C Direct Addressing Starting Address

| Starting Address | Bank | Bit 17 57 to 60 | Bit 16 59 to 58 | Bit 15 61 to 62 | Bit 14 63 to 64 | Bit 13 65 to 66 |
|---|---|---|---|---|---|---|
| 0 | 0 | I | I | I | I | I |
| 20000 | 1 | I | I | I | I | R |
| 40000 | 2 | I | I | I | R | I |
| 60000 | 3 | I | I | I | R | R |
| 100000 | 4 | I | I | R | I | I |
| 120000 | 5 | I | I | R | I | R |
| 140000 | 6 | I | I | R | R | I |
| 160000 | 7 | I | I | R | R | R |
| 200000 | 10 | I | R | I | I | I |
| 220000 | 11 | I | R | I | I | R |
| 240000 | 12 | I | R | I | R | I |
| 260000 | 13 | I | R | I | R | R |
| 300000 | 14 | I | R | R | I | I |
| 320000 | 15 | I | R | R | I | R |
| 340000 | 16 | I | R | R | R | I |
| 360000 | 17 | I | R | R | R | R |
| 400000 | 20 | R | I | I | I | I |
| 420000 | 21 | R | I | I | I | R |
| 440000 | 22 | R | I | I | R | I |
| 460000 | 23 | R | I | I | R | R |
| 500000 | 24 | R | I | R | I | I |
| 520000 | 25 | R | I | R | I | R |
| 540000 | 26 | R | I | R | R | I |
| 560000 | 27 | R | I | R | R | R |
| 600000 | 30 | R | R | I | I | I |
| 620000 | 31 | R | R | I | I | R |
| 640000 | 32 | R | R | I | R | I |
| 660000 | 33 | R | R | I | R | R |
| 700000 | 34 | R | R | R | I | I |
| 720000 | 35 | R | R | R | I | R |
| 740000 | 36 | R | R | R | R | I |
| 760000 | 37 | R | R | R | R | R |

R = jumper removed.
I = jumper installed.

### Using Multiple Boards

Up to 16 MRV11-C boards may be configured in a single system. When multiple boards are present, each board has a unique control and status register address assigned in increasing order from 177000 (777000 in PDP-11/23 systems). Each board can have a unique 4Kb area of the physical address space set aside for its windows, but it is also possible to share one 4Kb area of the address space among all MRV11-C boards installed in the system. This is done by using the enable/disable capability discussed earlier. When enable/disable is implemented, the disable bit in the CSR will be set automatically by BINIT on the bus or by execution of the RESET instruction. Therefore, the initial state of the system will have all boards disabled. To access a particular segment of ROM in this multiboard configuration, the programmer first enables the desired board and maps the segment. When access to that segment is completed, the board is again disabled to allow another board to be selected some other time.

**Chip Enable Jumpers**

| Sockets Enabled | Chip Enable Signal | Wirewrap Jumpered Pins |
|---|---|---|
| XE43, XE44 | CE0 | J86 to J87 |
| XE37, XE38 | CE1 | J84 to J85 |
| XE31, XE32 | CE2 | J82 to J83 |
| XE25, XE26 | CE3 | J80 to J81 |
| XE41, XE42 | CE4 | J78 to J79 |
| XE35, XE36 | CE5 | J76 to J77 |
| XE29, XE30 | CE6 | J74 to J75 |
| XE23, XE24 | CE7 | J72 to J73 |

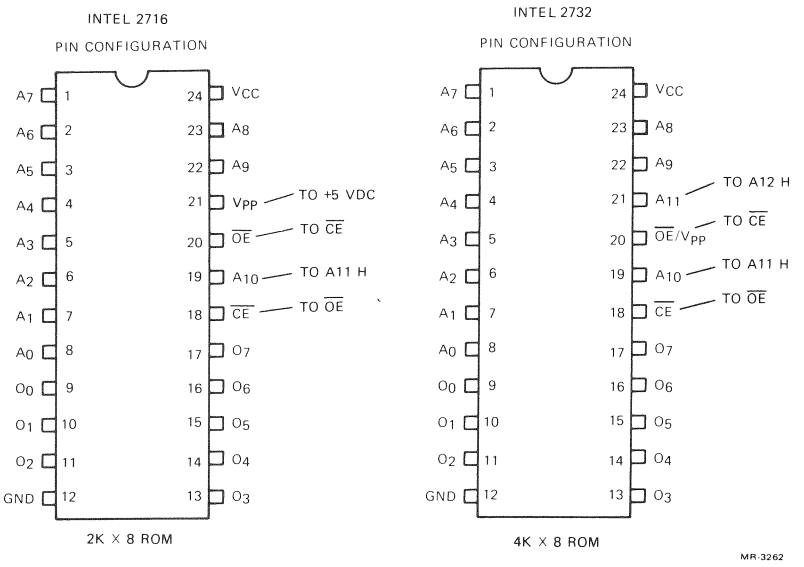
**NOTE**
**J40 and J110 are unused at this time.**

### ROM Chips

The ROM is provided by the user and consists of up to 16 chips that are inserted into prewired sockets. The chips will be either 1K × 8 bit, 2K × 8 bit, or 4K × 8 bit ROMs. When the MRV11-C is fully populated, the result will be either 16K, 32K, or 64K bytes of memory. These ROMs can be supplied by a variety of vendors and the basic configuration for many of the ROMs is standardized except for pins 18, 19, 20, and 21. The configuration of these pins will vary depending upon the size of the ROM and the vendor who supplies them. The user should verify the vendor's specifications in order to determine if a particular ROM can be used on the MRV11-C.

The MRV11-C module is configured so that the user can select the signals that are applicable to pins 18, 19, and 21. The board provides wirewrap pins for the user to select the A11, A12, 5 Vdc or ground. There are three individual loops that interconnect all chips and three wirewrap pins available for each individual chip. Wirewrap pin J112 interconnects pin 19 of all the chips and pin J116 interconnects pin 21 of all the chips; these are normally designated as the A10 or A11 inputs to the chips.

Wirewrap pin J114 interconnects wirewrap pins that are individually associated with each chip. Pin 18 of each chip is individually wired to a wirewrap pin and chip pin 20 is wired to the chip enable signal. Chip pin 20 is also individually wired to a wirewrap pin. The user must determine from the vendor's specifications which signals apply to which pins and must install jumper wires as needed to configure an operational module.




MRV11-C ROM Pin Configuration Sample

# MRV11-D UNIVERSAL PROM MODULE

**GENERAL**

The MRV11-D is a flexible, high density, dual size module used with the LSI-11 bus. The module contains 41 jumper posts, 2 switch packs, and 16 28-pin memory chip sockets. A variety of user ROMs, such as fusible link PROMs, ultraviolet eraseable (UV E) PROMs, and masked ROMs are acceptable to use. The module is shipped from the factory with all jumpers installed.

The MRV11-D accepts several densities, up to and including 32K by 8; with 16 32K devices, memory capacity is 512K bytes.

| **Amps** | | **Bus Loads** | |
|---|---|---|---|
| +5 | +12 | AC | DC |
| 1.6 | | 2 | 1 |

(plus ROM chip power)

**Standard Addresses**

Recommended page mode
- Window 0 is addressed between 17773000 and 17773776
- Window 1 is addressed between 17765000 and 17765776
- PCR address is fixed at location 1777520

Page mode PCR is used configured between 17777000 and 1777036.
Console octal debugging technique (ODT)
Terminal addresses used by console ODT addresses

16-bit addressing = 177560 - 177566
18-bit addressing = 777560 - 777566
22-bit addressing = 1777560 - 1777566

Detailed technical information is beyond the scope of this manual. For more information, refer to the *Microcomputer Processor Handbook*, EB-18451-20.

# MRV11-D/M8578

## Diagnostic Programs

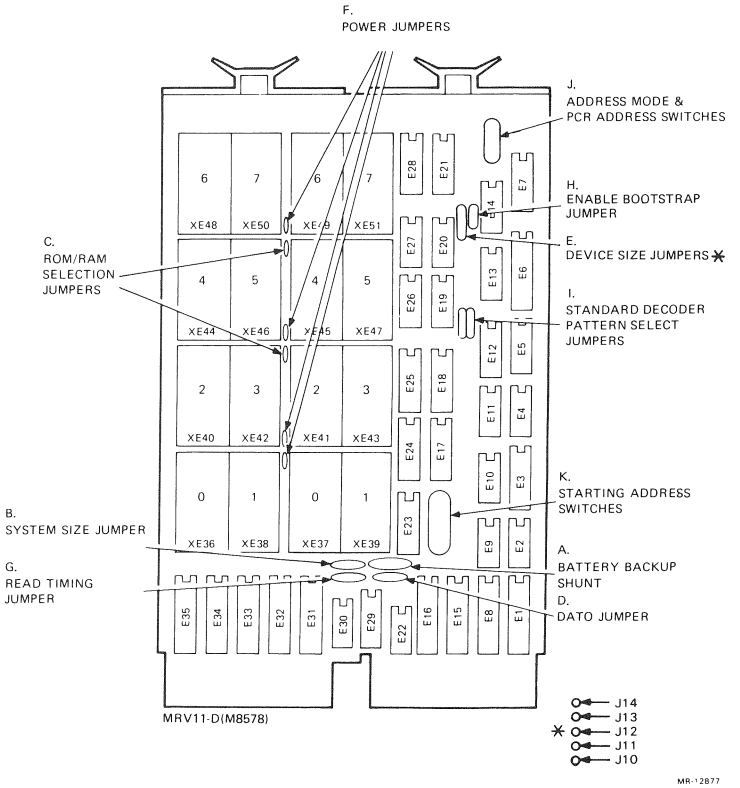
None

### Related Documentation

*MRV11-D Universal PROM Module User Guide* (EK-MRV1D-UG)
Field Maintenance Print Set (MP-00566)

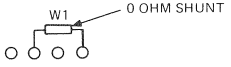
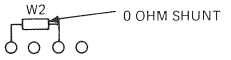
### PROM Sizes and Pinouts

The MRV11-D contains 16 28-pin sockets to house the various PROMs and static RAM devices that can be used in the module. The sockets can house 2K by 8, 4K by 8, 8K by 8, 16K by 8, and 32K by 8 PROMs. In addition, the bottom half of the socket array (chip sets 0 through 3) can accommodate static RAM. The 2K by 8 and 4K by 8 PROMs contain 24 pins while the others contain 28 pins.




MRV11-D (M8578) Jumper and Switch Locations

A.
BATTERY BACKUP SHUNT

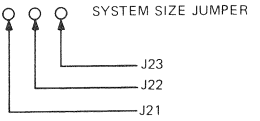
| JUMPER CONNECTION | DESCRIPTION |
|---|---|
|   | SHIPPED CONFIGURATION. NO BATTERY BACKUP ON SYSTEM; +5V ONLY |
|   | BATTERY BACKUP PROTECTION FOR RAMS |

NOTE

INSTALL W1 OR W2 BUT NOT BOTH.

MR-12878

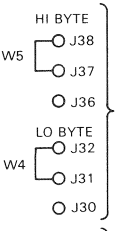
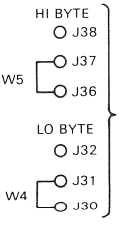
B.
SYSTEM SIZE JUMPERS (W3)




| JUMPER CONNECTION | DESCRIPTION |
|---|---|
|   | SPECIFIES 16-BIT OR 18-BIT SYSTEM. |
|   | SPECIFIES 22-BIT SYSTEM. |

MR-12879

C.
ROM/RAM SELECTION JUMPERS (W4, W5)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
|   | THIS CONFIGURATION IS USED FOR ALL ROM MEMORY (NO RAM). BOTH JUMPER CLIPS (W4 AND W5) MUST BE INSERTED IN THE UPPERMOST PINS. |
|   | THIS CONFIGURATION IS FOR ROM/RAM MEMORY. RAM IS INSTALLED IN CHIP SETS 0 THROUGH 3 (BOTTOM HALF OF ARRAY). WHEN RAM IS INSERTED. BOTH JUMPER CLIPS MUST BE INSTALLED IN THE LOWER PINS. |

MR-12926

D.
DATO JUMPER CONNECTION (W6)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
| W6<br>J15 J16 J17 | CAUSES BUS TIMEOUT WHEN ACCESSED BY DATO CYCLE. NOT USED WHEN RAM IS INSTALLED. |
| W6<br>J15 J16 J17 | WITH RAM INSTALLED, USE THIS CONFIGURATION WHICH WILL RESPOND TO DATO CYCLES. |

NOTE
THE PCR OR THE BOOTSTRAP PCR WILL NOT TIMEOUT IN EITHER CONFIGURATION WHEN ACCESSED BY DATO CYCLES. EITHER JUMPER CONNECTION MAY BE USED, BUT THE CLIP MUST BE INSTALLED TO ALLOW ANY DATO CYCLE ON THE MODULE.

MR-12880

E.
DEVICE SIZE JUMPERS (W7, W8)

THE TABLE BELOW REFLECTS THE REV C AND REV D ETCH CONFIGURATION. THE ETCH AND BOARD NUMBER IS LOCATED ON THE COMPONENT SIDE OF THE MODULE ALONG THE LEFT HAND SIDE.

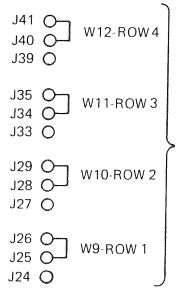
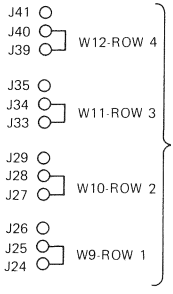
5015213C — REV C ETCH
50152130 — REV D ETC

| JUMPER CONNECTION (REV C ETCH / REV D ETCH) | DESCRIPTION |
|---|---|
| TO PIN 41 (+5V) (WIRE WRAP) — J14 O; J13 — W8; J12 — W8 | CHOOSES 2K BY 8 DEVICE ONLY |
| W7: J11 — W7; J10 — W7 | |
| W8: J14 — W8; J13 — W8<br>W7: J12 — W7; J11 — W7; J10 — W7 | CHOOSES 4K BY 8, 8K BY 8, OR 16K BY 8 DEVICES. |
| W8: J14 — W8; J13 — W8<br>W7: J12; J11 — W7; J10 — W7 | CHOOSES 32K BY 8 DEVICES |

NOTE: A NEW ARRAY DECODER IS REQUIRED IF YOU USE 32K AND 16K BY 8 DEVICES. USE DIFFERENT QUANTITIES THAN THOSE DESIGNATED BY THE STANDARD DECODER, OR MIX 4K, 8K OR 16K BY 8 DEVICES. TO MIX 4K, 8K OR 16K BY 8 DEVICES WITH 32K BY 8 DEVICES YOU MUST PROPERLY CONFIGURE THE POWER JUMPERS FOR EACH ROW. ROWS CONTAINING 32K BY 8 DEVICES MUST BE JUMPERED FOR ADDRESS RATHER THAN POWER. (SEE TABLE 3-6)

MR-12927

F.
POWER JUMPER CONNECTIONS
(W9,W10,W11,W12)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
|  | THIS CONFIGURATION IS FOR 2K BY 8 AND 4K BY 8 ROMS AND 8K BY 8 STATIC RAM. THE POWER JUMPER MAY BE IN EITHER POSITION FOR THE 8K BY 8 ROM. THE POSITION SHOWN PROVIDES +5V POWER TO PIN 26. THE CONFIGURING IS DONE ON A ROW BY ROW BASIS. FOR EXAMPLE, IF 4K BY 8 ROMS ARE INSTALLED IN ROWS 1, 2, 3 AND 16K BY 8 ROMS ARE INSTALLED IN ROW 4, THE ROW 4 JUMPER WOULD BE CONNECTED BETWEEN THE TWO LOWER PINS WHILE ALL THE OTHER JUMPERS ARE CONNECTED AS SHOWN. |
|  | FOR 16K BY 8 OR 32K BY 8 DEVICES, THE POWER JUMPER MUST BE IN THIS POSITION. IN THIS POSITION, PIN 26 IS CONNECTED BY AN ADDRESS LINE. |

MR-12888

G.
READ TIMING JUMPER (W13)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
|  | 450 ns READ TIME (NORMAL). |
|  | 200 ns READ TIME (FAST). IN THIS CONFIGURATION, SPEED ADVANTAGE IS OBTAINED BUT THE SLOWEST DEVICE INSTALLED ON THE BOARD MUST MEET THE 200 ns ACCESS TIME REQUIREMENT. |

MR-12887

H.
ENABLE BOOTSTRAP JUMPER (W14)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
| J6 ○<br>J5 ○ W14<br>J4 ○ | ENABLES BOOTSTRAP. ALLOWS 512 BYTES AT 17773000 (WINDOW 0), AND 512 BYTES AT 17765000 (WINDOW 1) TO BE USED AS BOOTSTRAP. BOOTSTRAP PCR ADDRESS IS 17777520. |
| J6 ○<br>J5 ○ W14<br>J4 ○ | DISABLES BOOTSTRAP ON MRV11-D. NONE OF THE ABOVE LOCATIONS RESPOND. |

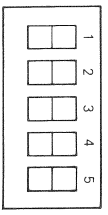
MR-12881

I.
STANDARD DECODER PATTERN
SELECT JUMPERS (W15,W16)

| JUMPER CONNECTION | DESCRIPTION |
|---|---|
| J9 ○ J3 ○<br>J8 ○ W16 J2 ○ W15<br>J7 ○ J1 ○ | 2K BY 8 ROMS, 1/2 POPULATED |
| J9 ○ J3 ○ W15<br>J8 ○ W16 J2 ○<br>J7 ○ J1 ○ | 2K BY 8 ROMS, FULLY POPULATED |
| J9 ○ W16 J3 ○<br>J8 ○ J2 ○ W15<br>J7 ○ J1 ○ | 4K BY 8 ROMS, FULLY POPULATED |
| J9 ○ W16 J3 ○ W15<br>J8 ○ J2 ○<br>J7 ○ J1 ○ | 8K BY 8 ROMS, FULLY POPULATED |

MR-12882

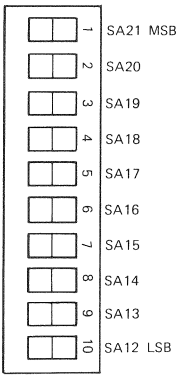
J.
PCR ADDRESS SWITCHES




| SWITCH | DESCRIPTION |
|---|---|
| | NOTE<br>ORIENT MODULE WITH HANDLES FACING AWAY AND FINGERS TOWARD YOU. |
| 1 ON=DIR OF=PAGE<br>DIRECT/PAGE | TO SELECT DIRECT MODE ADDRESSING, PUSH RIGHT SIDE OF ROCKER SWITCH DOWN (SWITCH ON). TO SELECT PAGE MODE ADDRESSING, PUSH LEFT SIDE OF ROCKER SWITCH DOWN (SWITCH OFF). |
| 2 PCR4<br>3 PCR3<br>4 PCR2<br>5 PCR1<br>PCR4, PCR3, PCR2, PCR1 | THESE SWITCHES CONTROL THE ADDRESS OF THE PAGE CONTROL REGISTER. THE SWITCHES ALLOW ANY ADDRESS FROM 17777000 TO 17777036 TO BE SELECTED ON EVEN WORD BOUNDARIES.<br><br>PUSHING DOWN THE RIGHT SIDE OF THE ROCKER SWITCH PRODUCES A LOGICAL 0 (SWITCH ON). PUSHING DOWN THE LEFT SIDE PRODUCES A LOGICAL 1 (SWITCH OFF). |
| Default: | $17777036_8$ |

MR-12883

K.
STARTING ADDRESS SWITCHES




| SWITCH | DESCRIPTION |
|---|---|
| SA1–SA10 ROCKER SWITCHES. PUSHING THE RIGHT SIDE OF THE SWITCH DOWN TURNS THE SWITCH ON (LOGIC 1). PUSHING THE LEFT SIDE OF THE SWITCH DOWN TURNS THE SWITCH OFF (LOGIC 0). | SETS UP STARTING ADDRESS OF THE MODULE. PERMITS ANY STARTING ADDRESS FROM 0 TO 17770000 ON 4K BYTE BOUNDARIES.. |

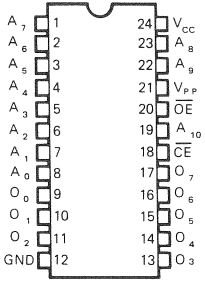
NOTE

MODULE IS ORIENTED WITH HANDLES FACING AWAY AND FINGERS TOWARD YOU.

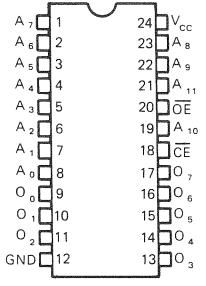
MR-12884

The basic differences on the 2764, 27128, 27256, and static RAM are in the functions of pins 26 and/or 27. The figure below shows these differences. For example, on the 16K by 8 PROM (27128), pin 26 is used as an address pin (A13). On the 32K by 8 PROM (27256), pins 26 and 27 are used as address pins (A13 and A14, respectively).

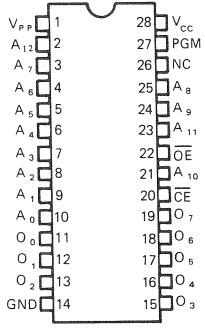
INTEL 2716 PIN CONFIGURATION
2K BY 8 PROM



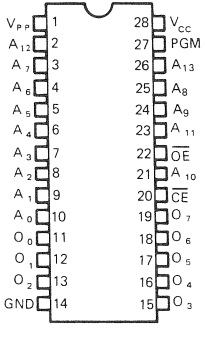

INTEL 2732A PIN CONFIGURATION
4K BY 8 PROM



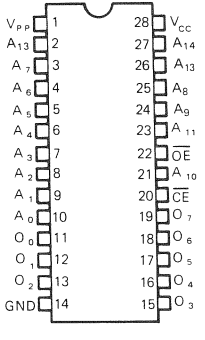

INTEL 2764 PIN CONFIGURATION
8K BY 8 PROM



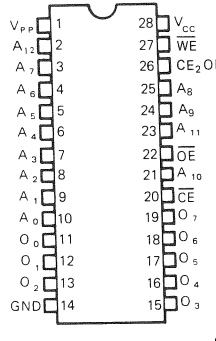

27128 PIN CONFIGURATION
16K BY 8 PROM




27256 PIN CONFIGURATION
32K BY 8 PROM



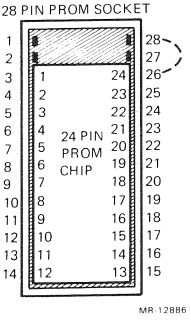

STATIC RAM




MR-12885

Compatible PROM Types

When installing a 24-pin PROM (2K by 8, 4K by 8) in a 28-pin socket, install it with the notch on top and bottom justified. Pin 1 of the PROM inserts into pin 3 of the socket. On 28-pin devices, pin 28 is the power pin. For 24-pin devices, pin 28 of the socket must be strapped to pin 26 of the socket to provide power to the device. The power jumpers strap these pins together, as shown in the following figure.




Insertion of 24-Pin PROM Chips

**NOTE**

**If you are using 24-pin devices such as the 2716 (2K by 8 PROM) on a revision C etch board, you must wire-wrap J13 (Vpp) to J40 (pin 26 of row 4). It is also necessary to jumper J40 to J41 (+5 V). However, you cannot use the jumper clip because a wire-wrap exists on J40. Therefore, you must wire-wrap, rather than jumper, J40 to J41. This procedure ensures proper read mode operation. On a revision D etch board, you can install 2K by 8 PROMs without wire-wrap.**

**Storage Capacity per ROM Chip Size and Number of Chips**

| Number of Chips Installed | (Capacity Measured in Kbytes) 2K by 8 | 4K by 8 | 8K by 8 | 16K by 8 | 32K by 8 |
|---|---|---|---|---|---|
| 2 | 4 | 8 | 16 | 32 | 64 |
| 4 | 8 | 16 | 32 | 64 | 128 |
| 6 | 12 | 24 | 48 | 96 | 192 |
| 8 | 16 | 32 | 64 | 128 | 256 |
| 10 | 20 | 40 | 80 | 160 | 320 |
| 12 | 24 | 48 | 96 | 192 | 384 |
| 14 | 28 | 56 | 112 | 224 | 448 |
| 16 | 32 | 64 | 128 | 256 | 512 |

**Typical EPROMs**

| UV PROMs | Chip Array Size | Maximum Memory Array Size |
|---|---|---|
| Intel 2716 | 2K by 8 | 32 Kbytes |
| Intel 2732 | 4K by 8 | 64 Kbytes |
| Intel 2764 | 8K by 8 | 128 Kbytes |
| Intel 27128 | 16K by 8 | 256 Kbytes |
| **Masked ROMS** | | |
| Mostek MK3700 | 8K by 8 | 128 Kbytes |
| NCR 23128 | 16K by 8 | 256 Kbytes |
| NEC 23256 | 32K by 8 | 512 Kbytes |
| National 52364 | 8K by 8 | 128 Kbytes |
| Signetics 23128 | 16K by 8 | 256 Kbytes |
| Synertek 2365 | 8K by 8 | 128 Kbytes |
| Synertek 2365A | 8K by 8 | 128 Kbytes |
| Synertek 2316B | 2K by 8 | 32 Kbytes |
| Synertek 2333-3 | 4K by 8 | 64 Kbytes |

# MSV11-B READ/WRITE MEMORY

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 0.6 | 0.3 | 1.89 | 1.0 | none |
| (1.12 max.) | (0.7 max.) | | | |

### Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 (0-17776).

### Vectors, DEC/X11 Exerciser Program

None

### Diagnostic Programs

Refer to Appendix A.

### Related Documentation

Field Maintenance Print Set (MP00067)
*Microcomputer Processor Handbook* (EB-18451-20)

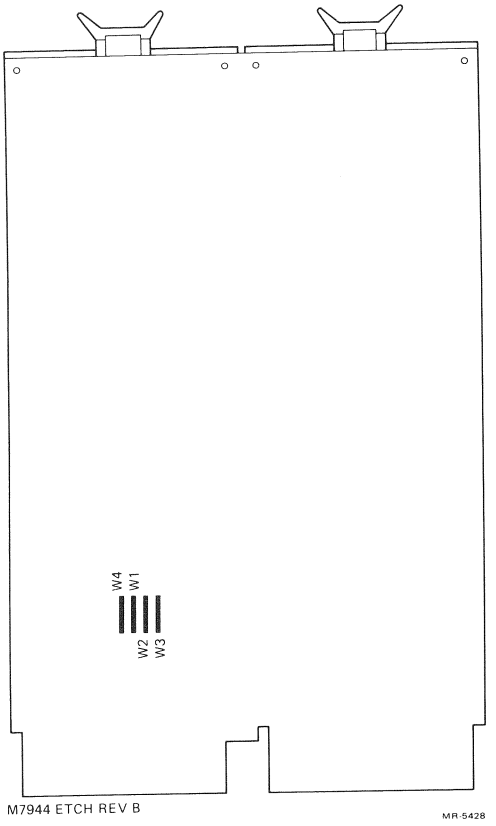
### NOTES

1. **Only one dynamic memory module in a system is needed to reply to the refresh bus functions initiated by the processor. The module selected should be the one with the longest access time (usually the module electrically farthest from the refreshing device).**

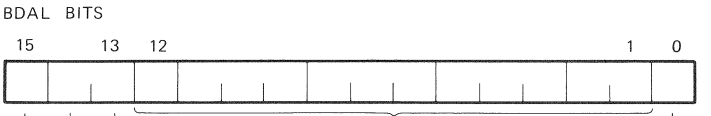
NOTES (Cont)

2. If a REV11 (M9400YA or YC) provides refresh, only the processor-resident memory (if present) should reply to refresh. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.

3. Refer to the Refresh Configuration Procedures in the "Systems Configurations" section.




M7944 Etch Rev B




| W1 | W2 | W3 | Bank No. | Address Range | Octal Address Range |
|---|---|---|---|---|---|
| I | I | I | 0 | 0-4K | 000000-017776 |
| I | I | R | 1 | 4-8K | 020000-037776 |
| I | R | I | 2 | 8-12K | 040000-057776 |
| I | R | R | 3 | 12-16K | 060000-077776 |
| R | I | I | 4 | 16-20K | 100000-117776 |
| R | I | R | 5 | 20-24K | 120000-137776 |
| R | R | I | 6 | 24-28K | 140000-157776 |
| R | R | R | 7 | 28-32K | 160000-177776 |

NOTE: I = Installed, R = Removed

MR-5429

MSV11-B Address Format/Jumpers

**NOTE**

**Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.**

**MSV11-B Address Format/Jumpers**

**Reply to Refresh**

| **Function** | **W4** |
|---|---|
| Reply | R |
| Don't reply | I |

# MSV11-C MOS READ/WRITE MEMORY

| Module | Model | Description |
|---|---|---|
| M7955-YA | MSV11-CA | 4K by 16-bit read/write memory |
| M7955-YB | MSV11-CB | 8K by 16-bit read/write memory |
| M7955-YC | MSV11-CC | 12K by 16-bit read/write memory |
| M7955-YD | MSV11-CD | 16K by 16-bit read/write memory |

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 1.1 | 0.54 | 2.32 | 1 | None |
| (2.0 max.) | (0.56 max.) | | | |

### Standard Addresses

Module is shipped configured to start at bank 0.

### Vectors

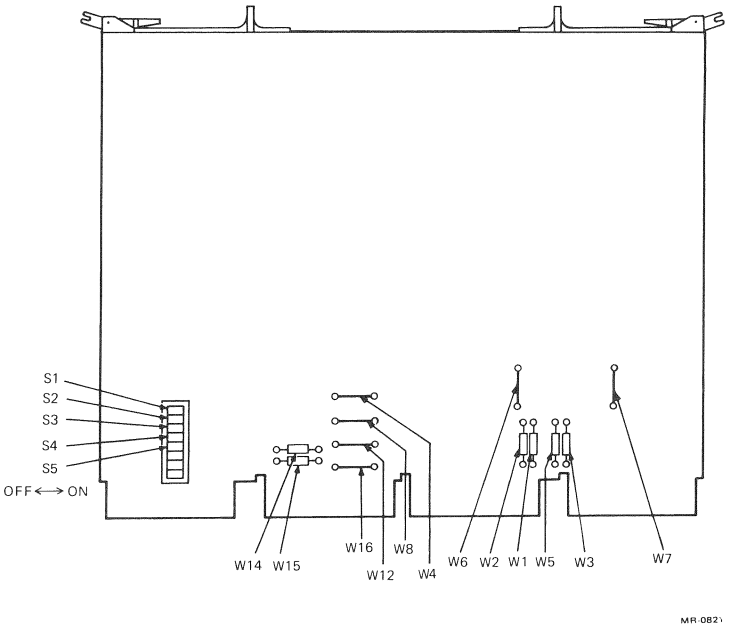
None

### Diagnostic Programs

Refer to Appendix A.

### Related Documentation

*MSV11-C User's Manual* (EK-MSV11-OP)
Field Maintenance Print Set (MP00259)
*Microcomputer Processor Handbook* (EB-18451-20)




M7955/MSV11-C Jumpers

**NOTES**

1. **Only one dynamic memory module in a system is needed to reply to the refresh bus transactions initiated by the processor. The module selected should be the one with the longest access time.**

2. **If a REV11 (M9400-YA or M9400-YC) provides refresh, only the processor-resident memory (if present) should reply to refresh. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.**

3. **If MSV11-Cs are mixed with MSV11-Bs, the MSV11-Cs should use internal refresh. Again, the memory electrically farthest from the refreshing device should reply. Refer to the "Refresh Configuration Procedure" in the "Systems Configurations" section.**

**MSV11-C Jumper Configuration When Shipped**

| Jumper Name | Jumper State | Function Implemented |
|---|---|---|
| W1 | I | Battery backup power connected to system power. |
| W2 | I | |
| W3 | I | |
| W5 | I | |
| | | Battery backup power only. W1 R, W2 I, W3 I, W5 R<br>W1 I, W2 R, W3 R, W5 I |
| | | Battery backup power available but not desired for this MSV11-C module. |
| W6 | I | Internal refresh enabled. |
| W7 | I | Reply to refresh disabled. |
| | | W6 W7 |
| | | External refresh; no reply. I R |
| | | External refresh; reply enabled. R R |
| W4 | * | Factory configured to enable the memory banks appropriate to the memory model. These are normally not changed except for: |
| W8 | * | |
| W12 | * | |
| W16 | * | 1. Maintenance - Refer to chapter 4 of *MSV11-C User's Manual*, EK-MSV11-OP.<br>2. Configuring for 28K system: Remove W16 to disable upper 4K. See configuration rules in the "Systems Configurations" section. |
| W14 | I | Bus grant continuity provided. |
| W15 | I | |

*Memory bank enable jumpers when supplied.

| Module Number | Option Designation | Memory Size | W4 | W8 | W12 | W16 |
|---|---|---|---|---|---|---|
| M7955-YD | MSV11-CD | 16K | I | I | I | I |
| M7955-YC | MSV11-CC | 12K | I | I | I | R |
| M7955-YB | MSV11-CB | 8K | I | I | R | R |
| M7955-YA | MSV11-CA | 4K | I | R | R | R |

**MSV11-CD Addressing Summary**

| Starting Address | MSV11-CD Banks | Address Range | Switch Setting S1 | S2 | S3 | S4 | S5 |
|---|---|---|---|---|---|---|---|
| 0 | 0-3 | 0-77777 | 1 | 1 | 1 | 1 | 1 |
| 20000 | 1-4 | 20000-117777 | 0 | 1 | 1 | 1 | 1 |
| 40000 | 2-5 | 40000-137777 | 1 | 0 | 1 | 1 | 1 |
| 60000 | 3-6 | 60000-157777 | 0 | 0 | 1 | 1 | 1 |
| 100000 | 4-7 | 100000-177777 | 1 | 1 | 0 | 1 | 1 |
| 120000 | 5-10 | 120000-217777 | 0 | 1 | 0 | 1 | 1 |
| 140000 | 6-11 | 140000-237777 | 1 | 0 | 0 | 1 | 1 |
| 160000 | 7-12 | 160000-257777 | 0 | 0 | 0 | 1 | 1 |
| 200000 | 10-13 | 200000-277777 | 1 | 1 | 1 | 0 | 1 |
| 220000 | 11-14 | 220000-317777 | 0 | 1 | 1 | 0 | 1 |
| 240000 | 12-15 | 240000-337777 | 1 | 0 | 1 | 0 | 1 |
| 260000 | 13-16 | 260000-357777 | 0 | 0 | 1 | 0 | 1 |
| 300000 | 14-17 | 300000-377777 | 1 | 1 | 0 | 0 | 1 |
| 320000 | 15-20 | 320000-417777 | 0 | 1 | 0 | 0 | 1 |
| 340000 | 16-21 | 340000-437777 | 1 | 0 | 0 | 0 | 1 |
| 360000 | 17-22 | 360000-457777 | 0 | 0 | 0 | 0 | 1 |
| 400000 | 20-23 | 400000-477777 | 1 | 1 | 1 | 1 | 0 |
| 420000 | 21-24 | 420000-517777 | 0 | 1 | 1 | 1 | 0 |
| 440000 | 22-25 | 440000-537777 | 1 | 0 | 1 | 1 | 0 |
| 460000 | 23-26 | 460000-557777 | 0 | 0 | 1 | 1 | 0 |
| 500000 | 24-27 | 500000-577777 | 1 | 1 | 0 | 1 | 0 |
| 520000 | 25-30 | 520000-617777 | 0 | 1 | 0 | 1 | 0 |
| 540000 | 26-31 | 540000-637777 | 1 | 0 | 0 | 1 | 0 |
| 560000 | 27-32 | 560000-657777 | 0 | 0 | 0 | 1 | 0 |
| 600000 | 30-33 | 600000-677777 | 1 | 1 | 1 | 0 | 0 |
| 620000 | 31-34 | 620000-717777 | 0 | 1 | 1 | 0 | 0 |
| 640000 | 32-35 | 640000-737777 | 1 | 0 | 1 | 0 | 0 |
| 660000 | 33-36 | 660000-757777 | 0 | 0 | 1 | 0 | 0 |
| 700000 | 34-37 | 700000-777777 | 1 | 1 | 0 | 0 | 0 |
| 720000 | x | x-x | 0 | 1 | 0 | 0 | 0 |
| 740000 | x | x-x | 1 | 0 | 0 | 0 | 0 |
| 760000 | x | x-x | 0 | 0 | 0 | 0 | 0 |

## NOTES

1. Switch setting:

   1 = ON
   0 = OFF

2. Each memory bank = one 4K address space.

3. Switches 6, 7, and 8 are not used.

**NOTE**

When used in PDP-11/23 systems, the MSV11-C memory cannot be configured in the 56K–64K byte (28K–32K word) range or in the 248K–256K byte (124K–128K word) range.

# MSV11-D,E MOS READ/WRITE MEMORY

| Model | Memory Capacity | Module | Parity Bits |
|---|---|---|---|
| MSV11-DA | 4K by 16 bits | M8044-AA | No |
| MSV11-DB | 8K by 16 bits | M8044-BA | No |
| MSV11-DC | 16K by 16 bits | M8044-CA | No |
| MSV11-DD | 32K by 16 bits | M8044-DA | No |
| MSV11-ED | 32K by 18 bits | M8045-DA | Yes |

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 2.0 | 0.41 | 2 | 1 | None |

## Standard Addresses

Module is shipped configured to start at bank 0.

## Vectors

None

## Diagnostic Programs

Refer to Appendix A.

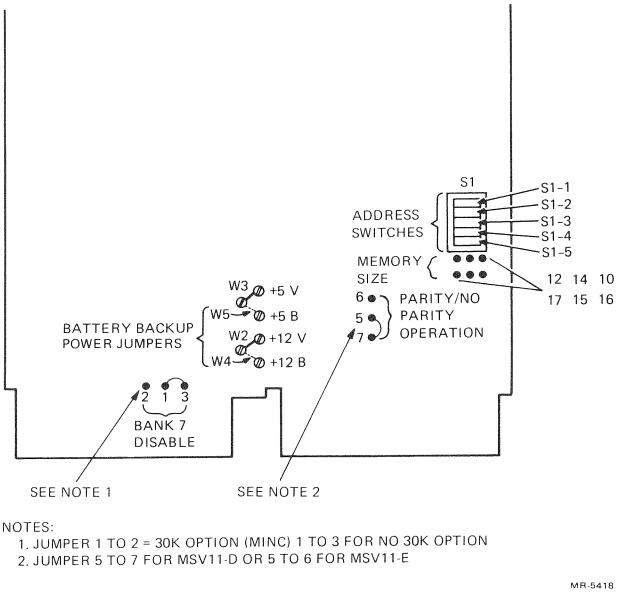
**NOTE**
**DEC diagnostic will not check parity.**

## Related Documentation

*MSV11-D, -E User's Manual* (EK-MSV1D-OP)
Field Maintenance Print Set (MP00259)
*Microcomputer Processor Handbook* (EB-18451-20)

### Address Selection

The MSV11-D or MSV11-E address can start at any 4K bank boundary. The address configured is the starting address for the contiguous portion of memory (4K, 8K, 16K, or 32K) contained on the module.




MSV11-D, MSV11-E Switch and Jumpers M8044,45

Set the switches to the desired starting address as listed in the table. Note that the module is designated to accommodate a 128K system addressing capability. However, the present addressing capability of the LSI-11 system, including all PDP-11/03, PDP-11V03 and PDP-11T03 systems, is 32K. PDP-11/23 systems, however, can address within the full 128K word range. By PDP-11 convention, the upper 4K address space is normally reserved for peripheral device and register addresses. Thus, with the present LSI-11 maximum addressing capability of 32K, bank 7 (address 160000-177777) normally should not be used for system memory.

Factory-configured modules will not respond to bank 7 addresses. In special applications that permit the use of the lower 2K portion of bank 7 for system memory (i.e., MINC), enable the lower 2K portion of bank 7 by removing the jumper from wirewrap pins 1 and 3 and connecting a new jumper from 1 to 2.

**NOTE**

**If 30K option is enabled, some diagnostics may not run.**

### Battery Backup Power

MSV11-D and MSV11-E modules are factory configured with power jumpers installed for normal system power only. If the system uses a battery backup power source, remove jumpers W2 and W3. Install new jumpers W4 and W5. (Two jumpers are removed and two new jumpers are installed.)

### Parity

One jumper is factory installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on the model. Do not reconfigure this jumper. Standard jumper configurations are listed below.

- All MSV11-D models: jumper installed from pin 7 to pin 5.
- All MSV11-E models: jumper installed from pin 6 to pin 5.

**NOTE**

**This memory parity feature is not supported by DEC diagnostics or CPUs.**

### Memory Size

Two jumpers are factory installed to configure addressing logic for memory size (number and type of memory-integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below.

| Models | Jumpers (Two Installed) Memory Select Pins | Memory Range Pins |
|---|---|---|
| MSV11-DA | From 17 to 14 | From 17 to 15 |
| MSV11-DB | From 12 to 14 | From 17 to 15 |
| MSV11-DC | From 16 to 14 | From 16 to 15 |
| MSV11-DD, ED | From 10 to 14 | From 16 to 15 |

## MSV11-D, MSV11-E Addressing Summary

| Starting Address | Switch Settings S1-1 | S1-2 | S1-3 | S1-4 | S1-5 | MSV11-DA, MSV11-EA | 4K Memory Bank(s) Selected MSV11-DB, MSV11-EB | MSV11-DC, MSV11-EC | MSV11-DD, MSV11-ED |
|---|---|---|---|---|---|---|---|---|---|
| 0 | N | N | N | N | N | 0 | 0-1 | 0-3 | 0-7 |
| 20000 | N | N | N | N | F | 1 | 1-2 | 1-4 | 1-10 |
| 40000 | N | N | N | F | N | 2 | 2-3 | 2-5 | 2-11 |
| 60000 | N | N | N | F | F | 3 | 3-4 | 3-6 | 3-12 |
| 100000 | N | N | F | N | N | 4 | 4-5 | 4-7 | 4-13 |
| 120000 | N | N | F | N | F | 5 | 5-6 | 5-10 | 5-14 |
| 140000 | N | N | F | F | N | 6 | 6-7 | 6-11 | 6-15 |
| 160000 | N | N | F | F | F | 7 | 7-10 | 7-12 | 7-16 |
| 200000 | N | F | N | N | N | 10 | 10-11 | 10-13 | 10-17 |
| 220000 | N | F | N | N | F | 11 | 11-12 | 11-14 | 11-20 |
| 240000 | N | F | N | F | N | 12 | 12-13 | 12-15 | 12-21 |
| 260000 | N | F | N | F | F | 13 | 13-14 | 13-16 | 13-22 |
| 300000 | N | F | F | N | N | 14 | 14-15 | 14-17 | 14-23 |
| 320000 | N | F | F | N | F | 15 | 15-16 | 15-20 | 15-24 |
| 340000 | N | F | F | F | N | 16 | 16-17 | 16-21 | 16-25 |
| 360000 | N | F | F | F | F | 17 | 17-20 | 17-22 | 17-26 |
| 400000 | F | N | N | N | N | 20 | 20-21 | 20-23 | 20-27 |
| 420000 | F | N | N | N | F | 21 | 21-22 | 21-24 | 21-30 |
| 440000 | F | N | N | F | N | 22 | 22-23 | 22-25 | 22-31 |
| 460000 | F | N | N | F | F | 23 | 23-24 | 23-26 | 23-32 |

## MSV11-D, MSV11-E Addressing Summary (Cont)

| Starting Address | Switch Settings S1-1 | S1-2 | S1-3 | S1-4 | S1-5 | MSV11-DA, MSV11-EA | 4K Memory Bank(s) Selected MSV11-DB, MSV11-EB | MSV11-DC, MSV11-EC | MSV11-DD, MSV11-ED |
|---|---|---|---|---|---|---|---|---|---|
| 500000 | F | N | F | N | N | 24 | 24-25 | 24-27 | 24-33 |
| 520000 | F | N | F | N | F | 25 | 25-26 | 25-30 | 25-34 |
| 540000 | F | N | F | F | N | 26 | 26-27 | 26-31 | 26-35 |
| 560000 | F | N | F | F | F | 27 | 27-30 | 27-32 | 27-36 |
| 600000 | F | F | N | N | N | 30 | 30-31 | 30-33 | 30-37 |
| 620000 | F | F | N | N | F | 31 | 31-32 | 31-34 | X |
| 640000 | F | F | N | F | N | 32 | 32-33 | 32-35 | X |
| 660000 | F | F | N | F | F | 33 | 33-34 | 33-36 | X |
| 700000 | F | F | F | N | N | 34 | 34-35 | 34-37 | X |
| 720000 | F | F | F | N | F | 35 | 35-36 | X | X |
| 740000 | F | F | F | F | N | 36 | 36-37 | X | X |
| 760000 | F | F | F | F | F | 37 | X | X | X |

**NOTES**

1. Switch settings:
   N = ON
   F = OFF
2. In unmapped systems, bank 7 cannot be selected as factory configured; however, the user can enable the lower 2K portion of bank 7.
3. X = Do not use.

# MSV11-L MOS READ/WRITE MEMORY

## GENERAL

**MSV11-L Modules**

| Model | Memory Capacity | MOS Chips | Module | Number of Chips |
|---|---|---|---|---|
| MSV11-LF | 128K bytes | 64K × 1 | M8059-FA | 18 |
| MSV11-LK | 256K bytes | 64K × 1 | M8059-KA | 36 |

## MSV11-L POWER

**Power Requirements**

| | +5 V ± 5% Current (Amps) | | | | +5 V 5% Power (Watts) | | | |
|---|---|---|---|---|---|---|---|---|
| | Standby | | Active | | Standby | | Active | |
| Type | Meas | Max | Meas | Max | Meas (+5 V) | Max (5.25 V) | Meas (+5 V) | Max (5.25 V) |
| 64K (LF) | 140 | 2.05 | 1.45 | 2.05 | 7.0 | 10.76 | 7.25 | 10.76 |
| 128K (LK) | 1.50 | 2.05 | 1.60 | 2.05 | 7.5 | 10.76 | 8.0 | 10.76 |

**Power Requirements (Cont)**

| | +5 V BBU 5% Current (Amps) | | | | +5 V BBU 5% Power (Watts) | | | |
|---|---|---|---|---|---|---|---|---|
| | Standby | | Active | | Standby | | Active | |
| Type | Meas | Max | Meas | Max | Meas (+5 V) | Max (5.25 V) | Meas (+5 V) | Max (5.25 V) |
| 64K (LF) | 0.9 | 1.26 | 1.35 | 1.85 | 4.5 | 6.62 | 6.75 | 9.71 |
| 128K (LK) | 1.0 | 1.38 | 1.40 | 1.97 | 5.0 | 7.25 | 7.0 | 10.34 |
| | +5 V Total 5% Current (Amps) | | | | +5 V Total 5% Power (Watts) | | | |
| | Standby | | Active | | Standby | | Active | |
| Type | Meas | Max | Meas | Max | Meas (+5 V) | Max (5.25 V) | Meas (+5 V) | Max (5.25 V) |
| 64K (LF) | 2.3 | 3.31 | 2.8 | 3.90 | 11.5 | 17.38 | 14.0 | 20.48 |
| 128K (LK) | 2.5 | 3.43 | 3.0 | 4.02 | 12.5 | 18.01 | 15.0 | 21.11 |

Meas = measured
Max = maximum

**NOTE**

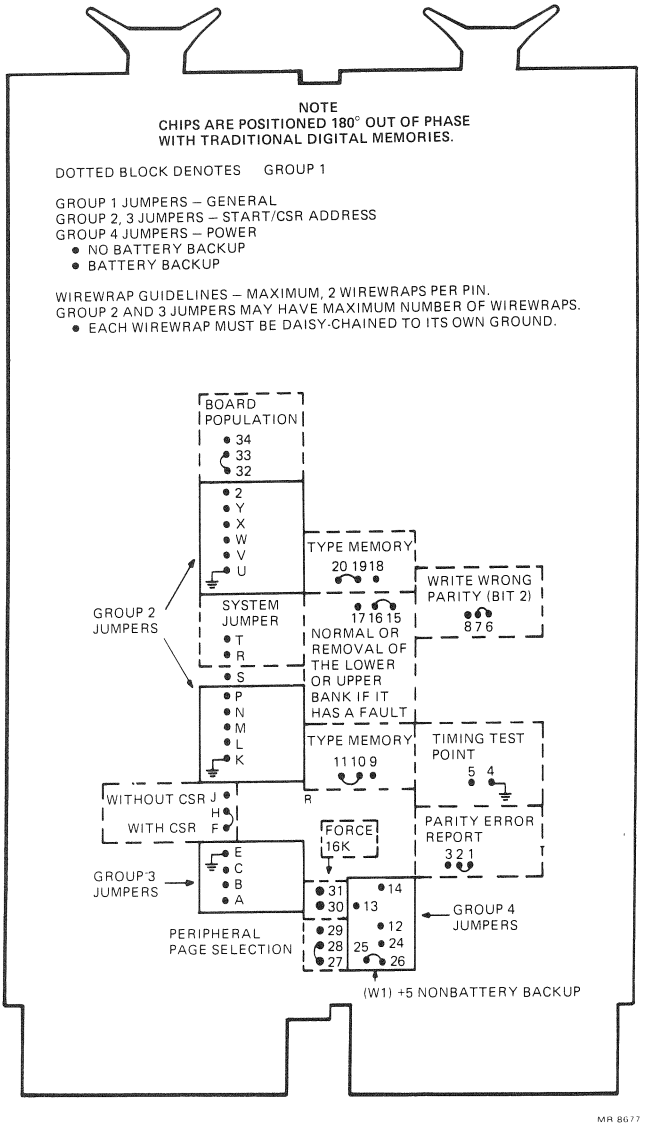
**Use the total table above for power requirements for factory configured option modules.**

## Diagnostic Programs

Refer to Appendix A.

## Related Documentation

*MSV11-L User's Guide* (EK-MSV0L-UG)
*MSV11-L Memory Module Configuration Guide* (EK-MSV1L-CG)
Field Maintenance Print Set (MP-01238)




MSV11-L Memory Module Layout

## CONFIGURATION

There are four groups of jumpers that alter the memory operation for a specific system application. The jumper groups are named as follows.

Group 1 - General jumpers
Group 2 - Starting address jumpers
Group 3 - CSR address jumpers
Group 4 - Power jumpers

### General Jumpers

The general configuration jumpers are described in the following table, and the normal or factory configuration is designated by being installed or removed.

**General Jumpers (Group 1)**

| Function | Jumper Configuration | Normal Condition |
|---|---|---|
| **Type Memory** | | |
| Nonparity | 9 to 10 | OUT |
| With parity | 11 to 10 | IN |
| Parity non-CSR | 18 to 19 | OUT |
| Parity with CSR | 20 to 19 | IN |
| **Parity Error Report** | | |
| Reported BDAL16 non-CSR | 3 to 2 | OUT |
| Reported BDAL16 and BDAL17 with CSR | 1 to 2 | IN |
| **Write Wrong Parity** | | |
| Diagnostic bit for tester use: | | |
| Disable | 8 to 7 | OUT |
| Enable | 6 to 7 | IN |

General Jumpers (Group 1) (Cont)

| Function | Jumper Configuration | *Normal* Condition |
|---|---|---|
| **CSR Selection** | | |
| Non-CSR | J to H | OUT |
| With CSR | F to H | IN |
| **Peripheral Page Selection** | | |
| 2K peripheral page | 29 to 28 | OUT |
| 4K peripheral page | 27 to 28 | IN |
| **Full or Half Memory Selection** | | |
| Half memory selection | 32 to 33 | OUT |
| Full memory selection | 34 to 33 | IN |
| **Removal of Lower or Upper Bank (with a Fault)** | | |
| Lower bank has failed | 17 to 16 | OUT |
| Normal operation or upper bank has failed | 15 to 16 | IN |
| **Extended or Normal Memory Selection** | | |
| Small system normal operation (128K) | R to T | OUT |
| Large system extended operation (2 megawords) | R to T | IN |

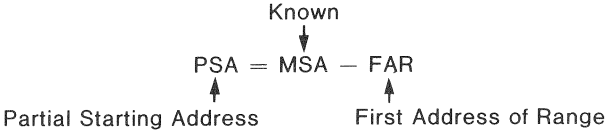
**Starting Address Jumpers**

Each MSV11-L memory module installed in a system is jumpered for its own starting address. The starting addresses are always on 4K boundaries. The module's starting address can be found by answering the question "How much memory does the system already have?" The value obtained is the module starting address in decimal k words. Module starting addresses and jumpers consist of two groups.

1. First address of the range (FAR) - Selects the first address of the 128K range that the starting address falls in.

2. Partial starting address (PSA) - Selects which 4K boundary within a specific multiple of 128K words the starting address falls in.

The module starting address (MSA) is determined by how much memory the system has in decimal k words. First address of the range plus partial starting address equals module starting address.




**First Address of Range (FAR)**

| Decimal (K) | Octal | Jumpers In (X) to Ground (K) P | N | M | L |
|---|---|---|---|---|---|
| 000-124 | 00000000-00760000 | | | | |
| 128-252 | 01000000-01760000 | | | | X |
| 256-380 | 02000000-02760000 | | | X | |
| 384-508 | 03000000-03760000 | | | X | X |
| 512-636 | 04000000-04760000 | | X | | |
| 640-764 | 05000000-05760000 | | X | | X |
| 768-892 | 06000000-06760000 | | X | X | |
| 896-1020 | 07000000-07760000 | | X | X | X |
| 1024-1148 | 10000000-10760000 | X | | | |
| 1152-1276 | 11000000-11760000 | X | | | X |
| 1280-1404 | 12000000-12760000 | X | | X | |
| 1408-1532 | 13000000-13760000 | X | | X | X |
| 1536-1660 | 14000000-14760000 | X | X | | |
| 1664-1788 | 15000000-15760000 | X | X | | X |
| 1792-1916 | 16000000-16760000 | X | X | X | |
| 1920-2044 | 17000000-17760000 | X | X | X | X |

Partial Starting Address (PSA)

| Decimal (K) | Octal | Jumpers in (X) to Ground (U) | | | | |
|---|---|---|---|---|---|---|
| | | DAL Pins 17 Z | 16 Y | 15 X | 14 W | 13 V |
| 0 | 00000000 | | | | | |
| 4 | 00020000 | | | | | X |
| 8 | 00040000 | | | | X | |
| 12 | 00060000 | | | | X | X |
| 16 | 00100000 | | | X | | |
| 20 | 00120000 | | | X | | X |
| 24 | 00140000 | | | X | X | |
| 28 | 00160000 | | | X | X | X |
| 32 | 00200000 | | X | | | |
| 36 | 00220000 | | X | | | X |
| 40 | 00240000 | | X | | X | |
| 44 | 00260000 | | X | | X | X |
| 48 | 00300000 | | X | X | | |
| 52 | 00320000 | | X | X | | X |
| 56 | 00340000 | | X | X | X | |
| 60 | 00360000 | | X | X | X | X |
| 64 | 00400000 | X | | | | |
| 68 | 00420000 | X | | | | X |
| 72 | 00440000 | X | | | X | |
| 76 | 00460000 | X | | | X | X |
| 80 | 00500000 | X | | X | | |
| 84 | 00520000 | X | | X | | X |
| 88 | 00540000 | X | | X | X | |
| 92 | 00560000 | X | | X | X | X |
| 96 | 00600000 | X | X | | | |
| 100 | 00620000 | X | X | | | X |
| 104 | 00640000 | X | X | | X | |
| 108 | 00660000 | X | X | | X | X |
| 112 | 00700000 | X | X | X | | |
| 116 | 00720000 | X | X | X | | X |
| 120 | 00740000 | X | X | X | X | |
| 124 | 00760000 | X | X | X | X | X |

**Module Starting Address (Example – 352K Words)**

| Names | First Address of Range (FAR) | | | | Partial Starting Address (PSA) | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Decimal k words binary address | 1Meg | 512K | 256K | 128K | 64K | 32K | 16K | 8K | 4K |
| BDAL values | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 |
| BDAL bits | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| Jumper pin names | P | N | M | L | Z | Y | X | W | V |
| Jumper pins | M to K | | | | Z to Y, Y to U | | | | |

**CSR Address Selection**

There are three addresses reserved for the CSR. Every MSV11-L memory module has one CSR. By convention the CSR addresses are assigned as follows. The memory module with the lowest starting address should be jumpered for the lowest CSR address. The remaining memory modules will be jumpered in sequence.

**CSR Address Jumpers (Group 3)**

| 22-Bit CSR Address | 18-Bit CSR Address | C | B | A |
|---|---|---|---|---|
| 17772100 | 772100 | | | |
| 17772102 | 772102 | | | X |
| 17772104 | 772104 | | X | |
| 17772106 | 772106 | | X | X |
| 17772110 | 772110 | X | | |
| 17772112 | 772112 | X | | X |
| 17772114 | 772114 | X | X | |
| 17772116 | 772116 | X | X | X |

Note: To obtain any 1 of 8 CSR addresses, wirewrap daisy-chain fashion from pin E, which is grounded, to each successive pin labeled X for that address.

### Power Jumpers

Power jumpers allow the MSV11-L memory module to use battery backup or nonbattery backup power.

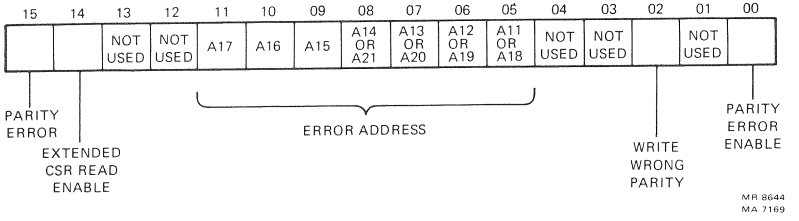
**Power Jumpers (Group 4)**

| Voltage Connection | Jumper Configuration |
|---|---|
| +5 V Nonbattery backup | 26 to 25 (W1) |
| +5 V Battery backup | 24 to 25 (W2)<br>14 to 13 (W3)*<br>or<br>12 to 13 (W4)* |

*Availability for the +5 V battery backup.

### CSR Bit Assignment

The CSR allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared by the asssertion of BUS INIT (L). The CSR bit assignments are as follows.




CSR Bit Assignments

**CSR Bit Descriptions**

| Bit | Name | Description |
|---|---|---|
| 15 | Parity error | If a parity error occurs on a DATI or DATIO(B) cycle, this bit will be set to a 1. This is a read/write bit and is reset to 0 via a power up or BUS INIT. Bit 15 will remain set unless rewritten or initialized. |
| 14 | Extended CSR Read Enable | This bit is not used on 128K word machines. It will be read as a 0. Bit 14 can be set to a 1 in a 2048K word machine only. In a 2048K word machine bit 14 is a read 1 write bit and is reset to 0 by power up or BUS INIT. When set, bit 14 allows retrieval of failed address bits of A18 through A21 stored in CSR bits 05 through 08 respectively. |
| 13, 12 | Not used | |
| 11-05 | Error address | If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 05-11 and bits A18-A21 are latched. The 128K word machines (18-bit address) require only one read on the CSR to obtain the failed address bits. CSR bit 14 = 0 allows the logic to pass A11-A17 to the LSI-11 bus. A 2048K word machine (22-bit address) requires two reads. The first read CSR bit 14 = 0 sends contents of CSR bits 05-11. Then the program must set CSR bit 14 = 1. This enables A18-A21 to be read from CSR bits 05-08.<br><br>The parity error addresses locate the parity error to a 1K segment of memory. These are read/write bits and are not reset to zero via power up or BUS INIT. If a second parity error is encountered, the new failed address will be stored in the CSR. |
| 04, 03 | Not used | |

**CSR Bit Descriptions (Cont)**

| Bit | Name | Description |
|---|---|---|
| 02 | Write wrong parity | If this bit is set to 1 and a DATO or DATOB cycle to memory occurs, wrong parity data will be written into the parity MOS RAMs. This bit may be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable.<br><br>1. With bit 02 set, write entire memory with any pattern.<br><br>2. Read first location in memory. If bit 00 of the CSR is set, then a parity error indication will be detected on the LSI-11 bus and the failed address (location 0) will be stored in the CSR.<br><br>3. Read the CSR and obtain the failed address. CSR bit 14 = 1 implies A11-A17 on CSR bits 05-11. CSR bit 14 = 1 implies A18-A21 on CSR bits 05-08. Bit 02 is a read/write bit reset to zero on power up or BUS INIT. |
| 01 | Not used | |
| 00 | Parity error enable | If a parity error occurs on a DATI or DATIO(B) cycle to memory and bit 00 is set = 1, then BDAL 16 (L) or BDAL 16 (L) and BDAL 17 (L), jumper selectable, will be asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power up or BUS INIT. |

# MSV11-P MOS MEMORY

## GENERAL

**MSV11-P Modules**

| Model | Memory Capacity | MOS Chips | Module | Number of Rows | Number of Chips |
|---|---|---|---|---|---|
| MSV11-PL | 512K bytes | 64K × 1 | M8067-LA | 8 | 72 |
| MSV11-PK | 256K bytes | 64K × 1 | M8067-KA | 4 | 36 |
| MSV11-PF | 128K bytes | 64K × 1 | M8067-FA | 8 | 72 |

**MSV11-PF (Multivoltage MOS RAMs) M8067-FA Power Requirements**

| Voltage | Standby Current(A) Measure Typical | Maximum | Active Current(A) Measure Typical | Maximum |
|---|---|---|---|---|
| +5 V Noncritical | 1.40 | 2.21 | 1.45 | 2.21 |
| +5 V BBU | 1.15 | 1.55 | 1.20 | 1.55 |
| **Total** +5 V | 2.55 | 3.76 | 2.65 | 3.76 |
| +12 V | 0.10 | 0.12 | 0.35 | 0.53 |
| **Voltage** | **Standby Power(W) Measure Typical** | **Maximum** | **Active Power(W) Measure Typical** | **Maximum** |
| +5 V Noncritical | 7.00 | 11.60 | 7.25 | 11.60 |
| +5 V BBU | 5.75 | 8.14 | 6.00 | 8.14 |
| **Total** +5 V | 12.75 | 19.74 | 13.25 | 19.74 |
| +12 V | 1.20 | 1.51 | 4.20 | 6.68 |
| Total Power | 13.95 | 21.25 | 17.45 | 26.42 |

**MSV11-PK (Single Voltage, Half Populated) M8067-KA Power**

| Voltage | Standby Current(A) Measure Typical | Maximum | Active Current(A) Measure Typical | Maximum |
|---|---|---|---|---|
| +5 V Noncritical | 1.65 | 2.10 | 1.70 | 2.10 |
| +5 V BBU | 1.35 | 1.80 | 1.75 | 2.10 |
| **Total +5** | 3.00 | 3.90 | 3.45 | 4.20 |
| | **Standby Power(W) Measure Typical** | **Maximum** | **Active Power(W) Measure Typical** | **Maximum** |
| **Voltage** | **(5.0)** | **(5.25)** | **(5.0)** | **(5.25)** |
| +5 V Noncritical | 8.25 | 11.00 | 8.50 | 11.0 |
| +5 V BBU | 6.75 | 9.45 | 8.75 | 11.0 |
| Total Power | 15.0 | 20.45 | 17.25 | 22.0 |

**MSV11-PL (Single Voltage, Fully Populated) M8067-LA Power**

| Voltage | Standby Current(A) Measure Typical | Maximum | Active Current(A) Measure Typical | Maximum |
|---|---|---|---|---|
| +5 V Noncritical | 1.65 | 2.10 | 1.70 | 2.10 |
| +5 V BBU | 1.45 | 1.90 | 1.85 | 2.20 |
| Total +5 V | 3.10 | 4.0 | 3.60 | 4.30 |
| | **Standby Power(W) Measure Typical** | **Maximum** | **Standby Power(W) Measure Typical** | **Maximum** |
| **Voltage** | **(5.0)** | **(5.25)** | **(5.0)** | **(5.25)** |
| +5 V Noncritical | 8.25 | 11.0 | 8.50 | 11.00 |
| +5 V BBU | 7.25 | 10.0 | 9.25 | 11.55 |
| Total +5 V | 15.5 | 21.0 | 17.75 | 22.55 |

**NOTE**

**Use the +5 V table (BOLD) for current requirements for factory configured modules.**

### Diagnostic Programs

Refer to Appendix A.

### Related Documentation

*MSV11-P User's Guide* (EK-MSV0P-UG)
Field Maintenance Print Set (MP-01239)

## CONFIGURATION

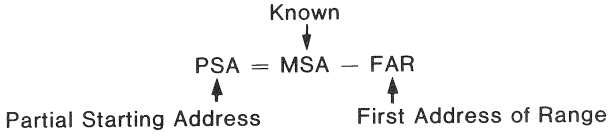
The jumpers on the MSV11-P memory module are divided into the following five groups.

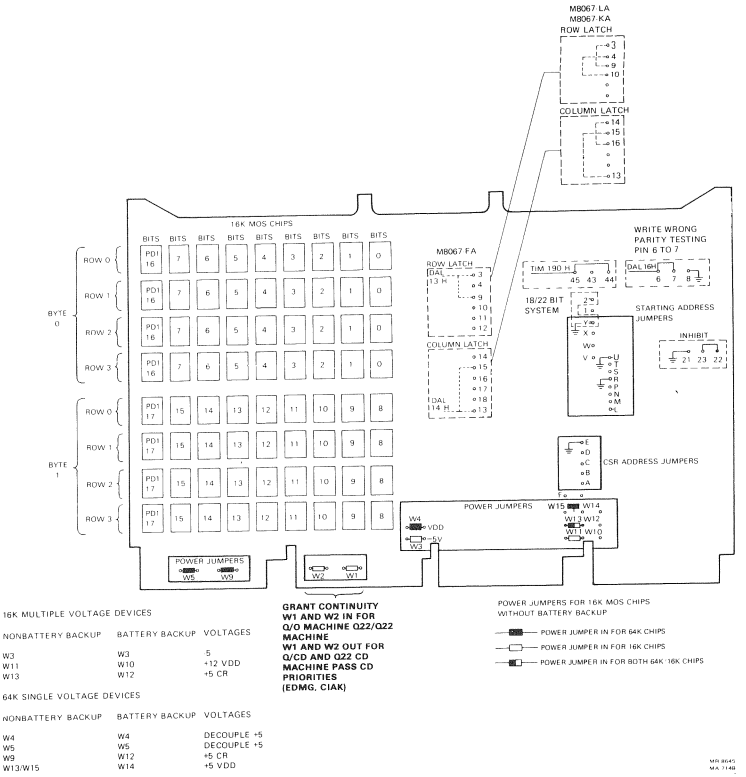
1. Starting address jumpers
2. CSR address jumpers
3. Power jumpers
4. Bus grant continuity jumpers
5. General jumpers

The location of the five jumper groups, four of which are enclosed in solid boxes and labeled, is shown in the following figure. The remaining jumpers are classified as general jumpers. The general jumpers are enclosed in dotted boxes.

### Configuring the Starting Address

The starting addresses for each module in the system is always selected on 4K boundaries. The memory size of the system is determined first by its byte content. This determines the module starting address (MSA). The first address of range (FAR) selects the 256K word range the starting address will fall into. This selection is described under FAR selection. The partial starting address (PSA) selects the 8K boundary within the 256K range selected. The selection is described under the PSA selection. The following equation is used for selecting the FAR and PSA.






MSV11-P Memory Module Layout

## FAR Starting Address Configurations (Part 1)

| First Address Ranges (FAR) | | Jumpers to Ground (Pin Y) | | |
|---|---|---|---|---|
| Decimal K words | Octal K words | Pin X (A21) | Pin W (A20) | Pin V (A19) |
| 000-248 | 00000000-01740000 | OUT | OUT | OUT |
| 256-504 | 02000000-03740000 | OUT | OUT | IN |
| 512-760 | 04000000-05740000 | OUT | IN | OUT |
| 768-1016 | 06000000-07740000 | OUT | IN | IN |
| 1024-1272 | 10000000-11740000 | IN | OUT | OUT |
| 1280-1528 | 12000000-13740000 | IN | OUT | IN |
| 1526-1784 | 14000000-15740000 | IN | IN | OUT |
| 1742-2040 | 16000000-17740000 | IN | IN | IN |

PSA Starting Address Configurations (Part 2)

| Partial Starting Address (PSA) | | Jumpers to Ground (Pin R) | | | | |
|---|---|---|---|---|---|---|
| Decimal K | Octal | Pin P (A18) | Pin N (A17) | Pin M (A16) | Pin L (A15) | Pin T (A14) |
| 0 | 00000000 | OUT | OUT | OUT | OUT | OUT |
| 8 | 00040000 | OUT | OUT | OUT | OUT | IN |
| 16 | 00100000 | OUT | OUT | OUT | IN | OUT |
| 24 | 00140000 | OUT | OUT | OUT | IN | IN |
| 32 | 00200000 | OUT | OUT | IN | OUT | OUT |
| 40 | 00240000 | OUT | OUT | IN | OUT | IN |
| 48 | 00300000 | OUT | OUT | IN | IN | OUT |
| 56 | 00340000 | OUT | OUT | IN | IN | IN |
| 64 | 00400000 | OUT | IN | OUT | OUT | OUT |
| 72 | 00440000 | OUT | IN | OUT | OUT | IN |
| 80 | 00500000 | OUT | IN | OUT | IN | OUT |
| 88 | 00540000 | OUT | IN | OUT | IN | IN |
| 96 | 00600000 | OUT | IN | IN | OUT | OUT |
| 104 | 00640000 | OUT | IN | IN | OUT | IN |
| 112 | 00700000 | OUT | IN | IN | IN | OUT |
| 120 | 00740000 | OUT | IN | IN | IN | IN |
| 128 | 01000000 | IN | OUT | OUT | OUT | OUT |
| 136 | 01040000 | IN | OUT | OUT | OUT | IN |
| 144 | 01100000 | IN | OUT | OUT | IN | OUT |
| 156 | 01140000 | IN | OUT | OUT | IN | IN |
| 160 | 01200000 | IN | OUT | IN | OUT | OUT |
| 168 | 01240000 | IN | OUT | IN | OUT | IN |
| 176 | 01300000 | IN | OUT | IN | IN | OUT |
| 184 | 01340000 | IN | OUT | IN | IN | IN |
| 192 | 01400000 | IN | IN | OUT | OUT | OUT |
| 200 | 01440000 | IN | IN | OUT | OUT | IN |
| 208 | 01500000 | IN | IN | OUT | IN | OUT |
| 216 | 01540000 | IN | IN | OUT | IN | IN |
| 224 | 01600000 | IN | IN | IN | OUT | OUT |
| 232 | 01640000 | IN | IN | IN | OUT | IN |
| 240 | 01700000 | IN | IN | IN | IN | OUT |
| 248 | 01740000 | IN | IN | IN | IN | IN |

### Control Status Register (CSR) Jumpers

Each MSV11-P memory module has a control status register. The bus master can read or write the CSR via the LSI-11 bus. The CSR is a 16-bit register whose address falls in the top 4K of system address space.

Each memory module has four CSR jumper pins (A, B, C, and D) that can be daisy-chained to pin E (the ground pin). The jumpers allow logic to detect a specific CSR address that has been assigned to a CSR memory module. The user determines which type of bus the module is being installed and connects the jumpers for each address as described in the following table.

**CSR Address Selection**

| Module Number | Extended LSI-11 Bus Address | LSI-11 Bus Address | Jumper to Ground (Pin E) D | C | B | A |
|---|---|---|---|---|---|---|
| 1 | 17772100 | 772100 | OUT | OUT | OUT | OUT |
| 2 | 17772102 | 772102 | OUT | OUT | OUT | IN |
| 3 | 17772104 | 772104 | OUT | OUT | IN | OUT |
| 4 | 17772106 | 772106 | OUT | OUT | IN | IN |
| 5 | 17772110 | 772110 | OUT | IN | OUT | OUT |
| 6 | 17772112 | 772112 | OUT | IN | OUT | IN |
| 7 | 17772114 | 772114 | OUT | IN | IN | OUT |
| 8 | 17772116 | 772116 | OUT | IN | IN | IN |
| 9 | 17772120 | 772120 | IN | OUT | OUT | OUT |
| 10 | 17772122 | 772122 | IN | OUT | OUT | IN |
| 11 | 17772124 | 772124 | IN | OUT | IN | OUT |
| 12 | 17772126 | 772126 | IN | OUT | IN | IN |
| 13 | 17772130 | 772130 | IN | IN | OUT | OUT |
| 14 | 17772132 | 772132 | IN | IN | OUT | IN |
| 15 | 17772134 | 772134 | IN | IN | IN | OUT |
| 16 | 17772136 | 772136 | IN | IN | IN | IN |

### Power Jumpers

The power jumpers are divided into the following two groups.

1. 16K multiple voltage devices (M8067-FA) with or without battery backup

2. 64K single voltage devices (M8067-LA and M8067-KA) with or without battery backup

**Power Jumpers**

**16K Multiple Voltage Devices**

| Nonbattery Backup | Battery Backup | Voltages |
|---|---|---|
| W3 | W3 | −5 |
| W11 | W10 | +12 VDD |
| W13 | W12 | +5 CR |

**64K Single Voltage Devices**

| Nonbattery Backup | Battery Backup | Voltages |
|---|---|---|
| W4 | W4 | Decouple +5 |
| W5 | W5 | Decouple +5 |
| W9 | W12 | +5 CR |
| W13/W15 | W14 | +5 VDD |

**Bus Grant Continuity Jumpers**

To install W1 and W2 in your system, identify the backplane bus structure as AB/AB or AB/CD. The jumpers are installed for an AB type backplane and removed for a CD type backplane as described below.

**Bus Grant Continuity**

| Backplane | Bus Type | W1 | W2 |
|---|---|---|---|
| H9270 (4 slot backplane) | AB/AB | IN | IN |
| H9275 (9 slot backplane) | AB/AB | IN | IN |
| H9273 (4 slot backplane) | AB/CD | OUT | OUT |
| H9276 (9 slot backplane) | AB/CD | OUT | OUT |

### General Jumpers

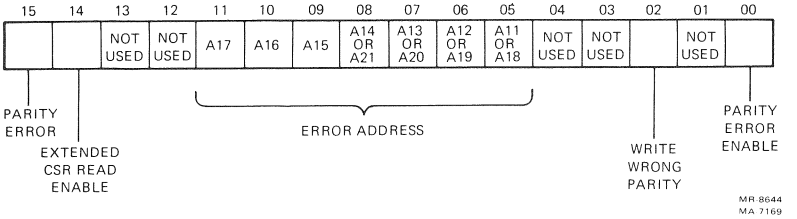
The general jumper group and their functions that have not yet been covered are described below.

**General Jumpers**

| Pin Numbers | Function |
|---|---|
| 6 to 7 | In - write wrong parity |
| 8 to 7 | In - disables wrong parity |
| 2 to Y | 2 to Y out - 22-bit machine<br>2 to Y in - 18-bit machine |
| 43 to 44 | In - single voltage MOS RAM access time (150 ns device) |
| 45 to 44 | In - multiple voltage MOS RAM access time (200 ns device) |
| 22 to 23 | Not used |
| 21 to 23 | Not used |
| F to H | F to H in - connected to force the starting address to 16K<br>F to H out - disables force function |
| 3 to 9 | 3 to 9 in - connected on 16K and 64K MOS chip |
| 13 to 15 | Connected on 16K and 64K MOS chip |
| 4 to 10 | Connected only on 64K MOS chip |
| 14 to 16 | Connected only on 64K MOS chip |

## CONTROL STATUS REGISTER (CSR) BIT ASSIGNMENT

The control status register (CSR) in the MSV11-P allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared by assertion of BUS INIT L. The CSR bit assignments are as follows.




(CSR) Bit Assignment

**CSR Bit Descriptions**

| Bit | Name | Description |
|---|---|---|
| 15 | Parity error | This bit set indicates that a parity error has occurred. The bit then turns on a red LED on the module. This provides visual indication of a parity error.<br><br>Bit 15 is a read/write bit. It is reset to zero via power-up or BUS INIT and remains set unless rewritten or initialized. |
| 14 | Extended CSR read enable | The use of this bit is explained in the error address description.<br><br>Bit 14 = 0, always for 128K word machine<br><br>Bit 14 = 0, first read on 2048K word machine<br><br>Bit 14 = 1, second read on 2048K word machine |
| 13, 12 | Not used | |

CSR Bit Descriptions (Cont)

| Bit | Name | Description |
|---|---|---|
| 11-05 | Error address | If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 05-11 and bits A18-A21 are latched. The 128K word machines (18-bit address) require only one read of the CSR register to obtain the failed address bits. CSR bit 14 = 0 allows the logic to pass A11-A17 to the LSI-11 bus. A 2048K word machine (22-bit address) requires two reads. The first read CSR bit 14 = 0 sends contents of CSR bits 05-11. Then the program must set CSR bit 14 = 1. This enables A18-A21 to be read from CSR bits 05-08.<br><br>The parity error addresses locate the parity error to a 1K segment of memory. These are read/write bits and are not reset to zero via power-up or BUS INIT. If a second parity error is encountered, the new failed address is stored in the CSR. |
| 04, 03 | Not used | |
| 02 | Write wrong parity | If this bit is set equal to 1 and a DATO or DATOB cycle to memory occurs, wrong parity data is written into the parity MOS RAMs. This bit can be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable.<br><br>1. With bit 02 set, writes entire memory with any pattern.<br><br>2. Read first location in memory, if bit 00 of the CSR is set, then a parity error indication is detected on the LSI-11 bus, and the failed address (location 0) is stored in the CSR.<br><br>3. Reads the CSR and obtains the failed address; CSR bit 14 = 0 implies A11-A17 on CSR bits 05-11. CSR bit 14 = 1 implies A18-A21 on CSR bits 05-08. Bit 02 is a |

**CSR Bit Descriptions (Cont)**

| Bit | Name | Description |
|---|---|---|
| | | read/write bit reset to zero on power-up or BUS INIT. |
| 01 | Not used | |
| 00 | Parity Error Enable | If a parity error occurs on a DATI or DATIO(B) cycle to memory, and bit 00 is set equal to 1, then BDAL 16 L and BDAL 17 L are asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power-up or BUS INIT. |

# MXV11-AA,AC MULTIFUNCTION MODULE

The MXV11 is a multifunction option module used for the LSI-11, LSI-11/2, or LSI-11/23 systems. It contains read/write memory provisions for read-only memory, two asynchronous serial line interfaces and a 60 Hz clock derived from a crystal oscillator.

Detailed technical information is beyond the scope of this document. Additional information can be found in the *Microcomputer Processor Handbook*, EB-18451-20.

## Model Designations

- MXV11-AA contains 8K bytes of random access memory.
- MXV11-AC contains 32K bytes of random access memory.

Both models have two 24-pin sockets that provide for +5 V read-only memories in which 1K × 8, 2K × 8, or 4K × 8 ROMs may be used. These sockets may also be used for 256 words of bootstrap code.

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | BC20M-XX |
| 1.2 | 0.1 | 2 | 2 | BC20N-XX (Refer to DLV11-KA) |
| | | | | BC21B-XX |

## Standard Addresses

RAM - Starts on any 8K boundary below 64KB.

| SLU | Channel 0 | Channel 1 |
|---|---|---|
| | 176500 | 177560 |

To disable RAM

MXV11-AC = Remove W4
MXV11-CA = Remove W5

### Standard Vectors

| | | |
|---|---|---|
| SLU | 300 | 60 |

### Diagnostic Programs

Refer to Appendix A.
Requires wraparound connectors to completely exercise SLU.

### Related Documentation

*MXV11-A Memory and Asynchronous Serial Line Interface User Guide (M8047)* (EK-MXV1A-UG)
Field Maintenance Print Set (MP-00730)

### Options

MXV11-A2 Boot ROMs for RX02, RX01, or TU58
PNs: 23-131F3-00, 23-132F3-00

### ROMs

Power: +5 V ± 5%

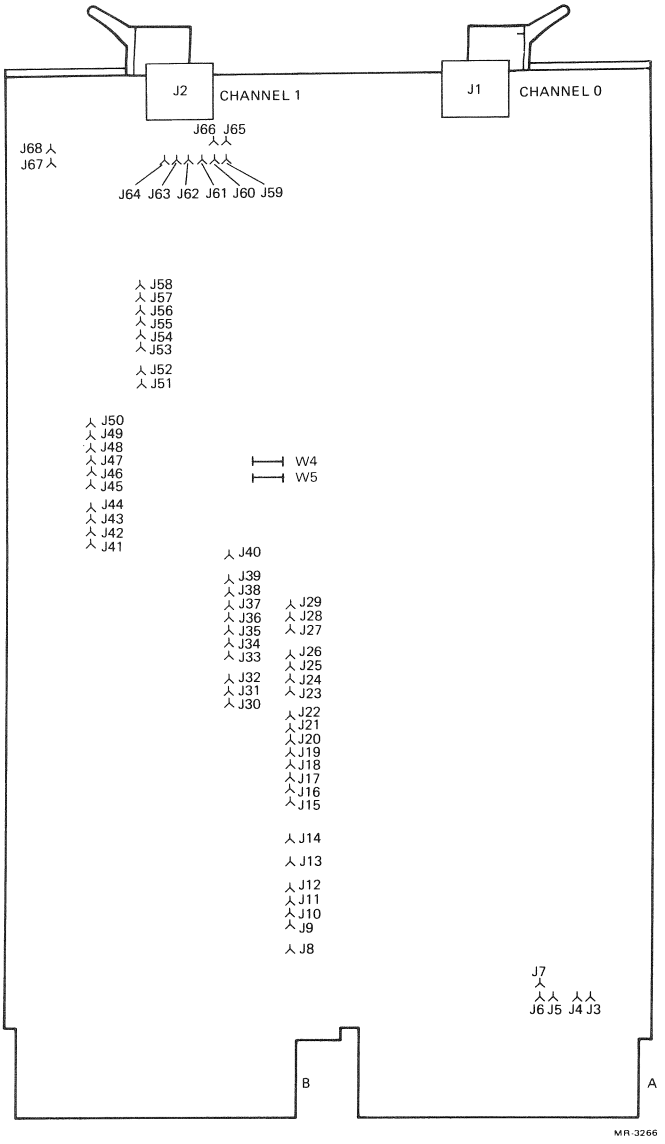
Pins: 24-Pin DIP

Access Time: Up to 450 nanoseconds

Array Size: 1K × 8, 2K × 8, or 4K × 8 bits

Type: Typical PROM types:

| UV PROMs | Chip Array Size | Memory Size |
|---|---|---|
| Intel 2758 | 1K × 8 bits | 1K words |
| Intel 2716 | 2K × 8 bits | 2K words |
| Intel 2732 | 4K × 8 bits | 4K words |
| Mostek MK2716 | 2K × 8 bits | 2K words |
| T.I. TMS 2516 | 2K × 8 bits | 2K words |
| T.I. TMS 2532 | 4K × 8 bits | 4K words |
| **Bipolar PROMs** | | |
| Intel 3628 | 1K × 8 bits | 1K words |
| Signetics 82S 2708 | 1K × 8 bits | 1K words |
| Signetics 82S 181 | 1K × 8 bits | 1K words |
| Signetics 82S 191 | 2K × 8 bits | 2K words |




MXV11-A Jumper Locations

**MXV11-A Jumper Functions**

| Pin | Function | Option |
|---|---|---|
| J3 | Clock L. Open collector output of the clock. Connected to pin AF1 (SSpare 2). Wirewrap to J4 to implement the clock option. | 60 Hz |
| J4 | BEVNT L. Event interrupt (pin BR1) used for the clock option. | 60 Hz |
| J5 | BDCOK H. DCOK (pin BA1) when high allows the processor to operate; when low initializes the system. Connected to J6 to use the boot option. | Boot |
| J6 | Framing Error. Open collector output of framing error from serial line one. Connected to pin AE1 (SSpare 1). Wirewrap to J5 to implement the boot option. Reset by bus initialize or reception of a valid character. | Break |
| J7 | BHALT L. Halt (pin AP1) when low will stop program execution and cause the processor to enter ODT microcode. Connected to J6 to implement the halt option. | Halt |
| J8 | GND. A ground signal that can be used to disable ROM by wirewrapping to J21 or to disable a serial line by wirewrapping to an address input pin (J23 or J24 for serial line 0; or J25, J26, J27, or J28 for serial line 1). | ROM |
| J9 | A13 L. Address bit 13 asserted low. Wirewrap to J11 to select bank 1 with the ROM address decoder. | ROM |
| J10 | A13 H. Address bit 13 asserted high. Wirewrap to J11 to select bank 0 with the ROM address decoder. | ROM |
| J11 | A13 M. Address bit 13 input to the ROM address decoder. See J9 and J10. Used only if J20 is wirewrapped to J21. | ROM |
| J12 | A03 H. Address bit 03 asserted high. Wirewrapped to the serial line address decoders (J23 or J24 for serial line 0, J25, J26, J27 or J28 for serial line 1) when address bit 03 is to be decoded as a 1. | SLU |

MXV11-A Jumper Functions (Cont)

| Pin | Function | Option |
|---|---|---|
| J13 | A04 H. Address bit 04 asserted high. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 1. | SLU |
| J14 | A05 H. Address bit 05 asserted high. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 1. | SLU |
| J15 | A09 H. Address bit 9 asserted high. Wirewrapped to the serial line one address decoder when address bit 09 is to be decoded as a 1. | SLU |
| J16 | A09 L. Address bit 09 asserted low. Wirewrapped to the serial line one address decoder when address address bit 09 is to be decoded as a 0. | SLU |
| J17 | A05 L. Address bit 05 asserted low. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 0. | SLU |
| J18 | A04 L. Address bit 04 asserted low. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 0. | SLU |
| J19 | A03 L. Address bit 03 asserted low. Wirewrapped to the serial line address decoders when address bit 03 is to be decoded as a 0. | SLU |
| J20 | ROM address. Output of the ROM address decoder. Connected to J21 when ROM is to be used in bank 0 or bank 1. | ROM |
| J21 | ROM select. ROM address selection enable asserted high. Wirewrapped to J8 (GND) to disable ROM, to J20 for bank 0 or bank 1, or to J22 for bootstrap. | ROM |
| J22 | Boot address. Output of the bootstrap address decoder. Connected to J21 when ROM is to be used in the bootstrap range from 173000-173776 (773000-773776 for LSI-11/23). | BOOT |
| J23 | Serial line 0 address decoder input asserted high. May be wirewrapped to A03 H (J12), A03 L (J19), A04 H (J13), or A04 L (J18). | SLU |

**MXV11-A Jumper Functions (Cont)**

| Pin | Function | Option |
|---|---|---|
| J24 | Serial line 0 address decoder input asserted high. May be wirewrapped to A03 or A04, whichever bit is not wired to J23. May be wirewrapped to GND (J8) to disable serial line 0. | SLU |
| J25-J28 | Serial line 1 address decoder input asserted high. Four address decoder inputs to be connected to address bits A03, A04, A05, and A09. Whether the high or low assertion state of a bit is wirewrapped to an input determines if that bit is decoded as a 1 or a 0. See J12 through J19. May be wirewrapped to GND (J8) to disable serial line 1. | SLU |
| J29 | ROM address bit 09 input. Wirewrapped to A09 H (J15) for normal ROM addressing and also for the MXV11-A2 option when the TU58 bootstrap is desired. Wirewrapped to A09 L (J16) for the MXV11-A2 option when the disk bootstrap is desired. | ROM |
| J30-J32 | RAM starting address selection. These pins are wirewrapped to J33 (logic 0) or J34 (logic 1) to select the RAM starting address (see the following). | RAM |
| J33 | GND. Logic 0 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets. | RAM, ROM |
| J34 | +3 V. Logic 1 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets. | RAM, ROM |

| J32 | J31 | J30 | Bank | Starting Address |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 000000 |
| 0 | 0 | 1 | 1 | 020000 |
| 0 | 1 | 0 | 2 | 040000 |
| 0 | 1 | 1 | 3 | 060000 |
| 1 | 0 | 0 | 4 | 100000 |
| 1 | 0 | 1 | 5 | 120000 |
| 1 | 1 | 0 | 6 | 140000 |
| 1 | 1 | 1 | 7 | 160000 |

**MXV11-A Jumper Functions (Cont)**

| Pin | Function | Option |
|---|---|---|
| J35 | A12 H. Address bit 12 asserted high. Used for addressing 4K × 8 bit ROMs. Wirewrapping to J37, J38 or J39, depending on the ROM used. | ROM |
| J36 | A11 H. Address bit 11 asserted high. Used for addressing 2K × 8 and 4K × 8 bit ROMs. Wirewrapping to J37, J38, or J39, depending on the ROM. | ROM |
| J37 | Pin 18 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +13 V, to J35 for A12, or to J36 for A11. | ROM |
| J38 | Pin 19 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3 V, to J35 for A12, or to J36 for A11. | ROM |
| J39 | Pin 21 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3 V, to J35 for A12 to J36 for A11 or to J40 for +5 V. | ROM |
| J40 | +5 V. Used to power some ROMs on pin 21. | ROM |
| J41 | Used for 150 baud. Wirewrapped to J45 for serial line 0, to J46 for serial line 1. (See following table.) | SLU |
| J42 | Used for 1200 baud. | SLU |
| J43 | Used for 300 baud. | SLU |
| J44 | Used for 2400 baud. | SLU |
| J45 | Clock 0. The clock input for serial line 0 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50. | SLU |
| J46 | Clock 1. The clock input for serial line 1 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50. | SLU |
| J47 | Used for 4800 baud. | SLU |
| J48 | Used for 9600 baud. | SLU |

**MXV11-A Jumper Functions (Cont)**

| Pin | Function | Option |
|---|---|---|
| J49 | Used for 19.2K baud. | SLU |
| J50 | Used for 38.4K baud. | SLU |
| J51 | Vector 0. Vector enable for channel 0. Used to drive vector bits that pass the test: logic 1 for channel 0, and logic 0 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07. | SLU |
| J52 | Vector 1. Vector enable for channel 1. Used to drive vector bits that pass the test: logic 0 for channel 0 and logic 1 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07. | SLU |
| J53 | Vector bit 03. Selects how bit 03 is to be driven for interrupt vectors. Wirewrapped to J51 if a logic 1 for channel 0 and a logic 0 for channel 1; to J52 if a logic 0 for channel 0 and a logic 1 for channel 1; to J57 if a logic 0 for both channel 0 and channel 1; or to J58 if a logic 1 for both channel 0 and channel 1. | SLU |
| J54 | Vector bit 04. Selects how bit 04 is to be driven for interrupt vectors. Wirewrapped the same as J53. | SLU |
| J55 | Vector bit 05. Selects how bit 05 is to be driven for interrupt vectors. Wirewrapped the same as J53. | SLU |
| J56 | Vector bits 06 and 07. Selects how bits 06 and 07 are to be driven for interrupt vectors. Wirewrapped the same as J53. | SLU |
| J57 | GND. Logic 0 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 0 for both serial line channels. | SLU |
| J58 | +3 V. Logic 1 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 1 for both serial line channels. | SLU |

**MXV11-A Jumper Functions (Cont)**

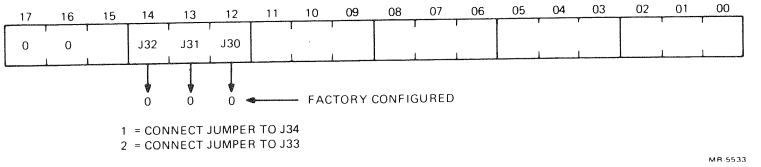
| Pin | Function | Option |
|---|---|---|
| J59 | Seven bits parity, eight bits no parity, channel 1. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity. | SLU |
| J60 | Two stop bits. Selects one or two stop bits for channel 1. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits. | SLU |
| J61 | Even parity. Selects odd or even parity for channel 1 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to ground (J56) for odd parity or to +3 V (J66) for even parity. | SLU |
| J62 | Seven bits parity, 8 bits no parity, channel 0. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity. | SLU |
| J63 | Two stop bits. Selects one or two stop bits for channel 0. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits. | SLU |
| J64 | Even parity. Selects odd or even parity for channel 0 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to logic 0 (J65) for odd parity or to logic 1 (J66) for even parity. | SLU |
| J65 | Logic 0. Ground signal used for configuring serial line interfaces. | SLU |
| J66 | Logic 1. +3 V signal used for configuring line interfaces. | SLU |
| J67 | Clock in. Clock input for baud rates, memory refresh and negative voltage generator. Wirewrapped to J68. Not a user option. | SLU |
| J68 | Clock out. Crystal oscillator output at 19.6608 MHz. Wirewrapped to J67. Not a user option. | SLU |

## Standard Factory Configuration

| Function | Wirewrap From | Pins To | Wirewrap Level |
|---|---|---|---|
| RAM Bank 0 | J30 | J31 | L1 |
| | J32 | J33 | L1 |
| | J31 | J32 | L2 |
| SLU Channel 0 Address 176500 | J23 | J18 | L1 |
| | J24 | J19 | L1 |
| SLU Channel 1 Address 177560 | J28 | J19 | L2 |
| | J26 | J15 | L1 |
| | J25 | J14 | L1 |
| | J27 | J13 | L1 |
| ROM Bootstrap (TU58) | J37 | J38 | L1 |
| | J21 | J22 | L1 |
| | J34 | J37 | L2 |
| | J33 | J39 | L2 |
| | J29 | J15 | L2 |
| SLU Vectors CH0 (300) | J53 | J57 | L1 |
| CH1 (60) | J54 | J52 | L1 |
| | J56 | J51 | L1 |
| | J54 | J55 | L2 |
| SLU Parameters (8 Data Bits, | J59 | J61 | L1 |
| No Parity, 1 Stop Bit) | J62 | J64 | L1 |
| | J60 | J63 | L1 |
| | J61 | J62 | L2 |
| | J59 | J66 | L2 |
| | J63 | J65 | L2 |
| Baud Rates CH0 (38.4K) | J45 | J50 | L1 |
| CH1 (9600) | J46 | J48 | L1 |
| Break Generation (Halt Option) | J6 | J7 | L1 |
| Crystal Clock | J68 | J67 | L1 |

**Configuring the RAM**
The RAM can be configured to start on any 8KB boundary below 64KB. Because of this restriction, the MXV11 (8KB version) is not usable for memory above 56KB. The MXV11 can be used in 18-bit memory address systems, but it is restricted to being assigned to the memory area at or below 56KB.

Five wirewrap terminals, J30 through J34, select the starting address. The following figure shows the jumper configurations required to obtain the desired starting addresses.



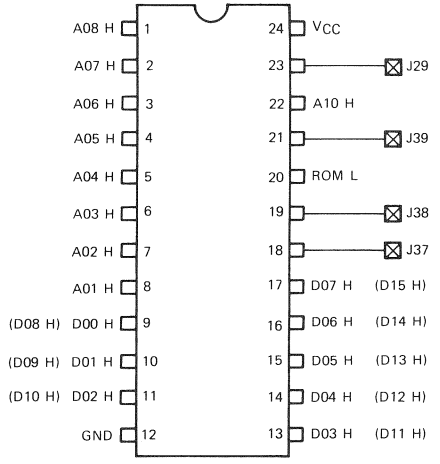

RAM Starting Address Selection

**Configuring the ROM**
Depending on the ROM type, the module's capacity is 1K, 2K, or 4K words using a pair of 1024 × 8-, 2048 × 8-, or 4096 × 8-bit ROMs respectively. The user configures jumpers on the module for the ROM type being used. The actual procedure for loading data into EPROMs, PROMs (or writing specifications for masked ROMs) will vary depending on the manufacturer, and is beyond the scope of this section. The user must refer to the manufacturer's data sheets and to the chapter, "Using PROMs" in the *Microcomputer Processor Handbook*, EB-18451-20. The user must be aware of the relationship of the EPROM, PROM, or ROM pins to the LSI-11 data bits, and the relationship of the pins to the memory address bits. Refer to the following figure for ROM socket pin assignments. All ROMs used on the MSV11-A must conform to these pin assignments.

The factory configuration allows for using the MSV11-A2 bootstrap ROMs.

**Configuring the Bootstrap ROM** – The ROM can be configured to operate in the I/O page to support bootstrap programs. The address area contains 256 words from 173000 to 173776 (773000 to 773776 for the LSI-11/23).

The MXV11-A is configured at the factory to allow for using the MXV11-A2 TU58 bootstrap. To reconfigure the MXV11-A to use the disk bootstrap, remove jumper J29 to J15 and install jumper J29 to J16.




MXV11-A ROM Socket Pin Assignment

**ROM Bank Selection –** If the MXV11-A sockets are used for program ROM instead of a bootstrap ROM, the memory must be selected by a jumper connecting J20 to J21. When main ROM memory is selected, the entire 4K word bank is enabled. If a 1K or 2K ROM is used, it will "wraparound" and give invalid data, depending on how the address lines are configured when the nonexisting ROM area is addressed. Main memory may be positioned in bank 0 or bank 1. To position the ROM in bank 0, jumper J10 to J11. To position the ROM in bank 1, jumper J9 to J11.

**Configuring the Specific ROM Types –** Additional jumpers must be connected depending on the type of ROM used. The "EPROM Address Jumpers" table describes the jumper configuration when using typical ROMs such as the Intel 2716 (2K × 8) or 2732 (4K × 8) EPROMs. The user must refer to the manufacturer's data sheets when configuring jumpers for other ROM types.

The function of wirewrap pins J29, J38, J37, and J39 are shown in the following table. These pins are to be connected as required to pins J33 through J40.

**ROM Upgrade Part Numbers**

23-131F3-00
23-132F3-00

**EPROM Address Jumpers**

| Function | From | 2716 ROM Bank 0 to | 2716 ROM Bank 1 to | 2732 ROM Bank 0 to | 2732 ROM Bank 1 to |
|---|---|---|---|---|---|
| Bank Enable | J20 | J21 | J21 | J21 | J21 |
| Bit 09 Input | J29 | J15 | J15 | J15 | J15 |
| Address or Enable | J38 | J36 | J36 | J36 | J36 |
| Address or Enable | J37 | J33 | J33 | J35 | J35 |
| Address or Enable | J39 | J40 | J40 | J33 | J34 |

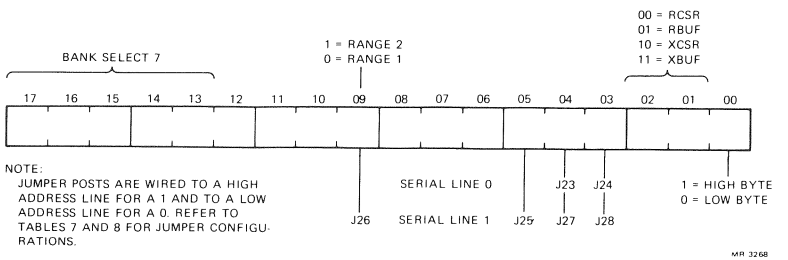
## CONFIGURING THE SERIAL LINE UNITS

### Serial Line Register Address Selection

Four device registers (RCSR, RBUF, XCSR, and XBUF) are provided for each of the two serial lines. Jumpers are configured to establish separate base addresses for each serial line as shown.

- Serial port 0 may be assigned to one of the four starting addresses: 176500, 176510, 176520, 176530.
- Serial port 1 may be assigned addresses in two ranges. The first range starts at 176500 and covers the eight starting addresses from 176500 to 176570. The second range starts at 177500 and also contains eight possible starting addresses, including the standard console address, 177560. Since several other standard DIGITAL devices use addresses in this second range, it is recommended that only the console address be used.

The format of an SLU address is shown in the following figure. Note that bits 13-17 are neither configured nor decoded by the MXV11-A module. These bits are decoded by the bus master module as the bank 7 select (BBS7 L) bus signal. This signal becomes active only when the I/O page is accessed. Bit 0 is used as the byte pointer.




MXV11-A SLU Address Format

Bits 1 and 2 select one of the four device registers within the addressed serial line. Bits 3 and 4 are used to select one of four possible device addresses for serial line 0. Bits 3, 4, 5, and 9 are used to select the device addresses in two ranges for serial line 1 (console). The following table describes the jumper combinations to select one of four device addresses for serial line 0 (I/O).

**Serial Line 0 Address Jumpers**

| Address (Octal) | Jumper Posts J23 to | J24 to |
|---|---|---|
| 176500 | J18 (Logic 0) | J19 (Logic 0) Factory Configuration |
| 176510 | J18 (Logic 0) | J12 (Logic 1) |
| 176520 | J13 (Logic 1) | J19 (Logic 0) |
| 176530 | J13 (Logic 1) | J12 (Logic 1) |

**NOTE**

| Logic 1 | Logic 0 |
|---|---|
| J13 (A04 H) | J18 (A04 L) |
| J12 (A03 H) | J19 (A03 L) |

Serial line 1 may have 16 possible device addresses in two ranges. The following table describes the jumper combinations to select the eight device registers available in range 1. Only one device address is used in range 2.

**Serial Line 1 Address Jumpers**

| Address (Octal) Range 1 | Jumper Posts J26 to | J25 to | J27 to | J28 to |
|---|---|---|---|---|
| 176500 | J16 | J17 | J18 | J19 |
| 176510 | J16 | J17 | J18 | J12 |
| 176520 | J16 | J17 | J13 | J19 |
| 176530 | J16 | J17 | J13 | J12 |
| 176540 | J16 | J14 | J18 | J19 |
| 176550 | J16 | J14 | J18 | J12 |
| 176560 | J16 | J14 | J13 | J19 |
| 176570 | J16 | J14 | J13 | J12 |
| **Range 2** | | | | |
| 177560 | J15 | J14 | J13 | J19 |

(See the following Note.)

**NOTE**

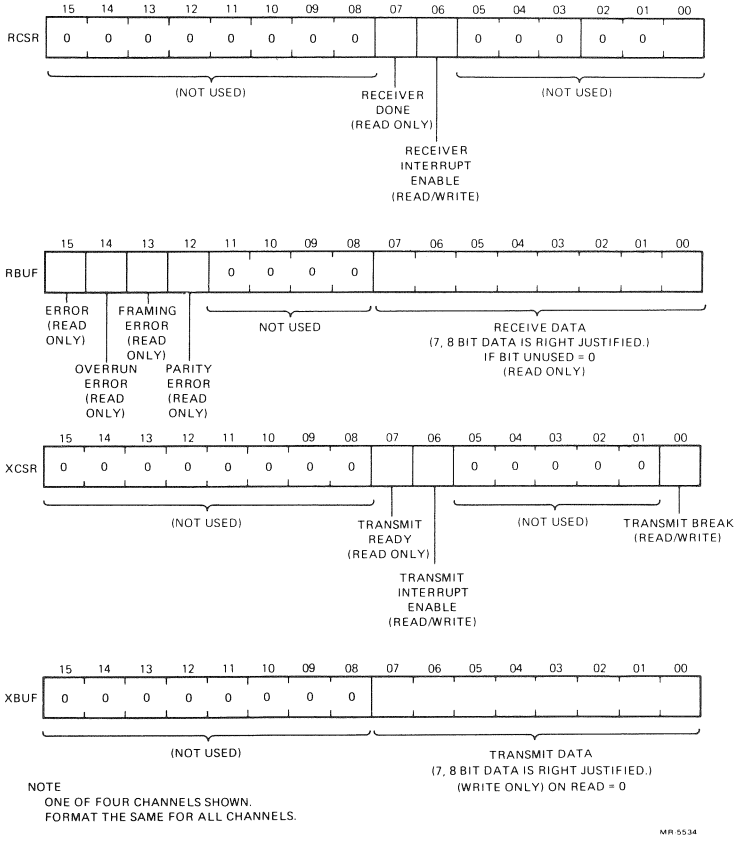
**Factory configurations use only one address in range 2 to avoid possible device conflicts. The remaining addresses are pre-assigned to other devices.**

| Logic 1 | Logic 0 |
|---|---|
| J15 (A09 H) | J16 (A09 L) |
| J14 (A05 H) | J17 (A05 L) |
| J13 (A04 H) | J18 (A04 L) |
| J12 (A03 H) | J19 (A03 L) |

### Control/Status Register

The MXV11-A has two control/status registers (CSRs) for each of its two serial line units. The following figure shows the control/status registers and the read/write data registers. Transmitter control/status registers 0 and 1 (XCSR0 and 1) and receiver control/status registers 0 and 1 (RCSR0 and 1) operate with serial lines 0 and 1, respectively.

Both serial line units have the same bit assignments. There are four registers for each serial line. They are sequential in this order: 0, receiver status; 2, receiver data; 4, transmitter status; and 6, transmitter data. All unused bits are read as 0.




MXV11-A SLU CSR Formats

**Bit Assignments for the Receiver Status Register**

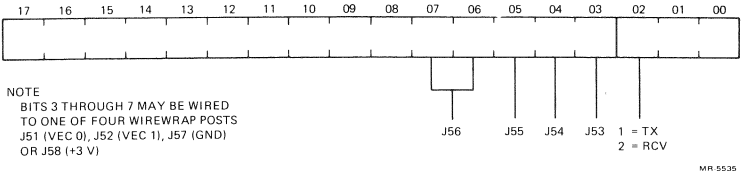
| Bit | Function |
|---|---|
| 6 | Interrupt enable, read/write. A 1 enables receiver interrupts, a 0 disables interrupts. Cleared by initialize. |
| 7 | Receiver done, read only. A 1 indicates that the serial interface has received a character. If enabled by bit 6, receiver done will request an interrupt. Receiver done is cleared by reading the receiver data register or by initialize. |
| 0-7 | Data bits, read only. Bit 0 is the least significant bit and bit 7 is the most significant. If seven data bits plus parity is selected, bit 7 will always read as a 0. |
| 12 | Parity error, read only. A 1 indicates that the word being read in bits 0 through 6 has a parity error. Bit 12 will always read 0 when eight data bits and no parity are selected. Cleared when read, or by initialize. |
| 13 | Framing error, read only. A 1 indicates that a start bit was detected, but there was no corresponding stop bit. A framing error will be generated when a break is received. Cleared when read, or by initialize. |
| 14 | Overrun error, read only. A 1 indicates that a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read, or by initialize. |
| 15 | Error, read only. A 1 indicates that one or more of bits 12, 13, and 14 are 1. Cleared when read, or by initialize. |

**Bit Assignments for the Transmitter Status Register**

| Bit | Function |
|---|---|
| 0 | Break, read/write. When set to a 1, bit 0 causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by writing a 0, or by bus initialize. |
| 6 | Interrupt enable, read/write. A 1 enables transmitter interrupts; a 0 disables interrupts. Cleared by initialize. |
| 7 | Transmitter ready, read only. A 1 indicates that the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready will request an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by initialize. |
| 0-7 | Data bits, write only. Bit 0 is the least significant bit and bit 7 is the most significant bit. If seven data bits plus parity are selected, bit 7 will not be transmitted. The transmitter data register will read all 0s. |

**Interrupt Vector Selection**

Two consecutive interrupt vectors (one for receive and one for transmit) are provided for each of the two serial lines. The interrupt vector format is shown in the following figure. Each SLU port can be independently configured to operate in one of two ranges: 000 to 074, or 300 to 376.




MXV11-A Interrupt Vector Format

The following table lists the vector addresses that may be assigned to the serial lines. Note that all vector addresses in the 000 to 074 range, except 060, are reserved vector locations. The jumper selectable bits are 3 through 7. Bits 6 and 7 are wired together.

**Serial Line Vector Addresses**

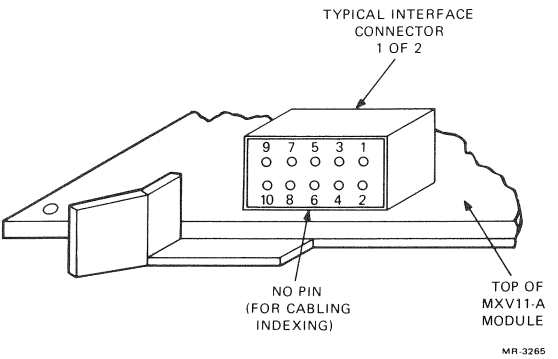
| Serial Line 1 (Console) | Serial Line 0 (I/O) |
|---|---|
| 000 | 300 |
| 010 | 310 |
| 020 DIGITAL Reserved | 320 |
| 030 Do not use | 330 |
| 040 | 340 |
| 050 | 350 |
| 060 Console | 360 |
| 070 DIGITAL Reserved | 370 |

The following example illustrates the procedure for configuring the vector addresses. Assume that 60 is the address for serial line 1 (console) and 310 is the address for serial line 0 (I/O). The example describes the relationship between the vector bases, vector address bits, and the jumper posts. The jumpers are configured using the following four rules.

1. If a bit = 1 in both vector bases, it is tied to J58 (logic 1).
2. If a bit = 0 in both vector bases, it is tied to J57 (logic 0).
3. If a bit = 1 for serial line 1 and a 0 for serial line 0, it is tied to J52 (vector 1).
4. If a bit = 0 for serial line 1 and a 1 for serial line 0, it is tied to J51 (vector 0).

### Interface Connector Pins

Two 10-pin connectors (one for each serial line) are provided on the MXV11-A module. Connector pins and signal functions are described in the following table and shown in the following figure.




MXV11-A Connector Pins

**MXV11-A I/O Connector Pin Functions**

| Pin | Signal | Function |
|---|---|---|
| 1 | UART CLOCK | The baud rate clock appears on this pin. When an internal baud rate is selected, this pin is a TTL output. When no baud rate is selected on the module, this is an external baud rate input. The high level for the clock > 3.0 V. |
| 2 | GND | |
| 3 | XMIT+ | Transmitter output |
| 4 | GND | |
| 5 | GND | |
| 6 | NC | Key, pin not provided |
| 7 | RCV− | Receiver input most negative |
| 8 | RCV+ | Receiver input most positive |
| 9 | GND | |
| 10 | +12 V | Power for the DLV11-KA option |

**Current Loop**

The MXV11-A module can interface with 20 mA active or passive current loop devices when used with the DLV11-KA option. This option consists of a DLV11-KB (EIA to 20 mA current loop converter) and a BD21A-03 interface cable. The MXV11-A does not have the capability to support the reader-run portion of the DLV11-KA option. The DLV11-KA option is placed between the MXV11-A serial line output and the 20 mA current loop peripheral device.

**MXV11-A Interface Cables**

| Cable | Application | Length |
|---|---|---|
| BC21B-05 | EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5-pin AMP female to RS-232C male). | 1.5 m (5 ft) |
| BC20N-05 | EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5-pin AMP female to RS-232C female). | 1.5 m (5 ft) |
| BC20M-50 | EIA RS-422 or RS-423 cable for high-speed transmission (19.2K baud) (2 × 5-pin AMP female to 2 × 5-pin AMP female). | 15 m (50 ft) |
| BC05D-10 | Extension cable used in conjunction with BC21B-05. | 3 m (10 ft) |
| BC05D-25 | Extension cable used in conjuntion with BC21B-05. | 7.6 m (25 ft) |
| BC03M-25 | "Null modem" extension cable used in conjunction with BC21B-05. | 7.6 m (25 ft) |

**NOTE**

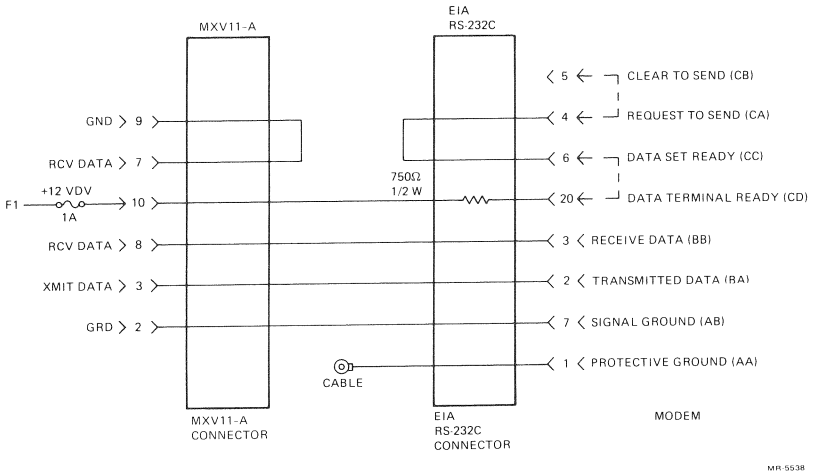
**"Strapped" logic levels are provided on Data Terminal Ready (DTR) and Request To Send (RTS) for operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).**

The MXV11-A may operate with several peripheral device cables and options for flexibility when configuring systems. A variety of cables and options, as well as the primary application of each, are shown with the MXV11-A.

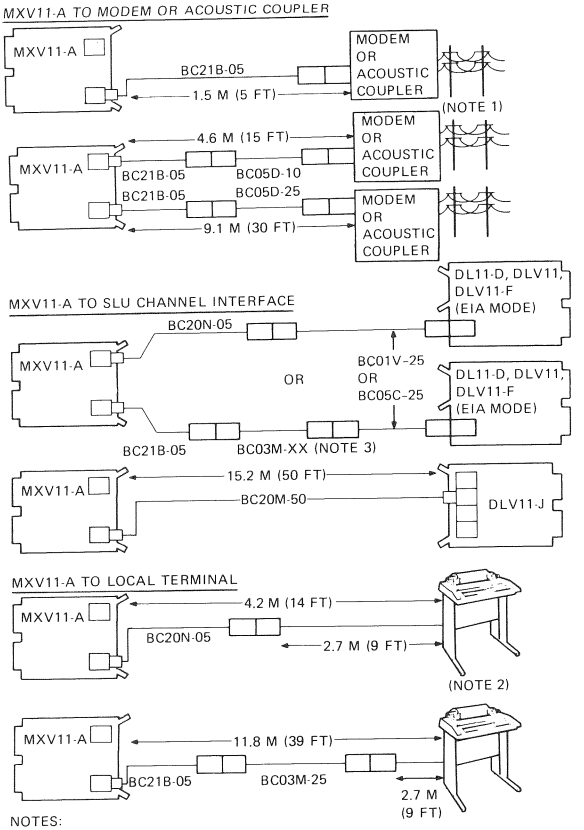
1. The receivers on the MXV11 have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, receive data (pin 7 on the 2 × 5-pin AMP connector) must be tied to signal ground (pins 2, 5, or 9) in order to maintain proper EIA levels (see the following figure).
2. To connect directly to a local EIA RS-232C terminal, it is necessary to use a null modem. To design the null modem into the cable, one must switch received data (pin 2) with transmitted data (pin 3) on the RS-232C male connector as shown in the following figure.

To mate to the 2 × 5-pin connector block, the following parts are needed:

| | |
|---|---|
| Cable Receptacle (QTY 1) | AMP PN 87133-5<br>DEC PN 12-14268-02 |
| Locking Clip Contacts (QTY 9) | AMP PN 87124-1<br>DEC PN 12-14267-00 |
| Key Pin (pin 6) (QTY 1) | AMP PN 87179-1<br>DEC PN 12-15418-00 |




B21B-05 Modem Cable

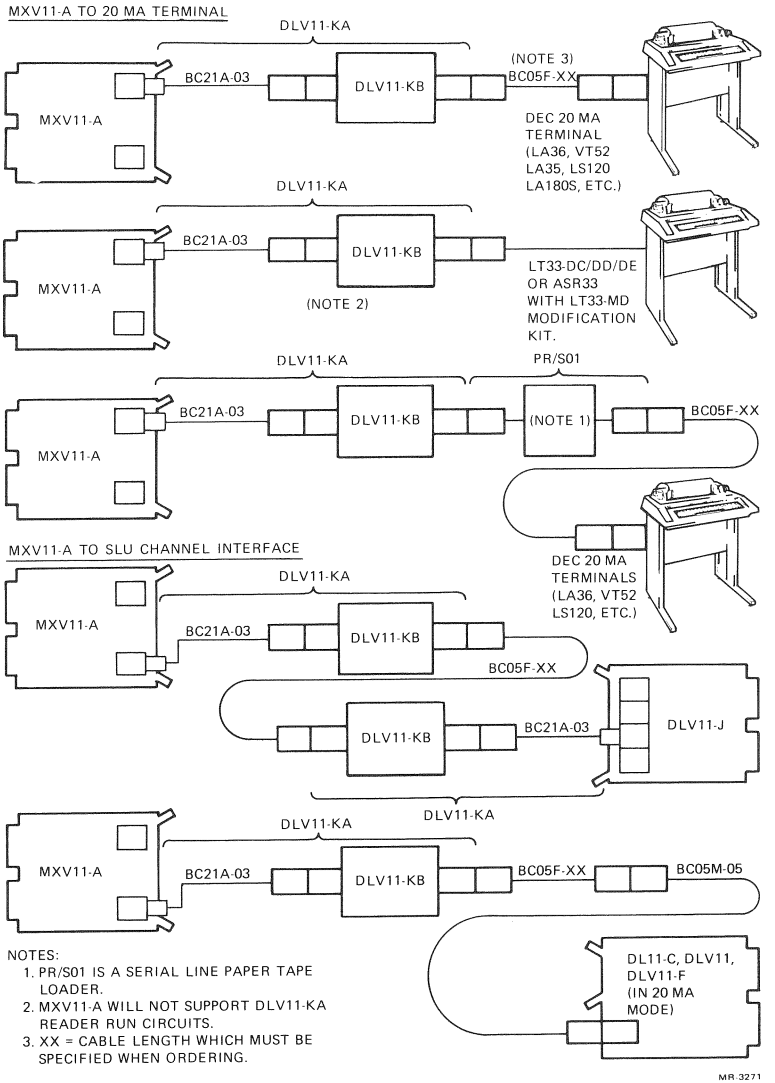



NOTES:

1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIS RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.
3. XX = CABLE LENGTH WHICH MUST BE SPECIFIED WHEN ORDERING.

MR-3270

MXV11-A EIA Cable Configurations




MXV11-A 20 mA Cable Configurations

# MXV11-B MULTIFUNCTION OPTION MODULE

## GENERAL

The MXV11-B is a multifunction option module used with the PDP-11/23 and KDJ11 processor systems. The MXV11-B read/write memory contains 128K bytes of dynamic MOS RAM without parity. The MXV11-B is configured from 64K SIPS (single inline package). Four SIPS provide 128K bytes (64K words) of memory storage. Battery backup is supplied when jumpers are configured to enable that feature and system supplied power is connected. This dual-height, multifunction module option can operate on a 22-bit Q-Bus system, (up to 316 words) on an 18- and 16-bit Q-Bus system unit.

### Features

W/R MOS RAM memory
5 V battery backup for MOS RAMs
Read only memory (ROM)
ROM window map logic (page control register)
Two asynchronous, serial line ports (SLU0 and SLU1)
Multiple LTC frequencies
LED diagnostic display register

### Electrical Specifications

**Power Requirements** – The following voltages are used by this module.

| Voltage | Tolerance | Pins |
|---|---|---|
| +5 V | ±5% | AA2 BA2, BV1 |
| +12 V | ±5% | AD2, BD2 |
| +5 VB | ±5% | AV1 |

Power dissipated in each power supply configuration is as follows.

**No battery backup**

| +5 V | | +12 V | |
|---|---|---|---|
| Typ | 17.25 W | Typ | 0.67 W |
| Max | 24.57 W | Max | 0.71 W |

**Battery backup configuration**

| +5 V | | +5 VB | | +12 V | |
|---|---|---|---|---|---|
| Typ | 12.90 W | Typ | 4.35 W | Typ | 0.67 W |
| Max | 15.95 W | Max | 8.60 W | Max | 0.71 W |

**Data retention mode**

VCC = 0 V, +12 V supply = 0

**+5 VB**

| | |
|---|---|
| Typ | 4.35 W |
| Max | 5.54 W |

**Related Documentation**

*MXV11-B Technical Manual* (EK-MXV1B-TM)
*MXV11-B User Guide* (EK-MXV1B-UG)
*MXV11-B2 ROM Set User Guide* (EK-MXVB2-UG)
*MXV11-B Multifunction Option Module User Guide* (EK-MXV1B-UG)
MXV11-B Field Maintenance Print Set (MP-01469-00)

**Program Options and Defaults**

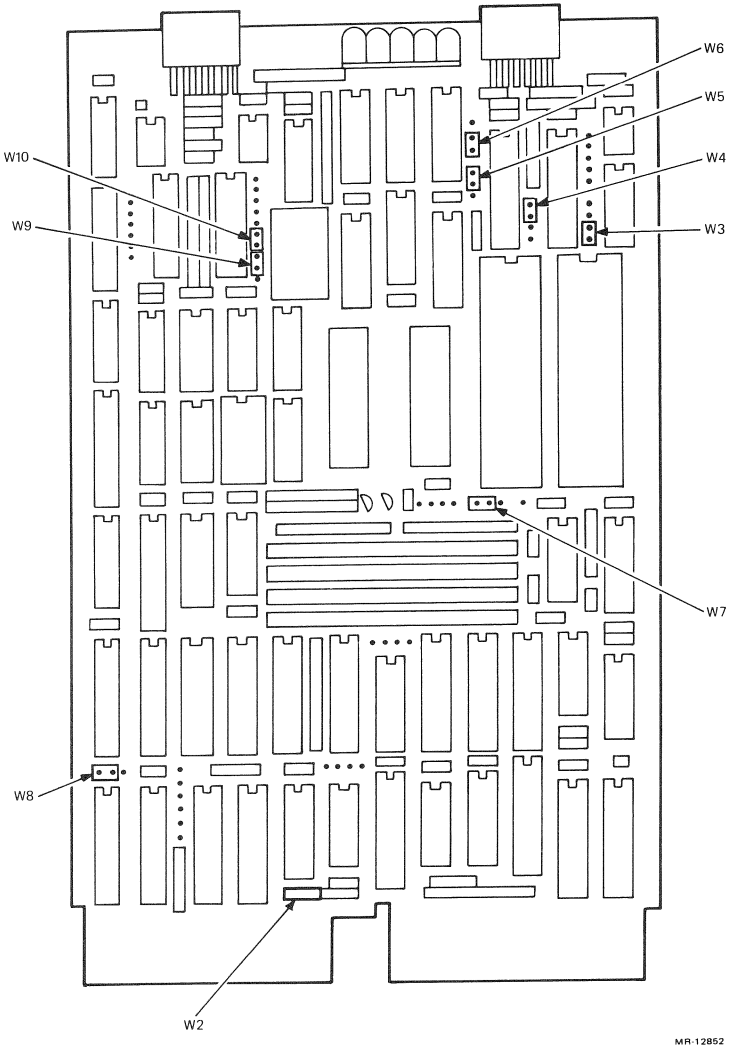
| | | Address/Vector |
|---|---|---|
| One MXV11-B | Channel 0 | 776500/300 |
| | Channel 1 | 777560/60 |
| Two MXV11-Bs | Channel 2 | 776510/310 |
| | Channel 3 | 776520/320 |

**Diagnostic Programs**

| | Test Functions |
|---|---|
| CVMX.BAO | Serial lines |
| | ROM |
| | Clock option |
| | Page Control Register (PCR) |
| | Diagnostic Display Register (DDM) |
| | Random Access Memory (RAM) |

**Default Jumpers**

*The default jumpers are as shown below.*




Default Configuration of Push-On Connectors

**Interface Connector Pins**

Two 10-pin connectors, one for each serial line, are provided on the MXV11-B module. The connector pins and signal functions are described below.

**MXV11-B I/O Connector Pin Functions**

| Pin | Signal | Function |
|---|---|---|
| 1 | BRCLK | Baud rate clock. This output provides a clock signal at a frequency of 16 times the selected baud rate. This pin is used as an output from the MXV11-B and does not accept external clock inputs. |
| 2 | Ground | |
| 3 | XMIT+ | Transmitter output |
| 4 | Ground | |
| 5 | Ground | |
| 6 | NC | Key, pin not provided |
| 7 | RCV– | Receiver input most negative |
| 8 | RCV+ | Receiver input most positive |
| 9 | Ground | |
| 10 | +12 V | Power for the DLV11-KA option |

Jumpers are used to configure:

| | |
|---|---|
| Console mode | Reboot |
| MXV11-B2 boot ROM set | Line time clock |
| System size | EVENT line |
| Boot and diagnostic ROMs | Software programmed baud rates |
| Clock | Battery |
| Halt | User-supplied ROMs |

**Baud Rates**

Each serial line can be software programmed or strapped to 300, 1200, 9600, or 38,400 baud and is compatible with EIA RS-423 or RS-232 signal levels.

When bit 06 is set, the BEVENT line clamp is removed and LTC is functional. The LTC address is 777546.

**CAUTION**

**There should be only one source drive on the BEVENT line in any system. On most systems, the system power supply provides the bevent signal. this source must be disabled if the mxv11-b is used to drive the line clock.**

This register is a write-only register, but generates a reply on DATIO and DATIO B lines. The DDR resides in location 777524 on the I/O page and is enabled when the MXV11-B has its boot and console functions enabled.

**Serial Line Unit Baud Rates**

| | | | SLU0 (See Note) | |
|---|---|---|---|---|
| | | J0B to GND (J10 to J9) | J0A to GND (J11 to J9) | Baud Rates |
| J11 | J0B | R | R | 300* |
| J10 | J0B | R | I | 1200 |
| J9 | GND | I | R | 9600 |
| | | I | I | 38.4K |

| | | | SLU1 (See Note) | |
|---|---|---|---|---|
| | | J1A to GND (J8 to J9) | J1B to GND J7 to J9) | Baud Rates |
| J9 | GND | R | R | 9600* |
| J8 | J1A | R | I | 38.4K |
| J7 | J1B | I | R | 300 |
| | | I | I | 1200 |

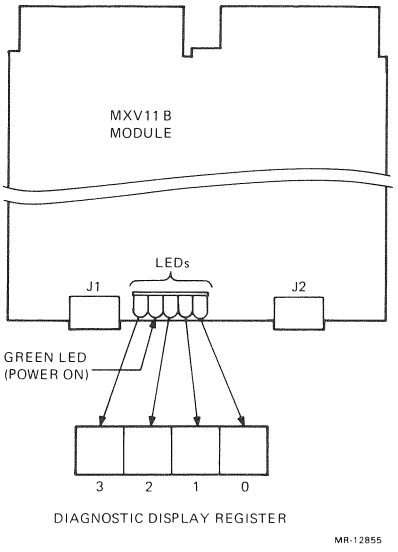
R = jumper removed
I = jumper inserted to ground
*Shipped configuration

**NOTE**

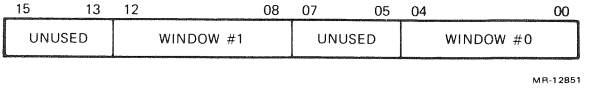
**SOFT EN to GND jumper (J14 to J13) must be removed; otherwise these jumpers have no effect. If the SOFT EN to GND jumper (J14 to J13) is installed and PBRE bit 1 is set, baud rates are software controlled.**

**LED Diagnostic Display Register**

The MXV11 has a diagnostic display register (DDR) which has four red LEDs to show system diagnostics and one green LED to indicate power-on.




MXV11-B Diagnostic Register (LEDs)



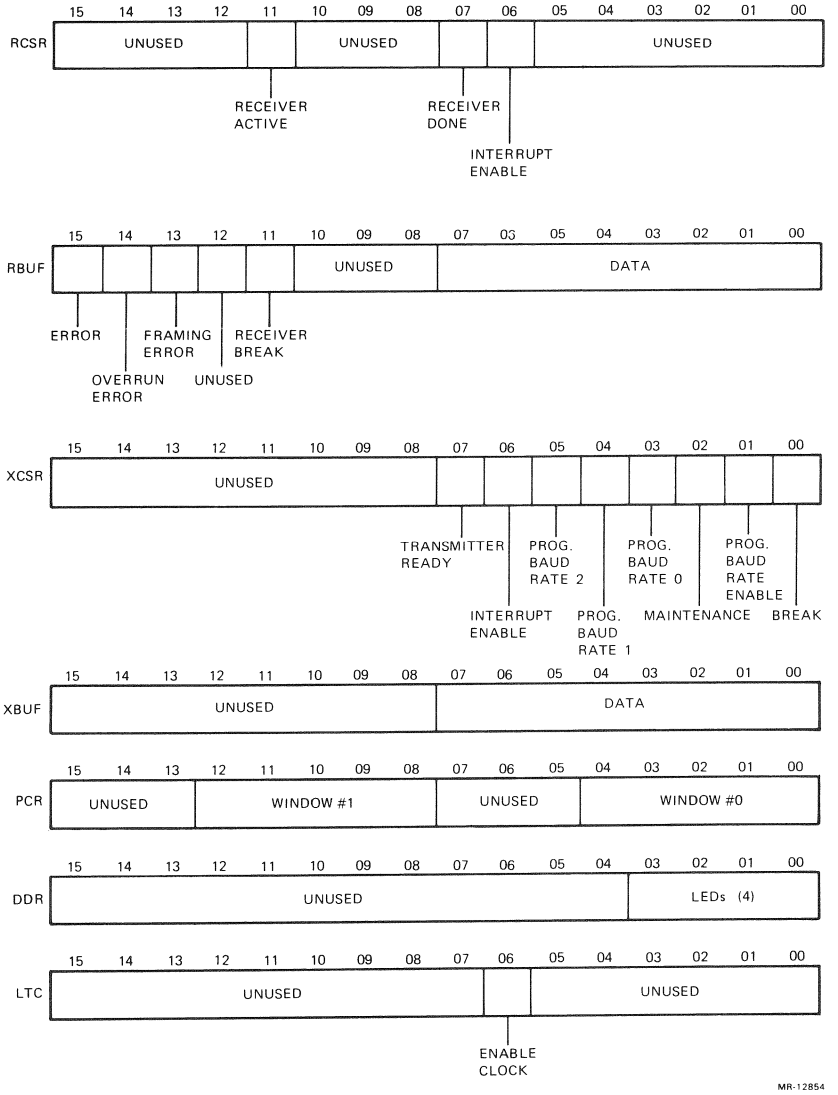

Page Control Register

**ROM Window Addresses for 16-, 18-, and 22-bit Q-Bus**

| Q-Bus | Window 1 Start Addr (octal) | End Addr (octal) | Window 0 Start Addr (octal) | End Addr (octal) |
|---|---|---|---|---|
| 16-bit | 165000 | 165777 | 173000 | 173377 |
| 18-bit | 765000 | 765777 | 773000 | 773377 |
| 22-bit | 17765000 | 17765777 | 17773000 | 17773377 |

**ROM Window Map**

| Window Field | Normalized 0 ROM Address | |
|---|---|---|
| 0 | 00000 | |
| 1 | 01000 | |
| 2 | 02000 | |
| 3 | 03000 | |
| 4 | 04000 | |
| 5 | 05000 | |
| 6 | 06000 | |
| 7 | 07000 | Maximum address for 2K by 8 PROM |
| 10 | 10000 | |
| 11 | 11000 | |
| 12 | 12000 | |
| 13 | 13000 | |
| 14 | 14000 | |
| 15 | 15000 | |
| 16 | 16000 | |
| 17 | 17000 | Maximum address for 4K by 8 PROM |
| 20 | 20000 | |
| 21 | 21000 | |
| 22 | 22000 | |
| 23 | 23000 | |
| 24 | 24000 | |
| 25 | 25000 | |
| 26 | 26000 | |
| 27 | 27000 | |
| 30 | 30000 | |
| 31 | 31000 | |
| 32 | 32000 | |
| 33 | 33000 | |
| 34 | 34000 | |
| 35 | 35000 | |
| 36 | 36000 | |
| 37 | 37000 | Maximum address for 8K by 8 PROM |




MXV11-B Register Bit Formats

**Receiver Status Register Bit Assignments (RCSR)**

| Bit | | Description |
|---|---|---|
| 15–12 | | Unused |
| 11 | RA<br>Receiver active<br>read only | A logic one indicates that the receiver is active. Set at the center of the start bit of the input serial data. Cleared at the expected center of the stop bit at the end of the time prior to the leading edge of RCV DONE. Also cleared by power up sequence. |
| 10–8 | | Unused |
| 7 | RD | A logic one indicates that the serial interface has received a character. If enabled by bit 6, receiver done requests an interrupt. Receiver done is cleared by reading the receiver data register or by power-up sequence. |
| 6 | IE<br>Interrupt enable<br>read/write | A logic one enables receiver interrupts; a zero disables interrupts. Cleared by initialization. |
| 5–0 | | Unused |

**Receiver Data Buffer Bit Assignments (RBUF)**

| Bit | | Description |
|---|---|---|
| 15 | ER<br>Error<br>read only | A logic one indicates that bit 13 and/or bit 14 is a one. Cleared when the bit is read or cleared by power-up sequence. |
| 14 | OE<br>Overrun error<br>read only | A logic one indicates a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read or by power-up sequence. |
| 13 | FE<br>Framing error<br>read only | A logic one indicates that a start bit was detected, but there was no corresponding stop bit. A framing error is generated when a break is received. Cleared when read or by power-up sequence. |
| 12 | | Unused |
| 11 | RB<br>Receiver break<br>read only | This bit is set when serial-in (SI) signal goes from a mark to a space and stays in the space condition for 11 bit times after serial reception starts. This bit is cleared when the SI signal returns to the mark condition, or by power-up sequence. |
| 10–8 | | Unused |
| 7-0 | DATA<br>read only | These eight bits hold the most recent byte received. When a new byte is transferred to the data buffer, the RCV DONE in the RCSR is set. Bit 0 is the LSB and bit 7 is the MSB. Cleared by power-up sequence. |

**Transmitter Status Register Bit Assignments (XCSR)**

| Bit | | Description |
|---|---|---|
| 15–8 | | Unused |
| 7 | TR<br>Transmitter read<br>read only | A logic one indicates the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready requests an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by power-up sequence. |
| 6 | IE<br>Interrupt enable<br>read/write | A logic one enables transmitter interrupts. A logic zero disables interrupts. Cleared by initialization. |
| 5–3 | BR2-BR0*<br>Programmable baud rate select<br>read/write | When PBR-bit 1 in XCSR is set, these baud bits determine the baud rate (set by software if SOFT jumper connected to GND). If SOFT jumper is connected to OPEN, baud rate is obtained via wire-wrap. Bits BR2-BR0 are cleared by PBR inhibit (SOFT EN) or by power-up sequence. |
| 2 | MAINT<br>Maintenance<br>read/write | This bit facilitates a maintenance self-test. When the bit is set, the the transmitter serial output is connected to the receiver serial input and the external serial input is disconnected. This bit is cleared by initialization. |

* Read only as a zero when programmable baud rate inhibit (PBRI) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper – J14–J15).

**Transmitter Status Register Bit Assigments (XCSR) (Cont)**

| Bit | | Description |
|---|---|---|
| 1 | PBR*<br>Programmable baud rate enable<br>Read/write when software programmable baud rates enabled (SOFT to GND jumper); else read only as 0. | This bit selects between internal and external baud rate selection. When set (enable), the baud rate is determined by the PBR2–0 bits in this register. When clear (inhibit), the baud rate is determined by the J1, J0 wire-wrap pins. This bit is cleared by power-up sequence or SOFT to OPEN jumper connected (programmable baud rate inhibit (J14 to J15). |
| 0 | BK<br>Break<br>read/write | When this bit is set, it causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by bus initialization. |

* Read only as a zero when programmable baud rate inhibit (PBRI) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper – J14–J15).

**Transmitter Data Buffer Bit Assignments (XBUF)**

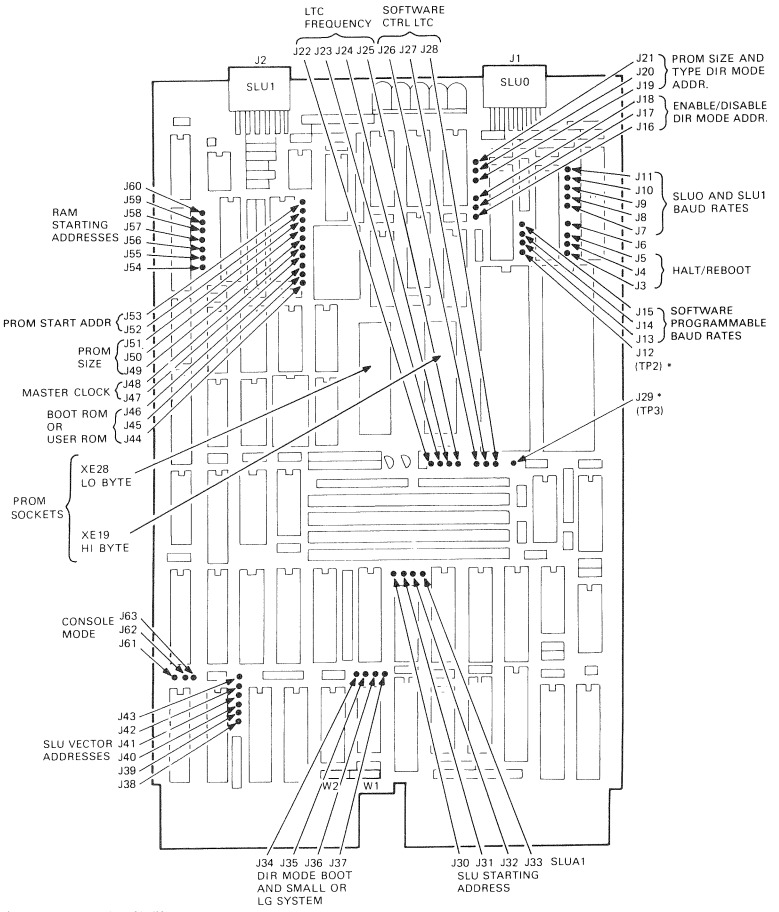
| Bit | | Description |
|---|---|---|
| 15–8 | | Unused |
| 7-0 | XMIT DATA BUFFER read/write | Transmitter data buffer – this byte register holds a copy of the most recent byte written into it. When a byte is written into this register, the transmit ready (TR) bit in the XCSR register is cleared. This byte is copied into the transmitter serial output register whenever that register is empty and the bit is clear. The TR bit is set when a byte is copied from the transmitter data buffer into the serial output register. Reading the contents of this register causes no other effect. Cleared by power-up sequence. |

**Definition of Cables**

| Cable | Application | Length |
|---|---|---|
| BC21B-05 | EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male) | 1.5 m (5 ft) |
| BC20N-05 | EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5 pin AMP female to RS-232C female) | 1.5 m (5 ft) |
| BC20M-50 | EIA RS-422 or RS-423 cable for high-speed transmission (19,200 baud) (2 × 5 pin AMP female to 2 × 5 AMP female) | 15 m (50 ft) |
| BC05D-10 | Extension cable used in conjunction with BC21B-05 | 3 m (10 ft) |
| BC05D-25 | Extension cable used in conjunction with BC21B-05 | 7.6 m (25 ft) |
| BC03M-25 | Null modem extension cable used in conjunction with BC21B-05 | 7.6 m (25 ft) |

**NOTE**

**Strapped logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).**




MXV11-B Jumper Locations

**Jumper Connections for MXV11-B Summary**

| Jumper | Name | Function | Connection* |
|---|---|---|---|
| J1 | Connector for SLU0 | SLU connectors | |
| J2 | Connector for SLU1 | | |
| J3 | HALT | Halt and reboot functions | POC (W3) |
| J4 | GND | | |
| J5 | RBOOT | | |
| J6 | OPEN | | |
| J7 | J1B | Serial line unit baud rates | WW |
| J8 | J1A | | |
| J9 | GND | | |
| J10 | J0B | | |
| J11 | J0A | | |
| J12 | TP2 | For engineering use | |
| J13 | GND | | |
| J14 | SOFT EN | Software programmable baud rates | POC (W4) |
| J15 | OPEN | | |
| J16 | GND | Enables or disables direct mode addressing | POC (W5) |
| J17 | PG L/DIR H | | |
| J18 | OPEN | | |
| J19 | AL12H | PROM size and type in direct mode addressing | POC (W6) |
| J20 | NA12H | | |
| J21 | +5 V | | |
| J22 | LTC COMM | Line time clock frequency | WW |
| J23 | 50 Hz | | |
| J24 | 60 Hz | | |
| J25 | 800 Hz | | |
| J26 | OPEN | Software control of line time clock | POC (W7) |
| J27 | LTC EN IN | | |
| J28 | LTC EN OUT | | |
| J29 | TP3 | For engineering use | |
| J30 | SLUA3 | Serial line unit starting address | WW |
| J31 | GND | | |
| J32 | SLUA2 | | |
| J33 | SLUA1 | | |

Jumper Connections for MXV11-B Summary (Cont)

| Jumper | Name | Function | Connection* |
|---|---|---|---|
| J34 | DIR MODE BOOT | | |
| J35 | OPEN | Direct mode boot and small or large system | WW |
| J36 | GND | | |
| J37 | SM/LG | | |
| J38 | JU1 | | |
| J39 | JU2 | | |
| J40 | GND | Serial line unit vector address | WW |
| J41 | JL1 | | |
| J42 | JL2 | | |
| J43 | JL3 | | |
| J44 | BOOT L/PROM H | | |
| J45 | GND | Boot ROM or user ROM | POC (W9) |
| J46 | OPEN | | |
| J47 | CLOCK IN | | |
| J48 | CLOCK OUT | Master clock | POC (W10) |
| J49 | PROM 1 | | |
| J50 | PROM 2 | | |
| J51 | GND | PROM size and PROM start address | WW |
| J52 | BSK1 | | |
| J53 | BSK2 | | |
| J54 | AJ13 | | |
| J55 | AJ14 | | |
| J56 | AJ15 | RAM starting address | WW |
| J57 | GND | | |
| J58 | AJ16 | | |
| J59 | AJ17 | | |
| J60 | AJ18 | | |
| J61 | OPEN | | |
| J62 | GND | Console mode | POC (W8) |
| J63 | CONSOLE | | |

*POC = Push-on connector
WW = Wire-wrap

**NOTE**

**W1 and W2 are 0 ohm resistors associated with battery backup option. Either one may be inserted but not both. The module is shipped with W2 inserted.**

**Miscellaneous Jumper Configurations**

| Connector | | Connection | Description |
|---|---|---|---|
| J63<br>J62<br>J61 | CONSOLE<br>GND<br>OPEN | GND to OPEN<br>(J62 to J61) | Enables console mode. SLU is fixed at address 77560 and vector address at 60. Select SLU 0 address from Table B and vector from Table C. |
| J63<br>J62<br>J61 | CONSOLE<br>GND<br>OPEN | CONSOLE to GND<br>(J63 to J62) | Disables console mode. For SLU addresses, refer to Table B and vectors from Table C. |
| J46<br>J45<br>J44 | OPEN<br>GND<br>BOOT L/PROM H | BOOT L/PROM H to GND<br>(J44 to J45) | Inserted when MXV11-B2 boot ROM set is installed in sockets XE19 and XE29. Enables the following registers to be addressed if the console GND to OPEN jumper (J62 to J61) is installed:<br>Page control register<br>Line time clock control<br>Diagnostic display register. |
| J46<br>J45<br>J44 | OPEN<br>GND<br>BOOT L/PROM H | GND to OPEN<br>(J45 to J46) | Inserted when ROMs are for user code (not bootstrap code). See Table A for addresses. |
| J37<br>J36<br>J35 | SM/LG SYS<br>GND<br>OPEN | SM/LG SYS to GND<br>(J37 to J36) | This is installed when the MXV11-B is connected in a Q22 bus backplane. Recognizes BDAL <21:00> L. This jumper must be installed if RAM is addressed above 128K words. |
| J37<br>J36<br>J35 | SM/LG SYS<br>GND<br>OPEN | GND to OPEN<br>(J36 to J35) | Installed when the MXV11-B is connected to a 16- or 18-bit Q-BUS. Recognizes BDAL <17:00> L only. |
| J36<br>J35<br>J34 | GND<br>OPEN<br>DIRECT MODE BOOT | DIR MODE BOOT to OPEN<br>(J34 to J35) | Module not wired for direct mode boot. |

**Miscellaneous Jumper Configurations (Cont)**

| Connector | | Connection | Description |
|---|---|---|---|
| J36<br>J35<br>J34 | GND<br>OPEN<br>DIRECT MODE BOOT | DIR MODE BOOT to GND<br>(J34 to J36) | Module enabled for direct mode boot. This jumper must be installed when the user boot is directly addressed. |
| J18<br>J17<br>J16 | OPEN<br>PG L/DIR H<br>GND | PG L/DIR H to GND<br>(J17 to J16) | Enables ROM boot map option and page mode on the MXV11-B. Disables user PROM addresses below 16K. |
| J18<br>J17<br>J16 | OPEN<br>PG L/DIR H<br>GND | PG L/DIR H to OPEN<br>(J17 to J18) | Enables PROM sockets XE19 and XE28 to be used for user defined PROMs. In this case, these sockets can only be addressed in memory locations below the 16K word boundary. |
| J48<br>J47 | CLOCK OUT<br>CLOCK IN | CLOCK OUT to CLOCK IN<br>(J48 to J47) | Factory test. Do not remove. This is the master clock, and provides on-board refresh and the charge pump to generate −12 V. |
| J3<br>J4<br>J5<br>J6 | HALT<br>GND<br>RBOOT<br>OPEN | HALT to GND<br>(J3 to J4) | Enables SLU 1 (console port) to halt the processor upon receiving a break character. |
| J3<br>J4<br>J5<br>J6 | HALT<br>GND<br>RBOOT<br>OPEN | HALT not connected to GND | Disables CPU halt function. |
| J3<br>J4<br>J5<br>J6 | HALT<br>GND<br>RBOOT<br>OPEN | RBOOT to GND | Causes a system reboot when a break condition is received from SLU 1. Forces BDC OK-H low on the bus. |

**NOTE**

**HALT to GND (J3 to J4) and RBOOT to GND (J5 to J4) cannot be simultaneously jumpered.**

**Miscellaneous Jumper Configurations (Cont)**

| Connector | | Connection | Description |
|---|---|---|---|
| J3<br>J4<br>J5<br>J6 | HALT<br>GND<br>RBOOT<br>OPEN | GND to OPEN<br>(J4 to J3) | Disables reboot function. |
| J26<br>J27<br>J28 | OPEN<br>LTC EN IN<br>LTC EN OUT | LTC EN IN to<br>LTC EN OUT<br>(J27 to J28) | Allows LTC to be software controlled. Enables control of BEVENT L on the bus via bit 06 of the LTC register. When bit 6 of LTC register is 0, BEVENT L will be asserted constantly low. This inhibits LTC interrupts. To address the LTC register (777546), the MXV11-B must be in boot mode (BOOT L/PROM H to GND) (J44 to J45) and SLU1 must be the console port (CONSOLE to GRD removed). |
| J26<br>J27<br>J28 | OPEN<br>LTC EN IN<br>LTC EN OUT | LTC EN IN<br>to OPEN<br>(J27 to J26) | Prevents bits 06 of the LTC register from controlling the BEVENT L line. |
| J22<br>J23 | LTC COMM<br>50 Hz | LTC COMM to<br>50 Hz<br>(J22 to J23) | When installed, the BEVENT line is driven from a 50 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line. |
| J24 | 60 Hz | LTC COMM to<br>60 Hz<br>(J22 to J24) | When installed, the BEVENT line is driven from a 60 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line. |

**CAUTION**

**LTC EN IN to LTC EN OUT (J27 to J28) should not be connected if the CPU has an LTC control register.**

**Miscellaneous Jumper Configurations (Cont)**

| Connector | | Connection | Description |
|---|---|---|---|
| J25 | 800 Hz | LTC COMM to 800 Hz (J22 to J25) | When installed, the BEVENT line is driven from an 800 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line. |
| J15<br>J14<br>J13 | OPEN<br>SOFT EN<br>GND | SOFT EN to GND (J14 to J13) | Enables software programmable baud rates for both SLU1 and SLU0 via the CSR. The baud rate jumpers in Table B have no effect if the PBRE bit is set. |
| J15<br>J14<br>J13 | OPEN<br>SOFT EN<br>GND | SOFT EN to OPEN (J14 to J15) | Baud rates are selected from Table B. |
| W1 | | W1 (0 ohm resistor) connected | Battery backup. +5 V is supplied by user on backplane pin AV1. DIGITAL does not supply battery backup. |
| W2 | | W2 (0 ohm resistor) connected | No battery backup. |
| J21<br>J20<br>J19 | +5 V<br>NA12H<br>BA12H | NA12H to +5 V (Normalized address 12) (J20 to J21) to (Buffered Address line 12) | Specifies 2K user UVROMs (2716) installed and direct mode addressing |
| J21<br>J20<br>J19 | +5 V<br>NA12H<br>BA12H | NA12H to BA12H (J20 to J19) | Specifies 4K or 8K user-supplied ROM in direct mode addressing. |

**NOTE**

**One of these jumpers (50, 60, or 800 Hz) should be installed: 1) If no external BEVENT source is provided in the system, and 2) If the user desires this source. Power supplies manufactured by DIGITAL normally supply BEVENT L to the backplane.**

**NOTE**

**There are cases where none of these jumpers (+5 V, NA4H, and AL12H) should be connected. In these cases, the push-on connector must be completely removed or must be connected to one of the outside pins to hold the connector. There is no open pin associated with these jumpers. For example, if 2K non-UV PROMs or the MXV11-B2 ROM is to be installed, these jumpers are all disconnected.**

**Table A. Jumpers for PROM Starting Address**

| | | BSK2 to GND (J53 to J51) | BSK1 to GND (J52 to J51) | User PROM Starting Address (octal) (Note) |
|---|---|---|---|---|
| J51 | GND | R | R | 000000* |
| J52 | BSK1 | R | I | 020000 |
| J53 | BSK2 | I | R | 040000 |
| | I | I | 060000 | |

R = jumper removed
I = jumper inserted to ground
* Shipped configuration. Remove all jumpers from BSK1 (J52) and BSK2 (J53) if not in user mode.

**NOTE**

**These addresses are for user supplied ROMs only. Jumpers BOOT L/PROM H to GND (J44 to J45) and PG L/DIR H to GND (J17 to J16) must be removed.**

**Table B. Serial Line Unit Starting Address Jumpers**

| | | SLUA3 to GND (J30 to J31) | SLUA2 to GND (J32 to J31) | SLU1 to GND (J33 to J31) | Starting Address SLU0 | SLU1 (See Note) |
|---|---|---|---|---|---|---|
| J33 | SLUA1 | R | R | R | 776500* | 776510* |
| J32 | SLUA2 | R | R | I | 776510 | 776520 |
| J31 | GND | R | I | R | 776520 | 776530 |
| J30 | SLUA3 | R | I | I | 776530 | 776540 |
| | | I | R | R | 776540 | 776550 |
| | | I | R | I | 776550 | 776560 |
| | | I | I | R | 776560 | 776570 |
| | | I | I | I | 776570 | 776600 |

R = jumper removed
I = jumper inserted to ground
*Shipped configuration

**NOTE**

**If the GND to OPEN jumper (J62 to J61) is installed (console enabled), the SLU1 address is fixed at the standard console address of 777560 and this column does not apply.**

Table C. Jumpers for SLU Vector Addresses

| | | JU2 to GND (J39 to J40) | JU1 to GND (J38 to J40) | JL3 to GND (J43 to J40) | JL2 to GND (J42 to J40) | JL1 to GND (J41 to J40) | SLU0 | SLU1 (See Note) |
|---|---|---|---|---|---|---|---|---|
| J43 | JL3 | R | R | R | R | R | 300* | 310* |
| J42 | JL2 | R | R | R | R | I | 010 | 020 |
| J41 | JL1 | R | R | R | I | R | 020 | 030 |
| J40 | GND | R | R | R | I | I | 030 | 040 |
| J39 | JU2 | R | R | I | R | R | 040 | 050 |
| J38 | JU1 | R | R | I | R | I | 050 | 060 |
| | | R | R | I | I | R | 060 | 070 |
| | | R | R | I | I | I | 070 | 100 |
| | | R | I | R | R | R | 100 | 110 |
| | | R | I | R | R | I | 110 | 120 |
| | | R | I | R | I | R | 120 | 130 |
| | | R | I | R | I | I | 130 | 140 |
| | | R | I | I | R | R | 140 | 150 |
| | | R | I | I | R | I | 150 | 160 |
| | | R | I | I | I | R | 160 | 170 |
| | | R | I | I | I | I | 170 | 200 |
| | | I | R | R | R | R | 200 | 210 |
| | | I | R | R | R | I | 210 | 220 |
| | | I | R | R | I | R | 220 | 230 |
| | | I | R | R | I | I | 230 | 240 |
| | | I | R | I | R | R | 240 | 250 |
| | | I | R | I | R | I | 250 | 260 |
| | | I | R | I | I | R | 260 | 270 |
| | | I | R | I | I | I | 270 | 300 |
| | | I | I | R | R | R | 300 | 310 |
| | | I | I | R | R | I | 310 | 320 |
| | | I | I | R | I | R | 320 | 330 |
| | | I | I | R | I | I | 330 | 340 |
| | | I | I | I | R | R | 340 | 350 |
| | | I | I | I | R | I | 350 | 360 |
| | | I | I | I | I | R | 360 | 370 |
| | | I | I | I | I | I | 370 | Undefined |

I = jumper inserted from specified pin to ground. Where multiple connections are made, they are daisy-chained.
R = jumper removed
*Shipped configuration

**NOTE**

**If the GND to OPEN jumper (J62 to J61) is installed (console enabled), SLU1 vector address is fixed at 60 and this column does not apply.**

**PROM Jumpers**

| | | NA12H to BA12H (J20 to J19) | NA12H to +5 V (J20 to J21) | Description |
|---|---|---|---|---|
| J19 | BA12H | R | R | |
| J20 | NA12H | I | R | |
| J21 | +5 V | R | I | Page mode – Boot ROM for 2K by 8 non-UV PROMs, 4K by 8 or 8K by 8 PROMs<br>Direct mode – for 2K by 8, non-UV PROMs, 4k by 8, or 8K by 8 PROMs*<br>Direct mode – for 2K by 8 UV PROMs |

R = jumper removed
I = jumper inserted
*Shipped configuration

**Jumpers to Configure PROM Size**

| | | PROM 2 to GND (J50 to J51) | PROM 1 to GND (J49 to J51) | PROM Size |
|---|---|---|---|---|
| J51 | GND | R | R | No ROMs* |
| J50 | PROM 2 | R | I | 2K by 8 |
| J49 | PROM 1 | I | R | 4K by 8 |
| | | | I | I 8K by 8† |

R = jumper removed
I = jumper inserted

* Shipped configuration. Additional jumpers are required depending on user mode/boot mode and direct addressing page addressing. Refer to the last three tables in this section.

† If the MXV11-B2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND jumper (J50 to J49 to J51).

**RAM Starting Address Jumpers**

| | | | AJ18 to GND (J60 to J57) | AJ17 to GND (J59 to J57) | AJ16 to GND (J58 to J57) | AJ15 to GND (J56 to J57) | AJ14 to GND (J55 to J57) | AJ13 to GND (J54 to J57) | RAM Starting Address (Words) |
|---|---|---|---|---|---|---|---|---|---|
| J60 | AJ18 | 00 | R | R | R | R | R | R | 0* |
| J59 | AJ17 | 01 | R | R | R | R | R | I | 4K |
| J58 | AJ16 | 02 | R | R | R | R | I | R | 8K |
| J57 | GND | 03 | R | R | R | R | I | I | 12K |
| J56 | AJ15 | 04 | R | R | R | I | R | R | 16K |
| J55 | AJ14 | 05 | R | R | R | I | R | I | 20K |
| J54 | AJ13 | 06 | R | R | R | I | I | R | 24K |
| | | 07 | R | R | R | I | I | I | 28K |
| | | 10 | R | R | I | R | R | R | 32K |
| | | 11 | R | R | I | R | R | I | 36K |
| | | 12 | R | R | I | R | I | R | 40K |
| | | 13 | R | R | I | R | I | I | 44K |
| | | 14 | R | R | I | I | R | R | 48K |
| | | 15 | R | R | I | I | R | I | 52K |
| | | 16 | R | R | I | I | I | R | 56K |
| | | 17 | R | R | I | I | I | I | 60K |
| | | 20 | R | I | R | R | R | R | 64K |
| | | 21 | R | I | R | R | R | I | 68K† |
| | | 22 | R | I | R | R | I | R | 72K† |
| | | 23 | R | I | R | R | I | I | 76K† |
| | | 24 | R | I | R | I | R | R | 80K† |
| | | 25 | R | I | R | I | R | I | 84K† |
| | | 26 | R | I | R | I | I | R | 88K† |
| | | 27 | R | I | R | I | I | I | 92K† |
| | | 30 | R | I | I | R | R | R | 96K† |
| | | 31 | R | I | I | R | R | I | 100K† |
| | | 32 | R | I | I | R | I | R | 104K† |
| | | 33 | R | I | I | R | I | I | 108K† |
| | | 34 | R | I | I | I | R | R | 112K† |
| | | 35 | R | I | I | I | R | I | 116K† |
| | | 36 | R | I | I | I | I | R | 120K† |
| | | 37 | R | I | I | I | I | I | 124K† |
| | | 40 | I | R | R | R | R | R | 128K† |
| | | 41 | I | R | R | R | R | I | 132K† |
| | | 42 | I | R | R | R | I | R | 136K† |
| | | 43 | I | R | R | R | I | I | 140K† |
| | | 44 | I | R | R | I | R | R | 144K† |
| | | 45 | I | R | R | I | R | I | 148K† |
| | | 46 | I | R | R | I | I | R | 152K† |
| | | 47 | I | R | R | I | I | I | 156K† |

RAM Starting Address Jumpers (Cont)

| | AJ18 to GND (J60 to J57) | AJ17 to GND (J59 to J57) | AJ16 to GND (J58 to J57) | AJ15 to GND (J56 to J57) | AJ14 to GND (J55 to J57) | AJ13 to GND (J54 to J57) | RAM Starting Address (Words) |
|---|---|---|---|---|---|---|---|
| 50 | I | R | I | R | R | R | 160K† |
| 51 | I | R | I | R | R | I | 164K† |
| 52 | I | R | I | R | I | R | 168K† |
| 53 | I | R | I | R | I | I | 172K† |
| 54 | I | R | I | I | R | R | 176K† |
| 55 | I | R | I | I | R | I | 180K† |
| 56 | I | R | I | I | I | R | 184K† |
| 57 | I | R | I | I | I | I | 188K† |
| 60 | I | I | R | R | R | R | 192K† |
| 61 | I | I | R | R | R | I | 196K† |
| 62 | I | I | R | R | I | R | 200K† |
| 63 | I | I | R | R | I | I | 204K† |
| 64 | I | I | R | I | R | R | 208K† |
| 65 | I | I | R | I | R | I | 212K† |
| 66 | I | I | R | I | I | R | 216K† |
| 67 | I | I | R | I | I | I | 220K† |
| 70 | I | I | I | R | R | R | 224K† |
| 71 | I | I | I | R | R | I | 228K† |
| 72 | I | I | I | R | I | R | 232K† |
| 73 | I | I | I | R | I | I | 236K† |
| 74 | I | I | I | I | R | R | 240K† |
| 75 | I | I | I | I | R | I | 244K† |
| 76 | I | I | I | I | I | R | 248K† |
| 77 | I | I | I | I | I | I | 252K† |

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.

R = jumper removed.

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

**NOTE**

**Be careful when configuring the MXV11-B RAM when ROM is used in the USER ROM address space. USER ROM address space is defined as bus addresses 0–16K, (00000–100000) on 4K boundaries. The RAM start address must be higher than the last location of the ROM or dual responses from both the RAM and ROM will occur. The chart below shows several examples of right and wrong ways of assigning RAM memory start addresses.**

| ROM Size | ROM Start | RAM Start | RAM End | Comments |
|---|---|---|---|---|
| 8K | 0K | 4K | 68K | Wrong, 4K overlap (4K→8K) |
| 8K | 4K | 0K | 64K | Wrong, 8K overlap (4K→12K) |
| 4K | 0K | 4K | 68K | Right, no overlap |
| 4K | 0K | 12K | 76K | Right, no overlap‡ |
| 8K | 4K | 12K | 76K | Right |

‡ Address space gap usually not recommended but up to user to decide depending on application.

**Jumper Connections for PROM Sizes in User Mode**

| Jumpers | | No PROMs | 2K by 8 | 4K by 8 | 8K by 8 |
|---|---|---|---|---|---|
| J16 | (GND) | J17 to J18 | J17 to J18 | J17 to J18 | J17 to J18 |
| J17 | (PG L/DIR H) | | | | |
| J18 | (OPEN) | | | | |
| J19 | (BA12H) | J19 to J20 | J20 to J21 | J19 to J20 | J19 to J20 |
| J20 | (NA12H) | | | | |
| J21 | (+5 V) | | | | |
| J44 | (BOOT L/PROM H) | J45 to J46 | J45 to J46 | J45 to J46 | J45 to J46 |
| J45 | (GND) | | | | |
| J46 | (OPEN) | | | | |
| J49 | (PROM1) | – | J49 to J51 | J50 to J51 | J49 to J50 to J51 |
| J50 | (PROM2) | | | | |
| J51 | (GND) | | | | |

**NOTE**

**Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J45 is connected to J46, and J49 is connected to J51.**

**Jumper Connections for PROM Sizes in Boot Mode (Page Addressing)**

| Jumpers | No PROMs | 2K by 8* | 4K by 8 | 8K by 8 |
|---|---|---|---|---|
| J16 (GND)<br>J17 (PG L/DIR H)<br>J18 (OPEN) | J17 to J18 | J16 to J17 | J16 to J17 | J16 to J17 |
| J19 (BA12H)<br>J20 (NA12H)<br>J21 (+5 V) | J19 to J20 | – | J19 to J20 | J19 to J20 |
| J44 (BOOT L/PROM H)<br>J45 (GND)<br>J46 (OPEN) | J45 to J46 | J44 to J45 | J44 to J45 | J44 to J45 |
| J49 (PROM1)<br>J50 (PROM2)<br>J51 (GND) | – | J49 to J51 | J50 to J51 | J49 to J50<br>to J51 |

*2K by 8 UV PROM cannot be used in page mode.

**NOTE**

**Jumper connections are indicated. For example, in the 8K by 8 PROM, J16 is connected to J17, J19 is connected to J20, J44 is connected to J45 and J49, J50 and J51 are connected.**

**Jumper Connections for PROM Sizes in Boot Mode (Direct Addressing)**

| Jumpers | | No PROMs | 2K by 8 | 4K by 8 | 8K by 8 |
|---|---|---|---|---|---|
| J16 | (GND) | J17 to J18 | J17 to J18 | J17 to J18 | J17 to J18 |
| J17 | (PG L/DIR H) | | | | |
| J18 | (OPEN) | | | | |
| J19 | (BA12H) | J19 to J20 | J20 to J21 | J19 to J20 | J19 to J20 |
| J20 | (NA12H) | | | | |
| J21 | (+5 V) | | | | |
| J44 | (BOOT L/PROM H) | J45 to J46 | J44 to J45 | J44 to J45 | J44 to J45 |
| J45 | (GND) | | | | |
| J46 | (OPEN) | | | | |
| J49 | (PROM1) | – | J49 to J51 | J50 to J51 | J49 to J50 to J51 |
| J50 | (PROM2) | | | | |
| J51 | (GND) | | | | |
| J34 | (DIR MODE BOOT) | – | J34 to J36 | J34 to J36 | J34 to J36 |
| J35 | (OPEN) | | | | |
| J36 | (GND) | | | | |

**NOTE**

**Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J44 is connected to J45, J49 is connected to J51, and J34 is connected to J36.**

# RKV11-D BUS INTERFACE FOR RKV11-D DISK DRIVE CONTROLLER

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 1.8 max. | 0 | 1.93 | 1 | (2) BC05L + M993-YA |

## Standard Address

| | | |
|---|---|---|
| RKDS | (Drive Status) | 177400 |
| RKER | (Error) | 177402 |
| RKCS | (Control/Status) | 177404 |
| RKWC | (Word Count) | 177406 |
| RKBA | (Bus Address) | 177410 |
| RKDA | (Disk Address) | 177412 |
| RKDB | (Data Buffer) | 177416 |

## Vector

220

## Diagnostic Programs

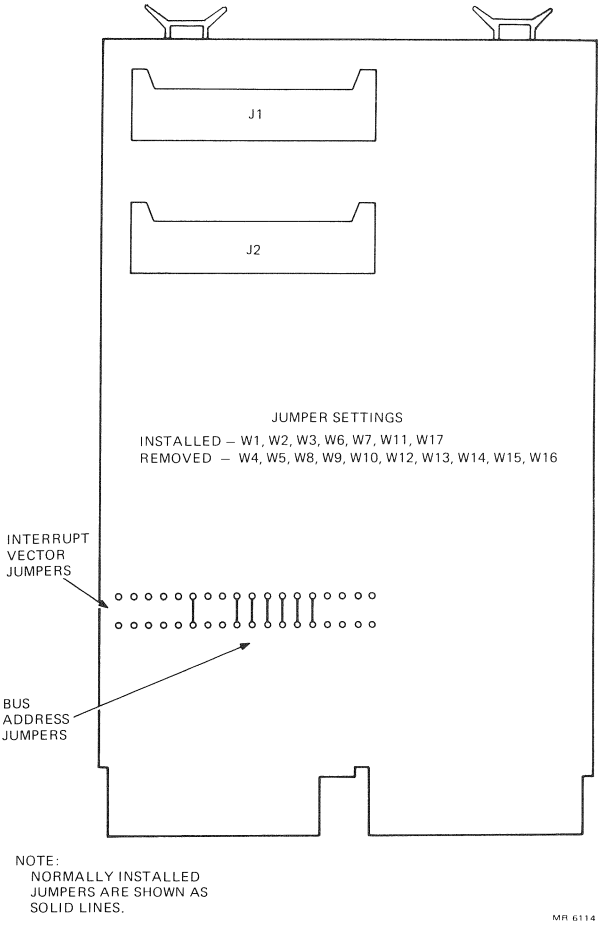
Refer to Appendix A.

**NOTE**

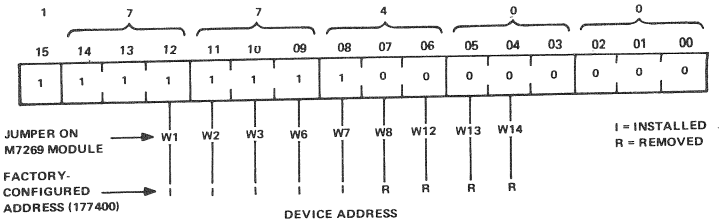
**The logic test programs should be run first, then the dynamic test, and finally the performance exerciser.**

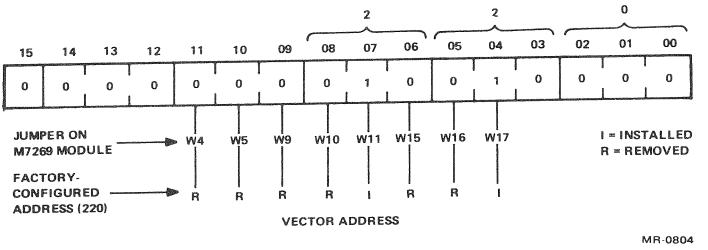
## Related Documentation

*RKV11-D Disk Drive Controller User's Manual* (EK-RKV11-OP-001)
*RKV11-Disk Drive Controller Technical Manual* (EK-RKV11-TM-001)
Field Maintenance Print Set (MP00223)
*RK05/RK05J/RK05F Disk Drive Maintenance Manual* (EK-RK5JF-MM-001)
*RK05/RK05J Disk Drive Preventive Maintenance Manual* (EK-RK05J-PM-001)
*RK05F DEC Disk Drive Preventive Maintenance Procedure* (ED-RK05F-PM-001)
*Microcomputer Interfaces Handbook* (EB-20175-20)




M7269 Jumpers



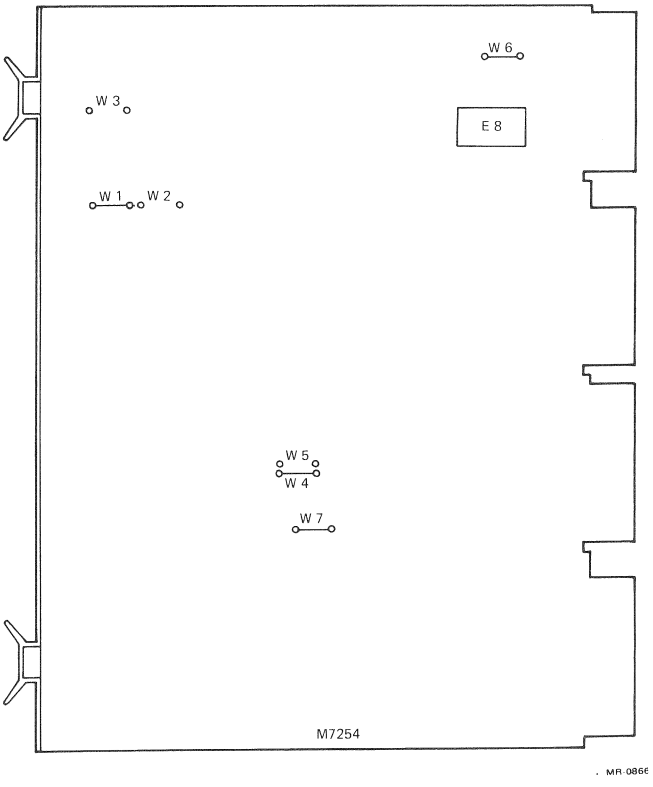



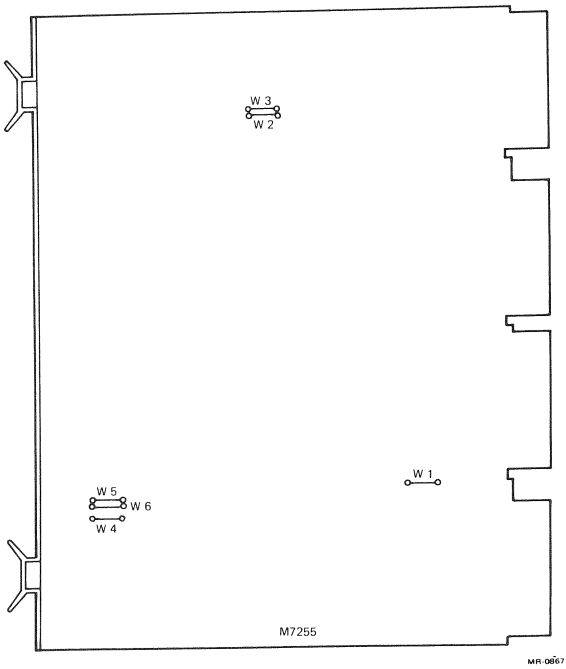

Jumper settings on the three RKV11-D modules are identical to those in the standard RK11-D configuration. A breakdown is given below for reference. There are no jumpers on M7268.

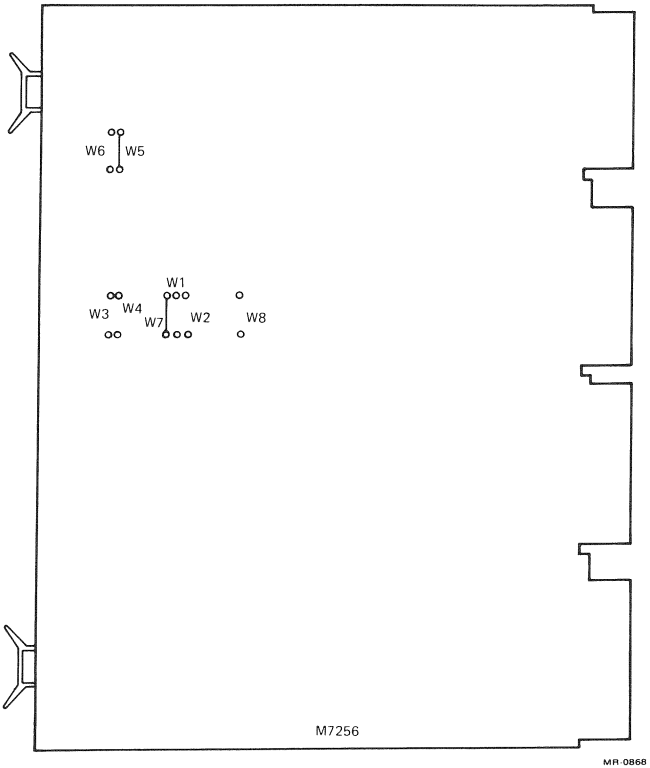
| Module | Installed | Removed |
|---|---|---|
| M7254* | W1, W4, W6, W7 | W2, W3, W5 |
| M7255** | W1, W2, W6 | W3, W4, W5 |
| M7256 | W2, W5, W7 | W1, W3, W4, W6, W8 |

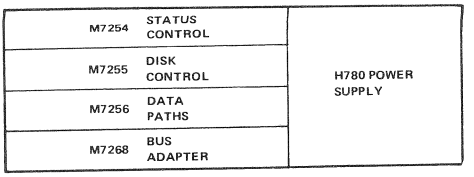
* Interrupt priority jumper (BR4-7) in socket E8 is not required since the RKV11-D was designed for single-line interrupt scheme only.

** 2.88 MHz crystal used DEC PN 18-10694-3.


W 6
W 3
E 8
W 1
W 2
W 5
W 4
W 7
M7254
MR-0866


W 3
W 2
W 1
W 5
W 6
W 4
M7255
MR-0967


W6
W5
W1
W3
W4
W7
W2
W8
M7256
MR-0868



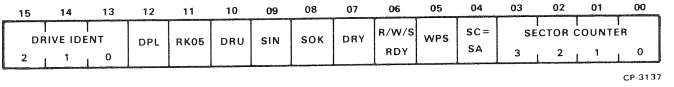

RKV11-D Module Utilization

## Drive Status Register (RKDS)

Address = 177400

**NOTE**

**This register is a read-only register, and contains the selected drive status and current sector address.**




**Bit Definitions**

| Bit | Function |
|---|---|
| 00-03 | Sector Counter (SC) - These four bits are the current sector address of the selected drive. Sector address 00 is defined as the sector following the sector that contains the index pulse. |
| 04 | Sector Counter Equals Sector Address (SC = SA) - Indicates that the disk heads are positioned over the disk address currently held in the sector address register. |
| 05 | Write-Protect Status (WPS) - Sets when the selected disk is in the write-protected mode. |
| 06 | Read/Write/Seek Ready (R/W/S RDY) - Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function. |
| 07 | Drive Ready (DRY) - Indicates that the selected disk drive complies with the following conditions. |

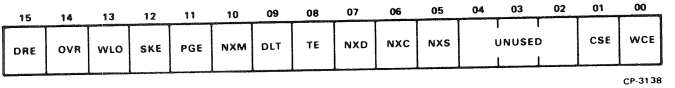
**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| | 1. The drive is properly supplied with power.<br>2. The drive is loaded with a disk cartridge.<br>3. The disk drive door is closed.<br>4. The LOAD/RUN switch is set to RUN.<br>5. The disk is rotating at a proper speed.<br>6. The heads are properly loaded.<br>7. The disk is not in a DRU (bit 10 or RKDS) condition. |
| 08 | Sector Counter OK (SOK) - Indicates that the sector counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the sector counter is not ready for examination, and a second attempt should be made. |
| 09 | Seek Incomplete (SIN) - Indicates that due to some unusual condition, to seek function cannot be completed. Can be accompanied by RKER 15 (drive error). Cleared by a drive reset function. |
| 10 | Drive Unsafe (DRU) - Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition recurs, an inoperative drive can be assumed, and corrective maintenance procedures should begin. Can be accompanied by RKER 15 (drive error). |
| 11 | RK05 Disk on Line (RK05) - Always set, to identify the selected disk drive as RK05. |
| 12 | Drive Power Low (DPL) - Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 15 (drive error). Reset by a BUS INIT or a control reset function. |
| 13-15 | Identification of Drive (ID) - If an interrupt occurs as the result of a hardware poll operation, these bits will contain the binary representation of the logical drive number that caused the interrupt. |

## Error Register (RKER)

Address = 177402

**NOTE**
**This is a read-only register.**




### Bit Definitions

| Bit | Function |
|---|---|
| 00 | Write Check Error (WCE) - Indicates that an error was encountered during a write check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition. |
| 01 | Checksum Error (CSE) - Sets while performing a read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition. |
| 02-04 | Unused. |

The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a control reset function.

### Bit Definitions

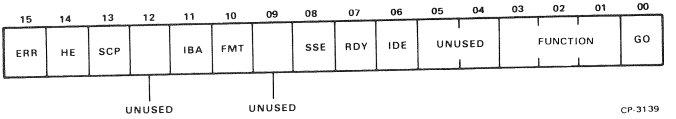
| Bit | Function |
|---|---|
| 05 | Nonexistent Sector (NXS) - Indicates that an attempt was made to a sector address greater than $13_8$. |
| 06 | Nonexistent Cylinder (NXC) - Indicates that an attempt was made to initiate a transfer to a cylinder address greater than $312_8$. |
| 07 | Nonexistent Disk (NXD) - Indicates that an attempt was made to initiate a function on a nonexistent drive. |
| 08 | Timing Error (TE) - Indicates that a loss of timing pulses for at least 5 $\mu$s has been detected. |

**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 09 | Data Late (DLT) - Sets during a write or write check function when the multibuffer file is empty and the operation is not yet complete. Sets during a read function when the multibuffer file is filled and the operation is not yet complete. |
| 10 | Nonexistent Memory (NXM) - Sets if memory does not respond with a RPLY within 20 $\mu$s of the time when the RKV11-D becomes bus master during a DMA sequence. Because of the speed of the RK05 disk drive, it is possible that NXM will be accompanied by RKER 09 (data late). |
| 11 | Programming Error (PGE) - Indicates that RKCS 10 (format) was set while initiating a function other than read or write. |
| 12 | Seek Error (SKE) - Sets if the disk head mechanism is not properly positioned while executing a normal read, write, read check, or write check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once. |
| 13 | Write Lockout Violation (WLO) - Sets if an attempt is made to write on a disk that is currently write protected. |
| 14 | Overrun (OVR) - Indicates that during a read, write, read check, or write check function, operations on sector $13_8$, surface 1 of cylinder address $312_8$ were finished, and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive. |
| 15 | Drive Error (DRE) - Sets if a function is either initiated or in process, and<br>a. one of the drives in the system senses a loss of either ac or dc power; or<br>b. the selected drive is not ready, or is in some error condition. |

## Control Status Register (RKCS)

Address = 177404




### Bit Definitions

| Bit | Function |
|---|---|
| 00 | Go - This bit can be loaded by the operator and causes the control to carry out the function contained in bits 01-03 of the RKCS (functions). Remains set until the control actually begins to respond to go, which may take from 1 $\mu$s to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector). Write only. |
| 01-03 | Function - The function register, or function bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. Read/write. The binary codings are as follows. |

| Bit 3 | Bit 2 | Bit 1 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | Control Reset |
| 0 | 0 | 1 | Write |
| 0 | 1 | 0 | Read |
| 0 | 1 | 1 | Write Check |
| 1 | 0 | 0 | Seek |
| 1 | 0 | 1 | Read Check |
| 1 | 1 | 0 | Drive Reset |
| 1 | 1 | 1 | Write Lock |

| | |
|---|---|
| 04, 05 | Unused. The RK11-D uses these bits. Since the PDP-11/03 bus structure has no provision for extended addressing, no connection is made to the bus from these bits on the RKV11-D. They will respond as two unused read/write bits in the status register; but, like the RK11-D they, will increment should the RKBA overflow. |

**Bit Definitions (Cont)**

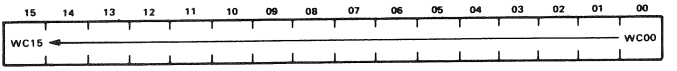
| Bit | Function |
|---|---|
| 06 | Interrupt on Done Enable (IDE) - When set, causes the control to issue a bus request and interrupt to vector address 220 if:<br>a. a function has completed activity<br>b. a hard error is encountered<br>c. a soft error is encountered and bit 08 of the RKCS (SSE) is set<br>d. RKCS 07 (RDY) is set and go is not set.<br>Read/write. |
| 07 | Control Ready (RDY) - Indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by go being set. Read only. |
| 08 | Stop on Soft Error (SSE) - If a soft error is encountered when this bit is set:<br>a. all control action will stop at the end of the current sector if RKCS 06 (IDE) is reset, or<br>b. all control action will stop and a bus request will occur at the end of the current sector if RKCS 06 (IDE) is set.<br>Read/write. |
| 09 | Unused. |
| 10 | Format (FMT) - FMT is under program control, and must be used only in conjunction with normal read and write functions. Used to format a new disk pack or to reformat any sector erased due to control or drive failure. Alters the normal write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head position is not checked for proper positioning before the write. Alters the normal read operation in that only one word, the header word, is transferred to memory per sector. For example, a three-word read function in format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking. Read/write. |
| 11 | Inhibit Incrementing the RKBA (IBA) - Inhibits the RKBA from incrementing during a normal transfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation. Read/write. |
| 12 | Unused. |

**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 13 | Search Complete (SCP) - Indicates that the previous interrupt was the result of some seek or drive reset function. Cleared at the initiation of any new function. Read only. |
| 14 | Hard Error (HE) - Sets when any of RKER 05-15 are set. Stops all control action, and processor reaction is dictated by RKCS 06 (IDE), until cleared, along with RKER 05-15, by INIT or a control reset function. Read only. |
| 15 | Error (ERR) - Sets when any bit of the RKER sets. Processor reaction is dictated by RKCS 06 and RKCS 08 (IDE and SSE). Cleared if all bits in the RKER are cleared. Read only. |

### Word Count Register (RKWC)

Address = 177406

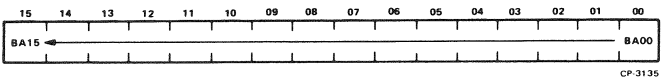



**Bit Definition**

| Bit | Function |
|---|---|
| 00-15 | WC00-WC15 - The bits in this register contain the 2's complement of words to be affected or transferred by a given function. The register increments by 1 after each word transfer. When the register overflows (all WC bits go to 0), the transfer is complete and RKV11-D operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred. Read/write. |

### Current Bus Address Register (RKBA)

Address = 177410

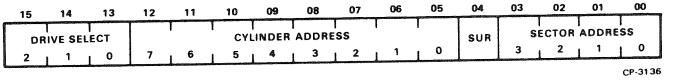



**Bit Definition**

| Bit | Function |
|---|---|
| 00-15 | BA00-BA15 - The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. Read/write. |

### Disk Address Register (RKDA)

Address = 177412




**NOTE**

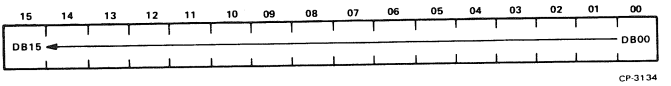
**This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready (RDY – bit 07 of the RKCS) state, and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.**

**Bit Definitions**

| Bit | Function |
|---|---|
| 00-03 | Sector Address (SA) - Binary representation of the disk sector to be addressed for the next function. The largest valid address (or number) for the sector address is $13_8$. |
| 04 | Surface (SUR) - When set, enables the lower disk head so that operation is performed on the lower surface; when reset, enables the upper disk head. |
| 05-12 | Cylinder Address (CYL ADDR) - Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312 . |
| 13-15 | Drive Select (DR SEL) - Binary representation of the logical drive number currently being selected. |

## Data Buffer Register (RKDB)

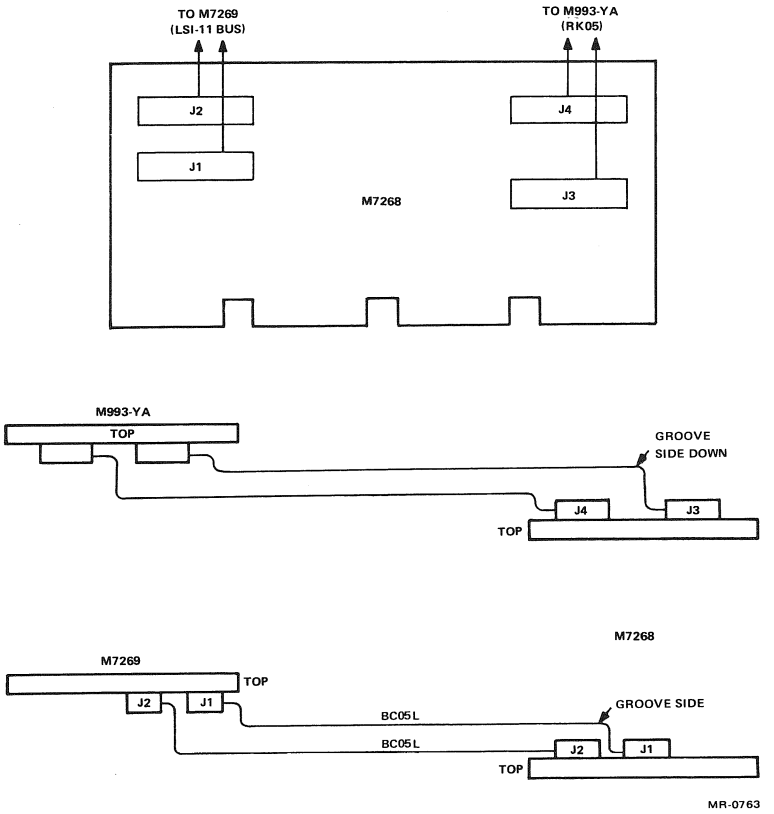
Address = 177416




### Bit Definition

| Bit | Function |
|---|---|
| 00-15 | DB00-DB15 - The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RKV11-D is bus master during a DMA sequence. Read only. |

**NOTE**
**Address 177414 is unused.**




RKV11-D Cable Connection

# RLV11 CONTROLLER MODULES

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | BC08R-XX |
| 6.5 | 1.0 | 3.2 | 1 | 70-12122 (1 per drive) |

Transition Bracket Assembly 70-12415-00
Terminator 70-12293-00

## Standard Addresses

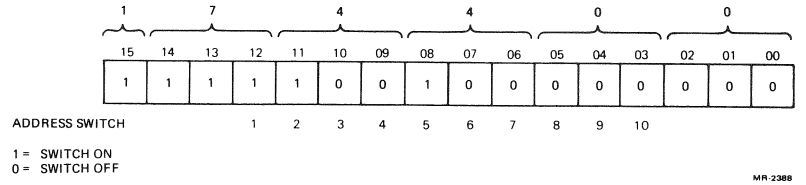
| | |
|---|---|
| CSR | 174400 |
| BAR | 174402 |
| DAR | 174404 |
| MPR | 174406 |

## Standard Vectors

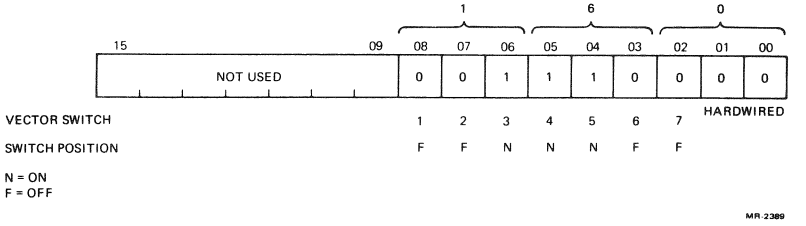
160

## Diagnostic Programs

Refer to Appendix A.




Address Selection



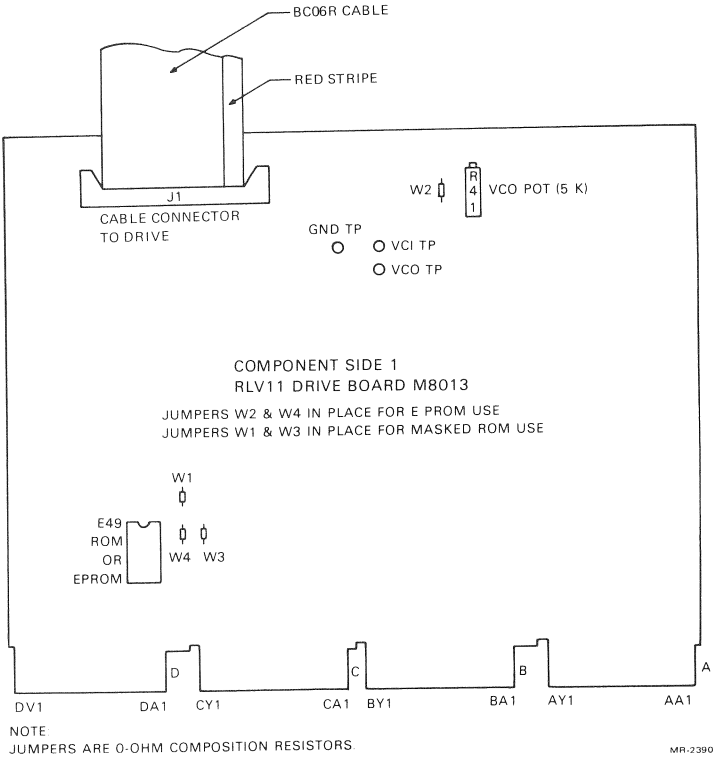

Vector Selection

## Related Documentation

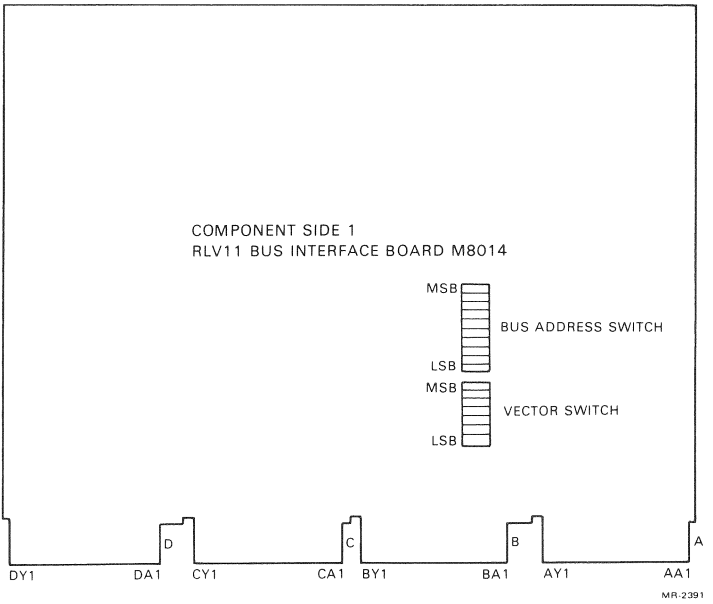
*RLV11 Controller Technical Description Manual* (EK-RLV11-TD)
RLV11 Field Maintenance Print Set (MP00635)
RL01 Field Maintenance Print Set (MP00347)
RL02 Field Maintenance Print Set (MP00553)
RL01 Disk Drive IPB (EK-ORL01-IP)
RL02 Disk Drive IPB (EK-ORL02-IP)
*RL01/RL02 User's Guide* (EK-RL012-UG)
*RL01/RL02 Pocket Service Guide* (EK-RL012-PG)
*Microcomputer Interfaces Handbook* (EB-20175-20)

**NOTE**

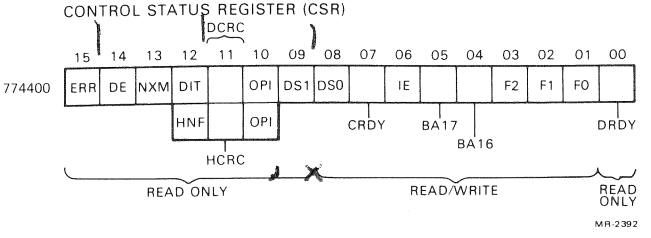
**The M8013 must be installed above the M8014. The RLV11 controllers can only be used in a backplane built as an H9273 (slots A and B = LSI bus and slots C and D = interboard bus). The BA11-N box currently is the only box that contains an H9273 backplane.**




RLV11 Drive Module (M8013)




RLV11 Bus Interface Module (M8014)




Control Status Register

**CSR Bit Definitions**

| Bit | Function |
|---|---|
| 0 | Drive Ready (DRDY) - When set, this bit indicates that the selected drive is ready to receive a command (no seek operation in progress). The bit is cleared when a seek operation is initiated and set when the seek operation is completed. |
| 1-3 | Function Code - These bits are set by software to indicate the command to be executed. |

| F2 | F1 | F0 | Command | Octal Code |
|---|---|---|---|---|
| 0 | 0 | 0 | MAINTENANCE MODE | 0 |
| 0 | 0 | 1 | WRITE CHECK | 1 |
| 0 | 1 | 0 | GET STATUS | 2 |
| 0 | 1 | 1 | SEEK | 3 |
| 1 | 0 | 0 | READ HEADER | 4 |
| 1 | 0 | 1 | WRITE DATA | 5 |
| 1 | 1 | 0 | READ DATA | 6 |
| 1 | 1 | 1 | READ DATA WITHOUT HEADER CHECK | 7 |

Command execution starts when CRDY (bit 7) of the CSR is cleared by software. In a sense, bit 7 can be considered a negative go bit.

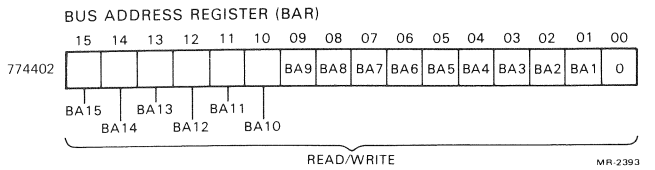
| | |
|---|---|
| 4-5 | Bus Address Extension Bits (BA15, BA17) - Two most significant bus address bits. Read and written as bits 4 and 5 of the CSR, they function as address bits 16 and 17 of the BAR. |
| 6 | Interrupt Enable (IE) - When this bit is set by software, the controller is allowed to interrupt the processor at the assertion of CRDY. This occurs at the normal or error termination of a command. Once an interrupt request is posted on the LSI bus, it is not removed until serviced even if IE is cleared. |

**CSR Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 7 | Controller Ready (CRDY) - When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. Software cannot set this bit because no registers are accessible while CRDY is 0. When set, this bit indicates that the controller is ready to accept another command. |
| 8-9 | Drive Select (DS0, DS1) - These bits determine which drive will communicate with the controller via the drive bus. |
| 10 | Operation Incomplete (OPI) - When set, this bit indicates that the current command was not completed within the OPI timer period. |
| 11 | Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE) - If OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC).<br><br>If OPI (bit 10) is cleared and bit 11 is set and the function command was a write check, a write check error (WCE) has occurred. |
| | **NOTE**<br>**Cyclic redundancy checking is done only on the desired header. It is performed on the first and second header words, even though the second header word is always 0.** |
| 12 | Data Late (DLT) or Header Not Found (HNF Error) - When OPI (bit 10) is cleared and bit 12 is set, it indicates that a data late condition occurred on a read without header check operation. One of two conditions exists:<br><br>**Write Operation –** The silo is empty, but the word count has not reached zero. (Bus request was ignored for too long.)<br><br>**Read Operation –** The silo is full (word being read could not enter the silo and the bus request was ignored too long.)<br><br>When OPI (bit 10) is set and bit 12 is also set, it indicates that a timeout occurred while the controller was searching for the correct sector to read or write (no header; compare [NHF]). |

CSR Bit Definitions (Cont)

| Bit | Function |
|---|---|
| | **Error Summary**<br><br>**Error** — **Bit 12** — **Bit 11** — **Bit 10** — **Comments**<br><br>OPI — 0 — 0 — 1 — 200 ms timeout<br>DCRC — 0 — 1 — 0<br>WCE — 0 — 1 — 0 — Function command is a write check.<br>HCRC — 0 — 1 — 1<br>DLT — 1 — 0 — 0<br>HNF — 1 — 0 — 1 |
| 13 | Nonexistent Memory (NXM) - When set, this bit indicates that during a DMA data transfer, the memory location addressed did not respond within 14 ms. |
| 14 | Drive Error (DE) - This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a GET STATUS command.<br><br>To clear the drive error bit, execute a GET STATUS command with bit 3 of the DAR. |
| 15 | Composite Error (ERR) - When set, this bit indicates that one or more of the error bits (bits 10-14) is set. When an error occurs, the current operation terminates and an interrupt routine is initiated if the interrupt enable bit (bit 6 of the CSR) is set. |




Bus Address Register

**BAR Bit Definitions**

The Bus Address Register (BAR) is a 16-bit word-addressable register with an address of 774 402. Bits 0 through 15 can be read or written; bit 0 should normally be written 0. Expansion bits 16 and 17 are programmable via bits 4 and 5 of the CSR.

The bus address register indicates the memory location involved in the DMA data transfer during a read or write operation. The contents of the BAR are automatically incremented by 2 as each word is transferred between system memory and controller in either direction. Clear the BAR by executing a BUS INIT.

**Disk Address Register (DAR)**
The Disk Address Register (DAR) is a 16-bit read/write word-addressable register with an address of 774 404. Its contents can have one of three meanings, depending on the function being performed. Clear this register by executing a BUS INIT.

**DAR During a SEEK Command –** To perform a seek function, it is necessary to provide address difference, head select, and head directional information to the selected drive.

DAR DURING SEEK COMMAND

| | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 774404 | DF8 | DF7 | DF6 | DF5 | DF4 | DF3 | DF2 | DF1 | DF0 | 0 | 0 | HS | 0 | DIR | 0 | 1 |

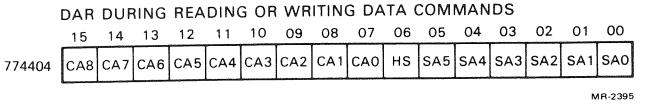
MR-2394

DAR SEEK Command

**Bit Definitions**

| Bits | Function |
|---|---|
| 0 | Marker (MRKR) - Must be a 1. |
| 1 | Must be a 0, indicating to the drive that a SEEK command is being requested and that the remaining bits in the register will contain the seek specifications. |
| 2 | Direction (DIR) - This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-14). |
| 3 | Must be a 0. |
| 4 | Head Select (HS) - Indicates which head (disk surface) is to be selected. Set = lower; clear = upper. |
| 5-6 | Reserved. |
| 7-14 | Cylinder Address Difference (DF<8:0>) - Indicates the number of cylinders the heads are to move on a seek. |
| 15 | Must be a 0. |

**DAR During READ or WRITE DATA Command** – For a read, write, or write check operation, the DAR is loaded with the address of the first sector to be transferred. Thereafter, as each adjoining sector is transferred, the DAR is automatically incremented by 1. If the DAR increments to the nonexistent sector address $50_8$, an OPI timeout will occur. The drive must then seek to a new track if the transfer is to continue.

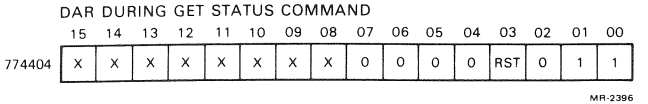



DAR READ/WRITE DATA Command

**Bit Definitions**

| Bit | Function |
|---|---|
| 0-5 | Sector Address (SA<5:0>) - Address of one of the 40 sectors on a track. (Octal range is 0 to 47.) |
| 6 | Head Select (HS) - Indicates which head (disk surface) is to be selected. Set = lower; clear = upper. |
| 7-14 | Cylinder Address (CA<8:0>) - Address of one of the 256 cylinders. (Octal range is 0 to 377.) |
| 15 | Must be a 0. |

**DAR During a GET STATUS Command** – After the GET STATUS command is deposited in the CSR, it is the DAR's responsibility to get the command transferred to the drive. Therefore, the DAR must also be programmed along with the CSR to do the GET STATUS command.



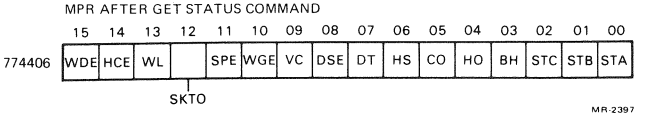

DAR GET STATUS Command

For a GET STATUS command, the DAR register bits must be programmed as follows.

**DAR Register Bits for a GET STATUS Command**

| Bit | Function |
|---|---|
| 0 | Marker (MRKR) - Must be a 1. |
| 1 | Get Status (GS) - Must be a 1, indicating to the drive that its status word is being requested. At the completion of the GET STATUS command, the drive status word is read into the controller multipurpose (MP) register (output stage of FIFO). With this bit set, bits 8-15 are ignored by the drive. |
| 2 | Must be a 0. |
| 3 | Reset (RST) - When this bit is set, the drive clears its error register of soft errors before sending a status word to the controller. |
| 4-7 | Must be a 0. |
| 8-15 | Not used. |

**Multipurpose Register (MPR)**
The MPR is two registers bearing the same base address. When writing into that location, the word counter accepts the data. When reading from that location, the FIFO output buffer provides the data.




MPR Status Word

**MPR After a GET STATUS Command –** When a GET STATUS command is executed and a status word is returned to the controller, the contents of the MPR (FIFO output stage) are defined as follows.

**Bits 0–2 – State<C:A) (ST<C:A>) –** These bits define the state of the drive.

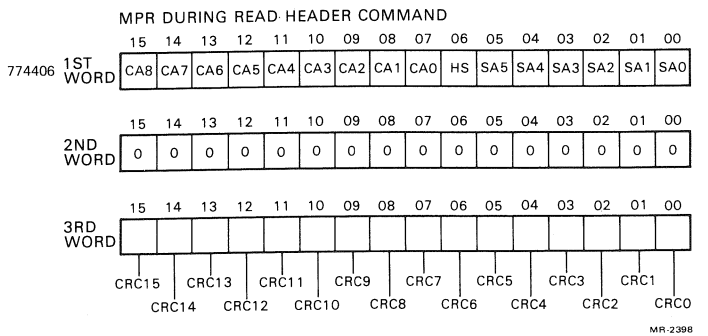
| Bits | | | Definition |
|---|---|---|---|
| C | B | A | |
| 0 | 0 | 0 | Load Cartridge |
| 0 | 0 | 1 | Spin Up |
| 0 | 1 | 0 | Brush Cycle |
| 0 | 1 | 1 | Load Heads |
| 1 | 0 | 0 | Seek Track Counting |
| 1 | 0 | 1 | Seek Linear Mode (Lock On) |
| 1 | 1 | 0 | Unload Heads |
| 1 | 1 | 1 | Spin Down |

**Bit Definitions**

| Bit | Function |
|---|---|
| 3 | Brush Home (BH) - Asserted when the brushes are not over the disk. |
| 4 | Heads Out (HO) - Asserted when the heads are over the disk. |
| 5 | Cover Open (CO) - Asserted when the cover is open or the dust cover is not in place. |
| 6 | Head Select (HS) - Indicates the currently selected head. |
| 7 | Drive Type (DT) - Set = lower; clear = upper. Set = RL02; clear = RL01. |
| 8 | Drive Select Error (DSE) - Indicates that multiple drive selection was detected. |
| 9 | Volume Check (VC) - VC is set every time the drive goes into load heads state. This asserts a drive error at the controller but not on the front panel. VC is an indication that the program does not really know which disk is present until it has read the serial number and bad sector file. (The disk might have been changed while the heads were unloaded.) |
| 10 | Write Gate Error (WGE) - Indicates that the drive sensed that write gate was asserted when sector pulse was asserted, or write gate was set with the drive not ready, or the drive was write locked. |

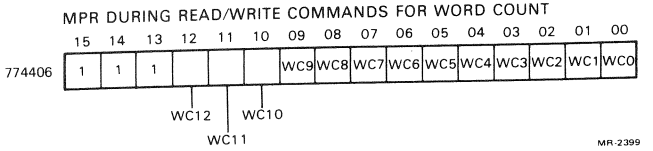
**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 11 | Spin Error (SPE) - Indicates that the spindle did not reach speed in the required time; or indicates over speeding. |
| 12 | Seek Time Out (SKTO) - Indicates that the heads did not come on track in the required time during a SEEK command or loss of "ready to read/write during lock on" mode. |
| 13 | Write Lock (WL) - Indicates write lock status of selected drive. Set = write protected. |
| 14 | Head Current Error (HCE) - Indicates that write current was detected in the heads when write gate was not asserted. |
| 15 | Write Data Error (WDE) - Indicates that write gate was asserted but no transitions were detected on the write data line. |




MPR Three Header Words

**MPR After a Read Header Command –** When a READ HEADER command is executed, three words will be stored in the multipurpose register (FIFO output buffer). The first header word will contain sector address (SA0:SA5), head select (HS - set = lower; clear = upper), and cylinder address information (CA0:CA8). The second word will contain all 0s. The third word will contain the header CRC information. All three words are readable by the main program.




MPR Used As Word Counter

**Bit Definitions**

| Bit | Function |
|---|---|
| 0-12 | Word Count (WC<12:0>) - 2's complement of total number of words to be transferred. |
| 13-15 | Must be a 1 for word count in correct range. |

**MPR During READ/WRITE DATA Commands –** When transferring data via DMA, the MPR functions as a word counter and is loaded by program with the 2's complement of the number of words to be transferred. It is then incremented by 1 by the controller as each word is transferred. The reading or writing operation generally is terminated when the word counter overflows. The word counter can keep track of from one data word to the full 40-sector count of 5120 data words (decimal). The maximum number of words that can be transferred in a single operation is limited by the number of sectors available to be written in the track.

**NOTE**

**The RL01/RL02 disk drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.**

1. **Program the data transfer to terminate at the end of the last sector of the track.**

2. **Program a seek to the next track. This can be accomplished either by a head switch to the other surface but the same cylinder, or a head switch to move to the next cylinder.**

3. **Program the data transfer to continue at the start of the first sector on the next track.**

# RLV12 DISK CONTROLLER

### Power Requirements

+5 Vdc ± 5% at 5.0 A
+12 Vdc ± 5% at 0.1 A

### Bus Loads

| DC | AC |
|---|---|
| 1 | 2.7 |

### Optional Drive Cables

| Cable | Part No. | Length |
|---|---|---|
| BC20J-20 | 7012122-20 | 6 m (20 ft) |
| BC20J-40 | 7012122-40 | 12 m (40 ft) |
| BC20J-60 | 7012122-60 | 18 m (60 ft) |

**NOTE**

**Total length of cable(s) from controller to the last drive must not exceed 30 m (100 ft).**

### FCC Cable Information

### Order Number

| | |
|---|---|
| RLV12-AP | Factory installed shielded cable and filter connector assembly, plus RLV12 option. |
| RLV12 | Disk Controller option only. |
| CK-RLV1A-KA | Cabinet Kit for BA23/Micro |
| CK-RLV1A-KB | Cabinet Kit for H3012/PDP-11/23S |
| CK-RLV1A-KC | Cabinet Kit for H349/PDP-11/23-PLUS |

## Standard Addresses

**Standard Address Assignments**

| Device Address | 16-Bit Addressing | 18-Bit Addressing | 22-Bit Addressing* |
|---|---|---|---|
| Starting address range | 160000-177770 | 760000-777770 | 17760000-17777760 |
| Starting address | 174400 | 774400 | 17774400 |
| Number of registers | 4 | 4 | 8 (5 are used; 3 are not) |
| Registers used | CSR (174400)<br>BAR (174402)<br>DAR (174404)<br>MPR (174406) | CSR (774400)<br>BAR (774402)<br>DAR (774404)<br>MPR (774406) | CSR (17774400)<br>BAR (17774402)<br>DAR (17774404)<br>MPR (17774406)<br>BAE (17774410) |
| **Interrupt Vector** | | | |
| Vector range | 0-774 | 0-774 | 0-774 |
| Standard vector | 160 | 160 | 160 |

*Factory configuration (FCO M8061-002)

## Diagnostic Programs

Refer to Appendix A.

## Related Documentation

*RLV12 Disk Controller User's Guide* (EK-RLV12-UG)
RL01 Field Maintenance Print Set (MP00347)
RL02 Field Maintenance Print Set (MP00553)
*RL01 Disk Drive IPB* (EK-ORL01-IP)
*RL02 Disk Drive IPB* (EK-ORL02-IP)
*RL01/RL02 User's Guide* (EK-RL012-UG)
*RL01/RL02 Pocket Service Guide* (EK-RL012-PG)

## CONFIGURATION

The user or installer can configure and install the RLV12 in a 16-, 18-, or 22-bit LSI-11 bus. The user can select the device address, interrupt vector, and memory parity error abort feature.

### Device Address Selection

Software control of the RLV12 is by means of four or five device registers — CSR, BAR, DAR, MPR, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension register (BAE) is added for upper address bit selection for 22-bit addressing. The usual device starting address is as follows.

**Device Starting Address**

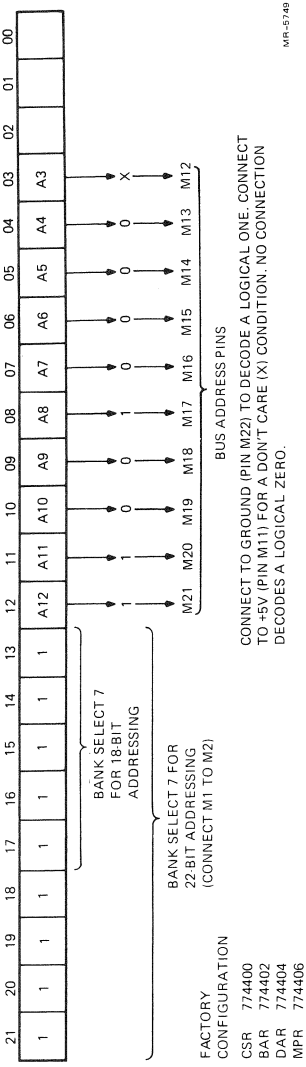
| Addressing Mode | Starting Address (Octal) |
|---|---|
| 16-bit | 174400 |
| 18-bit | 774400 |
| 22-bit | 17774400 |

The first register, the CSR, is assigned the starting address, and the other registers are incremented by 2.

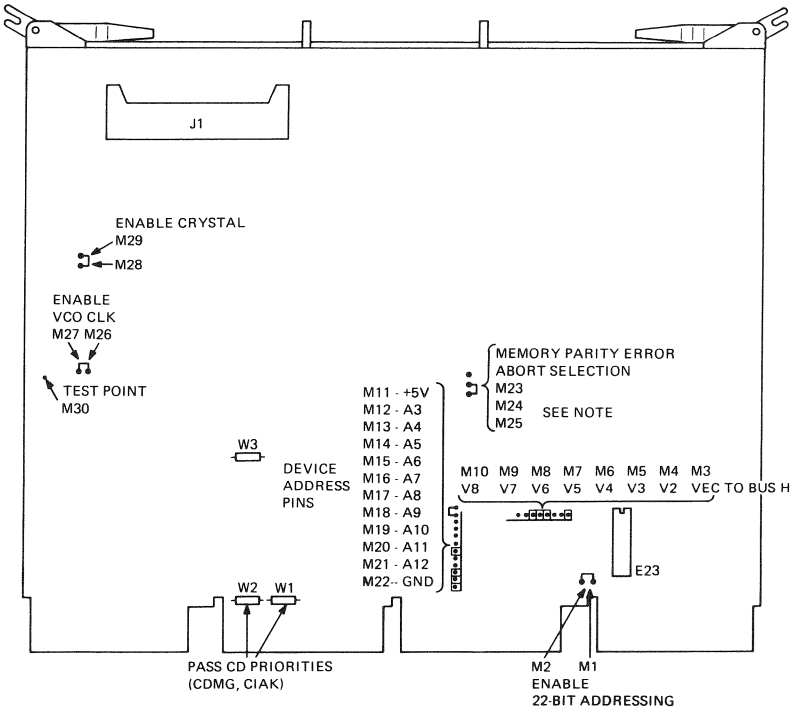
The device starting address is selected by jumpers for bits 03 through 12. A jumper from the selected bit to ground (M22) decodes a 1; no jumper decodes a 0; and a jumper to +5 V (M11) decodes an X (don't care) condition. The following figure shows the RLV12 device starting address format.

**NOTE**

**For 22-bit addressing, bit A3 is not decoded in the starting address.**




RLV12 Device Address Format



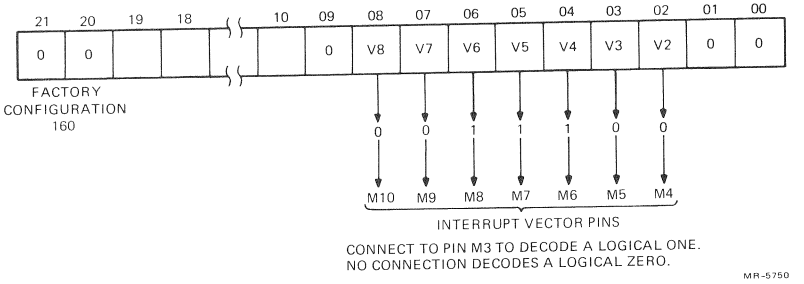

NOTE:
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING. THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS:

| CONNECTION | FUNCTION |
|---|---|
| M23 - M24 | NO PARITY |
| M24 - M25 | PARITY ERROR ABORT |

RLV12 Module Layout

### Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 160. The user may select another vector by changing the jumpers for bits V2-V8. A connection to M3 generates a 1 for that bit; no connection generates a 0. The RLV12 interrupt is at priority level 4.




RLV12 Interrupt Vector Format

### Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit LSI-11 buses. When sent from the factory, the module operates on a 22-bit bus. Jumper M1 to M2 is installed, which enables bank select 7 (BBS7) to be determined by the upper address bits (13-21). When the jumper is removed, the RLV12 has an 18-bit mode bank select 7.

**NOTE**

**The RLV12 may be used in a 16- or 18-bit system while configured to a 22-bit operation (factory-shipped configuration) provided it is the only RLV12 in the system.**

### Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24. This feature does not have to be disabled for nonparity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

**Jumpers That Remain Installed**

The module has two jumpers, W1 and W2, that enable priority signals to pass through the module. The module has these jumpers installed, and they should be left in.

| Jumper | Signal |
|---|---|
| W1 | CIAKI to CIAKO |
| W2 | CDMGI to CDMGO |

One jumper, W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator (VCO) during factory testing. These jumpers should be left in.

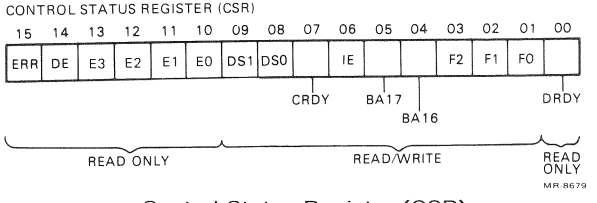
| Jumper | Oscillator |
|---|---|
| M26-M27 | VCO |
| M28-M29 | Crystal |

**CONTROL STATUS REGISTER (CSR)**

The control status register is a 16-bit, word-addressable register with a standard address of 774400 for 18-bit addressing, and 17774400 for 22-bit addressing. Bits 01 through 09 can be read or written; the other bits can only be read. The bit functions are described in the following table.

When the LSI-11 bus is initialized with BINIT L, bits 01-06 and 08-13 are cleared, and bit 07 (CRDY) is set. Bit 00 (DRDY) is set when the selected drive is ready to accept a command; otherwise, this bit is cleared. Bit 14 (DE) is clear as long as there is no drive error. Otherwise, this bit is set and stays set until the drive error is corrected; or if bit 03 (drive reset) is set in the DAR and the controller is sent a get status command, the DE bit is cleared.

Bit 15 (ERR) is set when there is a drive or controller error in bits 10-14.




Control Status Register (CSR)

**RLV12 Control Status Register Bit Assignments**

| Bit | Name | Description |
|---|---|---|
| 00 | DRDY | Drive ready - When set, this bit indicates that the selected drive is ready to receive a command or supply valid read data. The bit is cleared when a seek or head select operation is started and set when the seek operation is completed. |
| 01-03 | F0-F2 | Function code - These bits are the function code set by software to indicate the command to be executed. |

| Function F2 | F1 | F0 | Command | Octal Code |
|---|---|---|---|---|
| 0 | 0 | 0 | Maintenance mode | 0 |
| 0 | 0 | 1 | Write check | 1 |
| 0 | 1 | 0 | Get status | 2 |
| 0 | 1 | 1 | Seek | 3 |
| 1 | 0 | 0 | Read header | 4 |
| 1 | 0 | 1 | Write data | 5 |
| 1 | 1 | 0 | Read data | 6 |
| 1 | 1 | 1 | Read data without header check | 7 |

Command execution starts when CRDY (bit 07) of the CSR is cleared by software. The function code is cleared by initializing the bus (BINIT L).

| | | |
|---|---|---|
| 04, 05 | BA16, BA17 | Extended address bits - These two bits are the upper-order bus address bits for 18-bit buses. These bits are read and written as bits 04 and 05 of the CSR. They function as address bits 16 and 17 of the BAR. Writing bits 04 and 05 of the CSR also writes bits 0 and 1 of the BAE. |
| 06 | IE | Interrupt enable - When CRDY is asserted, bit 06 allows the controller to interrupt the processor. This interrupt occurs at the termination of a command. Once an interrupt request is placed on the LSI-11 bus, it is not removed until acknowledged by the LSI-11 processor even if IE (bit 06) is cleared. This bit is cleared by initializing the bus. |

**RLV12 Control Status Register Bit Assignments (Cont)**

| Bit | Name | Description |
|---|---|---|
| 07 | CRDY | Controller ready - When cleared by software, this bit indicates that the command in bits 01-03 is to be executed. This bit is set by the controller at the completion of a command, at the detection of an error, or by initializing the bus. Software cannot set this bit because registers are not accessible while CRDY is 0. |
| 08, 09 | DS0, DS1 | Drive select - These bits determine which drive will communicate with the controller via the drive bus. These bits are cleared by initializing the bus. |
| 10-13 | E0-E3 | Controller status errors - These bits are the error code set by the controller to indicate one of the following errors. |

| Error Code E3 | E2 | E1 | E0 | Error | Octal Code |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Operation incomplete (OPI) | 1 |
| 0 | 0 | 1 | 0 | Data CRC (DCRC) | 2 |
| 0 | 0 | 1 | 1 | Header CRC (HCRC) | 3 |
| 0 | 1 | 0 | 0 | Data late (DLT) | 4 |
| 0 | 1 | 0 | 1 | Header not found (HNF) | 5 |
| 1 | 0 | 0 | 0 | Nonexistent memory (NXM) | 10 |
| 1 | 0 | 0 | 1 | Parity error abort (PAR ERR) | 11 |

Operation incomplete indicates that the current command was not completed within the OPI timeout period of 550 ms.

A data CRC error indicates that while reading the data field from the disk an error was found.

A header CRC error indicates that while reading the header from the disk an error was found. The CRC check is performed on the first and second header words, although the second header word is always 0.

Data late indicates that the FIFO RAM was more than half full and the controller was not able to read the next sequential sector. This error may occur during a read without header check command.

RLV12 Control Status Register Bit Assignments (Cont)

| Bit | Name | Description |
|---|---|---|
| | | Header not found indicates that an OPI timeout occurred while the controller was searching for the correct sector to read or write. A header compare did not occur.<br><br>A nonexistent memory error indicates that during a DMA transfer the memory location addressed did not respond with RPLY within 10 μs.<br><br>A memory parity error abort indicates that a parity error was detected while reading the system's optional memory that has parity error checking. If an error was detected, the current command to the RLV12 is aborted. |
| 14 | DE | Drive error - This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a get status command. DE will not set ERR (bit 15) or CRDY (bit 07) until the usual occurrence of CRDY. |
| 15 | ERR | Composite error - When set, this bit indicates that one or more of the error bits (bits 10-14) are set. When an error occurs, the current operation terminates and an interrupt routine is started if the interrupt enable bit (bit 06 of the CSR) is set.<br><br>All error bits are cleared by initializing the bus by starting a new command, with the exception of DE and ERR if they were caused by a drive error. |

**BUS ADDRESS REGISTER (BAR)**

The bus address register is a 16-bit, word-addressable register with a standard address of 774402 for 18-bit addressing, and 17774402 for 22-bit addressing. Bits 00 through 15 can be read or written; bit 00 is usually written as 0. The bus address register indicates the memory location for the DMA data transfer during a read or write operation. The register's contents are automatically incremented by 2 as each word is transferred between the system memory and the controller.

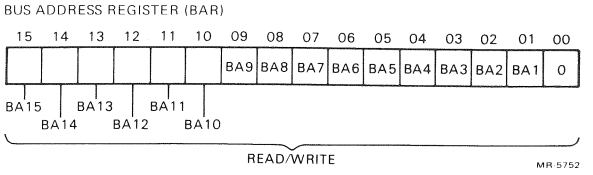
The bus address can be expanded for an 18-bit LSI-11 bus by using bits 04 and 05 (BA 16 and 17) of the CSR or by using bits 00 and 01 of the BAE register.

The bus address can be expanded for a 22-bit LSI-11 bus by using the BAE register (BAE 16-21).

**NOTE**

**When using 22-bit mode, writing CSR bits 04 and 05 modifies BAE bits 00 and 01 and vice versa.**

The BAR is cleared by initializing the bus (BINIT L).




Bus Address Register (BAR)

**DISK ADDRESS REGISTER (DAR)**

The disk address register is a 16-bit, read/write, word-addressable register with a standard address of 774404 for 18-bit addressing, and 17774404 for 22-bit addressing. Its contents have one of three meanings, depending on the command being performed.

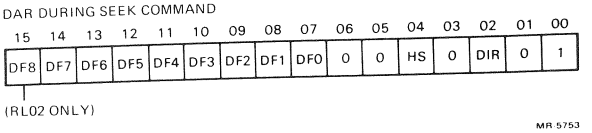
**Disk Address Commands**

| Command | DAR Function |
|---|---|
| Seek | Head selected, number of cylinders to move, direction. |
| Read data or write data | Head selected, cylinder address, sector address. |
| Get status | Send drive status to MPR; reset the error registers. |

The DAR is cleared by initializing the bus (BINIT L).

### DAR During a Seek Command

To perform a seek command, the program must provide the head selected (HS), direction to move (DIR), and the cylinder address difference (DF). The bits are as follows.



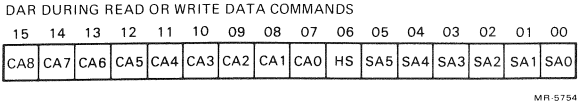

DAR During a Seek Command

**DAR Seek Command Word Format**

| Bit | Name | Description |
|---|---|---|
| 00 | MRKR | Marker - Must be a 1. |
| 01 | None | Must be a 0, indicating to the drive that a seek command is being issued and that the other bits in the register hold the seek specifications. |
| 02 | DIR | Direction - This bit indicates the direction in which the seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 07-15). |
| 03 | None | Must be a 0. |
| 04 | HS | Head select - Indicates which head (disk surface) is to be selected: 1 = lower, 0 = upper. |
| 05, 06 | None | Reserved. |
| 07-15 | DF | Cylinder address difference - Indicates the number of cylinders the heads are to move on a seek. |

### DAR During a Read, Write, or Write Check Command

For a read, write, or write check command, the DAR provides the head selected (HS) and the address of the first sector to be transferred (SA). The bits are described below. As each sector is transferred, the DAR sector address increments by 1.



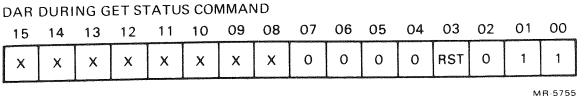

DAR During a Read, Write, or Write Check Command

**DAR Read/Write Data Command Word Format**

| Bit | Name | Description |
|---|---|---|
| 00-05 | SA | Sector address - Address of one of the 40 sectors on a track. (Octal range is 0 to 47.) |
| 06 | HS | Head select - Indicates which head (disk surface) is to be selected: 1 = lower; 0 = upper. |
| 07-15 | CA | Cylinder address - Address of one of the 256 cylinders for RL01 or 512 cylinders for RL02. (Octal range is 0 to 777.) |

### DAR During a Get Status Command

Both the CSR and the DAR must be programmed to perform a get status command. Then a get status command is placed in the CSR. The DAR bits are as follows.




DAR During a Get Status Command

**DAR Get Status Command Word Format**

| Bit | Name | Description |
|---|---|---|
| 00 | MRKR | Marker - Must be a 1. |
| 01 | GS | Get status - Must be a 1, indicating to the drive to send its status word. At the completion of the get status command, the drive status word is read into the controller multipurpose register (MPR). With this bit set, bits 08-15 are ignored by the drive. |
| 02 | None | Must be a 0. |
| 03 | RST | Reset - When this bit is set, the disk drive clears its error register of soft errors before sending a status word to the controller. |
| 04-07 | None | Must be a 0. |
| 08-15 | None | Not used. |

**MULTIPURPOSE REGISTER (MPR)**

The multipurpose register is a 16-bit, read/write, word-addressable register. It is accessed using the standard address of 774406 for 18-bit addressing, and 17774406 for 22-bit addressing. Following a read header command or a get status command, reading the MPR obtains sector header or drive status information.

Writing to the MPR is used to set the word count. The word count is cleared by initializing the bus (BINIT L).

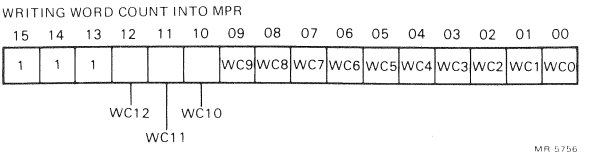
**Writing the MPR to Set the Word Count**

Before starting a DMA transfer, the MPR is loaded with the word count. The program must load the MPR with the 2's complement of the number of words to be transferred. The bits are described below. As each word is transferred, the MPR is automatically incremented by 1. The reading or writing operation continues until a word count overflow occurs, indicating that all words have been transferred.

The word count can range from 1 to 5120 data words. The maximum word count is limited by the maximum number of sectors available (40) and the maximum words per sector (128).

**NOTE**

**Once written, the word count cannot be read back. Reading the MPR does not change the word count.**



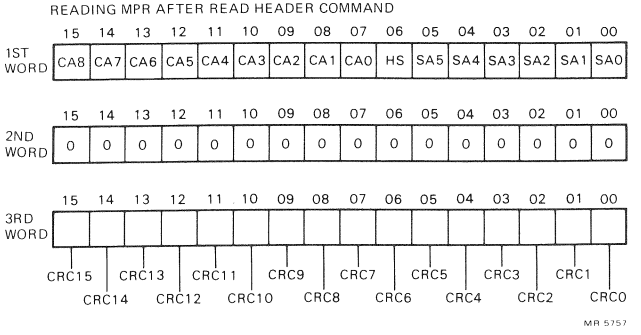

Writing the MPR to Set the Word Count

**MPR Word Count Format**

| Bit | Name | Description |
|---|---|---|
| 00-12 | WC | Word count - This is the 2's complement of the total number of words to be transferred. |
| 13-15 | None | Must be all ones for word count in correct range. |

**Reading the MPR After a Read Header Command**

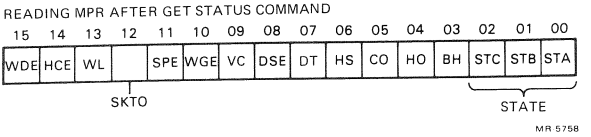
When a read header command is executed, three words can be sequentially read from the MPR, as the following figure shows. The first word includes the sector address, the head selected, and the cylinder address. The second word is all zeros. CRC information is the header for the third word.




Reading the MPR After a Read Header Command (Three Header Words)

### Reading the MPR After a Get Status Command

After a get status command is executed, a status word is stored in the MPR. The status word from the selected disk drive includes information on the functional state of the drive and any drive errors. The bits are described in the following table.




Reading the MPR After a Get Status Command

**MPR Status Word Format**

| Bit | Name | Description |
|---|---|---|
| 00-02 | STA, STB, STC | These bits (A, B, and C) define the state of the drive as follows. |

| C | B | A | State of Drive |
|---|---|---|---|
| 0 | 0 | 0 | Load state |
| 0 | 0 | 1 | Spin up |
| 0 | 1 | 0 | Brush cycle |
| 0 | 1 | 1 | Load heads |
| 1 | 0 | 0 | Seek track counting |
| 1 | 0 | 1 | Seek linear mode (lock on) |
| 1 | 1 | 0 | Unload heads |
| 1 | 1 | 1 | Spin down |

| | | |
|---|---|---|
| 03 | BH | Brush home - Asserted when the brushes are not over the disk. |
| 04 | HO | Heads out - Asserted when the heads are over the disk |
| 05 | CO | Cover open - Asserted when the cover is open or the dust cover is not in place. |
| 06 | HS | Head select - Indicates the head selected: 1 = lower, 0 = upper. |

**MPR Status Word Format (Cont)**

| Bit | Name | Description |
|---|---|---|
| 07 | DT | Drive type - Indicates the type of disk drive: 0 = RL01, 1 = RL02. |
| 08 | DSE | Drive select error - Indicates multiple drive selection is detected. |
| 09 | VC | Volume check - VC is set every time the drive goes into load heads state. This asserts a drive error at the controller, but not on the front panel. VC is an indication that the program does not know which disk is present until it has read the serial number and bad sector file. (The disk might have been changed while the heads were unloaded.) |
| 10 | WGE | Write gate error - Indicates that the write gate was asserted when the drive was not ready, the sector pulse was asserted, or the drive was write locked. |
| 11 | SPE | Spin error - Indicates that the spindle did not reach full speed within a specific time, or that it is turning too fast. |
| 12 | SKTO | Seek time out - Indicates that the heads did not come onto track within a specific time during a seek command. |
| 13 | WL | Write lock - Indicates write lock status of selected drive: 0 = unlocked; 1 = protected. |
| 14 | HCE | Head current error - Indicates that write current was detected in the heads when write gate was not asserted. |
| 15 | WDE | Write data error - Indicates write gate was asserted, but no pulses were detected on the write data line. |

## BUS ADDRESS EXTENSION REGISTER (BAE)

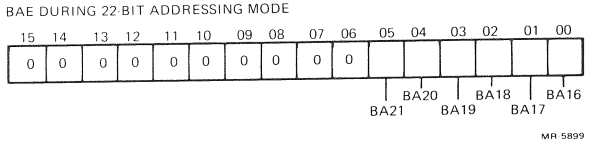
The bus address extension register is a 6-bit read/write register used to drive address bits 16-21 for a 22-bit LSI-11 bus. The BAE has a standard address of 17774410 for 22-bit addressing. A write to the BAE loads TS DAL 0-5 into BAE 0-5. Reading the BAE enables bank select 7 (BBS7 L) to the LSI-11 bus. (A jumper must be connected between M1 and M2 on the controller to enable 22-bit addressing.) When address bits 13-21 are all ones, the RLV12 drives BBS7 L to direct data to the I/O page.

The two least significant bits of the BAE (bus address lines 16 and 17) are mirrored in bits 04 and 05 of the CSR. The same bits can be read or written as CSR bits 04 and 05 or BAE bits 00 and 01.

**NOTE**

**Writing CSR bits 04 and 05 modifies BAE bits 0 and 1 and vice versa.**

The BAE register is cleared by initializing the bus (BINIT L).




BAE Register Word Format

# RQDX1 AND EXTENDER CONTROLLER MODULE (RX50, RD51, RD52)

**Amps**

| +5 V | +12 Vdc |
|---|---|
| 6.4 A | 7.3 mA |
| 8 A (max.) | 10 mA (max.) |

**Bus Loads**

| AC | DC |
|---|---|
| 2.5 | 1 |

**Standard Addresses**

| Address Mode | Octal Address |
|---|---|
| 16-bit | 172150 |
| 18-bit | 772150 |
| 22-bit | 17772150 |

**Vectors**

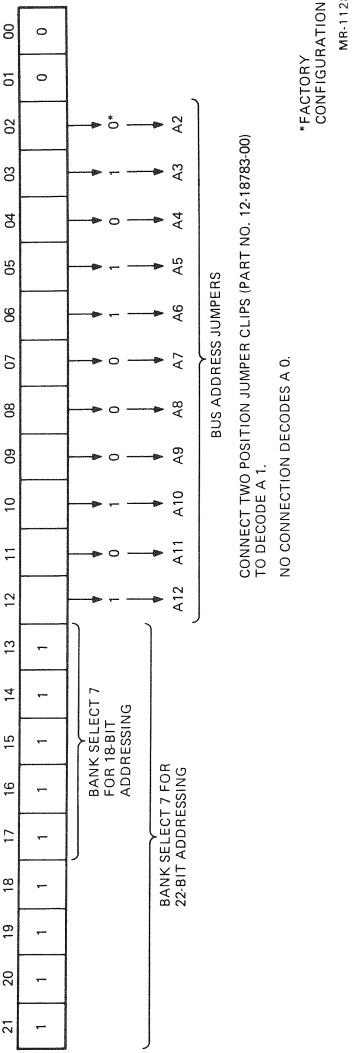
Software selectable (normally set to 154)

**Diagnostic Programs**

ZRQA?? BIN RDRX Performance Exerciser
ZRQB?? BIN RDRX Formatter (RD51)

**Related Documentation**

RQDX1 Field Maintenance Print Set (MP01731-01)
UDA50 Programmers Document Kit (QP-905-GZ)
*RQDX1 Controller Modules User's Guide* (EK-RQDX1-UG)



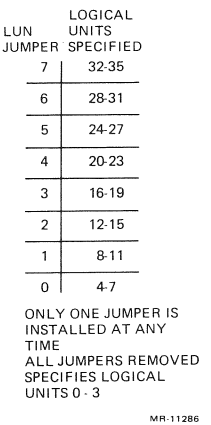

RQDX1 Address Selection Jumper Format

**RQDX1 Standard Address Jumper Configuration**

| Jumper | State | |
|---|---|---|
| A2 | OUT | Address selection (772150) |
| A3 | IN | |
| A4 | OUT | |
| A5 | IN | |
| A6 | IN | |
| A7 | OUT | |
| A8 | OUT | |
| A9 | OUT | |
| A10 | IN | |
| A11 | OUT | |
| A12 | IN | |

## LOGICAL UNIT NUMBER SELECTION

The location of the RQDX1 controller module logical unit number jumpers is shown below. These jumpers are set to the lowest logical unit number assigned to any disk/diskette drive controlled by the module. The controller module automatically sizes the logical unit configuration during initialization to determine how many (of four possible units) are actually present. This automatic sizing eliminates the need for the reconfiguration of jumpers when units (RD51 or RX50 drives) are added to or removed from the controller module. The standard configuration for the logical unit number jumpers (selecting logical unit number 0) is listed. To configure the module for logical unit numbers beginning with other than unit number 0, use the format shown below to determine the appropriate jumper configuration.




RQDX1 Logical Unit Number Jumper Format

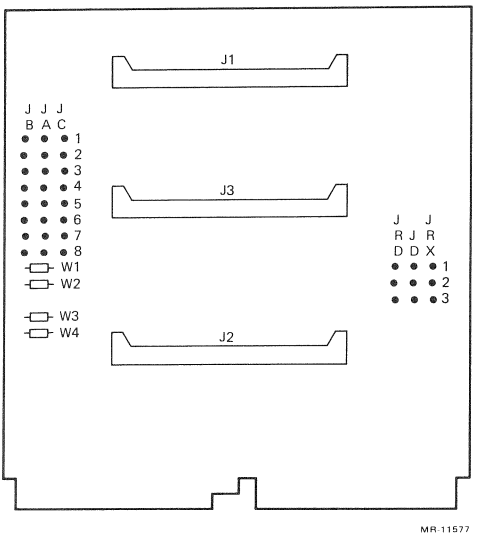
**RQDX1 Standard Logical Unit Number Jumper Configuration**

| Jumper | State | |
|---|---|---|
| LUN1 | OUT | Logical unit number (0)* |
| LUN2 | OUT | |
| LUN3 | OUT | |
| LUN4 | OUT | |
| LUN5 | OUT | |
| LUN6 | OUT | |
| LUN7 | OUT | |
| LUN8 | OUT | |

This indicates that logical unit numbers 0–3 are assigned to this controller module. The controller will automatically determine if less than four logical units are present.

**RQDX1-E Extender Module Jumper Configuration**

The RQDX1-E extender module is a dual-height module that provides signal connectors and requires appropriate jumper configurations. The J2 connector receives signals from the RQDX1 controller module. The other connectors (J1 and J3) distribute these signals to the disk and diskette drives. Jumper functions for the RQDX1-E extender module, as well as the jumpers installed in the factory configuration, are listed.




RQDX1-E Extender Module Jumper Locations

**RQDX1-E Extender Module Jumper Configuration**

| Jumpers | Functions | Factory Configuration* |
|---|---|---|
| W1–W4 | Must be installed (Manufacturing use only) | W1–W4 |
| JRD1–JRD3<br>JD1–JD3<br>JRX1–JRX3 | Select the external drive to be connected to the J3 connector | JD1 to JRD1<br>JD2 to JRD2<br>JD3 to JRD3 |
| JB1–JB8<br>JA–JA8<br>JC–JC8 | Determine which connector (J2 or J3) the RD read/write will connect to | JA2 to JC2<br>JA2 to JC2<br>JA3 to JB3<br>JA4 to JB4<br>JA5 to JB5<br>JA6 to JB6<br>JA7 to JC7<br>JA8 to JC8 |

* Factory configuration is set to connect an external RD51 disk drive to connector J3. To configure the module for an external RX50 (connected to J3), jumpers JD1 through JD3 are connected to JRX1 through JRX3 and jumpers JA1 through JA8 are connected to JB1 through JB8.

**Interrupt Vector**

The interrupt vector has a range of 0 to 774 and is software selectable. A vector selected by software must be greater than 0. The normal interrupt vector used by the RQDX1 controller module is 154.

**Interrupt Request Level**

The RQDX1 controller module interrupts at priority level 4 are determined by E3, a DC003 chip.

## RQDX1 CONTROLLER MODULE INSTALLATION

The RQDX1 module (M8639) is typically installed in the last occupied slot of the backplane. If empty slots are left between the other modules and the M8639 module, install grant cards (part no. G7272) in those empty slots to accommodate the interrupt and direct memory access structure of the backplane.

Before installing the module, make sure that the address and logical unit number jumpers are properly configured.

Install the 50-conductor signal cable (part no. BC02D-1D) to the J1 connector on the M8639 module. This cable must be connected to a signal distribution panel that will connect the appropriate signals to the RD51 and/or RX50 drives. An example of the MICRO/PDP-11 signal distribution panel connecting the M8639 module to an RD51 disk drive and an RX50 diskette drive is on the next page. The RD51 disk drive requires two signal cable connections. One is a 20-conductor cable (part no. 17-00282-00), the other is a 34-conductor cable (part no. 17-00286-00). The RX50 diskette drive requires a single 34-conductor signal cable (part no. 17-00285-02).

## RQDX1-E EXTENDER MODULE OPTION

Typically, in the MICRO/PDP-11, the RQDX1 controller module is located in the same mounting box as the disk and/or diskette drives that it controls. However, if the system mounting box cannot hold all of these drives, the optional RQDX1-E extender module may be used to connect the RQDX1 controller module signals to any drive that is external from the system mounting box.

**NOTE**

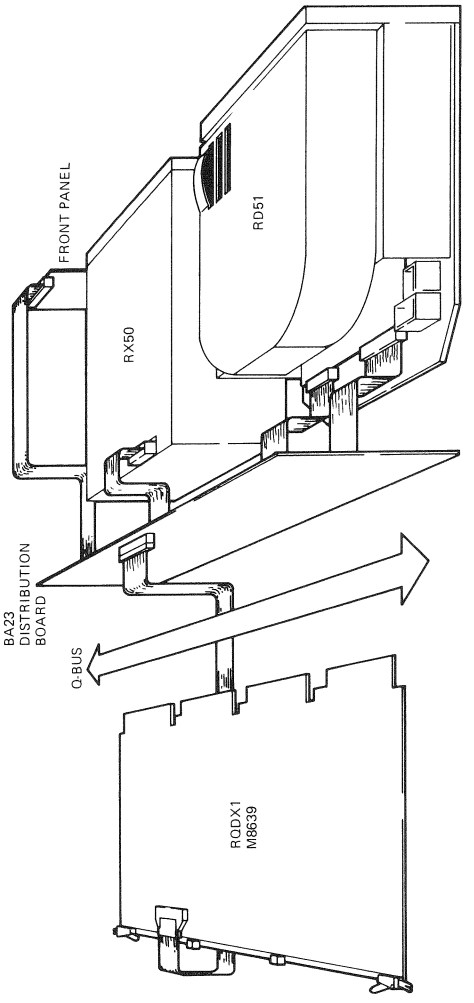
**Jumper selection (for configurations listed) is made by attaching two-position jumper clips (part no. 12-18783-00).**

## RQDX1-E EXTENDER MODULE INSTALLATION

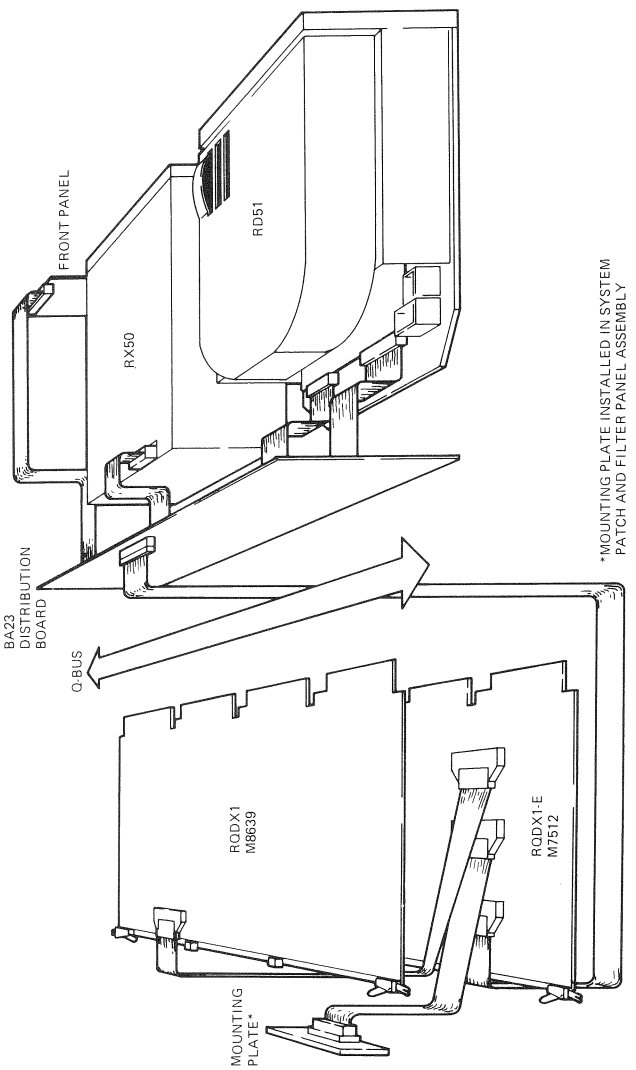
Installation of the RQDX1-E extender module option in the MICRO/PDP-11 system (BA23 mounting box) is as follows. The M7512 dual-height module is installed in the backplane slot directly below the M8639 (RQDX1) module, in connectors A and B. A cable (part no. BC02D-0K) connects the RQDX1 controller module to the RQDX1-E extender module through the J2 connector. Another cable (part no. 70-18652-01), attached to the J3 connector, connects the RQDX1-E extender module to a mounting plate (part no. 74-2866-01). This is mounted to the system's patch and filter panel assembly. The entire cable and mounting plate assembly may be ordered as part number 70-20691-01. This external plate provides the signals to be sent to the external drive. A third cable (part no. BC02D-1D – attached to the J1 connector on the RQDX1-E extender module) is connected to the signal distribution panel in the mounting box, providing signals to the disk or diskette drives that are installed in the system mounting box.

### Cable Signals

RQDX1 controller module signals on the J1 connector.




RQDX1 MICRO/PDP-11 Signal Distribution Connections




RQDX1-E Extender Module Connections

**J1 Connector Signals**

| J1 Pin | Signal Name |
|---|---|
| 1 | MFMWRTDT1 (H) (RD51 only signal) |
| 2 | MFMWRTDT1 (L) (RD51 only signal) |
| 3 | GROUND |
| 4 | HEAD SEL 2 (L) (RDXX only signal)* |
| 5 | GROUND |
| 6 | SEEKCPLT (L) (RD51 only signal) |
| 7 | RD1 RDY (H) (RD51 only signal) |
| 8 | WRT FAULT (L) |
| 9 | DRVBUSOE (L) |
| 10 | HEAD SEL 1 (L) (RD51 only signal) |
| 11 | RX0WPTLED (L) (RX50 only signal) |
| 12 | RD0 RDY (H) (RD51 only signal) |
| 13 | RX1WPTLED (L) (RX50 only signal) |
| 14 | DRVSL0ACK (L) (RD51 only signal) |
| 15 | MFMRDDAT0 (H) (RD51 only signal) |
| 16 | MFMRDDAT0 (L) (RD51 only signal) |
| 17 | MFMWRTDT0 (H) (RD51 only signal) |
| 18 | MFMWRTDT0 (L) (RD51 only signal) |
| 19 | MFMRDDAT1 (H) (RD51 only signal) |
| 20 | MFMRDDAT1 (L) (RD51 only signal) |
| 21 | GROUND |
| 22 | REDUCWRTI (L) |
| 23 | RD0WRTPRO (L) (RD51 only signal) |
| 24 | DRV SEL 4 (L) |
| 25 | GROUND |
| 26 | INDEX (L) |
| 27 | RD1WRTPRO (L) (RD51 only signal) |
| 28 | DRV SEL 1 (L) |
| 29 | DRV SEL 2 (L) |
| 30 | DRV SEL 3 (L) |
| 31 | RX2WPTLED (L) (RX50 only signal) |
| 32 | RXMOTORON (L) (RX50 only signal) |
| 33 | GROUND |
| 34 | DIRECTION (L) |
| 35 | GROUND |
| 36 | STEP (L) |
| 37 | GROUND |
| 38 | RXWRTDATA (L) (RX50 only signal) |
| 39 | GROUND |

*Reserved for future use.

**J1 Connector Signals (Cont)**

| J1 Pin | Signal Name |
|---|---|
| 40 | WRT GATE (L) |
| 41 | GROUND |
| 42 | TRACK 00 (L) |
| 43 | RX3WPTLED (L) (RX50 only signal) |
| 44 | DRVSL1ACK (L) (RD51 only signal) |
| 45 | GROUND |
| 46 | READ DATA (L) (RX50 only signal) |
| 47 | GROUND |
| 48 | HEAD SEL 0 (L) |
| 49 | GROUND |
| 50 | READY (L) |

**RD51 Disk Drive J1 Signal Connector Pin Assignments**

| GND Return Pin | Signal Pin | Signal Name |
|---|---|---|
| 1 | 2 | Reserved |
| 3 | 4 | Head select 2 |
| 5 | 6 | Write gate |
| 7 | 8 | Seek complete |
| 9 | 10 | Track 0 |
| 11 | 12 | Write fault |
| 13 | 14 | Head select 0 |
| 15 | 16 | Reserved (to J2 pin 7) |
| 17 | 18 | Head select 1 |
| 19 | 20 | Index |
| 21 | 22 | Ready |
| 23 | 24 | Step |
| 25 | 26 | Drive select 1 |
| 27 | 28 | Drive select 2 |
| 29 | 30 | Drive select 3 |
| 31 | 32 | Drive select 4 |
| 33 | 34 | Direction in |

**RD51 Disk Drive J2 Signal Connector Pin Assignments**

| GND Return Pin | Signal Pin | Signal Name |
|---|---|---|
| 2 | 1 | Drive selected |
| 4 | 3 | Reserved |
| 6 | 5 | Reserved |
| 8 | 7 | Reserved (to J1 pin 16) |
| | 9, 10 | Reserved |
| 12 | 11 | GND |
| | 13 | +MFM write data |
| | 14 | –MFM write data |
| 16 | 15 | GND |
| | 17 | +MFM read data |
| | 18 | –MFM read data |
| 20 | 19 | GND |

**RD51 Disk Drive J3 Power Connector Pin Assignments**

| GND Return Pin | Signal Pin | Signal Name |
|---|---|---|
| 2 | 1 | +12 V |
| 3 | 4 | +5 V |

### RX50 Diskette Drive J1 Connector Pin Assignments

| GND Return Pin | Signal Pin | Signal Name |
|---|---|---|
| 1 | 2 | TK43L (controls write current level) |
| 3 | 4 | Reserved |
| 5 | 6 | Drive select 3 L |
| 7 | 8 | Index L |
| 9 | 10 | Drive select 0 L |
| 11 | 12 | Drive select 1 L |
| 13 | 14 | Drive select 2 L |
| 15 | 16 | Motor on L |
| 17 | 18 | Direction (head movement direction) |
| 19 | 20 | Step L (head movement distance) |
| 21 | 22 | Write data L |
| 23 | 24 | Write gate L |
| 25 | 26 | Track 0 L |
| 27 | 28 | Write protect L |
| 29 | 30 | Read data L |
| 31 | 32 | Reserved |
| 33 | 34 | Ready L |

### RX50 Diskette Drive J3 Power Connector Pin Assignments

| GND Return Pin | Signal Pin | Signal Name |
|---|---|---|
| 2 | 1 | +12 V |
| 3 | 4 | +5 V |

# RXV11 FLOPPY DISK INTERFACE

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 1.5 max. | 0 | 1.74 | 1 | BC05L |

## Standard Addresses

| | First Device | Second Device |
|---|---|---|
| RXCS | 177170 | 177150 |
| RXDB | 177172 | 177152 |
| Vector | 264 | 270 |

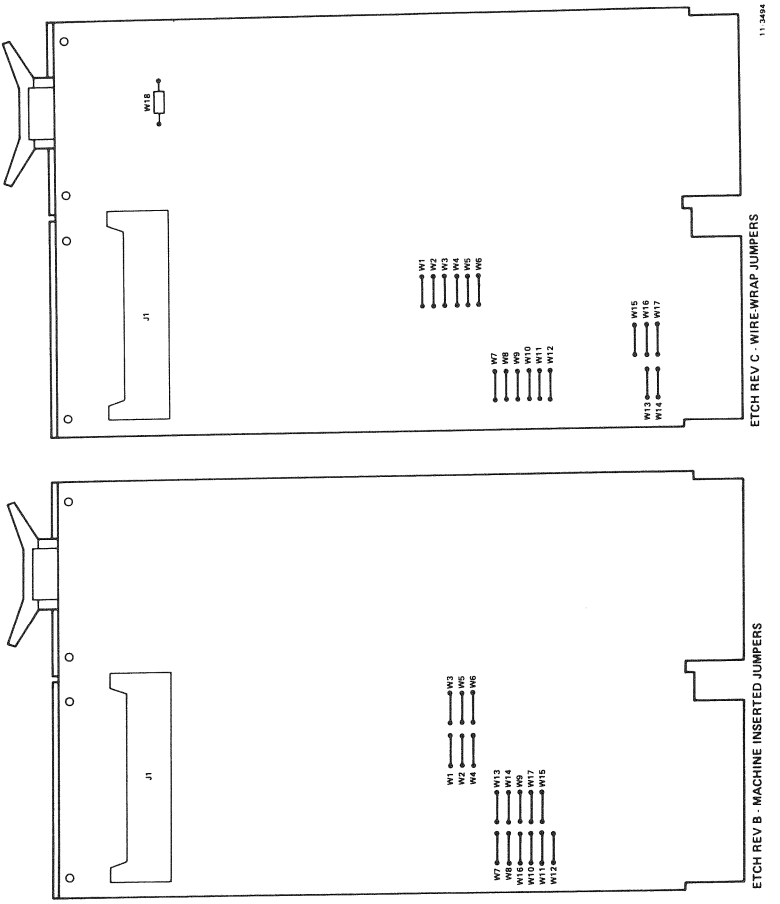
## Diagnostic Programs

Refer to Appendix A.

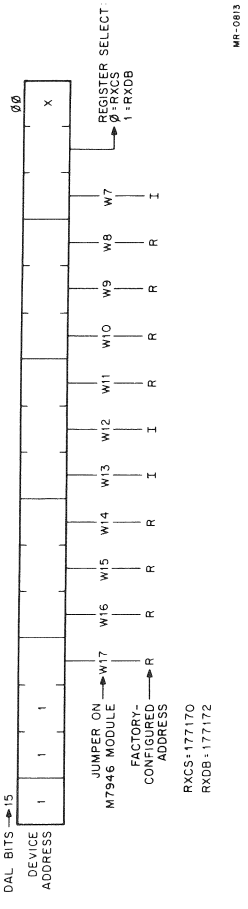
**NOTE**
**Run DZRXB before DZRXA.**

## Related Documentation

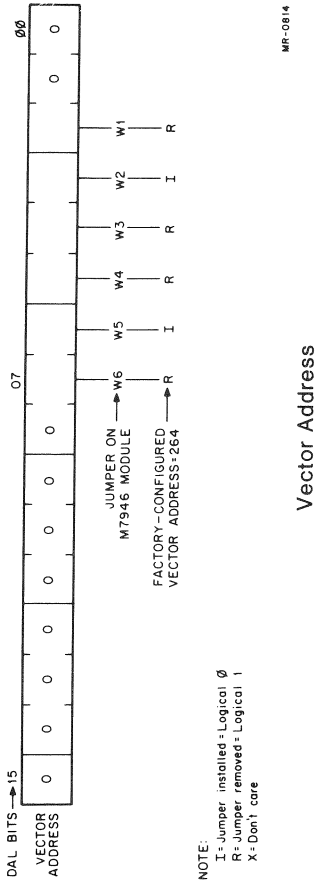
*RXV11 User's Manual* (EK-RXV11-OP-001)
Field Maintenance Print Set (MP00024)
*Microcomputer Interfaces Handbook* (EB-20175-20)




RXV11 Jumpers




Device Address




Vector Address

NOTE:
I = Jumper installed = Logical Ø
R = Jumper removed = Logical 1
X = Don't care

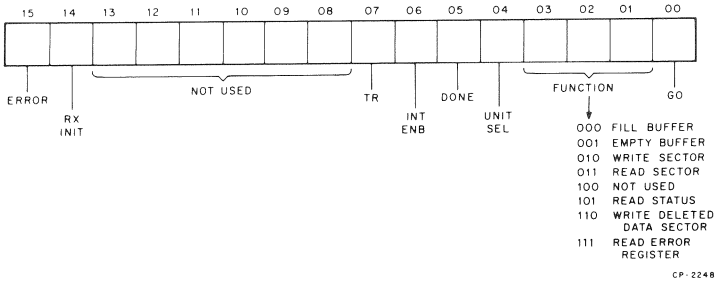
| Unit | Address | Address Jumpers | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | W17 | W16 | W15 | W14 | W13 | W12 | W11 | W10 | W9 | W8 | W7 |
| First (Drives 0, 1) | 177170 | R | R | R | R | I | I | R | R | R | R | I |
| Second (Drives 2, 3) | 177150 | R | R | R | R | I | I | R | R | I | R | I |

| Unit | Vector | Vector Jumpers | | | | | |
|---|---|---|---|---|---|---|---|
| | | W6 | W5 | W4 | W3 | W2 | W1 |
| First (Drives 0, 1) | 264 | R | I | R | R | I | R |
| Second (Drives 2, 3) | 270 | R | I | R | R | R | I |

## NOTES

1. **When inserting the cable in the RXV11 interface module, the red edge of the cable should be at the center of the module (near the pin A end of J1).**

2. **BUS INIT – Install W18 to pass bus INIT to the RX01 as initialize.**




Receiver Control/Status Register (RCSR)

### Bit Definitions

| Bit | Function |
|---|---|
| 0 | Go - Initiates a command to RX01. Write only. |
| 1-3 | Function Select - These bits code one of the eight possible functions. Write only. |
| 4 | Unit Select - This bit selects one of the two possible disks for execution of the desired function. Write only. |
| 5 | Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RXCS bit 6) is set. Read only. |
| 6 | Interrupt Enable - This bit is set by the program to enable an interrupt when the RX01 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RXV11 initialize bit (RXCS bit 14). Read/write. |

**Bit Definitions (Cont)**

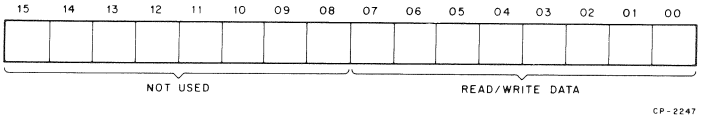
| Bit | Function |
|---|---|
| 7 | Transfer Request - This bit signifies that the RXV11 needs data or has data available. Read only. |
| 8-13 | Unused. |
| 14 | RXV11 Initialize - This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 bus. Write only.<br><br>**CAUTION**<br><br>**1. Loading the lower byte of the RXCS will also load the upper byte of the RXCS.**<br><br>**2. Setting this bit (BIS instruction) will not clear the interrupt enable bit (RXCS bit 06).**<br><br>Upon setting this bit in the RXCS, the RXV11 will negate done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the RX01 will zero the error and status register, set initialize done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 and drive 0. |
| 15 | Error - This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the initialize bit. When an error is detected, the RXES is automatically read into the RXDB. |

The RXDB register serves as a general purpose data path between the RX01 and the RXV11 interface. It may represent one of five RX01 registers according to the protocol of the command function in progress. The RX01 registers include RXDB, RXTA, RXSA, RXES, and RXER.

**CAUTION**

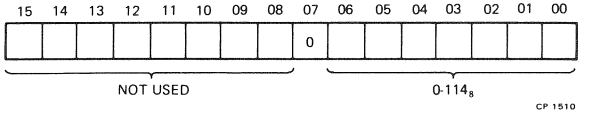
**Violation of protocol in manipulation of this register may cause permanent data loss. Refer to** *RXV11 User's Manual.*

**RXDB-RX Data Buffer** – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.



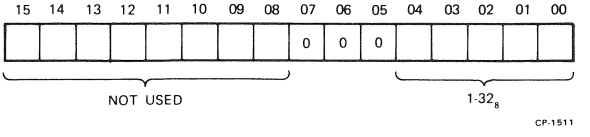

RXDB Format

**RXTA-RX Track Address** – This register is loaded to indicate on which of the 114 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



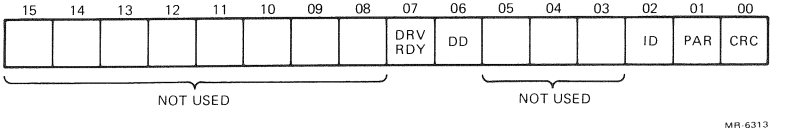

RXTA Format

**RXSA-RX Sector Address** – This register is loaded to indicate on which of the 32 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.




RXSA Format

**RXES-RX Error and Status** – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function.




RXES Format

**RXDB Bit Definitions**

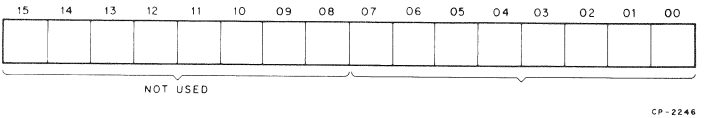
| Bit | Function |
|---|---|
| 0 | CRC Error - A cyclic redundancy check error was detected as information was received from a data field of the diskette. The RXES is moved to the RXDB, and error and done are asserted. |
| 1 | Parity Error - A parity error was detected on command or on address information being transferred to the RX01 from the LSI-11 bus interface. A parity error indication means that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and the error and done are asserted. |
| 2 | Initialize Done - This bit is asserted in the RXES to indicate completion of the initialize routine, which can be caused by RX01 power failure, system power failure, or programmable or LSI-11 bus initialize. |
| 3-5 | Unused. |
| 6 | Deleted Data Detected - During data recovery, the identification mark preceding the data field was decoded as a deleted data mark. |
| 7 | Drive Ready - This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed. |

**NOTES**

1. **The drive ready bit is valid only when retrieved via a read status function or at completion of initialize when it indicates status of drive 0.**

2. **If the error bit was set in the RXCS but error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a read error register function.**

**RXER-RX Error –** This register is located in the RX01 and contains specific RX01 error information. This information is normally accessed when the RXCS error bit 15 is set but RXES error bits 0 and 1 are not set. This is a read-only register.




RXER Format

| Octal Code | Error Code Meaning |
|---|---|
| 0010 | Drive 0 failed to see home on initialize. |
| 0020 | Drive 1 failed to see home on initialize. |
| 0030 | Found home when stepping out 10 tracks for INIT. |
| 0040 | Tried to access a track greater than 77. |
| 0050 | Home was found before desired track was reached. |
| 0060 | Self-diagnostic error. |
| 0070 | Desired sector could not be found after looking at 52 headers (two revolutions). |
| 0110 | More than 40 microseconds and no SEP clock seen. |
| 0120 | A preamble could not be found. |
| 0130 | Preamble found but no I/O mark found within allowable time span. |
| 0140 | CRC error on a header; no flag. |
| 0150 | The header track address of a good header does not compare with the desired track. |
| 0160 | Too many tries for an ID address mark. |
| 0170 | Data mark not found in allotted time. |
| 0200 | CRC error on reading the sector from the disk. No code appears in the ERREG. |
| 0210 | Parity error on some word from interface. |

# RXV21 FLOPPY DISK CONTROLLER

| Amps | | Bus Loads | | Cables |
|---|---|---|---|---|
| +5 | +12 | AC | DC | |
| 1.8 | | 3.0 | 1.0 | BC05L-15 |

**Standard Addresses**

| | First Controller | Second Controller |
|---|---|---|
| RXCS | 177170 | 177200 |
| RXDB | 177172 | 177202 |

**Standard Vectors**

264 270

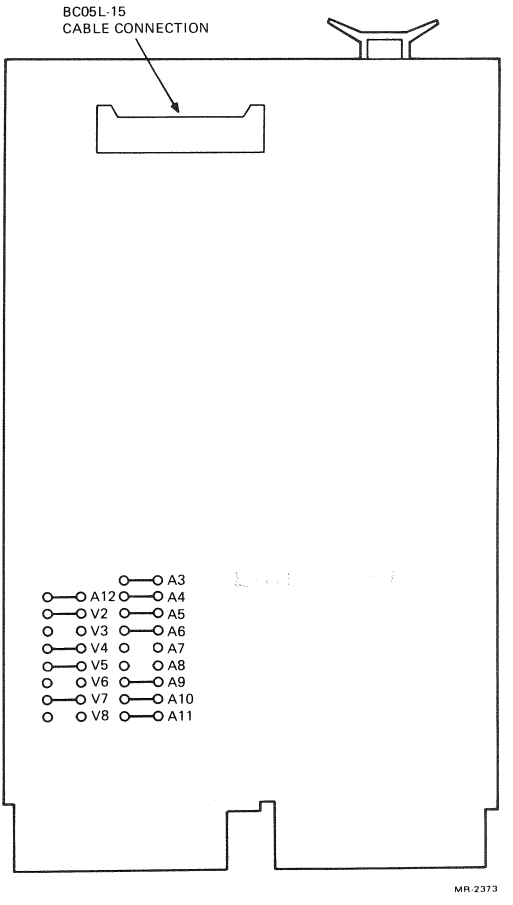
**Diagnostic Programs**

Refer to Appendix A.

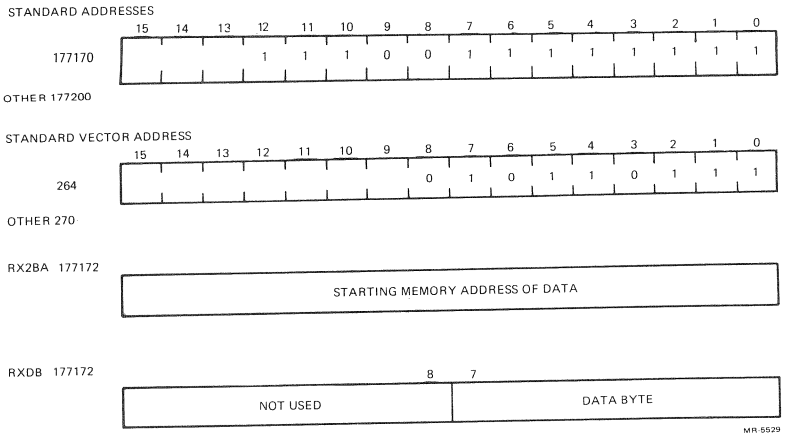
**Related Documentation**

RXV21 Field Maintenance Print Set (MP00628)
*RX02 Floppy Disk System User's Guide* (EK-RX02-UG)
RX01/RX02 Reference Card (EK-RX102-RC)
*RX02 Technical Manual* (EK-0RX02-TM)
*Minicomputer Interfaces Handbook* (EB-20175-20)
RX02 Field Maintenance Print Set (MP-00629-00)

**CAUTION**
**PDP-11/23 systems require the M8029 to be at CS revision E1 or higher.**




M8029 Module Address and Vector Jumpers




RXV21 Error Codes

**Error Codes**

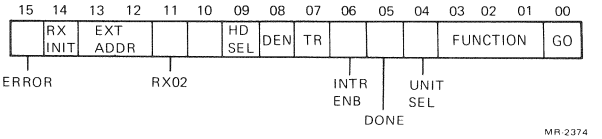
**Error Reg**

| 15 14 13 12 11 10 9 8<br>**Track addr sel DV** | 7<br>**DV SEL** | 6<br>**DEN DV1** | 5<br>**HD LD** | 4<br>**DEN DVO** | 3 | 2 | 1 | 0<br>**DEN CMD** |
|---|---|---|---|---|---|---|---|---|
| Target Sector | Target Track | | | | | | | |
| Current Track DV1 | Current Track DVO | | | | | | | |
| Word Count Reg | Error Code | | | | | | | |

The following sequence is used to get definitive error information following a bootstrap operation. (It is assumed that the bootstrap program has halted and the CPU is in ODT.)

1. Examine R5 (RF will contain RXES after an error).
2. Examine RXER by:

   - Loading the READ ERROR REGISTER command into RX2CS (777170/XXXXXX 17<CR>).
   - Examining the four words of error information that will be transferred into locations 2000, 2002, 2004, and 2006.
   - Reading and decoding this information using the format shown below. The error code can be used to help identify the failing FRU.




RX2CS Format RXV21

**Bit Definitions**

| Bit | Function |
|---|---|
| 0 | Go - Initiates a command to RX02. Write only. |
| 1-3 | Function Select - These bits code one of the eight possible functions described below. Write only.<br><br>**Code** **Function**<br><br>000 Fill Buffer<br>001 Empty Buffer<br>010 Write Sector<br>011 Read Sector<br>100 Set Media Density<br>101 Read Status<br>110 Write Deleted Data Sector<br>111 Read Error Code |
| 4 | Unit Select - This bit selects one of the two possible disks for execution of the desired function. This bit is readable only when done is set, at which time it indicates the unit previously selected. Read/write. |
| 5 | Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RX2CS bit 6) is set. Read only. |
| 6 | Interrupt Enable - This bit is set by the program to enable an interrupt when the RX02 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. Read/write; cleared by initialize. |
| 7 | Transfer Request - This bit signifies that the RXV21 needs data or has data available. Read only. |
| 8 | Density - This bit determines the density of the function to be executed. This bit is readable only when done is set, at which time it indicates the density of the function previously executed. Read/write. |

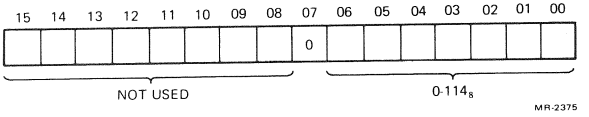
**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 9 | Head Select - This bit selects one of two heads for double-sided operation, readable only when done is set. At that time the side that was previously selected is not valid. |
| 10 | Reserved for future use. Must be written as a 0. |
| 11 | RX02 - This bit is set by the interface to inform the programmer that this is an RX02 system. Read only. |
| 12-13 | Extended Address - These bits are used to declare an extended bus address. Write only. |
| 14 | RXV21 Initialize - This bit is set by the program to initialize the RXV21 without initializing all devices on the UNIBUS. Write only. |

**CAUTION**

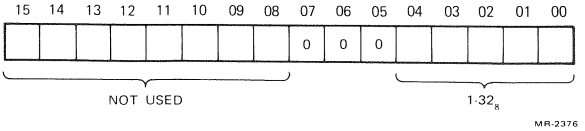
**Loading the lower byte of the RX2CS will also load the upper byte of the RX2CS.**

| | |
|---|---|
| | Upon setting this bit in the RX2CS, the RXV21 will negate done and move the head position mechanism of both drives (if two are available) to track 0. Upon completion of a successful initialize, the RX02 will zero the error and status register, and set initialize done. It will also read sector 1 of track 1 on drive 0 into the buffer. |
| 15 | Error - This bit is set by the RX02 to indicate that an error has occurred during an attempt to execute a command. Read only; cleared by the initiation of a new command or an initialize. |



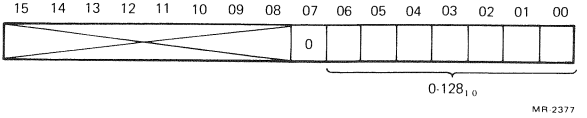

RX2TA Format (RXV21)

**RX2TA (RX Track Address) –** This register is loaded to indicate on which of the $114_8$ ($0-76_{10}$) tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8-15 are unused and are ignored by the control.



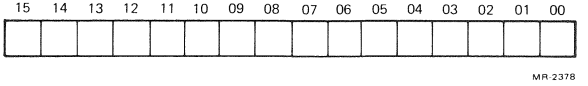

RX2SA Format (RXV21)

**RX2SA (RX Sector Address)** – This register is loaded to indicate on which of the $32_8$ ($1-26_{10}$) sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.




RX2WC Format (RXV21)

**RX2WC (RX Word Count Register)** – For a double-density sector, the maximum word count is $128_{10}$. For a single-density sector the maximum word count is $64_{10}$. If a word count is beyond the limit for the density indicated, the control asserts word count overflow (bit 10 of RX2ES). This is a write-only register. The actual word count, and not the 2's complement of the word count, is loaded into the register.




RX2BA and RX2DB Format (RXV21)

**RX2BA (RX Bus Address Register)** – This register specifies the bus address of data transferred during fill buffer, empty buffer, and read definitive error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is loaded with the address of the first data word to be transferred. This is a 16-bit, write-only register.

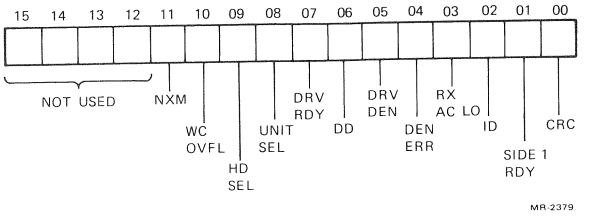
**RX2DB (RX Data Buffer)** – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

**RX2DB (Data Buffer Register [177172])** – This register serves as a general purpose data path between the RX02 and the interface. It may represent one of six RX02 registers according to the protocol of the function that is in progress.

This register is read/write if the RX02 is not in the process of executing a command; that is, it may be manipulated without affecting the RX02 subsystem. If the RX02 is actively executing a command, this register will only accept data if RX2CS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

**CAUTION**

**Violation of protocol in manipulation of the data buffer register may cause permanent data loss.**




RX2ES Format (RXV21)

**RX2ES (RX Error and Status)** – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RX2CS. This read-only register can be addressed only under the protocol of the function in progress. The RX2ES is located in the RX2DB upon completion of a function.

RXES bit assignments are as follows.

**Bit Definitions**

| Bit | Function |
|---|---|
| 0 | CRC Error - A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The data collected must be considered invalid. The RX2ES is moved to the RX2DB, and error and done are asserted. It is suggested that the data transfer be tried up to 10 times, as most errors are recoverable (soft). |
| 1 | Side 1 Ready - This bit, when set, indicates that a double-sided diskette is mounted in a double-sided drive and is ready to execute a function. This bit is valid only at the termination of an initialize sequence or a maintenance READ STATUS command. |

**Bit Definitions (Cont)**

| Bit | Function |
|---|---|
| 2 | Initialize Done - This bit is asserted in the RX2ES to indicate completion of the initialize routine which can be caused by RX02 power failure, system power failure, or programmable or bus initialize. |
| 3 | RX AC LO - This bit is set by the interface to indicate a power failure in the RX02 subsystem. |
| 4 | Density Error - This bit indicates that the density of the function in progress does not match the drive density. Upon detection of this error the control terminates the operation and asserts error and done. |
| 5 | Drive Density - This bit indicates the density of the diskette in the drive selected (indicated by bit 8). The density of the drive is determined during read and write sector operations. |
| 6 | Deleted Data - This bit indicates that in the course of recovering data, the "deleted data" address mark was detected at the beginning of the data field. The DRV DEN bit indicates whether the mark was a single- or double-density deleted data address mark. The data following the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or actual deletion of data due to this mark must be accomplished by user software. |
| 7 | Drive Ready - This bit indicates that the selected drive is ready if bit 7=1 and all conditions for disk operation are satisfied, such as door closed, power OK, diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved via a read status function or initialize. |
| 8 | Unit Select - This bit indicates that drive 0 is selected if bit 8=0. This bit indicates the drive that is currently selected. |
| 9 | Head Select - This bit indicates which side of a double-sided drive performed the last operation. |
| 10 | Word Count Overflow - This bit indicates that the word count is beyond sector size. The fill or empty buffer operation is terminated and error and done are set. |
| 11 | Nonexistent Memory Error - This bit is set by the interface when a DMA transfer is being performed and the memory address specified in RX2BA is nonexistent. |

**Function Codes**

Following the strict protocol of the individual function, data storage and recovery on the RXV21 occur with careful manipulation of the RX2CS and RX2DB registers. The penalty for violation of protocol can be permanent data loss.

A summary of the function codes is presented below.

| | |
|---|---|
| 000 | Fill Buffer |
| 001 | Empty Buffer |
| 010 | Write Sector |
| 011 | Read Sector |
| 100 | Set Media Density |
| 101 | Read Status |
| 110 | Write Deleted Data Sector |
| 111 | Read Error Code |

The following paragraphs describe in detail the programming protocol associated with each function encoded and written into RX2CS bits 1-3 if done is set.

**Fill Buffer (000)** – This function is used to fill the RX02 data buffer with the number of words of data specified by the RX2WC register. Fill buffer is a complete function in itself: the function ends when RX2WC overflows, and if necessary, the control has zero-filled the remainder of the buffer. The contents of the buffer may be written on the disk by means of a subsequent WRITE SECTOR command or returned to the host processor by an EMPTY BUFFER command. If the word count is too large, the function is terminated, error and done are asserted, and the word count overflow bit is set in RX2ES.

To initiate this function the RX2CS is loaded with the function. Bit 4 of the RX2CS (unit select) does not affect this function since no disk operation is involved. Bit 8 (density) must be properly selected since this determines the word count limit. When the command has been loaded, the done bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the data buffer register. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The data words are transferred directly from memory and when RX2WC overflows and the control has zero-filled the remainder of the sector buffer, if necessary, done is asserted, ending the operation. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated. Any read of the RX2DB during the data transfer is ignored by the interface. After done is true, the RX2ES is located in the RX2DB register.

**Empty Buffer (001)** – This function is used to empty the contents of the internal buffer through the RXV21 for use by the host processor. This data is in the buffer as the result of a previous FILL BUFFER or READ SECTOR command.

The programming protocol for this function is identical to that for the FILL BUFFER command. The RX2CS is loaded with the command to initiate the function. (This function will ignore bit 4 RX2CS, unit select.) RX2CS bit 8 (density) must be selected to allow the proper word count limit. When the command has been loaded, the done bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the RX2DB. When TR is again asserted the RX2BA may be loaded into the RX2DB. The RXV21 assembles one word of data at a time and transfers it directly to memory. Transfers occur until word count overflow, at which time the operation is complete and done goes true. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated. After done is true, the RX2ES is located in the data buffer register.

**Write Sector (010)** – This function is used to locate a desired sector on the diskette and fill it with the contents of the internal buffer. The initiation of the function clears RX2ES, TR, and done.

When TR is asserted, the program must load the desired sector address into RX2DB, which will drop TR. When TR is again asserted, the program must load the desired track address into the RX2DB, which will drop TR. TR will remain unasserted while the RX02 attempts to locate the desired sector. The diskette density is determined at this time and is compared with the function density. If the densities do not agree, the operation is terminated; bit 4 RX2ES is set, RX2ES is moved to the RX2DB, error (bit 15 RX2CS) is set, done is asserted, and an interrupt is initiated, if bit 6 RX2CS (interrupt enable) is set.

If the densities agree but the RX02 is unable to locate the desired sector within two diskette revolutions, the interface will abort the operation, move the contents of RX2ES to the RX2DB, set error (bit 15 RX2CS), assert done, and initiate an interrupt if bit 6 RX2CS (interrupt enable) is set.

If the desired sector has been reached and the densities agree, the RXV21 will write the $128_{10}$ or $64_{10}$ words stored in the internal buffer followed by a CRC character which is automatically calculated by the RX02. The RXV21 ends the function by asserting done and, if bit 6 RX2CS (interrupt enable) is set, initiating an interrupt.

**CAUTION**

**The contents of the sector buffer are not valid data after a power loss has been detected by the RX02. However, write sector will be accepted as a valid instruction and the (random) contents of the buffer will be written, followed by a valid CRC.**

**NOTE**

**The contents of the sector buffer are not destroyed during a write sector operation.**

**Read Sector (011)** – This function is used to locate the desired sector and transfer the contents of the data field to the internal buffer in the control. This function may also be used to retrieve rapidly (5 ms) the current status of the drive selected. The initiation of this function clears RX2ES, TR, and done.

When TR is asserted the program must load the desired sector address into the RX2DB, which will drop TR. When TR is again asserted, the program must load the desired track address into the RX2DB, which will drop TR.

TR and done will remain negated while the RX02 attempts to locate the desired sector. If the RX02 is unable to locate the desired sector within two diskette revolutions for any reason, the RXV21/RX211 will abort the operation, set done and error (bit 15 RX2CS), move the contents of the RX2ES to the RX2DB, and if bit 6 RX2CS (interrupt enable) is set, initiate an interrupt.

If the desired sector is successfully located, the control reads the data address mark and determines the density of the diskette. If the diskette (drive) density does not agree with the function density the operation is terminated and done and error (bit 15 RX2CS) are asserted. Bit 4 RX2ES is set (density error) and the RX2ES is moved to the RX2DB. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated.

If a legal data mark is successfully located, and the control and densities agree, the control will read data from the sector into the internal buffer. If a deleted data address mark was detected, the control will set bit 6 RX2ES (DD). As data enters the internal buffer, a CRC is computed based on the data field and the CRC bytes previously recorded. A nonzero residue indicates that a read error has occurred and the control sets bit 0 RX2ES (CRC error) and bit 15 RX2CS (error). The RXV21 ends the operation by asserting done and moving the contents of the RX2ES into the RX2DB. If bit 6 RX2CS is set, an interrupt is initiated.

If the desired sector is successfully located, the densities agree and the data is transferred with no CRC error; done will be set and if bit 6 RX2CS (interrupt enable) is set, the RXV21 initiates an interrupt.

**Set Media Density (100)** – This function causes the entire diskette to be reassigned to a new density. Bit 8 RX2CS (density) indicates the new density. The control reformats the diskette by writing new data address marks (double or single density) and zeroing all of the data fields on the diskette.

The function is initiated by loading the RX2CS with the command. Initiation of the function clears RX2ES and done. When TR is set, an ASCII "I" (111) must be loaded into the RX2DB to complete the protocol. This extra character is a safeguard against an error in loading the command. When the control recognizes this character it begins executing the command.

The control starts at sector 1, track 0 and reads the header information, then starts a write operation. If the header information is damaged, the control will abort the operation.

If the operation is successfully completed, done is set and if bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated.

**CAUTION**

**This operation takes about 15 seconds and should not be interrupted. If for any reason the operation is interrupted, an illegal diskette will be generated which may have data marks of both densities. This diskette should be completely reformatted.**

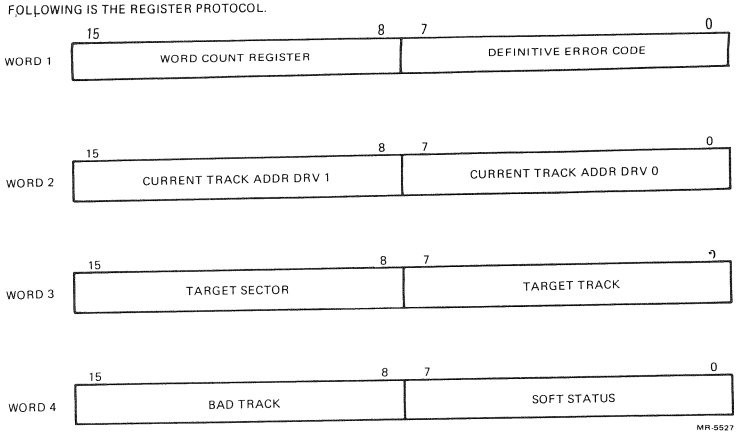
**Maintenance Read Status (101) –** This function is initiated by loading the RX2CS with the command. Done is cleared. The drive ready bit (bit 7 RX2ES) is updated by counting index pulses in the control. The drive density is updated by loading the head of the selected drive and reading the first data mark. The RX2ES is moved into the RX2DB. The RX2CS may be sampled when done (bit 5 RX2CS) is again asserted and if bit RX2CS (interrupt enable) is set, an interrupt will occur. This operation requires approximately 250 ms to complete.

**Write Sector with Deleted Data (110) –** This operation is identical to function 010 (write sector) with the exception that a deleted data address mark is written preceding the data rather than the standard data address mark. The density bit associated with the function indicates whether a single- or double-density deleted data address mark will be written.

**Read Error Code (111) –** The read error code function implies a read extended status. In addition to the specific error code, a dump of the control's internal scratch pad registers also occurs. This is the only way that the word count register can be retrieved. This function is used to retrieve specific information as well as drive status information depending upon detection of the general error bit.

The transfer of the registers is a DMA transfer. The function is initiated by loading the RX2CS with the command; then done goes false. When TR is true, the RX2BA may be loaded into the RX2DB and TR goes false. The registers are assembled one word at a time and are then transferred directly to memory.

FOLLOWING IS THE REGISTER PROTOCOL.




## Definitive Error Codes

| | |
|---|---|
| 10 | Drive 0 failed to see home on initialize. |
| 20 | Drive 1 failed to see home on initialize. |
| 40 | Tried to access a track greater than 76. |
| 50 | Home was found before desired track was reached. |
| 70 | Desired sector could not be found after 52 tries. |
| 110 | More than 40 $\mu$s and no SEP clock seen. |
| 120 | A preamble could not be found. |
| 130 | A preamble found but no ID mark found within allowable time. |
| 150 | The track address of a good header does not compare with desired track. |
| 160 | Too many tries for IDAM. |
| 170 | Data was not found in allotted time. |
| 200 | CRC on reading the sector from the disk. |
| 220 | Failed maintenance wraparound check. |
| 230 | Word count overflow. |

240 Density error.

250 Incorrect key word on SET DENSITY command.

**Register Protocol**

| | |
|---|---|
| Word 1<7:0> | Definitive error codes |
| Word 1<15:8> | Word count register |
| Word 2<7:0> | Current track address of drive 0 |
| Word 2<15:8> | Current track address of drive 1 |
| Word 3<7:0> | Target track of current disk access |
| Word 3<15:8> | Target sector of current disk access |
| Word 4<7> | Unit select bit* |
| Word 4<5> | Head load bit* |
| Word 4<6><4> | Drive density bit of both drives* |
| Word 4<0> | Density of READ ERROR REGISTER command* |
| Word 4<15:8> | Track address of selected drive** |

**RX02 Power Fail or Initialize**
When the RX02 control senses a loss of power within the RX02, it will unload the head and abort all controller action. The RXAC L line is asserted to indicate to the RXV21 that subsystem power has gone. The RXV21 asserts done and error and sets the RXAC L bit in the RXZES.

When the RX02 senses the return of power, it will remove done and begin a sequence to:

1. Move each drive head position mechanism to track 0
2. Clear any active error bits
3. Read sector 1 of track 1, on drive 0
4. Assert initialize done in the RXES.

Upon completion of the power-up sequence, done is again asserted. There is no guarantee that information being written at the time of a power failure will be retrievable; however, all other information on the diskette will remain unaltered.

---

* For DMA interfaces, the controller status soft register is sent to the interface at the end of the command. The four status bits are included in an 8-bit word. Unit select = bit 7; density of drive 1 = bit 6; head load = bit 5; density of drive 0 = bit 4; density of READ ERROR REGISTER command = bit 0.

** The track address of the selected drive-error is only meaningful on a code 150 error. The register contains the address of the cylinder that the head reached on a seek error.

# TSV05 TAPE TRANSPORT AND BUS INTERFACE/CONTROLLER

## GENERAL

The TSV05 tape transport subsystem provides magnetic tape storage capabilities to computer systems using quad-sized LSI-11 bus backplanes. The subsystem reads or writes up to 160,000 bytes per second in ANSI standard format. Data is recorded by phase encoding 1600 bits per inch on nine-track tape. Reading and writing are performed at either 25 or 100 inches per second.* The TSV05 subsystem is hardware compatible with 18- and 22-bit addressing versions of the LSI-11 bus quad backplane. It is software compatible with system and application programs written for the TS11 tape transport subsystem (as long as such programs use the DIGITAL-supplied device handler). Tape formatting, error detection and correction, and self-test diagnostics are included as integral components of the TSV05 subsystem.

| **Voltage** | **Bus Loads** | |
|---|---|---|
| | AC | DC |
| +5 Vdc @ 6.5 A (max.) | 3.0 (max.) | 1 |

**Standard Addresses**

| | |
|---|---|
| 772520/772522 | 1st unit |
| 772524/772526 | 2nd unit |
| 772530/772532 | 3rd unit |
| 772534/772536 | 4th unit |

**Vectors**

| | |
|---|---|
| 224 | 1st unit |
| ** | 2nd unit |
| ** | 3rd unit |
| ** | 4th unit |

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* 100 IPS operating speed requires enabling special features and the appropriate software.

** Rank of 37 in the floating vector area starting at 300.

**Diagnostic Programs**

| | |
|---|---|
| CVTSAA | Logic Test |
| CVTSBA | Advanced Logic Test |
| CVTSCA | Transport Test |
| CVTSDA | Advanced Transport Test |
| CVTSEA | Data Reliability Test |
| XTSAA0 | DEC-X11 |

**Related Documentation**

*TSV05 Tape Transport Pocket Service Guide* (EK-TSV05-PS)
*Operation and Maintenance Instructions for Model F880 Tape Transport* (799816- 000*)
*TSV05 Tape Transport Subsystem Installation Manual* (EK-TSV05-IN)
*XXDP User Guide* (AC-90931-MC)
*TS05 Tape Transport Operation and Acceptance Preventive Maintenance Remove/Replace* (EY-D3142-PS)
TSV05 Field Print Set (MP-01157)
*TSV05 Subsystem Technical Manual* (EK-TSV05-TM)
*Microcomputers and Memories* (EB-18451-20)
*Microcomputer Interfaces Handbook* (EB-17723-20)

**TSV05 Hardware**

TS05 tape transport

M7196 LSI-11 bus interface/controller module

H9642-series cabinet, including 874 power controller and remote power control cable

Pair of 7016855 bus cables for connecting tape transport input and output to the bus interface/controller module

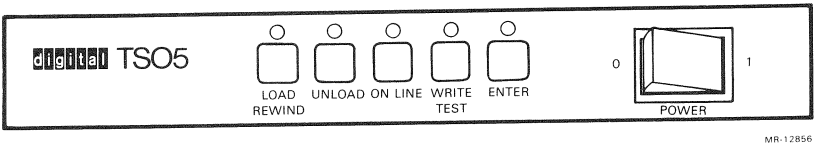
The bus interface/controller module plugs into the LSI-11 bus. The two cables connect the module with the tape transport.

| | Nominal, Vdc | Low Limit, Vdc | High Limit, Vdc |
|---|---|---|---|
| TSV05-BA | 120 | 102 | 128 |
| TSV05-BB | 240 | 204 | 256 |
| TSV05-BD | 220 | 187 | 235 |

**Electromagnetic Interference (EMI)**
The TSV05 subsystem complies with FCC Part 15, Subpart J, Class A and is designed to comply with VDE 0871 B requirements.

**NOTE**

**The TSV05 subsystem has been designed and tested to meet DIGITAL standards, including FCC requirements. The specifications in this chapter are based on this testing. DIGITAL cannot guarantee the TSV05 subsystem will meet these specifications if nontested equipment is installed into the TSV05 cabinet or the TSV05 cabinet is installed in nontested configurations.**



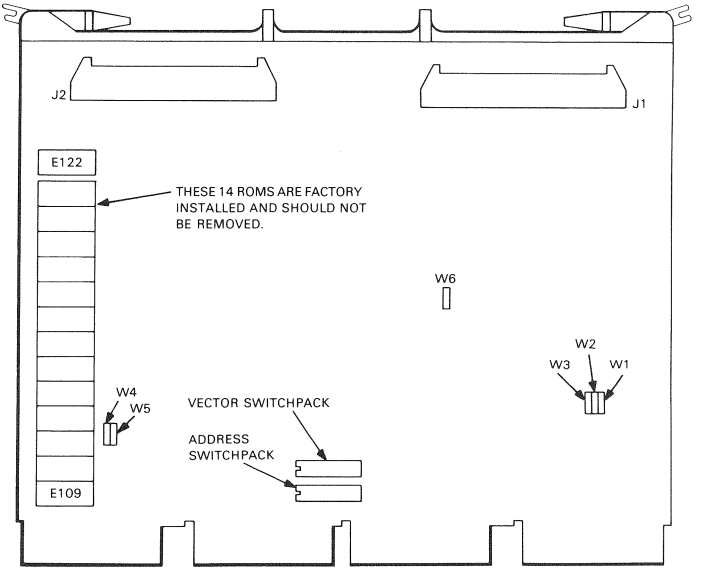

Operator Front Panel

**Controls and Indicators**

| Control/ Indicator | Type | Function |
|---|---|---|
| POWER | ON/OFF rocker switch and indicator | Switches line power ON and OFF. |
| LOAD REWIND | Tactile switch and indicator | 1. Blinks when the tape drive is executing a load or rewind sequence.<br>2. Lit continuously when the beginning of tape (BOT) marker is sensed.<br>3. Pressing the switch:<br>a. Initiates load sequence and advances tape to load point.<br>b. Rewinds the tape to load point. |
| UNLOAD | Tactile switch and indicator | 1. Pressing the switch causes the tape to be unloaded regardless of tape position.<br>2. Blinks when the tape drive is executing an unload sequence.<br>3. Lit continuously when the tape drive has completed its unload sequence and the front access door is unlocked. At this time, the tape may be removed and another tape inserted into the drive.<br>4. Lit continuously after a successful power up, indicating a tape may be loaded. |

**Controls and Indicators (Cont)**

| Control/ Indicator | Type | Function |
|---|---|---|
| ON-LINE | Tactile switch and indicator | 1. Lit when drive is ready and on-line.<br>2. Pressing the switch:<br>a. Takes the tape drive off-line and extinguishes the indicator.<br>b. Puts the tape drive on-line and lights the indicators. |
| | | **NOTE**<br>**Pressing the switch during a load sequence puts the tape drive on-line when the BOT marker is sensed.** |
| TEST | Tactile switch | Operational only in the test mode. Selects alternative operational mode for other switches. |
| WRITE | Indicator | 1. Lit when the write ring is installed and data may be written on tape.<br>2. When indicator is off, write ring is not installed and tape is file protected. |
| ENTER | Tactile switch | This control is used for manual loading and controlling the test mode. |




VECTOR SWITCHPACK

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ON / OFF | V8 | V7 | V6 | V5 | V4 | V3 | V2 | S1 | S0 | A12 | E58 |

ADDRESS SWITCHPACK

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ON / OFF | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | E57 |

V = VECTOR BIT
A = ADDRESS BIT

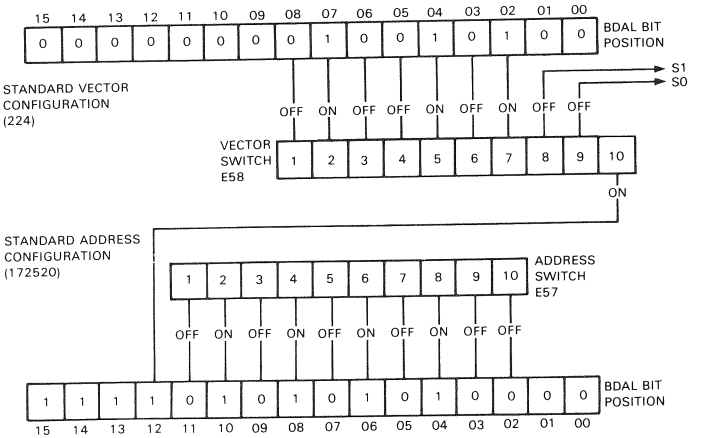
S1 = BUFFERING
S0 = EXTENDED FEATURES

| JUMPERS | | AS SHIPPED |
|---|---|---|
| W1 | BIRQ5 | OUT |
| W2 | BIRQ7 | OUT |
| W3 | BIRQ6 | OUT |
| W4 | BUS GRANT CONTINUITY | IN |
| W5 | BUS GRANT CONTINUITY | IN |
| W6 | SCLOCK ENABLE (USED DURING FACTORY REPAIR ONLY) | IN |

MR-12948

M7196 Switch and Jumper Identification

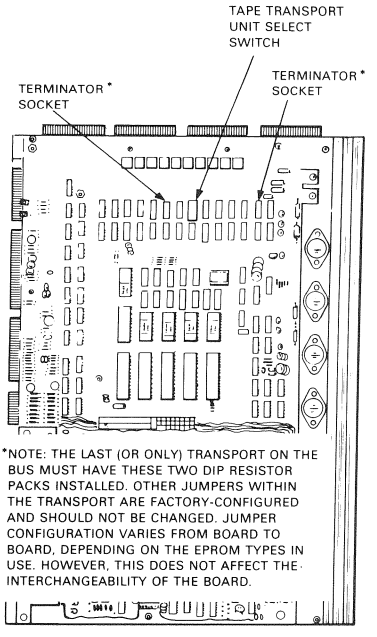
M7196 VECTOR AND ADDRESS SWITCHES

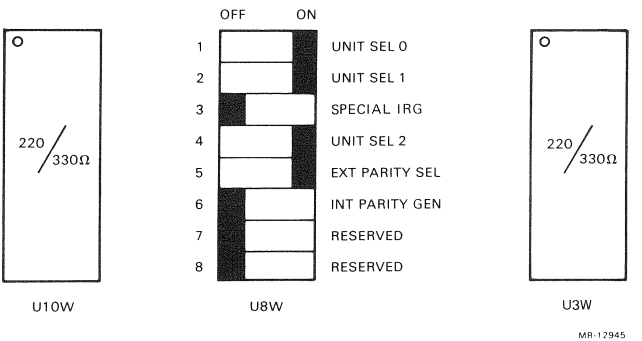



S0 = EXTENDED FEATURES (MUST BE "ON" FOR 22 BIT ADDRESSING)
S1 = BUFFERING ("ON" INCREASES THROUGHPUT BUT DATA WILL BE LOST IF POWER FAILS, NORMALLY NOT USED)

MR-12858

M7196 Vector and Address Switches




Transport Switch and Terminator Identification

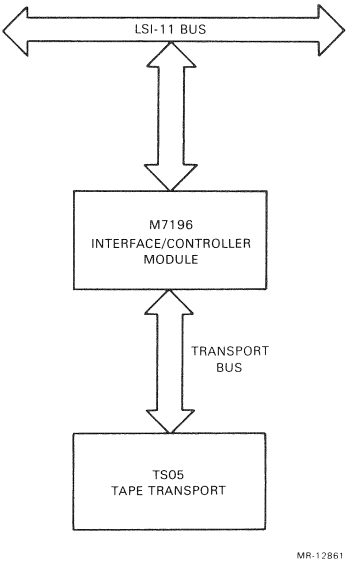
| MODEL | PLUG | RECEPTACLE | CIRCUIT RATING |
|---|---|---|---|
| TSV05-BA | SILVER<br>BRASS<br>NEMA #L5-30P<br>DEC #12-11193 | L5-30R<br>12-11194 | 120 V<br>24 A |
| TSV05-BB<br>-BD | BRASS 2<br>BRASS 1<br>NEMA #6-15P<br>DEC #90-08853 | 6-15R<br>12-11204 | 220/240 V<br>12A |

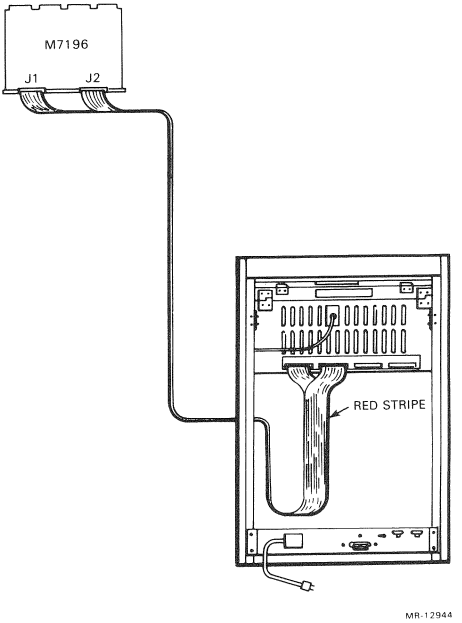
MR-12860

Power Line Connections

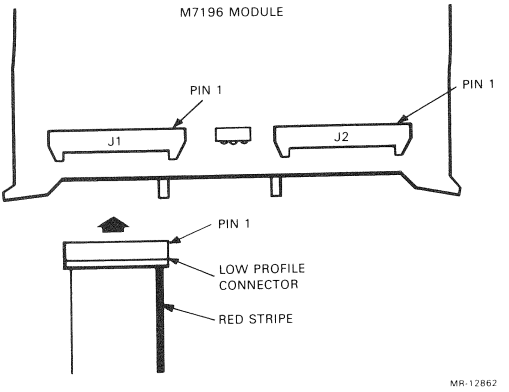
**Power Line Connections**

| Power Cord Color Code | | Pin connection | |
|---|---|---|---|
| **Color** | **Function** | **L5-30P** | **6-15P** |
| Brown | Hot | Brass | Brass 1 |
| Blue | Neutral | Silver | Brass 2 |
| Green/yellow | Ground | Ground | Ground |

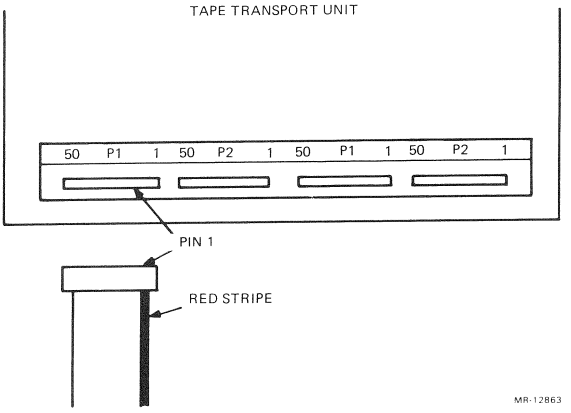



M7196 Interconnection




Cabling the M7196 Module




Cabling the Tape Transport

# VSV11 RASTER GRAPHICS SYSTEM

**GENERAL**

The VSV11 raster graphics system is a basic Q-Bus system designed for color graphics operation with LSI-11 hosts.

This raster graphics module set is installed in a LSI-11 bus and a C-D interconnect.

The first slot is reserved for either a CPU module or a connector which extends the Q-Bus from another backplane. If slot 1 contains a CPU module, jumpers W1 and W3 must be removed in an H9273-A backplane used in a BA11-S mounting box. Rows C and D carry the video bus signals of the VSV11 system. This is modified for 22-bit bus addressing. (backplanes H9273 and H9276).

The basic module set includes:

N7061-YA SYNC generator module
M7062 image memory
M7064 display processor module

**Power Requirements**

1. AC Power – The VSV11 system has one ac load, that being the M7064 (display process module), which is the only module in the VSV11 system that communicates with the CPU.

2. DC Power – To determine how many dc loads a VSV11 system has, count the number of VSV11 modules (M7061, M7062, M7064) that reside on the LSI bus. The total number is the number of dc loads. For example: a VSV11-AH consists of:

   1-M7061
   2-M7062
   1-M7064

   ---

   4=dc loads

# VSV11/M7061,2,4

## Module

| | |
|---|---|
| M7061 | +5 V @ 2.8 A<br>+12 V @ 0.11 A |
| M7062 | –5 V* @ 0.006 A<br>+5 V @ 1.7 A<br>+12 V @ 0.45 A |
| M7064 | +5 V @ 6.0 A |

**Standard Device Address**

767010

**Vector**

720 (octal)

**Diagnostic Program**

CVVSA?

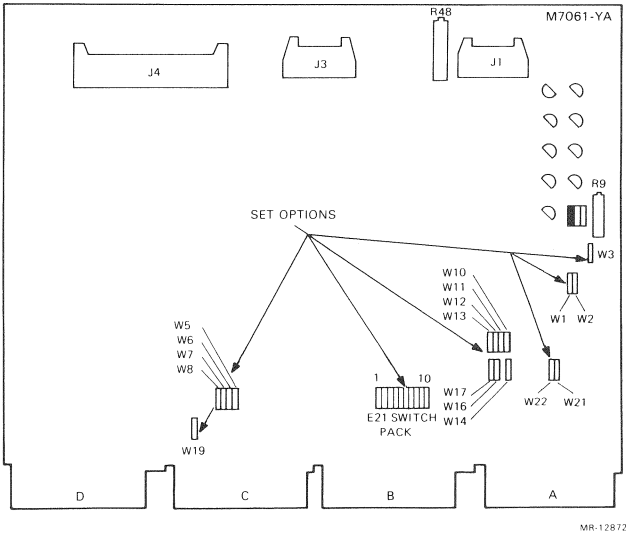
**Related Documentation**

*VSV11 Raster Graphics System User Guide* (EK-VSVFQ-UG)
*DW11 Installation Guide* (EK-DW11A-IN0)
*VSV11 Field Maintenance Print Set* (MP-01012)
*VRV02 Hitachi Monitor Maintenance Manual*
*VT101 Series Technical Manual* (EK-VT101-TM)

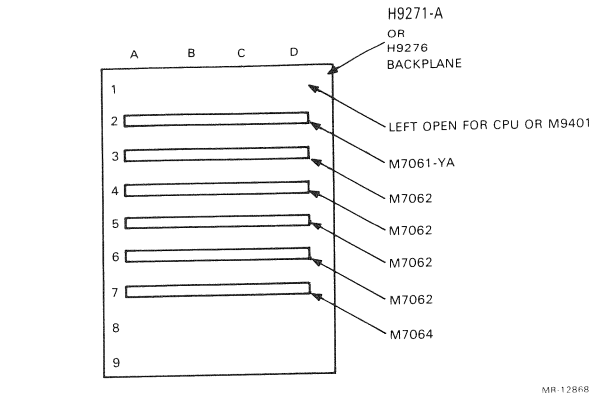
*Supplied by M7061 module.

**M7061-YA SYNC GENERATOR/CURSOR CONTROL BOARD**

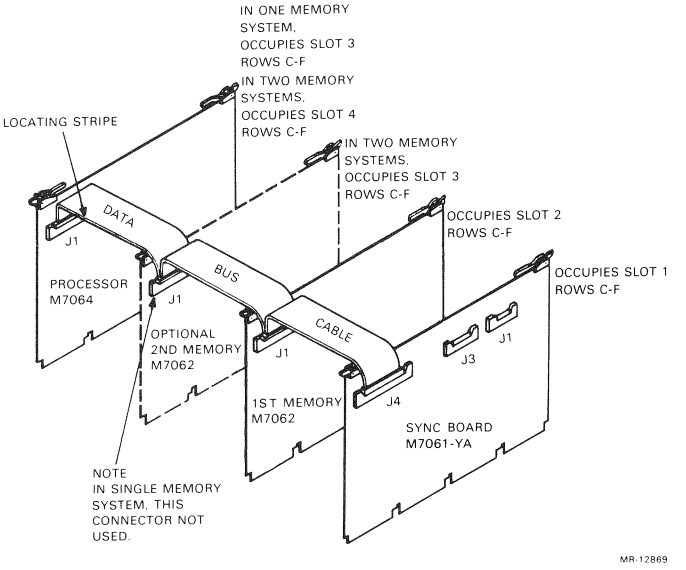
Jumpers and switches are configuration dependent and are located as shown.




M7061-YA Switches and Jumpers




Module Placement Example, Four (Extended) Memory Systems




Intermodule Cabling Example, One or Two Memory Systems

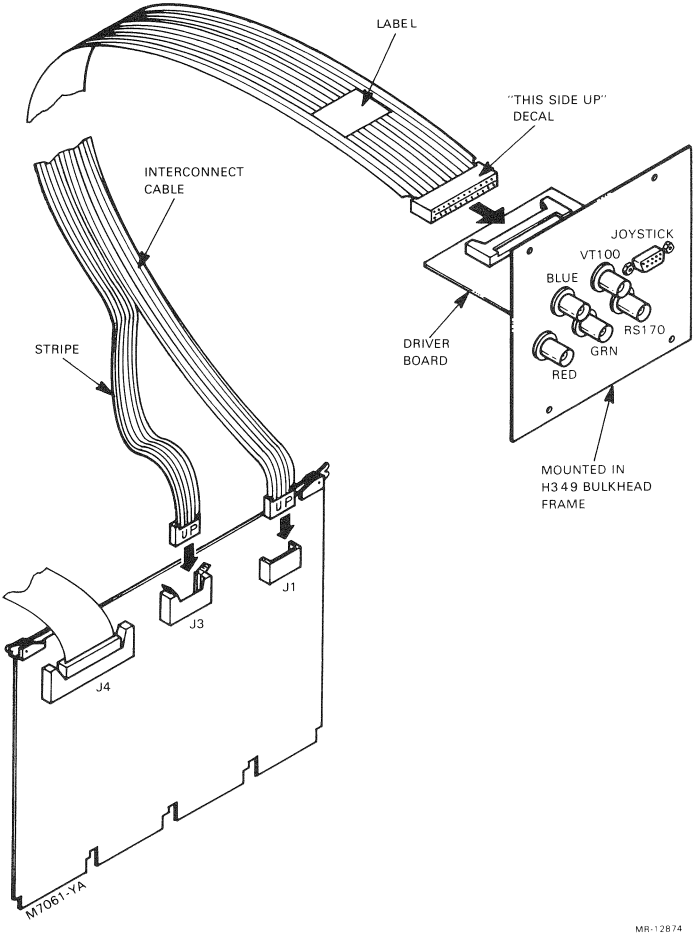
**M7061-YA Cable Connectors**

The three cable connectors located on the M7061-YA module are:

J1 – Accepts the drive board cable

J3 – Accepts the driver board cable with the read stripe toward J4

J4 – Accepts the beginning end of the daisy chain to memories and display processor.




M7061-YA Interconnecting Cables

**M7061-YA Switch Selections**

| Selection | Switch Settings | | |
|---|---|---|---|
| | E21-1 | E21-2 | |
| 60 Hz* | OFF | ON | |
| 50 Hz | ON | OFF | |
| | E21-3 | E21-9 | |
| Interlaced* | OFF | ON | |
| Noninterlaced | ON | ON | |
| Special | OFF | OFF | |
| | E21-4 | E21-5 | |
| Normal Scan* | OFF | ON | |
| Special Scan | ON | OFF | |
| | E21-6 | | |
| Master* | ON | | |
| Slave | OFF | | |
| | E21-7 | E21-8 | E21-10 |
| External Sync*† | ON | OFF | OFF |
| Internal Sync† | OFF | ON | ON |

*These are factory settings.
†Use external sync when doing adjustments.

**M7061-YA Jumper Selections**

| Selection | Jumper State | | | |
|---|---|---|---|---|
| | W19 | | | |
| Master* | IN | | | |
| Slave | OUT | | | |
| | W3 | | | |
| External Sync* | IN | | | |
| Internal Sync | OUT | | | |
| | W5 | W6 | W7 | W8 |
| Channel 0 | OUT | IN | OUT | IN |
| Channel 1 | OUT | IN | IN | OUT |
| Channel 2 | IN | OUT | OUT | IN |
| Channel 3 | IN | OUT | IN | OUT |
| | W10 | W11 | | |
| White Cursor* | IN | IN | | |
| Green and Blue Cursor | IN | OUT | | |
| Green and Red Cursor | OUT | IN | | |
| Green Cursor | OUT | OUT | | |
| | W16 | W17 | | |
| Small Cursor* | IN | IN | | |
| Large Cursor | OUT | OUT | | |
| | W21 | W22 | | |
| 16 Shades/Colors | OUT | IN | | |
| 8 Shades/Colors | IN | OUT | | |

*These are factory settings.

## VSV11 Module M7061-YA – E21 Factory Switch Settings

| Selection | E21 Switch No. 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | Customer Selection |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 60 Hz* | OFF | ON | | | | | | | | | |
| 50 Hz | ON | OFF | | | | | | | | | |
| Interlaced* | | | OFF | | | | | | ON | | |
| Noninter-laced | | | ON | | | | | | ON | | |
| Special | | | OFF | | | | | | OFF | | |
| Norm Scan* | | | | OFF | ON | | | | | | |
| Special Scan | | | | ON | OFF | | | | | | |
| Master* | | | | | | ON | | | | | |
| Slave | | | | | | OFF | | | | | |
| External Sync* | | | | | | | ON | OFF | | OFF | |
| Internal Sync | | | | | | | OFF | ON | | ON | |

*These are factory settings.

**VSV11 Module M7061-YA Factory Set Jumper W - States**

| Selection | Jumper W 3 | 5 | 6 | 7 | 8 | 10 | 11 | 16 | 17 | 19 | 21 | 22 | Customer Selection |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master* | | | | | | | | | | I | | | |
| Slave | | | | | | | | | | O | | | |
| External Sync* | I | | | | | | | | | | | | |
| Internal Sync | O | | | | | | | | | | | | |
| Channel 0 | | O | I | O | I | | | | | | | | |
| Channel 1 | | O | I | I | O | | | | | | | | |
| Channel 2 | | I | O | O | I | | | | | | | | |
| Channel 3 | | I | O | I | O | | | | | | | | |
| White Cursor* | | | | | | I | I | | | | | | |
| Gr+B1 Cursor | | | | | | I | O | | | | | | |
| GR+Rd Cursor | | | | | | O | I | | | | | | |
| Green Cursor | | | | | | O | O | | | | | | |
| Small Cursor* | | | | | | | | I | I | | | | |
| Large Cursor | | | | | | | | O | O | | | | |
| 16 Colors* | | | | | | | | | | | O | I | |
| 8 Colors | | | | | | | | | | | I | O | |

*These are factory settings.

O = Out
I = In

### M7062 MEMORY BOARD

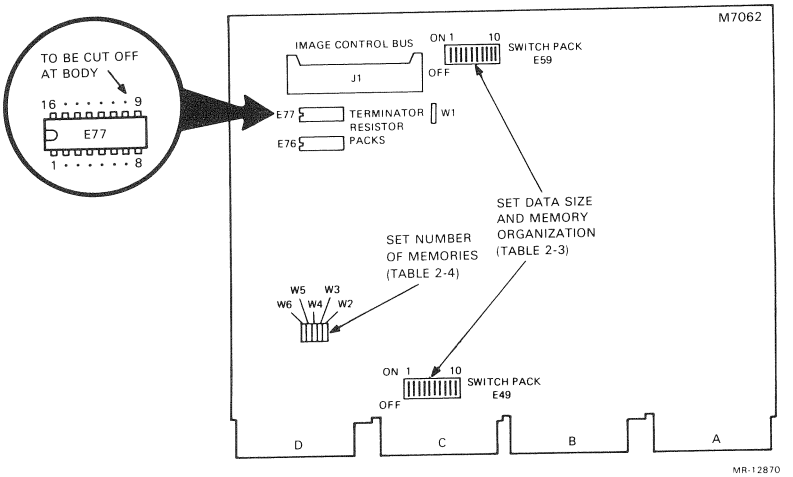
The M7062 memory board is used in all VSV11 system configurations. The number of memory boards installed can vary depending on the number of memory modules in the systems configuration. One, two, or four memory modules can be present in a VSV11 system configuration. A three memory module system does not exist.

### Switches and Jumpers

There are two switchpacks located on the M7062 module, E59 and E49, which are the data size and memory organization. These switches must be configured for the number of memory modules present in a systems configuration. Set the switch and jumpers as listed below.

**NOTE**

**Cut pin 9 on resistor pack E77 on the first memory module only, in any configuration including a one memory module configuration.**




M7062 Memory Board

**M7062 E49 and E59 Switch Settings* and E76/77 Terminator Configuration**

| | One Memory | | Two Memories | | Four Memories | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Channel 0 | | Channel 1 | |
| SW | Non-interlaced | Interlaced | 1st | 2nd | 1st | 2nd | 3rd | 4th |
| 1 | OFF | ON | ON | ON | ON | ON | ON | ON |
| 2 | OFF | ON | ON | ON | ON | ON | ON | ON |
| 3 | ON | ON | ON | OFF | ON | OFF | ON | OFF |
| 4 | ON | ON | ON | OFF | ON | OFF | ON | OFF |
| 5 | ON | OFF | OFF | ON | OF | ON | OFF | ON |
| 6 | ON | OFF | OFF | ON | OFF | ON | OFF | ON |
| 7 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 8 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 9 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 10 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| TRM | | | | | | | | |
| 76 | IN | IN | IN | OUT | IN | OUT | OFF | OFF |
| 77† | IN | IN | IN | OUT | IN | OUT | OUT | OUT |

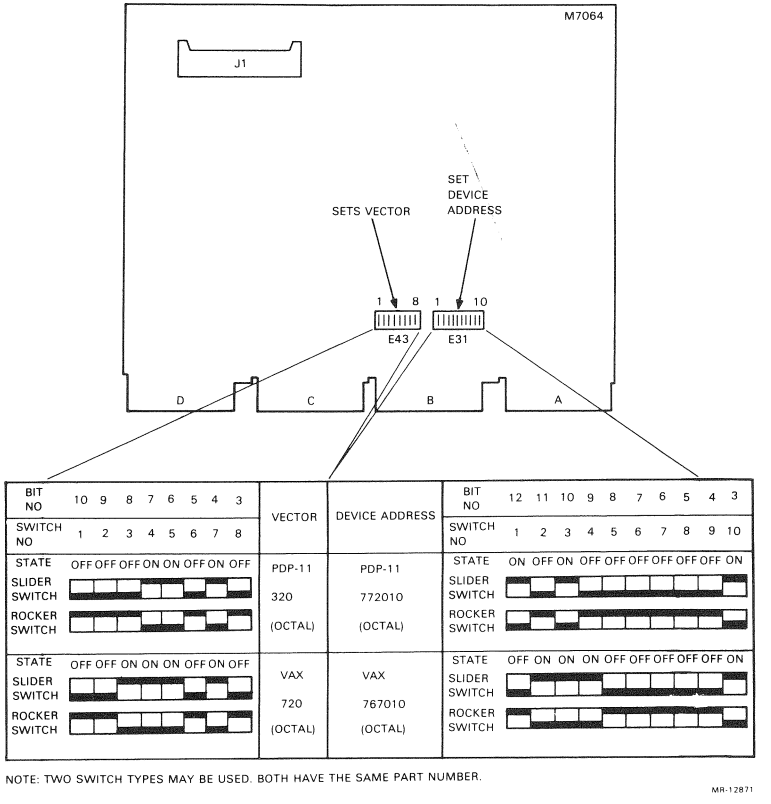
*Note that both switches are set identically.
†Always remove and cut pin 9 and reinstall when IN.

**M7062 Jumper Selections**

| W- | One Memory | Two Memories | Four Memories Channel 0 | Four Memories Channel 1 |
|---|---|---|---|---|
| 1 | IN | IN | IN | IN |
| 2 | IN | IN | IN | IN |
| 3 | OUT | OUT | OUT | OUT |
| 4 | OUT | OUT | OUT | IN |
| 5 | IN | IN | IN | IN |
| 6 | IN | IN | IN | OUT |

## M7064 DISPLAY PROCESSOR MODULE

The M7064 display processor module controls transactions between the control logic and the LSI-11 bus logic. Switches on this module accommodate the host system.




Address and Vector Switch Settings for Module M7064

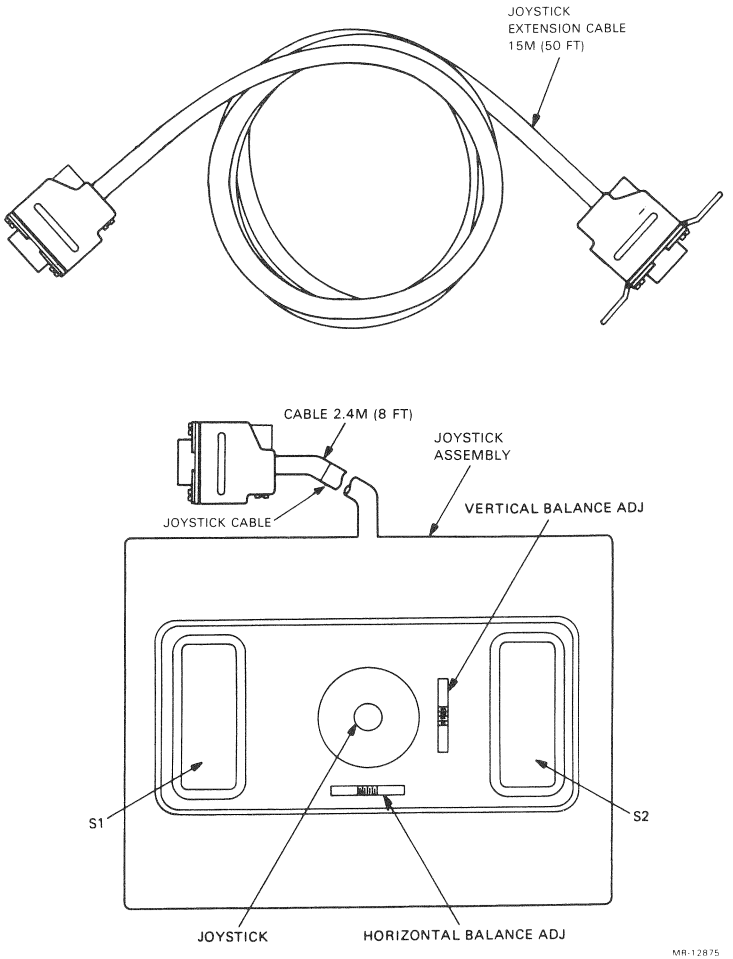
Install the sync generator module (M7061-YA) in slot 2 with either the CPU module or an M9401 bus extender card occupying slot 1. Next, insert the M7062 memory module(s) (up to 4). The last module to be inserted is the M7064 display processor module, next to the last memory module.

## VSV11 Module M7064 – Switch Settings

| Selection | System | Octal | Switch Pack | No. | Factory Setting | Customer |
|---|---|---|---|---|---|---|
| Vector | PDP-11 | 320 | E43 | 1 | OFF | |
| | | | | 2 | OFF | |
| | | | | 3 | OFF | |
| | | | | 4 | ON | |
| | | | | 5 | ON | |
| | | | | 6 | OFF | |
| | | | | 7 | ON | |
| | | | | 8 | OFF | |
| | VAX | 720 | E43 | 1 | OFF | |
| | | | | 2 | OFF | |
| | | | | 3 | ON | |
| | | | | 4 | ON | |
| | | | | 5 | ON | |
| | | | | 6 | OFF | |
| | | | | 7 | ON | |
| | | | | 8 | OFF | |
| Device Address | PDP-11 | 772010 | E31 | 1 | ON | |
| | | | | 2 | OFF | |
| | | | | 3 | ON | |
| | | | | 4 | OFF | |
| | | | | 5 | OFF | |
| | | | | 6 | OFF | |
| | | | | 7 | OFF | |
| | | | | 8 | OFF | |
| | | | | 9 | OFF | |
| | | | | 10 | ON | |
| | VAX | 767010 | E31 | 1 | OFF | |
| | | | | 2 | ON | |
| | | | | 3 | ON | |
| | | | | 4 | ON | |
| | | | | 5 | OFF | |
| | | | | 6 | OFF | |
| | | | | 7 | OFF | |
| | | | | 8 | OFF | |
| | | | | 8 | OFF | |
| | | | | 10 | ON | |

**Task Module 5 – Joystick**

The joystick is used in this system to move and mark the cursor on the screen. The equipment to be installed consists of the joystick itself, its cable, and an extension cable as shown below.

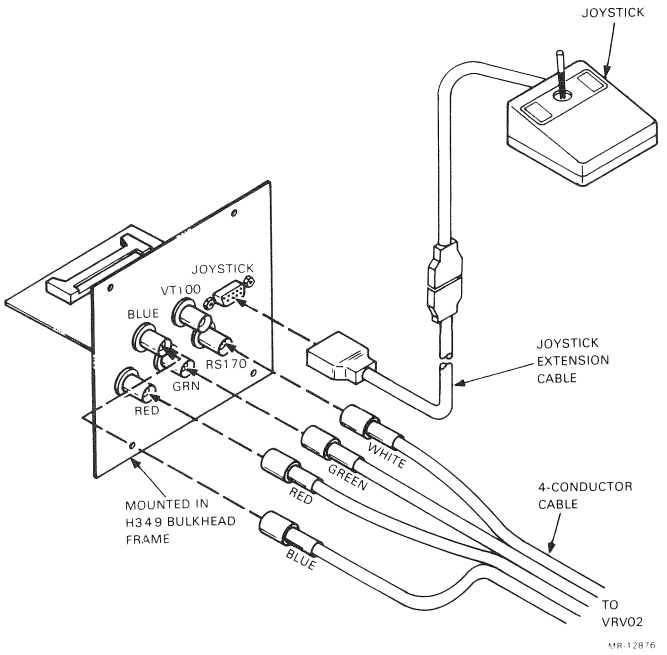



Joystick Components

**CAUTION**

***Never connect the joystick to a system while power is on. To do this can damage the M7061-YA Sync Gen/Cursor Ctrl module.***

Shown below are the joystick and 4-conductor cable connections.




Joystick Installation and 4-Conductor Cable Connection

# RC25 8-INCH DISK DRIVE SUBSYSTEM

## GENERAL

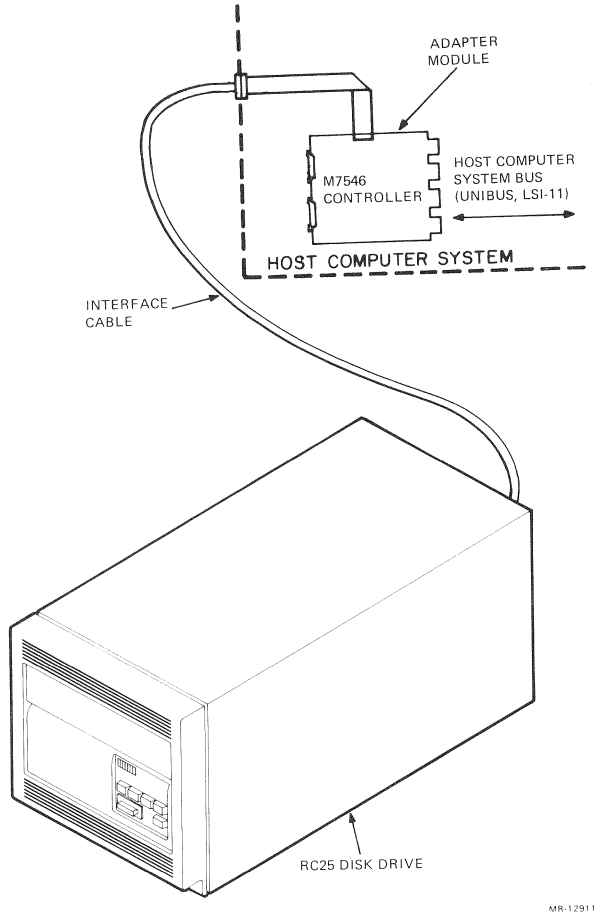
The RC25 is a self-contained mass storage device that is used with a host to store up to 52 million characters on two, hard, 8-inch disk platters.

One disk platter is fixed and the other is removable. Both platters are mounted on the same spindle. The RC25 is available as a table top or rack mounted subsystem. The two types of RC25 units are the master and the slave. The disks on the master and slave units are interchangeable.

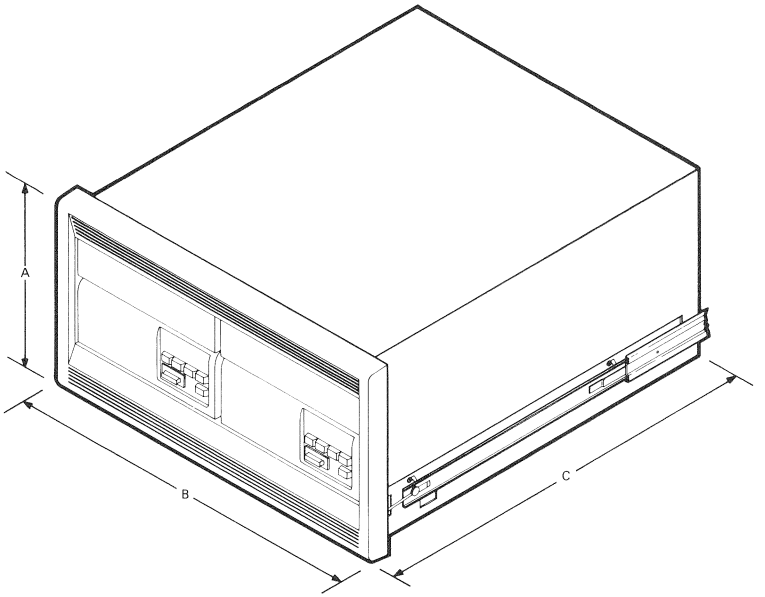
The master, containing the controller module, can drive two spindles (one master and one slave), and must be the first drive in a subsystem.

### Related Documentation

*RC25 Disk Subsystem User Guide* (EK-0RC25-UG)
*RC25 Slave Disk Drive Customer Installation Guide* (EK-RC25S-IN)
*RC25 Disk Subsystem Installation Guide* (EK-0RC25-IN)
*RC25 Disk Subsystem Pocket Service Guide* (EK-0RC25-PS)
Illustrated Parts Breakdown (EK-0RC25-IP)
RC25 Field Maintenance Print Set (MP-01612-00)
MSCP Basic Disk Functions Manual (AA-L619A-TK)
Storage Systems UNIBUS Port Description (AA-L621A-TK)



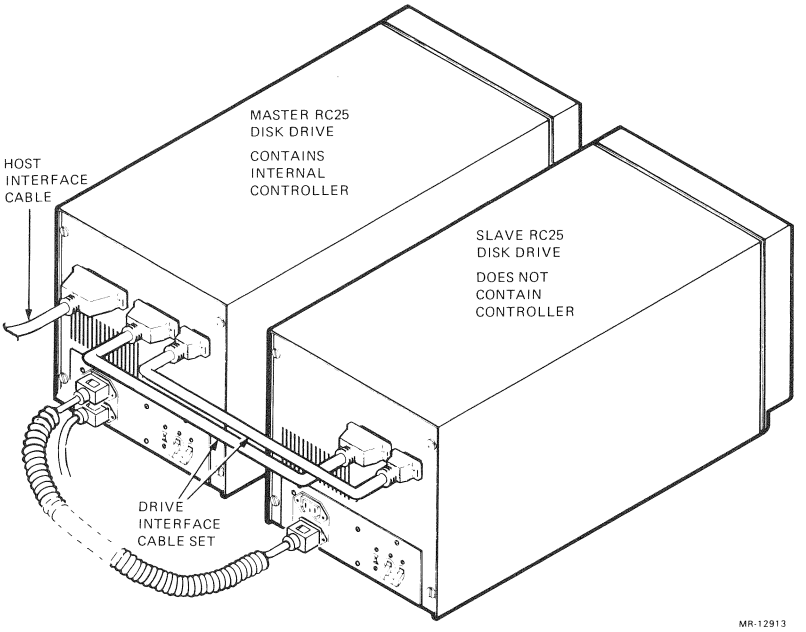

RC25 Disk Subsystem Components



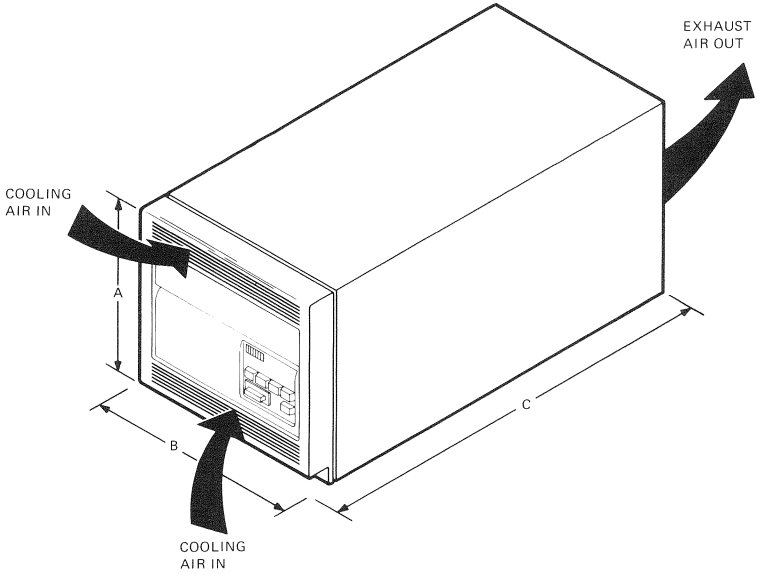

| DIMENSIONS | CENTIMETERS | INCHES |
|---|---|---|
| A. HEIGHT | 26.5 | 10.5 |
| B. WIDTH | 48.3 | 19.0 |
| C. DEPTH | 56.2 | 22.1 |

MR-12912

Space Planning for the Rack-Mount Unit



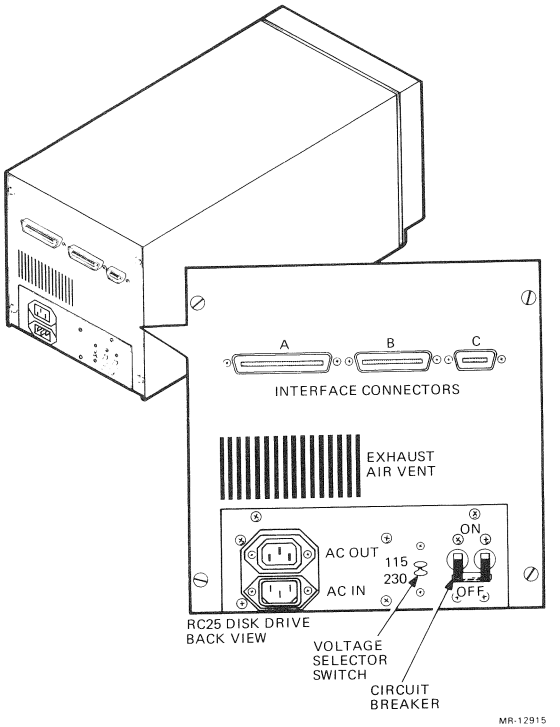

RC25 Master and Slave Disk Drives




| DIMENSIONS | CENTIMETERS | INCHES |
|---|---|---|
| A. HEIGHT | 25.6 | 10.1 |
| B. WIDTH | 25.4 | 10.0 |
| C. DEPTH | 52.1 | 20.5 |

MR-12914

Space Planning for the Tabletop Unit




Voltage Selector Switch and ON/OFF Circuit Breaker

## SPECIFICATIONS

The following list names the primary performance, power, environmental, and physical characteristics of the RC25.

### Size

| | |
|---|---|
| Tabletop model | |
| Height | 25.6 cm (10-1/8 in) |
| Width (master or slave) | 25.4 cm (10 in) |
| Depth | 52.1 cm (20-1/2 in) |
| Rackmount model | |
| Height | 26.5 cm (10-1/2 in) |
| Width | 48.3 cm (19 in) centers |
| Depth | 56.2 cm (22-1/8 in) |

### Weight

| | |
|---|---|
| Tabletop model | 22.7 kg (50 lb) |
| Rackmount model | |
| Single disk | 29.5 kg (65 lb) |
| Dual disk | 54.4 kg (120 lb) |

### Environment

| | |
|---|---|
| Temperature | |
| Operating | 10°–40°C (50°–104°F) ambient with a gradient of 10°C (18°F)/hr |
| Nonoperating (storage/shipping) | –40°–66°C (–40°–151° F) ambient with a gradient of 20°C (36°F)/hr |
| Relative humidity | |
| Operating | 10% – 90% with maximum wet bulb temperature of 28°C (82°F) and a minimum dew point of 2°C (36°F) with no condensation |
| Nonoperating (storage/shipping) | 5% – 95% with no condensation |
| Altitude | |
| Operating | Sea level to 2.4 km (8000 ft)<br>Maximum operating temperatures decrease by a factor of 1.8°C/1000–(1°F/1000 ft) for operation above sea level. |
| Nonoperating (storage/shipping) | Up to 9.1 km (30,000 ft) above sea level (actual or effective by means of cabin pressurization) |

| | |
|---|---|
| Shock | 5 g peak at 7–13 ms duration in three axes mutually perpendicular (maximum) |
| Heat Dissipation | |
| Single disk drive | 1091 Btu/h |
| Dual disk drive | 1828 Btu/h |
| Noise level (single disk) | 53 dB at 1 m |
| **Electrical** | |
| Voltage/frequency (single phase) | 90–128 Vac, 6.6 A, 47–63 Hz<br>180–256 Vac, 3.5 A, 47–63 Hz |
| Power (operating) | |
| Single disk | 320 W |
| Dual disk | 536 W |
| Line cord length (from enclosure) | 1.83 m (6 ft) |
| Plug type | |
| 120 Vac | NEMA 5-15P |
| 220–240 Vac | NEMA 6-15P |
| **Data Capacity (Formatted)** | |
| Single disk drive | 26.061824 Mb fixed disk<br>26.061824 Mb removable cartridge disk<br>52.123648 Mb total<br>(50,902 512-byte blocks/platter) |
| Dual disk drive | 52.123648 Mb fixed disk<br>52.123648 Mb removable cartridge disks<br>104.247296 Mb total<br>(101,804 512-byte blocks/platter) |
| **Media** | |
| Fixed | One 20 cm (7-7/8 in) double-sided nonremovable disk platter per drive |
| Removable | One 20 cm (7-7/8 in) double-sided disk platter in cartridge per drive |
| **Seek Time** | |
| Average seek | 35 ms maximum |
| One track seek | 10 ms maximum |
| Maximum seek | 55 ms maximum |

**Latency**

| | |
|---|---|
| Speed | 2850 r/min ± 9 r/min |
| Average rotational latency | 10.5 ms |
| Maximum rotational latency | 21.0 ms |
| Average access | 45.5 ms (overlapped seeks with double disk drive configuration) |

**Data Rates**

| | |
|---|---|
| Average long transfer rate | 0.57 Mb/sec typical |

| | |
|---|---|
| Spiral Read time | |
| Per track | 31 ms typical |
| Per disk | 50 s typical |
| Per drive | 1 min, 40 s typical |

**Start/Stop Time**

| | |
|---|---|
| Start time | 60 sec maximum (includes purge and self-test time) |
| Stop time | 30 sec maximum |

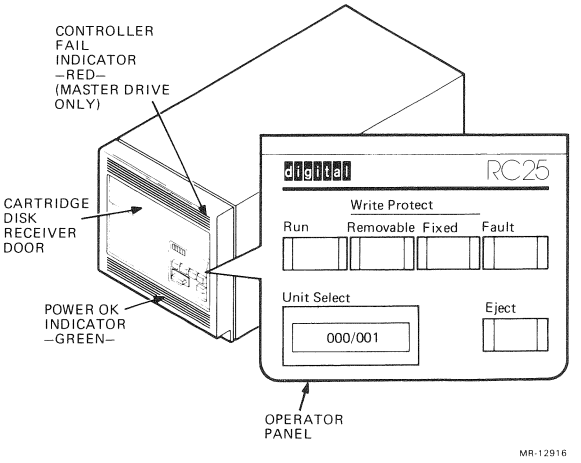
Safety precautions are listed with the following agencies.

| | |
|---|---|
| UL | Underwriter Laboratories |
| CSA | Canadian Standards Association |
| VDE | Verband Deutscher Electrotechniker (German Electrical Engineering Society) |
| IEC | International Electrotechnical Commission |

**Indicator States and Their Meaning**

| Run | *Write Protect* Removable | Fixed | Fault | Eject | Meaning |
|---|---|---|---|---|---|
| OFF | – | – | OFF | ON | The drive is not running and the cartridge receiver door is unlocked. |
| Slow flash* | – | – | OFF | OFF | The disk platters are spinning up or down. |
| ON | – | – | OFF | OFF | The drive is ready to accept commands. |
| – | OFF | – | OFF | – | The removable disk cartridge is write enabled. |
| – | ON | – | OFF | – | The removable disk cartridge is in the read-only state. Writing is prevented. |
| – | – | OFF | OFF | – | The fixed disk platter is write enabled. |
| – | – | ON | OFF | – | The fixed disk platter is in the read-only state. Writing is prevented. |
| – | – | – | ON | – | The drive has detected a failure. Press **FAULT** briefly and refer to the fault codes in Chapter 5 to determine what went wrong. |
| – | – | – | slow flash* | – | The drive is in maintenance mode and is running a test. |

*Slow flash is once per second.




RC25 Front View Showing Operator Panel

**Cartridge Loading**

The RC25 is designed to make correct loading easy. To load the cartridge disk, hold it label (writing) side up with the tapered end toward you. The opposite end has a small trap door through which the read/write heads enter. This end enters the cartridge receiver first.

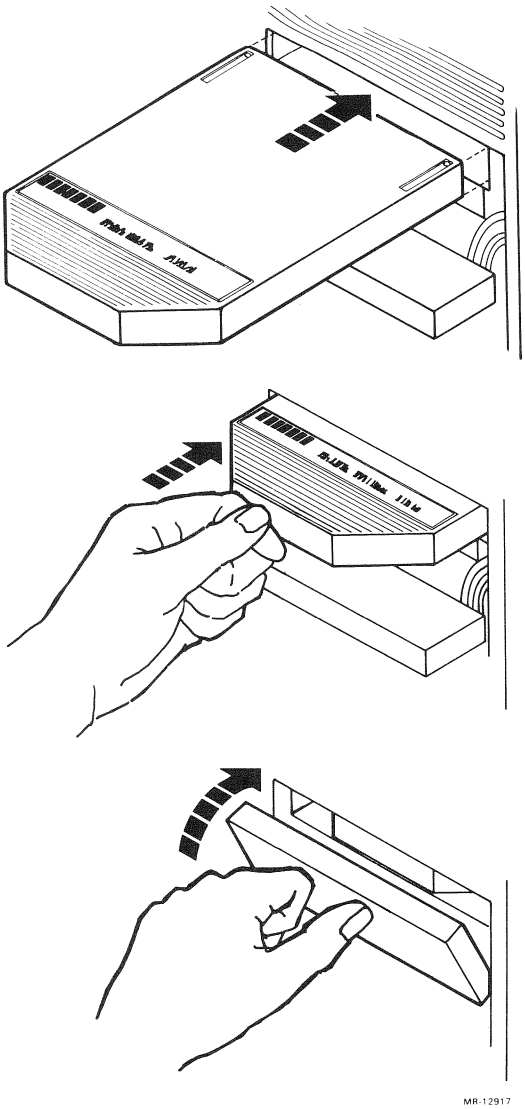
If the cartridge receiver door is not open, press the **EJECT** button. The door opens and swings down. Slide the cartridge straight in with a firm push until it locks into place. Close the receiver door firmly by swinging it back up and latching it into place.

**Cartridge Unloading**

Unloading the cartridge is as simple as loading. With the spindle stopped and the receiver door unlocked (**EJECT** indicator on), press the **EJECT** button. The door opens and the cartridge disk ejects. Once the door is open, grasp the cartridge and pull it straight out of the receiver.

**NOTE**

**Keep the cartridge receiver door closed when not in use to prevent atmospheric contaminants from entering the disk enclosure.**




Inserting the Disk Cartridge

**Disk Operating Procedures**

The procedures in this section are for starting and stopping the RC25.

**Starting Procedure**

| Operator Action | Disk Drive Response |
|---|---|
| None. | Initial state of disk drive:<br><br>**RUN** button is released (out).<br>**RUN** indicator is off.<br>**EJECT** indicator is on.<br>Spindle is stoppled |
| Press **EJECT**. | Cartridge receiver door opens and disk cartridge partially ejects. |
| Reload cartridge or replace with new cartridge. | None. |
| Close cartridge receiver door. | None. |
| Set **WRITE PROTECT** buttons. | Corresponding **WRITE PROTECT** indicator lights or goes off. |
| Press **RUN** in to lock it in. | Receiver door locks.<br>**EJECT** indicator goes off.<br>**RUN** indicator flashes slowly.<br>Disk platters spin up.<br>**RUN** indicator lights continuously. |
| Disk is ready for operation. | |

**NOTE**

**A disk cartridge must be installed to spin up and operate the disk drive. The fixed disk does not spin up and run without a removable cartridge in place. The spin-up cycle takes approximately 1 minute. It involves spinning the disk platters up to operating speed, cleaning the internal air system, loading the read/write heads, and performing a self-test.**

**Stopping Procedure**

| Operator Action | Disk Drive Response |
|---|---|
| None. | Initial state of disk drive:<br><br>**RUN** button is pressed in.<br>Disk platters are spinning.<br>**RUN** indicator is on.<br>**EJECT** indicator is off. |
| Press **RUN** in to release it. | **RUN** indicator flashed slowly.<br>Disk platters slow down.<br><br>When disk platters stop spinning:<br><br>**RUN** indicator goes off.<br>**EJECT** indicator lights.<br>Receiver door unlocks. |
| Press **EJECT**. | Receiver door opens partially. Push down door to eject cartridge fully. |
| Remove disk cartridge. | |
| Close receiver door. | |

**CAUTION**

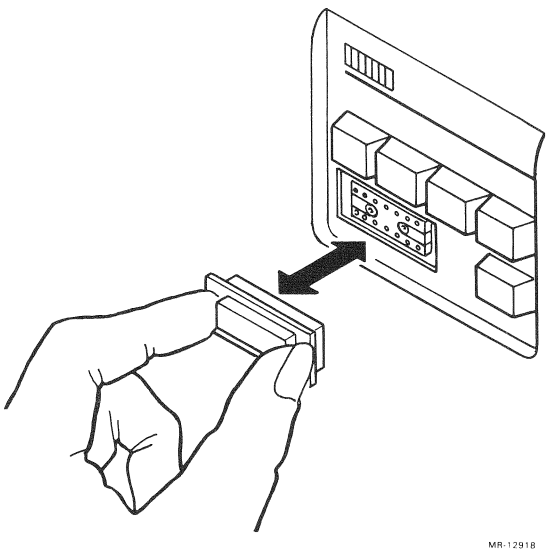
**Do not try to open the receiver door until the EJECT indicator lights and the EJECT button is pressed; you can damage the disk drive and cartridge.**

**Unit Select Number**

The host computer system (or computer network) locates a peripheral device via a unit select number. The RC25 can have any number pair from 0/1 to 252/253. It has a pair of numbers because both disk platters have a unique number. The removable disk platter always has an even number and the fixed disk platter always has an odd number. The unit select number is chosen during installation, but may be changed any time thereafter.

The unit select number is determined by a factory wired plug. This plug can be removed and replaced to change the number. However, the RC25 cannot function without a plug in place. The result is a fault indication. Two disk drives with the same unit select number also cause a fault.

Change the unit select number plug by grasping the plug handle and pulling it straight out of the operator panel. Install the new number plug by pushing it straight into the empty, recessed socket. When installing the new plug, be sure to hold it so the numbers are right side up. Do not try to force an upside down plug into the socket. This mistake creates a false number and destroys the electronic components inside the operator panel.




Changing the Unit Select Number Plug

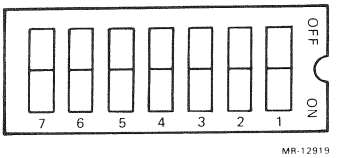
## HOW TO MODIFY THE UNIT SELECT NUMBER PLUG

If you want to use a unit select number pair of 8/9 or higher for your RC25, you must open and modify the unit select number plug. The procedure in this appendix shows you how to make the modification.

1. Remove the plug on the operator panel by grasping the plug handle and pulling it straight out.

2. The plug contains a small, eight-position DIP switch. Remove this switch from the handle by spreading apart the two plastic retaining tabs and pulling straight out.

3. When working with the switch, hold it so the number 1 position is on the left, as shown below.




Unit Select Number Switch

4. Find the number pair you want and set the seven switches as indicated. Three different types of switches are used in the RC25: one slide switch and two types of rocket switches. It is important to identify which type of switch your drive has before trying to change the number. To change the number with a slide switch, push the switch tab to OFF or ON (up or down) as indicated in the table. To change the number with a rocket switch, press in on the corresponding side of the switch.

5. After setting the new number, press the DIP switch back into the plug handle and insert the plug back into the operator panel.

## Unit Select Number Switch Settings

| Unit Number | DIP Switch Position Number 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 0/1 | ON | ON | ON | ON | ON | ON | ON |
| 2/3 | ON | ON | ON | ON | ON | ON | OFF |
| 4/5 | ON | ON | ON | ON | ON | OFF | ON |
| 6/7 | ON | ON | ON | ON | ON | OFF | OFF |
| 8/9 | ON | ON | ON | ON | OFF | ON | ON |
| 10/11 | ON | ON | ON | ON | OFF | ON | OFF |
| 12/13 | ON | ON | ON | ON | OFF | OFF | ON |
| 14/15 | ON | ON | ON | ON | OFF | OFF | OFF |
| 16/17 | ON | ON | ON | OFF | ON | ON | ON |
| 18/19 | ON | ON | ON | OFF | ON | ON | OFF |
| 20/21 | ON | ON | ON | OFF | ON | OFF | ON |
| 22/23 | ON | ON | ON | OFF | ON | OFF | OFF |
| 24/25 | ON | ON | ON | OFF | OFF | ON | ON |
| 26/27 | ON | ON | ON | OFF | OFF | ON | OFF |
| 28/29 | ON | ON | ON | OFF | OFF | OFF | ON |
| 30/31 | ON | ON | ON | OFF | OFF | OFF | OFF |
| 32/33 | ON | ON | OFF | ON | ON | ON | ON |
| 34/35 | ON | ON | OFF | ON | ON | ON | OFF |
| 36/37 | ON | ON | OFF | ON | ON | OFF | ON |
| 38/39 | ON | ON | OFF | ON | ON | OFF | OFF |
| 40/41 | ON | ON | OFF | ON | OFF | ON | ON |
| 42/43 | ON | ON | OFF | ON | OFF | ON | OFF |
| 44/45 | ON | ON | OFF | ON | OFF | OFF | ON |
| 46/47 | ON | ON | OFF | ON | OFF | OFF | OFF |
| 48/49 | ON | ON | OFF | OFF | ON | ON | ON |
| 50/51 | ON | ON | OFF | OFF | ON | ON | OFF |
| 52/53 | ON | ON | OFF | OFF | ON | OFF | ON |
| 54/55 | ON | ON | OFF | OFF | ON | OFF | OFF |
| 56/57 | ON | ON | OFF | OFF | OFF | ON | ON |
| 58/59 | ON | ON | OFF | OFF | OFF | ON | OFF |
| 60/61 | ON | ON | OFF | OFF | OFF | OFF | ON |
| 62/63 | ON | ON | OFF | OFF | OFF | OFF | OFF |
| 64/65 | ON | OFF | ON | ON | ON | ON | ON |
| 66/67 | ON | OFF | ON | ON | ON | ON | OFF |
| 68/69 | ON | OFF | ON | ON | ON | OFF | ON |

## Unit Select Number Switch Settings (Cont)

| Unit Number | DIP Switch Position Number 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 70/71 | ON | OFF | ON | ON | ON | OFF | OFF |
| 72/73 | ON | OFF | ON | ON | OFF | ON | ON |
| 74/75 | ON | OFF | ON | ON | OFF | ON | OFF |
| 76/77 | ON | OFF | ON | ON | OFF | OFF | ON |
| 78/79 | ON | OFF | ON | ON | OFF | OFF | OFF |
| 80/81 | ON | OFF | ON | OFF | ON | ON | ON |
| 82/83 | ON | OFF | ON | OFF | ON | ON | OFF |
| 84/85 | ON | OFF | ON | OFF | ON | OFF | ON |
| 86/87 | ON | OFF | ON | OFF | ON | OFF | OFF |
| 88/89 | ON | OFF | ON | OFF | OFF | ON | ON |
| 90/91 | ON | OFF | ON | OFF | OFF | ON | OFF |
| 92/93 | ON | OFF | ON | OFF | OFF | OFF | ON |
| 94/95 | ON | OFF | ON | OFF | OFF | OFF | OFF |
| 96/97 | ON | OFF | OFF | ON | ON | ON | ON |
| 98/99 | ON | OFF | OFF | ON | ON | ON | OFF |
| 100/101 | ON | OFF | OFF | ON | ON | OFF | ON |
| 102/103 | ON | OFF | OFF | ON | ON | OFF | OFF |
| 104/105 | ON | OFF | OFF | ON | OFF | ON | ON |
| 106/107 | ON | OFF | OFF | ON | OFF | ON | OFF |
| 108/109 | ON | OFF | OFF | ON | OFF | OFF | ON |
| 110/111 | ON | OFF | OFF | ON | OFF | OFF | OFF |
| 112/113 | ON | OFF | OFF | OFF | ON | ON | ON |
| 114/115 | ON | OFF | OFF | OFF | ON | ON | OFF |
| 116/117 | ON | OFF | OFF | OFF | ON | OFF | ON |
| 118/119 | ON | OFF | OFF | OFF | ON | OFF | OFF |
| 120/121 | ON | OFF | OFF | OFF | OFF | ON | ON |
| 122/123 | ON | OFF | OFF | OFF | OFF | ON | OFF |
| 124/125 | ON | OFF | OFF | OFF | OFF | OFF | ON |
| 126/127 | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| 128/129 | OFF | ON | ON | ON | ON | ON | ON |
| 130/131 | OFF | ON | ON | ON | ON | ON | OFF |
| 132/133 | OFF | ON | ON | ON | ON | OFF | ON |
| 134/135 | OFF | ON | ON | ON | ON | OFF | OFF |
| 136/137 | OFF | ON | ON | ON | OFF | ON | ON |
| 138/139 | OFF | ON | ON | ON | OFF | ON | OFF |

**Unit Select Number Switch Settings (Cont)**

| Unit Number | DIP Switch Position Number 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 140/141 | OFF | ON | ON | ON | OFF | OFF | ON |
| 142/143 | OFF | ON | ON | ON | OFF | OFF | OFF |
| 144/145 | OFF | ON | ON | OFF | ON | ON | ON |
| 146/147 | OFF | ON | ON | OFF | ON | ON | OFF |
| 148/149 | OFF | ON | ON | OFF | ON | OFF | ON |
| 150/151 | OFF | ON | ON | OFF | ON | OFF | OFF |
| 152/153 | OFF | ON | ON | OFF | OFF | ON | ON |
| 154/155 | OFF | ON | ON | OFF | OFF | ON | OFF |
| 156/157 | OFF | ON | ON | OFF | OFF | OFF | ON |
| 158/159 | OFF | ON | ON | OFF | OFF | OFF | OFF |
| 160/161 | OFF | ON | OFF | ON | ON | ON | ON |
| 162/163 | OFF | ON | OFF | ON | ON | ON | OFF |
| 164/165 | OFF | ON | OFF | ON | ON | OFF | ON |
| 166/167 | OFF | ON | OFF | ON | ON | OFF | OFF |
| 168/169 | OFF | ON | OFF | ON | OFF | ON | ON |
| 170/171 | OFF | ON | OFF | ON | OFF | ON | OFF |
| 172/173 | OFF | ON | OFF | ON | OFF | OFF | ON |
| 174/175 | OFF | ON | OFF | ON | OFF | OFF | OFF |
| 176/177 | OFF | ON | OFF | OFF | ON | ON | ON |
| 178/179 | OFF | ON | OFF | OFF | ON | ON | OFF |
| 180/181 | OFF | ON | OFF | OFF | ON | OFF | ON |
| 182/183 | OFF | ON | OFF | OFF | ON | OFF | OFF |
| 184/185 | OFF | ON | OFF | OFF | OFF | ON | ON |
| 186/187 | OFF | ON | OFF | OFF | OFF | ON | OFF |
| 188/189 | OFF | ON | OFF | OFF | OFF | OFF | ON |
| 190/191 | OFF | ON | OFF | OFF | OFF | OFF | OFF |
| 192/193 | OFF | OFF | ON | ON | ON | ON | ON |
| 194/195 | OFF | OFF | ON | ON | ON | ON | OFF |
| 196/197 | OFF | OFF | ON | ON | ON | OFF | ON |
| 198/199 | OFF | OFF | ON | ON | ON | OFF | OFF |
| 200/201 | OFF | OFF | ON | ON | OFF | ON | ON |
| 202/103 | OFF | OFF | ON | ON | OFF | ON | OFF |
| 204/205 | OFF | OFF | ON | ON | OFF | OFF | ON |
| 206/207 | OFF | OFF | ON | ON | OFF | OFF | OFF |
| 208/209 | OFF | OFF | ON | OFF | ON | ON | ON |

## Unit Select Number Switch Settings (Cont)

| Unit Number | DIP Switch Position Number 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 210/211 | OFF | OFF | ON | OFF | ON | ON | OFF |
| 212/213 | OFF | OFF | ON | OFF | ON | OFF | ON |
| 214/215 | OFF | OFF | ON | OFF | ON | OFF | OFF |
| 216/217 | OFF | OFF | ON | OFF | OFF | ON | ON |
| 218/219 | OFF | OFF | ON | OFF | OFF | ON | OFF |
| 220/221 | OFF | OFF | ON | OFF | OFF | OFF | ON |
| 222/223 | OFF | OFF | ON | OFF | OFF | OFF | OFF |
| 224/225 | OFF | OFF | OFF | ON | ON | ON | ON |
| 226/227 | OFF | OFF | OFF | ON | ON | ON | OFF |
| 228/229 | OFF | OFF | OFF | ON | ON | OFF | ON |
| 230/231 | OFF | OFF | OFF | ON | ON | OFF | OFF |
| 232/233 | OFF | OFF | OFF | ON | OFF | ON | ON |
| 234/235 | OFF | OFF | OFF | ON | OFF | ON | OFF |
| 236/237 | OFF | OFF | OFF | ON | OFF | OFF | ON |
| 238/239 | OFF | OFF | OFF | ON | OFF | OFF | OFF |
| 240/241 | OFF | OFF | OFF | OFF | ON | ON | ON |
| 242/243 | OFF | OFF | OFF | OFF | ON | ON | OFF |
| 244/245 | OFF | OFF | OFF | OFF | ON | OFF | ON |
| 246/247 | OFF | OFF | OFF | OFF | ON | OFF | OFF |
| 248/249 | OFF | OFF | OFF | OFF | OFF | ON | ON |
| 250/251 | OFF | OFF | OFF | OFF | OFF | ON | OFF |
| 252/253 | OFF | OFF | OFF | OFF | OFF | OFF | ON |
| ILLEGAL | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

# RD51 11 Mb WINCHESTER DISK DRIVE SUBSYSTEM

## GENERAL

The RD51 fixed Winchester single element disk subsystem, found inside the MICRO/PDP-11 and the MICRO VAX, can be attached to an existing 22-bit MICRO, MICRO VAX, or a PDP-11/23 PLUS system.

The RD51 controller interface is used for both the RD51 and the RX50 disk and diskette drives.

### Related Documentation

*MICRO/PDP-11 Technical Manual* (EK-OLCP5-TM)
*MICRO/PDP-11 Owner's Manual* (EK-OLCP5-OM)
*MICRO/PDP-11 Unpacking and Installation* (EK-OLCP5-IN)
*RQDX1 Controller Module User Guide* (EK-OLCP5-UG)
*MICRO/PDP-11 System Option Manual* (EK-OLCP5-OD)
*H9302 Rack Mount Adapter Kit Instruction Manual* (EK-LEP03-IN)

### RD51 Subsystem Component Specification

Unit Storage Capacity

11 megabytes (formatted data) 18 sectors

Power Supply Assembly

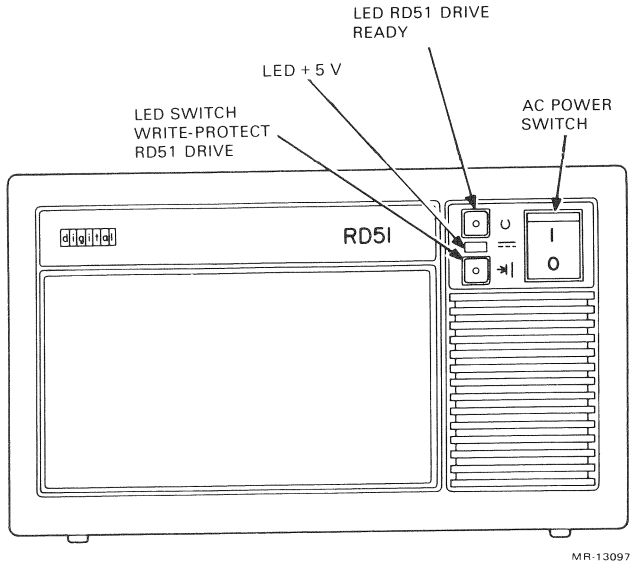
| | |
|---|---|
| Inputs | |
| Switchable line voltage | 100–120 Vac (normal)<br>200–240 Vac (normal) |
| Line frequency | 47–63 Hz either input range |
| Line current | 120 Vac @ 2 A RMS (max)<br>240 Vac @ 1 A RMS (max) |
| Output | |
| Power | 65 watts (max) |
| DC Voltage | +12A Vdc +5% 1 A min. (4.5 A max.)<br>+12B Vdc ±10% .12 A (max.)<br>+5 Vdc ±5% @ .3 A min to 2 A (max.) |

# RD51

| | |
|---|---|
| Dimension | 12 in long<br>9 in wide<br>3 1/2 in high |
| Weight | 14 lbs |

**Controls and Indicators**
Switch ON/OFF (1 or 0) rocker switch – connects ac power to the subassemblies internal dc power supply.

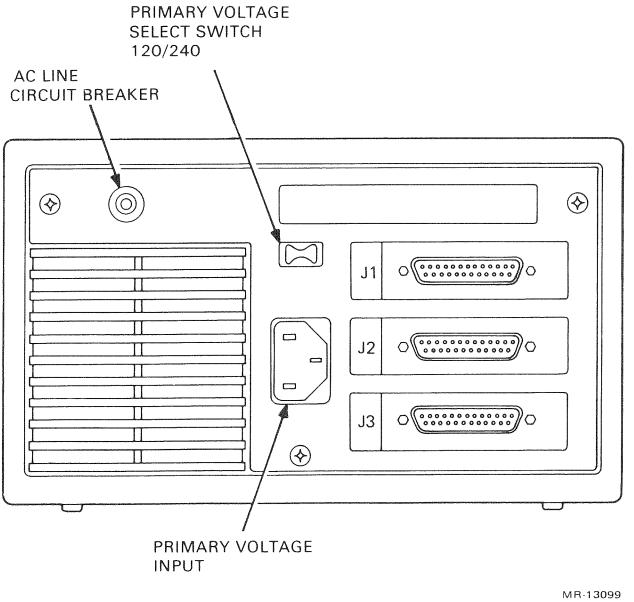
| Front Panel LEDs | Lit | Not lit |
|---|---|---|
| Top Green LED | RD51 ready | RD51 not ready |
| Middle Green LED | DC power present | DC power not present |
| Amber LED | RD51 write protect | RD51 not write protected |




Front Panel, Switches and Indicators

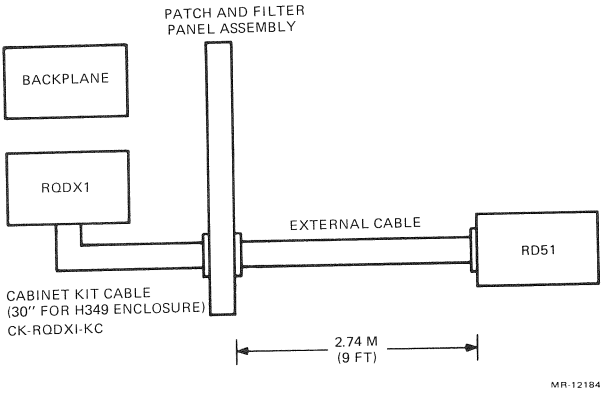
**Rear Panel Connectors**
J1 - DUO
J2 - DU1
J3 - DU2

Inside the BA23 system chassis (MICRO/PDP-11 and MICRO VAX 1) an RQDX1 drive controller, RQDX1-E extender module and cables are used. (Cabinet kit CK-RQDX1-KA)

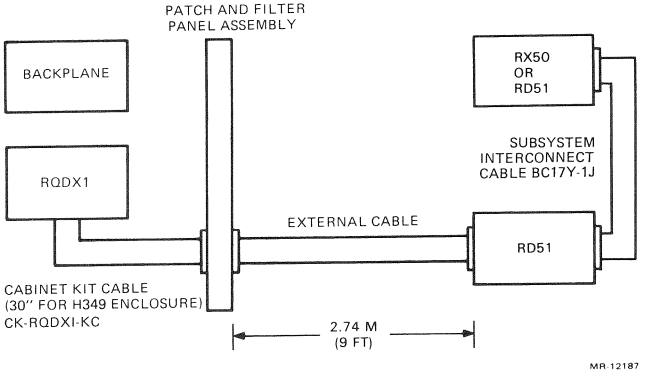



Rear Panel Assembly

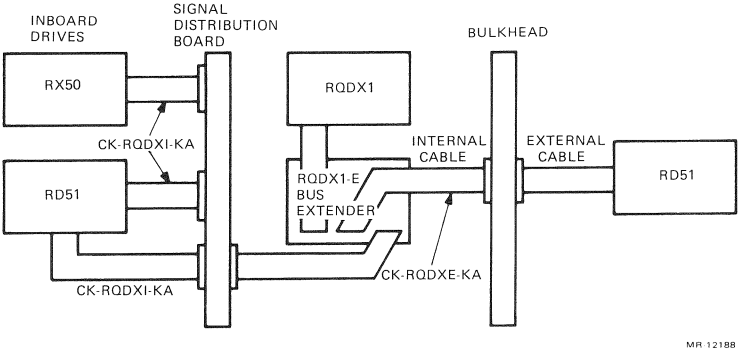
## VARIOUS CONFIGURATIONS FOR EXPANSION OF THE RD51




Single Expansion Configuration




Double Expansion Configuration




Maximum Expansion Configuration

### J1, J2 and J3 Pin Numbers and Signal Names

Connectors J1, J2, and J3 have identical signal names and pin numbering.

| Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|
| J1-01 | MEMWRTDT1 (H) | J1-42 | INDEX (L) |
| J1-34 | MEMWRTDT1 (L) | J1-26 | RD1WRTPRQ (L) |
| J1-18 | GROUND | J1-10 | DRV SEL 1 (L) |
| J1-02 | HEAD SET 2 (L) | J1-43 | DRV SEL 2 (L) |
| J1-35 | GROUND | J1-27 | DRV SEL 3 (L) |
| J1-19 | SEEKOPLT | J1-11 | RX2WPTLED (L) |
| J1-03 | RD1 RDY (H) | J1-44 | RXMOTORON (L) |
| J1-36 | WPT FAULT (L) | J1-28 | GROUND |
| J1-20 | GROUND | J1-12 | DIRECTION (L) |
| J1-04 | READ SEL 1 (L) | J1-45 | GROUND |
| J1-37 | RXOWPTLED (L) | J1-29 | STEP (L) |
| J1-21 | RD0 RDY (H) | J1-13 | GROUND |
| J1-05 | RX1WPTLED (L) | J1-46 | RXWRTDATA (L) |
| J1-38 | DRVSLOACK (L) | J1-30 | GROUND |
| J1-22 | MEMRDDAT0 (H) | J1-14 | WRT GATE (L) |
| J1-06 | MFMRDDAT0 (L) | J1-47 | GROUND |
| J1-39 | MFMWRTDT0 (H) | J1-31 | TRACK 00 (L) |
| J1-23 | MFMWRTDT0 (L) | J1-15 | RX3WPTLED (L) |
| J1-07 | MFMRDDAT1 (H) | J1-48 | DRVSL1ACK (L) |
| J1-40 | MFMRDDAT1 (L) | J1-32 | GROUND |
| J1-24 | GROUND | J1-16 | READ DATA (L) |
| J1-08 | RFDUCWRTI (L) | J1-49 | GROUND |
| J1-41 | RD0WRTPRO (L) | J1-33 | HEAD SEL 0 (L) |
| J1-25 | DRV SEL 4 (L) | J1-17 | GROUND |
| J1-09 | GROUND | J1-50 | READY (L) |

**Power Supply Connectors**

AC Power Input Connector

| Pin No. | Signal |
|---|---|
| 1 | Ground |
| 2 | ac phase |
| 3 | ac neutral |

DC Power Output Connector

| Pin No. | Signal |
|---|---|
| 1 | +5 V |
| 2 | +5 V |
| 3 | +5 V |
| 4 | Return |
| 5 | Return |
| 6 | Return |
| 7 | Return |
| 8 | 12 VA |
| 9 | 12 VA |
| 10 | 12 VB |
| 11 | No pin |
| 12 | No connection |

### Logical Unit Number Selection

The logical unit number (LUN) selection is set by jumpers on the RQDX1 Controller module. These jumpers are set to the lowest LUN assigned to any RD51 or RX50 drive subsystem that is controlled by the RQDX1. The RQDX1 module automatically senses the logical unit configuration during initialization of the system to determine how many of the four possible units are actually present.

The LUN jumper format allows only one jumper to be installed at a time, and each individual jumper specified a group of four logical units as follows.

| LUN Jumper | LUNs Specified |
|---|---|
| No jumper installed | 0–3 |
| 1 | 4–7 |
| 2 | 8–1 |
| 3 | 12–15 |
| 4 | 16–19 |
| 5 | 20–23 |
| 6 | 24–27 |
| 7 | 28–31 |
| 8 | 32–35 |

Within the context of RQDX1 configurations as shown below, if number 4 jumper is connected and using configuration number 2, then:

16 = unit 0
17 = unit 1
18 = unit 2
19 = unit 3

| Configuration | External subsystem disk drives | Logical numbers for disk drives |
|---|---|---|
| 1 | One RD51, one RX50 | Unit 0 = RD51<br>Units 1, 2 = RX50 |
| 2 | Two RX50s | Units 0, 1 = RX50<br>Units 2, 3 = RX50 |
| 3 | Two RD51s, one RX50 | Unit 0 = RD51<br>Unit 1 = RD51<br>Units 2, 3 = RX50 |
| 4 | Two RD51s | Unit 0 = RD51<br>Unit 1 = RD51 |
| 5 | One RX50 | Units 0, 1 = RX50 |

**Expansion**

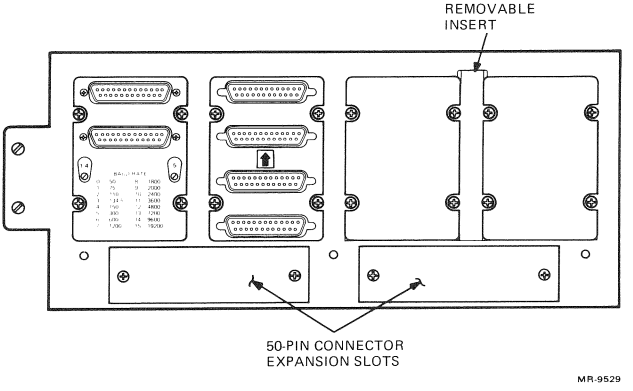
MICRO/PDP-11 and MICRO VAX I systems contain inboard RD51-A and RX50-AA drives and both systems are housed in BA23 enclosures. Each system also contains an RQDX1 controller. The controller has a capacity of four LUNs, three of which are used internally. Thus, only one RD51 drive can be added externally to the MICRO/PDP-11 and MICRO VAX I.

A BA23 enclosure (MICRO/PDP-11 and MICRO VAX I) prior to any add-on RD51, contains:

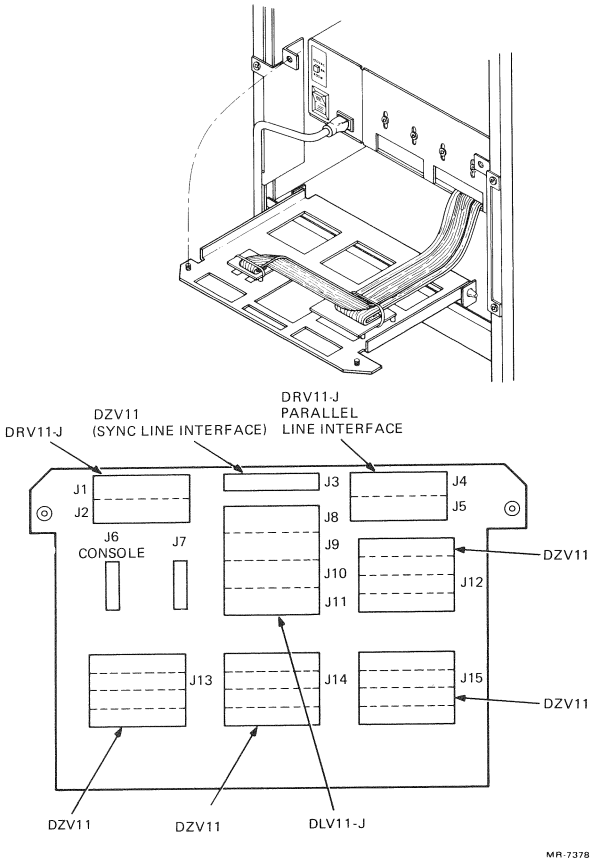
1 RQDX1 controller
1 CK-RQDX1-KA cabinet kit
1 RD51-A (drive only)
1 RX50-AA (drive only)

To accommodate an external add-on drive, an RQDX1-E bus extender and cable must be added internally and connected to the patch and filter panel assembly.

A PDP-11/23 PLUS system, to accommodate external add-on drives, requires internally an RQDX1 controller and a cabinet key cable CK-RQDX1-KC connected to the H349 distribution panel.




BA23 Patch and Filter Panel Assembly




PDP-11/23 PLUS/H349 Distribution Panel (Bulkhead)

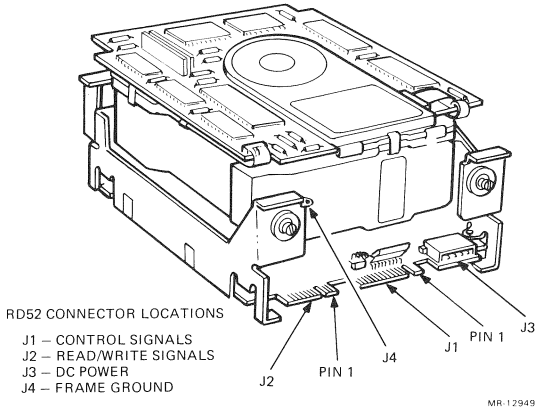
# RD52 31 Mb WINCHESTER DISK DRIVE SUBSYSTEM

**GENERAL**

The RD52 fixed disk drive uses an RQDX1 controller and contains three nonremovable 5-1/4 inch disks as storage media. The three 5-1/4 inch disks can store up to 31 megabytes of formatted data.

The interface between the disk drive and the host controller consists of four connections:

11 - Control Signals
12 - Read/Write Signals
13 - DC power
14 - Frame ground




RD52 Connector Locations

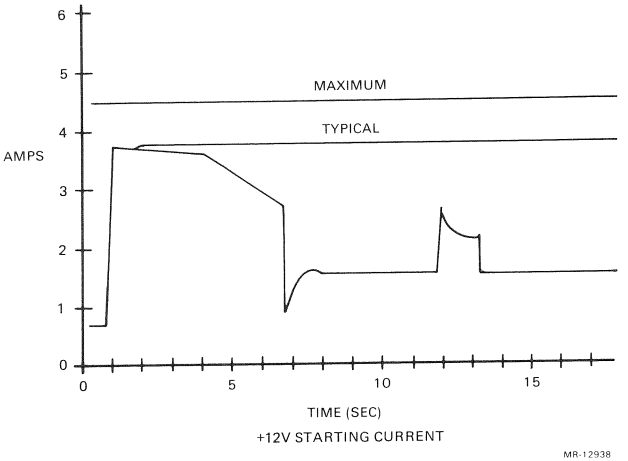
# RD52

## Power Requirement

+5 Vdc +5% @ 1.0 A
+12 Vdc +5% @ 2.5 A (4.5 A max.)

| VOLTAGE | MAX START | TYP START | MAX SEEK-ING | TYP SEEK-ING | MAX STEADY STATE | TYP STEADY STATE | MAX RIPPLE P-P |
|---|---|---|---|---|---|---|---|
| +5 | 1.5 AMP | 1 AMP | 1.5 AMP | 1 AMP | 1.5 AMP | 1 AMP | 50 mV |
| +12 | 4.5 AMP | 3.8 AMP | 3 AMP | 2.5 AMP | 2 AMP | 1.5 AMP | 50 mV |

CURRENT REQUIRMENTS




+12 V Starting Current

## Related Documentation

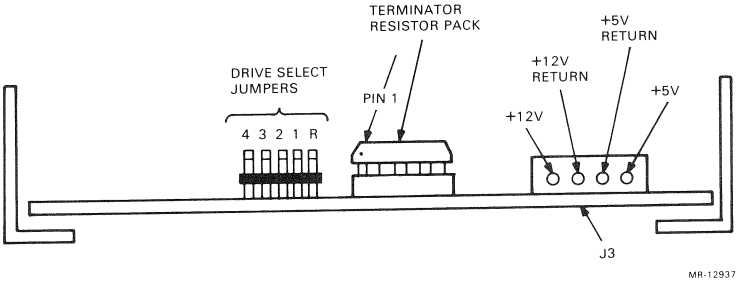
*RD52-D,R Disk Drive Subsystem Owners Manual* (EK-LEP03-OM)

## Physical Size

Height – 3.25 in
Width – 5.75 in
Depth – 8.0 in
Weight – 14 lbs

**Connectors**

J1 – 34 pin – control signal
J2 – 20 pin +12 Vdc data signals
J3 – 4 pin +5 Vdc dc power
J4 – single log – frame ground

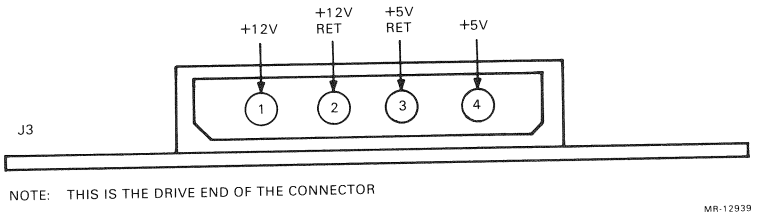



RD52 Power Connector (J3)

**CAUTION**

**Damage will occur to the drive if the +5 V and +12 V connections are reversed.**

CAUTION: DAMAGE WILL OCCUR TO THE DRIVE IF THE +5V AND +12V CONNECTIONS ARE REVERSED.




Selectable Address Internal

**NOTE**

**This is the drive end of the connector.**

# RD52

**Environmental Limits**

| | |
|---|---|
| Operating temperature | 10° to 50 ° C |
| Non operating temperature | −40° to 60° C |
| Operating humidity | 10% to 80% |
| Non operating humidity | 5% to 95% |
| Maximum wet bulb | 25° C (Non-condensing) |
| Thermal gradient | 10°C per hour |
| Operating altitude | 0 to 10,000 feet |
| Operating vibration | .5 G at 10–500 Hz |
| Non operating shock | 30 Gs |

Capacity Unformatted (+10 space cylinders)

| | |
|---|---|
| Per drive | 33.07 MB |
| Per surface | 6.61 MB |
| Per track | 10.416 KB |

Capacity Formatted (+10 Spare Cylinders)

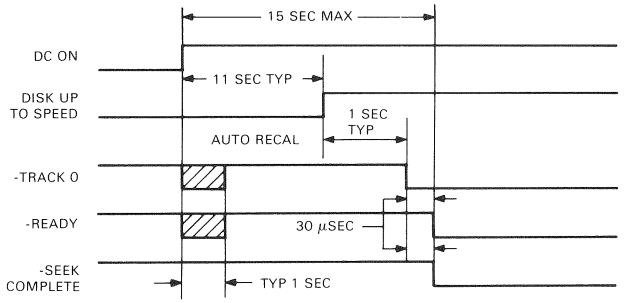
| | |
|---|---|
| Per drive | 26.00 MB |
| Per surface | 5.20 MB |
| Per track | 8.192 KB |
| Per sector | 256 bytes |
| Sectors/Track | 32 |
| Transfer rate | 5 Mbit/sec |

Seek Time

| | |
|---|---|
| Track to track | 3.0 ms |
| Average | 30.0 ms |
| Maximum | 60.0 ms |
| Settling | 3.0 ms |
| Average latency | 8.33 ms |
| Start time | 15 sec |

**Functional Summary**

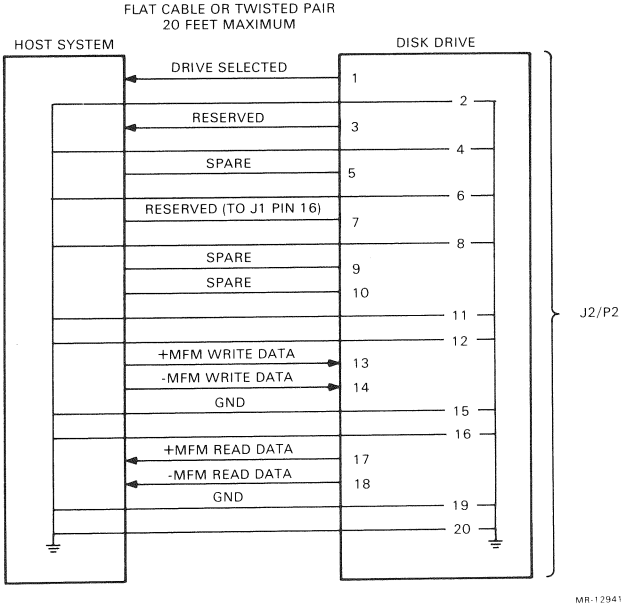
| | |
|---|---|
| Rotation ±1% | 3600 rpm |
| Recording max | 8780 bpi |
| Flux density | 8780 fci |
| Track density | 800 tpi |
| Data cylinders | 645 |
| Tracks | 3175 |
| R/W heads | 5 |
| Disks | 3 |
| Index | 1 |




-TRACK 0, -READY AND -SEEK COMPLETE WILL NOT BE PRESENT AT THE INTERFACE UNLESS THE DRIVE IS SELECTED.

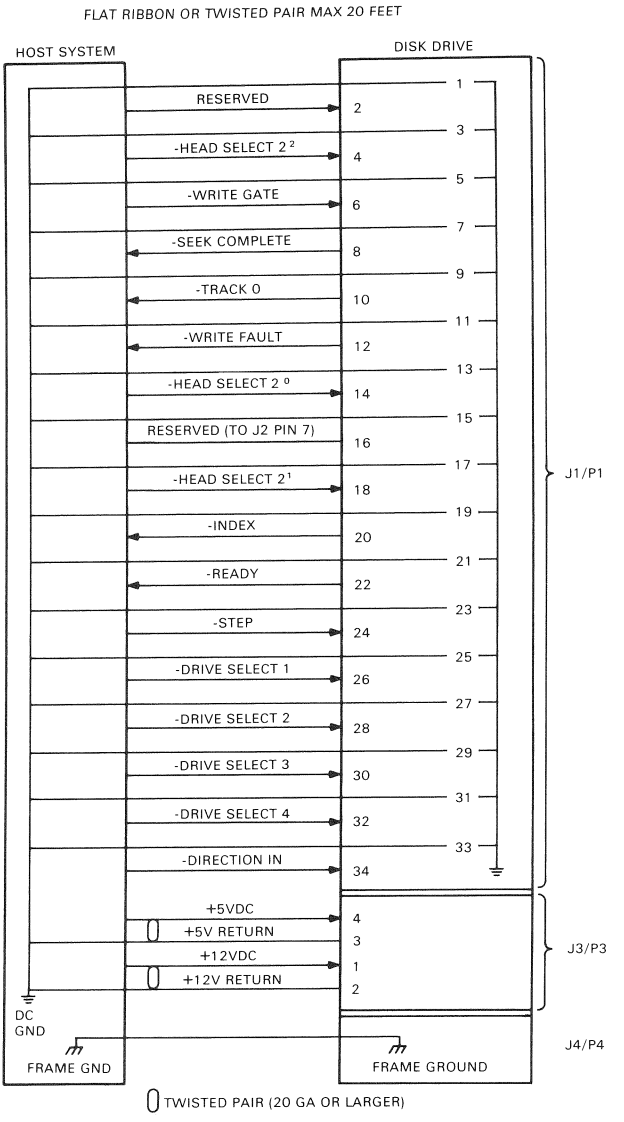
MR-12940

Power-Up Sequence

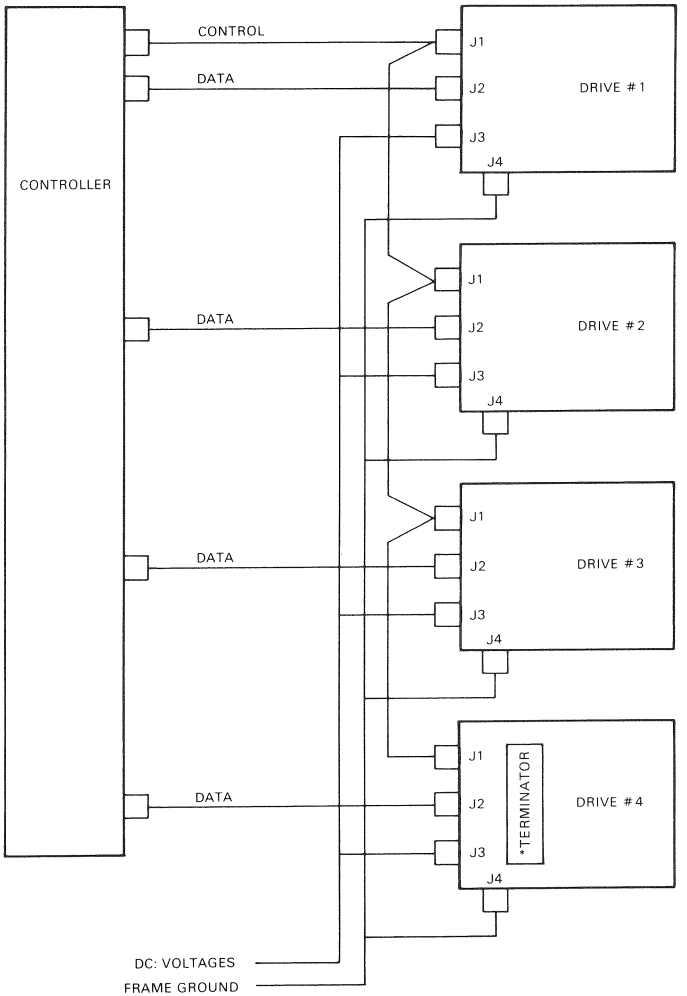



MR-12941

Data Signals



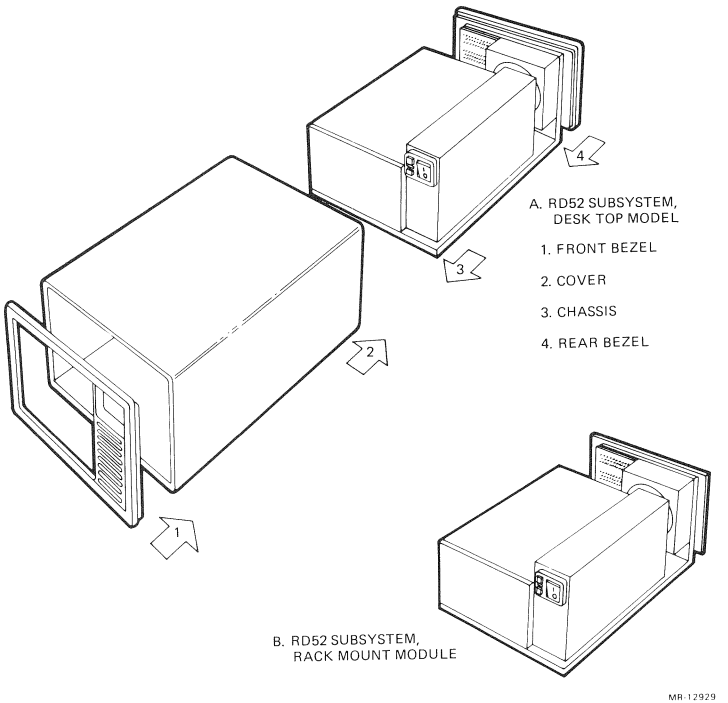

Control Signals



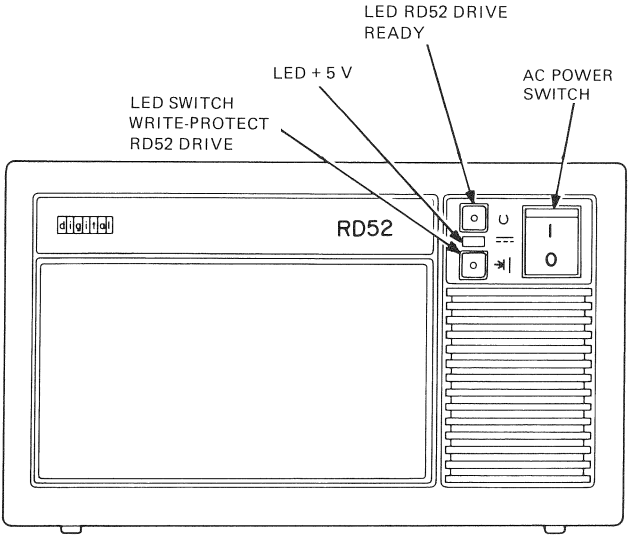

*THE LAST OR ONLY DRIVE IN THE CONTROL CABLE STRING MUST HAVE THE TERMINATOR RESISTOR PACK INSTALLED. ALL OTHER DRIVES MUST HAVE THEIR TERMINATORS REMOVED.

MR-12943

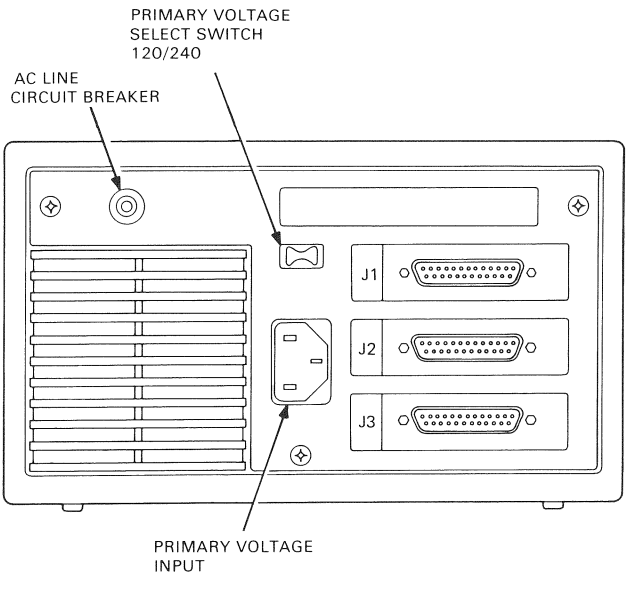
Typical Connection, Four Drives



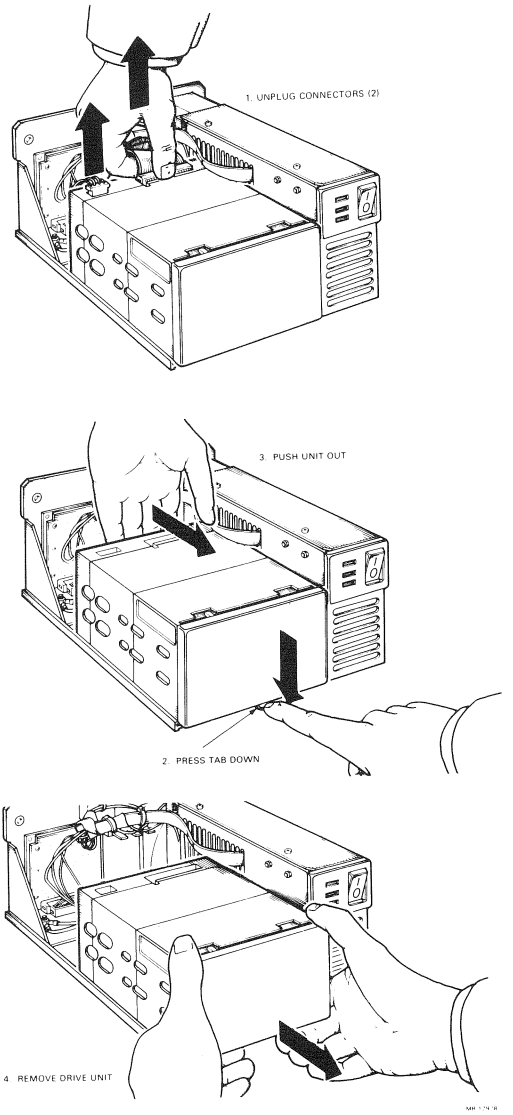

RD52 Desk-Top and Rack Mounting Housings



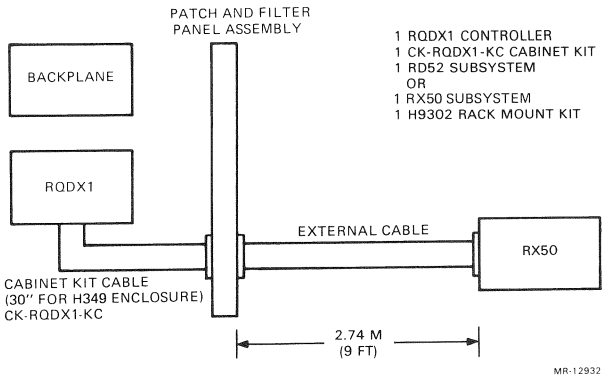

Front Panel, Switches and Indicators



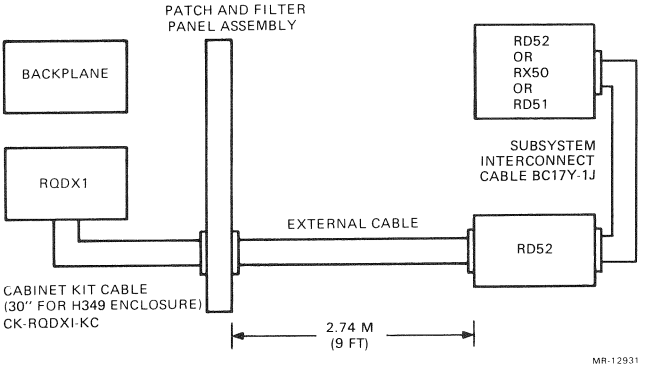

Rear Panel



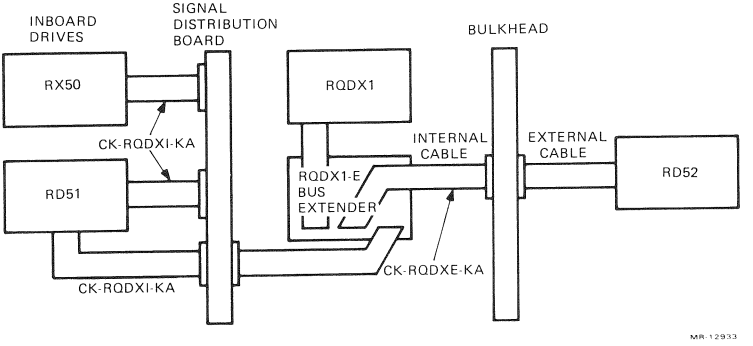

Removal of Flexible Disk Drive Signal and Power Cable




One Subsystem Add-On to a PDP-11/23 PLUS




Two Subsystem Add-Ons to H349 Distribution Panel




Maximum Expansion Configuration

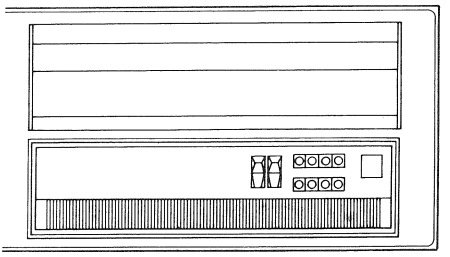
# RK05 DISK DRIVE SUBSYSTEM

### RK05 Disk Drive

The RK05-J disk drive uses a removable disk cartridge and the RK05-F uses a fixed, dual-density disk cartridge. Both drives are interfaced by the RKV11-D option. The RKV11-D is set at address 177400 and vector 220. Applicable diagnostic programs are found in Appendix A.

### Related Documentation

RKV11-D Field Maintenance Print Set (MP-00223-00)
RK05-J Field Maintenance Print Set (MP-0RK05-0J)
RK05-F Field Maintenance Print Set (MP-0RK05-0F)
*RKV11-D User's Guide* (EK-RKV11-OP)
*Microcomputer Interfaces Handbook* (EB-20175-20)
*RK05 Disk Drive User's Guide* (EK-0RK05-OP)
*RK05/05J/05F Maintenance Manual* (EK-RK5JF-MM)
*RK05 Exercisor Maintenance Manual* (EK-RK05X-MM)




RK05 Disk Drive

**Controls and Indicators for the RK05, RK05-J, and RK05-F**

| Controls and Indicators | Description |
|---|---|
| RUN/LOAD (Rocker Switch) | Placing this switch in the RUN position (provided that all interlocks are safe):<br>a. locks the drive front door<br>b. accelerates the disk to operating speed<br>c. loads the read/write heads<br>d. lights the RDY indicator.<br>Placing this switch in the LOAD position:<br>a. unloads the read/write heads<br>b. stops the disk rotation<br>c. unlocks the drive front door when the disk has stopped<br>d. lights the LOAD indicator. |
| | **CAUTION**<br>**Do not switch to the LOAD position during a write operation; this results in erroneous data being recorded.** |
| WT PROT (Rocker Switch Spring-Loaded Off) | Placing this momentary contact switch in the PROT position lights the WT PROT indicator and prevents a write operation; it also turns off the FAULT indicator, if that is lit.<br>Depressing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation. |
| PWR (Indicator) | Lights when operating power is present. Goes off when operating power is removed. |
| RDY (Indicator) | Lights when:<br>a. the disk is rotating at the correct operating speed<br>b. the heads are loaded<br>c. no other conditions are present (all interlocks safe) to prevent a seek, read, or write operation.<br>Goes off when the RUN/LOAD switch is set to LOAD. |

**Controls and Indicators for the RK05, RK05-J, and RK05-F (Cont)**

| Controls and Indicators | Description |
|---|---|
| ON CYL (Indicator) | Lights when:<br>a. the drive is in the ready condition<br>b. a seek or restore operation is not being performed<br>c. the read/write heads are positioned and settled.<br>Goes off during a seek or restore operation. |
| FAULT (Indicator) | Lights when:<br>a. erase or write current is present without a write gate<br>b. the linear positioner transducer lamp is inoperative.<br>Goes off when the WT PROT switch is pressed, or when the drive is recycled through a run/load sequence. |
| WT PROT (Indicator) | Lights when:<br>a. the WT PROT switch is pressed<br>b. the operating system sends a WRITE PROTECT command.<br>Goes off when the WT PROT switch is pressed a second time, or when the drive is recycled through a run/load sequence. |
| LOAD (Indicator) | Lights when the read/write heads are fully retracted and the spindle has stopped rotating. |
| WT (Indicator) | Lights when a write operation occurs. Goes off when the write operation terminates. |
| RD (Indicator) | Lights when a read operation occurs. Goes off when the read operation terminates. |

## Performance Specifications

### Storage Medium

| | |
|---|---|
| Type | Single-disk magnetic cartridge (RK05, RK05J - removable; RK05F - nonremovable) |
| Disk Diameter | 5.51 cm (14 inches) |

### Magnetic Heads

| | |
|---|---|
| Number | 2 |

### Bit Transfer

| | |
|---|---|
| Transfer Code | Double frequency, NRZ recording |
| Transfer Rate | 1.44 m bit/s |

### Electrical Requirements

| | |
|---|---|
| Voltage | 115/230 Vac @ 50/60 Hz ± .05 Hz |
| Power | 250 VA |
| Starting Current | Power only: 1.8 A<br>Start spindle: 10 A (for 2 seconds) |

### Model Designation

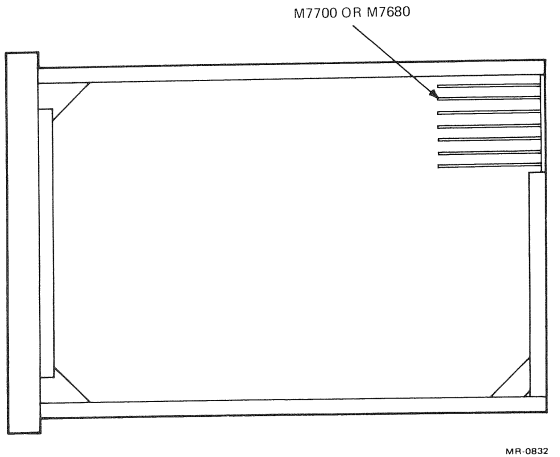
RK05-AA, RK05J-AA, RK05F-AA, RK05F-FA 95 - 130 Vac @ 60 ± 0.5 Hz
RK05-AB, RK05J-AB, RK05F-AB, RK05F-FB 290 - 260 Vac @ 60 ± 0.5 Hz
RK05-BA, RK05J-BA, RK05F-AC, RK05F-FC 95 - 130 Vac @ 50 ± 0.5 Hz
RK05-BB, RK05J-BB, RK05F-AD, RK05F-FD 190 - 260 Vac @ 50 ± 0.5 Hz

### Dimensions and Weight

Width: 48 cm (19 in)
Depth: 67 cm (26.5 in)
Height: 27 cm (10.5 in)
Weight: 50 kg (110 lb)

### Unit Selection

An RK05 disk drive may be configured to respond to a desired unit designation by selecting the appropriate setting on a rotary switch. The rotary switch is located on the second module in the card cage. The circuit cards are located behind the prefilter, and may be accessed by removing the rear cover panel on the bottom side of the disk drive unit. In the RK05-J, the rotary switch is on the M7700 module. In the RK05-F it is on the M7680.



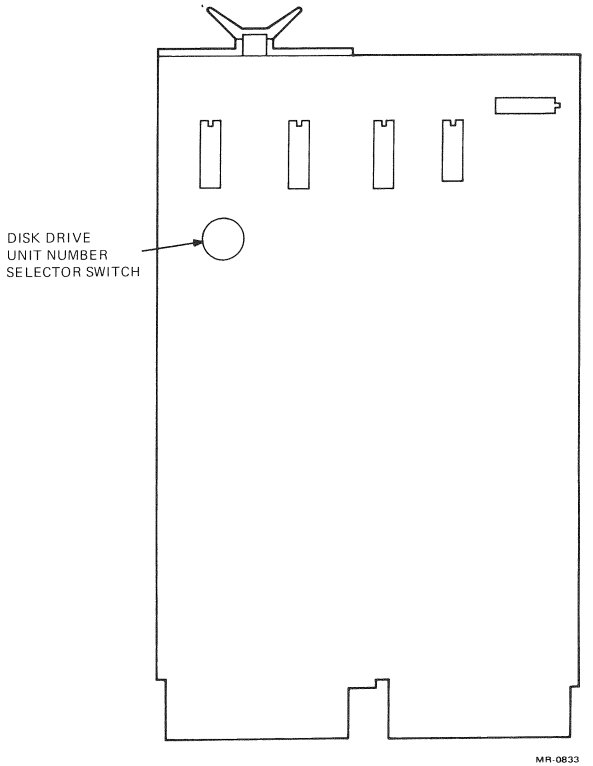

M7700 or M7680 Placement

### Bootstrap Program for RK05

If an RK05 is used in a system that has no hardware bootstrap module, the disk drive may be booted by entering the following program manually.

```
@R0/000000 0n0000<CR>*
@R1/000000 177404<CR>
@1000/000000 000005<LF>
001002/000000 010061<LF>
001004/000000 000006<LF>
001006/000000 012761<LF>
001010/000000 177400<LF>
001012/000000 000002<LF>
001014/000000 012711<LF>
001016/000000 000005<LF>
001020/000000 105711<LF>
001022/000000 100376<LF>
001024/000000 005007<CR>
@1000G
```

*n = 0 for drive 0; 2 for drive 1; and 4 for drive 2.




Controller Switches

# RL01/RL02 5.2/10.4 Mb CARTRIDGE DISK DRIVE UNIT

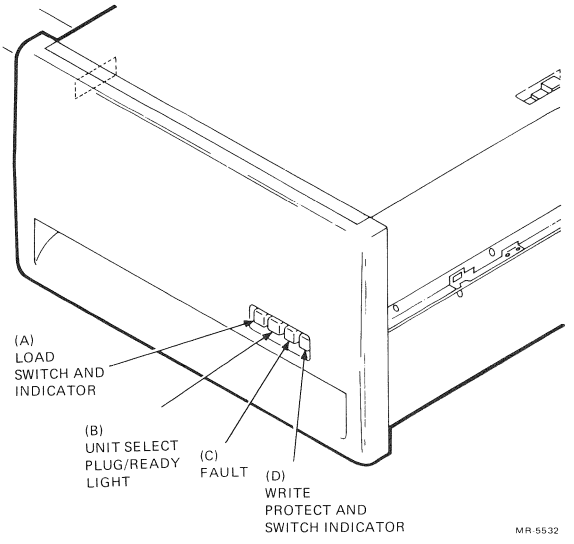
**RL01/RL02 Disk Drive**
The RL01 is a 5,000,000 byte disk drive that uses a modified, removable, 5440-style cartridge (RL01K-DC). The RL02 is a dual-density version of the RL01. The RL02 uses an RL02K-DC cartridge. Both the RL01 and RL02 use the RLV11 interface module. Up to four drives of either type in any combination can be connected to an RLV11 interface. The RLV11 is normally configured for a bus address of 77440X octal with a vector address of 160 octal. For more in-depth information, refer to the RLV11 (M8013/8014) section. Additional information can be found in the following manuals.

*RL01/RL02 Disk Drive Technical Manual* (EK-RL012-TM)
*RLV11 Technical Description* (EK-RLV11-TD)
*RL01/RL02 Pocket Service Guide* (EK-RL012-PG)
*RL01/RL02 Disk Subsystem User's Guide* (EK-RL012-UG)
*RL01 Illustrated Parts Breakdown* (EK-0RL01-IP)
*RL02 Illustrated Parts Breakdown* (EK-0RL02-IP)
RL01 Field Maintenance Print Set (MP-00527-00)
RL02 Field Maintenance Print Set (MP-00698-00)
RLV11 Field Maintenance Print Set (MP-00635-00)
*Microcomputer Interfaces Handbook* (EB-20175-20)

**Specifications RL01/RL02**

**Medium**

| | |
|---|---|
| Type: | Single platter, top-loading cartridge (similar to IBM 5440). Embedded servo information. |
| Capacity: | RL01K-DC = 5.2 Mb<br>RL02K-DC = 10.4 Mb |
| Cylinders: | RL01 = 256<br>RL02 = 512 |
| Sectors: | 40 |
| Heads: | 2 |




RL01/RL02 Controls and Indicators

**Data Transfer**
MFM (Miller coding) recording; 244 ns cell time; 4.1 megabytes/s (4.9 μs/word).

**RL01/RL02 Bootstrap**
Ensure that the heads are over cylinder 0 and head 0 is selected by releasing the LOAD switch, waiting for the LOAD indicator to light, then depressing the LOAD switch. After the drive is ready, initialize the controller with a system initialize. Perform a bit status clear. Load the following program into memory.

| LOC | Contents | Comments |
|---|---|---|
| 10000 | 012737 | Load CSR |
| 10002 | 000014 | |
| 10004 | 174400 | |
| 10006 | 000001 | Wait |

Start the program at 10000 and allow it to run for a few seconds, halt the program and restart at 00000.

## RL01/RL02 Controls and Indicators

| Switches | Function |
|---|---|
| Power ON/OFF Circuit Breaker (Located in the rear of the drive) | In the OFF position, ac power is removed from the drive.<br><br>In the ON position, ac power is supplied to the drive. |
| (A) LOAD | This is a PUSH/PUSH alternating action switch. When depressed, the RL01/RL02 begins a "cycle up" sequence, provided that:<br><br>• the RL01/RL02K cartridge is installed<br>• the cartridge cover is in place<br>• the access door is closed<br>• all ac and dc voltages are within spec<br>• the R/W heads are retracted<br>• the brushes are in the "home" position.<br><br>When released, the RL01/RL02 will begin a "cycle down" sequence. |
| (B) UNIT SELECT PLUG | This is a cam-operated switch that is activated by inserting a numbered, cammed button. The switch contacts are binary encoded so that the drive assumes the logical unit number that is printed on the button. |
| (D) WRITE PROTECT | This is an alternating action PUSH/PUSH switch. When depressed, the drive assumes a write protect status (during a write operation). When released, the drive is no longer write protected. |

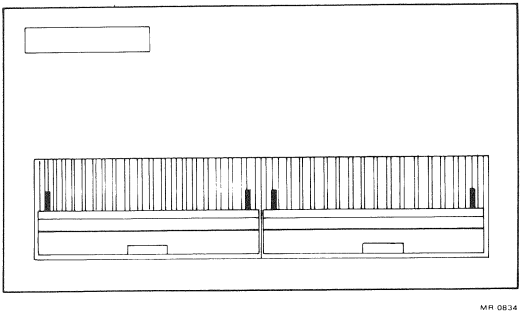
**RL01/RL02 Controls and Indicators (Cont)**

| Indicators | Function |
|---|---|
| (A) LOAD (Yellow) | Indicates that the drive is ready to have a cartridge loaded (or unloaded). The LOAD indicator will light when:<br><br>• the spindle is stopped<br>• the R/W heads are "home"<br>• the brushes are "home." |
| (B) READY (White) | When lit, indicates a "drive ready" condition; i.e., the heads are loaded and detented. |
| (C) FAULT (Red) | Indicates when one of the following has occurred.<br><br>• drive select error<br>• seek timeout error (1.5 second)<br>• write current in heads during "sector time"<br>• loss of system clock from RLV11<br>• write data error (no transitions)<br>• spin error (over speed or 40 sec timeout)<br>• write gate error (attempting to write when not ready, when write protected, or during sector time) |
| (D) WRITE PROTECT (Yellow) | Indicates that drive is write protected. That is, write operations to the cartridge will be inhibited (and the FAULT indicator will light). |

# RX01 FLOPPY DISK DRIVE

### RX01 Floppy Disk Drive

The RX01 floppy disk drive is part of the RXV11 floppy disk system, and is interfaced by the RXV11 interface module (M7946). The disk system uses address 177170 and vector 264 for the first option, and address 177174 and vector 270 for a second option.




RX01 Floppy Disk

### Model Designations

RXV11-AA Single Drive System, 115 V/60 Hz
RXV11-AC Single Drive System, 115 V/50 Hz
RXV11-AD Single Drive System, 230 V/50 Hz
RXV11-BA Dual Drive System, 115 V/60 Hz
RXV11-BC Dual Drive System, 115 V/50 Hz
RXV11-BD Dual Drive System, 230 V/50 Hz

### Related Documentation

*RXV11 User's Manual* (EK-RXV11-00)
*RX01/RX8/RX11 Floppy Disk System Maintenance Manual* (EK-RX01-MM)
RXV11 Field Maintenance Print Set (MP-00024-00)
RX01 Field Maintenance Print Set (MP-00296-00)
RX01/RX02 Reference Card (EK-RX01-RC)
*Microcomputer Interfaces Handbook* (EB-20175-20)

**NOTE**

**50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion. Refer to the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual* for complete input power modification details.**

### AC Power

The RXV11 floppy disk system is available in the following three ac voltage/model configurations.

| Models | Voltage/Frequency |
|---|---|
| RXV11-AA, -BA | 100 Vac–132 Vac, 60 Hz |
| RXV11-AC, -BC | 100 Vac–132 Vac, 50 Hz |
| RXV11-AD, -BD | 180 Vac–264 Vac, 50 Hz, in one of two voltage ranges. The actual voltage range is user-selected by installing the appropriate power harness during system installation, as follows. |

| Voltage Range | Power Harness PN |
|---|---|
| 180–240 | 70-10696-04 |
| 200–264 | 70-10696-03 |

### Power Consumption

| | |
|---|---|
| RX01 | 3 A at 24 V (dual), 75 W;<br>5 A at 5 V, 25 W |
| RXV11 interface (M7946) | Not more than 1.5 A at 5 Vdc |
| Power input (ac) | 4 A at 115 Vac<br>2 A at 230 Vac |

# RX01

## Bootstraps for Manual Entry

### Full Length Version

```
@1000/000000 12702<LF>
001002/000000 1002n7<LF>*
001004/000000 12701<LF>
001006/000000 177170<LF>
001010/000000 130211<LF>
001012/000000 1776<LF>
001014/000000 112703<LF>
001016/000000 7<LF>
001020/000000 10100<LF>
001022/000000 10220<LF>
001024/000000 402<LF>
001026/000000 12710<LF>
001030/000000 1<LF>
001032/000000 6203<LF>
001034/000000 103402<LF>
001036/000000 112711<LF>
001040/000000 111023<LF>
001042/000000 32011<LF>
001044/000000 1776<LF>
001046/000000 100756<LF>
001050/000000 103766<LF>
001052/000000 105711<LF>
001054/000000 100771<LF>
001056/000000 5000<LF>
001060/000000 22710<LF>
001062/000000 240<LF>
001064/000000 1347<LF
001066/000000 122702<LF>
001070/000000 247<LF>
001072/000000 5500<LF>
001074/000000 5007<CR>
```

*n = 4 for unit 0
n = 6 for unit 1
<LF> = Line Feed
<CR> = Carriage Return
Starting address = 1000

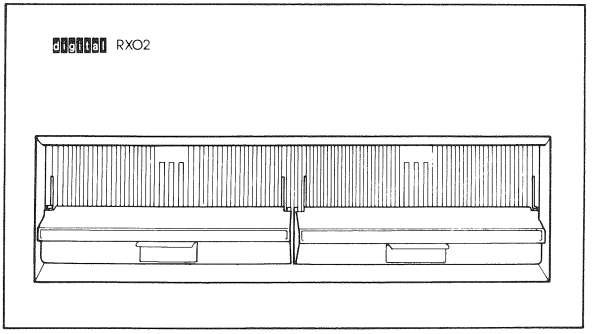
### Abbreviated Version (Drive 0 Only)

```
@1000/000000 5000<LF>
001002/000000 12701<LF>
001004/000000 177170<LF>
001006/000000 105711<LF>
001010/000000 1776<LF>
001012/000000 12711<LF>
001014/000000 3<LF>
001016/000000 5711<LF>
001020/000000 1776<LF>
001022/000000 100405<LF>
001024/000000 105711<LF>
001026/000000 100004<LF>
001030/000000 116120<LF>
001032/000000 2<LF>
001034/000000 770<LF>
001036/000000 0<LF>
001040/000000 5007<CR>
```

# RX02 FLOPPY DISK DRIVE

**RX02 Floppy Disk Drive**

The RX02 is part of the RXV11-XX floppy disk system. The RXV21-BX options use the RX02 in double-density mode with the RXV21 (M8029) interface module. The RXV21-DX options use the RX02 in single-density mode with the RXV11 (M7946) interface module.




Front View of the Floppy Disk System

The density mode of the RX02 is selected by switches on the M7744 controller module. This module is located in the RX02 floppy disk drive. The following switch settings define the mode of the RX02.

**Controller Configuration Switch Settings (Located on M7744 Module)**

| Interface | S1-1 | S1-2 |
|---|---|---|
| RX211/RXV21 | OFF | ON |
| RX8E/RX11/RXV11 | ON | OFF |
| RX28 | OFF | OFF |

**NOTE**

**The subject of the RX02 as used in a PDP-8 system is beyond the scope of this document.**

Detailed configuration and diagnostic information is contained in this manual. Refer to the section covering the applicable interface (M7946 or M8029).

## Related Documentation

*RX02 Floppy Disk System User's Guide* (EK-0RX02-UG)
RX01/RX02 Reference Card (EK-RX102-RC)
*Microcomputer Interface Handbook* (EK-20175-20)
RX02 Print Set (MP-00629-00)

## Module Designations

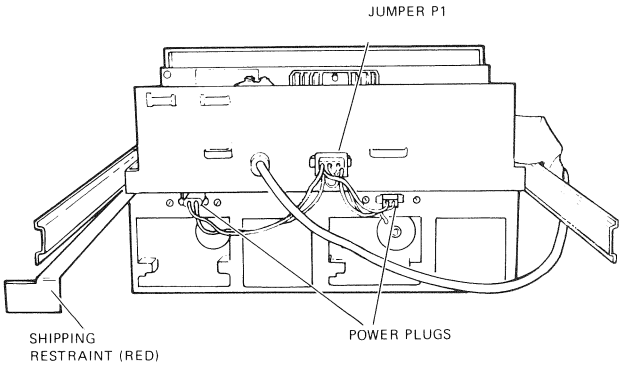
| | | | | |
|---|---|---|---|---|
| RXV21 | -DA | M7946 | RX02-DA | 115 V, 60 Hz |
| | -DC | M7946 | RX02-DC | 115 V, 50 Hz |
| | -DD | M7946 | RX02-DD | 230 V, 50 Hz |
| | -BA | M8029 | RX02-BA | 115 V, 60 Hz |
| | -BC | M8024 | RX02-BC | 115 V, 50 Hz |
| | -BD | M8027 | RX02-BD | 230 V, 50 Hz |

### Power Requirements

The RX02 is designed to use either a 60 Hz Vac or a 50 Hz power source. The 60 Hz version will operate from 90 Vac-128 Vac, without modifications, and will use less than 4 A operating. The 50 Hz version will operate within four voltage ratings and will require field verification/modification to ensure that the correct voltage option is selected. The voltage ranges of 90 Vac-120 Vac and 184 Vac-240 Vac will use less than 4 A operating. The voltage ranges of 100 Vac-128 Vac and 200 Vac-256 Vac will use less than 2 A. Both versions of the RX02 will be required to receive the input power from an ac source (e.g., 861 power control) that is controlled by the system's power switch.

### Input Power Modification Requirements

The 60 Hz version of the RX02 uses the H771-A power supply and will operate on 90 Vac-128 Vac, without modification. To convert to operate on a 50 Hz power source in the field, the H771-A supply must be replaced with an H771-C or -D and the drive motor belt and drive motor pulley must be replaced. The H771-C operates on a 90 Vac-120 Vac or 100 Vac-128 Vac power source. The H771-D operates on a 184 Vac-240 Vac or 200 Vac-256 Vac power source. To convert the H771-C to the higher voltage ranges or the H771-D to the lower voltage ranges, the power harness and circuit breaker must be changed. The appropriate jumper and circuit breaker are shown in the following figure.




| VOLTAGE (VAC) | JUMPER | CIRCUIT BREAKER |
|---|---|---|
| 90-120 | 70-10696-02 | 3.5 A, 12-12301-01 |
| 100-128 | 70-10696-01 | 3.5 A, 12-12301-01 |
| 184-240 | 70-10696-04 | 1.75 A, 12-12301-00 |
| 200-256 | 70-10696-03 | 1.75 A, 12-12301-00 |

MR-5531

RX02 (Rear View)

## Bootstrap for Manual Entry (ODT)

### RX02/RXV11 (M7946)

```
@1000/XXXXXX    5000<LF>
1002/XXXXXX     12701<LF>
1004/XXXXXX     177170<LF>
1006/XXXXXX     105711<LF>
1010/XXXXXX     1776<LF>
1012/XXXXXX     12711<LF>
1014/XXXXXX     3<LF>
1016/XXXXXX     5711<LF>
1020/XXXXXX     1776<LF>
1022/XXXXXX     100405<LF>
1024/XXXXXX     105711<LF>
1026/XXXXXX     1000004<LF>
1030/XXXXXX     116120<LF>
1032/XXXXXX     2<LF>
1034/XXXXXX     770<LF>
1036/XXXXXX     0<LF>
1040/XXXXXX     5000<LF>
1042/XXXXXX     110<CR>
@1000G
```

<LF> = Line Feed.
<CR> = Carriage Return.
XXXXXX = Original contents of location opened

## RX02/RXV21 (M8029)

| | |
|---|---|
| @2000/XXXXXX | 12701<LF> |
| 2002/XXXXXX | 177170<LF> |
| 2004/XXXXXX | 12700<LF> |
| 2006/XXXXXX | 100240<LF> |
| 2010/XXXXXX | 5002<LF> |
| 2012/XXXXXX | 12705<LF> |
| 2014/XXXXXX | 200<LF> |
| 2016/XXXXXX | 12704<LF> |
| 2020/XXXXXX | 401<LF> |
| 2022/XXXXXX | 12703<LF> |
| 2024/XXXXXX | 177172<LF> |
| 2026/XXXXXX | 30011<LF> |
| 2030/XXXXXX | 1776<LF> |
| 2032/XXXXXX | 100436<LF> |
| 2034/XXXXXX | 12711<LF> |
| 2036/XXXXXX | 407<LF> |
| 2040/XXXXXX | 30011<LF> |
| 2042/XXXXXX | 1776<LF> |
| 2044/XXXXXX | 100431<LF> |
| 2046/XXXXXX | 110413<LF> |
| 2050/XXXXXX | 304<LF> |
| 2052/XXXXXX | 30011<LF> |
| 2054/XXXXXX | 1776<LF> |
| 2056/XXXXXX | 110413<LF> |
| 2060/XXXXXX | 304<LF> |
| 2062/XXXXXX | 30011<LF> |
| 2064/XXXXXX | 1776<LF> |
| 2066/XXXXXX | 1100420<LF> |
| 2070/XXXXXX | 12711<LF> |
| 2072/XXXXXX | 403<LF> |
| 2074/XXXXXX | 30011<LF> |
| 2076/XXXXXX | 1776<LF> |
| 2100/XXXXXX | 100413<LF> |
| 2102/XXXXXX | 10513<LF> |
| 2104/XXXXXX | 30011<LF> |
| 2106/XXXXXX | 1776<LF> |
| 2110/XXXXXX | 100407<LF> |
| 2112/XXXXXX | 10213<LF> |
| 2114/XXXXXX | 6052<LF> |
| 2116/XXXXXX | 60502<LF> |
| 2120/XXXXXX | 122424<LF> |
| 2122/XXXXXX | 120427<LF> |
| 2124/XXXXXX | 7<LF> |

**RX02/RXV21 (M8029) (Cont)**

```
2126/XXXXXX     3737<LF>
2130/XXXXXX     5000<LF>
2132/XXXXXX     5007<LF>
2134/XXXXXX     0<CR>
@2000G
```

# RX50 FLOPPY DISK DRIVE SUBSYSTEM

**GENERAL**
The RX50 R/D (rack or desk mount) uses an RQDX1 controller interface which controls up to four logical units. The RX50 uses two logical units and the RD51 uses one logical unit. With a system using an RQDX1 controller, the maximum configuration that can be used is two RX50 disk drive units or one RX50 and one RD50 disk unit, expandable by one RD51 drive unit by using an RQDX1-E bus extender option.

**RX50 Flexible Disk Drives – 120 Vac or 240 Vac Voltage Selectable**

Power Supply

| | +12 Av | +5 V | +12 Battery voltage |
|---|---|---|---|
| Minimum | .1 A | .3 A | 0 A |
| Maximum | 1.3 A | 5.0 A | .12 A |

RX50 Voltage

| | | | |
|---|---|---|---|
| Maximum | 3 A | .8 A | .12 A |
| Minimum | 1.3 A | .5 A | .12 A |
| Standby | 0.1 A | .5 A | .12 A |

Capacity (diskette)
800K bytes

**Related Documentation**

*MICRO/PDP-11 System, Technical Manual* (EK-OLCP5-TM)
*MICRO/PDP-11 System, Owner's Manual* (EK-OLCP5-OM)
*MICRO/PDP-11 System, Unpacking and Installation Guide* (EK-OLCP5-IN)
*MICRO/PDP-11 System Option Manual* (EK-OLCP5-OD-001)
*RQDX1 Controller Module User's Guide* (EK-RQDX1-UG)
(includes RQDX1-E Bus Extender)
*H9302 Rack Mounting Kit Installation Manual* (EK-LEP03-IN)

**Compatibility**
RX50 R/D units are used as add-ons in the PDP-11/23 PLUS, MICRO/PDP-11, MICRO VAX I, and other Q-BUS hosts.

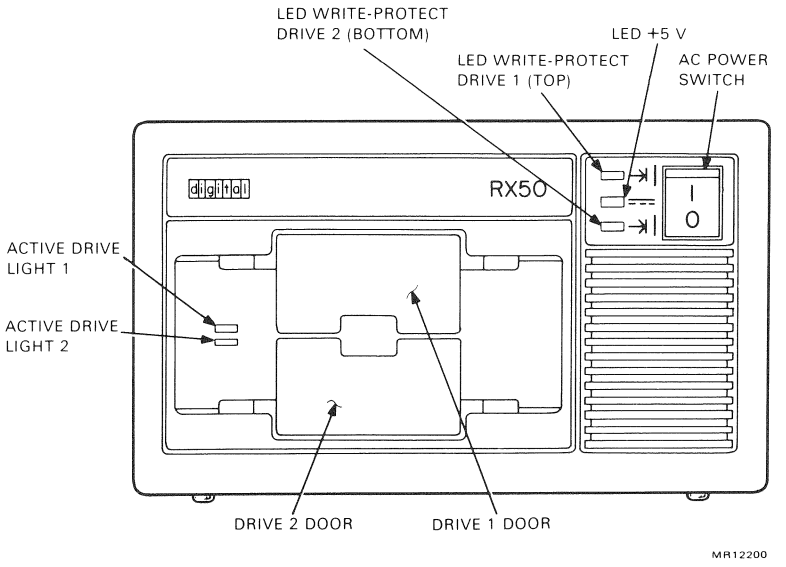
**Front Panel Controls and Indicators**

AC power ON/OFF switch – connects ac power to the internal power supply.

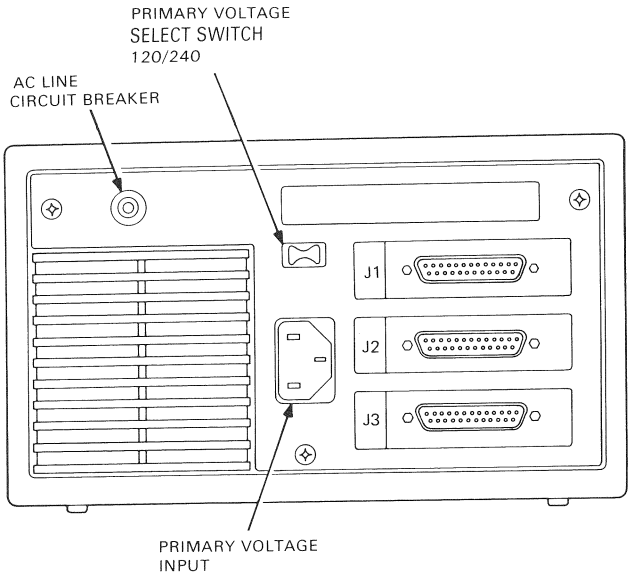
| | |
|---|---|
| TOP THREE LEDs | LIT |
| 1st (yellow) LED | When top drive is write protected |
| 2nd (green) LED | +5 Vdc is being supplied to the drive |
| 3rd (yellow) LED | When bottom drive is write protected |

**NOTE**

**Never open a disk drive door when either drive's light is on (active drive).**




Front Panel, Switches and Indicators




RX50 Rear View

**RX50 Subsystem Dimensions and Weights**

Dimensions

| | |
|---|---|
| Desk top configuration and rack mount configuration | Approximately 12 inches long 9 inches wide, 5-1/2 inches high |

Weights

| | |
|---|---|
| Desk top configuration and rack mount configuration | Approximately 14 pounds |

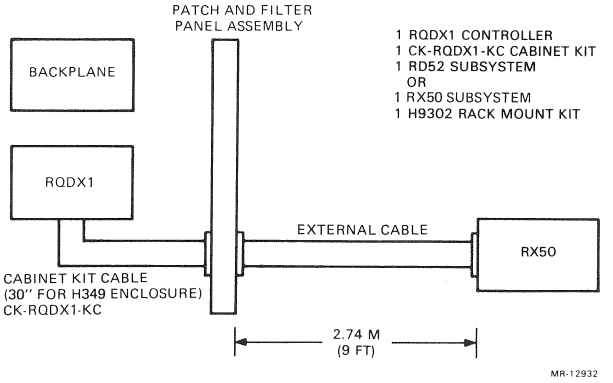
The hardware requirements for the BA23 enclosure are:

1 RQDX1 Controller
1 CK-RQDX1-KA cabinet kit
1 RX50-D subsystem
or
1 RX50-R subsystem
1 H9302 rack adapter kit.

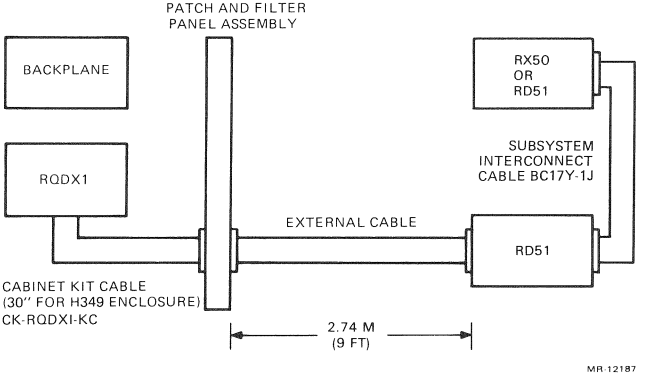
The hardware requirements for the H349 enclosure are:

1 RQDX1 controller
1 CK-RQDX1-KC cabinet kit
1 RX50-D subsystem
or
1 RX50-R subsystem
1 H9302 rack adapter kit.

The figure below illustrates how to add two subsystems, RD51 and RX50, to a BA23 or an H349 enclosure.




Single Expansion Configuration




Double Expansion Configuration

# RX50

The hardware requirements for the BA23 enclosure are:

1 RQDX1 controller
1 CK-RQDX1-KA cabinet kit.

The two subsystems can be either:

2 RD51-D subsystems or 2 RD51-R with 1 H9302 adapter kit or
1 RD51-D or -R with 1 H9302
1 RX50-D or -R with H9302
1 BC17Y-1 J subsystem interconnection cable.

The hardware requirements for the H349 enclosure are:

1 RQDX1 controller
1 CK-RQDZ1-KC cabinet kit

and the two subsystems can be either:

2 RD51-D subsystems or 2 RD51-R with 1 H9302 rack adapter kit or:

1 RD51-D or 1 RD51-R with 1 H9302 rack adapter kit
1 RX50-D or RX50-R
1 BC17Y-1J subsystem interconnection cable.

The hardware requirements are:

1 RQDX1-E RQDX1 extender
1 CK-RQDXE-KA cabinet kit RD/RX controller EXT BA23
1 RD51-D
or
1 RD51-R with 1 H302 rack adapter kit.

## SYSTEM AND EXTERNAL SUBSYSTEM INTERCONNECT

System enclosures such as the BA23 and H349 have a patch and filter panel assembly, attached to the rear of the unit. This panel has an unused area that can be used for system expansion. The internal system cabling for the external subsystem is contained in the cabinet kits and will be connected to a proper connector on the internal side of the patch panel. The subsystem user can simply connect to the external connector of the port used.

### J1, J2 and J3 Pin Numbers and Signal Names

Connectors J1, J2 and J3 have the same signal names and pin numbering.

| Pin Numbers | Signal Names | Pin Numbers | Signal Names |
|---|---|---|---|
| J1-01 | MEMWRTDT1 (H) | J1-25 | DRV SEL 4 (L) |
| J1-34 | MEMWRTDT1 (L) | J1-09 | GROUND |
| J1-18 | GROUND | J1-42 | INDEX (L) |
| J1-02 | HEAD SET 2 (L) | J1-26 | RD1WRTPRO (L) |
| J1-35 | GROUND | J1-10 | DRV SEL 1 (L) |
| J1-19 | SEEKOPLT | J1-43 | DRV SEL 2 (L) |
| J1-03 | RD1 RDY (H) | J1-27 | DRV SEL 3 (L) |
| J1-36 | WPT FAULT (L) | J1-11 | RX2WPTLED (L) |
| J1-20 | GROUND | J1-44 | RXMOTORON (L) |
| J1-04 | READ SEL 1 (L) | J1-28 | GROUND |
| J1-37 | RXOWPTLED (L) | J1-12 | DIRECTION (L) |
| J1-21 | RD0 RDY (H) | J1-45 | GROUND |
| J1-05 | RX1WPTLED (L) | J1-29 | STEP (L) |
| J1-38 | DRVSLOACK (L) | J1-13 | GROUND |
| J1-22 | MEMRDDAT0 (H) | J1-46 | RXWRTDATA (L) |
| J1-06 | MFMRDDAT0 (L) | J1-30 | GROUND |
| J1-39 | MFMWRTDT0 (H) | J1-14 | WRT GATE (L) |
| J1-23 | MFMWRTDT0 (L) | J1-47 | GROUND |
| J1-07 | MFMRDDAT1 (H) | J1-31 | TRACK 00 (L) |
| J1-40 | MFMRDDAT1 (L) | J1-15 | RX3WPTLED (L) |
| J1-24 | GROUND | J1-48 | DRVSL1ACK (L) |
| J1-08 | RFDUCWRTI (L) | J1-32 | GROUND |
| J1-41 | RD0WRTPRO (L) | J1-16 | READ DATA (L) |
| | | J1-49 | GROUND |
| | | J1-33 | HEAD SEL 0 (L) |
| | | J1-17 | GROUND |
| | | J1-50 | READY (L) |

## Power Supply Connectors

### AC Power Input Connector

| Pin No. | Signal |
|---|---|
| 1 | Ground |
| 2 | AC phase |
| 3 | AC neutral |

### DC Power Output Connector

| Pin No. | Signal |
|---|---|
| 1 | +5 V |
| 2 | +5 V |
| 3 | +5 V |
| 4 | Return |
| 5 | Return |
| 6 | Return |
| 7 | Return |
| 8 | 12 VA |
| 9 | 12 VA |
| 10 | 12 VB |
| 11 | No pin |
| 12 | No connection |

### Logical Unit Number Selection

The logical unit number (LUN) selection is set by jumpers on the RQDX1 controller module. These jumpers are set to the lowest LUN logical unit number assigned to any RD51 or RX50 drive subsystem that is controlled by the RQDX1. The RQDX1 module automatically senses the logical unit configuration during initialization of the system to determine how many of the four possible units are actually present.

The LUN jumper format allows only one jumper to be installed at a time, and each individual jumper specifies a group of 4 logical units as follows.

| LUN Jumper | LUNs Specified |
|---|---|
| No jumper installed | 0–3 |
| 1 | 4–7 |
| 2 | 8–11 |
| 3 | 12–15 |
| 4 | 16–19 |
| 5 | 20–23 |
| 6 | 24–27 |
| 7 | 28–31 |
| 8 | 32–35 |

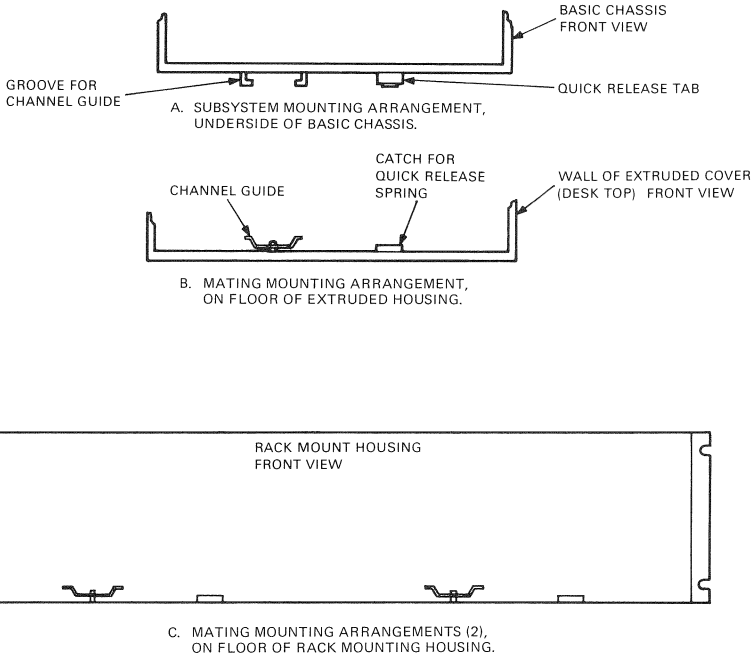
Within the context of RQDX1 configurations as shown below, if the number 4 jumper is connected and configuration number 2 is being used, then:

16 = unit 0
17 = unit 1
18 = unit 2
19 = unit 3

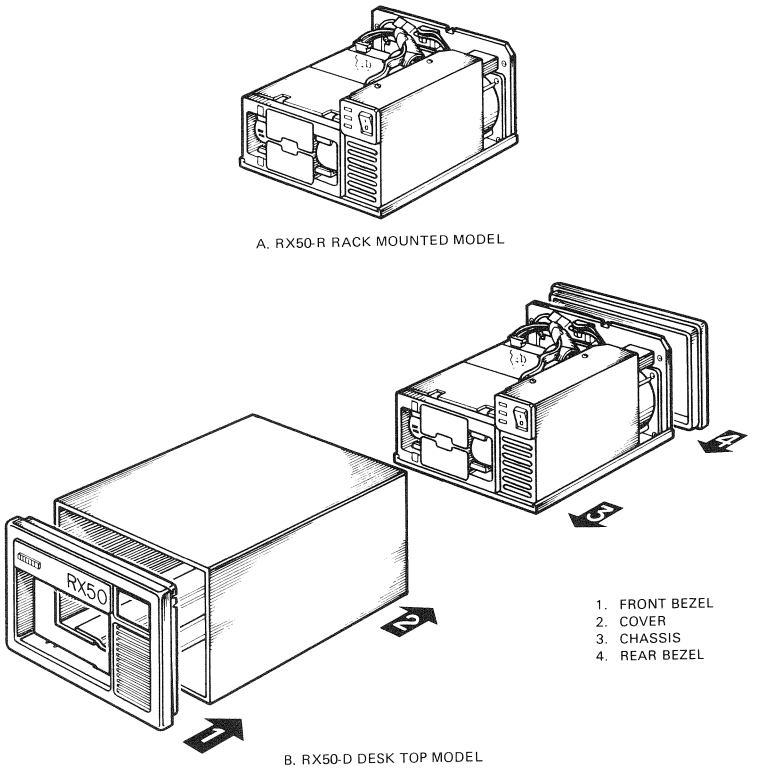
| Configuration Number | External Subsystem Disk Drives | Logical Unit Numbers for Disk Drive |
|---|---|---|
| 1 | One RD51, one RX50 | Unit 0 = RD51<br>Units 1, 2 = RX50 |
| 2 | Two RX50s | Units 0, 1 = RX50<br>Units 2, 3 = RX50 |
| 3 | Two RD51s, one RX50 | Unit 0 = RD51<br>Unit 1 = RD51<br>Units 2, 3 = RX50 |
| 4 | Two RD51s | Unit 0 = RD51<br>Unit 1 = RD51 |
| 5 | One RX50 | Units 0, 1 = RX50 |
| 6 | One RD51 | Unit 0 = RD51 |

## System Controller Options

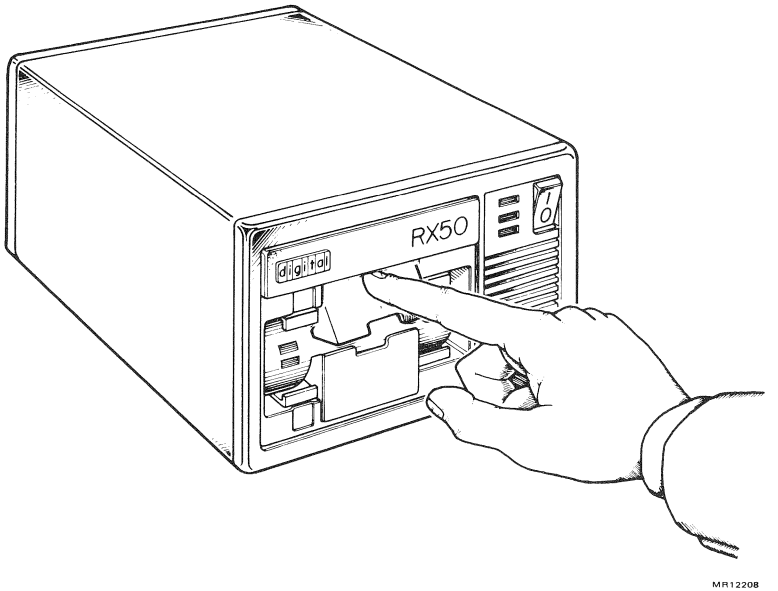
| Model | | Description |
|---|---|---|
| RQDX1 | Controller/Interface, MSCP Q-BUS | RX50 and/or RD51 MSCP controller.<br><br>One controller handles up to four logical units. No more than two RX50s per controller. One RX50L is equal to two LUNs. |
| RQDX1-E | Bus EXTENDER w/cable | Enables external drive (RX50, RD51) to connect to MICRO/PDP-11 internal controller-to-drive bus. Allows either one external RX50 or one external RD51 to be connected to the MICRO/PDP-11 controller depending on the RQDX1 configuration guidelines. |
| CK-RQDX1-KA | Cabinet kit for installing the RQDX1 controller in a BA23 enclosure (MICRO/PDP-11). | |
| CK-RQDX1-KC | Cabinet kit for installiing the RQDX1 controller with the H349 I/O panel (PDP-11/23 PLUS). | |
| CK-RQDXE-KA | Cabinet kit for installing the RQDX1-E extender in a BA23 enclosure (MICRO/PDP-11). | |
| BQ01-C | Country kit, Doc, for RQDX1 Controller and Extender. | |
| RQ01-D | Country kit, Doc, Labels, Diagnostic for RX50-R, -D. | |
| BQ01-E | Country kit, Doc, Labels for RD51-R, -D. | |



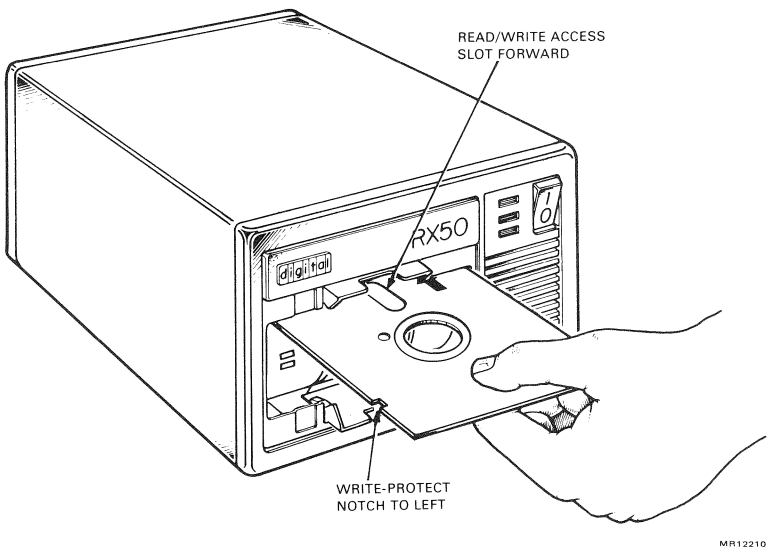

Mounting Channel and Quick Release Latch



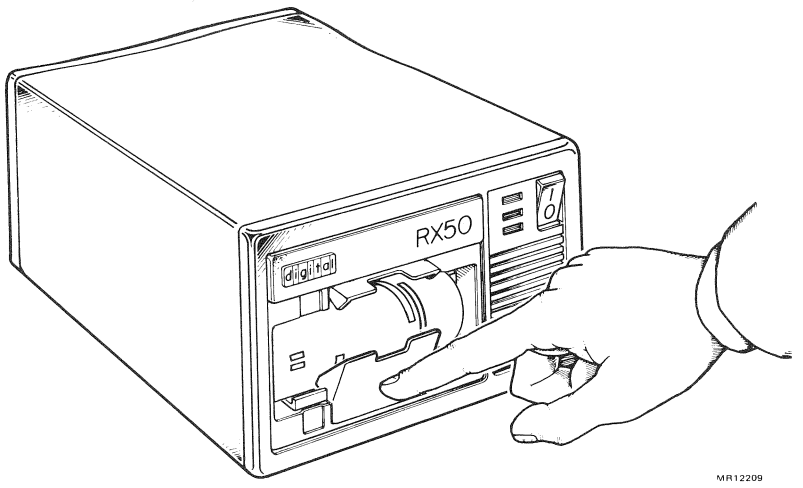

RX50 Desk-Top and Rack Mounting Housing



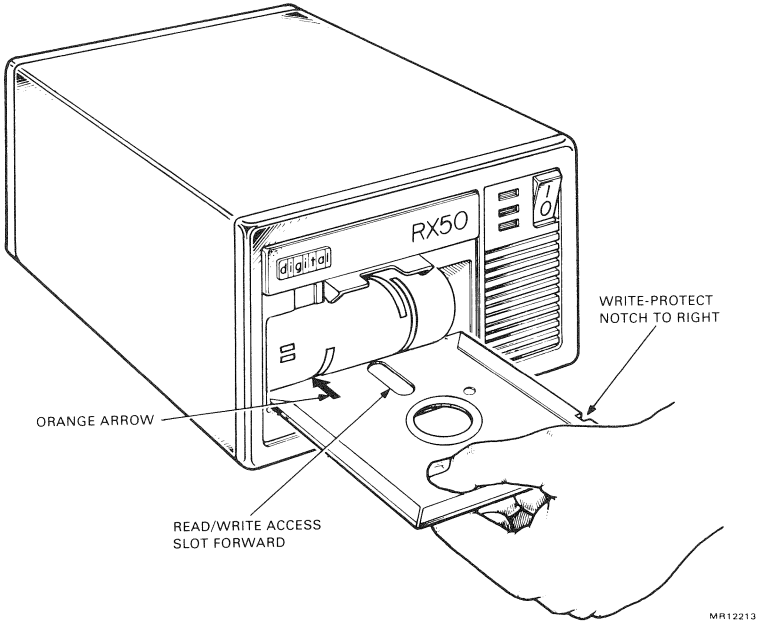

Opening the Drive 1 Door



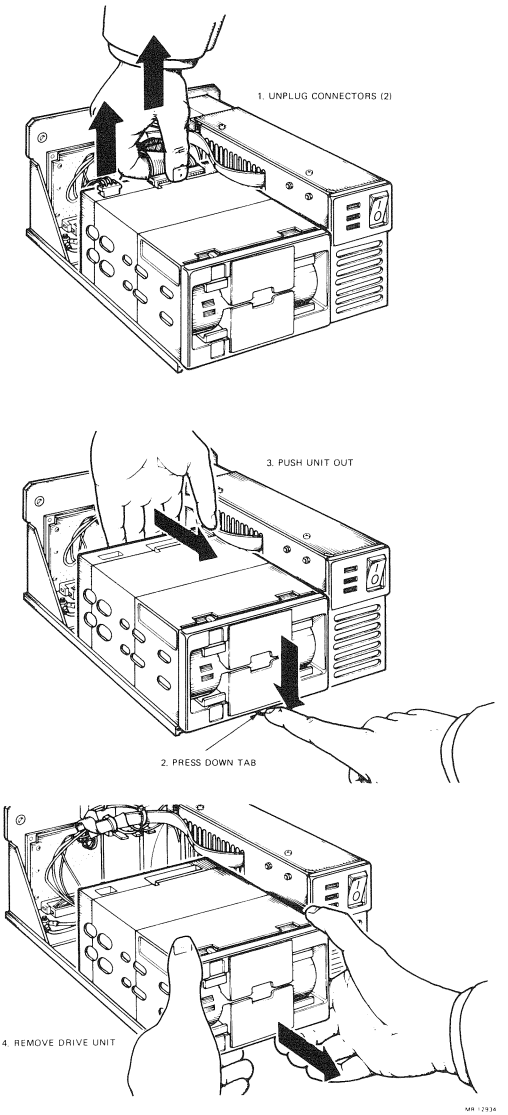

Inserting a Flexible Disk in Drive 1



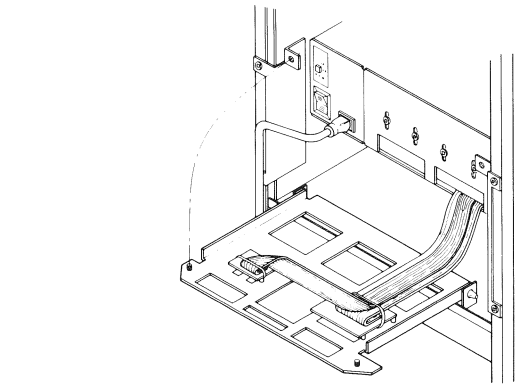

Opening the Drive 2 Door

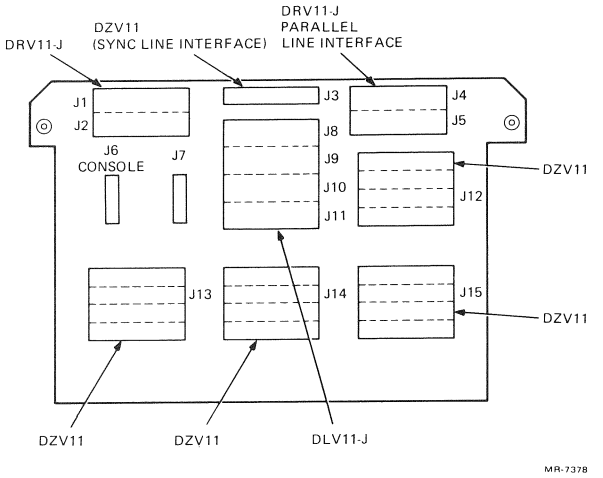



Inserting a Flexible Disk in Drive 2

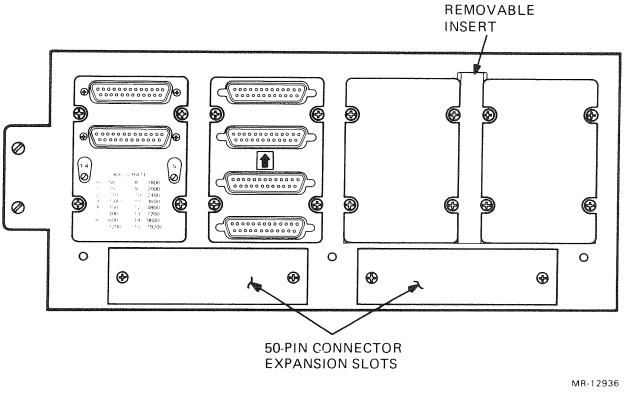



Removal of Flexible Disk Drive Signal and Power Cable

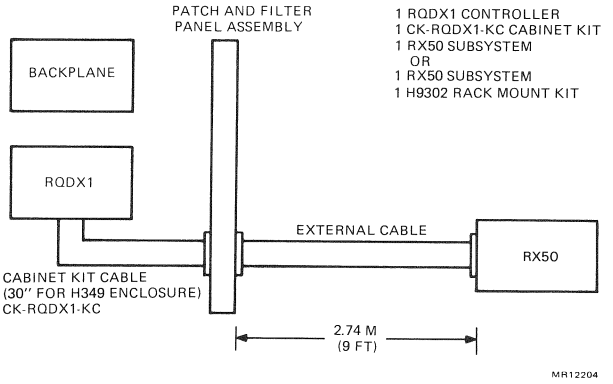





H349 Distribution Cable




BA23 Patch and Filter Panel Assembly




One Subsystem Add-On to a PDP-11/23 PLUS

# TU58 TAPE CASSETTE UNIT

## GENERAL

The TU58 DECtape II is a random access, fixed length block, mass storage tape unit. Tape cartridges are DIGITAL's preformatted reel-to-reel packages containing 42.7m (140 ft) long by 3.91mm (0.150 in) wide tape. The TU58 processor consists of an 8095 processor, supported by firmware in a 2Kb, read only memory (ROM).

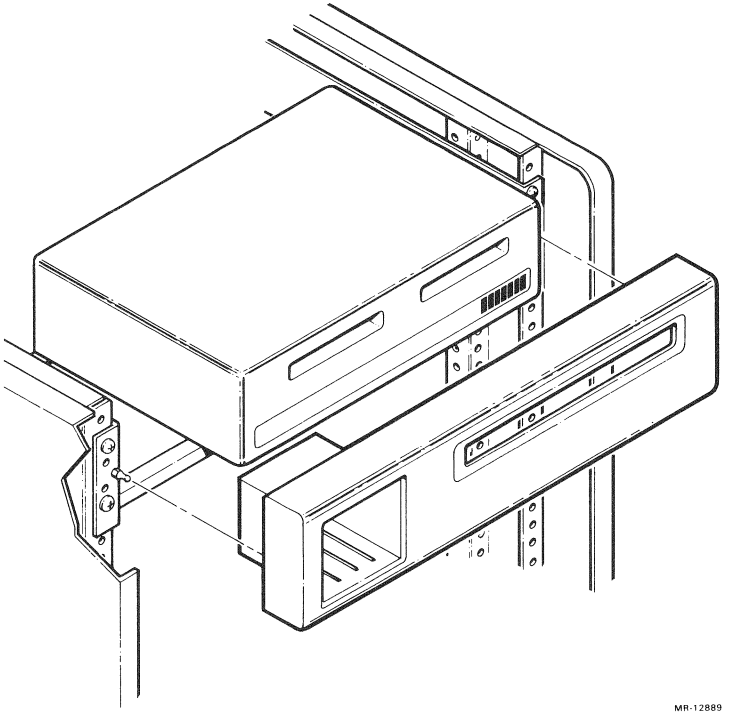
### Power Consumption

Board plus 1 and 2 drives

- 11 W typical, drive running
- +5 V ± 5% @ 0.75 A (max.)
- +12 V +10, -5% @ 1.2 A, peak
- 0.6 A average running
- 0.1 A idle

Rackmount

- 90–128 Vac 180–256 Vac
- 47–63 Hz, 35 W (max.)




Installing the Bezel

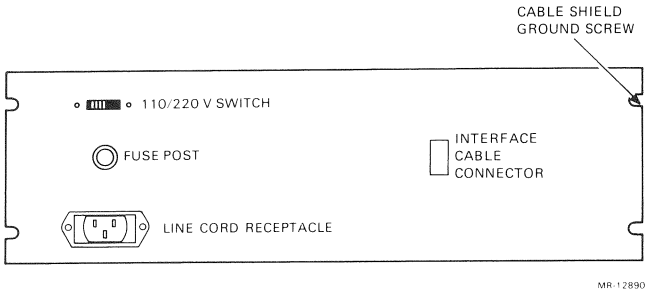
# TU58

## Related Documentation

*TU58 DECtape II User's Guide* (EK-0TU58-UG)
*TU58 DECtape II Pocket Service Guide* (EK-0TU58-PS)
*TU58 DECtape II Technical Manual* (EK-0TU58-TM)
*TU58 DECtape II Illustrated Parts IPB* (EK-0TU58-IP)
Field Maintenance Print Set (MP00747-CA)
Field Maintenance Print Set (MP01014-EA)
Field Maintenance Print Set (MP01013-VA)
Field Maintenance Print Set (MP01063-DB)

## Model Distinctions

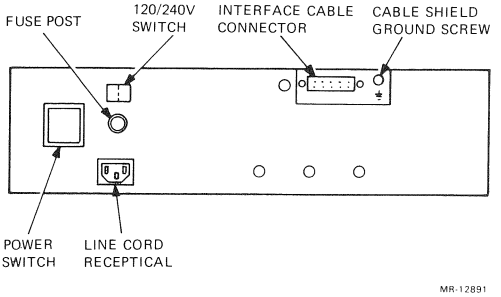
CA Rackmount
- Large chassis
- Two drives
- Serial interface controller board
- Switch selectable 120/240 Vac
- Detachable line cord
- 2 cartridges
- Boot ROM for MR11
- Two I/O cables (BC17A/BC178-18)
- Diagnostic kit (ZJ278-RG)




TU58-CA Rear Panel

DA Rackmount

Tabletop chassis
TU58-CA features with additional accessory assembly hardware kit (70-16753-00)




TU58-DA Rear Panel

EA Tabletop

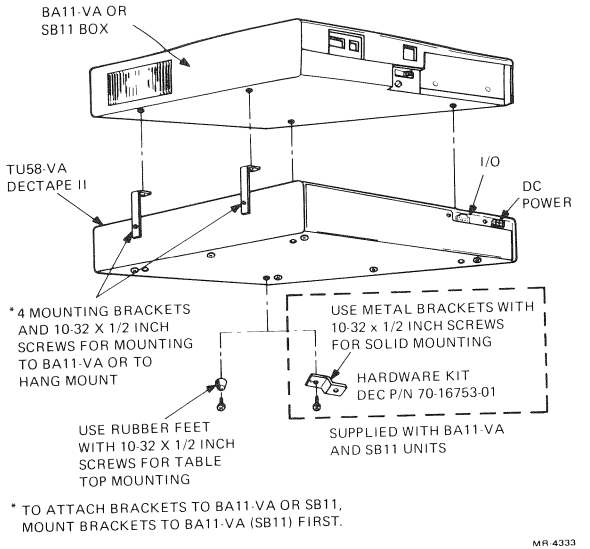
Two drives
Serial interface controller board

EB Tabletop

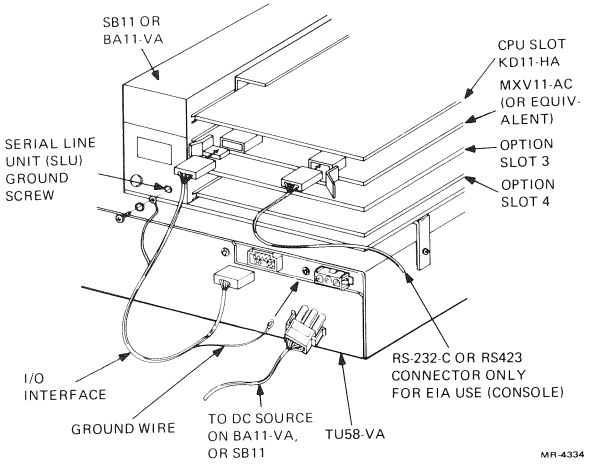
Two drives
Serial interface controller board
Two I/O cables (BC17A-18/ BC17B-18)
Boot ROM for MR11-EA
Accessory assembly hardware kit (70-16753-00)
Field Maintenance Print Set (MP01014)

VA Tabletop

Two drives
Serial interface controller
DC Power cable (70-17569-00)
I/O interface cable (70-17568-1F)
Two cartridges
MXV11-A2 boot ROM
Field Maintenance Print Set (MP01013)
Accessory assembly hardware kit (70-16753-01)




Mounting Choices for the TU58-VA




Interfacing the TU58-VA

**Accessories**

TU58-DB

Rackmount kit for tabletop versions

TU58-EC

Accessory kit with detachable line cord for hardware kit (70-16753-00)
User's guide
Field Maintenance Print Set (MP01014)

TU58-ED

Accessory kit with 120V/240V detachable line cord
Fuse for 230 Vac
Two cartridges
Two I/O cables (70-BC17A-18/BC178-18)
Boot ROM for MR11-EA
Accessory assembly hardware kit (70-16753-00)
User guide
Field Maintenance Print Set (MP01014)

TU58-VB

Accessory kit with dc power cable (70-17569-1C)
I/O cable (70-177568-1F)
Two cartridges
MXV11-A2 boot ROM
User's Guide
Field Maintenance Print Set (MP01013)
Configuration Guide

## Serial Interface Standards

To interface with the TU58, options with their appropriate cables are listed below. In accordance with RS422 (balanced) and RS423 (unbalanced) signal standards, the TU58 is compatible with devices complying with RS232-C.

**NOTE**

**BC22D-10 replaces BC17A-18 and BC17B-18. The new cable has an improved shield connection to comply with FCC regulations.**

| | |
|---|---|
| DL11 or DLV11 | 5.4 m (18 ft) 10 to 40 pin connector = BC17A-18 |
| DLV11-J | 5.4 m (18 ft) 10 to 10 pin connector = BC178-18 |
| or MXV11 | 5.4 m (50 ft) 10 to 10 pin connector = BC20M-50 |
| EIA | 1.5 m (5 ft) 10 pin to DB25S female = BC20N-05 (null modem cable) |
| | 1.5 m (5 ft) 10 pin to DB25P male = BC21B-05 (Modem cable) |

### TU58/PDP-11 Toggle-in Boot

This boots drive 0 only.

| | | |
|---|---|---|
| 1000/012701 | 1024/005012 | 1050/005003 |
| 1002/176500 | 1026/012700 | 1052/105711 |
| 1004/012701 | 1030/000004 | 1054/100376 |
| 1006/176504 | 1032/005761 | 1056/116123 |
| 1010/010100 | 1034/000002 | 1060/000002 |
| 1012/005212 | 1036/042700 | 1062/022703 |
| 1014/105712 | 1040/000020 | 1064/001000 |
| 1016/100376 | 1042/010062 | 1066/101371 |
| 1020/006300 | 1044/000002 | 1070/005007 |
| 1022/001005 | 1046/001362 | |

# APPENDIX A
# DIAGNOSTIC MEDIA AVAILABILITY

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M4002-XX | KWV11-C | VKWA??.BI? | 17,18 19,20, 21 | KWV11-A Diagnostic | | AC-8222C-MC AK-8225C-MC | 4 | 13 | 18 | 19 | 20 |
| M7264-XX | KD11-F/ KD11-H/ KD11-HW (LSI-11) | VKAA??.BI? | | LSI-11 Basic Instruction Test | (Listing) (Binary PT) | AC-8186C-MC AK-8188C-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAB??.BI? | | LSI-11 EIS Instruction Set Test | (Listing) (Binary PT) | AC-8190A-MC AK-8192A-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAC??.BI? | 5 | LSI-11 FIS Instruction Set Test | (Listing) (Binary PT) | AC-8194C-MC AK-8197C-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAD??.BI? | 5 | LSI-11 Traps Test | (Listing) (Binary PT) | AC-8198C-MC AK-8-IC-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAH??.BI? | | LSI-11 4K System Exerciser | (Listing) (Binary PT) | AC-8210A-MC AK-8212A-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAI??.BI? | 6 | LSI-11 DIS Move & String Test | (Listing) (Binary PT) | AC-8214A-MC AK-8217A-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAJ??.BI? | 6 | LSI-11 DIS Decimal Instructions | (Listing) (Binary PT) | AC-8218A-MC AK-8221A-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAL??.BI? | 5 | LSI-11 Trap Test (30K + FIS) | (Listing) (Binary PT) | AC-F012A-MC AK-F014A-MC | 4 | 13 | 18 | 19 | 20 |
| | | XCPA??.OBJ | | DEC/X11 Processor Test Module | (Listing) (Binary PT) | AC-E664G-MC AK-E665G-MC | | | | | |
| | | XCPB??.OBJ | | DEC/X11 EIS Exerciser Module | (Listing) (Binary PT) | EC-E667J-MC AK-E668J-MC | 1 | 14 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M7269 | RKV11-D | ZRKH??.BI? | 7,8 | RK11/RK05 Performance Exerciser | (Listing)<br>(Binary PT) | AC-9232G-MC<br>AK-9235G-MC | 2 | 13 | 18 | 19 | 20 |
| | | ZRKI??.BI? | 7 | RK11 Utility Package | (Listing)<br>(Binary PT) | AC-9236F-MC<br>AC-9239F-MC | 2 | 13 | 18 | 19 | 20 |
| | | ZRKJ??.BI? | 7 | RK11 Basic Logic Test No. 1 | (Listing)<br>(Binary PT) | AC-9240E-MC<br>AK-9243E-MC | 2 | 13 | 18 | 19 | 20 |
| | | ZRKK??.BI? | 7,9 | RK11 Basic Logic Test No. 2 | (Listing)<br>(Binary PT) | AC-9244F-MC<br>AK-9247F-M1 | 2 | 13 | 18 | 19 | 20 |
| | | ZRKL??.BI? | 7,10 | RK11/RK05 Dynamic Test | (Listing)<br>(Binary PT) | AC-9248E-MC<br>AK-9251E-MC | 2 | 13 | 18 | 19 | 20 |
| | | XRKA??.OBJ | 7 | DEC/X11 RK11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E676G-MC<br>AK-E677G-MC | 6 | 16 | 18 | 19 | 20 |
| M7270 | KD11-HA | VKAA??.BI? | | LSI-11 Basic Instruction Test | (Listing)<br>(Binary PT) | AC-8186C-MC<br>AK-8188C-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAB??.BI? | | LSI-11 EIS Instruction Set Test | (Listing)<br>(Binary PT) | AC-8190A-MC<br>AK-8192A-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAC??.BI? | 5 | LSI-11 FIS Instruction Set Test | (Listing)<br>(Binary PT) | AC-8194C-MC<br>AK-8197C-M1 | 4 | 13 | 18 | 19 | 20 |
| | | VKAD??.BI? | 5 | LSI-11 Traps Test | (Listing)<br>(Binary PT) | AC-8198C-MC<br>AK-8201C-MC | 4 | 13 | 18 | 19 | 20 |
| | | VKAH??.BI? | | LSI-11 4K System Exerciser | (Listing)<br>(Binary PT) | AC-8210A-MC<br>AK-8212A-MC | 4 | 13 | 18 | 19 | 20 |
| | | XCPA??.OBJ | | DEC/X11 Processor Test Module | (Listing)<br>(Binary PT) | AC-E664G-MC<br>AK-E665G-MC | 1 | 14 | 18 | 19 | 20 |
| | | XCPB??.OBJ | | DEC/X11 EIS Exerciser Module | (Listing)<br>(Binary PT) | AC-E667J-MC<br>AK-E668J-MC | 1 | 14 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M7940 | DLV11 | VKAE??.BI? | 11a,12 | DLV11 Test | (Listing) | AC-8202B-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8205B-MC | | | | | |
| | | XDLA??.OBJ | 11a | DEC/X11 DL11 Exerciser Module | (Listing) | AC-E709J-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E710J-MC | | | | | |
| M7941 | DRV11 | VKAF??.BI? | 13 | DRV11 Test | (Listing) | AC-8206D-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8208D-MC | | | | | |
| | | XDRA??.OBJ | 13 | DEC/X11 DR11-A Exerciser Module | (Listing) | AC-E854D-MC | 5 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E855D-MC | | | | | |
| M7942 | MRV11-AA | NA | | | | | | | | | |
| M7944 | MSV11-B | ZKMA??.BI? | 4a | MOS/Core 0-124K Exerciser | (Listing) | AC-8850F-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8854F-MC | | | | | |
| | | ZQMC??.BI? | 4b | 0-124K Memory Exerciser (16K) | (Listing) | AC-9045F-MC | 12 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9048F-MC | | | | | |
| M7946 | RXV11 | ZRXA??.BI? | 7,14 | RX11 System Reliability TEST | (Listing) | AC-9334E-MC | 7 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9337E-MC | | | | | |
| | | ZRXB??.BI? | 7 | RX11 Interface Diagnostic | (Listing) | AC-9339F-MC | 7 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9343F-MC | | | | | |
| | | XRXA??.OBJ | 7 | DEC/X11 RX01 Exerciser Module | (Listing) | AC-E736E-MC | 6 | 16 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E737E-MC | | | | | |
| M7948 | DRV11-P | NA | | | | | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M7949 | LAV11 | ZLAE??.BI? | | LA180 Printer Diagnostic | (Listing) | AC-8906B-MC | 7 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8908B-MC | | | | | |
| | | XLPA??.OBJ | | DEC/X11 LP11 Exerciser Module | (Listing) | AC-E670F-MC | 6 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E671F-MC | | | | | |
| M7950 | DRV11-B | VDRA??.BI? | 13,15 | DRV11-B DMA Interface Diagnostic | (Listing) | AC-8178A-MC | 8 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8180A-MC | | | | | |
| | | VDRB??.BI | | DRV11-B Interprocessor Exerciser | (Listing) | AC-8182A-MC | 8 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8184A-MC | | | | | |
| | | XDRF??.OBJ | 13 | DEC/X11 DRV11-B Exerciser Module | (Listing) | AC-E739C-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E740C-MC | | | | | |
| M7951 | DUV11-DA | ZDUQ??.BI? | 16 | DUV11 Off-Line Logic Tests | (Listing) | AC-8704C-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8707C-MC | | | | | |
| | | ZDUR??.BI? | 16 | DUV11 Off-Line Receiver Tests | (Listing) | AC-8708B-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8711B-MC | | | | | |
| | | ZDUS??.BI? | 16 | DUV11 Off-Line Receiver Timing | (Listing) | AC-8712B-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8715B-MC | | | | | |
| | | ZDUT??.BI? | 16 | DUV11 Off-Line Transmitter Tests | (Listing) | AC-8716B-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8719B-MC | | | | | |
| | | ZDUU??.BI? | 16 | DUV11 Off-Line Timing & Interrupt | (Listing) | AC-8720B-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8723B-MC | | | | | |
| | | ZDUV??.BI? | 16 | DUV11 Off-Line Combined Tests | (Listing) | AC-8724B-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8727B-MC | | | | | |
| | | XDUA??.OBJ | | DEC/X11 DU11 Exerciser Module | (Listing) | AC-E718I-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E719I-MC | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M7952 | KWV11-A | VKWA??.BI? | 17,18 19,20, 21 | KWV11-A Diagnostic | (Listing) | AC-8222C-MCM | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8225C-MC | | | | | |
| | | XKWE??.OBJ | | DEC/X11 KWV11-K Exerciser Module | (Listing) | AC-E920B-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E921B-MC | | | | | |
| M7954 | IBV11-A | VIBA??.BI? | 22,23, 24 | IBV11-A Diagnostic | (Listing) | AC-A880A-MC | 8 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-A882A-MC | | | | | |
| | | VIBB??.BI? | 22,23, 24 | IBV11-A (30K) Diagnostic | (Listing) | AC-F015A-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-F017A-M1 | | | | | |
| | | XIBA??.OBJ | 25 | IBV11-A Exerciser Module | (Listing) | AC-E914D-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E915D-MC | | | | | |
| M7955 | MSV11-C | ZKMA??.BI? | 4a | MOS/Core 0-124K Exerciser | (Listing) | AC-8850F-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8854F-MC | | | | | |
| | | ZQMC??.BI? | 4b | 0-124K Memory Exerciser (16K) | (Listing) | AC-9045F-MC | 12 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9048F-MC | | | | | |
| M7957 | DZV11 | VDZA??.BI? | 26,27 | DZV11 4 Line Asynch MUX 1 OF 2 | (Listing) | AC-A877A-MC | 9 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-A879A-MC | | | | | |
| | | VDZB??.BI? | 26,27 | DZV11 4 Line Asynch MUX 2 OF 2 | (Listing) | AC-A938A-MC | 9 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-A940A-MC | | | | | |
| | | VDZC??.BI? | 26,27 | DZV11 Cable and Echo Test | (Listing) | AC-A941A-MC | 9 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-A943A-MC | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VDZD??.BI? | | DZV11 Overlay for ITEP | (Listing)<br>(Binary PT) | AC-A935A-MC<br>AK-A937A-MC | 9 | 15 | 18 | 19 | 20 |
| | | XDZB??.OBJ | | DEC/X11 DZV11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E911C-MC<br>AK-E912C-MC | 5 | 14 | 18 | 19 | 20 |
| M8012 | BDV11-AA | VM8A??.BI? | 28,29,<br>30 | BDV11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-B061C-MC<br>AK-B063C-MC | 8 | 13 | 18 | 19 | 20 |
| | | XBMD??.OBJ | | DEC/X11 LSI-11 BDV11 Exerciser | (Listing)<br>(Binary PT) | AC-F060C-MC<br>AK-F061C-MC | 1 | 14 | 18 | 19 | 20 |
| M8013/<br>M8014 | RLV11 | VRLA??.BI? | | RLV11 RL01 Diskless Test | (Listing)<br>(Binary PT) | AC-B107B-MC<br>AK-B109B-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLG??.BI? | 7,31 | RL11/RLV11 Controller Test 1 | (Listing)<br>(Binary PT) | AC-F111B-MC<br>AK-F108B-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLH??.BI? | 7,32,<br>33 | RL11/RLV11 Controller Test 2 | (Listing)<br>(Binary PT) | AC-F115B-MC<br>AK-F112B-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLI??.BI? | 7,34,<br>35 | RL01/02 Drive Test 1 | (Listing)<br>(Binary PT) | AC-F119C-MC<br>AK-F116C-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLJ??.BI? | 7,36 | RL01/02 Drive Test 2 | (Listing)<br>(Binary PT) | AC-F123B-MC<br>AK-F120B-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLK??.BI? | 7,35,<br>37 | RL01/02 Performance Exerciser | (Listing)<br>(Binary PT) | AC-F127B-MC<br>AK-F124B-MC | 10 | 17 | 18 | 19 | 20 |
| | | ZRLL??.BI? | 7,35 | RL01/02 Drive Compatibility Test | (Listing)<br>(Binary PT) | AC-F131B-MC<br>AK-F128B-MC | 11 | 17 | 18 | 19 | 20 |
| | | ZRLM??.BI? | 7,35,<br>38 | RL01/02 Bad Sector File Tool | (Listing)<br>(Binary PT) | AC-F135B-MC<br>AK-F132B-MC | 11 | 17 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ZRLN??.BI? | 7,39, 40 | RL01/02 Drive Test 3 | (Listing)<br>(Binary PT) | AC-F843A-MC<br>AK-F844-MC | 11 | 17 | 18 | 19 | 20 |
| | | XRLA??.OBJ | 7 | RL11/RLV11/RL01/RL02 Exerciser | (Listing)<br>(Binary PT) | AC-E965D-MC<br>AK-E966D-MC | 6 | 16 | 18 | 19 | 20 |
| M8016 | KPV11-X | VKPA??.BI? | 41,42, 43 | KPV11-A Diagnostic | (Listing)<br>(Binary PT) | AC-A883A-MC<br>AK-A885A-MC | 8 | 13 | 18 | 19 | 20 |
| M8017 | DLV11-E | VDVA??.BI? | 11b | DLV11-E Off-Line Test | (Listing)<br>(Binary PT) | AC-B150B-MC<br>AK-B152B-MC | 8 | 13 | 18 | 19 | 20 |
| | | XDLA??.OBJ | 11b | DEC/X11 DL11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E709J-MC<br>AK-E710J-MC | 5 | 14 | 18 | 19 | 20 |
| M8018 | KUV11-AA | VKUA??.BI? | 44 | KUV11-AA (LSI WCS) Diagnostic | (Listing)<br>(Binary PT) | AC-E102A-MC<br>AK-E104A-MC | 4 | 13 | 18 | 19 | 20 |
| | | XKUA??.OBJ | 45 | DEC/X11 KUV11-AA Exerciser Module | (Listing)<br>(Binary PT) | AC-E992B-MC<br>AK-E993B-MC | 5 | 14 | 18 | 19 | 20 |
| M8020 | DPV11-XX | VDPV??.BI?<br>XDPV??.OBJ | | DPV11 Functional Diagnostic<br>DPV11 Module | | AC-S039?-M? | 4 | 13 | 18 | 19 | 20 |
| M8021 | MRV11-BA | VMRA??.BI? | | LSI-11 UVPROM-RAM (MRV11-BA) Test | (Listing)<br>(Binary PT) | AC-B153A-MC<br>AK-B155A-MC | 8 | 15 | 18 | 19 | 20 |
| | | ZKMA??.BI? | 4a,46 | MOS/Core 0-124K Exerciser | (Listing)<br>(Binary PT) | AC-8850F-MC<br>AK-8854F-MC | 4 | 13 | 18 | 19 | 20 |
| | | ZQMC??.BI? | 4b,46 | 0-124 K Memory Exerciser (16K) | (Listing)<br>(Binary PT) | AC-9045F-MC<br>AK-9048F-MC | 12 | 13 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M8027 | LPV11 | ZLAE??.BI? | | LA180 Printer Diagnostic | (Listing)<br>(Binary PT) | AC-8906B-MC<br>AK-8908B-MC | 7 | 13 | 18 | 19 | 20 |
| | | XLPA??.OBJ | | DEC/X11 LP11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E670F-MC<br>AK-E671F-MC | 6 | 14 | 18 | 19 | 20 |
| M8028 | DLV11-F | VDVC??.BI? | 11a | DLV11-F Off-Line Test | (Listing)<br>(Binary PT) | AC-E0068-MC<br>AK-E008B-MC | 8 | 13 | 18 | 19 | 20 |
| | | XDLA??.OBJ | 11a | DEC/X11 DL11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E709J-MC<br>AK-E710J-MC | 5 | 14 | 18 | 19 | 20 |
| M8029 | RXV21 | ZRXC??.BI? | 7 | RX02 Utility Driver | (Listing)<br>(Binary PT) | AC-E509A-MC<br>AK-E511A-MC | 3 | 13 | 18 | 19 | 20 |
| | | ZRXD??.BI? | 7 | RX02 SS Performance Exerciser | (Listing)<br>(Binary PT) | AC-E512B-MC<br>AK-E514B-MC | 3 | 13 | 18 | 19 | 20 |
| | | ZRXE??.BI? | 7 | RX02 Formatter Program | (Listing)<br>(Binary PT) | AC-E622A-M2<br>AK-E624A-M2 | 2 | 13 | 18 | 19 | 20 |
| | | ZRXF??.BI? | 7 | RX02 FCTN/Log | (Listing)<br>(Binary PT) | AC-E625A-MC<br>AK-E627A-M1 | 3 | 13 | 18 | 19 | 20 |
| | | XRXB??.OBJ | 7 | DEC/X11 RX02 Exerciser Module | (Listing)<br>(Binary PT) | AC-F098C-MC<br>AK-F100C-MC | 6 | 16 | 18 | 19 | 20 |
| M8043 | DLV11-J | VDLA??.BI? | 47,48 | DLV11-J Test | (Listing)<br>(Binary PT) | AC-E188B-MC<br>AK-E190B-MC | 8 | 15 | 18 | 19 | 20 |
| | | XDLA??.OBJ | 48 | DEC/X11 DL11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E709J-MC<br>AK-E710J-MC | 5 | 14 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M8044/ M8045 | MSV11-DX/ MSV11-EX | ZKMA??.BI? | 4a | MOS/Core 0-124K Exerciser | (Listing) | AC-8850F-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8854F-MC | | | | | |
| | | ZQMC??.BI? | 4b | 0-124K Memory Exerciser (16K) | (Listing) | AC-9045F-MC | 12 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9048F-MC | | | | | |
| M8047 | MXV11-AX | VMXA??.BI? | 48 | MXV11-AX Diagnostic | (Listing) | AC-E656A-MC | 12 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E658A-MC | | | | | |
| | | ZKMA??.BI? | 4a | MOS/Core 0-124K Exerciser | (Listing) | AC-8850F-MC | 4 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-8854F-MC | | | | | |
| | | ZQMC??.BI? | 4b | 0-124K Memory Exerciser (16K) | (Listing) | AC-9045F-MC | 12 | 13 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-9048F-MC | | | | | |
| | | XDLA??.OBJ | 48 | DEC/X11 DL11 Exerciser Module | (Listing) | AC-E709J-MC | 5 | 14 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-E710J-MC | | | | | |
| M8048 | MRV11-C | NA | | | | | | | | | |
| M8049 | DRV11-J | VDRC??.BI? | 49 | DRV11-J Diagnostic Test Part 1 | (Listing) | AC-F756A-M1 | 8 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-F757A-M1 | | | | | |
| | | VDRD??.BI? | 49 | DRV11-J Diagnostic Test Part 2 | (Listing) | AC-F759A-MC | 8 | 15 | 18 | 19 | 20 |
| | | | | | (Binary PT) | AK-F760A-MC | | | | | |
| M8053 | DMV11 | VDMA??.BI | | DMV11 MCTRL Diagnostic No. 1 | | | | | | | |
| | | VDMB??.BI | | DMV11 MCTRL Diagnostic No. 2 | | | | | | | |
| | | VDMC??.BI | | DMV11 Line Unit Diagnostic No. 1 | | | | | | | |
| | | VDMD??.BI | | DMV11 Line Unit Diagnostic No. 2 | | | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | VDME??.BI | | DMV11 Line Unit Diagnostic No. 3 | | | | | | |
| | | XDMD??.OBJ | | DEC/X11 DM11 Exerciser | AC-F805?-M? | | | | | |
| | | XDMF??.OBJ | | DEC/X11 DM11 Exerciser | AC-F807?-M? | | | | | |
| M8059 | MSV11-L | VMSA??.BI | | Memory Exerciser | AC-S435A-MC<br>AK-S436A-MC | | | | | |
| | | ZKMA??.BI | | MOS 0-124K Exerciser | AC-8850F-MC<br>AK-8854F-MC | | | | | |
| M8061 | RLV12 | VRLB??.BI | | Diskless Diagnostic | | | | | | |
| | | ZRLG??.BI | | Controller Test Part 1 | | | | | | |
| | | ZRLH??.BI | | Controller Test Part 2 | | | | | | |
| | | ZRLI??.BI | | Drive Test Part 1 | | | | | | |
| | | ZRLJ??.BI | | Drive Test Part 2 | | | | | | |
| | | ZRLN??.BI | | Drive Test Part 3 | | | | | | |
| | | ZRLK??.BI | | Performance Exerciser | | | | | | |
| | | ZRLL??.BI | | Compatibility Test | | | | | | |
| | | ZRLM??.BI | | Bad Sector File | | | | | | |
| M8063 | KXT11-AA | NKXAA | | KXT11-AA Exerciser | | | | | | |
| M8064 | (See M8053) | | | | | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M8067 | MSV11-P | VMSA??.BI | | Memory Exerciser | | AC-S435A-MC<br>AK-S436A-MC | | | | | |
| | | ZKMA??.BI | | MOS 0-124K Exerciser | | AC-8850F-MC<br>AK-8854F-MC | | | | | |
| M8186 | KDF11-A | JKDA??.BI? | 50 | KTF11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-F138C-MC<br>AK-F136C-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDB??.BI? | | DCF11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-F141C-M1<br>AK-F139C-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDC??.BI? | | KEF11-AA Diagnostic No. 1 | (Listing)<br>(Binary PT) | AC-F241B-MC<br>AK-F240B-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDD??.BI? | 51 | KEF11-AA Diagnostic No. 2 | (Listing)<br>(Binary PT) | AC-F244B-MC<br>AK-F243B-MC | 9 | 13 | 18 | 19 | 20 |
| | | XCPA??.OBJ | | DEC/X11 Processor Test Module | (Listing)<br>(Binary PT) | AC-E664G-MC<br>AK-E665G-MC | 1 | 14 | 18 | 19 | 20 |
| | | XCPB??.OBJ | | DEC/X11 EIS Exerciser Module | (Listing)<br>(Binary PT) | AC-E667J-MC<br>AK-E668J-MC | 1 | 14 | 18 | 19 | 20 |
| | | XFPA??.OBJ | | DEC/X11 FP11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E742G-MC<br>AK-E743G-MC | 5 | 14 | 18 | 19 | 20 |
| M8188 | FPF11 | JFPA??.BI | | FLT PNT Diagnostic No. 1 | | AC-F405C-MC<br>AH-F406C-MC | | | | | |
| | | JFPB??.BI | | FLT PNT Diagnostic No. 2 | | AC-S442A-MC<br>AK-S443A-MC | | | | | |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M8189 | KDF11-BA | JKDA??.BI? | 50 | KTF11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-F138C-MC<br>AK-F136C-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDB??.BI? | | DCF11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-F141C-M1<br>AK-F139C-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDC??.BI? | | KEF11-AA Diagnostic No. 1 | (Listing)<br>(Binary PT) | AC-F241B-MC<br>AK-F240B-MC | 9 | 13 | 18 | 19 | 20 |
| | | JKDD??.BI? | 51 | KEF11-AA Diagnostic No. 2 | (Listing)<br>(Binary PT) | AC-F244B-MC<br>AK-F243B-MC | 9 | 13 | 18 | 19 | 20 |
| | | XCPA??.OBJ | | DEC/X11 Processor Test Module | (Listing)<br>(Binary PT) | AC-E664G-MC<br>AK-E665G-MC | 1 | 14 | 18 | 19 | 20 |
| | | XCPB??.OBJ | | DEC/X11 EIS Exerciser Module | (Listing)<br>(Binary PT) | AC-E667J-MC<br>AK-E668J-MC | 1 | 14 | 18 | 19 | 20 |
| | | XFPA??.OBJ | | DEC/X11 FP11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E742G-MC<br>AK-E743G-MC | 5 | 14 | 18 | 19 | 20 |
| | | VM8A??.BI | 28,29,30 | BDV11-AA Diagnostic | (Listing)<br>(Binary PT) | AC-B061C-MC<br>AK-B063C-MC | 8 | 13 | 18 | 19 | 20 |
| M8631 | MCV11 | VMSA??.BI | | Memory Exerciser | | AC-S435A-MC<br>AK-S436A-MC | | | | | |
| M9400/<br>M9401 | REV11-X/<br>TEV11/<br>BCV1X | ZM9A??.BI? | | Bootstrap/Terminator Test | (Listing)<br>(Binary PT) | AC-8954E-MC<br>AK-8957E-MC | 7 | 13 | 18 | 19 | 20 |
| | | XBMC??.OBJ | | DEC/X11 Bootstrap/Terminator | (Listing)<br>(Binary PT) | AC-F057N-MC<br>AK-F058N-MC | 1 | 14 | 18 | 19 | 20 |

| Module Number | Option Name | Diagnostic and DEC/X11 File Names | Notes | Diagnostic and DEC/X11 Module Titles | | Listing and Paper Tape PNs | RX01 | RX02 | RK05 | RL01 | RL02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A012 | ADV11-A | VADA??.BI? | 1 | ADV11 Performance Test | (Listing)<br>(Binary PT)<br>(DOC/<br>PT Kit) | AC-8174C-MC<br>AK-8176C-MC<br>ZJ250-RB | 8 | 13 | 18 | 19 | 20 |
| | | XADC??.OBJ | 2,3 | DEC/X11 ADV11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E923B-MC<br>AK-E924B-MC | 1 | 14 | 18 | 19 | 20 |
| A0026 | AXV11-C | VAXA??.BI | | AXV11 Diagnostic Test | | | | | | | |
| A6001 | AAV11-A | VAAA??.BI? | | AAV11 Diagnostic Test | (Listing)<br>(Binary PT)<br>(DOC/PT<br>KIT) | AC-8169A-MC<br>AK-8172A-MC<br>ZJ248-RB | 8 | 15 | 18 | 19 | 20 |
| | | XAAC??.OBJ | | DEC/X11 AAV11 Exerciser Module | (Listing)<br>(Binary PT) | AC-E917B-MC<br>AK-E918B-MC | 1 | 14 | 18 | 19 | 20 |
| A6006 | AAV11-C | VAAA??.BI | | AAV11-C Diagnostic Test | | | | | | | |
| A8000 | ADV11-C | VAXA??.BI | | ADV11-C Diagnostic Test | | | | | | | |
| G653/<br>H223 | MMV11-A | ZKMA??.BI? | 4a | MOS/Core 0-124K Exerciser | (Listing)<br>(Binary PT) | AC-8850F-MC<br>AK8854F-MC | 4 | 13 | 18 | 19 | 20 |
| | | ZQMC??.BI? | 4b | 0-124K Memory Exerciser (16K) | (Listing)<br>(Binary PT) | AC-9045F-MC<br>AK-9048G-MC | 12 | 13 | 18 | 19 | 20 |

**Notes**

1. Wraparound test and auto-tests require Berg test connector 70-12894-00.

2. Requires an analog ground on any channel to be tested.

3. May be run asynchronously if KWV11 is present in system. If run asynchronously, XKWE??.OBJ must be deselected from the DEC/X11 run.

4a. Memory space under test should be contiguous and read/write. For systems having noncontiguous memory, the memory boundaries must be defined by the operator before running the program. This diagnostic requires 8K of memory space to run in.

4b. This test will run successfully only on an 11/23 processor with a minimum of 16K of memory.

5. LTC must be disabled.

6. VKAA??.BI? and VKAD??.BI? should be run on the CPU prior to running this test.

7. Scratch media must be mounted in drives to be tested before starting the diagnostic.

8. ZRKJ??.BI?, ZRKK??.BI?, ZRKL??.BI?, and ZRKI??.BI? (if needed) should be run on subsystem before running this test.

9. ZRKJ??.BI? should be run on the sybsystem before running this test.

10. ZRKJ??.BI? and ZRKK??.BI? should be run on the subsystem before running this test.

11a. A wraparound test connector must be installed to run this test. The connector is not available from stock. The F.E. must make one up himself. The following instructions (excerpted from Tech Tip PDP-11/03 TT-11) tell how this is done. The following items are required:

| | |
|---|---|
| 1 Berg connector | (12-10918-15) |
| 4 Berg pins | (12-10089-07) |
| #22 wire | (90-07350-00). |

Crimp a short length of wire between two Berg pins. Make up two sets of these. Install one set from pin F to pin J, and one set from pin E to pin M of the Berg connector.

11b. To completely exercise the modem control portion of the DLV11-E, a special wraparound connector (H315) must be installed on the modem end of the I/F cable. This test connector loops back certain control lines as well as the data lines.

12. The test has baud rate dependent configuration requirements.

| Baud Rate | No. of Stop Bits | No. of Bits |
|---|---|---|
| 110 | 2 | 8 |
| All others | 1 | 8 |

13. Requires BC08R test cable for full test of module's data lines.

14. ZRXB??.BI? should be run on the subsystem before running this test.

15. If a REV11 is in the system, DMA refresh must be disabled and CPU refresh must be enabled.

16. H315A connector required for external loopback testing.

17. If customer hardware is connected to the KWV11 which could inject signals on ST1, ST2 or slave in inputs, it must be disconnected from the inputs.

18. All switches in switch pack 2 should be left off unless you are instructed otherwise.

19. I/O signal test no. 1 (ST1 in, ST2 out); install a jumper between J1-SS (ST2 out) to J1-VV (ST1 in).

**Switch Pack 2**

| Switch | State |
|---|---|
| 1 | Off |
| 2 | On |
| 3 | Off |
| 4 | Off |
| 5 | On |
| 6 | On |
| 7 | Not used. |

Use a program starting address of 210.

20. I/O signal test no. 2 (clock overflow tests); install a jumper between J1-RR (clock overflow) to J1-TT (ST2 in).

**Switch Pack 2**

| Switch | State |
|---|---|
| 1 | Off |
| 2 | Off |
| 3 | Off |
| 4 | On |
| 5 | Off |
| 6 | On |
| 7 | Not used. |

Use a program starting address of 214.

21. I/O signal test no. 3 (ST1 out, ST2 in); install a jumper between J1-UU (ST1 out) to J1-TT (ST2 in).

**Switch Pack 2**

| Switch | State |
|---|---|
| 1 | Off |
| 2 | Off |
| 3 | Off |
| 4 | On |
| 5 | On |
| 6 | On |
| 7 | Not used. |

Use a program starting address of 220.

22. Test may be run with a "known good module" in the system for comparison. The good module should be located second (electrically) on the bus, with a cable connecting it and the module under test.

"known good module" address - 760160
"known good module" vector - 660

23. Starting restrictions:

If a free-running clock, such as 60 Hz from the power supply, is attached to the BEVNT bus line on REV C/D/E systems, an interrupt to location 100 will occur when using the ODT "G" and "L" commands. This will happen prior to the program executing the first instruction. This program cannot disable the BEVNT bus line by inhibiting interrupts.

User systems requiring a free-running clock attached to the BEVNT bus line can temporarily avoid this situation by setting the PSW to 200, loading the PC with the starting address, and then using the "P" command, instead of using the starting address and the "G" command.

Before using the "L" command, the PSW can be set to 200 to inhibit interrupts after loading the absolute loader.

24. Possible program bombs:

The first two tests check to see if the IBV11-A responds to the address the program thinks it is at. If not, a bus error occurs.

Bus errors may alter the preset contents of location 4 before the trap is executed. Program control may be transferred to an area of the program which is not set up to handle the trap. Or, control may be passed to some totally unknown and irrelevant piece of code residing accidently in memory. If this occurs, the program will most probably bomb, and it may also overwrite parts of itself. If this occurs, the program must be reloaded before proceeding.

25. If the IB-bus cable is not removed from the module under test, any errors which are detected could be from some device out on the IB-bus and not necessarily from the IBV11-A.

26. If run in staggered maintenance mode, an H329 staggered turnaround connector is required.

27. If run in external maintenance mode, an H325 cable turn-around connector is required on all lines which have been selected to be tested.

28. This test assumes that the module under test resides in the same backplane where the line time clock is generated.

29. Test 3 assumes that switch no. 5 of E21 is in the ON position.

30. For the rocker switch test, the operator should specify the configuration for the module under test.

31. VRLA??.BI? should be run on the subsystem before running this test.

32. VRLA??.BI? and ZRLG??.BI? should be run on the subsystem before running this test.

33. A KWV11 programmable line clock is required to run test no. 7.

34. VRLA??.BI?, ZRLG??.BI?, and ZRLH??.BI? should be run on the subsystem before running this test.

35. A KWV11 programmable line clock is required for some tests.

36. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, and ZRLI??.BI? should be run on the subsystem before running this test.

37. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, ZRLJ??.BI?, and ZRLN??.BI? should be run on the subsystem before running this test.

38. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, ZRLJ??.BI?, ZRLK??.BI, and ZRLN??.BI? should be run on the subsystem before running this test.

39. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, and ZRLJ??.BI? should be run on the subsystem before running this test.

40. A KWV11 programmable line clock is required for tests 1 and 4.

41. To check the power fail circuitry, nonvolatile memory must be in the first 4K of memory.

42. Power up option no. 1 should be selected on the CPU module for power fail testing.

43. The module should be in the standard factory configuration.

    jumpers in: W1-W5, W7, W8, W11, W13-W15
    jumpers out: W6, W9, W10, W12

44. If the test is to be run in all address modes, then an extender card and a special test cable (17-00124-01) are required.

45. The exerciser may be run with the module in address modes 1 or 3 only.

46. This test may be run only if RAM is present on the board.

47. All channels must be configured to the same bit-word length.

48. A wraparound connector (H3270) is required for the data wraparound tests for each of the lines to be tested.

49. Requires a BC05W-02 cable to be installed between the Berg connectors. The cable should have a half twist in it.

50. JKDB??.BI? should be run on the first 16K of memory before running this test.

51. JKDC??.BI? should be run on the module before running this test.

## Media Availability

| No. | Media Package Identifier | Title | Notes | Media PNs | Documentation Media Kit PNs |
|---|---|---|---|---|---|
| 1 | CZZGG?? | DXDP+ 7 DEC/X11 EXEC 1 | 1 | AS-9645?-M? | ZJ271-RY |
| 2 | CZZGL?? | DXDP+ 12 RC,RF,RK11 | | AS-9650?-M? | |
| 3 | CZZGO?? | DXDP+ 15 RX11 DIAG | | AS-9653?-M? | |
| 4 | CZZGY?? | DXDP+ 25 LSI FLP 1 | 1 | AS-9663?-M? | ZJ271-RY |
| 5 | CZZGZ?? | DXDP+ 26 DEC/X11 EXEC 2 | 1 | AS-9664?-M? | ZJ271-RY |
| 6 | CZZHD?? | DXDP+ 30 DEC/X11 EXEC 3 | 1 | AS-9668?-M? | ZJ271-RY |
| 7 | CZZHE?? | DXDP+ 31 LSI FLP 2 | 1 | AS-9669?-M? | ZJ271-RY |
| 8 | CZZHG?? | DXDP+ 33 LSI FLP 3 | 1 | AS-9671?-M? | ZJ271-RY |
| 9 | CZZHQ?? | DXDP+ 43 LSI FLP 4 | 1 | AS-C638?-M? | ZJ271-RY |
| 10 | CZZHZ?? | DXDP+ 52 RL02 DIAG no. 1 | 1 | AS-F547?-M? | ZJ271-RY |
| 11 | CZZID?? | DXDP+ 56 RL02 DIAG no. 2 | 1 | AS-F753?-M? | ZJ271-RY |
| 12 | CZZIH?? | DXDP+ 60 LSI FLP 5 | 1 | AS-F804?-M? | ZJ271-RY |
| 13 | CZZMC?? | DYDP+ 3 LSI-11 no. 1 | 2 | BA-F021?-M? | ZJ271-RX |
| 14 | CZZMD?? | DYDP+ 4 DEC/X11 no. 1 | 2 | BA-F022?-M? | ZJ271-RX |
| 15 | CZZMT?? | DYDP+ 20 LSI-11 no. 2 | 2 | BA-F048?-M? | ZJ271-RX |
| 16 | CZZMU?? | DYDP+ 21 DEC/X11 no. 2 | 2 | BA-F049?-M? | ZJ271-RX |
| 17 | CZZMZ?? | DYDP+ 26 LSI-11 no. 3 | 2 | BA-F558?-M? | ZJ271-RX |
| 18 | CZZZD?? | LSI-11 DKDP + Diagnostic PKG | | AN-9696?-M? | ZJ278-RE |
| 19 | CZZLA?? | DLDP+ (RL01) Diagnostic PKG no. 1 | | AX-E380?-M? | ZJ278-RQ |
| 20 | CZZLN?? | DLDP+ (RL02) Diagnostic PKG | | BC-F916?-M? | ZJ278-RH |

**Notes**

1. Documentation/media kit ZJ271-RY contains all of these floppies as well as all of the applicable documentation.
2. Documentation/media kit ZJ271-RX contains all of these floppies as well as all of the applicable documentation.

# APPENDIX B
# FLOATING ADDRESSES / VECTORS

## FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus are the same as UNIBUS devices. UNIBUS devices are used to explain the ranking sequence.

The floating-address convention used for communications and for other devices that interface with the PDP-11 series of products assigns addresses sequentially starting at 760 010 (or 160 010) and proceeds upward to 763 776 (or 163 776). For the sake of compatibility with UNIBUS conventions, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (1XX XXX).

Floating addresses are assigned in the following sequence.

| Rank | UNIBUS Device | LSI-11 Device |
|---|---|---|
| 1 | DJ11 | |
| 2 | DH11 | |
| 3 | DQ11 | |
| 4 | DU11 | DUV11 |
| 5 | DUP11 | |
| 6 | LK11A | |
| 7 | DMC11 | |
| 8 | DZ11 | DZV11 |
| 9 | KMC11 | |
| 10 | RL11 (extras) | RLV11 (extras) |

## FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for UNIBUS devices. UNIBUS devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide for the user.

The floating-vector convention used for communications and for devices that interface with the PDP-11 series of products assigns vectors sequentially starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector limit of 377.) The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned to all the DLV11s (up to a maximum of 32); addresses are then assigned consecutively to each unit of the next highest-ranked device (DRV11 or DLV11-E, and so forth), then to the other devices according to their rank.

**Ranking for Floating Vectors**
**(Start at 300 and proceed upward.)**

| Rank | UNIBUS | LSI-11 Bus |
|---|---|---|
| 1 | DC11 | |
| 2 | KL11, DL11-A, -B | DLV11, -F, -J |
| 3 | DP11 | |
| 4 | DM11-A | |
| 5 | DN11 | |
| 6 | DM11-BB | |
| 7 | DR11-A | DRV11-B |
| 8 | DR11-C | DRV11 |
| 9 | PA611 Reader | |
| 10 | PA611 Punch | |
| 11 | DT11 | |
| 12 | DX11 | |
| 13 | DL11-C, -D, -E | DLV11-E |
| 14 | DJ11 | |
| 15 | DH11 | |
| 16 | GT40 | |
| 17 | LPS11 | |
| 18 | DQ11 | |
| 19 | KW11-W | KWV11 |
| 20 | DU11 | DUV11 |

# APPENDIX C
# LSI-11 BUS SPECIFICATION

## GENERAL

**NOTE**

**This is not the complete LSI-11 bus specification, but is included to permit users to design and implement typical interfaces to the LSI-11 bus.**

The processor, memory, and I/O devices communicate via 38 bidirectional signal lines that constitute the LSI-11 bus. Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are functionally divided as follows:

18 Data/address lines – BDAL<17:00>
6 Data transfer control lines – BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT
3 Direct memory access control lines – BDMG, BDMR, BSACK
6 Interrupt control lines – BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7
5 System control lines – BDCOK, BHALT, BINIT, BPOK, BREF

Most LSI-11 bus signals are bidirectional and use terminations for a negated (high) signal level. Devices connect to these lines via high-impedance bus receivers and open collector drivers. The asserted state is produced when a bus driver asserts the line low. Although bidirectional lines are electrically bidirectional (any point along the line can be driven or received), certain lines are functionally unidirectional. These lines communicate to or from a bus master (or signal source), but not both. Interrupt acknowledge (BIACK) and direct memory access grant (BDMG) signals are physically unidirectional in a daisy-chain fashion. These signals start at the processor output signal pins. Each is received on device input pins (BIAKI or BDMGI) and conditionally retransmitted via device output pins (BIAKI or BDMGI) and conditionally retransmitted via device output pins (BIAKO or BDMGO). These signals are received from higher priority devices and are retransmitted to lower priority devices along the bus.

**Master/Slave Relationship**

Communication between devices on the bus is asynchronous. A master/slave relationship exists throughout each bus transaction. At any time, there is one device that has control of the bus. This controlling device is called the "bus master." The master device controls the bus when communicating with another device on the bus, called the slave. The bus master (typically the processor or a DMA device) initiates a bus transaction. The slave device responds by acknowledging the transaction in progress and by receiving data from, or transmitting data to, the bus master. LSI-11 bus control signals transmitted or received by the bus master or bus slave device must complete the sequence according to bus protocol.

The processor controls bus arbitration (i.e., who becomes bus master at any given time). A typical example of this relationship is the processor, as master, fetching an instruction from memory (which is always a slave). Another example is a disk, as master, transferring data to memory as slave. Theoretically, any device can be master or slave, depending on the circumstances. Communication on the LSI-11 bus is interlocked so that for each control signal issued by the master device, there must be a response from the slave in order to complete the transfer. It is this master/slave signal protocol that makes the LSI-11 bus asynchronous. The asynchronous operation precludes the need for synchronizing with clock pulses.

Since bus cycle completion by the bus master requires response from the slave device, each bus master must include a timeout error circuit that will abort the bus cycle if the slave device does not respond to the bus transaction within 10 microseconds.

The actual time before a timeout error occurs must be longer than the reply time of the slowest peripheral or memory device on the bus.

The signals and pin assignments are tabulated as shown below. The pin nomenclature is for reference and is only required when examining DIGITAL modules and circuit schematics. A functional description of the LSI-11 bus pins and signals is also found below.

## Categories of LSI-11 Bus Signal Lines

| Number of Pins | Functional Category | DIGITAL's Nomenclature (Name) (Pin) | | | | | |
|---|---|---|---|---|---|---|---|
| 18 | Data/Address | BDAL0, AU2 | BDAL1, AV2 | BDAL2, BE2 | BDAL15, BV2 | BDAL16, AC1 | BDAL17, AD1 |
| 6 | Data Control | BDOUT, AE2 | BRPLY, AF2 | BDIN, AH2 | BSYNC, AJ2 | BWTBT, AK2 | BBS7, AP2 |
| 6 | Interrupt Control | BIRQ7, BP1 | BIRQ6, AB1 | BIRQ5, AA1 | BIRQ4, AL2 | BIAKO, AN2 | BIAKI, AM2 |
| 4 | DMA Control | BDMR, AN1 | BDMGO, AS2 | BDMGI, AR2 | BSACK, BN1 | | |
| 6 | System Control | BHALT, AP1 | BREF, AR1 | BDCOK, BA1 | BPOK, BB1 | BEVNT, BR1 | BINIT, AT2 |
| 3 | +5 Vdc | AA2, BA2, BV1 | | | | | |
| 2 | +12 Vdc | AD2, BD2 | | | | | |
| 2 | −12 Vdc | AB2, BB2 | | | | | |
| 2 | +12 B* | AS1, BS1 | | | | | |
| 1 | +5 B* | AV1, (AE1, AS1 alternates) | | | | | |
| 8 | GND | AC2, AJ1, AM1, AT1, BC2, BJ1, BM1, BT1 | | | | | |
| 8 | S SPARES | AE1, AAF1, AH1, BC1, BD1, BE1, BF1, BH1 | | | | | |
| 4 | M SPARES | AK1 – AL1, BK1 – BL1 (pairs connected) | | | | | |
| 2 | PSPARES | AU1, BU1 | | | | | |

* Battery

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| AA1 | BIRQ5 L | Interrupt request priority level 5 |
| AB1 | BIRQ6 L | Interrupt request priority level 6 |
| AC1 | BDAL16 L | Address line 16 during addressing protocol; memory error line during data transfer protocol. |
| AD1 | BDAL17 L | Address line 17 during addressing protocol; memory error enable during data transfer protocol. |
| AE1 | SSPARE1 (alternate +5 B) | Special spare – not assigned or based in DIGITAL cable or backplane assemblies; available for user connection. Optionally, this pin may be used for +5 V battery (+5 B) backup power to keep critical circuits alive during power failures. A jumper is required on LSI-11 bus options to open (disconnect) the +5 B circuit in systems that use this line as SSPARE1. |
| AF1 | SSPARE2 | Special spare – not assigned or bused in DIGITAL cable or backplane assemblies; available for user interconnection. In the highest priority device slot, the processor may use this pin for a signal to indicate its RUN state. |
| AH1 | SSPARE3 SRUN | Special spare – not assigned nor bused in DIGITAL cable or backplane assemblies; available for user interconnection. |
| AJ1 | GND | Ground – System signal ground and dc return. |
| AK1 AL1 | MSPAREA MSPAREB | Maintenance Spare – Normally connected together on the backplane at each option location (not bused connection). |
| AM1 | GND | Ground – System signal ground and dc return. |

**Functional Descriptions (Cont)**

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| AN1 | BDMRL | Direct memory access (DMA) request – device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The devices responds by negating BDMR L and asserting BSACK L. |
| AP1 | BHALT L | Processor halt – When BHALT L is asserted, the processor responds by going into console ODT mode. |
| AR1 | BREF L | Memory refresh – used to refresh dynamic memory devices. The LSI-11 processor microcode features automatic refresh control. BREF L is asserted during this time to override memory bank selection decoding. Interrupt requests and BBS7 are blocked out during this time. |
| AS1 | +5 B or +12 B (battery) | +12 or +5 Vdc battery backup power to keep critical circuits alive during power failures. This signal is not bused to BS1 in all DIGITAL backplanes. A jumper is required on all LSI-11 bus options to open (disconnect) the backup circuit from the bus in systems that use this line at the alternate voltage. |
| AT1 | GND | Ground – system signal ground and dc return. |
| AU1 | PSPARE1 | Power spare 11 (not assigned a function; not recommended for use) – If a module is using –12 V (on BB2) and if the module is accidentally inserted backward in all the backplane, –12 Vdc appears on pin AU1. |
| AV1 | +5 B | +5 V battery power – secondary +5 V power connection. Battery power can be used with certain devices. |

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| BA1 | BDCOK H | DC power OK – Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation. |
| BB1 | BPOK H | AC power OK – Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated. |
| BC1<br>BD1<br>BE1<br>BF1<br>BH1 | SSPARE 4<br>SSPARE 5<br>SSPARE 6<br>SSPARE 7<br>SSPARE 8 | Special spares – not assigned or bused in DIGITAL's cable and backplane assemblies; available for user interconnections. **Caution**. These pins may be used as test points by DIGITAL in some options. |
| BJ1 | GND | Ground – system signal ground and dc return. |
| BK1<br>BL1 | MSPAREB<br>MSPAREB | Maintenance spares – Normally connected together on the backplane at each option location (not a bused connection). |
| BM1 | GND | Ground – system signal ground and dc return. |
| BN1 | BSACK L | This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master. |
| BP1 | BIRQ7 L | Interrupt request priority level 7 |
| BR1 | BEVNT L | External event interrupt request – When the processor latches the leading edge and arbitrates as a level 6 interrupt. A typical use of this signal is a line time clock interrupt. |
| BS1 | +12 B | +12 Vdc battery backup power (not bused to AS1 in all DIGITAL backplanes) |
| BT1 | GND | Ground – system signal ground and dc return. |
| BU1 | PSPARE2 | Power spare 2 (not assigned a function, not recommended for use) – If a module is using –12 V (on pin AB2) and if the module is accidentally inserted backwards in the backplane, –12 Vdc appears on pin BU1. |

**Functional Descriptions (Cont)**

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| BV1 | +5 | +5 V power – Normal +5 Vdc system power |
| AA2 | +5 | +5 V power – Normal +5 Vdc system power |
| AB2 | –12 | –12 V Power – –12 Vdc (optional) power for devices requiring this voltage. |
| AC2 | GND | Ground – system signal ground and dc return |
| AD2 | +12 | +12 V Power – +12 Vdc system power |
| AE2 | BDOUT L | Data Output – BDOUT, when asserted, implies that valid data is available on BDAL <0:15> L and that an output transfer, with respect to the bus master device is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer. |
| AF2 | BRPLY L | Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus. |
| AH2 | BDIN L | Data Input – BDIN L is used for two types of bus operation:<br>1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device.<br>2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring.<br>The master device must deskew input data from BRPLY L. |

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| AJ2 | BSYNC L | Synchronize – BSYNC L is asserted by the bus master device to indicate that it has placed an address on the bus. The transfer is in process until BSYNC L is negated. |
| AK2 | BWTBT L | Write/Byte – BWTBT L is used in two ways to control a bus cycle:<br>1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence.<br>2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing. |
| AL2 | BIRQ4 L | Interrupt request priority level 4 |
| AM2<br>AN2 | BIAKI L<br>BIAKO L | Interrupt acknowledge – In accordance with interrupt protocol, the processor asserts BIAKO L to acknowledge the honoring of an interrupt. The bus transmits this to BIAKI L of the next priority device (electrically closest to the processor). This device accepts the interrupt acknowledge under two conditions:<br>1. The device requested the bus by asserting an interrupt, and<br>2. The device has the highest priority interrupt request on the bus at that time.<br>If these conditions are not met, the device asserts BIAKO L to the next device on the bus. This process continues in a daisy-chain fashion until the device with the highest interrupt priority receives the interrupt acknowledge (IAK) signal. |
| AP2 | BBS7 L | Bank 7 select – The bus master asserts this signal to reference the I/O page (including that portion of the I/O page reserved for nonexistent memory). The address in BDAL<0:12> L when BBS7 L is asserted is the address within the I/O page. |

**Functional Descriptions (Cont)**

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| AR2<br>AS2 | BDMGI L<br>BDMGO L | Direct memory access grant – The bus arbitrator asserts this signal to grant bus mastership to a requesting device, according to bus mastership protocol. The signal is passed in a daisy-chain from the arbitrator (as BDMGO L) through the bus to BDMGI L of the next priority device (electrically closest device on the bus). This device accepts the grant only if it requested to be bus master (by a BDMR L). If not, the device passes the grant (asserts BDMGO L) to the next device on the bus. This process continues until the requesting device acknowledges the grant. |
| AT2 | BINIT L | Initialize – This signal is used for system reset. All devices on the bus are to return to a known, initial state; i.e., registers are reset to zero, and logic is reset to state 0. Exceptions should be completely documented in programming and engineering specifications for the device. |
| AU2 | BDAL0 L | Data/address line 00. |
| AV2 | BDAL1 L | Data/address line 01. |
| BA2 | +5 | +5 Vdc power. |
| BB2 | −12 | −12 Vdc power (optional, not required for DIGITAL LSI-11 hardware options). |
| BC2 | GND | Power supply return. |
| BD2 | +12 | +12 Vdc power. |
| BE2 | BDAL2 L | Data/address line 02. |
| BF2 | BDAL3 L | Data/address line 03. |
| BH2 | BDAL4 L | Data/address line 04. |
| BJ2 | BDAL5 L | Data/address line 05. |

| Bus Pin | Signal Mnemonic | Signal Function |
|---|---|---|
| BK2 | BDAL6 L | Data/address line 06. |
| BL2 | BDAL7 L | Data/address line 07. |
| BM2 | BDAL8 L | Data/address line 08. |
| BN2 | BDAL9 L | Data/address line 09. |
| BP2 | BDAL10 L | Data/address line 10. |
| BR2 | BDAL11 L | Data/address line 11. |
| BS2 | BDAL12 L | Data/address line 12. |
| BT2 | BDAL13 L | Data/address line 13. |
| BU2 | BDAL14 L | Data/address line 14. |
| BV2 | BDAL15 L | Data/address line 15. |

## DATA TRANSFER BUS CYCLES

Data transfer bus cycles are as follows:

| Bus Cycle Mnemonic | Description | Function (with respect to the bus master) |
|---|---|---|
| DATI | Data word input | Read |
| DATO | Data word output | Write |
| DATOB | Data byte output | Write byte |
| DATIO | Data word input/output | Read-modify-write |
| DATIOB | Data byte input/byte output | Read-modify-write byte |

These bus cycles, executed by bus master devices, transfer 16-bit words or 8-bit bytes to or from slave devices. The following bus signals are used in a data transfer operation.

| Mnemonic | Description | Function |
|---|---|---|
| BDAL<17:00> L | 18 Data/address lines | BDAL<15:00> L are used for word and byte transfers. BDAL<17:16> L are used for extended addressing, memory parity error, and memory parity error enable functions. |
| BSYNC L | Synchronize | Strobe signals |
| BDIN L | Data input strobe | |
| BDOUT L | Data output strobe | |
| BRPLY L | Reply | |
| BWTBT L | Write/byte control | Control signals |
| BBS7 L | Bank select 7 | |

Data transfer bus cycles can be reduced to three basic types: DATI, DATOB and DATIOB. These transactions occur between the bus master and one slave device selected during the addressing portion to the bus cycle.

### Bus Cycle Protocol

Before initiating a bus cycle, the previous bus transaction must have been completed (BSYNC L negated) and the device must become bus master. The bus cycle can be divided into two parts, an addressing portion and a data transfer portion. During the addressing portion, the bus master outputs the address for the desired slave device (memory or device register). The selected slave device responds by latching the address bits and holding this condition for the duration of the bus cycle (until BSYNC L becomes negated). During the data transfer portion, the actual data transfer occurs.

**Device Addressing**

The device addressing portion of a data transfer bus cycle comprises an address setup and deskew time and an address hold/deskew time. During the address setup and deskew time, the bus master does the following:

Asserts BDAL<17:00> L with the desired slave device address bits

Asserts BBS7 L if a device in the I/O page is being addressed

Asserts BWTBT L if the cycle is a DATO(B) bus cycle

Asserts BSYNC at least 150 ns after BDAL<17:00> L, BBS7 L, and BWTBT L are valid.

During this time the address, BBS7 L, and BWTBT L signals are asserted at the slave bus receiver for at least 75 ns before BSYNC goes active. Devices in the I/O page ignore the five high-order address bits BDAL<17:13> and instead decode BBS7 along with the 13 low-order address bits. An active BWTBT L signal indicates that a DATO(B) operation follows, while an inactive BWTBT L indicates a DATI or DATIO(B) operation.

The address hold/deskew time begins after BSYNC L is asserted. The master must hold the address at BDAL at least 100 ns after the assertion of BSYNC.

The slave device uses the active BSYNC L bus receiver output to clock BDAL address bits, BBS7 L and BWTBT L, into its internal logic. BWTBT L, BBS7 L, and BDAL<17:00>L will remain active for a minimum of 25 ns after the BSYNC L bus receiver goes active. BSYNC L remains active for the duration of the bus cycle.

Device selected logic must be reset at the end of the current bus cycle. The device should not wait until the next BSYNC L signal to reset the device selected logic.

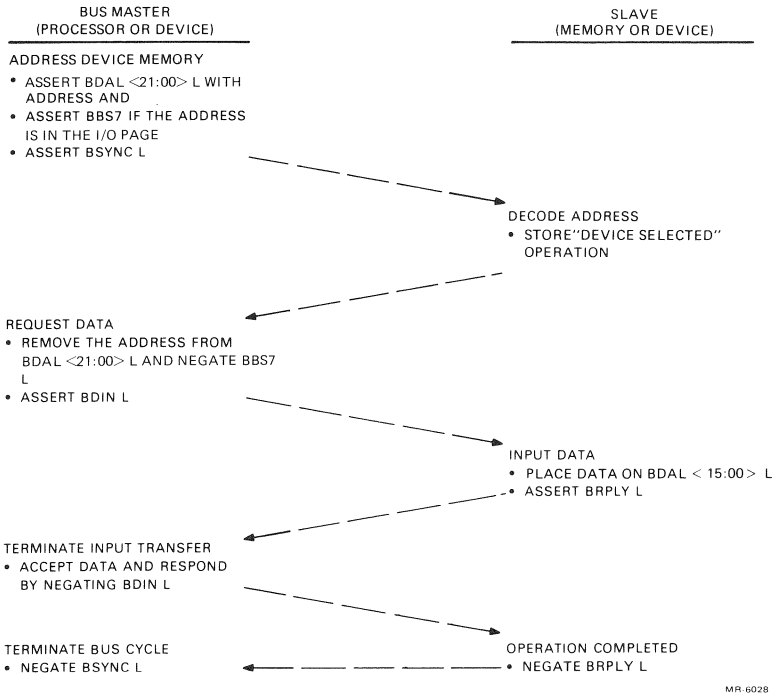
Memory and peripheral devices are addressed similarly, except for the way the slave device responds to BBS7. Addressed peripheral devices must not decode address bits on BDAL<17:13> L. Addressed peripheral devices may respond to a bus cycle only when BBS7 is asserted (low) during the addressing portion of the cycle. When asserted, BBS7 L indicates that the device address resides in the I/O page (the upper 4K address space). Memory devices generally do not respond to addresses in the I/O page; however, some system applications may permit memory to reside in the I/O page for use as DMA buffers, read-only-memory bootstraps or diagnostics, etc.

**DATI**

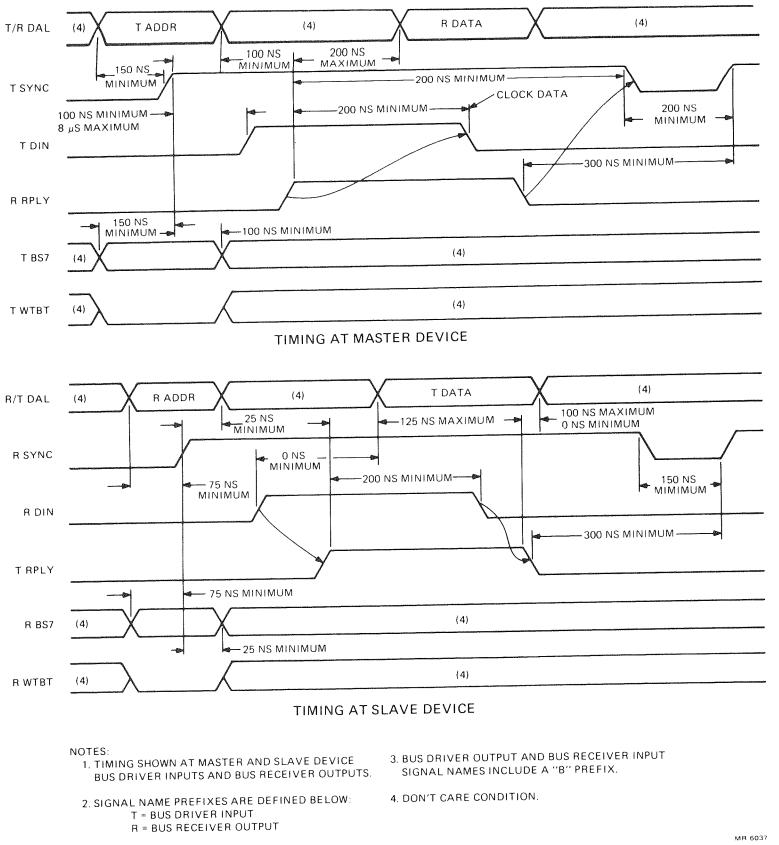
The DATI bus cycle is a read operation. During DATI, data is input to the bus master. Data consists of 16-bit word transfers over the bus. During the data transfer portion of the DATI bus cycle, the bus master asserts BDIN L, 100 ns minimum, 8 ns maximum, after BSYNC L is asserted. The slave device responds to BDIN L active in the following ways:

Asserts BRPLY L after receiving BDIN L and 125 ns (maximum) before BDAL bus driver data bits are valid

Asserts BDAL<17:00> L with the addressed data and error information.




DATI Bus Cycle




DATI Bus Cycle Timing

When the bus master receives BRPLY L, it does the following:

Waits at least 200 ns deskew time and then accepts input data at BDAL<17:00>L bus receivers. BDAL<17:16>L are used for transmitting parity errors to the master.

Negates BDIN L no less than 150 ns and no more than 2 microseconds after BRPLY L goes active.

The slave device responds to BDIN L negation by negating BRPLY L and removing read data from BDAL bus drivers. BRPLY L must be negated no more than 100 ns prior to removal of read data. The bus master responds to the negated BRPLY L by negating BSYNC L.

Conditions for the next BSYNC L assertion are as follows:

BSYNC L must remain negated for 200 ns (minimum)

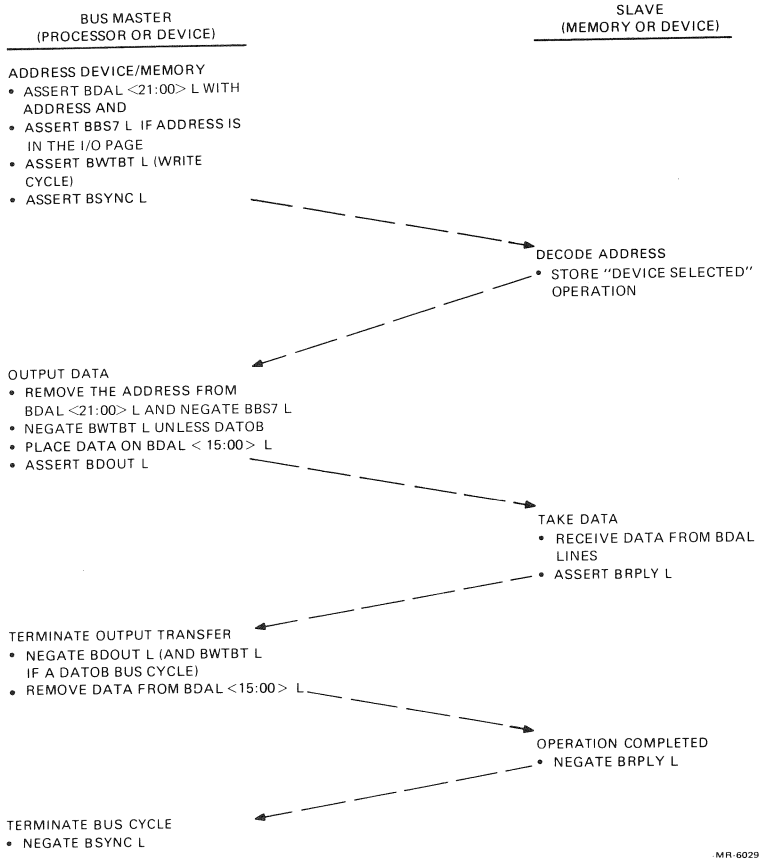
BSYNC L must not become asserted within 300 ns of previous BRPLY L negation.

**NOTE**

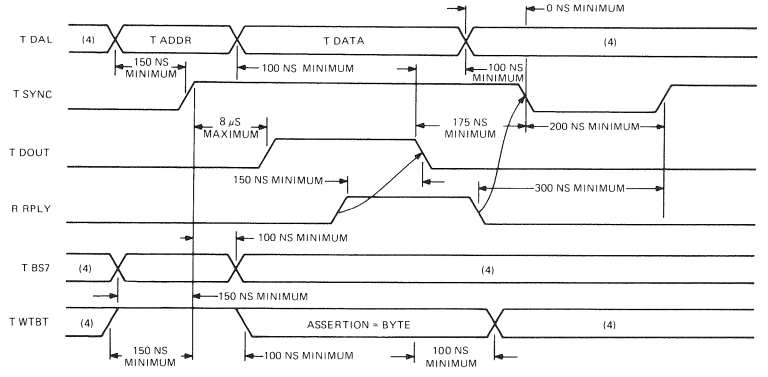
**Continuous assertion of BSYNC L retains ccontrol of the bus by the bus master, and the previously addressed slave device remains selected. This is done for DATIO(B) bus cycles where DATO or DATOB follows a DATI without BSYNC L negation and a second device addressing operation. Also, a slow slave device can hold off data transfers to itself by keeping BRPLY L asserted, which will cause the master to keep BSYNC L asserted. Exceeding 15 $\mu$sec hold time will cause loss of memory if bus refresh is being used.**

## DATOB

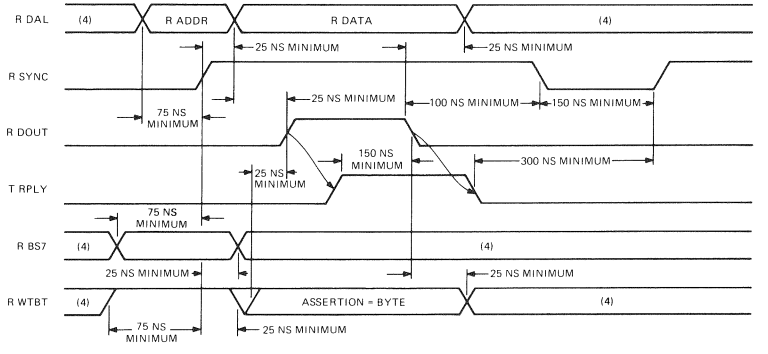
DATOB is a write operation. Data is transferred in 16-bit words (DATO) or 8-bit bytes (DATOB) from the bus master to the slave device. The data transfer output can occur after the addressing portion of a bus cycle when BWTBT L had been asserted by the bus master, or immediately following an input transfer part of a DATIOB bus cycle.




DATO or DATOB Bus Cycle




TIMING AT MASTER DEVICE




TIMING AT SLAVE DEVICE

NOTES:
1. TIMING SHOWN AT MASTER AND SLAVE DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS.
2. SIGNAL NAME PREFIXES ARE DEFINED BELOW:
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT
3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX.
4. DON'T CARE CONDITION.

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DATO or DATOB Bus Cycle Timing

The data transfer portion of a DATOB bus cycle comprises a data set-up and deskew time and a data hold and deskew time.

During the data set-up and deskew time, the bus master outputs the data on BDAL<16:00> L at least 100 ns after BSYNC L is asserted. If it is a word transfer, the bus master negates BWTBT L at least 100 ns after BSYNC L assertion and BWTBT L remains negated for the length of the bus cycle. If the transfer is a byte transfer, BWTBT L remains asserted. If it is the output of a DATIOB, BWTB L becomes asserted and lasts the duration of the bus cycle. During a byte transfer,

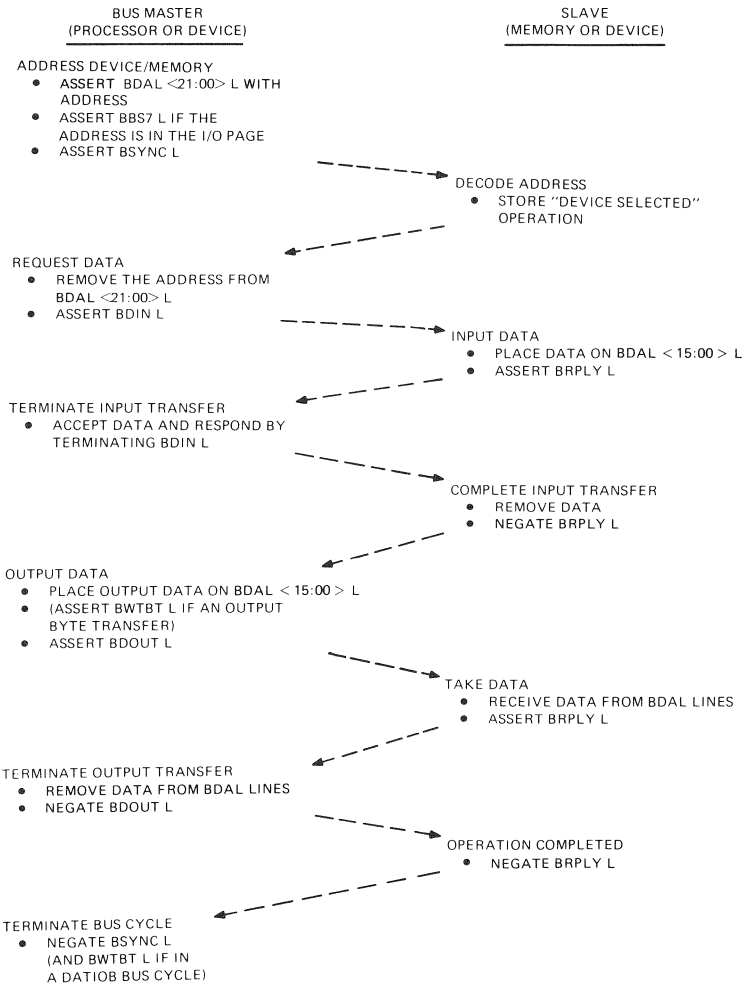
BDAL 00 L selects the high or low byte. This occurs while in the addressing portion of the cycle. If asserted, the high byte (BDAL<15:08> L) is selected; otherwise, the low byte (BDAL<07:00> L) is selected. An asserted BDAL 16 L at this time will force a parity error to be written into memory if the memory is a parity-type memory. BDAL 17 L is not used for write operations. The bus master asserts BDOUT L between 100 ns and 8 usec after BDAL and BWTBT L bus drivers are stable. The slave device responds by asserting BRPLY L within 10 microseconds to avoid bus timeout. This completes the data setup and deskew time.

During the data hold and deskew time, the bus master receives BRPLY L and negates BDOUT L. BDOUT L must remain asserted for at least 150 ns from the receipt of BRPLY L before being negated by the bus master. BDAL<16:00> L bus drivers remain asserted for at least 100 ns after BDOUT L negation. The bus master then negates BDAL inputs.

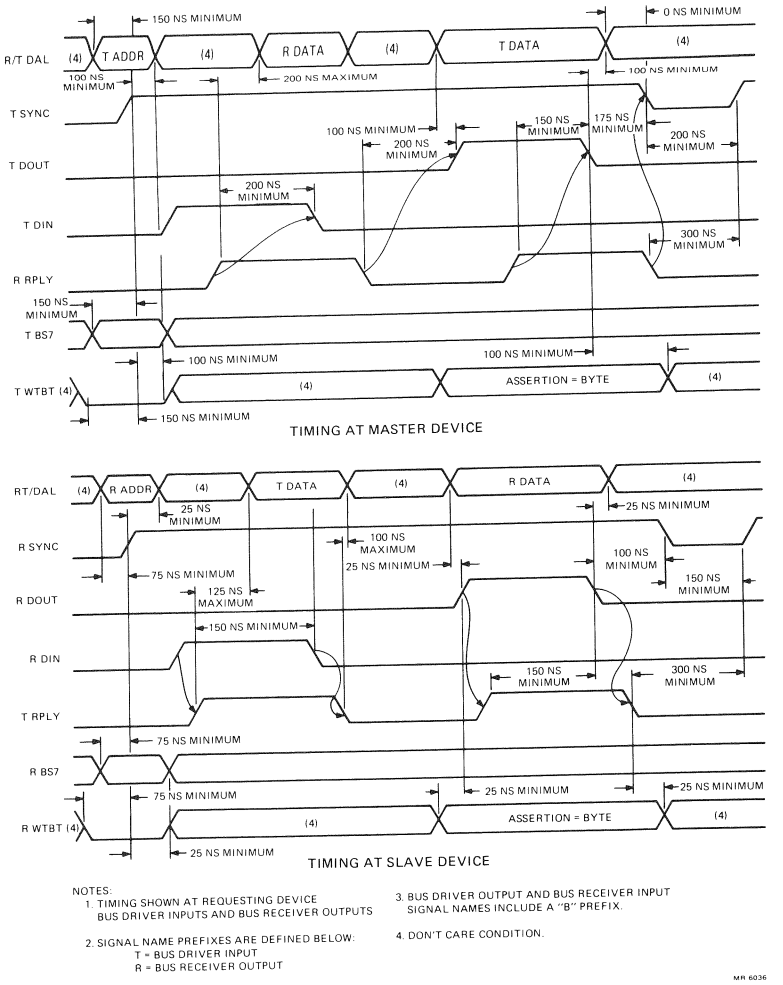
During this time, the slave device senses BDOUT L negation. The data is accepted and the slave device negates BRPLY L. The bus master responds by negating BSYNC L. However, the processor will not negate BSYNC L for at least 175 ns after negating BDOUT L. This completes the DATOB bus cycle. Before the next cycle BSYNC L must remain unasserted for at least 200 ns.

**DATIOB**

The protocol for a DATIOB bus cycle is identical to the addressing and data transfer portions of the DATI and DATOB bus cycles. After addressing the device, a DATI cycle is performed as explained above; however, BSYNC L is not negated. BSYNC L remains active for an output word or byte transfer (DATOB). The bus master maintains at least 200 ns between BRPLY L negation during the DATI cycle and BDOUT L assertion. The cycle is terminated when the bus master negates BSYNC L, which is the same as described for DATOB.




DATIO or DATIOB Bus Cycle




DATIO or DATIOB Bus Cycle Timing

**Parity Protocol**

The KDF11-AA recognizes memory parity errors and traps to location $114_8$ if one occurs. A parity error detection occurs during every DATI or DATI portion of a DATIOB cycle. The processor samples BDAL 16 L and BDAL 17 L after the 200 ns REPLY deskew time similar to BDAL <15:00> L. BDAL 16 L is interpreted as a parity error signal from memory and BDAL 17 L is interpreted as a parity error enable signal from an external parity controller module. BDAL 17 L is used by

software to enable parity detection which is done by addressing a parity status register on the LSI-11 bus. Parity status register hardware then asserts BDAL 17 L during the BDIN L portion of DATI cycles to inform the processor or bus master that detection is enabled. BDAL 16 L is used to indicate a parity error and is asserted by the selected memory at REPLY time. Upon system power-up, memory may contain random data and erroneous parity error signals may be used (BDAL 16 L asserted). Until known data is written into memory, software keeps BDAL 17 L negated, to avoid false traps. After known data and correct parity have been written into memory, software can enable parity detection in the parity status register. If both BDAL 16 L and BDAL 17 L are asserted at REPLY time, an abort and trap to location $114_8$ will occur. The assertion of BDAL 16 L during BDOUT L will cause memory to write wrong parity as a diagnostic tool for maintenance purposes.

**Direct Memory Access**

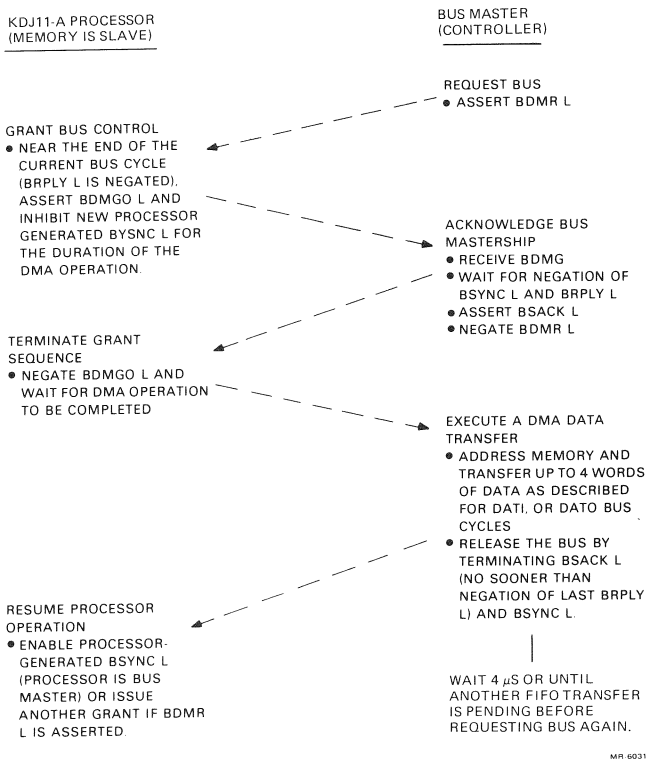
The direct memory access (DMA) capability allows direct data transfers between I/O devices and memory. This is useful when using mass storage devices (e.g., disks) that move large blocks of data to and from memory. A DMA device only needs to know the starting address in memory, the starting address in mass storage, the length of the transfer, and whether the operation is read or write. When this information is available, the DMA device can transfer data directly to (or from) memory. Since most DMA devices must perform data transfers in rapid succession or lose data, DMA devices are provided the highest priority.

DMA is accomplished after the processor (normally the bus master) has passed bus mastership to the highest priority DMA device that is requesting the bus. The processor arbitrates all requests and grants the bus to the DMA device located electrically closest to the processor. A DMA device remains bus master indefinitely until it relinquishes its mastership. The following control signals are used during bus arbitration:

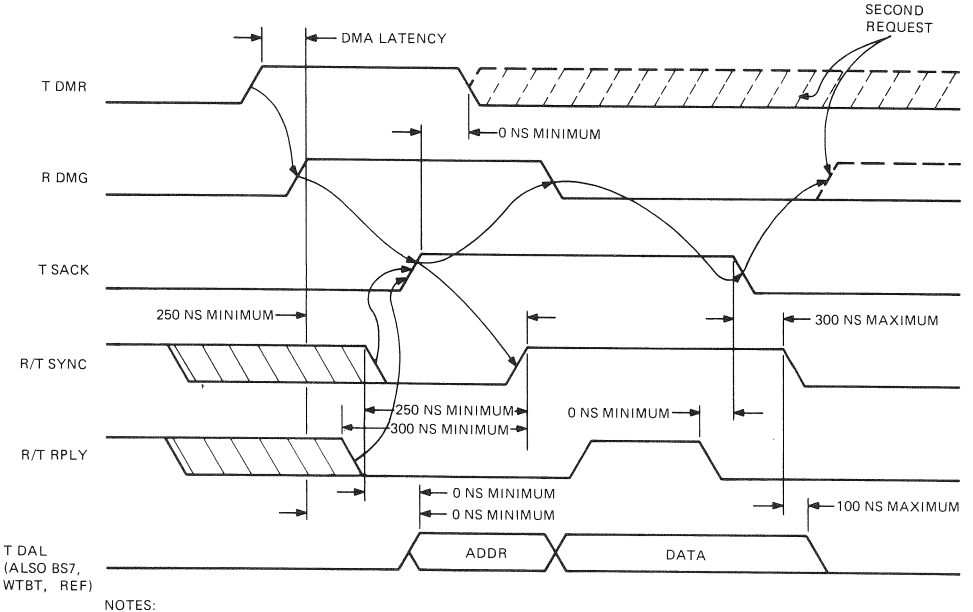
| | |
|---|---|
| BDMGI L | DMA Grant Input |
| BDMGO L | DMA Grant Output |
| BDMR L | DMA Request Line |
| BSACK L | Bus Grant Acknowledge |

## DMA PROTOCOL

A DMA transaction can be divided into three phases: the bus mastership acquisition phase, the data transfer phase, and the bus mastership relinquish phase.




DMA Request/Grant Sequence




NOTES:

1. TIMING SHOWN AT REQUESTING DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS.

2. SIGNAL NAME PREFIXES ARE DEFINED BELOW:
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT

3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX.

**DMA Request/Grant Timing**

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During the bus mastership acquisition phase, a DMA device requests the bus by asserting BDMR L. The processor arbitrates the request and initiates the transfer of bus mastership by asserting BDMGO L. The maximum time between BDMR L assertion and BDMGO L assertion is DMA latency. This time is processor-dependent. BDMGO L/BDMGI L is one signal that is daisy-chained through each module in the backplane. It is driven out of the processor on the BDMGO L pin, enters each module on the BDMGI L pin, and exits on the BDMGO L pin. Propagation delay from BDMGI L to BDMGO L must be less than 500 ns per LSI-11 bus slot. Since this delay directly affects system performance, it should be kept as short as possible. This signal passes through the modules in descending order of priority until it is stopped by the requesting device. The requesting device blocks the output of BMDGO L and asserts BSACK L if BRPLY L and BSYNC L are negated. Propagation delay from BDMGI L to BSACK L must be less than 500 ns.

During the data transfer phase, the DMA device continues asserting BSACK L. The actual data transfer is performed as described in the sections on DATI, DATO, and DATIO.

**NOTE**

**If multiple-data transfers are performed during this phase, consideration must be given to the use of the bus for other system functions, such as memory refresh (if required).**

The DMA device can assert BSYNC L for a data transfer no less than 250 ns after it receives BDMGI L and its BSYNC L and BRPLY L become negated.

During the bus mastership relinquish phase the DMA device relinquishes the bus by negating BSACK L. This occurs after completing (or aborting) the last data transfer cycle (BRPLY L negated). BSACK L may be negated no more than 300 ns before negating BSYNC L.

## INTERRUPTS

The interrupt capability of the LSI-11 bus allows any I/O device to temporarily suspend (interrupt) current program execution and divert processor operation to service the requesting device. The processor inputs a vector from the device to start the service routine (handler). Like the device register address, hardware fixes the device vector at locations within a designated range (below location 001000). The vector is used as the first of a pair of contiguous addresses. The content of the first address is read by the processor and is the starting address of the interrupt handler. The content of the second address is a new processor status word (PS). The new PS can raise the interrupt priority level, thereby preventing lower level interrupts from breaking into the current interrupt service routine. Control is returned to the interrupt program when the interrupt handler is ended. The original (interrupted) program's address (PC) and its associated PS are stored on a stack. The original PC and PS are restored by a return from interrupt (RTI or RTT) instruction at the end of the handler. The use of the stack and the LSI-11 bus interrupt scheme can allow interrupts to occur within interrupts (nested interrupts), depending on the PS.

Interrupts can be caused by LSI-11 bus options. Interrupt operations can also originate from within the processor. These interrupts are called traps. Traps are caused by programming errors, hardware errors, special instructions, and maintenance features.

The LSI-11 bus signals that are used in interrupt transactions are as follows:

| | |
|---|---|
| BIRQ4 L | Interrupt request priority level 4 |
| BIRQ5 L | Interrupt request priority level 5 |
| BIRQ6 L | Interrupt request priority level 6 |
| BIRQ7 L | Interrupt request priority level 7 |
| BIAKI L | Interrupt acknowledge input |
| BIAKO L | Interrupt acknowledge output |
| BDAL<15:00> L | Data/address lines |
| BDIN L | Data input strobe |
| BRPLY L | Reply |

There are two classes of LSI-11 CPUs. One, the 11/03 CPU class, treats all interrupts as level 4. The other, the 11/23 CPU class, can distinguish between the four interrupt levels.

### Device Priority

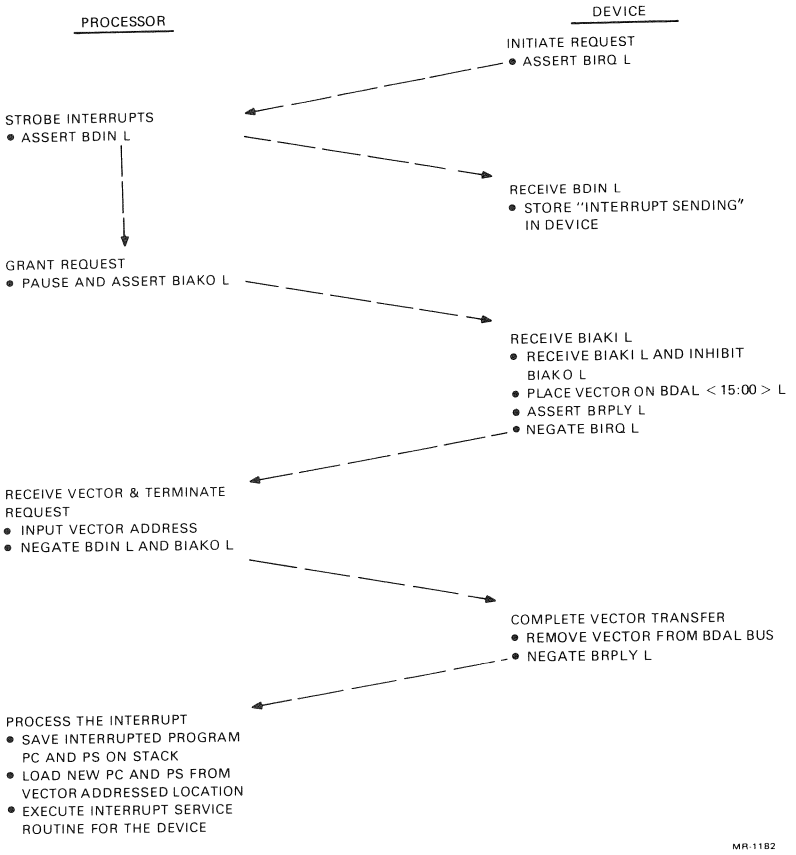
The LSI-11 bus supports the following two methods of device priority:

Distribution arbitration – Priority arbitration is implemented in logic on the interrupting device based on request priority information on the bus. When devices of equal priority level request an interrupt, priority is given to the device electrically closest to the processor.

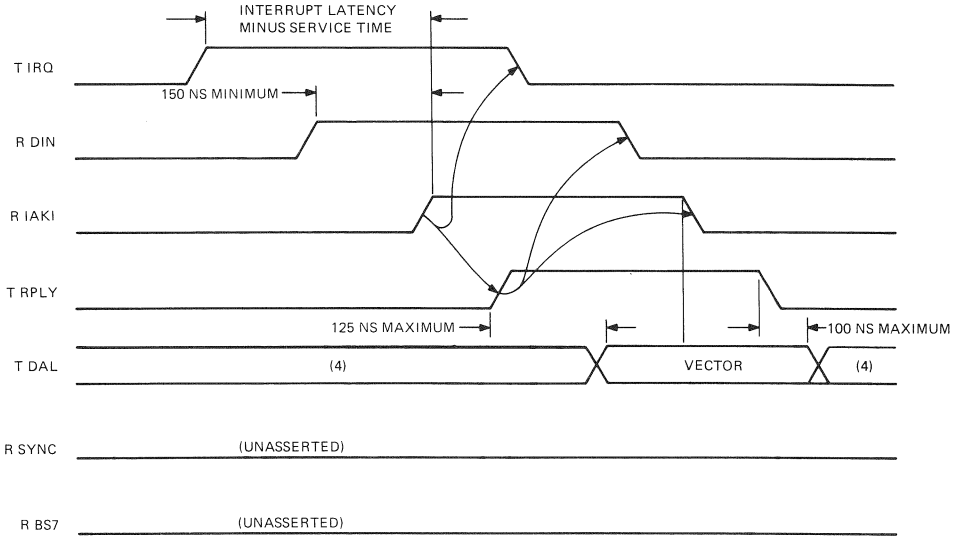
Position-defined arbitration – Priority is determined solely by electrical position on the bus. The closer a device is to the processor, the higher its priority is.

**Interrupt Protocol**

Interrupt protocol has three phases: interrupt request phase, interrupt acknowledge and priority arbitration phase, and interrupt vector transfer phase.




Interrupt Request/Acknowledge Sequence




NOTES:

1. TIMING SHOWN AT REQUESTING DEVICE BUS DRIVER INPUTS AND BUS RECEIVER OUTPUTS.

2. SIGNAL NAME PREFIXES ARE DEFINED BELOW:
   T = BUS DRIVER INPUT
   R = BUS RECEIVER OUTPUT

3. BUS DRIVER OUTPUT AND BUS RECEIVER INPUT SIGNAL NAMES INCLUDE A "B" PREFIX.

4. DON'T CARE CONDITION.

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Interrupt Protocol Timing

The interrupt request phase begins when a device meets its specific conditions for interrupt requests. For example, the device is ready, done, or an error has occurred. The interrupt enable bit in a device status register must be set. The device then initiates the interrupt by asserting the interrupt request line(s). BIRQ4 L is the lowest hardware priority level and is asserted for all interrupt requests for compatibility with previous LSI-11 processors. The level a device is configured at must also be asserted. A special case exists for level 7 devices which must also assert level 6. See item 2 of the arbitration discussion involving the 4-level scheme (below) for an explanation.

| Interrupt Level | Lines Asserted by Device |
|---|---|
| 4 | BIRQ4 L |
| 5 | BIRQ4 L, BIRQ5 L |
| 6 | BIRQ4 L, BIRQ6 L |
| 7 | BIRQ4 L, BIRQ6 L, BIRQ7 L |

The interrupt request line remains asserted until the request is acknowledged.

During the interrupt acknowledge and priority arbitration phase the processor will acknowledge interrupts under the following conditions:

On the 11/03 class processors, the PS bit 7 is cleared. On 11/23 class processors, the device interrupt priority is higher than the PS<07:05>

The processor has completed instruction execution and no additional bus cycles are pending.

The processor acknowledges the interrupt request by asserting BDIN L, and no less than 225 ns later asserting BIAKO L. The device electrically closest to the processor receives the acknowledge on its BIAKI L bus receiver.

At this point, the two types of arbitration must be discussed separately. If the device that receives the acknowledge uses the 4-level (distributed) interrupt scheme, it reacts as described below:

1. If not requesting an interrupt, the device asserts BIAKO L and the acknowledge propagates to the next device on the bus.

2. If the device is requesting an interrupt it must check to see that no higher level device is currently requesting an interrupt. This is done by monitoring higher level request lines. The table below lists the lines that need to be monitored by devices at each priority level.

3. In addition to asserting levels 4 and 7, level 7 devices must drive level 6. This is done to simplify the monitoring and arbitration by level 4 and 5 devices. In

this protocol, level 4 and 5 devices need not monitor level 7, since level 7 devices assert level 6. Level 4 and 5 devices will become aware of a level 7 request since they monitor the level 6 request.

| Device Priority Level | Line(s) Monitored |
|---|---|
| 4 | BIRQ5, BIRQ6 |
| 5 | BIRQ6 |
| 6 | BIRQ7 |
| 7 | – |

4. If no higher level device is requesting an interrupt, the acknowledge is blocked by the device (BIAKO L is not asserted). Arbitration logic within the device uses the leading edge of BDIN L to clock a flip-flop that blocks BIAKO L. Arbitration is won and the interrupt vector transfer phase begins.

5. If a higher level request line is active, the device disqualifies itself and asserts BIAKO L to propagate the acknowledge to the next device along the bus.

Signal timing must be carefully considered when implementing 4-level interrupts. Refer to the previous figure for interrupt protocol timing.

If a single-level interrupt (position defined) device receives the acknowledge, it reacts as follows:

1. If not requesting an interrupt, the device asserts BIAKO L and the acknowledge propagates to the next device on the bus.

2. If the device was requesting an interrupt, the acknowledge is blocked using the leading edge of BDIN L and arbitration is won. The interrupt vector transfer phase begins.

The interrupt vector transfer phase is enabled by BDIN L and BIAKI L. The device responds by asserting BRPLY L and its BDAL<15:00> L bus driver inputs with the vector address bits. The BDAL bus driver inputs must be stable no more than 125 ns after BRPLY L is asserted. The processor then inputs the vector address and negates BDIN L and BIAKO L. The device then negates BRPLY L and no more than 100 ns later removes the vector address bits. The processor then enters the device's service routine.

**NOTE**

**Propagation delay from BIAKI L to BIAKO L must be no greater than 500 ns per LSI-11 bus slot.**

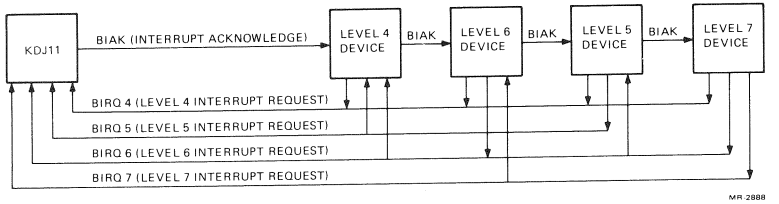
**The device must assert BRPLY L no more than 10 microseconds after BIAKI L is asserted at the input to the module. Since the magnitude of**

**both these times directly affects system performance, they should be kept as short as possible. Typical DIGITAL designs have less than 55 ns propagation delay from BIAKI L to BIAKO L.**

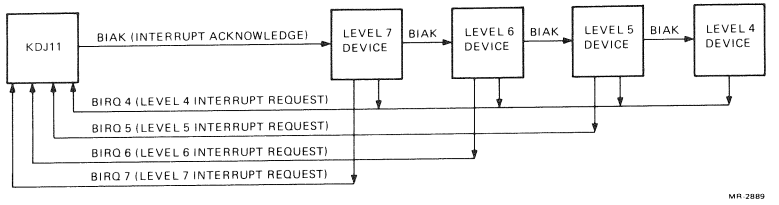
### 4-Level Interrupt Configurations (LSI-11/21)

Users who have high-speed peripherals and desire better software performance can use the 4-level interrupt scheme. Both position-independent and position-dependent configurations can be used with the 4-level interrupt scheme.

The position-independent configuration is shown below. This allows peripheral devices that use the 4-level interrupt scheme to be placed in the backplane in any order. These devices must send out interrupt requests and monitor higher level request lines as described above. The level 4 request is always asserted by a requesting device regardless of priority, to allow compatibility if an LSI-11/2 or LSI-11 processor is in the same system. If two or more devices of equally high priority request an interrupt, the device physically closest to the processor will win arbitration.




Position-Independent Configuration (LSI-11/23)




Position-Dependent Configuration (LSI-11/23)

The position-dependent configuration is shown above. This configuration is simpler to implement. A constraint is that peripheral devices must be inserted with the highest priority device located closest to the processor and the remaining devices placed in the backplane in decreasing order of priority, with the lowest priority devices farthest from the processor. With this configuration, each device only has to assert its own level and level 4 (for compatibility with an LSI-11 or LSI-11/2). Monitoring higher level request lines is unnecessary. Arbitration is achieved through the physical positioning of each device on the bus. Devices which use the position dependent scheme must be placed on the bus behind all position independent devices and in order of decreasing priority.

## CONTROL FUNCTIONS

The following LSI-11 bus signals provide control functions.

| | |
|---|---|
| BREF L | Memory refresh |
| BHALT L | Processor halt |
| BINIT L | Initialize |
| BPOK H | Power OK |
| BDCOK H | DC power OK |

### Memory Refresh

If BREF is asserted during the address portion of a bus data transfer cycle, it causes all dynamic MOS memories to be simultaneously addressed. The sequence of addresses required for refreshing the memories is determined by the specific requirements for each memory. The complete memory refresh cycle consists of a series of refresh bus transactions. A new address is used for each transaction. The effect of multiple data transfers by DMA devices must be carefully considered since they could delay memory refresh cycles.

### Halt

Assertion of BHALT L stops program execution and forces the processor unconditionally into console ODT mode.

### Initialization

Devices along the bus are initialized when BINIT L is asserted. The processor can assert BINIT L as a result of executing a RESET instruction or as part of a power-up sequence. BINIT L is asserted for approximately 10 $\mu$s when RESET is executed.

### Power Status

Power status protocol is controlled by two signals, BPOK H and BDCOK H. These signals are driven by some external device (usually the power supply) and are defined as follows.

### BDCOK H

The assertion of this line indicates that dc power has been stable for at least 3 ms. The negation of this line indicates that only 5 $\mu$s of dc power reserve remains. Once BDCOK H is negated it must remain in this state for at least 1 $\mu$s before being asserted again. BDCOK H may be pulsed low for a minimum of 1 $\mu$s to cause the CPU to restart.

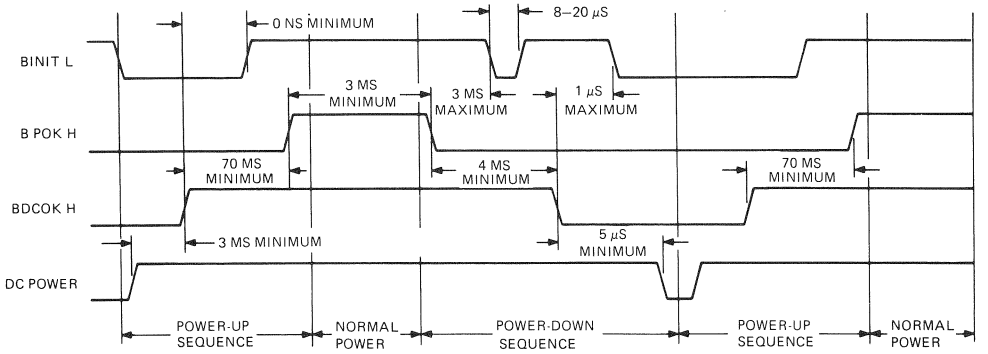
### BPOK H

The assertion of this line indicates that there is at least an 8 ms reserve of dc power and that BDCOK H has been asserted for at least 70 ms. Once BPOK H has been asserted, it must remain asserted for at least 3 ms. The negation of this line indicates that power is failing and that only 4 ms of dc power reserve remains.

## Power-Up/Down Protocol

Power-up protocol begins when the power supply applies power with BDCOK H negated. This forces the processor to assert BINIT L. When the dc voltages are stable, the power supply or other external device asserts BDCOK H. The power supply asserts BPOK H no less than 70 ms after BDCOK H is asserted. The processor then performs its power-up sequence. Normal power must be maintained at least 3 ms before a power-down sequence can begin.

A power-down sequence begins when the power supply negates BPOK H. The current bus master, if not the processor, should relinquish the bus as soon as possible (maximum 1 ms). When the current instruction is completed, the processor traps to a power-down routine. The processor traps to location $24_8$ which contains the PC that points to the power-down routine. The end of the routine is terminated with a HALT instruction to avoid any possible memory corruption as the dc voltages decay. The power fail routine has 4 ms to execute and HALT from the time BPOK L is negated.




NOTE:
ONCE A POWER-DOWN SEQUENCE IS STARTED, IT MUST BE COMPLETED BEFORE A POWER-UP SEQUENCE IS STARTED.

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Power-Up/Power-Down Timing

## BUS ELECTRICAL CHARACTERISTICS

*This section contains information about the electrical characteristics of the LSI-11 bus.*

### AC Load Definition

AC load is a unit of measure of capacitance between a signal line and ground, as specified below. A unit load is defined as 9.35 pF of capacitance.

### DC Load Definition

DC load is a unit of measure of the dc current flowing in a signal line. A unit load is defined as 105 $\mu$A flowing into a device when the signal line is in the high state.

### 120 Ohm LSI-11 Bus

The electrical conductors interconnecting the bus device slots are treated as transmission lines. A uniform transmission line, terminated in its characteristic impedance, will propagate an electrical signal without reflections. Insofar as bus drivers, receivers and wiring connected to the bus have finite resistance and nonzero reactance, the transmission line impedance becomes nonuniform, and thus introduces distortions into pulses propagated along it. Passive components of the LSI-11 bus (such as wiring, cabling and etched signal conductors) are designed to have a nominal characteristic impedance of 120 ohms.

The maximum length of interconnecting cable, excluding wiring within the backplane, is limited to 4.88 m (16 ft).

### Bus Drivers

Devices driving the 120 ohm LSI-11 bus must have open collector outputs and meet the following specifications.

DC Specifications

Output low voltage when sinking 70 mA of current: 0.7 V maximum

Output high leakage current when connected to 3.8 Vdc: 25 $\mu$A (even if no power is applied to them, except for BDCOK H and BPOK H)

These conditions must be met at worst-case supply voltage, temperature, and input signal levels.

AC Specifications

Bus driver output pin capacitive load: Not to exceed 10 pF

Propagation delay: Not to exceed 35 ns

Skew (difference in propagation time between slowest and fastest gate): Not to exceed 25 ns

Rise/Fall Times: Transition time from 10 percent to 90 percent for positive transition, and from 90 percent to 10 percent for negative transition, must be no faster than 10 ns and no slower than 1 $\mu$s.

**Bus Receivers**

Devices that receive signals from the 120 ohm LSI-11 bus must meet the following requirements.

DC Specifications

Input low voltage (maximum): 1.3 V

Input high voltage (minimum): 1.7 V

Maximum input current when connected to 3.8 Vdc: 80 $\mu$A even if no power is applied to them.

These specifications must be met at worst-case supply voltage, temperature, and output signal conditions.

AC Specifications

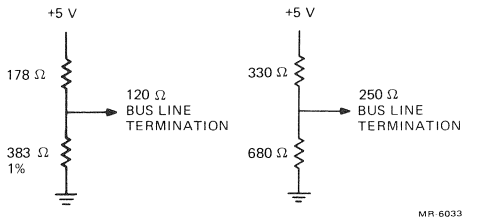
Bus receiver input pin capacitance load: Not to exceed 10 pF

Propagation delay: Not to exceed 35 ns

Skew (difference in propagation time between slowest and fastest gate): Not to exceed 25 ns

**Bus Termination**

The 120 ohm LSI-11 bus must be terminated at each end by an appropriate terminator. This is to be done as a voltage divider with its Thevenin equivalent equal to 120 ohms and 3.4 V nominal. This type of termination is provided by an REV11-A refresh/boot/terminator, or the BDV11-AA.




Bus Line Terminations

Each of the several LSI-11 bus lines (all signals whose mnemonics start with the letter B) must see an equivalent network with the following characteristics at each end of the bus.

Input impedance (with respect to ground): Z = 120 ohm ±10%.
Open circuit voltage: 3.4 Vdc +5%
Capacitance Load: Not to exceed 30 pF

**NOTE**

**The resistive termination may be provided by the combination of two modules (i.e., the processor module supplies 220 ohms to ground). Both of these two terminators must be physically resident within the same backplane.**

**Bus Interconnecting Wiring**
This section contains the electrical characteristics of the bus transmission lines.

**Backplane Wiring**
The wiring that interconnects all device interface slots on the LSI-11 bus must meet the following specifications:

1. The conductors must be arranged such that each line exhibits a characteristic impedance of 120 ohms (measured with respect to the bus common return).

2. Crosstalk between any two lines must be no greater than 5 percent. Note that worst-case crosstalk is manifested by simultaneously driving all but one signal line and measuring the effect on the undriven line.

3. DC resistance of signal path, as measured between near-end terminator and far-end terminator module (including all intervening connectors, cables, backplane wiring, connector-module etch, etc.) must not exceed 2 ohms.

4. DC resistance of common return path, as measured between near-end terminator and far-end terminator module (including all intervening connectors, cables, backplane wiring, connector-module etch, etc.) must not exceed an equivalent of 2 ohms per signal path. Thus, the composite signal return path dc resistance must not exceed 2 ohms divided by 40 bus lines, or 50 milliohms. Note that although this common return path is nominally at ground potential, the conductance must be part of the bus wiring; the specified low impedance return path must be provided by the bus wiring as distinguished from common system or power ground path.

**Intra-Backplane Bus Wiring**

The wiring that interconnects the bus connector slots within one contiguous backplane is part of the overall bus transmission line. Due to implementation constraints, the nominal characteristic impedance of 120 ohms may not be achievable. Distributed wiring capacitance in excess of the amount required to achieve the nominal 120 ohm impedance may not exceed 60 pF per signal line per backplane.

**Power and Ground**

Each bus interface slot has connector pins assigned for the following dc voltages.*

+5 Vdc – Three pins (4.5 A maximum per bus device slot)
+12 Vdc – Two pins (3.0 A maximum per bus device slot)
Ground – Eight pins (shared by power return and signal return).

**NOTE**

**Power is not used between backplanes on any interconnecting bus cables.**

* The maximum allowable current per pin is 1.5 A. +5 Vdc must be regulated to ±5%; maximum ripple: 100 mV pp. +12 Vdc must be regulated to ±3%; maximum ripple: 200 mV pp.

## SYSTEM CONFIGURATIONS

LSI-11 bus systems can be divided into two types:

Systems containing one backplane

Systems containing multiple backplanes

Before configuring any system, three characteristics for each module in the system must be known. These characteristics include:

Power consumption – +5 Vdc and +12 Vdc current requirements.

AC bus loading – the amount of capacitance a module presents to a bus signal line. AC loading is expressed in terms of ac loads where one ac load equals 9.35 pF of capacitance.

DC bus loading – the amount of dc leakage current a module presents to a bus signal when the line is high (undriven). DC loading is expressed in terms of dc loads where one dc load equals 105 microamperes (nominal).

Power consumption, ac loading, and dc loading specifications for each module are included in the Microcomputer Handbook Series.

**NOTE**

**The ac and dc loads and the power consumption of the processor module, terminator module, and backplane must be included in determining the total loading of a backplane.**

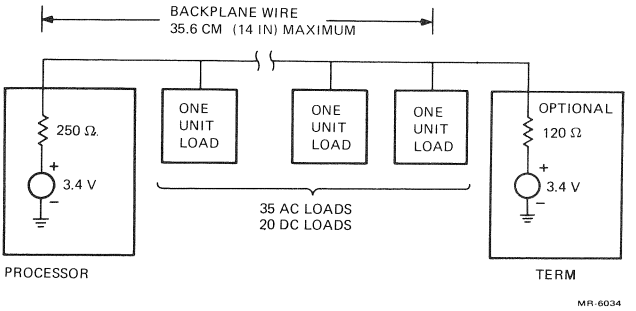
### Rules for Configuring Single Backplane Systems

1. The bus can accommodate modules that have up to a total of 20 ac loads (total) before an additional termination is required. The processor has onboard termination for one end of the bus. If more than 20 ac loads are included, the other end of the bus must be terminated with 120 ohms.

2. A single backplane, terminated bus can accommodate modules comprising up to a total of 35 ac loads.

3. The bus can accommodate modules up to a total of 20 dc loads.

4. The bus signal lines on the backplane can be up to 35.6 cm (14 in) long.




Single Backplane Configuration

**Rules for Configuring Multiple Backplane Systems**

1. Up to three backplanes may compose the system. The signal lines on each backplane can be up to 25.4 cm (10 in) long.

2. Each backplane can accommodate modules that have up to a total of 20 ac loads. Unused ac loads from one backplane may not be added to another backplane. It is desirable to load backplanes equally, or with the highest ac loads in the first and second backplanes.

3. DC loading of all modules in all backplanes cannot exceed a total of 20 loads.

4. Both ends of the bus must be terminated with 120 ohms. This means that the first backplane must have an impedance of 120 ohms (obtained via the processor 220 ohm terminations and a separate 220 ohm terminator), and the last backplane must have a termination of 120 ohms.

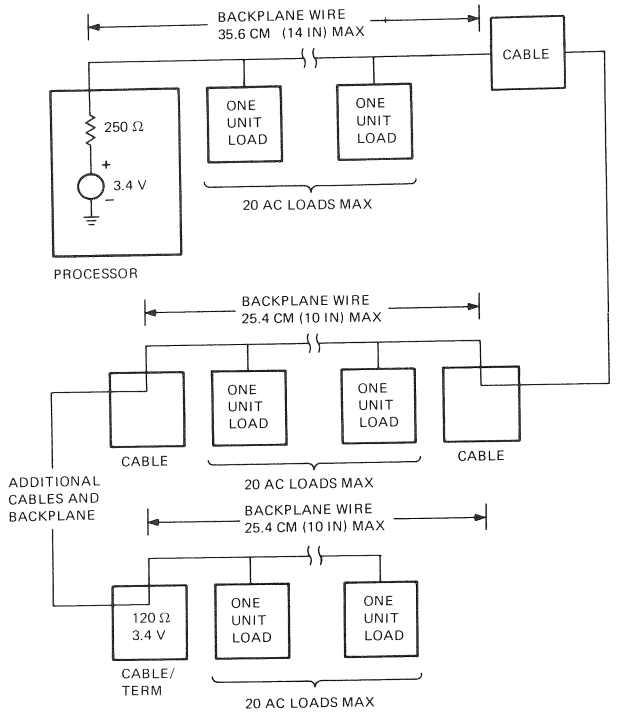
5. The cables used to connect the backplanes should adhere to the following rules.

    a. The cable(s) connecting the first two backplanes is 61 cm (2 ft) or greater in length.

    b. The cable(s) connecting the second backplane to the third backplane is 22 cm (4 ft) longer or shorter than the cable(s) connecting the first and second backplanes.

    c. The combined length of both cables cannot exceed 4.88 m (16 ft).

    d. The cables used must have a characteristic impedance of 120 ohms.




NOTES:
1. TWO CABLES (MAX) 4.88 M (16 FT) (MAX) TOTAL LENGTH.
2. 20 DC LOADS TOTAL (MAX).

MR-6035

Multiple Backplane Configuration

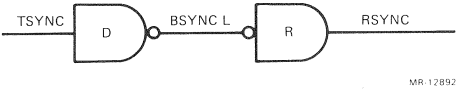
**Power Supply Loading**

Total power requirements for each backplane can be determined by obtaining the total power requirements for each module in the backplane. Obtain separate totals for +5 V and +12 V power. Power requirements for each module are specified in the Microcomputer Handbook Series.

When distributing power in multiple backplane systems, do not attempt to distribute power via the LSI-11 bus cables. Provide separate, appropriate power wiring from each power supply to each backplane. Each power supply should be capable of asserting BPOK H and BDCOK H signals according to bus protocol; this is required if automatic power fail/restart programs are implemented, or if specific peripherals require an orderly power-down halt sequence. The proper use of BPOK H and BDOK H signals is strongly recommended.

**NOTE**

**Timing diagrams reference signals at driver inputs (eg. TSYNC) and receiver outputs (eg. RSYNC). However, the accompanying text refers to the signals names in their bus specific form (eg. BSYNC). The relationship between the three signal names are shown below. Most timing numbers indicated in the text are given with respect to the R and T versions of the signals shown in the timing diagrams. In all cases the timing diagrams are the overriding authority.**




Signal Naming Conventions

# APPENDIX D
# FCC INFORMATION

## GENERAL

To meet Federal Communications Commission (FCC) and Verband Deutscher Elektroteckniker (VDE) mission requirements, it is necessary to prevent excessive electromagnetic interference from escaping from a computer systems enclosure.

DIGITAL has designed the LSI-11 cabinet kit system options to reduce interference by shielding cabinets and cables.

### Grandfather Terms

Products produced before October 1, 1981 and which would normally fall into the FCC verified category (commercial, industrial, and/or business use) were given "Grandfather Status", which means that they could continue to be built and labeled "untested" through September, 1983. Units built after September, 1983 must meet the applicable technical electromagnetic interference (EMI) limits of the FCC regulations, and must be labeled as such.

### Date of Manufacture

The date of manufacture for FCC purposes, is the date on which a product completes its volume build, receives its identity and labels, and moves into the finished goods category.

It is not necessary that all products be fully configured as they would be shipped in order to comply with the date of manufacture (DOM) requirements.

For instance, if a PDP-11/23 processor could be inventoried as a basic machine, after October, 1983 additional communications options, memory and floating point processor (FPP) might be added.

### Exempt

Exempt means that when a computing device is intended for several end-user applications, the device is exempt from part 15J testing/labeling/marketing rules. There are no exemptions from general prohibitions against interfering with licensed communications, both existing and proposed.

### Mixed Systems

Individual products maintain their identity and FCC label status in a mixed system. FCC rules applying to each individual product will apply.

When DIGITAL sells a product or products which create a mixed system, either as a sale or field add-on to another DIGITAL product, DIGITAL is responsible for the ability for each DIGITAL Class A or B product involved to continue to apply.

Interconnection of DIGITAL products with non-DIGITAL products is the responsibility of the purchaser of the products.

**Specific FCC Related Labels**

**Class B Certified**

These labels are for use on products marketed for use in the home or in residential areas.

Untested

These labels are used on "Grandfather" units. The use of these labels ends 30 September 1983, which is when production of all "Grandfather" products must cease.

Class A Verified

These labels are used on products marketed for end use in industrial, commercial, and business applications.

Class B Verified

Can be used on the same types of products as above (Class A Verified), if the product passed the stricter test limits of Class B.

**FCC Module List**

The FCC does not require labeling of subassemblies, modules, cables, etc. They do require that manufacturers inform their customers of "the interference potential" of such products. The method used to determine this information at the point of sale is to separate the products by generating a list for those which have successfully been integrated into Class A or Class B products.