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LSI-11, PDP-11/03
user's manual

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual contains technical data that will enable LSI-11 and PDP-11/03 microcomputer users to interface and use LSI-11 system components effectively. Before reading the detailed technical content of this manual, the user should become familiar with the basic characteristics of the LSI-11 processor, as described in the *LSI-11, PDP-11/03 Microprocessor Handbook.*

1.2 SCOPE

This manual contains hardware descriptions and information for using LSI-11 system modules, including system configuration, installation, and interfacing. The manual is organized as follows:

Chapter 1	Introduction
Chapter 2	LSI-11 and PDP-11/03 System Overview
Chapter 3	LSI-11 Bus
Chapter 4	LSI-11 Module Descriptions (including functional theory of operation)
Chapters 5—9	Use of the Various LSI-11 Modules (including jumper configurations, interfacing, and programming information)
Chapter 10	User-Designed Interfaces
Chapter 11	System Configuration and Installation
Chapter 12	Peripherals (including the basic devices available and the required LSI-11 interface module, and cables required for each)

In addition, quick reference information is included in appendixes. This information includes a memory map, LSI-11 bus pin assignments, the 7-bit ASCII code, and a summary of LSI-11 instructions.

1.3 REFERENCES

The *LSI-11, PDP-11/03 Processor Handbook* is a required reference manual for using LSI-11 system components. In addition, standard hardware and interface components are listed and described in the *Hardware/Accessories Catalog* and the *Logic Handbook.*

CHAPTER 2
LSI-11 SYSTEM OVERVIEW

2.1 GENERAL

All LSI-11 and PDP-11/03 systems are configured by selecting various LSI-11 module options which can be installed in a backplane. Although individual system requirements (in which the LSI-11 system functions as a controller and/or data processor) may vary greatly in each application, LSI-11's modular concept allows for efficient use of the microcomputer in a compact, cost-effective, flexible system design. The PDP-11/03 is a packaged LSI-11 system, including a processor, 4K memory, enclosure, H9270 backplane, and H780 power supply.

In general, all LSI-11 and PDP-11/03 systems include the KD11-F or KD11-J microcomputer. The KD11-F is a single 8.5 by 10 inch module that contains the LSI-11 microprocessor and a 4K by 16-bit semiconductor read/write memory. The KD11-J uses the same microcomputer module as the KD11-F; however, it is supplied with the MMV11-A 4K by 16-bit core memory instead of the semiconductor memory. Either type of basic LSI-11 or PDP-11/03 system can be expanded by adding various memory and peripheral device interface options.

2.2 SYSTEM CONFIGURATIONS

LSI-11 systems can be configured using one of three general approaches:

1. *Modules only:* The user purchases only the basic module(s).
2. *Modules and backplane:* The user purchases an LSI-11 subsystem that is easily mounted in a larger system.
3. *LSI-11 system in a box:* The user purchases a PDP-11/03 system. It includes the KD11-F or KD11-J processor and 4K memory, an H9270 backplane, and an H780 power supply installed in a rack-mountable enclosure.

Systems are configured using the basic modules described in the following paragraphs.

2.3 LSI-11 MICROCOMPUTER

This paragraph focuses on the KD11-F (processor and 4K semiconductor memory), which is the basic LSI-11 microcomputer. The KD11-J has all of the basic features of the KD11-F, except for the semiconductor memory; the MMV11-A core memory is included as a separate module.

Each KD11-F features:

- A low-cost, powerful processor for integration into any small- or medium-sized computer system.
- Direct addressing of 32K 16-bit words or 64K 8-bit bytes (K = 1024).
- Efficient processing of 8-bit characters without the need to rotate, swap, or mask.
- Asynchronous operation that allows system components to run at their highest possible speed; replacement with faster devices means faster operation without other hardware or software changes.
- A modular component design that provides ease and flexibility in configuring systems.
- Hardware memory stack for handling structured data, subroutines, and interrupts.
- Direct memory access for high data rate devices inherent in the bus architecture.
- Eight general-purpose registers that are available for data storage, pointers, and accumulators. Two are dedicated: SP and PC.
- A bus structure that provides position-dependent priority as peripheral device interfaces are connected to the I/O bus.

- Fast interrupt response without device polling.
- A powerful and convenient set of programming instructions.
- A jumper-selected power-up mode that enables restart through a power-up vector, console Octal Debugging Technique (ODT) microcode subset, or a bootstrap program.
- On-board 4K RAM
- An ODT microprogram that controls all manual entry/display functions previously performed by a control panel through a serial ASCII device (optional) which is capable of transmitting and receiving ODT commands and data.
- Compact size (only 8.5 by 10 in.).

2.4 I/O BUS CONCEPT

The LSI-11 I/O bus is simple, fast, and easy to use as an interface between the LSI-11 microcomputer, memory, and peripheral interface modules. It comprises 17 control lines and a 16-line data/address bus. All modules connected to this bus receive the same interface signals.

Address/data and control lines are open-collector lines which are asserted low. The microcomputer module is capable of driving six device locations along the bus. Peripheral interface or memory modules can be installed in any location along this bus.

Both address and data words (or bytes) are time multiplexed over 16 bus lines. For example, during a programmed data transfer, the LSI-11 microcomputer first asserts an address on the bus for a fixed time. After the address time has been completed, the processor performs either an input or output data transfer; the actual data transfer is asynchronous and requires a response from the addressed device. Bus synchronization and control signals provide this function.

Control signal lines include two daisy-chained grant signals which provide a priority-structured I/O system. The highest priority device is the module electrically closest to the KD11-F (or KD11-J) module. Higher priority devices pass a grant signal to lower priority devices only when not requesting service. (Memory options or devices which do not use these signals must connect the chain.)

The KD11-F contains a memory address register and 4K bank address decoder for its resident memory, which can be assigned to bank 0 or bank 1. Bank 7 is also decoded when addresses ranging from 160000 to 177777 are placed on the bus. These addresses are normally used for addressing nonmemory devices, thus eliminating the need for bank address decoding on peripheral device interface modules.

The bus provides a vectored interrupt capability for any interface device. Hence, device polling is not required in interrupt processing routines. This results in a considerable savings in processing time when many devices requiring interrupt service are interfaced along the bus. When a device receives an interrupt grant (acknowledge), the KD11-F inputs the device's interrupt vector. The vector points to two addresses which contain a new processor status word and the starting address of the interrupt service routine for the device.

One bus signal line functions as an external event interrupt input to the KD11-F module. This signal line can be connected to a frequency source, such as a line frequency, and used as a line time clock (LTC) interrupt. A jumper on the KD11-F module enables or inhibits this function. When enabled, the device connected to this line has the highest interrupt priority external to the processor. Interrupt vector 100_8 is reserved for this function, and an interrupt request via the BEVNT line causes new PC and PS words to be loaded from locations 100_8 and 102_8.

Memory refresh of dynamic MOS read/write memory is accomplished by bus signals. Refresh operation is controlled by either the processor module microcode or a user-supplied intelligent DMA device.

The processor can be placed in the Halt mode by asserting one bus signal. This allows peripheral devices or a separate switch to invoke console ODT microcode operation.

Power-up/power-down sequencing is controlled by two bus signals. One signal, when in its true state, implies that primary power is normal. The second signal is in its true state when sufficient dc power is available (and voltages are normal) for normal system logic operation. These signals are produced by circuits contained in the H780 power supply (PDP-11/03 only) or by the user's system (circuits external to the LSI-11 system components).

Direct memory access (DMA) operation is controlled by three bus signals. Logic on the processor module, which is normally bus master, arbitrates DMA requests and grants bus mastership to the highest priority device requesting the bus. Priority is position-dependent through the use of a daisy-chained DMA grant signal.

2.5 MEMORY OPTIONS

Memory options are available for expanding memory to 28K. The basic LSI-11 microcomputer is supplied with read/write memory. KD11-F's memory consists of a 4K dynamic MOS array which is physically located on the processor module. KD11-J's memory is a 4K magnetic core array contained on a separate module; the processor module supplied with the KD11-J contains no semiconductor memory components.

Optional memory modules include:

MRV11-AA — 4K by 16-bit programmable read-only memory on an 8.5 by 5 inch module. Requires one device location on the I/O bus. Can be configured using either 256 by 4-bit or 512 by 4-bit field programmable or masked ROMs for a maximum capacity of 2048 or 4096 16-bit words.

MSV11-A — 1K by 16-bit static read/write memory on an 8.5 by 5 inch module. Requires one device location on the I/O bus.

MMV11-A — 4K by 16-bit core memory on an 8.5 by 10 by 0.9 inch module. Requires two device locations on the I/O bus when installed in the backplane (preferred location slots A4-D4). This allows a daughterboard (part of the MMV-11-A) to extend slightly beyond the backplane without using additional device locations. If not installed in this location, the MMV11-A requires four device locations because of the additional module thickness (0.9 inch instead of 0.5 inch for all other modules).

MSV11-B — 4K by 16-bit dynamic MOS read/write memory on an 8.5 by 5 inch module. Requires one device location on the I/O bus. Refresh is automatically performed by the KD11-F processor microcode or by an external device.

2.6 PERIPHERAL INTERFACE OPTIONS

Two basic interface modules are used for serial and parallel programmed I/O transfer between the LSI-11 bus and peripheral devices. The DLV11 is a serial line unit used for serial 5- to 8-bit data transfers between a device and the bus. It interfaces either EIA-compatible or 20 mA current loop devices to the bus using optional cables which select the type of serial interface desired. The cables are completely connector- and pin-compatible with available modems, DECwriter, DECscope, and teletypewriter options. The DRV11 is a general-purpose parallel line unit interface which is capable of 16-bit input and 16-bit output parallel transfers to/from user devices.

Both interface units contain all required control/status registers, interrupt control logic, and bus interface logic. The user can easily assign unique device and vector addresses for each device by changing the jumpers on each interface module.

Peripheral interface options include:

DLV11 — Serial line unit interface on an 8.5 by 5 inch module. Requires one device location on the bus. Jumpers select crystal-controlled baud rates (50—9600 baud) and serial word format, including number of stop bits, number of data bits, and even, odd, or no parity bit. Optional interface cables include the BC05M, which connects the DLV11 to 20 mA current loop peripheral devices, and the BC05C, which connects the DLV11 to EIA-compatible devices (modems) via a Cinch DB-25P connector.

DRV11 — General-purpose parallel line unit interface on an 8.5 by 5 inch module. Requires one device location on the bus. Two 40-pin connectors are included on the module for user interface application. One is the 16-bit input and the other is the 16-bit output. Optional interface cables are described in the Hardware/Accessories Catalog.

2.7 BACKPLANE, POWER SUPPLY, AND HARDWARE OPTIONS

Backplane, power supply, and hardware options provide a convenient means for configuring the LSI-11 system. An LSI-11 system usually requires an interconnection scheme. The H9270 backplane assembly is the most convenient to use. It is prewired for the LSI-11 I/O bus pinning and can accept one KD11-F microcomputer and up to six LSI-11 interface or memory modules. It includes a card guide assembly which provides mechanical stability for the modules. Power and ground are applied to the backplane via a screw-terminal block.

Power can be obtained from the system in which the LSI-11 subsystem is installed, or the H780 (115 or 230 Vac input) power supply (included in PDP-11/03 systems) can be used. The power supply provides the required regulated voltages for all LSI-11 modules connected to the backplane. In addition, it generates the necessary bus signals to initiate the KD11-F or KD11-J power-up or power-fail processor sequence. Hardware options include standard hardware accessories listed in DIGITAL's Hardware/Accessories Catalog.

2.8 POWER REQUIREMENTS

The power requirements for LSI-11 system modules are given in Table 2-1.

Table 2-1
LSI-11 Modules Power Requirements

Designation	+5 V ±5%		+12 V ±3%	
	Typ	Max	Typ	Max
KD11-F	1.8A	2.4A	0.8A	1.6A
KD11-J	6.4A	9.0A	1.2A	1.5A
DLV11	1.0A	1.6A	180 mA	250 mA
DRV11	0.9A	1.6A		
MRV11-AA (without memory chips)	0.4A	0.6A		
MRV11 (with 4K memory chips)	2.8A	4.1A		
MSV11-A	0.8A	1.8A	0.1A	0.1A
MSV11-B	0.6A	1.2A	0.3A	0.7A
MMV11-A (standby)	3.0A		0.2A	
MMV11-A (operating)	7.0A		0.6A	

The input power requirements for PDP-11/03 systems are:

PDP-11/03-AA or -BA

100-127 Vac (115 Vac nominal), 50 ± 1 Hz or 60 ± 1 Hz, single phase, 400 W maximum (including options) (190 W typical)

PDP-11/03-AB or -BB

200-254 Vac (230 Vac nominal), 50 ± 1 Hz or 60 ± 1 Hz, single phase, 400 W maximum (including options) (190 W typical)

2.9 GENERAL SPECIFICATIONS

Dimensions (in.)

KD11-F

10.5 × 8.50 × 0.5

MSV11-A

5×8.50×0.5

MSV11-B

5×8.50×0.5

MRV11-AA

5×8.50×0.5

MMV11-A

10×8.50×0.9

DLV11

5×8.50×0.5

DRV11

5×8.50×0.5

Electrical

Input Logic Levels

TTL Logical Low: 0.8 Vdc max
TTL Logical High: 2.0 Vdc min

Output Logic Levels

TTL Logical Low: 0.4 Vdc max
TTL Logical High: 2.4 Vdc min

Bus Receivers

Logical Low: 1.3 Vdc max, -10μA max at 0V
Logical High: 1.7 Vdc min, 80μA max at 2.5V

Bus Drivers

Logical Low: 0.8 Vdc max at 70 mA
Logical High: 25μA max at 3.5V

Environmental

Ambient Temperature, *PDP-11/03 System:*

Operating: 5° to 40° C

Ambient Temperature, *LSI-11 modules:*

Operating: 5° to 50° C (41° to 122° F)
Nonoperating: —40° to 66° C (—40° to + 150° F)
Derate at 60° C/1000 ft. above 8000 ft.

Humidity

10 to 90 percent, noncondensing

Air Flow

200 linear ft./minute min. (modules only)

CHAPTER 3
THE LSI-11 BUS

3.1 CHOOSING AN I/O TRANSFER TYPE

Before interfacing the processor with any peripheral device, the designer must determine the type of I/O transfer that would be best suited for the application: programmed I/O transfers, DMA, or interrupt-driven transfers.

Programmed I/O transfers are executed by single- or double-operand instructions. The instruction can be used to input or output a 16-bit data word or an 8-bit byte. By including the device's address as the effective source or destination address, the user selects the input or output operation. In many instances, the programmer inputs a byte from the device's CSR to determine that the device has input data ready or that it is ready to accept the processor's output data.

DMA transfers are the fastest method of transferring data between memory and a device. They can occur between processor bus cycles and do not alter processor status in any way. Addressing, controlling the size of the data block (number of word or byte transfers in the operation), and type of transfer are under the control of the requesting device. The processor does not modify data being moved in the DMA mode. Thus, blocks of data can be moved at memory speeds via the DMA transfer mode. The processor sets up these conditions before the DMA transfer is executed.

Interrupts allow the processor to continue a programmed operation (sometimes called a background program) without waiting for a device to become ready to transfer data. When the device does become ready, it interrupts the processor's background program execution and causes execution of a device interrupt service routine. After the device's service routine has been executed, the background program is restored and program execution resumes at the point where it was interrupted.

3.2 DEVICE PRIORITY

Each device has an I/O priority based on its distance from the processor. When two or more devices request interrupt service, the device electrically closer to the microcomputer will receive the interrupt grant (acknowledge). The microcomputer can be inhibited from issuing more grants by setting the processor's priority to 4 in the PS word. Bit 7 in the new PS word should be a 1. If further interrupts are to be serviced, the processor's priority should be 0, and bit 7 in the new PS word should be a 0. Consequently, interrupts can be nested to any level. Factors to consider when assigning device priorities are:

1. *Device Operating Speed* — Data from a fast device is available for only a short period; highest priorities are usually assigned to fast devices to prevent loss of data and to prevent the bus from being tied up by slower devices.
2. *Ease of Data Recovery* — If data from a device is lost, recovery may be automatic, may require manual intervention, or may be impossible to recover; highest priorities are assigned to devices whose data cannot be recovered.
3. *Service Requirements* — Some devices cannot function without help from the processor, while DMA devices can operate independently and require only minimal processor intervention; devices requiring continual help from the processor for servicing are assigned to lowest priorities to prevent tying up the processor.

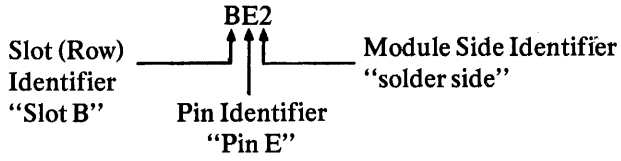
Both address and data are multiplexed onto the 16 BDAL lines. In addition, individual control signals sequence programmed I/O operations, direct memory access (DMA), and processor interrupts. Any bus-

compatible module can be inserted into any bus location and still receive interface signals; however, the module's priority, which is position-dependent along the bus, will change.

3.3 MODULE CONTACT FINGER IDENTIFICATION

DIGITAL plug-in (FLIP CHIP) modules, including LSI-11 modules, all use the same contact finger (pin) identification system. The LSI-11 I/O bus is based on the use of double-height modules. These modules plug into a two-slot bus connector, each containing 36 lines per slot (18 each on component and solder sides of the circuit board). Although the LSI-11 processor module and core memory module are quad-height modules that plug into four connector slots, only two slots (A and B) are used for interface purposes on the processor module. Etched circuit jumpers on the unused portion of the module maintain continuity of grant signals BIAKI L to BIAKO L and BDMGI L to BDMGO L. These daisy-chained signals are described later.

Slots, shown as ROW A and ROW B in Figure 3-1, include a numeric identifier for the side of the module. The component side is designated side "1" and the solder side is designated side "2." Letters ranging from A through V (excluding G, I, O, and Q) identify a particular pin on a side of a slot. Hence, a typical pin is designated as:



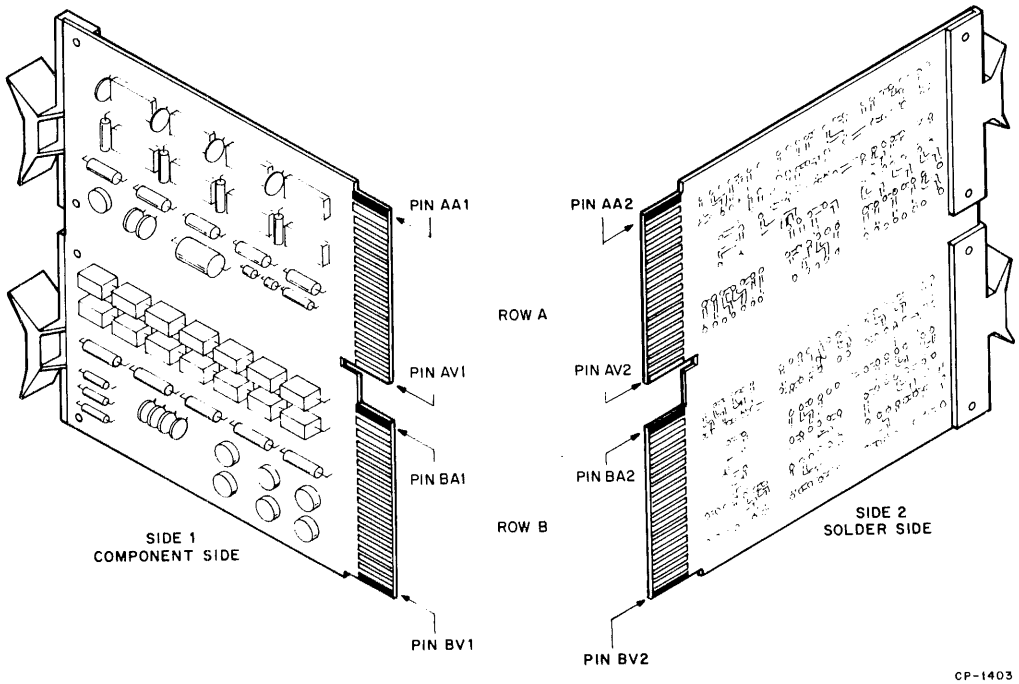


Figure 3-1 Module Contact Finger Identification

Note that the positioning notch between the two rows of pins mates with a protrusion on the connector block for correct module positioning.

Quad-height modules are similarly pin numbered. They are identified in Figure 3-2.

Individual connector pins, viewed from the underside (wiring side) of a backplane, are identified as shown in Figure 3-3. Only the pins for one bus location (two slots) are shown in detail. This pattern of pins is repeated eight times on the H9270 backplane, allowing the user to install one LSI-11 microcomputer module (four slots) and up to six additional two-slot modules.

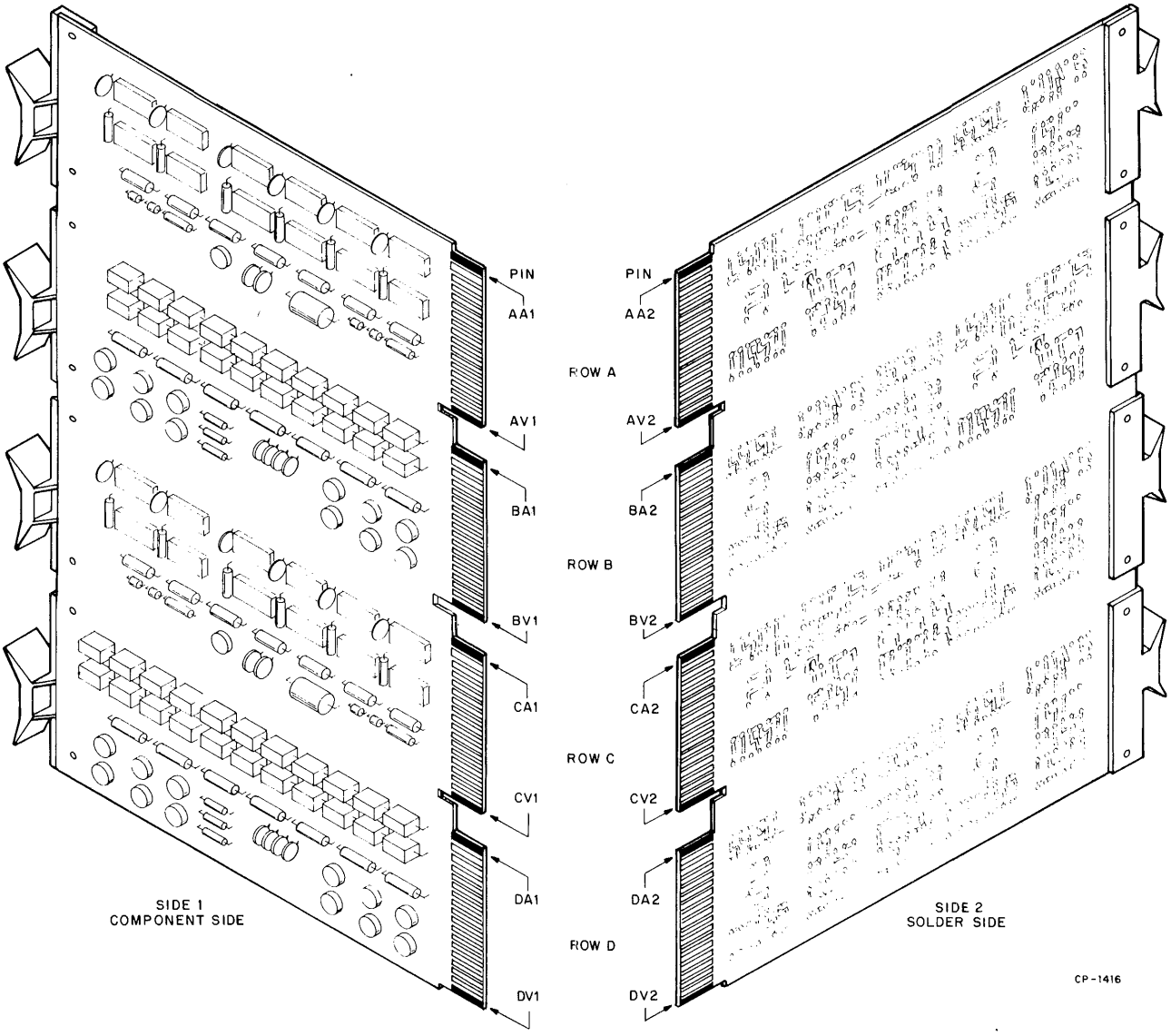


Figure 3-2 Quad Module Contact Finger Identification

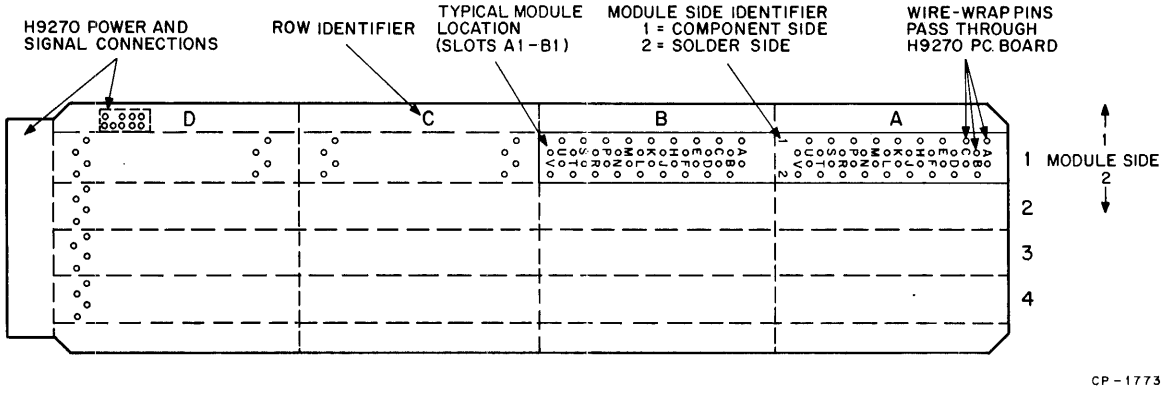


Figure 3-3 LSI-11, PDP-11/03 Backplane Module Pin Identification

3.4 BUS SIGNALS

H9270 backplane pin assignments are listed and described in Table 3-1. Only slots A and B are listed. However, they are identical to slots C and D, respectively. Applicable bus cycle timing and specifications are discussed in Paragraphs 3.12, 3.13, and 3.14.

Table 3-1
Backplane Pin Assignments

Bus Pin	Mnemonic	Description
AA1 AB1 AC1 AD1	BSPARE1 BSPARE2 BSPARE3 BSPARE4	Bus Spare (Not assigned. Reserved for DIGITAL use.)
AE1 AF1 AH1	SSPARE1 SSPARE2 SSPARE3	Special Spare (Not assigned, not bused. Available for user interconnections.) – SRUN (ON PROCESSOR
AJ1	GND	Ground — System signal ground and dc return.
AK1 AL1	MSPAREA MSPAREA	Maintenance Spare — Normally connected on the backplane at each option location (not bused connection).
AM1	GND	Ground — System signal ground and dc return.
AN1	BDMR L	Direct Memory Access (DMA) Request — A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt — When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the processor module is removed) and DMA request/grant sequences are enabled. When in the halt state, the processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF L	Memory Refresh — Asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC L/BDIN L bus transaction. **CAUTION** **The user should avoid using multiple DMA data transfers [Burst or "hog" mode] during a processor-generated refresh operation so that a complete refresh cycle can occur once every 1.6 ms.**
AS1	PSPARE3	Spare (Not assigned. Customer usage not recommended.)
AT1	GND	Ground — System signal ground and dc return.
AU1	PSPARE1	Spare (Not assigned. Customer usage not recommended.)
AV1	+5B	+5 V Battery Power — Secondary +5 V power connection. Battery power can be used with certain devices.
BA1	BDCOK H	DC Power OK — Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.

Table 3-1 (Cont)
Backplane Pin Assignments

Bus Pin	Mnemonic	Description
BB1	BPOK H	Power OK — Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BC1	SSPARE4	Special Spare (Not assigned, not bused. Available for user interconnections.)
BD1	SSPARE5	
BE1	SSPARE6	
BF1	SSPARE7	
BH1	SSPARE8	
BJ1	GND	Ground — System signal ground and dc return.
BK1	MSPAREB	Maintenance Spare -- Normally connected on the backplane at each option location (not a bused connection).
BL1	MSPAREB	
BM1	GND	Ground — System signal ground and dc return.
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BSPARE6	Bus Spare (Not assigned. Reserved for DIGITAL use.)
BR1	BEVNT L	External Event Interrupt Request — When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100_8. A typical use of this signal is a line time clock interrupt.
BS1	PSPARE4	Spare (Not assigned. Customer usage not recommended.)
BT1	GND	Ground — System signal ground and dc return.
BU1	PSPARE2	Spare (Not assigned. Customer usage not recommended.)
BV1	+5	+5 V Power — +5 Vdc system power.
AA2	+5	+5 V Power — Normal +5 Vdc system power.
AB2	-12	-12 V Power — -12 Vdc (optional) power for devices requiring this voltage. **NOTE** **LSI-11 modules which require negative voltages contain an inverter circuit (on each module) which generates the required voltage(s); hence, -12 V power is not required with DIGITAL-supplied options.**
AC2	GND	Ground — System signal ground and dc return.
AD2	+12	+12 V Power — +12 Vdc system power.
AE2	BDOUT L	Data Output — BDOUT, when asserted, implies that valid data is available on BDAL0—15 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply — BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transactions. It is generated by a slave device to indicate that it has input data available on the BDAL bus or that it has accepted output data from the bus.

Table 3-1 (Cont)
Backplane Pin Assignments

Bus Pin	Mnemonic	Description
AH2	BDIN L	Data Input — BDIN L is used for two types of bus operations: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize — BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL0—15 L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte — BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
AL2	BIRQ L	Interrupt Request — A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. This signal informs the processor that a device has data to input to the processor or it is ready to accept output data. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output — This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin.
AP2	BBS7 L	Bank 7 Select — The bus master asserts BBS7 L when an address in the upper 4K bank (address in the 28-32K range) is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant-Input and DMA Grant-Output— This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle. **CAUTION** **DMA device transfers must be single transfers and must not interfere with the memory refresh cycle.**
AT2	BINIT L	Initialize — BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).

Table 3-1 (Cont)
Backplane Pin Assignments

Bus Pin	Mnemonic	Description
AU2	BDAL0 L	Data/Address Lines — These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.
AV2	BDAL1 L	
BA2	+5	+5 V Power — Normal +5 Vdc system power.
BB2	-12	-12 V Power — -12 Vdc (optional) power for devices requiring this voltage.
BC2	GND	Ground — System signal ground and dc return.
BD2	+12	+12 V Power — +12 V system power
BE2	BDAL2 L	
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	Data/Address Lines — These 14 lines are part of the 16-line data/address bus previously described.
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

3.5 BUS CYCLES

3.5.1 General

Every processor instruction requires one or more I/O operations. The first operation required is a data input transfer (DATI), which fetches an instruction from the location addressed by the program counter (PC or R7). This operation is called a DATI bus cycle. If no additional operands are referenced in memory or in an I/O device, no additional bus cycles are required for instruction execution. However, if memory or a device is referenced, additional DATI, data input/output (DATIO or DATIOB), or data output transfer (DATO or DATOB) bus cycles are required. Between these bus cycles, the processor can service DMA requests. In addition, the processor can service interrupt requests only prior to an instruction fetch (DATI bus cycle) if the processor's priority is zero. (PS word bit 7 is 0.)

The following paragraphs describe the types of bus cycles. Note that the sequences for I/O operations between processor and memory or between processor and I/O device are identical. DATO (or DATOB) cycles are equivalent to write operations, and DATI cycles are equivalent to read operations. In addition, DATIO cycles include an input transfer followed by an output transfer. The DATIO cycle provides an efficient means of executing an equivalent read-modify-write operation by making it unnecessary to assert an address a second time.

3.5.2 Input Operations

The sequence for a DATI operation is shown in Figure 3-4. DATI cycles are asynchronous and require a response from the addressed device or memory. The addressed memory or device responds to its input request (BDIN L) by asserting BRPLY L. If BRPLY is not asserted within 10μs (max) after BDIN L is asserted, the processor terminates the cycle and traps through location 4.

Note that BWTBT L is not asserted during the address time, indicating that an input data transfer is to be executed.

A DATIO cycle is equivalent to a read-modify-write operation. An addressing operation and an input word transfer are first executed in a manner similar to the DATI cycle; however, BSYNC L remains in the active state after completing the input data transfer. This causes the addressed device or memory to remain

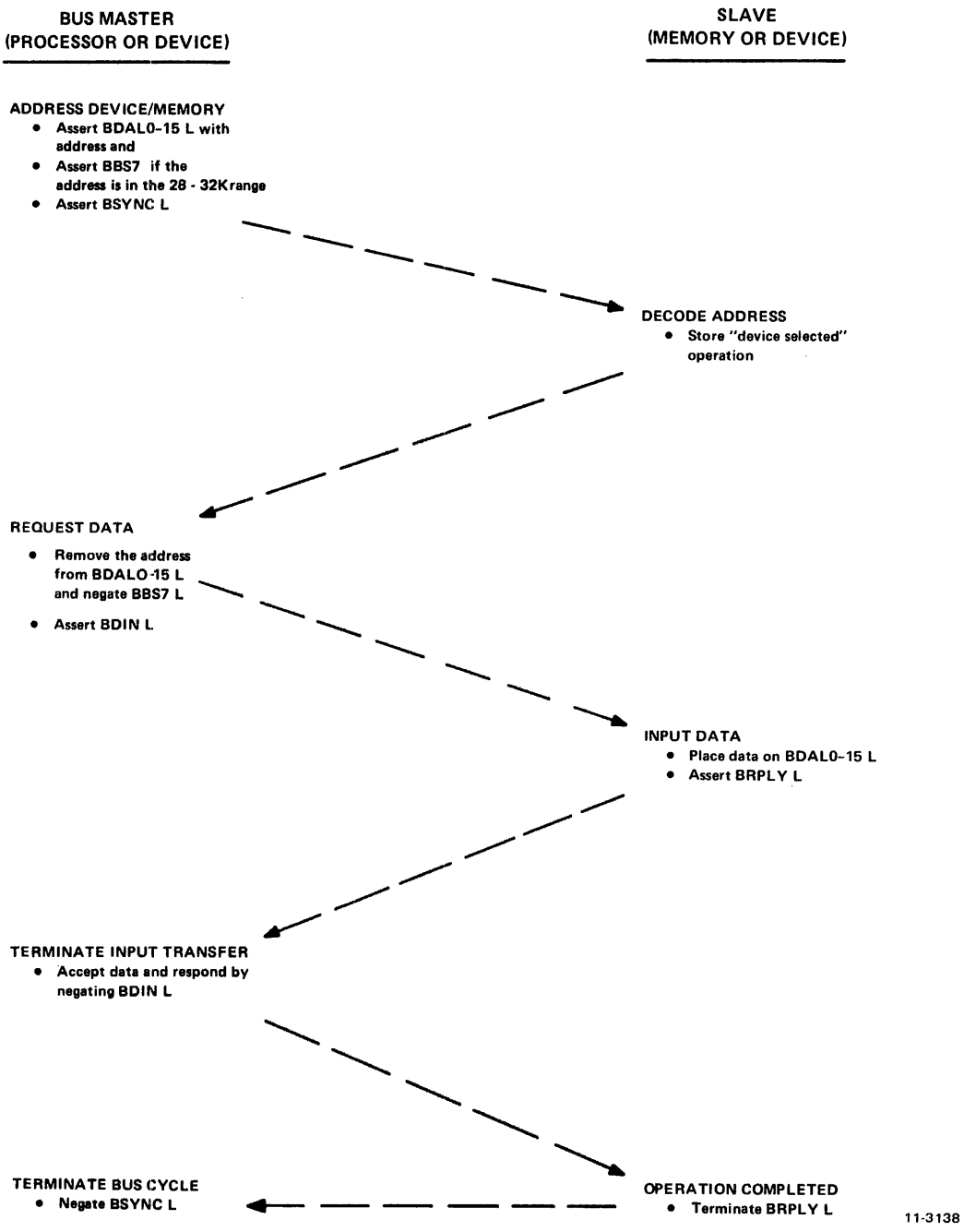


Figure 3-4 DATI Bus Cycle

selected, and an output data transfer follows without any further addressing. After completing the output transfer, the device terminates BSYNC L, completing the DATIO cycle. The actual sequence required for a DATIO cycle is shown in Figure 3-5. Note that the output data transfer portion of the bus cycle can be a byte transfer; hence, this cycle is shown as DATIOB.

3.5.3 Output Operations

The sequence required for a DATO or the equivalent output byte (DATOB) bus cycle is shown in Figure 3-6. Like the input operations, failure to receive BRPLY L within 10μs after asserting BDOUT L is an error, and results in a processor time-out trap through location 4.

Note that BWTBT L is asserted during the addressing portion of the cycle to indicate that an output data transfer is to follow. If a DATOB is to be executed, BWTBT L remains active for the duration of the bus cycle; however, if a DATO (word transfer) is to be executed, BWTBT L is negated during the remainder of the cycle.

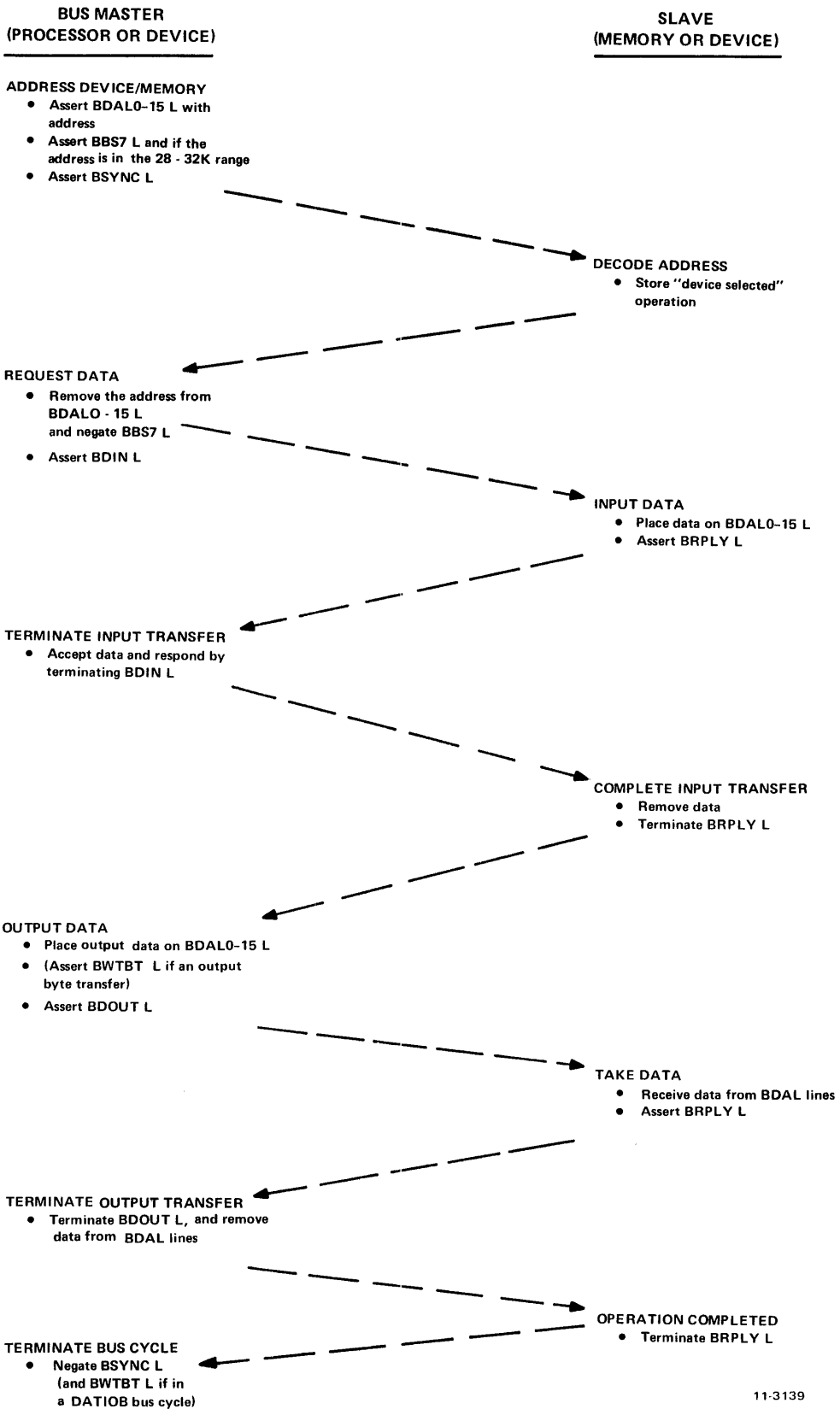


Figure 3-5 DATIO or DATIOB Bus Cycle

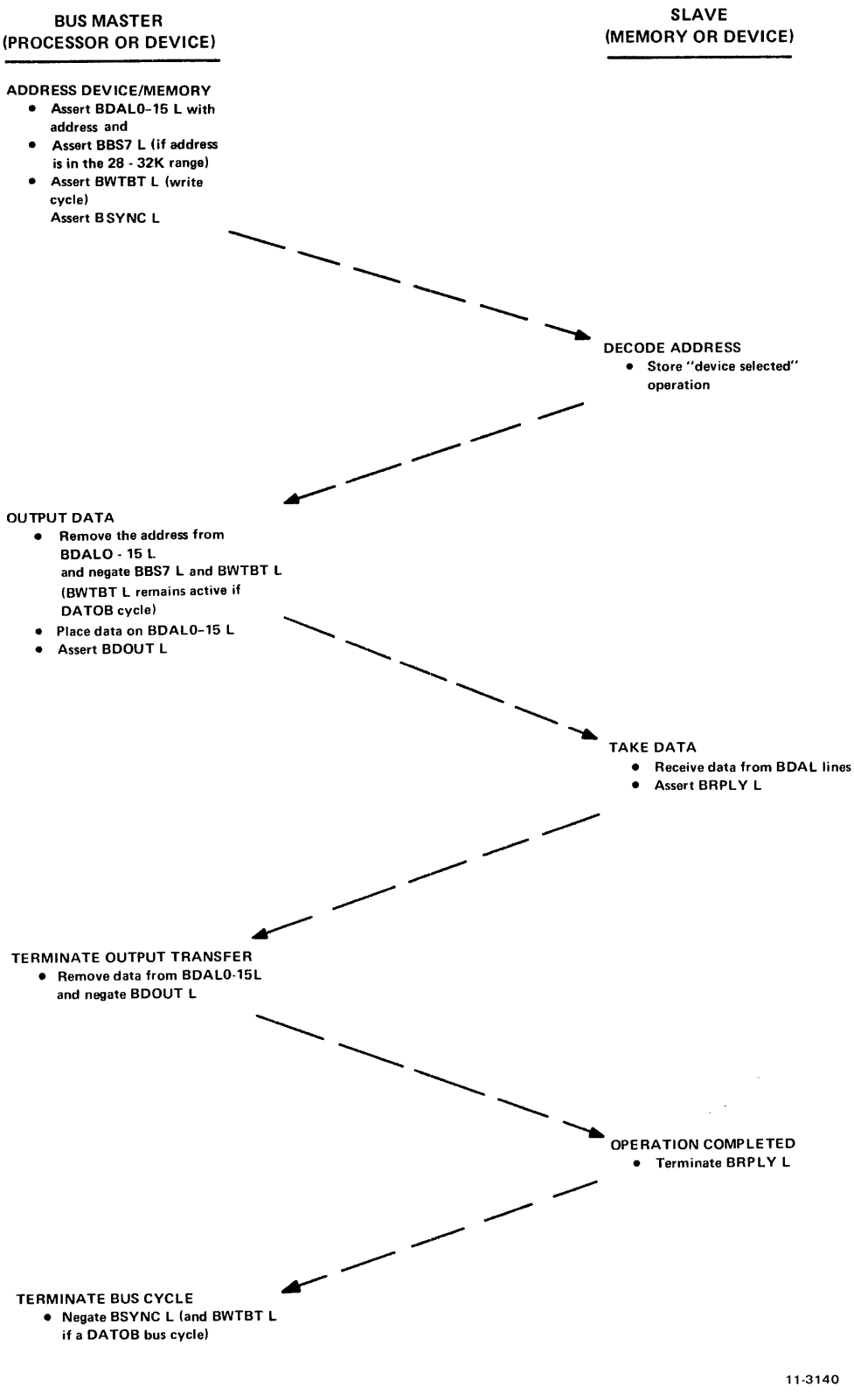


Figure 3-6 DATO or DATIOB Bus Cycle

3.6 DMA OPERATIONS

DMA I/O operations involve a peripheral device and system memory. A device can transfer data to or from the 4K memory on the processor module or any read/write memory module along the bus. The actual sequence of operations for executing the data transfer once a device has been granted DMA bus control is as previously described for input and output I/O bus cycles, except the DMA device, not the processor, is bus master (controls the operation). Memory addressing, timing, and control signal generation/response are provided by logic contained on the device's DMA interface module; the processor is not involved with address and data transfers during a DMA operation.

The required DMA sequence is shown in Figure 3-7. A device requests the I/O bus by asserting BDMR L. After completing the present bus cycle, the processor responds by asserting BDMGO L, allowing the device

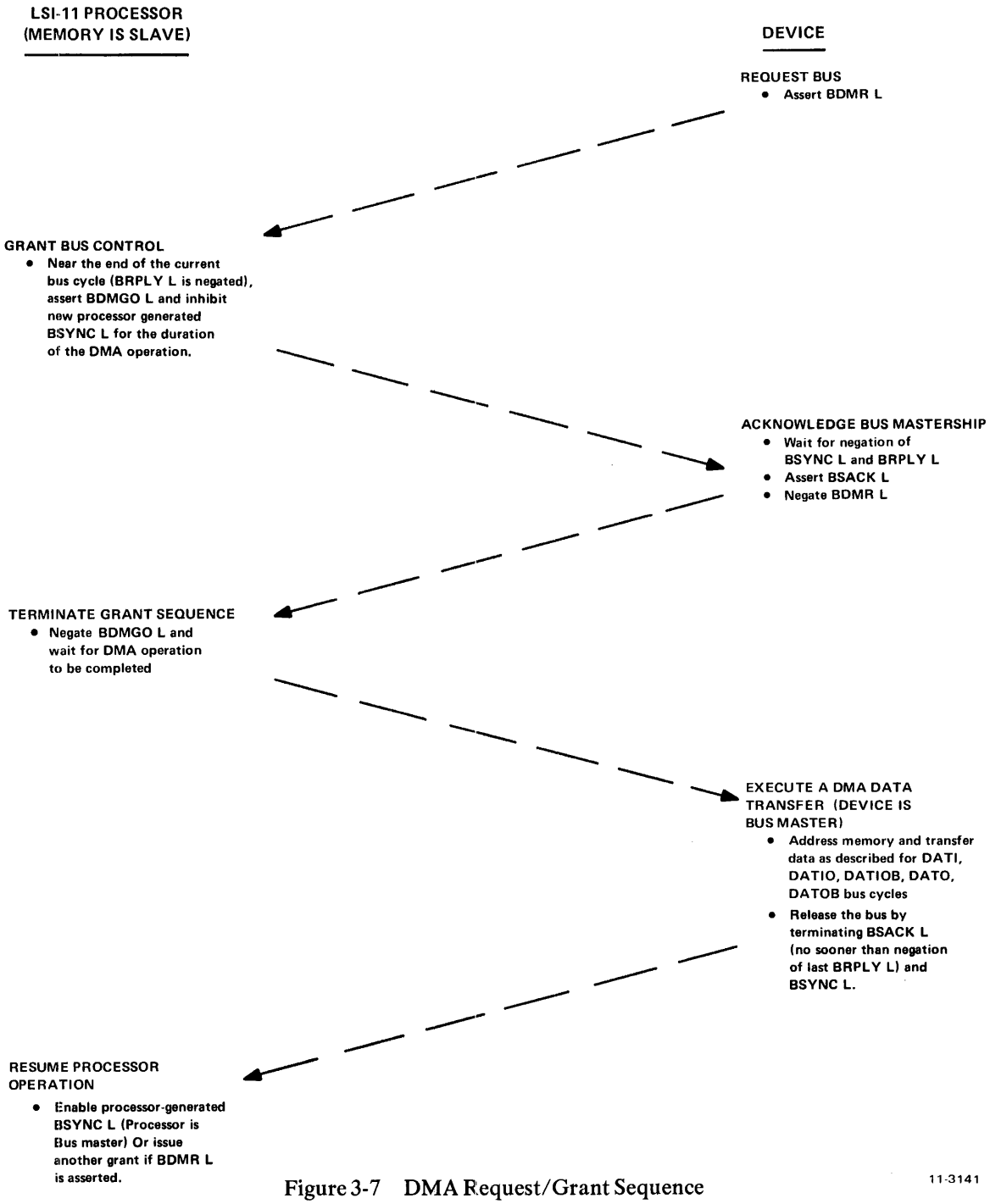


Figure 3-7 DMA Request/Grant Sequence

to become bus master. It also inhibits further processor generation of BSYNC L, preventing processor-initiation of a new bus cycle. The device responds by asserting BSACK L and negating BDMR L, causing the processor to terminate BDMGO L; the device is now bus master and it can execute the required data transfer in the same manner described for a DATI, DATIO, DATIOB, DATO, or DATOB bus cycle. When the data transfer is completed, the device returns bus master control to the processor by terminating the BSACK L and BSYNC L signals.

3.7 INTERRUPTS

Interrupts are requests made by peripheral devices which cause the processor to temporarily suspend its present (background) program execution to service the requesting device. Each device which is capable of requesting an interrupt has a service routine which is automatically entered when the processor acknowledges the interrupt request. After completing the service routine execution, program control is returned to the interrupted program. This type of operation is especially useful for the slower peripheral devices.

A device can interrupt the processor only when interrupts are enabled and the device is the closest device to the processor along the I/O bus. The processor's priority in the PS word is 4 when external interrupts are disabled and 0 when external interrupts are enabled. Device priority is highest for devices electrically closest to the processor along the bus.

Any device that can interrupt the processor can also interrupt the service routine execution of a lower priority device if the processor's priority is 0 during that execution; hence, interrupt nesting to any level is possible with this interrupt structure. Each device normally contains a control status register (CSR), which includes an interrupt enable bit. A program must set this bit before an interrupt request can actually be granted to a device.

An interrupt vector associated with each device is hard-wired into the device's interface/control logic. This vector is an address pointer that allows automatic entry into the service routine without device polling.

When an interrupt request is issued via the external event signal line, the processor automatically services the request via location 100_8; it does not input a vector address as done for other external interrupt devices. This interrupt function is normally used for a line time clock input based on the frequency of the local ac power (50 or 60 Hz).

The interface control and data signal sequence required for interrupts is shown in Figure 3-8. A device requests interrupt service by asserting BIRQ L. The processor can acknowledge interrupt requests only between instruction executions by generating an active (low) BDIN L signal, enabling the device's vector response. The processor then asserts the BIAKO L signal. The first device on the bus receives this daisy-chained signal at its BIAKI L input. If it is not requesting service, it passes the signal via its BIAKO L output to the next device, and so on, until the requesting device receives the signal. The device that did not pass the BIAKO L signal responds by asserting BRPLY L (low) and placing its interrupt vector on data/address bus lines BDAL0—15 L. Automatic entry to the service routine is then executed by the processor as previously described.

NOTE

If a device fails to assert BRPLY L in response to BDIN L within 10 μ sec, the processor enters the Halt state.

3.8 BUS INITIALIZATION

Devices along the I/O bus are initialized whenever the system dc voltages are cycled on or off, or when a RESET instruction is executed. Initialization during the power-on/power-off sequence is described in Paragraph 3.9. When the RESET instruction is executed, the processor responds by asserting BINIT L for approximately 10μs. Devices along the bus respond to the BINIT L signal, as appropriate, by clearing registers and presetting or clearing flip-flops.

3.9 POWER-UP/POWER-DOWN SEQUENCE

Power status signals BPOK H and BDCOK H must be asserted or negated in a particular sequence as dc operating power is applied or removed. Initially, BDCOK H and BPOK H are passive (low). As dc voltages rise to operating levels, BINIT L is asserted by the processor module. Approximately 3 ms (min) after +5 V and +12 V power are normal, an external signal source, or the H780 power supply in PDP-11/03 systems, produces an active BDCOK H signal; the processor responds by negating BINIT, and waits for BPOK H. The BPOK H signal, produced by an external signal source or the H780 power supply, goes true (high) 70 ms (min) after BDCOK H goes high. The processor responds by executing the user-selected power-up routine (Chapter 5); if BHALT L is asserted, the console microcode is executed.

During a power-down sequence, the external signal source first negates BPOK H, causing the processor to execute the power-fail trap (PC at 024, PS at 026).

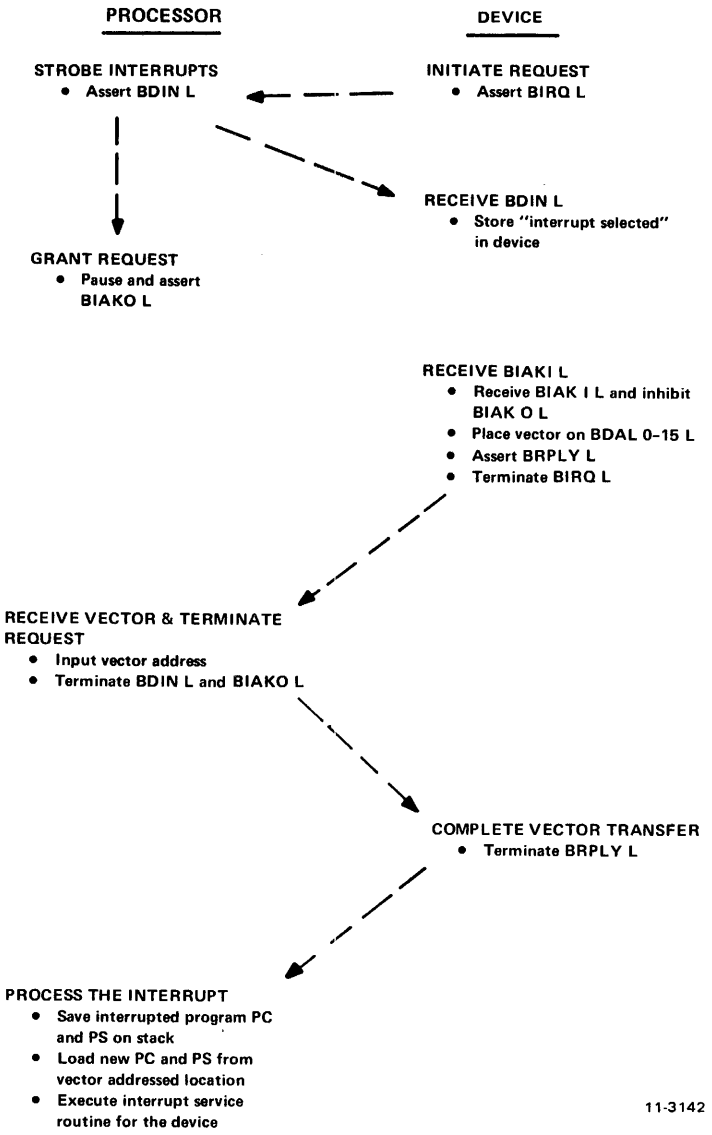


Figure 3-8 Interrupt Request/Acknowledge Sequence

Approximately 3 ms (max) later, the processor initializes the bus by asserting BINIT L in response to the external signal negation of BDCOK H.

3.10 HALT MODE

The BHALT L bus signal can be asserted low to place the processor in the Halt mode. When in the Halt mode, the RUN indicator (PDP-11/03 only) is extinguished, interrupts external to the processor module are ignored, and the processor executes the console ODT microcode. Although the user could assert this line by a separate switch or a custom module, it is normally asserted by the HALT/ENABLE switch (PDP-11/03 only) or the user-designated device's SLU interface module when the Framing Error Halt is enabled (Paragraph 6.2.2.8). Note that when in the Halt mode, the processor arbitrates DMA requests, and refresh operations. Thus, in addition to bus transactions between the processor and the console device, bus transactions can occur for DMA and refresh.

3.11 MEMORY REFRESH

Memory refresh operations are required when any dynamic MOS memory devices are used in a system. These memory devices are included on KD11-F and MSV11-B modules. Memory refresh is normally controlled by the processor microcode, which is automatically executed once every 1.6 ms. However, refresh

could be controlled by a user-supplied DMA device on the bus. (For example, when used in an intelligent terminal application, the refresh logic could be included on the user's DMA interface module.)

A complete refresh operation requires 64 BSYNC/BDIN transactions which must be completed within 2 ms. The processor (or other device controlling the refresh operation) first asserts BREF L for each BSYNC/BDIN transaction during the addressing portion of each refresh operation. BREF L causes all dynamic MOS memory devices to be simultaneously enabled and addressed, overriding local bank selection circuits. Refresh is then accomplished by executing 64 BSYNC/BDIN transactions, in a manner similar to the DATI bus cycle, incrementing the "row" address (bits 1—6) once for each transaction. Address bit 0 is not significant in the refresh operation. When refresh is controlled by processor microcode, the operation takes approximately 130μs.

Note that only one dynamic MOS memory device is required to assert BRPLY L during the refresh BSYNC/BDIN transactions. This should be performed by the slowest device on the bus. MSV11-B modules each contain a jumper which the user can insert to prevent the module from asserting BRPLY L during refresh operations. The slowest memory device will normally be the MSV11-B module located the greatest electrical distance from the processor module along the bus.

3.12 BUS SPECIFICATIONS

Electrical

Refer to electrical specifications listed in Paragraph 2.9.

NOTE

All bus lines are open-collector, resistor-terminated to a 3.4 V nominal.

Bus Drivers and Receivers

Recommended Bus Drivers

Type 957, P/N DEC 8881-1, quad 2-input NAND gates (Refer to specifications in the Hardware/Accessories Catalog.)

Recommended Bus Receivers

Type 956, P/N DEC 8640, quad 2-input NOR gates (Refer to the specifications in the Hardware/Accessories Catalog.)

Recommended Bus Transceivers

Type DEC 8641, quad unified bus transceiver.

3.13 BUS CONFIGURATIONS

In the following descriptions, a unit load is equal to one bus receiver and two bus drivers and less than 10 pF of circuit board etch. Bus terminations are shown in Figure 3-9.

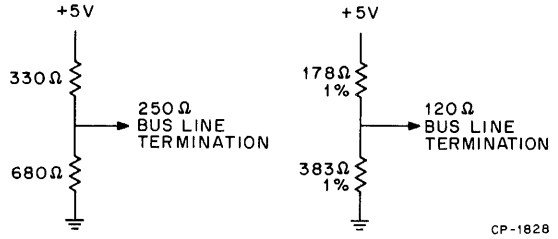


Figure 3-9 Bus Line Terminations

Minimum Configuration (Figure 3-10)

1. The processor terminates the bus lines to Zt = 250 Ω.
2. Ten-inch maximum backplane wire (each bus line for a 4 by 4 backplane), 6 unit loads or less.

Intermediate Configuration (Figure 3-11)

1. The processor terminates the bus lines to Zt = 250 Ω.

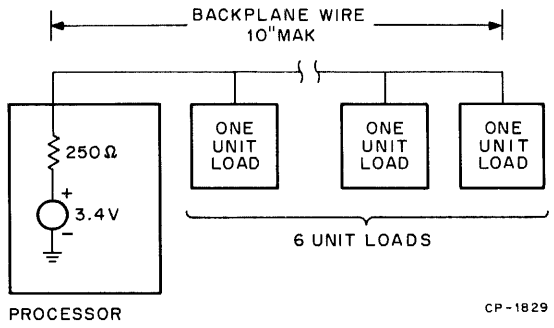


Figure 3-10 Minimum Configurations

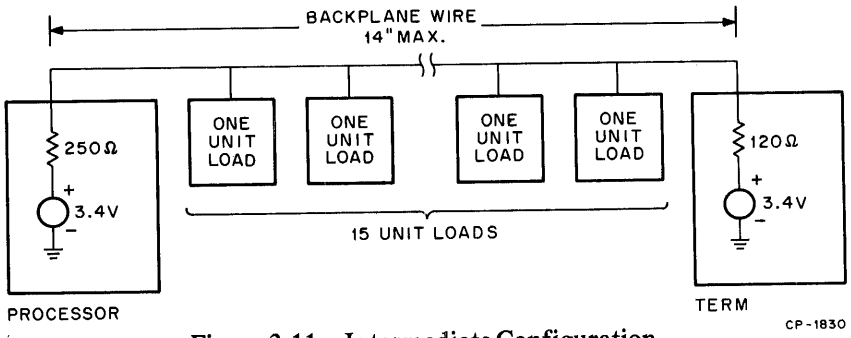


Figure 3-11 Intermediate Configuration

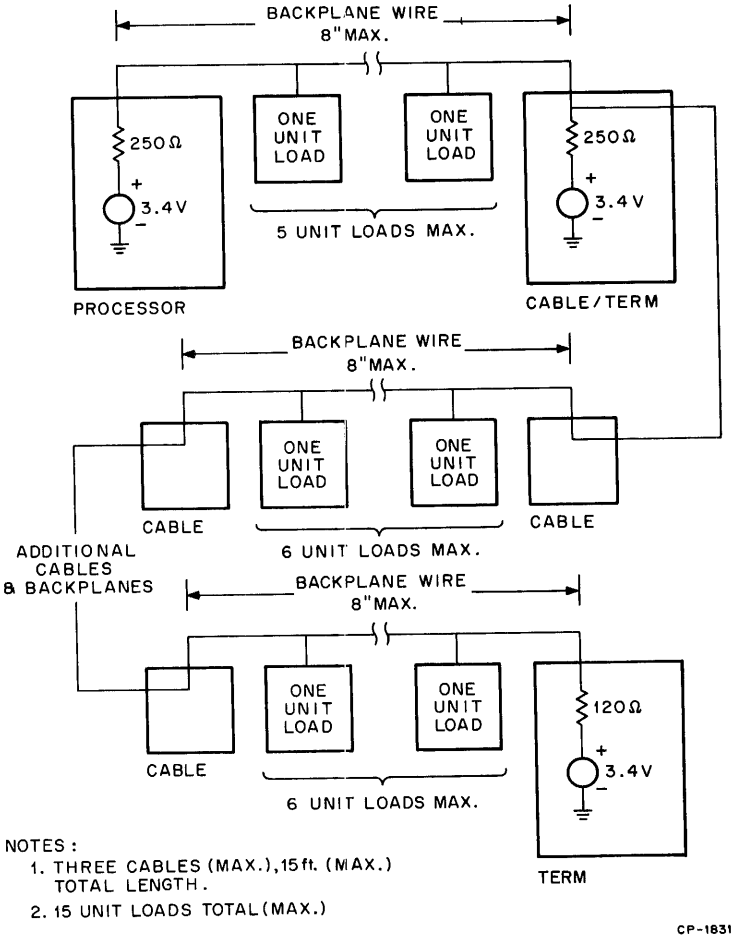


Figure 3-12 Maximum Configuration

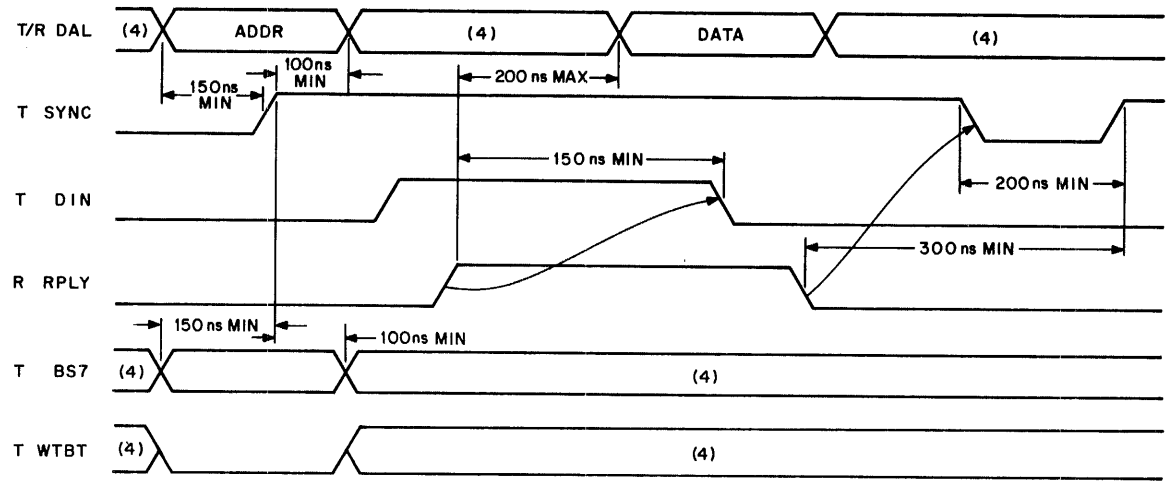
2. Fourteen-inch maximum backplane wire (each bus line for a 9 by 4 backplane), 15 unit loads or less.
3. An additional 120 Ω termination is required.

Maximum Configuration (Figure 3-12)

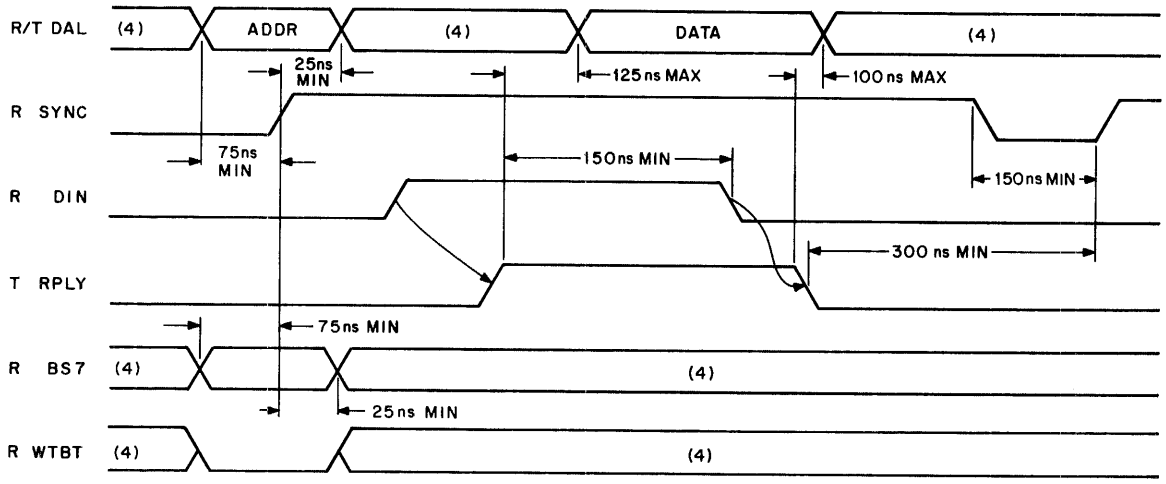
1. The processor terminates the bus lines to Zt = 250 Ω .
2. Eight-inch maximum backplane wire on each backplane (each bus line for 4 by 4 backplanes); 6 unit loads maximum each backplane, 15 unit loads total (maximum); daisy-chained on 2 ft (minimum) 120 Ω cable, three cables maximum, total cable length not exceeding 15 ft.
3. Two additional terminations (one 250 Ω and one 120 Ω) are required.

3.14 BUS SIGNAL TIMING

Bus signal timing requirements at master and slave devices are shown in Figures 3-13 through 3-18.



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

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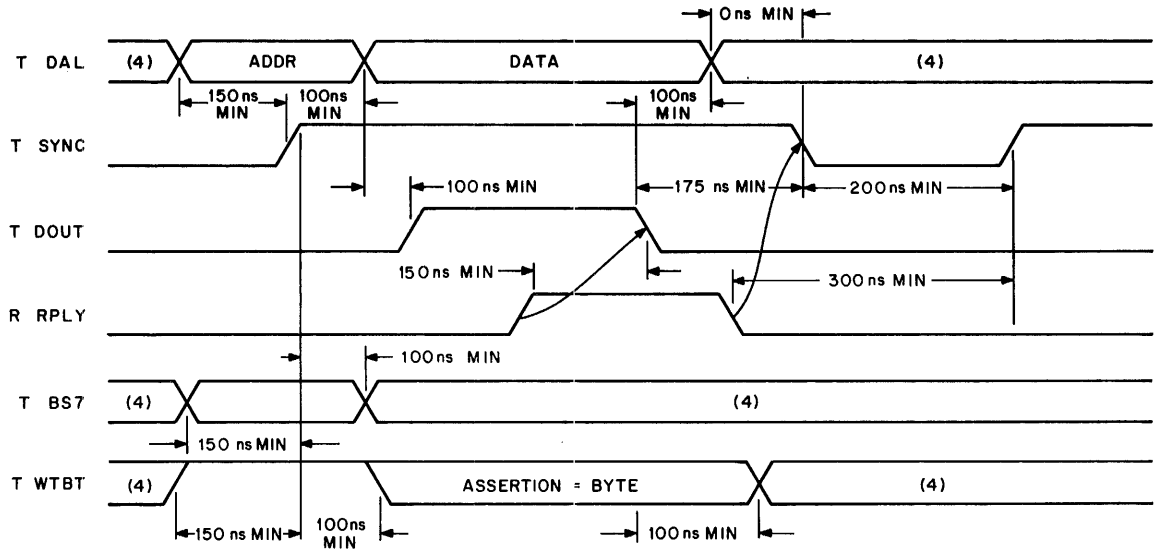
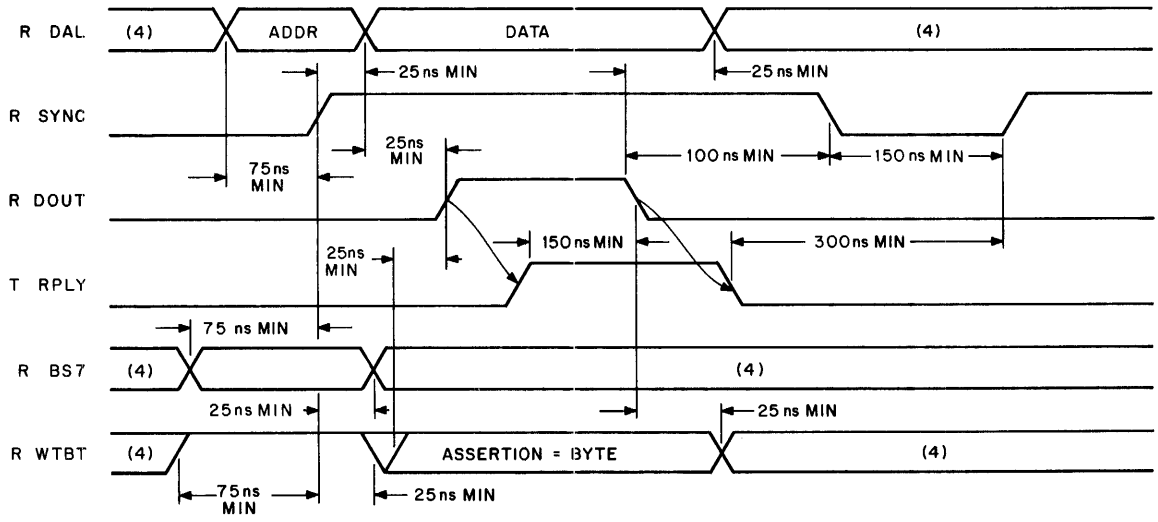
Figure 3-13 DATI Bus Cycle Timing



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

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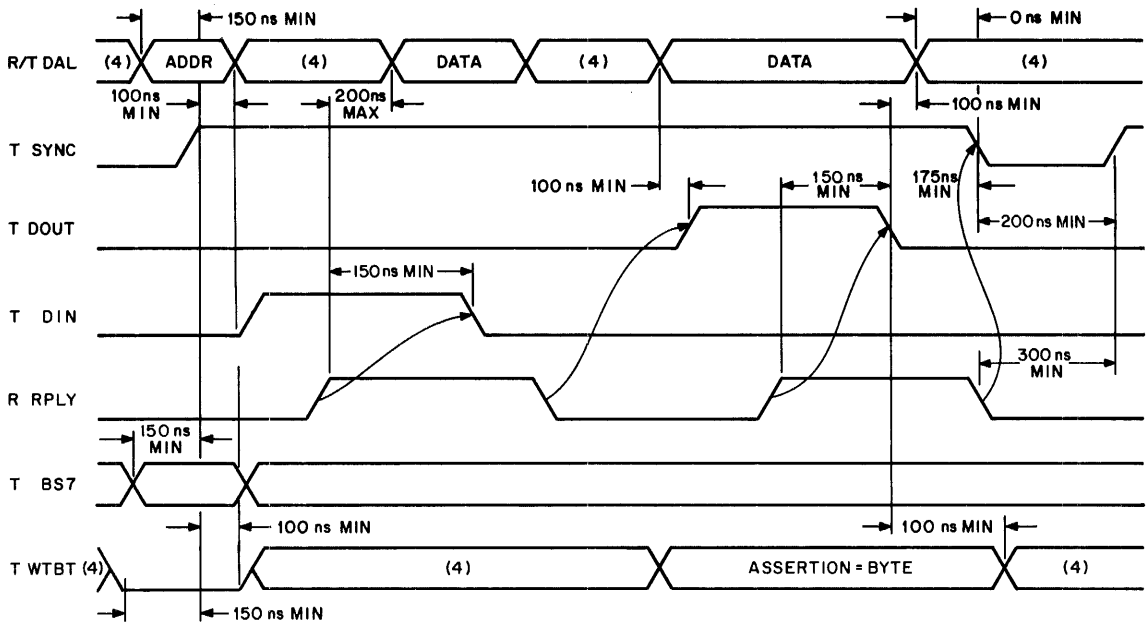
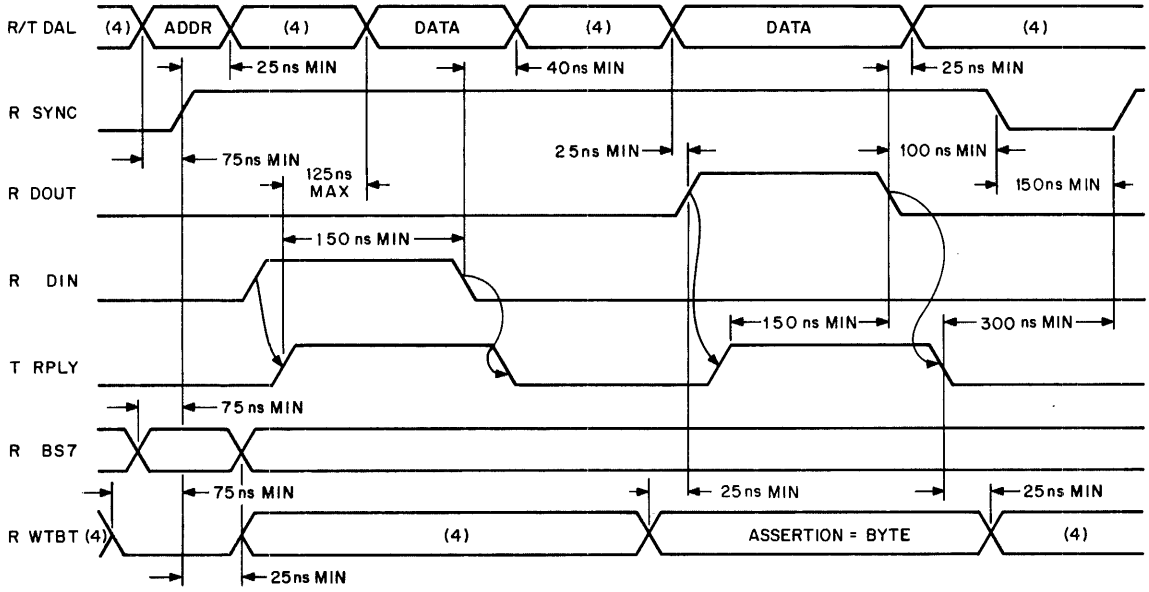
Figure 3-14 DATO or DATOB Bus Cycle Timing



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Requesting Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

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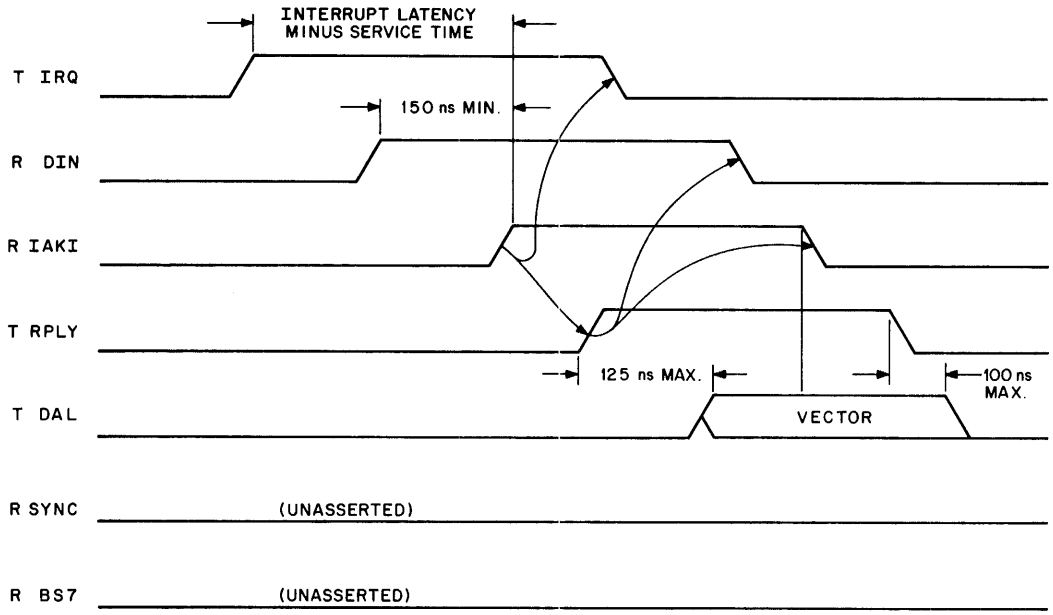
Figure 3-15 DATIO Bus Cycle Timing



NOTES:
1. Timing shown at Requesting Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal Name Prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.

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Figure 3-16 Interrupt Transaction Timing

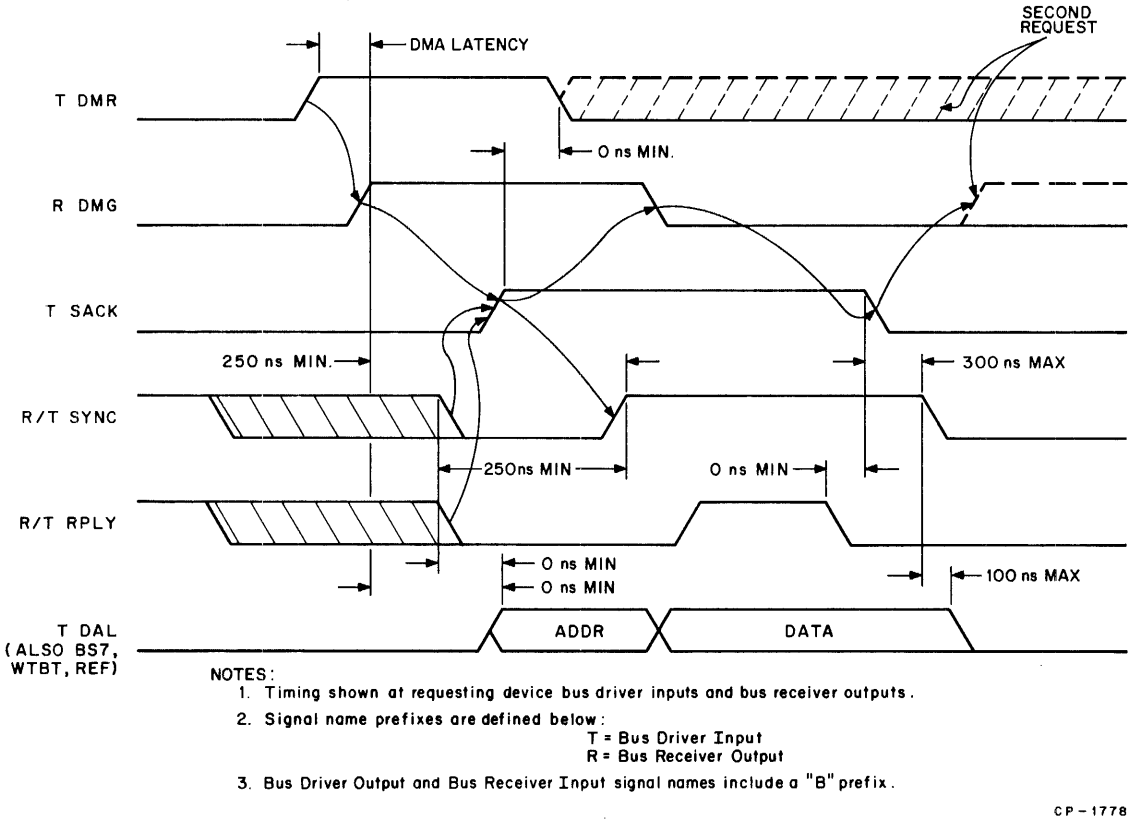


Figure 3-17 DMA Request/Grant Timing

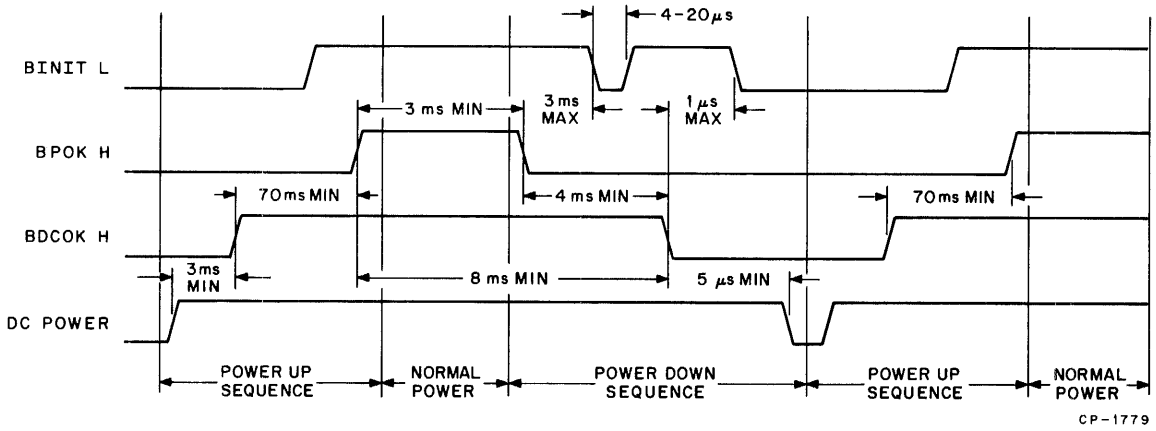


Figure 3-18 Power-Up/Power-Down Timing

CHAPTER 4
LSI-11 MODULE DESCRIPTIONS

4.1 GENERAL

This chapter contains detailed descriptions of each LSI-11 module. The level of coverage is sufficient to enable users to interface their systems with the PDP-11/03 or LSI-11 using standard LSI-11 modules or user-designed interfaces. Refer to Chapter 3 for detailed bus timing information.

LSI-11 modules covered in this chapter are listed in Table 4-1. Note that a separate description for the KD11-J microcomputer is not provided; it comprises the same M7264 module as the KD11-F microcomputer, except that a resident semiconductor memory is not supplied. Instead, the MMV11 core memory module is supplied with the KD11-J option.

Table 4-1
LSI-11 Modules

Option	Module Number	Module Option	Description Para. No.
KD11-F	M7264	LSI-11 microcomputer and 4K semiconductor memory	4.2
KD11-J	M7264-YA, H223, G653	LSI-11 microcomputer and 4K core memory	4.2
KEV-11	—	EIS/FIS processor chip	4.2
MMV11-A	H223, G653	4K by 16-bit core memory	4.3
MRV11-A	M7942	4K by 16-bit PROM	4.4
MSV11-B	M7944	4K by 16-bit dynamic read-write memory	4.5
MSV11-A	M7943	1K by 16-bit static read-write memory	4.6
DLV11	M7940	Serial line unit	4.7
DRV11	M7941	Parallel line unit	4.8
H780-A and H780-B		Power Supply	4.9

4.2 KD11-F MICROCOMPUTER

4.2.1 General

The KD11-F microcomputer is contained on a single 8.5 by 10 inch printed circuit board (M7264). The module includes all basic microcomputer functions common to both the KD11-F and KD11-J microcomputers and a resident 4K by 16-bit semiconductor read/write memory. KD11-F functions are shown in Figure 4-1. KD11-F microcomputers features are given in Paragraph 2.3.

NOTE

The following description reflects the circuits shown in drawing CS M7264 Rev. E.

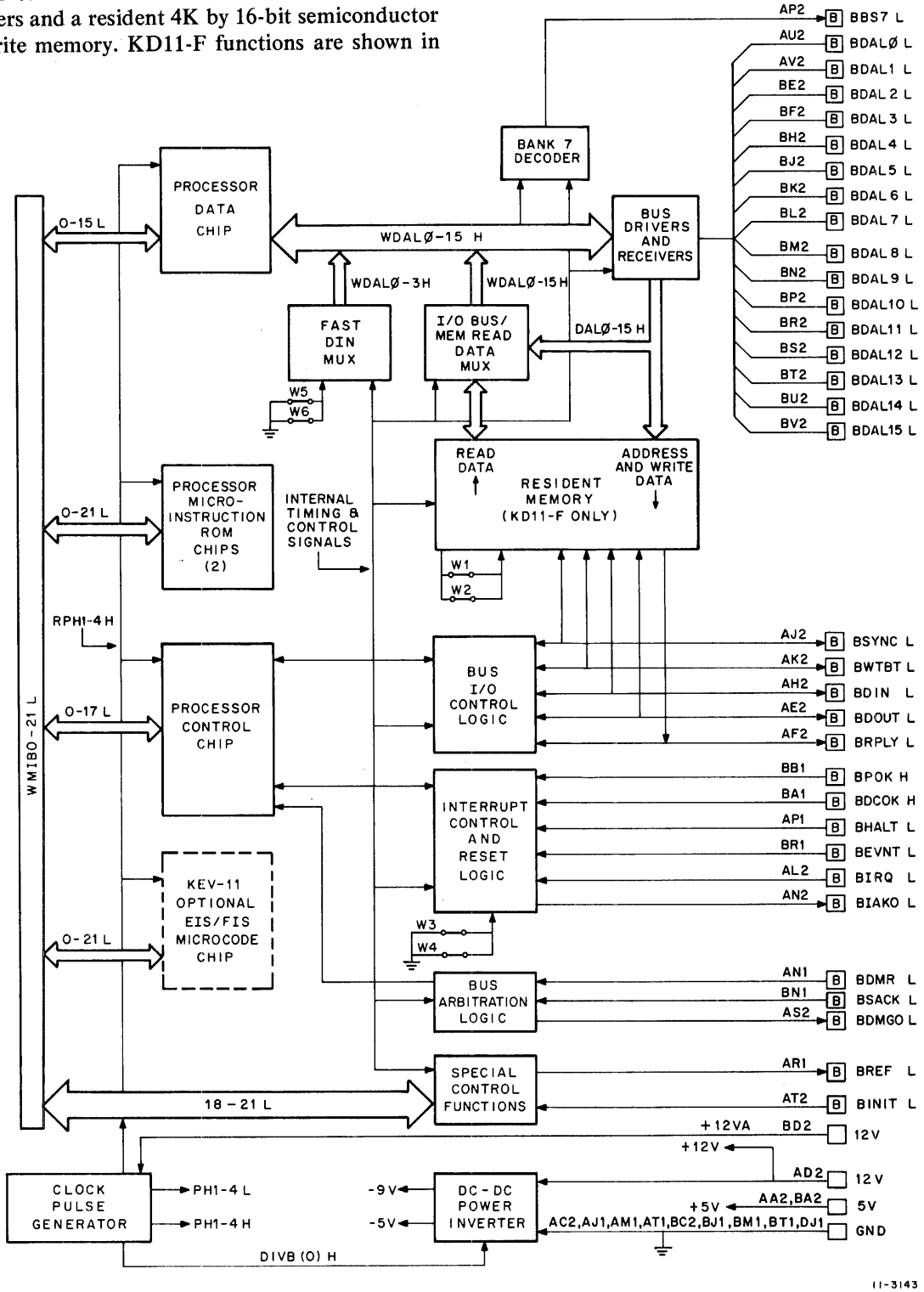


Figure 4-1 KD11-F Microcomputer Logic Block Diagram

4.2.2 Basic Microcomputer Functions

Basic functional blocks of the LSI-11 microcomputer are shown in Figure 4-1 and described in the following paragraphs. The KD11-F's resident memory is described separately (Paragraph 4.2.3).

4.2.2.1 Microprocessor Chip Set — The main function contained on the processor module is the microprocessor chip set. This chip set includes a control chip, a data chip, and two microinstruction ROM chips (microms). In addition, an optional KEV-11 microm that contains EIS/FIS microcode can be installed on the module. Microprocessor chips communicate with each other over a special 22-bit microinstruction bus, WMIB0-21 L. All address and data communication between the microprocessor chips and other processor module functional blocks is via the data chip and the 16-bit data/address lines, WDAL0-15 H (from the data chip).

Processor module control signals interface with the microprocessor chips via the control chip. Eight input and five output microprocessor control signals provide this function.

Timing and synchronization of all microprocessor chips (and all processor module functions) are controlled by four nonoverlapping clock generator signals (Paragraph 4.2.2.2). Typical operating speed is approximately 360 ns (90 ns each phase), based on an 11.1 MHz oscillator signal.

The control chip generates a sequence of microinstruction addresses which access the microinstruction microm chips. The addressed microinstruction is then transferred to the data and control chips. Most of the microinstructions are executed by the data chip; however, various jumps, branches, and I/O operations are executed in the control chip.

The data chip contains the data paths, logic, arithmetic logic unit (ALU), processor status bits, and registers that are most familiar to PDP-11 and LSI-11 users. Registers include the eight general registers (R0—R7) and an instruction register. The user's program has access to all general registers and processor status (PS) bits. All PDP-11 instructions enter this chip via the WDAL bus. Data and addresses to and from the microprocessor are also transferred to and from the processor over this 16-bit bus.

CAUTION

Do not remove processor chips from their sockets. Improper handling could permanently damage the chips.

4.2.2.2 Clock Pulse Generator — The clock pulse generator produces four nonoverlapping clock signals for processor timing and synchronization. A voltage-controlled oscillator generates a basic CK H signal, ranging from 10 to 13 MHz (10 MHz is nominal).

Maintenance clock gates receive and distribute the basic CK H signal to a two-stage counter and an RC filter circuit. The two-stage counter outputs are decoded by the four-state decoder, producing the basic four nonoverlapping clock phases. The pulse produced on the leading edge of each basic clock pulse inhibits the decoder for 10 ns, preventing the overlap of each phase. Each of the four phase signals (RPH1 through RPH4) are positive-going, MOS-compatible 100 ns (nominal) pulses which are bused to each of the microprocessor chips through resistors. PH1 L through PH4 L and PH1 H through PH4 H are similarly timed; however, they are TTL-compatible for distribution elsewhere on the module.

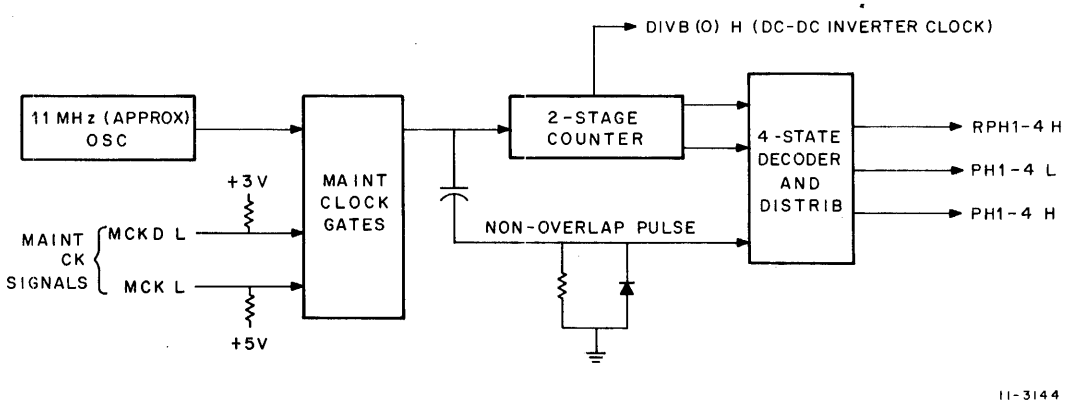


Figure 4-2 Clock Pulse Generator

4.2.2.3 Bus Interface and Data/Address Distribution — All LSI-11 processor module communication to and from external I/O devices and memories is accomplished using the LSI-11 bus 16-bit data/address lines (BDAL0-15 L) and bus control signals. The processor module interfaces to the bus using bus driver/receiver chips, as shown in Figure 4-3. Each DEC 8641 chip contains four open-collector drivers and four high-impedance receivers. Each driver output is common to a receiver input. Hence, either processor output data (from the driver outputs) or input data (from the bus) can stimulate bus receiver inputs.

Note that all four drivers in a chip are enabled or disabled by a pair of DRIVER ENABLE L inputs. A high input will inhibit all four drivers; when both enable inputs are low, the drivers are enabled and output data is gated onto the bus. Signals which control bus drivers include EDAL L, INIT (1) H, and DMGCY H. False states enable certain control signals which are described later.

EDAL L is a control signal which enables the 16-bit data/address bus drivers. When in the active state, EDAL L gates WDAL0—15 H onto the BDAL0—15 L bus.

EDAL L is generated by the logic shown in Figure 4-4. During a processor-controlled address/data output bus cycle, or during the addressing portion of a processor-controlled input bus cycle, SACK L and DMG(1) L are passive (high). The passive signals are gated, producing a low (passive) DMGCY H signal. This signal is inverted and gated with the passive DIN L signal, producing the active EDAL L signal. During a DMA cycle in which data in the processor module's resident 4K memory is to be read by a DMA device, BANK OR REF H goes high; this signal is gated with DINR H and DMG CYCLE H to produce the active EDAL L signal.

DMGCY H and INIT (1) H are processor module logic control signals which inhibit certain bus drivers during an Initialize or DMA operation. Bus drivers are enabled when these signals are in the false (low) state.

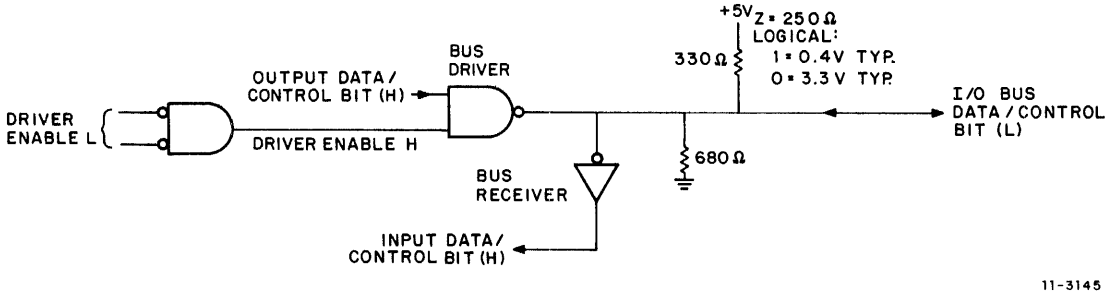


Figure 4-3 LSI-11 Bus Loading and Driver/Receiver Interface

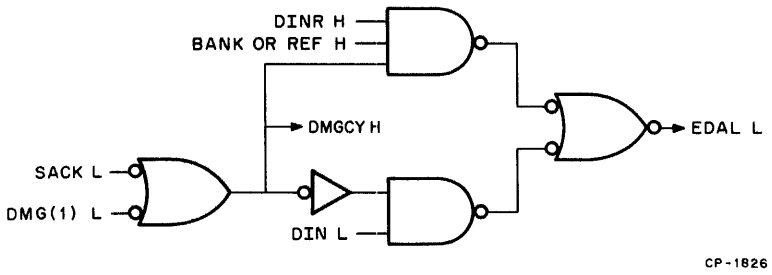


Figure 4-4 EDAL L Logic

A list of bus driver output signals and their respective enable signals is provided below.

Bus Driver (Signal)	Enable Signal(s) (Low=Enable)
BDAL0-15 L	EDAL L
BSYNC L BBS7 L BREF L BIAKO L	INIT (1) H, DMGCY H
BDMG L BRPLY L BDIN L BDOUT L	INIT (1) H
BWTBT L BINIT L	Always enabled

The near-end bus termination resistors are contained on the processor module. Each bus driver output is terminated by a pair of resistors, as shown in the figure, establishing the nominal 250 Ω bus impedance and the 3.4 V nominal voltage level. No additional terminations are required for bus-compatible devices connected to the same backplane.

Address and data information are distributed on the processor module via the WDAL0-15 H and DAL0-15 H 16-bit buses. WDAL0-15 H interface directly with the microprocessor's data chip, the DEC 8641 bus drivers, and the I/O bus/memory read data multiplexer. All processor input data from the I/O bus is via the bus receivers, the DAL0-15 H bus, the data multiplexer, the WDAL0-15 H bus, and the microprocessor's data chip. Resident memory data input is discussed later.

4.2.2.4 Bus I/O Control Signal Logic — Bus I/O control signals include BSYNC L, BWTBT L, BDIN L, BDOUT L, and BRPLY L. In addition, BIAKO L can be considered a bus I/O control signal; however, since it is only used during the interrupt sequence, it is discussed in Paragraph 4.2.2.6. Logic circuits which produce and/or distribute these signals are shown in Figure 4-5. Each signal is generated or received as described in the following paragraphs.

BSYNC L — The control chip initiates the BSYNC L signal sequence by raising WSYNC H during PH2. Inverters apply the high SYNC H signal to the Sync flip-flop D input. On the trailing edge of PH3 L, the Sync flip-flop sets, producing an active (high) SYNC (1) H input to the BSYNC L bus driver. SYNC (1) H is gated with REPLY (1) H (when active) to produce a direct preset input to the Sync flip-flop. This ensures that BSYNC L will remain active until after the bus slave device terminates its BRPLY L signal and the Reply flip-flop is reset. [REPLY (1) H is low.] The Sync flip-flop then clocks to the reset (BSYNC L passive) state on the trailing edge of PH3 L.

BWTBT L — BWTBT L is the buffered/inverted control chip WWB H output signal. This signal asserts during PH1 of the addressing portion of a bus cycle to indicate that a write (output) operation follows. It remains active during the output data transfer if a DATOB bus cycle is to be executed.

BDIN L — BDIN L is the inverted, buffered control chip's WDIN H signal. This signal goes active during PH2 following an active RPLY H signal.

BDOUT L — The control chip initiates the BDOUT L signal sequence by raising WDOUT H during PH2. This signal is gated with the passive REPLY (1) L (high) signal to produce an active low D input to the DOUT flip-flop. The flip-flop sets on the leading edge of PH3 H, producing an active BDOUT L signal. It clocks to the reset state on PH3 following the REPLY (1) L active (low) signal.

BRPLY L — BRPLY L is a required response from a bus slave device during input or output operations. DIN L and DOUT (1) L are ORed to produce an active I/O L signal whenever a programmed transfer occurs. I/O L enables the time-out counter in the bus error detection portion of the interrupt logic. I/O L is inverted to produce I/O H, which enables the reply gate REPLY H signal input to the control chip.

BRPLY L is received either from the LSI-11 bus or resident memory and inverted to produce a high input to the Reply flip-flop. PH1 H clocks the flip-flop to set state, producing active REPLY (1) H and REPLAY (1) L signals. REPLY (1) L is ORed with DMR (1) L to produce an active BUSY H signal. The processor's control chip responds by entering a wait state, inhibiting completion of the processor-generated bus transfer for the duration of REPLY (1) L. REPLY (1) H is gated with I/O H to produce an active REPLY H signal, informing the processor that the output data has been taken or that input data is available on the bus. REPLY H goes passive when I/O H goes passive. The bus slave device will then terminate the BRPLY L signal, indicating that it has completed its portion of the data transfer. On the next PH1 H clock pulse, the Reply flip-flop resets and REPLY (1) H and L and BUSY H go passive.

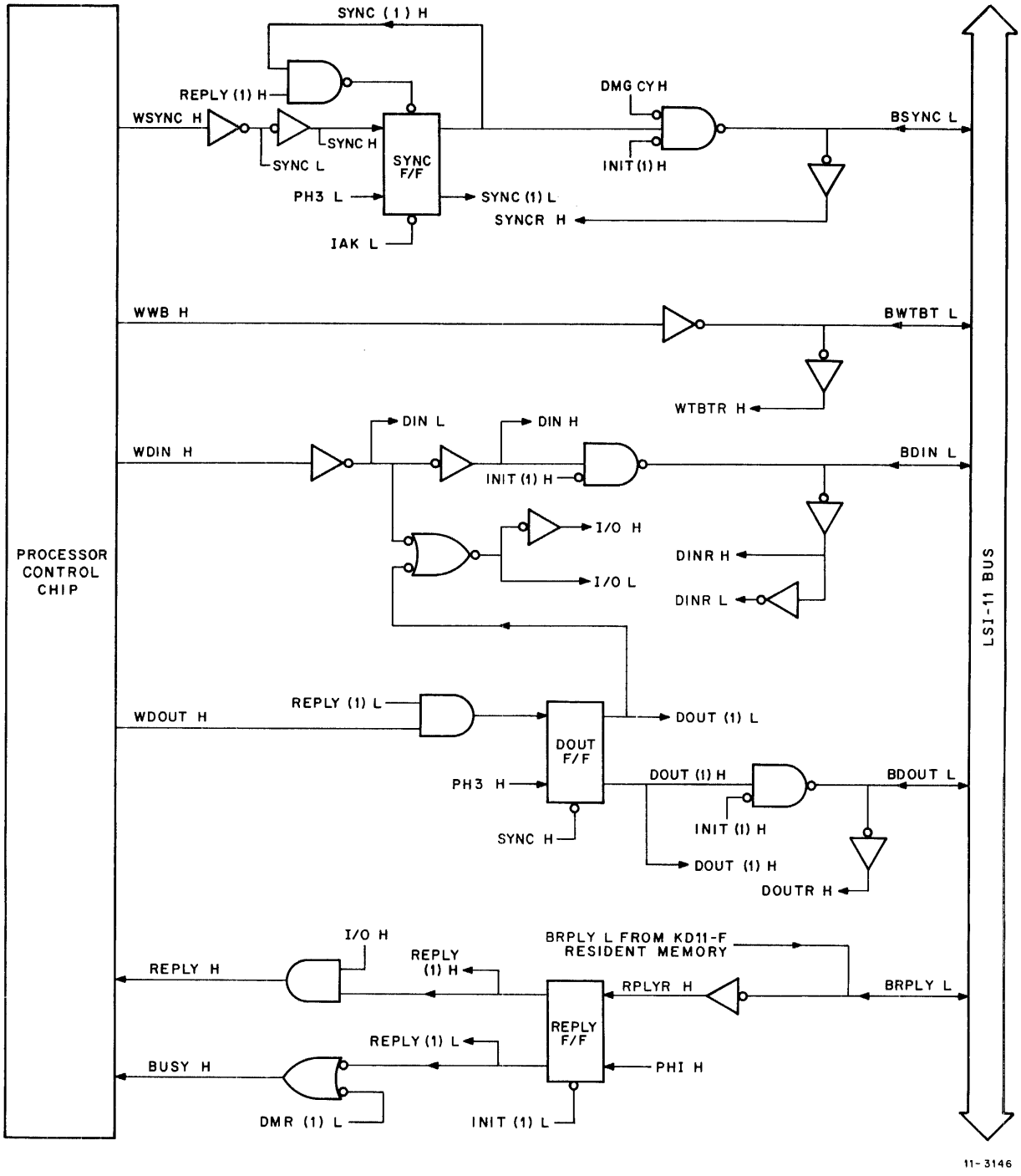


Figure 4-5 Bus I/O Control Signal Logic

4.2.2.5 Bank 7 Decoder — The bank 7 decode circuit is shown in Figure 4-6. Buffers receive WDAL0-15 H bits and distribute them to the bank 7 decoder and BDAL bus drivers. Bank 7 is decoded during the addressing portion of the bus cycle. If a peripheral device address is referenced, an address in bank 7 (28-32K address space) is used, and WDAL13, 14, and 15 H are all active (high). This address is decoded and BBS7 L is asserted. When active, BBS7 L enables addressing of nonmemory devices along the bus. During interrupt vector bus transactions, IAK L becomes asserted. IAK L inhibits WDAL15 H, preventing BBS7 L signal generation, which could result in an invalid input data transfer.

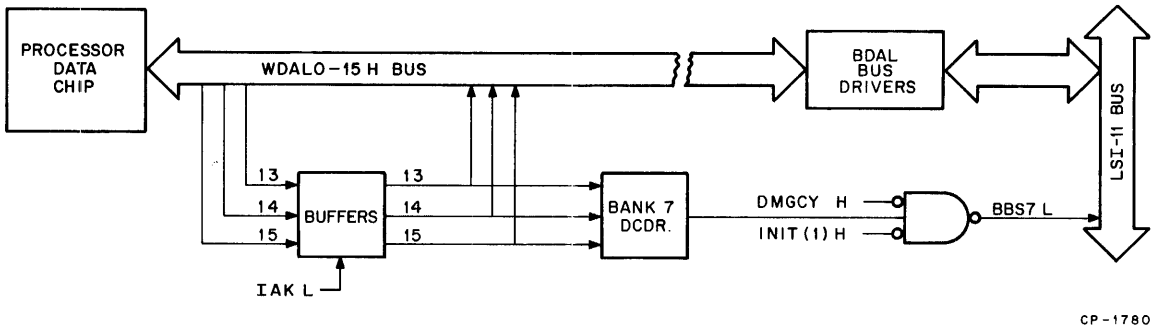


Figure 4-6 Bank 7 Decoder

4.2.2.6 Interrupt Control and Reset Logic — Interrupt control and reset logic functions are shown in Figure 4-7. Reset functions include bus error and power-fail (BDCOK H negated). Interrupt functions include power-fail (impending), Halt mode (console microcode control), refresh interrupt, event (or line time clock) interrupt, and external BIRQ interrupts. The various functions are described in the following paragraphs.

Power-Fail/Restart Sequence— A power-fail sequence is initiated when BPOK H goes low, clocking the Power-Fail flip-flop to the set state. PFAIL (1) L is ORed with HALT L to produce a high signal. This signal is latched during PH3 H, producing an active IPIRQ H (interrupt 1) input to the processor control chip. The processor then interrupts program execution. Note that the low (passive) BPOK H signal is inverted to produce an active PFAIL H input to the fast DIN multiplexer; this signal status is checked by the microcode to ensure that BPOK H is asserted.

Upon entry to this microcode routine, the processor requests a fast DIN cycle. This request is decoded as ROM CODE 5 L, presetting the fast DIN flip-flop. FDIN (0) H goes low, enabling the fast DIN multiplexer to place start-up microcode option jumper data, the passive time-out error [TERR (1) H] signal, and the active PFAIL H signal on WDAL0-3 H. The processor receives the fast DIN information via the data chip. An active PFAIL H signal informs the processor that a power-fail condition is in progress, rather than the halt condition.

If the power failure continues, BDCOK H goes passive (low) and produces an active DC LO L signal, clearing the Power-Fail flip-flop and the power-fail/halt and reset latches and initializing the processor and all devices (Paragraph 4.2.2.1). The active RESET L signal then initializes the processor, causing it to abort console (halt) or power-fail microcode execution and enter a "no operation" state. The processor remains in this condition until BDCOK H returns to the active state.

The power-up restart condition occurs when DC LO L goes false; RESET L goes passive (high) on the next PH2 H clock pulse. The processor responds by executing a fast DIN cycle to determine the start-up microcode option jumper configuration. Once the fast DIN cycle has been completed, the processor executes the power-up option selected, and normal operation resumes when BPOK is asserted.

Halt Mode — The Halt mode is entered either by executing the HALT instruction or by a device asserting the BHALT L signal. The processor halts program execution and enters microcode execution as described for a power-fail operation. However, when the processor executes the fast DIN cycle, the PFAIL H bit (WDAL3 H) is not active and console microcode (not a power-fail sequence) is executed. Negation of BHALT L will allow the processor to resume PDP-11 program execution. On the next PH2 H clock pulse, IPIRQ H goes false (low) and the processor Run mode is enabled.

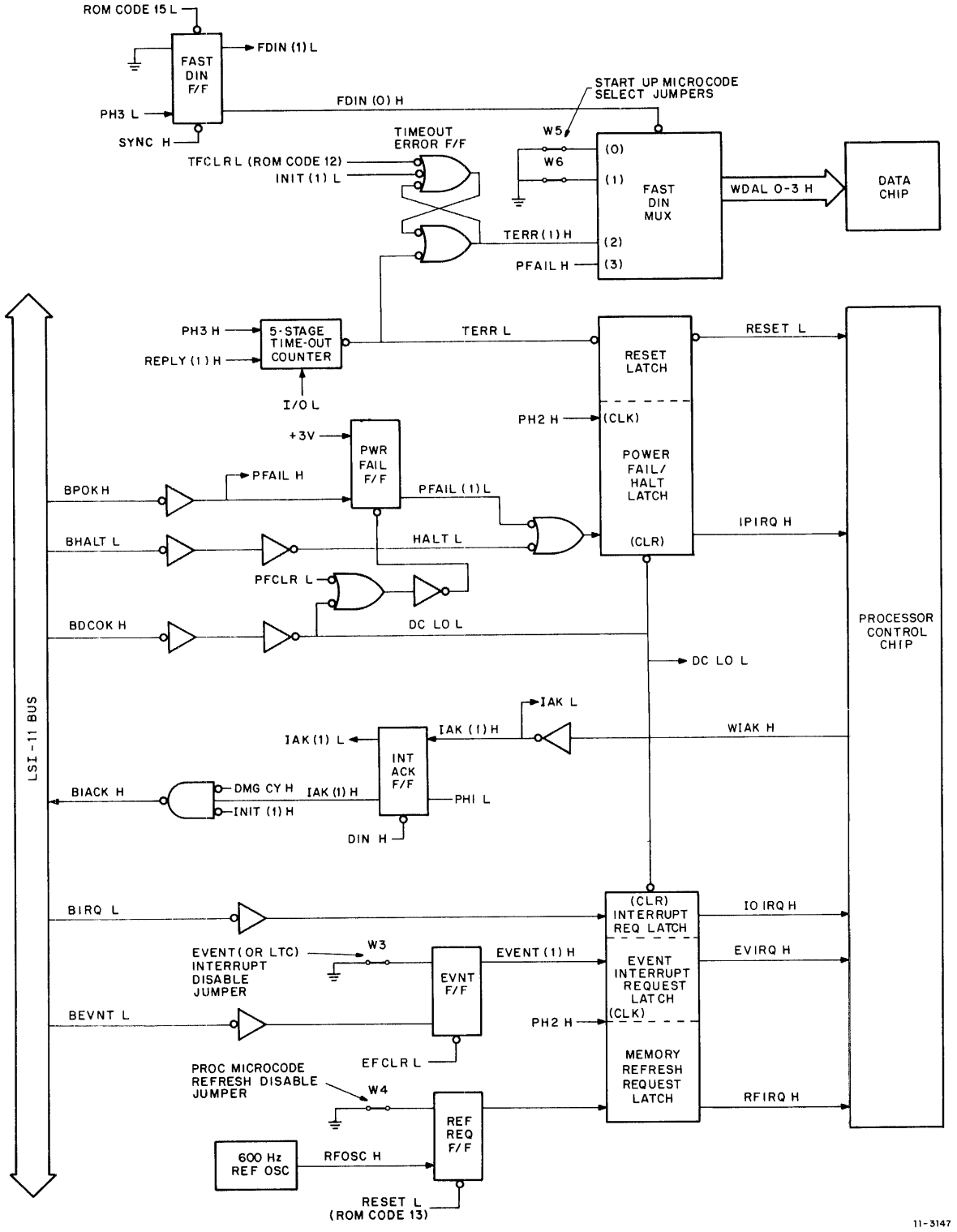


Figure 4-7 Interrupt Control and Reset Logic

Bus Errors — A bus error results in aborting program execution and entry into a trap service routine via vector location 004. A bus error occurs when a device fails to respond to the processor's DBIN L or BDOUT L signal by not returning a BRPLY L signal within 10 μs (approximately). An active I/O signal inhibits the reset input of the 5-stage time-out counter, enabling counter operation. [When not in a processor-controlled bus I/O cycle, I/O L is passive (high), clearing the counter.] The counter proceeds with counting PH3 H

clock pulse signals. Normally BRPLY L would be asserted, producing an active REPLY (1) H signal which inhibits the counter; the count would remain stable until cleared by a passive I/O L signal. However, if BRPLY L is not received within 10 μs, the full count (32_{10}) is attained. This is the error condition; TERR L goes low and TERR (1) H goes high. The next PH2 H clock pulse clocks the reset latch to the reset (active) state, producing an active RESET L signal. The processor responds by executing the reset microcode. After entering the microcode, the processor executes a fast DIN cycle and determines that a time-out (bus) error TERR (1) H, rather than a power-fail condition, has occurred. It then responds by executing the bus error trap service routine. TFCLR L (ROM code 2) is generated by the processor to clear the TERR latch.

Normal I/O Interrupts — "Normal" I/O interrupts are those interrupt requests which are generated by external devices using bus interrupt request BIRQ L. The request is initiated by asserting BIRQ L. This signal is inverted to produce a high signal, which is stored in the interrupt request latch on the next PH2 H pulse. The stored request produces IOIRQ H, which informs the processor of the request. If processor status word priority is 0, the processor responds by producing an active WIAK H (interrupt acknowledge) and WDIN H signals. WDIN H is buffered onto the BDIN L signal line to signal devices to stabilize their priority arbitration. WIAK H is inverted, producing IAK L, setting the Interrupt Acknowledge flip-flop on the trailing edge of PH1 L one cycle after BDIN L is asserted. The high (active) interrupt acknowledge signal is enabled onto the BIAKO L signal line by passive (low) DMGCY H and INIT (1) H signals. The highest priority device requesting interrupt service responds to the processor's BDIN L and BIAK L signals by placing its vector on the BDAL bus and asserting BRPLY L, inputting its vector to the processor. Note that BSYNC L is not asserted during this operation and that no device addressing occurs. The device also clears its BIRQ L signal. The processor responds to BRPLY L by terminating BDIN L and BIAK L.

Refresh — Memory refresh is initiated by a 600 Hz refresh oscillator. This function is enabled when jumper W4 is not installed. The leading edge of RFOSC H clocks the Refresh Request flip-flop to the set state. On the next PH2 H clock pulse, the memory refresh request latch stores the request and applies an active RFIRQ H signal to the processor's control chip. The processor responds by producing an active RF SET L signal and executing the refresh microcode. RF SET L sets the Refresh flip-flop, producing the BREF L signal (Paragraph 4.2.2.7) and clearing the Refresh Request flip-flop, which terminates the request. TFCLR L resets the Refresh flip-flop when the refresh operation is completed. Note that BREF is not asserted if DMGCY H or INIT (1) H is asserted.

Event Line Interrupt — The event line interrupt function can be used as a line time clock interrupt, or as desired by the user. This interrupt differs from the normal I/O interrupt request by being the highest priority external interrupt, and it does not input a vector in order to enter its service routine. The interrupt is initiated by the external device by asserting BEVNT L. This signal is inverted to produce a high (active) signal, which clocks the Event flip-flop to the set state. (Note that when W3 is installed, the flip-flop remains reset and the event function is disabled.) On the next PH2 H clock pulse, the event interrupt request latch stores the active EVNT (1) H signal. An active EVIRQ H signal is then applied to the control chip. If processor status word priority is 0, the interrupt will be serviced. Service is gained via vector 100_8, which is dedicated to the event interrupt. Hence, a bus DIN operation does not occur when obtaining the vector. The request is cleared by the microcode generated EFCLR L signal.

4.2.2.7 Special Control Functions — Special control functions include microcode-generated bus initialize and memory refresh operations and five special control signals which are internally on the processor module. Special control function logic circuits are shown in Figure 4-8. Microinstruction bus lines WMIB18-21 L are buffered to produce the four SROM0-3 H signals. The actual codes for the special functions are contained on SROM0-2 H; SROM3 H is always active when a special function is to be decoded, enabling the 1 of 8 decoder during PH3 H. The resulting decoded functions are described below.

ROM Code 10 — Not used.

ROM Code 11 [IFCLR and SRUN L] — This code is produced by the processor to clear the Initialize flip-flop and to assert the SRUN L signal for a RUN indicator in PDP-11/03 systems.

ROM Code 12 [TFCLR L] — This code is a trap function clear signal which clears the Refresh Request and Time-Out Error flip-flops (Paragraph 4.2.2.6).

ROM Code 13 [RFSET L] — This code is used to set the Refresh flip-flop. The active (high) flip-flop output is gated with passive (low) INIT (1) H and DMG (1) H signals to produce the active BREF L signal. The flip-flop normally resets by the microcode-generated TFCLR L signal after completing the refresh operation, or whenever a power failure occurs. (DC LO L goes active and clears the flip-flop.)

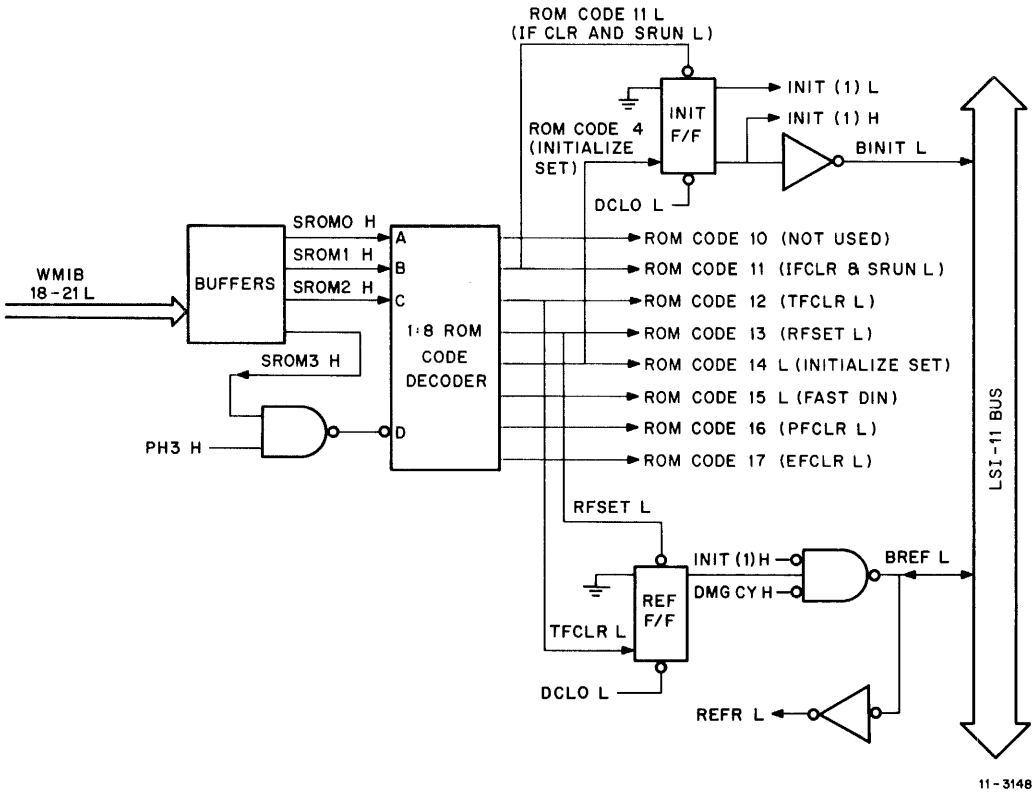


Figure 4-8 Special Control Functions

ROM Code 14 [Programmed Initialize] — A programmed LSI-11 bus initialize operation can be performed by executing the RESET instruction. The processor responds by generating ROM Code 14 L (decoded). On the positive-going trailing edge of this signal, the Initialize flip-flop clocks to the reset (active) state, producing the active initialize signal. Approximately 10μs later, the processor produces a TFCLR L signal, clearing the initialize signal.

During a power failure, the active DC LO L signal is distributed to the Initialize flip-flop clear input; when cleared, the flip-flop is in the active state and INIT (1) H, INIT (1) L, and BINIT L initialize signals are used to clear (or initialize) all LSI-11 system logic functions. When normal power resumes, the processor microcode terminates the initialize cycle by generating TFCLR L, presetting the Initialize flip-flop; this is the passive (noninitialize) or normal flip-flop state and all initialize signals return to their passive states.

ROM Code 15 [Fast DIN Cycle] — The processor generates this code when a fast DIN cycle is required. The fast DIN cycle allows the processor to read (input) the selected start-up mode, time-out error, and power fail signal status (Paragraph 4.2.2.6).

ROM Code 16 [PFCLR L] — This code clears the Power Fail flip-flop (Paragraph 4.2.2.7).

ROM Code 17 [EFCLR L] — This code clears the Event flip-flop (or line time clock interrupt request) (Paragraph 4.2.2.7).

4.2.2.8 Bus Arbitration Logic — Bus arbitration logic (Figure 4-9) enables the LSI-11 bus to be used by DMA devices or the processor. The device (or processor) controlling the bus is called the bus master. When no DMA requests are pending, the processor is bus master and all data transfers are programmed. When a DMA device is bus master, processor operation is suspended until the DMA operation is finished.

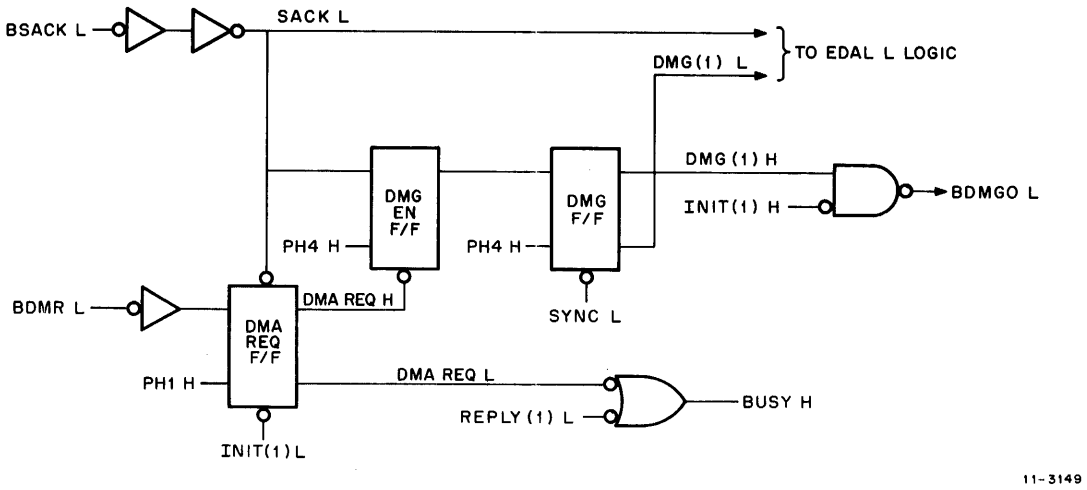


Figure 4-9 Bus Arbitration Logic

Prior to a DMA request, the DMA Request flip-flop is reset (Figure 4-10); the DMA REQ H signal is passive (low), clearing the DMG Enable flip-flop. A device initiates a DMA request by asserting BDMR L. The request is inverted to produce a high signal, which is clocked into the DMA Request flip-flop on the next PH1 H clock pulse, producing active DMA REQ H and L signals. DMA REQ L is ORed with REPLY (1) L, producing BUSY H and causing the processor to "wait" after completing its present bus cycle. On the leading edge of PH4 H, the stored DMA request sets the DMG Enable flip-flop. The processor is finished with its present bus cycle and releases the bus when SYNC L goes passive (high).

On the first PH4 H clock pulse following the passive state of SYNC L, the DMG flip-flop clocks to the set state and DMG (1) H and DMG (1) L go to their active states. DMG (1) H produces the active BDMG grant (BDMGO L) signal. DMG (1) L enables EDAL L signal generation when the DMA operation involves KD11-F resident memory. The DMA device responds to the BDMG signal by negating BDMR L and asserting BSACK L, enabling EDAL L signal generation and keeping the DMA Request flip-flop in the set state. On the first PH4 H clock phase following the active state of BSACK L, the DMG Enable flip-flop clocks to the reset state and DMG EN H goes low. The following PH4 H clock pulse clocks the DMG flip-flop

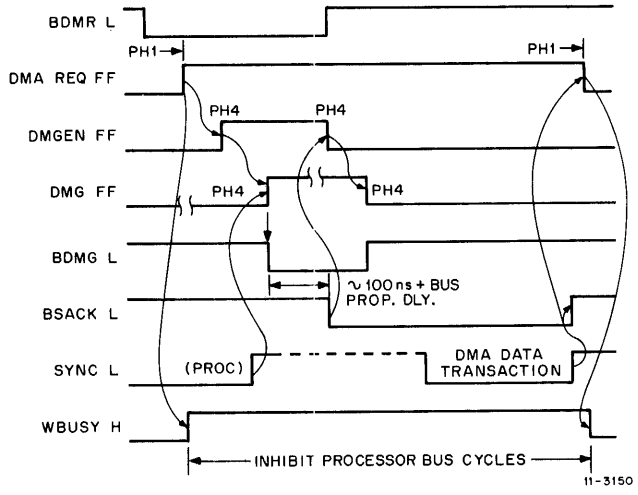


Figure 4-10 DMA Grant Sequence

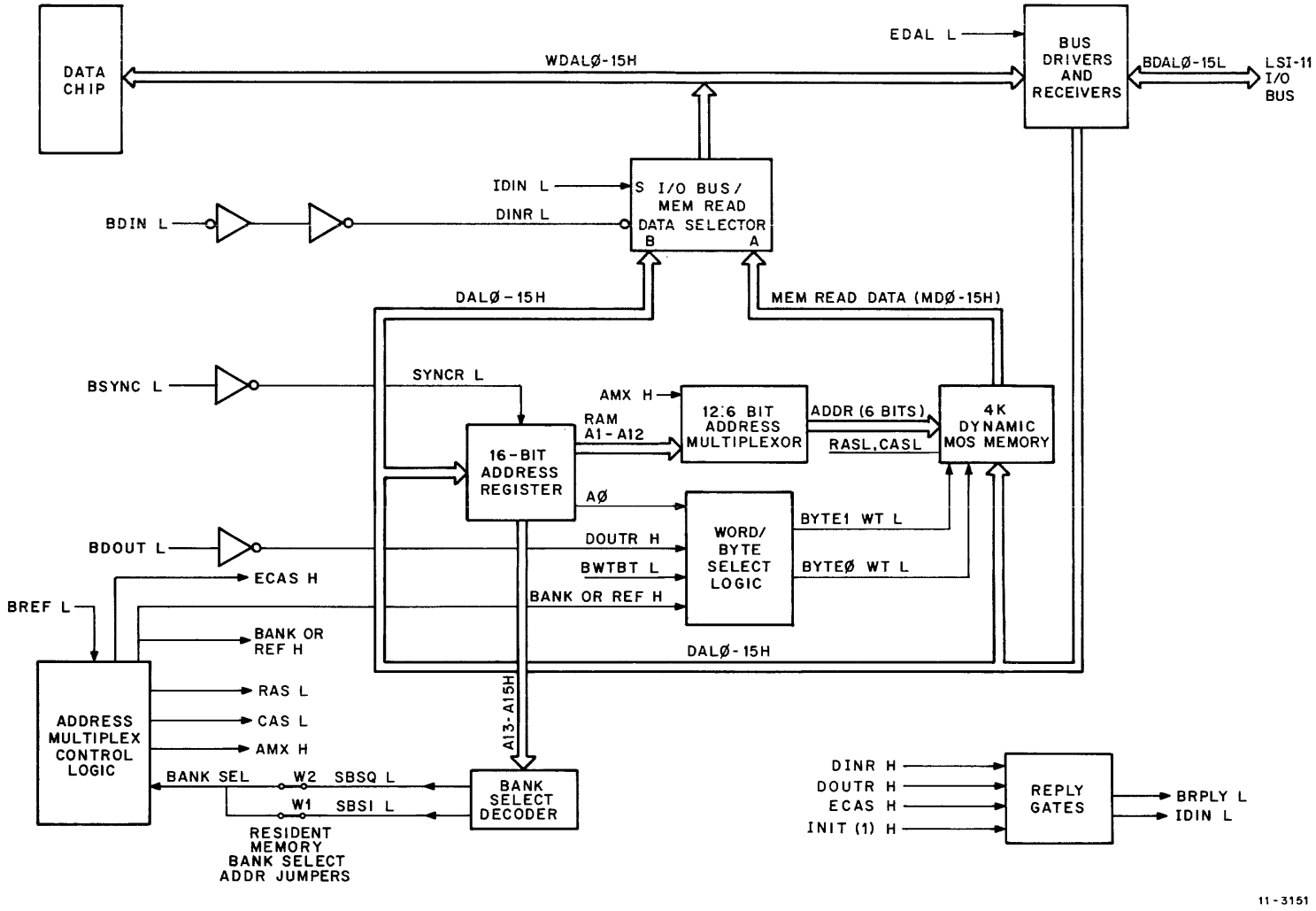


Figure 4-11 KD11-F Resident Memory

to the reset state and BDMGO L goes passive (high), terminating the DMA request/grant sequence. BSACK L remains asserted for the duration of the DMA operation, preventing new DMA requests from being arbitrated.

The DMA device releases the bus by terminating BSACK L. The following PH1 H clock pulse clocks the DMA request flip-flop to the passive state. BUSY H then goes passive, enabling a processor-initiated bus cycle. Once the processor-initiated cycle is entered, SYNC L inhibits (clears) the DMG flip-flop for the duration of the processor's present bus cycle.

4.2.3 KD11-F Resident Memory

The 4K by 16-bit dynamic MOS read/write memory is included on the KD11-F processor module only. (KDll-J basic memory is magnetic core, which is contained on a separate MMV11-A core memory unit.) Resident memory can reside in either the first or second 4K address bank. One of two jumpers can be installed on the module to select the desired bank (bank 0 or 1).

The basic functions involving the resident memory are shown in Figure 4-11. Resident memory comprises sixteen 4K by 1-bit memory chips, addressing, and control logic. The memory chips, which are 16-pin devices, require an address multiplexer to address the chips with two 6-bit bytes. The complete addressing, write, and read operations are described below.

Addressing is initiated by a master device — either the LSI-11 processor or a DMA device — by placing the 16-bit address on BDAL0-15 L and asserting BSYNC L, latching the address in the 16-bit address register. Note that the resident memory address will appear on the BDAL bus even when the processor is bus master; the resident memory functions exactly as a memory located elsewhere along the LSI-11 bus. Address bits are routed via BDAL bus receivers onto the processor module's DAL0-15 H bus to the address register input. Stored address bits A13—A15 H are then decoded by the bank select decoder. SBS0 L (bank 0) and SBS1 L (bank 1) will go active (low) only when their respective bank addresses are decoded. W1 or W2 then applies the selected address to the address multiplex control logic, enabling the resident memory response. Address multiplex logic immediately generates an active row address strobe (RAS), which remains active for the duration of the BSYNC L signal. Address multiplex control (AMX) is initially high, multiplexing the stored row address (bits A7—A12 H) through the 12:6-bit address multiplexer and into all memory chips. After 150 ns, address multiplex control logic generates an active column address strobe (CAS) and a low AMX signal. The multiplexer output bits (A1-A6) are then strobed into all memory chips, completing the addressing portion of the memory operation.

When in a memory read operation, each of the 16 memory chips places an addressed bit on the memory read data bus. This data is multiplexed via port A of the I/O bus/memory read data selector only when in a resident memory read (or refresh) operation; the select input of the data selector is asserted low for this data selection. The read data is then placed on WDAL0-15 H, where it can be read by the microprocessor data chip or gated onto the BDAL bus via bus drivers for input to a DMA device.

When in a memory write operation, the addressing portion of the operation is similar to the read cycle addressing, except BWTBT L may be asserted by the master device to indicate that a write operation is to follow. After the addressing portion of the cycle has been completed, BWTBT L either goes passive (high) if a DATO (word) write cycle is to be performed, or remains asserted (BWTBT L remains low) if a DATOB (byte) write cycle is to be performed. Word1byte select logic responds to the DATO cycle by asserting both BYTE 1 WT L and BYTE 0 WT L for the duration of the cycle, enabling DAL0-15 H data bits into the addressed location in all memory chips. However, when in a DATOB cycle, only one active signal is produced, depending upon the state of the stored byte pointer (address bit A0). If A0 is low (even byte), only BYTE 0 WT L goes active, enabling only DAL0-7 H bits to be written into the addressed location in the appropriate eight memory chips. Similarly, if A1 is high (odd byte), only BYTE 1 WT L goes active, enabling only DAL8-15 H bits to be written into the addressed location in the appropriate eight memory chips.

Resident memory, as well as any LSI-11 bus device, must respond to any data transaction by generating an active BRPLY L signal. Reply gates provide this function. Approximately 150 ns after CAS L goes true (as previously described), the reply gates are enabled; the gates will respond to either an active BDIN L or BDOUT L signal by asserting BRPLY L. Reply gates are inhibited during an initialize operation.

Resident memory requires a refresh operation once every 1.6 ms. This operation is entirely under the control of either processor microcode or an external DMA device, as selected by the user. Resident memory responds to BREF L, generated by the refresh-controlling device, by simulating a "bank selected" operation. (All memory banks are simultaneously refreshed.) Refresh is then accomplished by executing 64 successive BSYNC L/BDIN L operations while incrementing BDAL1-6 L by one location on each bus transaction. Refresh is simply a series of forced memory read operations where only the row addresses are significant. Each of the 64 rows in all dynamic MOS memory chips in an LSI-11 system are simultaneously refreshed in this manner.

4.2.4 DC-DC Power Inverter

The dc-to-dc power inverter circuit provides on-board generation of required negative dc voltages. Input dc power for the inverter circuit is obtained directly from the +12 V input. The inverter switching rate is clocked by the clock pulse generator's DIVB (0) H 2.8 MHz output. Output negative dc voltages are zener-regulated to -5 V and -9 V. The -9 V output is distributed to all resident memory chips. The -5 V output is distributed to microprocessor chips (data chip, microm chips, and control chip).

4.3 MMV11-A 4K BY 16-BIT CORE MEMORY

4.3.1 General

The MMV11-A 4K by 16-bit core memory option provides nonvolatile read/write storage of user programs and data. Memory 4K addressing is user-selected by switches contained on the option. The MMV11-A is completely LSI-11 bus-compatible and capable of either programmed I/O data transfers with the processor or transfers with another LSI-11 DMA bus device.

The MMV11-A features:

- 4096 by 16-bit capacity
- Typical access time = 425 ns; full read/restore cycle time = 1.15 μs.
- Nonvolatile read/write storage — stored data remains valid when power is removed.
- User-selected bank address — three switches allow the user to select the bank address for the option.
- +5 V and +12 V power — only the normal backplane power is required to power the option.
- No adjustments, no periodic maintenance.

The MMV11-A is contained on two modules which are mated to comprise a single assembly as shown in Figure 4-12. The modules include memory interface and timing board (module type G653 and core stack (module type H223). The actual size of the assembly is 8.5 by 10 by 0.9 in. The G653 module includes handles and retractors on the top edge and fingers on the bottom edge which plug into the LSI-11 bus. Circuits contained on this module include interface, control and timing logic, bus receivers and drivers, the 16-bit data paths, sense amplifiers, and a +5 Vdc to -5 Vdc

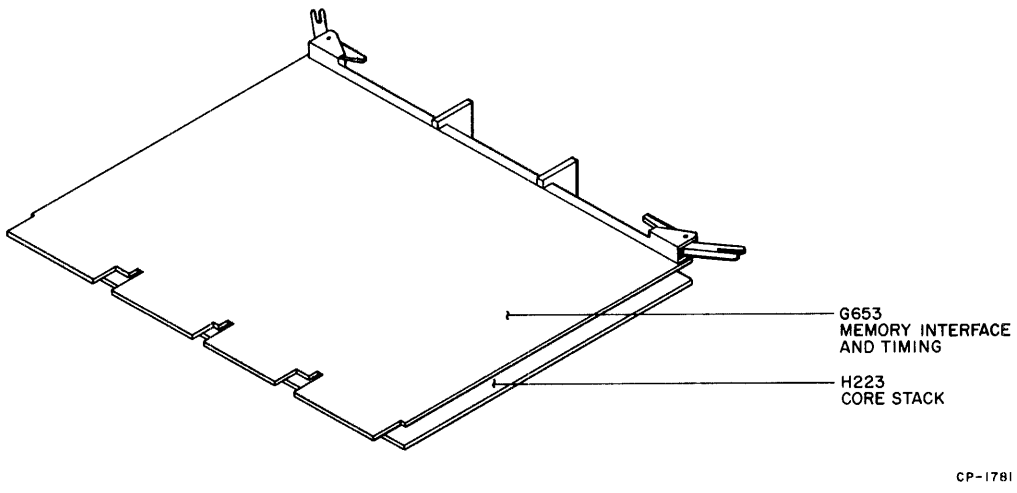


Figure 4-12 MMV11-A Core Memory Option

inverter. The H223 module is slightly smaller, includes no handles or bus fingers, and plugs onto the No. 2 (solder) side of the G653 module via special connector pins. Spacers are located between the modules to stiffen the assembly and to maintain the 0.9 in. dimension. Circuits contained on the H223 module include the 4096 by 16 core stack, 12-bit address register, X and Y drives, stack charge, temperature compensation, and a series +11 V, Vcc switch which removes drive power when BDCOK H goes low (power fail) or BINIT L is asserted.

4.3.2 Functional Description

4.3.2.1 Introduction — The MMV11-A memory is a read/write, random access, coincident current magnetic core type with a cycle time of 1.15 μs and an access time of 425 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits and the memory consists of 4096 (4K) words.

Major functions contained in the MMV11-A are shown in Figure 4-13. Memory data can be stored (written) or read by executing appropriate bus cycles: DATO (16-bit word) write; DATOB (8-bit byte) write; DATI (16-bit word) read; DATIO (16-bit word) read-modify-write; and DATIOB (16-bit word) read-modify-(8-bit byte) write.

Each of the functions shown in Figure 4-13 is briefly described below:

Bus Receivers and Drivers — These devices interface directly with the LSI-11 bus and the G653 logic circuits. BDAL bus drivers are gated on by DATA OUT L during a read operation [DATI or the input portion of a DATIO(B) bus cycle].

Bank Decoder — The bank decoder receives address bits A13-15 L and responds when the bank address is as user-selected on the three bank address switches on the G653 module. It responds by producing an active DSEL H signal which initiates memory cycle timing. This signal is enabled only when power is normal and bus initialize or refresh operations are not in progress.

Timing and Control — Timing and control circuits receive bus and internal control signals and generate appropriate read/write timing and control signals. It also generates the BRPLY L signal in response to BDIN L and BDOUT L.

Address Register — The address register stores the 12-bit word address within the 4K bank during the addressing portion of the bus cycle. Latched bits LA1—6H are applied to Y drive circuits and LA7—12H are applied to X drive circuits.

X and Y Drives — X and Y drive circuits control X and Y read/write currents through all core mats. Address decoding activates 1 out of 64 X wires and 1 out of 64 Y wires. Because the active X and Y wires each have one-half the current required for core saturation, only one core out of 4096 cores in each core mat is saturated. Direction of current is determined by a read or write operation.

Core Stack — The core stack comprises sixteen 4096-core mats. Each mat is associated with one memory bit position at all 4096 locations. Each core has three wires passing through it: one X, one Y, and one sense/inhibit wire. The sense/inhibit wire passes through all 4096 cores in one mat. Hence, the stack contains 16 sense/inhibit lines.

The sense/inhibit line ends terminate at sense amplifier inputs. During a write operation, an inhibit current, equal to saturation current, is applied to the center of the sense/inhibit line when a logical 0 is to be written in the addressed core. This current splits and one-half saturation current flows through all cores in the mat and into termination diodes at the sense amplifier inputs. The wire is threaded through the cores in a manner that causes the current to flow in a direction opposite to that of the Y write current; this prevents core saturation, which would write a logical 1 in the addressed core.

Sense Amplifiers — Sense amplifiers respond to induced voltage impulses during the read cycle. They are strobed during a critical time of the cycle, producing an active (high) output when a logical 1 is read, regardless of the induced polarity on the two ends of the sense/inhibit wires for each bit.

Inverters — The inverters receive sense amplifier outputs, invert them, and direct-set previously cleared memory data register bits when a logical 1 is sensed.

Memory Data Register — The 16-bit memory data register is cleared upon entry to a read cycle; sensed logical 1s set appropriate bits. During a restore cycle (DATI bus cycle) (no memory contents are to be modified), the same bits (low-active) are written into the same addressed location. During a write cycle [DATO, DATOB, or the write portion of a DATIO(B) bus cycle], bus data bits are clocked into the high and/or low byte(s), depending upon the type of bus cycle (word or high byte or low byte).

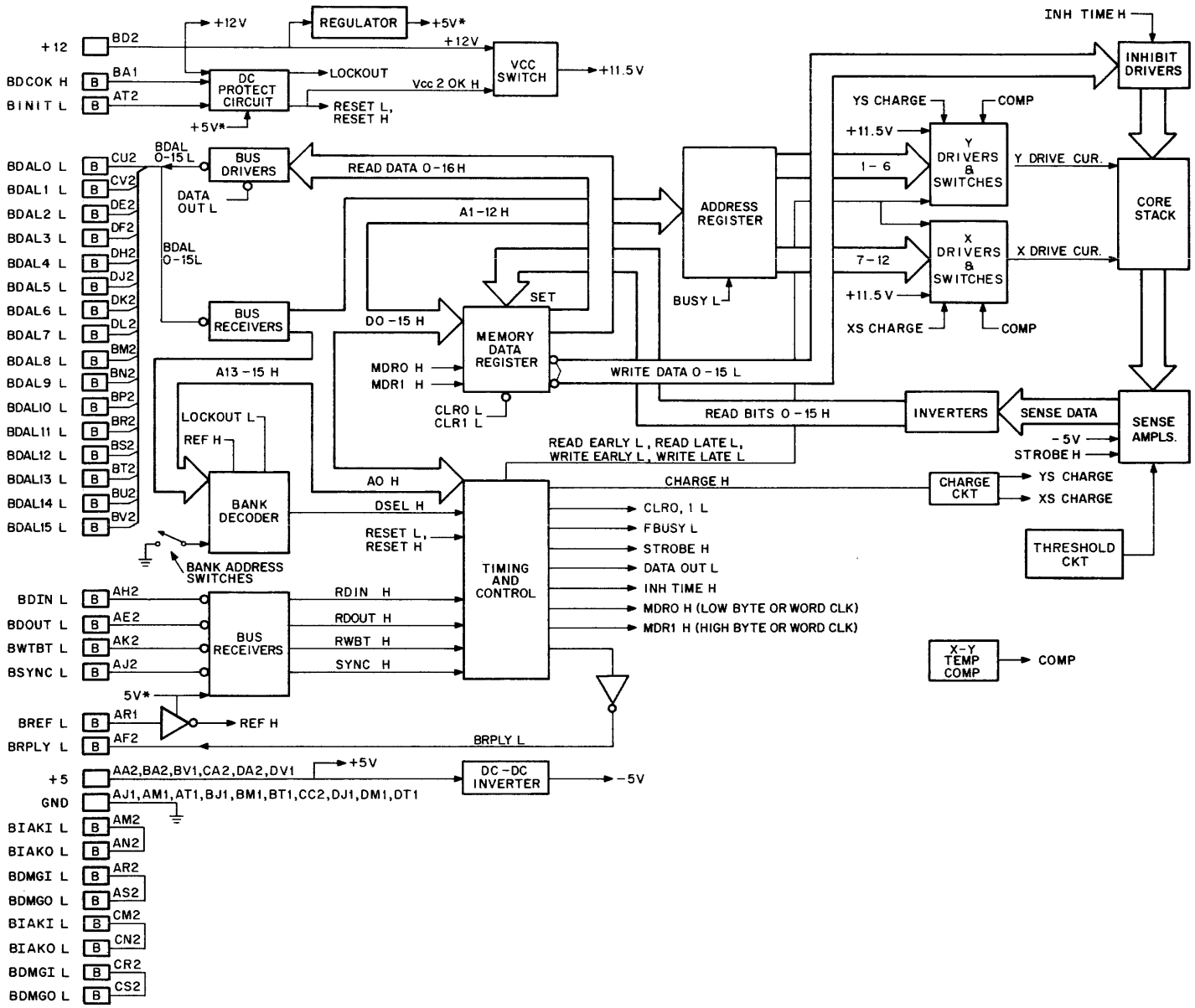


Figure 4-13 MMV11-A Logic Block Diagram

Inhibit Drivers — Inhibit drivers, one for each bit position, produce an inhibit current during the write cycle at INH TIME H if a logical 0 is to be written. The current inhibits core saturation, which would produce a stored logical.

Charge Circuit — The charge circuit applies the correct operating voltage to X and Y drive circuits during the read and write memory cycles to prevent "sneak" currents through unselected stack diodes.

X—Y Temperature Compensation — X—Y temperature compensation circuits alter drive currents over the required operating temperature range to provide reliable operation.

DC—DC Inverter — The dc—dc inverter circuit generates -5 V power for sense amplifiers from the +5 V power.

DC Protection — DC protection circuits respond to an active BINIT L or passive BDCOK H signal by producing active LOCKOUT L, RESET H, RESET L, and passive VCC2OK H signals. These signal conditions prevent memory circuit operation and the possible loss of stored data.

Vcc Switch — The Vcc switch applies +11.5 V to X and Y driver circuits when not in an initialize or power fail condition.

4.3.2.2 Core Addressing — When a memory location is addressed, one core in each of the 16 mats are accessed for a read or write operation. Figure 4-14 illustrates a portion of the X—Y drive and associated circuits for one Y wire. Six address bits (A1—A6) select 1 of 64 Y wires. A similar circuit (not shown) involving the remaining six address bits (A7—A12) selects 1 of 64 X wires. Hence, by placing 64 cores (in each mat) on each Y wire and passing a different X wire through each core, one of 64 cores on the active Y wire will be selected. Since the remaining Y wires have a similar 64 cores each and receive the same X wires, 64 × 64, or 1 out of 4096 addressing is accomplished in each of the core mats. A single Y wire is driven as described below.

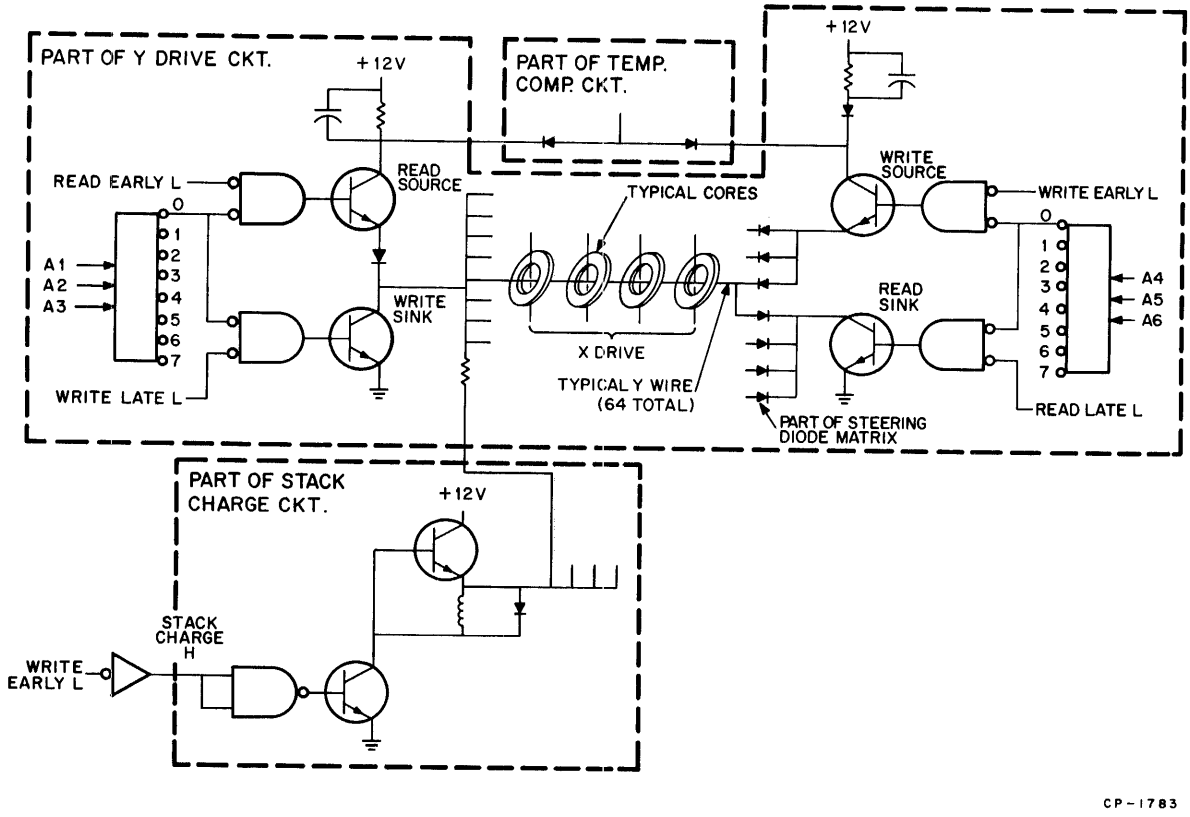


Figure 4-14 MMV11-A Core Addressing

Two 1:8 (octal) decoders are used in Y wire selection, each receiving three address bits from the address register. Only one output from each decoder will be active during addressing. Assuming address XX00 (the zeros are the Y portion of the 12-bit address), the portion of the Y drive circuit shown will be enabled. During a read operation, READ EARLY L goes active and turns on one of the eight read current source transistors. A diode in its emitter circuit couples the drive to eight Y wires, each terminating at the diode steering matrix. The diodes provide a read current path to all eight read sink transistors. READ LATE L goes active 25 ns after the Y source is turned on, and turns on one of the eight read sink transistors, completing a read current path to ground. Hence, 1 of 64 Y wires is selected, producing a read half-current through 64 cores in all memory mats. Similar X drive circuits will produce an X read half-current in 64 cores in each mat in exactly the same manner. Only one core in each mat will receive an X and a Y read half-current, causing the core to saturate in the 0 state. If the core was previously in the 1 state, a voltage pulse will be induced in the sense/inhibit wire as it switches to the 0 state.

A write cycle is always preceded by a read cycle. The write operation is similar to the read operation, except write current flows through the addressed wire in a direction opposite to the read current direction. The core in each mat receiving X and Y write half-currents will respond by saturating in the 1 state. However, since a 0 may be desired, a third wire (sense/inhibit) will conduct a half-current which opposes the magnetizing effect of the Y write currents. Thus, core saturation is not attained and the cores where 0s are written remain saturated in the 0 state from the previous read cycle.

Temperature compensation is applied to driver circuits via a source current, which is inversely proportional to temperature; an increase in temperature decreases available drive current.

The stack charge circuit applies a +11 V (approximately) signal to the sink ends of all X (not shown) and Y wires during the write cycle. The level is applied during WRITE EARLY time. Since WRITE LATE L occurs 25 ns after WRITE EARLY L, the write sink transistor is cut off, and the full 11 V signal charges the stray capacitance of the X-Y lines, reducing the capacitive delay effect as the X and Y write source transistors turn on; the 11 V signal also reverse biases diodes not selected by addressing circuits, preventing sneak currents. The addressed sink transistor, turned on by the active WRITE LATE L signal, provides the return path for the selected X and Y wires; only those two wires will go to approximately 0 V, causing one X and one Y diode to become forward biased, enabling the write half-currents to flow. Resistors coupling the charge voltage to write sink transistors limit the charge current through the addressed write sink transistors during the remainder of the write cycle. This circuit performs the same function for read cycles by grounding the buses and preventing sneak currents through unselected stack diodes.

4.3.2.3 Read/Write Data Path — The basic read/write data path is shown in Figure 4-13. Upon entering a read cycle, the memory data register is cleared by CLR0 L and CLR1 L. X and Y read currents produce active sense amplifier outputs for those cores containing stored logical 1s as they are switched to the 0 states. These signals are inverted and applied to the direct-set inputs of the flip-flops comprising the memory data registers, setting the appropriate bits. During a write cycle, CLR0 L (DATOB low byte address), or CLR1 L (DATOB high byte address), or both CLR0 L and CLR1 L (DATO word address) clear the previously read data. The bus data is then received and clocked into the register flip-flops by CLK MDR0H and/or CLK MDR1 H, as appropriate. Write data bits are then routed to inhibit drivers which inhibit writing 1s when write bits are 0s (high). Inhibit half-current through addressed cores prevents X-Y write half-currents from switching cores to the 1 state.

The sense/inhibit wire passes through all cores in a core mat, as shown in Figure 4-15. The circuit shown in the figure is repeated for each of the 16 core mats. During the read portion of a memory cycle, a logical 1 stored in the addressed core will cause an induced voltage to appear on the sense/inhibit wire as the core switches from the 1 saturation state to the 0 saturation state. If a 0 was previously written, no appreciable voltage is produced since the core is already saturated in the 0 state. During the read operation, the sense/inhibit wire functions as a loop whose ends terminate at the sense amplifier inputs. Any difference in potential (either polarity) will enable a sense amplifier output. STROBE H occurs during X and Y drive read currents at a critical time (the time of peak core switching output when 1s are read). Thus, only the correct voltage pulse produced when a core goes from the 1 state to the 0 state is gated into the Memory Data Register flip-flop.

The threshold circuit establishes the signal voltage level at which a logical 1 is read during strobe time. A signal voltage magnitude greater than approximately 17 mV during strobe time results in a valid 1 level.

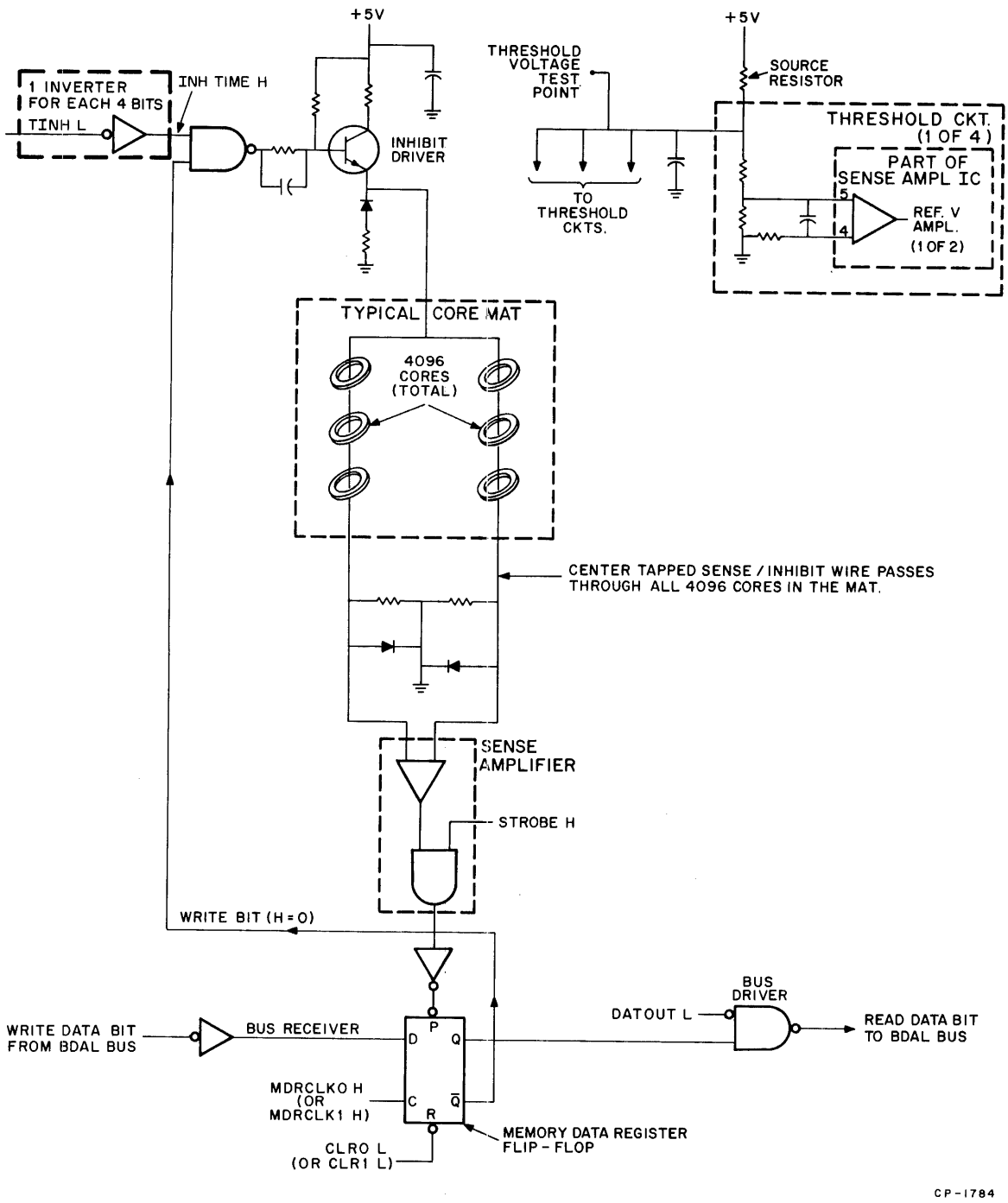


Figure 4-15 MMV11-A Read/Write Bit Data Path

Signal levels less than the 17 mV threshold value are considered invalid and result in 0 levels being read. Four threshold circuits share a common source resistor. Each threshold circuit provides a reference amplifier input voltage to two sense amplifier ICs, each containing two sense amplifiers; hence, one threshold circuit provides a threshold voltage for four data bits.

When in the write portion of the memory cycle, the inhibit driver remains off if a 1 write data bit is stored in the memory data register flip-flop. However, if a 0 is to be written, the write bit is high, enabling a gate input

for the inhibit driver. At INH TIME H during the write cycle, the inhibit driver produces an inhibit current equal to core saturation in a direction that would produce a logical 0. However, note that the inhibit current is applied to the center of the sense/inhibit wire. Thus, half-currents flow into each half of the sense/inhibit wire, preventing the addressed core from saturation in the 1 state. Diodes at the sense amplifier ends of the wire provide a ground return for the two inhibit half-currents. The two resistors terminate the ends of the wires. The inhibit driver transistor collector is clamped to ground through a diode and resistor to prevent breakdown during turnoff. The emitter resistor limits peak current.

4.3.2.4 Timing and Control — All memory bus cycles comprise a read and a write operation. During a DATI bus transaction, a memory read-restore cycle is executed. The data is first read and placed on the I/O bus. The same data is then written in the same addressed location. During a DATO bus transaction, a memory read-modify-write cycle is executed. After reading the contents of the addressed location, bus data is clocked into the memory data register. Previously read data is lost. The modified word is then written into the addressed location during the remainder of the cycle. If a DATOB bus transaction is being executed, only an 8-bit portion of the memory data register is modified, and one byte of the previously read word is retained for the write operation. A DATIO bus transaction actually initiates two separate memory cycles. The first cycle (read-restore) is initiated by the master device by placing the memory address on BDAL0—15 L and asserting BSYNC L. After receiving and modifying the memory read data, the master device outputs the new data to the memory and asserts BDOUT L, which initiates the next memory cycle (read-modify-write). Timing and control logic functions generate all of the timing and control signals for the memory cycles described above. Logic operation for each type of bus transaction is described in detail in the following paragraphs.

A memory cycle is initiated when the correct bank address asserted by the bus master device is decoded on the leading edge of BSYNC L. DSEL H is the decoded bank address signal; note that it is inhibited during refresh bus cycles (when BREF L is asserted), or when an initialize or power fail condition exists. The logical state of DSEL H is clocked in the Busy flip-flop on the leading edge of SYNC H (Figure 4-16). When DSEL H is active (high), the Busy flip-flop sets and FBUSY H and FBUSY L go to their true states. FBUSY L enables one input of the read initiate gate. The remaining gate input is enabled by the negative-going pulse produced by the RC circuit connected to FBUSY L. Thus, on the leading edge of FBUSY L, the state of FBUSY H is clocked into the Read flip-flop, causing it to go to the set state. This sequence is shown in Figures 4-17 and 4-18.

The read-restore (DIN) cycle continues as shown in Figure 4-17. FREAD H activates the read time generator, producing time signals prefixed with "RT." Each signal is a 225 positive-going pulse whose leading edge is delayed with respect to FREAD H. Hence, the leading edge of RT225 H, shown in Figure 4-16, occurs 225 ns after the leading edge of FREAD H, and approximately 275 ns after BSYNC L is asserted. Note that RT225 H is inverted and applied to the clear input of the Read flip-flop, establishing the 225 ns pulse width for RT pulses. RT225 H goes low, 225 ns later. This time occurs 400 ns (total) after BSYNC L is asserted and it is referenced on Figure 4-16 as (T500 L).

The pulse produced by the RC network on the leading edge of FBUSY L is inverted to produce the CLR0 L and CLR1 L signals, which clear the memory data register for the new read data. READ EARLY occurs on the leading edge of FREAD H and remains active for the duration of RT50 H, producing a 300 ns pulse. RT25 H goes high 25 ns later, producing the READ LATE L signal; this signal remains true for the duration of RT100, resulting in a 325 ns pulse. Read data is valid at the sense amplifier inputs from 200 to 275 ns after READ EARLY L goes active. RT175 H is gated with RT50 H to produce the sense amplifier strobes STROBE 0 and 1 H. The trailing edge of RT50 H occurs 100 ns after the leading edge of RT175 H, negating the strobes. During strobe time, the sense amplifier data bits set the appropriate flip-flops that comprise the memory data register, and store the memory read data.

The bus master device initiates the data transfer portion of the DATI transaction by asserting BDIN L. The Replay Enable flip-flop is set on the trailing edge of RT100 H 375 ns after BSYNC L. If RDIN H (BDIN L inverted) is received earlier than 375 ns after BSYNC L, the Reply flip-flop input gates wait 375 ns to produce an active RPLY SET L signal (Figure 4-17), which direct-sets the Reply flip-flop and produces the active FRPLY H and BRPLY L signals. FRPLY L is gated with RDIN L and inverted, producing the DATA OUT L signal which gates memory data register bits onto the BDAL bus. If RDIN H is received later than 375 ns after BSYNC L, the Reply flip-flop sets on the leading edge of RDIN H. The trailing edge of RT150 H (T425 L) is gated with RPLY SET L, producing a write

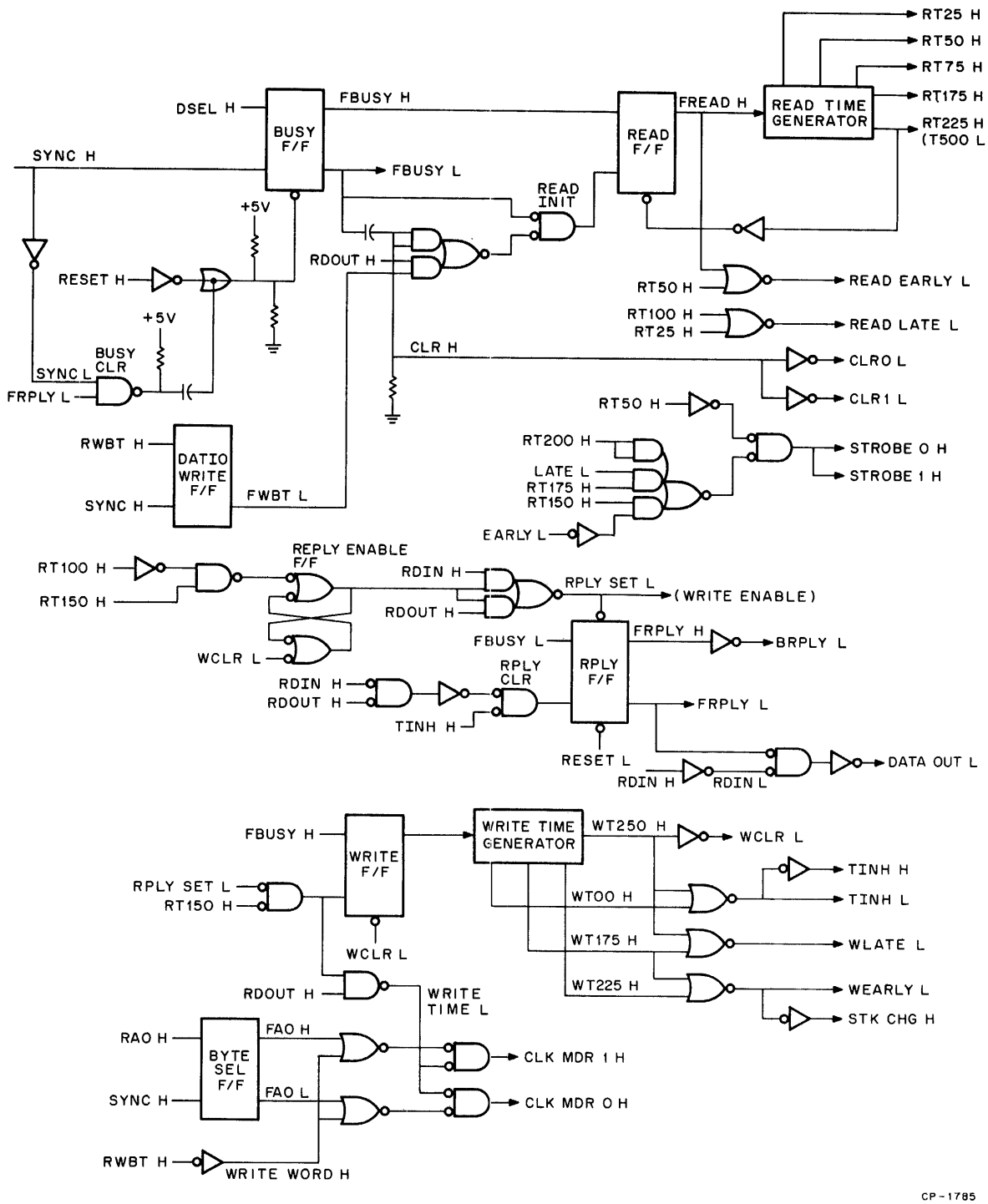


Figure 4-16 MMV11-A Timing and Control Circuits

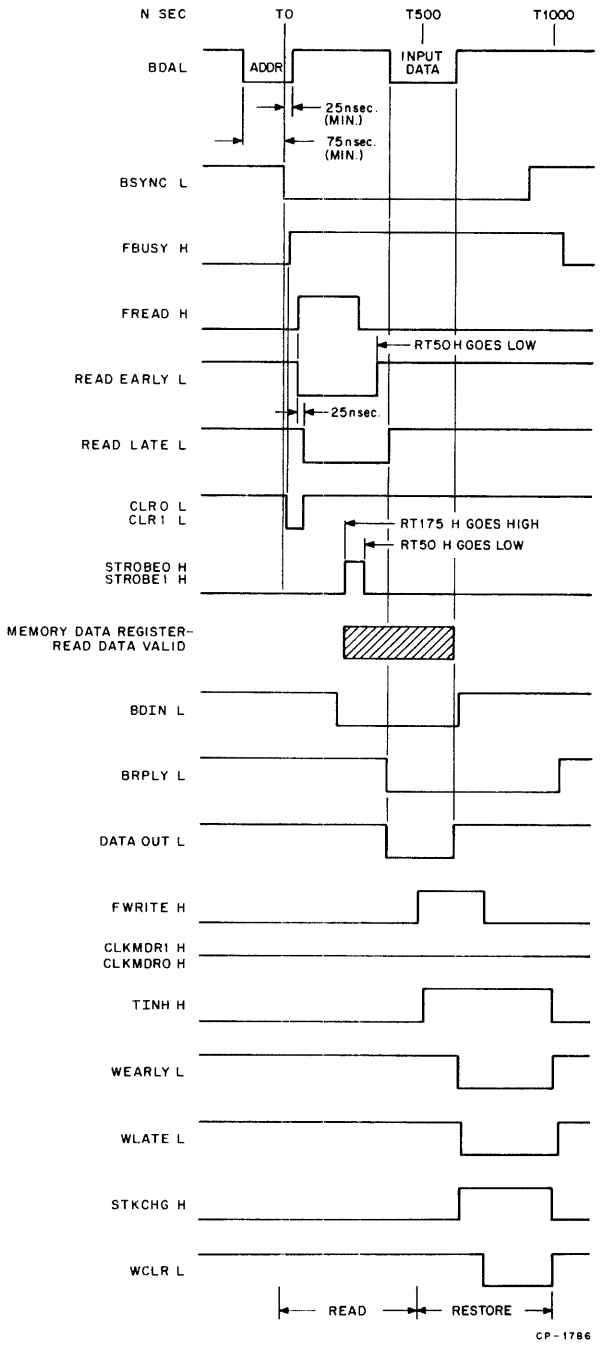


Figure 4-17 Read-Restore Memory Cycle Timing

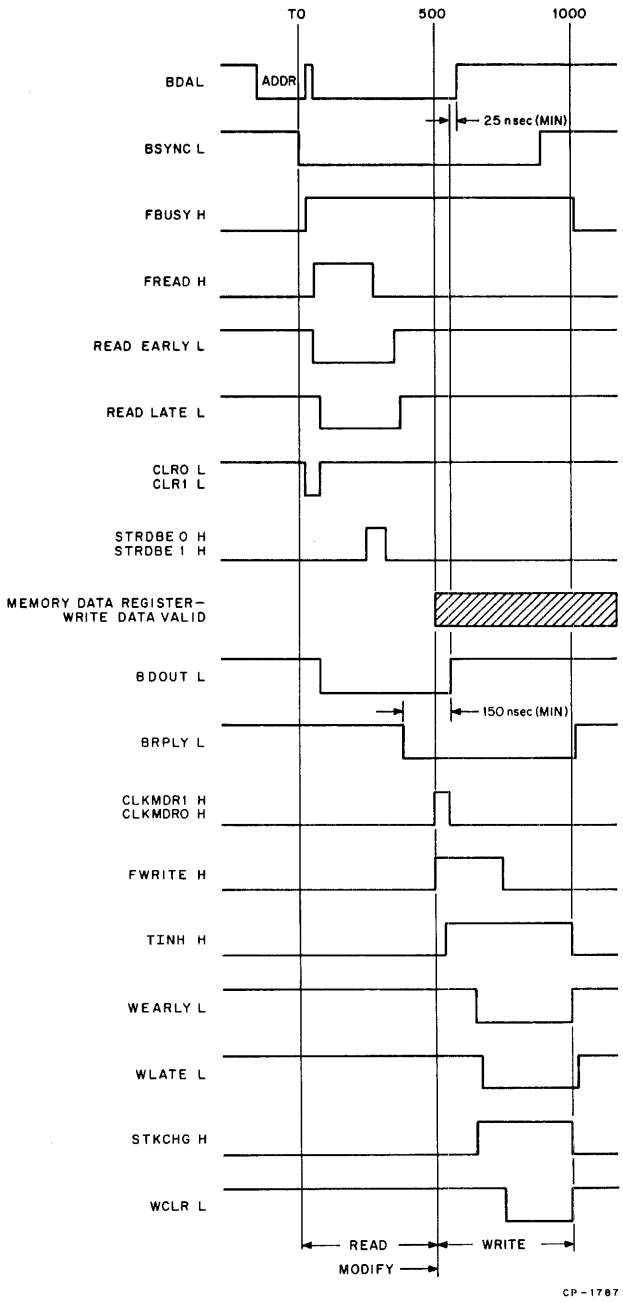


Figure 4-18 Read-Modify-Write Memory Cycle Timing

initiate pulse which clocks the high FBUSY H signal into the Write flip-flop, initiating the restore portion of the memory cycle.

Restore timing is produced by the write time generator in a manner similar to that described for read time generation. At WT00 H time, TINH H and TINH L (475 ns pulses) are produced for the inhibit drivers. TINH H also inhibits the Reply Clear gate, and the Reply flip-flop remains set for the remainder of the memory cycle. WEARLY L and STK CHG H go active on the leading edge of WT175 H and remain active for 350 ns. Similarly, WLATE L goes active on the leading edge of WT175 H and remains active for 325 ns. At WT250 H time, WCLR L is produced, clearing the Reply Enable and Write flip-flops; thus, write time generator outputs are 250 ns pulses. Memory data is restored (written) during the time that TINH H, WEARLY L, and WLATE L are active. The memory cycle terminates when both SYNC L and FRPLY L go to their passive states. The Busy Clear gate detects this condition, producing a low pulse which clears the Busy flip-flop, and the memory cycle ends.

The DATO cycle is similar to the DATI cycle except that during the addressing portion of the bus cycle, the bus master device asserts BWTBT L. RWBT H goes high, and the leading edge of SYNC H clocks the byte flip-flop to the set state. The active FWBT L signal is only used when in the write portion of the DATIO cycle, as described later. However, during a DATO bus transaction, RDIN H is not received; instead, RDOUT H is received, enabling the REPLY SET L gates, as shown in Figure 4-18. RDOUT enables one input to the WRITE TIME L gate. At the same time that the Write flip-flop clocks to the set state, WRITE TIME L goes low, enabling CLK MDR0 and 1 H gates. Since a DATO bus cycle is in progress, BWTBT L remains passive during the data transfer portion of the bus cycle. Hence, RWBT H is low, WRITE WORD H is high, and the two byte select OR gates apply low signals to the remaining CLK MDR gates. CLK MDR 0 and 1 H then clock the BDAL bus data into the memory data register; the previously read data is lost. The write portion of the cycle continues as described for the restore portion of the DATI operation.

When executing a DATOB bus transaction, BWTBT L and RWBT H remain active for the duration of the bus cycle. Hence, the WRITE WORD H signal remains passive. The Byte Select flip-flop that stores byte address bit RA0 H during addressing time enables generation of only one CLK MDR H signal. When RA0 H is low, FA0 L goes high and CLK MDR 0 H clocks low byte data bits from only BDAL0—7 L into the memory data register. Register bits 8—15 remain unchanged. Similarly, when RA0 H is high, FA0 H goes high and CLK MDR 1 H clocks high byte data bits from only BDAL8—15 L into the memory data register. Register data bits 0—7 remain unchanged. The write portion of the memory cycle then continues as previously described.

When executing a DATIO bus cycle, two complete memory cycles are executed. They include a DATI and a DATO or DATOB cycle as previously described. However, when executing a DATIO bus transaction, BSYNC L remains active for the duration of the transaction. Hence, SYNC H, which generates FBUSY L during the read-restore portion of the cycle, cannot initiate the second read-modify-write memory cycle. Instead, FWBT L, stored during the addressing portion of the cycle, enables a read initiate pulse on the leading edge of RDOUT H. The Read flip-flop goes to the set state and operation continues as described for DATO or DATOB bus transactions.

4.3.2.5 DC Protection and Vcc Switch — DC protection and Vcc switch circuits are shown in Figure 4-19. The dc protection circuit is activated during power-fail

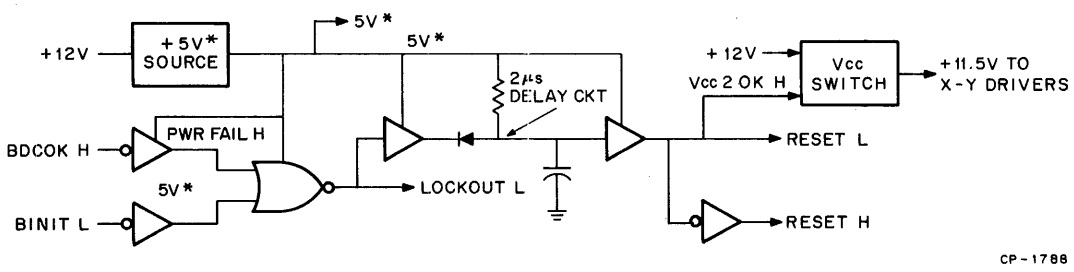


Figure 4-19 DC Protection and Vcc Switch Circuits

or bus initialize conditions. BDCOK H and BINIT L are inverted and ORed to produce LOCKOUT L. Normally, this signal is passive (high), enabling bank addressing and resulting in an active DSEL H signal when the memory is addressed. However, if BDCOK H goes low (power fail) or BINIT L is asserted low, LOCKOUT L immediately inhibits the bank addressing function.

The reset signals are also generated by this circuit. RESET L goes active (low) whenever LOCKOUT L is active. A 2 μs delay circuit enables the memory to complete its present cycle before RESET. RESET L is also inverted to produce RESET H; both signals are used to clear (initialize) memory timing control circuits.

To produce a 5V* source for reset circuits and bus receivers BSYNC L, BDIN L, BDOUT L, BWTBT L, and BREF L, +12 V power is regulated. Thus, if +12 V is removed, all MMV11 memory operations are disabled. However, if +5 V is removed and the +12 V remains, the 5 V* allows memory protect logic to remain functional.

RESET L is also applied to the VCC20K H input to the Vcc switch circuit. This signal is high only when both +5 V and +12 V power sources are normal. The Vcc switch comprises a transistor (Vcc switch), which is turned on when power is normal to produce +11.5 V power for X-Y driver circuits.

4.3.2.6 DC-DC Inverter — The dc-dc inverter circuit is shown in Figure 4-20. It is comprised of an inverter oscillator using a saturable transformer, a negative rectifier, and a filter. A 3-terminal regulator chip produces the regulated -5 V for sense amplifier operation.

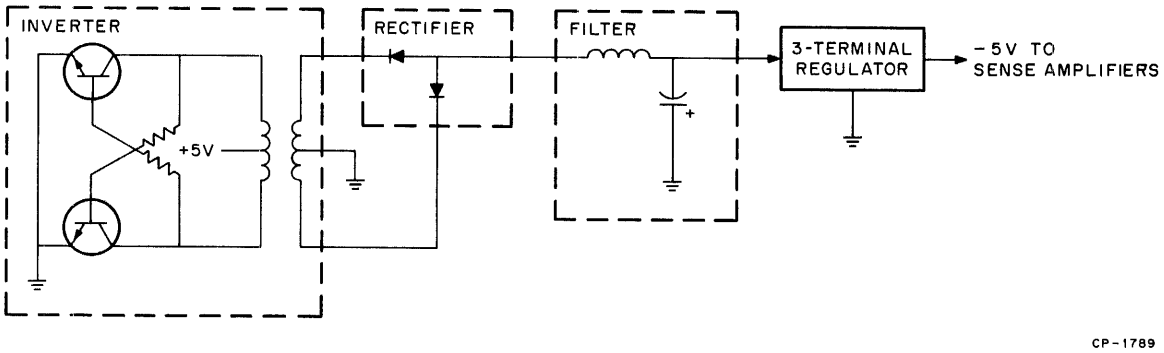


Figure 4-20 DC-DC Inverter Circuit

4.4 MRV11-A 4K BY 16-BIT READ-ONLY MEMORY

4.4.1 General

The MRV11-A is a basic read-only memory module on which the user can install programmable read-only memory (PROM) or masked read-only memory (ROM) chips. All PROM/ROM chip sockets and addressing and control circuits are contained on a single 8.5 by 5 inch module.

The MRV11-A features:

- 4096 by 16-bit capacity using 512 by 4-bit chips or 2048 by 16-bit capacity using 256 by 4-bit chips.
- Compatibility with chips available from multiple sources.
- Unpopulated addressable 1K portions of the module that can be shared by read/write memory modules (MSV11-A).
- Jumpers that allow the user to select the 4K memory address space which the MRV11-A will respond, chip type, and upper or lower 2K segment (when 256 by 4-bit chips are used).

4.4.2 Functional Description

4.4.2.1 General — Major functions contained on the MRV11-A module are shown in Figure 4-21. ROM data stored on the module can be addressed and read by the LSI-11 processor or other DMA devices by executing a DATI bus cycle. Data/address lines BDAL0-15 L and three bus interface control signals (BSYNC L, BDIN L, and BRPLY L) comprise all interface signals required for accessing the read-only memory. BREF L inhibits BRPLY L and BDAL bus drivers during memory refresh operations.

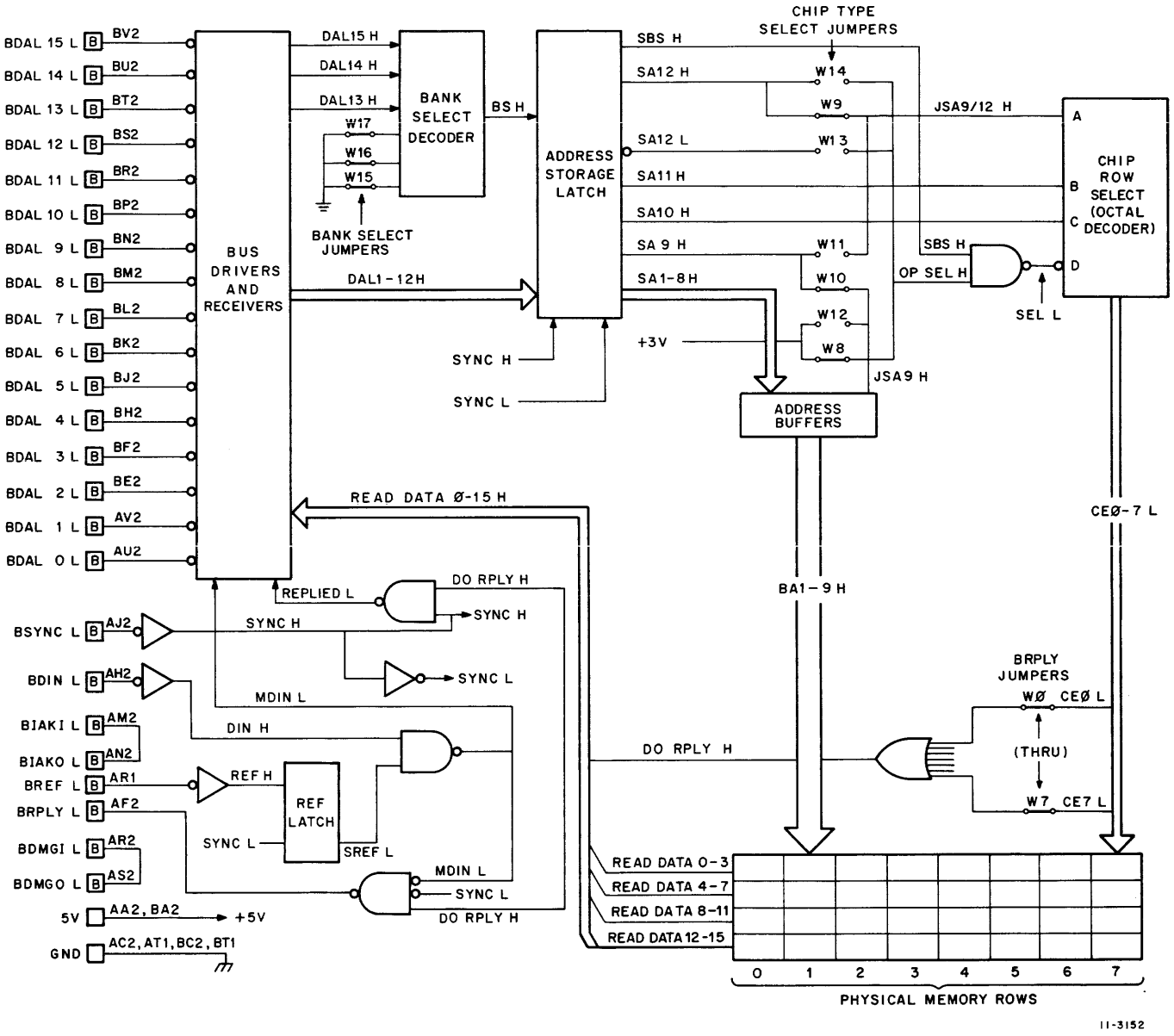


Figure 4-21 MRV11-A Logic Block Diagram

4.4.2.2 Addressing — A master device can address any 16-bit word in the 4K module by placing appropriate address bits on BDAL1-15 L during the addressing portion of the DATI cycle. BDAL0 is not used on the MRV11-A since this address bit functions only as a byte pointer during DATOB and the write portion of DATIOB bus cycles. Bus receivers route DAL13-15 H to the bank select decoder and DAL1-12 H to the address storage latch. Bank selection occurs when the 4K address encoded on DAL13-15 H is equal to the user-configured value selected by jumpers W17-W15. The resulting bank select (BS H) and address bits DAL13-15 H are then stored in the address storage latch on the leading edge of BSYNC L. Stored address bits SA1-8 H are buffered to produce BA1-9 H which are applied to all ROM/PROM chips on the module.

When 512 by 4-bit chips are used, SA9 H is routed via jumper W10 to a buffer, producing the inverted BA9 H address bit for all chips (pin 14). However, when 256 by 4-bit chips are used, W10 is removed and W12 is connected, forcing a low (chip enable) signal to become applied to all chips (pin 14); note that 256 by 4-bit chips do not receive address bit 9.

Memory chips sockets are arranged in eight physical rows of four sockets each. The memory is expanded by installing all four chips in each desired row. Four chips provide the full 16-bit word storage for LSI-11 instructions and data. Only one row is enabled by a chip enable (CE) signal, produced by chip row select logic and chip type jumpers.

When 512 by 4-bit chips are used, jumpers W8, W9, and W10 are installed. The chip row select octal decoder receives stored address bits SA10, SA11, and SA12 on its A, B, and C inputs, respectively, as shown in Figure 4-22. Bank Select Stored (SBS H) is gated to produce a low SEL L enable signal, which is applied to the D input of the decoder. (The decoder is actually a decimal decoder; whenever a high signal is applied to its D input, outputs 0-7 are inhibited.) One decoder output goes low, enabling the appropriate physical row addressed by bits SA10-12 L.

When 256 by 4-bit chips are used, jumpers W8, W9, and W10 are removed and jumpers W11, W12, and either W13 or W14 are installed, as shown in Figure 4-23. SA10 and SA11 are applied to octal decoder A and B inputs, respectively. Bit SA9, which is not used to directly address the 256 by 4-bit chips is then applied to input C of the octal decoder. SA12 H and SA12 L are available for jumper selection of the desired 2K segment within the 4K bank. W13, when installed, selects the lower 2K; W14 selects the upper 2K. When the selected segment is addressed, OP SEL goes high. This signal is gated with SBS H to produce the low (active) octal decoder enable signal.

4.4.2.3 Data Read Operation — Once the ROM/PROM chip sockets are addressed, the data can be read by the bus master device. Data is available within 120 ns after BSYNC L is received. One active CE0-7 L signal produces the active DO RPLY H signal, which enables reply and BDAL bus driver gating. Active DO RPLY H and SYNC H signals are gated, producing the REPLIED L signal, which enables one of the two bus driver enable inputs. The remaining enable input is MDIN L. The bus master device asserts BDIN L to request the data. DIN H is ANDed with the passive (high) SREF L signal, producing MDIN L, and read data is enabled onto BDAL0-15 L. Active MDIN L, SYNC L, and DO RPLY H signals also enable the BRPLY L bus driver, producing the required response to BDIN L.

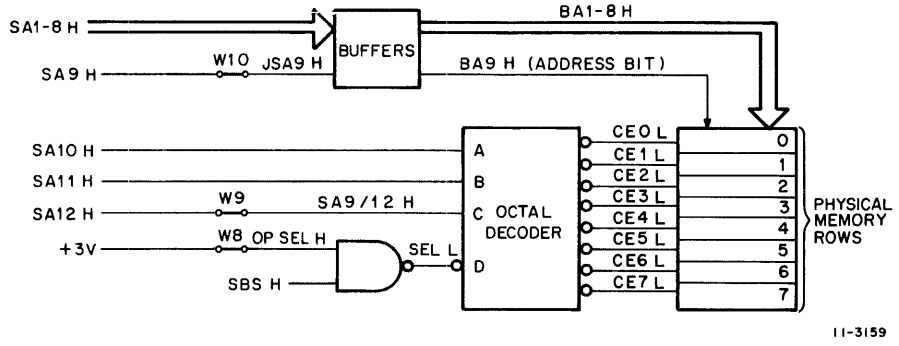


Figure 4-22 512 by 4-Bit Chip-Jumper Configuration

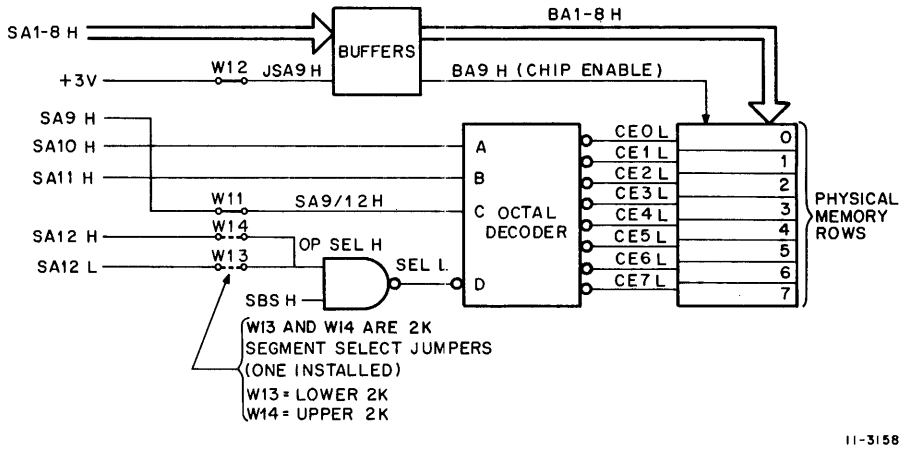


Figure 4-23 256 by 4-Bit Chip-Jumper Configuration

When the system is in a memory refresh operation, the MRV11-A must not respond to the BSYNC/BDIN refresh bus transactions. BREF L is asserted during the addressing portion of the bus cycle and the refresh latch stores REF H on the leading edge of SYNC L. SREF L goes low and inhibits the MDIN L signal. Hence, BDAL and BRPLY L bus drivers are not enabled.

4.5 MSV11-B 4K BY 16-BIT SEMICONDUCTOR READ/WRITE MEMORY

4.5.1 General

The MSV11-B is a 4K by 16-bit dynamic MOS read/write memory module which can be used for temporary storage of user programs and data. The storage capacity is 4096, 16-bit words. Memory address selection is user-configured by installing or removing jumpers contained on the module. Memory refresh is directly controlled by LSI-11 bus signals. Refresh operations can be automatically controlled by the LSI-11 microcomputer module once every 1.6 ms (approximately) or performed by another device. The MSV11-B is LSI-11 bus-compatible and capable of either programmed I/O data transfers with the processor or DMA transfers with other LSI-11 bus devices.

The MSV11-B features:

- 4096 by 16-bit word.
- Fast access time — 550 ns maximum.
- Low power — 12.7 W for the module, worst case.
- Dynamic MOS memory chips — Refresh is automatically controlled by processor or by a DMA device.
- User-configured 4K addresses — Three jumpers allow user address configuration.

4.5.2 Functional Description

Major functions contained on the MSV11-B module are shown in Figure 4-24. Memory data can be stored (written) or read by the LSI-11 microcomputer, or other bus master devices operating in the DMA mode, with appropriate bus cycles: DATO (16-bit word write operation); DATOB (8-bit byte write operation); DATI (16-bit read operation); or DATIOB [16-bit read-modify-write (8 or 16-bit) operation].

Addressing is initiated by a master device (either the LSI-11 processor or a DMA device) by placing the 16-bit address on BDAL0-15 L and asserting BSYNC L, latching the address (and bank select information) in the address register. Address bits are routed from the BDAL bus receivers onto the module's DAL0-15 H bus to the 13-bit address and bank select register input. Address bits BDAL13-15 L are decoded by the bank address decoder. Decoder output signal BS H will go active (high) only when the jumper-selected bank address is decoded. The active BS H signal is stored along with the 13-bit memory address for the duration of the operation.

The memory array comprises sixteen 16-pin 4K by 1-bit memory chips which require the address multiplexer to address the array with two 6-bit bytes. Address multiplexer control logic responds to the active SYNC H and stored active bank select (LBS L) signal by immediately generating an active Row Address Strobe (RAS). This signal remains active for the duration of the active SYNC H signal. Address

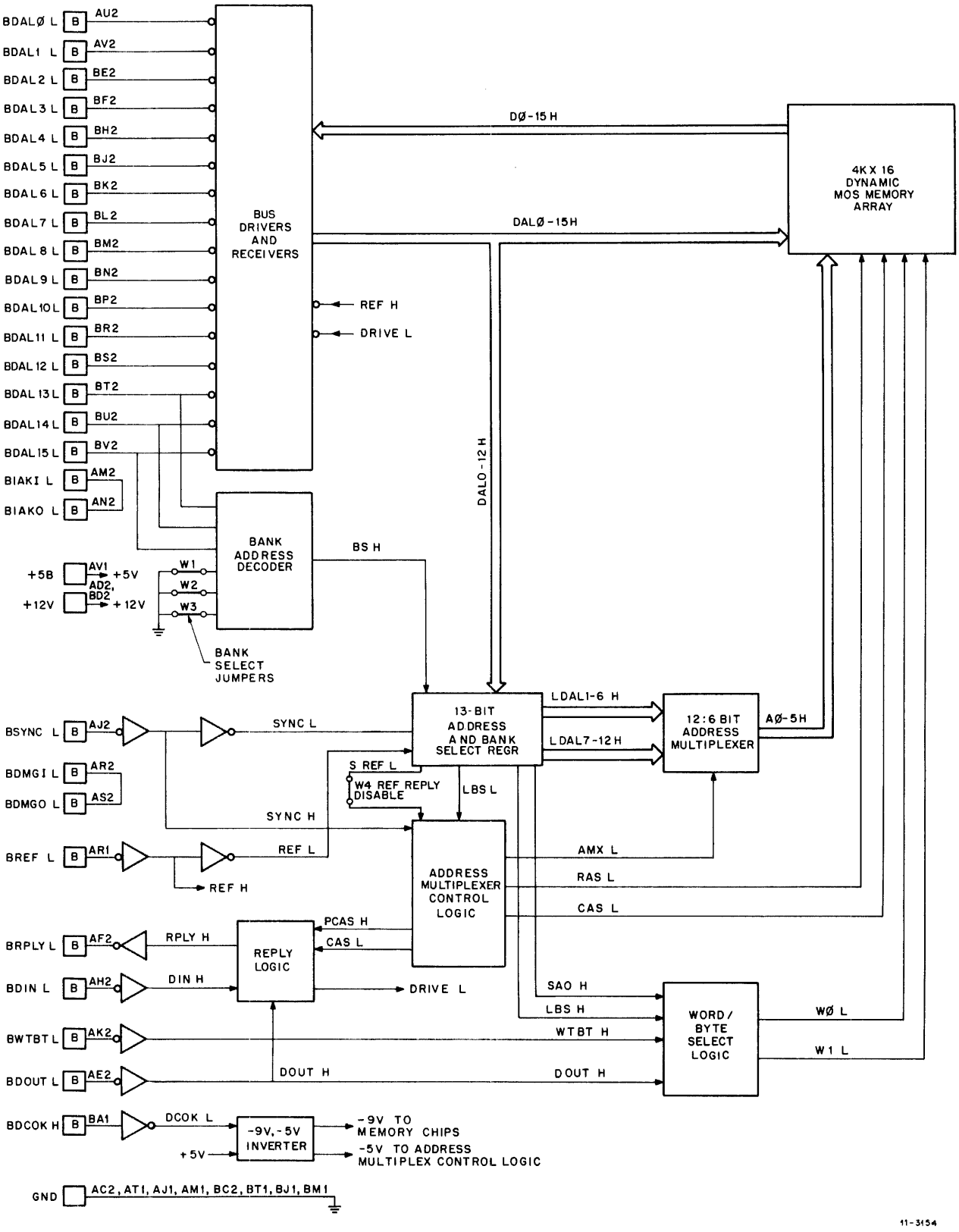


Figure 4-24 MSV11-B Logic Block Diagram

multiplex control AMX L is initially passive (high), multiplexing the stored row address bits (LDAL7-12 H) through the 12:6-bit address multiplexer and into all memory chips. After approximately 150 ns, address multiplex control logic generates an active column address strobe (CAS) and an active AMX L signal. Multiplexer column address bits (LDAL1-6 H) are then strobed into all memory chips. This completes the chip addressing portion of the memory operation.

When in a memory read operation, the bus master device asserts BDIN L. The data from the accessed memory location is present on the D0-15 H bus and at bus driver inputs. Reply logic responds to BDIN L by generating an active DRIVE L signal which gates the memory read data onto BDAL0-15 L for input to the requesting device; reply logic also asserts BRPLY L to complete the data transfer portion of the cycle.

When in a memory write operation (or the write portion of a DATIOB cycle) the addressing portion of the operation is similar to the read cycle addressing. After the addressing portion of the cycle has been completed, the master device asserts BDOUT L, and BWTBT L either goes passive (high) if a DATO (word) write cycle is to be performed, or remains asserted if a DATOB (byte) write cycle is to be performed. Word/byte select logic responds to the DATO cycle by asserting both W0 L and W1 L for the duration of the cycle, enabling DAL0-15 H bits to be written into the addressed location in all memory chips. However, in a DATOB cycle with A0 H low (even byte), only W0 L goes active, enabling the writing of DAL0-7 H into the addressed location in the appropriate eight memory chips. Similarly, if A0 H is high (odd byte), only W1 L goes active, enabling only DAL8-15 H bits to be written into the addressed location in the appropriate eight memory chips. The reply logic also responds to the active BDOUT L signal by asserting BRPLY L, indicating that the data has been written, completing the data transfer.

The memory chips in the MSV11-B require a refresh operation once every 1.6 ms. This operation is entirely under the control of either processor microcode or a DMA device, as selected by the user. The address multiplex control logic responds to BREF L, generated by the refresh-controlling device, by simulating a "bank selected" operation. (All system memory banks are simultaneously selected during refresh.) Refresh is then accomplished by a device by executing 64 successive BSYNC L/BDIN L operations while incrementing BDAL1-6 by one on each bus transaction. Refresh is simply a series of forced memory read operations where only the row addresses are significant. Each of the 64 rows in all dynamic MOS memory chips in an LSI-11 system are simultaneously refreshed in this manner. The REF H signal inhibits all BDAL bus drivers for the duration of the refresh operation.

A dc-to-dc inverter circuit is included on the module for negative voltage generation. Output voltages include -9 V for the MOS memory chips and -5 V for linear devices in the address multiplex control logic. Hence, only +12 V and +5 V power inputs are required for module operation. The BDCOK H signal starts dc-to-dc inverter oscillation when bus power is applied.

4.6 MSV11-A 1K BY 16-BIT SEMICONDUCTOR READ/WRITE MEMORY

4.6.1 General

The MSV11-A is a 1K by 16-bit static MOS read/write memory module which can be used for temporary storage of user programs and data. The storage capacity is 1024 16-bit words. Memory 1K address segment selection can be user-configured by installing or removing jumpers contained on the module. The MSV11-A is capable of either programmed I/O data transfers with the processor or DMA transfers with another LSI-11 bus device.

The MSV11-A features:

- Fast access time
- Low power
- Static MOS memory chips — Refresh not required.
- User-programmed bank and segment address — Five jumpers are provided for this purpose: three are for 4K address selection and two are for a 1K segment within the 4K address space.
- Use of unpopulated 1K segment addresses of MRV11-A — Unpopulated 1K PROM segments on the MRV11-A read-only memory module can be addressed as read/write memory using the MSV11-A. Hence PROM and read/write memory can reside in the same 4K address space.
- Pin and signal compatible with LSI-11 bus-configured backplanes.

4.6.2 Functional Description

Major functions contained on the MSV11-A are shown in Figure 4-25. Memory data can be stored (written) or read by the LSI-11 microcomputer, or other bus master device operating in the DMA mode by executing appropriate bus cycles: DATO (16-bit write operation); DATOB (8-bit byte write operation); DATI (16-bit read operation); or DATIO(B) [16-bit read-modify-write (8 or 16-bit) operation].

Addressing is initiated by a master device (either the LSI-11 processor or a DMA device) by placing the 16-bit address on BDAL0-15 L and asserting BSYNC L, latching the address (and bank select) in the address register. Bus address bits DAL0-15 L are received and distributed to the address register via DAL0-10 H and to the bank/segment address decoder via DAL11-15 H. When the five high-order address bits are equal to the jumper-selected bank and segment address, the decoder asserts SEL H. SEL H is stored (SSEL H) in the address register, along with the 11-bit address, for the duration of the operation.

The memory array can only be accessed when SSEL H and SYNC L are active. SSEL H and SYNC H are ANDed to produce SYNC SEL L, which enables the memory array via the chip enable (CE) inputs on each memory chip. When enabled in this manner, the memory chips respond to stored address bits DAL0-15 H for the duration of the BSYNC L signal.

When in a memory read operation, the bus master device asserts BDIN L after completing the addressing portion of the bus cycle. The addressed 16-bit memory read data is then placed on D0-15 H and applied to the bus driver inputs. The DIN L signal, which enables the bus drivers previously conditioned by an active SYNC L signal, enables memory read data onto the BDAL0-15 bus. Reply logic responds to the active DIN H signal by asserting BRPLY L. This informs the bus master device that memory read data is available on the BDAL bus.

When in a memory write operation (or the write portion of a DATIO(B) cycle), the addressing portion of the bus cycle is similar to read cycle addressing. After the addressing portion of the cycle has been completed, the master device asserts BDOUT L, and BWTBT L is negated if a DATO (word) write cycle is to be performed, or asserted (low) if a DATOB (byte) write cycle is to be performed. Word/byte select logic responds to the 16-bit DATO cycle by asserting both W0 L and W1 L for the duration of the cycle, enabling DAL0-15 H bits to be written into the addressed location in all memory chips. However, in an 8-bit DATOB cycle with BA0 H passive (low = even byte), only W0 L is asserted, enabling DAL0-7 H to be written into the addressed location in the appropriate eight memory chips. Similarly, in a DATOB cycle with BA0 L active (low = odd byte), only W1 L is asserted, enabling DAL8-15 H to be written into the addressed location in the appropriate eight memory chips. The reply logic responds to the active DOUT H signal by asserting BRPLY L, indicating that the data has been written and completing the data transfer.

4.7 DLV11 SERIAL LINE UNIT

4.7.1 General

The DLV11 is the basic interface module used for connecting asynchronous serial line devices to the LSI-11 bus. All circuits are contained on a single 8.5 by 5 inch module.

The DLV11 features:

- Either an optically isolated 20 mA current loop or an EIA interface selected by using the appropriate interface cable option.
- Selectable crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, and an externally supplied rate.
- Jumper-selectable stop bit and data bit formats.
- LSI-11 bus interface and control logic for interrupt processing and vector generation.
- Interrupt priority determined by electrical position along the LSI-11 bus.
- Control/status register (CSR) and data registers compatible with PDP-11 software routines. CSRs and data buffer registers directly accessed via processor instructions.
- Plug, signal, and program compatible with PDP-11 DL11A, B, C series.

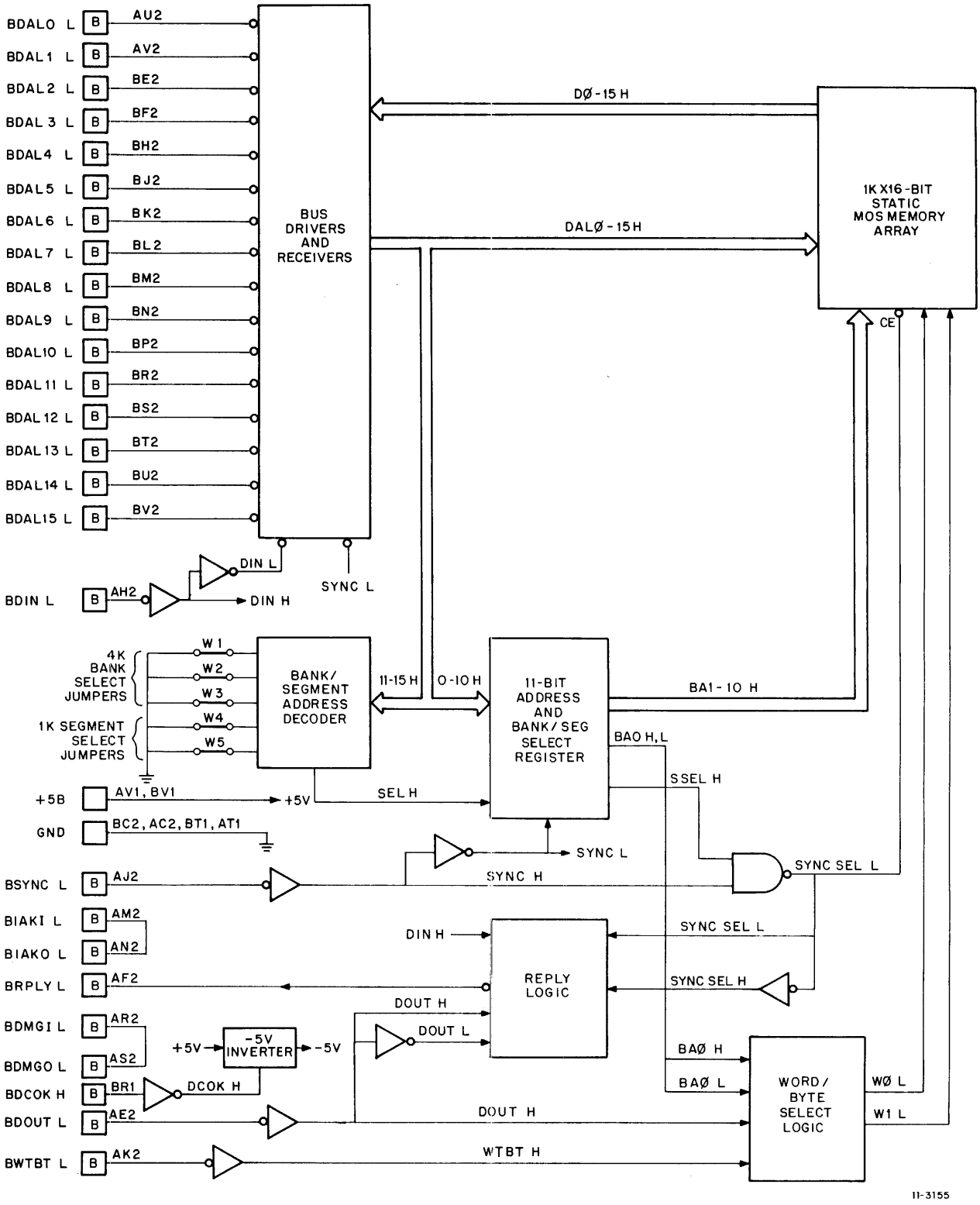


Figure 4-25 MSV11-A Logic Block Diagram

4.7.2 Functional Description

4.7.2.1 General — Major functions contained on the DLV11 module are shown on Figure 4-26. Communications between the LSI-11 microcomputer and the DLV11 are executed via programmed I/O operations or interrupt-driven routines, as described in Chapter 3.

4.7.2.2 UAR/T Operation — The main function on the DLV11 module is the Universal Asynchronous Receiver/Transmitter (UAR/T) chip. This is a 40-pin LSI chip that is capable of parallel I/O with the computer bus and asynchronous serial I/O with an external device. Jumpers which allow the user to select parity functions, number of stop bits, and number of data bits are described in Paragraph 6.2.2. Both transmit and receive functions are totally asynchronous in operation. The transmit clock is always driven by the baud rate generator's CLK L signal. CLK L is applied to one MSPAREB backplane pin (BK1), where it is connected to MSPAREB pin BL1; this is the receive function UAR/T clock input (RCLK L) signal.

When a user application requires split transmit and receive baud rates, the MSPARE jumper can be broken from pins BK1 and BL1 and an external receive baud rate signal can be applied to BL1 (the drive frequency should be 16 times the desired baud rate).

4.7.2.3 Baud Rate Generator — The baud rate generator produces the desired UAR/T clock and a fixed 2.4576 MHz clock for the -12 V inverter circuit. A crystal-controlled oscillator produces the basic 2.4576 MHz frequency for the baud rate generator. A single baud rate generator chip divides this frequency to produce the available baud rates. Jumpers, which are described in Paragraph 6.2.2, select the desired baud rate for the CLK L output signal.

4.7.2.4 Bus Drivers and Receivers — Bus drivers and receivers interface directly with the LSI-11 bus. Line receivers produce RDAB0-12 H signals in response to BDAL0-12 L bus signals. When an input data or vector transfer is desired, function decoding and control logic generates an active INPUT ENABLE signal, which enables the bus drivers. When a data input operation is selected, the UAR/T receiver data buffer contents (RD0-7 H) are routed through the data selector (DDAB0-7H) to the BDAL bus. When responding to an interrupt acknowledge signal, interface control logic generates VEC L, which selects the vector address produced by jumpers W6-W10 (Paragraph 6.2.2). In addition, DAL0, 6, 7, and 15 are driven by CSR selection and gating circuits when a data input transfer from either the receiver (RCSR) or transmitter (XCSR) control/status registers is performed.

4.7.2.5 Address Decoding — Address decoding logic responds to the address present on the bus when BSYNC L is asserted. The DLV11 device address is contained on RDAB3-12 H, along with address bits RDAB0, 1, and 2 H, which are decoded by function decoding logic. Address bits are not required for bank selection since all devices, such as any DLV11, reside in the upper 4K bank (addresses ranging from 28-32K). The processor generates an active BBS7L signal, indicating an I/O device addressing operation. Address selection jumpers A3-A12 allow the user to configure address bits 3-12, as described in Paragraph 6.2.2. When the DLV11 is addressed, device selection is indicated by an active ME signal. This signal remains active throughout the entire I/O cycle (while BSYNC L remains active), enabling function decoding.

4.7.2.6 Function Decoding and Control — Function decoding and control logic decodes DLV11 internal gating functions based upon address selection, address bits RDAB0, 1, and 2 H, bus signals BDIN L, BDOUT L, and BSYNC L, and the VEC L signal generated by the interface control logic. In addition to generating function select signals, this circuit inverts BSYNC L to produce SYNC H whose leading edge clocks the address decoding logic. A truth table of function select signals is provided in Table 4-2.

4.7.2.7 Interface Control Logic — Interface control logic produces the BRPLY L signal in response to I/O operations, contains the interrupt control logic, and receives and distributes the BINIT L initialize signal. This function also contains the Transmit Data Interrupt Enable (TDINTEN H) flip-flop and Receiver Data Interrupt Enable (RDINTEN H) flip-flop; both flip-flops can be read or written by the LSI-11 microcomputer. RDINTEN is set or reset by BDAL6 L; the flip-flop is clocked on the leading edge of SEL0OUT L. Similarly, TDINTEN is set or reset by BDAL6 L; this flip-flop is clocked on the leading edge of SEL4OUT L.

Receiver-generated interrupts occur as a result of the RDINTEN flip-flop being set (interrupts enabled) and an active receiver Data Available (DA H) UAR/T status signal. When this condition occurs, the Receiver Data Interrupt Request flip-flop sets and generated an active BIRQ L signal. The LSI-11 microcomputer responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request

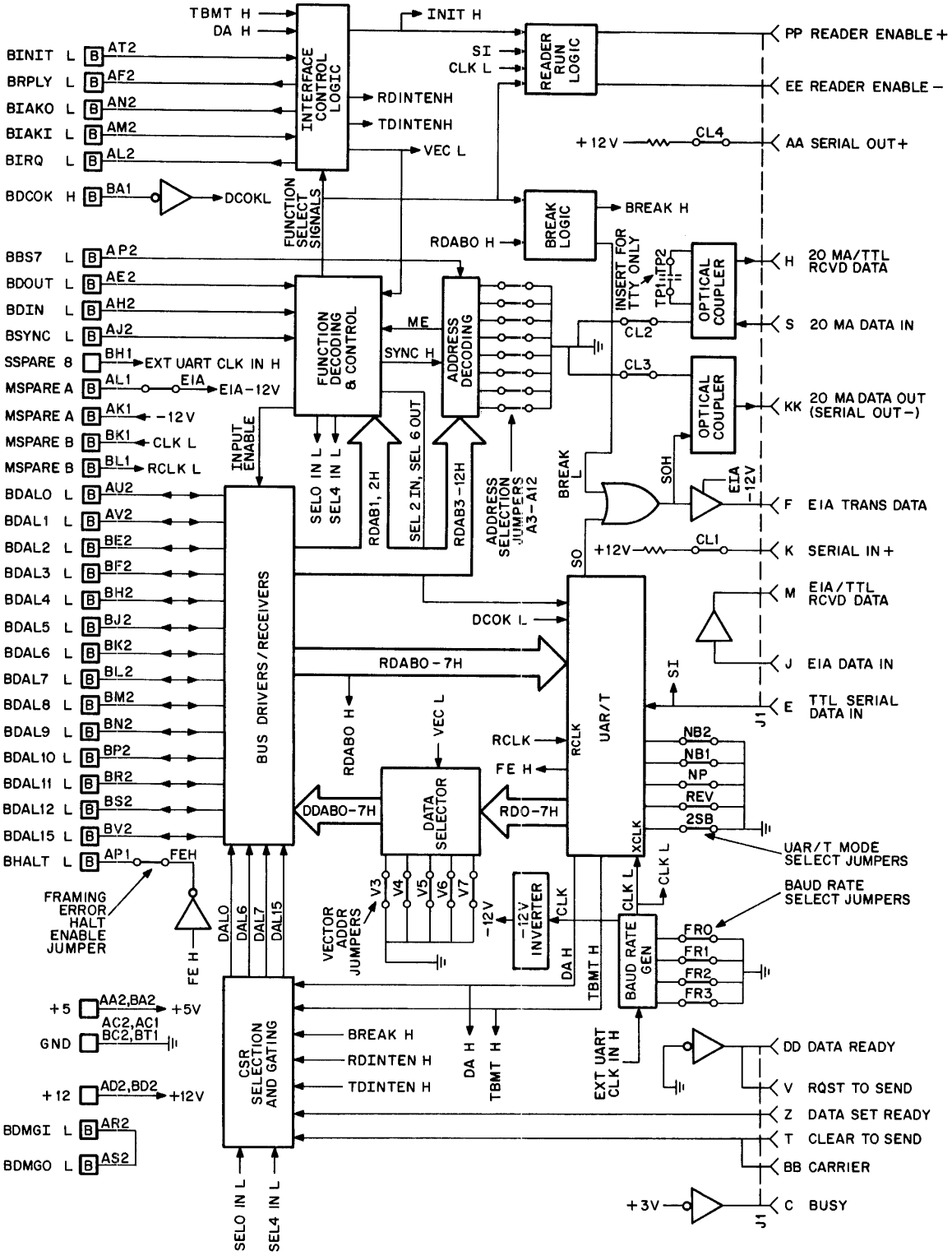


Figure 4-26 DLV11 Logic Block Diagram

Table 4-2
DLV11 Function Decoding

Address Inputs		Control Inputs			Function Select Signals (low-active)						
A1	A2	BDIN L	BDOUT L	ME L	SEL0IN L	SEL2IN L	SEL4IN L	SEL0OUT L	SEL6IN L	SEL4OUT L	SEL6OUT L
X	X	X	X	H	H	H	H	H	H	H	H
L	L	L	X	L	L	H	H	H	H	H	H
H	L	L	X	L	H	L	H	H	H	H	H
L	H	L	X	L	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	L
H	H	L	H	L	H	H	H	H	L	H	H

is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The interface control logic receives BIAKI L and responds by generating active VEC L and BRPLY L signals, placing its interrupt vector on the LSI-11 bus and clearing the BIRQ L signal. Once the service routine for the DLV11's receive function has been entered, the receiver data buffer (RBUF) can be read. The stored BIAK signal is cleared when the next BIAKI L signal is received and the DLV11 is not requesting an interrupt.

Transmitter-generated interrupts occur in a manner similar to the receiver-generated interrupts. However, they occur as a result of the TDINTEN flip-flop being set (interrupts enabled) and when the Transmitter Buffer Empty (TBMT H) UAR/T signal is active (high). Once the service routine has been entered for the DLV11's transmit function, the transmitter data buffer (XBUF) can be loaded and a new character transmission initiated. Note that if the transmitter and receiver functions request interrupts simultaneously, the receiver function has priority over the transmitter. If BIAKI L is received and the DLV11 is not requesting an interrupt, it passes BIAKO L for a lower priority interrupt request.

The interface control logic also generates the DLV11's BRPLY L signal. It generates this signal when any function select signal is asserted or VEC L is generated.

The system initialize signal (BINIT L) is generated by the processor to reset all peripheral device registers. Interface control logic responds by clearing all control flip-flops, including the Interrupt Request, Interrupt Acknowledge, and Break flip-flops. The UAR/T's RBUF and XBUF data registers are not cleared by BINIT L; however, the initialize signal does clear the DA H signal and set the TBMT H signal.

4.7.2.8 CSR Selection and Gating — CSR selection and gating logic enables the LSI-11 microcomputer to read receiver and transmitter control/status bits. Functions are summarized below.

Read RCSR (SEL0IN L asserted)

CARRIER or CLR TO SEND or DATA SET READY → BDAL15

DAH → BDAL7

ROINTEN H → BOAL6

Read XCSR (SEL4IN L asserted)

TBMT H → BDAL7

TDINTEN H → BDAL6

BREAK H → BDAL0

4.7.2.9 Break Logic — Break logic comprises the Break status flip-flop. It is set or cleared by the LSI-11 microcomputer by BDAL0 L while executing a bus output cycle with the XCSR. Thus, the duration of the break signal is program controlled. The Break flip-flop is clocked on the leading edge of the SEL4-OUT H signal. When set, the serial output line is continuously asserted (space). The status of the Break flip-flop can be read in XCSR bit 0.

4.7.2.10 Reader Run Logic — The reader run logic enables DLV11 generation of a READER RUN pulse for 20 mA current loop teletypewriter devices. It is enabled by loading RCSR bit 0; the LSI-11 microcomputer asserts BDAL0 L and causes generation of the SEL0OUT H signal (load RCSR). READER RUN is asserted and remains active for the duration of one-half of a start bit. The start bit of the serial input (SI) from the low-speed reader initiates a 4-bit binary counter. When eight CLK L pulses have been counted (equivalent to one-half of the start bit), READER RUN is negated. After the complete character has been read by the LSI-11 microcomputer, the next character can be read in the same manner.

4.7.2.11 EIA Interface Circuits — An EIA interface is provided by EIA drivers and receivers. EIA signal drivers are provided for EIA TRANS DATA, RQST TO SEND, DATA TERMINAL READY (always an active high/space state), and BUSY (always an active

low/mark state). Jumper EIA applies -12 V to the EIA driver chip when the DLV11 is used with EIA-compatible devices. EIA signal receivers are provided for EIA DATA IN, CARRIER or CLEAR TO SEND, and DATA SET READY. The optional BC05C modem cable connects the output signal of the EIA DATA IN driver (EIA/TTL RCVD DATA) to the TTL SERIAL DATA IN input to the UAR/T.

4.7.2.12 20 mA Loop Current Interface — The 20 mA loop current interface is provided by optical isolation. An active 20 mA current loop is provided when jumpers CL1 through CL4 are installed. If the jumpers are removed, 20 mA passive current loop operation is selected. The optional BC05M cable assembly connects the 20 mA/TTL RCVD DATA optical coupler signal output to the TTL SERIAL DATA IN input of the UAR/T. When the DLV11 is used with a 110 baud teletypewriter device, a 0.005 μF, 100 V filter capacitor should be installed between terminals TP1 and TP2.

4.7.2.13 -12 V Inverter — The -12 V inverter circuit generates -12 V for use by the UAR/T chip and EIA driver and receiver chips. Input to the circuit is the CLK signal (2.4576 MHz) and +12 V. The output is zener regulated to -12 V.

4.8 DRV11 PARALLEL LINE UNIT

4.8.1 General

The DRV11 is a general-purpose interface unit used for connecting parallel line devices to the LSI-11 bus. All circuits are contained on a single 8.5 by 5 inch module.

The DRV11 features:

- 16 diode-clamped data input lines.
- 16 latched output lines.
- 16-bit word or 8-bit byte programmed data transfers.
- User-assigned device address decoding.
- LSI-11 bus interface and control logic for interrupt processing and vector generation.
- Interrupt priority determined by electrical position along the LSI-11 bus.
- Control/status registers (CSR) and data registers that are compatible with PDP-11 software routines. Plug, signal, and program compatible with DR11-C.
- Four control lines to the peripheral device for NEW DATA READY, DATA TRANSMITTED, RQSTA, and RQSTB.
- Logic compatible with TTL or DTL devices.
- Program-controlled data transfer rate of 90K words per second (maximum).
- Maximum drive capability of 25 ft of cable.

4.8.2 Functional Description

4.8.2.1 General — Major functions contained on the DRV11 module are shown in Figure 4-27. Communications between the LSI-11 microcomputer and the DRV11 are executed via programmed I/O operations or interrupt-driven routines, as described in Chapter 3.

The DRV11 is capable of storing one 16-bit output word or two 8-bit output bytes in DROUTBUF. The stored data (OUT0-15 H) is routed to the user's device via an optional I/O cable connected to J1. Any programmed operation that loads either a byte or a word in DROUTBUF causes a NEW DATA READY H signal to be generated, informing the user's device of the operation.

Input data (DRINBUF) is gated onto the BDAL bus during a DATI bus cycle. All 16 bits are placed on the bus simultaneously; however, when the processor is involved in 8-bit byte operation, it uses only the high or low byte. When the data is taken by the processor, a DATA TRANS H pulse is sent to the user's device to inform the device of the data transfer.

4.8.2.2 Addressing — When addressing a peripheral device interface such as the DRV11, the processor places an address on BDAL0-15 L, which is received and distributed as BRD0-15 H in the DRV11. The address is in the upper 4K (28-32K) address space. On the leading edge of BSYNC L, the address decoder decodes the address selected by jumpers A3-A12 and sets the Device Selected flip-flop (not shown); the active flip-flop output is the ME signal, which enables function selection and I/O control logic operation. At the same time, function selection logic stores address bits BRD0-2.

4.8.2.3 Function Selection — Function selection and I/O control logic monitors the ME signal and bus signals BDIN L, BDOUT L, and BWTBT L. It responds by generating appropriate Select signals which control internal data gating, NEW DATA READY H or DATA TRANS H output signals for the user's

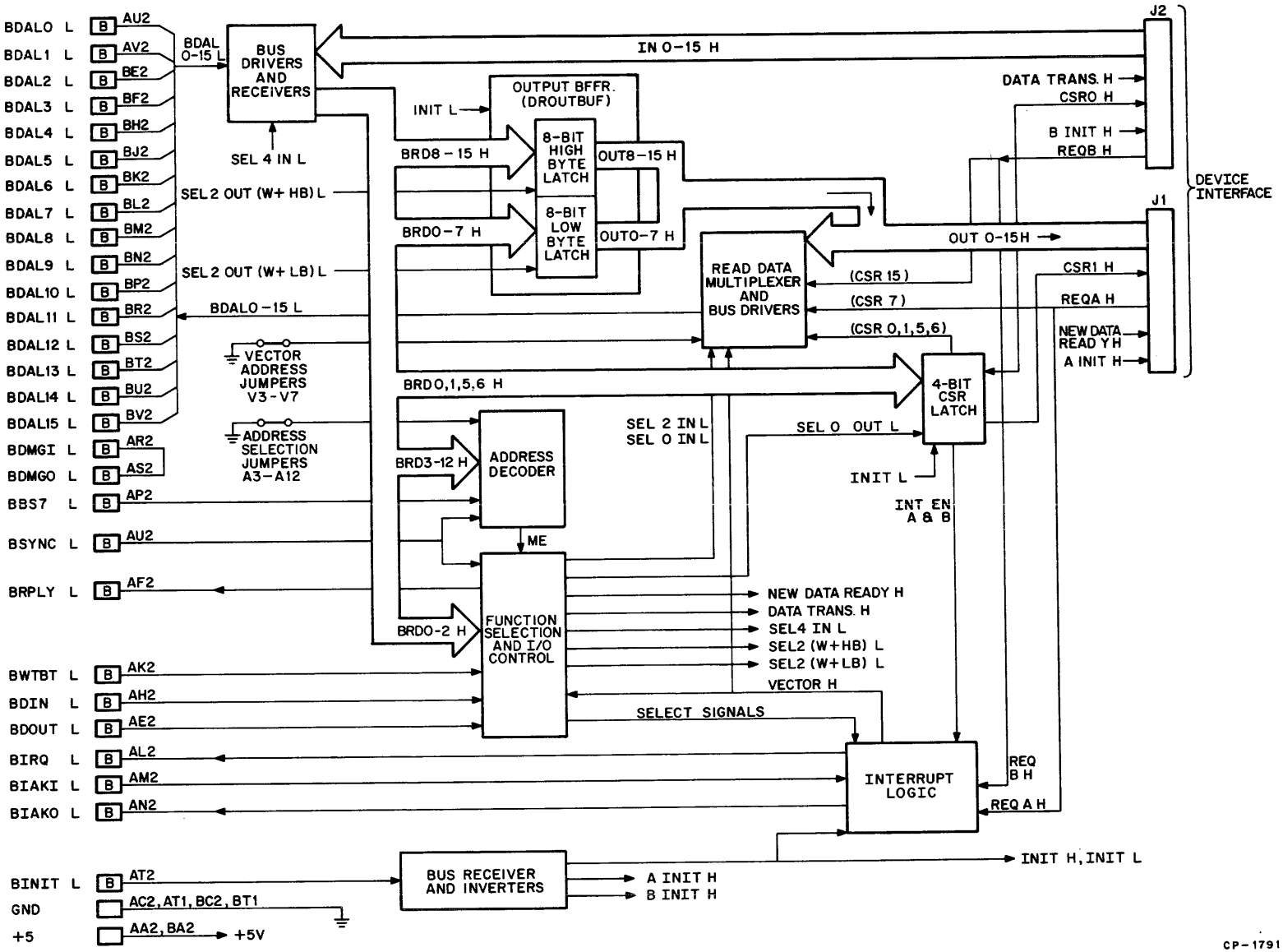


Figure 4-27 DRV11 Logic Block Diagram

Table 4-3
DRV11 Device Function Decoding

Programmed Operation	Stored Device Addr. Bits 0-2	BWTBT L During Data Transfer	BDIN L	BDOUT L	Bus Cycle Type	Select Signals
Write DRCSR	0 0	0 1	H H	L L	DATO DATOB	SEL0OUT L
Read DRCSR	0	0	L	H	DATI or DATIP	SEL0IN L
Write DROUTBUF Word	2	0	H	L	DATO	SEL2OUT (W+HB) L, SEL2OUT (W+LB) L, and NEW DATA READY H
Low Byte	2	1	H	L	DATOB	SEL2OUT (W+LB) L and NEW DATA READY H
High Byte	3	1	H	L	DATOB	SEL2OUT (W+HB) L and NEW DATA READY H
Read DROUTBUF	2	0	L	H	DATI or DATIP	SEL2IN L
Read DRINBUF	4	0	L	H	DATI	SEL4IN L and DATA TRANS H

NOTE
When addressed, the DRV11 always responds to either BDIN L or BDOUT L by asserting BRPLY L [L = assertion].

device, and the BRPLY L bus signal which informs the processor that the DRV11 has responded to the programmed I/O operation. Since the DRV11 appears to the processor as three addresseable registers (DRCSR, DROUTBUF, and DRINBUF) that can be involved in either word or byte transfers, the three low-order address bits stored during the addressing portion of the bus cycle are used for function selection. The select signals relative to I/O bus control signals and address bits 0-2 are listed in Table 4-3.

NEW DATA READY H is active for the duration of BDOUT L when in a DROUTBUF write operation. This signal is normally active for 300 ns. However, by adding an optional capacitor in the BRPLY L portion of the circuit, the leading edge of BRPLY L is delayed, effectively increasing the duration of the NEW DATA READY H pulse to 1200 ns (maximum); adding the capacitor also increases the DATA TRANS H pulse width in exactly the same manner.

DATA TRANS H is active for the duration of BDIN L when in a DRINBUF read operation. This signal is normally active for 300 ns. The time, however, can be extended by adding the optional capacitor to the BRPLY L portion of the circuit as previously described.

4.8.2.4 Read Data Multiplexer — The read data multiplexer selects the proper data and places it on the BDAL bus when the processor inputs DRCSR, DROUTBUF or interrupt vectors; DRINBUF contents are gated onto the bus separately. The select signals (previously described) and VECTOR H, produced by the interrupt logic, control read data selection.

4.8.2.5 DRCSR Functions — The control/status register (DRCSR) is comprised of separate functions. Four of the six significant DRCSR bits can be involved in either write or read operations. The remaining two bits, 7 and 15, are read-only bits that are controlled by the external device via the REQ A H and REQ B H signals, respectively. The four read/write bits are stored in the 4-bit CSR latch. They represent CSR0 and CSR1 (DRCSR bits 0 and 1, respectively), which can be used to simulate interrupt requests when used with an optional maintenance cable. INT ENB A and INT ENB B (bits 6 and 5, respectively) enable interrupt logic operation. Note that CSR0 and CSR1 are available to the user's device for any user application.

4.8.2.6 DRINBUF Input Data Transfer — DRINBUF is an addressable 16-bit read-only register that receives data from the user's device for transmission to the LSI-11 bus. Data to be read is provided by the user's device on the IN0-15 H signal lines. Since the input buffer consists of gating logic rather than a flip-flop register, the user's device must hold the data on the lines until the data input transaction has been completed.

The input data is read during a DATI sequence while bus drivers are enabled by the SEL4IN L signal. The DATA TRANSMITTED pulse that is sent to the user's device by the function select logic informs the device of the transaction. Input data can be removed on the trailing edge of this pulse.

4.8.2.7 DROUTBUF Output Data Transfer — DROUTBUF is comprised of two 8-bit latches, enabling either 16-bit word or 8-bit byte output transfers. Two SEL 2 signals function as clock signals for the latches. When in a DATO bus cycle, both signals clock data from the internal BRD0-15 H bus into the latches. However, when in a DATOB cycle, only one signal clocks data into an 8-bit latch, as determined by address bit 0 previously stored during the addressing portion of the bus cycle.

The NEW DATA READY H pulse generated by the function select logic is sent to the user's device to inform the device of the data transaction. The data can be input to the device on the trailing edge of this pulse.

4.8.2.8 Interrupts — The DRV11 contains LSI-11 bus-compatible interrupt logic that allows the user's device to generate interrupt requests. Two independent interrupt request signals (REQ A H and REQ B H) are capable of requesting processor service via separate interrupt vectors. In addition, DRCSR contains two interrupt enable bits (INT EN A and INT EN B) (bits 6 and 5, respectively), which independently enable or disable interrupt requests. REQ A and REQ B status can be read by the processor in DRCSR bits 7 and 15, respectively. Since separate interrupt vectors are provided for each request, one of the requests could be used to imply that device data is ready for input and the remaining request could be used to imply that the device is ready to accept new data.

An interrupt sequence is generated when a DRCSR INT EN bit (A or B) is set and its respective REQ signal is asserted by the device. The processor responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The DRV11 receives BIAKI L and the interrupt logic generates

VECTOR H, which gates the jumper-addressed vector information through the read data multiplexer and bus drivers and onto the LSI-11 bus. The processor then proceeds to service the interrupt request as described in Chapter 3.

4.8.2.9 Maintenance Mode — The maintenance mode allows the user to check DRV11 operation by installing an optional BC08R cable between connectors J1 and J2. This maintenance cable allows the contents of the output buffer DROUTBUF to be read during a DRINBUF DATI bus cycle. In addition, interrupts can be simulated by using DRCSR bits CSR0 and CSR1. CSR1 is routed via the cable directly to the REQ B H input and CSR0 is routed to the REQ A H input. By setting or clearing INT EN A, INT EN B, and CSR0 and CSR1 bits in the CRCSR register, a maintenance program can test the interrupt facility.

4.8.2.10 Initialization — BINIT L is received by a bus driver, inverted, and distributed to DRV11 logic to initialize the device interface. The buffered initialize signal is available to the user's device via the AINIT H and BINIT H signal lines. DRV11 logic functions cleared by the BINIT signal include DROUTBUF, CRCSR (bits 0, 1, 5, and 6), and interrupt logic.

4.9 H780 POWER SUPPLY

4.9.1 General

The H780 power supply provides dc operating power to all backplane slots contained in a PDP-11/03 microcomputer system. Depending upon the configuration ordered, the primary power input is 115 or 230 Vac, 50 or 60 Hz. In addition to providing operating power, the H780 generates power supply status and line time clock signals which are distributed over the LSI-11 bus. Three LED indicators and three switches are on the H780's front panel. The indicators include RUN, which illuminates when the LSI-11 processor is in the run state, and DC ON, which illuminates when normal dc operating voltages are applied to the LSI-11 backplane. The DC ON indicator status is controlled by circuits contained in the H780. The DC ON/OFF switch allows the operator to turn off the H780 dc output voltages without turning off system primary power. This allows safe module installation or removal with no dc power applied to the backplane. A normal power-up/power-down sequence is produced when this switch is operated. The ENABLE/HALT switch enables the operator to manually assert the BHALT L bus signal, causing the LSI-11 microcomputer to execute the console (ODT) microcode. When in the ENABLE position, program execution can be initiated via console ODT commands. The LTC ON/OFF switch enables or disables H780 generation of the line time clock (BEVNT L) signal. One spare LED indicator is included. Two fans provide cooling air for the H780 power supply and all modules contained in the PDP-11/03 enclosure.

The H780 features:

- +5 V ± 3%, 18 A (maximum) and +12 V ± 3%, 3.5 A (maximum); combined dc power must not exceed 120 W.
- Overcurrent/short circuit protection — Output voltages return to normal after removal of overload or short. Current limited to approximately 1.2 times the normal maximum rating.
- Overvoltage protection — +5 V limited to +6.3 V (approx); +12 V limited to +15 V (approx).
- Dual primary power configuration — Can be connected for nominal 115 V, 60 Hz or 230 V, 50 Hz input power.
- Efficiency — Switching regulator circuits provide greater than 65 percent overall efficiency.
- System control/indicator panel — A simple system control/indicator panel allows the user to control dc power on/off and microcomputer Run/Halt mode. Indicators display the actual dc power and processor status.
- Line Time Clock — A bus-compatible signal is generated by the power supply for the event (line time clock) interrupt input to the processor. This signal is either 50 or 60 Hz, depending upon primary power line frequency input to the power supply.
- Power Fail/Automatic Restart — Fault detection and status circuits monitor ac and dc voltages and generate bus-compatible BPOK H and BDCOK H signals (respectively) to inform the LSI-11 system modules of power supply status.
- Fans — Built-in fans provide cooling for the power supply and LSI-11 modules contained in the PDP-11/03 enclosure.

4.9.2 Specifications

Electric

Input Voltage
100—127 V rms, 50 ± 1 Hz or 60 ± 1 Hz
200—254 V rms, 50 ± 1 Hz or 60 ± 1 Hz

Input Power (full load)
400 W maximum

Output Voltages
+5 V ± 3%, 0—18 A load (static and dynamic)
+12 V ± 3%, 0—3.5 A load (static and dynamic)
Maximum output power: 120 W (total)

Output Protection
Current limited to 1.2 times maximum normal rating (approximately)
Voltage +5 V and +12 V outputs limited to +6.3 V (nominal) and +15 V (nominal). respectively

Output Ripple
5 V output: Less than 100 mV pk-to-pk
12 V output: Less than 200 mV pk-to-pk

Output Regulation
Line: +5 V, 1.0% max
+12 V, 0.5% max
Load: (Static and dynamic ($\Delta I < 0.1$ A/μs):
+5 V, 1% max
+12 V, 0.5% max
Load Interaction: 1.0%

Load Term Stability
0.2%/1000 hr max

Line Protection
H780A (115 V input): Fast blow 5 A fuse
H780B (230 V input): Fast blow 3 A fuse

Noise
AC component above 100 kHz meets DEC STD 102.7; H780B units will meet VDE N-12 limits for European environment.

Front Panel Control and Indicators
DC ON/OFF switch
RUN/HALT switch
LTC ON/OFF switch
RUN indicator
DC ON indicator
Spare indicator

Rear Panel Controls and Indicators
AC ON/OFF power switch

Backplane Signals
BPOK H
BDCOK H
BEVNT L
BHALT L
SRUN L

Mechanical

Cooling
Two self-contained fans provide 200 LFPM air flow.

Size
5-1/2 in. w × 3-1/2 in. h × 14-5/8 in.

Weight
13 lbs

Environmental

Temperature
5°—50° C operating

Humidity
90% maximum without condensation

4.9.3 Functional Description

4.9.3.1 General — Major functions contained in the H780 power supply are shown in Figure 4-28. These functions include circuits which produce unregulated dc voltage and regulated dc voltage for H780 circuit operation, +5 V and +12 V switching regulators, overload and short-circuit protection, +5 V and +12 V crowbar (overvoltage protection) circuits, and logic signal generation circuits. The following paragraphs describe each of these functions in detail.

4.9.3.2 Unregulated Voltage and Local Power — Unregulated voltage and local power circuits provide operating dc power for power supply logic and control circuits, and dc power for the +5 V and +12 V regulator circuits. These circuits are shown in Figure 4-29. AC power is supplied to the H780 via an ac input plug and cable. A toggle switch mounted on the rear of the H780 assembly applies ac power to the power supply. Normally, this switch remains in the ON position, allowing ac power to be controlled by power distribution and control circuits in which the PDP-11/03 system is installed. Primary circuit overload protection is provided by a fuse mounted on the rear of the H780 unit. Primary power circuits are factory-wired for 115 Vac (model H780A) or 230 Vac (model H780B) operation. Power transformer primary windings and the two fans operate directly from the switched ac power.

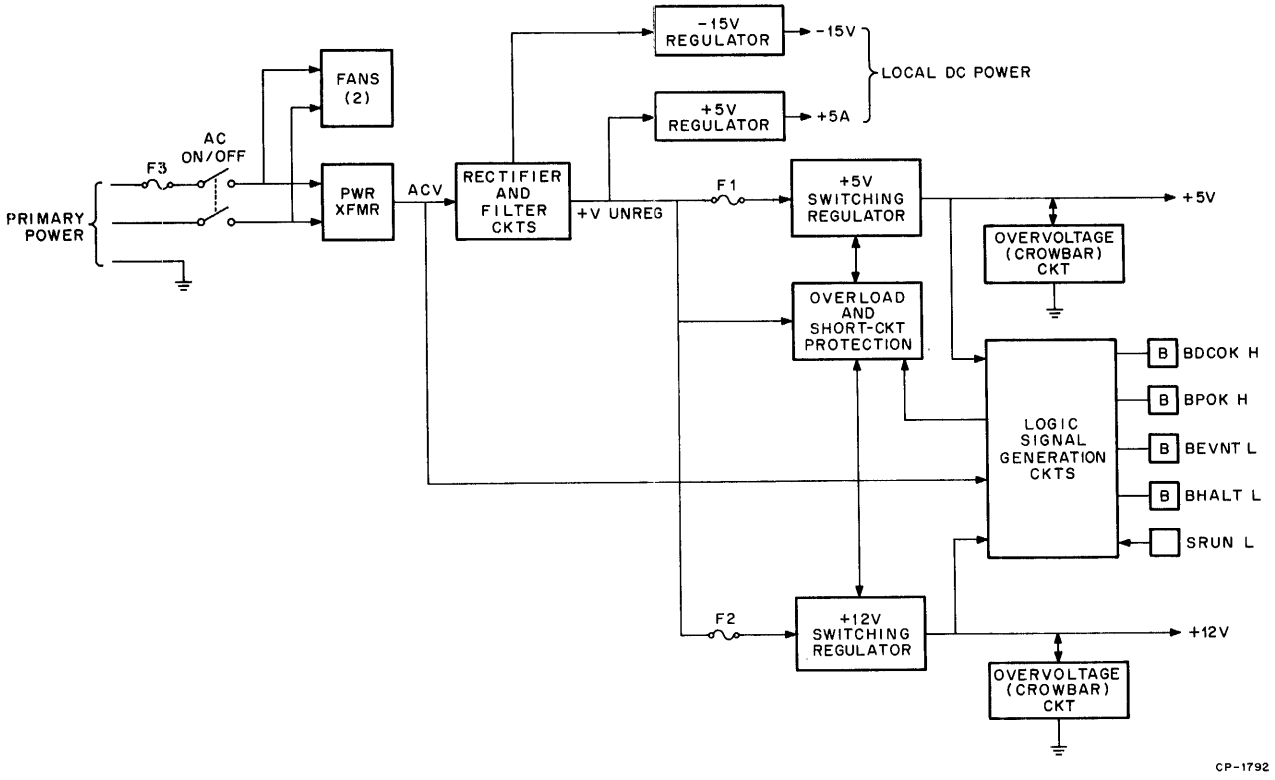


Figure 4-28 H780 Power Supply Block Diagram

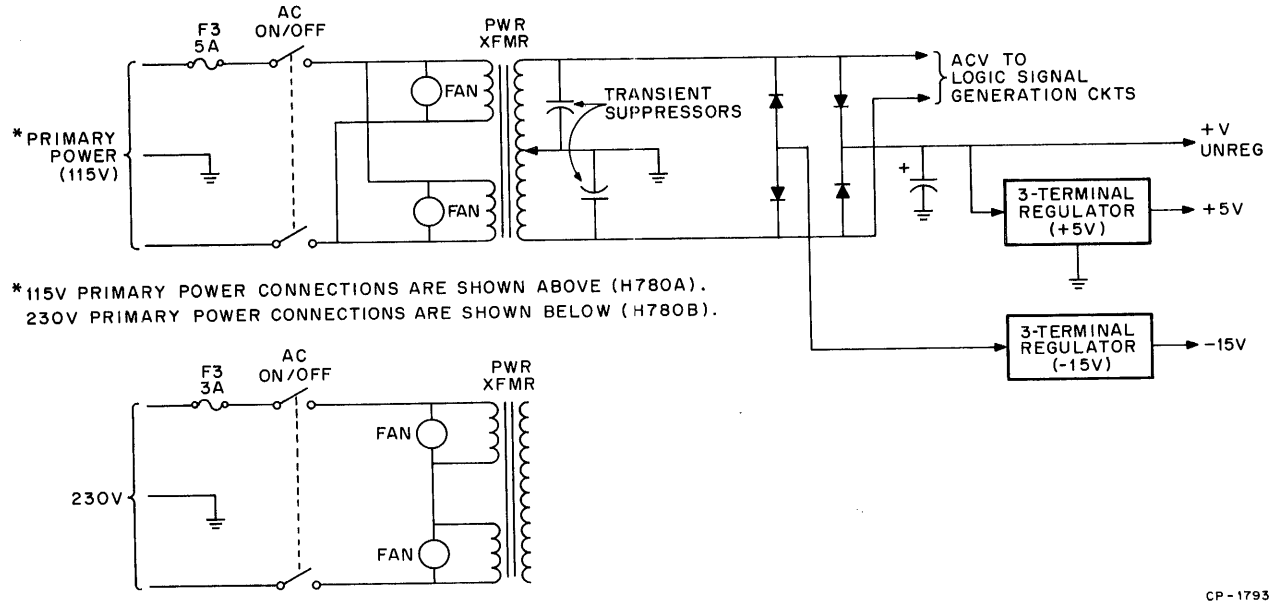


Figure 4-29 Unregulated Voltage and Local DC Power

A single center-tapped secondary winding supplies power for regulator circuits and internal circuit operation. Conventional full-wave rectifiers and a -15 V, 3-terminal regulator IC provide regulated voltage for internal distribution. The rectifiers also provide +24 V (approx) for internal distribution and regulator operation. A 3-terminal regulator integrated circuit provides +5 V logic and control power for H780 circuits. The +5 V and +12 V regulators use the same +24 V unregulated voltage for regulation and distribution to LSI-11 modules. AC voltage from one side of the transformer secondary is also routed to the line time clock (LTC) circuit, which generates a BEVNT L bus signal for a line time clock processor interrupt. When used with a 60 Hz line frequency, the interrupt occurs at 16.667 ms intervals; a 50 Hz line frequency will produce interrupts at 20 ms intervals.

4.9.3.3 Basic Regulator Circuit — Both +5 V and +12 V regulator circuits receive the +24 V unregulated input power. The +5 V and +12 V regulator circuits are identical except for component values. Hence, only the basic +5 V regulator is described in detail.

The basic regulator is a switching regulator which operates at approximately 20 kHz. The main controlling element is a 3-terminal regulator which operates at approximately the regulated output voltage level. Basic regulator circuits are shown in Figure 4-30. Note that the ground terminal of the 3-terminal regulator is connected to a potentiometer, allowing factory adjustment of the terminal voltage over a -0.7 to +0.5 V range. Hence, the 3-terminal regulator output in the +5 V regulator circuit can range from 4.3 to 5.4 V (approx).

Normal switching regulator operation is accomplished when the control transistor is turned on. Forward bias for the control transistor is supplied via R14. It is turned off only during fault conditions (overcurrent or shorted output voltage) or when the input ac line voltage is below specifications. Its emitter supplies unregulated voltage to the 3-terminal regulator. At less than 50 mA regulator output current (approx), the 3-terminal regulator supplies the output voltage. However, as load current through the 3-terminal regulator is increased beyond this value, the voltage drop across R27 forward biases the driver transistor. The pass switch transistor then turns on and applies the unregulated +24 V to L2. The output capacitor then charges toward the +5 V value, current limited by the inductance of L2. When the output voltage rises to the 3-terminal regulator regulation voltage, the 3-terminal regulator turns off; current through R27 stops, and the

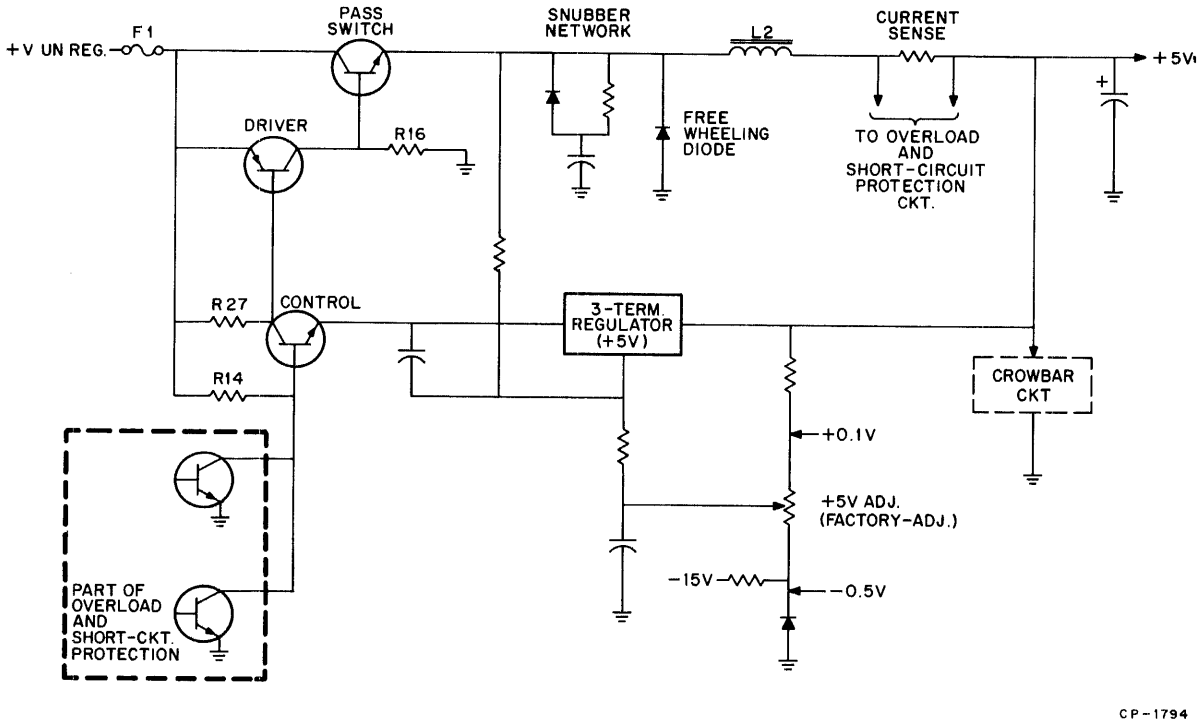


Figure 4-30 Basic Regulator Circuit

driver transistor is not forward biased. Hence the driver and pass switch transistors cut off. The energy stored in L2 continues to charge the capacitor bank slightly beyond the designed output voltage via the freewheeling diode and the current sense resistor. Once the inductor's stored energy is spent, the load discharges the output capacitor until the output voltage drops below the 3-terminal regulator's regulation voltage. At that point, current through R27 increases and turns on the driver and pass switch transistors, and the cycle repeats. Note that as the load is increased, the pass switch must remain on longer in order to charge the output capacitor to the regulated voltage value. This process repeats at a 12—20 kHz rate, producing the switching regulator operation.

Switching losses in the pass switch transistor are minimized by the snubber network. This network operates during the "off" switching transient (as the pass switch is biased off) by controlling the rate of increasing collector to emitter voltage as collector current decreases.

The control transistor is turned off during a fault condition by overload and short-circuit protection circuits. When a fault condition is detected, the control transistor's base voltage drops to nearly 0 V, causing it to cut off. When cut off, operating voltage is removed from the 3-terminal regulator and R27 current is 0, disabling the switching regulator circuit.

4.9.3.4 Overload and Short-Circuit Protection — Each H780 dc output is overload and short-circuit protected. When in an overload condition, excessive power supply current is sensed, causing both switching regulators to go off and then cycle on and off at a low-frequency rate (approximately 7.5 Hz) until the overload is removed. Each time the power supply cycles on, the circuit checks for the overload condition. If the load current returns to normal, the 20 kHz switching regulator operation resumes.

Overcurrent sensing circuits for +5 V and +12 Vdc outputs are identical except for component values. A 5 V power supply overcurrent condition results in an increased voltage drop across the current sense resistor (Figure 4-31), forward biasing the current sense transistor. (During normal operation, this transistor is not forward biased.) Current sense transistor collector voltage then drops from the normal +24 V (approx) to the +5 V regulator output value; this voltage, which is less than the +16 V reference applied to the current limit comparator's inverting input, is diode-coupled to the comparator's non-inverting input, causing the comparator's output to go low; the diode coupling provides an OR logic function for both +5 V and +12 V overcurrent fault conditions. The comparator's low output signal triggers the 20 μs one-shot whose OVERCURRENT L pulse output triggers the 135 ms one-shot and sets the Current Limit flip-flop. The OVERCURRENT L pulse is also ORed with the

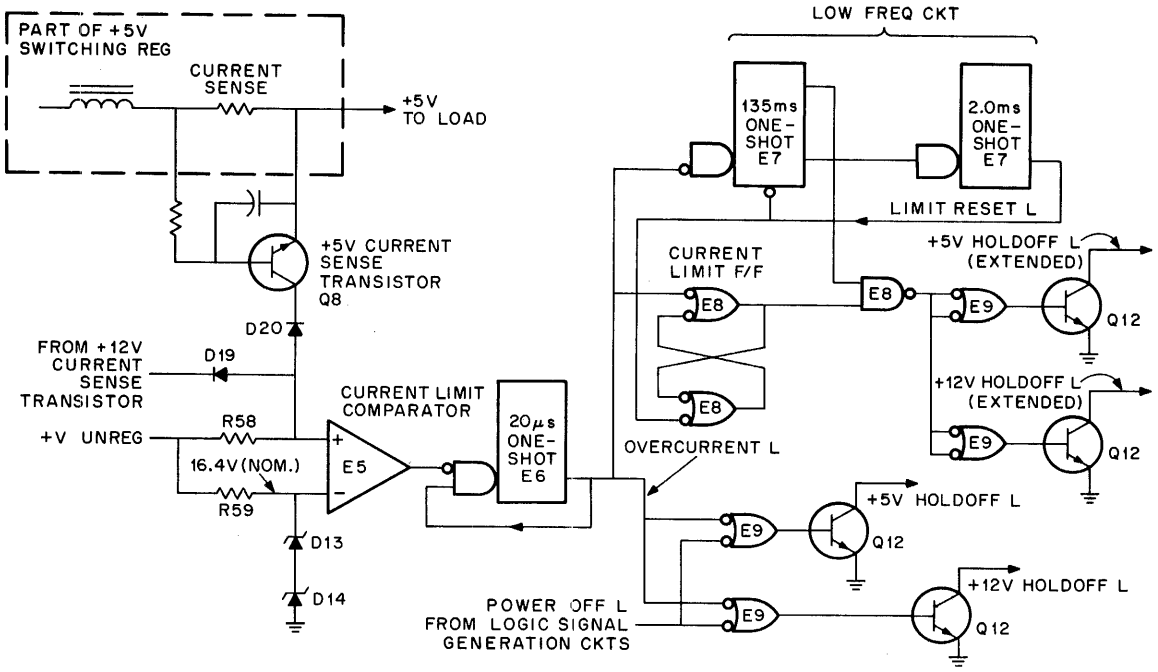


Figure 4-31 Overload and Short-Circuit Protection

POWER OFF L signal, turning on the +5 V and +12 V hold-off transistors. Both switching regulators are then disabled. The high 135 ms one-shot output pulse is ANDed with the Current Limit flip-flop output, turning on +5 V and +12 V extended hold-off transistors. Hold-off signals remain in this state and inhibit switching regulator operation for the 135 ms pulse duration. At the end of this time, the 135 ms one-shot resets, terminating the delayed hold-off signals, and triggers the 2.0 ms one-shot. Its active low output resets the Current Limit flip-flop and clears the 135 ms one-shot for 2.0 ms, allowing the regulator pass switch transistors to operate for 2 ms (minimum). At the end of this time, the 135 ms one-shot is again enabled (the clear input goes high) and a new overcurrent cycle is enabled. If the overload is removed, normal operation resumes; otherwise, the overload causes a new overload condition to occur and the cycle repeats, as described above.

Switching regulator operation is suspended when the operator places the DC ON/OFF switch in the OFF position. Logic signal generation circuits respond by immediately asserting BPOK H low to initiate a processor power-fail sequence. After a 5—10 ms "pseudo delay," POWER OFF L is asserted low. This low signal is wire-ORed with OVERCURRENT L, inhibiting the switching regulator operation, and dc power is removed from the backplane.

4.9.3.5 Crowbar Circuits — Crowbar circuits are connected across both +5 V and +12 V power supply outputs for overvoltage protection. An overvoltage condition could occur if +12 V and +5 V outputs shorted together, or if a driver or switch transistor becomes shorted. When shorted to a higher voltage source, the crowbar fires, shorting the supply voltage that it is protecting to ground (dc return). In this condition, the overload and short-circuit protection circuits respond by limiting the duty cycle of the switch transistor until the overvoltage source is removed. However, when the overvoltage is caused by a shorted driver or switch transistor, short-circuit protection is ineffective, and the excessive current caused by the crowbar circuit firing will blow the regulator's fuse (F1 for +5 V or F2 for +12 V).

The crowbar circuit for the +5 V output is shown in Figure 4-32. It comprises a 5.6 V zener diode D9, diode D8, programmable unijunction transistor Q9, and silicon-controlled rectifier (SCR) Q15. R19, D8, and D9 supply the 6.1 Vdc (approx) crowbar reference (threshold) voltage to the gate of Q9 via R21. Q9 is normally off and its cathode supplies a 0 V gate input to Q15. An overvoltage is coupled into the circuit via C7, causing the gate voltage of Q9 to rise; this triggers Q9 and its cathode voltage rises to the output (overvoltage) potential. Q15 then fires and shorts (crowbars) the supply output. The circuit remains in this condition until the overvoltage is removed (Q15 current goes to zero) and either the power supply switch transistor is off due to short circuit protection, or the regulator's dc fuse opens.

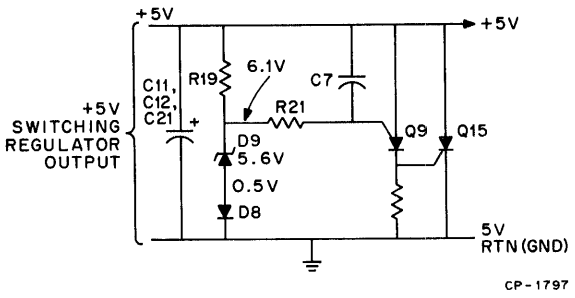


Figure 4-32 Crowbar Circuit

The +12 V crowbar circuit functions in a similar manner. However, the reference voltage for this power supply is approximately 13.5 V.

4.9.3.6 Logic Signal Generation — Logic signal generation circuits produce LSI-11 bus signals for power normal/power fail and line time clock interrupt functions and processor Run-Enable/Halt mode. The RUN indicator circuit monitors the SRUN L backplane (nonbused) signal and provides an active display when the processor is in the Run mode. BPOK H and BDCOK H indicate power status. When both are high, power to the LSI-11 bus is normal and no power fail condition is pending. However, if primary power goes abnormally low (or is removed) for more than 16.5 ms, BPOK H goes low and initiates a power-fail processor interrupt. If the power-fail condition continues for more than an additional 4 ms, a "pseudo delay" circuit causes BDCOK H to go low. The circuit also causes the overload and short-circuit protection circuit to inhibit +5 V and +12 V control transistors; normal output voltages are available for 50 μs (minimum) after BDCOK H goes low (depending on the loading of the dc output voltages). The DC ON/OFF switch simulates an AC ON/OFF operation by turning switching regulators on or off without turning system primary power off. A normal power-up/power-down sequence is produced by this circuit. The line time clock circuit produces a processor interrupt at the power line frequency (either 50 or 60 Hz). The circuit simply asserts the BEVNT L line at the line frequency.

DC voltage monitor circuits respond to both +5 V and +12 V power supply outputs. A +2.5 V reference at the voltage comparator's noninverting input is established by +5 A and a voltage divider comprised of R25 and R3, as shown in Figure 4-33. Voltages are sensed at the anodes of diodes D17 and D18. The cathode of D17 is connected directly to the +5 V output. D18 is connected to a voltage divider

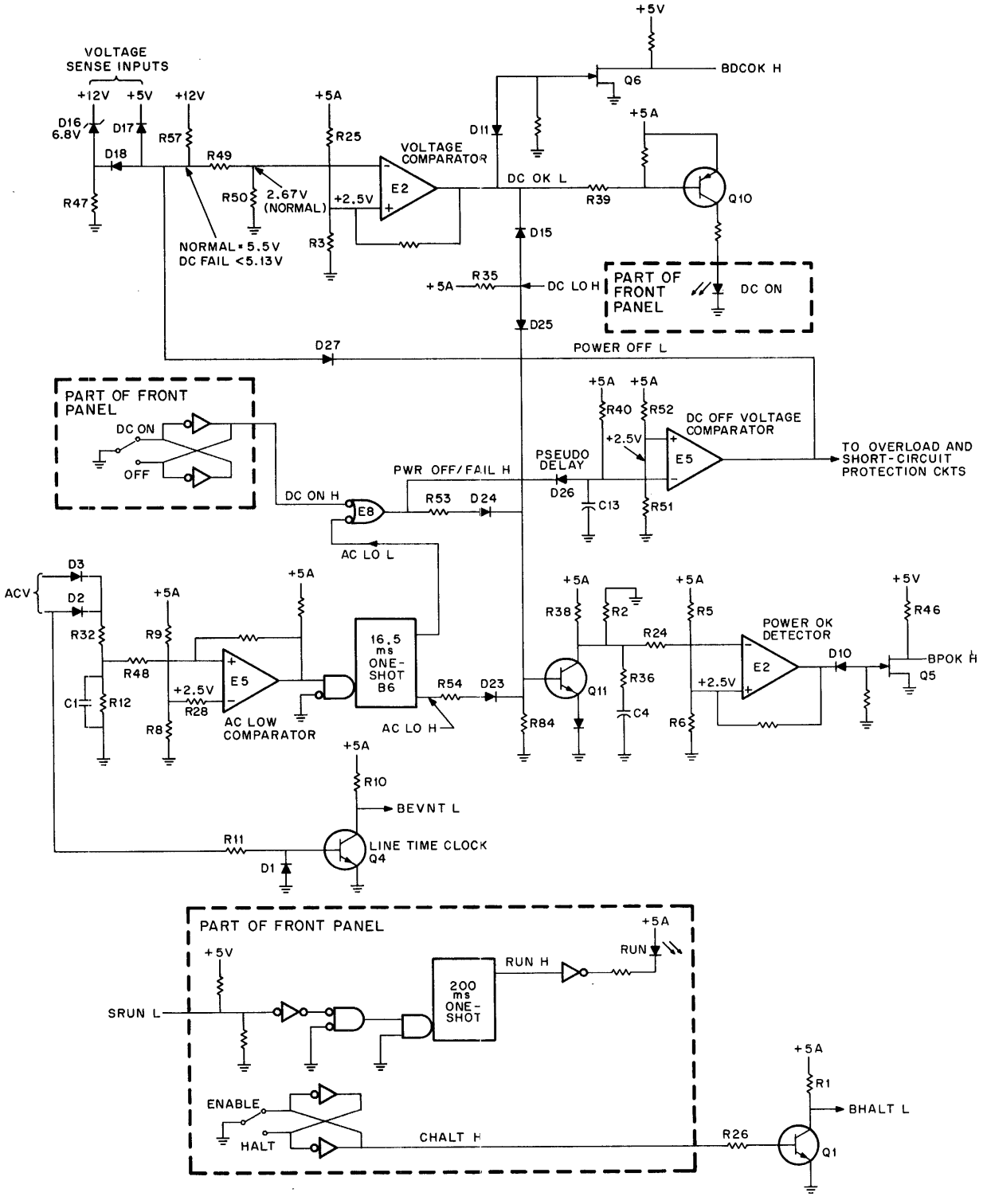


Figure 4-33 Logic Signal Generation

comprising 6.8 V zener diode D16 and R47. The sensed voltage is always 6.8 V less than the +12 V power supply output voltage (but not less than 0 V). Normally, the junction of D17, D18, R57, and R49 is clamped to +5.5 V (nominal) via D17, which is connected to the +5 V output. Voltage divider R49 and R50 provide a portion of the sensed voltage to the comparator's inverting input. This voltage is normally 2.7 V, causing the comparator's output to go low. The low signal forward biases DC ON panel indicator driver transistor Q10, producing a DC ON indication, and reverse biases the BDCOK H FET bus driver Q6. As a result, Q6 cuts off, and its source voltage rises to +5 V, producing the active BDCOK H signal.

A low +5 V output results in a decrease in voltage at the voltage comparator's inverting input. A voltage less then 4.6 V reduces the voltage at the comparator's inverting input to less than the +2.5 V reference. Hence, the comparator's output goes high, turning off the DC ON indicator and allowing Q6 to conduct. Q6 asserts the BDCOK H bus signal low, indicating that a dc power-fail condition exists.

The low +12 V operation is similar to that described for low +5 V operation. An output voltage less than 11.3 V results in BDCOK H being asserted low (power-fail condition).

AC voltage monitor circuits include an ac low comparator, 16.5 ms delay, and a BPOK H bus driver circuit which is enabled only when BDCOK H is in the active (dc voltage normal) state. Rectifiers D2 and D3 produce positive-going dc voltage pulses at twice the ac line frequency. R32, R12, and C1 produce nominal +3.9 V (peak) normal line voltage pulses which are coupled to the noninverting input of the ac low comparator via R48. R8 and R9 produce a +2.5 V reference for the comparator's inverting input. The comparator's normal output is a series of pulses occurring at twice the ac power line frequency. Each positive-going leading edge retriggers the 16.5 ms one-shot, keeping it in the set state. The 16.5 ms one-shot output is diode-ORed with DCOK L via diodes D25 and D23 and PWR OFF/FAIL H via D24. Normally, the three signals are low and Q11 remains cut off. In this condition, C4 charges to +3.125 V via R36 and R38. This signal is then applied to the power OK comparator's inverting input via R24. Since the noninverting input is referenced to +2.5 V by voltage divider R5 and R6, the comparator's output goes low, biasing off FET Q5. Q5's source voltage then rises toward +5 V via R46 producing the active BPOK H signal. Power-up/power-down sequence timing is shown in Figure 4-34.

A power failure is first detected when the pulsating dc voltage at the ac low comparator's noninverting input is less than +2.5 V (peak). The comparator's output then remains low, allowing the 16.5 ms one-shot to go out of the retrigger mode. The one-shot resets 16.5 ms after the leading edge of the last valid ac voltage alternation; the 16.5 ms delay is equivalent to a full line cycle (two-alternation) failure. The high one-shot

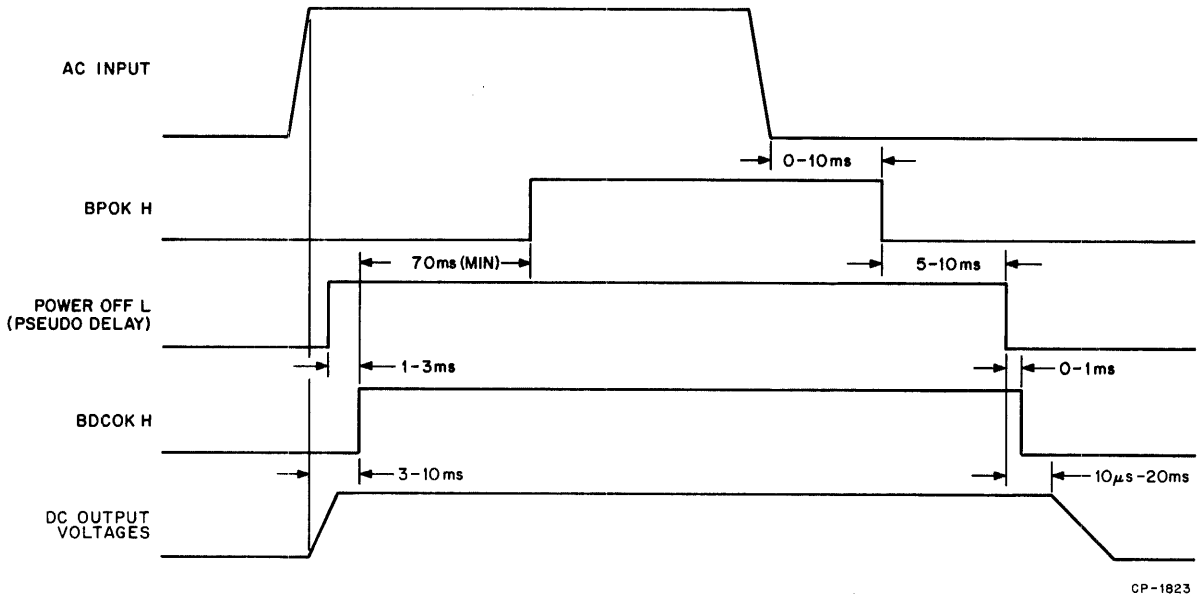


Figure 4-34 Power-Up/Power-Down Sequence

output is then coupled via D23 to the base of Q11, forward biasing it. Q11 conducts and rapidly discharges C4; R36 limits peak discharge current. The low voltage thus produced is less than the +2.5 V reference at the power OK comparator's input, and its output goes high. Q5 then conducts and asserts the BPOK H signal low (power fail). The AC LO L signal produced by the 16.5 ms one-shot is ORed with the DC ON H signal, producing a high POWER OFF/FAIL H signal. This signal reverse biases D26, allowing C13 to charge to 5 V via R40. After a 5—10 ms (approximately) "pseudo delay," C13's voltage rises above the dc off voltage comparator's +2.5 V reference (noninverting) input. The comparator's output goes low, asserting POWER OFF L low and turning off the switching regulators (Paragraph 4.9.3.4).

When normal power is restored, the 16.5 ms one-shot returns to the retrigger (set) mode. AC LO L goes high (false) and PWR OFF/FAIL H goes low, discharging C13. The dc off voltage comparator's inverting input immediately goes low and its output goes high, enabling switching regulator operation. The low AC LO H one-shot output removes forward bias from the base of Q11, cutting it off. Its collector voltage then rises as C4 charges at a relatively slow rate. R38 controls the charging rate of C4 and ensures that ac voltage and dc output voltages are normal for approximately 100 ms (70 ms minimum) before BPOK H goes high.

The DC ON/OFF switch simulates a power failure when it is placed in the OFF position. Cross-coupled inverters provide switch debounce protection and a low (false) DC ON H signal is produced. This signal is ORed with AC LO L, causing a power-fail sequence to occur as previously described. BPOK H is immediately asserted low. After the 5—10 ms pseudo delay, dc switching regulator operation is inhibited and dc power is removed from the backplane. When the DC ON/OFF switch is returned to the ON position, PWR OFF/FAIL H goes low, rapidly discharging C13. POWER OFF L then goes high and switching regulator operation resumes. Approximately 100 ms later, BPOK H goes high and normal processor operation is enabled. DC ON/OFF circuit timing is shown in Figure 4-35.

BEVNT L is the bused interrupt requet line which is normally used for line time clock interrupts. Q4 is forward-biased during positive alternations of the ac line and produces low-active BEVNT L signals. D1 clips negative alternations and limits Q4's reverse base to emitter voltage.

The RUN indicator is illuminated whenever the processor is executing programs. SRUN L, a non-bused backplane signal, is a series of pulses which occur at 3—5μs intervals whenever the processor is in the Run mode. The pulses trigger a 200 ms one-shot on each SRUN L pulse leading edge, keeping it in the retrigger

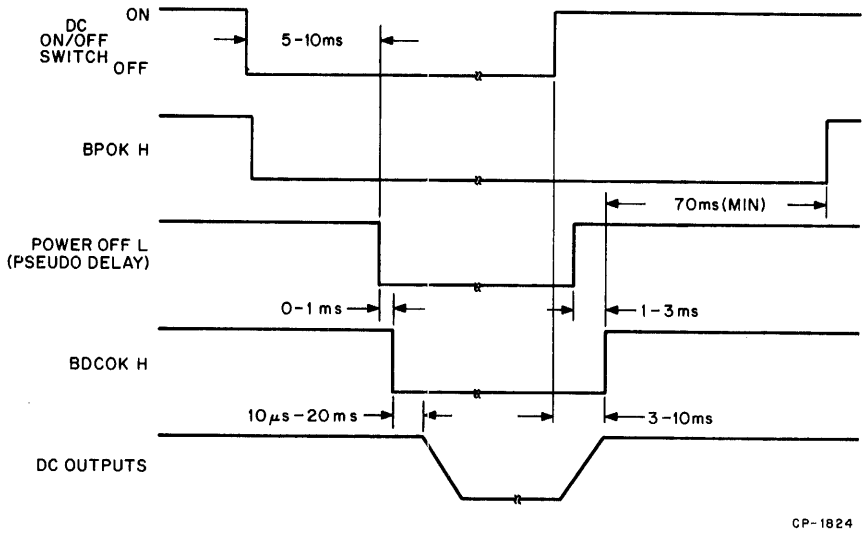


Figure 4-35 DC ON/OFF Circuit Timing

mode. Its high RUN H output signal is then inverted, producing a 0 V signal that turns on the RUN indicator. When the processor is in the Halt mode, SRUN L pulses cease and the 200 ms one-shot resets after the 200 ms delay. The RUN indicator turns off, indicating the Halt mode.

The HALT/ENABLE switch allows the operator to manually assert the BHALT L signal low, causing the processor to execute console ODT microcode. When in the ENABLE position, BHALT L is not asserted, and the Run mode is enabled. Cross-coupled inverters provide a switch debounce function.

4.9.4 H780 Connections

H780 connections are shown in Figure 4-36. The H9270 backplane connections and interconnecting cables are also shown. Note that cable connectors are wired 1:1. Both connectors on the H780/H9270 signal cable are 10-pin connectors which are wired in exactly the same manner, as listed in Figure 4-36. Similarly, both ends of the panel signal/power cable are wired to 16-pin connectors in the same pin/signal configuration.

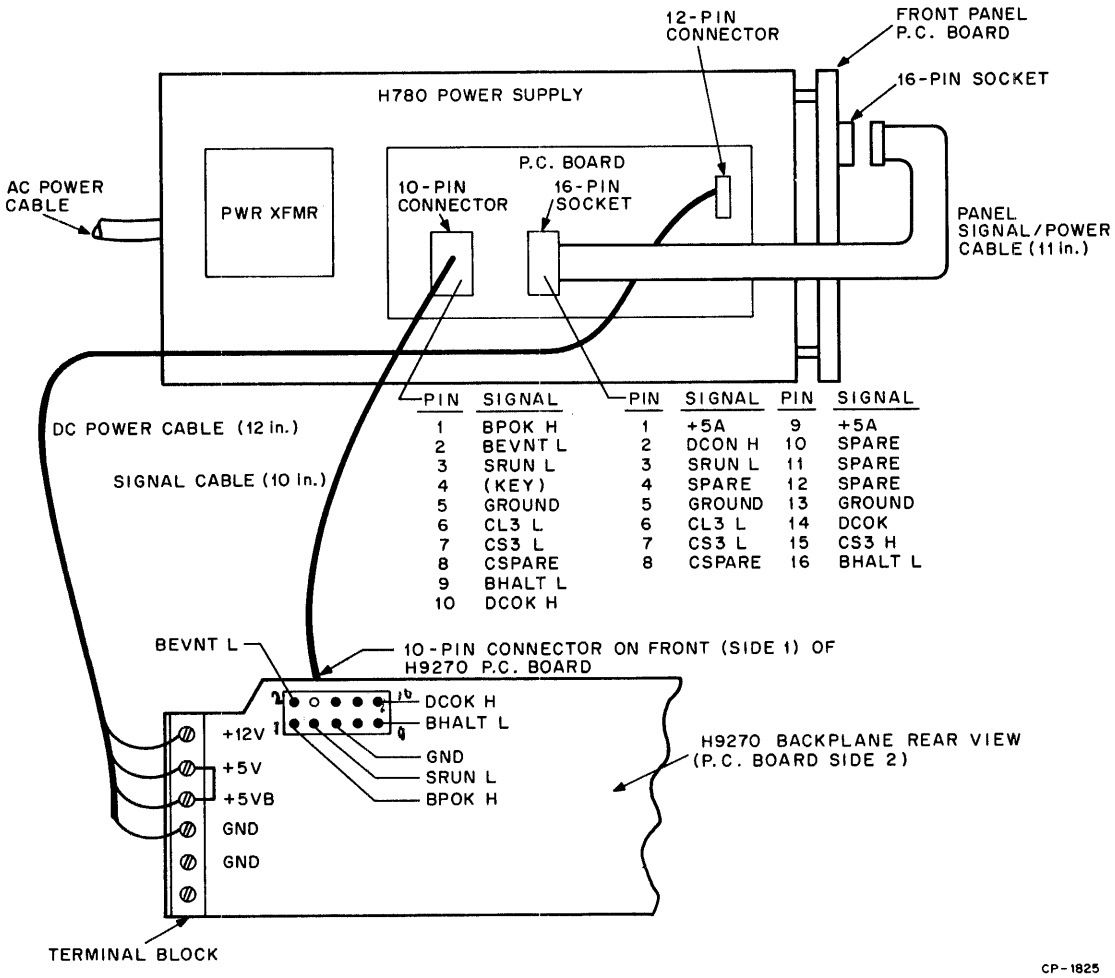


Figure 4-36 H780 Connections

CHAPTER 5
USING KD11-F and KD11-J PROCESSORS

5.1 GENERAL

Before installing and using the KD11-F or KD11-J processor in the LSI-11 or PDP-11/03 system, the user must select certain processor features (jumper-selected), determine where the processor and option modules should be installed on the backplane, be aware of trap and interrupt functions, and ensure the conditions for bus initialization. These items are discussed in detail in the following paragraphs.

5.2 JUMPER-SELECTED FEATURES

5.2.1 General

Wire-wrap posts are provided on the LSI-11 microcomputer module to allow the user to select various features, as listed in Table 5-1. These features include: memory refresh enable/disable, line time clock (LTC, or external event interrupt) enable/disable, power-up mode selection, and resident memory bank selection (KD11-F only). Jumpers are located as shown in Figure 5-1. Jumpers are factory-installed as listed in Table 5-2 and can be altered by the user for a particular application, as described in the following paragraphs.

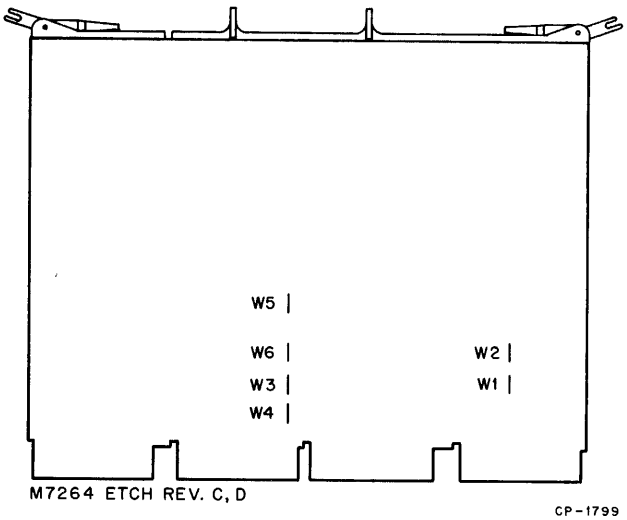
Table 5-1
Summary of KD11 Jumpers

W1	W2	W3	W4	W5	W6	Function
X	X	X	R	X	X	Memory Refresh
X	X	R	X	X	X	Line Time Clock Enable
X	X	X	X	R	R	Power-Up to 24
X	X	X	X	I	R	Power-Up to ODT
X	X	X	X	R	I	Power-Up to 173000
X	X	X	X	I	I	Power-Up to special microcode
R	I	X	X	X	X	Resident Memory Bank 0
I	R	X	X	X	X	Resident Memory Bank 1

NOTE
X = Don't Care
I = Installed
R = Removed

Table 5-2
KD11 Factory Jumper Configuration

Jumper	Installed	Removed	Function
W1		X	BANK 1 Disabled
W2	X (KD11-F)	X (KD11-J)	BANK 1 Enabled (KD11-F only)
W3		X	Line Time Clock Enable
W4	X (KD11-J)	X (KD11-F)	Memory Refresh Enable (KD11-F only)
W5		X	Power-Up
W6		X	Mode 0



NOTE
W1 through W6 are wire-wrap jumpers

Figure 5-1 Jumper Locations

5.2.2 Memory Refresh

The LSI-11 processor has the capability of completely controlling the refreshing of all dynamic MOS memories in a system when jumper W4 is removed. Memory refresh is always required when dynamic MOS memory devices are used in the LSI-11 system,

such as the KD11-F resident memory and the MSV11-B 4K by 16-bit read/write memory module. The refresh operation can be controlled by a device other than the LSI-11 processor, if available, such as a DMA refresh device. If such a device is used, or if no dynamic MOS memory devices are present in the system (KD11-J), install W4. The refresh sequence is described below.

The processor's memory refresh sequence is controlled by resident microcode in the processor which is initiated by an interrupt that occurs once ever 1.6 ms. It is the highest priority processor interrupt. Once the sequence is initiated, the processor will execute 64 BSYNC L/BDIN L bus transactions while asserting BREF L. The BREF L signal overrides memory bank address bits 13—15 and allows all memory units to be simultaneously enabled. After each bus transaction, BDAL1—6 L is incremented by 1 until all 64 rows have been refreshed by the BSYNC L/BDIN L transaction. This process takes approximately 130 μs during which external interrupts (BIRQ L and BEVNT L) are ignored. However, DMA requests can be granted between each of the 64 refresh transactions.

5.2.3 Line Time Clock

LTC (or external event) interrupts are enabled when jumper W3 is removed and the processor is running. The jumper can be inserted to disable this feature. The LTC interrupt is initiated by an external device when it asserts the BEVNT L signal. This is the highest priority external interrupt request; processor interrupts have higher priorities. If external interrupts are enabled (PS bit 7 = 0), the processor PC (R7) and PS word are pushed onto the processor's stack. The LTC (or external event device) service routine is entered by vector address 100 ; the usual interrupt vector address input operation by the processor is not required since vector 100 is generated by the processor.

The first instruction of the service routine will typically be fetched within 16 μs from the time BEVNT L is asserted; however, if optional EIS/FIS instructions are being executed, this time could extend to 50.45 μs. This time could also be extended by processor trap execution (memory refresh, T-bit, power fail, etc.), or by asserting the BHALT L signal.

5.2.4 Power-Up Mode Selection

Since the LSI-11 can be used in a variety of system applications that have either (or both) volatile (semiconductor read/write) or nonvolatile (PROM or core) memory, one of four power-up mode features are available for user selection. These are selected (or changed) by wire-wrap jumpers W5 and W6 on the KD11-F or KD11-J processor (M7264) module. Note that the jumpers affect only the power-up mode (after BDCOK H and BPOK have been asserted); they do not affect the power-down sequence.

The state of the BHALT L signal is significant during the power-up sequence. When this signal is asserted, it causes the processor's ODT console microcode (a subset of an Octal Debugging Technique program) to become invoked after the power-up sequence. The console device must be properly installed for correct use of the BHALT L signal.

The power-up modes are listed in Table 5-3. Detailed descriptions of each mode are provided in the paragraphs which follow.

Table 5-3
Power-Up Modes

Mode	Jumpers		Mode Selected
	W6	W5	
0	R	R	PC at 24 and PS at 26, or Halt mode
1	R	I	ODT Microcode
2	I	R	PC at 173000 for user bootstrap
3	I	I	Special processor microcode (not implemented)

NOTE
R = Jumper Removed
I = Jumper Installed

Power-Up Mode 0

This option places the processor in a microcode sequence that fetches the contents of memory locations 24 and 26 and loads their contents into R7 and the PS, respectively. A microcode service translation at this point interrogates the state of the BHALT L signal; depending on the state of this signal, the processor either enters ODT microcode (BHALT L asserted low) or begins program execution with the current contents of R7 as the starting address (BHALT L not asserted).

Note that the T-bit (PS bit 4) is loaded with the contents of PS bit 4 in location 26. This mode should be used only with nonvolatile memory locations 24 and 26 or with BHALT L asserted. This power-up sequence is shown in Figure 5-2.

Power-Up Mode 1

This mode immediately places the processor in the console microcode regardless of the state of the BHALT L signal. This mode assumes a console interface device at bus address 177560.

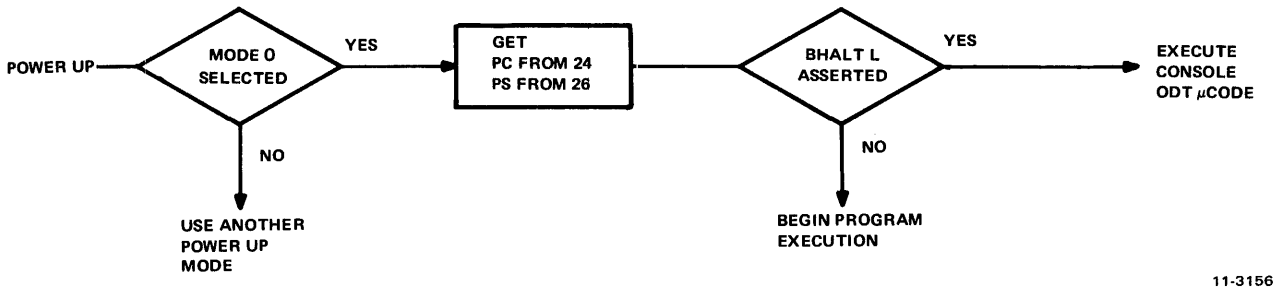


Figure 5-2 Mode 0 Power-Up Sequence

Power-Up Mode 2

This mode places the processor in a microcode sequence that loads a starting address of 173000 into R7 and begins program execution at this location if the BHALT L signal is not asserted.

Note that before 173000 is loaded into R7, PS bit 4 (T-bit) is cleared and bit 7 (interrupt disable) is set. The user's program must set these bits, as desired, and set up a valid stack pointer (R6). This option should be used with nonvolatile memory (ROM, PROM, or core) at address 173000. A time-out trap through location 4 will occur if no device exists at location 173000.

If BHALT L is asserted, the processor will not execute the instruction at location 173000 and will immediately execute the console microcode. This power-up mode sequence is shown in Figure 5-3.

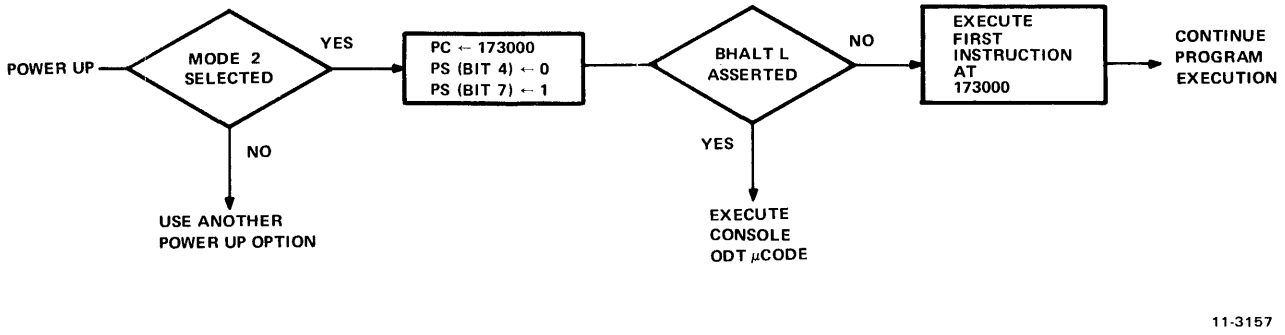


Figure 5-3 Mode 2 Power-Up Sequence

Power-Up Mode 3

This microcode sequence allows access to future microcode expansion in the fourth microm page (microlocations 3000 to 3777). After BDCOK H and BPWROK H are asserted and the internal flags are cleared, a micro jump is made to microlocation 3002. If this option is selected and no microm responds to the fourth page microaddress, a microtrap will occur through microlocation 0 which will, in turn, cause a reserved user instruction trap through location 10.

Note that the state of BHALT L is not checked before control is transferred to the fourth microm page.

5.2.5 Resident Memory 4K Address Selection

Jumpers W1 and W2 are used for selecting the 4K (bank) address for the KD11-F resident memory. Only one jumper must be installed, as follows.

W1 installed = Bank 1 (addresses 20000—37776)
W2 installed = Bank 0 (address 0—17776)

NOTE

If no jumper is installed, the 4K resident memory will not respond to any address.

5.3 INSTALLATION

Prior to installation, the processor module jumpers must be configured as directed in Paragraph 5.2. PDP-11/03 systems are shipped from the factory with the KD11-F or KD11-J processor installed. Refer to Chapter 11 for LSI-11 processor module installation details.

5.4 USING THE LSI-11 MICROCOMPUTER

5.4.1 General

Most of the operational characteristics are discussed in the *LSI-11, PDP-11/03 Processor Handbook* and related software publications. This discussion includes the use of the LTC (external event interrupt) feature, bus initialization, and trap and interrupt priority.

5.4.2 Interrupt and Trap Priority

Interrupts and traps are quite similar in their operation. Interrupts are service requests from devices external to the processor; traps are interrupts which are generated within the processor. Their main operational difference, however, is that external interrupts can only be recognized when PS priority (bit 7) is zero; traps can be executed at any time, regardless of the PS priority bit status.

The highest priority trap is memory refresh, when enabled (Paragraph 5.2.2). Memory refresh does not require an interrupt vector since it is entirely controlled by processor microcode; memory refresh operations are completely transparent to the user programs and PS bits are not altered in any way. The remaining traps, including EMT, BPT, IOT, and TRAP instructions, and hardware-generated Trace Trap, Bus Error, Power Fail, etc. are described in the *LSI-11, PDP-11/03 Processor Handbook.* The LTC (external event) interrupt has the highest priority of all external interrupts, when enabled (Paragraph 5.2.3). It is acknowledged (serviced) only when PS priority bit 7 = 0. This interrupt always uses vector address 100 . It loads a new PC from location 100 and a new PS from location 102. All other external interrupts are requested by a device asserting the BIRQ L signal. If PS bit 7 = 0, the request is acknowledged and the processor inputs a user-assigned vector address for the device's service routine PC (starting address) and PS. For example, when the requesting device is the console device, vectors 60 (console input) or 64 (console output) are used. These vectors are reserved for the console device by most DIGITAL software systems.

5.4.3 Halt Mode

The LSI-11 microcomputer can operate in either a Run or Halt mode. When in the Halt mode, normal program execution is not performed and the processor executes ODT console microcode. However, the processor will execute memory refresh in a normal manner and arbitrate DMA requests; all external interrupts are ignored.

The Halt mode can be entered in one of four ways:

1. When the BHALT L signal is asserted.
2. When a HALT instruction has been executed.
3. By power-up sequence.
4. When a double bus error has occurred [a bus error trap with SP (R6) pointing to nonexistent memory].

The LSI-11 microcomputer does not use conventional control panel lights and switches. Instead, the ODT console microcode routine provides all control panel features on a peripheral device which can be interfaced at bus address 177560 and interpret ASCII characters. In a typical configuration there is no bus device that responds to address 177570 (the PDP-11 SWR address). The peripheral device used with the ODT console microcode is called the console device, which can be any device capable of interpreting ASCII characters. The prompt character sequence and detailed use of console ODT commands are contained in the *LSI-11, PDP-11/03 Processor Handbook.*

5.5 INITIALIZATION AND POWER FAIL

Initialization occurs during a power-up or power-fail sequence, or when a RESET instruction is executed. The processor responds to these conditions by asserting the BINIT L bus signal. BINIT L can be used to clear or initialize all device registers on the bus. In addition, the DRV11 parallel line unit applies the buffered initialize signal to pins on both of its device interface connectors for initializing the user's device.

During the power-up sequence, the processor asserts BINIT L in response to a passive (low) power supply-generated BDCOK H signal. When BDCOK H goes active (high), the processor terminates BINIT L and the jumper-selected power-up sequence is executed. Similarly, if power fails, the power supply-generated BPOK H signal goes passive (low) and causes the processor to push the PC and PS onto the stack and enter a power-fail routine via vector location 24. The processor will execute a user power-fail routine until either BDCOK H goes passive (low), indicating that dc operating power may not sustain processor operation, or BPOK H returns to the active state. BINIT L will go active if BDCOK H goes passive.

Note that if a HALT instruction is executed after entering the power-fail routine, the ODT microcode will not be executed until BPOK H is reasserted. If BPOK H goes passive while the processor is in the Halt mode, the power-fail routine will not be executed.

CHAPTER 6
LSI-11 INTERFACE MODULES

6.1 GENERAL

Two LSI-11 interface modules provide a simple means for interfacing peripheral devices to the LSI-11 bus. The DLV11 is an asynchronous serial line interface that is capable of transmitting and receiving 20 mA current loop or EIA serial data, ranging in rate from 50 to 9600 baud. Two optional cable types are available for connecting 20 mA or EIA devices to the DLV11. The DRV11 is a general-purpose parallel line interface. It is capable of storing and transmitting either two 8-bit bytes or one 16-bit word, and receiving 8-bit bytes or 16-bit words.

The remainder of this chapter described DLV11 and DRV11 functions, jumpers, installation, interfacing to peripherals, and programming.

6.2 DLV11 SERIAL LINE UNIT

6.2.1 General

The DLV11 Serial Line Unit interfaces serial I/O devices to the LSI-11 bus, as shown in Figure 6-1.

6.2.2 Jumper-Selected Addressing, Vectors, and Module Operations

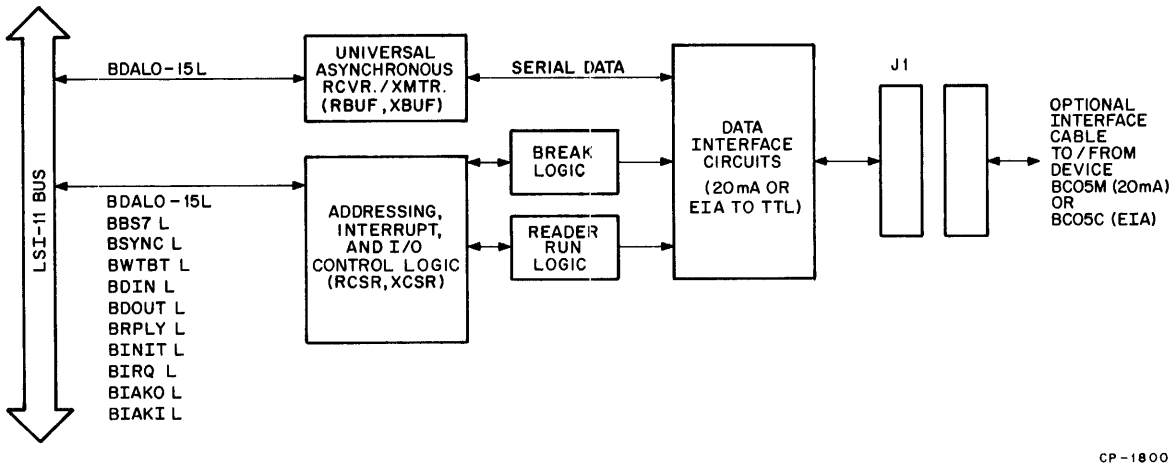


Figure 6-1 DLV11 Serial Line Unit

6.2.2.1 Locations — Thirty jumper locations are provided on the DLV11 module, as shown in Figure 6-2. Jumpers are installed at the factory for use as the console device (Paragraph 6.2.7) and can be altered by the user for his particular system application, as described in the following paragraphs.

6.2.2.2 Addressing — Jumpers involved with addressing include A3 through A12. Only address bits 03 through 12 are programmed by the jumpers for correct DLV11 addressing, producing the 16-bit address word shown in Figure 6-3. The appropriate jumpers are removed to produce logical 1 bits; jumpers installed will produce logical 0 bits.

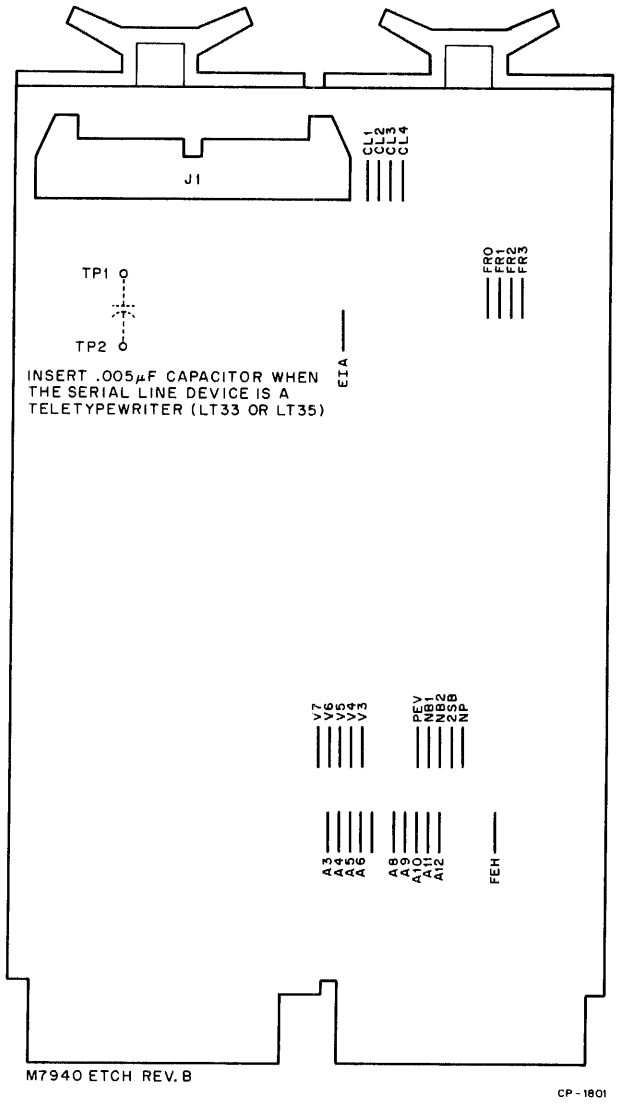


Figure 6-2 DLV11 Jumper Locations

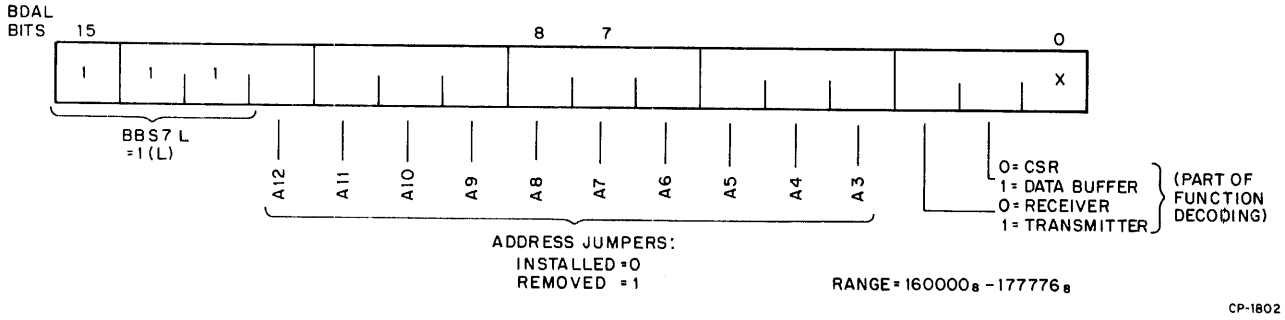


Figure 6-3 DLV11 Addresses

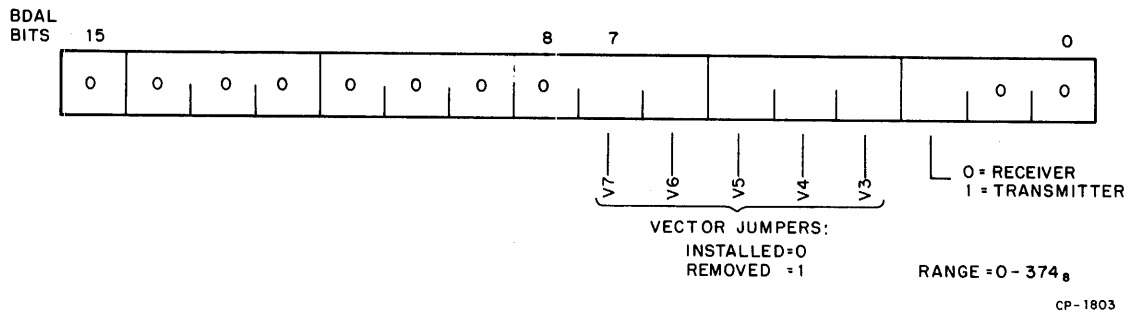


Figure 6-4 DLV11 Interrupt Vectors

6.2.2.3 Vectors — Jumpers involved with vector addressing include V3 through V7. Only vector bits 03 through 07 are programmed by the jumpers for correct DLV11 vector addressing, producing the 16-bit address shown in Figure 6-4. The appropriate jumpers are removed to produce logical 1 bits; jumpers installed will produce logical 0 bits.

6.2.2.4 UAR/T Operation — UAR/T operation is programmed via jumpers NP, 2SB, NB1, NB2, and PEV as shown below.

Number of Data Bits

	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

2SB installed = One stop bit
2SB removed = Two stop bits

Parity Transmitted

NP removed = No parity bit
NP and PEV installed = Odd parity
NP installed and PEV removed = Even parity

6.2.2.5 Baud Rate Selection — Baud rate is programmed via jumpers FR0 through FR3 as shown in Table 6-1.

6.2.2.6 EIA Interface — EIA drivers are enabled when jumper EIA is installed. This jumper applies -12 V to the EIA driver chip. It should be removed during 20 mA current loop operation.

6.2.2.7 20 mA Current Loop Interface — Jumpers CL1 through CL4 are associated with 20 mA current loop interface operation. Remove EIA and remove or install jumpers as desired for the functions listed below:

Table 6-1
Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
2400	I	R	R	R
2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I
External (via pin BH1)	I	I	I	X

NOTE
I = installed **X = don't care**
R = removed

Active Current Loop (Jumpers configuration as shown in Figure 6-5.)

Transmit = CL3 and CL4 installed
Receive = CL1 and CL2 installed

Passive Current Loop (Jumpers configured as shown in Figure 6-6.)

Transmit = CL3 and CL4 removed
Receive = CL1 and CL2 removed

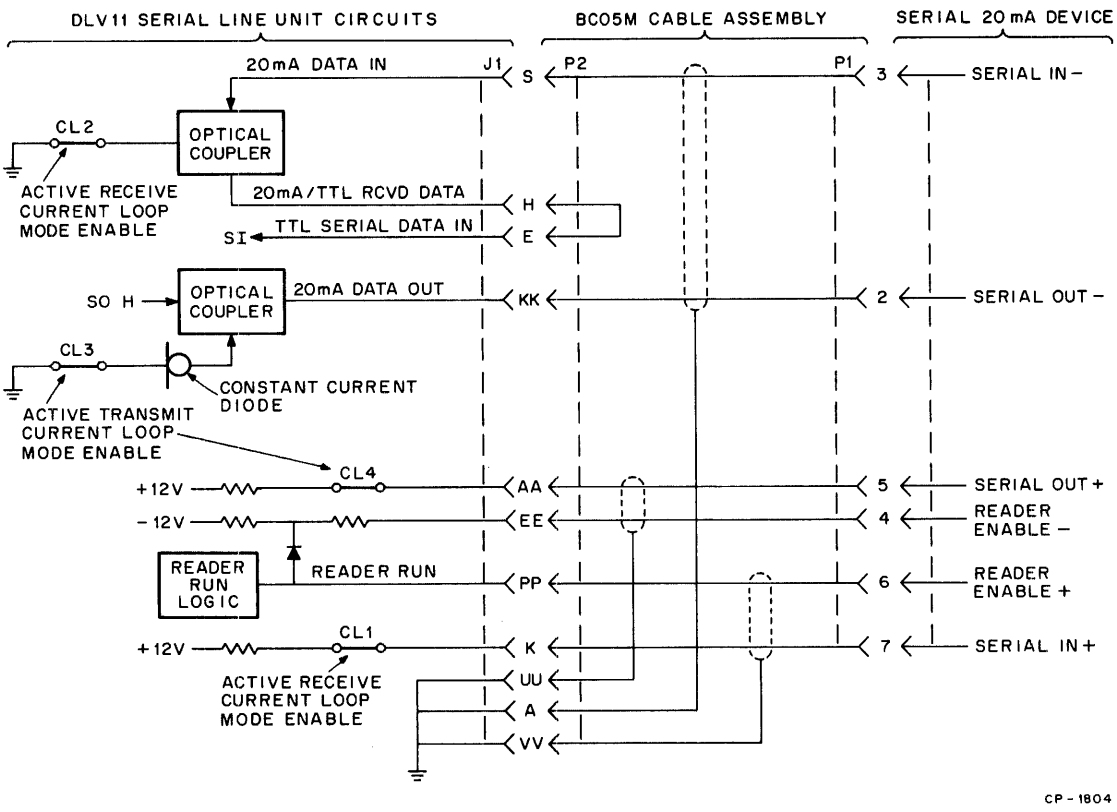


Figure 6-5 Active 20 mA Current Loop Interface

The DLV11 is supplied with jumpers CL1 through CL4 wired for the active transmit, active receive mode (Figure 6-5). When in this mode, serial current limiting to 23 mA is provided by resistors (one each for transmit and receive functions) connected to the +12 V source. Note that when module power is removed, the 20 mA transmit optical coupler closes the serial loop (active or passive mode). When the DLV11 is used in the passive 20 mA mode (Figure 6-6), the serial device must produce the 20 mA current. Current limiting must be provided for transmit and receive currents in the serial device.

6.2.2.8 Framing Error Halt — A framing error halt allows entry to console microcode directly from the console device by pressing the BREAK key, producing a framing error. A framing error occurs when the received character has no valid stop bit. This error condition is detected by the UAR/T. FEH is factory-installed, causing the assertion of BHALT L when the framing error is detected. The processor then executes console microcode.

6.2.3 Installation

Prior to installing the DLV11 on the backplane, first establish the desired priority level (Chapter 3) to determine the backplane slot in which the module will be installed. Then, check that jumpers are removed or installed as described for your application (Paragraph 6.2.2). Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

6.2.4 Interfacing with 20 mA Current Loop Devices

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Mate-N-Lok connector that is pin-compatible with the following peripheral options:

LA36 DECwriter
LT33 Teletypewriter
LT35 Teletypewriter

*The -X in the cable number denotes length in feet, as follows: -1, -6, -10, -20, -25. For example, a 10-ft EIA interface cable would be ordered as BC05C-10.

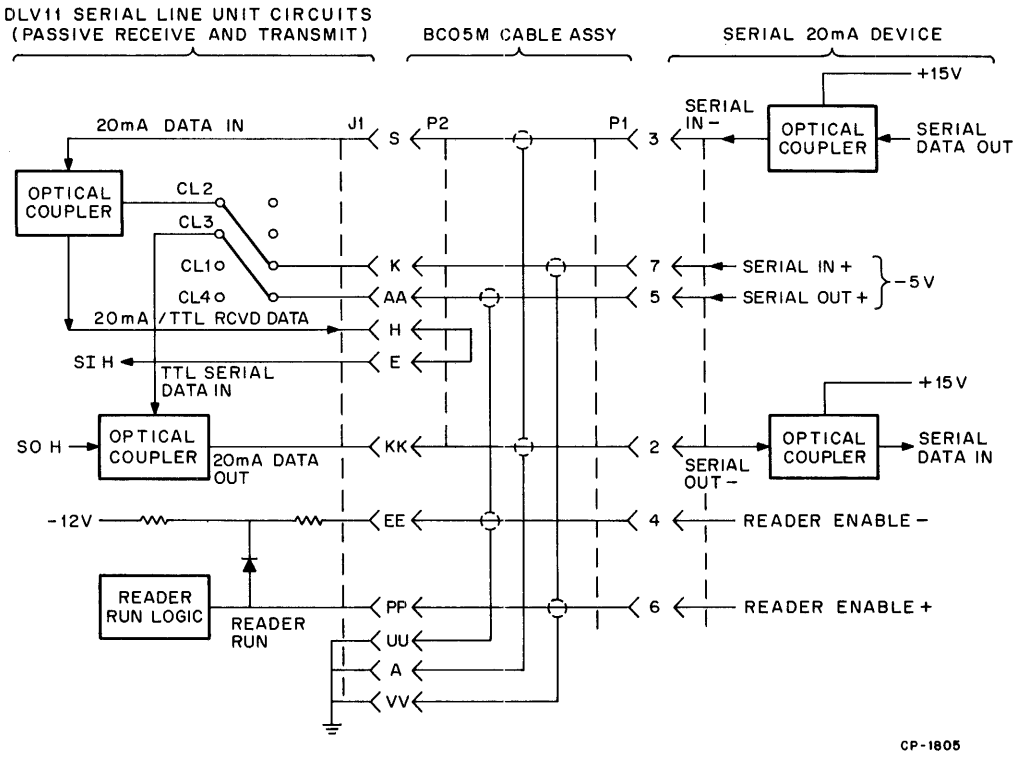


Figure 6-6 Passive 20 mA Loop Jumper Configuration

VT05B Alphanumeric Terminal
VT50 DECscope
RT02 Alphanumeric Terminals
DF01-A Acoustic Telephone Coupler

The complete interface circuit provided by the BC05M cable and the associated DLV11 jumpers is shown in Figure 6-5.

NOTE

When the DLV11 is used with teletypewriter devices, a 0.005 μF capacitor must be installed between split lugs TP1 and TP2.

After configuring the module jumpers and installing the proper interface, the DLV11 can be installed in the backplane.

6.2.5 Interfacing with EIA-Compatible Devices

When interfacing with EIA devices, the BC05C modem cable provides the correct connection to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113 modems. Connector pinning and signal levels conform to EIA Specification RS232C. The complete EIA interface circuit is shown in Figure 6-7.

6.2.6 Programming

6.2.6.1 Addressing — Addresses for the DLV11 can range from 160000 through 17777X_8. The least significant three bits (only bits 01 and 02 are used; bit 0 is ignored) address the desired register in the DLV11, as follows:

Address	Addressed Register
1XXXX0	RCSR (Receiver control/status)
1XXXX2	RBUF (Receiver data buffer)
1XXXX4	XCSR (Transmit control/status)
1XXXX6	XBUF (Transmit data buffer)

Address bits 03 through 12 are jumper-selected as directed in Paragraph 6.2.2.2.

Since each DLV11 module has four registers, each requires four addresses. Addresses 177560—177566 are reserved for the DLV11 used with the console peripheral device. Additional DLV11 modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11 modules to be addressed.

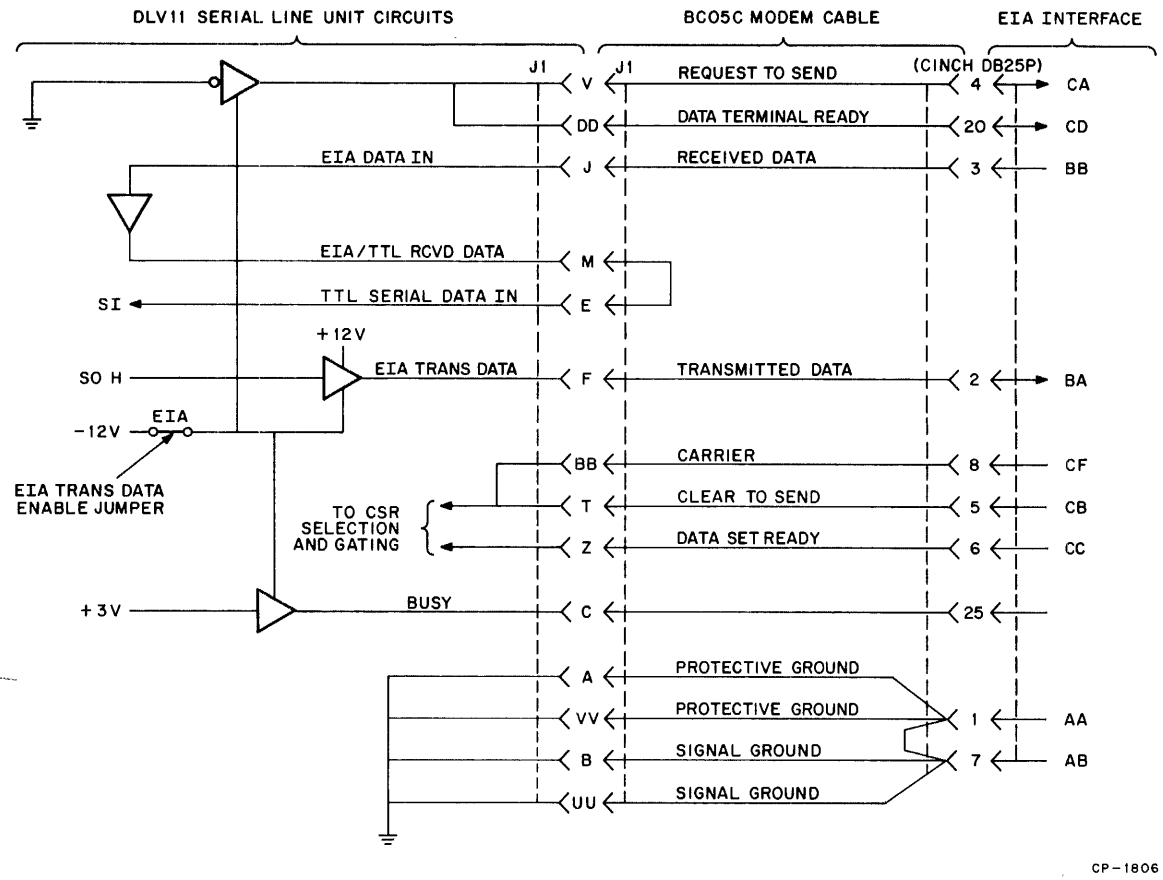


Figure 6-7 EIA Interface

6.2.6.2 Interrupt Vectors — Two interrupt vectors are jumper-selected on each DLV11 as described in Paragraph 6.2.2.3:

000XX0 Receiver interrupt vector
000XX4 Transmitter interrupt vector

Vectors can range from addresses 0 through $37X_8$. Vectors 60 and 64 are reserved for the console peripheral device. Additional DLV11 modules should be assigned vectors following any DRV11 modules installed in the system starting at address 300.

6.2.6.3 Word Formats — The four word formats associated with the DLV11 are shown in Figure 6-8 and are described in Table 6-2.

6.2.7 Console Device

The console device is a serial line device, such as the LA36 DECwriter, that uses a DLV11 Serial Line Unit. The following device addresses must be used for the console device:

Register	Address
RCSR	177560
RBUF	177562
XCSR	177564
XBUF	177566

Vector addresses must be assigned as follows:

Interrupt Vector	Address
Console Receiver	000060
Console Transmitter	000064

6.3 DRV11 PARALLEL LINE UNIT

6.3.1 General

The DRV11 Parallel Line Unit is a general-purpose device interface module that connects parallel I/O devices to the LSI-11 bus, as shown in Figure 6-9.

6.3.2 Jumper-Selected Addressing and Vectors

Table 6-2
Word Formats

Word	Bit(s)	Function
RCSR	15	Dataset Status — Set when CARRIER or CLEAR TO SEND and DATA SET READY signals are asserted by an EIA device. Read-only bit.
	14—08	Not used. Read as 0.
	07	Receiver Done — Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is addressed or when the DBCOK H signal goes false (low). A receiver interrupt request is generated by the DLV11 when this bit is set and receiver interrupt is enabled (bit 6 is also set). Read-only bit.
	06	Interrupt Enable — Set under program control when it is desired to generate a receiver interrupt request when a character is ready for input to the processor (bit 7 is set). Cleared under program control or by the BINIT signal. Read/write bit.
	05—01	Not used. Read as 0.
	00	Reader Enable — Set by program control to advance the paper tape reader on a teletypewriter device to input a new character. Automatically cleared by the new character's start bit. Write-only bit.
RBUF	15—08	Not used. Read as 0.
	07—00	Contains five to eight data bits in a right-justified format. MSB is the optional parity bit. Read-only bit.
XCSR	15—08	Not used. Read as 0.
	07	Transmit Ready — Set when XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by the BDCOK H signal. Automatically cleared when XBUF is loaded. When transmitter interrupt is enabled (bit 6 also set), an interrupt request is asserted by the DLV11 when this bit is set. Read/write bit.
	06	Interrupt Enable — Set under program control when it is desired to generate a transmitter interrupt request when the DLV11 is ready to accept a character for transmission. Reset under program control or by the BINIT signal. Read/write bit.
	05—01	Not used. Read as 0.
	00	Break — Set or reset under program control. When set, a continuous space level is transmitted. BINIT resets this bit. Read/write bit.
XBUF	15—08	Not used.
	07—00	Contains five to eight right-justified data bits. Loaded under program control for serial transmission to a device. Write only.

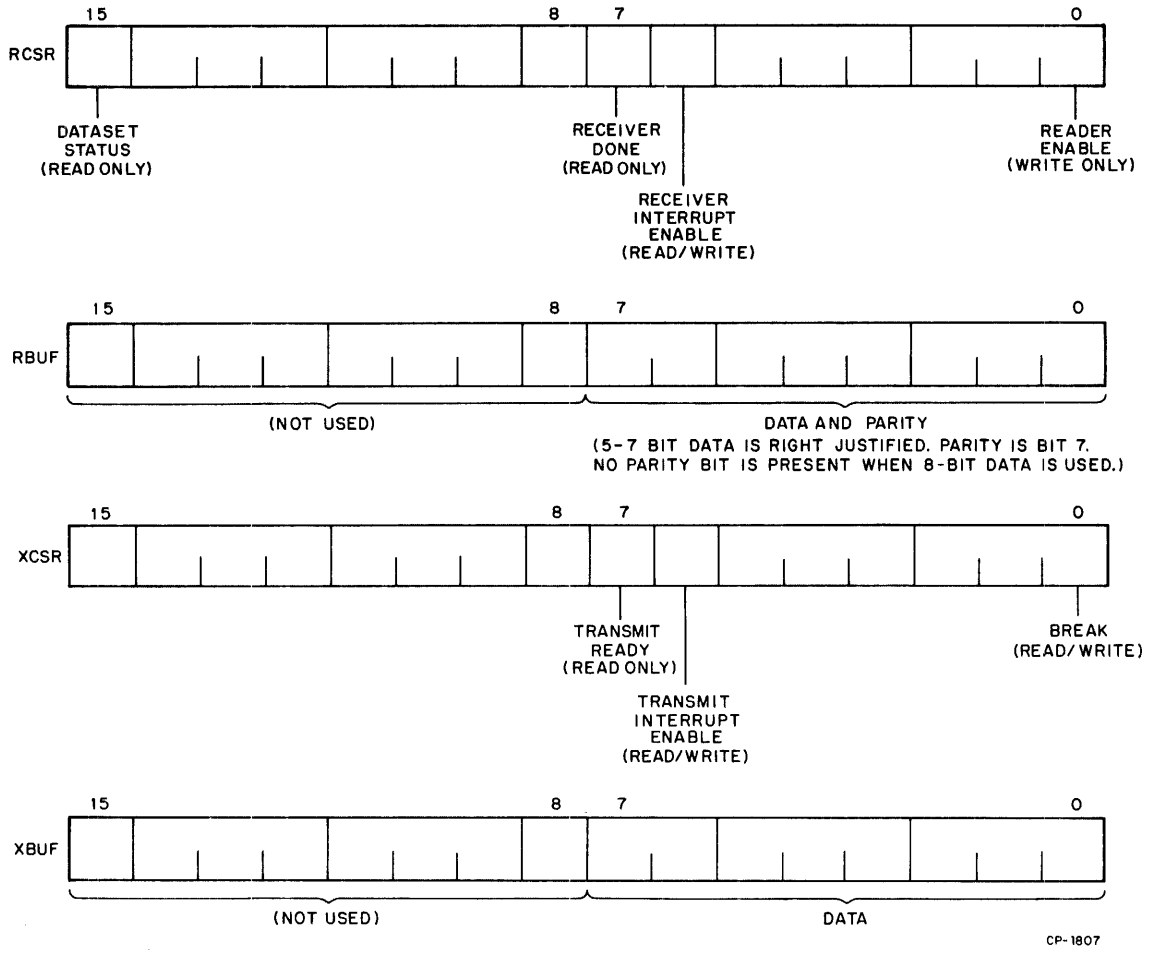


Figure 6-8 DLV11 Word Formats

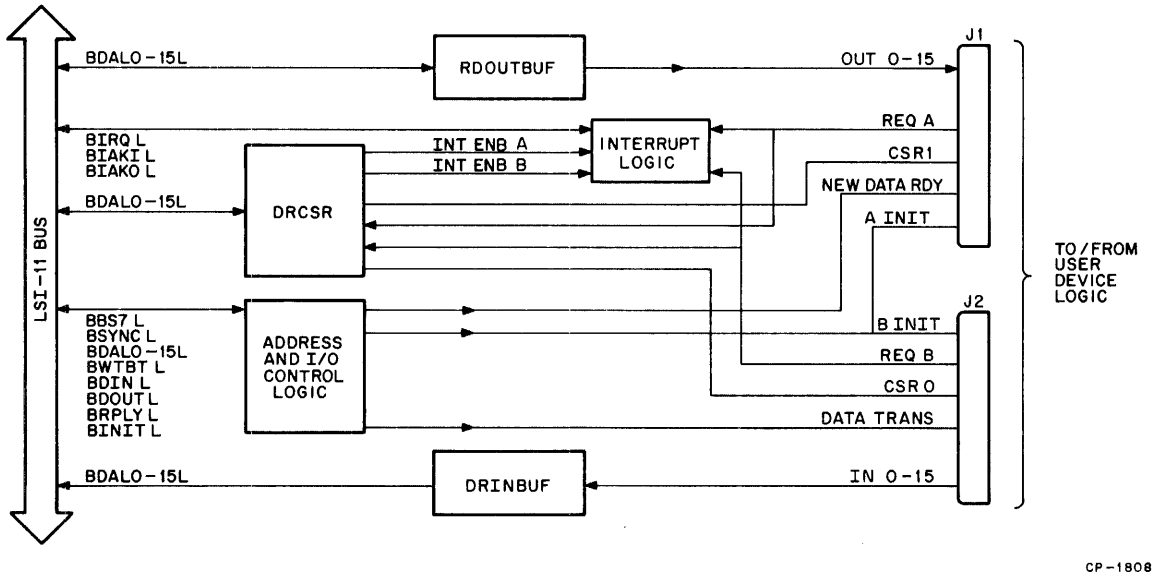


Figure 6-9 DRV11 Parallel Line Unit

6.3.2.1 Locations — Jumpers for device address and vector selection are provided on the DRV11 as shown in Figure 6-10. Jumpers are installed at the factory for address 167770 (DRCSR) and vectors 300 (interrupt A) and 304 (interrupt B). These can be cut or removed by the user to program the module for his system application, as described in the following paragraphs.

6.3.2.2 Addressing — Jumpers involved with addressing include A3 through A12. Only address bits 03 through 12 are programmed by jumpers for DRV11 addressing, producing the 16-bit address word shown in Figure 6-11. The appropriate jumpers are removed to produce logical 1 bits; jumpers installed will produce logical 0 bits.

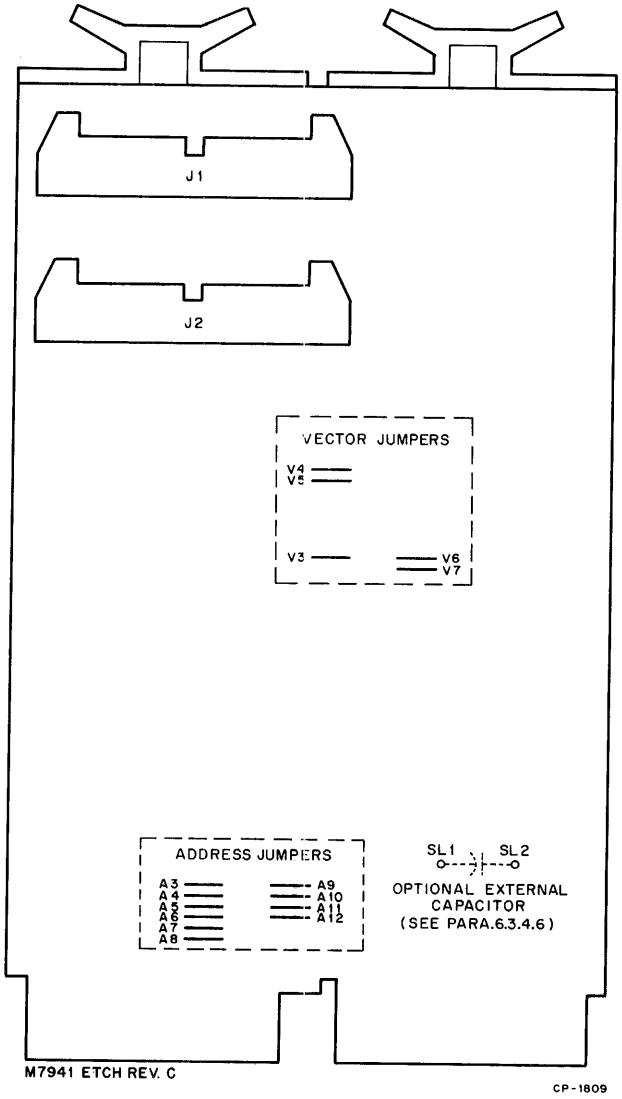


Figure 6-10 DRV11 Jumper Locations

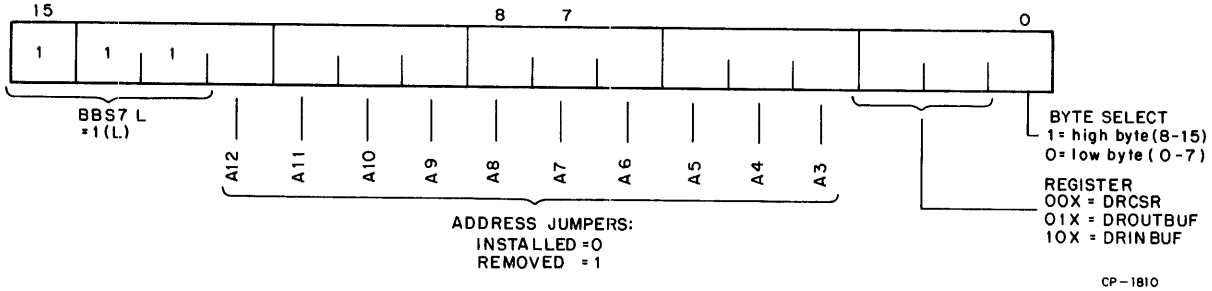


Figure 6-11 DRV11 Device Address

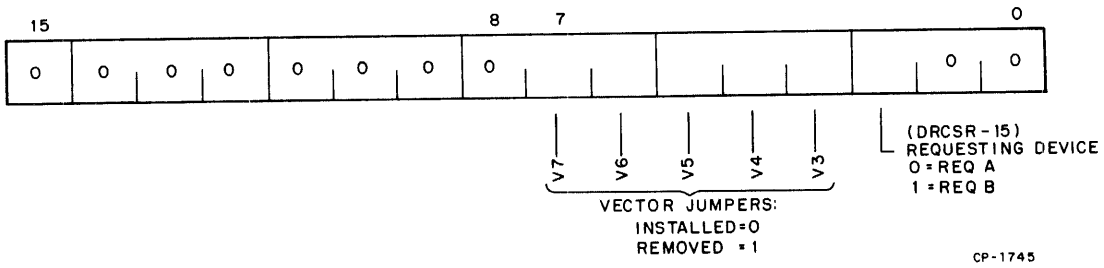


Figure 6-12 DRV11 Vector Address

6.3.2.3 Vectors — Jumpers involved with vector addressing include V3 through V7. Only vector bits 03 through 07 are programmed by the jumpers for DRV11 vector addressing, producing the 16-bit word shown in Figure 6-12. The appropriate jumpers are removed to produce logical 1 bits; jumpers installed will produce logical 0 bits.

6.3.3 Installation

Prior to installing the DRV11 on the backplane, first establish the desired priority level (Chapter 3) for the backplane slot installation. Check that proper device address and vector jumpers are installed, as directed in Paragraph 6.3.2. The DRV11 can then be installed on the backplane. Connection to the user's device is via optional cables.

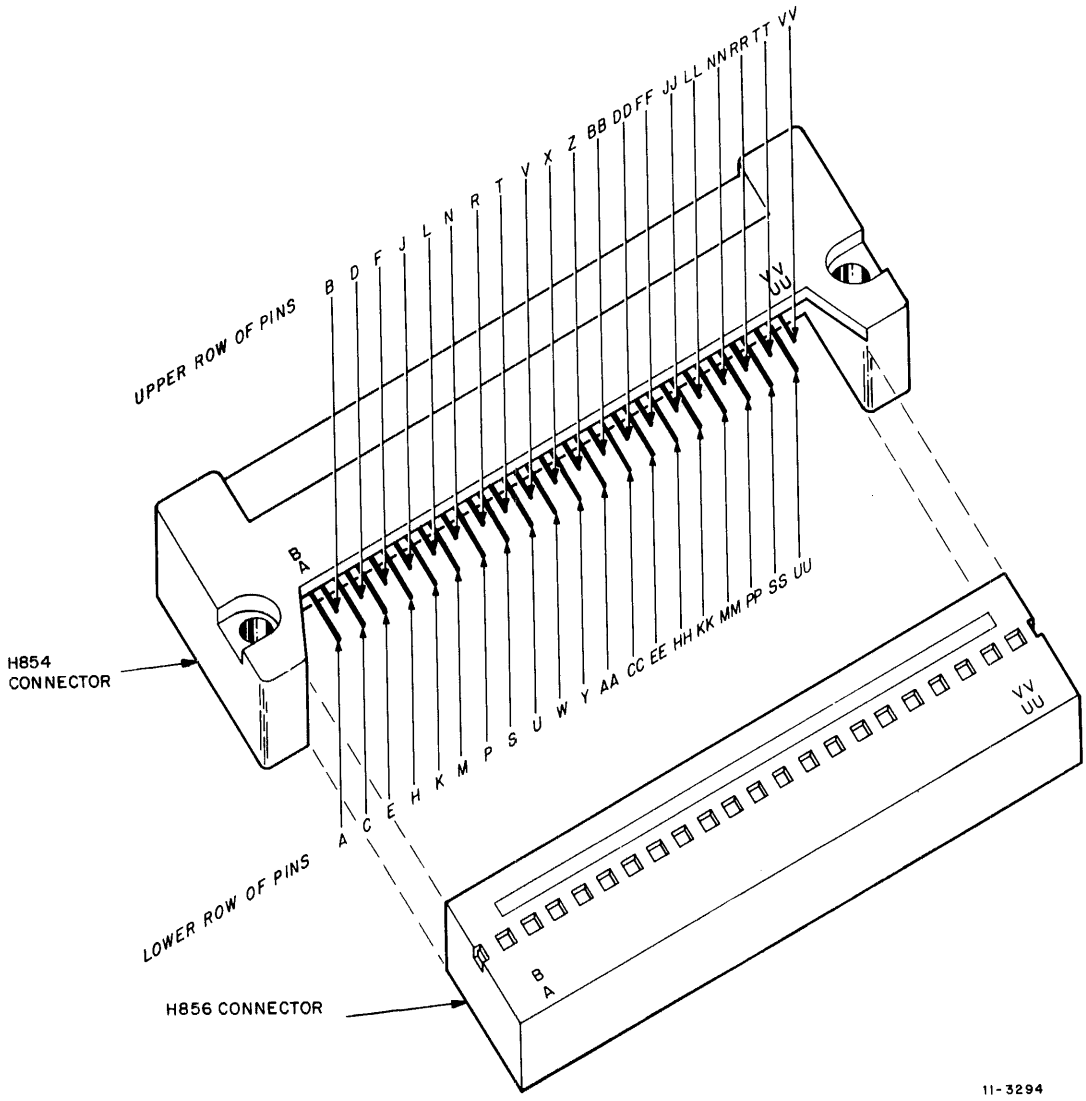


Figure 6-13 J1 or J2 Connector Pin Locations

6.3.4 Interfacing to the User's Device

6.3.4.1 General — Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Pins are located as shown in Figure 6-13. Signal pin assignments for input interface J2 (connector No. 2) and output interface J1 (connector No. 1) are listed in Table 6-3. Optional cables and connectors for use with the DRV11 include:

*BC08R-X** — Maintenance cable, 40-conductor flat with H856 connectors on each end. Available in lengths of 1, 6, 10, 20, and 25 feet.

BC11K-25 — Signal cable, 20 twisted pair with H856 connector on one end; remaining end is terminated by the user.

H856 — Socket, 40-pin female, for user-fabricated cables.

*The -X in the cable number denotes length in feet, as follows: -1, -6, -10, -12, -20, -25. For example, a 10-ft maintenance cable would be ordered as BC08R-10.

When using the BC11K-25 cable, connect the free end of the cable using the wiring data contained in Table 6-4. Refer to the *Hardware/Accessories Catalog* for additional optional interface accessories.

6.3.4.2 Output Data Interface — The output interface is the 16-bit buffer (DROUTBUF). It can be either loaded or read under program control. When loaded by a DATO or DATOB bus cycle, the NEW DATA READY H 300 ns pulse is generated to inform the user's device of the data transfer. The trailing edge of this positive-going pulse should be used to strobe the data into the user's device in order to allow data to settle on the interface cable. The system initialize signal (BINIT L) will clear DROUTBUF.

All output signals are TTL levels capable of driving eight unit loads except for the following:

NEW DATA READY = 30 unit loads
DATA TRANSMITTED = 30 unit loads
INIT (Initialize)* = 10 unit loads per connector

*Common signal on both connectors.

Table 6-3
DRV11 Input and Output Signal Pins

Inputs			Outputs		
Signal	**Connector Pin**		**Signal**	**Connector Pin**	
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H, E	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	CC	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS*	2	C
			CSR0	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

*Pulse signals, approximately 300-ns wide. Width can be changed by user.

Table 6-4
BC11K Signal Cable Connections

Twisted Pair	Color	Pin	Connector No. 1	Connector No. 2
Black/white-orange	black	A	OPEN	OPEN
	wh-org	B	OPEN	OPEN
Black/white-yellow	black	C	OUT00	DATA TRANS.
	wh-yel	D	OPEN	OPEN
Black/white-grey	black	E	OPEN	IN02
	wh-gry	F	OPEN	OPEN
Black/white-red	black	H	OPEN	IN02
	wh-red	J	GND	GND
Black/white-green	black	K	OUT01	CSR0
	wh-grn	L	OUT04	GND
Brown/green	brown	M	GND	IN15
	green	P	INIT	IN13
Brown/red	brown	N	OUT05	IN14
	red	R	OUT06	GND
Black/white-blue	black	S	GND	REQ B
	wh-blu	T	OUT07	GND
Black/orange	black	U	OUT03	IN12
	orange	V	GND	IN11
Black/white-violet	black	W	OUT08	IN10
	wh-vio	X	OUT09	GND
Black/red	black	Y	GND	IN09
	red	Z	OUT10	IN08
Brown/yellow	brown	AA	OUT11	GND
	yellow	BB	OUT12	IN03
Black/blue	black	CC	GND	IN07
	blue	DD	CSR1	GND
Brown/orange	brown	EE	GND	IN06
	orange	FF	OUT13	OPEN
Brown/blue	brown	HH	OUT14	IN05
	blue	JJ	OUT15	GND
Black/yellow	black	KK	GND	IN04
	yellow	LL	REQ A	IN01
Brown/violet	brown	MM	GND	GND
	violet	NN	OUT02	INIT
Black/violet	black	PP	GND	GND
	violet	RR	OUT02	INIT
Black/green	black	SS	GND	GND
	green	TT	OPEN	IN00
Pink/white-red	pink	UU	GND	GND
	wh-red	VV	NEW DATA RDY	OPEN

6.3.4.3 Input Data Interface — The input interface is the 16-bit DRINBUF read-only register, comprising gated bus drivers that transfer data from the user's device onto the LSI-11 bus under program control. DRINBUF is not capable of storing data; hence, the user must keep input data on the IN lines until read by the LSI-11 microprocessor. When read, the DRV11 generates a positive-going 300 ns DATA TRANSMITTED H pulse which informs the user's device that the data has been accepted. The trailing edge of the pulse indicates that the input transfer has been completed.

All input signals are one standard TTL unit load; inputs are protected by diode clamps to ground and +5 V.

6.3.4.4 Request Flags — Two signal lines (REQ A H and REQ B H) can be asserted by the user's device as flags in the DRCSR word. REQ B is available via Connector No. 2, and it can be read in DRCSR bit 15. REQ A is available via Connector No. 1, and it can be read in DRCSR bit 7. Two DRCSR interrupt enable bits, INT ENB A (bit 6) and INT ENB B (bit 5), allow automatic generation of an interrupt request when their respective REQ A or REQ B signals are asserted. Interrupt enable bits can be set or reset under program control.

In a typical application, REQ A and REQ B are generated by Request flip-flops in the user's device. The user's Request flip-flop should be set when servicing is required and cleared by NEW DATA READY or DATA TRANSMITTED when the appropriate data transaction has been completed.

6.3.4.5 Initialization — The BINIT L processor-generated initialize signal is applied to DRV11 circuits for interface logic initialization. It is also available to the user's circuits via connectors J1 and J2 as follows:

Connector/Pin	Signal
J1/P	AINIT H
J2/RR	BINIT H
J2/NN	BINIT H

An active BINIT L signal will clear: DROUTBUF data; CRCSR bits 6, 5, 1, 0; bits 16 and 7 (when the maintenance cable is connected); and Interrupt Request and Interrupt Acknowledge flip-flops.

6.3.4.6 NEW DATA READY and DATA TRANSMITTED Pulse Width Modification — An optional capacitor can be added by the user to the DRV11 module to extend the pulse width of both the NEW DATA READY and DATA TRANSMITTED pulse widths. The module without external capacitance (as shipped) will produce 300 ns pulses. The capacitor can be added in the location shown in Figure 6-10 to produce the approximate pulse widths listed below.

Optional External Capacitance (pF)	Approximate Pulse Width (ns)
None	300
1200	500
1800	600
6000	1200

6.3.4.7 BC08R Maintenance Cable — When using the optional BC08R maintenance cable, the connections listed in Table 6-5 are provided. Cable connectors P1 and P2 are connected to DRV11 connectors J1 and J2, respectively. Note that CSR0 (J2-K), which can be set or reset under program control, is routed to the REQ A input (J1-LL); similarly, CSR1 (J1-DD) is routed to REQ B (J2-S). Hence, a maintenance program can output data to DROUTBUF and read the same data via the cable and DRINBUF. DRCSR bits 0 (CSR0) and 1 (CSR1) can be used to simulate REQ A and REQ B signals, respectively. If the appropriate INT ENB bit (DRCSR bits 5 or 6) is set, the simulated signal will generate an interrupt request.

6.3.5 Programming

6.3.5.1 Addressing — Address for the DRV11 can range from 160000 through $17777X_8$. The least significant three bits address the desired DRV11 register as follows:

Address	Device Register
1XXXX0	DRCSR
1XXXX2	DROUTBUF
1XXXX4	DRINBUF

Addresses 177560—177566 are reserved for the console device and should not be used for DRV11 addressing. The following address assignments are normally used:

First DRV11
DRCSR = 167770
DROUTBUF = 167772
DRINBUF = 167774

Second DRV11
167760 to 167764

Third DRV11
167750 to 167754

Table 6-5
BC08R Maintenance Cable Signal Connections

Connector No. 2		Connector No. 1	
Pin	**Name**	**Name**	**Pin**
VV	OPEN	OPEN	A
UU	GND	OPEN	B
TT	IN00	OUT00	C
SS	GND	OPEN	D
RR	INIT H	OPEN	E
PP	GND	OPEN	F
NN	INIT H	OPEN	H
MM	GND	GND	J
LL	IN01	OUT01	K
KK	IN04	OUT04	L
JJ	GND	GND	M
HH	IN05	OUT05	N
FF	OPEN	INIT H	P
EE	IN06	OUT06	R
DD	GND	GND	S
CC	IN07	OUT07	T
BB	IN03	OUT03	U
AA	GND	GND	V
Z	IN08	OUT08	W
Y	IN09	OUT09	X
X	GND	GND	Y
W	IN10	OUT10	Z
V	IN11	OUT11	AA
U	IN12	OUT12	BB
T	GND	GND	CC
S	REQ B	CSR1	DD
R	GND	GND	EE
P	IN13	OUT13	FF
N	IN14	OUT14	HH
M	IN15	OUT15	JJ
L	GND	GND	KK
K	CSR0	REQ A	LL
J	GND	GND	MM
H	IN02	OUT02	NN
F	OPEN	GND	PP
E	IN02	OUT02	RR
D	OPEN	GND	SS
C	DATA TRANS	OPEN	TT
B	OPEN	GND	UU
A	OPEN	NEW DATA RDY	VV

Table 6-5 (Continued)
BC08R Maintenance Cable Signal Connections

6.3.5.2 Interrupt Vectors — Two interrupt vectors are jumper-selected in the range of 0 through $37X_8$. The least significant three bits identify the interrupting function.

000XX0	Interrupt A
000XX4	Interrupt B

Vectors 60 and 64 are reserved for the console device and should not be used for DRV11 vectors.

6.3.5.3 Word Formats — The three word formats associated with the DRV11 are shown in Figure 6-14 and are described in Table 6-6.

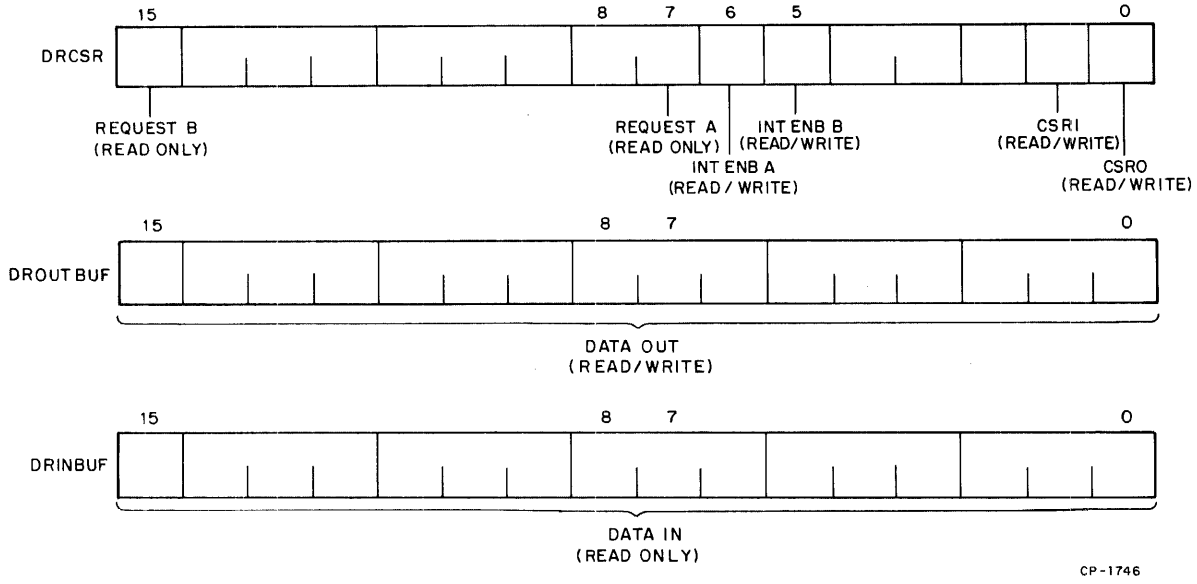


Figure 6-14 DRV11 Word Formats

Table 6-6
Word Formats

Word	Bit(s)	Function
CRCSR	15	REQUEST B — This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is asserted by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT when in maintenance mode.
	14—08	Not used. Read as 0.
	07	REQUEST A — Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Read-only bit. Cleared by INIT when in maintenance mode.
	06	INT ENB A — Interrupt enable bit. When set, allows an interrupt request to be generated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by BINIT.
	05	INT ENB B — Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set.
	04—02	Not used. Read as 0. Can be loaded or read by the program (read/write bit). Cleared by INIT.
	01	CSR1 — This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Can be loaded or read by the program (read/write bit). Cleared by INIT.

Table 6-6 (Continued)
Word Formats

Word	Bit(s)	Function
DRCSR	00	CSR0 — Performs the same functions as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.
DROUTBUF	15—00	Output Data Buffer — Contains a full 16-bit word or one or two 8-bit bytes: High Byte = 15—8; Low Byte = 7—0. Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.
DRINBUF	15—00	Input Data Buffer — Contains a full 16-bit word or one or two 8-bit bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

CHAPTER 7
USING MSV11-A AND MSV11-B READ/WRITE MEMORY MODULES

7.1 GENERAL

MSV11-A (1K) and MSV11-B (4K) read/write memory modules provide temporary storage of user programs and data in an inexpensive, compact, low-power memory subsystem. Full address decoding is provided on both module types. The user can select the 4K address space (bank) in which the module is addressed by installing or removing jumpers. Two additional jumpers are provided on the MSV11-A module for selection of a 1K segment within the selected 4K bank.

Both module types are LSI-11 bus-compatible and can be accessed by the LSI-11 microcomputer or any DMA device that becomes bus master. The MSV11-A and MSV11-B interface with the LSI-11 bus as shown in Figures 7-1 and 7-2, respectively.

7.2 MSV11-A JUMPERS

MSV11-A jumpers are located as shown in Figure 7-3. Jumpers not installed represent logical 0s; jumpers installed represent logical 1s. Address jumpers are assigned as shown in Figure 7-5.

7.3 MSV11-B JUMPERS

7.3.1 Addressing

MSV11-B address jumpers are located as shown in Figure 7-4. The module is supplied with all address jumpers installed. Figure 7-6 illustrates a 16-bit address and how jumpers are assigned for the MSV11-B module.

7.3.2 Reply to Refresh

Only one dynamic memory module in a system is required to reply to the refresh bus transactions initiated by the processor. The module selected to reply should be the module with the slowest access time. Jumper W4 enables or inhibits the MSV11-B reply as follows:

W4 installed: MSV11-B will not assert BRPLY in response to refresh bus signals.

W4 removed: MSV11-B will reply to refresh bus BSYNC/BDIN transactions by asserting BRPLY L.

7.4 MSV11-B BUS RESTRICTION

The MSV11-B module requires a refresh sequence once every 1.6 ms. This is performed automatically by the KD11-F or KD11-J LSI-11 microcomputer.

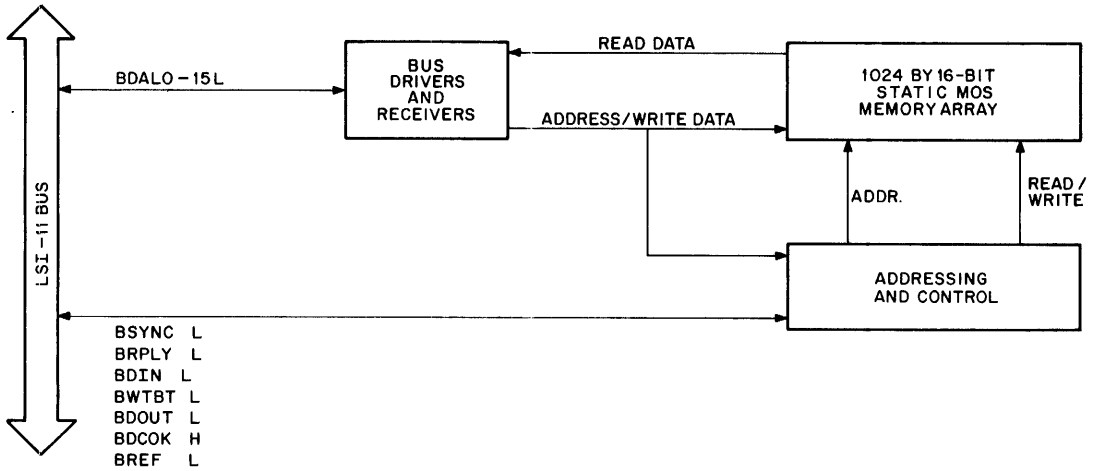


Figure 7-1 MSV11-A 1K by 16-Bit Read/Write Memory

CP-1747

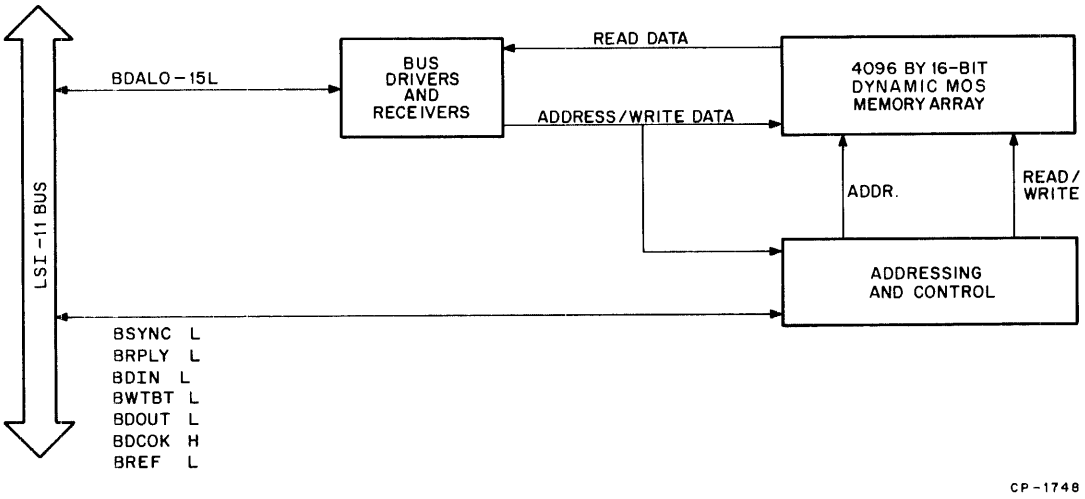


Figure 7-2 MSV11-B 4K by 16-Bit Read/Write Memory

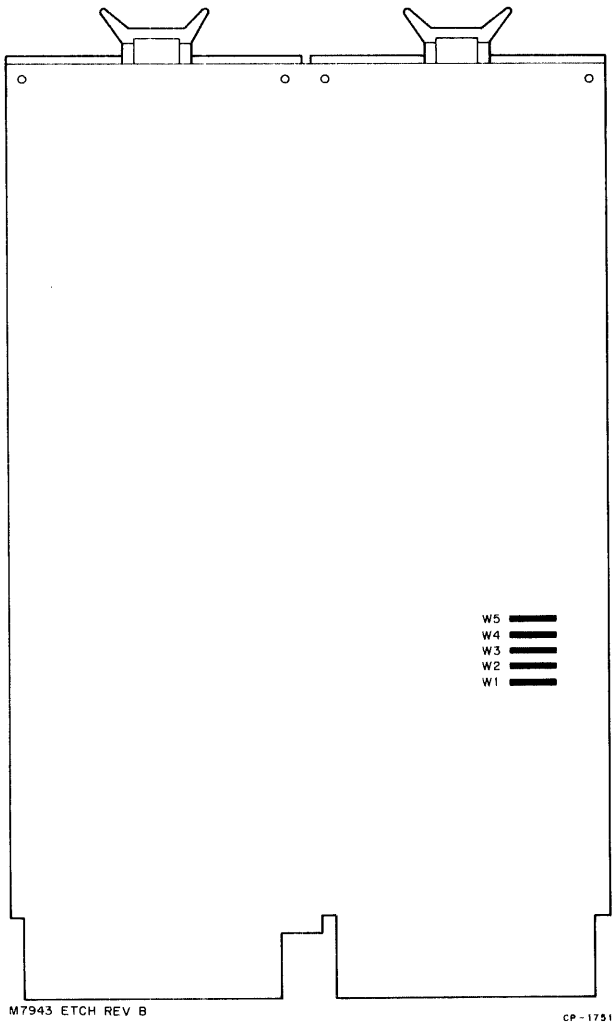


Figure 7-3 MSV11-A Jumper Locations

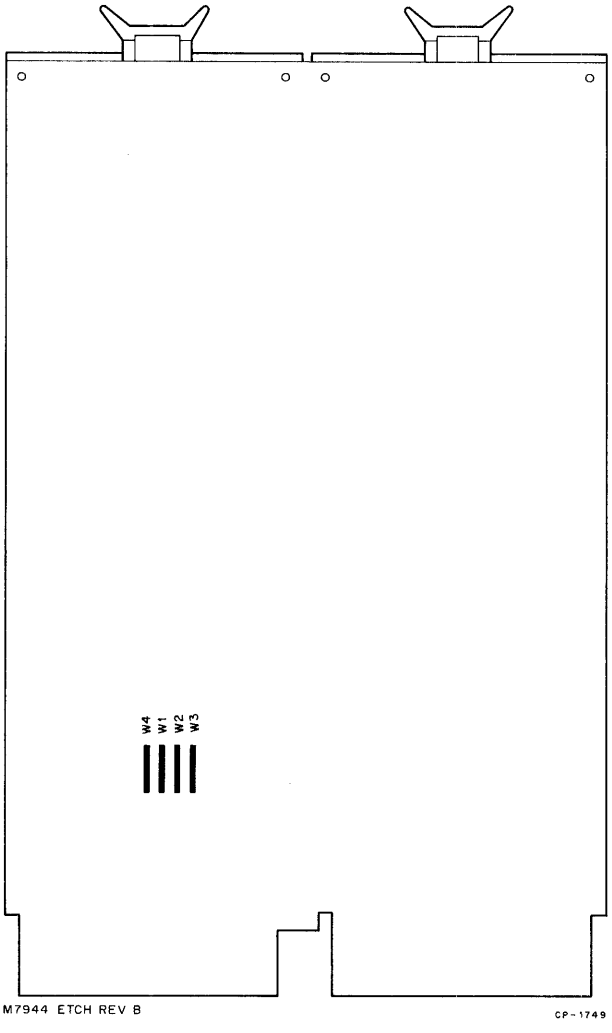


Figure 7-4 MSV11-B Jumper Locations

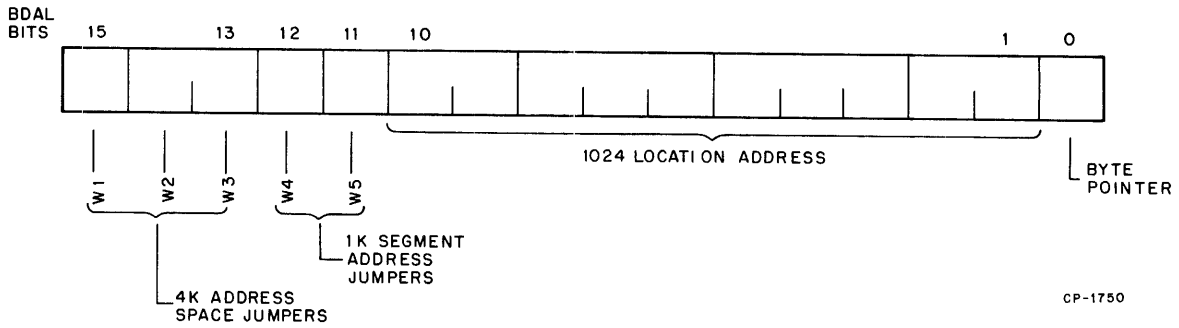


Figure 7-5 MSV11-A Address Format/Jumpers

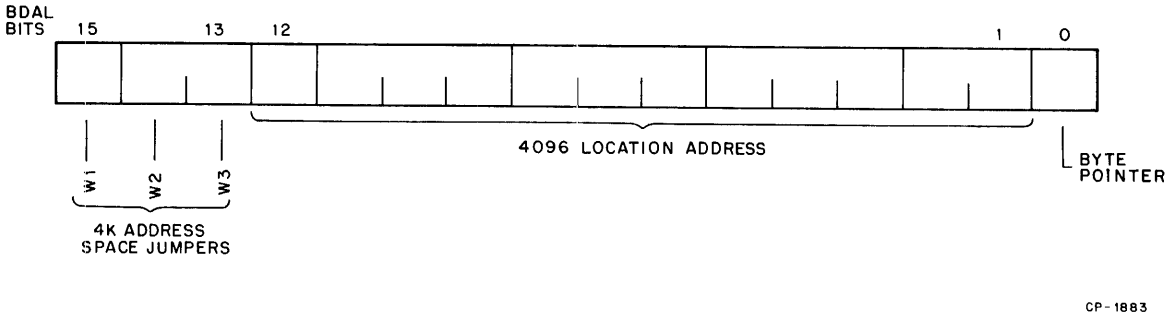


Figure 7-6 MSV11-B Address Format/Jumpers

CHAPTER 8
USING MMV11-A CORE MEMORY

8.1 GENERAL

The MMV11-A core memory option comprises two modules (G653 and H223) which are mated by connector pins in a single 8.5 by 10 by 0.9 inch assembly. It requires two device locations (electrical positions) on the backplane when installed in slots A4-D4 (Figure 11-1); otherwise, because of its total thickness (0.9 inch), the MMV11-A requires four physical device locations when installed in any other backplane slot.

8.2 SWITCH-SELECTED ADDRESSING

8.2.1 General

The only preparation required for the MMV11-A before it is installed in the backplane is to select its bank address. This is accomplished by opening or closing switches in appropriate address bit locations to produce the desired bank address decoding.

(Refer to Paragraph 11.3.3 for installation considerations.) Memory capacity is 4096 16-bit words. Address decoding jumpers allow the user to select the 4K bank address to which the MMV11-A will respond.

The MMV11-A is fully LSI-11 bus-compatible and can be accessed by the LSI-11 microcomputer or any DMA device that becomes bus master. It interfaces with the bus as shown in Figure 8-1.

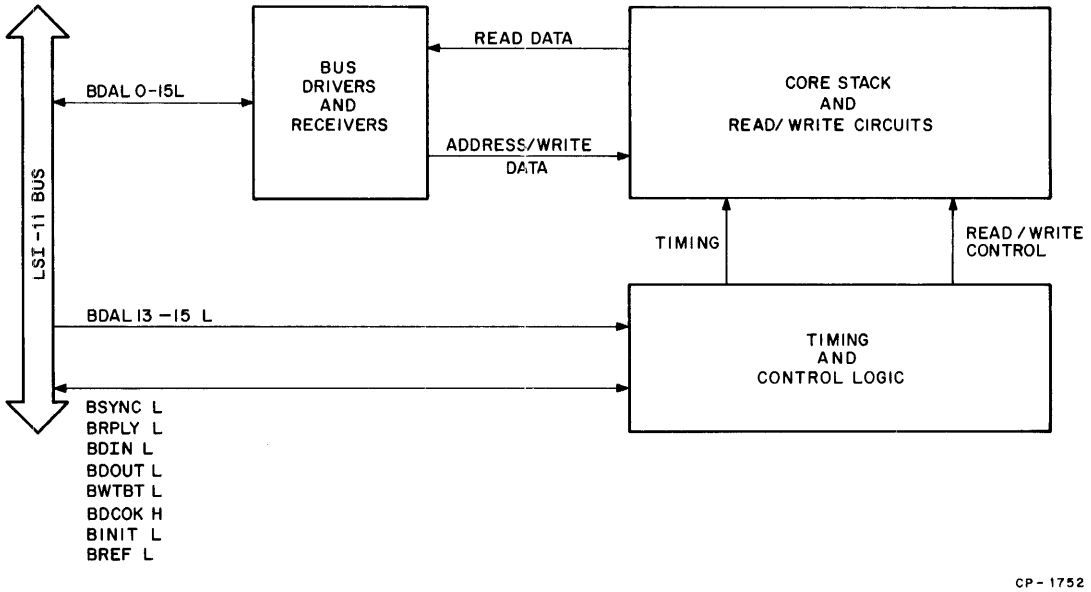


Figure 8-1 MMV11-A 4K by 16-Bit Core Memory

MMV11-A bank address switches are used as shown in Figure 8-3. The figure illustrates a 16-bit address and how switches are assigned to each address bit. Open or close switches to produce the desired bank address as directed in the figure. Switches are located on the G653 module (component side) as shown in Figure 8-2.

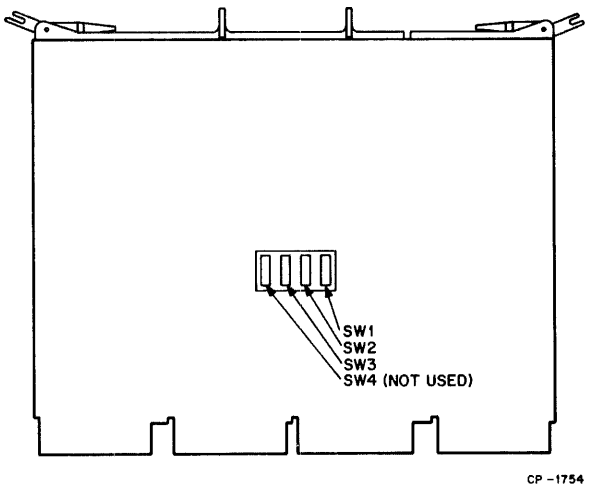


Figure 8-2 Bank Address Switch Locations

8.3 BUS RESTRICTIONS

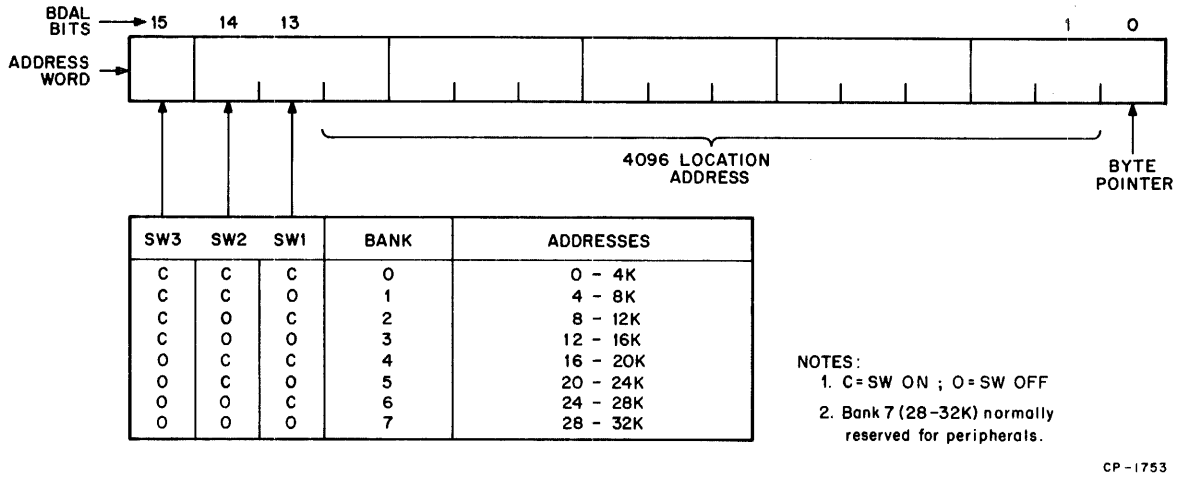
The BDMGI L and BIAKI L bus lines must be jumpered to BDMGO L and BIAKO L lines, respectively, under the H223 module when installed between the processor and I/O device interface modules in order to maintain daisy-chain signal continuity.

Pins which must be connected are:

From	To	Signal
AM2	AN2	BIAKI/O L
CM2	CN2	BIAKI/O L
AR2	AS2	BDMGI/O L
CR2	CS2	BDMGI/O L

Bus pins can be identified as shown in Figures 3-2 and 3-3.

Memory refresh is not required for this memory option. If memory refresh is used for other memory options, such as the KD11-F's resident memory and the MSV11-B semiconductor memory, the MMV11-A will not respond to the refresh operation.



SW3	SW2	SW1	BANK	ADDRESSES
C	C	C	0	0 - 4K
C	C	O	1	4 - 8K
C	O	C	2	8 - 12K
C	O	O	3	12 - 16K
O	C	C	4	16 - 20K
O	C	O	5	20 - 24K
O	O	C	6	24 - 28K
O	O	O	7	28 - 32K

NOTES:
1. C = SW ON ; O = SW OFF
2. Bank 7 (28-32K) normally reserved for peripherals.

Figure 8-3 MMV11-A Addressing

CHAPTER 9
USING MRV11-A READ-ONLY MEMORY

9.1 GENERAL

The MRV11-A (Figure 9-1) is a read-only memory module which allows the use of user-supplied, preprogrammed, programmable read-only memory (PROM) and masked read-only memory (ROM) chips in a compact, nonvolatile memory subsystem. Depending upon chip types, the module's capacity is either 4096 16-bit words or 2048 16-bit words, using 512 by 4-bit or 256 by 4-bit chips, respectively. Full address decoding is provided on the module. The user can select the 4K address bank in which the module resides by installing (or removing) jumpers on the module. Similarly, when using 256 by 4-bit chips, the user can jumper-select the upper or lower 2K segment within the selected 4K address bank. Note that 512 by 4-bit and 256 by 4-bit chips cannot be mixed on a MRV11-A module; the user configures jumpers on the module for the chip type being used.

A partial listing of manufacturer's chips that will operate in the MRV11-A is given in Table 9-1.

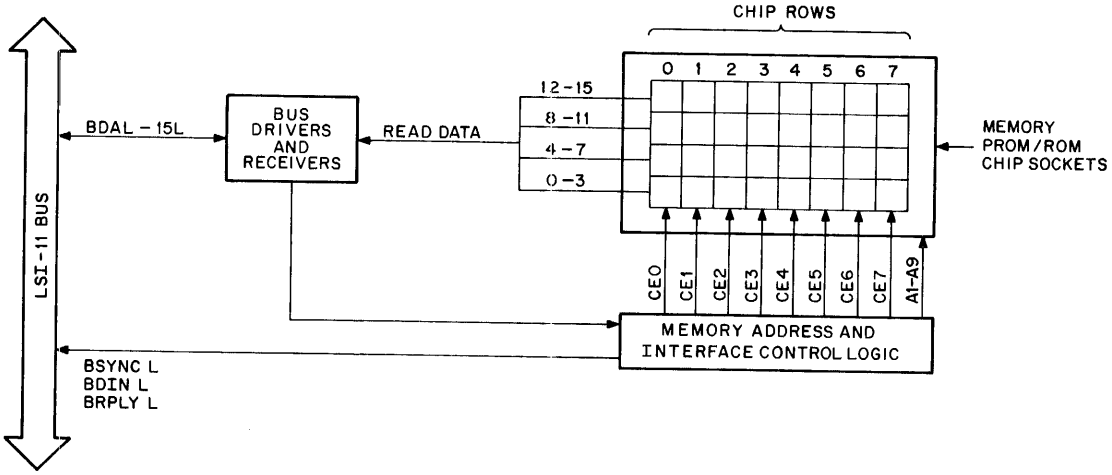


Figure 9-1 MRV11-A Read-Only Memory

Table 9-1
MRV11-A Chips

Manufacturer or Source	512 by 4-Bit Chips		256 by 4-Bit Chips	
	Model/Type	PROM/ROM	Model/Type	PROM/ROM
Digital Equipment Corp.	MRV11-AC	PROM	—	—
Intersil	IM5624	PROM	IM5623	PROM
Signetics			8259	PROM

Chips used must be tristate output devices which conform to the device pinning, data, and addressing described in the remainder of this chapter.

The user can install chips in increments of four chips each. When using 512 by 4-bit chips, memory expansion is in 512-word increments. When using 256 by 4-bit chips, memory expansion is in 256-word increments. Unused portions within the 4K bank in which the MRV11-A resides can be used by another memory device, such as the MSV11-A 1K by 16-bit read/write memory module. Jumpers on the MRV11-A can be cut by the user to prevent an incorrect BRPLY L signal from being generated when unpopulated locations are addressed on the module.

The information contained in the remainder of this chapter will enable the user to prepare the MRV11-A

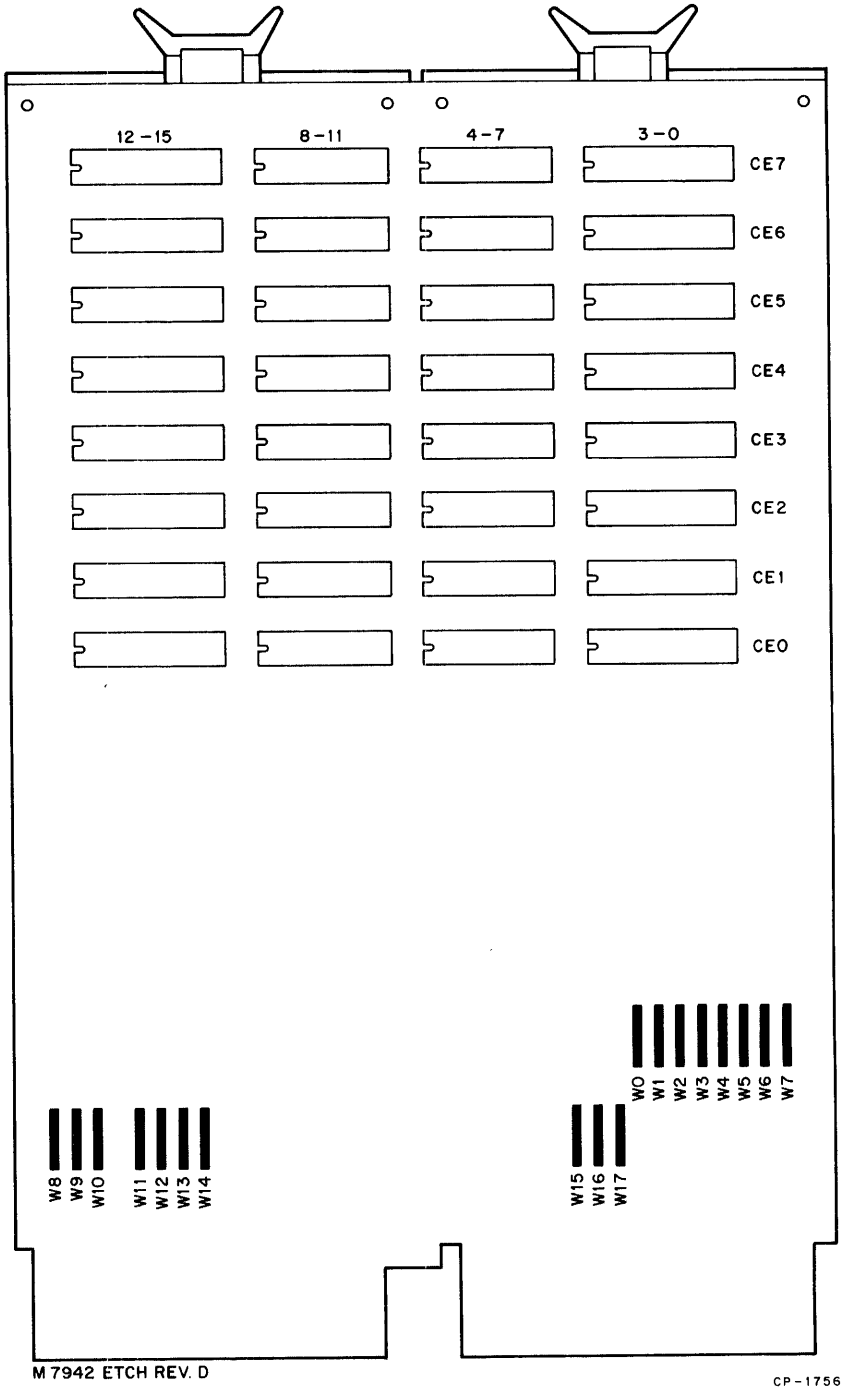


Figure 9-2 MRV11-A Jumper Locations

for use (jumper-selected addressing and chip selection) and includes information required for correct PROM and ROM programming.

9.2 JUMPER-SELECTED ADDRESSING AND CHIP TYPE

9.2.1 General

Jumpers which allow the user to select the 4K bank in which the module can be addressed and jumpers which allow the use of 512 by 4-bit or 256 by 4-bit PROM (or ROM) chips are provided on the MRV11-A. In addition, jumpers may be removed from the module to prevent the module from generating an active BRPLY L signal when a portion of the module is addressed that does not contain PROM or ROM chips. Jumpers are located as shown in Figure 9-2.

9.2.2 Chip Type Selection

The module is supplied with jumpers W8, W9, and W10 installed for use with 512 by 4-bit chips. When using 256 by 4-bit chips, W8, W9, and W10 must be cut or removed and jumpers W11 and W12 installed; in addition, either W13 (lower 2K) or W14 (upper 2K) must be installed to properly address the lower 2K or upper 2K address segment within the 4K memory bank.

9.2.3 Addressing and Reply

The user must consider both 4K bank address selection and BRPLY L signal generation when configuring a module for use. Chips (either PROM or ROM, 512 by 4 or 256 by 4) are arranged in eight physical rows (CE0—CE7) of four chips each. Entire rows can be unpopulated, allowing those addressed locations to be used by read/write memory contained on another module. When this is done, the BRPLY L jumpers (W0—W7) associated with the unused rows should be cut or removed to prevent the MRV11-A from returning a BRPLY L signal when those rows are addressed. A listing of octal addresses (within a 4K bank), physical rows, and BRPLY L jumpers is provided in Table 9-2; use data listed for the chip type being used.

The 4K bank in which the MRV11-A resides is programmed by connecting bank address jumpers W15—W17, as appropriate. The module is supplied with no bank address jumpers installed (bank 0). Jumpers not installed represent logical 0s; jumpers installed represent logical 1s.

Figure 9-3 illustrates addressing words used with the MRV11-A. Refer to the addressing format for the type of PROM or ROM chips being used.

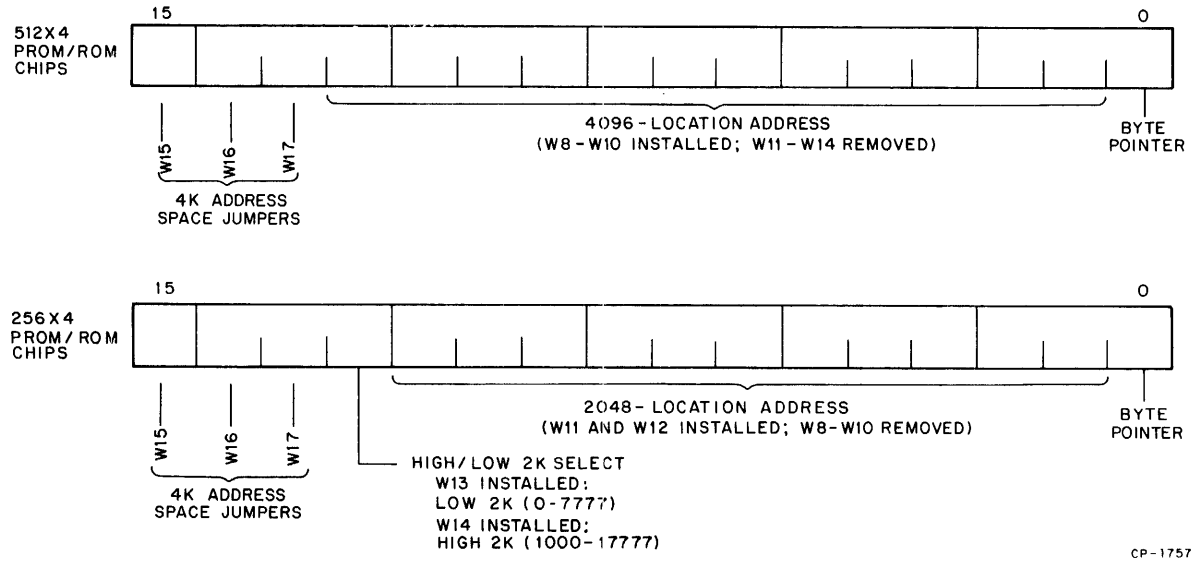


Figure 9-3 MRV11-A Address Word Formats

Table 9-2
PROM/ROM Chip Addressing Data

512 by 4 Chips			256 by 4 Chips			
Word/Byte Address	Physical Row	BRPLY L Jumper	Word/Byte Address W13 Installed	Word/Byte Address W14 Installed	Physical Row	BRPLY L Jumper
0-1777	CE0	W0	0-777	10000-10777	CE0	W0
2000-3777	CE1	W1	1000-1777	11000-11777	CE4	W4
4000-5777	CE2	W2	2000-2777	12000-12777	CE1	W1
6000-7777	CE3	W3	3000-3777	13000-13777	CE5	W5
10000-1777	CE4	W4	4000-4777	14000-14777	CE2	W2
12000-13777	CE5	W5	5000-5777	15000-15777	CE6	W6
14000-15777	CE6	W6	6000-6777	16000-16777	CE3	W3
16000-17777	CE7	W7	7000-7777	17000-17777	CE7	W7

9.3 PROGRAMMING PROM AND ROM CHIPS

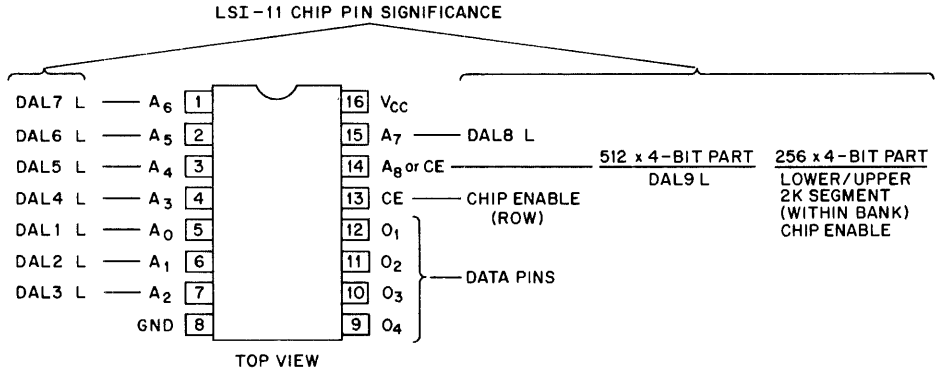
The actual procedure for loading data into PROM chips or writing specifications for masked ROM chips will vary, depending upon the chip manufacturer. Those procedures are beyond the scope of this document. (See chip manufacturer's data sheets.) However, the user must be aware of the chip pins versus LSI-11 data bit relationship, and the chip pin versus memory address bits. Address and data pins are described below.

As previously discussed, chips are arranged in rows of four chips each. Each chip contains locations of four bits each. Hence, four chips are used to provide the 16-bit data word formats for each row. Rows are designated by their respective Chip Enable (CE0—CE7) signals. Depending upon the chip type used, a row of four chips contains 512 or 256 16-bit read-only memory locations. The actual chip within a row is designated by one additional digit (0, 1, 2, or 3). Hence, the data pins are assigned to LSI-11 bus bits as listed in Table 9-3.

Table 9-3
Data Pin Assignments

Chip Pin	Chip 0	Chip 1	Chip 2	Chip 3
9	BDAL3	BDAL7	BDAL11	BDAL15
10	BDAL2	BDAL6	BDAL10	BDAL14
11	BDAL1	BDAL5	BDAL9	BDAL13
12	BDAL0	BDAL4	BDAL8	BDAL12

Addressing of chips is shown in Figure 9-4. All chips used on the MRV11-A must conform to this information. Observe that the only difference between 512 by 4-bit and 256 by 4-bit chip pins is pin 14. The 512 by



NOTE:
Designations immediately adjacent to pins are typical designations used by chip manufacturers — not LSI-11 designations. LSI-11 designations for correct addressing are located away from the chip. Observe that these signals are low — active; they are double-inverted bus signals (low = logical "1").

IC-0169

Figure 9-4 PROM/ROM Chip Pin Addressing

4-bit part uses this pin for address bit DAL9; the 256 by 4-bit part uses this pin for a chip enable when both bank address and 2K segment address are true. Also note that bus address bits do not follow in sequence with chip manufacturer's address designations. The pinning arrangement shown allows for the use of commonly available PROM and ROM chips and optimum (compact) MRV11-A module layout.

9.4 PROGRAMMING RESTRICTIONS

Special care must be used when programming PROMs or ROMs for use with MTPS instructions and KEV11 option EIS instructions. These instructions fetch source operands via the DATIO bus cycle, rather than the DATI bus cycle. Hence, fetching a source operand from a PROM or ROM location will result in a bus error (timeout) because the processor will attempt to write into the same location. When fetching MTPS or EIS instruction source operands, first MOVe the source operand from the PROM or ROM location to a general register. MTPS or EIS instruction can then be executed using the general register contents as the source operand. If desired, read-write memory could be used instead of the general register to temporarily store the source operand.

9.5 TIMING AND BUS RESTRICTION

Addressed memory read data is available within 120 ns after the BSYNC L signal is received by the MRV11-A. Logic on the module responds to DATI bus cycle only. DATO or DATOB bus cycles will result in a bus time-out error. Logic functions on the module are not affected by the bus initialize (BINIT L) signal.

CHAPTER 10
USER-DESIGNED INTERFACES

10.1 GENERAL

This chapter contains sample circuits and information which can be utilized in user-designed hardware that is installed on the LSI-11 bus. The user must ensure that the circuit, as used in a particular application, conforms to the LSI-11 bus specifications included in Chapter 3. The various interface module and prewired backplane options previously described in this manual are designed for ease of user prototype development. However, in those applications that require a special interface module, hardware components listed in the *Hardware/Accessories Catalog* will enable backplane connector-compatible systems to be rapidly assembled.

10.2 BUS RECEIVER AND DRIVER CIRCUITS

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 10-1. Any device that meets these requirements is acceptable. To perform these functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 10-1. A typical bus driver circuit is shown in Figure 10-2. Note that DEC 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package.

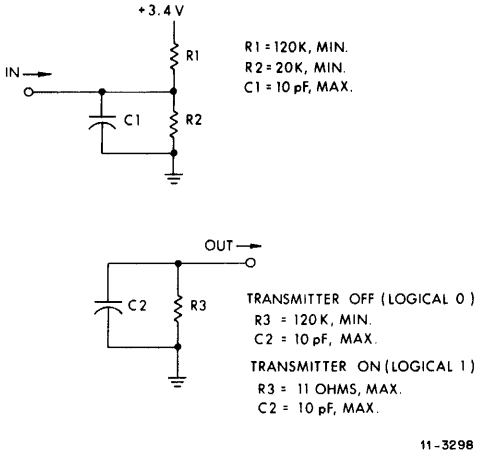


Figure 10-1 Bus Driver and Receiver Equivalent Circuits

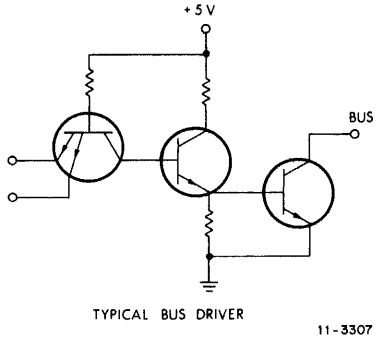


Figure 10-2 Typical Bus Driver Circuit

Table 10-1
LSI-11 Bus Driver, Receiver, Transceiver Characteristics

	Characteristic		Specifications	Notes
Receiver (DEC 8640, DEC 8641)	Input high threshold	VIH	1.7 V min.	1
	Input low threshold	VIL	1.3 V max.	1
	Input current at 2.5 V	IIH	80 μA max.	1, 3
	Input current at 0 V	IIL	10 μA max.	1, 3
	Output high voltage	VOH	2.4 V min.	2

Table 10-1 (Continued)
LSI-11 Bus Driver and Receiver Characteristics

	Characteristic		Specifications	Notes
	Output high current	IOH	(16 TTL loads)	2, 3
	Output low voltage	VOL	0.4 V max.	2
	Output low current	IOL	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min. 35 ns max.	4, 5
	Propagation delay to low state	TPDL	10 ns min. 35 ns max.	4, 5
Driver (DEC 8881, DEC 8641)	Input high voltage	VIH	2.0 V min.	6
	Input low voltage	VIL	0.8 V max.	6
	Input high current	IIH	60μA max.	6
	Input low current	IIL	—2.0 mA max.	6
	Output low voltage at 70 mA sink	VOL	0.8 V max.	1
	Output high leakage current at 3.5 V	IOH	25μA max.	1, 3
	Propagation delay to low state	TPDL	25 ns max.	5, 7
	Propagation delay to high state	TPDH	35 ns max.	5, 8

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390 Ω to +5 V and 1.6 K Ω in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
5. Times are measured from 1.5 V level on input to 1.5 V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.
7. Conditions of 100 Ω to +5 V, 15 pF to ground on output.
8. Conditions of 1 K Ω to ground on output.

Bus receivers and drivers should be well grounded and bypassed with capacitors. They should be located within 4 in. (of etch) from the module fingers which plug into the backplane.

10.3 PROGRAMMED INTERFACE

A typical programmed I/O interface is shown in Figure 10-3. Note that only the control logic portion is shown in detail. This circuit is capable of input and output data transfers to and from four addressable data registers in the user's device. In addition, the reply gate will respond to programmed I/O and vector transfers.

Address/data bus interface is provided by DEC 8641 quad unified bus transceiver ICs, keeping component count to a minimum. Note that the DEC 8641 IC at the bottom of Figure 10-3 shows complete address/data I/O signal connections; the remaining DEC 8641s include only the interface signals required for device addressing. However, those ICs will normally be connected for the same type of data I/O interface as shown at the bottom of the figure for bits 0, 13, 14, and 15.

Addressing occurs in the 28-32K address range; BBS7 L is always asserted for this address range. Received

data/address bits R3 H—R12 H and BS7 H are applied to 8136 (address) hex comparator/latch ICs where they are compared to a user-configured device address produced by switches or jumpers. The switches or jumpers must produce high logic levels for logical 1s and low logic levels for logical 0s. The result of the address comparison is latched in each 8136 on the leading edge of BSYNC L. The 8136 outputs will latch for the duration of BSYNC L, producing an active device selected (DEV SEL H) signal. The 74175 hex latch shown in Figure 10-3 latches address bits 0, 1, and 2 on the leading edge of BSYNC L. Bits 1 and 2 encode four

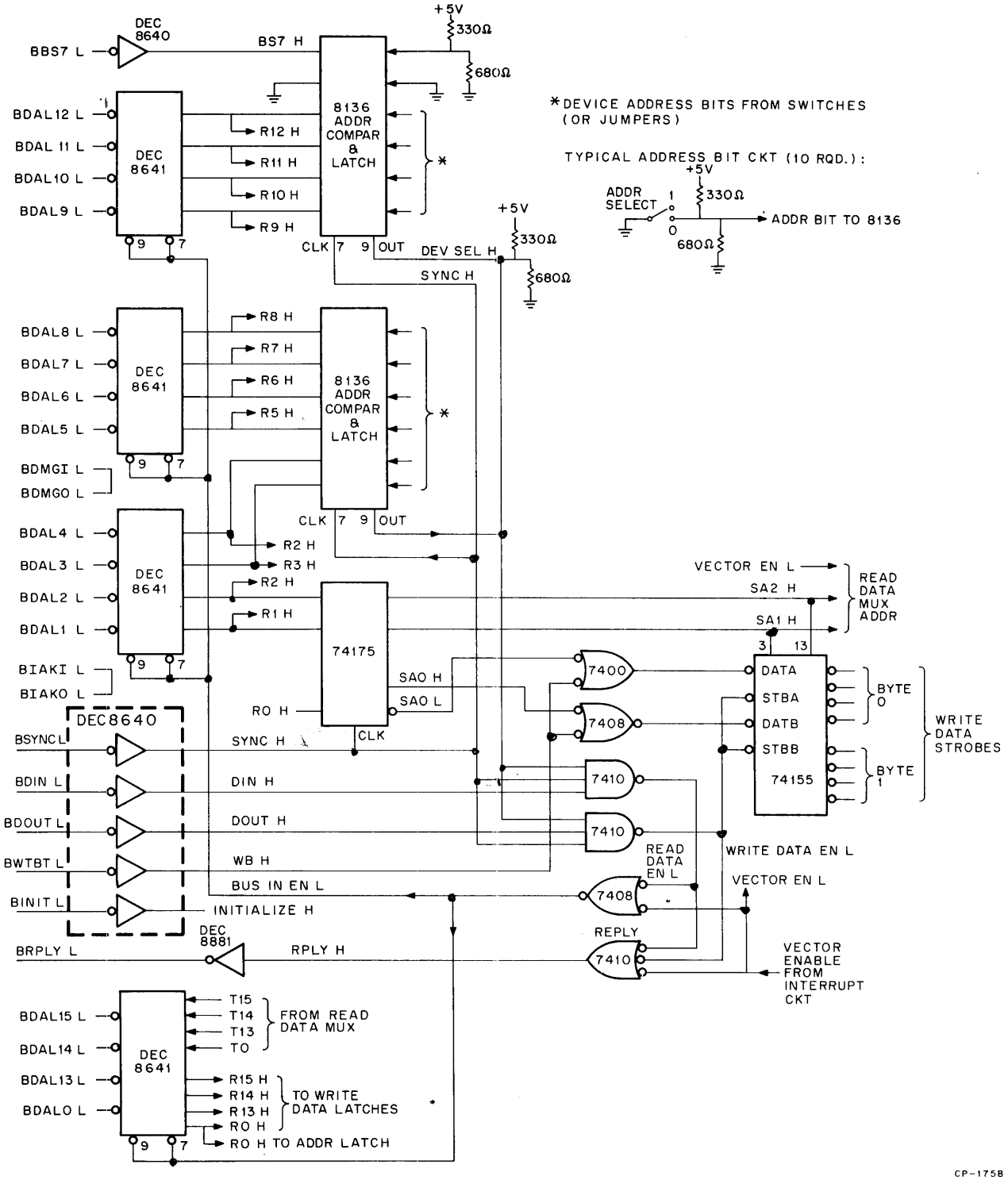


Figure 10-3 Programmed I/O Interface

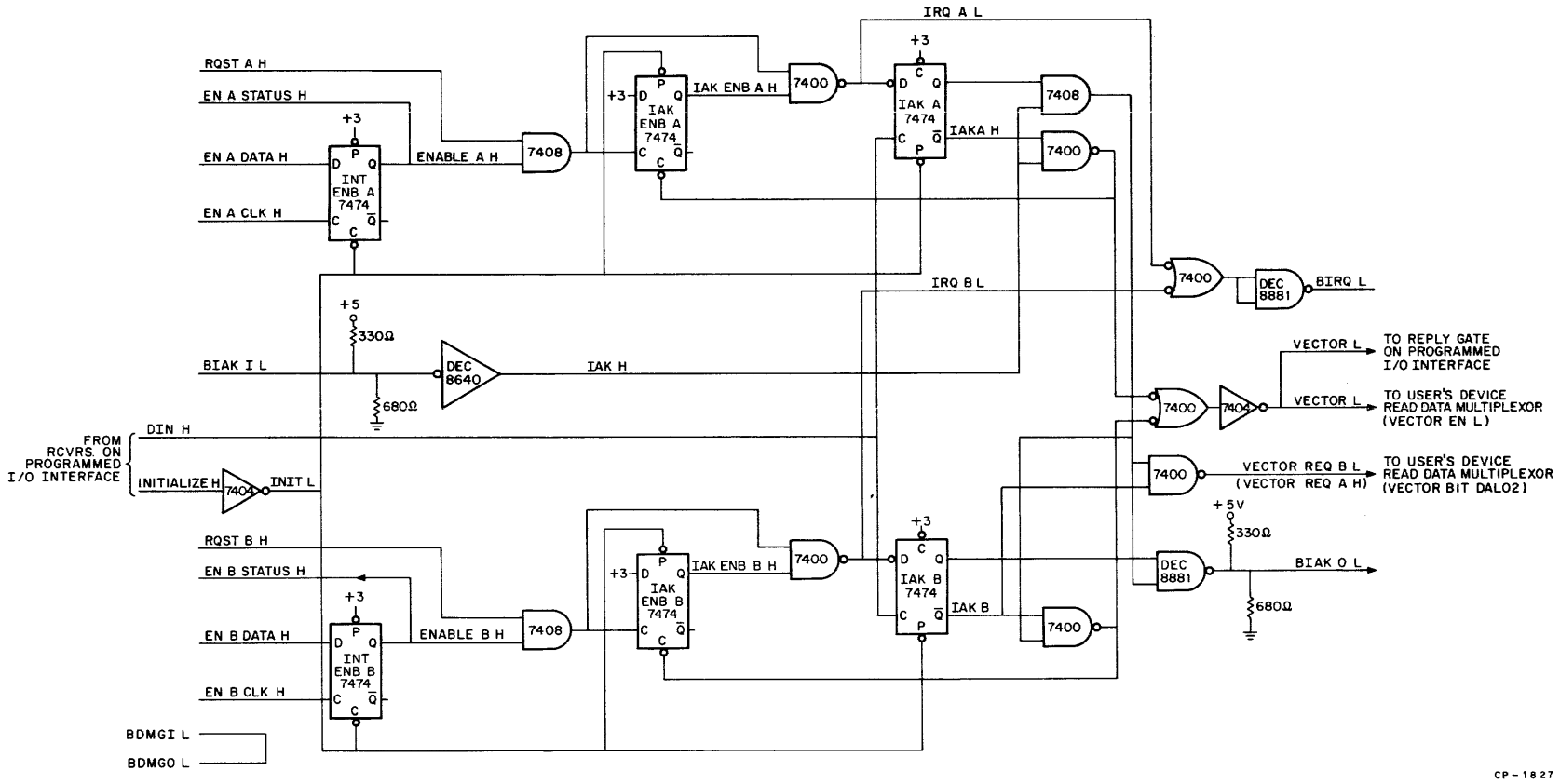


Figure 10-4 Dual Interrupt Interface

unique bus addresses for user-supplied I/O functions. Address bit 0 is a byte pointer which is only used for DATOB or the write portion of DATIOB bus cycles.

Read data should be multiplexed using stored address bits SA1 H and SA2 H. In addition, an interface circuit that also includes interrupt logic should use VECTOR EN L to inhibit register read data and enable the interrupt vector transfer during the interrupt sequence.

Write data strobed for the four addressable device registers are produced by a 74155 dual 2:4 demultiplexer; however, other devices and circuits can be used. Both sections of the 74155 are simultaneously strobed by the WRITE DATA EN L signal. During word transfers, WB H is passive (low), enabling the DATA and DATB demultiplexer inputs. As a result of the logical state of stored address bits SA1 H and SA2 H, one Byte 0 and one Byte 1 write data strobe will go active, enabling writing into all 16 bits of the addressed device register. However, when outputting a byte to one of the registers, WB H goes active (high), enabling stored address bit 0 (SA0 H and SA0 L) to assert only one data input (DATA or DATB) on the 74155. Hence, only one of the eight write strobes will go to the active state; an 8-bit transfer to the appropriate high or low byte in the addressed register is this completed.

10.4 INTERRUPT LOGIC

The basic logic functions required in an interrupt circuit are shown in Figure 10-4. This is a dual interrupt circuit which will enable and control two interrupt request sources (A and B) supplied by the user. The four flip-flops, ENABLE A and B, and INT REQ A and B comprise bits of one or two control/status registers (CSR). The set/reset status of the Enable flip-flops is established by a programmed output transfer. EN A CLK H and EN B CLK H signals are the write data strobes shown in Figure 10-3; EN A DATA H and EN B DATA H would then be two of the received data bits (DEC 8641 "Rn" outputs). Similarly, INT REQ A and B flip-flop outputs INT REQ A and INT REQ B would be read as bits in the CSR via the read data multiplexer in the device's logic.

A typical interrupt sequence for "device A" is described below. An interrupt is enabled under program control by setting the ENABLE A flip-flop. When the user's device is ready for service, it produces an active RQST A H signal, which is ANDed with ENABLE A. The AND gate output clocks the IAK ENB A flip-flop to the set state and IRQA L is produced. Note that if the user's device terminates the RQST A H signal, the IRQA L signal will go low (false), causing BIRQ to go false. IRQA L is ORed with IRQB L and applied to a type DEC 8881 bus driver, asserting the BIRQ bus signal line. The processor responds by asserting BDIN L, producing a high DIN H signal. This signal clocks the device states (A or B requesting or not requesting service) into the IAK flip-flops. At a later time, the processor asserts BIAKI L, producing a high IAK H signal. IAK H is gated with the IAK flip-flop signals, giving the highest priority to Request A, if both are requesting service. The 7400 gate associated with the IAK A flip-flop Q output goes low, clearing the IAK ENB A flip-flop, and producing VECTOR H and BRPLY L signals. VECTOR H is used for gating the vector address bits onto the I/O bus. With the device's IAK ENB flip-flop clear, it will not generate another interrupt until the device again requests service.

When not requesting service, both Interrupt Acknowledge (IAK) flip-flops remain cleared. The flip-flop Q outputs are both gated with IAK H, producing an active BIAKO L signal which is passed to the next (lower priority) device on the I/O bus. The INIT L signal, produced by a bus receiver and inverter, clears all Enable and IAK flip-flops, and presets (a don't care condition) all INT ENB flip-flops. When requesting service, the IAK flip-flops inhibit passing BIAKO L to the next lower priority device.

CAUTION

IAK flip-flops must function as synchronizers. (Data setup has no guaranteed minimum time.) Type 7474 and 74S74 are preferred.

10.5 DMA INTERFACE LOGIC

A simple DMA request circuit is shown in Figure 10-5. In addition to this circuit, bus address, word count, control/status registers, and burst transfer control logic would normally be included. All registers would be accessible via programmed I/O operations.

A DMA request is initiated by a device by producing an active REQ H signal. The RQST H signal must remain high until bus mastership is no longer required. The type DEC 8881 bus driver then asserts BDMR L.

The processor arbitrates the request by asserting BDMGI L, setting the Claim flip-flop in the first requesting device along the BDMG daisy chain. The state of the Claim flip-flop is sampled by two gates after the DMG delay. CLAIM (0) H is low (false) and it inhibits the DMGO EN H gate. Hence, when the Claim flip-flop is set, BDMGO L is not passed to lower priority devices. The active (high) CLAIM (1) H signal is gated

with DDMG H producing a low signal which enables one of the three 7427 gate inputs. When BSYNC L and BRPLY L become negated, passive (low) SYNCR H and RPLYR H signals are gated with CLAIM (1) H and the 7427 output goes high. This transition clocks the Master flip-flop to the set state producing the active MASTER H signal, enabling BSACK L and negating BDMR L signals. MASTER H is used by the DMA device to enable its bus cycle. BSACK L informs the processor that the bus is in use. At the end of the bus cycle, the device negates REQ H, clearing the Claim and Master flip-flops. MASTER H and BSACK L signals then go passive.

When not requesting DMA service, the device must pass BDMG signals to lower priority devices on the I/O bus. The active (high) CLAIM (0) H signal is gated with DDMG H producing an active DMGO EN H signal. This signal enables the BDMGO L bus driver and DMG H is gated onto the bus.

The actual DMG delay is determined by the RC circuit shown on the figure, and should be 100 ns (min). BINIT L initializes the circuit by clearing the Claim and Master flip-flops.

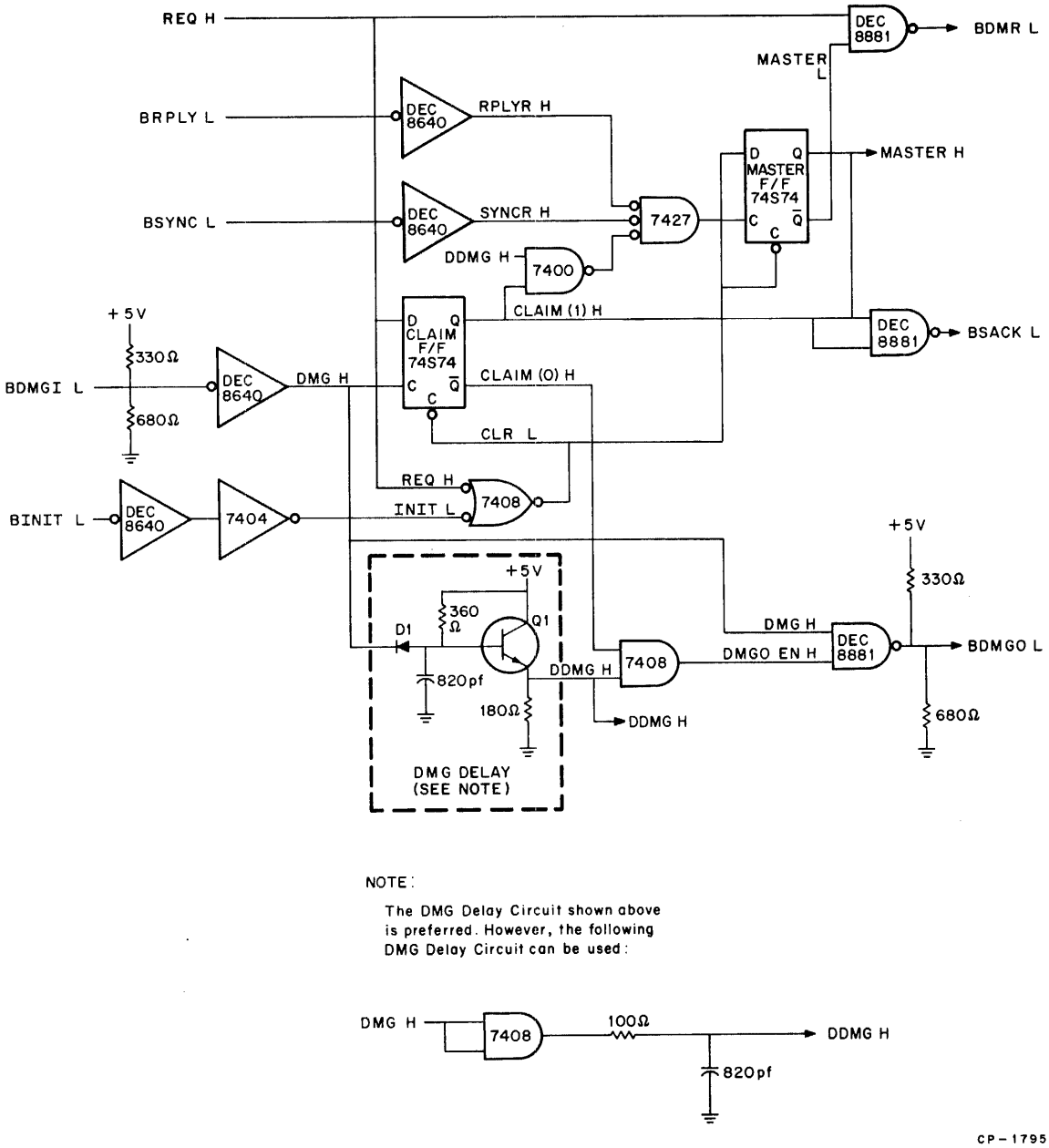


Figure 10-5 DMA Arbitration Logic

If dynamic MOS memory is used in the system (KD11-F processor and/or MSV11-B memory), a DMA device is restricted to one bus cycle for each BDMG signal from the processor. This must be done to allow the processor to execute memory refresh transactions. In systems which include dynamic MOS memory and use more than one DMA device, the DMA interface designer *must* ensure that sufficient time will be allowed for the processor to execute memory refresh transactions.

CAUTION

The Claim flip-flop must function as a synchronizer. (Data setup has no guaranteed minimum time.) Types 7474 and 74S74 are preferred.

CHAPTER 11
SYSTEM CONFIGURATION AND INSTALLATION

11.1 GENERAL

This chapter contains the basic considerations and requirements for configuring and installing LSI-11 or PDP-11/03 systems. The following paragraphs apply to both LSI-11 systems and PDP-11/03 systems, except where clearly stated otherwise.

11.2 CONFIGURATION CHECKLIST

LSI-11 and PDP-11/03 systems comprise user-selected module options as required for a particular application. Each module may require jumper alterations or switch settings to provide the correct addressing, operation, etc. for the user's application. A module configuration checklist for each module type is provided below. Detailed information for configuring the modules can be obtained by referring to the paragraphs listed in the checklist.

KD11 Processor Jumpers

Power-up mode (Paragraph 5.2.4)
Memory refresh enable (Paragraph 5.2.2)
Line time clock enable (Paragraph 5.2.3)
Resident memory 4K address selection (KD11-F only) (Paragraph 5.2.5)

DLV11 Serial Line Unit Jumpers

Device address (Paragraph 6.2.2.2)
Vector address (Paragraph 6.2.2.3)
Universal asynchronous receiver transmitter operation (Paragraph 6.2.2.4)
Baud rate selection (Paragraph 6.2.2.5)
EIA interface (Paragraph 6.2.2.6)
20 mA current loop interface (Paragraph 6.2.2.7)
Framing error halt (Paragraph 6.2.2.8)

DRV11 Parallel Line Unit Jumpers and Pulse Width Modification

Device address (Paragraph 6.3.2.2)
Vector address (Paragraph 6.3.2.3)
NEW DATA READY and DATA TRANSMITTED pulse width modification (Paragraph 6.3.4.6)

MMV11-A Memory 4K Address Selection

4K address select switches (Paragraph 8.2)

MRV11-A PROM/ROM Memory Jumpers

Memory address (Paragraph 9.2.3)
Reply signal (Paragraph 9.3)
512 by 4-bit or 256 by 4-bit PROMs (Paragraph 9.2.2)

MSV11-A 1K by 16 Random Access Memory Address Jumpers (Paragraph 7.2)

MSV11-B 4K by 16 Random Access Memory Jumpers

Memory address (Paragraph 7.3.1)
Reply to refresh (Paragraph 7.3.2)

The following checklist is for LSI-11 system configurations. It includes items that are not contained on particular modules but which must be checked to ensure that the system is properly installed.

1. BDCOK, BPOK, BEVNT, and BHALT signals connected as required to H9270 backplane assembly (Paragraph 11.7.5).
2. Modules inserted in H9270 backplane slots according to desired priority (Paragraph 11.3).
3. Jumpers added to H9270 backplane when core memory (MMV11-A) is located between processor and I/O device modules (Paragraph 11.3.3).
4. Correct cabling selected for I/O device modules (Paragraph 11.5).
5. Modules inserted in backplane slots with components facing in the correct direction (Paragraph 11.4).
6. Correct power and ground inputs to H9270 backplane connector block (Paragraphs 11.7.3. and 11.7.4).

a. Voltage and current requirements met

b. Correct terminal block power connections made

c. Proper ground connection

7. Environmental requirements met (Paragraph 11.7.5).

NOTE

Special cooling considerations might be required if more than one core or PROM module, or a combination of core and PROM modules, are implemented on one H9270 backplane assembly.

11.3 DEVICE PRIORITY

11.3.1 General

Device priority is established by the relative position of the device interface module along the I/O bus in which the devices are installed. The H9270 backplane is structured to allow the user to configure device priority by installing modules in appropriate positions. The H9270 is an LSI-11 option which should be considered when selecting LSI-11 system modules. The PDP-11/03 includes one factory-installed H9270 backplane.

11.3.2 Priority Selection Using the H9270 Backplane

Figure 11-1 is a front view of the H9270 backplane, showing typical module locations. The processor module should be installed in backplane slots A1-D1.

The LSI-11 bus structure includes two daisy-chained signals: BIAKO L/BIAKI L (for interrupts) and BDMGO L/BDMGI L (for DMA grant). These signals normally propagate through option modules until they reach the requesting device. Option 1, as shown in Figure 11-1, is the first device location to receive the daisy-chained signals when the processor module is installed in slots A1-D1. Hence, six options can be installed in the backplane. The PDP-11/03 is shipped with the processor module installed in the backplane as shown in the figure. Do not relocate the processor module to another location; a separate non-bused (jumper) connection is provided on the backplane to this location for proper RUN indicator operation.

Note that the daisy-chained BIAK and BDMG signals always follow in increasing numbered option locations, as shown in the figure. Do not configure the system with unused option locations in the backplane between the processor module and I/O devices which require either of the two daisy-chained signals; an unused location will break the daisy-chain signal continuity, and devices in higher numbered locations will not receive interrupt or DMA grant signals. Unused locations should occur only in the highest numbered option locations.

11.3.3 H9270 Backplane/MMV11-A Configuration

The MMV11-A position on the backplane should be carefully considered when configuring the system. The MMV11-A's physical size is four times greater than other LSI-11 module options, and it will require either two or four device (or option) locations on the backplane, depending on where it is located on the backplane. It is actually comprised of two 8.5 by 10 in. modules which are mated in a single assembly. However, only one module has fingers which plug into the backplane. Hence, if the MMV11-A is installed in backplane row 4, the MMV11-A module not having backplane fingers will be located below the backplane (where "row 5" should be located) and rows 2 and 3 will be available for other options. Thus, row 4 is the recommended location for the MMV11-A.

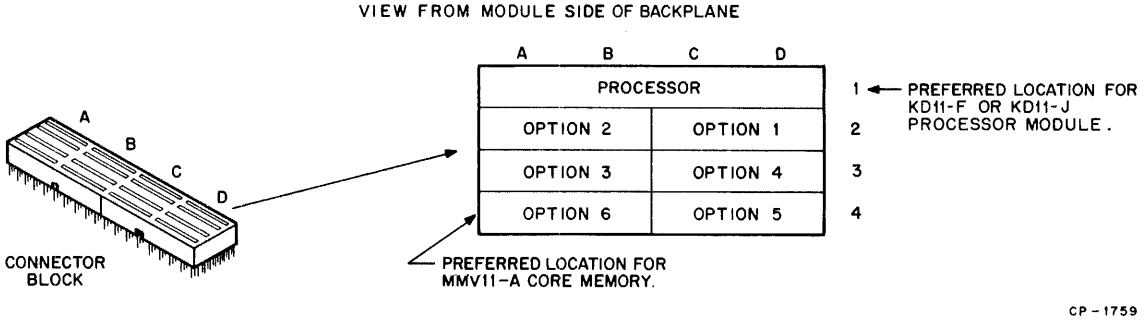


Figure 11-1 Typical Configuration LSI-11 Backplane — Processor and Option Locations

If the MMV11-A is installed in row 2, as shown in Figure 11-2, row 3 will also be occupied by the MMV11-A; however, the portion of the assembly in row 3 does not have backplane fingers. If any device modules are to be installed in row 4, it is necessary to install jumpers on the backplane in order to complete the DMA and interrupt grant signal chain. These jumpers (two required) should be wire wrapped between the backplane pins listed below:

H9270 Backplane/MMV11-A Jumpers

From	To	Signal
A01N2	A04M2	BIAKI/O L
A01S2	A04R2	BDMGI/O L

NOTE

These jumpers are required only if the MMV11-A is installed in row 2.

11.4 MODULE INSERTION AND REMOVAL

Modules must be installed or removed only when dc power is removed from the backplane. The PDP-11/03 contains a control/indicator panel on the front of the power supply; the DC ON/OFF switch allows the user to turn off dc power for safe module insertion and removal.

Modules must be installed in the backplane with components facing row 1, as shown in Figure 11-3.

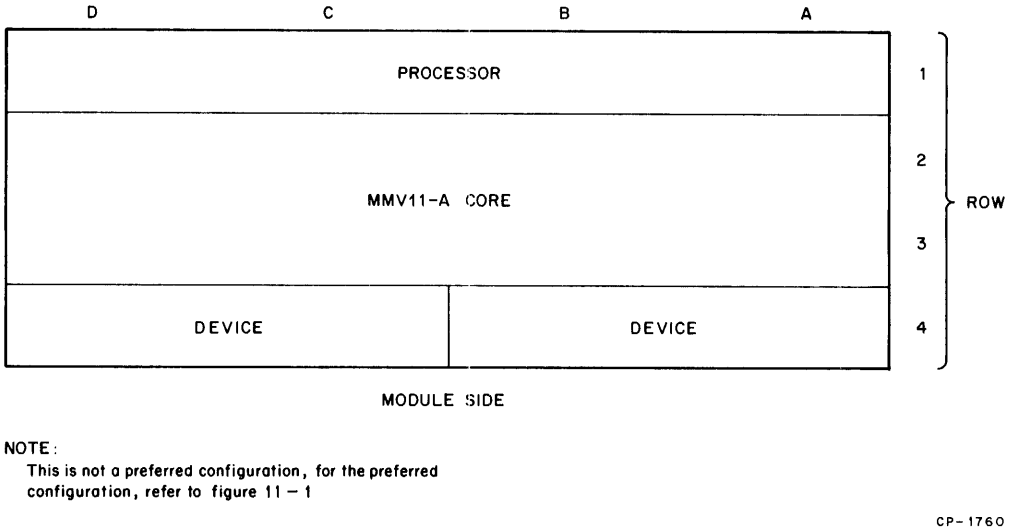


Figure 11-2 H9270 Backplane/MMV11-A Core

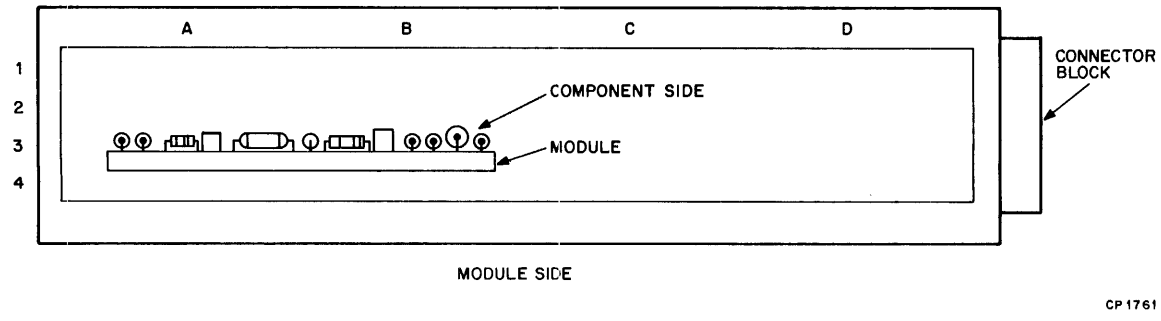


Figure 11-3 Module Installation in the H9270 Backplane

CAUTION

The LSI-11 modules and the backplane assembly mounting blocks may be damages if the modules are plugged in backward.

DC power must be removed from the backplane during module insertion or removal.

11.5 I/O CABLING

Recommended I/O cable options for use with the DLV11 serial line unit and DRV11 parallel line unit are listed below:

DLV11 Serial Line Unit	**Cable***
20 mA Current Loop	BC05M-X
EIA Interface	BC05C-X

DRV11 Parallel Line Unit	**Cable***
Any combination of one input and one output cable may be selected from the two types listed:	
Flat Cable	BC08R-X
Twisted Pair	BC11K-25

11.6 PDP-11/03 INSTALLATION PROCEDURE

11.6.1 Packaging and Mounting

The PDP-11/03 is packaged as shown in Figure 11-4. It is designed with a removable front panel. Removing the front panel exposes the LSI modules and cables. This enables replacement or installation of a module from the front of the PDP-11/03. The 11/03 power supply is located on the right-hand side of the PDP-11/03 when viewed from the front. The power supply contains three front panel switches and indicators which are accessible through a cutout in the front panel. Therefore, when the front panel is removed, the lights and switches are still attached and functional.

*The -X in the cable number denotes length in feet, as follows: -1, -6, -10, -20, -25. For example, a 10-ft EIA interface cable would be ordered as BC05C-10.

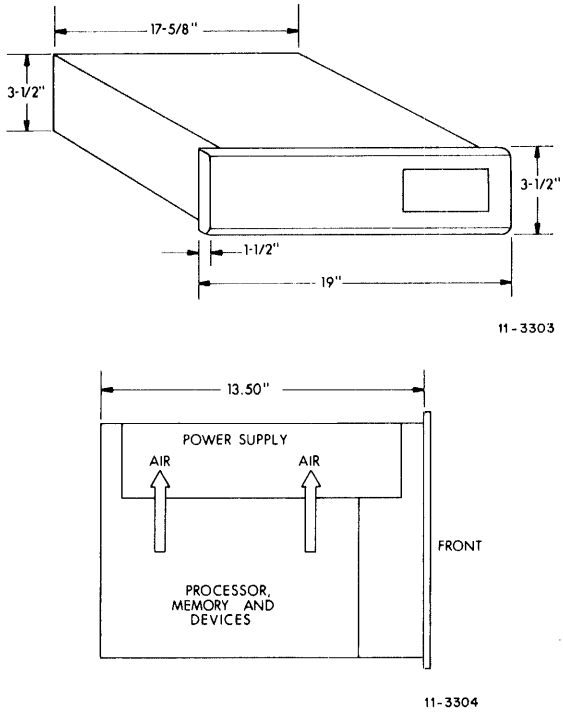


Figure 11-4 H9270 Backplane

Table 11-1
PDP-11/03 Input Power Electrical Specifications

Parameter	Model	Specifications
Input Power	PDP-11/03-AA or PDP-11/03-BA	100—127 Vac, 114 Vac nominal; 50 ± 1 Hz or 60 ± 1 Hz, single phase
	PDP-11/03-AB or PDP-11/03-BB	200—254 Vac, 230 Vac nominal; 50 ± 1 Hz or 60 ± 1 Hz, single phase
Input Power	All	400 W max at full load; 190 W typical
Temporary Line Dips Allowed	All	100% of nominal voltage: 9 to 20 ms 40% of nominal voltage: 20 to 96 ms 28% of nominal voltage: 96 to 500 ms

The PDP-11/03 is designed to mount in a standard 19 in. cabinet (Figure 11-5). A standard 19 in. cabinet has two rows of mounting holes in the front, spaced 18-5/16 apart. The holes are located 1/2 in. or 5/8 in. apart. Standard front panel increments are 1-3/4 in.

11.6.2 Power Requirements

Input (primary) power requirements are listed in Table 11-1.

An appropriate power cable and plug is supplied with all PDP-11/03 models. Note that a ground wire (and ground pin on the plug) must be connected to the normal service ground to ensure safe operation. Do not cut or remove the ground pin.

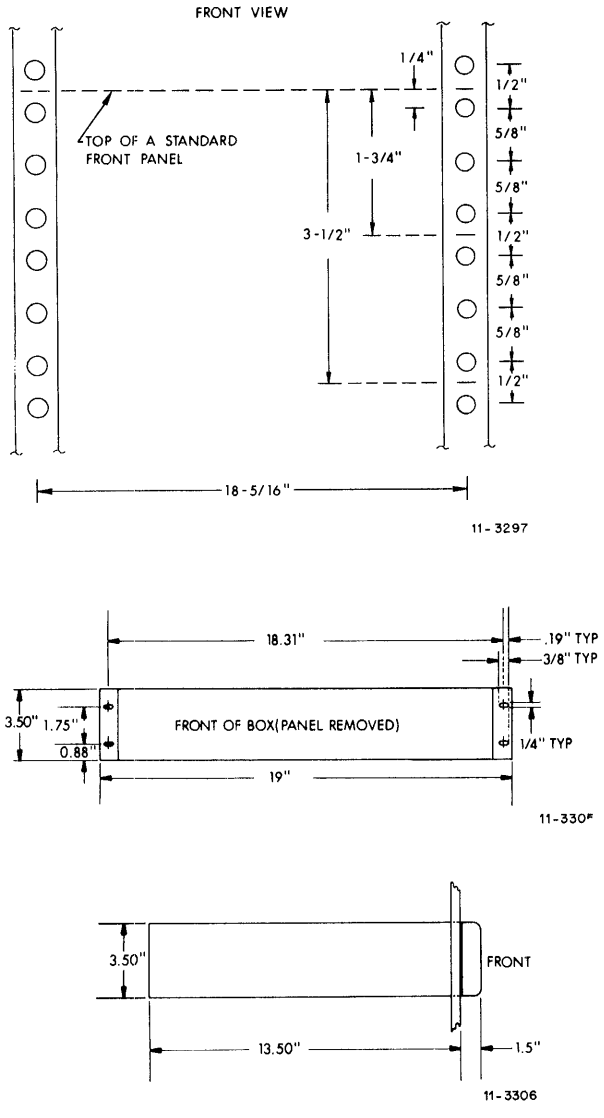


Figure 11-5 PDP-11/03 Cabinet Mounting

The H780 power supply provides the required dc power for the backplane in the PDP-11/03 enclosure. Typical dc power requirements will range from 33 to 120 W (max). In addition, the power supply generates the necessary BPOK H and BDCOK H power supply status signals, displays the RUN and DC status, and contains the ENABLE/HALT, DC ON/OFF, and LTC ON/OFF control switches.

Before attempting to operate the system, ensure that the system is configured as previously described in this chapter, and that environmental requirements are met.

11.6.3 Environmental Requirements

The PDP-11/03 will operate at temperatures of 41° to 104° F (5° to 40° C) with a relative humidity of 10 to 90 percent (no condensation), with adequate air flow across the modules. The fans in the H780 power supply will provide adequate air flow within the specified temperature range.

11.7 LSI-11 SYSTEM INSTALLATION

11.7.1 General

When installing the LSI-11 system, the user must mount the H9270 backplane, provide dc operating power, ground, and externally generated bus signals, and observe system environmental requirements. The following paragraphs describe the above items in detail.

11.7.2 Mounting the H9270 Backplane

The H9270 backplane (Figure 11-6) is designed to accept the KD11-F or KD11-J microcomputer and up to six I/O interface or memory modules. Mounting of the H9270 backplane can be accomplished in any one of three planes, as shown in Figures 11-7, 11-8, and 11-9.

11.7.3 DC Power Connections

11.7.3.1 Voltage and Current Requirements — A power supply for a single backplane LSI-11 system should have the following capacity:

+5 V ± 2% load; 0—18 A static/dynamic
+12 V ± 2% load; 0—2.5 A static/dynamic
+5 ripple: less than 1% of nominal voltage
+12 ripple: less than 150 mV pp (frequency 5 kHz)

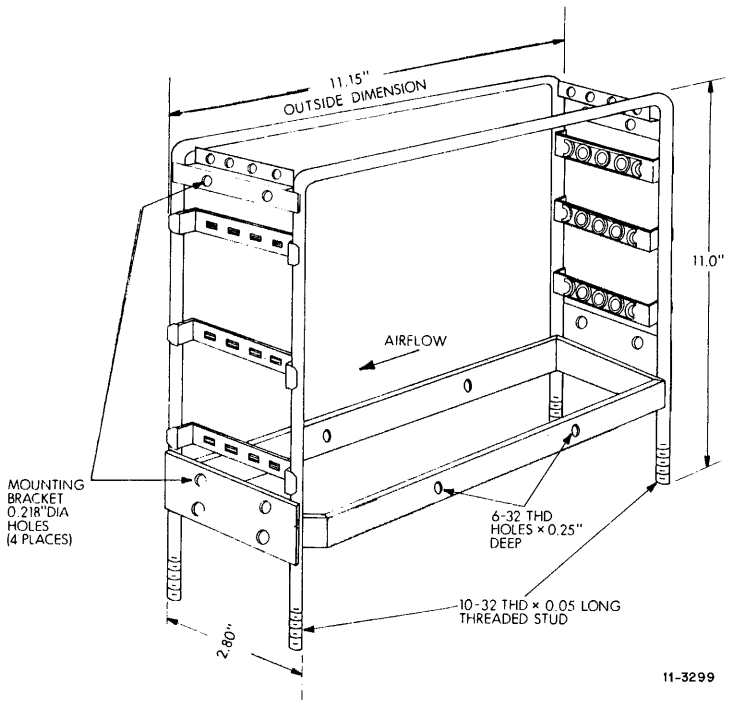


Figure 11-6 H9270 Backplane Mounting

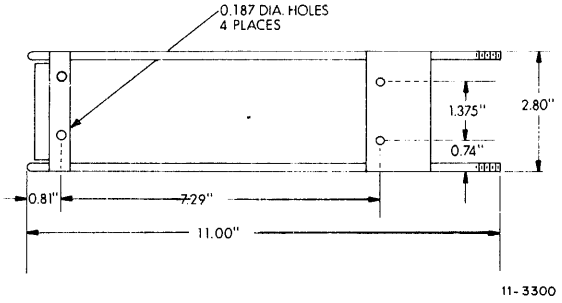


Figure 11-7 H9270 Side Mounting

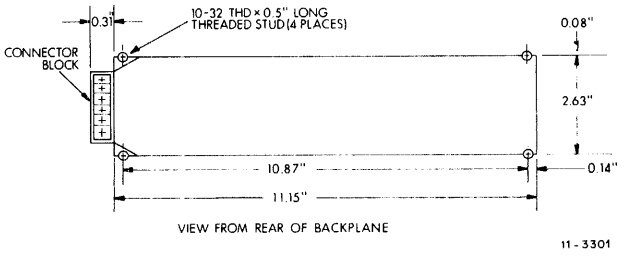


Figure 11-8 H9270 Rear Mounting

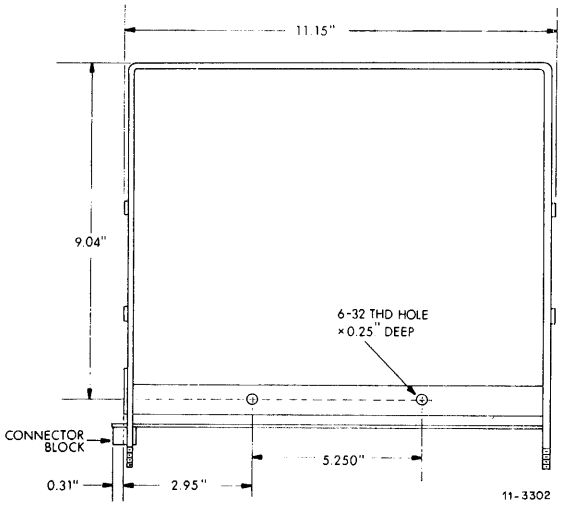


Figure 11-9 H9270 Top And Bottom Mounting

11.7.3.2 H9270 Backplane Power Connections — Perform the following steps to connect power to the H9270 backplane (Figure 11-10):

1. Select wire size. (14 gauge is recommended.) Consider load current and distance between the power supply and backplane.
2. For a standard system, connect the applicable wires to the H9270 connector block per Table 11-2.

   For battery backup, remove the jumper between +5V and +5B and connect the applicable wires to the H9270 connector block per Table 11-3.
3. Connect the ground terminals at the power sources.
4. It is recommended that the H9270 frame/casting be electrically connected to system/power supply ground.

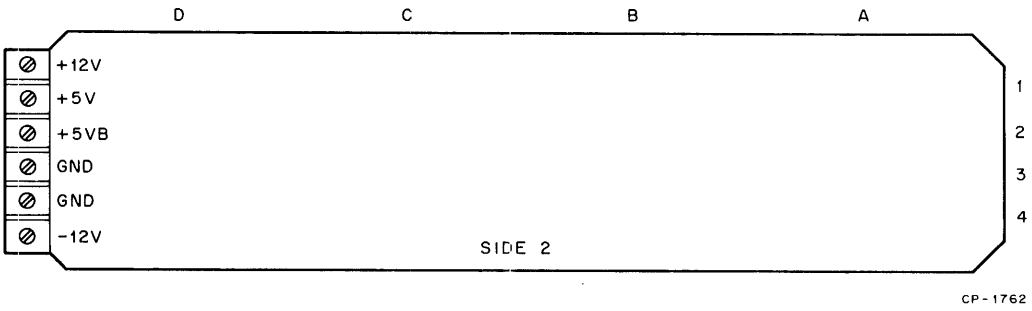


Figure 11-10 H9270 Backplane Terminal Block

Table 11-2
H9270 Backplane Standard Power Connections

Power Source (From)	H9270 Connector Block (To)	
+12 V	+12 V	
+5 V	+5 V +5B	Factory Connected
GND GND	GND GND	Factory Connected
-12 V	-12 V	(This voltage is not required. The connection is available for custom interfaces.)

Table 11-3
H9270 Backplane Battery Backup Power Connections

Power Source (From)	H9270 Connector Block (To)	
+12 V	+12 V	
+5 V (System Power) +5 B (Battery Backup)	+5 V +5B	Remove Factory Connection
GND GND	GND GND	Factory Connected
-12 V	-12 V	(This voltage is not required. The connection is available for custom interfaces.)

11.7.4 H9270 Backplane Ground Connection

Connect the H9270 backplane ground wire to system (or frame) ground in which the H9270 is installed. The ground terminal is located as shown in Figure 11-10.

11.7.5 Environmental Requirements

All LSI-11 modules will operate at temperatures of 41° to 122° F (5° to 50° C) with a relative humidity of 10 to 90 percent (no condensation), with adequate air flow across the modules. When operating at the maximum temperature (122° F or 50° C), air flow must maintain the inlet to outlet air temperature rise to 12.5° F (7° C) maximum. Air flow should be directed across the modules as shown in Figure 11-12.

11.7.6 Externally Generated Bus Signals

11.7.6.1 General— Externally generated bus signals include BDCOK H and BPOK H power status, BEVNT L (line time clock) (if required), and BHALT L (if desired). The signals are applied to the backplane via a connector and an optional mating connector as shown in Figure 11-13. The signals must conform to LSI-11 bus configuration specifications described in paragraphs 3.12, 3.13, and 10.2. Connections made to the backplane via the ribbon cable shown in Figure 11-13 must not exceed 12 inches in length. Each signal is discussed in the following paragraphs.

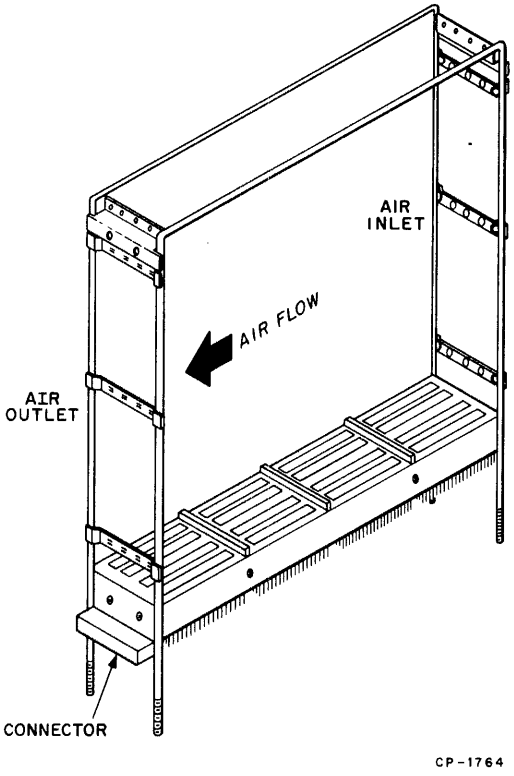


Figure 11-12 H9270 Backplane Air Flow

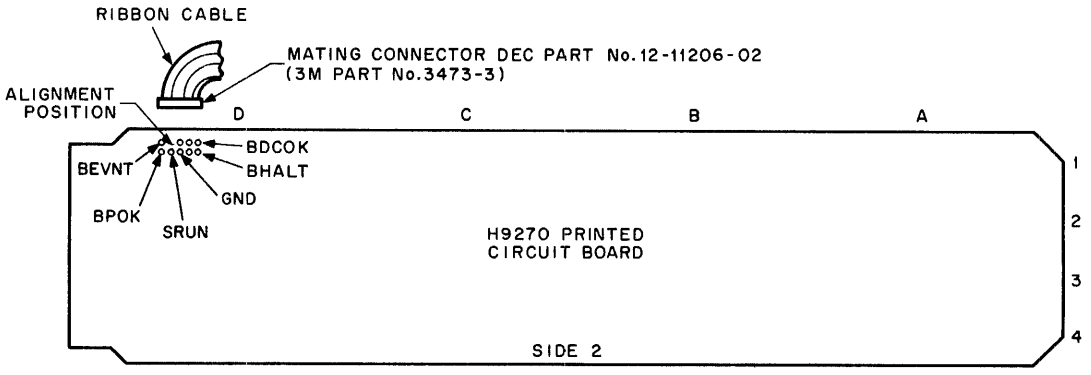


Figure 11-13 H9270 Backplane Printed Circuit Board

11.7.6.2 BDCOK H and BPOK H — The processor monitors power supply status and responds, as appropriate, by the BDCOK H and BPOK H signals. These signals are defined below:

BPOK H Assertion
8.0 ms of dc power reserve and BDCOK has been asserted for 70 ms min; 3.0 ms minimum assertion of BPOK required.

BPOK H Negation
4.0 ms of dc power reserve, but power is failing; 1.0 μs minimum negation time for BPOK.

BDCOK H Assertion
3.0 ms of dc power has been applied; 1.0 μs minimum assertion time for BDCOK.

BDCOK H Negation
5.0 μs of dc power reserve but no sooner than 3.0 ms after BPOK negation; 1.0 μs minimum negation time for BDCOK.

During the power-up sequence, after dc power has been applied (Figure 11-14), the processor asserts BINIT L in response to a passive (low) power supply-generated BDCOK H signal. When BDCOK H goes active (high), the processor terminates BINIT L after approximately 12 μs, and waits for assertion (high) of BPOK; then the user-selected power-up mode is executed. Similarly, if power fails (Figure 11-15), the power supply-generated BPOK H signal goes passive (low) and causes the processor to push the PC and PS onto the stack and enter a power fail routine via vector location 24 (power fail trap location). The processor will execute the power fail routine until either BDCOK H goes passive (low), indicating the dc operating power may not sustain processor operation, or BPOK H returns to the active state. BINIT L will be asserted if BDCOK H goes passive.

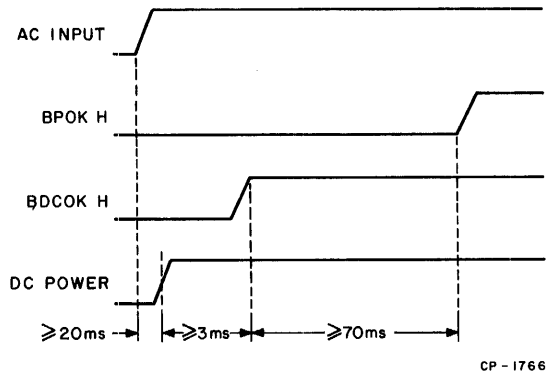


Figure 11-14 Power-Up Sequence

Generation of BPOK H and BDCOK H signals can be provided automatically via user-supplied logic, or manual operation can be selected, as follows:

Automatic: Connect BPOK H and BDCOK H signals from the power supply logic to H9270 backplane as shown in Figure 11-13.

Manual: Connect ground to a momentary ON/OFF switch (BDCOK switch), as shown in Figure 11-16. Connect the BDCOK switch output to the BDCOK H input on the H9270 backplane via a switch bounce eliminator. To initialize the processor after power is applied, the BDCOK switch must be momentarily depressed (off), then released (on).

NOTES

A switch bounce eliminator must be used with the manual BDCOK switch, as shown.

If the manual method of applying BDCOK H is selected, contents of semiconductor read/write memory may be lost when BDCOK switch is depressed.

NOTE

It is not necessary to negate the BPOK H signal when manually initializing the processor. BPOK H may be left unconnected.

11.7.6.3 BEVNT L Signal — The BEVNT L signal input to the H9270 backplane (Figure 11-13) is the external event interrupt. Asserting the BEVNT L signal initiates the LTC (line time clock) interrupt on the processor. The processor will trap through location 100_8 if PS bit 7 = 0. A typical circuit for generating BEVNT L is shown in Figure 11-13.

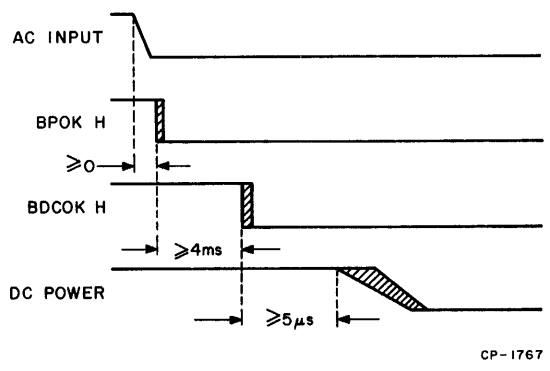


Figure 11-15 Power-Down Sequence

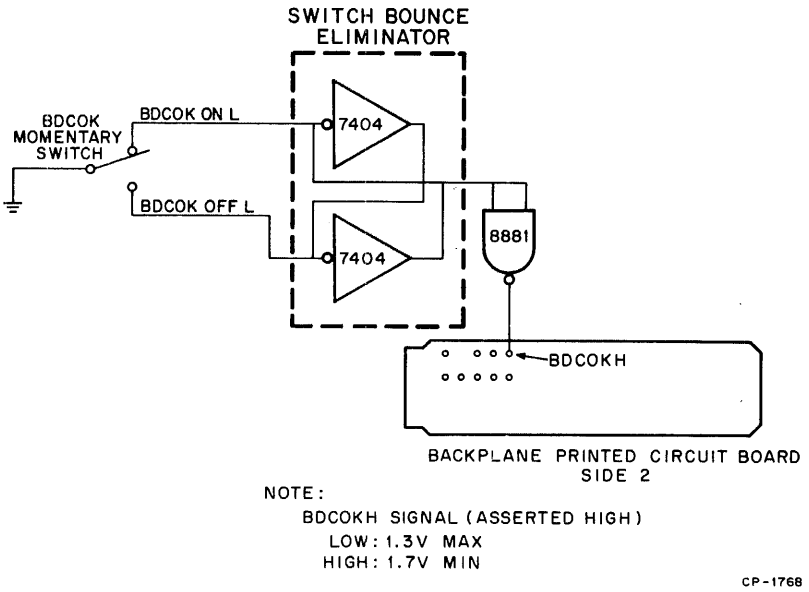


Figure 11-16 BDCOK H Signal Routing Diagram

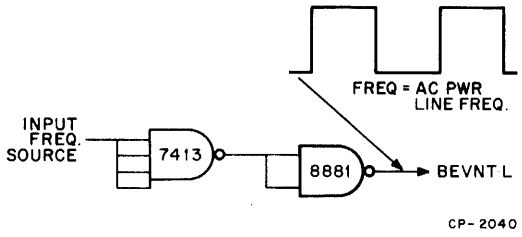


Figure 11-17 BEVNT L Signal

11.7.6.4 BHALT L Signal — Manual control of the Halt mode can be obtained by connecting a BHALT L signal line to the H9270 backplane printed circuit board as shown in Figure 11-13. The BHALT L signal level should meet bus specifications described in Paragraph 3.12.

When in the Halt mode, user program execution is not performed and the processor executes ODT console microcode. However, the processor will execute memory refresh in a normal manner and respond to DMA requests, even when BHALT is asserted; all device and LTC interrupt requests are ignored.

11.8 SYSTEM OPERATION

11.8.1 General

The procedures included in the following paragraphs describe power turn-on and operational checks for LSI-11 and PDP-11/03 systems. Refer to the *LSI-11, PDP-11/03 Processor Handbook* for detailed operation, including console ODT and program execution.

11.8.2 PDP-11/03 Power-On

Proceed as follows:

1. Ensure that the system is properly configured as previously described.
2. Place the DC ON/OFF switch in the down position (DC OFF).
3. Place the AC ON/OFF switch on the rear of H780 power supply in the ON position.
4. Place the HALT/ENABLE switch in the desired power-up position.

NOTE

The dc power can be applied with the HALT/ENABLE switch is either position. However, processor power-up mode is affected by this switch and jumper-selected power-up modes, as listed in Table 11-4.

5. Place the LTC ON/OFF switch in the OFF position.
6. Place the DC ON/OFF switch in the up (DC ON) position. The console device should respond with a printout (or display) as shown in Table 11-4.
7. Proceed with initial power-on checkout by entering and executing the program listed in Paragraph 11.8.4.

Table 11-4
Console Power-Up Printout (or Display)

Conditions	Mode 0 (Jumpers W5, W6 removed)	Mode 1 (Jumper W6 removed, W5 installed)	Mode 2 (Jumper W6 installed, W5 removed)	Mode 3 (Jumper W5 W6 installed)
BHALT L (unasserted), Dynamic RAM Memory	Processor will execute program. If there is no data in memory terminal will print out "000 002." (See Note 2.)	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Processor will execute program at location 173000. (See Note 2.)	No printout at terminal.
BHALT L (unasserted), Core Memory	Processor will execute program in core. (See Note 2.)	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Processor will execute program at location 173000. (See Note 2.)	No printout at terminal.
BHALT L (asserted), Dynamic RAM Memory	Terminal will print out contents of memory location 024 (normally "000 000").	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Terminal will print out "173000."	No printout at terminal.
BHALT L (asserted), Core Memory	Terminal will print out contents of memory location 024 (normally "000 000").	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Terminal will print out "173000."	No printout at terminal.

NOTES

1. If mode 3 is selected, and microaddress (3000—3777) is not implemented, the processor will trap to memory location 010. Trapping to 010 will be treated as a reserved instruction trap.
2. Whenever the PDP-11/03 is executing a program, the RUN indicator should be lit. If no program is provided or if a HALT instruction is executed, the RUN indicator will be extinguished.

11.8.3 LSI-11 Power-On

Proceed as follows:

1. Ensure that there is no dc power applied to the H9270 backplane.
2. Remove all modules from the backplane.
3. It is recommended that a single switch be used to apply +5 V and +12 V to the H9270 backplane. There is no required voltage application sequence.
4. Turn power-on.
5. At the H9270 backplane, check for the following voltages:

   Row 1, Slot A, Pin A2: +5 V
   Row 1, Slot A, Pin D2: +12 V
   Row 1, Slot A, Pin V1: +5 V

CAUTION

Do not plug in modules with power applied to H9270 backplane.

6. Turn power off.
7. Ensure that the system is properly configured and installed as previously described.
8. Turn on system power. Observe that the console device responds as described in Table 11-4.
9. Proceed with initial power-on checkout by entering and executing the program listed in Paragraph 11.8.4.

11.8.4 ASCII Character Console Printout Program

The following is a program that can be used to printout ASCII characters. The successful completion of this program can be used as a guide in determining the correct operation of the following:

KD11-F or -J Processor

DLV11 Serial Line Unit

LSI-11 data transfer and data control bus signals

Power input connections for +12 V and +5 V

This program does not explicitly check the following bus signals.

BDMR L	BHALT L	BSACK L
BPOK H	BIRQ L	
BDMGI/O L	BDCOK H	
BEVNT L	BIAKI/O L	

This program outputs all ASCII characters and may include control codes for specific devices.

Enter and execute the program via the console device as directed below:

1. Enter Starting address.
2. Press slash (/).
3. Enter instruction (octal code).
4. Press LINE FEED.
5. Repeat above steps until all instructions have been entered.
6. Press RETURN.
7. Enter starting address.
8. Press G.
9. Press the BREAK key on the console device to stop program. If the console device does not include the BREAK key, press the HALT switch (PDP-11/03 panel or the manual HALT switch described in Paragraph 11.7.6.4).

A sample console printout of the above program is shown in Figure 11-18.

11.9 PAPER TAPE SYSTEM OPERATION

11.9.1 General

Paper tape systems include no mass storage devices and programs must be read into system memory prior to system operation. Programs are read from punched paper tapes using either an optional low-speed reader, such as the LT-33 Teletypewriter, or a high-speed reader (user-supplied). The normal sequence of operations is:

1. Load the Absolute Loader
2. Load program tapes
3. Execute the program

11.9.2 References

Various paper tape software options are available for PDP-11 users. Refer to the following publication for program descriptions and operating instructions:

PDP-11 Paper Tape Software Programming Handbook (DEC-11-XPTSA-B-D).

The above manual can be ordered as directed at the rear of this manual.

	Address/Instruction	Mnemonic
Starting Address	001000/105737	TSTB @ #177564
	001002/177564	
	001004/100375	BPL. -4
	001006/110037	MOVB R0, @ #177566
	001010/177566	
	001012/005200	INC R0
	001014/000137	JMP @ #1000
	001016/001000	

```
                1000G !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRS
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←@ABCDEF
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←@ABCDEF
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←@ABCDEF
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←@ABCDEF
```

Figure 11-18 Sample Console Printout

11.9.3 Loading the Absolute Loader

The Absolute Loader program tape is loaded using the Bootstrap Loader which is resident in the processor's microcode. The Bootstrap Loader is executed via the Halt mode and console ODT commands as directed below:

1. Enter the Halt mode
   PDP-11/03 — Place the HALT/ENABLE switch in the HALT position. The console device prints the @ prompt character.

   LSI-11 — Since LSI-11 systems are completely user-configured, the HALT mode can be entered via one or more of the following means:

   a. Momentarily place the user-supplied HALT/ENABLE switch in the HALT position; return the switch to the ENABLE position.

   b. Press the BREAK key on the console device (FEH jumper must be installed in the console SLU interface module).

   c. Initialize the processor by momentarily negating BDCOK H (processor module jumper W5 must be installed and W6 removed).

2. Place the Absolute Loader tape (DEC-11-UABLB-A-PO) in the paper tape reader. Note that a long portion of the tape is punched with the octal value 351 (Channels 8, 7, 6, 4, and 1 are punched); position the tape so that any of those characters is located over the reader head.

3. Enable the tape reader as follows:

   LT33 Teletypewriter

   a. Enable the low-speed reader by placing the LINE/OFF/LOCAL switch in the LINE position.

   b. Place the START/STOP/FREE switch in the START position.

   High-Speed Reader — Turn the reader on and place "on line", as appropriate for the type of reader being used.

4. Enter the reader's CSR address by typing the value on the console device. For example, if the console device includes a paper tape reader (such as the LT33 low-speed reader), type:

   @177560

   NOTE

   In the above example, and all examples which follow, characters printed by ODT are shown underlined. Characters entered by the operator are shown not underlined.

   The value 177560 is the console device's CSR.

5. Load the Absolute Loader tape by typing L immediately after the reader device's CSR. The tape will automatically be read followed by printing the Absolute Loader's starting

address on a new line and the @ character on the following line. The complete command is shown below:

@ 177560L
037500
@

The starting address of the absolute loader depends upon the size of the system read/write memory (in any increments). Memory sizing is automatic and the Absolute loader will be properly located for the particular system in which it is loaded. The above example is for a system containing 8K memory.

A listing of typical printouts for 4K memory increments is provided below:

MEMORY SIZE	PRINTOUT
4K	017500 @
8K	037500 @
12K	057500 @
16K	077500 @
20K	117500 @
24K	137500 @
28K	157500 @

If a proper printout of the absolute loader's starting address is not obtained, repeat Step 5.

11.9.4 Loading Program Tapes

11.9.4.1 General — Program tapes are loaded into memory by the Absolute Loader program. The Absolute Loader can be used for normal loading and relocated loading operations. Normal loading causes the program being loaded to load at an absolute address punched in the program tape. Relocated loading allows loading certain program tapes into any specific area in memory, or to continue loading from where the loader left off on a previous load operation.

11.9.4.2 Normal Loading Procedure —

1. Place the program tape in the reader with blank (leader) tape over the read head.
2. Enable the tape reader as described in Paragraph 11.9.3, Step 3.
3. Read the program tape:
   a. If processor halted at Absolute Loader starting address (Paragraph 11.9.3, Step 5), type P (Proceed command).
   b. Load additional programs by typing the starting address of the loader program (previously printed out as described in Paragraph 11.9.3, Step 5), followed by the G command, as follows:

      @037500G

NOTE

1. **The above example is applicable for an 8K memory system. Use an appropriate starting address as printed out on the console device after loading the Absolute Loader.**
2. **Leading 0's can be ignored. For example, 037500 can be entered as: @ 37500G.**

After loading the program tape, the Absolute Loader program halts. The Halt PC+2 address is printed on a new line, followed by the @ character on the following line. The complete program loading sequence is shown below:

@ 177560L
037500
@ P
037712 First Prog. Tape Loaded

11.9.4.3 Relocated Loading Procedure — Relocated loading can be specified by setting the software switch register (in the Absolute Loader program) to a particular value. This value is normally 0, and normal program loading is selected by default. Note that the software switch register's address is dependent upon the Absolute Loader starting address, as previously printed. Use the first three octal digits of the starting address as the most significant three digits and 516 as the three least significant digits. Hence, 037516 is the software switch register location for the Absolute Loader when loaded in an 8K system.

To continue loading from a previous load operation, type:

@ 037516/000000 1 CR LF
@

NOTE

The above example is for an 8K memory system.

This type of relocated loading is particularly useful for large programs which are contained on more than one tape. To select relocated loading which uses an address (bias) contained in the software switch register, type:

```
@037516/000000 nnnnnn CR LF
@
```

NOTES

1. **The above example is for an 8K memory system.**
2. **Select a relocation value nnnnnn as specified in the *PDP-11 Paper Tape Software User's Handbook*. Observe that the least significant "n" value entered must be an odd number; this sets the software switch register bit 0 to a logical 1, selecting the relocated loading mode.**
3. **The program being loaded must be in a Position Independent Code (PIC) format to allow relocation.**

11.9.4.4 Self Starting Programs — Some programs are self starting (described in the Paper Tape Software Programming Handbook), and can automatically proceed execution immediately after loading. When this is desired, the processor Run mode must be enabled. Place the HALT/ENABLE (PDP-11/03 panel, or equivalent user-supplied LSI-11 system) switch in the ENABLE position. Load the program tape as previously described. Instead of the Absolute Loader program halting after loading the program tape, program control transfers to the loaded program's starting address, and the processor proceeds with normal program execution.

11.9.5 Program Starting and Execution

Once a program has been correctly loaded, the Run mode can be enabled and program execution started. Place the HALT/ENABLE switch (PDP-11/03 panel, or equivalent user-supplied LSI-11 switch) in the ENABLE position. Start normal program execution as follows:

```
@200G
```

The 200 in the above example is a typical starting address. Each program listing specifies the correct starting address. G is the Go command, and program execution will immediately commence, starting at the specified location.

Single instruction execution, when desired, is obtained by operating the processor in the Halt mode. Place the HALT/ENABLE switch in the HALT position. Enter the starting address (or a desired address for the first instruction to be executed) as described for normal program execution. The G command causes the processor to initialize the system and then Halt with the PC (R7) pointing to the first instruction. This address is printed on the console device as shown in the following example:

```
@ 200G CR LF
000200 CR LF
@
```

Successive instruction executions will occur each time the Proceed (P) command is entered via the console device.

An example of single word instruction execution using the P command is shown below:

```
@ 200G
000200
@ P
000202
@ P
000204
@ P
000206
@
```

Note that after executing each instruction, the processor halts and prints the address of the next instruction. Thus, Branch, Jump, and JSR instructions will alter the PC as required in normal program execution, allowing the operator time to observe program operation.

NOTE

Avoid single instruction execution of programs using interrupts. Those interrupts cannot be serviced by the processor when in the Halt mode because the Halt mode service has higher priority than device interrupts.

11.10 RT-11 SYSTEM OPERATION

11.10.1 General

RT-11 is an optional high-performance Operating System that combines PDP-11 hardware with user-oriented software. Two RT-11 Operating System monitors are provided: The Single Job monitor (RT-11 SJ) and Forward/Background monitor (RT-11 FB). Minimum hardware requirements include a console device, the RXV11 Floppy Disk, and 8K read/write memory.

RXV11 hardware includes the RX01 single or dual floppy disk drive, M7946 interface module, and BC05L-15 interface cable. Models are available for 115 V, 60 Hz and 230 V, 50 Hz operation.

RT-11 software is described in four publications:

RT-11 System Reference Manual (DEC-11-ORUGA-C-DN2)

RT-11 System Generation Manual (DEC-11-ORGMA-A-D)

RT-11 Software Support Manual (DEC-11-ORPGA-B-DN1)

RT-11 System Message Manual (DEC-11-ORMEA-A-D).

Refer to those documents for RT-11 system software operation. Manuals can be ordered as directed at the rear of this manual. The remainder of this discussion involves getting the PDP-11/03 or LSI-11 system running and responding to RT-11 Keyboard Monitor commands.

11.10.2 Using the RX01

The RX01 contains no operator controls or indicators other than the load door(s) on the front panel. The left drive on dual drive models is named DX0 and the right drive is DX1. Load the RT-11 diskette in the left (or only) drive: this drive (DX0) is called the SYStem device in RT-11 software.

NOTE

RT-11 can be bootstrapped and run on DX1 if DX0 is inoperative.

Additional details for the RX01 drive are included in the RX8/RX11 *Floppy Disk System Maintenance Manual* (EK-RX01-MM-PRE2). That manual covers hardware used with PDP8 and other PDP-11 systems. However, the RX11/RX01 interface is identical to the RXV11/RX01 interface, and the RX11 and RXV11 are software compatible.

11.10.3 RXV11 Bootstrap

11.10.3.1 General — The RXV11 bootstrap loader program loads the RT-11 monitor from disk into system memory. No RT-11 operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the REV11-A or REV11-C option, or it can be entered and executed via the console device.

11.10.3.2 Booting The System Using The REV11-A or REV11-C — The REV11-A or REV11-C implements the RXV11 bootstrap (and other bootstrap programs) in four pre-programmed ROM chips. When system power is applied, and LSI-11 processor Mode 2 power-up sequence is configured on the processor module, the system responds with a dollar sign ($) on a new line. The operator then responds by typing the device to be bootstrapped. DX (or DX0) is disk drive 0; DX1 is the second drive in dual drive RXV11 systems. A normal sequence of operations from power up through booting DX0 is shown below:

```
$DX
RT-11SJ   V02C-XX
.
```

After executing the DX0 bootstrap, the system responds by displaying the RT-11 monitor in use (RT-11SJ or RT-11FB) and the particular version in use (V02C-XX); the version is changed as RT-11 software changes are implemented. Finally, a dot is displayed on the next line, indicating that the RT-11 Keyboard Monitor is ready to accept a command. The system is correctly booted and RT-11 programs can be executed as desired.

11.10.3.3 Booting The System Via The Console Device — When the REV11-A or REV11-C option is not included in the system, the operator must enter a bootstrap program via the console device. Place the processor in the Halt mode and proceed as shown below; observe that underlined characters are printed by the processor and non-underlined characters are entered by the operator:

```
@1000/000000 12702 <LF>
001002/000000 1002n7 <LF>*
001004/000000 12701 <LF>
001006/000000 177170 <LF>
001010/000000 130211 <LF>
001012/000000 1776 <LF>
001014/000000 112703 <LF>
001016/000000 7 <LF>
001020/000000 10100 <LF>
001022/000000 10220 <LF>
001024/000000 402 <LF>
001026/000000 12710 <LF>
001030/000000 1 <LF>
001032/000000 6203 <LF>
001034/000000 103402 <LF>
001036/000000 112711 <LF>
001040/000000 111023 <LF>
001042/000000 30211 <LF>
001044/000000 1776 <LF>
001046/000000 100756 <LF>
001050/000000 103766 <LF>
001052/000000 105711 <LF>
001054/000000 100771 <LF>
001056/000000 5000 <LF>
001060/000000 22710 <LF>
001062/000000 240 <LF>
001064/000000 1347 <LF>
001066/000000 122702 <LF>
001070/000000 247 <LF>
001072/000000 5500 <LF>
001074/000000 5007 <CR>
```

*n=4 for Unit 0
n=6 for Unit 1
<LF>=Line Feed
<CR>=Carriage Return

The bootstrap program can be started at location 1000. Enable the Run mode by placing the HALT/ENABLE switch (on the PDP-11/03 panel, or an equivalent LSI-11 switch) in the ENABLE position. Start the program using the Go command as follows:

@1000G

After a few seconds the RT-11 monitor will be loaded in system memory. The monitor will identify itself on the console device by typing a message, such as: RT-11SJ V02X-XX. This printout is followed by the Keyboard Monitor prompt character (.) printed on the next line.

11.10.4 Using the RT-11

Requests for the desired RT-11 modules are always entered from the Keyboard Monitor. When executing a system program, control is normally returned to the Keyboard Monitor. The Keyboard Monitor can be entered at any time by simultaneously typing CTRL C keys.

CAUTION

1. **A temporary loss of power will abort RT-11 operation and the LSI-11 processor will power-up through the selected mode. RT-11 must be restarted. If the REV11-A or REV11-C option is used, the console device will display $ and the system waits for the operator to specify the desired bootstrap (DX). If the REV11-A or REV11-C is not used, enter the bootstrap program and start at location 1000.**
2. **Halting the processor will cause the processor to abort RT-11 operation. When the processor halts it prints the address (PC) on the console device, followed by the prompt character @ . RT-11 operation can continue by typing P. If desired, the system can be rebooted as previously described.**

CHAPTER 12
PERIPHERALS

This chapter contains a brief listing of peripherals available for use in PDP-11/03 and LSI-11 I/O applications. All peripherals listed are serial line devices which interface via the DLV11 Serial Line Unit interface module. Refer to Table 12-1 for peripheral types, models, brief specifications, and required interface options (DLV11 and either the BC05M 20 mA current loop interface cable or the BC05C EIA interface cable). Contact your local Digital Equipment Corporation Sales Office for detailed information on any of the peripherals listed.

Typical applications are shown in Figures 12-1 through 12-3. Note that peripherals listed other than the RT01 can be used as the console device. The RT01 is not capable of use as the console device. Although the RT02-A is not capable of full console operation, it can be used as the console device, but it is limited to the following ODT commands:

ODT Command	RT02-A Keys
CR	SEND
LF	SHIFT and CLEAR
/	SHIFT and ÷
@	SHIFT and @
G	SHIFT and GO
RO	SHIFT and ERROR

The console device can either be directly interfaced to the DLV11 or it can be operated in a remote location and interfaced via data sets or acoustic couplers and telephone lines. However, only the LA36, LT33, and VT50 are capable of remotely placing the LSI-11 system in the Halt state by asserting a line break (continuous "space" transmission). (This feature is jumper-enabled on the DLV11 through the use of framing error detection.)

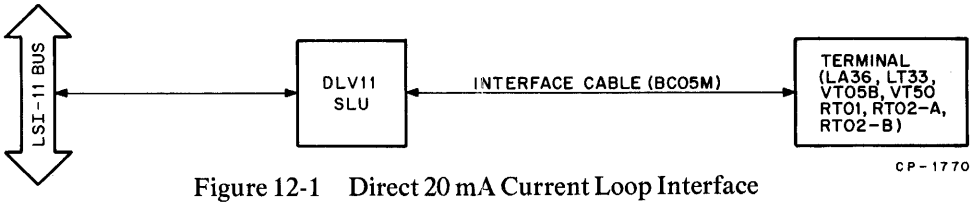


Figure 12-1 Direct 20 mA Current Loop Interface

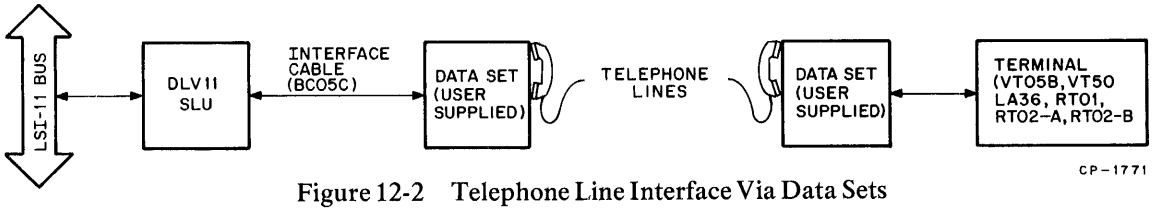


Figure 12-2 Telephone Line Interface Via Data Sets

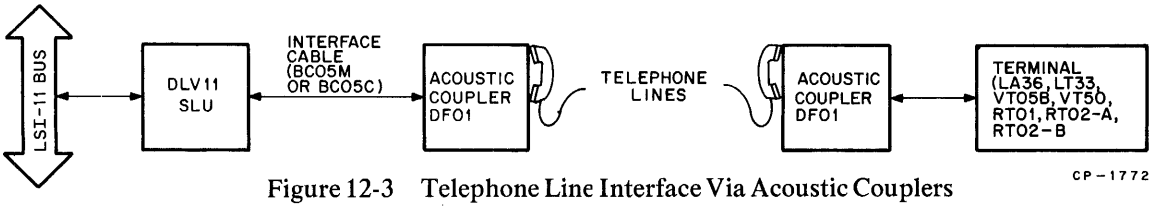


Figure 12-3 Telephone Line Interface Via Acoustic Couplers

Table 12-1
LSI-11 Peripheral Options

Terminal Type	Model	Name	Use as Console Device	Display Capacity	I/O Speed (baud rate)	BREAK Key	Serial Interface Type	Required Interface Options
Keyboard/Printer	LA36	DECwriter II	Yes	132 characters/line	300	Yes	20 mA loop optional EIA	DLV11, BC05M DLV11, BC05C
Keyboard/Printer and Paper Tape Reader/Punch	LT33	Teletypewriter	Yes	72 characters/line	110	Yes	20 mA loop	DLV11, BC05M
Keyboard/CRT Display	VT05B	Alphanumeric Terminal	Yes	1440 characters (72 char. X 20 lines)	110—2400	No	20 mA loop or EIA	DLV11, BC05M DLV11, BC05C
Keyboard/CRT Display	VT50	DECscope	Yes	960 characters (80 char. X 12 lines)	75—9600 75—9600	Yes	20 mA loop or optional EIA	DLV11, BC05M DLV11, BC05C
Data Entry Terminal (Decimal 0—9 display plus four status indicators)	RT01	DEC-LINK	No	4, 8, or 12 characters (optional)	110 or 300	No	20 mA loop or EIA	DLV11, BC05M DLV11, BC05C
Alphanumeric Data Entry Terminal	RT02-A	30 Character Keyboard Remote Terminal	Yes, with limited Command Set	32 characters	110—300 (20 mA) 110—1200 (EIA)	No	20 mA loop or EIA	DLV11, BC05M DLV11, BC05C
Full Alphanumeric Data Entry Terminal	RT02-B	Alphanumeric Terminal	Yes	32 characters	110—300 (20 mA) 110—1200 (EIA)	No	20 mA loop or EIA	DLV11, BC05M DLV11, BC05C
Acoustic Coupler (To be used with one of the above terminals)	DF01-A	Acoustic Telephone Coupler	All I/O characteristics of the terminal are retained.		110—300	—	20 mA loop or EIA	DLV11, BC05M DLV11, BC05C

APPENDIX A
MEMORY MAP

RESERVED VECTOR LOCATIONS

000 (RESERVED)
004 TIME OUT & OTHER ERRORS
010 ILLEGAL & RESERVED INSTRUCTION
014 BPT INSTRUCTION AND T BIT
020 IOT INSTRUCTION
024 POWER FAIL
030 EMT INSTRUCTION
034 TRAP INSTRUCTION
060 CONSOLE INPUT DEVICE
064 CONSOLE OUTPUT DEVICE
100 EXTERNAL EVENT LINE INTERRUPT
244 FIS (OPTIONAL)
264 RXV11

RESERVED DEVICE ADDRESSES

165000
↕ REV11 ROM ADDRESSES
165777

173000
↕ REV11 ROM ADDRESSES
173777

177170 RXV11 (RXCS)
177172 RXV11 (RXDB)

177550 (PRS)
177552 (PRB)
177554 (PPS)
177556 (PPB)
} HIGH-SPEED PAPER TAPE READER/PUNCH

177560 (RCSR)
177562 (RBUF)
177564 (XCSR)
177566 (XBUF)
} CONSOLE DEVICE REGISTERS

APPENDIX B
LSI-11 BUS PIN ASSIGNMENTS

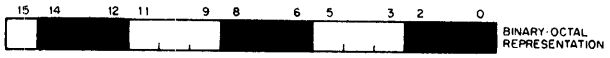
Row A (Same as Row C)		Row B (Same as Row D)	
Module Side 1 (Component Side)			
AA1	BSPARE1	BA1	BDCOK H
AB1	BSPARE2	BB1	BPOK H
AC1	BSPARE3	BC1	SSPARE4
AD1	BSPARE4	BD1	SSPARE5
AE1	SSPARE1	BE1	SSPARE6
AF1	SSPARE2	BF1	SSPARE7
AH1	SSPARE3	BH1	SSPARE8
AJ1	GND	BJ1	GND
AK1	MSPARE A	BK1	MSPARE B
AL1	MSPARE A	BL1	MSPARE B
AM1	GND	BM1	GND
AN1	BDMR L	BN1	BSACK L
AP1	BHALT L	BP1	BSPARE6
AR1	BREF L	BR1	BEVNT L
AS1	PSPARE3	BS1	PSPARE4
AT1	GND	BT1	GND
AU1	PSPARE1	BU1	PSPARE2
AV1	+5B	BV1	+5B
Module Side 2 (Solder Side)			
AA2	+5	BA2	+5
AB2	-12	BB2	-12
AC2	GND	BC2	GND
AD2	+12	BD2	+12
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	BWTBT L	BK2	BDAL6 L
AL2	BIRQ L	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDAL0 L	BU2	BDAL14 L
AV2	BDAL1 L	BV2	BDAL15 L

APPENDIX C
7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	\
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	054	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	056	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	] or ↑	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	— or ←	177	DEL

APPENDIX D
SUMMARY OF LSI-11 INSTRUCTIONS

WORD FORMAT



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) +(1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	−(R)	(R) − (1 or 2); is adrs
5	auto-decr deferred	@−(R)	(R) − 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING Reg = 7

2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND

Op Codes

■	= 0 for word/1 for byte
SS	= source field (6 bits)
DD	= destination field (6 bits)
R	= gen register (3 bits), 0 to 7
XXX	= offset (8 bits), +127 to −128
N	= number (3 bits)
NN	= number (6 bits)

Operations

( )	= contents of
s	= contents of source
d	= contents of destination
r	= contents of register
←	= becomes
X	= relative address
%	= register definition

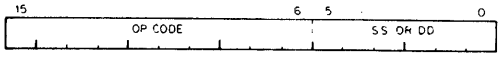
Boolean

∧	= AND
∨	= inclusive OR
⊻	= exclusive OR
∽	= NOT

Condition Codes

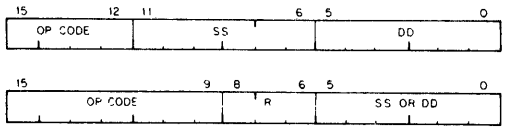
*	= conditionally set/cleared
—	= not affected
0	= cleared
1	= set

SINGLE OPERAND: OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■ 050DD	clear	0	0	1	0	0
COM(B)	■ 051DD	complement (1's)	∽ d	*	*	0	1
INC(B)	■ 052DD	increment	d + 1	*	*	*	–
DEC(B)	■ 053DD	decrement	d − 1	*	*	*	–
NEG(B)	■ 054DD	negate (2's compl)	−d	*	*	*	*
TST(B)	■ 057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■ 060DD	rotate right	→ C, d	*	*	*	*
ROL(B)	■ 061DD	rotate left	C, d ←	*	*	*	*
ASR(B)	■ 062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■ 063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	0	0
Multiple Precision							
ADC(B)	■ 055DD	add carry	d + C	*	*	*	*
SBC(B)	■ 056DD	subtract carry	d − C	*	*	*	*
SXT	0067DD	sign extend	0 or −1	–	*	0	–
Processor Status (PS) Operators							
MFPS	1067DD	move byte from PS	d ← PS	*	*	0	–
MTPS	1064SS	move byte to PS	PS ← s	*	*	*	*

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst



Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■ 1SSDD	move	d ← s	*	*	0	–
CMP(B)	■ 2SSDD	compare	s − d	*	*	*	*
ADD	06SSDD	add	d ← s + d	*	*	*	*
SUB	16SSDD	subtract	d ← d − s	*	*	*	*
Logical							
BIT(B)	■ 3SSDD	bit test (AND)	s ∧ d	*	*	0	–
BIC(B)	■ 4SSDD	bit clear	d ← (∽s) ∧ d	*	*	0	–
BIS(B)	■ 5SSDD	bit set (OR)	d ← s ∨ d	*	*	0	–
XOR	074RDD	exclusive OR	d ← r ⊻ d	*	*	0	–

Optional EIS

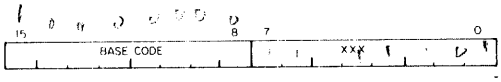
MUL	070RSS	multiply	r ← r x s	*	*	0	*
DIV	071RSS	divide	r ← r/s	*	*	*	*
ASH	072RSS	shift arithmetically		*	*	*	*
ASHC	073RSS	arith shift combined		*	*	*	*

Optional FIS

FADD	07500R	floating add	*	*	0	0
FSUB	07501R	floating subtract	*	*	0	0
FMUL	07502R	floating multiply	*	*	0	0
FDIV	07503R	floating divide	*	*	0	0

BRANCH: B - - location

If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)
adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	≠ 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	−	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1
Signed Conditional Branches				
BGE	002000	br if greater or equal (to 0)	≥0	N ⊻ V = 0
BLT	002400	br if less than (0)	<0	N ⊻ V = 1
BGT	003000	br if greater than (0)	>0	Z v (N ⊻ V) = 0
BLE	003400	br if less or equal (to 0)	≤0	Z v (N ⊻ V) = 1
Unsigned Conditional Branches				
BHI	101000	branch if higher	>	C v Z = 0
BLOS	101400	branch if lower or same	≤	C v Z = 1
BHIS	103000	branch if higher or same	≥	C = 0
BLO	103400	branch if lower	<	C = 1

JUMP & SUBROUTINE

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
MARK	0064NN	mark	aid in subr return
SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) − 1, then if (R) ≠ 0: PC ← Updated PC − (2 x NN)

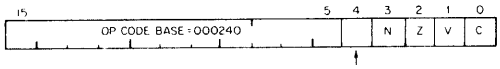
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)

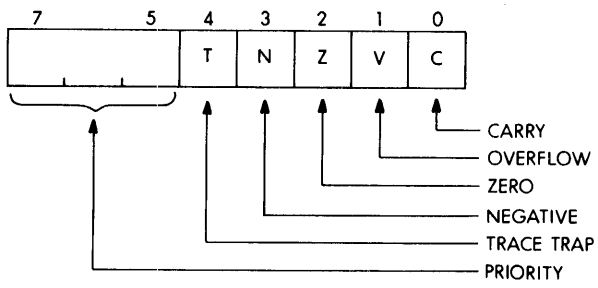
CONDITION CODE OPERATORS:



0 = CLEAR SELECTED COND. CODE BITS
1 = 'SET' SELECTED COND. CODE BITS

Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	–	–	–	0
CLV	000242	clear V	–	–	0	–
CLZ	000244	clear Z	–	0	–	–
CLN	000250	clear N	0	–	–	–
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	–	–	–	1
SEV	000262	set V	–	–	1	–
SEZ	000264	set Z	–	1	–	–
SEN	000270	set N	1	–	–	–
SCC	000277	set all cc bits	1	1	1	1

PROCESSOR STATUS WORD



POWERS OF 2

n	2^n	n	2^n
0	1	10	1,024
1	2	11	2,048
2	4	12	4,096
3	8	13	8,192
4	16	14	16,384
5	32	15	32,768
6	64	16	65,536
7	128	17	131,072
8	256	18	262,144
9	512	19	524,288

ABSOLUTE LOADER

Starting Address: — 500
Memory Size:

4K	017
8K	037
12K	057
16K	077
20K	117
24K	137
28K	157

BOOTSTRAP LOADER

Address	Contents	Address	Contents
— 744	016 701	— 764	000 002
— 746	000 026	— 766	— 400
— 750	012 702	— 770	005 267
— 752	000 352	— 772	177 756
— 754	005 211	— 774	000 765
— 756	105 711	— 776	177 560 (TTY)
— 760	100 376		
— 762	116 162		

NUMERICAL OP CODE LIST

OP Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07 – 00 00 77	(unused)
00 01 DD	JMP
00 02 0R	RTS
00 02 10 – 00 02 27	(reserved)
00 02 40	NOP
00 02 41 – 00 02 77	cond codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 67 DD	SXT
00 70 00 – 00 77 77	(unused)
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40 – 07 67 77	(unused)
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC, BHIS
10 34 XXX	BCS, BLO
10 40 00 – 10 43 77	EMT
10 44 00 – 10 47 77	TRAP
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 SS	MTPS
10 67 DD	MFPS
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB

TRAP VECTORS

000	(reserved)
004	Time Out & other errors
010	illegal & reserved instr
014	BPT instruction
020	IOT instruction
024	Power Fail
030	EMT instruction
034	TRAP instruction
244	FIS (optional)

ODT COMMANDS

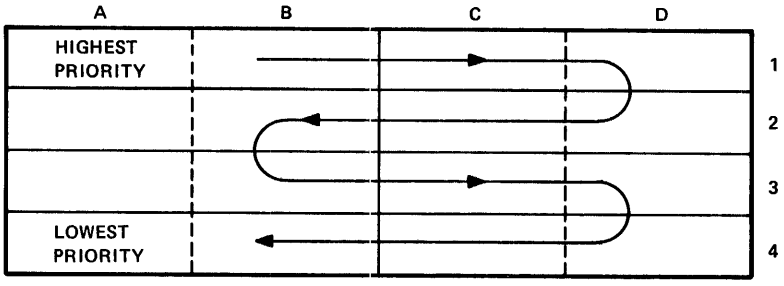
Format	Description
RETURN	Close opened location and accept next command.
LINE FEED	Close current location; open next sequential location.
↑	Open previous location.
←	Take contents of opened location, index by contents of PC, and open that location.
@	Take contents of opened location as absolute address and open that location.
r/	Open the word at location r.
/	Reopen the last location.
$n/or Rn/	Open general register n (0-7) or S (PS register).
r;G or rG	Go to location r and start program.
nL	Execute bootstrap loader using n as device CSR. Console device address is 177560.
;P or P	Proceed with program execution.
RUBOUT	Erases previous numeric character. Response is a backslash (\).

7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	`
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	054	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	_	177	DEL

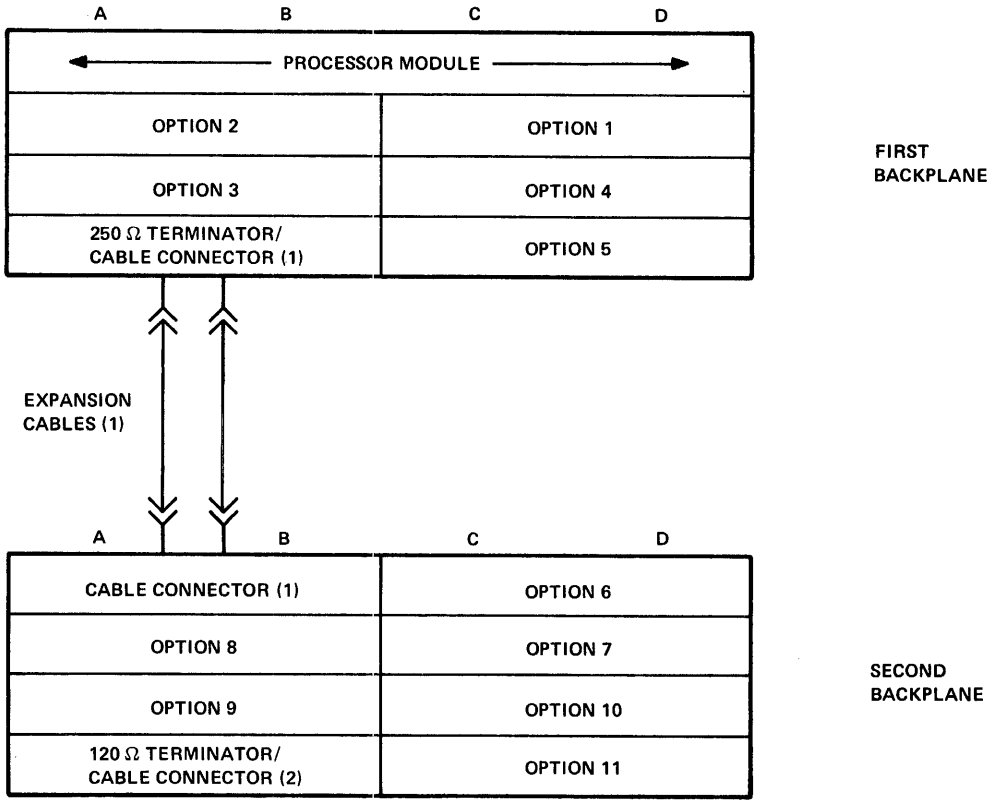
APPENDIX E
H9270 BACKPLANE CONFIGURATIONS

E.1 BASIC DAISY CHAIN GRANT PRIORITY



Note:
Arrow indicates BDMG and BIAK daisy chain signal routing from highest priority device slot to lowest priority device slot on the backplane.

E.2 TWO BACKPLANE CONFIGURATION

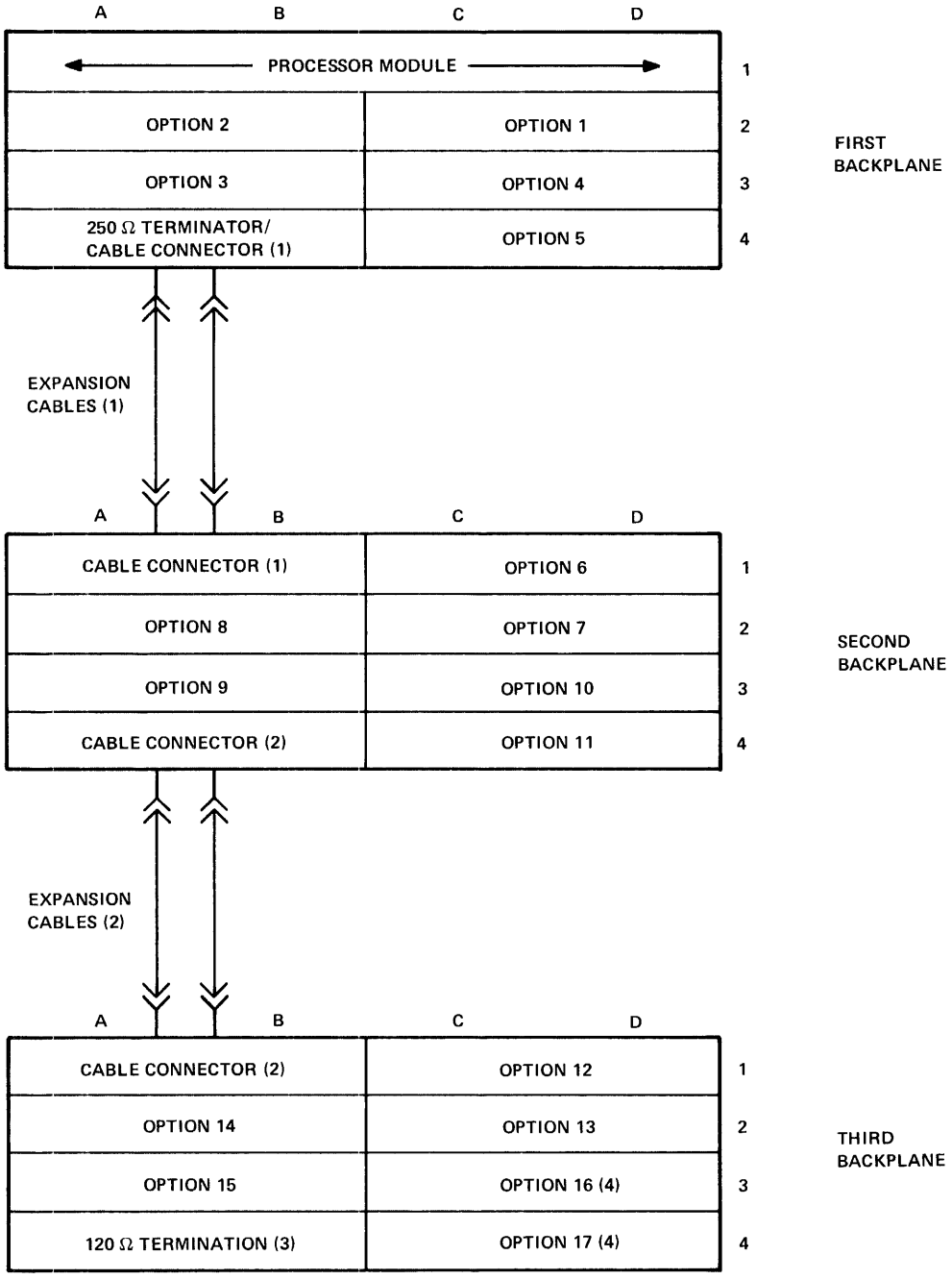


Notes:
1. Included in BCV1B bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)

2. Included in TEV11 bus terminator option.

CP-2047

E.3 THREE BACKPLANE CONFIGURATION



Notes:

1. Included in BCV1B bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)

2. Included in BCV1A bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)

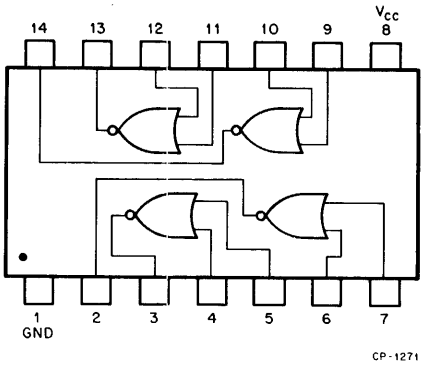
3. Included in TEV11 bus terminator option.

4. The LSI11 Bus is restricted to 15 options, maximum. These option slots would only be used when previous option(s) occupy more than 1 option location.

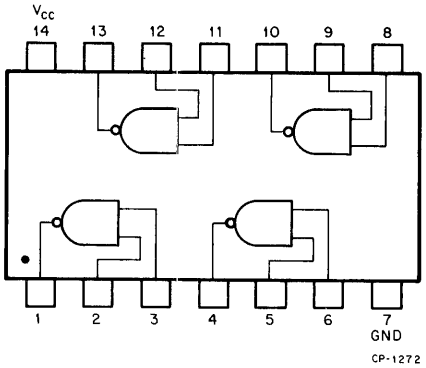
CP-2048

APPENDIX F
BUS INTERFACE I.C. PINS

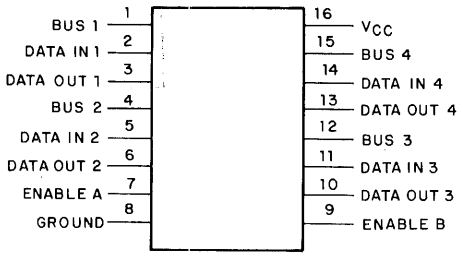
F.1 DEC 8640 QUAD 2 - INPUT NOR GATES
(Bus Receiver)

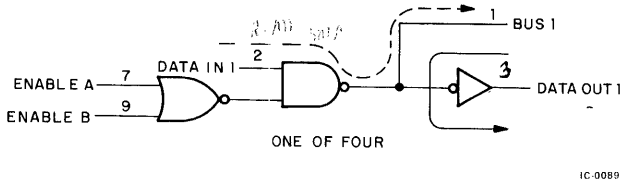


F.2 DEC 8881 QUAD 2 - INPUT NAND GATE
(Bus Driver)



F.3 DEC 8641 QUAD UNIFIED BUS TRANSCEIVER
(Bus Receiver/Driver)





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LSI-11, PDP-11/03 User's Manual
Changes and Additions
November 1975

This change package will update your manual (EK-LSI11-TM-001) to the revision (EK-LSI11-TM-002). Carefully revise the manual as described below.

Correct the indicated text as directed.

Correct your copy of the manual as directed below. Text to be changed is shown underlined:

Page	Text as Printed	Change to
1-1, Paragraph 1.1, last line:	Microprocessor	Processor
3-1, second paragraph, line 7:	CSR	control/status register (CSR)
3-1, paragraph 3.2, 3. *Service Requirements,* last line:	typing	tying
3-4, **CAUTION,** line 1:	should	must
3-10, Figure title:	DATIOB	DATOB
4-5, last paragraph, line 4:	REPLAY	REPLY
4-7, paragraph 4.2.2.6, second paragraph, line 5:	PH3 H	PH2 H
4-7, paragraph 4.2.2.6, third paragraph, line 3:	5	15

Page	Text as Printed	Change to
4-14, paragraph 4.2.4, lines 6 and 7:		
	delete: zener-regulated to -5V and -9V. The -9V output is	
6-7, XCSR, Bit 07, last line:		
	Read/write bit.	Read-only bit.
9-3, paragraph 9.2.3, second paragraph, line 4:		
	no	all
9-3, paragraph 9.2.3, second paragraph, line 5:		
	Jumpers not installed represent logical 0s; jumpers in-	Jumpers installed represent logical 0s; jumpers not in-
9-4, Table 9-2, 512 by 4 chips Word/Byte address, line 5:		
	10000–1777	10000–11777
B-1, pin BV1		
	+5B	+5
D-4, 7-BIT ASCII CODE:		
	delete this table (refer to revised Appendix C)	

CONFIGURING

LSI-11 PROCESSOR MODULE JUMPERS

(SUPPLEMENT TO THE LSI-11, PDP-11/03 USER'S MANUAL)

JULY 1976

DIGITAL EQUIPMENT CORPORATION
COMPONENTS GROUP HEADQUARTERS
ONE IRON WAY
MARLBOROUGH, MA., 01752

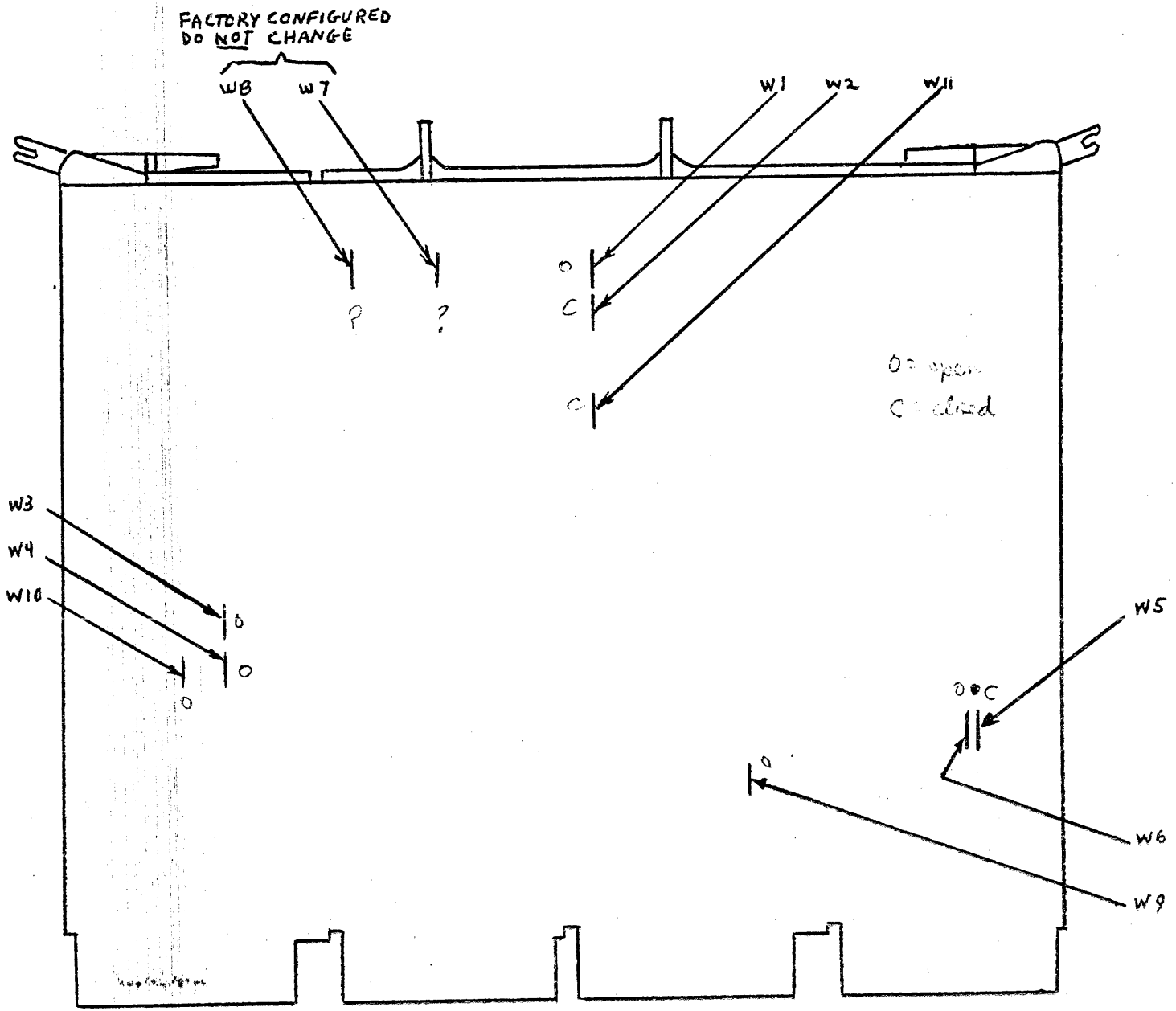

FIGURE 1 KD11-F and KD11-J JUMPER LOCATIONS

CONFIGURING LSI-11 PROCESSOR MODULE JUMPERS

GENERAL - The processor module contains 11 wire wrap posts which allow the user to configure the module for a specific system application. KD11-F and KD11-J processor modules are factory configured as shown in Table 1. Jumpers can be user-configured as described in the following paragraphs. Jumpers are located on the processor module as shown in Figure 1.

Table 1

KD11-F and KD11-J Factory-Installed Jumpers

	KD11-F (M7264)		KD11-J (M7264-YA)	
Jumper	Status	Function	Status	Function
W1	R	Resident memory bank 1 not selected	R	Resident memory bank 1 not selected
W2	I	Resident memory bank 0 selected	R	Resident memory bank 0 not selected
W3	R	Event line (LTC) interrupt enabled	R	Event line (LTC) interrupt enabled
W4	R	Processor-controlled memory refresh enabled	I	Processor controlled memory refresh disabled
W5	R	Power-up mode 0 selected	R	Power-up mode 0 selected
W6	R		R	
W7	-	Factory-configured bias voltage (do not change)	-	Factory-configured bias voltage (do not change)
W8	-		-	
W9	R	Enable reply from resident memory	I	Disable reply from resident memory
W10	R	Disable reply from resident memory during refresh	R	Disable reply from resident memory during refresh
W11	I	Enable on-board memory select	R	Disable on-board memory select

NOTE I= Installed
R= Removed

MEMORY REFRESH

The LSI-11 processor has the capability of completely controlling the refreshing of all dynamic MOS memories in a system when jumper W4 is removed. Memory refresh is always required when dynamic MOS memory devices are used in the LSI-11 system, such as the KD11-F resident memory and the MSV11-B 4K by 16-bit read/write memory module. The refresh operation can be controlled by a device other than the LSI-11 processor, if available, such as the REV11-A and REV11-C options. If such a device is used, or if no dynamic MOS memory devices are present in the system (KD11-J), install W4. The refresh sequence is described below.

The processor's memory refresh sequence is controlled by resident microcode in the processor which is initiated by an interrupt that occurs once every 1.6 ms. It is the highest priority processor interrupt. Once the sequence is initiated, the processor will execute 64 BSYNC L/BDIN L bus transactions, while asserting BREF L. The BREF L signal overrides memory bank address bits 13-15 and allows all memory units to be simultaneously enabled. After each bus transaction, BDAL1-6L is incremented by 1 until all 64 rows have been refreshed by the BSYNC L/BDIN L transaction. This process takes approximately 130μs during which external interrupts (BIRQ L and BEVNT L) are ignored. However, DMA requests can be granted between each of the 64 refresh transactions.

LINE TIME CLOCK

LTC (or external event) interrupts are enabled when jumper W3 is removed and the processor is running. The jumper can be inserted to disable this feature. The LTC interrupt is initiated by an external device when it asserts the BEVNT L signal. This is the highest priority external interrupt request; processor interrupts have higher priorities. If external interrupts are enabled (PS bit 7 = 0), the processor PC (R7) and PS word are pushed onto the processor's stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector address input operation by the processor is not required since vector 100 is generated by the processor.

The first instruction of the service routine will typically be fetched within 16μs from the time BEVNT L is asserted; however, if optional EIS/FIS instructions are being executed, this time could extend to 50.45μs. This time could also be extended by processor trap execution (memory refresh, T-bit, power fail, etc.), or by asserting the BHALT L signal.

POWER-UP MODE SELECTION

Since the LSI-11 can be used in a variety of system applications that have either (or both) volatile (semiconductor read/write) or nonvolatile (PROM or core) memory, one of four power-up mode features are available for user selection. These are selected (or changed) by wire-wrap jumpers W5 and W6 on the KD11-F or KD11-J processor (M7264) module. Note that the jumpers affect only the power-up mode (after BDCOK H and BPOK have been asserted); they do not affect the power-down sequence.

Reader's Comments

LSI-11, PDP-11/03 User's Manual
EK-LSI11-TM-002

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

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