EK-KXJCA-IN-001

KXJ11-CA Single-Board Computer

Installation Guide

digital™

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KXJ11-CA Single-Board Computer

Installation Guide

Prepared by Educational Services
of Digital Equipment Corporation

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Chapter 1
Introduction

This guide describes how to install the KXJ11-CA module.

> **NOTE**
>
> Before changing the factory shipped jumper configuration, make sure the jumpers match the jumpers shown in Figure 2-1, and verify that the module is operating as described in Section 6.2.

Installation includes the following activities.

1. Selecting operating characteristics and installing appropriate jumpers (Chapter 2)
2. Determining power supply requirements (Chapter 3)
3. Installing the board into a backplane (Chapter 4)
4. Selecting and connecting cables from serial and parallel I/O interfaces to external devices (Chapter 5)
5. Verifying proper operation (Chapter 6)

Chapter 2
Selecting Operating Features

Several characteristics of the KXJ11-CA are defined by jumper settings. This section describes the characteristics that are part of the factory-shipped configuration. It also shows how to change these characteristics by changing the appropriate jumpers.

Figure 2-1 illustrates the factory-shipped jumper settings. Table 2-1 summarizes the meaning of each jumper setting. The sections that follow describe the various jumper setting alternatives available.

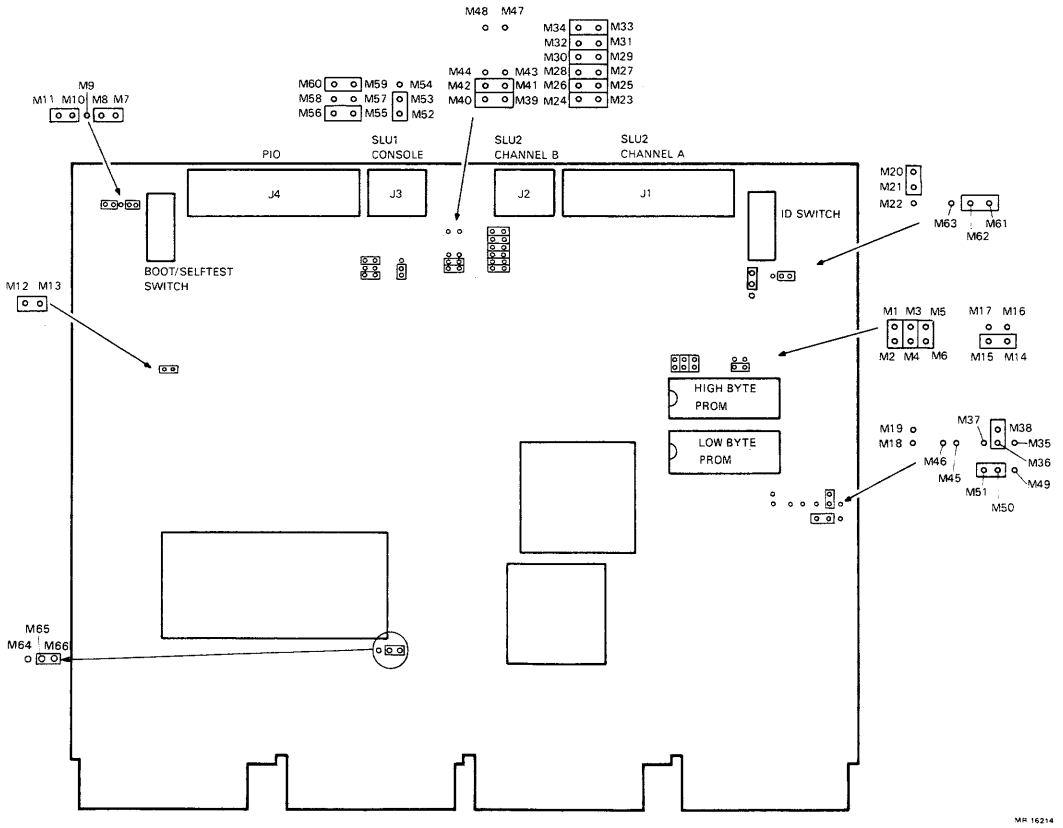


Figure 2-1 KXJ11-CA Jumper Layout

Table 2-1 Factory Shipped Jumper Configuration

Function	Setting	Jumpers Installed
Q-Bus Size	22 bits	M3 to M4 M5 to M6
Q-Bus Base Address	17760240	M1 to M2
ID Switch Position	5	
DMA Requests		
SLU2 Channel A Receiver	Enabled	M10 to M11
8036 Counter/Timer	Disabled	
SLU2 Channel A Transmitter	Enabled	M7 to M8
Locked Instruction Enable	Disabled	M65 to M66
BREAK Enable	Enabled	M12 to M13
HALT Option Selection	MicroODT	M14 to M15
Power-Up Option Selection	Firmware	No jumper
PROM Addressing	15-bit	No jumper
SLU1 Baud Rate	9600	M56 to M55 M60 to M59
SLU1 Transmitter	RS423	M62 to M61
SLU1 Receiver	RS423	No jumper
SLU2 Channel A Receiver	RS422	M34 to M33 M32 to M31 M30 to M29 M28 to M27 M26 to M25 M24 to M23
SLU2 Channel B Transmitter	RS422	M38 to M36 M51 to M50
SLU2 Channel B Receiver	RS422	M42 to M41 M40 to M39 M20 to M21
Real-Time Clock Interrupt	60 Hz	M52 to M53
Boot/Self-Test Switch Position	5	

NOTE

The SLU2 Channel A Transmitter is not configured with jumpers, but is configured by selecting appropriate signals on connector J1.

2.1 Boot/Self-Test Switch

The boot/self-test switch is a 16-position switch that is used if the board is configured to execute firmware (rather than MicroODT) upon power-up. It has three functions.

1. It determines how the KXJ11-CA will act when a special interrupt condition exists, including whether or not self-tests will run (see Section 3.5, *The KXJ11-CA Single-Board Computer User's Guide*, EK-KDJCA-UG-001).
2. It determines whether special interrupt handling is performed either by user code or by firmware.
3. It determines where in memory the on-board PROM is mapped. There are two alternatives — low memory or high memory. The memory maps associated with low and high PROM mapping are shown in Figures 2-2 and 2-3, respectively.

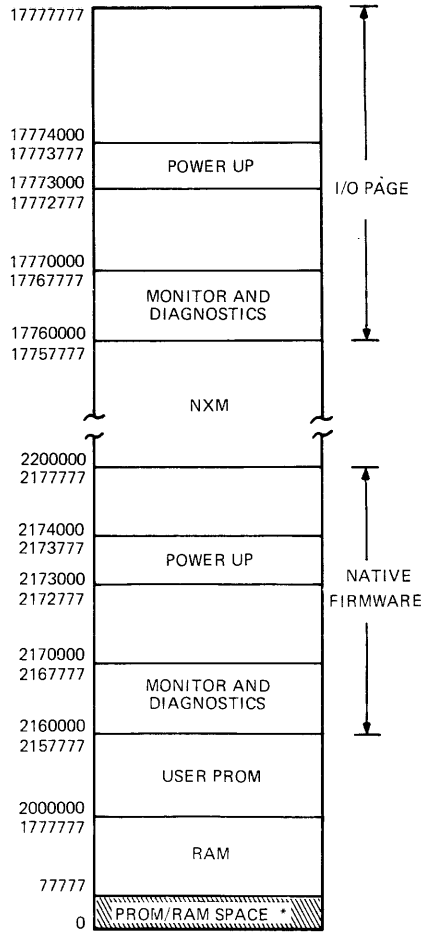


Figure 2-2 Memory Mapping — PROM in Low Memory

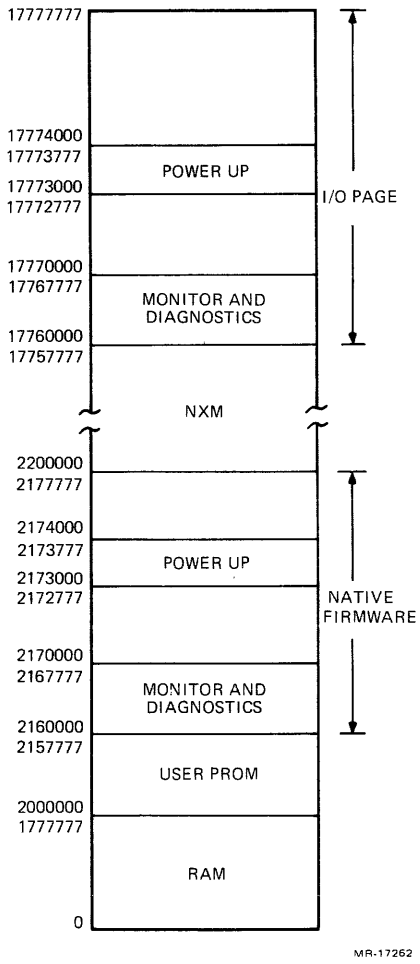


Figure 2-3 Memory Mapping — PROM in High Memory

The location of the boot/self-test switch is shown in Figure 2-4. Table 2-2 summarizes the functions associated with each switch position.

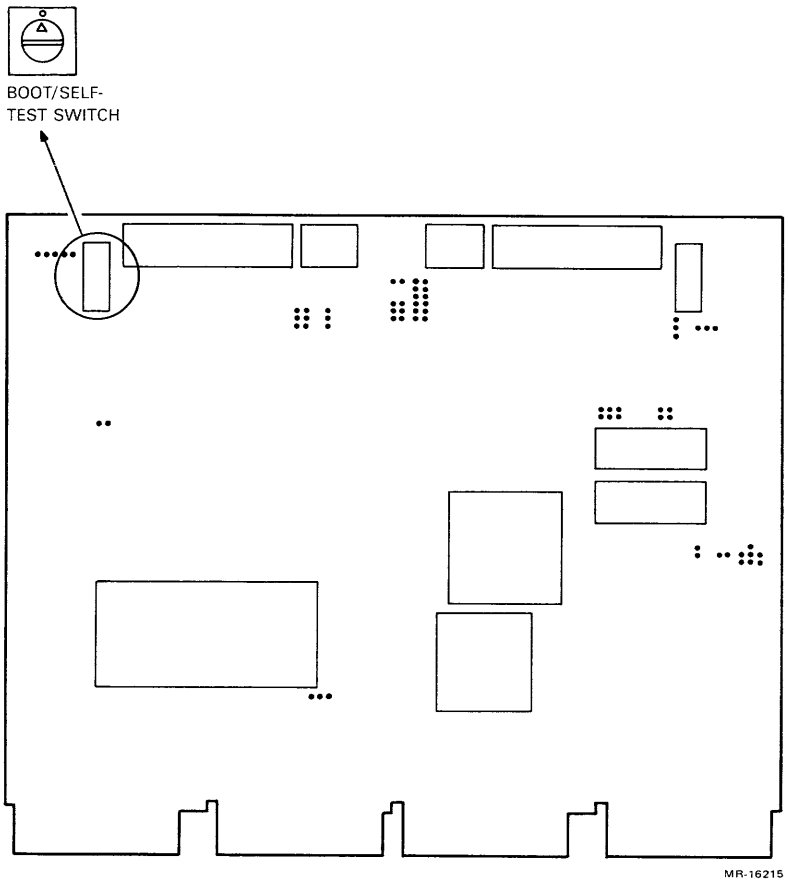


Figure 2-4 Boot/Self-Test Switch

Table 2-2 Boot/Self-Test Switch Functions

Switch Position	KXJ11-CA Special Interrupt Response	Special Interrupt Handling	PROM Mapping
0	User PROM application code is executed. No self-tests are performed.	Firmware	Low
1	User PROM application code is executed. Auto self-tests are performed.	Firmware	Low

Table 2-2 Boot/Self-Test Switch Functions (Cont)

Switch Position	KXJ11-CA Special Interrupt Response	Special Interrupt Handling	PROM Mapping
2	User PROM application code is executed. Auto self-tests are performed. The user (P)ROM checksum test is also performed.	Firmware	Low
3	Application code is booted from a TU58 via SLU1. Auto self-tests are performed, then the TU58 primary bootstrap is executed.	Firmware	High
4	MicroODT is entered. No self-tests are performed.	Firmware	High
5	Auto self-tests are performed. The KXJ11-CA awaits command from the arbiter via TPR0.	Firmware	High
6	No self-tests are performed. The KXJ11-CA awaits a command from the arbiter via TPR0.	Firmware	High
7	Auto self-tests are performed continuously. No application code is booted or executed. Loopback connectors (see Section 5.3) are installed for these tests.	None	High
8	User PROM application code is executed. No self-tests are performed.	User Code	Low
9	User PROM application code is executed. Auto self-tests are performed.	User Code	Low
10	User PROM application code is executed. Auto self-tests are performed. The user (P)ROM checksum test is also performed.	User Code	Low
11	Application code is booted from a TU58 via SLU1. Auto self-tests are performed, then the TU58 primary bootstrap is executed.	User Code	High
12	MicroODT is entered. No self-tests are performed	User Code	High

Table 2-2 Boot/Self-Test Switch Functions (Cont)

Switch Position	KXJ11-CA Special Interrupt Response	Special Interrupt Handling	PROM Mapping
13	Auto self-tests are performed. The KXJ11-CA awaits a command from the arbiter via TPR0.	User Code	High
14	No self-tests are performed. The KXJ11-CA awaits a command from the arbiter via TPR0.	User Code	High
15	Auto self-tests are performed continuously. No application code is booted or executed. Loopback connectors (see Section 5.3) are installed for these tests.	None	High

NOTES

1. Switch position 5 is the factory-shipped configuration.
2. The encoded value of the boot/self-test switch position is available in the KXJCSRB register in bits <7:4>. For example, switch position 1 would be encoded as 0001 in KXJCSRB <7:4>.
3. The user (P)ROM checksum test looks for a checksum at the highest word address of user (P)ROM. Similarly, the firmware checksum test looks for a checksum at the highest word address of the firmware PROM. Either checksum is calculated and checked according to the following DECPROM algorithm:

   CHECKSUM = 0
   FOR I = number of PROM addresses to be checksumed
   DO CHECKSUM = CHECKSUM + contents of address
   (high order carry from addition is discarded)
   CHECKSUM = ROTATE_LEFT_ONE_BIT (bit0 → bit1, bit1 → bit2, ... ,bit15 → bit0) NEXT I

4. Special interrupt handling can be performed by user code in switch positions 8-15. This function is useful in applications that need to continue running after the Q-Bus signal BHALT or the Q-Bus signal BINIT has been asserted. For switch positions 0 through 7, special interrupt handling is done by firmware.
5. If the KXJ11-CA is in standalone mode, switch positions 5, 6, 13, and 14 should not be used. These positions cause the KXJ11-CA to idle and wait for a command. In standalone mode, the KXJ11-CA will idle indefinitely, waiting for an arbiter command that will never come.

2.2 Q-Bus Size

The KXJ11-CA may be configured to handle 16-, 18-, or 22-bit Q-Bus addressing. This is accomplished with the Q-Bus size jumpers (see Figure 2-5). 22-bit addressing is selected as part of the factory-shipped configuration.

Jumper Connection				Description
M3	o	o	M5	22-bit addressing selected*
M4	o	o	M6	
M3	o	o	M5	18-bit addressing selected
M4	o	o	M6	
M3	o	o	M5	16-bit addressing selected
M4	o	o	M6	

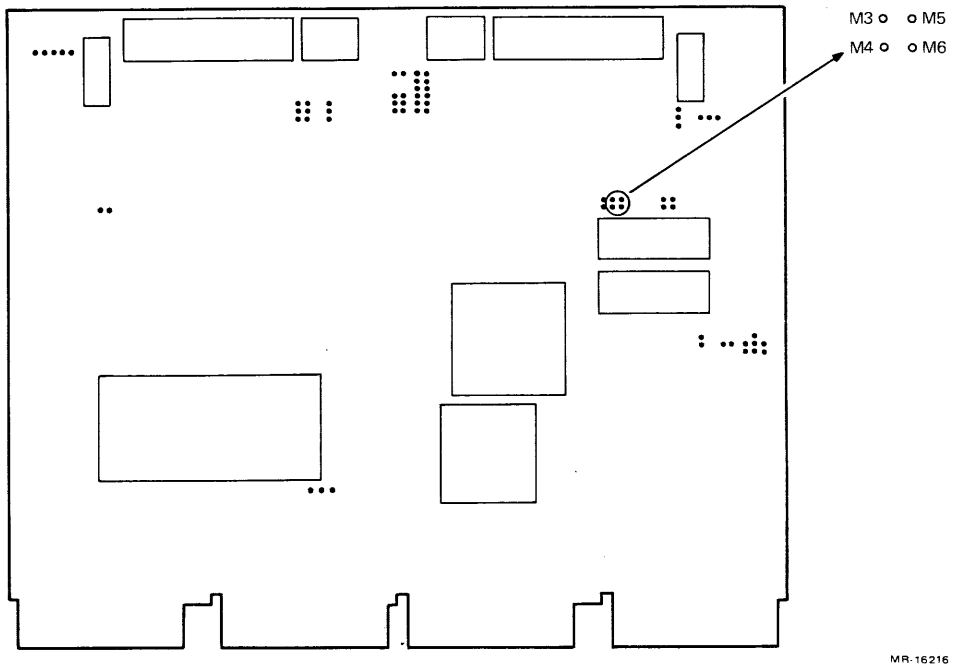


Figure 2-5 Q-Bus Size Selection

* Factory-shipped configuration

2.3 Q-Bus Base Address Selection

In systems with multiple I/O processor boards, make sure each board has a unique Q-Bus base address to distinguish the boards from one another. This is accomplished on the KXJ11-CA by setting the ID switch and installing or removing a jumper which connects M1 and M2.

Table 2-3 lists the base addresses that can be selected. Table 2-3 lists 22-bit addresses. If the KXJ11-CA is configured for 16- or 18-bit addressing, use the lower 16 or 18 bits of the addresses specified in Table 2-3.

Table 2-3 Q-Bus Base Address Selection

ID Switch Position	Base Address (Jumper IN)	Base Address (Jumper OUT)
0	*	*
1	*	*
2	17760100	17762100
3	17760140	17762140
4	17760200	17762200
5†	17760240†	17762240
6	17760300	17762300
7	17760340	17762340
8	17775400	17777400
9	17775440	17777440
10	17775500	17777500
11	17775540	17777540
12	17775600	17777600
13	17775640	17777640
14	17775700	17777700
15	17775740	17777740

* These switch positions disable the Q-Bus interface. That is, the KXJ11-CA is running in standalone mode.

† Factory-shipped configuration

Figure 2-6 shows the locations of jumper connections M1 and M2, and the ID switch. The factory-shipped base address is 17760240.

Jumper Connection		Description
o	M1	Factory-shipped configuration
o	M2	Base address = 17760240

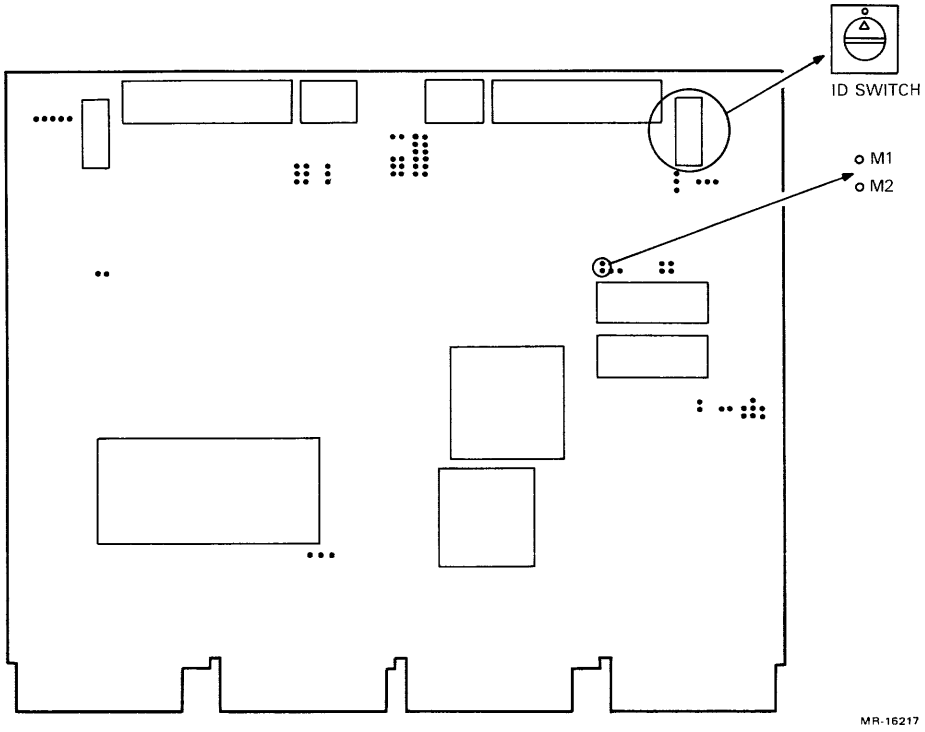


Figure 2-6 Q-Bus Base Address Selection

2.4 DMA Requests

DMA requests to the on-board DMA transfer controller (DTC) may come from several sources. The KXJ11-CA has a set of jumpers that enable or disable DMA requests from: (1) the SLU2 channel A receiver, (2) the SLU2 channel A transmitter, or (3) the on-board 8036 PIO counter/timer. The location of these jumpers is shown in Figure 2-7. Only two of the three sources may be specified (jumpered) at one time. The two sources that are jumpered as part of the factory configuration are SLU2 channel A receiver and SLU2 channel A transmitter.

Jumper Connection					Description
M11	M10	M9	M8	M7	Allows DMA channel 0 requests from SLU2
o——o		o	o	o	channel A receiver*
M11	M10	M9	M8	M7	Allows DMA channel 1 requests from PIO
o	o	o——o		o	counter/timer (pin C1 used as request line)
M11	M10	M9	M8	M7	Allows DMA channel 1 requests from SLU2
o	o	o	o——o		channel A transmitter*

NOTE

Do not connect a jumper between M10 and M9. This configuration is not supported.

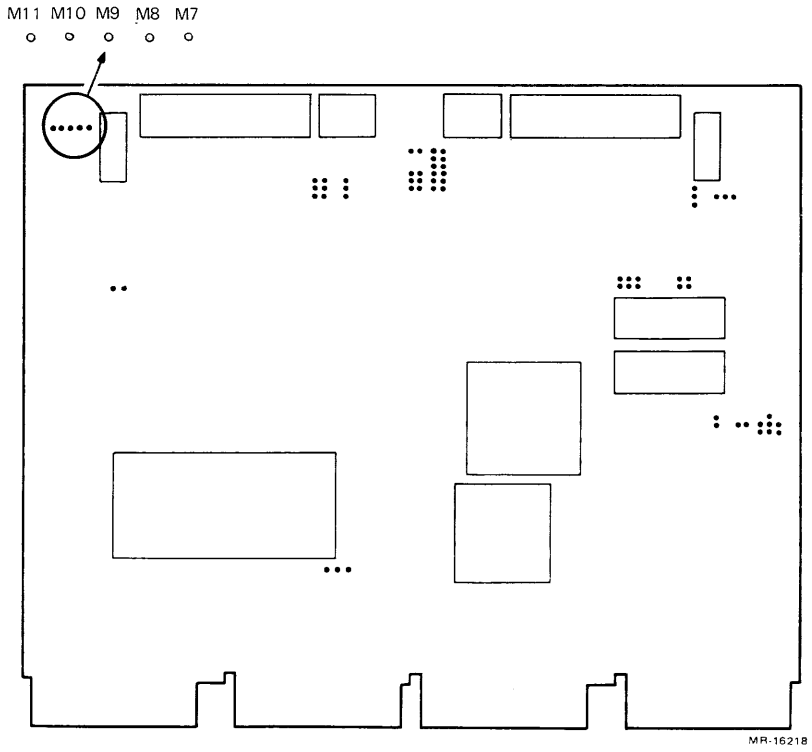


Figure 2-7 DMA Requests

* Factory-shipped configuration

2.5 Locked Instruction Enable

The KXJ11-CA has a set of jumpers that enable or disable the locking characteristic of the WRTLCK, TSTSET, and ASRB interlocked instructions. The location of the jumpers is shown in Figure 2-8. Locking is disabled as part of the factory-shipped configuration. For most applications, locking must be disabled. If locking is enabled, a Q-Bus timeout may cause a trap to location 4 if the Q-Bus is heavily loaded, and one of these instructions is executed.

Jumper Connection	Description
M64 M65 M66 o——o o	The locking characteristic of the WRTLCK, TSTSET, and ASRB instructions is enabled
M64 M65 M66 o o——o	The locking characteristic of the WRTLCK, TSTSET, and ASRB instructions is disabled*

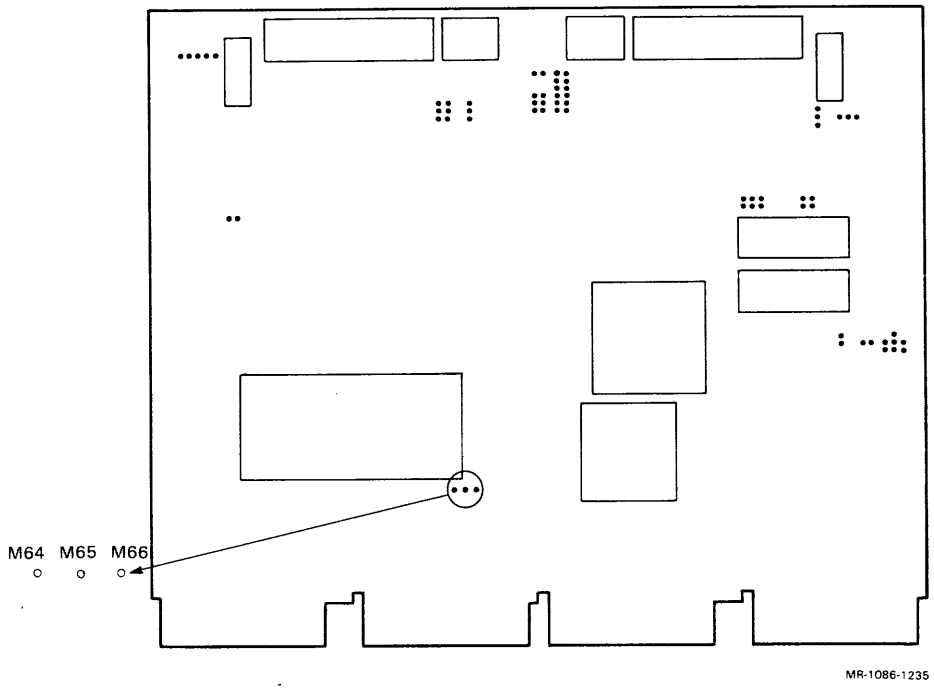


Figure 2-8 Locked Instruction Enable

* Factory-shipped configuration

2.6 BREAK Enable Selection

There is a jumper on the board that enables or disables console BREAK requests from SLU1 (the on-board DLART) to the J-11. The location of this jumper is shown in Figure 2-9. A BREAK is generated by SLU1 when a console terminal is attached to the system and the BREAK key on the console keyboard is pressed. When BREAK is received, the J-11 executes MicroODT. BREAK requests are enabled as part of the factory-shipped configuration.

Jumper Connection			Description
M13	o——o	M12	Console BREAK requests enabled*
M13	o o	M12	Console BREAK requests disabled

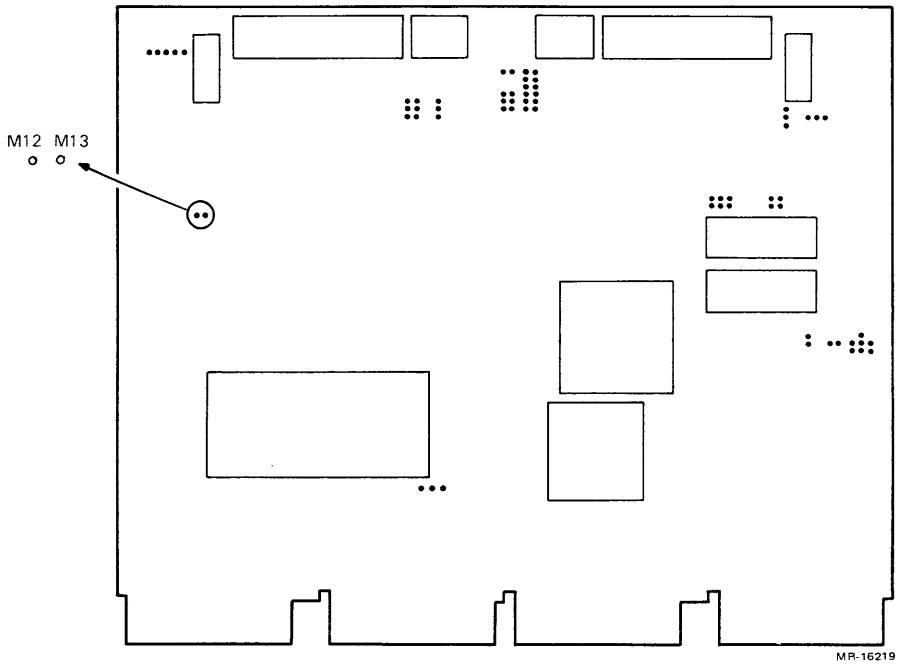


Figure 2-9 BREAK Enable

* Factory-shipped configuration

2.7 HALT Option Selection

A jumper on the KXJ11-CA determines what action will be taken if a HALT instruction is executed in kernel mode. The location of this jumper is shown in Figure 2-10. The jumper affects the state of bit 3 of the Maintenance Register (see Section 3.2.10, *The KXJ11-CA Single-Board Computer User's Guide*, EK-KXJCA-UG-001). If the jumper is installed (the factory-shipped configuration), a HALT instruction executed in kernel mode causes the processor to enter MicroODT. If the jumper is not installed, the KXJ11-CA traps to location 4 in kernel instruction space and sets bit 7 in the CPU error register.

Jumper Connection			Description
M15	o——o	M14	MicroODT is entered when a HALT instruction is executed in kernel mode*
M15	o o	M14	KXJ11-CA traps to location 4 in kernel instruction space and sets bit 3 of the CPU error register if a HALT instruction is executed in kernel mode

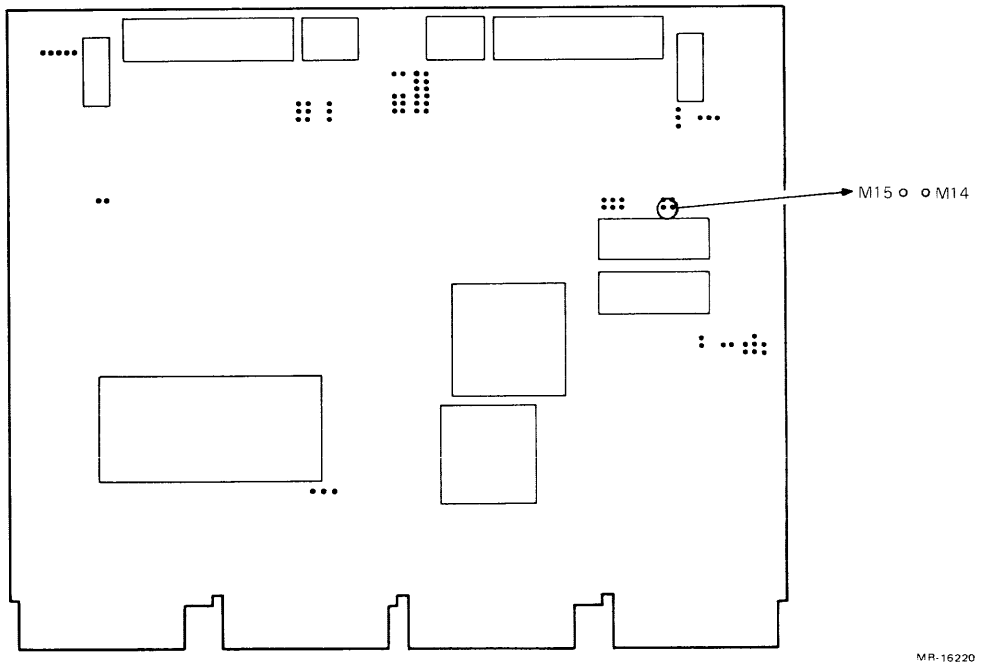


Figure 2-10 HALT Option Selection

* Factory-shipped configuration

2.8 Power-Up Option Selection

The power-up jumper (see Figure 2-11) determines what action the KXJ11-CA will take when the board is powered up or reset. The jumper affects the state of bit 2 of the Maintenance Register (see Section 3.2.10, *The KXJ11-CA Single-Board Computer User's Guide*, EK-KXJCA-UG-001). At power-up, if the jumper is installed, the processor enters MicroODT with the PS register cleared. This is also known as power-up option 1. If the jumper is not installed, (the factory-shipped configuration), the KXJ11-CA executes the firmware power-up code at location 173000 during power-up (PC = 173000, PS = 340). This is also known as power-up option 3. Only power-up options 1 and 3 are used for the KXJ11-CA.

Jumper Connection			Description
M17	o——o	M16	MicroODT is entered during power-up
M17	o o	M16	The KXJ11-CA bootstraps through location 173000 during power-up*

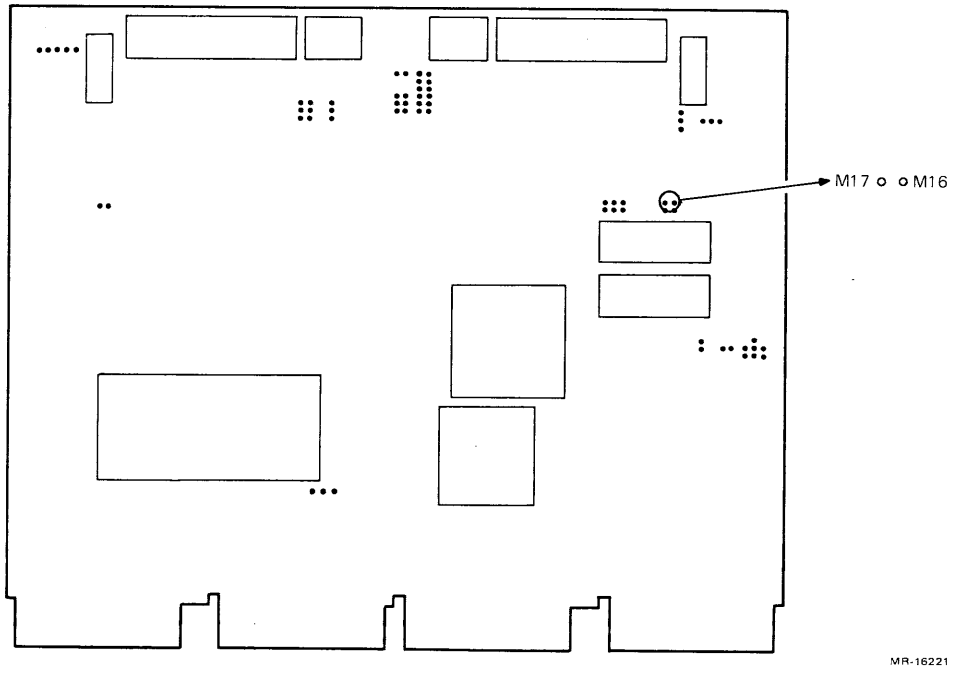


Figure 2-11 Power-Up Option Selection

2.9 PROM Addressing

The KXJ11-CA can be jumpered to accommodate various PROM types. The location of the PROM addressing jumper is shown in Figure 2-12. If the jumper is not installed, the on-board PROMs use 15-bit addresses. PROMs such as the Intel 2764 (8K × 8) and 27128 (16K × 8) use 15-bit addresses. If the jumper is installed, the PROMs use 16-bit addresses. This accommodates PROMs such as the Intel 27256 (32K × 8) that use 16-bit addresses. 15-bit PROM addressing is specified as part of the factory-shipped configuration.

Jumper Connection		Description
o	M19	15-bit addressing selected*
o	M18	
o	M19	16-bit addressing selected
o	M18	

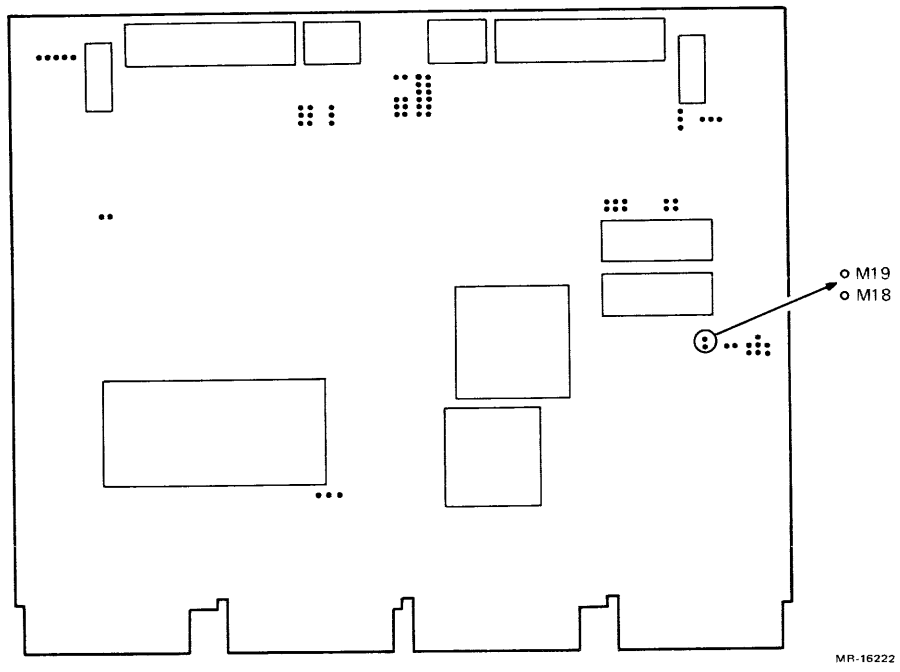


Figure 2-12 PROM Addressing

* Factory-shipped configuration

2.10 SLU1 Baud Rate

The jumpers shown in Figure 2-13 select the default baud rate for the SLU1 transmitter and receiver. The default baud rate for SLU1 is set when the KXJ11-CA is powered up or reinitialized. This rate can be changed under software control, if KXJCSRJ<3> is set. Table 2-4 shows the various baud rates that can be selected. A default baud rate of 9600 is specified as part of the factory-shipped configuration.

Jumper Connection			Description
M60	o——o	M59	Factory shipped configuration
M58	o o	M57	9600 baud
M56	o——o	M55	

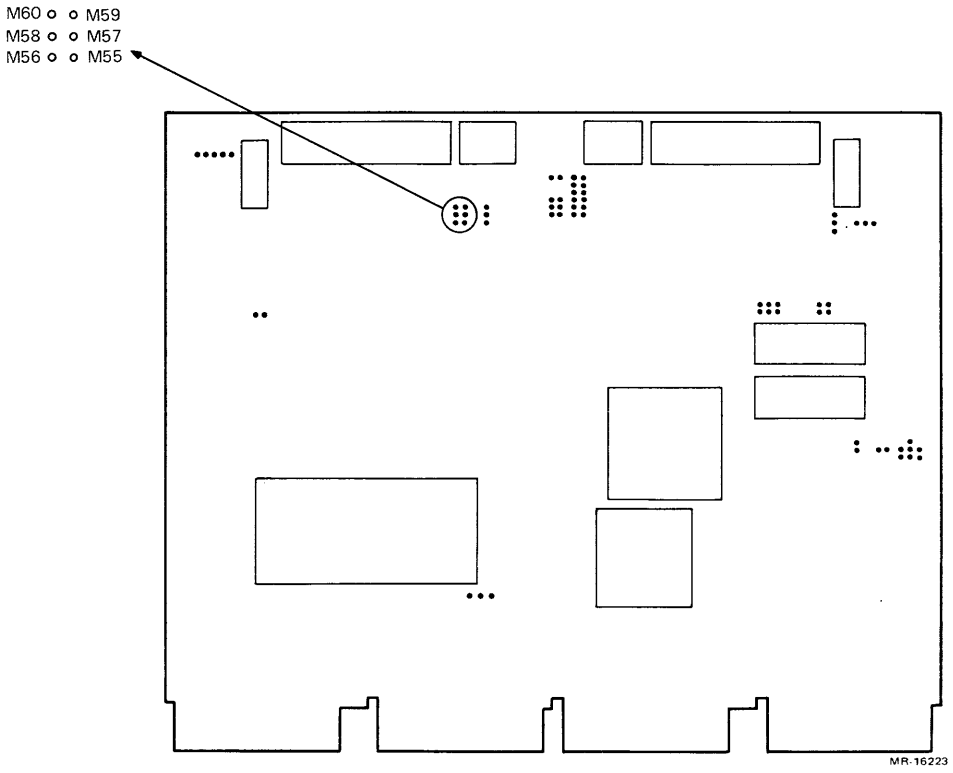


Figure 2-13 SLU1 Baud Rate

Table 2-4 SLU1 Baud Rate Jumpering

Baud Rate	M56 to M55	M58 to M57	M60 to M59
38400	In	In	In
19200	In	In	Out
9600*	In	Out	In
4800	In	Out	Out
2400	Out	In	In
1200	Out	In	Out
600	Out	Out	In
300	Out	Out	Out

* Factory-shipped configuration

2.11 SLU1 Transmitter

The SLU1 transmitter can be jumpered to send either single-ended (RS423) or differential (RS422) asynchronous serial data via connector J3. The location of the jumpers is shown in Figure 2-14. RS423 transmission is selected as part of the factory-shipped configuration.

Jumper Connection	Description
M63 M62 M61 o o——o	RS423 transmission selected*
M63 M62 M61 o——o o	RS422 transmission selected

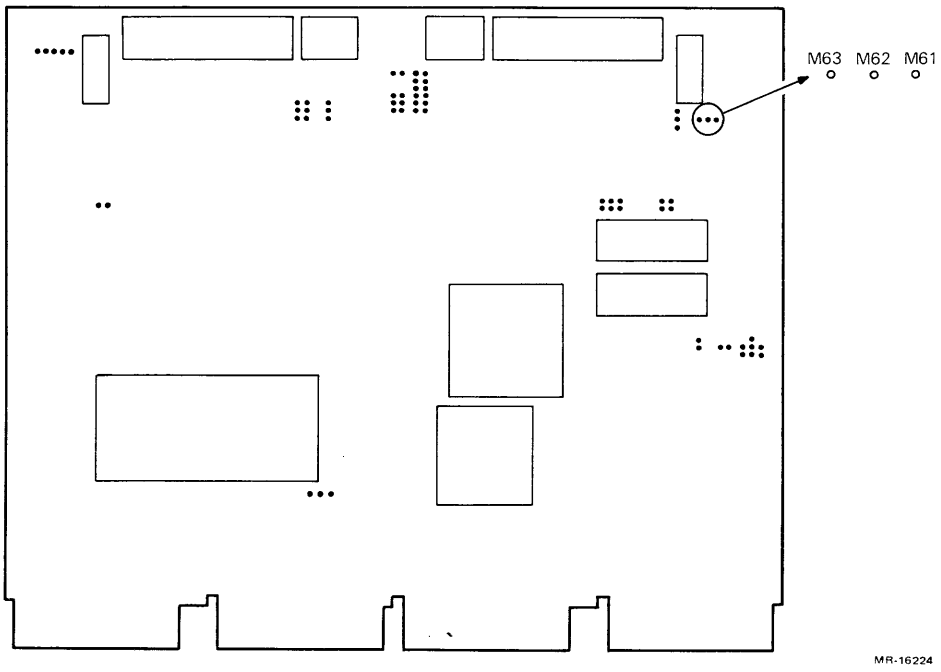


Figure 2-14 SLU1 Transmitter

* Factory-shipped configuration

2.12 SLU1 Receiver

The SLU1 receiver can be jumpered to receive either single-ended (RS423) or differential (RS422) asynchronous serial data via connector J3. The location of the jumper is shown in Figure 2-15. RS423 reception is selected as part of the factory-shipped configuration.

Jumper Connection	Description
M48 M47 o———o	RS422 reception selected
M48 M47 o o	RS423 reception selected*

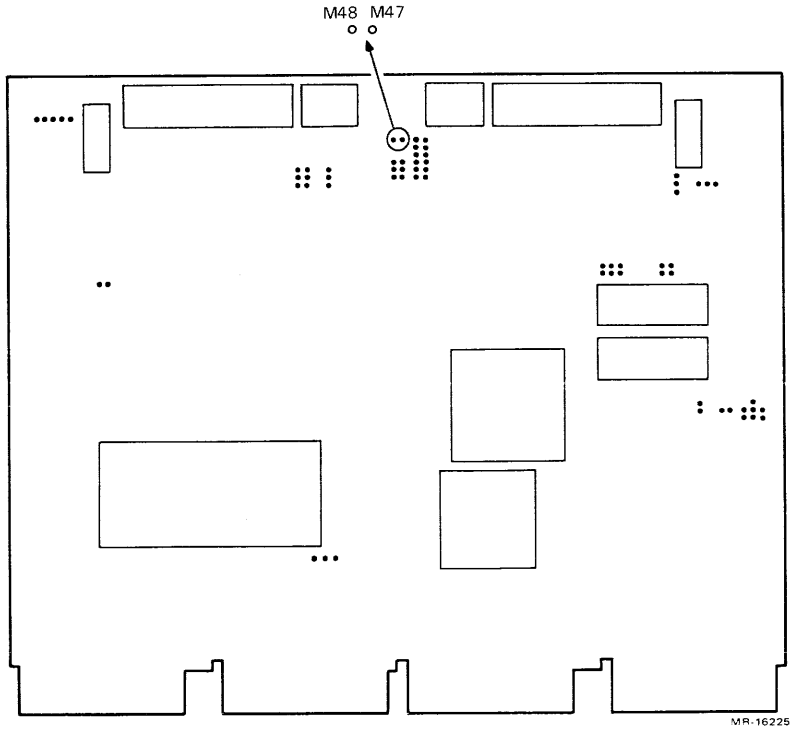


Figure 2-15 SLU1 Receiver

* Factory-shipped configuration

2.13 SLU2 Channel A Receiver

The SLU2 channel A receiver can be jumpered to receive either single-ended (RS423) or differential (RS422) serial data via connector J1. The location of the jumpers is shown in Figure 2-16. RS422 reception is selected as part of the factory-shipped configuration.

Jumper Connection			Description
M34	o——o	M33	RS422 reception selected*
M32	o——o	M31	
M30	o——o	M29	
M28	o——o	M27	
M26	o——o	M25	
M24	o——o	M23	
M34	o o	M33	RS423 reception selected
M32	o o	M31	
M30	o o	M29	
M28	o o	M27	
M26	o o	M25	
M24	o o	M23	

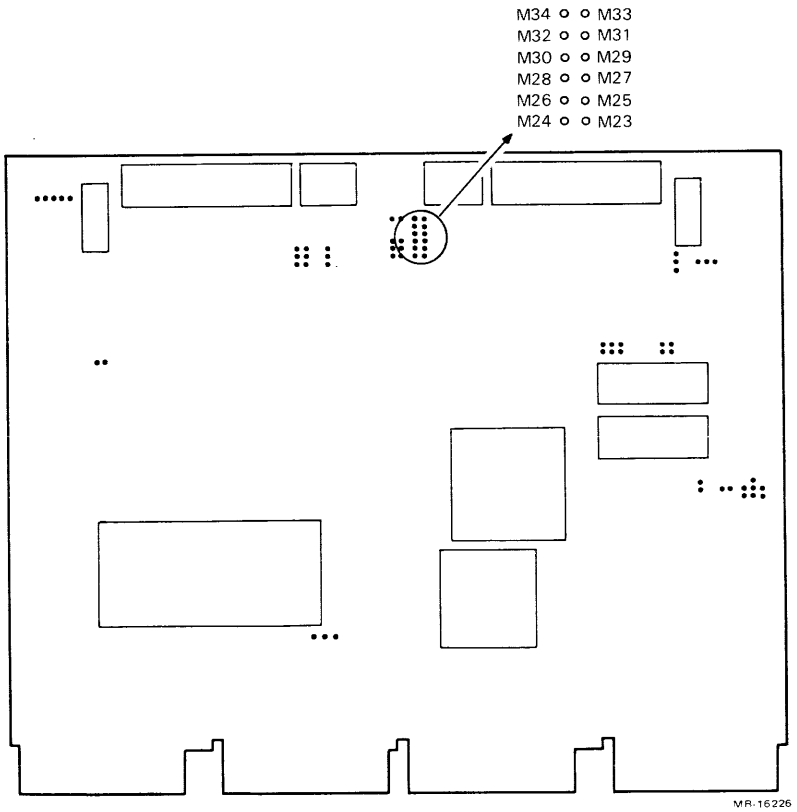
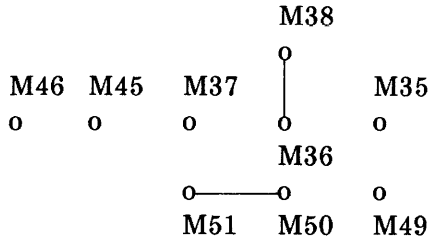
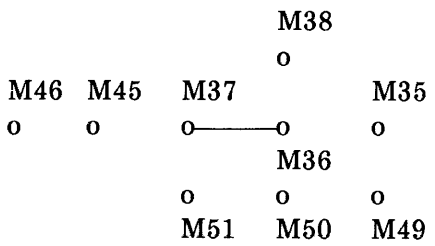


Figure 2-16 SLU2 Channel A Receiver

* Factory-shipped configuration

2.14 SLU2 Channel B Transmitter

The SLU2 channel B transmitter can be jumpered to send single-ended (RS423), differential (RS422), or party line (CCITT R1360) serial data via connector J2. The location of the jumpers is shown in Figure 2-17. RS422 transmission is selected as part of the factory-shipped configuration.

Jumper Connection	Description
	RS422 transmission selected*
	RS423 transmission selected
	Party line transmission selected

* Factory-shipped configuration

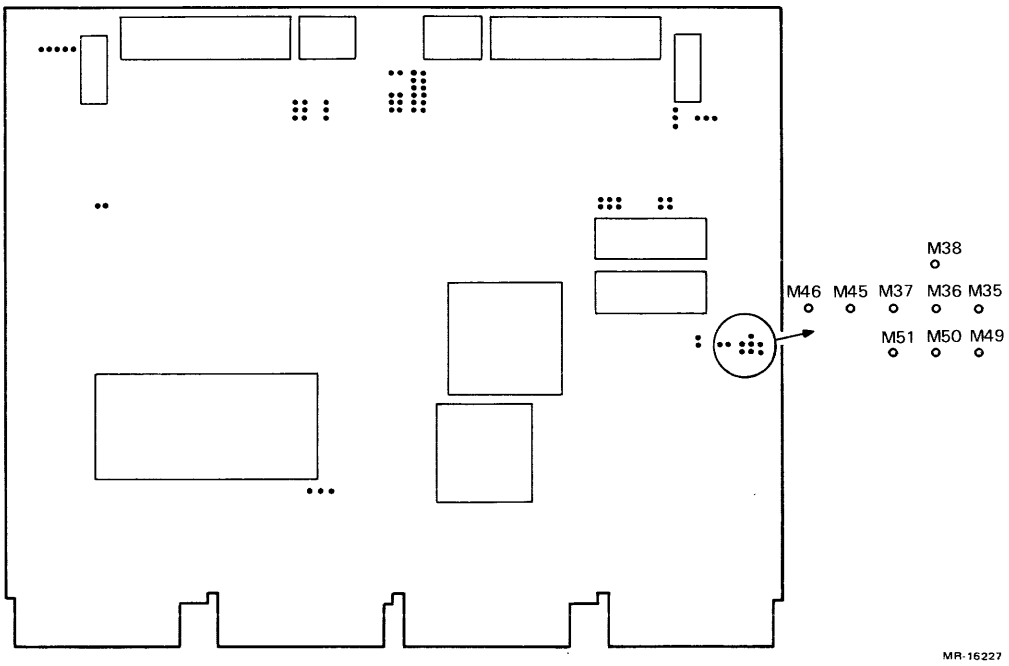


Figure 2-17 SLU2 Channel B Transmitter

2.15 SLU2 Channel B Receiver

The SLU2 channel B receiver can be jumpered to receive single-ended (RS423), differential (RS422), or party line (CCITT R1360) serial data via connector J2. Two groups of jumpers are involved and shown in Figure 2-18. RS422 reception is selected as part of the factory-shipped configuration.

Jumper Connection						Description
M44	o	o	M43	o	M20	RS422 reception selected*
M42	o——	——o	M41	o	M21	
M40	o——	——o	M39	o	M22	
M44	o	o	M43	o	M20	RS423 reception selected
M42	o	o	M41	o	M21	
M40	o	o	M39	o	M22	
M44	o——	——o	M43	o	M20	Party line reception selected
M42	o	o	M41	o	M21	
M40	o	o	M39	o	M22	

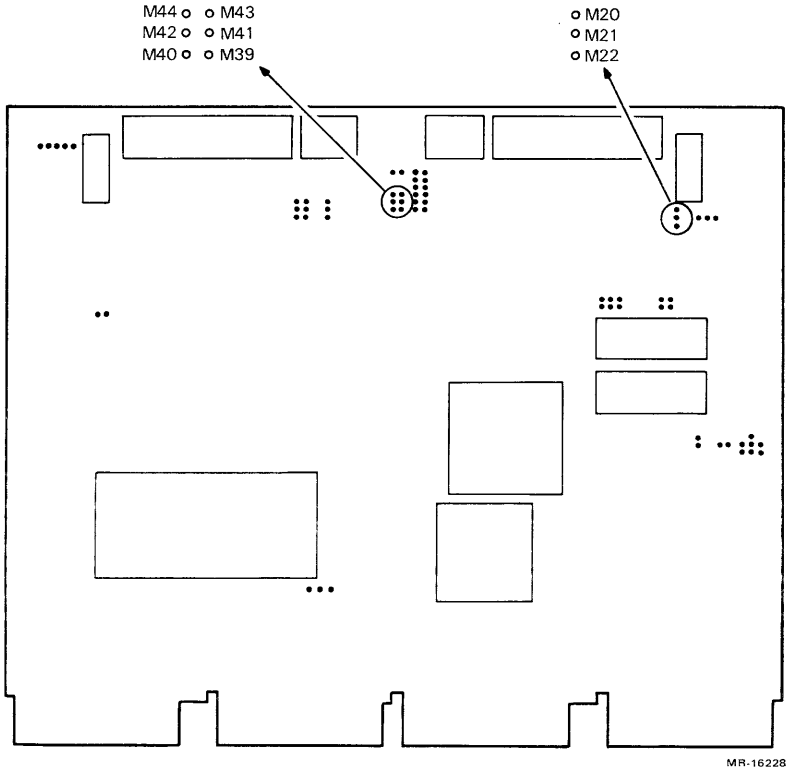


Figure 2-18 SLU2 Channel B Receiver

* Factory-shipped configuration

2.16 Real-Time Clock Interrupt

SLU1 (the on-board DLART) can generate real-time clock interrupts at frequencies of 50 and 60 Hz. Jumpers M52, M53, and M54 select either the 50 Hz or the 60 Hz real-time clock as input to the interrupt control logic. If interrupts are enabled, each clock "tick" results in a maskable priority level 6 interrupt request to the on-board J-11. The location of the real-time clock interrupt jumpers is shown in Figure 2-19. A real-time clock rate of 60 Hz is specified as part of the factory-shipped configuration.

Jumper Connection	Description
o M54 o M53 o M52	60 Hz real-time clock selected*
o M54 o M53 o M52	50 Hz real-time clock selected

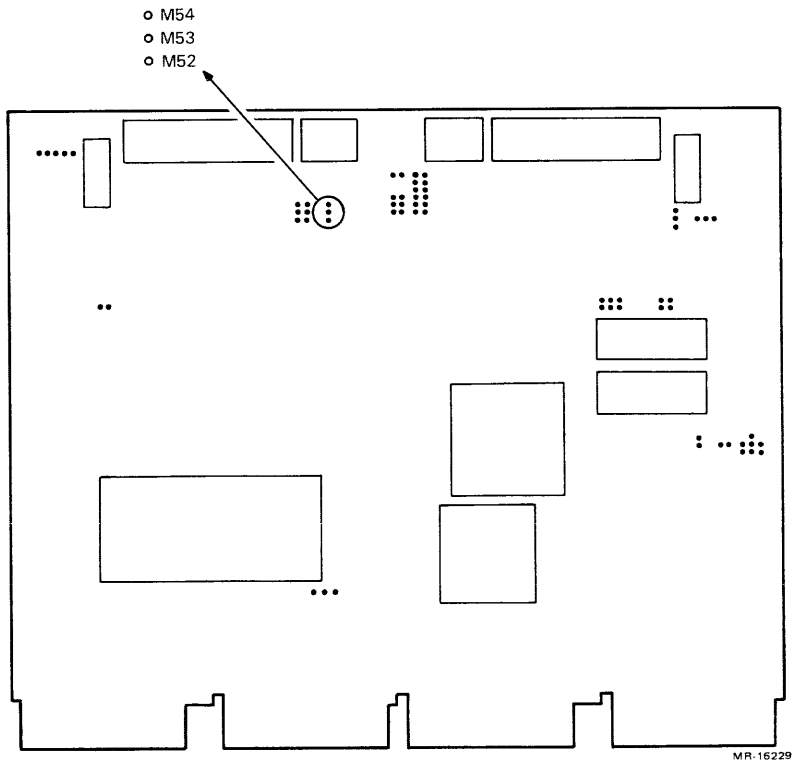


Figure 2-19 Real-Time Clock Interrupt

* Factory-shipped configuration

Chapter 3
Power Supply Considerations

When installing the KXJ11-CA, make sure the power supply can handle the extra load presented by the board. The KXJ11-CA draws a maximum of 6A at +5V. In addition, the KXJ11-CA draws a maximum of 1.4A at +12V, for systems with the DLV11-KA option, or .4A maximum at +12V, for systems without the DLV11-KA option. The board adds 2.7 ac loads and 1.0 dc loads to the bus.

In standalone mode, at least four power fingers (backplane connections) and four ground fingers for +5 Vdc must be connected to the power supply. In addition, at least two power fingers and two ground fingers for +12 Vdc must be connected to the power supply.

Chapter 4
Installing the KXJ11-CA in a Backplane

The KXJ11-CA plugs into any Digital standard quad-height Q-Bus backplane (see Figure 4-1). No special backplane wiring or jumpering is required to accommodate the KXJ11-CA. However, the grant structure must be preserved if there are blank slots between the KXJ11-CA and the top of the backplane. This can be accomplished by inserting grant cards where appropriate. (Figure 4-2 is an example of the use of grant cards.) The dual-height grant card (M8659) preserves grant continuity for slots A and B, and grant card G7272 preserves both the DMA and interrupt grant continuity for slot C. The KXJ11-CA board must also be configured for the proper Q-Bus address size.

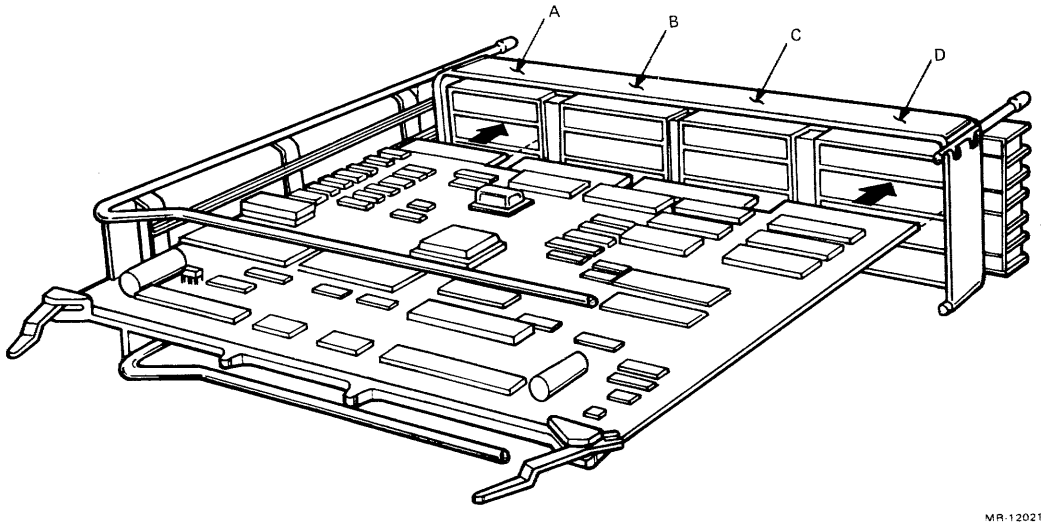


Figure 4-1 Backplane Installation

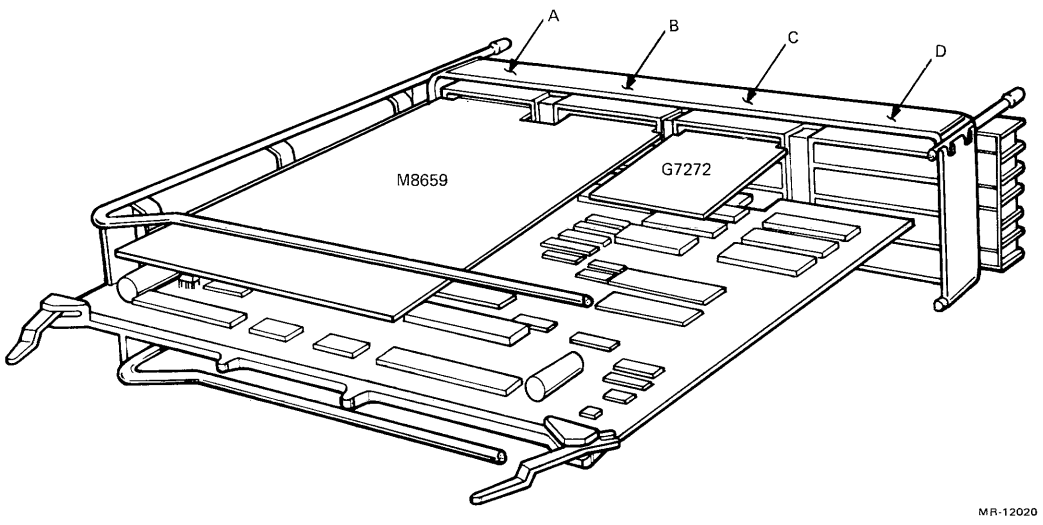


Figure 4-2 Using Grant Cards

4.1 Edge Connector Pin Assignments

Table 4-1 summarizes the edge connector pin assignments for the KXJ11-CA. The board is designed to mate with Digital standard quad height backplanes for Q-Bus based systems.

Table 4-1 KXJ11-CA Pin Identification

Component Side		Solder Side	
Pin	KXJ11-CA Signal	Pin	KXJ11-CA Signal
AA1	NC	AA2	+5V
AB1	NC	AB2	NC
AC1	BDAL16 L	AC2	GND
AD1	BDAL17 L	AD2	NC
AE1	NC	AE2	BDOUT L
AF1	NC	AF2	BRPLY L
AH1	NC	AH2	BDIN L
AJ1	GND	AJ2	BSYNC L
AK1	NC	AK2	BWTBT L
AL1	NC	AL2	BIRQ4 L
AM1	GND	AM2	BIAKI L
AN1	BDMR L	AN2	BIAKO L
AP1	BHALT L	AP2	BBS7 L
AR1	NC	AR2	BDMGI L
AS1	NC	AS2	BDMGO L
AT1	GND	AT2	BINIT L
AU1	NC	AU2	BDAL0 L
AV1	+5VB	AV2	BDAL1 L
BA1	BDCOK H	BA2	+5V
BB1	BPOK H	BB2	NC
BC1	BDAL18 L	BC2	GND
BD1	BDAL19 L	BD2	+12V
BE1	BDAL20 L	BE2	BDAL2 L
BF1	BDAL21 L	BF2	BDAL3 L
BH1	NC	BH2	BDAL4 L
BJ1	GND	BJ2	BDAL5 L
BK1	NC	BK2	BDAL6 L
BL1	NC	BL2	BDAL7 L
BM1	GND	BM2	BDAL8 L
BN1	BSACK L	BN2	BDAL9 L
BP1	NC	BP2	BDAL10 L
BR1	NC	BR2	BDAL11 L
BS1	NC	BS2	BDAL12 L
BT1	GND	BT2	BDAL13 L
BU1	NC	BU2	BDAL14 L
BV1	+5V	BV2	BDAL15 L

Table 4-1 KXJ11-CA Pin Identification (Cont)

Component Side		Solder Side	
Pin	KXJ11-CA Signal	Pin	KXJ11-CA Signal
CA1	NC	CA2	+5V
CB1	NC	CB2	NC
CC1	NC	CC2	GND
CD1	NC	CD2	NC
CE1	NC	CE2	NC
CF1	NC	CF2	NC
CH1	NC	CH2	NC
CJ1	NC	CJ2	NC
CK1	NC	CK2	NC
CL1	NC	CL2	NC
CM1	NC	CM2	IAK L (Note 2)
CN1	NC	CN2	IAK L (Note 2)
CP1	NC	CP2	NC
CR1	NC	CR2	DMG L (Note 3)
CS1	NC	CS2	DMG L (Note 3)
CT1	GND	CT2	NC
CU1	NC	CU2	NC
CV1	NC	CV2	NC
DA1	NC	DA2	+5V
DB1	NC	DB2	NC
DC1	NC	DC2	GND
DD1	NC	DD2	NC
DE1	NC	DE2	NC
DF1	NC	DF2	NC
DH1	NC	DH2	NC
DJ1	NC	DJ2	NC
DK1	NC	DK2	NC
DL1	NC	DL2	NC
DM1	NC	DM2	NC
DN1	NC	DN2	NC
DP1	NC	DP2	NC
DR1	NC	DR2	NC
DS1	NC	DS2	NC
DT1	GND	DT2	NC
DU1	NC	DU2	NC
DV1	NC	DV2	NC

NOTES

1. NC = Not connected
2. Pin CM2 is jumpered to pin CN2 for the interrupt acknowledge daisy chain.
3. Pin CR2 is jumpered to pin CS2 for the DMA grant daisy chain.

Chapter 5
Connectors and External Cabling

The KXJ11-CA communicates with external devices via a parallel I/O connector (J4) and three serial I/O connectors (J1, J2, and J3). This section specifies the pin assignments of these connectors and lists the types of cables that can be used with each connector.

5.1 Parallel I/O Interface (J4)

The parallel I/O (PIO) interface signals appear at connector J4. These signals are buffered. They can be driven over a 50-foot distance via a ribbon cable, or round cable with a 40-pin AMP contact housing (AMP part number 746473-9) at each end. A PIO cable is not provided with the KXJ11-CA. The following PIO cables are recommended for use in the KXJ11 and are available from Digital Equipment Corporation.

- Shielded ribbon cable BC06 R
- "Mirror image" cable BC05 L

Figure 5-1 lists the pin assignments for J4, the parallel I/O connector.

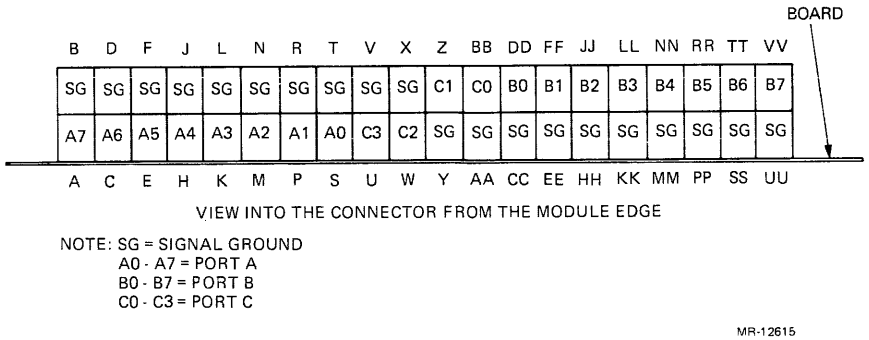


Figure 5-1 Parallel I/O Interface Pin Assignments

5.2 Serial I/O Lines (J1, J2, J3)

The KXJ11-CA has three serial I/O lines.

- SLU2 channel A (J1), a synchronous/asynchronous serial line with modem control
- SLU2 channel B (J2), a synchronous/asynchronous serial line without modem control
- SLU1 (J3), the console asynchronous serial line (no modem control)

Each serial line is compatible with the EIA RS232-C and RS422/RS423 protocols. In addition, SLU2 channel B (J2) is compatible with the CCITT R1360 party line protocol. To interface the KXJ11-CA with a 4-20 mA current loop device via the serial lines, use the DLV11-KA option.

Users must supply their own serial line cables. The following cables are recommended for use for the J2 and J3 serial I/O lines and are available from Digital Equipment Corporation.

BC20N-05	A 5-foot EIA RS232-C null modem cable for a direct connection between the KXJ11-CA and an EIA terminal. This cable has a 10-pin (2 × 5) AMP female connector on one end and a 25-pin RS232-C female connector on the other.
BC21B-05	A 5-foot EIA RS232-C modem cable for a connection between the KXJ11-CA and a modem or acoustic coupler. This cable has a 10-pin (2 × 5) AMP female connector on one end and a 25-pin RS232-C male connector on the other.
BC20M-50	A 50-foot EIA RS422 or RS423 cable for a direct connection between the KXJ11-CA and a remote processor. Used in applications requiring high data transmission speeds (up to 19.2 K baud), this cable has a 10-pin (2 × 5) AMP female connector on each end.

The pin designations for J2 and J3 are shown in Figure 5-2.

All three serial lines are factory configured to handle differential inputs and outputs. If you change the configuration of any of the serial lines to handle single-ended inputs or outputs, make sure the return (-) signal(s) on the cable are tied to signal ground.

Because there is no standard cable available from Digital Equipment Corporation for SLU2 channel A, you need to construct your own cable. A standard 40-pin AMP connector may be used (AMP part number 746473-9) for connection to J1. Figure 5-3 illustrates the pin assignments for SLU2 channel A (J1).

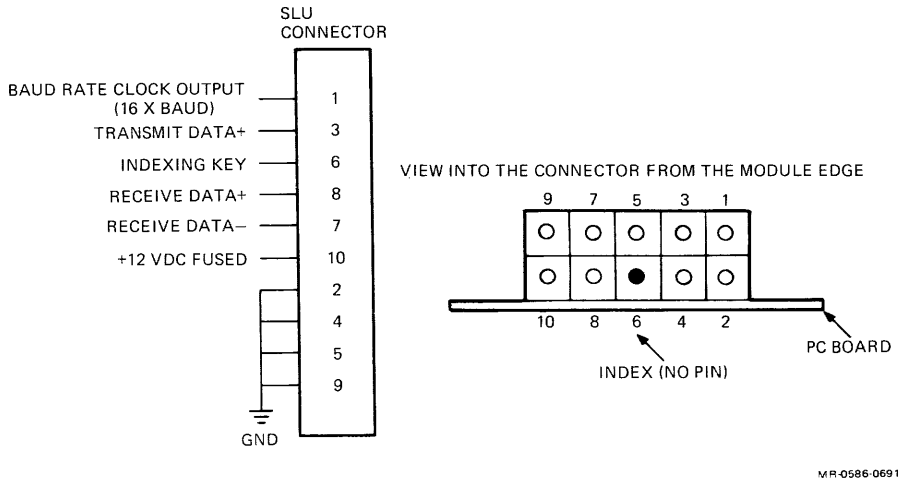


Figure 5-2 J2 and J3 Pin Assignments (10-Pin)

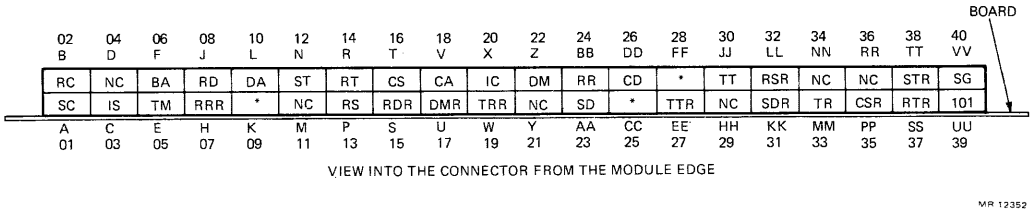


Figure 5-3 J1 Pin Assignments (40-Pin)

Tables 5-1 through 5-3 show the correspondence between the pins of the standard connectors for the RS422/RS423, RS232, and CCITT protocols, and the pins of J1. These tables make it easy to construct an appropriate cable. The KXJ11-CA register address associated with each signal is specified in the last column of each table for ease of programmer reference. For further details, see the register descriptions in Chapters 3 and 6 of *The KXJ11-CA Single-Board Computer User's Guide* (EK-KXJCA-UG-001).

Table 5-1 RS422/RS423 Interface to J1

Pin	Circuit	Direction	Function	RS-232	CCITT	Pin	Location
1	SHIELD	—	Protective Ground			—	
2	SI	From Modem		CI	112	5,E	17777522
3	SPARE					—	
4	SD	To Modem	Send Data (+)	BA	103	23,AA 6,F	17775706
5	ST	From Modem	Send Timing (+)	DB	114	12,N	17777520
6	RD	From Modem	Receive Data (+)	BB	104	8,J	17775702
7	RS	To Modem	Request to Send (+)	CA	105	13,P 18,V	17775704
8	RT	From Modem	Receive Timing (+)	DD	115	14,R	17775720
9	CS	From Modem	Clear to Send (+)	CB	106	16,T	17775700
10	LL	To Modem	Local Loop		141	25,CC	Dummy Gen.
11	DM	From Modem	Data Mode (+)	CC	107	22,Z	17775710
12	TR	To Modem	Terminal Ready (+)	CD	108/2	33,M 26,DD	17777520
13	RR	From Modem	Receiver Ready (+)	CF	109	24,BB	17775700
14	RL	To Modem	Remote Loop		140	9,K	Dummy Gen.
15	IC	From Modem	Incoming Call	CE	125	20,X	17775710
16	SF/SR	To Modem	Select Frequency		126	3,C	17777520
			Signal Rate Select	CH	111	3,C	
17	TT	To Modem	Terminal Timing (+)	DA	113	30,JJ 10,L	17777530
18	TM	From Modem	Test Mode		142	5,E	17777522
19	SG	To Modem	Signal Ground	AB	102	40,W	
20	RC	From Modem	Receive Common		102b	2,B	
21	SPARE					—	
22	SDR	To Modem	Send Data (-)			31,KK	
23	STR	From Modem	Send Timing (-)			38,TT	
24	RDR	From Modem	Receive Data (-)			15,S	
25	RSR	To Modem	Request to Send (-)			32,LL	

Table 5-1 RS422/RS423 Interface to J1 (Cont)

Pin	Circuit	Direction	Function	RS-232	CCITT	Pin	Location
26	RTR	From Modem	Receive Timing (-)			37,SS	
27	CSR	From Modem	Clear to Send (-)			35,PP	
28	IS	To Modem	Terminal in Service			3,C	17777520
29	DMR	From Modem	Data Mode (-)			17,V	
30	TRR	To Modem	Terminal Ready (-)			19,W	
31	RRR	From Modem	Receiver Ready (-)			7,H	
32	SS	To Modem	Select Standby		116	28,FF Gen.	Dummy
33	SQ	From Modem	Signal Quality	CG	110	—	
34	NS	To Modem	New Signal			—	
35	TTR	To Modem	Terminal Timing (-)			27,EE	
36	SB	From Modem	Standby Indication		117	—	
37	SC	To Modem	Send Common		102a	1,A	

NOTES

1. Pins K 9, 25 CC, and 28 FF are driven by dummy generators that disable RL (CCITT 140), LL (CCITT 141), and SS (CCITT 116) respectively.
2. The label NC indicates no connection.
3. The suffix R in a three-letter pin label (such as RDR) signifies that the pin is associated with the return side of a differential driver or receiver.
4. Circuit IS can be redefined to mean SF. Or IS can be redefined as SR. In the second case, TM is also redefined as SI.

Table 5-2 RS232-C Interface to J1

Pin	Circuit	Direction	Function	CCITT	Pin	Location
1	AA	—	Protective Ground	101	39,UU	
2	BA	To Modem	Transmitted Data	103	6,F	17775706
3	BB	From Modem	Received Data	104	8,J	17775702
4	CA	To Modem	Request to Send	105	18,V	17775704
5	CB	From Modem	Clear to Send	106	16,T	17775700
6	CC	From Modem	Data Set Ready	107	22,Z	17775710
7	AB	—	Signal Ground	102	40,W	
8	CF	From Modem	Receiver Ready	109	24,BB	17775700
9	—	(From Modem)	(+ DC Test Voltage)		—	
10	—	(To Modem)	(- DC Test Voltage)		—	
11	—	—	Unassigned		—	
12	SCF	From Modem	Secondary Carrier Detector	122	—	
13	SCB	From Modem	Secondary Clear to Send	121	—	
14	SBA	To Modem	Secondary Transmitted Data	118	—	
15	DB	From Modem	Transmitter Clock	114	12,N	17777520
16	SBB	From Modem	Secondary Received Data	119	—	
17	DD	From Modem	Receiver Clock	115	14,R	17777520
18	—	To Modem	Receiver Dibit Clock			
19	SCA	To Modem	Secondary Request to Send	120	—	
20	CD	To Modem	Data Terminal Ready	108/2	26,DD	17777520
21	CG	From Modem	Signal Quality Detector	110	—	
22	CE	From Modem	Ring Indicator	125	20,X	17775710
23	CH/CI	To Modem	Data Rate Selector	111	5,E	17777522
				112	3,C	17777520
24	DA	To Modem	External Transmitter Clock	113	10,L	17777530
25	CN	To Modem	Force Busy		—	

Table 5-3 CCITT/V.35 Interface to J1

Pin	Circuit	Direction	Function	RS232	RS449	Pin	Location
A	101	—	Protective Ground	AA		39,UU	
B	102	—	Signal Ground	AB	SG	40,W	
C	105	To Modem	Request to Send	CA	RS	18,V	17775704
D	106	From Modem	Ready for Sending	CB	CS	16,T	17775700
E	107	From Modem	Data Set Ready	CC	DM	22,Z	17775710
F	109	From Modem	RCV Line Signal Det	CF	RR	24,BB	17775700
H	108/1	To Modem	Connect Data Set				
	108/2	To Modem	Data Terminal Ready	CD	TR	26,DD	17777520
J	125	From Modem	Calling Indicator	CE	IC	20,X	17775710
R	104	From Modem	Received Data A	BB	RD	8,J	17775702
T	104	From Modem	Received Data B		RD	—	
V	115	From Modem	Receive Timing A	DD	RT	14,R	17777520
X	115	From Modem	Receive Timing B		RT	—	
Y	114	From Modem	Transmit Timing A	DB	ST	12,N	17777520
AA	114	From Modem	Transmit Timing B		ST	—	
P	103	To Modem	Transmit Data A	BA	SD	6,F	17775706
S	103	To Modem	Transmit Data B		SD	—	
U	113	To Modem	Terminal Timing A	DA	TT	10,L	17777530
W	113	To Modem	Terminal Timing B		TT	—	

5.3 Loopback Connectors

Loopback connectors (not provided with the KXJ11-CA) are attached to the serial or parallel communication ports to determine whether or not they are operating correctly (see Figure 5-4). They are typically used in conjunction with the running of diagnostic programs, and in some firmware self-tests (see Section 2.1). These connectors may be ordered from Digital Equipment Corporation or may be built by the user.

There are three different types of loopback connectors available from Digital. A 10-pin loopback connector (Digital part number H3270) is plugged into either J2 to test SLU2 channel B, or into J3 to test SLU1. A 40-pin loopback connector (Digital part number H3022) is plugged into J1 to test SLU2 channel A. This loopback connector can also be configured to test RS422 or RS423 operation (see Figure 5-4). The third type of loopback connector is also 40 pins (Digital part number H3021), and is plugged into J4 to test the parallel I/O port.

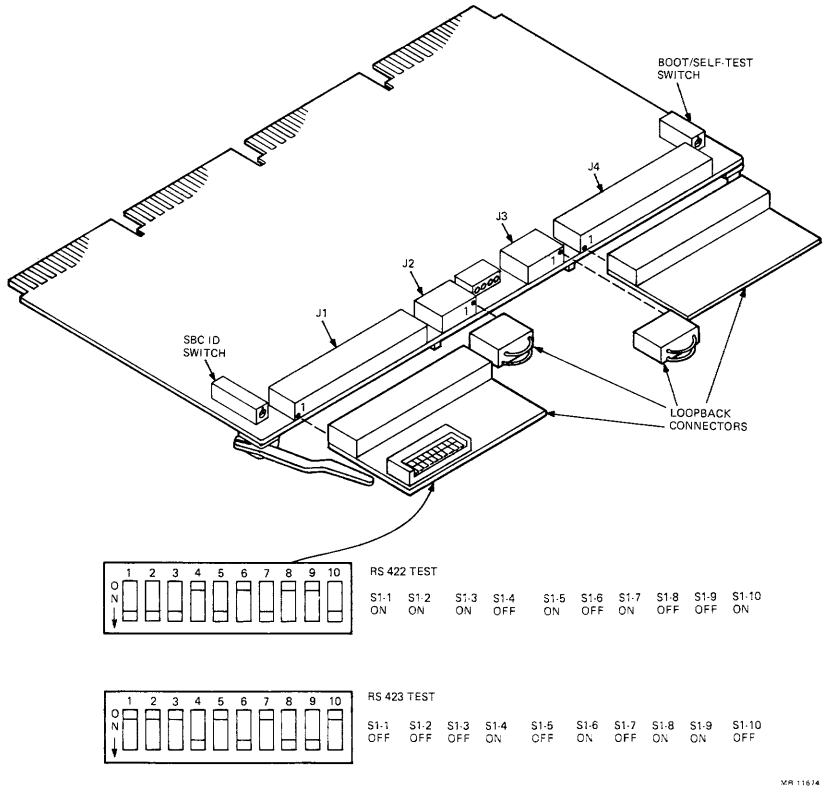


Figure 5-4 Loopback Connectors

Chapter 6
Diagnostics

6.1 Error Detection and Reporting with the LEDS

There are four LEDs on the edge of the KXJ11-CA board that the native firmware uses to indicate the state of the board. These are especially useful for diagnostic purposes during power-up or reinitialization. These LEDs verify that the board is operating properly or, if there is a problem with the board, can help the user locate the difficulty. Table 6-1 summarizes the conditions the LEDs can indicate.

Upon power-up or reinitialization, all four LEDs are illuminated for approximately 1/2 second, if they are working properly. When the KXJ11-CA is installed in a backplane in a box, the LEDs are labeled L4 through L1 from left to right. If the KXJ11-CA runs its self-tests (this is determined by the setting of the boot/self-test switch), L4 is off and L3 - L1 should be on as the self-tests run. If one of the self-tests fails, L4 is illuminated, and L3 - L1 indicate the test that failed. Self-tests are run in the order listed in Table 6-1. Thus, if a test fails, the user can also determine which tests (if any) passed.

If all the self-tests run without error, the KXJ11-CA performs a boot operation. The boot/self-test switch setting determines which function is performed. L4 remains off and L3 - L1 indicate the status of the executing code. Note that the boot/self-test switch may be set so self-tests are not run. If self-tests have not been run, then L4 is off, and L3 - L1 indicate the state of the board as it executes code.

Table 6-1 LED Display Definitions

LEDs				
L4	L3	L2	L1	Meaning
x	x	x	x	All LEDs on for 1/2 second at the start of a power-up or reinitialization operation
x	x	x	x	Can't access Control/Status Registers in I/O page (fatal error); or the power-up jumper (M16-M17) is installed, which precludes self-tests.
x	o	o	o	DMA or RTC test failed
x	o	o	x	RAM test failed
x	o	x	o	ROM checksum test failed
x	o	x	x	Serial line test of SLU1 failed
x	x	o	o	Serial line test of SLU2 channel A failed
x	x	o	x	Serial line test of SLU2 channel B failed
x	x	x	o	Parallel port test failed
o	x	x	x	Auto self-tests running. Auto self-tests do not require loopback connectors.
o	x	x	o	Loopback tests and auto self-tests running
o	x	o	x	Q-Bus ODT mode
o	x	o	o	Unused
o	o	x	x	Waiting for command
o	o	x	o	Performing DTC load
o	o	o	x	TU58 primary bootstrap executing
o	o	o	o	Executing non-native code

Quick LED Reference

LEDs				
L4	L3	L2	L1	Meaning
x	-	-	-	Self-test error detected
x	x	x	x	Fatal self-test error detected
o	-	-	-	No self-test errors detected
o	o	o	o	Application running without error

Legend

x = On
o = Off
- = Don't care (either On or Off)

6.2 Diagnostic Testing with XXDP+

The KXJ11-CA can be tested by running XXDP+, a diagnostic operating system that is booted from the user's system disk. This section explains how to run the XXDP+ diagnostics to test the KXJ11-CA. More information on XXDP+ is found in *The XXDP+ System User's Manual* (AC-F348F-MC).

When you have successfully booted XXDP+ from the system disk, a message such as the one shown below appears on the console terminal. The items that are blank (underscore) indicate values that are system-dependent.

```
BOOTING UP XXDP-_______ MONITOR

XXDP-SM _____ MONITOR VERSION ____
BOOTED FROM ____
____KW OF MEMORY
NON-UNIBUS SYSTEM

RESTART ADDR: _______
THIS IS XXDP= ___ TYPE "H" or "H/L" FOR HELP
.
```

When the "period" (.) prompt appears, the user types in

```
R ZKXA??<CR>
```

This initiates the running of the tests. The message

```
ZKA__.BIN
```

appears on the console, followed by several lines of system information (the underscore indicates characters that are system dependent). Then the following message should appear.

```
USE <ESC> TO HALT

KXJ FUNCTIONAL TEST

SWR     OCTAL     FUNCTION

15      100000    HALT ON ERROR
14      040000    INHIBIT ERROR SUMMARY
13      020000    INHIBIT ERROR REPORTS
12      010000    IOP IO# KNOWN GOOD FOR TESTING
11      004000    TEST STAND ALONE IOP
10      002000    ENABLE EXTENDED MEMORY TESTS
09      001000    LOOP ON ERROR
08      000400    LOOP ON TEST IN SWR<6:0>
07      000200    INHIBIT TEST NUMBER/TITLE

SWR = 140000 NEW =
```

At this point, type <CR>, which runs the tests until an error is detected. As the tests run, their results are displayed on the console. If an error is detected, a self-explanatory error message is displayed, and the tests halt if bit 15 in the SWR is set to 1. The halt causes an entry into MicroODT. To continue after an error has caused a halt, type

```
P<CR>
```

using the console keyboard.

If no errors are detected, testing can be terminated, if the BREAK enable jumper is installed, by pressing the ESCAPE key (which halts the KXJ11-CA and causes micro-ODT to be entered), or by pressing the BREAK key (which halts the arbiter).

READER'S COMMENTS

Your comments and suggestions will help us in our efforts to improve the quality and usefulness of our publications.

1. **Which of the following most closely describes your job?** **1** ⊂a⊃ ⊂b⊃ ⊂c⊃ ⊂d⊃ ⊂e⊃ ⊂f⊃ ⊂g⊃ ⊂h⊃ ⊂i⊃

   (a) Administrative support (d) Scientist/Engineer (g) Educator/Trainer
   (b) Programmer/Analyst (e) Systems Manager (h) Computer Operator
   (c) Software support (f) Sales (i) Other _____

2. **How many years of experience do you have with computers?** **2** ⊂a⊃ ⊂b⊃ ⊂c⊃ ⊂d⊃ ⊂e⊃

   (a) Less than 1 (b) 1 to 3 (c) 4 to 6 (d) 7 to 9 (e) 10 or more

3. **What did you like *most* about this manual?**

4. **What did you like *least* about this manual?**

5. **How do you rate this manual?**

   Indicate your opinion of the quality of the manual. For each aspect of quality, darken your response on the five-point scale, where (1) = POOR and (5) = EXCELLENT

(a) Accuracy	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(b) Completeness	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(c) Usefulness of Examples/Figures	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(d) Clearness of Language	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(e) Helpfulness of Index/Table of Contents	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(f) Consistency in Presenting Information	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(g) Logical Organization	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(h) Visual Appeal	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(i) Relevance of Information	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(j) Ease of Learning	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(k) Ease of Use	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(l) YOUR OVERALL IMPRESSION	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(m) Quality Relative to Other Digital Manuals	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(n) Quality Relative to Other Companies' Manuals	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃

6. **List any errors you found in the manual. (Reference page, table, or figure numbers.)**

7. **Do you have any additional comments?**

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