digital

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JAN 84/REV 1
EK-KDJ1A-CG-001

KDJ11-A CONFIGURATION GUIDE

Introduction

The KDJ11-A has nine jumpers for the user selectable features. The location of these jumpers are shown in the following figure and their functions are described below. A jumper is installed by pushing an insulated jumper wire (P/N 12-18783-00) on the two wirewrap pins provided on the module.

Jumper Identification

Jumper	Function
W9	BVNT recognition
W8	Wakeup disable
W7	Power-up option bit <01>
W6	Bootstrap address bit <12>
W5	HALT trap option bit <03>
W4	Bootstrap address bit <13>
W3	Power-up option bit<02>
W2	Bootstrap address bit <14>
W1	Bootstrap address bit <15>

Power-Up Options

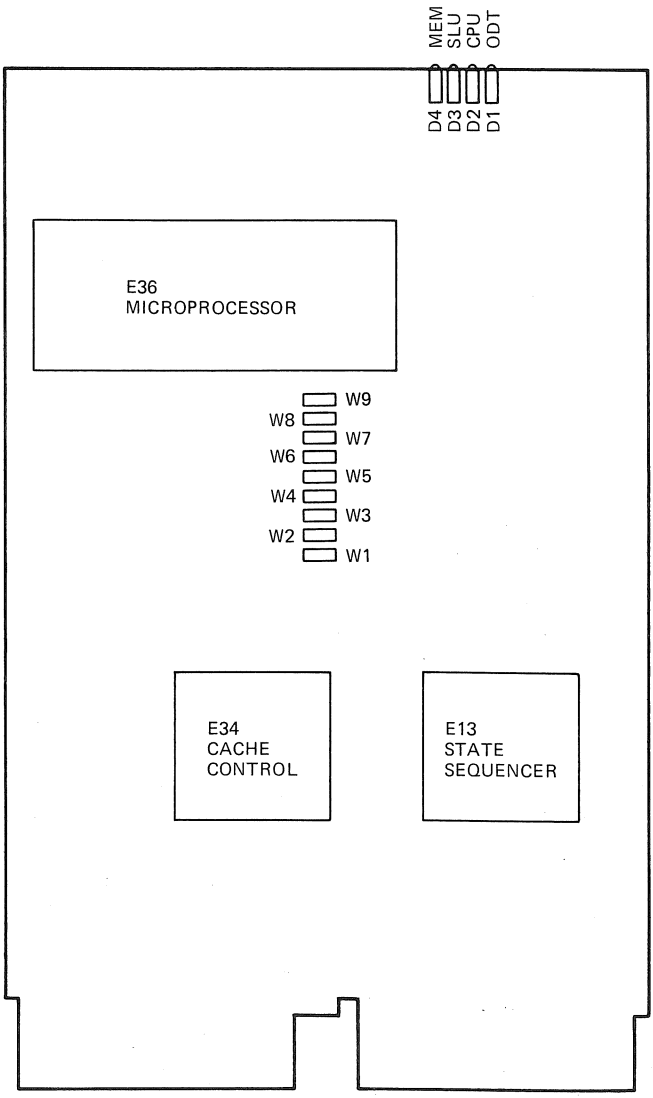
There are four power-up options. These options are selected by jumpers W7 and W3. The bits are set (1) when the jumpers are removed. The power-up options are described below.

Option 0 — The KDJ11-A reads physical memory locations 24 and 26, and loads the stored data into the PC and PS, respectively. The KDJ11-A either services pending interrupts, or starts program execution at the memory location pointed at by the PC.

Option 1 — The KDJ11-A unconditionally enters micro-ODT with the PS cleared. Pending service conditions are ignored.

Option 2 — The KDJ11-A sets the PC to 173000 and the PS to 340. The KDJ11-A then either services pending interrupts or starts program execution at the memory location pointed at the PC. This option is used for the standard bootstrap.

Option 3 — The KDJ11-A reads the four bootstrap address jumpers and loads the results into PC<15:12>. PC<11:00> are set to zero, and the PS is set to 340. The KDJ11-A then either services pending interrupts, or starts the program execution at the memory location pointed at by the PC.



KDJ11-A Jumper Locations

Power-Up Options

Option	W3	W7	Power-Up Mode
0	IN	IN	PC at 24, PS = 26
1	IN	OUT	Micro-ODT, PS = 0
2	OUT	IN	PC at 173000, PS = 340
3	OUT	OUT	Users bootstrap, PS = 340

KDJ11-A Jumper Locations

Halt Option

The HALT option determines the action taken after a HALT instruction is executed in the kernel mode. At the end of a HALT instruction, the KDJ11-A checks BPOK before checking the HALT option. If BPOK is asserted, the KDJ11-A continues based on the status of the HALT option which is controlled by the W5 jumper. When the jumper is "removed", the KDJ11-A will trap to location 4 in the kernel data space and set bit <07> of the CPU Error register. If the jumper is "installed", the KDJ11-A enters the micro-ODT mode. If BPOK is negated, the option is not recognized and the KDJ11-A loops until BPOK is asserted and the power-up sequence is initiated.

Boot Address

The boot address jumpers select the starting address for the user's bootstrap program when power-up option 3 is selected. The state of the highest four bits, <15:12> are determined by jumpers W1, W2, W4, and W6, respectively. A bit will be set (1) when the respective jumper for that bit is "installed" and the bit will be read as a zero when the jumper is "removed". During the power-up sequence, the KDJ11-A reads the address determined by bits <15:12> and forces the remaining bits to read as zeros. Therefore, the user's bootstrap program can reside on any 2048 word boundary.

Wakeup Disable

The KDJ11-A module has an on-board wakeup circuit to properly sequence the BDCOK signal. When jumper W8 is "removed", the wakeup circuit is enabled and the module will properly sequence the BDCOK signal. The wakeup circuit is disabled when W8 is "installed" and external logic must be used to properly sequence the BDCOK signal.

BEVNT Recognition

The LSI-11 bus signal BEVNT provides an external event interrupt request to the KDJ11-A. Recognition of BEVNT is disabled when the W9 jumper is "installed". This disables the operation of the Line Time Clock register. When the jumper is "removed", the BEVNT input is recognized and is under control of the Line Time Clock register.

Factory Configuration

The factory or shipped configuration is described below. The user should review these features and reconfigure if it is necessary.

Factory Configuration

Jumper	Status	Function
W9	OUT	BEVNT register enabled
W8	OUT	Wakeup circuit enabled
W7	IN	Power-up option 2
W6	IN	Bit <12> set (1)
W5	OUT	HALT traps to location 4
W4	IN	Bit <13> set (1)
W3	OUT	Power-up option 2
W2	IN	Bit <14> set (1)
W1	IN	Bit <15> set (1)

Diagnostic LEDs

The module has four LEDs that monitor the status of the module. The LEDs are designated as D1 through D4 and are located on the edge of the module as shown in the previous figure. The D1 LED is turned on only when the module is operating in the micro-ODT mode. The D2-D4 LEDs are used with the diagnostics run during the power-up sequence. These LEDs are turned on at the beginning of the sequence, and upon the successful pass of the diagnostic are turned off. Each LED monitors a primary function of the module as described below.

LED D1 — Micro-ODT is entered.

LED D2 — Module could not do a read and write transaction to the CPU Error register. This indicates the microcode is not running.

LED D3 — Module attempted to read location 17 777 560 and timed out. This indicates the console terminal is not responding.

LED D4 — Module attempted to read location 0 and timed out or attempted to read location 17 777 700 and did not time out. This indicates the memory system is not responding.

The LEDs can indicates the most probable failure when troubleshooting the system as described below.

Probable System Failure

D1	D2	D3	D4	Probable Failure
X	ON	ON	ON	CPU module
X	OFF	ON	ON	LSI-11 bus
X	ON	OFF	ON	CPU module
X	OFF	OFF	ON	LSI-11 bus or memory
X	ON	ON	OFF	CPU module
X	OFF	ON	OFF	SLU module
X	ON	OFF	OFF	CPU module
X	OFF	OFF	OFF	Console terminal