LA21 DEP 4000
LA200 SR = 4000 INIT RUN
HALTS A 0222
SET MD DISPLAY → CHECK AC = 7777 & LINK IS SET
PRESS RUN "DO NOT PRESS INIT"
HALT AT 1763 = GOOD PASS.

IDENTIFICATION

PRODUCT CODE: MAINDEC-08-DJKKA-B-D

PRODUCT NAME: PDP-8/A CPU TEST

DATE CREATED: FEBRUARY 15, 1975

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: MICHAEL J. HARE

TABLE OF CONTENTS

HOW TO USE THIS DOCUMENT FOR:

LOADING AND RUNNING THE DIAGNOSTIC

READ SECTION 3, THEN SEE SECTIONS 4.1 AND 4.2 FOR LOADING AND STARTING INFORMATION. THERE ARE SEVEN (7) PAPER TAPES ASSOCIATED WITH THIS PROGRAM:

MAINDEC-08-DJKKA-B-PB1 FIELD SERVICE/XOR 4K VERSION
MAINDEC-08-DJKKA-B-PM1 FIELD SERVICE 1K SEGMENT PART 1
MAINDEC-08-DJKKA-B-PM2 FIELD SERVICE 1K SEGMENT PART 2(I/O SIMULATOR REQUIRED)
MAINDEC-08-DJKKA-B-PB2 ACT-8/A 4K VERSION *
MAINDEC-08-DJKKA-B-PB3 ACT-8/A 1K SEGMENT PART 1 *
MAINDEC-08-DJKKA-B-PB4 ACT-8/A 1K SEGMENT PART 2 *
MAINDEC-08-DJKKA-B-PB5 ACT-8/E VERSION **

* WILL RUN ONLY IN CONJUNCTION WITH THE ACT-8/A INTERFACING PROGRAM AND THE ACT-8/A OPERATING SYSTEM.
** WILL RUN ONLY UNDER CONTROL OF THE ACT-8/E SYSTEM.

FINDING ERROR INFORMATION

SEE SECTION 5 FOR ERROR INFORMATION. CHECK SECTION 3 FOR POSSIBLE VIOLATION OF PROGRAM RESTRICTIONS.

XOR TROUBLESHOOTING

SEE SECTION 4.2.3 FOR XOR INITIALIZATION INSTRUCTIONS.

1. ABSTRACT

THE PDP-8/A INSTRUCTION TEST IS DESIGNED TO TEST ALL LOGIC ON THE 8/A CPU BOARD THAT IS TESTABLE BY THE USE OF PROGRAMMED INSTRUCTIONS. IN ORDER TO TEST LOGIC ON THE CPU BOARD THAT IS DIRECTLY CONCERNED WITH DATA BREAKS AND/OR INTERRUPTS, A SPECIAL SIMULATOR IS REQUIRED. THIS TEST WILL RUN IN ANY FIELD(SEE 2.2 BELOW), AND WILL POWER FAIL IF A POWER FAIL OPTION IS INSTALLED IN THE CPU.

2. REQUIREMENTS

2.1 HARDWARE

THE FOLLOWING HARDWARE IS REQUIRED FOR THE EXECUTION OF THE 8/A INSTRUCTION TEST:

PROCESSOR-PDP-8/A HEX CPU BOARD (SEE SECTION 3-B)

MEMORY-MIMIMUM 1K REQUIRED

OPTIONS- NONE REQUIRED

SPECIAL- PDP-8/A I/O SIMULATOR TO TEST I/O FUNCTIONS.

2.2 STORAGE

THE 8/A INSTRUCTION TEST USES LOCATIONS 0000 THRU 3777. SPECIAL RIM FORMAT BINARY TAPES ARE AVAILABLE TO ALLOW RUNNING THE TEST IN 1K OF MEMORY, BY EXECUTING THE TEST IN TWO CONSECUTIVE 1K SEGMENTS. IN THIS CASE ADDRESSES 0000 THRU 1777 ARE USED. WHEN RUNNING THE XOR VERSION OF THE TEST, LOCATIONS 0000 THRU 4177 ARE USED. THE 4K VERSION OF THIS TEST WILL RUN IN ANY FIELD, SO LONG AS THE LOCATIONS 00000 THRJ 00177, AND LOCATION 01777 EXIST AND ARE R/W MEMORY.

2.3 PREREQUISITE SOFTWARE

NO OTHER SOFTWARE IS NECESSARY TO TEST THE 8/A CPU BOARD.

3. RESTRICTIONS

THE FOLLOWING RESTRICTIONS APPLY TO THE 8/A INSTRUCTION TEST:

A. 1K TO 3K MACHINES-SPECIAL RIM FORMAT PAPER TAPES ARE REQUIRED TO RUN THIS TEST IN MACHINES WITH LESS THAN 4K OF MEMORY. SEE SECTION 4.1.2.

B. TRADITIONAL PDP-8 COMPUTERS - THIS TEST IN NON-OPERATIONAL ON PDP-8, PDP-8/I, PDP-8/L, PDP-12, AND PDP-8/S COMPUTERS. THIS TEST IS OPERATIONAL ON PDP-8/E, PDP-8/F, AND PDP-8/M COMPUTERS. (SEE SECTION 4.2.1 FOR INITIALIZATION)

C. INTERRUPTS - NO INTERRUPTS EXCEPT POWER FAIL AND THOSE FROM THE DATA BREAK/INTERRUPT SIMULATOR ARE PERMITTED.

D. MACHINES WITH PROGRAMMER'S CONSOLE - TO RUN PART 2 OF THIS TEST (USING THE I/O SIMULATOR), IN A MACHINE WITH A PROGRAMMER'S CONSOLE INSTALLED, THE DISPLAY MUST BE SET FOR THE "MD", "STATE", OR "STATUS" OR AN ERROR HALT WILL OCCUR.

E. DEVICE CODE "77" - IN ORDER TO COMPLETELY TEST ROM H, IT IS NECESSARY TO EXECUTE AN IOT INSTRUCTION WITH BIT 3 OF THE IOT A "1". E.G. 64XX, 65XX, 66XX, 67XX. THE IOT INSTRUCTION USED BY THE TEST IS 6770. IF THIS IOT CONFLICTS WITH A DEVICE ON THE SYSTEM UNDER TEST, DISCONNECT THE DEVICE FROM THE MACHINE WHILE RUNNING PART 2 OF THIS TEST.

F. IT IS RECOMMENDED THAT THE PROGRAM BE RELOADED AFTER AN ERROR HAS BEEN DETECTED.

G. NO OTHER DATA BREAK OR INTERRUPT DEVICE MAY BE OPERATING ON THE CPU WHILE RUNNING PART TWO OF THIS TEST WITH THE PDP-8/A I/O SIMULATOR.

H. IN ORDER TO RUN PART 2 OF THIS TEST IN A CPU THAT CONTAINS A TIME SHARE OPTION(M837 ONLY), THE TIME SHARE OPTION MUST BE DISABLED AS IT MAY CAUSE UNEXPECTED INTERRUPTS.

4. STANDARD TEST PROCEDURE

4.1 PROGRAM LOADING PROCEDURE

4.1.1 4K TO 32K MACHINES

FOR MACHINES WITH 4K TO 32K OF MEMORY THE STANDARD BINARY LOADER TECHNIQUE IS USED. USE PAPER TAPE 08-DJKKA-PB1.

4.1.2 1K TO 3K MACHINES

THE INSTRUCTION TEST IS SEGMENTED INTO TWO (2) 1K SEGMENTS THAT MAY BE RUN CONSECUTIVELY IN A 1K MACHINE. THE 1K SEGMENTS ARE PUNCHED ON TWO RIM FORMAT PAPER TAPES LABELED 08-DJKKA-PM1 AND PM2. SEGMENT 1 SHOULD ALWAYS BE RUN PRIOR TO SEGMENT 2. TO LOAD EITHER SEGMENT PERFORM THE FOLLOWING STEPS:

NOTE: THE SECOND 1K SEGMENT IS ONLY FOR USE WITH AN 8/A I/O SIMULATOR. IF NO SIMULATOR IS AVAILABLE, THE SECOND 1K SEGMENT SHOULD NOT BE RUN.

A. DEPOSIT THE FOLLOWING INSTRUCTIONS INTO PAGE ZERO:

ADDRESS	CONTENTS (HIGH SPEED)	(LOW SPEED)
0156	6014	6032
0157	6011	6031
0160	5357	5357
0161	6016	6036
0162	7106	7106
0163	7006	7006
0164	7510	7510
0165	5374	5357

0166	7006	7006
0167	6011	6031
0170	5367	5367
0171	6016	6034
0172	7420	7420
0173	3776	3776
0174	3376	3376
0175	5357	5356

B, PLACE RIM TAPE IN READER ON LEADER PORTION OF TAPE.

C, LOAD ADDRESS 0156, INIT AND CONTINUE.

D, HALT COMPUTER WHEN ENTIRE TAPE HAS BEEN READ IN.

NOTE: WHEN RUNNING THE SECOND 1K SEGMENT, ADD 2000 TO THE ADDRESS OF ANY ERROR HALTS BEFORE CONSULTING THE LISTING.

4.2 PROGRAM RUN PROCEDURE

4.2.1 INITIALIZATION

IF NO INITIALIZATION IS PERFORMED, THE PROGRAM WILL ASSUME THAT NO PROGRAMMER'S CONSOLE OR I/O SIMULATOR IS AVAILABLE.

PERFORM THE FOLLOWING INITIALIZATION FOR OTHER CONFIGURATIONS:

A, MACHINES WITH PROGRAMMER'S CONSOLE

1) LOAD ADDRESS 0021,
2) SET SR0=1 TO INDICATE A PROGRAMMER'S CONSOLE IS AVAILABLE,
3) SET SR3=1 IF A CPU I/O SIMULATOR IS AVAILABLE,
4) SET SR5=1 IF RUNNING THE XOR VERSION,
5) SET SR6=1 IF THE PROCESSOR IS A PDP-8/E FAMILY COMPUTER, (PDP8-E,F, OR M)
6) DEPOSIT
7) PROGRAM IS NOW INITIALIZED

B, MACHINES WITHOUT PROGRAMMER'S CONSOLE

NOTE: ADDRESS 0021 IS ALREADY INITIALIZED TO INDICATE NO PROGRAMMER'S CONSOLE.

1) IF NO PROGRAMMER'S CONSOLE IS AVAILABLE, USE ANY MEANS AVAILABLE TO INITIALIZE LOCATION 21 AS DESCRIBED IN (A,) ABOVE.
2) IF RUNNING THE 2K VERSION, OR THE FIRST 1K SEGMENT, INITIALIZE LOCATION 0221 TO A 7000, TO PREVENT THE INITIAL HALT.
3) START PROGRAM AT LOCATION 0200.

4.2.2 PROGRAM START

TO START THE TEST, DO THE FOLLOWING:

A, PERFORM INITIALIZATION IF NECESSARY, SEE SECTION 4.2.1.
B, LOAD ADDRESS 0200
C, MAKE SR SETTINGS IF DESIRED, SEE SECTION 6.
D, DEPRESS INIT, THEN CONTINUE
E, COMPUTER SHOULD HALT WITH MA=0222, AC=7777, AND LINK=1.

F, VERIFY THAT THE PC, AC, AND LINK ARE CORRECT. IF THEY ARE CORRECT, PROCEED TO STEP G. IF THEY ARE INCORRECT, REFER TO "ERRORS" SECTION 5.1,
G, SET FRONT PANEL INDICATE SWITCH TO "MD", "STATE", OR "STATUS" POSITION.
H, DEPRESS CONTINUE. !!!! DO NOT DEPRESS INIT. !!!!
I, THE COMPUTER SHOULD RUN CONTINUOUSLY, UNLESS AN ERROR IS DETECTED, OR UNLESS SR3=1, (SEE SECTION 6).

4.2.3 XOR VERSION

THE 2K (STANDARD) VERSION OF THIS TEST CONTAINS ALL NECESSARY CODE TO ALLOW THIS PROGRAM TO RUN ON THE POP-8/A XOR TESTER. TO RUN THE XOR VERSION, INITIALIZE LOCATION 0021 AS DESCRIBED IN SECTION 4,2,1, THEN START AT LOCATION 0200. AFTER THE FIRST PASS THRU THE DIAGNOSTIC, THE PROGRAM WILL BE MODIFIED FOR XOR TESTING. THE DEVICE CODE SWITCHES ON THE XOR SHOULD BE SET TO 00 WHEN RUNNING THIS TEST.

NOTE: 1K SEGMENTS OF THIS PROGRAM DO NOT CONTAIN XOR CODE.

4.2.4 ACT-8/A VERSION

THE ACT-8/A VERSION OF THIS PROGRAM IS A SPECIALLY MODIFIED VERSION OF THE BASIC PROGRAM. THE DIFFERENCES BETWEEN THE STANDARD VERSION AND THE ACT-8/A VERSION ARE AS FOLLOWS:

A, ALL ERROR HALTS ARE REPLACED WITH A "JMS SUBROUTINE" IN THE ACT-8/A VERSION, THIS SUBROUTINE GETS THE PC OF THE ERROR AND DOES A JMP TO LOCATION 76520 TO NOTIFY THE ACT-8/A MONITOR OF THE PROGRAM DETECTED ERROR,

B, AT THE END OF EACH SUCCESSFUL PASS OF THE TEST, THE PROGRAM DOES A JMS TO LOCATION 76500 TO NOTIFY THE ACT-8/A MONITOR OF THE SUCESSFUL PASS, RETURN IS MADE TO THE PROGRAM FROM THE MONITOR AND TESTING RESUMES, TESTING WILL CONTINE WITH THE MONITOR BEING NOTIFIED OF EACH SUCCESSFUL PASS UNTIL EITHER AN ERROR OCCURS OR THE MONITOR LOADS ANOTHER PROGRAM,

C, XOR CODE IS NOT IMPLEMENTED IN THE ACT-8/A VERSION,

D, THE ACT-8/A VERSION HAS THREE BINARY TAPES:

MD-08-DJKKA-PB2 4K VERSION
MD-08-DJKKA-PB3 1K SEGMENT PART 1
MD-08-DJKKA-PB4 1K SEGMENT PART 2

THESE THREE PROGRAMS ARE THE EQUIVALENT OF THE THREE FIELD SERVICE VERSIONS, WITH THE EXCEPTION OF THE DIFFERENCES NOTED ABOVE,

4.2.5 ACT-8/E VERSION

THE ACT-8/E VERSION OF THIS TEST IS A SPECIALLY MODIFIED VERSION OF THE BASIC 2K PROGRAM, USE PAPER TAPE DJKKA-PB5, THE DIFFERENCES BETWEEN THE ACT-8/E VERSION AND THE BASIC 2K VERSION ARE AS FOLLOWS:

A, ALL ERROR HALTS ARE REP[illegible]ED WITH A "JMS S[illegible]OUTINE" IN THE ACT-8/E VERSION, THE S[illegible]UTINE NOTIFIES T[illegible]ACT-8/E MONITOR

OF THE ERROR.

B. IF BIT2 OF LOCATION 0022 = 1, THEN AFTER ONE PASS THROUGH THE TEST THE ACT-8/E MONITOR IS NOTIFIED OF THE GOOD PASS AND PROGRAM EXECUTION CEASES.

C. IF BIT2 OF LOCATION 0022 = 0, THE PROGRAM RUNS FOR 10 MINUTES (AS TIMED IN A CORE MEMORY MACHINE), AT THE END OF TEN MINUTES THE ACT-8/E MONITOR IS NOTIFIED OF A GOOD PASS.

D. XOR CODE IS NOT IMPLEMENTED IN THE ACT-8/E VERSION.

E. POWER FAIL IS NOT IMPLEMENTED IN THE ACT-8/E VERSION.

F. THE ACT-8/E VERSION RUNS ONLY IN FIELD 0.

5. ERRORS

5.1 ERROR HALTS

ALL PROGRAM ERRORS ARE INDICATED BY MEANS OF ERROR HALTS. THE PROGRAM LISTING CONTAINS A BRIEF EXPLANATION OF THE ERROR TO THE RIGHT OF EACH HALT IN THE LISTING. USE THE PC CONTENTS AFTER THE ERROR HALT TO FIND THE ERROR INFORMATION IN THE LISTING.

NOTE: IF RUNNING THE 2ND 1K SEGMENT IN A 1K CPU, ADD 2000 TO THE ADDRESS OF ANY ERROR HALT BEFORE CONSULTING THE LISTING.

THE FOLLOWING ERRORS HAVE BEEN INCLUDED HERE, BECAUSE THEY REQUIRE FURTHER EXPLANTION:

PC=0036 THIS INDICATES THAT AN UNEXPECTED INTERRUPT WAS RECEIVED BY THE CPU. LOCATION 0000 WILL CONTAIN THE ADDRESS+1 OF WHERE THE PROGRAM WAS INTERRUPTED. E.G. IF LOCATION 0000 CONTAINS 2635, THEN THE COMPUTER WAS INTERRUPTED AFTER THE INSTRUCTION AT LOCATION 2634.

PC=0221 THIS IS NOT AN ERROR HALT UNLESS THE AC IS NOT EQUAL TO 7777 OR THE LINK IS NOT EQUAL TO 1. IF THE AC OR THE LINK IS INCORRECT, LOAD ADDRESS 0200, DEPRESS THE HALT KEY, AND DEPRESS CLEAR MOMENTARILY. THE PROGRAM MAY NOW BE EXECUTED ONE INSTRUCTION AT A TIME BY DEPRESSING THE CONTINUE KEY. THE OPERATOR SHOULD CHECK THE CONTENTS OF THE AC AND LINK AGAINST THE EXPECTED CONTENTS GIVEN IN THE PROGRAM LISTING AFTER EXECUTING EACH INSTRUCTION. WHEN AN INSTRUCTION IS EXECUTED AND THE COMPUTER REGISTERS NO LONGER AGREE, THE FAILING INSTRUCTION HAS BEEN FOUND.

PC=1631 A SKIP ERROR OCCURED DURING THE TEST OF ROMS "D" AND "F". THE INSTRUCTION IN THE AC WAS EXECUTED, AND RESULTED IN A SKIP WHEN NONE WAS EXPECTED, OR DID NOT SKIP WHEN IT WAS EXPECTED TO SKIP. MAKE A NOTE OF THE INSTRUCTION, THEN DEPRESS CONTINUE TO GET THE CONTENTS OF THE AC, MQ AND LINK AT THE TIME OF THE FAILURE. TO EXECUTE THE FAILING INSTRUCTION AGAIN, DEPRESS CONTINUE. TO EXECUTE THE NEXT INSTRUCTION (OR NEXT DATA PATTERN WITH SAME INSTRUCTION), MAKE A NOTE OF THE AC, LINK, AND MQ CONTENTS FOR REFERENCE, THEN LOAD ADDRESS 1673, DEPRESS

CLEAR , THEN CONTINUE. IF FURTHER ERROR HALTS OCCUR, THE ERROR INFORMATION SHOULD BE RECORDED FOR USE IN DETERMINING A PATTERN FOR THE FAILURE, (E.G, CLL CML COMBINATION SKIPS, SPA SNA WON'T SKIP IF LINK IS SET, ETC.)

PC=1650 A DATA ERROR OCCURRED DURING THE TEST OF ROMS "D" AND "F", THE INSTRUCTION IN THE AC WAS EXECUTED, AND RESULTED IN INCORRECT CONTENTS OF THE AC, MQ, OR LINK. MAKE A NOTE OF THE INSTRUCTION, THEN DEPRESS CONTINUE TO GET THE EXPECTED CONTENTS OF THE AC, LINK, AND MQ. MAKE A NOTE OF THE EXPECTED CONTENTS, THEN DEPRESS CONTINUE TO GET THE CONTENTS OF THE AC, MQ, AND LINK AS THEY WERE FOUND AFTER THE INSTRUCTION WAS EXECUTED. TO EXECUTE SAME INSTRUCTION AGAIN DEPRESS CONTINUE, TO EXECUTE NEXT INSTRUCTION, OR NEXT DATA PATTERN FOR SAME INSTRUCTION, LOAD ADDRESS 1673, CLEAR AND CONTINUE. IF FURTHER ERRORS OCCUR, THE ERROR INFORMATION SHOULD BE RECORDED FOR USE IN FINDING A POSSIBLE PATTERN IN THE ERROR, E.G. CLL CMA CML COMBINATION DOES NOT WORK CORRECTLY.

PC=ALL OTHER HALTS REFER TO PROGRAM LISTING UNDER PROPER PC.

5.1.2 LOOPING ON ERROR

NOTE: DISREGARD THIS INFORMATION WHEN RUNNING THE XOR VERSION. XOR LOOPING IS AUTOMATIC.

TO LOOP ON A FAILING INSTRUCTION, (OTHER THAN ROM "D" & "F" TEST), IT IS NECESSARY TO DEPOSIT A JUMP INSTRUCTION IN PLACE OF THE ERROR HALT THAT IS OCCURING. THE JUMP INSTRUCTION SHOULD CAUSE THE PROGRAM TO JUMP BACK TO THE POINT WHERE THE FAILING INSTRUCTION IS EXECUTED. NOTE: IF SPECIAL CONDITIONS ARE REQUIRED (E.G, AC & LINK MUST BE CLEAR, AC MUST BE EQUAL TO 7777, ETC) THE OPERATOR WILL HAVE TO DEPOSIT THE PROPER INSTRUCTIONS TO CAUSE THESE CONDITIONS PREVIOUS TO THE FAILING INSTRUCTION, AND MAKE THE JMP AFTER THE FAILING INSTRUCTION JUMP ACCORDINGLY.

EXAMPLE:

```
ADDRESS         CONTENTS        MNEMONIC

0361            1024            TAD K1          /AC TO 0001 LINK=1
0362            1054            TAD K7777       /AC TO 0000 LINK TO 0
0363            7450            SNA             /SHOULD NOT SKIP IF AC=0000
0364            7430            SZL             /SHOULD SKIP IF LINK=0
0365            7402            HLT             /CARRY FAILED TO PROPAGATE THRU ADDER
```

IF THE PROGRAM IS HALTING AT ADDRESS 0365 WITH THE AC NON-ZERO, ONE OR BOTH OF THE TAD INSTRUCTIONS ARE FAILING, IN ORDER TO LOOP ON THE FAILING INSTUCTIONS, A JUMP TO THE FIRST TAD INSTRUCTION (LOCATION 0361) COULD BE PLACED AT LOCATION 0365, BUT THE AC WOULD NOT BE CLEAR, AND THE LINK WOULD NOT BE SET WHEN THE FIRST TAD IS EXECUTED. IN ORDER TO LOOP CORRECTLY, THE FOLLOWING PATCH IS REQUIRED TO SET THE AC AND LINK TO THE PROPER VALUES. "*" INDICATES INSTRUCTIONS THAT WERE DEPOSITED FOR LOOPING PURPOSES.

```
ADDRESS         CONTENTS        MNEMONIC

0360*           7320            CLA CLL CML     (CLEAR AC, SET LINK)
0361            1024            TAD K1
0362            1054            TAD K7777
0363            7450            SNA
0364            7430            SZL
0365*           5360            JMP .-5         (FAILED, DO AGAIN)
0366*           7402            HLT             (DID NOT FAIL)
```

THE LOOP SHOULD BE EXECUTED THE FIRST TIME DOING ONE INSTRUCTION AT A TIME WITH HALT/SS SELECTED, TO INSURE THAT THE INSTRUCTION IS STILL FAILING, AND THAT ANY INSTRUCTIONS INSERTED (IN THE ABOVE EXAMPLE THE JMP .-5, AND THE CLA CLL CML) ARE NOT ALSO FAILING.

IN ORDER TO RUN THE PROGRAM AGAIN AFTER REPAIRS HAVE BEEN MADE, A RELOAD OF THE PROGRAM IS REQUIRED.

5.2 ERROR PRINTOUTS

NO ERROR PRINTOUTS ARE USED BY THIS TEST, ALL ERRORS ARE INDICATED BY PROGRAM HALTS.

6. SWITCH REGISTER SETTINGS

6.1 NORMAL OPERATING SWITCHES

MACHINES WITH PROGRAMMER'S CONSOLE SHOULD INITIALIZE THE PROGRAM TO USE THE PROGRAMMER'S CONSOLE SWITCH REGISTER, (SEE SECTION 4.2.1). MACHINES WITHOUT PROGRAMMER'S CONSOLE USE LOCATION 0020 IN LIEU OF A SWITCH REGISTER. REGARDLESS OF WHETHER THE PROGRAMMER'S CONSOLE SWITCH REGISTER OR ADDRESS 0020 IS USED, THE BITS HAVE THE FOLLOWING PURPOSES:

BIT	FUNCTION WHEN 0	FUNCTION WHEN 1
0-2	NOT USED	NOT USED
3	LOOP ON COMPLETE TEST	HALT AT END OF TEST
4-11	NOT USED	NOT USED

6.2 ERROR SWITCHES

NO ERROR SWITCHES ARE PROVIDED, SEE SECTION 5.1.2 FOR ERROR LOOPING PROCEDURE

7. REVISIONS

THE "B" REVISION WAS RELEASED TO DELETE THE "LOAD ADDRESS" TEST WHICH COULD CAUSE MARGINAL (BUT LEGAL) FAILURES, CERTAIN TESTS WERE ALSO ADDED TO CATCH FAILURES THAT WERE NOT CAUGHT IN THE FAULT INSERTION OF THE "A" REVISION. THE "B" VERSION OF THE SOURCE ALSO SUPPORTS AN ACT-8/E VERSION.

8. PROGRAM DESCRIPTION

8.1 BASIC INSTRUCTION TESTS

DURING THE FIRST PORTION OF THE TEST, ALL BASIC GROUP 1 AND GROUP 2 OPERATE INSTRUCTIONS ARE TESTED. NO COMBINED OPERATES ARE TESTED EXCEPT CLA CLL. THEN ALL MRI INSTRUCTIONS ARE TESTED, USING BOTH DIRECT AND INDIRECT ADDRESSING. DURING THIS SECTION THE ADDER IS TESTED BY THE USE OF TAD INSTRUCTIONS AND IAC. FINALLY BASIC GROUP 3 OPERATE INSTRUCTIONS ARE TESTED.

8.2 TEST OF ROMS "D" AND "F"

ROMS "D" AND "F" ON THE CPU MODULE ARE TESTED BY EXECUTING ALL GROUP 1,2, AND 3 OPERATE INSTRUCTIONS OF THE FORM: 7XXØ, 7XX1. FOR EACH INSTRUCTION THUS TESTED, 8 DIFFERENT DATA COMBINATIONS OF AC,MQ, AND LINK ARE USED, THE SEQUENCE OF ROM TESTING IS AS FOLLOWS:

A. THE AC, LINK, AND MQ ARE SET TO SPECIFIED VALUES.
B. THE INSTRUCTION TO BE TESTED IS EXECUTED.
C. THE AC, LINK, AND MQ ARE SAVED, AND WHETHER THE INSTRUCTION SKIPPED IS NOTED.
D. THE AC, LINK, AND MQ ARE SET TO THE SAME VALUES AS IN STEP A.
E. THE INSTRUCTION IS SIMULATED USING ONLY THOSE INSTRUCTIONS THAT WERE TESTED DURING THE FIRST PART OF THE TEST. (BASIC OPERATE AND MRI INSTRUCTIONS)
F. THE RESULTS OF THE SIMULATION ARE COMPARED TO THE RESULTS OF THE ACTUAL INSTRUCTION. ANY DIFFERENCES RESULT IN AN ERROR HALT.

8.3 DATA BREAK/INTERRUPT TESTING

THE LOGIC ON THE CPU BOARD CONCERNED WITH DATA BREAKS AND INTERRUPTS IS TESTED BY THE USE OF A SPECIAL SIMULATOR. I/O SKIPS, AC TRANSFERS, INTERRUPTS, INDICATE LOGIC, AND DATA BREAKS ARE TESTED IF THE SIMULATOR IS AVAILABLE. ALL OMNIBUS LINES ARE TESTED EITHER DIRECTLY OR INDIRECTLY WITH THE EXCEPTION OF "NEXT TIME STATE STALL" (BR2) AND THE UNUSED OMNIBUS LINE(BS2).

8.4 UNTESTED LOGIC

DUE TO CERTAIN HARDWARE RESTRICTIONS, SOME LOGIC ON THE PDP-8/A CPU BOARD IS NOT TESTED BY THIS PROGRAM. BELOW IS A LIST OF LOGIC THAT IS KNOWN TO BE UNTESTED.

ROM A - ADDRESSES ØØ THRU Ø3 (EXTENDED LOAD ADDRESS 7)
ADDRESSES Ø4 THRU Ø7 (EXTENDED LOAD ADDRESS)
ADDRESSES 14 THRU 17 (LOA