INSTRUCTION MANUAL

DATA COMMUNICATION CHANNEL DP01A

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-08-I8BA-D

DATA COMMUNICATION CHANNEL
DP01A

INSTRUCTION MANUAL
FOR USE WITH PDP-8

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

This manual provides general information, installation, operation, programming, maintenance, and technical reference data for the DP01A Bit Synchronous Data Communication Channel manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

The DP01A is an interface between the PDP-8 computer and a full-duplex serial asynchronous modem communication link having interface characteristics compatible with Electronics Industries Association (EIA) Standard RS-232B.

The DP01A consists of two basic assemblies, a control section and a computer interface section. The Type 637 control section performs serial-to-parallel and parallel-to-serial conversion and data set control. The interface section adapts the 637 to the input/output bus of the PDP-8 computer. (With another interface, the 637 can also be used with other computers.)

An XOR option adds a non-memory reference XOR command to the PDP-8, to facilitate special character detection and longitudinal message parity generation.

Other publications that contain information pertinent to the DP01A or related equipment are listed in Table 1-1.

Table 1-1
Reference Documents

Document Number	Title
C-105	Digital Logic Handbook
F-85	PDP-8 User Handbook
F-87	PDP-8 Maintenance Manual
RS-232B*	EIA Standard: Interface between Data Processing Terminal Equipment and Data Communication Equipment
Maindec-08-D8KA-D	DP01A IOT and Data Test
Maindec-08-D8FA-D	DP01A Bit Synchronous Data Communication System IOT and Data Test

*Published by Engineering Department, Electronic Industries Association.

1.1 FUNCTIONAL DESCRIPTION

The DP01A (Figure 1-1) consists of two independent serial channels controlled by programmed IOT instructions from the PDP-8, and synchronized by timing pulse streams from the associated data set. (Timing can optionally be generated within the DP01A.)

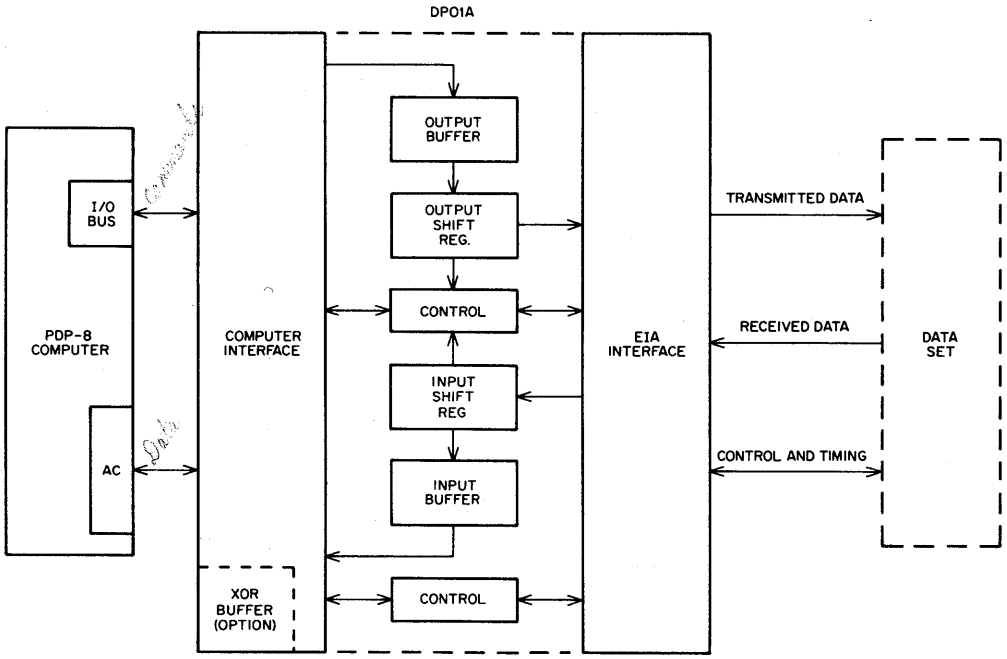


Figure 1-1 DP01A Synchronous Data Channel

Output characters are transferred in parallel from the computer to a buffer register, then serially shifted to the data set communication terminal. Input characters from the data set are shifted into a register, transferred to a buffer register, and made available to the PDP-8 on an interrupt basis. Double buffering, both on input and output, allows a full character time in which to coordinate the program and the real-time data. Control of the communication terminal is also through programmed IOT commands.

Synchronization between the DP01A and the distant data set is established by a sync character code. Once a sync character is detected, a receiving channel assembles every 6, 7, 8, or 9 successive bits to form a character.

1.1.1 Data Format

Serial data is transmitted and received continuously once synchronization is achieved. The transmission format consists of sync characters (three in succession are recommended) followed by the characters which make up the text of the message. Character lengths of 6, 7, 8, or 9 bits are selected by a prewired patch plug, to allow the DP01A to communicate with remote sites at various word lengths. Sync characters provide a time reference at the start of every message to enable a receiving terminal to determine which successive bits in the incoming serial stream make up each character. When a receiving terminal recognizes a sync character, it assembles every Nth bit in a buffer (N=6, 7, 8, or 9). Sync characters employed by the DP01A are:

Bits Per Character	Sync Characters
6	010 110
7	0 010 110
8	10 010 110
9	010 010 110

A brief message using 9-bit characters is illustrated in Figure 1-2.

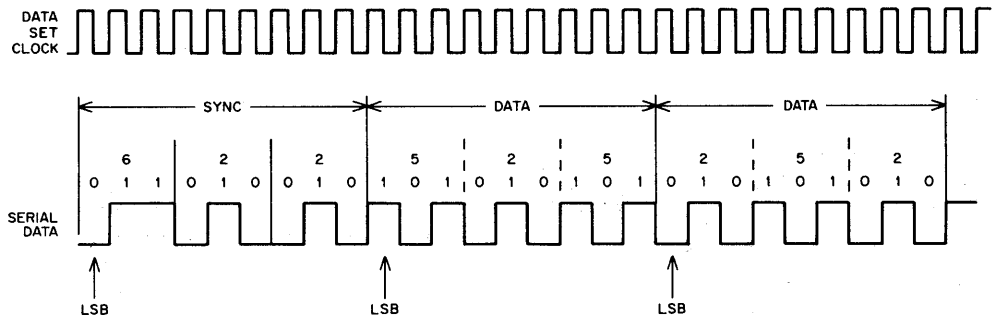


Figure 1-2 DP01A Serial Message Format (9-Bit Characters)

1.2 SPECIFICATIONS

Specifications for the DP01A are summarized in Table 1-2.

Table 1-2
DP01A Summary of Specifications

Type of Channel	Serial synchronous, half or full duplex
Speed	Up to 50,000 baud
Interface	Conforms to EIA Standard RS-232B
Data Format	6, 7, 8, or 9-bit serial characters selected by pre-wired plug-in connector; unique sync character code for each character length; least significant bit is transmitted first.
Compatible Data Sets	Type / Speed (Baud) Bell 201A / 2K Bell 201B / 2400 Bell 205B / 600,1200, 1800

Table 1-2 (cont)
DP01A Summary of Specifications

Compatible Data Sets (cont)	Type		Speed (Baud)
	Rixon	FM-12	1200
	Rixon	Sebit 48	4800
	GE	TDM Series	2400
	Lenkurt	26C	150-2400

CHAPTER 2

INSTALLATION

2.1 MECHANICAL ASSEMBLY

The DP01A logic is divided into a control section and an interface section, each occupying one Type 1943 standard DEC mounting panel (see Figure 2-1). The logic mounting panels may be installed in any standard 19-in. rack assembly, such as the DEC CAB-3 option cabinet.

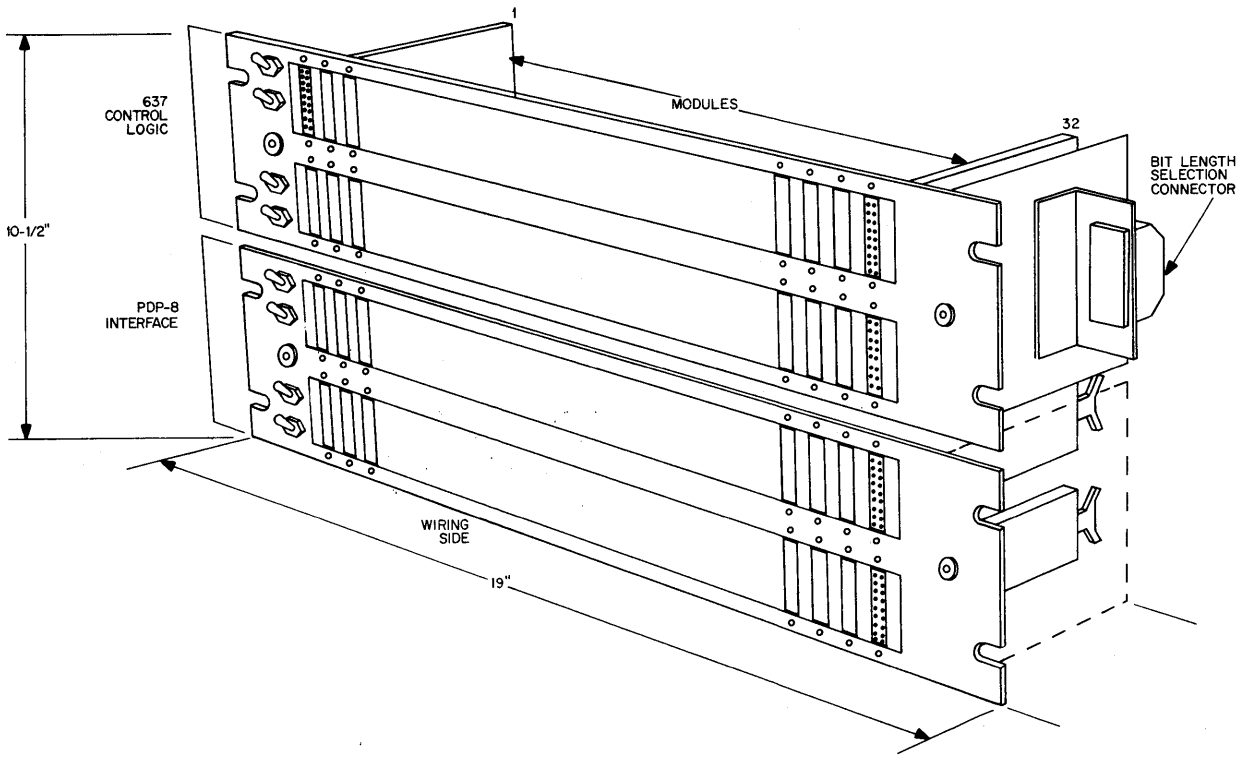


Figure 2-1 DP01A Physical Layout

2.1.1 Cabling

The control and interface panels are connected together and to the computer I/O bus by plug-in ribbon cables, for installation flexibility. Additional connector sockets are provided for extension of the I/O bus to other options.

Connections to the associated data set are through a 25-ft interconnecting cable terminated by a Cinch or Cannon DB-19604-432 (DB25-P) hooded connector.

System cabling is shown in drawing number D-IC-637-0-12 in Chapter 7 of this manual.

2.1.2 Module Locations

Connector slot assignments for logic and cable modules are shown on the Module Utilization Diagrams, drawing numbers D-MU-637-0-8 and D-MU-637-0-11, supplied in Chapter 7.

2.2 POWER

The DP01A usually obtains dc power directly from the +10 and -15V power supplies of the PDP-8. (In most PDP-8 systems the existing power supplies have adequate reserve power to operate the DP01A without an additional power source.) Current demand, for system planning purposes, is as follows.

Power Supply Current	
-15V	+10V
105 mA	2.24A

2.3 EIA INTERFACE

The DP01A EIA Line Interface shown in drawing number D-BS-637-0-3 (Chapter 7) consists of level-conversion modules and an interconnecting cable for direct connection to a data set. Characteristics of the interface signals are summarized below.

Request to Send - This signal is under control of the DP01A. It is turned ON when the first sync character of a message is loaded and is held ON throughout transmission. When transmission is completed, this output is turned OFF under program control. The SERIAL CLOCK TRANSMIT signal must be available from the data set in order to turn this line on or off.

Transmitted Data - Serial data is presented to the data set on this output. A positive polarity (+6V) represents a binary 0, or space, and a negative polarity (-6V) represents a binary 1, or mark. Between transmissions, the line is held in the marking (-6V) condition.

Local Timing - This optional output is used only when data set timing is supplied from the DP01A. The output is obtained from a R405 crystal clock module.

Data Terminal Ready - This output controls connection of the data set signal converter to the communication channel. (For a detailed description refer to EIA STD RS-232B.)

Serial Clock Transmit - This square wave signal from the data set synchronizes DP01A output data with the data set transmitter timing. When DP01A internal timing is used, the LOCAL TIMING signal is returned to the DP01A, under data set control as SERIAL CLOCK TRANSMIT.

Serial Clock Receive - This square wave signal from the data set is similar to the SERIAL CLOCK TRANSMIT signal, but is synchronized with the data set receiver timing circuits.

Data Set Ready - This input is ON at all times when the data set is prepared to send or receive data. When OFF, the line indicates that the data set is not in an operative condition.

Clear to Send - This input is OFF when the data set is activated but not in the transmitting state. The line turns ON approximately 150 ms after the DP01A generates a REQUEST TO SEND signal. (During this delay, a line echo suppressor operates and the distant receiver establishes carrier synchronization.)

Received Data - Incoming serial data from the data set is received by the DP01A at this input. A positive polarity indicates a binary 0, negative polarity a binary 1.

Ring Indicator - When ON, this input indicates that a ringing signal is being received by the data set from a remote station.

CHAPTER 3
OPERATION

The DP01A has no operating controls except the marginal check switches described in Chapter 6. Operation is automatic, under control of the PDP-8 program and the timing signals from the associated data set.

The only other operator function is installing a character-length-selection connector in the receptacle on a bracket at the right side of the control logic assembly. Connectors for 6, 7, 8, and 9-bit characters are supplied with the equipment and are labeled accordingly. Wiring details are shown in drawing number D-AR-637-0-9.

CHAPTER 4
PROGRAMMING

4.1 IOT COMMANDS

The following IOT commands are assigned to the DP01A.

Instruction	Octal Code	Description
Skip on Transmit Flag (STF)	6611	Causes the program to skip the next instruction if the Transmit Flag is in the 0 state. When the Transmit Flag is in the 1 state, the transmit buffer register is ready to accept another character.
Clear Transmit Flag (CTF)	6602	Resets the Transmit Flag. If Transmit Active Flag is not set, CTF also causes the program to skip the next instruction.
Transmit a Character (TAC)	6601	Causes the contents of the PDP-8 accumulator (6,7,8, or 9 bits right-justified) to be transferred into the transmit buffer register.
Clear Idle Mode (CIM)	6604	Resets the transmit logic Idle Mode flip-flop.
Set Idle Mode (SIM)	6614	Sets the transmit Idle Mode flip-flop.
Skip on Receive Flag (SRF)	6651	Causes the program to skip the next instruction if the Receive Flag is not set. (The Receive Flag is set when the first incoming sync character is detected, and stays set until the Receive End Flag is set.)
Read Receive Buffer (RRB)	6612	Transfers the contents of the Receive Buffer (6, 7, 8, or 9 bits right-justified) to the PDP-8 accumulator. RRB also resets the Receive Flag.
Skip on Receive End Flag (SEF)	6621	Causes the program to skip the next instruction if the Receive End Flag is not set. (The Receive End Flag flip-flop is set when the receive logic has stopped receiving serial data from the communications equipment due to termination of the SERIAL CLOCK RECEIVE pulse train.)
Clear End Flag (CEF)	6622	Resets the Receive End Flag.
Set Ring Enable (SRE)	6624	Set the Ring Enable flip-flop which permits the Ring Flag to request a program interrupt.
Clear Ring Enable (CRE)	6644	Resets the Ring Enable flip-flop.

Instruction	Octal Code	Description
Skip on Ring Indicator (SRI)	6631	Causes the program to skip the next instruction if the Ring Flag is not set. The Ring Flag is set when a RING input is received from the data set.
Clear Ring Flag (CRF)	6632	Resets the Ring Flag.
Set Terminal Ready (STR)	6634	Sets the Terminal Ready flip-flop. (See description of DATA TERMINAL READY interface signal.)
Clear Terminal Ready (CTR)	6642	Resets the Terminal Ready flip-flop.
Skip on Data Set Ready (SSR)	6641	Causes the program to skip the next instruction if the communications equipment is in the "ready" state. (See description of the DATA SET READY interface line.)
Clear Receiver Active (CRA)	6652	Resets the Receive Active flip-flop, taking the receive logic out of the "active" state. No more incoming characters are transferred to the receive buffer register until another sync character is detected.

The following commands pertain to the Exclusive OR Buffer Option only.

Clear XOR Buffer (COB)	6661	Clears the Exclusive OR Buffer.
Inclusive OR Buffer (IOB)	6664	Transfers 1s from the AC to the buffer register.
Read OR Buffer (ROB)	6662	Transfers the buffer register content to the input mixers of the PDP-8 accumulator.
Exclusive OR Buffer (XOB)	6654	Causes an Exclusive OR of the AC with the buffer register.

CHAPTER 5
PRINCIPLES OF OPERATION

A simplified block diagram of the DP01A appears in Figure 5-1. The system consists basically of a computer interface, input and output character assembly logic, and an EIA interface section.

The computer interface operates from the PDP computer I/O bus, responding to programmed IOT instructions assigned to the DP01 System. The IOT instructions transfer parallel data to and from the character assembly logic, set or reset control circuits, and test control flags for a skip condition.

Output data is transferred from the computer accumulator to a buffer register and then, under control of data-set timing signals, transferred to a shift register and shifted serially to the data set. The input circuits operate in reverse, assembling serial data from the data set until the shift register contains a complete character. The character is then transferred to a buffer register and held until it can be read by the computer.

The EIA interface section converts data and control levels from DEC logic levels to signals conforming to EIA Specification RS-232B.

5.1 LOGIC ELEMENTS

5.1.1 IOT Selection Logic

IOT commands from the PDP-8 or 8/S are interpreted by the W103 IOT selector modules shown in drawing number D-BS-637-0-13. The W103 outputs are identified by the instruction's octal code. R107 inverters distribute decoded outputs to the communications control logic through interconnecting cables. The R107 outputs are identified by the instruction's mnemonic code.

Additional inverters are provided in the communications logic to supply the opposite polarity of all the IOT command pulses. These are shown on drawing number D-BS-637-0-4.

The read-in gates that transfer assembled input characters to the computer's AC are shown on the same drawing. IOT 6612 (RRB) strobes the receive buffer register content to the computer IM 3-11 lines through the interconnecting cable.

5.1.2 Skip and Priority Interrupt Logic

The gates that generate the SKIP and PI signals to the computer are shown in drawing number D-BS-637-0-4. A priority interrupt request is produced under the following conditions.

Receive Flag is set

Receive End Flag is set

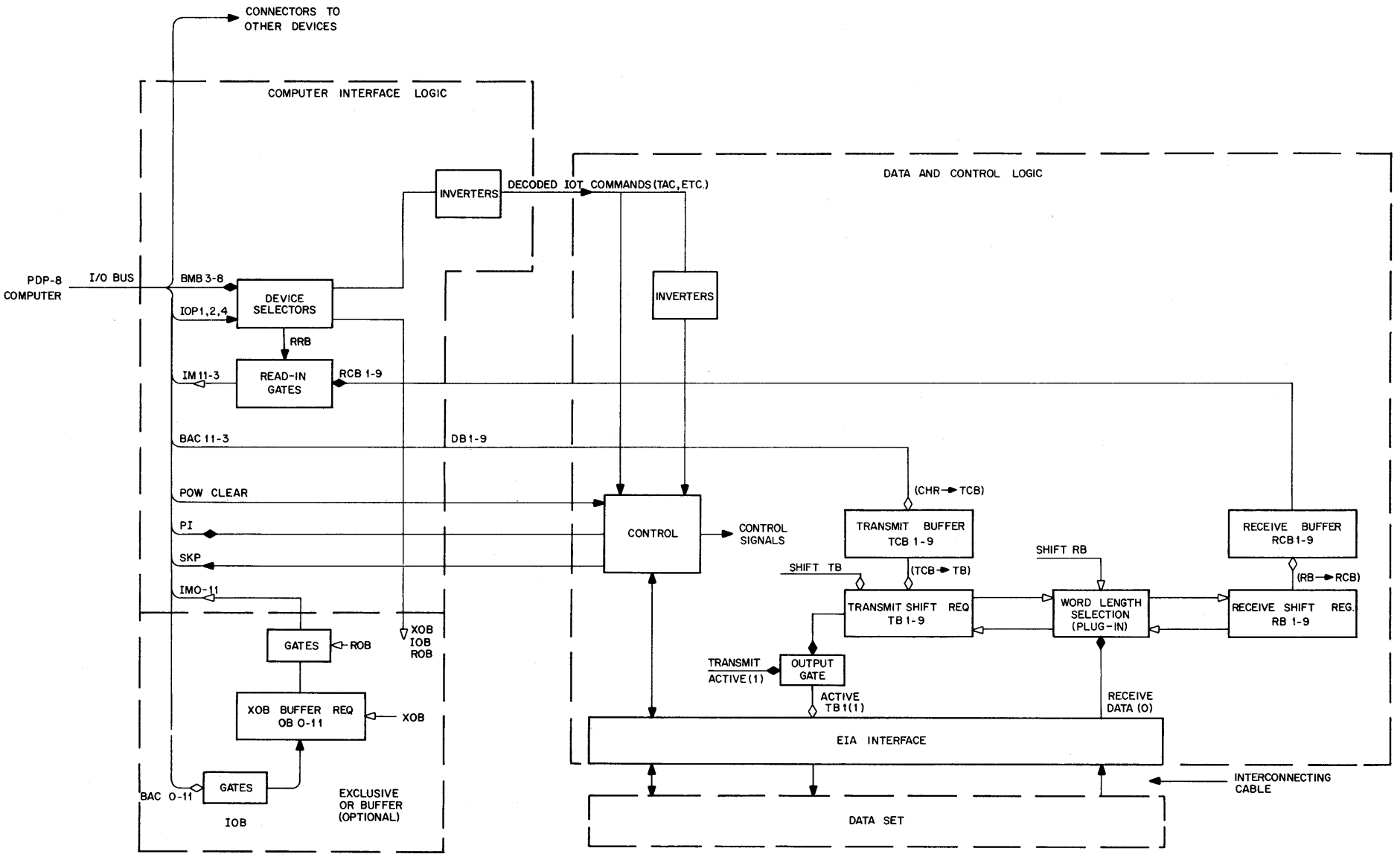


Figure 5-1 DP01A Data Flow

Transmit Flag is set

Ring Flag is set when the Ring Enable flip-flop is also set

The PI line is inverted on drawing number D-BS-637-0-13 and the resulting signal is ORed to the PDP-8 INTERRUPT line.

When the SKIP logic produces a negative pulse during one of the six assigned I/O skip instructions, the computer's program is incremented so that the program skips the next instruction. During the STF instruction, for example, if the transmit flag is reset, a SKIP pulse is generated. If the transmit flag is set during the STF, no SKIP pulse occurs; the program executes the next instruction. The other skip instructions operate in the same way.

The negative SKIP pulse is inverted and ORed to the PDP-8 SKIP line.

5.1.3 Receive Logic

The receive logic on drawing number D-BS-637-0-1 consists of the receive buffer register (RCB 1-9), the receive shift register (RB 1-9), a sync character detector, and the control logic that determines the receive timing sequence.

5.1.3.1 Receive Buffer Register - The RCB register stores assembled characters from the RB register until they can be sampled by the computer. Each character is jam-transferred in by the RB → RCB pulse. Sampling is performed by the RRB instruction, through gating logic in the computer interface section of the DP01A. All nine bits of the register are transferred to the computers AC input lines, regardless of the selected character length:

RCB Register Bit	Computer Input Bit
1	11
↓	↓
9	3

Characters having fewer than nine bits are right-justified by the character assembly cycle.

5.1.3.2 Receive Shift Register - This register continually assembles serial data from the data set. When a sync character is detected, a 1 is set into the input stage of the register and shifting continues until the 1 is present in stage RB1. After one more shift, a fully assembled character is transferred to the RCB register and another 1 is set into the input stage. Input character assembly continues in this manner as long as the RECEIVE CLOCK input from the data set triggers the SHIFT RB pulses. Characters are shifted into the RB register least significant bit first.

The register is of variable length, depending on the number of bits per character in the assigned message format. In the 9-bit connection, the RECEIVE DATA (0) line drives a pair of pulse amplifiers which jam the data bit into shift register stage RB9 by collector pulldown. The register is shifted toward RB1 and a new bit is entered into RB9 during every SHIFT RB pulse.

5.1.3.3 Sync Character Detector - An expanded R111 NAND gate, is connected as a decoder to detect the sync character appropriate to the selected character length. Bits RB8 and RB9 are patched to the decoder so that the sync character is detected as it appears shifted one place left. For example, the 9-bit sync character (010 010 110) is detected as 100 101 100.

In systems using half-duplex 4-wire operation, the TRANSMIT ACTIVE(1) level inhibits sync character detection, and thus prevents setting of the Receive Active state, when the Transmit Active mode is in effect. Furthermore, systems using 2-wire transmission will terminate with a Receive End Flag.

5.1.3.4 Control Logic - Operation of the control flip-flops and logic gating are discussed later in the description of the receiving sequence of operation.

5.1.4 Transmit Logic

The transmit logic on drawing number D-BS-637-0-2 consists of the transmit buffer register and data gating, the transmit shift register, a sync character decoder, a "last bit transmitted" detector, and the control logic that determines the transmit operating sequence.

5.1.4.1 Transmit Buffer Register and Gating - The TCB register stores parallel characters from the computer until the transmit shift register is ready for another character. Each character is jam-transferred in by the CHR → TCB pulse during a TAC instruction.

The input gating preceding the register employs R107 inverters which provide both polarities of the computer data to permit jam transfer without resetting the TCB register. The data lines (DB 1-9) are identical to the computer BAC output bus lines except for numbering. Data is gated from the computer accumulator as follows.

Computer Output Bit	DB Line
11	1
↓	↓
3	9

5.1.4.2 Transmit Shift Register - This variable-length register shifts data characters to the data-set TRANSMITTED DATA line when the Transmit Active condition is in effect. The number of stages is matched to the selected character length by the plug-in bit-length selection connector. Shown in broken lines on the print are the connections for a 9-bit character.

The END bit synchronizes the demand for new characters. When data is transferred in from the TCB register by TCB → TB, a 1 is set into the END stage. Each subsequent SHIFT TB pulse shifts the character and END bit toward TB1, and shifts 0s into the END bit.

5.1.4.3 Sync Character Detector - The decoder at the lower right of drawing number D-BS-637-0-2 monitors the contents of the TCB register during a TAC instruction. The TCB = SYNC CHR signal is at ground when the TCB register contains a sync character appropriate to the selected character length.

5.1.4.4 Last Bit Detector - Another decoder at the upper right of drawing number D-BS-637-0-2 monitors the contents of the TB register and produced the LAST BIT TRANSMITTED signal when TB3 through 9 and the END bit are all 0s. This condition occurs at the beginning of a transmission after the register has been cleared, or after the END bit has been shifted to TB2.

5.1.4.5 Control Logic - Control flip-flops and logic gates on drawing numbers D-BS-637-0-2 and D-BS-637-0-3 develop the enabling conditions and strobe pulses that set up the transmission sequence. These signals are discussed in the following description of sequential operation.

5.1.5 EIA RS-232B Interface

Signals exchanged with the associated data set or communication equipment are converted from standard DEC logic levels of 0 and -3V to voltages conforming to Electronics Industries Association (EIA) Standard RS-232B. EIA interface signals are voltages more positive than +3V and more negative than -3V. They are interpreted as follows.

Data Circuits	Control Circuits	Polarity
Mark (1)	OFF	-
Space (0)	ON	+

Timing inputs and the RING signal from the data set are shaped by W501 Schmitt Triggers before being distributed to the communications control logic. The SERIAL CLOCK RECEIVE and SERIAL

CLOCK TRANSMIT inputs are converted to standard positive pulses producing Receive and Transmit clocks, as shown on drawing D-BS-637-0-3.

Shown on the same drawing are some of the flag flip-flops associated with the data set control lines. Functions of these signals are summarized in Chapter 2.

5.2 SEQUENCE OF OPERATION

5.2.1 Receiving Channel

A detailed timing chart of a receive sequence, showing the important logic states during reception of a sync character and two data characters consisting of alternate 1s and 0s, appears in Figure 5-2. A detailed flow chart appears in Figure 5-3.

Serial data on the RECEIVED DATA line is continually assembled in a shift register under control of the SERIAL CLOCK RECEIVE pulse stream from the data set. When a sync character is detected, a sentinel bit is set in the most significant bit of the receiving shift register. The next incoming character is fully assembled when the sentinel bit is shifted out of the least significant stage. At that time the assembled character is transferred to the receive buffer register, a program interrupt request is generated, and a new sentinel bit is inserted into the shift register MSB. The program responds to the interrupt request with an instruction which loads the assembled character into the computer's accumulator. This sequence is repeated for every character until the data set clock stops.

5.2.1.1 Starting Condition - The INI signal, derived from the computer power clear generated during power on, clears the status flip-flops indicated on the flow chart. Thereafter, events are under control of the SERIAL CLOCK RECEIVE line from the data set, which develops the SHIFT RB pulses.

5.2.1.2 Receive Active - SHIFT RB pulses enter serial data from the data set's RECEIVE DATA line into the most significant stage of the RB register. Once a sync character is detected, the next shift pulse sets the REC ACTIVE flip-flop. This flip-flop enables transfer of assembled characters to the computer by enabling the RB → RCB pulse discussed later. The flip-flop is reset either when the RECEIVE IN PROGRESS delay times out or when a CRA instruction is delivered by the computer.

5.2.1.3 Sentinel Bit - When the REC ACTIVE flip-flop is set after sync character detection, it triggers a pulse amplifier which resets the RB register (wiping out the sync character). The RB register reset pulse also triggers a pulse which is patched through the bit-length selection connector to force the shift register input stage (RB9 for a 9-bit character) to the 1 condition. This acts as a sentinel bit; a complete character will be present in the RB register when this bit is shifted out of RB1.

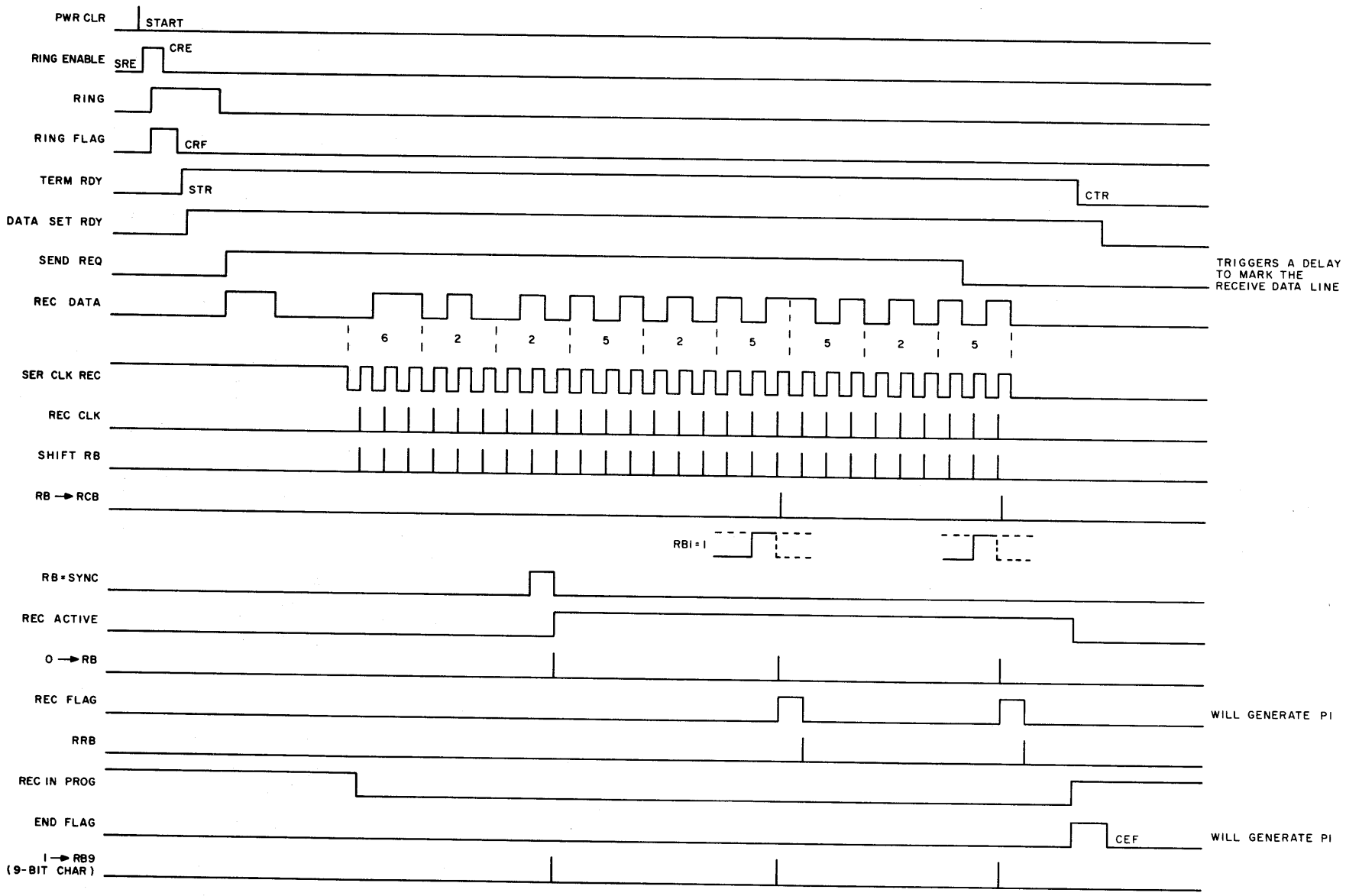


Figure 5-2 DP01A Receiving Channel Timing

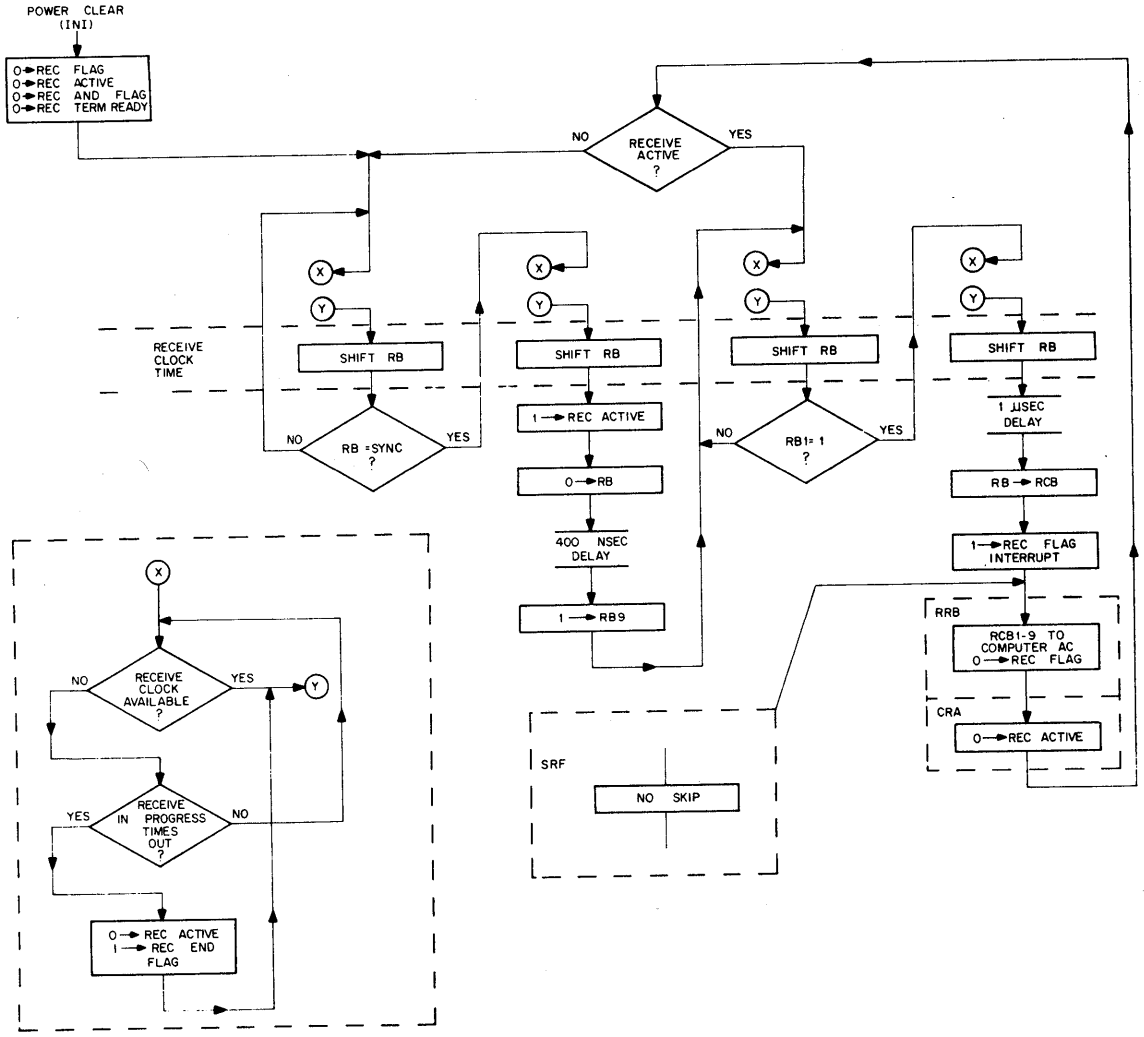


Figure 5-3 Receive Logic Detailed Flow Chart

5.2.1.4 Input to Computer - Once the sentinel bit is detected in RB1, the RB → RCB pulse is generated, after a 1 μs delay. The RB → RCB pulse transfers the assembled character to the RCB buffer register and also sets the REC FLAG flip-flop, which in turn develops a program interrupt request. (See drawing number D-BS-637-0-4.) The program normally responds with an SRF instruction to test whether it is the Receive Flag that is interrupting. Since the test is for "receive flag not set", the program proceeds to the next instruction, normally a jump to a subroutine that handles received data. As a minimum, the subroutine must read the buffered character with an RRB instruction, which also resets the REC FLAG flip-flop and turns off the interrupt.

5.2.1.5 Next Character - During the interrupt, character assembly continues in the shift register while the previous character is stored in the buffer register. Each RB → RCB pulse also triggers the logic chain which enters a new sentinel bit in the RB input stage. After the sentinel bit is shifted to RB1, RB → RCB is again generated, an interrupt request is made, and the cycle repeats. A character is lost if the program fails to read it before the next character is ready, but assembly continues without interruption.

5.2.1.6 Receive in Progress Delay - As long as SHIFT RB pulses occur, they prevent the RECEIVE IN PROGRESS delay from recovering. If the shift pulses stop for more than the delay period (1-1/2 bit time), the delay unit recovers and the RECEIVE IN PROGRESS line steps to ground. Delays for the three most frequently used baud rates are shown on drawing number D-BS-637-0-1.

Until a sync character is received, timeout has no effect. Thereafter, a timeout resets the REC ACTIVE flip-flop and stops character transfer to the computer until another sync character is detected.

5.2.1.7 Receive End Flag - When the data set receive clock stops long enough for the RECEIVE IN PROGRESS delay to time out (1-1/2 bit time), the REC END FLAG flip-flop is set, causing a program interrupt request. The condition of the flip-flop can be tested by an SEF instruction and reset by a CEF instruction.

5.2.2 Transmitting Channel

A detailed timing chart of a short message transmission appears in Figure 5-4. A detailed flow chart appears in Figure 5-5.

The DP01A transmit logic enters the "transmit active" mode when the program loads a sync character for transmission. Thereafter, the character is shifted out on the TRANSMITTED DATA line under control of the data set SERIAL CLOCK TRANSMIT pulse stream.

Since the DP01A operates in a bit synchronous mode, data must be made available for transmission as it is needed, since every N bits are assembled to form a character. Even an extra bit or a dropped bit will cause faulty character assembly at the receiving station. The DP01A safeguards against interruptions in the character pattern by double buffering and by program interrupt requests for new characters.

In the normal "transmit active" mode of operation automatically selected by the first sync character of a new transmission, the DP01A will stop transmitting (hold the TRANSMITTED DATA line in the binary 1 condition) if a new character is not available for transmission. An alternate "transmit idle" mode can also be set up by the program. In the transmit idle mode, when a new character is not

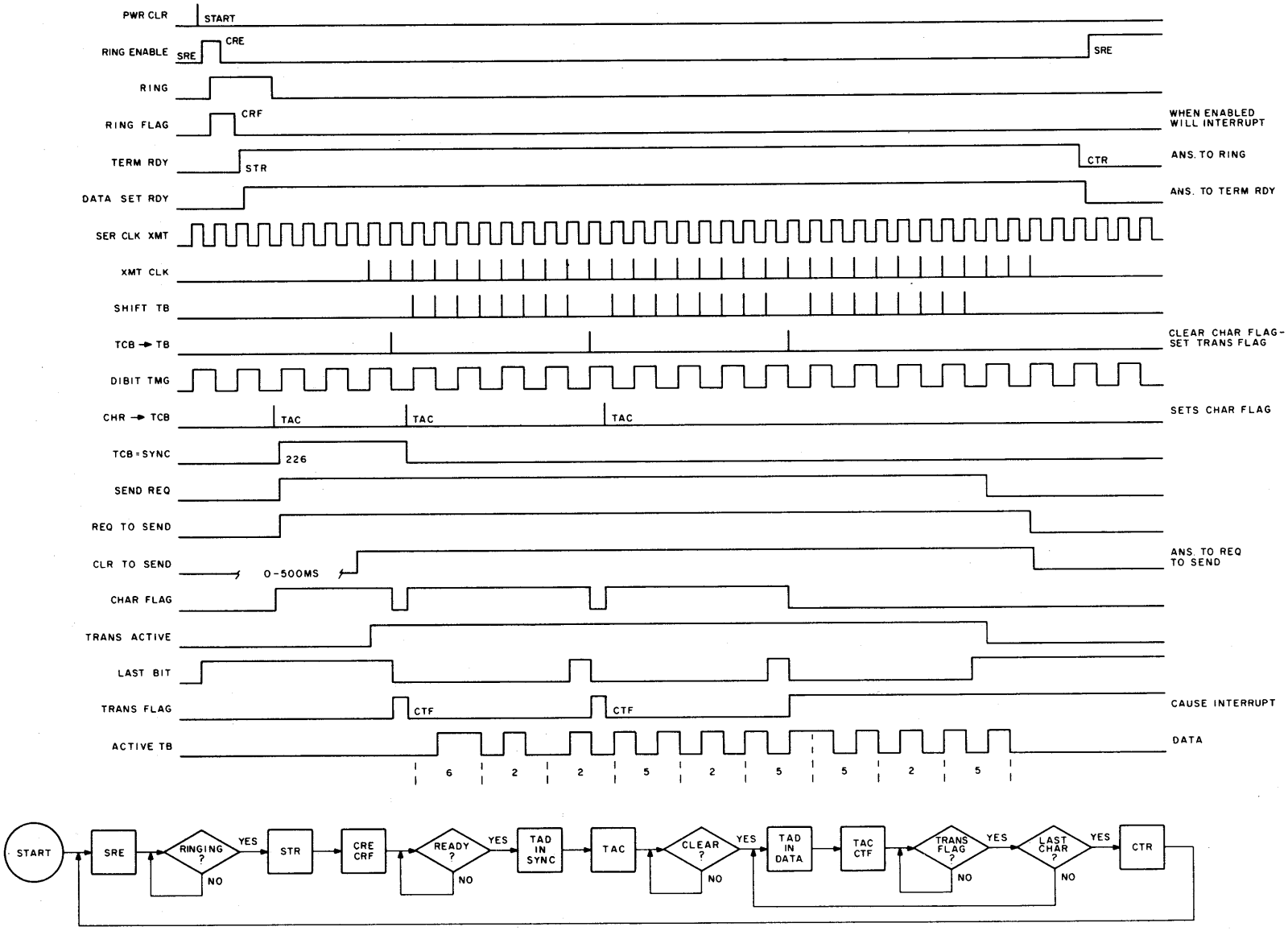


Figure 5-4 DP01A Transmitting Channel Timing

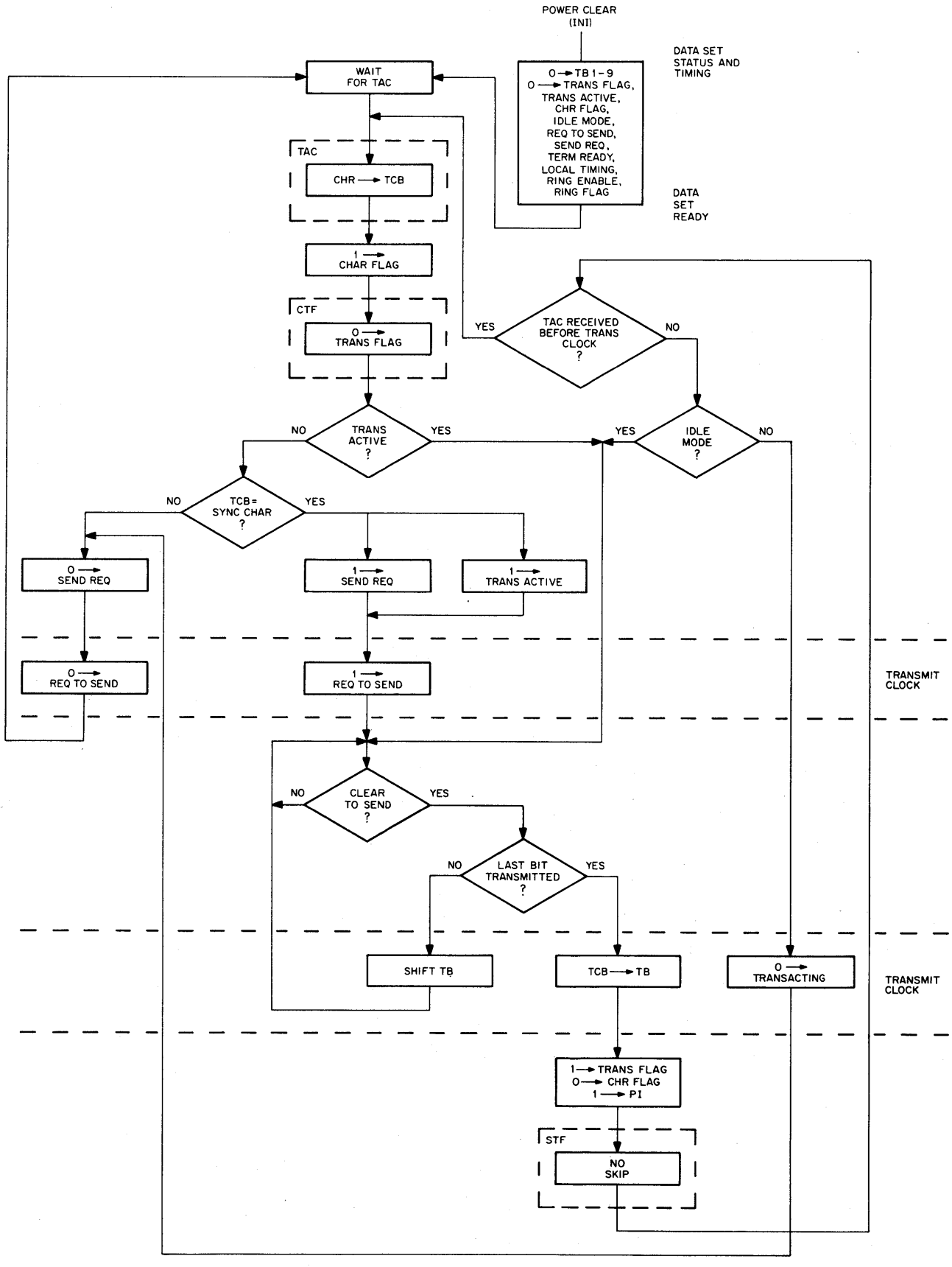


Figure 5-5 Transmit Logic, Detailed Flow Chart

available, communication with the distant terminal is maintained by repeating an idle character (the last character that was transmitted). The idle mode is desirable in applications that require a relatively long time to establish transmission.

5.2.2.1 Starting Condition - After a power clear pulse from the PDP-8 (INI), the transmit logic is in the condition shown at the upper left of the detailed flow chart. The IDLE MODE flip-flop can be either set or reset by the program.

Because the REQ TO SEND flip-flop is reset, the data set holds the CLEAR TO SEND line OFF. As a result, the TRANSMIT CLOCK is blocked and no shift pulses are generated. Since the TRANS ACTIVE flip-flop is also reset, the transmit data line (ACTIVE TB (1)) is held at ground, for a permanent mark condition. Nothing more happens until the PDP-8 delivers a character to the transmit buffer register, by a TAC instruction.

5.2.2.2 First Character - The TAC instruction produces the CHR → TCB strobe pulse which transfers data from the PDP-8 DB lines to the TCB register, and also sets the character flag. The program has the option to test the transmit flag at this time by a CTF instruction. (On the first character cycle, of course, the transmit flag is always reset.)

If the first character is a sync character, the SEND REQ and TRANS ACTIVE flip-flops are set. During the next TRANSMIT TIMING pulse, the REQ TO SEND flip-flop is set and the corresponding signal is applied to the data set. Once the data set replies with a CLEAR TO SEND signal, the TRANSMIT TIMING pulse train is gated to the TRANSMIT CLOCK line.

If the character in TCB is not a sync character, the SEND REQ flip-flop is reset and the next TRANSMIT TIMING pulse resets the REQ TO SEND flip-flop.

On the first (sync) character, because the TB register is reset, the LAST BIT TRANSMITTED signal is true. Consequently, the first TRANSMIT CLOCK generates the TCB → TB pulse rather than the SHIFT TB pulse. The TCB → TB pulse sets the Transmit Flag and resets the Character Flag. The Transmit Flag forces the computer INTERRUPT line to ground, for a program interrupt request. The condition of the Transmit Flag can be tested by an STF instruction to confirm that it is the DP01A that is interrupting. (When the Transmit Flag is set, a "no skip" condition on the SKIP line results.)

5.2.2.3 Successive Data Characters - In order to sustain continuous serial transmission, the PDP-8 must respond to the interrupt and deliver another character for the TCB register by a TAC instruction before the next TRANSMIT CLOCK pulse. If the TAC is received in time, CHR → TCB loads the character, sets the CHAR FLAG, and resets the TRANS FLAG.

Starting with the next TRANSMIT CLOCK pulse, SHIFT TB pulses are produced to shift the TB register toward TB1. Bits in TB1 are presented to the ACTIVE TB(1) line. When the character is fully shifted out, the LAST BIT TRANSMITTED line blocks further SHIFT TB pulses and enables the TCB → TB pulse, transferring the buffered character to the shift register and enabling a new character demand via the PI line. This sequence continues until the PDP-8 fails to deliver a character before the next TRANSMIT CLOCK pulse.

5.2.2.4 Ending Message (Not Idle Mode) - When the program fails to deliver a new character in time and IDLE MODE is not selected, both SHIFT TB and TCB → TB are inhibited and the TRANS ACTIVE flip-flop is reset. The transmit logic resets the SEND REQ and REQ TO SEND flip-flops and waits for another sync character to set up the transmit sequence again.

5.2.2.5 Ending Message (Idle Mode) - If the IDLE MODE is selected, when the last bit of a character is transmitted and a TAC is not received in time, TCB → TB and related signals are generated, replacing the previous character in the output shift register. SHIFT TB pulses are enabled until the last bit is transmitted again, and the TCB → TB sequence is repeated. In this manner, the last character received from the PDP-8 is retransmitted continuously, until a new data character is delivered by TAC instruction or the idle mode is reset by a CIM instruction.

5.3 EXCLUSIVE OR BUFFER (OPTIONAL)

An exclusive OR buffer, can be added to the computer interface section. (See drawing number D-BS-DP01A-0-3.)

The buffer logic consists of an 11-stage flip-flop register, input loading and XOR gating, and output gating.

All stages of the OB register are cleared by the COB command. The IOB command can then be used to transfer 1s from the computer AC to the register. If clearing is omitted, the IOB command places the inclusive OR of AC and OB in the register.

The XOR function is performed by the DCD input gates under control of the XOB command. Logic of a single stage follows the truth table below:

Previous OB Bit	BAC Bit	New OB Bit
0	0	0
0	1	1
1	0	1
1	1	0

Note that if the BAC bit is a 1, the corresponding OB bit is complemented to place the exclusive OR of BAC and OB in OB.

The content of the OB register is placed on the IM 0-11 lines during an ROB command.

CHAPTER 6
MAINTENANCE

The DP01A always operates in association with a PDP-8 computer installation; the general instructions in Chapter 9 of the PDP-8 Maintenance Manual apply to the DP01A as well. No additional maintenance equipment is required. Periodic preventive maintenance and mechanical checks for the PDP-8 installation should include the DP01A assembly.

6.1 DIAGNOSTICS

The following diagnostic programs are designed specifically for checkout of the DP01A logic. Use these tests during marginal checking and trouble analysis.

Document Number	Title
Maindec-08-D8FA-D	DP01A Bit Synchronous Communication System IOT and Data Test
Maindec-08-D8K8-D	DP01A IOT and Data Test

6.2 MARGINAL CHECKS

The DP01A receives +10V and -15V dc power directly from the PDP-8 power supplies. Marginal check selector switches on the DP01A logic panels permit the marginal check features of the PDP-8 to be applied to the DP01A logic as well. Follow the marginal check instructions in Chapter 9 of the PDP-8 Maintenance Manual, and select the DP01A module row to be checked by placing the +10 or -15 selector switch for that row in the MC position (up). (See Figure 2-1.) During marginal checking, run the diagnostic programs to verify DP01A operation.

Be sure to turn all DP01A marginal check switches off (down) after completing tests.

6.3 ADJUSTMENTS

6.3.1 Adjusting One-Shot Delays

All one-shot delays in the DP01A are listed below. These are calibrated at the factory and usually do not need adjustment unless a module is replaced. A simple way to start a delay for adjustment, without a pulse generator or other timing source, is to momentarily ground the inputs to the delay's DCD input gate, while observing the delay on a scope. Screwdriver adjustments are provided on the modules

for delay time adjustment. The delay can be observed dynamically during a diagnostic test cycle, for confirmation of accuracy. If modules are replaced, delays should be adjusted before running diagnostics.

Delay	Module	Logic Print	Timing
Assembled Character Sampling	R302	D-BS-637-0-1	1.0 μs
Receive in Progress	R303	D-BS-637-0-1	See table on Logic Print
Inactive Data Muting	R302	D-BS-637-0-3	4.5 ms

6.4 CORRECTIVE MAINTENANCE

Refer to the PDP-8 Maintenance Manual for general instructions.

Troubleshooting the DP01A system is straightforward. The diagnostic self-test permits methodical performance checking with the DP01A completely independent of the data set. Equipment operation can be checked against the flow charts and timing diagrams in Chapter 5 of this manual. No special test equipment is required.

6.4.1 Diagnostic Testing

MAINDEC-08-D8FA-D supplied with the DP01A requires that the W990 test connector is installed as shown in Figure 6-1. Timing is generated under program control by connecting unused IOT command 6354 to the LOCAL TIMING output line and feeding the pulses into the SERIAL CLOCK TRANSMIT and RECEIVE input lines. The program-controlled TERMINAL READY line is also wrapped around to simulate the DATA SET READY and RING inputs to the DP01A. Similarly, REQUEST TO SEND simulates CLEAR TO SEND, and TRANSMIT DATA simulates RECEIVE DATA. A complete duplex message is readily simulated by the program. A transmitted sync character, assembled by the receive logic, initiates a receive sequence, and every character transmitted thereafter is assembled by the receive circuits for checking.

MAINDEC-08-D8K8-D supplied with the DP01A, is designed to operate with the DP01A connected to a modem.

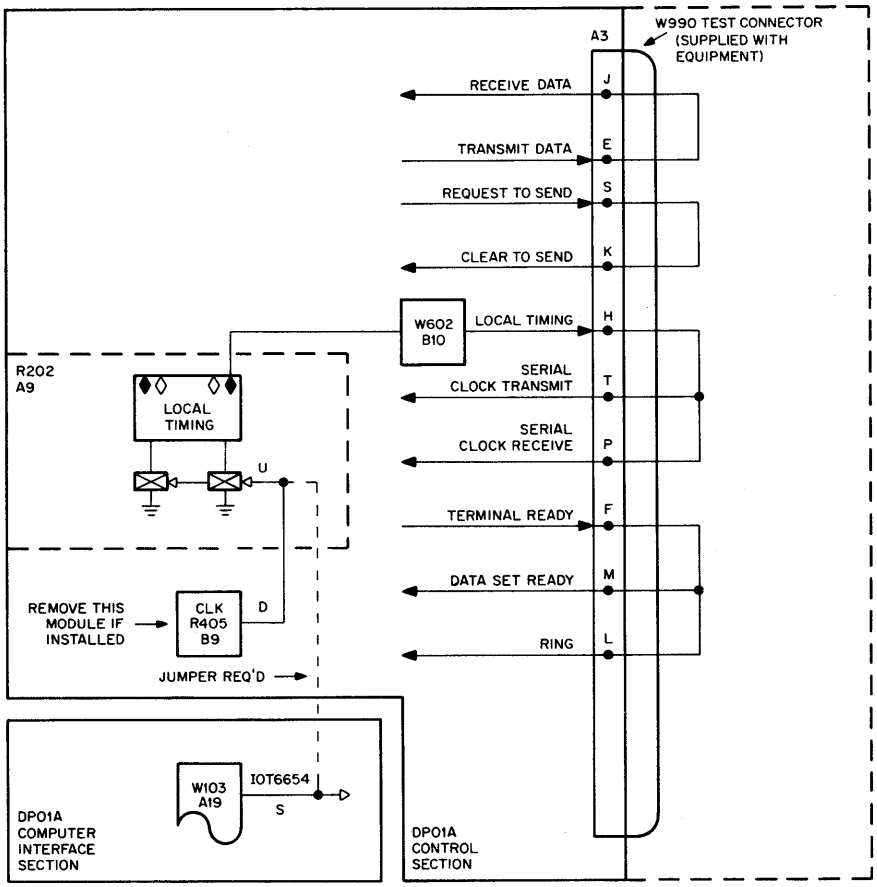


Figure 6-1 Connections for Diagnostic Testing Using Maindec-08-D8FA

CHAPTER 7
ENGINEERING DRAWINGS AND GLOSSARY

7.1 ENGINEERING DRAWINGS

This section contains reduced copies of DP01A logic diagrams and special-purpose module schematics. Drawings reproduced here for reference purposes apply to standard production equipment. During actual maintenance, refer to the current prints supplied with the equipment.

Logic diagram graphic conventions, logic symbols, and signal names correspond to those used in the PDP-8 drawing system. Refer to the PDP-8 Maintenance Manual for definitions.

A schematic is provided (following the logic diagrams) for the S202 Dual Flip-Flop module. All other module types are described in the Digital Logic Handbook (C-105).

Other engineering drawings (assembly drawings, parts lists, etc.) used primarily for reference in maintenance are listed on the master drawing breakdown (D-DI-637-0-16). Table 7-1 is an index to the drawings and schematics supplied in this section.

Table 7-1
Logic Diagram and Schematic Index

7.2 SIGNAL GLOSSARY

A glossary of signal names for the DP01A appears at the end of this section. Signals generated on the D-BS-637- - series of logic diagrams are defined and the originating print number is given. For similar information on the signals on the PDP-8 I/O bus, refer to the PDP-8 Maintenance Manual.

SIGNAL GLOSSARY

Signal	Logic Print (D-BS-637-0-)	Function
ACTIVE TB1(1)	2	Transmitted serial data to output level converter
ALLOW TRANSMIT	2	Enables transfer of characters from TCB to TB register
CEF	4	Decoded CEF instruction
CHR FLAG	2	Character flag
CHR → TCB	4	Strobes computer AC to TCB register during TAC instruction
CIM	4	CIM instruction decoded
CLEAR TO SEND	3	Control line from data set; enables transmit clock
CRE	4	CRE instruction decoded
CTF	4	CTF instruction decoded
CTR	4	CTR instruction decoded
DATA SET READY	3	Control line from data set; condition can be tested by SSR instruction
END	2	TB register END bit
IDLE MODE	2	Status flip-flop set and reset by program
IM 3-11	13	I/O bus input lines to computer AC
INI	4	Derived from computer POWER CLEAR pulse
INTERRUPT	13	Computer program interrupt request line
LAST BIT TRANSMITTED	2	TB 3-9 and END bit all 0s
LOCAL TIMING	3	DP01A internal clock (optional)

SIGNAL GLOSSARY (cont)

Signal	Logic Print	Function
PI	4	Program interrupt request gate
RB → RCB	1	Gates assembled received characters from RB to RCB register
RB = SYNC CHR	1	RB register contains sync character appropriate to selected character length
RB 1-9	1	Receive shift register
RCB 1-9	1	Receive character buffer register
REC ACTIVE	1	Status flip-flop; set when sync character is detected, reset when data set Receive clock stream is interrupted.
RECEIVE CLOCK	3	RECEIVE TIMING, inverted
RECEIVE DATA	3	Serial data from data set
RECEIVE IN PROGRESS	1	Delay that times out when data set receive clock stops longer than a selected interval.
RECEIVE TIMING	3	Data set SERIAL CLOCK RECEIVE, shaped and inverted
REC FLAG	1	Status flip-flop; is set and requests interrupt when an assembled character is ready; reset by RRB instruction
REQ TO SEND	3	Control line to data set, requests service in transmit mode; turned on when a sync character is delivered from the computer and held on for one clock time
RING	3	Control line from data set; indicates ringing on communication line
RING ENABLE	3	Status flip-flop, set and reset by program
RING FLAG	3	Status flip-flop; set by RING line, reset by program; condition can be tested by SRI instruction
RRB	4	RRB instruction decoded
SEF	4	SEF instruction decoded
SEND REQ	3	Synchronizing flip-flop for REQ TO SEND line

SIGNAL GLOSSARY (cont)

Signal	Logic Print	Function
SHIFT RB	1	RB register shift pulses
SHIFT TB	2	TB register shift pulses
SIM	4	SIM instruction decoded
SKIP	4,13	Computer I/O bus SKIP line
SRE	4	SRE instruction decoded
SRF	4	SRF instruction decoded
SRI	4	SRI instruction decoded
SSR	4	SSR instruction decoded
STR	4	STR instruction decoded
TAC	4	TAC instruction decoded
TB 1-9	2	Transmit shift register
TCB=SYNC CHAR	2	TCB 1-8 contains sync character appropriate to selected character length
TCB → TB	2	Transfers computer output characters from TCB to TB register
TCB 1-9	2	Transmit character buffer register
TERM READY	3	Status flip-flop, set and reset by program; controls DATA TERMINAL READY output line to data set
TRANS ACTIVE	2	Status flip-flop; set when sync character is delivered, enabling data transfer to shift register and output shifting; reset when computer fails to deliver the next character in time (unless idle mode is selected).
TRANS FLAG	2	Status flip-flop; set when buffered data is transferred to shift register; reset by program
TRANSMIT CLOCK	3	Pulse train driven by TRANSMIT TIMING; enabled only when CLEAR TO SEND is on
TRANSMIT TIMING	3	Shaped version of data set SERIAL CLOCK TRANSMIT

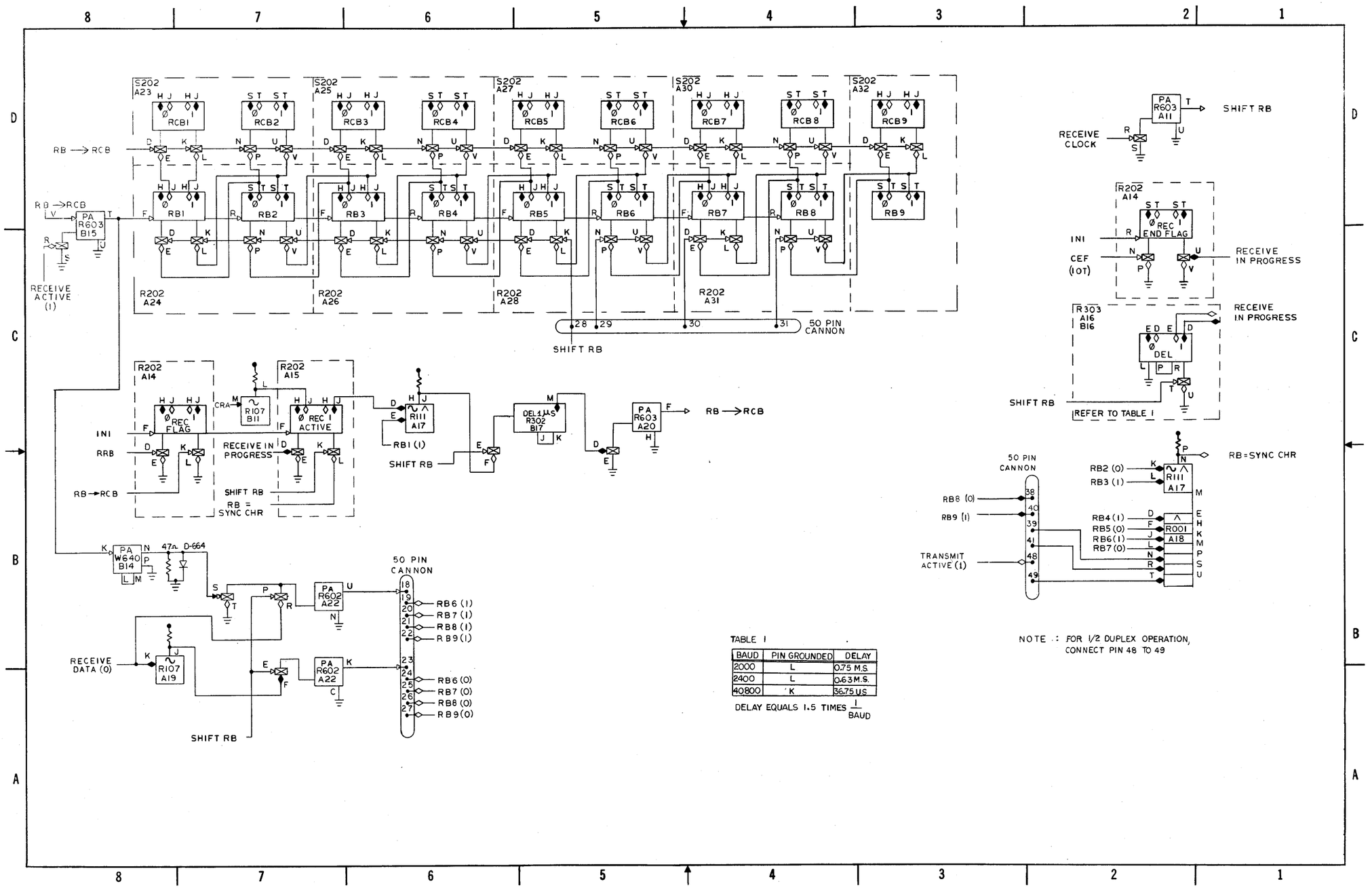


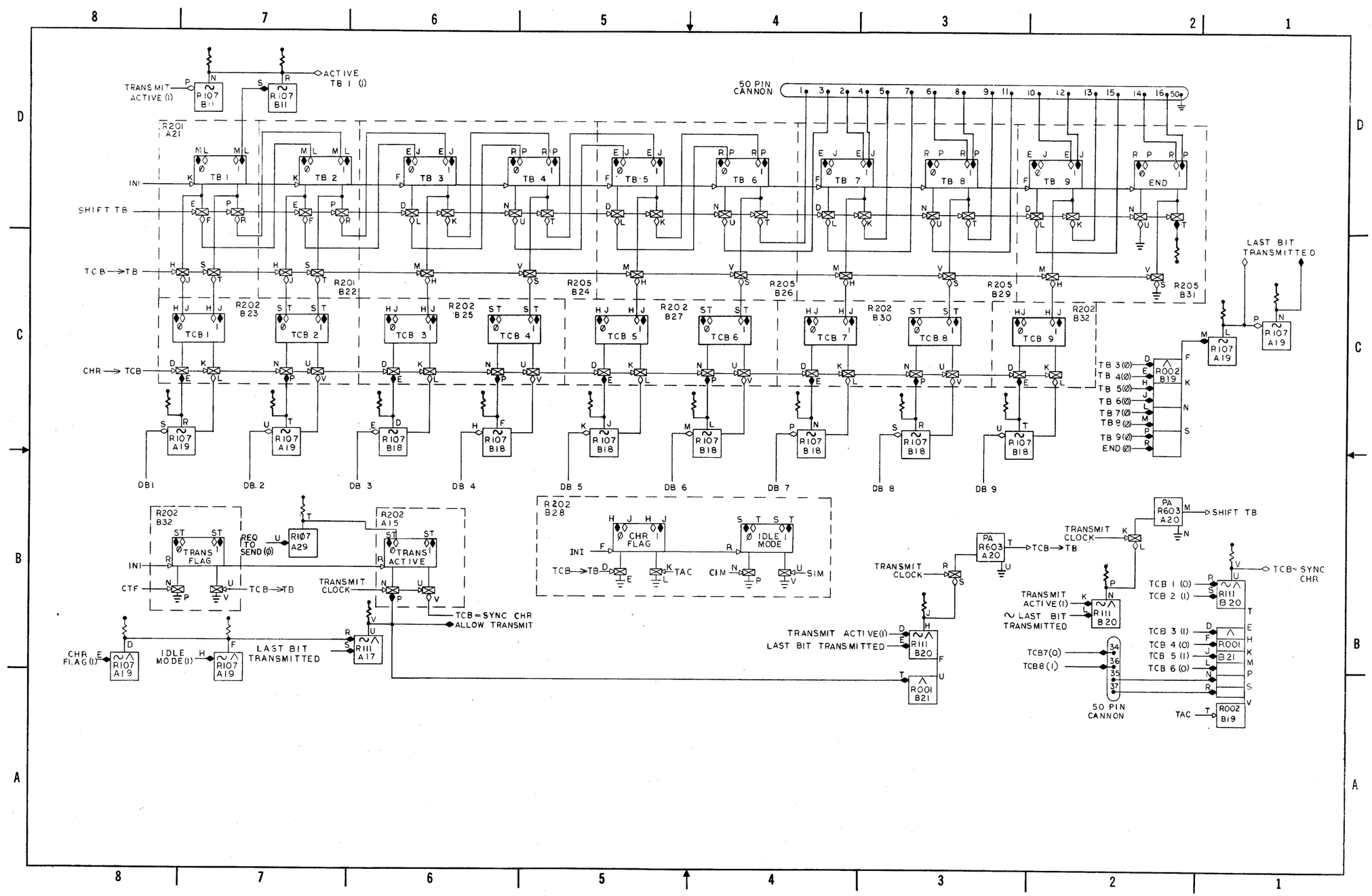
TABLE I

BAUD	PIN GROUNDED	DELAY
2000	L	0.75 M.S.
2400	L	0.63 M.S.
40800	K	36.75 µS

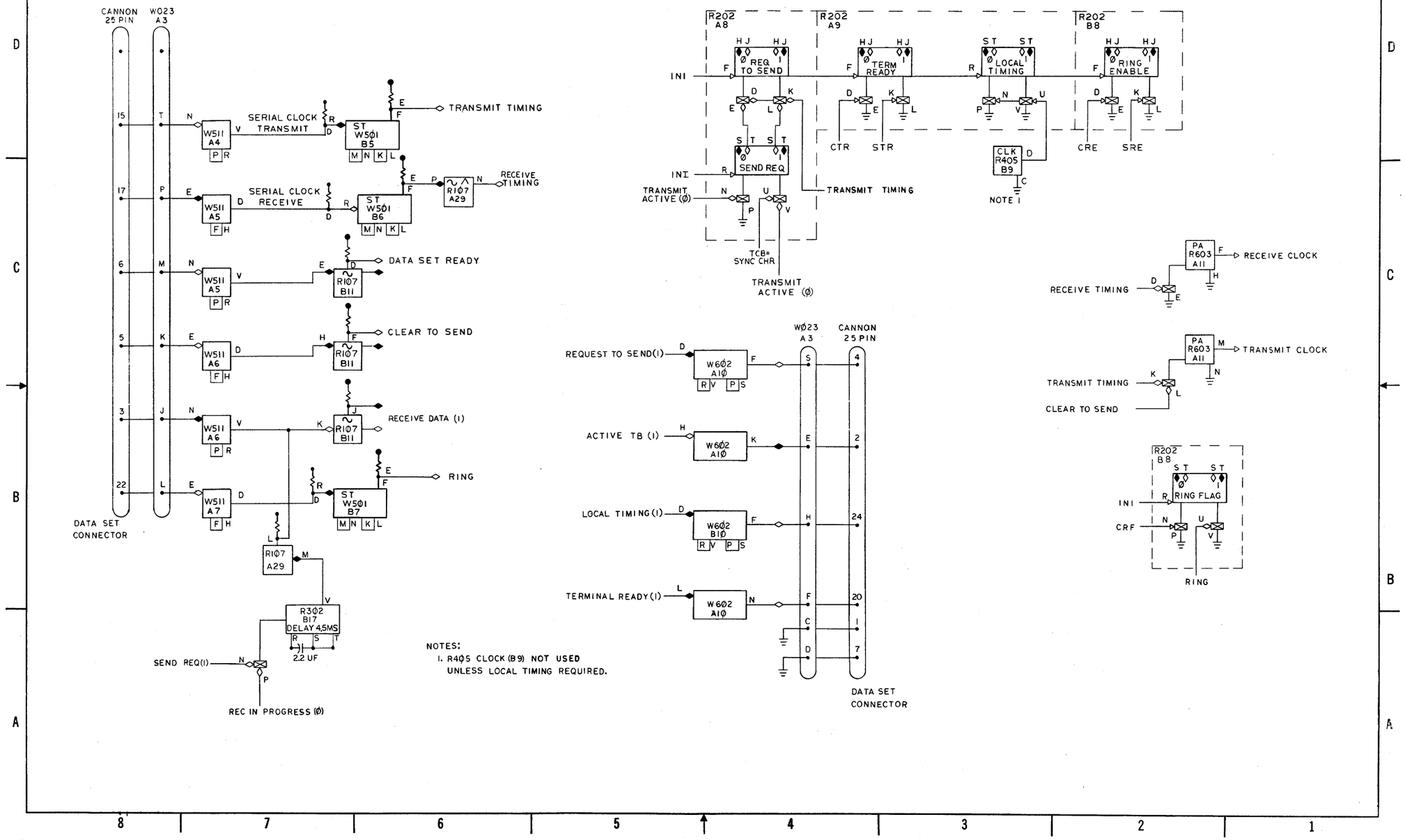
DELAY EQUALS 1.5 TIMES $\frac{1}{\text{BAUD}}$

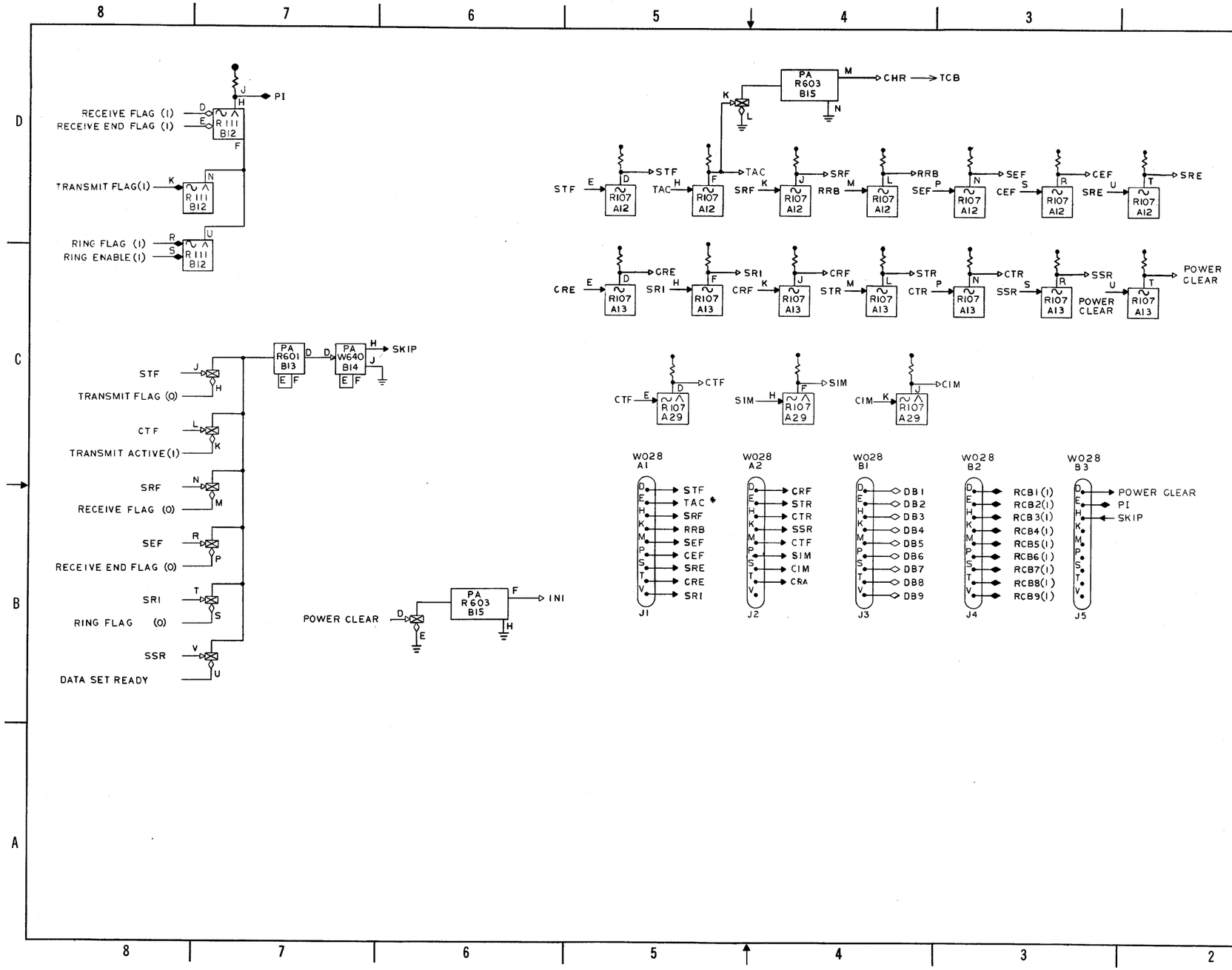
NOTE : FOR 1/2 DUPLEX OPERATION, CONNECT PIN 48 TO 49

D-BS-637-0-1 Receiver Logic



D-BS-637-0-2 Transmit Logic

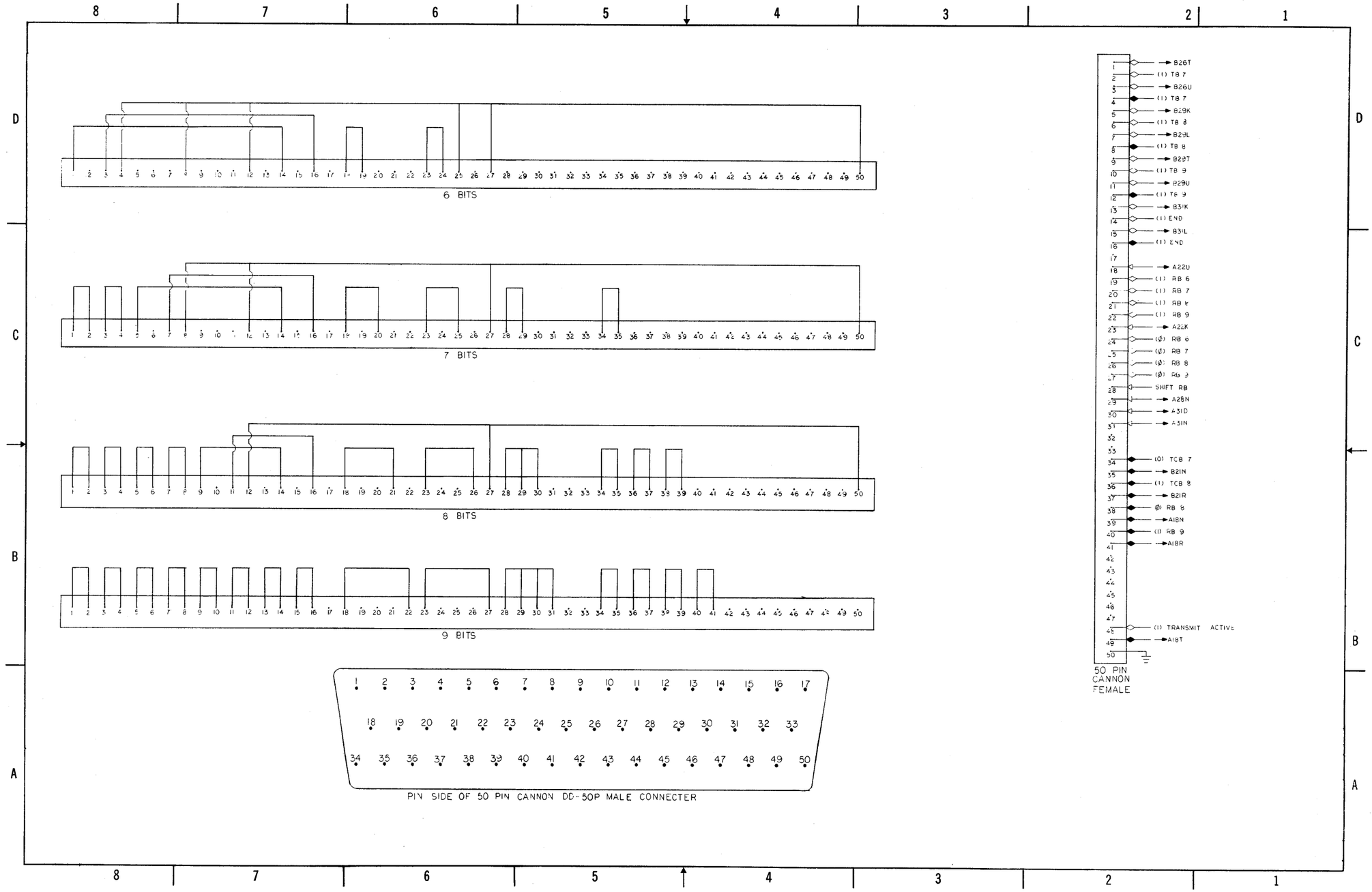

CANNON 25 PIN
W023 A3
TRANSMIT TIMING
SERIAL CLOCK TRANSMIT
W511 A4
ST W501 B5
RECEIVE TIMING
SERIAL CLOCK RECEIVE
W511 A5
R107 A29
ST W501 B6
DATA SET READY
R107 B11
CLEAR TO SEND
W511 A6
RECEIVE DATA (1)
RING
W511 A7
ST W501 B7
DATA SET CONNECTOR
R107 A29
R302 B17 DELAY 4.5MS
2.2 UF
SEND REQ(1)
REC IN PROGRESS (Ø)
NOTES:
1. R405 CLOCK (B9) NOT USED UNLESS LOCAL TIMING REQUIRED.
R202 A8
R202 A9
R202 B8
Ø REQ TO SEND
Ø TERM READY
Ø LOCAL TIMING
Ø RING ENABLE
INI
SEND REQ
TRANSMIT ACTIVE (Ø)
TRANSMIT TIMING
CTR
STR
CLK R405 B9
NOTE 1
CRE
SRE
TCB= SYNC CHR
TRANSMIT ACTIVE (Ø)
REQUEST TO SEND(1)
ACTIVE TB (1)
LOCAL TIMING(1)
TERMINAL READY(1)
W602 A1Ø
W602 B1Ø
DATA SET CONNECTOR
PA R603 A11
RECEIVE TIMING
RECEIVE CLOCK
TRANSMIT TIMING
CLEAR TO SEND
TRANSMIT CLOCK
RING FLAG
CRF
RING


RECEIVE FLAG (I)
RECEIVE END FLAG (I)
TRANSMIT FLAG(I)
RING FLAG (I)
RING ENABLE(I)
PI
R111 B12
PA R603 B15
CHR
TCB
STF
TAC
SRF
RRB
SEF
CEF
SRE
R107 A12
CRE
SRI
CRF
STR
CTR
SSR
POWER CLEAR
R107 A13
CTF
SIM
CIM
R107 A29
PA R601 B13
PA W640 B14
SKIP
TRANSMIT FLAG (0)
TRANSMIT ACTIVE(I)
RECEIVE FLAG (0)
RECEIVE END FLAG (0)
RING FLAG (0)
DATA SET READY
PA R603 B15
INI
W028 A1
W028 A2
W028 B1
W028 B2
W028 B3
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
RCB1(I)
RCB2(I)
RCB3(I)
RCB4(I)
RCB5(I)
RCB6(I)
RCB7(I)
RCB8(I)
RCB9(I)
J1
J2
J3
J4
J5

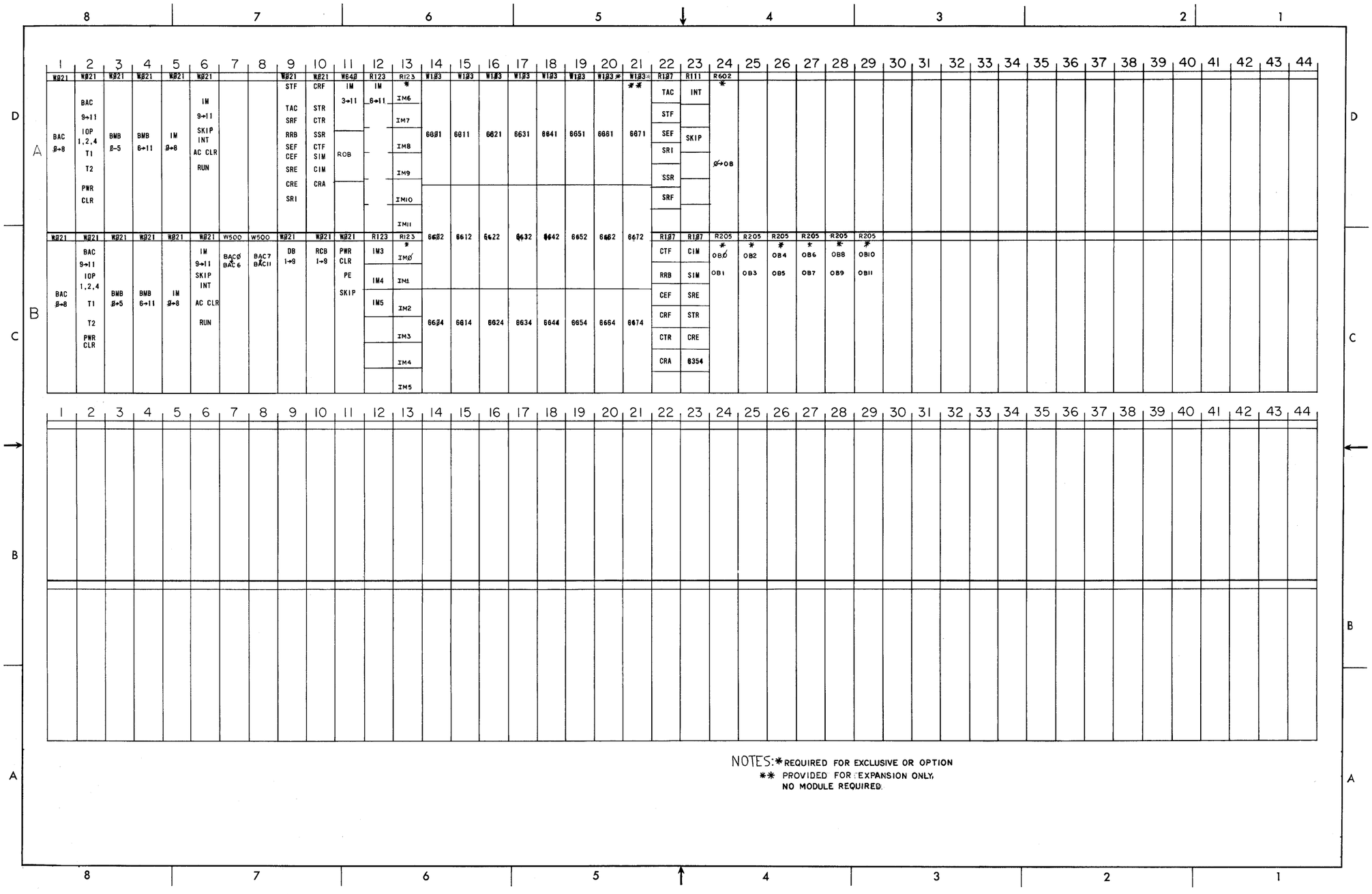
	1	2	3	4	5	6	7	8
A	W025 STF W025 TAC W025 SRF W025 RRB W025 SEF W025 CEF W025 SRE W025 CRE W025 SRI	W025 CRF W025 STR W025 CTR W025 SSR W025 CTF W025 SIM W025 CIM	W023 DATA SET	W511 SER CLOCK TRANSM.	W511 SER CLOCK REC. W511 DATA SET RDY	W511 CLR TO SEND W511 REC DATA	W511 RING	R202 REQ TO SEND R202 SEND REQ
B	W028 DBI THRU DB9	W028 RCB1(I) THRU RCB9(I)	W028 PWR CLR PI SKIP		W501 TRANSM TIMING	W501 REC TIMING	W501 RING	R202 RING ENABLE RING FLAG
C								
D								

	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A	R202 TERM RDY LOCAL TIMING	W602 REQ TO SEND (1) ACT TB (1) TERM RDY	R603 REC CLOCK TRANSM. CLOCK SHIFT RB	R107 STF TAC SRF RRB SEF CEF SRE	R107 CRE SRI CRF STR CTR SSR PWR CLR	R202 REC FLAG REC END FLAG	R202 REC ACTIVE TRANSM ACTIVE	R303 REC IN PROG.	R111 RB→RCB RBI = SYNC. CHR COMP TRANS ACTIVE	R001 RB = SYNC CHR	R107 0→XMIT ENABLE 0→XMIT ENABLE REC DATA (0) LAST BIT TRANSM. TCB1 IN TCB2 IN	R603 RB→RCB SHIFT TB TCB→TB	R201 TBI	R602 0'S→RB 1 S→RB	S202 RCB 1 RCB 2	R202 RB 1 RB 2	S202 RCB 3 RCB 4	R202 RB 3 RB 4	S202 RCB 5 RCB 6	R202 RB 5 RB 6	R107 CTF SIM CIM RS 0→RD RECEIVE TIMING 0→TRANS ACTIVE	S202 RCB 7 RCB 8	R202 RB 7 RB 8	S202 RCB 9 RB 9
B	R405 * CLOCK	W602 LOCAL TIMING	R107 DATA SET RDY CLR TO SEND REC DATA(I) 0→REC ACTIVE ACT TB 1 (I) CRA	R111 PI PI PI PI	R601 SKIP	W640 SKIP RCV ACTIVE DELAY	R603 INI CHR→TCB CLR RB		R302 RB→RCB RS = 0→RD	R107 COMP TCB3 TO TCB9	R002 LAST BIT TAC	R111 TCB→TB SHIFT TB TCB = SYNC CHR	R001 TCB EQ SYNC CHR TCB = TB	R201 TB 2	R202 TCB 1 TCB 2	R205 TB 3 TB 4	R202 TCB 3 TCB 4	R205 TB 5 TB 6	R202 TCB 5 TCB 6	R202 CHR FLAG IDLE MODE	R205 TB 7 TB 8	R202 TCB 7 TCB 8	R205 TB 9 END	R202 TCB 9 TRANSM FLAG
C																								
D																								

* R405 REQUIRED ONLY IF LOCAL TIMING IS USED

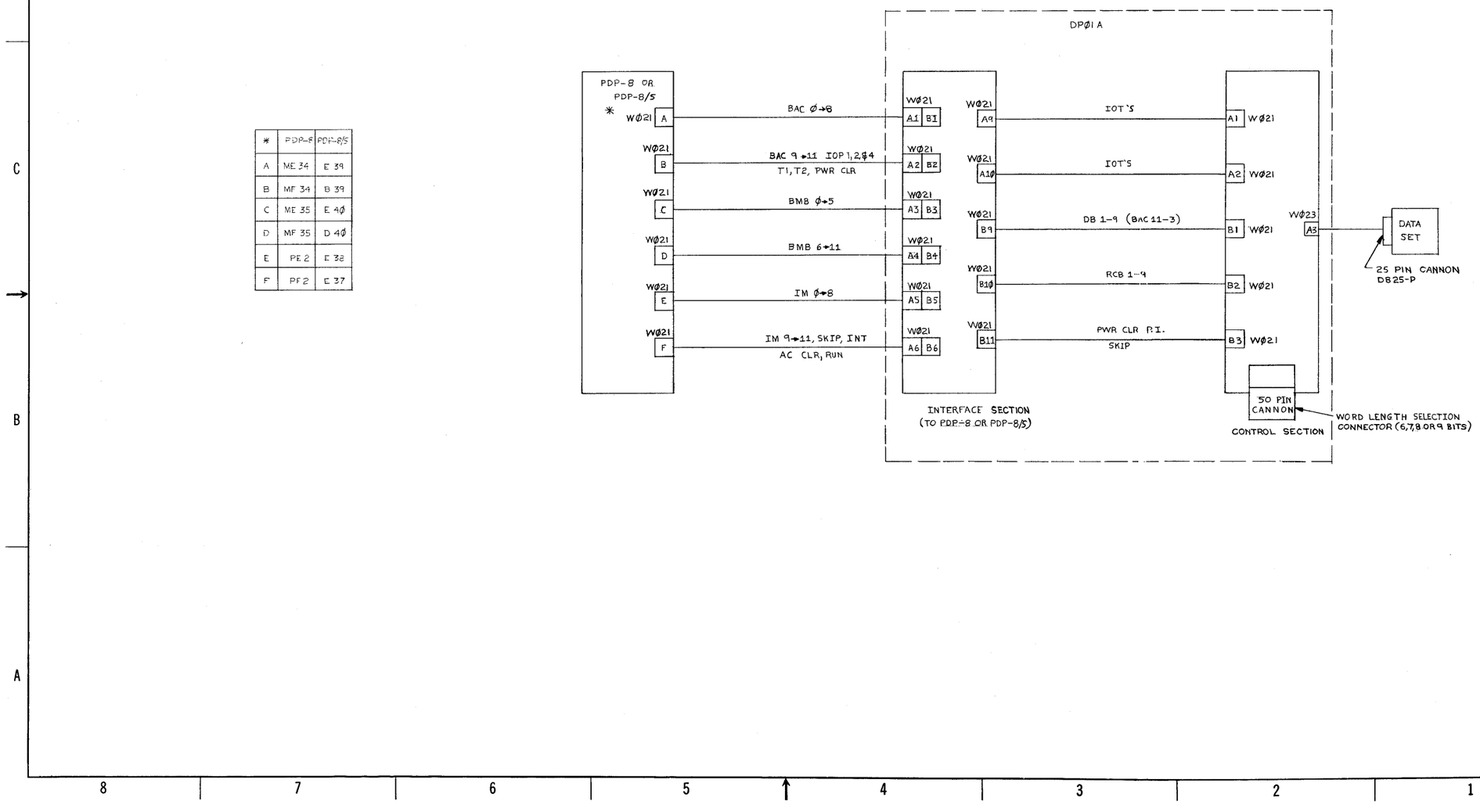


D-AR-637-0-9 DP01A Word Length Selection

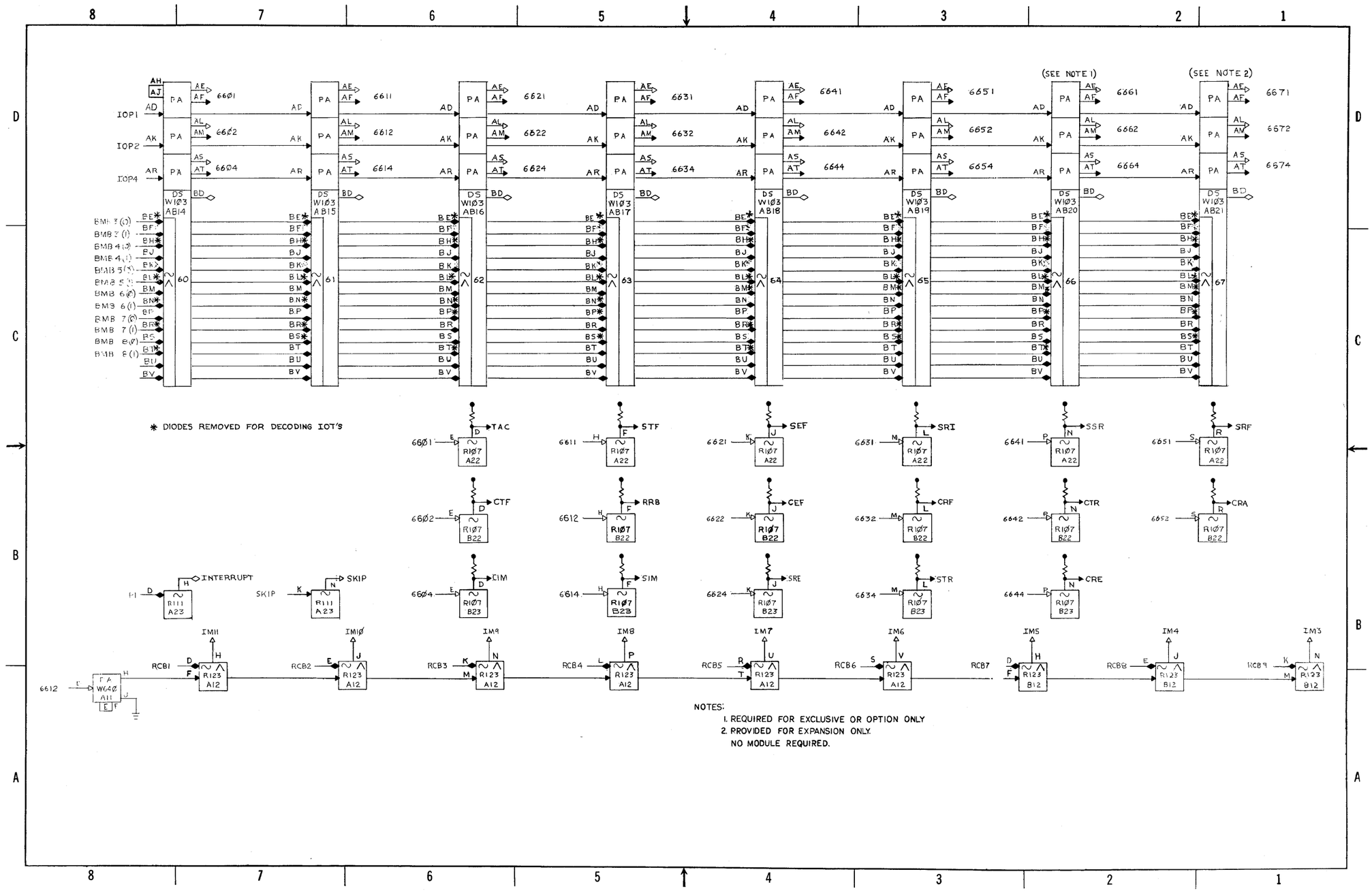


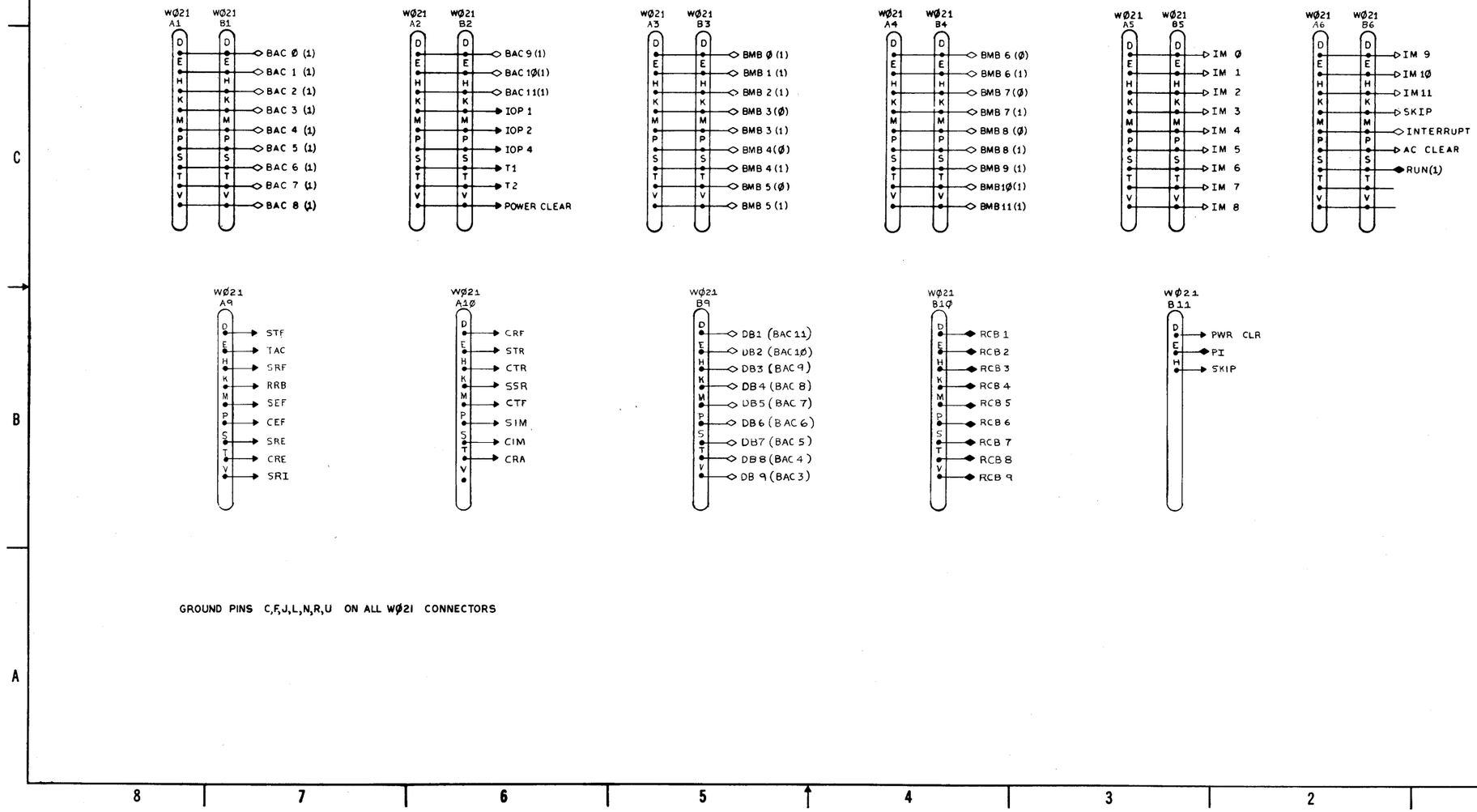
D-MU-637-0-11 Module Utilization
(Interface Section)

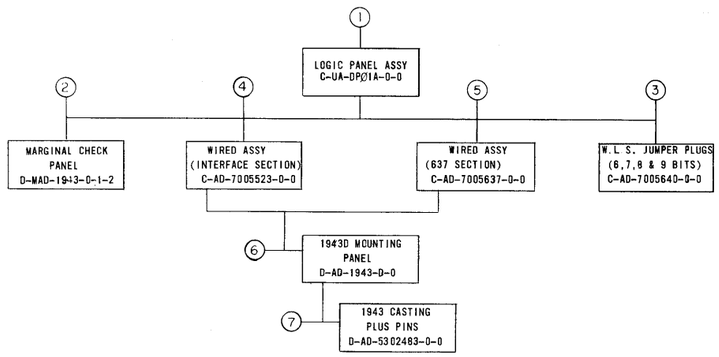
*	PDP-8	PDP-8/S
A	ME 34	E 39
B	MF 34	B 39
C	ME 35	E 40
D	MF 35	D 40
E	PE 2	E 32
F	PF 2	E 37



D-IC-637-0-12 Interconnecting Cable Diagram
(DP01A)


(SEE NOTE 1)
(SEE NOTE 2)
IOP1
IOP2
IOP4
6601
6602
6604
6611
6612
6614
6621
6622
6624
6631
6632
6634
6641
6642
6644
6651
6652
6654
6661
6662
6664
6671
6672
6674
BMB 3 (Ø)
BMB 2 (1)
BMB 4 (Ø)
BMB 5 (1)
BMB 5 (Ø)
BMB 6 (Ø)
BMB 6 (1)
BMB 7 (Ø)
BMB 7 (1)
BMB 8 (Ø)
BMB 8 (1)
* DIODES REMOVED FOR DECODING IOT'S
TAC
STF
SEF
SRI
SSR
SRF
CTF
RRB
CEF
CRF
CTR
CRA
INTERRUPT
SKIP
CIM
SIM
SRE
STR
CRE
IM11
IMIØ
IM9
IM8
IM7
IM6
IM5
IM4
IM3
RCB1
RCB2
RCB3
RCB4
RCB5
RCB6
RCB7
RCB8
RCB9
NOTES:
1. REQUIRED FOR EXCLUSIVE OR OPTION ONLY
2. PROVIDED FOR EXPANSION ONLY.
NO MODULE REQUIRED.

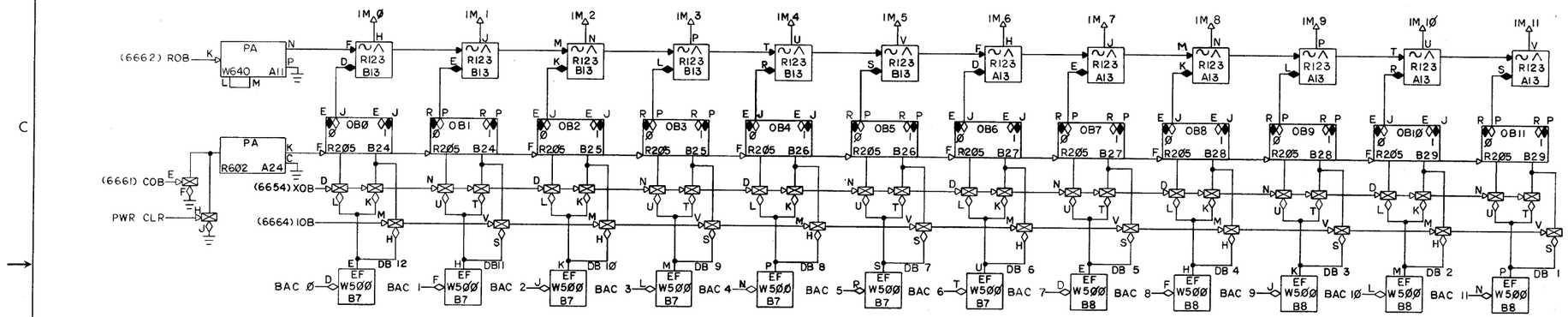

W Ø 21 A1
W Ø 21 B1
BAC Ø (1)
BAC 1 (1)
BAC 2 (1)
BAC 3 (1)
BAC 4 (1)
BAC 5 (1)
BAC 6 (1)
BAC 7 (1)
BAC 8 (1)
W Ø 21 A2
W Ø 21 B2
BAC 9 (1)
BAC 1Ø (1)
BAC 11 (1)
IOP 1
IOP 2
IOP 4
T1
T2
POWER CLEAR
W Ø 21 A3
W Ø 21 B3
BMB Ø (1)
BMB 1 (1)
BMB 2 (1)
BMB 3 (Ø)
BMB 3 (1)
BMB 4 (Ø)
BMB 4 (1)
BMB 5 (Ø)
BMB 5 (1)
W Ø 21 A4
W Ø 21 B4
BMB 6 (Ø)
BMB 6 (1)
BMB 7 (Ø)
BMB 7 (1)
BMB 8 (Ø)
BMB 8 (1)
BMB 9 (1)
BMB 1Ø (1)
BMB 11 (1)
W Ø 21 A5
W Ø 21 B5
IM Ø
IM 1
IM 2
IM 3
IM 4
IM 5
IM 6
IM 7
IM 8
W Ø 21 A6
W Ø 21 B6
IM 9
IM 1Ø
IM 11
SKIP
INTERRUPT
AC CLEAR
RUN (1)
W Ø 21 A9
STF
TAC
SRF
RRB
SEF
CEF
SRE
CRE
SRI
W Ø 21 A1Ø
CRF
STR
CTR
SSR
CTF
SIM
CIM
CRA
W Ø 21 B9
DB 1 (BAC 11)
DB 2 (BAC 1Ø)
DB 3 (BAC 9)
DB 4 (BAC 8)
DB 5 (BAC 7)
DB 6 (BAC 6)
DB 7 (BAC 5)
DB 8 (BAC 4)
DB 9 (BAC 3)
W Ø 21 B1Ø
RCB 1
RCB 2
RCB 3
RCB 4
RCB 5
RCB 6
RCB 7
RCB 8
RCB 9
W Ø 21 B11
PWR CLR
PI
SKIP
GROUND PINS C,F,J,L,N,R,U ON ALL WØ21 CONNECTORS



MECHANICAL			DEPT USAGE		
FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	LOGIC PANEL ASSY LOGIC PANEL ASSY (PL). RIGHT END PANEL CONNECTOR END PANEL DATA SET CABLE (PL) DATA SET CABLE (PL) CANNON CONNECTOR BAR-50 PIN	C-UA-DP01A-0-0 A-PL-DP01A-0-0 C-MD-1943-0-1-0-1 C-MD-7406348-0-0 D-AD-7005639-0-0 A-PL-7005639-0-0 B-MD-00647			
2	MARGINAL CHECK PANEL MARGINAL CHECK PANEL (PL)	D-MAD-1943-0-1-2 A-PL-1943-0-1-2			
3	W.L.S.JUMPER PLUGS (6,7,8 & 9 BITS) W.L.S. JUMPER PLUGS (6,7,8 & 9 BITS) (PL)	C-AD-7005640-0-0 A-PL-7005640-0-0			
4	WIRED ASSY (INTERFACE SECTION) WIRED ASSY (INTERFACE SECTION) (PL)	C-AD-7005523-0-0 A-PL-7005523-0-0			
5	WIRED ASSY (637 SECTION) WIRED ASSY (637 SECTION) (PL)	C-AD-7005637-0-0 A-PL-7005637-0-0			
6	1943D MOUNTING PANEL 1943D MOUNTING PANEL (PL)	D-AD-1943-D-0 A-PL-1943-D-0			
7	1943 CASTING PLUS PINS 1943 CASTING PLUS PINS (PL) 1943 FRAME CASTING	D-AD-5302483-0-0 A-PL-5302483-0-0 E-MD-1202885-0-0			

ELECTRICAL			DEPT USAGE		
FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	BIT SYNC DATA COMM SYS DP01A MODULE UTILIZATION RECEIVER LOGIC TRANSMIT LOGIC STD RS232 INTERFACE PDP INTERFACE WIRE LIST (637 SECTION)	A-ML-DP01A-C D-MU-637-0-9 D-BS-637-0-1 D-BS-637-0-2 D-BS-637-0-3 D-BS-637-0-4 K-WL-637-0-5			
	DP01A IOT SELECTION LOGIC DP01A I/O CONNECTORS INTERFACE DP01A O/P BUFFER WIRE LIST LOGIC ASSY TO 50 PIN CONN EXTERNAL COMPONENTS LIST (CONTROL SEC)	D-MU-637-0-11 D-BS-637-0-13 D-BS-637-0-14 K-WL-637-0-15 D-BS-DP01A-0-3 A-WL-637-0-7 A-CP-637-0-17			
2	MOUNTING PANEL 1943	B-CS-1943			
3	637 WORD LENGTH SELECTION	D-AR-637-0-9			
REF.	INTERCONNECTING CABLE DIAGRAM	D-IC-637-0-12			

D-DI-DP01A-0-1 DP01A Master Drawing Breakdown



D-BS-DP01A-0-3 OR Buffer (optional)

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