EK-MCV1D-UG-002

MCV11-D

User Guide

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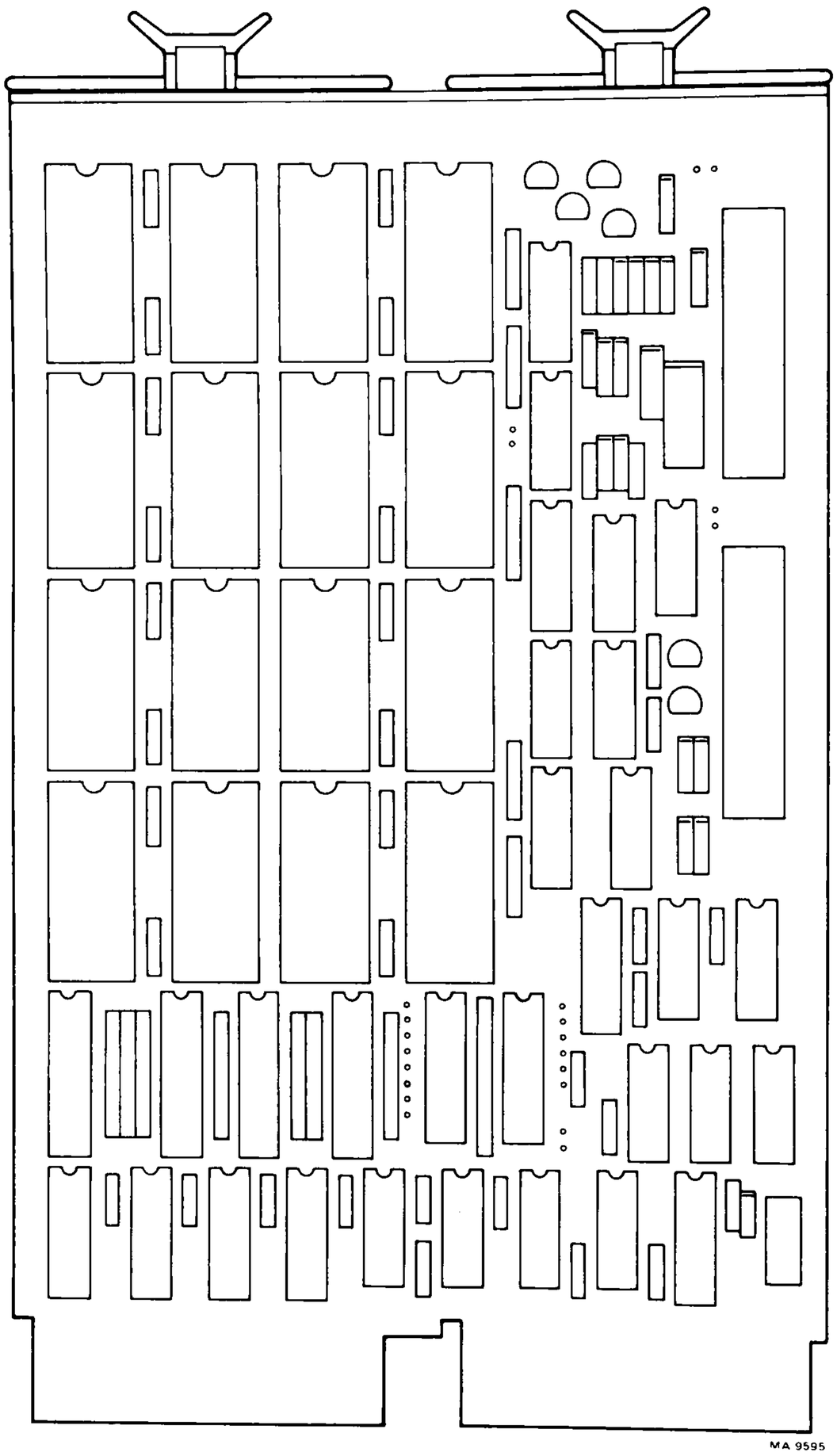


MCV11-D Memory Module

CHAPTER 1
CHARACTERISTICS AND SPECIFICATIONS

1.1 INTRODUCTION

This manual describes the MCV11-D family of memories. The MCV11-D memories are static random access memories (RAMs), using complimentary metal oxide semiconductor (CMOS) RAMs designed for use with the LSI-11 bus. The MCV11-D memories provide storage for 16-bit words. This is a QBus (LSI-11 bus) characteristic.

There are two versions of the MCV11-D memory, as shown in Table 1-1.

The MCV11-D memory modules use CMOS RAMs and Schottky TTL with no parity and operate from a single 5 V power supply. The CMOS RAM is a 16,384-bit static random access memory, organized into 2048 locations, 8-bits wide. The CMOS RAM is suited for low power applications that require battery operation or battery backup for nonvolatility. (Onboard batteries only provide data retention for battery backup applications.)

Table 1-1 MCV11-D Versions

Option Designator	Module Designator	Storage Capacity	CMOS Chips	Module Population	Number of RAMs
MCV11-DC	M8631-C	32K bytes	2K by 8	Full	16
MCV11-DA	M8631-A	8K bytes	2K by 8	Quarter	4

1.2 GENERAL DESCRIPTION

The MCV11-D consists of a single, dual-height module that contains the LSI-11 bus interface, timing and control logic, CMOS storage array and two 1.2 V rechargeable batteries.

The module starting address is jumper selectable and must start on any 4K boundary within system address space. The MCV11-D allows the lower 2K of the 4K I/O page to serve as memory locations.

NOTE: There is no address interleaving with MCV11-D memory modules.

The CMOS RAM includes the following features.

Pin compatibility with 2K × 8 EPROM, PROM, ROM
Low power dissipation
Single 5 V power supply
Data retention voltage, 2.0 V to 5.5 V
Static operation
Identical cycle and access times
Fast access time, 250 ns (max)
All inputs and outputs, directly TTL compatible
Three-state outputs
Standard 24-pin plastic package

The MCV11-D memories have two rechargeable nickel cadmium (nicad) cylindrical cells mounted on the module. Each cell is size AAA, 1.2 V nominal, with a 180 mA/hr capacity at 25° C. The battery has an estimated operating life of over five years at normal operating temperatures. A continuously high operating temperature will reduce the battery life substantially.

DIGITAL recommends that you replace batteries when they no longer provide data retention for the required period of time. This provides the longest operating life from a set of cells with a minimum maintenance cost. You should only adopt a battery replacement schedule in those applications that cannot tolerate a data retention loss due to the battery wearing out. In high temperatures where battery life is shortened, you may have to replace batteries yearly.

The main feature of the batteries mounted on the memory module is data retention. Table 1-2 shows typical and worst case data retention times.

Table 1-2 Data Retention Times

Option	Size	Typical Data Retention	Worst Case Data Retention
MCV11-DC	32K bytes	1180 hr	100 hrs
MCV11-DA	8K bytes	2647 hr	333 hrs

1.3 SPECIFICATIONS

The following paragraphs provide functional, electrical, and environmental specifications.

1.3.1 Functional Specifications

Table 1-3 shows the functional specifications for the MCV11-D.

Table 1-3 Access and Cycle Times

Bus Cycles	Access Time* Typical	Maximum	Notes	Cycle Time† Typical	Maximum	Notes
DATI	225	250	1	520	570	4
DATO(B)	50	55	2	500	550	4
DATIO(B)	590	620	3	1010	1070	5

*Tacc (ns)
†Tcyc (ns)

NOTES:

1. *R SYNC H to T RPLY H with minimum timing (25 ns) from R SYNC H to R DIN H and typical or maximum module propagation delays.*
2. *R SYNC H to T RPLY H with minimum timing (50 ns) from R SYNC H to R DOUT H and typical or maximum module propagation delays.*
3. *R SYNC H to T RPLY H (DATO portion of cycle) with minimum timing (25 ns) from R SYNC H to R DIN H and minimum timing (350 ns) from T RPLY H (DATI portion of cycle) to R DOUT H.*
4. *R SYNC H to TIM 130 H negated.*
5. *R SYNC H to TIM 130 H negated (DATO).*

1.3.2 Electrical Specifications

Electrical specifications provide voltages, current, and power requirements for the MCV11-D.

1.3.2.1 Voltage – The MCV11-D requires only 5 volts. The voltage margins are 5 V ± 5% and +5 V BBU (2.8 V - 5.25 V) for data retention use only.

Voltage	Pin	Function
+5 V	AA2, BA2, BV1	Used for control logic and normal operation.
+5 V BBU	AV1	Used for external battery backup of RAMs. Onboard batteries remain active and charged while +5 V BBU is in use. Onboard batteries will generate current when neither +5 V nor +5 V BBU is available.

NOTE: See Appendix A for data specifications or characteristics.

Table 1-4 MCV11-D Power

Current and Power		Active Mode	Standby Mode	Data Retention Mode
MCV11-DC (32K byte)				
Current	+5 V (Typ)*	1.23 A	1.22A	0
	+5 V (Max)*	2.16 A	2.15A	0
	+5 V BBU (Typ)†	1 mA	1 mA	9 mA
	+5 V BBU (Max)†	2 mA	2 mA	14 mA
Power	+5 V (Typ)	6.20 W	6.10 W	.045 W
	+5 V (Max)	11.34 W	11.29 W	.073 W
MCV11-DA (8K byte)				
Current	+5 V (Typ)*	1.20 A	1.19A	0
	+5 V (Max)*	2.09 A	2.08A	0
	+5 V BBU (Typ)†	1 mA	1 mA	9 mA
	+5 V BBU (Max)†	2 mA	2 mA	14 mA
Power	+5 V Typ	6.00 W	5.95 W	.045 W
	+5 V Max	10.97 W	10.92 W	.073 W

* The +5 V current is recorded with no +5 V BBU supply connected.

† The +5 V BBU current assumes +5 V = 4.75 V and +5 V BBU = 5.25 V. In the active and standby mode, a majority of current comes from the +5 V supply, so it appears as though very little current is required by the +5 V BBU supply. In the data retention mode, the +5 V supply is assumed to be at 0 V. The current supplied by +5 V BBU is used to trickle charge the batteries. If the batteries were disconnected, +5 V BBU would be typically 20 μA.

1.3.2.2 MCV11-D Power – Table 1-4 shows the power requirements for the MCV11-DC and MCV11-DA.

NOTE: See Appendix A for battery information.

1.3.3 Environmental Specifications

Environmental specifications cover storage and operating temperatures, relative humidity, altitude and air flow specifications for the MCV11-D.

1.3.3.1 Temperature – There are two temperature ranges for the MCV11-D, storage and operating.

Storage Temperature Range – The recommended storage temperature range is −30° to +60° C, with a −40° to +66° C range allowed for short periods.

Before operating a module stored beyond the operating temperature range, you must bring that module within the operating range. Allow the module to stabilize for a minimum of five minutes before applying power.

Operating the module outside the recommended temperature range may cause a battery failure.

Exposing a battery to high temperature (>50° C) for long periods of time accelerates self-discharge. You must recharge the battery to assure memory nonvolatility.

Operating Temperature Range – The recommended operating temperature range is +5° to +60° C. Reduce the maximum operating temperature by 1° C for each 1000 feet of altitude above 8000 feet.

Battery capacity (and therefore the length of data retention) falls off by 2 percent for every 1° C increase in temperature above 35° C. High temperatures (45° to 60° C) reduces the battery life.

1.3.3.2 Relative Humidity – The relative humidity range is 10 to 90 percent (noncondensing) for storage and operating conditions.

1.3.3.3 Operating Airflow – You must provide adequate airflow to limit the inlet to outlet temperature rise across the module to 5° C when the inlet temperature is +55° C. Operation below +50° C requires airflow to limit the inlet to outlet temperature rise across the module to 10° C maximum.

1.3.3.4 Altitude – The module will not be mechanically or electrically damaged by atmospheric pressures at altitudes up to 50,000 feet (90MM mercury), for both operating and storage conditions.

NOTE: Reduce the maximum operating temperature by 1° C for each 1000 feet of altitude above 8000 feet.

2.3 CONFIGURING THE MCV11-D MEMORY MODULE

There are five groups of MCV11-D memory module jumpers.

Module starting address jumpers
System selection jumper
Manufacturing test jumper
Memory I/O page address jumper
Memory module battery backup jumper

2.3.1 Module Starting Address (MSA) Jumpers

To configure the MSA jumpers, you need the module starting address. From the module starting address you can obtain the necessary data to configure the jumpers.

Table 2-1 is divided into two sections of jumpers.

Part 1 lists the First Address of Range (FAR). This selects the first address of the 128K range the starting address falls in.

Part 2 lists the Partial/Starting Address (PSA). This selects which 4K boundary within a specific 128K range the starting address falls in.

You can find the memory module starting address (MSA) by determining how much memory the system has in decimal K bytes. Change this byte value to a decimal K word value. This word value is the MSA.

Table 2-1 Starting Address Jumpers (Part 1)

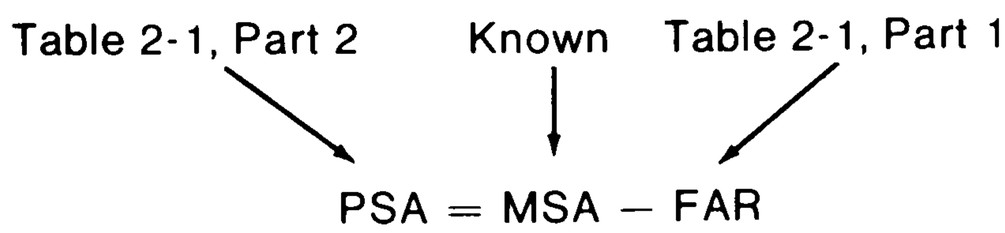
First Starting Address Range (FAR)		Jumpers In (X) to Ground (R)			
Decimal (K)	Octal	L	M	N	P
000 - 124	00000000 - 00760000	-	-	-	-
128 - 252	01000000 - 01760000	-	-	-	X
256 - 380	02000000 - 02760000	-	-	X	-
384 - 508	03000000 - 03760000	-	-	X	X
512 - 636	04000000 - 04760000	-	X	-	-
640 - 764	05000000 - 05760000	-	X	-	X
768 - 892	06000000 - 06760000	-	X	X	-
896 - 1020	07000000 - 07760000	-	X	X	X
1024 - 1148	10000000 - 10760000	X	-	-	-
1152 - 1276	11000000 - 11760000	X	-	-	X
1280 - 1404	12000000 - 12760000	X	-	X	-
1408 - 1532	13000000 - 13760000	X	-	X	X
1536 - 1660	14000000 - 14760000	X	X	-	-
1664 - 1788	15000000 - 15760000	X	X	-	X
1792 - 1916	16000000 - 16760000	X	X	X	-
1920 - 2044	17000000 - 17760000	X	X	X	X

Table 2-1 Starting Address Jumpers (Part 2)

Partial Starting Address (PSA)		Jumpers In (X) To Ground (F)				
Decimal (K)	Octal	A	B	C	D	E
0	00000000	–	–	–	–	–
4	00020000	–	–	–	–	X
8	00040000	–	–	–	X	–
12	00060000	–	–	–	X	X
16	00100000	–	–	X	–	–
20	00120000	–	–	X	–	X
24	00140000	–	–	X	X	–
28	00160000	–	–	X	X	X
32	00200000	–	X	–	–	–
36	00220000	–	X	–	–	X
40	00240000	–	X	–	X	–
44	00260000	–	X	–	X	X
48	00300000	–	X	X	–	–
52	00320000	–	X	X	–	X
56	00340000	–	X	X	X	–
60	00360000	–	X	X	X	X
64	00400000	X	–	–	–	–
68	00420000	X	–	–	–	X
72	00440000	X	–	–	X	–
76	00460000	X	–	–	X	X
80	00500000	X	–	X	–	–
84	00520000	X	–	X	–	X
88	00540000	X	–	X	X	–
92	00560000	X	–	X	X	X
96	00600000	X	X	–	–	–
100	00620000	X	X	–	–	X
104	00640000	X	X	–	X	–
108	00660000	X	X	–	X	X
112	00700000	X	X	X	–	–
116	00720000	X	X	X	–	–
120	00740000	X	X	X	X	–
124	00760000	X	X	X	X	X

NOTE: To obtain any starting address on 4K boundaries from 0 – 124K, wirewrap daisy chain fashion from pin F, which is grounded to each successive pin labeled with X for that address.

To jumper the module starting address (MSA), proceed as follows.



You can find the FAR jumpers by identifying the 128K word range that contains the MSA value. In this case the MSA is 336K and is located in the third group of 128K words. The FAR value for this MSA (336K words) is 256K. Use Table 2-1, Part 1 and locate 256K words; this shows pin W wirewrapped to pin R (the ground pin).

You can find the PSA jumpers by solving the equation.

PSA = MSA − FAR
PSA = 336K − 256K
PSA = 80K

Use Table 2-1, Part 2 and locate 80K words; this shows pin A wirewrapped to pin C, which is wirewrapped to pin F (the ground pin).

Following are two additional examples of how to determine the correct module jumpers from an MSA value. These examples show how the MSA jumper pins are found.

Example 1
The system has 512K bytes of memory. To jumper the memory module, change this byte value (512K) to a word value (256K). This word value is the MSA.

Insert this value into the equation.

PSA = MSA − FAR
PSA = 256K − FAR

To find the value of FAR use Table 2-1, Part 1 and locate the address range that the MSA value falls in. Take the first address of the address range and insert it into the equation.

PSA = MSA − FAR
PSA = 256K − 256K
PSA = 0K

Use Table 2-1, Part 1 and locate the FAR value (256K words). This means pin N wirewraps to pin R (ground pin).

Use Table 2-1, Part 2 and locate the PSA value (0K words). This means no wirewraps on pins A, B, C, D, and E.

Example 2
The system has 672K bytes of memory. To jumper the memory module, change this byte value (672K) to a word value (336K). This word value is the MSA.

Insert this value into the equation.

PSA = MSA − FAR
PSA = 336K − FAR
PSA = 336K − 256K
PSA = 80K

Use Table 2-1, Part 1 and locate the FAR value (256K words). This means pin N wirewraps to pin R (ground pin).

Use Table 2-1, Part 2 and locate the PSA value (80K words). This means pin A wirewraps to pin C and pin C to pin F.

2.3.2 Determining the MSA by Identifying the MSA Jumpers

Remove the module from the backplane and locate the MSA jumpers. List the MSA pins that are jumpered. Refer to Table 2-2 and mark an X under the pin names that have wirewraps on them. Add the binary weights associated with the jumper pin names that have an X. The result will be the MSA.

Table 2-2 shows jumper pin names N, A and C have Xs associated with the pins. Add the binary weights. The result is the memory module starting address (MSA).

Pins	Binary Weight
N	256K
A	64K
C	16K
MSA =	336K

Table 2-2 Read Starting Address Jumper (Example – 352K Words)

Names	Starting Address Range				Partial Starting Address Range				
Decimal K words binary address	1Meg	512K	256K	128K	64K	32K	16K	8K	4K
BDAL values	21	20	19	18	17	16	15	14	13
BDAL bits	0	0	1	0	1	1	0	0	0
Jumper pin names	L	M	N	P	R	A	B	C	D	E	F
Jumper pins											

2.3.3 System Selection Jumper

Small/large system selection is set by the condition of jumper pin J. Small systems use 16- or 18-bit addressing, with pin J unconnected. Large systems use 22-bit addressing, with pin J wrapped to pin R.

2.3.4 Manufacturing Test Jumper

This jumper, when installed (pin T to pin S), allows addresses to start at 128K. The jumper is installed during manufacturing test. When the modules leave manufacturing test, the jumper is removed.

2.3.5 Memory I/O Page Address Jumper

When a customer wants to use the bottom 2K of the I/O space as a memory address, jumper U to V.

2.3.6 Memory Module Battery Backup Jumper

When you receive an MCV11-D memory, there will be two 1.2 V rechargeable nicad batteries. Pins Y and Z are the clip carrier pins (no electronic function); they should have a clip across them. Remove the clip and connect it across pins W and X. This installs module battery backup.

CHAPTER 3
FUNCTIONAL DESCRIPTION

3.1 MEMORY AND THE LSI-11 BUS

The MCV11-D memory modules interface with the LSI-11 bus (Figure 3-1).

The bus master device, CPU or DMA, initiates commands to memory. As a result, the memory modules are slaves to the bus master. Devices must gain control of the LSI-11 bus before data transfers can occur. Devices gain control of the bus by arbitration in the CPU or by a user-defined controller. The device that wins the arbitration becomes bus master as soon as the LSI-11 bus signals BSYNC and BRPLY are negated. This bus master device can then transfer data.

The bus master is now ready to issue commands. These commands initiate a bus cycle. Table 3-1 shows the type of bus cycles the bus master can perform.

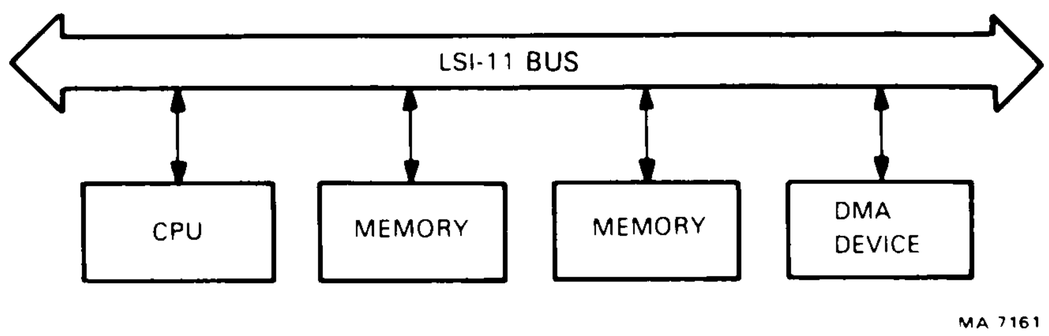


Figure 3-1 Typical System

Table 3-1 Bus Cycle Summary

Bus Cycle Mnemonics	Description	Function with Respect to Bus Master
DATI	Data word input	Read word.
DATO	Data word output	Write word.
DATOB	Data byte output	Write byte.
DATIO	Data word input/output	Read word, modify, write word.
DATIOB	Data word input/byte outputs	Read word, modify, write byte.

Bus cycles include the following sequential events.

Address cycle
Data cycle
Termination of the bus cycle

The memory uses the following LSI-11 bus signals (Figure 3-2) to perform DATI, DATO(B), and DATIO(B) bus cycles.

The signal BDCOK L allows the memory to sense dc power.

3.1.1 LSI-11 Bus Signals

Table 3-2 lists the LSI-11 bus signals, with active levels and definitions.

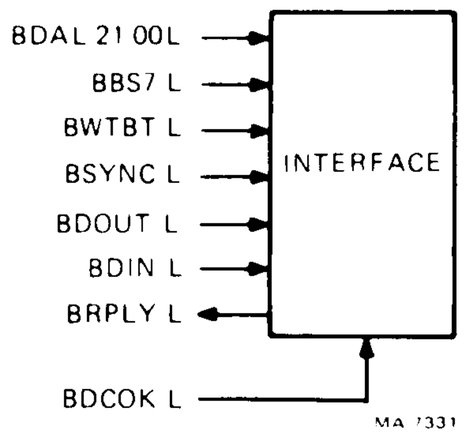


Figure 3-2 MCV11-D Memory Interface

Table 3-2 LSI-11 Bus Signals

Signal Names	Cycle	Definitions
Bus Data Address Lines (BDAL 21–00 L)	Address	BDAL 21–00 L is received and decoded as an address by the slave (memory).
	Data Write	When the bus master does a memory write, DATO(B), or DATIO(B), the data transfers on BDAL 15–00 L.
	Data Read	The bus master receives data on BDAL 15–00 L.
Bus Write/Byte (BWTBT L)	Address	When BWTBT is active, a write operation is enabled. When BWTBT is negated, a read operation is enabled.
	Data	If BWTBT is active during the data cycle, the write operation performed is "WRITE BYTE." Address bit 0 tells the logic what byte will be modified. If BWTBT is negated during the data cycle, the write operation performed is "WRITE WORD."

Table 3-2 LSI-11 Bus Signals (Cont)

Signal Names	Cycle	Definitions
Bus Bank 7 Select (BBS7 L)	Address	The bus master generates BBS7 during the address cycle and removes the signal at the end of the address cycle. The memory on receiving the signal BBS7 L generates BS7 H. BS7 H means two things. 1. The address being received is an I/O address and inhibits MEM SEL L, which prevents memory reads or writes. 2. If pins Q and R are jumpered and DAL 12 H, the customer can use the lower 2K of I/O address space as memory addresses. BBS7 L negated (BBS7 H) means the address on the LSI-11 bus is a memory address. The PROMs decode the received address against the starting address. If the address is within the range of the memory module, MEM SEL L is generated. This allows a read or write request to be serviced.
Bus Synchronize (BSYNC L)	Address Data	BSYNC L is asserted by the bus master to indicate that it has placed an address on the LSI-11 bus. The transfer is in progress until BSYNC L is negated. When the memory receives BSYNC L, it resets the LAT SYNC flip-flop, which does the following. • Enables the read/write request signals. • Latches DAL00–DAL12, N/A 13, N/A 14, and WTBT L. • Enables RPLY for DOUT operations. • Allows signal WTBT to be decoded. • Enables timing logic.
Bus Data Input (BDIN L)	Data	When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master and requires a response (BRPLY) from the addressed slave (memory). When memory receives BDIN L, it enables RPLY (covered later under BRPLY). LAT DOUT H is negated; when RPLY L is generated, the data is gated on the BDAL bits 15–00.

Table 3-4 Dialogue DATO(B) Cycle (Cont)

Bus Master	Memory
	The address is gated into the RAMs when row select (Row 0–7 L) becomes active. The signal OE (chip output enable) has no effect because WT BYTE is active, telling the control section of the RAMs that a write operation is about to occur and the data is on the tristate bus. As soon as the WT BYTE signal or signals is negated, the data is written into the selected RAMs. **Termination of Bus Cycle**
Bus master receives BRPLY L and removes data and BDOUT L from the LSI-11 bus.	When generated, BRPLY L is sent out on the LSI-11 bus.
Bus master negates BDOUT.	Memory receives BDOUT negated and negates BRPLY.
Bus master receives BRPLY L negated, which negates BSYNC. This terminates the bus cycle.	

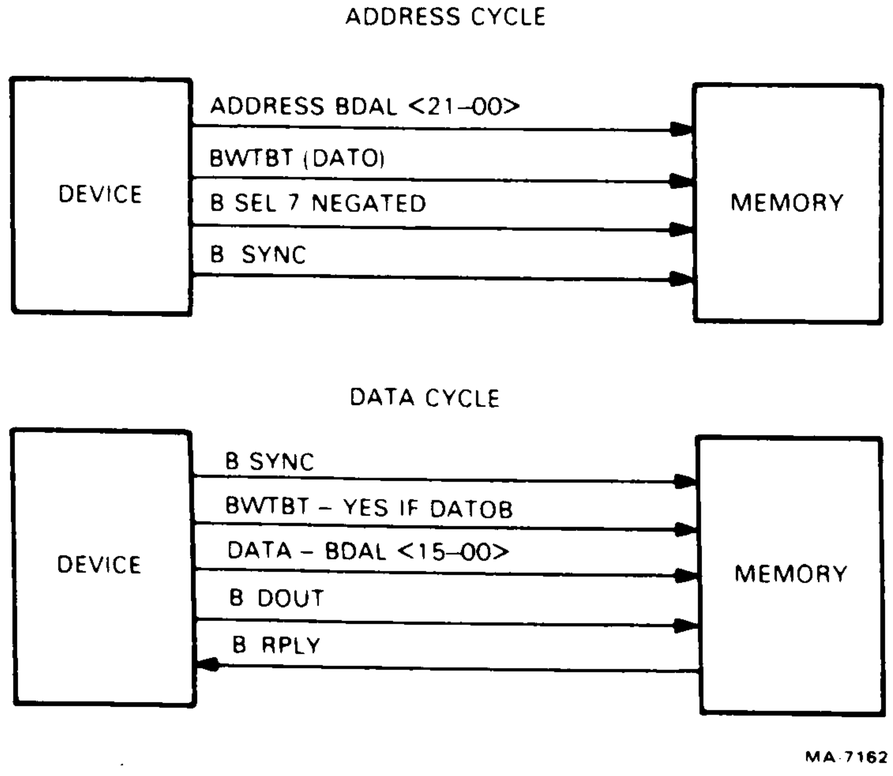


Figure 3-3 Dialogue DATO(B)

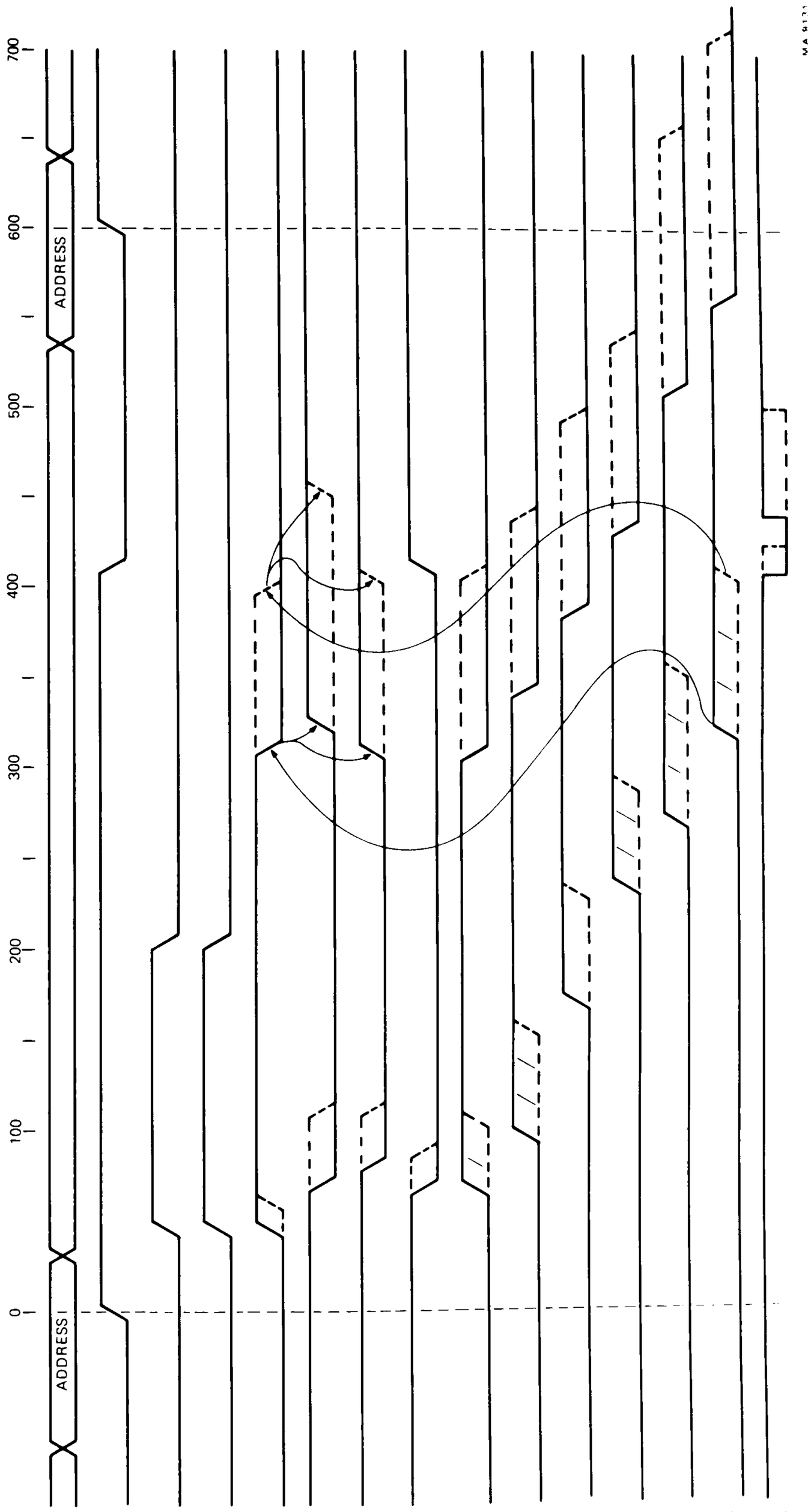


Figure 3-4 DOUT Signal Sequence (Minimum QBus Timing)

Table 3-5 Dialogue DATI Cycle

Bus Master	Memory
	Address Cycle
BDAL 21–00L	Memory receives the address and accepts or rejects it, depending on how the module was jumpered. The memory module that accepts the address generates MSEL L, provided BS7 H, B REF L, B INIT, and LOCKOUT H are negated.
BBS7 L	BBS7 L asserts only during a peripheral page access. This memory cannot be selected with BBS7 asserted. The only exception occurs when the starting address is jumpered into this area and a wirewrap is installed between Q and R. The signal BS7 H negated enables the address decode logic to generate MSEL L; this means a specific memory module has been selected.
BWTBT (NEGATED) H	When the memory receives the signal BWTBT H, the RD REQ gate is enabled.
BSYNC L	When the memory module has been selected (MSEL L) and SYNC H becomes active, the signal LAT SYNC is generated. The memory module uses SYNC H and LAT SYNC to perform the following tasks. • Latches the address. • Asserts RD REQ H, which initiates memory timing and row selection. (TIM 25 generates OE (output enable) and approximately 250 ns after row selection data appears on the data tristate bus). • Removes the clear signal from the WT REQ FF. • Enables the clock signal for the END FF. • Enables RPLY for a DIN cycle. • Removes clear from write word/byte FF. • Enables the LAT DOUT FF.
	Data Cycle
Bus master takes the address of the LSI-11 bus.	
BSYNC L	Still active.
BDIN L	When memory receives BDIN L, it responds with BRPLY. Reply allows the transmitters to transfer the read data on the LSI-11 bus. Approximately 250 ns after row selection (Row 0–7 L) the data is on the memory tristate bus. From the tristate bus the data travels through the transmitters to the bus master via the LSI-11 bus.

Table 3-5 Dialogue DATI Cycle (Cont)

Bus Master	Memory
	Termination of Bus Cycle
	Memory sends BRPLY L to the bus master.
Bus master receives BRPLY L, indicating memory will place data on the BDAL lines. BRPLY L negates BDIN L.	
	Memory receives BDIN negated and negates BRPLY L.
Bus master receives BRPLY L negated, which negates BSYNC. This terminates the bus cycle.	

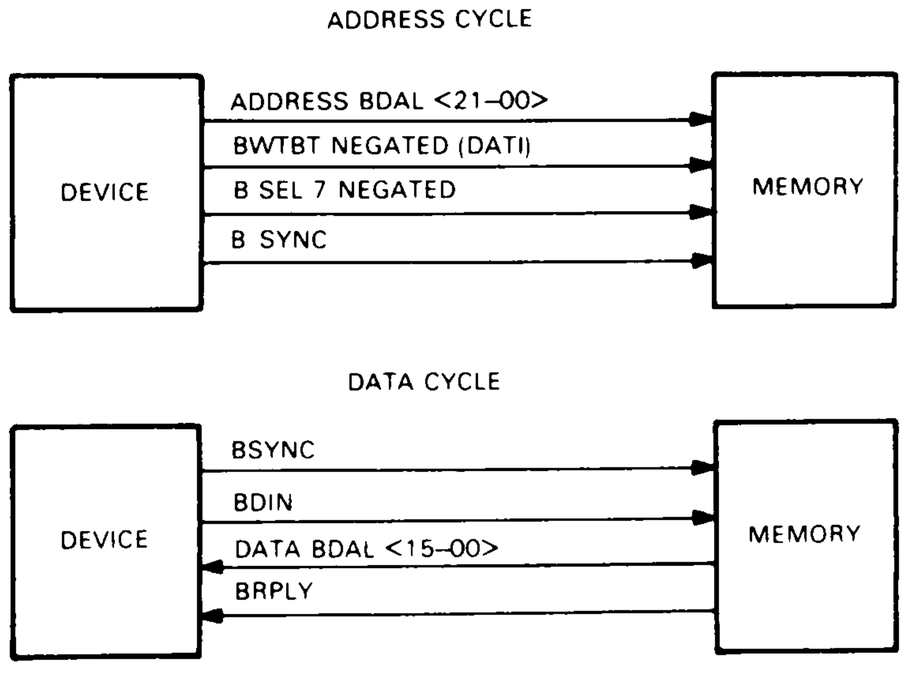


Figure 3-5 Dialogue DATI

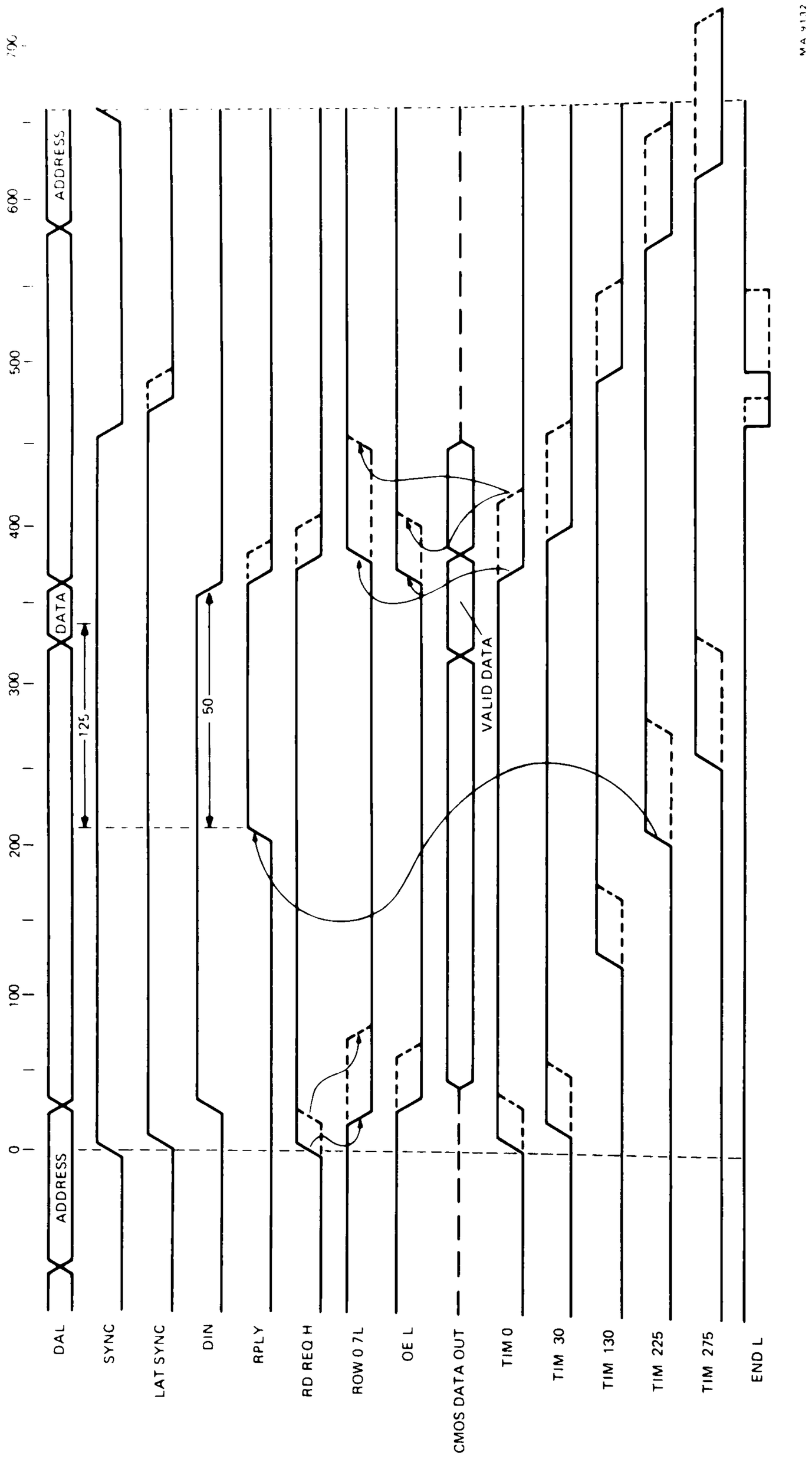


Figure 3-6 DIN Signal Sequence (Minimum QBus Timing)

Table 3-6 Dialogue DATIO(B) Cycle

Bus Master	Memory
	Address Cycle
BDAL 21–00 L	When SYNC asserts, memory receives the address and is selected if the address falls within the module's selected address range. The memory module that accepts the address generates MSEL L, provided BS7 H and LOCKOUT H are negated.
BBS7 L	BS7 H negated enables the address decode logic to generate MSEL L; this means a specific memory module has been selected.
BWTBT (NEGATED) H	When SYNC asserts, memory receives BWTBT H; this enables the RD REQ gate.
BSYNC L	When the memory module is selected (MSEL L) and SYNC H becomes active, LAT SYNC is generated. The memory module uses SYNC H and LAT SYNC to perform the following tasks. • Latches the address. • Asserts RD REQ H, which initiates memory timing and row selection. TIM 25 generates OE (output enable); approximately 250 ns after row selection data appears on the data tristate bus. • Enables WT REQ FF. • Removes clear signal from WT REQ FF. • Enables clock signal for END FF. • Enables BRPLY for a DIN cycle. • Removes clear from WRITE word/byte FF. • Enables the LAT DOUT FF.
	Data Cycle
Bus master takes the address off the LSI-11 bus.	
BSYNC L	Still active.
BDIN L	When memory receives BDIN L, it enables BRPLY L; approximately 209 ns from the leading edge of BSYNC L, the transmitters are enabled to transfer read data on the LSI-11 bus. Approximately 250 ns after row selection (Row 0–7 L) the data is on the memory tristate bus. From the tristate bus the data travels through the transmitters to the bus master via the LSI-11 bus.
Bus master receives BRPLY L, indicating memory will place its data on the BDAL lines and negate BDIN L. Bus master receives the data.	

Table 3-6 Dialogue DATIO(B) Cycle (Cont)

Bus Master	Memory
	Pause
BSYNC	Still active.
BDIN L negated	When memory receives BDIN L negated, it removes data from the BDAL lines by negating BRPLY L.
Bus master receives BRPLY L negated and gets ready to output data.	BRPLY L negated to the LSI-11 bus.
	Data Cycle
BSYNC L	Still active.
BWTBT L	Memory receives BWTBT L. BWTBT still active – write byte. BWTBT negated – write word.
BDAL 15–00 L (DATA)	Memory receives the input data to two octal D-type transparent latches and edge-triggered FFs (SN74S373). The signal WT BYTE at this time is negated. This means the outputs of the two SN74S373s have high impedance (Z).
BDOUT L	Memory receives BDOUT L and the following events occur. • BRPLY L is generated and sent back to the bus master via LSI-11 bus. • WT REQ H gets set and initiates memory timing. As soon as WT BYTE 0 and/or 1 are generated, two events occur. • Data is gated on the 2K × 8 RAM tristate bus as CMOS memory input. • CMOS control (BWBT L) determines write word or write byte. The address is gated into the CMOS RAM when row select becomes active (Row 0–7 L). OE (chip output enable) has no effect because WT BYTE is active, telling the control section of the CMOS that a write operation is about to occur and data is on the tristate bus. As soon as the WT BYTE signal or signals is negated, data is written into the selected CMOS RAM.

Table 3-6 Dialogue DATIO(B) Cycle (Cont)

Bus Master	Memory
	Termination of Bus Cycle
	BRPLY L
Bus master receives BRPLY L and removes data and BDOUT L from the LSI-11 bus.	
BDOUT negated.	
	Memory receives BDOUT negated and negates BRPLY L.
Bus master receives BRPLY L negated, which negates BSYNC. This terminates the bus cycle.	

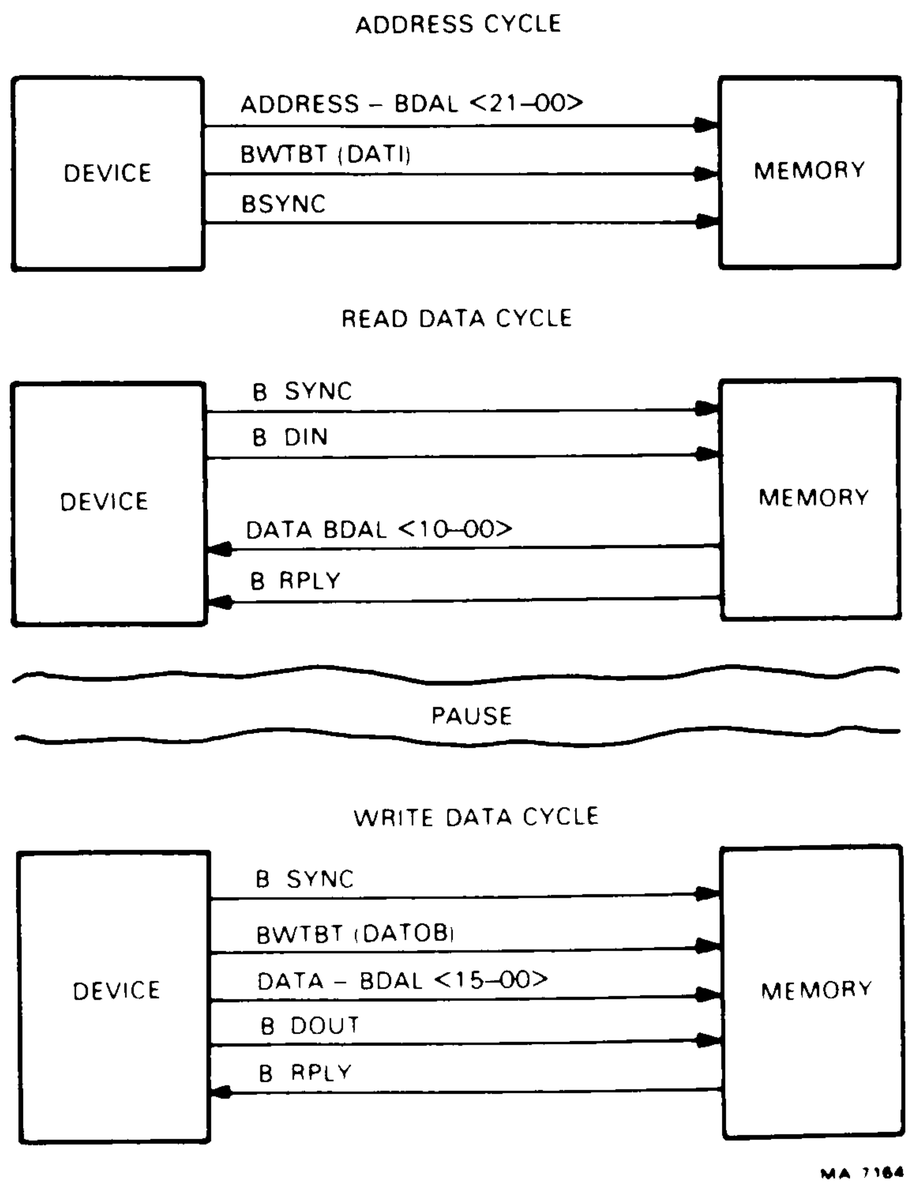


Figure 3-7 Dialogue DATIO(B)

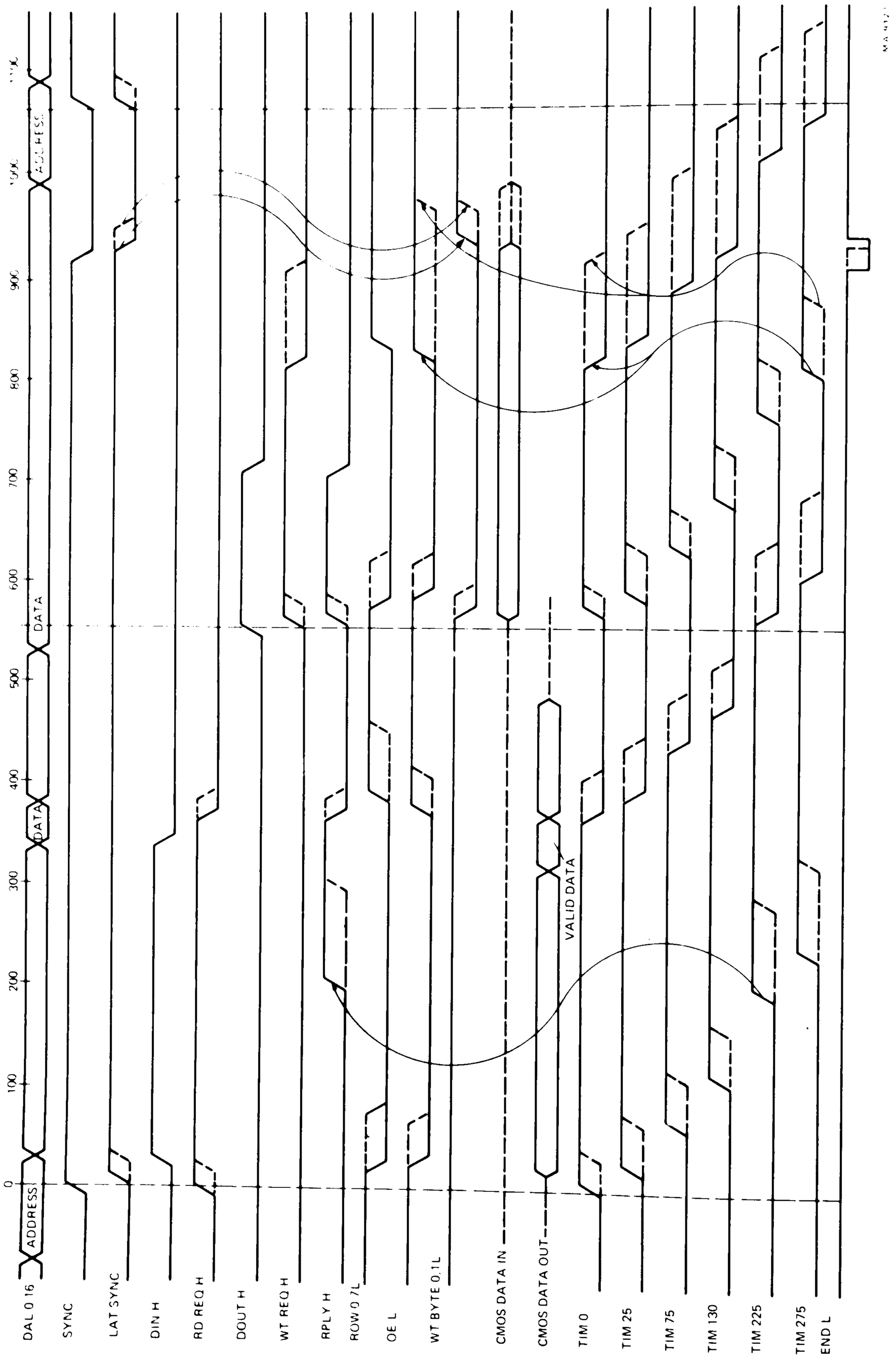


Figure 3-8 DATIO Signal Sequence (Minimum QBus Timing)

3.1.3 Functional Block Diagram Description

Figure 3-9 shows the relationship of the MCV11-D functional blocks. The following paragraphs discuss each block of the MCV11-D memory module.

Interface - The interface connects the memory to the LSI-11 bus by transceivers. The interface is divided into two sections.

Address/data
Control

The address section receives bus data address lines (BDAL) 21-00. The data then transfers on BDAL 15-00.

The interface monitors the address lines and sends DAL bits 21-13 to the module selection block. DAL bits 12-00 are sent to the address latch and latched if the memory module is selected. The data transfers from BDAL 15-00 to memory on memory writes, and from memory to BDAL 15-00 on memory read.

The control section passes control into the memory to govern the memory's operation (read, write, etc.). This sends control signals to the control and timing section, and WTBT1 to the address latch.

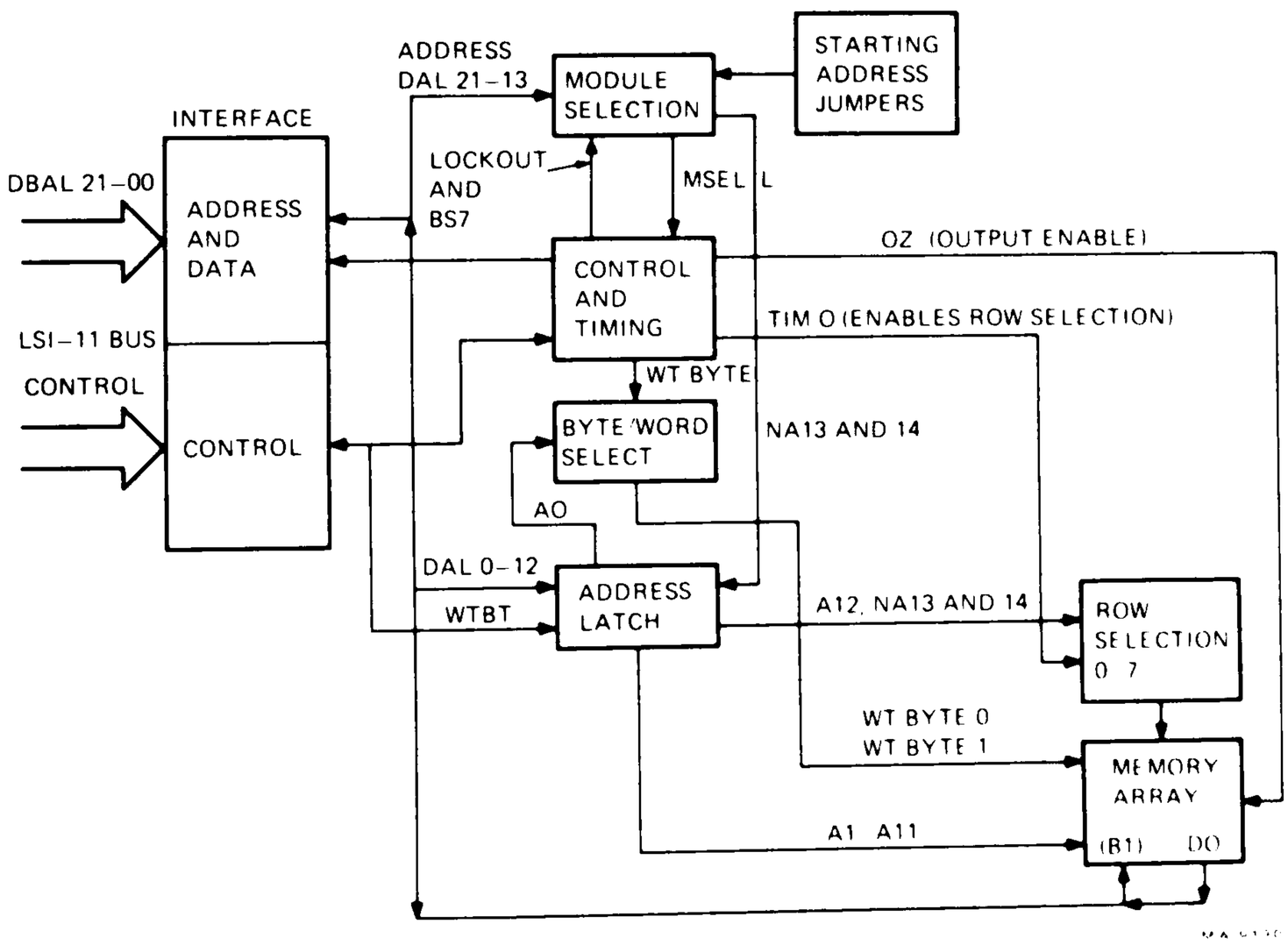


Figure 3-9 Functional Block Diagram

Module Selection - There are two PROMs in the module selection block. These PROMs monitor the address lines (BDAL 21-13) and compare them to the starting address jumpers.

The M8631-C PROMs are programmed to recognize four groups of 4K words. The starting address jumpers indicate the first address of the four groups. If the address received belongs to one of the four groups, the PROMs enable the module to be selected (MSEL L) and indicate what group the address belongs to (N/A14 and N/A13).

The M8631-A PROMs are programmed to recognize one group of 4K words. The starting address jumpers indicate the first address of the group. If the address received belongs to the memory module, the PROMs enable the memory module to be selected (MSEL L) and indicate the group the address belongs to (N/A14 and N/A13). In this case N/A14 and N/A13 are both low.

Address Latch - The address latch stores DAL 12-00, WTBT, N/A13, and N/A14 when the memory module is selected and BSYNC received. The address latch does the following tasks.

1. Sends the address to the memory array (A1–A11).

2. Sends the row selection control (N/A14, N/A13, and A12) to the row selection block.

3. Sends address bit A0 to the byte/word select block.

Control and Timing - When a memory module is selected and it receives a DIN or DOUT, the memory module generates a read or write request. The request initiates the timing.

The timing signals that this request generates are TIM 0 H, TIM 30, TIM 75, TIM 130, TIM 225, and TIM 275 H. At this time specific control signals are developed.

Example

TIM 0 H enables row selection logic.
TIM 0 H and TIM 30 H develop the control signal OE (output enable).

Memory Array - A memory read is performed when OE and ROW are active, *and* WTBYTE 0 and-WTBYTE 1 are negated.

A memory write is performed when the WTBYTE signal(s) and ROW are asserted.

OE asserts during the memory read or write cycles, but only functions during a memory read cycle (when the data is gated from the CMOS RAMs onto a tristate data bus, D00-D15).

Byte/Word Select - When the memory module receives data, it writes the data, word, or byte format into the CMOS RAM. The WTBT is monitored twice.

1. During an address cycle
   a. WTBT active means a write cycle.
   b. WTBT negated means a read cycle.

2. During a data cycle
   a. WTBT active means write byte.
      A0 H means write upper byte (WTBYTE 1 L).
      A0 L means write lower byte (WTBYTE 0 L).

   b. WTBT negated means write word and generate signals WTBYTE 1 L and WTBYTE 0 L.

NOTE: The byte not selected during a WTBT operation performs a dummy read.

3.1.4 Power-Down/Power-Up (LOCKOUT)

During a power-down cycle, BDCOK H deasserts; this indicates that the power supplies will shut down after 1 ms (minimum). Also, all signals on the LSI-11 bus will go to an unknown, uncontrolled state.

When BDCOK H deasserts, it asserts the lockout signal; this prevents an unwanted memory cycle that could destroy data in one or more memory locations during a power-down. Lockout prevents an access to memory during a power-down cycle, by locking row 0-7 into the unasserted state (high). The lockout initializes the control logic (END CLR) and switches to battery backup by shutting off the voltage transistors (Q5 and Q6) that feed the RAMs.

On a power-up cycle, the power supplies come into tolerance while BDCOK H is still deasserted. Within 400 ns of BDCOK H assertion, the lockout signal deasserts, enabling the series pass transistors (Q5 and Q6), initializing logic (END CLR), and unlocking the array for memory accesses.

Figure 3-10 shows the Power-Up/Power-Down Timing Diagram.

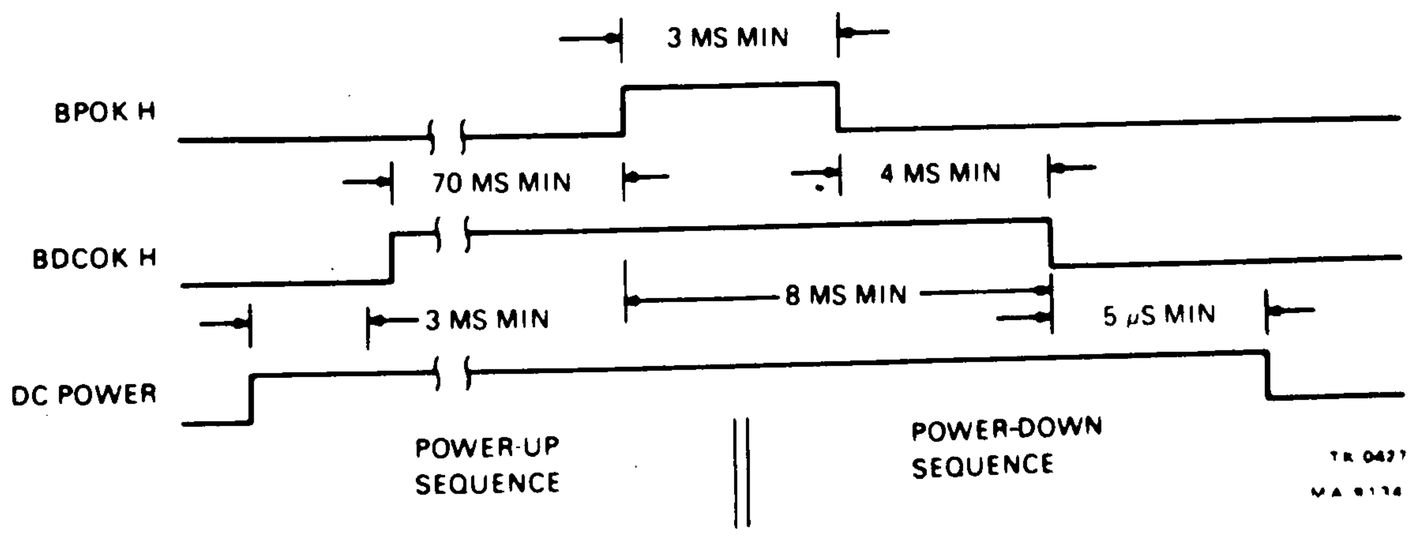


Figure 3-10 Power-Up/Power-Down Timing Diagram for QBus Power-Fail Conditions

3.1.5 PROMs

There are two memory modules.

M8631-C module has 32K bytes of memory. (Requires eight row selections.)

M8631-A module has 8K bytes of memory. (Requires two row selections.)

The memory module starting address (MSA) is jumper selectable. The logic used to monitor addresses requires two PROMs. The PROM outputs generate enables to the MSEL L logic and normalized address bits N/A13, N/A14 for row selection.

There are three types of PROMs.

E21	(M8631-C and M8631-A)	The E21 PROMs are programmed the same because high-order bits (DAL 18-21, INIT and high-order bits (DAL 18-21, INIT and REF) are the same.
E19	(M8631-C only)	The E19 PROMs are programmed differently because of different-size memory modules.
E19	(M8631-A only)	

All starting addresses must start on 4K word boundaries. The PROM jumper inputs establish the starting address of a memory module.

The M8631-C PROMs are programmed to recognize four groups of 4K words. These groups define the state of PROM output bits N/A14 and N/A13 (normalized address bits) as follows.

Group 0	N/A14 = L, N/A13 = L
Group 1	N/A14 = L, N/A13 = H
Group 2	N/A14 = H, N/A13 = L
Group 3	N/A14 = H, N/A13 = H

Table 3-7 gives four examples of PROMs response to the following conditions. (See the MCV11-DC Print Set, MP-01309.)

- Starting address jumpers set for 0000 0000.
  Starting address is 0K.

- Starting address jumpers set for 0002 0000.
  Starting address is 8K.

- Starting address jumpers set for 0076 0000 (M8631-C only). The DAL lines 17-13 are all high. This means the next three address groups have C(H) and S(L) in E19 and E21 (carry from E19 PROM to E21 PROM).

  NOTE: C is the carry signal. S is the select signal.

- The following four signals inhibit MSEL L from occurring: LOCKOUT, BS7, INIT, and REF.

The M8631-A PROMs are programmed to recognize only one group of 4K words. This means that PROM output bits N/A14 and N/A13 will always be low. The starting address jumper points to the first memory address the memory module will accept. Control signals DAL 12, N/A13, and N/A14 determine which pair of CMOS RAMs are selected through a one-of-eight decoder.

3.1.6 Batteries

See Appendix A.

3.1.7 Module Handling and Portability

See Appendix B.

Table 3-7 PROM Table for M8631-C Module

E21 Input Pins						E21 DAL Lines				E21 Output Pins				E19 Input Pins						E19 DAL Lines					E19 Output Pins					
Bit		Jumpers				21	20	19	18	S	C	–	–	Jumpers						17	16	15	14	13	C	S	N/A 14	N/A 13		Address
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	04	03	02	01	A9	A8	A7	A6	A5		A4	A3	A2	A1	A0	04	03	02		01	Range
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	H		L	L	L	L	L	L	H	L		L	0000 0000
																														0001 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	H		L	L	L	L	H	L	H	L		H	0002 0000
																														0003 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	H		L	L	L	H	L	L	H	H		L	0004 0000
																														0005 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	H		L	L	L	H	H	L	H	H		H	0006 0000
																														0007 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	L		L	L	L	L	H	L	H	L		L	0002 0000
																														0003 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	L		L	L	L	L	H	L	L	H		H	0004 0000
																														0005 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	L		L	L	L	L	H	H	L	H		L	0006 0000
																														0007 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	H	H	H	H	L		L	L	L	H	L	L	L	H		H	0010 0000
																														0011 7776
L	L	H	H	H	H	L	L	L	L	H	L	*	*	L	L	L	L	L		H	H	H	H	H	L	H	L		L	0076 0000
																														0077 7776
L	L	H	H	H	H	L	L	L	H	L	H	*	*	L	L	L	L	L		L	L	L	L	L	L	H	L		H	0100 0000
																														0101 7776
L	L	H	H	H	H	L	L	L	H	L	H	*	*	L	L	L	L	L		L	L	L	L	L	H	H	L		L	0102 0000
																														0103 7776
L	L	H	H	H	H	L	L	L	H	L	H	*	*	L	L	L	L	L		L	L	L	L	H	L	H	L		H	0104 0000
																														0105 7776
H	L									L	L	*	*																	
L	H									L	L	*	*																	
H	H									L	L	*	*																	

Both outputs low inhibit M SEL L.

* Don't care

CHAPTER 4
MAINTENANCE

4.1 GENERAL

This chapter covers the maintenance procedures that apply to both versions of the MCV11-D. In order to perform corrective maintenance on this product, you should understand the basic operation of the MCV11-D as described in the previous chapters. This knowledge together with adequate diagnostic testing knowledge should aid in the isolation of MCV11-D malfunctions.

NOTE: All power must be off before installing or removing modules. Make sure the component side of the memory always faces in the same direction as the other modules within the LSI-11 system.

4.2 PREVENTIVE MAINTENANCE

The MCV11-D does not require preventive maintenance or adjustments. This memory is self-contained.

The rechargeable nicad batteries are a chemical source of energy. They will wear out with years of use. This wear is indicated by a slow reduction in data retention time rather than an abrupt inability to carry a charge. Battery replacement is the only recommended method of returning full data retention capacity to the system.

NOTE: With power off, the batteries still have voltage on them. Nicad batteries can deliver high currents if shorted. Avoid shorting out batteries by proper handling of the module.

4.2.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other defects.

4.2.2 Power Voltage Check

The MCV11-D uses the following power sources.

+5 V only
+5 V BBU (if available)
Two 1.2 V nicad batteries

Measure the +5 V from backplane pins AA2, BA2, and BV1 to ground The ground pins on the backplane are AJ1, AM1, AT1, BJ1, BM1, BT1, AC2, and BC2.

Measure the +5 V BBU from backplane pin AV1 to ground.

The two 1.2 V batteries connect in series. To make this voltage check, proceed as follows.

- Turn off power and remove the memory module from the backplane.
- Be careful - do not short the batteries. Nicad batteries deliver high currents if directly shorted.
- Measure the voltage from pin 24 of the RAM to the ground pin (pin 12) on the RAM chip.

  The voltage you read from pin 24 to pin 12 is the battery voltage minus the voltage drop across R18.

  If the voltage at the chip reads 0 V, make sure the jumper clip is installed. If installed, refer to Paragraph A.3.4 for diagnosing a data retention problem.

4.2.3 Charge/Discharge Cycles

The charge rate for the batteries is approximately 12 mA as long as +5 V is present. It takes 24 hours to totally charge a fully discharged battery. One hour of charge replaces approximately 1/24 of the total charge.

Discharge rates vary much less than a C/100 rate (capacity 180 mA/hrs/100 = 1.8 mA/hrs). The longer the system is shut down, the less capacity the battery has for data retention.

If system shutdown is too long, a data loss results.

Figure 4-1 graphs the effect of temperature on the capacity of a new battery. Characteristics of batteries are different and fall within the range. Different brands of new batteries show various capacities when fully charged at different temperatures. As temperature increases, each battery loses some capacity.

Figure 4-2 shows an example of charge/discharge at 25° C. The batteries are fully charged at 8 am Thursday. When the system is running during the day, the batteries charge at the rate of 1/24 of total capacity per hour. When shut down, the batteries start discharging (Figure 4-2). There are three different charge/discharge times.

Week days
Weekends
Long weekends

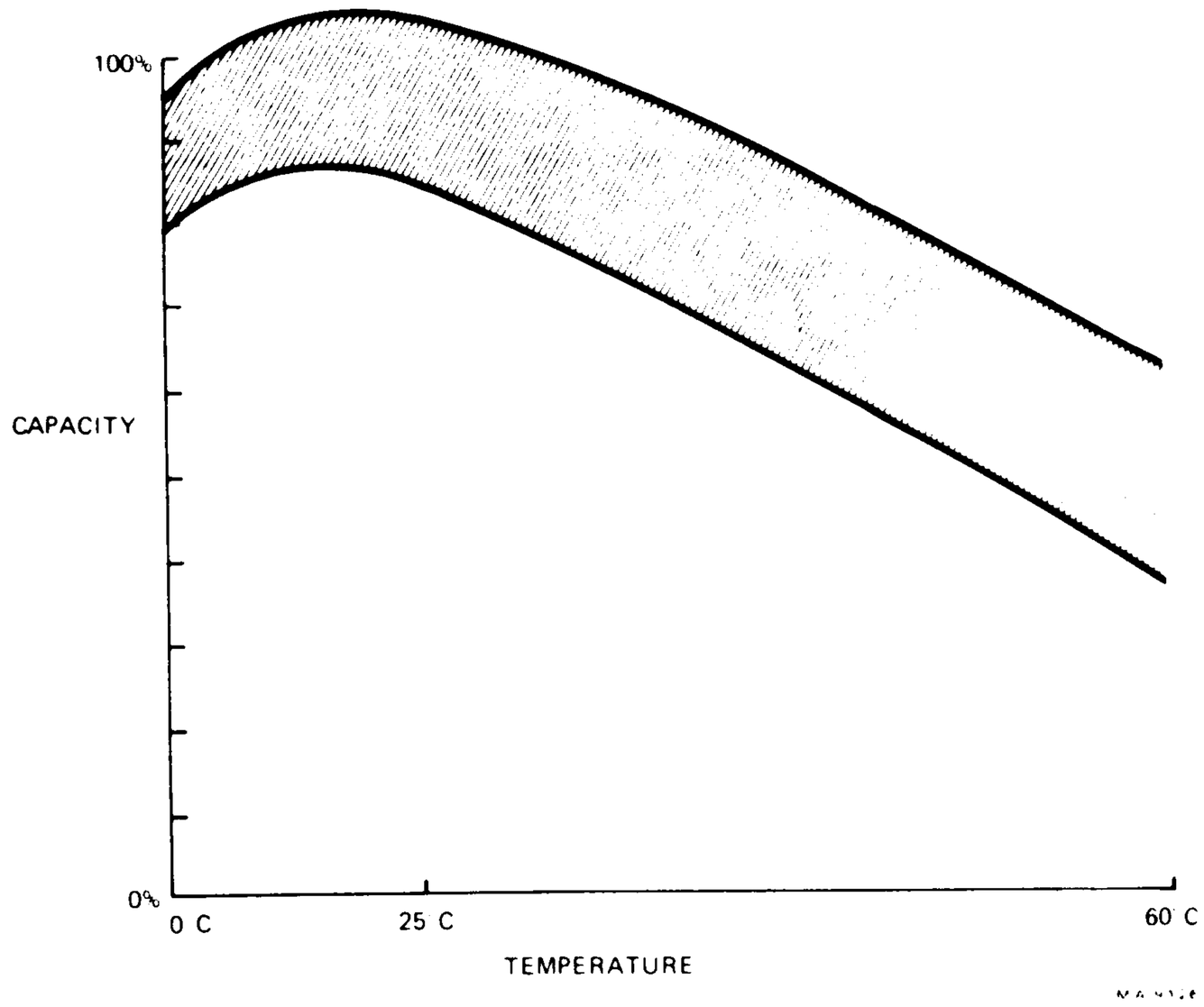


Figure 4-1 Battery Environment Performance

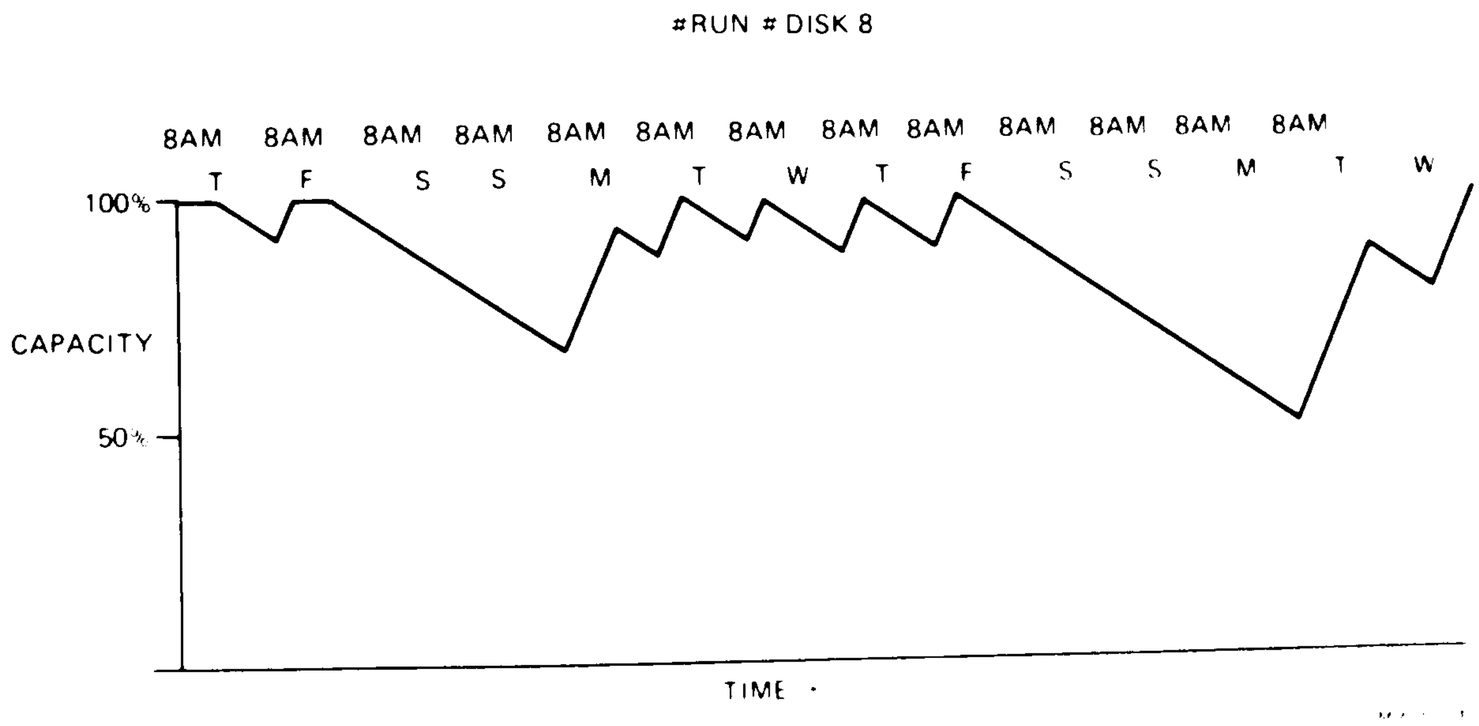


Figure 4-2 Charge/Discharge at 25 C

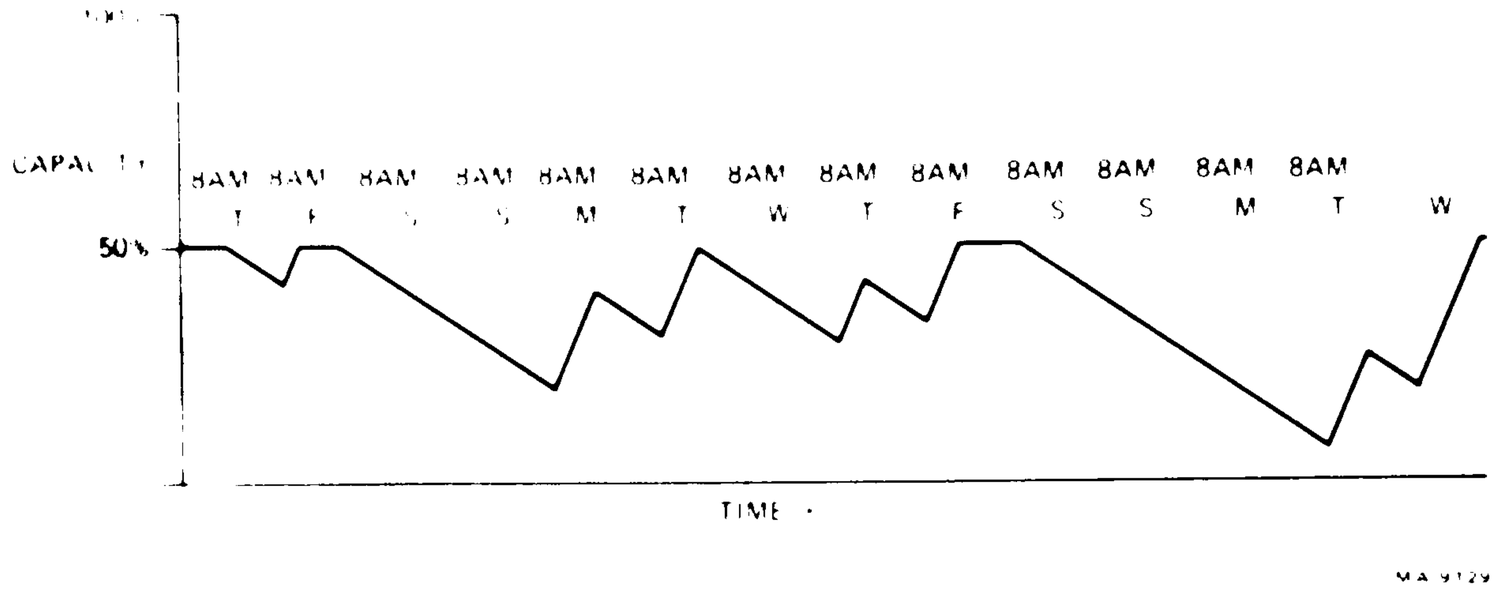


Figure 4-3 Charge/Discharge at 60 C

Figure 4-3 shows the same charge/discharge intervals with an operating temperature at 60° C.

CAUTION: When you find a bad cell you should always replace both cells with batteries from the same vendor.

Be careful not to short out the batteries.

4.3 DIAGNOSTIC TESTING

There are two memory diagnostic programs for testing the MCV11-D available from DIGITAL.

The MAINDEC-11-CVMSA diagnostic serves as a generic memory test for initial problem isolation.

MAINDEC-11-CVMEMA serves as a subsequent power-fail diagnostic test to detect battery or RAM failures.

Proper use of MAINDEC-11-CVMEMA requires minimal operator intervention together with basic knowledge of the system.

Power up the system for at least 30 minutes before running the MAINDEC-11-CVMEMA diagnostic.

4.4 DIGITAL SERVICES

Maintenance services may be performed by the user or by DIGITAL as desired. DIGITAL's maintenance and on-site services are described in the *Microcomputer and Memories Handbook* (EB-18451-20).

APPENDIX A
BATTERY INFORMATION

A.1 BATTERY SPECIFICATIONS

The following paragraphs cover the battery specifications for the MCV11-D.

Type - Rechargeable nickel cadmium cylindrical cell with wire leads. Each cell is size AAA, 1.2 V nominal, with a 180 mA/hr capacity at 25° C.

Capacity - A rating of the cell's ability to deliver a specified current at its nominal voltage for a given period of time. The time-current product is a constant for a new cell at 25° C. A 180 mA/hr cell delivers 180 mA for 1 hour or 18 mA for 10 hours.

A cell's capacity decreases from this nominal value with high temperatures or age. High temperature decreases a cell's capacity at a rate of 2 percent for every 1° C increase in temperature above 35° C. A cell also decreases in capacity by about 10 percent for every year of active use.

Storage Life - A battery can be stored for many years in either the fully charged, partial, or discharged state with no cell degradation. Several charge/discharge cycles will return the cell to normal capacity.

Operating Life - The projected battery operating life is over five years at normal operating temperatures (5° C < T (ambient) < 35° C). However, continuous high temperatures (>45° C) shorten the expected life of a battery. DIGITAL recommendeds replacing batteries yearly in critical applications at high temperatures that require maximum data retention reliability.

Charge, Discharge Rates - The module contains the battery charger, which will continuously trickle charge the batteries at a C 15 rate (12 mA) as long as +5 V is available. A totally discharged battery requires 24 hours of charging at this rate to fully recharge

In the data retention mode, the batteries typically discharge at much less than the C 100 rate

Battery Environment - The environmental specifications are as follows

1 The operating temperature is 20° C to 60° C. High temperatures limit both the battery life and the amount of charge a battery can accept

2 Cells can operate from sea level to an altitude of 50,000 ft (90MM mercury)

3 Normal commercial relative humidity range is from 10 to 90 percent noncondensing.

Physical - The battery is a sealed cell that will not leak its electrolyte when mounted in any position. Failure of the discharge circuit (board-level short circuit) causes the battery to fully discharge. Shorting a fully charged battery causes its internal temperature to rise to approximately 70° C and result in gas leakage. This gas is nontoxic and does not create any explosive hazards. However, cell life is reduced.

Battery Voltage (1.2 V Nominal) - Nickel cadmium batteries have a relatively flat voltage characteristic over a large range in capacity. Figure A-1 shows the change in voltage as the battery is charged.

Battery voltage is a poor indication of the cell's capacity.

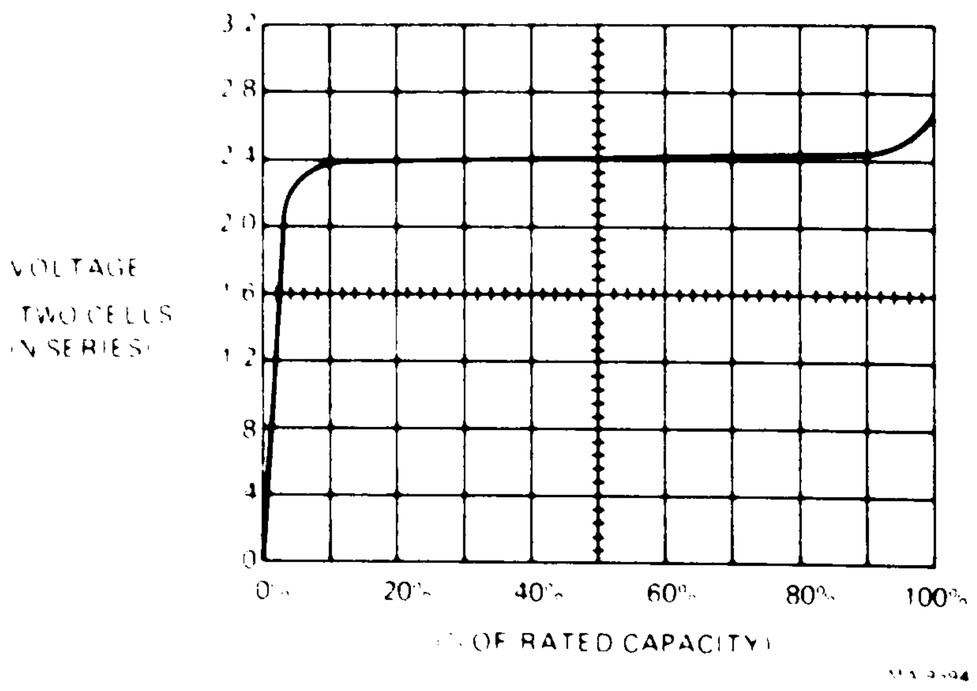


Figure A-1 Nicad Battery Characteristic Curve

A.2 BATTERY OPERATION

The following paragraphs cover initial power-up and data retention.

Initial Power-Up - The initial charge on any battery cannot be guaranteed when the module reaches the customer site. Therefore the module should run in a powered-up backplane for at least 30 minutes before a power-down data retention diagnostic can be reliably performed.

Due to the inefficiencies of a battery undergoing a charge, 24 hours are required to return a totally discharged battery to full charge. Half this charge time on an empty battery yields only half of the rated capacity and therefore only half its data retention time. Allowing enough charge time is especially important during the initial power-up.

Data Retention - The batteries require a charge time between each discharge period to return to full capacity. Batteries that are deeply discharged from a long power-down period need longer charge periods to restore full capacity. One hour of charging yields roughly 1 24 of the full data retention time.

Option	Size	Typical Data Retention	Worst Case Data Retention
MCV11-DC	32K bytes	1180 hours	100 hours
MCV11-DA	8K bytes	2647 hours	333 hours

Typical data retention times are normally expected from the average module used in normal low temperature applications. Shorter data retention times result when modules are used at high temperature, modules are several years old, or modules use a "lot run" of higher current CMOS RAMs.

The worst case data retention time represents a module that experiences the worst combination of the above parameters high temperatures, old batteries, and a "lot run" of higher current CMOS RAMs

A.3 BATTERY MAINTENANCE

The following paragraphs cover battery troubleshooting, replacement, and miscellaneous maintenance.

A.3.1 Troubleshooting

Three factors can cause premature loss of all data in the memory battery failure, RAM failure, and charging circuit failure

1. There are two types of battery failure

   a. Hard failure such as an expelled electrolyte or low-resistance internal short circuit (dead cell)

   b Soft failure such as a high-resistance internal short circuit (low storage capacity)

2 RAM failure is caused by high current leakage in a device.

3 Charging circuit failure is caused by high current leakage in a device.

Use the following procedure to diagnose a data retention problem.

1 Check to see that battery has some capacity (cell voltage > 1.2 V and power on the module for at least 30 minutes).

2 Measure current sourced by the battery to the RAMs. You can do this by removing the jumper clip and inserting an ammeter or by measuring the voltage drop across R18 with clip in. Current draw in excess of 1 mA for the 32K byte version indicates a RAM failure or a charging circuit failure. Current draw less than 1 mA indicates a battery capacity problem.

A.3.2 Replacement

You need the following materials to replace a battery. (See MCV11-D Print Set, MP-01309.)

1. Two batteries with wire leads
2. Two rubber tie-down straps

Always replace both batteries when one requires servicing. It is important that both batteries are at the same relative point in their life cycles to prevent a capacity mismatch.

A.3.3 Miscellaneous

There are three other maintenance problems you should know about.

Reverse Charge - With mismatched cells (one old and one new), one cell may completely discharge while the other cell is still supplying current. This can lead to cell reversal, where the discharged cell takes on a reverse potential. Totally discharging both cells can temporarily relieve this condition. For this reason, always replace cells in pairs to prevent this mismatch.

Memory Effect/Overcharge Effect - The "memory effect" of nicad batteries is an apparent reduction in the cell's capacity experienced under the following set of circumstances.

High temperature
Trickle charge with high-current discharges
Highly repetitive partial charge/discharge cycles
Cell cutoff voltages above 1.0 V

Occasional deep discharge cycles are sufficient to allow a cell to regain its original energy.

Long, sustained overcharging (trickle charge) causes a drop in the ni-cad voltage and an apparent reduction in capacity in high-temperature, high-discharge-current applications. This phenomenon results from an increase in the effective internal resistance of the cell. Like the "memory effect," the cells recover from the "overcharge effect" with a deep cycle.

The MCV11-D is not sensitive to either "memory effect" or "overcharge effect." The low discharge rate and the memory cutoff voltage at a cell voltage of 1.0 V make this memory all but immune to these two effects.

Crystal Formation - At high temperature a small white crystal formation may appear at the anode of the battery. This crystal formation is not harmful and may be wiped away if desired. High temperatures increase the vapor pressure of the electrolyte, causing some vapor leakage through the vent seal.

APPENDIX B
MODULE HANDLING AND PORTABILITY

B.1 HANDLING

A jumper clip is provided to connect the battery to the RAM array. With the jumper connecting pins W and X, the RAMs have voltage on their power pin (pin 24) even when the module is removed from the backplane. Use care in handling the module to prevent short circuits (that is, avoid metal surfaces such as tables, rings, or other modules when stacking). The best method of handling a board when the memory contents are of no concern is to disconnect the jumper clip from pins W and X; this takes voltage off the RAM array. Make sure the battery is not directly shorted in handling.

B.2 PORTABILITY

Once the memory is loaded with a program or data, the module can be removed from a backplane and inserted in the backplane of another system. This memory retains data as long as the battery is connected to the RAM array (pins W and X) and sufficient capacity remains in the battery. Use care in handling the module to safeguard memory contents. Avoid static discharge or momentary short circuits; otherwise the contents of memory cannot be guaranteed. Also avoid transporting the module in a static-proof bag, since the surface conductivity of the bag may cause a short circuit and destroy the contents of memory.

B.3 EXTERNAL BATTERIES

An external 5 V battery backup supply can connect to pin AV1 on the backplane (+ 5 V BBU). This pin connects to the RAMs through a diode and supplies data retention voltage to the array at any voltage from 2.7 V to 5.5 V (with onboard batteries disconnected). You can achieve extremely long data retention times by sizing the external battery appropriately. This is especially important for high-temperature applications where the onboard batteries may not provide sufficient capacity for the customer's application, or where an external battery pack contains custom-designed voltage of capacity monitoring devices for use in the most demanding applications.

With the onboard batteries connected (pins W and X), the use of the external battery back-up becomes more complicated. As long as the external voltage supply level is set greater than one diode drop above the onboard battery voltage (V_{bat} = 2.4 V - 2.85 V), the external supply will supply the data retention voltage level to the RAMs and trickle charge the onboard batteries. The trickle-charge rate (and therefore the external supply current drain) depends on the voltage level of the external supply. At 5.5 V, the external supply will source about 12 mA; at 3.4 V, the external supply will source less than 1 mA. When the external voltage supply drops below 3.4 V, the onboard battery provides the data retention voltage to the RAMs. The external supply will not source current until the onboard battery becomes depleted and drops its terminal voltage.

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