**DZV11 asynchronous
multiplexer
user's guide**

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

CONTENTS (Cont)

FIGURES

TABLES

TABLES (CONT)

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZV11, shown in Figure 1-1, is an asynchronous multiplexer that provides an interface between an LSI-11 processor and four asynchronous serial data communication channels. It can be used with the LSI-11 processor in a variety of applications that include data concentration, real time processing and cluster controlling. The DZV11 provides an EIA RS232C interface and enough data set control to permit dial-up (auto answer) operation with modems capable of full-duplex operation*, such as the Bell models 103, 113, 212, or equivalent. Remote operation over private lines for full-duplex point to point or full-duplex multipoint as a control (master) station is also possible. Figure 1-2 depicts several of the possible applications for the DZV11 in an LSI-11 system.
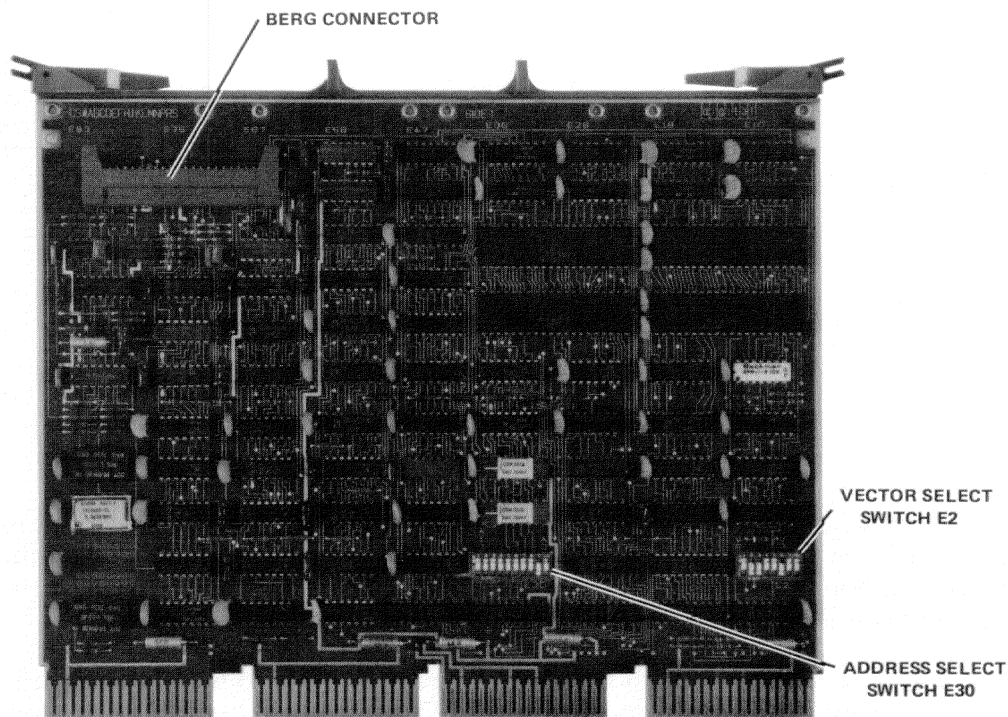
Figure 1-1   DZV11-A (M7957 Module)

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*The DZV11 data set control does not support half-duplex operations or the secondary transmit and receive operations available with some modems such as the Bell 202, etc.
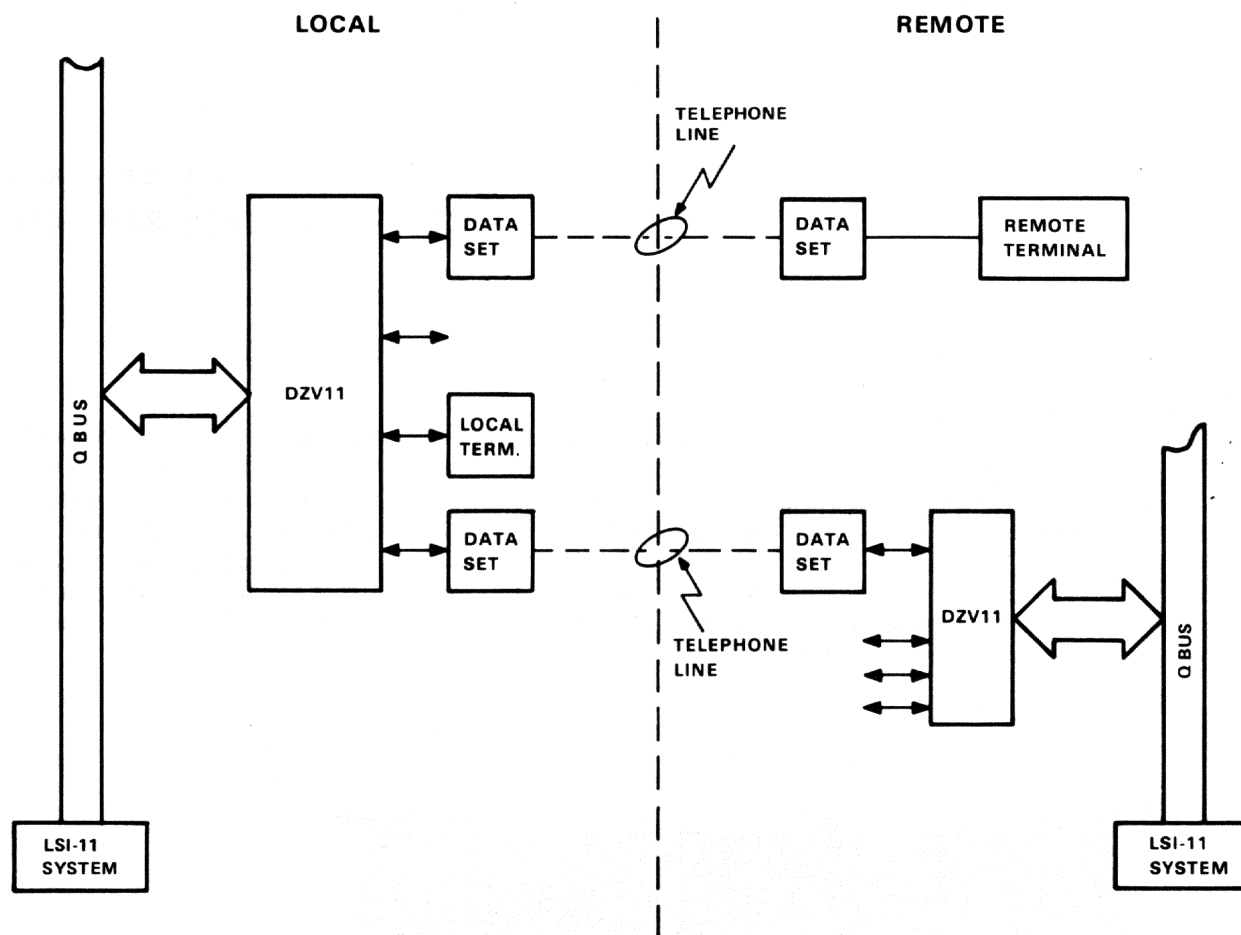
Figure 1-2   DZV11 System Applications

The DZV11 has several features that provide flexible control of parameters such as baud rate, character length, number of stop bits for each line, odd or even parity for each line, and transmitter-receiver interrupts. Additional features include limited data set control, zero receiver baud rate, break generation and detection, silo buffering of received data, and line turnaround.

Program compatibility is maintained with the Unibus option DZ11-A. The only compatibility exception is the number of serial channels supported. The DZV11 does not support 20 mA operation.

1.2   PHYSICAL DESCRIPTION
The DZV11 comprises a single quad size module, 21.6 cm × 26.5 cm (8.51 inches × 10.44 inches), and is designated as the M7957 module. All input and output leads are available on a Berg header. The DZV11 connects to the LSI-11 QBUS by the H9270 mounting panel or equivalent. All QBUS input/output signals enter and leave the module via the mounting panel pins.

1.2.1 DZV11 Configurations

The DZV11 can be supplied in two configurations. The DZV11-A, as shown in Figure 1-1, consists of the M7957 module only. Cabling assemblies for connection to terminals and modem channels are not supplied with the DZV11-A, but are available in the DZV11-B. The DZV11-B consists of an M7957 module, BC11U-25 cable assembly, and two accessory test connectors, H329 and H325. This configuration is shown in Figure 1-3.
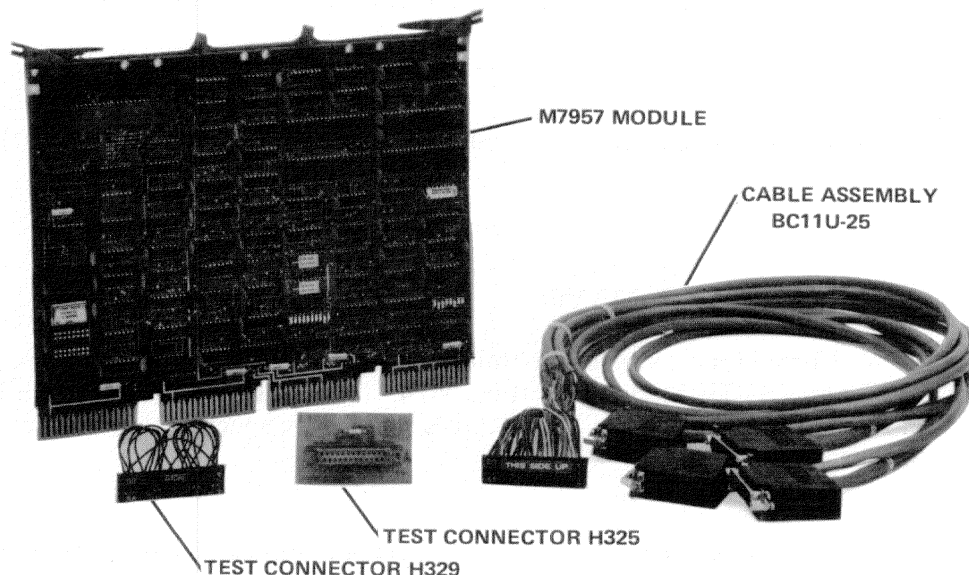
9024-2

Figure 1-3   DZV11-B (M7957 Module, H325 and H329
Connectors and Cable Assembly BC11U-25)

1.2.2 BC11U Interface Cable

The interfacing cable for terminal and modem connections to the DZV11-B is provided by the BC11U cable assembly (see Figure 1-3). It consists of four separate cables, 762 cm (25 feet) in length, each terminated by a separate EIA type connector housing and a common Berg housing. Each cable within the assembly provides nine input/output leads. The EIA connector pinning conforms to EIA standard RS232C and CCITT* recommendation V.24. The leads supported by the DZV11-B are:

Circuit AA (CCITT 101)	Pin 1	Protective Ground
Circuit AB (CCITT 102)	Pin 7	Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
Circuit BB (CCITT 104)	Pin 3	Received Data
Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CE (CCITT 125)	Pin 22	Ring Indicator
Circuit CF (CCITT 109)	Pin 8	Carrier

NOTE
Signal ground and protective ground are connected together.

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*CCITT – the Consultive Committee International Telegraph and Telephone is an advisory committee established under the United Nations to recommend worldwide standards.

1.2.3 Test Connectors
Figure 1-4 shows the two accessory test connectors, H329 and H325, that are provided with each DZV11-B. The H325 plugs into an EIA connector on the BC11U to loopback data and modem signals onto a single line. The H329 plugs into the M7957 module socket housing and provides staggered loopback of the data and modem lines. The loopback connections are shown in Figure 1-5.

1.3 SPECIFICATIONS
Environmental, electrical, and performance specifications for the DZV11 are discussed in the following paragraphs.

1.3.1 Environmental
The DZV11 operates in an environment from 5° to 50° C (41° to 122° F) and in a relative humidity of 10% to 95%.

1.3.2 Electrical
Power Consumption   1.15 A @ +5 Vdc
                           0.39 A @ +12 Vdc

For each line the DZV11 provides a voltage level interface whose levels and connections conform to EIA standard RS232C and CCITT recommendation V.24. The leads supported by the DZV11 are listed in topic 1.2.2. Each DZV11 meets the LSI-11 QBUS Interface specification and represents one unit load as an interface.

1.3.3 Performance
The following paragraphs describe the DZV11 performance capabilities and restrictions.

1.3.3.1 Maximum Configurations – The DZV11 multiplexer is assigned a device address in the floating address space. The floating address space starts at 760010 and extends to 764000. A maximum configuration of DZV11s would not be limited by floating address space, but would be limited by the rules governing an intermediate size system configuration. Therefore, a maximum of seven DZV11 multiplexers may reside in a nine by four backplane.

1.3.3.2 Throughput – Each DZV11 is capable of a throughput rate of 10,970 characters per second. This rate is calculated as follows:

(Bits/Second × No. Lines × Direction) divided by Bits/Character.
(9600 × 4 × 2) 1/7 equals 10,970 Characters/Second.

For a character service routine of 100 μs or less, the device throughput rate can be sustained.

1.3.3.3 Receivers – The receivers provide serial to parallel conversion of 5, 6, 7, 8 level code with one start space and at least one stop mark. The character length, number of stop bits, parity generation and operating speed are programmable parameters for each line. A receiver and transmitter of a corresponding line share the same operating speed with provisions for enabling/disabling of that receive line.

Each receiver is double-buffered and has an allowable input distortion of 43.75% on any bit. Also, the accumulated character distortion must not exceed 43.75%. Break detection is provided on each receiver.
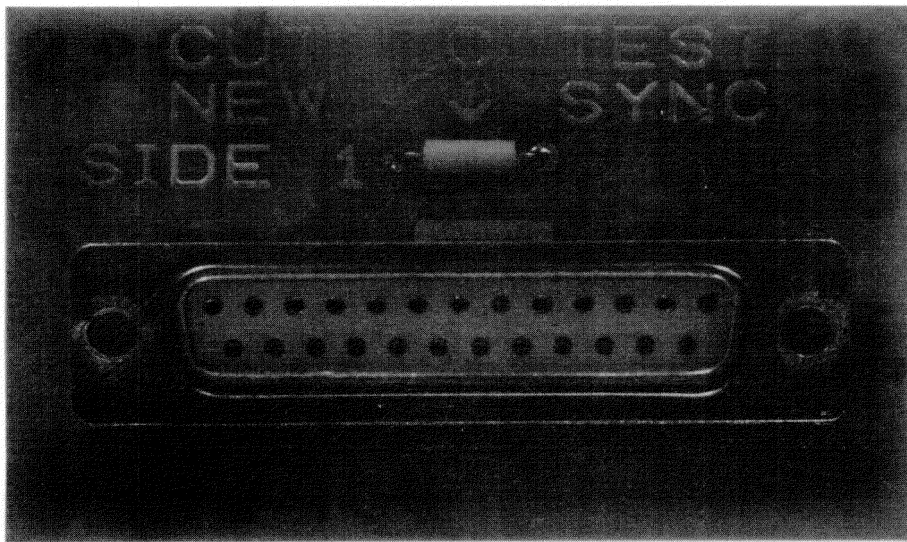
H325
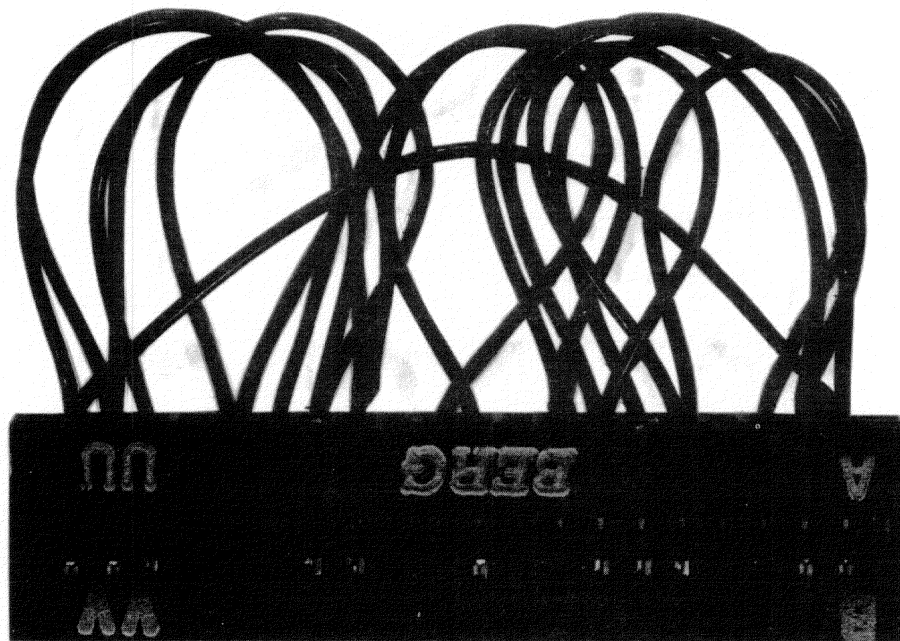
H329

9024-1

Figure 1-4   Test Connectors H325 and H329

H329 STAGGERED TURNAROUND

TRANSMIT 0 ──────────────▶ RECEIVE 1

DTR 0 ──────────────▶ RING 1

──▶ CARRIER 1

RING 0 ◀──────

CARRIER 0 ◀────── DTR 1

RECEIVE 0 ◀────────────── TRANSMIT 1
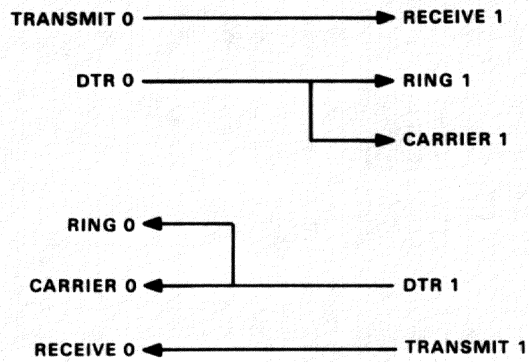
NOTE:
LINES 2&3 ARE STAGGERED IN THE SAME WAY.

H325 LOOPBACK CONNECTIONS

SCE ── 24 ──▶

SCT ── 15 ──

SCR ── 17 ──

SEC XMIT ── 11 ──▶

SEC RCV ── 12 ──

XMIT DATA ── 2 ──▶

RCV DATA ── 3 ──

REQ TO SEND ── 4 ──▶

CLR TO SEND ── 5 ──

CARRIER ── 8 ──

NEW SYNC ── 14 ──▶

DATA SET RDY ── 6 ──○ JUMPER
                     REMOVED
DTR ── 20 ──▶ ──○

RING ── 22 ──
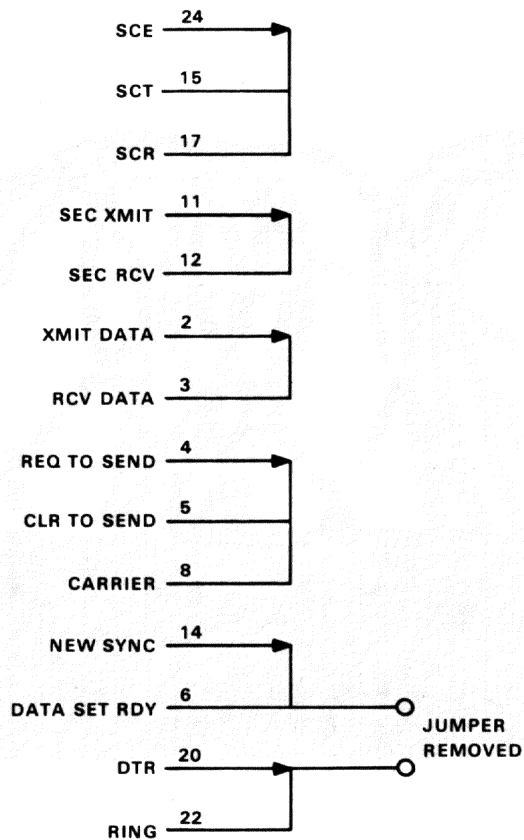
MA-0551

Figure 1-5   Loopback Connections

1-6

1.3.3.4 Transmitters – The transmitters provide parallel to serial conversion of 5, 6, 7, 8 level code with or without parity. The parity sense when selected can be either odd or even. The stop code can be either 1 or 2 units except when 5 level code is selected. When 5 level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks are capable of being transmitted on any line. The gross start-stop distortion for a transmitter's TTL output will be less than 2.5% for an 8-bit character.

1.3.3.5 Baud Rate Generator – The baud rate generator is a MOS/LSI device which provides the DZV11 multiplexer with full programmable capability for operating speed selection. Each line has an independent generator capable of producing 1 of 15 selectable baud rates. Speed tolerance for all rates is less than 0.3% with a clock duty of 50% ± 5%. (See below for rates.)

1.3.3.6 Performance Summary – The following summarizes the programmable features offered for each line:

Character length	5, 6, 7, or 8 level code
Number of stop bits	1 or 2 for 6, 7, 8 level code 1 or 1.5 for 5 level code
Parity	odd, even or none
Baud rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600
Breaks	Can be generated and detected on each line.

1.3.4 Interrupts
The following interrupts are available on DZV11.

Receiver Done Interrupt
Occurs every time a character appears at the output of the receiver buffer register and the Silo Alarm is disabled. Can be enabled or disabled from the bus.

Silo Alarm Interrupt
Occurs after 16 entries have been made into the receive buffer register by the scanner. This interrupt disables Receiver Done Interrupt and is rearmed when the receive buffer register has been read.

Transmit Interrupt
Occurs every time the scanner finds a UART buffer empty condition, and the transmitter control register bit is set for that line. Can be enabled or disabled from the bus.

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZV11 Asynchronous Multiplexer.

2.2 UNPACKING AND INSPECTION

The DZV11 is packaged in accordance with commercial packaging practices. First, remove all packing material and check the equipment against the shipping list. (Table 2-1 contains a list of supplied items per configuration.) Report damage or shortages to the shipper immediately and notify the DIGITAL representative. Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths.

2.3 INSTALLATION PROCEDURE

The following paragraphs describe the installation of the DZV11 option in an LSI-11 system.

2.3.1 Jumper Configuration

There are 16 machine-insertable jumpers on the M7957 module. (See drawing D-UA-M7957-0-0 for jumper locations.)

2.3.1.1 Device Operation – Jumpers W10 and W11 must be installed only when the module is used on an H9270 backplane, or one that applies QBUS signals to the C and D sections of the module.

Table 2-1 Items Supplied per Configuration

Quantity	Description	A	B
1	M7957 module	X	X
1	BC11U-25 cable assembly		X
1	H329 test connector		X
1	H325 test connector		X
1	Print set (B-TC-DZV11-0-1) DZV11-A and -B order number MP00462	X	X
1	Software kit ZJ251-RB	X	X
1	DZV11 User's Guide (EK-DZV11-UG)	X	X

2.3.1.2 Modem Control Jumpers – There are eight jumpers which are used for additional modem control support. The jumpers labeled W1 through W4 connect Data Terminal Ready to Request to Send. This allows the DZV11 to assert both DTR and RTS if using a modem which requires control of RTS. The remaining four jumpers, W5 through W8, provide connection of the Forced Busy function to the Request to Send lead. Assertion of RTS places an ON or BUSY condition to the modems that implement this function. This jumper should normally be cut out unless the modem has the Forced Busy feature and the system software is implemented to control it. These jumpers must be installed for diagnostic testing of the DZV11-B option. (See Table 2-2, Jumper Configuration.)

Table 2-2   Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	03
W2	DTR to RTS	02
W3	DTR to RTS	01
W4	DTR to RTS	00
W5	RTS to FB	03
W6	RTS to FB	02
W7	RTS to FB	01
W8	RTS to FB	00

2.3.2 Module Installation
To install the M7957 module, perform the following:

1. Refer to Paragraph 4.2 for descriptions of the address assignments. Set the switches at E30 so that the module will respond to its assigned address. When a switch is closed (ON), a binary 1 is decoded. When a switch is open (OFF), a binary 0 is decoded. Note that the switch labeled 1 corresponds to address bit 12, 2 corresponds to address bit 11, etc. (See Figure 2-1 and Table 2-3.)

ADDRESS SELECTOR

	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	
ON	1	2	3	4	5	6	7	8	9	10	SWITCH E30
OFF											
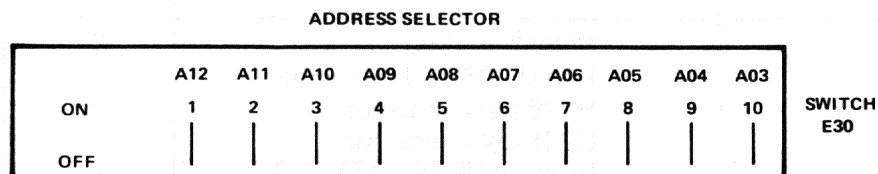
MA-0915

Figure 2-1   M7957 Address Selection

Table 2-3   Address Switch Selection

E30 Switch Address	1 A12	2 A11	3 A10	4 A9	5 A8	6 A7	7 A6	8 A5	9 A4	10 A3
160000	–	–	–	–	–	–	–	–	–	–
160010	–	–	–	–	–	–	–	–	–	X
160020	–	–	–	–	–	–	–	–	X	–
160030	–	–	–	–	–	–	–	–	X	X
160040	–	–	–	–	–	–	–	X	–	–
160050	–	–	–	–	–	–	–	X	–	X
160060	–	–	–	–	–	–	–	X	X	–
160070	–	–	–	–	–	–	–	X	X	X
160100	–	–	–	–	–	–	X	–	–	–
.										
.										
.										
.										
163760	–	–	X	X	X	X	X	X	X	–
163770	–	–	X	X	X	X	X	X	X	X

NOTE: X = ON
         – = OFF

2.   Vector selection is accomplished by the 8-position switch at E2. Switch positions 7 and 8 are not used. Switch position 6 corresponds to vector bit 3, 5 corresponds to vector bit 4, etc. When a switch is closed (ON), a binary 1 is decoded. When a switch is open (OFF), a binary 0 is decoded. (See Figure 2-2 and Table 2-4.)
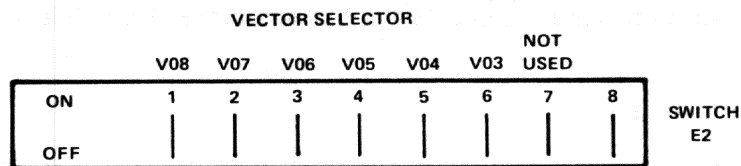
Figure 2-2   M7957 Vector Selection

Table 2-4 Vector Switch Selection

E2 Switch Vector	1 V08	2 V07	3 V06	4 V05	5 V04	6 V03
300	–	X	X	–	–	–
310	–	X	X	–	–	X
320	–	X	X	–	X	–
330	–	X	X	–	X	X
340	–	X	X	X	–	–
350	–	X	X	X	–	X
360	–	X	X	X	X	–
370	–	X	X	X	X	X
400	X	–	–	–	–	–
.						
.						
.						
760	X	X	X	X	X	–
770	X	X	X	X	X	X

NOTE: X = ON
             – = OFF

3. If the module is part of the DZV11-A option, perform step 3. If it is a part of the DZV11-B option, proceed to step 4 for testing.

    a.   Insert the module in a quad QBUS slot of the backplane.

CAUTION
Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

    b.   Run the DZV11 diagnostics, MAINDECs DVDZA and DVDZB, in internal mode to verify operation. Refer to the listing for assistance. Run at least three passes without error.

    c.   Proceed to step 8.

4. Insert the H329 test connector in J1 with the letter side facing up. J1 is the cable connector at the top of the M7957 module.

5. Insert the module in a quad QBUS slot of the backplane.

CAUTION
Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

Run the DZV11 diagnostics, MAINDECs DVDZA and DVDZB, in the staggered mode to verify module operation. Refer to the diagnostic listing for the correct procedure. Run at least three passes without error.

6. Replace the H329 test connector with the Berg end of the BC11U cable assembly. Observe the "This Side Up" wording on the assembly. Refer to D-UA-DZV11-0-0 for installation help.

7. Connect the H325 test connector on the first line and run MAINDEC DVDZC. Select the cable test portion of the diagnostic. Three passes are required without error. Repeat this step for each line.

8. Run DEC/X11 systems exerciser to verify the absence of QBUS interference with other system devices.

9. The DZV11 is now ready for connection to external equipment. If the connection is to a local terminal through the DZV11-B option, a null modem cable assembly must be used. Use the BC03M or BC03P null modem cables for connection between the BC11U and the terminal. The H312-A null modem unit may also be used in place of the null modem cables. If connection is to a Bell 103 or equivalent modem, install the appropriate line of the BC11U connector into the connector on the modem. A BC05D cable may be required between the BC11U and the modem. Refer to Paragraph 2.3.1.2, Modem Control Jumpers, for selection of jumpers for modem options such as RTS and Forced Busy. All of the cables mentioned, excluding the BC11U, must be ordered separately as they are not components of a standard DZV11 shipment. When possible, run the diagnostic DVDZC in echo test mode to verify the cable connections and the terminal equipment.

CHAPTER 3
DEVICE REGISTERS

3.1 SCOPE
This chapter provides a description of each DZV11 register, its format, and bit functions.

3.2 DEVICE REGISTERS
The DZV11 contains six addressable registers. A comprehensive pictorial of these registers' bit assignments is shown in Figure 3-1. Table 3-1 lists the registers and associated DZV11 addresses.

Table 3-1 DZV11 Register Address Assignments

Register	Mnemonic	Address	Program Capability
Control and Status Register	CSR	76XXX0	Read/Write
Receiver Buffer	RBUF	76XXX2	Read Only
Line Parameter Register	LPR	76XXX2	Write Only
Transmitter Control Register	TCR	76XXX4	Read/Write
Modem Status Register	MSR	76XXX6	Read Only
Transmit Data Register	TDR	76XXX6	Write Only

XXX = Selected in accordance with floating device address scheme.

3.2.1 Control and Status Register
The control and status register (CSR) is a byte and word addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device Master Clear (CSR 04). The format is shown in Figure 3-1 and the bit assignments are listed in Table 3-2.

3.2.2 Receiver Buffer
The Receiver Buffer (RBUF) is a 16-bit read only register which contains the received character at the output of the FI/FO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the Valid Data bit (RBUF 15) is cleared by BINIT or by setting device Master Clear (CSR 04). Bits 00–14 are not affected. The bit assignments for the RBUF register are listed in Table 3-3.

Figure 3-1 Register Bit Assignments

		MSB 15	14	13	12	11	10	09	HIGH 08	LOW 07	06	05	04	03	02	01	LSB 00
DR0	CONTROL & STATUS (CSR)	RO TRDY	RW TIE	RO SA	RW SAE	NOT USED	NOT USED	RO TLINE B	RO TLINE A	RO RDONE	RW RIE	RW MSE	RW CLR	RW MAINT	NOT USED	NOT USED	NOT USED
DR2	RECEIVER BUFFER (RBUF)	RO DATA VALID	RO OVRN ERR	RO FRAM ERR	RO PAR ERR	NOT USED	NOT USED	RO RX LINE B	RO RX LINE A	RO RBUF D7	RO RBUF D6	RO RBUF D5	RO RBUF D4	RO RBUF D3	RO RBUF D2	RO RBUF D1	RO RBUF D0
	LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	WO RX ENAB	WO SPEED CODE D	WO SPEED CODE C	WO SPEED CODE B	WO SPEED CODE A	WO ODD PAR	WO PAR ENAB	WO STOP CODE	WO CHAR LGTH B	WO CHAR LGTH A	NOT USED	WO LINE B	WO LINE A
DR4	TRANSMIT CONTROL (TCR)	NOT USED	NOT USED	NOT USED	NOT USED	RW DTR 3	RW DTR 2	RW DTR 1	RW DTR 0	NOT USED	NOT USED	NOT USED	NOT USED	RW LINE ENAB 3	RW LINE ENAB 2	RW LINE ENAB 1	RW LINE ENAB 0
DR6	MODEM STATUS (MSR)	NOT USED	NOT USED	NOT USED	NOT USED	RO CO 3	RO CO 2	RO CO 1	RO CO 0	NOT USED	NOT USED	NOT USED	NOT USED	RO RI 3	RO RI 2	RO RI 1	RO RI 0
	TRANSMIT DATA (TDR)	NOT USED	NOT USED	NOT USED	NOT USED	WO BRK 3	WO BRK 2	WO BRK 1	WO BRK 0	WO TBUF 7	WO TBUF 6	WO TBUF 5	WO TBUF 4	WO TBUF 3	WO TBUF 2	WO TBUF 1	WO TBUF 0

BYTES

MA-0552

Figure 3-1 Register Bit Assignments

Table 3-2 CSR Bit Assignments

Bit	Title	Function
00–02	Not used	
03	Maintenance	This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is read/write.
04	Master Clear	When written to a 1, generates "Initialize" within the DZV11. A read back of the CSR with this bit set, indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTS are cleared with the following exceptions: 1. Only bit 15 of the receiver buffer register (VALID DATA); the remaining bits 00–14 are not. 2. The high byte of the transmitter control register is not cleared by Master Clear. 3. The modem status register is not cleared by Master Clear.
05	Master Scan Enable	This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready (CSR 15) will be inhibited from setting and the received character buffers (silos) will be cleared.
06	Receiver Interrupt Enable	This bit, when set, permits the setting of CSR 07 or CSR 13 to generate a receiver interrupt request. This bit is read/write.
07	Receiver Done	This is a read only bit that will set when a character appears at the output of the FI/FO buffer. To operate in interrupt per character mode, CSR 06 must be set and CSR 12 must be cleared. With CSR 06 and CSR 12 cleared, character flag mode would be indicated. Receiver Done will clear when the receiver buffer register (RBUF) is read or when Master Scan Enable (CSR 05) is cleared. If the FI/FO buffer contains an additional character, the Receiver Done flag will stay cleared a minimum of 1 μs before presenting that character.
08–09	Transmitter Line Number	These read only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when Transmitter Ready (CSR 15) is set and will be cleared when Master Scan Enable is cleared. Bit 08 is the least significant bit.
10–11	Not used	

Table 3-2 CSR Bit Assignments (Cont)

Bit	Title	Function
12	Silo Enable Alarm	This is a read/write bit, when set, enables the silo alarm counter to keep count of the number of characters stored in the FI/FO buffer. The counter will be cleared when the Silo Alarm Enable bit is cleared. Conditioning of this bit must occur prior to any character reception.
13	Silo Alarm	This is a read only bit set by the hardware after 16 characters have been entered into the FI/FO buffer. Silo Alarm will be held cleared when Silo Alarm Enable (CSR 12) is cleared. This bit will be reset by a read to the receiver buffer register and will not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR 06) is set, the occurrence of Silo Alarm will generate a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the Silo Alarm bit.
14	Transmitter Interrupt Enable	This bit must be set for Transmitter Ready to generate an interrupt. It is read/write.
15	Transmitter Ready	This bit is read only and is set by the hardware. This bit will set when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The Transmitter Line Number, specified in CSR 08 and CSR 09, is only valid when Transmitter Ready is set. Transmitter Ready will be cleared by any of the following conditions: 1. Master Scan Enable cleared. 2. When the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09. 3. At the conclusion of the load instruction of the transmit data register (low byte only). If additional transmit lines require service, Transmitter Ready will reappear within 1.4 μs from the completion of the transmit data register load instruction. The occurrence of Transmitter Ready with Transmitter Interrupt Enable set, will generate a transmitter interrupt request.

Table 3-3 RBUF Bit Assignments

Bit	Title	Function
00–07	Received Character	These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
08–09	Received Character Line Number	These bits contain the line number upon which the aforementioned character was received. Bit 08 is the least significant bit.
10–11	Not used	
12	Parity Error	This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
13	Framing Error	This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error	This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.
15	Valid Data	This bit, when set, indicates that the data presented in bits 00–14 is valid. This bit permits the use of a character handling program that takes characters from the FI/FO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.

3.2.3 Line Parameter Register
The line parameter register (LPR) controls the operating parameters associated with each line in the DZV11. The LPR is a word addressable, write only register. The line parameters for all lines must be reloaded following an occurrence of either BINIT or device Master Clear. Table 3-4 lists bit assignments.

3.2.4 Transmitter Control Register
The transmitter control register (TCR) is a byte and word addressable register. The low byte of the TCR register contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 00 corresponds to line 00, bit 01 to line 01, etc. Setting of a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty condition. An interrupt will then be generated if Transmitter Interrupt Enable is set. The scanner clock will restart when either the transmit data register is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running, (i.e., Transmitter Ready is set or Master Scan Enable is cleared.)

The TCR bits are represented in bits 00–03. These bits are read/write and are cleared by BINIT or device Master Clear. Bits 04–07 are unused and read as zero.

The high byte of the TCR register contains the writable modem control lead, data terminal ready (DTR). Bit designations are as follows:

Bit	Name
08	DTR Line 00
09	DTR Line 01
10	DTR Line 02
11	DTR Line 03
12–15	Unused; read as zero

Assertion of a DTR bit puts an ON condition on the appropriate modem circuit for that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the Request to Send circuits to be asserted with Data Terminal Ready assertions.

Table 3-4   LPR Bit Assignments

Bit	Title	Function
00–01	Parameter Line Number	These bits specify the line number for which the parameter information (bits 3–12) is to apply. Bit 00 is the least significant bit.
02	Not used	Must always be written as a zero when specifying the parameter line number. Writing this bit as a one will extend the parameter line number field into nonexistent lines. Parameters for lines 00–03 will not be affected.
03–04	Character Length	These bits are set to receive and transmit characters of the length (excluding parity) as shown below. 04 03 0 0 5 bit 0 1 6 bit 1 0 7 bit 1 1 8 bit
05	Stop Code	This bit sets the stop code length (0 = 1 unit stop, 1 = 2 unit stop or 1.5 unit stop if a 5-level code is employed).
06	Parity Enable	If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
07	Odd Parity	If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.

Table 3-4   LPR Bit Assignments (Cont)

Bit	Title	Function
08–11	Speed Code	The state of these bits determine the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Invalid

Bit	Title	Function
12	Receiver Enable	This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit will be cleared following a BINIT or device Master Clear.
13–15	Not used	

3.2.5   Modem Status Register

The modem status register (MSR) is a 16-bit read only register. A read to this register results in the status of the readable modem control leads, Ring and Carrier. The ON condition of a modem control lead is interpreted as a logical one. Bits 04–07 and 12–15 are unused and read as a zero. Remaining bit designations are as follows:

Bit	Name
00	Ring Line 00
01	Ring Line 01
02	Ring Line 02
03	Ring Line 03
04–07	Unused; read as zero.
08	Carrier Line 00
09	Carrier Line 01
10	Carrier Line 02
11	Carrier Line 03
12–15	Unused; read as zero.

3.2.6 Transmit Data Register

The transmit data register (TDR) is a byte and word addressable, write only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when Transmitter Ready (CSR 15) is set. That character which is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the TDR is designated as the break control register.

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12-15 are unused. Setting a break bit will force that line's output to space. This condition will remain until cleared by the program. This register is cleared by BINIT or device Master Clear. The break control register can be utilized regardless of the state of the device Maintenance bit (CSR 03).

4.1 SCOPE

This chapter contains information for programming the DZV11 in the most efficient manner. To do so, the programming controls must be fully understood. The following paragraphs discuss the DZV11 from the programming point of view and describe recommended programming methods.

4.2 DEVICE ADDRESS ASSIGNMENTS

The device address assigned to the DZV11 resides in the floating address space of the LSI-11. This address space ranges from 160010_8 to 163776_8. Each DZV11 requires increments of 10_8 address locations and the first option should be configured with an address of 160010_8. The initial configured address assumes that the system consists of only DZV11s in the floating address field. If the DUV11 option is also configured in the floating address field, assign the DZV11 an address which establishes a gap of 10_8 address locations between the last DUV11 and the first DZV11. For example: If the system consisted of one DUV11 located at 160010_8, the DZV11 should be configured with an address of 160030_8.

4.3 INTERRUPT VECTOR ADDRESS ASSIGNMENTS

The DZV11 device vector address is selected from the floating vector space. This space ranges from address 300_8 to address 776_8. Each DZV11 requires increments of 10_8 address locations for its two contiguous interrupt vectors. If the DZV11 is the only option in the floating vector area, configure it for a vector of 300_8. If there are options other than the DZV11 residing in the floating vector area, other configuration rules must be applied. When configuring the device vector, only the first vector address must be considered. The first vector, or base vector, must start on a zero boundary.

A zero boundary is one which has the three least significant bits equal to zero. The second vector is controlled by the first vector and data bit 02. Data bit 02 is generated by the M7957 hardwware.

Any option ahead of DZV11 in the floating vector space which is not in the configuration should not occupy any vector space gap. For example, if only one DZV11 is in the system the vector for the DZV11 should be 300. The simplest case is as follows:

Option	Address	Vector	Comment
GAP	160010	–	No QBUS compatible DJ11
GAP	160020	–	No QBUS compatible DH11
GAP	160030	–	No QBUS compatible DQ11
GAP	160040	–	No DUV11
GAP	160050	–	No QBUS compatible DUP11
GAP	160060	–	No QBUS compatible LK11
GAP	160070	–	No QBUS compatible DMC11
DZV11	160100	300	
GAP	160110	–	No more DZV11s

Each DZV11 requires two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests were generated from each section, the receiver section would have priority in placing its vector onto the LSI bus. A receiver interrupt to address XX0 will be generated from having either a Receiver Done (CSR 07) or Silo Alarm (CSR 13) occurrence. A transmitter interrupt to address XX4 will be generated by Transmitter Ready (CSR 15). Additional prerequisites for generating interrupts are that the individual interrupt enable bits (CSR 06 and CSR 14) be set. The recommended method of clearing interrupt enable bits is to first raise the processor status word to level four, next clear these interrupt enable bits and then lower the processor status word to zero. Using this method prevents false interrupts from being generated.

4.4 PROGRAMMING FEATURES

The DZV11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

4.4.1 Baud Rate

Selection of the desired transmission and reception speed is controlled by the conditions of bits 08–11 of the LPR. Table 4-1 depicts the required bit configuration for each operating speed. The baud rate for each line is the same for both the transmitter and receiver. The receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 4-1 Baud Rate Selection Chart

Bits				Baud Rate
11	10	09	08	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not used

4.4.2 Character Length

The selection of one of the four available character lengths is controlled by bits 03 and 04 of the LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5-level), 01 (6-level), 10 (7-level), and 11 (8-level). For character lengths of 5, 6, and 7, the high-order bits of the received character are forced to zero.

4.4.3 Stop Bits

The length of the stop bits in a serial character string is determined by bit 05 of the LPR. If bit 05 is a zero, the stop length is one unit; bit 05 set to a one selects a 2-unit stop unless the 5-level character length (bits 03 and 04 at zero) is selected, in which case the stop bit length is 1.5 units.

4.4.4 Parity

The parity option is selected by bit 06 of the LPR. Parity is enabled on transmission and reception by setting bit 06 to a one. Bit 07 of the LPR allows selection of even or odd parity, and bit 06 must be set for bit 07 to be significant. The parity bit is generated and checked by hardware and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character has a parity error.

4.4.5 Interrupts

The receiver interrupt enable (RIE) and silo alarm enable (SAE) bits in the CSR control the circumstances upon which the DZV11 receiver interrupts the LSI-11 processor.

If RIE and SAE are both clear, the DZV11 never interrupts the LSI-11 processor. In this case, the program must periodically check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZV11 will interrupt the LSI-11 processor to the DZV11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZV11 will interrupt when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced.) Alternatively, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt.

If RIE and SAE are both set, the DZV11 will interrupt the LSI-11 processor to the DZV11 receiver vector when the silo alarm (SA) bit in the CSR is set. The SA bit will be set when 16 characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described in Paragraph 4.4.6 to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE
If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity, the LSI-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo, it should ensure that DZV11 receiver interrupts are inhibited. This should be done by raising the LSI-11 processor priority. The silo alarm interrupt feature can significantly reduce the LSI-11 processor overhead required by the DZV11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The transmitter interrupt enable (TIE) bit controls transmitter interrupts to the LSI-11 processor. If enabled, the DZV11 will interrupt the LSI-11 processor at the DZV11 transmitter interrupt vector when the transmitter ready (TRDY) bit in the CSR is set, indicating that the DZV11 is ready to accept a character to be transmitted.

4.4.6 Emptying the Silo
The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the silo so it will not be lost and will clear out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the data valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. The TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the silo to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo will not be available for at least one μs. Therefore, on fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of one μs. This will prevent a false indication of an empty silo.

4.4.7 Transmitting a Character
The program controls the DZV11 transmitter through four registers on the QBUS: the control and status register (CSR), the line parameter register (LPR), the transmit control register (TCR), and the transmit data register (TDR).

Following DZV11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the master scan enable (MSE) bit in the CSR. The program should set the transmitter interrupt enable (TIE) bit in the CSR if it wants the DZV11 transmitter to operate on a program interrupt basis.

The TCR is used to enable and disable transmission on each line. One bit in this register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC, and BICB instructions. (If word instructions are used, the line enable bits and the DTR bits are simultaneously accessed.)

The DZV11 transmitter is controlled by a scanner which is constantly looking for an enabled line (line enable bit set) which has an empty UART transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 2-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the LSI-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 3 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the line enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data lead for any line is the one state. The break bits are used to apply a continuous zero signal to the line. One bit in the TDR is associated with each line. The line will remain in this condition as long as the bit remains set. The program should use a MOVB instruction to access the BRK bits. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous zero sending state. The program may use this facility for sending precisely timed zero signals by setting the break bit and using transmit ready interrupts as a timer.

It should be remembered that each line in the DZV11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the one state at the end of the zero sending period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the zero sending period, the program should load an all-zero character to be transmitted. When the scanner requests service, indicating this character has begun transmission, the program should clear the BRK bit and load the next data character.

4.4.8 Data Set Control

The program may sense the state of the carrier and ring indicator signals for each data set and may control the state of the data terminal ready signal to each data set. The program uses two registers to access the DZV11 data set control logic. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The data terminal ready (DTR) bits in the TCR are read/write bits. Setting or clearing a bit in this register will turn the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and line enable bits will be simultaneously accessed.) The DTR bits are cleared by the INIT signal on the QBUS but is not cleared if the program clears the DZV11 by setting the CLR bit of the CSR.

The carrier (CO) and ring (RI) bits in the MSR are read-only bits. The program can determine the current state of the carrier signal for a line by examining the appropriate bit in the MSR. It can determine the current state of the ring signal by examining the appropriate bit of the ring register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16-bit register by using MOV or BIT instructions. The DZV11 data set control logic does not interrupt the LSI-11 processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

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