DK8-EP
programmable
real time clock
engineering drawings

digital equipment corporation · maynard, massachusetts

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DK8-EP-Ø	A	1	PROGRAMMABLE R.T. CLOCK
A-PL-DK8-EP-Ø	A	1	PROGRAMMABLE R.T. CLOCK (PL)
E-CS-M86Ø-Ø-1	#	3	REAL-TIME CL. CONTROL, DK8-EP
E-CS-M518-Ø-1	#	3	SCHMITT TRIGGERS & INPUT LOGIC
A-SP-DK8-EP-1	REF	11	DK8EP CLOCK SPECIFICATION
A-SP-DK8-EP-2	REF	5	ACCEPTANCE PROCEDURE
A-AL-DK8-EP-3		1	ACCESSORY LIST (DK8-EP)

REVISIONS			
REV.	DATE	CHG. NO.	APP'D
A	10/71	DK8E-4	A.W.
B	1/72	LAB8E-13	G.B.

DRN D. CRABBE DATE 4-1-71
CHK'D DATE 4-28-11
ENG. DATE 4-28-11
PROJ. ENG. DATE
PROD. DATE
PROJECT
SCALE
SHEET 1 OF 1

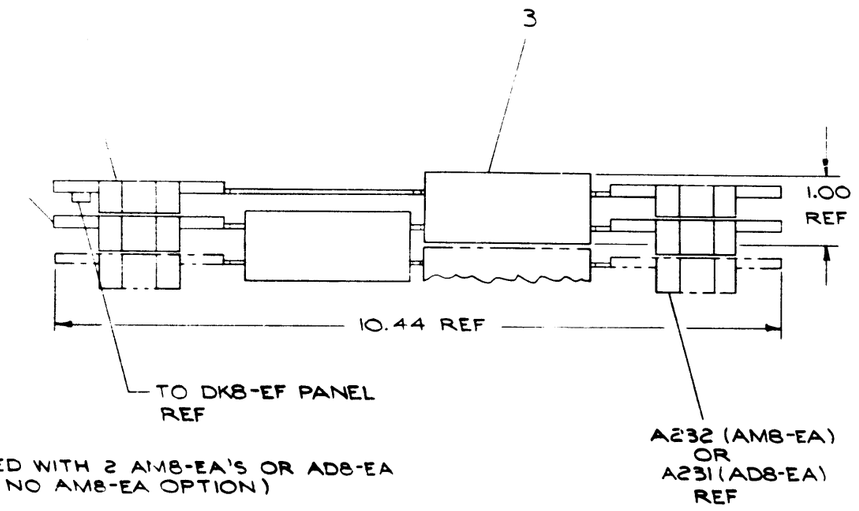
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
DK8-EP PROGRAMMABLE R.T. CLOCK

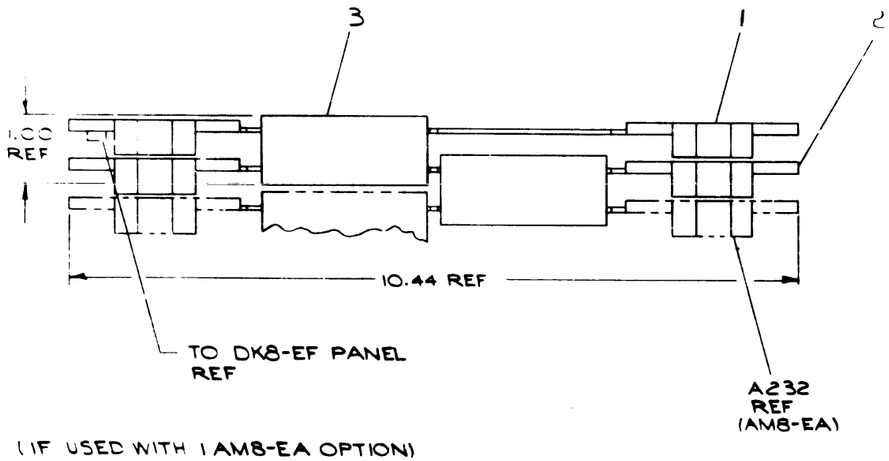
SIZE	CODE	NUMBER	REV.
A	ML	DK8-EP	B

DIST

DEC FORM NO 16-013
DMA 108



(IF USED WITH 2 AM8-EA'S OR AD8-EA WITH NO AM8-EA OPTION)



(IF USED WITH 1 AM8-EA OPTION)

NOTES:
1. ITEM NO.1 AND NO.2 MUST ALWAYS BE FACING FRONT OF MACHINE AS SHOWN.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

REVISIONS			
REV.	CHANGE NO	CHK	
A	[illegible]	[illegible]	

FIRST USED ON OPTION/MODEL: LAB8-E

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
± .005 ± 1/64 ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

		DATE
DRWN	[illegible]	4-27-71
CHK'D	W K Cudde	4-28-71
ENG	W K Cudde	4-28-71
MFG	[illegible]	4-28-71
QUAL	[illegible]	4-29-71

NEXT HIGHER ASSY: D-UA-DK8-ES-Ø
SCALE: 1/1
SHEET: 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: PROGRAMABLE R.T. CLOCK

SIZE: D | CODE: UA | NUMBER: DK8-EP-Ø | REV: A

DIST.

DEC FORM NO CRD 100

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY D.K. CRABBE	CHECKED O.K. Crabbe	SECTION
DATE 4-1-71	DATE 4-28-71	1
ENG O.K. Crabbe	PROD Paul Green	ISSUED SECT.
DATE 4-28-71	DATE 5/3/71	1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
1	M518	SCHMITT TRIGGER & INPUT LOGIC	1
2	M860	REAL-TIME CL. CONTROL, DK8-EP	1
3	B-UA-H851-Ø-Ø	EDGE CONNECTOR H851	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
PROGRAMABLE R.T. CLOCK	D-UA-DK8-EP-Ø	A	PL	DK8-EP-Ø	A	DK8E-CCCC4
	SHEET 1 OF 1	DIST				

DEC FORM NO 16-1031

AA2, BA2, CA2 +5V

AC2, AF1, AF2, AN1, AN2, AT1
AT2, BC1, BC2, BF1, BF2, BN1
BN2, BT1, BT2, CC1, CC2, CF1
CF2, CN1, CN2, CT1, CT2, DC1
DC2, DF1, DF2, DN1, DN2, DT1, DT2

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C57 C58 C59

C57: 6.8UF 35V
C58: 6.8UF 35V
C59: 6.8UF 35V

6 5 4

MB60

E5 E4 E3 E2 E1
E10 E9 E8 E7 E6
E15 E14 E13 E12 E11
E20 E19 E18 E17 E16
E24 E23 E22 E21
E27 E26 E25
E30 E29 E28
E33 E32 E31
E38 E37 E36 E35 E34
E42 E41 E40 E39
E47 E46 E45 E44 E43
E52 E51 E50 E49 E48

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52

C57 — C58 — C59

R8 R1 R11 C53 R9 D3 R10 R3 D1 R2 C54 R4 R7 R6 D2 C55 R5 C56 R15 R14 C62 R16 C61 R13 C60 R12

A B C D

8.44 REF

NOTES:
1. UNLESS OTHERWISE NOTED:
CAPACITORS ARE .01UF 100V 20%
DIODES ARE D664
ICS ARE DEC 7400
RESISTORS ARE 1/4W 5%

DEC 384	1	8		
DEC 74*5	11	4		
DEC 8881	8	16		
DEC 830	1	8		
DEC 9300	1	8		
DEC 8266	8	16		
IC TYPE	GND	+5V	ITEM NO.	ASSY.

ETCH BOARD REV F

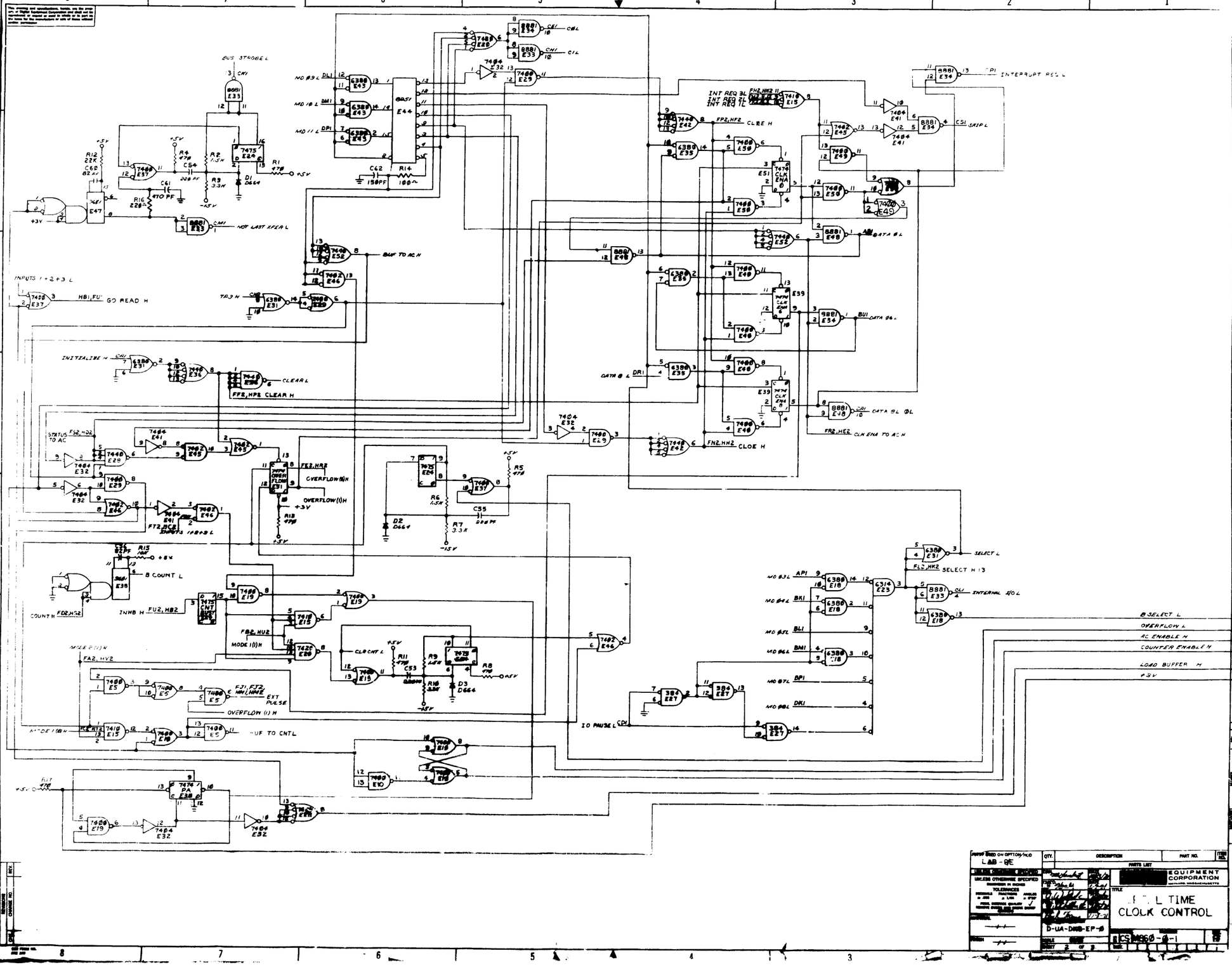
DIGITAL EQUIPMENT CORPORATION

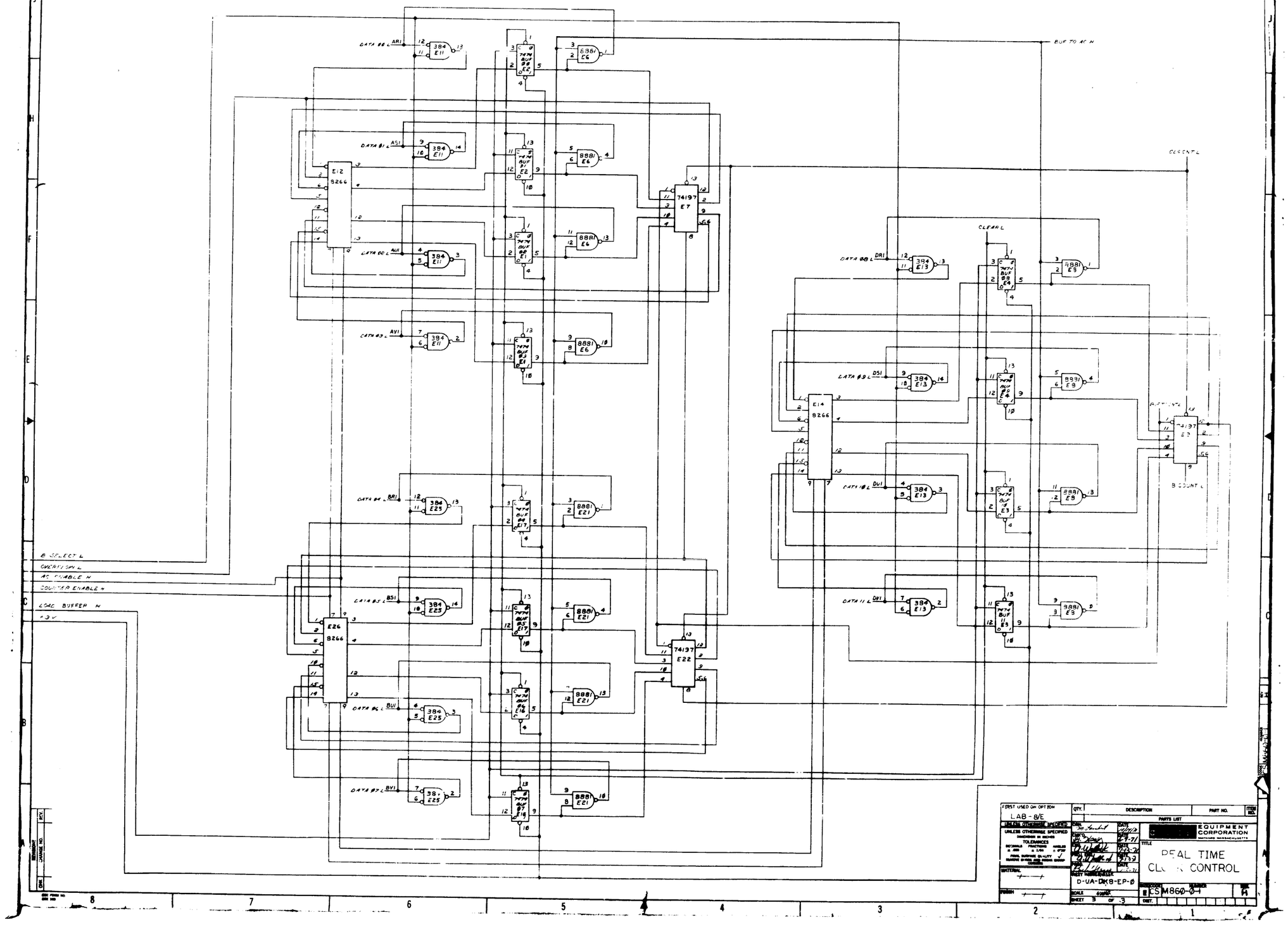
REAL TIME CLOCK CONTROL

D-MA-8W8-EP-0

MB60

QTY.	REF DESIGNATION	DESCRIPTION	PART NO.
		CAP 470PF 100V ±2%	1300224
		RES 220 1/4W 5%	3002271
		RES 100 1/4W 5%	3001001
		RES 22K 1/4W 5%	3012296
		RES 10K 1/4W 5%	3009779
		RES 3.3K 1/4W 5%	3004439
		RES 1.5K 1/4W 5%	3003971
		RES 470 1/4W 5%	3003716
		CAP .01UF 100V 20% DISC	1000819
		CAP 150PF	1000819
		CAP .047F 100V 20% DISC	1001610
		CAP 6.8UF 35V 20% TANT	1000367
		CAP 220PF 100V 5% DIP	1000021
		CAP 0.22UF 100V 5% DIP	1000015
		CAP 6.8UF 35V 20% DIP	1000367
		DIODE D664	1100114
		IC DEC 7437	1909032
		IC DEC 8281	1909398
		IC DEC 8214	1909732
		IC DEC 8300	1905777
		IC DEC 8266	1909934
		IC DEC 8881	1909705
		IC DEC 7408	1905456
		IC DEC 384	1901982
		IC DEC 9601	1901373
		IC DEC 7415	1901050
		IC DEC 7402	1901004
		IC DEC 7440	1901379
		IC DEC 7430	1905577
		IC DEC 7410	1905576
		IC DEC 7400	1905575
		IC DEC 7414	1905547
		SOCKET 936-11 STANDOFF	9006760
		HANDLE-PRINTED CIRCUIT BOARD	9007197-06
		1940 CABLE ASSY	9007764
		PRINTED CIRCUIT BOARD	7007813
		MODIFY PER DWG	
		ASSY PER DWG	
		X-Y COORDINATE HOLE LOC	


BUS STROBE L
INITIALIZE H
INPUTS 1+2+3 L
HBI,FU1 GO READ H
TR3 H
BUF TO AC H
NOT LAST XFER L
CLEAR L
FF2,HF2 CLEAR H
STATUS TO AC
FS2,HS2
FT2,HT2
OVERFLOW(0)H
OVERFLOW(1)H
B COUNT L
COUNT H
INHB H
FU2,HB2
MODE 1(1)H
FA2,HV2
EXT PULSE
FJ1,FJ2,HJ1,HJ2
BUF TO CNTL
CLR CNT L
INT REQ 3L
INT REQ 5L
INT REQ 7L
FN2,HN2
CLBE H
CLOE H
DATA 0 L
DATA 8 L
DATA 9 L
CLK ENA TO AC H
INTERRUPT REQ L
CSI SKIP L
IO PAUSE L
SELECT L
SELECT H 13
INTERNAL I/O L
B SELECT L
OVERFLOW L
AC ENABLE H
COUNTER ENABLE H
LOAD BUFFER H
+5V
REAL TIME CLOCK CONTROL
EQUIPMENT CORPORATION
D-LA-DMB-EP-B
MAINDEC-08-DLAB-D



FIRST USED ON OPTION: LAB-8/E

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINISH: SURFACE QUALITY MARKING SHALL BE MACHINE STAMP

MATERIAL

FINISH

PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.

DRWN [illegible] DATE 2-9-71
CHK'D [illegible] DATE 2-23-71
APVD [illegible] DATE 3-1-71
MFG APVL [illegible] DATE
TEST REQUIREMENTS: D-UA-DK8-EP-0

EQUIPMENT CORPORATION

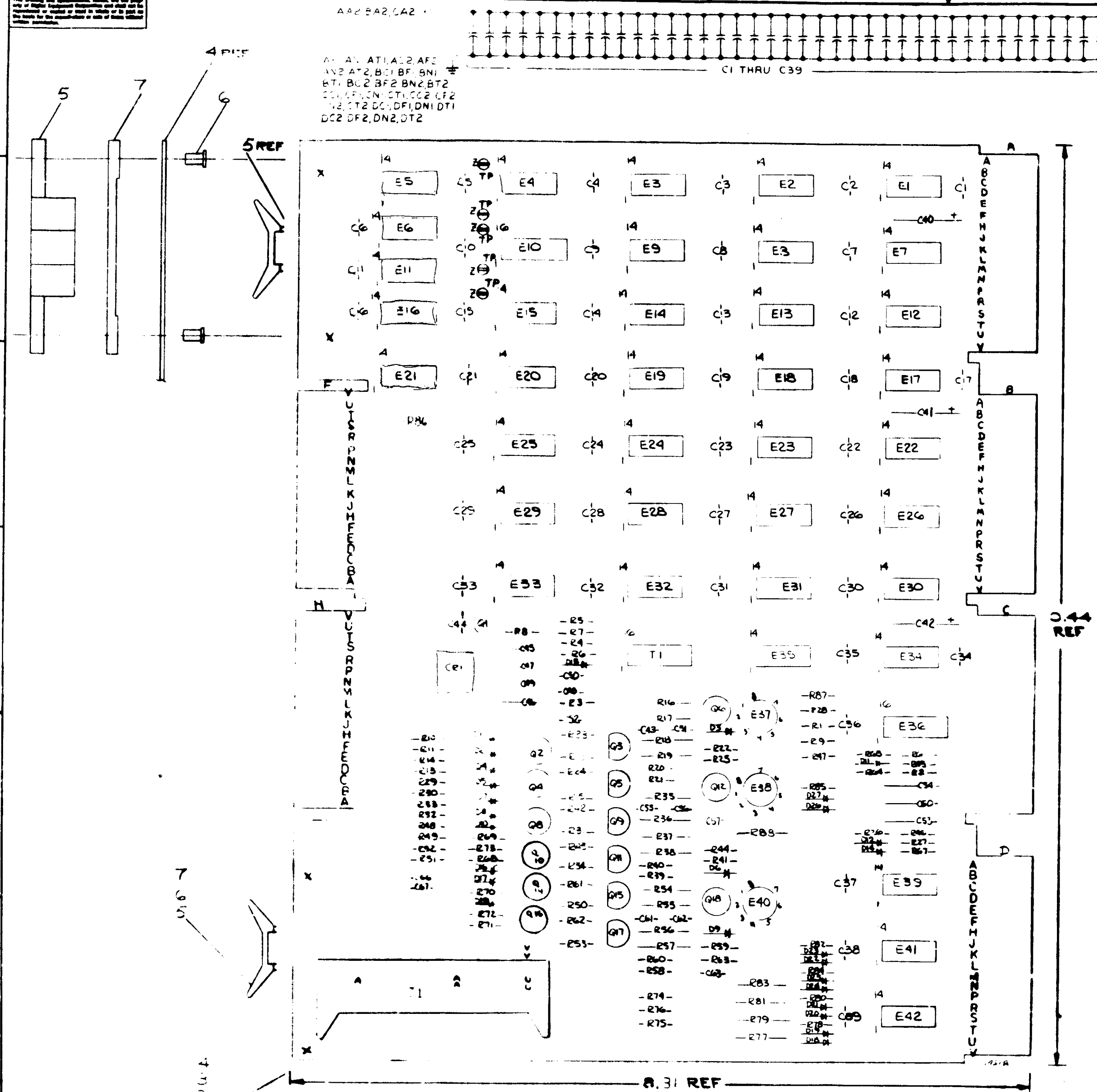
TITLE: REAL TIME CLOCK CONTROL

SCALE: none SHEET 3 OF 3

DRAWING NO. ES M860-0-1 REV. A1

DIST.

BILL OF MATERIAL: DRWG. NO. / CHANGE NO. / REV.



NOTES:

QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
3	R2 R46 R66	RES. 4.7K, 1/4W, 5%	1300447	54
3	C53, C54, C60	CAP 1000PF 100V 5% MICA	1000042	53
5		LUG, SPLIT	9006735	52
1	CR1	CRYSTAL 20MC	1809880	51
	J1	RIGHT ANGLE HEADER 40 PIN	1209941	50
1	T1	TRANSFORMER	1609651	49
6	Q2,Q4,Q8,Q10,Q14,Q16	TRANSISTOR 2N4250	1503142	48
7	Q1,Q3,Q5,Q9,Q11,Q15,Q17	TRANSISTOR DEC 3009B	1503100	47
3	Q6, Q12, Q18	TRANSISTOR DEC 6B	1509090-01	46
1	C47	CAP 100PF 100V 5% DM	1000016	45
1	C46	CAP 10PF 100V 5% DM	1000006	44
1	C45	CAP 47PF 100V 5% DM	1000011	43
1	C49	CAP 68PF 100V 5% DM	1000014	42
50	C1-C39,C43,C51-C52, C55-C57,C61-C63,C66,C67	CAP .01UF 100V 20% DM	1001610	41
3	C40-C42	CAP 6.8UF 35V 20% STANT	1000067	40
3	C44,C48,C50	CAP .047UF 16V +5-20% CER	1009678	39
25	D1-D15, D18-D27	DIODE D664	1100114	38
2	D16, D17	DIODE 1N752A	1102808	37
2	R16-R19,R35-R38,R54-R57	RES 34.8K 1/8W 1% MF	1303156	36
5	R77,R79,R81,R83,R88	RES 47Ω 1/2W 5%	1301695	35
6	R15,R31,R34,R50,R53,R12	RES 270K 1/4W 10%	1301310	34
5	R27,R28,R45,R47,R67	RES 470Ω 5%	1300316	33
15	R1,R4,R5,R7,R21,R40,R60,R68, R70,R74,R75,R76,R86,R87,R9	RES 1K	1300365	32
14	R6,R10,R13,R25,R29,R32, R44 R48,R51,R63 R85	RES 3.3K	130[illegible]	31
1	R3	RES 220	1300271	30
4	R78,R80,R82,R84	RES 270Ω	1301972	29
6	R11,R14,R30,R33,R49,R52	RES 47K	1302177	28
3	R26,R64,R65	RES 1.5K	1300391	27
3	R22,R41,R59	RES 2.2K	1300417	26
6	R23,R24,R42,R43,R61,R62	RES 8K	1302465	25
3	R20,R39,R58	RES 62K	1304840	24
2	R69,R72	RES 750Ω	1301401	23
2	R71,R73	RES 10Ω	1301317	22
1	R8	RES 10K 1/4W 5%	1300479	21
3	E7, E22, E34	I.C. DEC 380	1909485	20
2	E19, E41	I.C. DEC 7404	1909686	19
3	E8,E23,E35	I.C. DEC 888	1909705	18
1	E10	I.C. DEC 74151	1909936	17
1	E42	I.C. DEC 7417	1909929	16
10	E1,E12,E14,E16,E17,E20, E26,E30,E32,E33	I.C. DEC 7400	1905575	15
7	E2,E13,E18,E21,E24,E27,E31	I.C. DEC 7474	1905547	14
4	E3,E25,E28,E29	I.C. DEC 7402	1909004	13
5	E4,E5,E6,E11,E15	I.C. DEC 7490	1909051	12
1	E9	I.C. DEC 7410	1905576	11
1	E36	I.C. DEC 7475	1909050	10
1	E33	I.C. DEC 7470	1905589	9
3	E37,E38,E40	I.C. DEC [illegible]	1909344	8
2		SPACER (CABLE CLAMP)	1202704	7
4		EYELET GS4-11 STIMPSON	9006780	6
2		HANDLE FLIP CHIP-MAGENTA	9008337-06	5
1		ETCHED CIRCUIT BOARD	5009630	4
REF		MODULE HISTORY DWG	B-MH-M518-0-6	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AM-M518-0-5	2
REF		X-Y COORDINATE HOLE LOC.	K-CO-M518-0-4	1

PARTS LIST

IC TYPE	GND	+5V
DEC 380		8
DEC 7415	8	16
DEC 7490	10	5
DEC 7475	12	5

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTFULLY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO	AWG	FROM PT	TO PT

JUMPER LIST

DEC NO.	EIA NO.
2N4250	—
DEC 6B	—
DEC 3009B	2N3009
1N752A	SAME
D664	1N3606

SEMICONDUCTOR CONVERSION CHART

FIRST USED ON OPTION/MOD: LAB-8/E

ETCH BOARD REV E

ORIGINATED M518-00001 A WALLACK
E M518-00002 A WALLACK

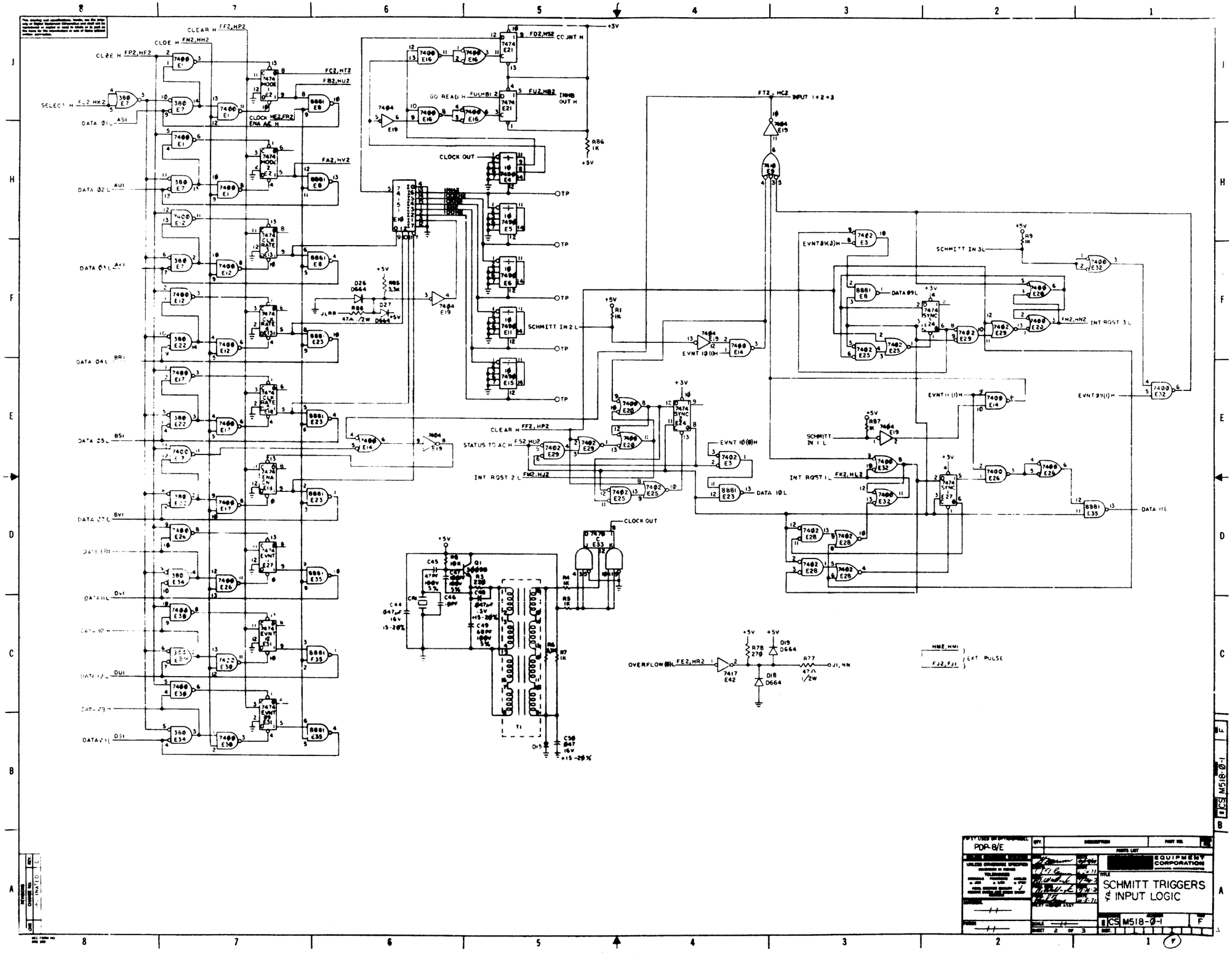
[redacted] EQUIPMENT CORPORATION

TITLE: SCHMITT TRIGGERS & INPUT LOGIC

NEXT HIGHER ASSY D-UA-DK8-EP-0

E CS M518-0-1 REV F

SCALE 2/1 SHEET 1 OF 3


CLEAR H FF2,HP2
CLOE H FN2,HH2
CLRE H FP2,HF2
SELECT H FL2,HK2
DATA Ø1 L ASI
DATA Ø2 L AUI
DATA Ø4 L AVI
DATA Ø8 L BRI
DATA 25 L BSI
DATA 27 L BVI
DATA 28 L
DATA 29 L
DATA 30 L DVI
DATA 31 L DUI
DATA 32 L
DATA 33 L DSI
FC2,HT2
FB2,HU2
FA2,HV2
CLOCK HF2,FR2 ENA AC H
GO READ H FU1,HB1
FD2,HS2 CO JNT H
FU2,HB2 INHB OUT H
CLOCK OUT
SCHMITT IN 2 L
SCHMITT IN 3 L
SCHMITT IN 1 L
INPUT 1+2+3
FT2, HC2
EVNT Ø8(8) H
EVNT 10 (10) H
EVNT 11 (11) H
EVNT Ø9 (1) H
DATA Ø9 L
DATA 10 L
DATA 11 L
INT RQST 3 L
INT RQST 2 L
INT RQST 1 L
FH2,HN2
FK2,HL2
FM2,HJ2
FS2,HU2
STATUS TO AC H
OVERFLOW L FE2,HR2
FJ2,FJ1 EXT PULSE
+3V
+5V
TP
D26 D664
D27 D664
D18 D664
D19 D664
R86 1K
R88 47Ω /2W
R85 3.3K
R1 1K
R9 1K
R87 1K
R78 270
R77 47Ω 1/2W
R4 1K
R5 1K
R7 1K
C44 .047μF 16V ±5-20%
C45 47PF
C46 100PF
C47 .047μF ±5%
C48 220PF
C49 680PF
C50 .047 16V +15-20%
Q1 2N4058
T1
D15
CR
PDP-8/E
EQUIPMENT CORPORATION
SCHMITT TRIGGERS & INPUT LOGIC
CS M518-0-1
SHEET 2 OF 3
SIZE F
DWG NO CS M518-0-1
REV F

SCHMITT IN 1L

SCHMITT IN 2L

SCHMITT IN 3L

+15V DA2

+6.2 V

COMMON

-6.2 V

-15V A82 B82 C82

J1A,B,C,E,H,K,M,P,S,U,W,Y,AA,CC,EE,HH,KK,MM,PP,SS,UU AND VV

PDP-8/E

DIGITAL EQUIPMENT CORPORATION

SCHMITT TRIGGERS & INPUT LOGIC

SIZE E CS M518-0-1 REV F

SHEET 3 OF 3

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 7/24/71

TITLE REAL TIME CLOCK, DK8-EP

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	ABSE-00013	LAWRANCE	1-6-72	[illegible]	2-1-72

ENG G.Wallack APPD D.D.Mash

SIZE	CODE	NUMBER	REV
A	SP	DK8-EP-1	A

DEC FORM NO. DRA 107

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE Real Time Clock, DK8-EP

1. Overall Description

The DK8-EP is an option, to the PDP-8/E computer, that may be used to measure or count intervals of time in a large variety of ways. Major features include: a 12 bit counter and overflow logic utilizing MSI circuits; a 12 bit clock buffer register; 5, program selectable, count rates plus provisions for an external clock source; crystal controlled clock for accuracy and stability and 3 external input circuits that feature variable threshold Schmitt triggers. The Schmitt Triggers are a feature only used with the DK8-ES option.

2. General Specifications

2.1 The basic system includes: the 12 bit counter plus overflow; 12 bit clock buffer register; the crystal controlled clock and frequency dividers; the I/O and control logic and the external sync logic.

2.2 Option jumpers on the M518 module connect in the Schmitt triggers to the external sync logic.

2.3 All control functions, IOT decoding and registers are contained on 1 8½ inch Quad board numbered M860. The input logic and Schmitt triggers are contained on another Quad board, number M518. The modules are connected together with a top connector type H851 that connects the boards together on the top fingers of the boards.

2.4 Operating Conditions are:

Temperature: 30 F to 130 F
Relative humidity: 10 to 90%, non-condensing
Power Required: M518-430ma at +5 volts
120ma at +15 volts
120ma at -15 volts
M860-900ma at +5 volts

2.5 Logically the DK8-EP contains the following features:

2.5.1 Clock Enable Register
The clock enable register provides for:
a) Clock rate selection
b) Mode control
c) Interrupt enable
d) External event enable
e) Overflow to Interrupt

SIZE	CODE	NUMBER	REV
A	SP	DK8-EP-1	A

DEC FORM NO 16-1022 DRA 107

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE Real Time Clock, DK8-EP

f) Ext start pulse
g) Inhibit Clock pulses

This register is under the control of 3 IOT's
a) 6130: Zeroes to the clock enable register
b) 6132: Ones to the clock enable register
c) 6134: Clock enable register to the AC.

2.5.2 Clock Buffer
The clock buffer stores data being transferred from the AC to the clock counter or from the clock counter to the AC.

2.5.3 Clock Counter

The clock counter is a 12 bit binary up counter using MSI circuits with overflow which is sent off the board via the edge connector. The contents of the clock counter maybe transferred to the clock buffer or the clock counter maybe preset by the clock buffer. When overflow occurs, the clock buffer is automatically loaded into the clock counter when in certain modes.

2.5.4 Programmable Time Base
The program selectable time base provides pulses to the clock counter according to the rate set in the clock enable register. Rates range from 1 M Hz. to 100 Hz., in powers of ten, plus an external input. The clock pulses may be inhibited by setting bit 7 in the clock enable register.

2.5.5 External Input Channels
The three external input channels with Schmitt triggers may provide for three separate input events which can actuate the clock, cause an interrupt or skip pulse or cause the contents of the clock counter to be transferred to the clock buffer. These functions are controlled by the clock enable register.

SIZE	CODE	NUMBER	REV
A	SP	DK8-EP-1	A

DEC FORM NO 16-1022 DRA 107

CONTINUATION SHEET

TITLE Real Time Clock, DK8-EP

2.5.6 Crystal Clock
The crystal clock is an extremely simple clock operating at 20 M Hz. and requires no adjustments. MSI circuit decade counters are used to divide the base clock frequency down to:

a) 1 M Hz.
b) 100 K Hz.
c) 10 K Hz.
d) 1 K Hz.
e) .1 K Hz.

2.5.7 Schmitt Triggers
The Schmitt triggers on the M518 module are threshold dectors that can accept pulse or continuously varying analog inputs. Inputs to the Schmitt triggers may be cabled directly to the M518 or may be brought through the optional front panel, DK8-EF. TTL signals may be brought onto the M518 via the edge connector to actuate the input sync logic. The signal must transition to Ø volts from a nominal +3 volts for a minimum duration of 100 ns. The Schmitt triggers have the following characteristics:

Nominal Input Voltage Range	±5 Volts
Input Type	Differential
Input Impedance	50K Ohms
Minimum Input Pulse Width	2 u sec.
Maximum Input Voltage	±50 Volts
Hysteresis	0.3 Volts
Common Mode Rejection	35 db.
Propogation Delay	600 ns.

When connected to the Laboratory Peripheral Panel, DK8-EF:

Input Threshold - Variable between ±5 Volts
Slope - + & -, Switch selectable
Output Voltages - A) Ø to 5V (falling edge denotes firing of shmitt and resets on recrossing the threshold voltage for OUT 1, 2, and 3.
B) Clock in and Overflow Out - 0 to 5 V

SIZE	CODE	NUMBER	REV
A	SP	DK8-EP-1	A

DEC FORM NO DRA 107A

2.5.8 Input Synchronization Logic
The major features of the input sync logic are:

2.5.8.1 Input Channels
There are three input channels which are used to convert asynchronous external events into synchronized control and status signals for the clock control logic. The three inputs may be driven from the Schmitt triggers or directly with an external TTL signal.

2.5.8.2 Input Enable Flip-Flop
This flip-flop, if set to a one, enables the pulse from the sync logic to reach the control gating. It is set and cleared under program control.

2.5.8.3 Input Flip-Flop
The input flip-flop is set by an external signal from either the Schmitt triggers or external TTL signal. The input flip-flop provides synchronization between asynchronous external events and internal clock timing.

2.5.8.4 Sync Flip-Flop
The sync flip-flop is loaded with the input flip-flop on the next Status to AC IOT and continues to remain set during succeeding Status to AC IOT's. When the sync flip-flop is loaded, the input flip-flop is cleared.

2.5.8.5 Enable Event Interrupt
This flip-flop connects the sync flip-flop to the interrupt request line on the Omnibus. It is set and cleared via bit 8 in the clock enable register.

3. Specification of Vendor Supplied Equipment

See applicable Purchase Specifications for board components.

4. Programming

4.1 The IOT instructions are:

Mnemonic	Octal Code	Function
CLZE	6130	Ø's to the Clock Enable register corresponding to those bits set to a 1 in the AC. The AC is not cleared.
CLSK	6131	Skip on clock interrupt. Interrupt conditions are: a) Overflow status set to a 1. b) Any of the 3 sync flip-flops set to a 1 in the status register.
CLOE	6132	Ones to the Clock Enable register corresponding to those bits set to a 1 in the AC. The AC is not cleared.
CLAB	6133	Contents of the AC are loaded into the clock then to the buffer and counter. The AC is not cleared.
CLEN	6134	Contents of the clock enable register are loaded into the AC. Previous contents of the AC are lost.

Clock Enable Registers Function

AC Bit	Functions
Ø	Enable clock overflow to set bit Ø of the status register.
1 & 2	Mode Control ØØ Counter runs at selected rate. Overflow occurs every 4096 counts. Overflow remains set until cleared by the IOT 6135. Ø1 Counter runs at selected rate. Overflow causes the clock buffer to be transferred to the clock counter which continues to run. Overflow remains set until cleared with IOT 6135. 1Ø Counter runs at selected rate. When an enabled event occurs, the clock counter is transferred to the clock buffer and the counter continues. 11 Counter runs at selected rate. When an enable event occurs, the clock counter is transferred to the clock buffer and the clock counter continues to run from Ø.
3,4 & 5	Count Rate ØØØ Stop ØØ1 External clock source Ø1Ø Ø.1 K Hz. Ø11 1 K Hz. 1ØØ 1Ø K Hz. 1Ø1 1ØØ K. Hz. 11Ø 1 M Hz. 111 Stop
6	When set to 1, overflow causes an EXT start pulse.
7	When set to a 1, the crystal clock circuit is inhibited from generating clock pulses that increment counter.
8	Enabled events in channels 1, 2 or 3 or an enabled overflow (bit Ø) cause an interrupt request when bit 8 is set to a one.

AC bit	Functions
9, 10 & 11	Enable events 9 - input 1 10 - input 2 11 - input 3

Mnemonic	Octal Code	Function
CLSA	6135	The contents of the clock status register is loaded into the AC and then cleared in the status register. This prevents status information from being lost during the interrogation of the status register.

Clock Status Register.

AC bit	Status Condition
Ø	Overflow
1 thru 8	not used
9	input 1
1Ø	input 2
11	input 3

Mnemonic	Octal Code 1	Function
CLBA	6136	The contents of the clock buffer are loaded into the AC. Old value of the AC is lost.
CLCA	6137	The contents of the clock counter are transferred into the clock buffer and then the contents of the clock buffer are loaded into the AC. The old value of the AC is lost.

NOTE:

The clock counter may be rea ile it is counting. Gating in the clock control prevents data from being strobed out of the counter after a specified time after a clock pulse. This specified time, approximately 500 ns., allows the data to "settle" in the counter. This feature allows the counter to be read any number of times without introducing timing errors, in counting the amount of time between intervals and also eliminates false counts that are the result of reading the counter as one or more bits are in transition from one state to another.

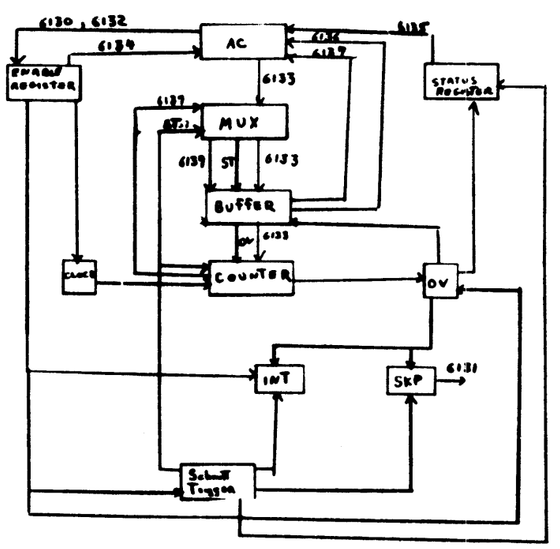
4.2 There are no maintenance instructions.

4.3 Data format is 12 parallel bits to and from counter and to and from buffer. The clock counter may be incremented in a binary count sequence.

4.4 There are no operator controls.

5. Interface Specifications

All signals to and from the DK8-EP to the computer conform to the constraints of the 8/E bus.



INSTALLATION PROCEDURES DK8EP/DK8ES

1. Verification of Parts

   A. 1 ea. M518 module
   B. 1 ea. M860 module
   C. 1 ea. H851 top block connector (2 if AD8-E is installed) For DK8ES option add
   D. 1 ea. 7008492 diagnostic jumper cable
   E. DKEF front panel assy
   F. 5-BNC Connectors
   G. Three (3) standard 3 conductor phone plugs #12-Ø943Ø.

2. Installation (DK8EP)
   A. Install M860 and M518 modules as per D-MU-LAB8-E-4.
   B. Install top block connector as specified in D-MU-LAB8-E-4 (connector may be installed on either side of the module)

3. Installation (DK8ES)

   A. Install DK8EF front panel assy in H945 option box.
   B. Install M860 module as per D-MU-LAB8-E-4.
   C. Attach DK8EF panel cable to M518 module after routing it through the H945 option box.
   D. Install M518 and M851 as per D-MU-LAB8-E-4.
   E. Check if AD8-E or AM8-E option are installed. If yes, then attach another H851 as specified in the MUL to these options.

4. Refer to acceptance and checkout procedures and Maindec for checkout and shipping software.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 09/15/71

TITLE DK8-EP/DK8-ES ACCEPTANCE PROCEDURES

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	LABBE 00013	LAWRENCE	1-6-72	[illegible]	1-7-72

ENG [signature] APPD [signature] SIZE A CODE SP NUMBER DK8-EP-2 REV A

DEC FORM NO. DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DK8-EP/DK8-ES ACCEPTANCE PROCEDURES

SCOPE: The purpose of this procedure is to establish the minimum requirements for DK8-EP and DK8-ES acceptance testing.

I. SHIPPING HARDWARE
- A. DK8-EP
  1. M860 - Control Module
  2. M518 - Schmitt Triggers and Logic Module
  3. M851 - Edge connector
- B. DK8-ES
  1. DK8-EP
  2. DK8-EF - Front Panel Assembly
  3. Diagnostic Jumper Cable - #70-08492
  4. Five (5) BNC Connectors #12-01655 DEC
  5. Three (3) standard 3 conductor phone plugs- #12-09430

II. SHIPPING DOCUMENTATION AND SOFTWARE
- A. Print Sets
  1. A-ML-DK8-EP
  2. A-ML-DK8-ES
- B. Diagnostic Software
  1. Maindec-8E-D8AC-PB
  2. Maindec-8E-D8AC-D-(D)
- C. Manuals
  1. Lab-8E Maintenance Manual
  2. Lab-8E Users Guide
  3. Lab-8E Programming Card

III. TEST HARDWARE
- A. DK8EP
  1. Oscilloscope
- B. DK8-ES
  1. Oscilloscope - Model 453 or equivelent.
  2. Two (2) scope probes.

IV ACCEPTANCE TESTS
- A. DK8-EP - this section is to be completed for DK8-EP and DK8-ES options.

NOTE: See A-AL-DK8-EP-3; A-AL-DK8-ES-1; A-AL-DK8-EF-1 for a detailed shipping list.

SIZE A CODE SP NUMBER DK8-EP-2 REV A

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DK8-EP DK8-ES ACCEPTANCE PROCEDURES

IV. ACCEPTANCE TESTS
- A. 1. DK8-EP/ES Register Test
  - a. Load Maindec-8E-D8AB-PB as per its document.
  - b. Load 0200 into the switch register.
  - c. Depress Addr Load then clear the switch register.
    1. Set bit 00 to a "1".
  - d. Depress Clear Key then the Continue Key.
  - e. Observe printout - DK8E CLOCKS DIAGNOSTIC.
  - f. After each pass the program will printout DK8E PASS COMPLETE.
  - g. Allow the test to run for five (5) passes.
    1. Each pass takes approximately 3.5 minutes
  - h. Pass - five (5) passes without an error printout.

NOTE: If the clock option is a DK8-ES proceed to section IV.B.

2. External Pulse Test
- a. Load 0200 into the switch register.
  1. Depress Addr Load
- b. Set switch register to 0020
  1. Depress Clear Key, then the Continue Key
- c. Observe printout - DK8E CLOCKS DIAGNOSTIC
- d. With the oscilloscope observe a 40 microsecond pulse rate at pins FJ2, FJ1, HM1, and HM2 on the edge connectors which connect the M860 and the M518 modules.

NOTE: Set TIME/DIV to 10 microseconds to observe this signal. Scope synchronization may be difficult. The waveform is aperiodic.

This concludes the DK8-EP Acceptance Testing.

SIZE A CODE SP NUMBER DK8-EP-2 REV A

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DK8-EP/DK8-ES ACCEPTANCE PROCEDURES

IV. ACCEPTANCE TESTS
- B. DK8-ES
  1. External Pulse Test
  - a. Load 0200 into the switch register then depress the Addr Load Key.
  - b. Set switch register to 0020, then depress the Clear Key and the Continue Key.
  - c. Observe printout - DK8E CLOCKS DIAGNOSTIC
  - d. With the oscilloscope observe a 40 microsecond pulse rate at pins FJ2, FJ1, HM1 and HM2 on the edge connectors which connect the M860 and M518 modules.

NOTE: Set TIME/DIV to 10 microseconds to observe this signal. Scope synchronization may be difficult. The waveform is aperiodic.

- e. Place the scope probe on the connector, on the front panel, which is labeled OVERFLOW.
  1. Observe a signal whose pulse rate is 40 microseconds.

2. External Clock Test
- a. Load 0200 into the switch register, then depress Addr. Load.
- b. Set the switch register to 0014.
  1. Depress Clear Key then the Continue Key.
- c. Observe printout - DK8E CLOCKS DIAGNOSTIC.
- d. On the front panel, DK8-EF, ground the input CLOCK IN.
  1. The TTY bell should ring

3. DK8-EF Front Panel Check
- a. Turn off computer power.
- b. Plug the test cable #70-08492 into the 28 VAC RECEPTACLE J5 on the processor, and plug the three phone jacks into the front panel inputs marked In 1, In 2, and In 4. Turn computer power on.
  1. Place slope 1, 2, and 3 switches to the + position.

NOTE: Never install or remove the 7008492 Diagnostic cable with power on. Serious damage to the H724 Transformer may result as plugs are inserted into panel on a live machine.

SIZE A CODE SP NUMBER DK8-EP-2 REV A

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

IV. ACCEPTANCE TESTS

B. 3. c. Place a scope probe on out 1.
1. Observe a 60 hz square wave.
2. Check OUT 2 and OUT 4 four the same square wave.

d. Place a probe on OUT 1 and a second probe on OUT 2.
1. Place SLOPE 2 to the - position.
2. OUT 2 signal should be 180° out of phase with OUT 1.

e. Place the second probe from OUT 2 to OUT 4.
1. Place SLOPE 4 to the - position.
2. OUT 4 signal should be 180° out of phase with OUT 1.
3. Place SLOPE 1 to the - position
4. OUT 1 and OUT 4 should be in phase.
a. Place the three SLOPE switches to the + position.

f. While monitoring OUT 1 on the scope, rotate the appropriate THRESHOLD pot.
1. There should be a noticeable movement of the waveform in both directions.
a. The square wave may cut out at either or both ends of the THRESHOLD pot movement.
2. Repeat for OUT 2 and OUT 4.
a. Leave the THRESHOLD pots at mid-travel.

4. Schmitt Trigger Input Logic Test
a. Load 0200 into the switch register.
1. Depress Addr Load
2. Set switch register to 2000.
3. Depress Clear Key then the Continue Key.
b. Observe printout - DK8E CLOCKS DIAGNOSTIC
c. After each pass the program will printout DK8E PASS COMPLETE

NOTE: Random errors may be caused by noisy 6ØHz power. This can be verified by using a signal generator set to 6Ø Hz as the input to the Schmitt triggers.

d. Allow the program to make five (5) passes.
1. Each pass takes approximately two (2) minutes.

e. Pass - five (5) passes without an error printout.

This concludes the DK8-ES Acceptance Testing.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

DRAFT BY K.Symes DATE 12-17-71	CHECKED MH Lawrence DATE 12/21/71	SECTION
ENG DATE	PROD DATE 1/4/72	ISSUED SECT.

SPECIFIC
D EQUIPMENT
DN EQUIPMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO	DWG NO. / PART NO.	DESCRIPTION	QUANTITY VARIATION	KIT CHK BY	INSTALLATION BY
1	M518	Schmitt Trigger Module	1		
2	M860	Real Time Clock Control Module	1		
3	M8E	Edge Connector	1		
4	DK8-EP	DK8-EP Print Set	1		
5	LAB-8E	Lab-8/e Print Set	1		
6	MAINDEC 8E-D8AB-PB	DK8-EP Diagnostic - Binary Tape	1		
7	MAINDEC 8E-D8AB-DL	DK8-EP Diagnostic - Document	1		
8	DEC-LB-HRZA-D	Lab-8/e User's Handbook	1		
9	DEC-LB-HXZA-D	Lab-8/e Maintenance Manual	1		
10		Lab-8/e Programming Card	1		
		NOTE: When item 8 or 9 is temporarily waived,			
		ship the following:			
	A-SP-DK8EP-1	DK8EP Engineering Specification	1		
	A-SP-DK8EP-2	DK8EP Acceptance Procedure	1		

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV	ECO NO
DK8-EP Accessory List	SHEET 1 OF 2	A	AL	DK8-EP-3		