EK-DZQ11-UG-001

DZQ11 Asynchronous Multiplexer User's Guide

Prepared by Educational Services
of
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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZQ11 is a Q-bus option. Its outline is shown in Figure 1-1. The DZQ11 is an asynchronous multiplexer that interfaces between a Q-bus processor and four asynchronous serial data communication lines. It can be used in many applications such as data concentration, real-time processing, and cluster controlling. The DZQ11 communications interfaces are compatible with RS-232-C (V.28) and RS-423-A (V.10/X.26). There is enough modem control to permit dial-up (auto-answer) operation with full-duplex modems *, such as the Bell models 103, 113, 212, or equivalent. Remote full-duplex working, as a control (master) station over private lines, is also possible for point-to-point or multipoint operation. Figure 1-2 shows some possible applications for the DZQ11 in a Q-bus system.

All the DZQ11 parameters can be easily controlled. These parameters are:

- Baud rate
- Character length
- Number of stop bits for each line
- Odd or even parity for each line
- Transmitter receiver interrupts.

Additional features include:

- Limited modem control
- Zero receiver baud rate
- Break generation and detection
- Silo buffering of received data
- Line turnaround.

The DZQ11 is program-compatible with the Q-bus DZV11 and with the UNIBUS option DZ11-A. The only exception is the number of serial lines supported. The DZQ11 does not support 20 mA operation.

Documents describing the DZQ11 are:

- DZQ11 Asynchronous Multiplexer User's Guide – EK-DZQ11-UG
- DZQ11 Asynchronous Multiplexer Technical Manual – EK-DZQ11-TM
- Field Maintenance Printset – MP01795
- DZQ11 Maintenance Card – EK-DZQ11-MC

* The DZQ11 modem control does not support half-duplex operation or the secondary transmit-and-receive operation available on some modems (such as the Bell 202).

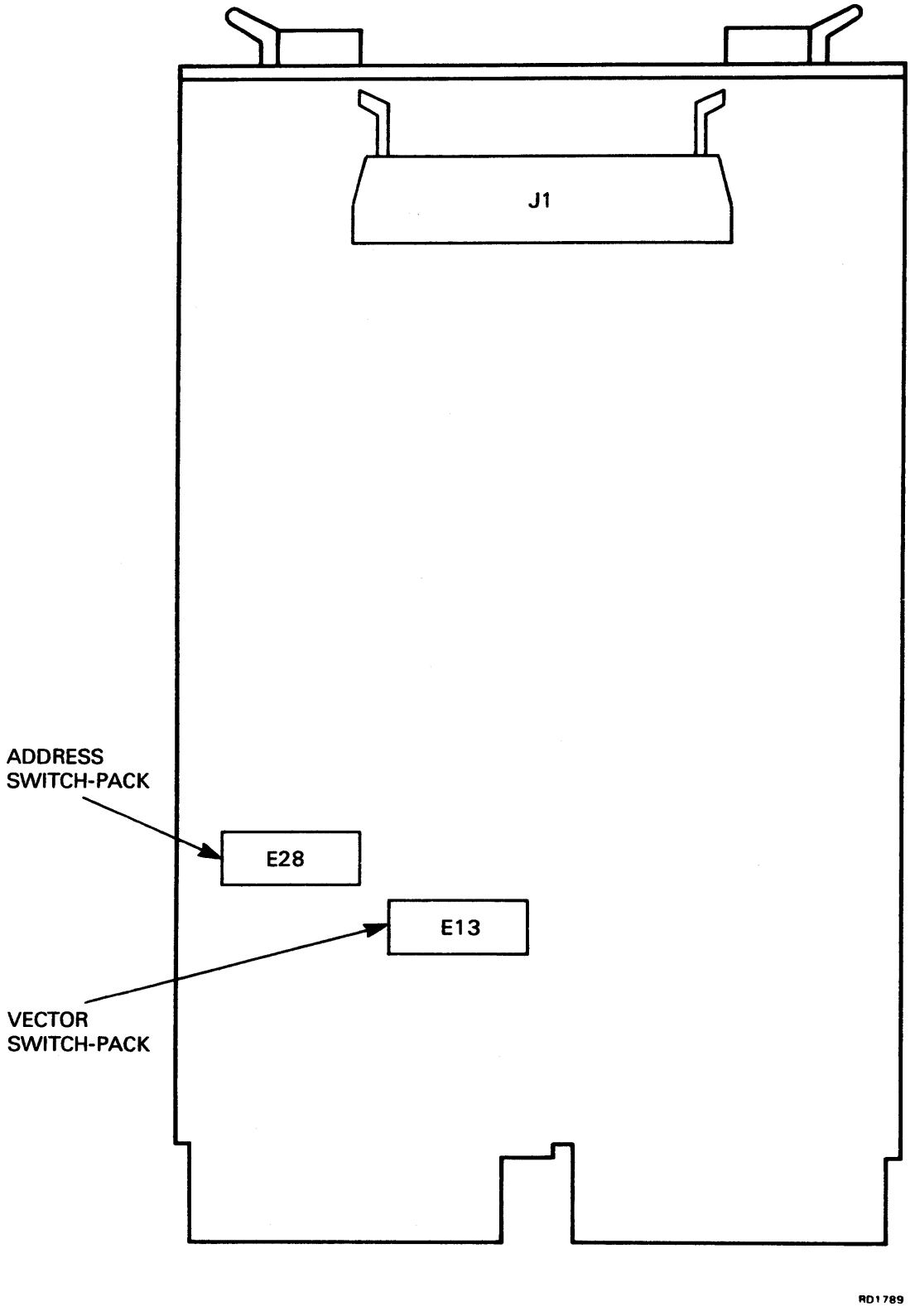


Figure 1-1 M3106 Module

1.2 PHYSICAL DESCRIPTION

The DZQ11 is made up of two components connected by a ribbon cable. The components are:

1. A single dual-height module, 21.6 × 13.2 cm (8.51 × 5.19 inches), called the M3106 module. All input and output connections are available on a Berg * header. This module includes all active circuitry as well as the line drivers and receivers.

2. A distribution panel 6.7 × 8.5 cm (2.6 × 3.3 in) which contains four filtered D-type connectors and a Berg header. This header connects to the M3106 by means of a 40-way ribbon connector.

NOTE

A G7272 Grant Continuity card may be needed. Refer to Section 2.3.2 for an explanation.

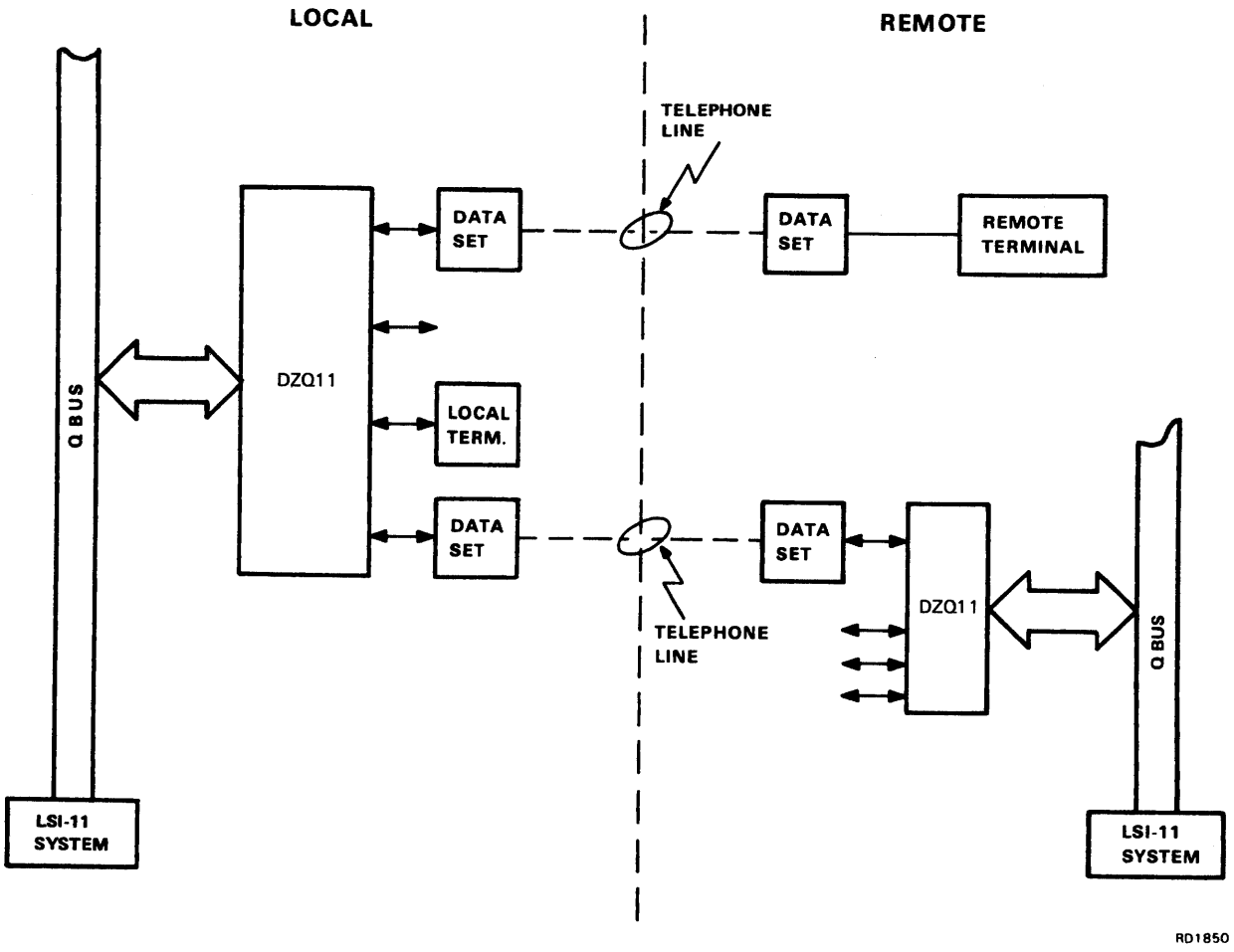


Figure 1-2 DZQ11 System Applications

* Berg is a registered trademark of the Berg Corporation.

1.2.1 DZQ11 Configurations

The basic option supplied is the DZQ11-M and is made up of the following:

1.	Logic Module	M3106
2.	User's Guide	EK-DZQ11-UG
3.	Maintenance Card	EK-DZQ11-MC
4.	Turnaround test connector	H329

The basic option (DZQ11-M) can be supplied with one of five cabinet kits for installation into different systems. These are:

1. CK-DZQ11-DA (21-inch cable), example of use – PDP-11/23S
2. CK-DZQ11-DB (12-inch cable), example of use – Micro/PDP-11
3. CK-DZQ11-DC (30-inch cable), example of use – PDP-11/23+
4. CK-DZQ11-DF (36-inch cable), example of use – PDP-11/83
5. CK-DZQ11-D3 unshielded option (BC11U-25 cable).

The first four cabinet kits are almost identical except for the length of the flat ribbon cables, and the addition of an adapter plate in the CK-DZQ11-DC. They are made up of the following:

1. BC05L-xx cable (see NOTE)
2. H325 line-loopback connector
3. The distribution panel – 70-19964-00
4. Mounting bolts and washers for the distribution panel.

A system integrated DZQ11 option is a DZQ11-DP.

NOTE

The distribution panels provide noise filtering and static discharge protection on the communications lines. The -DC version has an adapter plate which allows the panel to be mounted in the PDP-11/23+.

BC05L-xx cables are supplied in different lengths for each kit as previously specified.

The CK-DZQ11-D3 cabinet kit is a cable assembly made up of four cables, with D-type connectors at one end, and the other end connected to a socket which fits in the module connector. This kit does not provide noise filtering or static discharge protection on the communications lines.

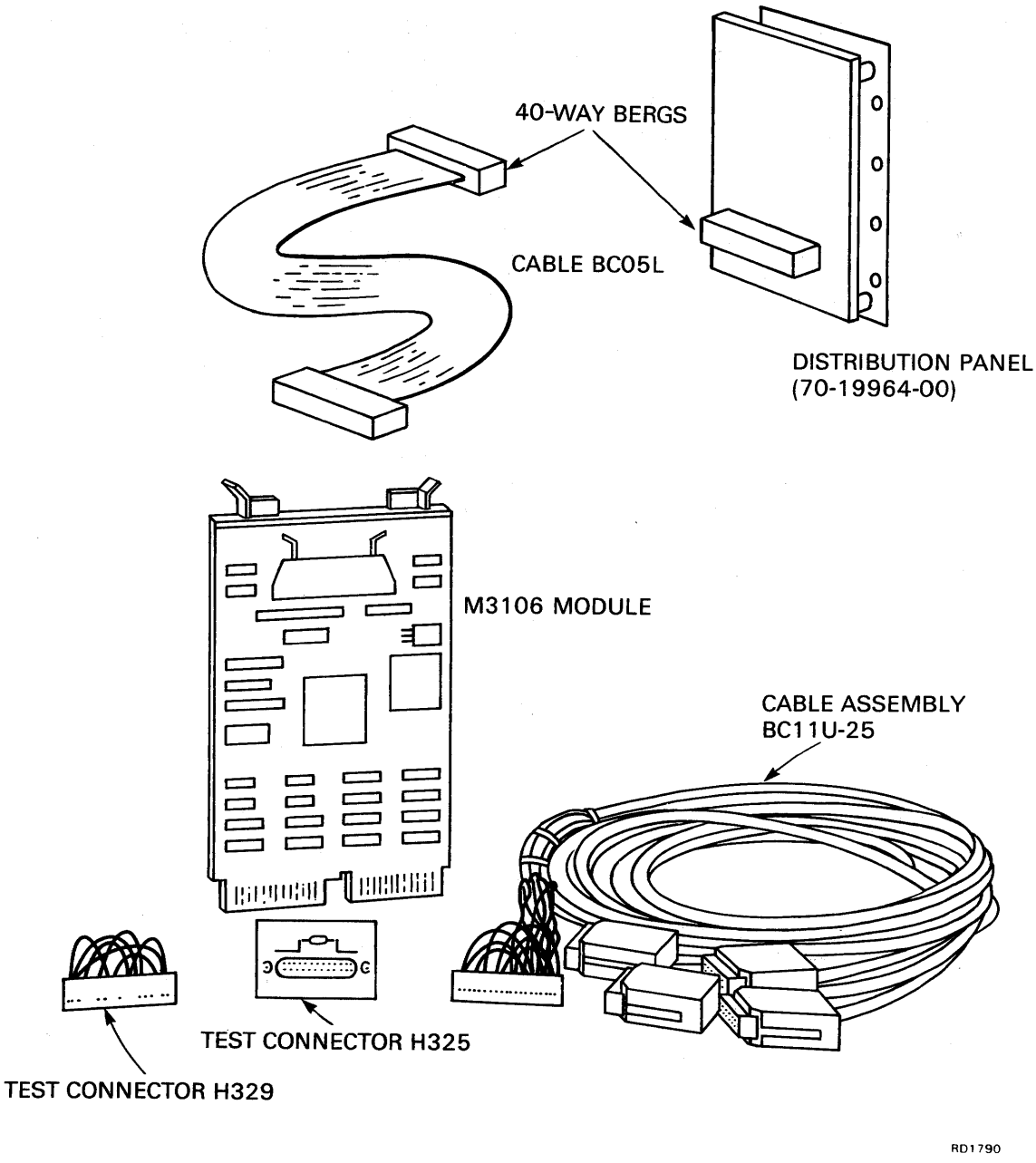


Figure 1-3 Elements of the DZQ11 Option

1.2.2 Interface Cables

The connections from the DZQ11 use 25-pin male subminiature D-type connectors as specified for RS-232-C.

Circuit AA (CCITT* 101)	Pin 1	Protective Ground
Circuit AB (CCITT 102)	Pin 7	Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
Circuit BB (CCITT 104)	Pin 3	Received Data
Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CE (CCITT 125)	Pin 22	Ring Indicator
Circuit CF (CCITT 109)	Pin 8	Carrier

NOTE

Signal ground and protective ground are connected together, through the chassis, by jumper W1 on the 70-19964-00 distribution panel.

1.2.3 Test Connectors

Figure 1-4 shows the two accessory test connectors, H329 and H325.

The H329 plugs into the module I/O connector and connects line 0 to line 1, and line 2 to line 3.

The H325 plugs into an EIA connector on the distribution panel, or BC11U-25 cable assembly, to loopback data and modem signals over a single line. The loopback connections are shown in Figure 1-5.

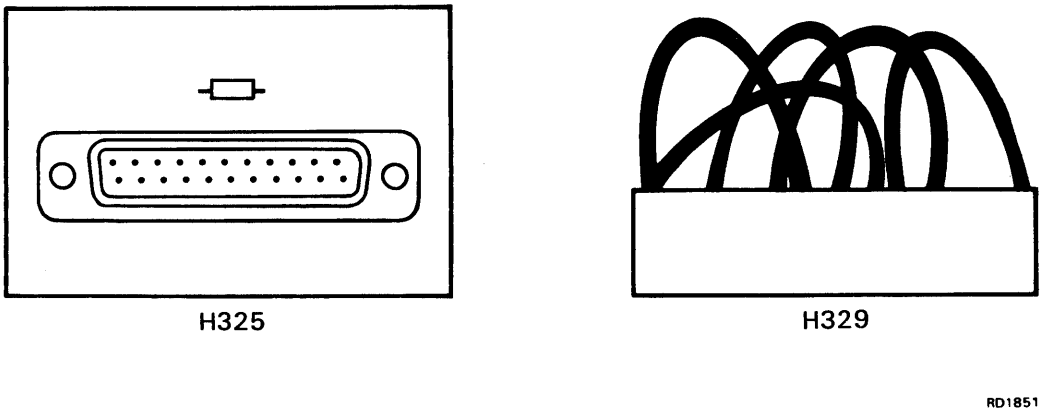


Figure 1-4 Test Connectors H325 and H329

* CCITT – The International Consultative Committee for Telegraphy and Telephony is an advisory committee created under the United Nations to recommend worldwide standards.

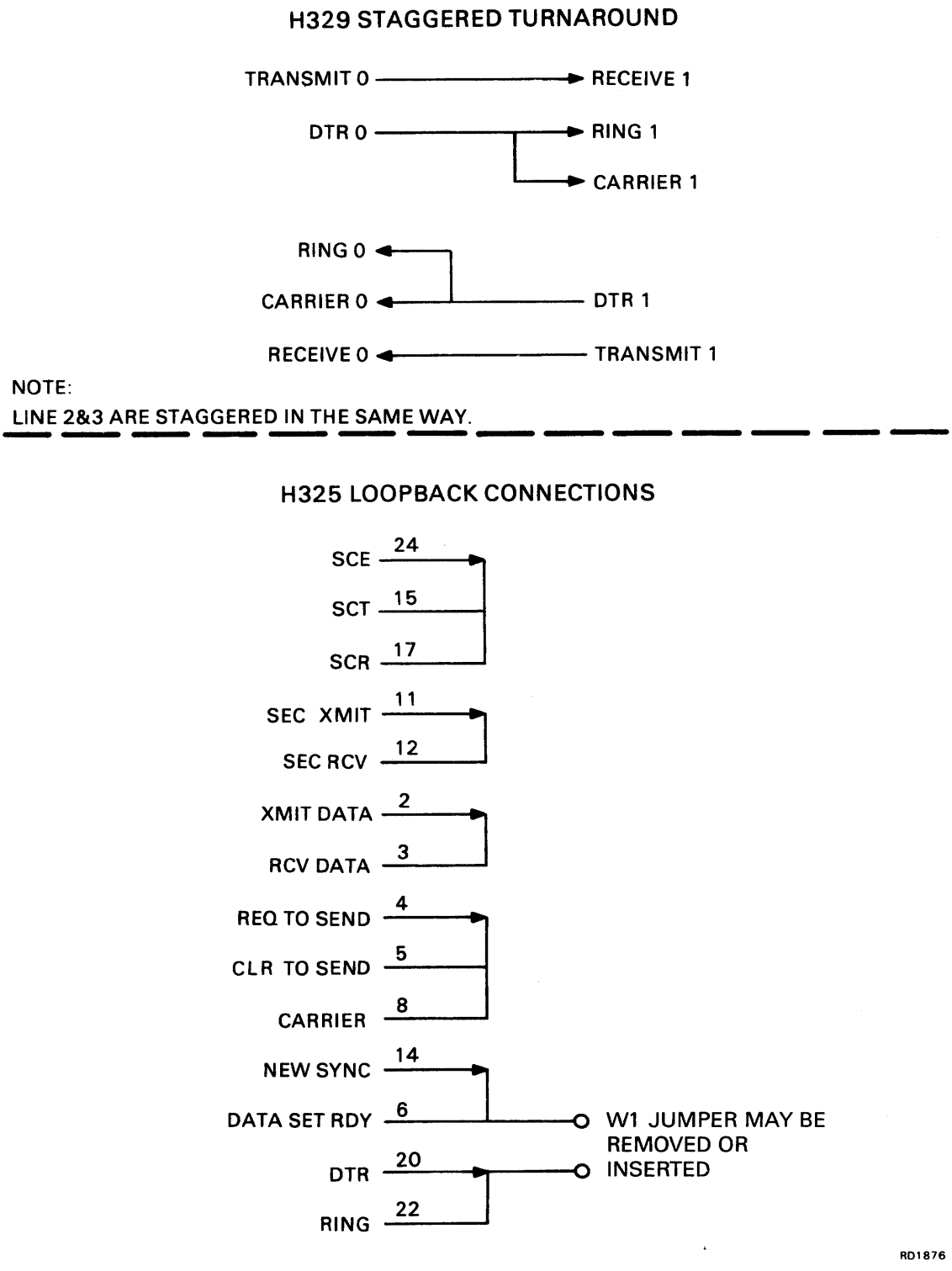


Figure 1-5 Loopback Connection

1.3 SPECIFICATIONS

Environmental, electrical, and performance specifications for the DZQ11 are listed in the following paragraphs.

1.3.1 Environmental

Storage temperature	0 degrees C to 66 degrees C (32 degrees F to 151 degrees F)
Operating temperature	5 degrees C to 60 degrees C (41 degrees F to 140 degrees F)
Relative humidity	10% to 95% non-condensing

1.3.2 Electrical

Power consumption	1.100 A at +5 V dc typical 0.236 A at +12 V dc typical
Q-bus loading	Q-bus ac loads – 1.5 ac loads Q-bus dc loads – 1.0 dc loads

1.3.3 Performance

The following paragraphs describe the DZQ11 performance capabilities and restrictions.

1.3.3.1 Interfaces – The DZQ11 interfaces with the host computer bus and also with the four data communication lines.

1. System Bus Interface

   The DZQ11 module interfaces directly to a Q22 or other Q-bus via connectors A and B. The module meets the DIGITAL Q-bus specification.

2. Serial Interfaces

   The DZQ11 serial interfaces comply with a subset of EIA/CCITT standards RS-232-C/V.24. The electrical characteristics are compatible with EIA/CCITT standards RS-232-C/V.28 and RS-423/V.10 (unbalanced interface).

1.3.3.2 Maximum Configurations – The DZQ11 multiplexer is assigned a device address in the floating address space. The floating address space starts at 760010_8 and extends to 763776_8. Maximum configuration of DZQ11s is not limited by floating address space, but is limited by the rules controlling a system configuration of average size.

As the DZQ11 needs one backplane AB slot-pair, it is physically possible to mount:

- Two M3106 modules in a PDP-11/23-S
- Three M3106 modules in a Micro/PDP-11
- Four to five M3106 modules in a PDP-11/23+

These numbers are the absolute maximum, because of the limited number of 70-19964-00 distribution panels that can be installed in the rear panel of the mounting box. These numbers may also be limited by the available capacity of the power supply, if other options are installed in the mounting box.

1.3.3.3 Throughput – Each DZQ11 is capable of a throughput of 10 970 characters per second (chars/s). This rate is computed as follows.

(Bits/s × number of lines × directions) divided by bits/char

(9 600 × 4 × 2)/7 equals 10 970 chars/s, at 5 bits/char with one start and one stop bit and no parity.

The full device throughput can only be maintained when a character service routine takes 100 microseconds or less.

The DZQ11 has a maximum non-standard data rate of 19 800 baud. At this rate the throughput is 22 625 characters per second.

1.3.3.4 Receivers – The receivers perform serial-to-parallel conversion of 5-, 6-, 7-, or 8-level code with one start bit and at least one stop bit. The character length, number of stop bits, parity generation, and operating speed are programmable parameters for each line. Both the receiver and the transmitter of a corresponding line share the same operating speed, and the receiver line can be enabled or disabled.

Each receiver is double buffered and has an acceptable input distortion of 43.75% on any bit. The sum of the character distortion must also not exceed 43.75%. An exception to this is the stop bit. The stop bit can tolerate an error of 50%, that is, the receiver will accept a stop bit as short as one half of a bit period. Break detection is provided on each receiver via a register bit. In addition, the configuration of switchpack E13-9 and E13-10 can cause the processor to boot or halt when a break is detected on line 3.

1.3.3.5 Transmitters – The transmitters provide parallel-to-serial conversion of 5-, 6-, 7- or 8-level code with or without parity. The parity sense, when selected, can be either odd or even. The stop code can be either 1 or 2 units except when 5-level code is selected. When 5-level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks can be transmitted on any line. The maximum start-stop distortion for the output of a transmitter is less than 2.5% for an 8-bit character.

1.3.3.6 Baud-Rate Generator – The baud-rate generators are completely programmable. Each line has an independent generator which can select 1 of 16 baud rates. Speed tolerance for all rates is better than 0.3%. The baud rates are shown in Section 1.3.3.7.

1.3.3.7 Performance Summary – The following list shows the programmable features offered for each line.

Character length	5-, 6-, 7-, or 8-level code
Number of stop bits	1 or 2 for 6-, 7-, or 8-level code. 1 or 1.5 for 5-level code
Parity	Odd, even, or none
Baud rates	50, 75, 110, 134.5, 150, 300, 600, 1 200, 1 800, 2 000, 2 400, 3 600, 4 800, 7 200, and 9 600 (and non-standard 19 800)
Breaks	Can be generated and detected on each line Line 3 has a hardware response to detected breaks which, when enabled, may generate a HALT or RESET. This facility can be selected by switches.

1.3.4 Interrupts

The following interrupts are available on the DZQ11.

1.3.4.1 Receiver-Done Interrupt – The receiver-done interrupt occurs every time a character appears at the output of the receiver buffer register and the silo alarm is disabled. The receiver-done interrupt can be enabled or disabled from the bus.

1.3.4.2 Silo-Alarm Interrupt – The silo-alarm interrupt occurs after 16 entries have been made into the receive buffer register by the scanner. This interrupt disables the receiver-done interrupt, and is armed again when the receive buffer register has been read.

1.3.4.3 Transmit Interrupt – The transmit interrupt occurs every time the scanner finds a buffer-empty condition, and the transmitter control register bit is set for that line. It can be enabled or disabled from the bus.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZQ11 asynchronous multiplexer. It contains information on the following:

- Device and vector address selection
- Recommended cables
- Testing after installation
- Floating address and vector assignment.

2.2 UNPACKING AND INSPECTION

The DZQ11 is packed following normal commercial packing practices. To unpack, first remove all packing material and check the equipment against the shipping list. (Table 2-1 contains a list of supplied items per configuration.) Report any damage or shortages to the shipper immediately and inform the local DIGITAL office. Examine all parts and carefully examine the module for damage, loose components, and breaks in the etched paths.

CAUTION

The M3106 is supplied in a protective sleeve. Do not remove the sleeve until you are about to install the module. Protect the module from static during installation.

WARNING

Procedures which call for the removal of the system covers should be performed by trained personnel only. Information on such procedures is included for user information only.

Table 2-1 Items Supplied per Configuration

DZQ11-M Base Option	
Description	**Quantity**
M3106 module	1
H329 test connector	1
DZQ11 User's Guide (EK-DZQ11-UG)	1

CK-DZQ11-DA/DB/DC/D3/DF Cabinet kits	Quantity				
Description	**DA**	**DB**	**DC**	**D3**	**DF**
70-19964-00 distribution panel	1	1	1	–	1
74-28684-01 adapter plate	–	–	1	–	–
BC05L-1K 21-inch cable	1	–	–	–	–
BC05L-01 12-inch cable	–	1	–	–	–
BC05L-2F 30-inch cable	–	–	1	–	–
BC11U-25 cable assembly	–	–	–	1	–
BC05L-03 36-inch cable	–	–	–	–	1
H325 test connector	1	1	1	1	1
90-06633-00 screws	4	4	8	–	4
90-06021-01 washers	4	4	8	–	4

2.3 INSTALLATION PROCEDURE

The following paragraphs describe the installation of the DZQ11 option in a Q-bus system.

2.3.1 Modem Control Jumpers

There are eight jumpers used for modem control (Figure 2-1). The jumpers labelled W1 to W4 connect the Data Terminal Ready (DTR) circuit to the Request To Send (RTS) circuit. This allows the DZQ11 to assert both DTR and RTS when using modems that need control of RTS. These jumpers must be installed for running the cable and external diagnostic programs. The four jumpers W5 to W8 connect the Forced Busy (FB) circuits to the RTS circuits. When these jumpers are installed, asserting an RTS circuit also places an ON or BUSY level on the corresponding FB circuit. Jumpers W5 to W8 are normally cut out unless they are needed by the modems used. Table 2-2 shows the jumper line assignments.

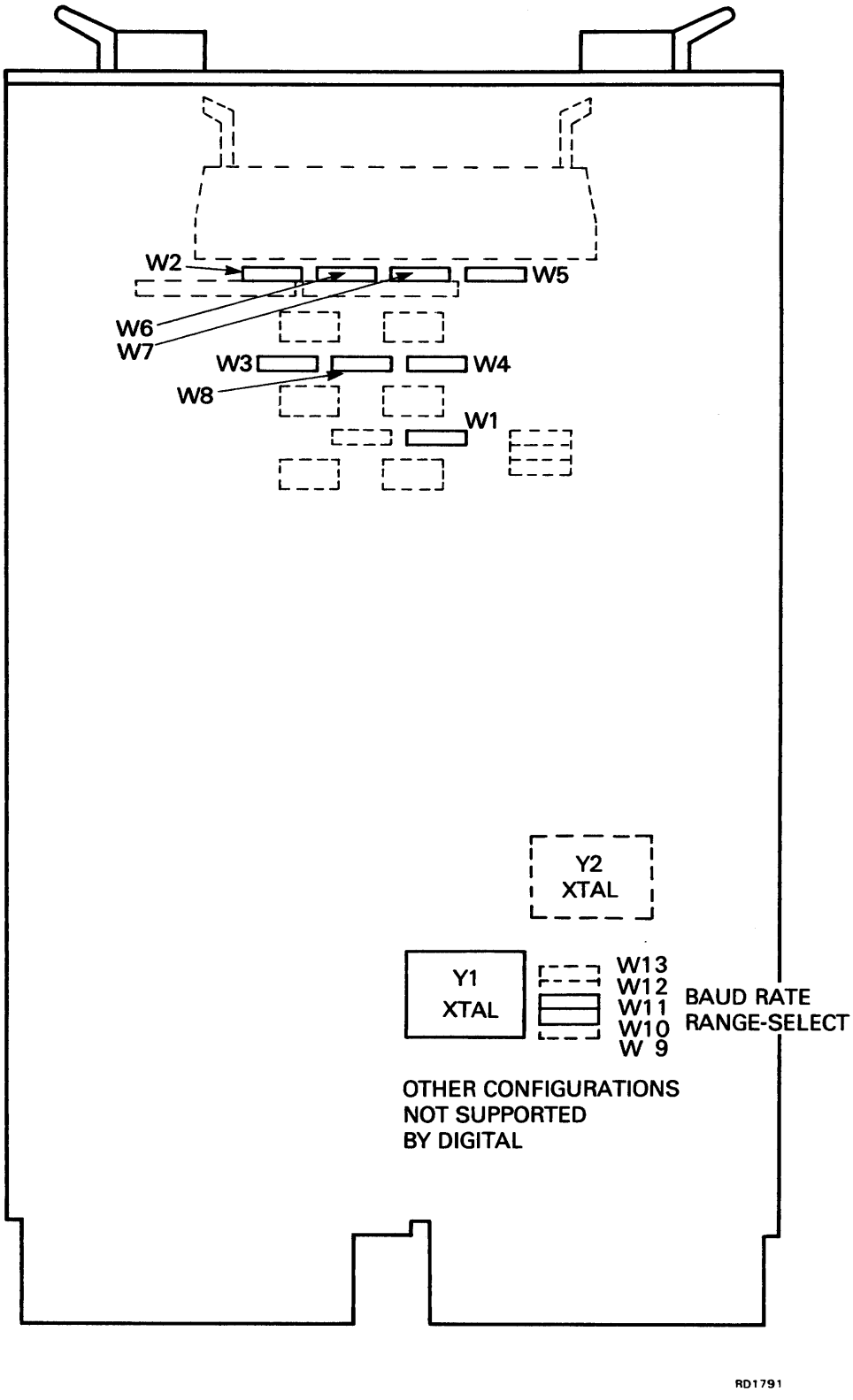


Figure 2-1 Jumper Location on M3106 Module

Table 2-2 Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

2.3.2 Module Installation

To install the M3106 module, perform the following.

NOTE

This checkout procedure should be performed by trained maintenance personnel only.

CAUTION

Switch off power before inserting or removing modules.

The M3106 is a fine-line-etch PCB. Handle it carefully to avoid damaging the etch.

Take anti-static measures to protect the module.

1. The Q-bus Interrupt Acknowledge and the DMA Grant signals are daisy-chained through the AB slots of the Q-bus backplane. If a DZQ11 is followed by a quad-size option in an AB/AB (Q/Q) backplane, it may cause an AB slot-pair to be left vacant. In order to maintain the continuity of the daisy-chained signals, a G7272 Grant Continuity card should be installed in the vacant A slot.

2. Refer to Section 2.4 for descriptions of the address assignments. Set the switches at E28 so that the module responds to its assigned address. When a switch is closed (ON), a binary 1 is encoded. When a switch is open (OFF), a binary 0 is encoded. The switch numbered 1 is connected to address bit 12, 2 is connected to address bit 11, and so on (Table 2-4).

3. The 10-position switch at E13 performs the vector selection. Switch position 7 is not used. Switch position 6 is connected to vector bit 3, 5 is connected to vector bit 4, and so on. When a switch is closed (ON), binary 1 is encoded. When a switch is open (OFF), a binary 0 is encoded (Table 2-5).

4. Position 8 of the vector selection switch is a test switch which can disconnect the DZQ11 oscillator from all circuitry. Make sure that this switch is in the ON position before installation.

5. Positions 9 and 10 of switch E13 control the DZQ11 response to a Break character received on Line 3. There are three valid options: HALT, BOOT, and no response. Table 2-3 lists the switch selections.

Table 2-3 Break Character Response Options

Switch 9	Switch 10	Effect of Break Character on Line 3	
OFF	OFF	No effect	(normal operation)
ON	OFF	Causes Processor to halt	(specific application)
OFF	ON	Causes Processor to boot	(specific application)
ON	ON	Illegal Condition	

6. Make sure that +5 volts is present between AA2 and ground and that +12 volts is present between AD2 and ground. Measure at the nearest accessible point, if the backplane cannot be accessed.

7. Remove power and insert the module in an AB slot of the backplane.

8. Apply power and make sure that the +5 volts and +12 volts is present with the module installed.

CAUTION

Insert and remove modules slowly and carefully to prevent damage to the module components on the card guides, and to avoid changing switch selections in error.

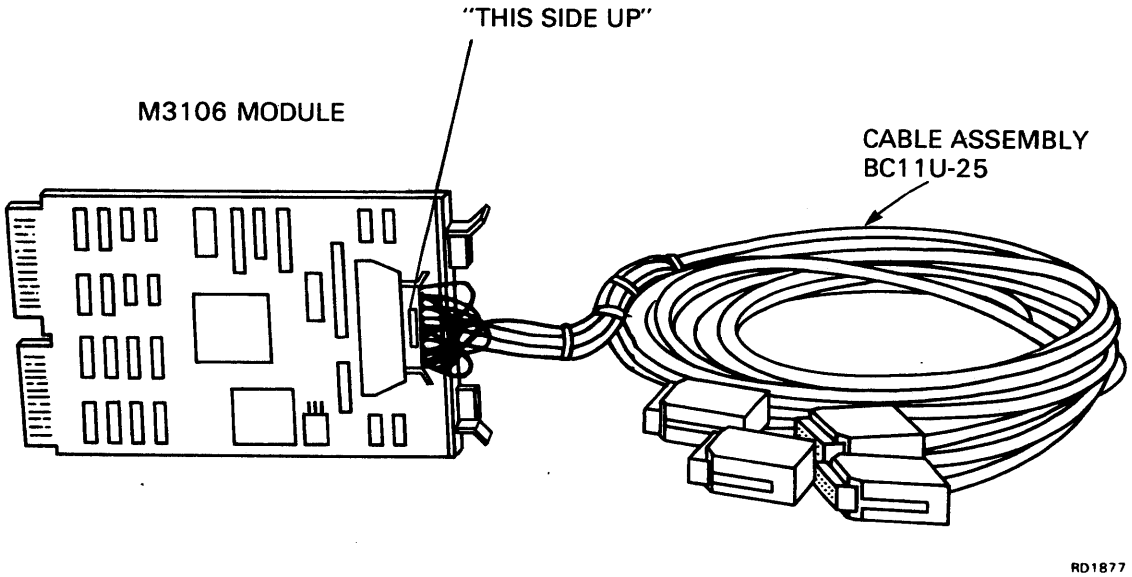
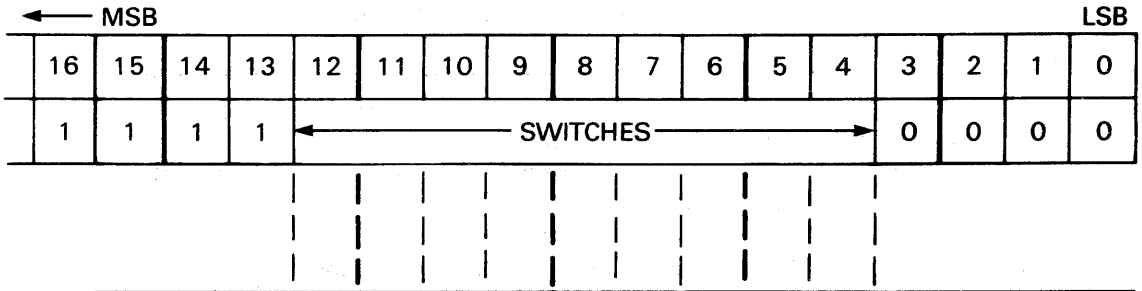


Figure 2-2 DZQ11 Installation (BC11U-25)

Table 2-4 Address Switch Selection



SWITCH NUMBER	E28 1	E28 2	E28 3	E28 4	E28 5	E28 6	E28 7	E28 8	E28 9	E28 10	DEVICE ADDRESS
											17760000
										ON	17760010
									ON		17760020
									ON	ON	17760030
								ON			17760040
								ON		ON	17760050
								ON	ON		17760060
								ON	ON	ON	17760070
							ON				17760100
						ON					17760200
						ON	ON				17760300
					ON						17760400
					ON		ON				17760500
					ON	ON					17760600
					ON	ON	ON				17760700
			ON	ON	ON	ON	ON	ON	ON		17763760
			ON	ON	ON	ON	ON	ON	ON	ON	17763770

ON = SWITCH CLOSED TO RESPOND TO A LOGICAL 1 ON THE BUS

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Table 2-5 Vector Switch Selection

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	← SWITCHES →						1/0	0	0

REFER TO SECTION 2.3.2 FOR SETTING OF E13 - 7 TO 10

SWITCH NUMBER	E13 1	E13 2	E13 3	E13 4	E13 5	E13 6	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700
	ON	ON	ON	ON	ON		760
	ON	ON	ON	ON	ON	ON	770

ON = SWITCH CLOSED TO PRODUCE A LOGICAL 1 ON THE BUS

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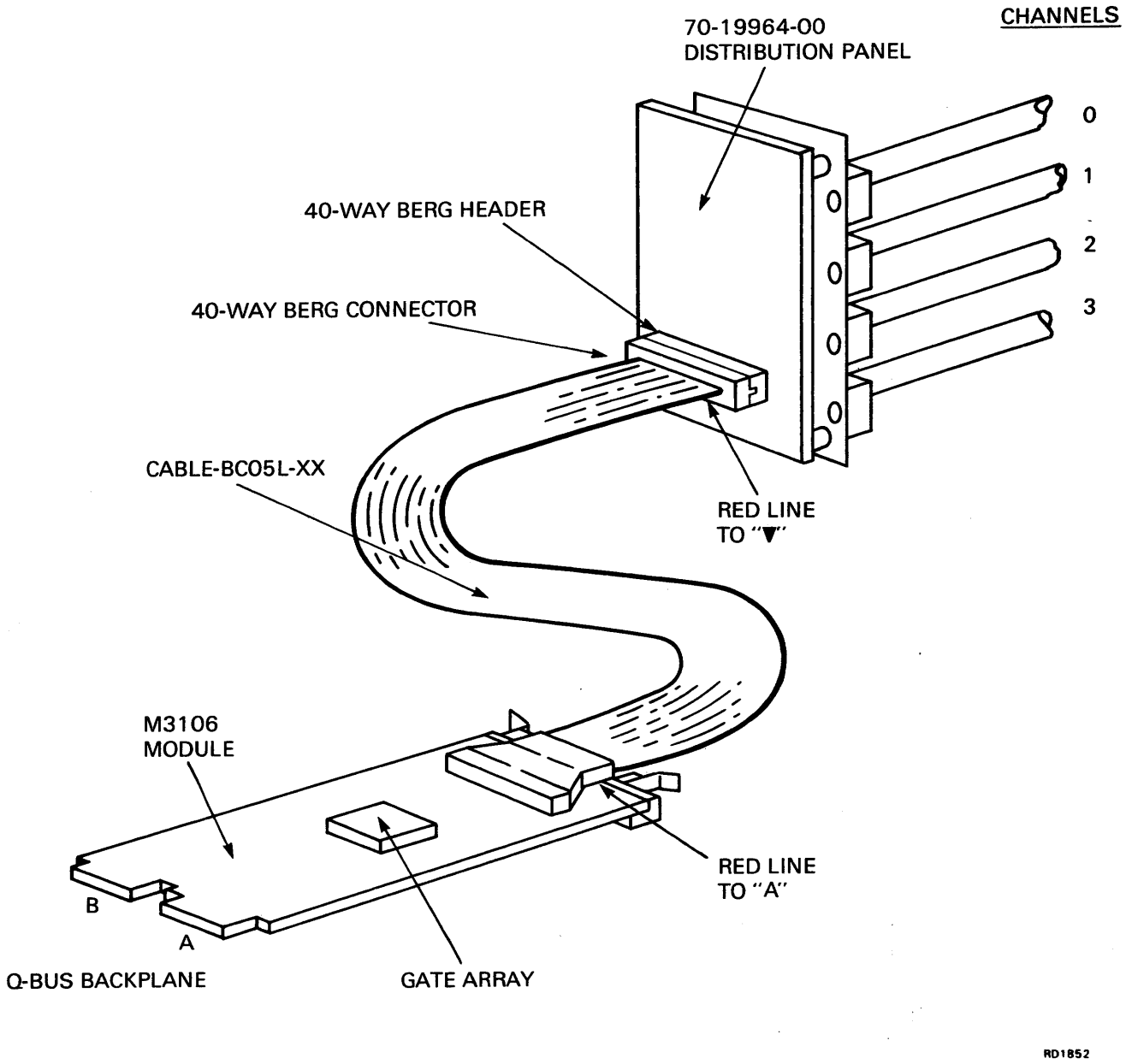

Figure 2-3 DZQ11 Installation (70-19964-00)

2.3.3 Testing DZQ11s in PDP-11 Systems

The following diagnostics are available to test DZQ11s installed in PDP-11 systems. DZITA and DVDZD are only used when a link between two processors is to be tested.

CVDZA	DZV11/DZQ11 Logic Test – Part 1
CVDZB	DZV11/DZQ11 Logic Test – Part 2
CVDZC	DZV11/DZQ11 Cable/Echo Test
CXDZB	DECX/11 Module
DZITA	Interprocessor Test Program (ITEP)
DVDZD	Overlay for ITEP

Test the option as follows.

1. Run diagnostics CVDZA and CVDZB in internal mode, to verify operation. Refer to the listing for more help. Run at least three passes without error.

2. Insert the H329 test connector in J1 with the letter side facing up. J1 is the cable connector at the top of the M3106 module.

   Run CVDZA and CVDZB in the staggered mode, to verify module operation. Refer to the diagnostic listing for the correct procedure. Run at least three passes without error.

3. If the unshielded cab-kit (D3) version is used, replace the H329 test connector with the Berg end of the BC11U cable assembly. Follow the 'This side up' instruction on the assembly. Refer to Figure 2-2 for assembly and interconnection instructions.

4. If the cab-kit versions CK-DZQ11-DA, -DB or -DF are used, feed the cable through the rear of the cabinet and connect the Berg plug to the distribution panel. Mount the distribution panel in the opening at the rear of the cabinet.

   The -DC version is provided with an adapter plate to fit the large opening in a PDP-11/23+. Mount the adapter plate on the distribution panel, with four of the eight screws provided. Mount the distribution panel as described above.

5. Connect the H325 test connector on the first line and run diagnostic CVDZC. Select the cable-test part of the diagnostic. Three passes are needed without error. Repeat this step for each line.

6. Run the DECX/11 system exerciser to verify the absence of Q-bus interference with other system devices.

7. The DZQ11 is now ready for connection to external equipment. If the connection is to a local terminal through either of the two options (BC11U-25 or 70-19964-00), a null modem cable assembly must be used. Use the BC22A, BC22D, or BC03P null modem cables for connection between the option and the terminal. The H312-A null modem unit may also be used in place of the null modem cables.

   Connections between the option and a modem should be made using a BC22E or BC05D cable.

   All of the cables referred to, with the exception of the BC11U-25, must be ordered separately as they are not components of a DZQ11 option.

   If a terminal is available, run the diagnostic CVDZC in echo-test mode to verify the cable connections and the terminal equipment.

2.3.4 Testing in MicroVAX Systems

The following diagnostic tests are available for testing DZQ11s in MicroVAX systems.

EHXDZ	DZV11/DZQ11 Test
EHKMV	Macroverify – MicroVAX System Test

Macroverify is a standalone diagnostic which contains a DZV11/DZQ11 test module.

Refer to the appropriate diagnostic listing, or to Chapters 11 and 14 of the MicroVAX Owner's Guide, for details of how to run EHXDZ and EHKMV.

Test the option as follows.

1. Boot from the MicroVAX system tests diskette (number 2 of 2). Attach and select the DZQ11 that is to be tested.

2. Run EHXDZ for three error-free passes of the internal (default) test.

3. Install the H329 staggered loopback connector on the M3106 module. Run EHXDZ for three error-free passes of the staggered test.

4. Remove the H329. Install the BC05L cable and the distribution panel.

5. If the operation of a terminal link is to be tested, connect the terminal line to the distribution panel. Run the EHXDZ echo test on that line until the link is proven. Depending on the terminal, a null-modem may be needed for this test. Exit echo test by ^ Z (CTRL/Z).

6. Remove all external cables and connectors from the distribution panel. Boot the CPU tests diskette (number 1 of 2). The Macroverify diagnostic will run automatically when the boot process is complete. When the test completes, the status of all options will be displayed.

7. If no device has a TEST FAILED status, the DZQ11 is now ready for connection to external equipment. If the connection is to a local terminal, a null modem cable assembly must be used. Use the BC22A, BC22D, or BC03P null modem cables for connection between the option and the terminal. The H312-A null modem unit may also be used in place of the null modem cables.

   Connections between the option and a modem should be made using a BC22E or BC05D cable.

   All of the referenced cables must be ordered separately as they are not components of a DZQ11 option.

2.4 DEVICE ADDRESS ASSIGNMENTS

On UNIBUS and Q-bus systems, a range of addresses (xxx60010_8 to xxx63776_8) in the top 4K words is assigned as floating address space (xxx means all top address bits = 1).

The first part of the list of options (sufficient to include the DZQ11) which can be assigned floating device addresses is given in Table 2-6. 'Rank' gives the sequence of address assignment for both Q-bus and UNIBUS options.

If addresses are assigned according to defined rules, configuration programs can check which options are installed in a system. Having a combined list allows us to use one set of configuration rules and one configuration program for both Q-bus and UNIBUS systems.

Table 2-6 Floating Address Assignments

Rank	Device	Size (decimal)	Modulus (octal)
1	DJ11	4 words	10
2	DH11	8 words	20
3	DQ11	4 words	10
4	DU11, DUV11*	4 words	10
5	DUP11	4 words	10
6	LK11A	4 words	10
7	DMC11/DMR11	4 words	10
8	DZ11, DZS11, DZQ11*/DZV11* DZ32	4 words	10

* Q-bus device

For example, the address assignment sequences could be:

UNIBUS	Q-bus
DJ11	No Q-bus equivalent of DJ11
DH11	No Q-bus equivalent of DH11
DQ11	No Q-bus equivalent of DQ11
DU11	DUV11
DUP11	No Q-bus equivalent of DUP11
LK11A	No Q-bus equivalent of LK11A
DMC11	No Q-bus equivalent of DMC11
DZ11	DZQ11 and so on.

Devices of the same type are given sequential addresses, therefore all DUV11s in a system will have lower addresses than DZQ11s or DZV11s.

For the purpose of address assignment, DZQ11s and DZV11s are considered as devices of the same type.

The column *Size(decimal)* in Table 2-6, shows how many words of address space are needed for each device. The column *Modulus(octal)* is the modulus used for starting addresses. For example, devices with an octal modulus of 10 must start at an address which is a multiple of 10_8. The same rule is used to select a gap address (see assignment rules) after an option, or for a nonexistent device.

The assignment rules are as follows.

1. Addresses, starting at xxx60010, are assigned according to the sequence of Table 2-6
2. Option and gap addresses are assigned according to the octal modulus as follows.
   a. Devices with an octal modulus of 10 are assigned an address on a 10_8 boundary (the three lowest-order address bits = 0)
   b. Devices with an octal modulus of 20 are assigned an address on a 20_8 boundary (the four lowest-order address bits = 0)
3. Address space equal to the device's modulus must be allowed for each device which is connected to the bus
4. A one-word gap, assigned according to rule 2, must be allowed after the last device of each type. This gap could be bigger when rule 2 is applied to the following rank
5. A one-word gap, assigned according to rule 2, must be allowed for each unused rank on the list if a device with a higher address is used. This gap could be bigger when rule 2 is applied to the following rank

Two examples of address assignment follow. Table 2-7 shows addresses for a system with one DUV11 and one DZQ11. Table 2-8 shows addresses for a system with no DUV11 and two DZQ11s. Note that where there is no Q-bus device at a specific rank, the UNIBUS device parameters must be used to assign the gap. Vector assignments (see Section 2.5) are also shown in these tables.

Table 2-7 is supported by a description of how to apply the assignment rules.

Table 2-7 One DUV11 and One DZQ11

Rank	Address	Designation	Vector
1	xxx60010	DJ11 gap	
2	xxx60020	DH11 gap	
3	xxx60030	DQ11 gap	
4	xxx60040	DUV11	300
	xxx60050	DUV11 gap	
5	xxx60060	DUP11 gap	
6	xxx60070	LK11A gap	
7	xxx60100	DMC11 gap	
8	xxx60110	DZQ11	310
	xxx60120	DZQ11 gap	

The first floating address is 760010. As a DJ11 has a modulus of 10_8, its gap can be assigned to 760010. The next available location becomes 760012.

As a DH11 has a modulus of 20_8, it cannot be assigned to 760012. The next modulo 20 boundary is 760020, so the DH11 gap is assigned to this address. The next available location is therefore 760022.

A DQ11 has a modulus of 10_8. It cannot be assigned to 760022. Its gap is therefore assigned to 760030. The next available location is 760032.

The DUV11 has a modulus of 10_8. It cannot be assigned to 760032. It is therefore assigned to 760040. As the size of DUV11 is four words, the next available address is 760050.

There is no second DUV11, so a gap must be left to indicate that there are no more DUV11s. As 760050 is on a 10_8 boundary. The DUV11 gap can be assigned to this. The next available address is 760052.

And so on.

Table 2-8 Two DZQ11s

Rank	Address	Designation	Vector
1	xxx60010	DJ11 gap	
2	xxx60020	DH11 gap	
3	xxx60030	DQ11 gap	
4	xxx60040	DUV11 gap	
5	xxx60050	DUP11 gap	
6	xxx60060	LK11A gap	
7	xxx60070	DMC11 gap	
8	xxx60100	1st DZQ11	300
8	xxx60110	2nd DZQ11	310
	xxx60120	DZQ11 gap	

2.5 INTERRUPT VECTOR ADDRESS ASSIGNMENTS

Addresses between 300_8 and 774_8 are designated as the floating vector space. These addresses are assigned in sequence as in Table 2-9.

Each device needs two 16-bit locations for each vector. For example, a device with one receive and one transmit vector needs four words of vector space.

The vector assignment rules are as follows.

1. Each device occupies vector address space equal to 'Size' words. For example, the DLV11-J occupies 16 words of vector space. If its vector was 300_8 the next available vector would be 340_8.
2. There are no gaps, except those needed to align an octal modulus.

The vector addresses shown in Tables 2-7 and 2-8 are assigned according to these rules.

Table 2-9 First Part of Q-bus Vector Address Assignments List

Device	Size (decimal)	Modulus (octal)
DLV11-J	16	10
DLV11,DLV11-F	4	10
DRV11-B	4	10
DRV11	4	10
DLV11-E	4	10
VSV11	8	10
KWV11	4	10
DUV11	4	10
DZV11/DZQ11	4	10

CHAPTER 3
DEVICE REGISTERS

3.1 SCOPE
This chapter describes the format and bit function of each register in the DZQ11.

3.2 DEVICE REGISTERS
The DZQ11 contains six addressable registers. Figure 3-1 shows the bit assignments of these registers and Table 3-1 lists the registers and related DZQ11 addresses.

Table 3-1 DZQ11 Register Address Assignments

Register Name	Mnemonic	Address	Program Capability
Control and Status Reg.	CSR	76XXX0	Read/Write
Receiver Buffer	RBUF	76XXX2	Read Only
Line Parameter Register	LPR	76XXX2	Write Only
Transmitter Control Reg.	TCR	76XXX4	Read/Write
Modem Status Register	MSR	76XXX6	Read Only
Transmit Data Register	TDR	76XXX6	Write Only

XXX = Selected in agreement with the floating device address system.

3.2.1 Control and Status Register
The control and status register (CSR) can be addressed with a byte or word address. All bits in the CSR are cleared by an occurrence of BINIT, or by setting device Master Clear (CSR<04>). The format is shown in Figure 3-1 and the bit assignments are listed in Table 3-2.

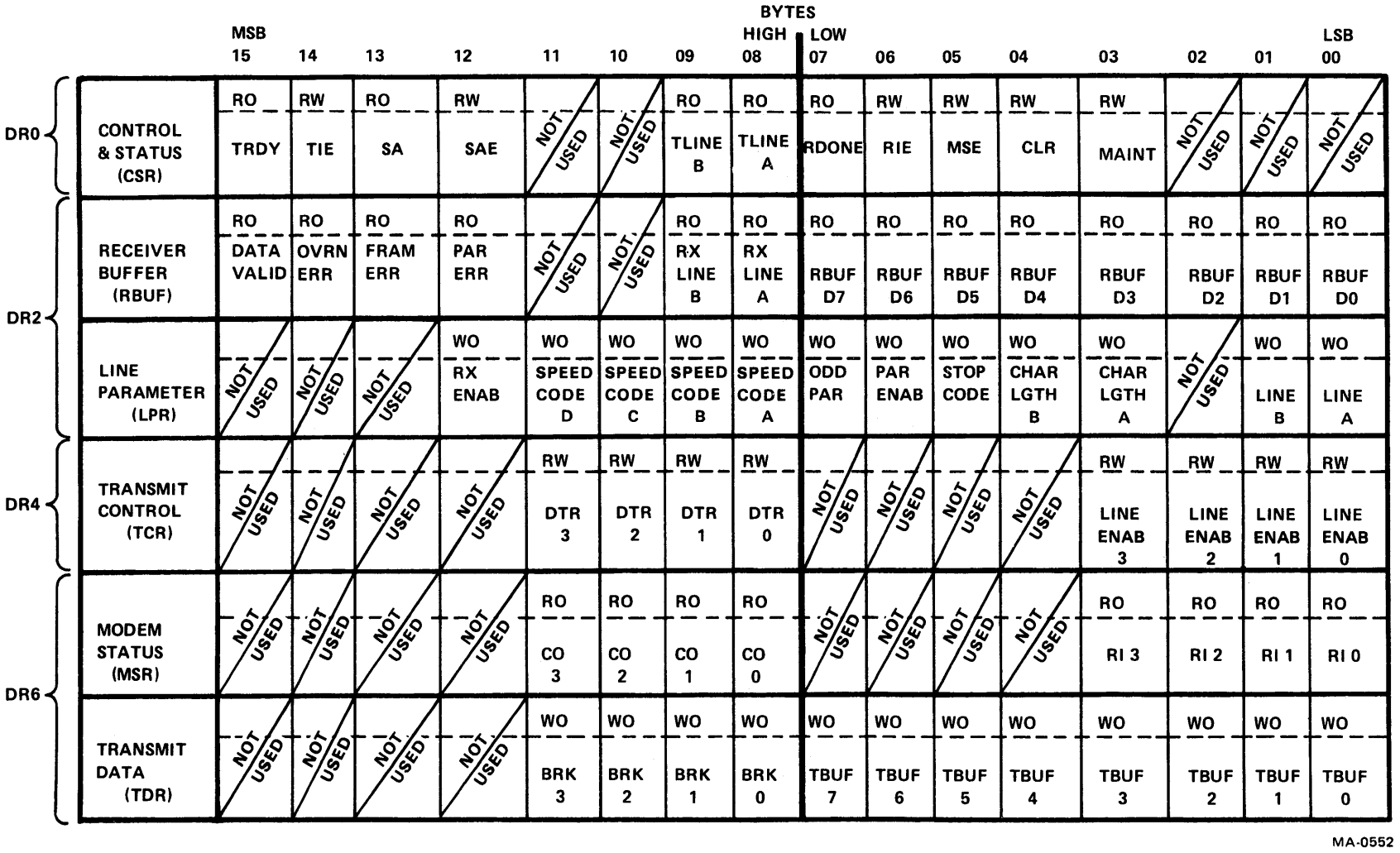

Figure 3-1 Register Bit Assignment

Table 3-2 CSR Bit Assignments

Bit	Title	Function
<02:00>	Not used	
<03>	Maintenance (MAINT)	This is a READ/WRITE bit. When set it loops the serial output connections of the transmitter to the corresponding serial input connections of the receiver at the UART. (Used for loopback test only.)
<04>	Master Clear (CLR)	When written to a 1, this bit generates 'initialize' within the DZQ11. A read-back of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTs are cleared with the following exceptions: 1. Only bit 15 of the receiver buffer register (Data Valid) is cleared; the other bits (<14:00>) are not. 2. The high byte of the transmitter control register is not cleared by Master Clear. 3. The modem status register is not cleared by Master Clear.
<05>	Master Scan Enable (MSE)	This read/write bit must be set to permit the receiver and transmitter control sections to start scanning. When cleared, Transmitter Ready (CSR<15>) is inhibited from setting, and the received character buffers (silos) are cleared.
<06>	Receiver Interrupt Enable (RIE)	This bit permits the generation of an interrupt, when CSR<07> or CSR<13> is set. This bit is read/write.
<07>	Receiver Done (RDONE)	This is a read-only bit that is set when a character appears at the output of the first-in/first-out (FIFO) buffer. For the DZQ11 to run in the interrupt-per-character mode, CSR<06> must be set and CSR<12> must be cleared. With CSR<06> and CSR<12> cleared, character-flag mode is indicated. Receiver Done clears when the receiver buffer register (RBUF) is read or when Master Scan Enable (CSR<05>) is cleared. If the FIFO buffer contains an additional character, the Receiver Done flag stays clear for up to 1 microsecond, while that character bubbles through to the bottom of the FIFO.
<09:08>	Transmitter Line Number (TLINE B and TLINE A)	These read-only bits indicate the line number whose transmit buffer needs servicing. These bits are valid only when Transmitter Ready (CSR<15>) is set, and are cleared when Master Scan Enable is cleared. Bit <08> is the least-significant bit.
<11:10>	Not used	

Table 3-2 CSR Bit Assignments (Cont)

Bit	Title	Function
<12>	Silo Alarm Enable (SAE)	This is a read/write bit. When set, it enables the silo-alarm and prevents RDONE (bit <07>) from causing interrupts. If the receiver interrupt enable bit (bit <06>) is set, SAE enables the silo-alarm (bit <13>) to generate an interrupt after 16 silo entries. If silo-alarm is not set, then SAE may be used as a flag to indicate that 16 or more characters are in the silo.
<13>	Silo Alarm (SA)	This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo Alarm is held cleared when Silo Alarm Enable (CSR<12>) is cleared. This bit is cleared by a read to the receiver buffer register and does not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR<06>) is set, the occurrence of Silo Alarm generates a receiver interrupt request. Flag mode operation of the Silo Alarm bit is permitted with CSR<06> cleared.
<14>	Transmitter Interrupt Enable (TIE)	This is a read/write bit which must be set for Transmitter Ready to generate an interrupt.
<15>	Transmitter Ready (TRDY)	This read-only bit is set by the hardware when the transmitter scanner stops on a line whose transmit buffer may be loaded with another character and whose related TCR bit is set. The transmitter line number, specified in CSR<09:08>, is only valid when Transmitter Ready is set. Transmitter Ready is cleared by any of the following conditions: 1. When Master Scan Enable is cleared. 2. When the related TCR bit is cleared for the line number pointed to in CSR<09:08> If additional transmit lines need service, Transmitter Ready appears again within 1.4 microseconds of the completion of the 'transmit data register load' instruction. When Transmitter Ready occurs with Transmitter Interrupt Enable set, a transmitter interrupt request is generated.

3.2.2 Receiver Buffer

The receiver buffer (RBUF) is a 16-bit read-only register that contains the received character at the output of the FIFO buffer. A read of the register causes the character entry to be removed from the buffer, and all other entries to shift down to the lowest location that is not occupied. Only the Data Valid bit (RBUF<15>) is cleared by BINIT or by setting device Master Clear (CSR<04>). Bits <14:00> are not affected. The bit assignments for the RBUF register are listed in Table 3-3.

Table 3-3 RBUF Bit Assignments

Bit	Title	Function
<07:00>	Received Character (RBUF D<7:0>)	These bits contain the received character, right justified. the least-significant bit is bit <00>. For short characters, bits that are not used are logic low. The parity bit is not shown.
<09:08>	Received Line Number (RX LINE B and RX LINE A)	These bits contain the line number on which the Received Character was received. Bit <08> is the least significant.
<11:10>	Not used	
<12>	Parity Error (PAR ERR)	This bit is set if the sense of the parity of the received character does not agree with the parity defined for that line.
<13>	Framing Error (FRAM ERR)	This bit is set if the received character did not have a stop bit present at the correct time. This bit is usually interpreted as indicating that a break has been received.
<14>	Overrun Error (OVRN ERR)	This bit becomes set when a received character is overwritten in the UART buffer (by a following character), before it has been transferred by the scanner to the FIFO.
<15>	Data Valid (DATA VALID)	This bit, when set, indicates that the data in bits <14:00> is valid. This bit permits the use of a character-handling program which again and again takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit <15> until the program gets a word for which bit <15> is zero.

3.2.3 Line Parameter Register

The line parameter register (LPR) controls the operating parameters related to each line in the DZQ11. The LPR must be addressed with a word address and is a write-only register. The line parameters for all lines must be loaded again following an occurrence of either BINIT or device Master Clear. Table 3-4 lists bit assignments.

Table 3-4 LPR Bit Assignments

Bit	Title	Function
<01:00>	Parameter Line Number (LINE B and LINE A)	These bits specify the line number for which the parameter information (bits <12:3>) is to apply. Bit <00> is the least-significant bit.
<02>	Not used	Must always be written as a zero when specifying the parameter line number. Writing this bit as a one extends the parameter line number field into nonexistent lines. Parameters for lines 00 to 03 are not affected.

Table 3-4 LPR Bit Assignments (Cont)

Bit	Title	Function
<04:03>	Character Length (CHAR LGTH B and CHAR LGTH A)	These bits are set to receive and transmit characters of the length (except parity) shown below.

Bit 04	Bit 03	
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

<05>	Stop Code (STOP CODE)	This bit sets the stop code length; 0 = 1 unit stop, 1 = 2 unit stop (or 1.5 unit stop if a 5-level code is used).
<06>	Parity Enable (PAR ENAB)	If this bit is set, characters transmitted on the line have an appropriate parity bit added, and characters received on the line have their parity checked.
<07>	Odd Parity (ODD PAR)	If this bit is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit <06> is set, characters of even parity are generated on the line, and incoming characters are expected to have even parity. If bit <06> is not set, then the setting of this bit will not have any effect.
<11:08>	Speed code (SPEED CODE D to SPEED CODE A)	The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1 200
1	0	0	0	1 800
1	0	0	0	2 000
1	0	1	0	2 400
1	0	1	1	3 600
1	1	0	0	4 800
1	1	0	1	7 200
1	1	1	0	9 600
1	1	1	1	19 800 *

* Not supported by standard software.

Table 3-4 LPR Bit Assignments (Cont)

Bit	Title	Function
<12>	Receiver Enabled (RX ENAB)	This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit is cleared following a BINIT or device Master Clear.
<15:13>	Not used	

NOTE

The M3106 module can be modified by jumpers W9 to W13, so that code 1111 selects baud rates other than 19 800. This modification is not supported by DIGITAL.

3.2.4 Transmitter Control Register

The transmitter control register (TCR) is a byte- and word-addressable register. The low byte of the TCR contains the transmitter control bits, and must be set to start transmission on a line. Each TCR bit position is related to a line number. For example, TCR<00> is related to line 00, bit <01> to line 01, and so on. Setting a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a 'transmit buffer empty' condition. An interrupt is then generated if Transmitter Interrupt Enable is set. The scanner clock restarts when either the transmit data register (TDR) is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running, (that is, Transmitter Ready is set or Master Scan Enable is cleared).

The line enable bits are represented in TCR<03:00>. These bits are read/write and are cleared by BINIT or device Master Clear. Bits <07:04> are not used, and are read as zero.

The high byte of the TCR register contains the modem control signal that can be written, data terminal ready (DTR). The bits are defined as follows:

Bit	Name
<08>	DTR Line 00
<09>	DTR Line 01
<10>	DTR Line 02
<11>	DTR Line 03
<15:12>	Not used; read as zero

Assertion of a DTR bit creates an ON condition on the appropriate modem circuit for that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the RTS circuits to be asserted using DTR assertions.

3.2.5 Modem Status Register

The modem status register (MSR) is a 16-bit read-only register. A read to this register gives the status of the modem control signals that can be read, Ring and Carrier. The ON condition of a modem control signal is interpreted as a logical one. Bits <07:04> and <15:12> are not used and are read as a zero. The other bits are defined as follows:

Bit	Name	Bit	Name
<00>	Ring Line 00	<08>	Carrier Line 00
<01>	Ring Line 01	<09>	Carrier Line 01
<02>	Ring Line 02	<10>	Carrier Line 02
<03>	Ring Line 03	<11>	Carrier Line 03
<07:04>	Not used; read as zero	<15:12>	Not used; read as zero.

3.2.6 Transmit Data Register

The transmit data register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR<00> is the least-significant bit. Loading of a character should occur only when Transmitter Ready (CSR<15>) is set. The character that is loaded into this register is routed to the line defined in CSR<09:08>. The high byte of the TDR is defined as the break control register.

There is a corresponding break bit for each of the four multiplexer lines. TDR<08> represents the break bit for line 00, TDR<09> for line 01, and so on. TDR<15:12> are not used. Setting a break bit forces the output of that line to space. This register is cleared by BINIT or device Master Clear. The break control register can be used regardless of the state of the Device Maintenance bit (CSR<03>).

CHAPTER 4
PROGRAMMING

4.1 SCOPE

This chapter contains information for programming the DZQ11 in the most efficient way. To do so, the programming controls must be completely understood. The following paragraphs discuss the DZQ11 from the programming point of view and describe recommended programming methods.

4.2 PROGRAMMING FEATURES

The DZQ11 has some programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to get the wanted operating parameters.

4.2.1 Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the way that the DZQ11 receiver interrupts the processor.

If RIE and SAE are both clear, the DZQ11 never interrupts the processor. In this event, the program must regularly check that the data is available in the silo, and empty the silo when data is present. If the program operates from a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety element to cover processor-response delays and time to empty the silo. The Receiver Done (RDONE) bit in the CSR is set when a character is available in the silo. The program can regularly check this bit with a test byte or bit test instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZQ11 interrupts the processor and forces it to the DZQ11 receiver vector address, when RDONE is set. This indicates the presence of a character at the bottom of the silo. The interrupt service routine can get the character by performing a move instruction from the RBUF. If the program then dismisses the interrupt, the DZQ11 interrupts when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Another way is for the interrupt service routine to respond to the interrupt by emptying the silo before it dismisses the interrupt.

If RIE and SAE are both set, the DZQ11 interrupts the processor to the DZQ11 receiver vector when the Silo Alarm (SA) bit in the CSR is set. The SA bit is set when 16 characters have been placed in the silo after the last time the program has accessed the RBUF. Accessing the RBUF clears the SA bit and the related counter. The program should follow the procedure described in Section 4.2.2 to empty the silo completely in response to a Silo Alarm interrupt. This makes sure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each Silo Alarm interrupt, characters coming in while interrupts are being processed build up without being counted by the Silo Alarm circuit. The silo may in the end overflow without the alarm being issued.

If the Silo Alarm interrupt is used, the program will not be interrupted when fewer than 16 characters are received. In order to respond to short messages during periods of medium activity, the program should regularly empty the silo. The scanning period depends on the wanted response time to received characters. While the program is emptying the silo, it should make sure that DZQ11 receiver interrupts are inhibited. This should be done by raising the processor priority. The Silo Alarm interrupt feature can greatly decrease the processor overhead that would be needed by the DZQ11 receiver. This is done by removing the need to enter and exit an interrupt service routine each time a character is received.

The Transmitter Interrupt Enable (TIE) bit controls transmitter interrupts to the processor. If enabled, the DZQ11 interrupts the processor at the DZQ11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set. This indicates that the DZQ11 is ready to accept a character to be transmitted.

Each DZQ11 needs two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests are generated from each section, the receiver section would have priority in placing its vector on the Q-bus. A receiver interrupt to address XX0 is generated from having either a Receiver Done (CSR<07>) or Silo Alarm (CSR<13>) occurrence. A transmitter interrupt to address XX4 is generated by Transmitter Ready (CSR<15>). An additional prerequisite for generating interrupts is that the individual interrupt enable bits are set. The recommended method for clearing interrupt enable bits is first to raise the processor status word to level 4; next, to clear these interrupt enable bits; and then lower the processor status word to zero. Using this method prevents false interrupts from being generated.

4.2.2 Emptying the Silo

The program can empty the silo by performing consecutive move instructions from the RBUF to temporary storage. Each move instruction copies the bottom character in the silo so that it is not lost, and clears out the bottom of the silo, allowing the next character to move down for access by a following move instruction. The program can determine when it has emptied the silo by testing the Data Valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed by branching on the condition code following each move instruction. The test or bit test instruction must not access the RBUF because these instructions cause the next entry in the silo to move down without saving the current bottom character. Also, following a move from the RBUF, the next character in the silo is not available for at least one microsecond. Therefore, on fast CPUs, the program must use enough instructions or no-operation instructions to make sure that consecutive moves from the RBUF are separated by not less than one microsecond. This prevents a false indication of an empty silo.

4.2.3 Transmitting a Character

The program controls the DZQ11 transmitter through four registers on the Q-bus: the control and status register (CSR), the line parameter register (LPR), the transmit control register (TCR), and the transmit data register (TDR).

Following DZQ11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the TIE bit in the CSR if it wants the DZQ11 transmitter to interrupt the processor.

The TCR is used to enable and disable transmission on each line. One bit in this register is related to each line. The program can set and clear bits by using move, move byte, bit set, bit set byte, bit clear, and bit clear byte instructions. (If word instructions are used, the Line Enable bits and the DTR bits are accessed together.)

The DZQ11 transmitter is controlled by a scanner which is continuously looking for an enabled line (Line Enable bit set) which has an empty transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 2-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit allows the scanner to continue its search for lines needing service.

To start transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a move byte instruction. If the interrupts are to be used, a useful way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This occurs if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY, to make sure that it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner in the end finds the line being started. If more than one line needs service, the scanner requests service in priority order as determined by line number. Line 3 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY. Because the transmitters are double buffered, a high-priority line may request two consecutive loads.

To terminate transmission on a line, the program loads the last character normally, and waits for the scanner to request an additional character for the line. The program clears the Line Enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data connection for any line is the one state. The Break (BRK) bits are used to apply a continuous zero signal to the line. One bit in the TDR is related to each line. The line stays in this condition as long as the bit stays set. The program should use a move byte instruction to access the BRK bits.

If the program continues to load characters for a line after setting the BRK bit, transmitter operation appears normal to the program regardless of the fact that no characters can be transmitted while the line is in the continuous zero-sending state. The program may use this facility for sending correctly timed zero signals by setting the BRK bit and using transmit ready interrupts as a timer. The program must also make sure that the line returns to the one state at the end of the zero-sending period before transmitting any additional data characters.

The following procedure does this. When the scanner requests service the first time after the program has loaded the last data character, because the lines are double buffered, the last data character has only started transmission. The program should therefore load an all zero character, and wait for the next service request while the last character is transmitted. When the scanner requests service the second time, the program should set the BRK bit for the line, and the zero character is overwritten. At the end of the zero-sending period, the program should load an all zero character to be transmitted. When the scanner requests service, indicating this character has started transmission, the program should clear the BRK bit and load the next data character.

4.2.4 Data Set Control

The program may sense the state of the Carrier and Ring Indicator signals for each modem and may control the state of the Data Terminal Ready signal to each modem. The program uses two registers to access the DZQ11 modem control logic. There are no hardware interlocks between the modem control logic and the receiver and transmitter logic. Any wanted sequence should be done under program control.

The Data Terminal Ready (DTR) bits in the TCR are read/write bits. Setting or clearing a bit in this register turns the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and Line Enable bits are accessed together.) The DTR bits are cleared by the INIT signal on the Q-bus but are not cleared if the program clears the DZQ11 by setting the CLR bit of the CSR.

The Carrier (CD) and Ring (RI) bits in the MSR are read-only bits. The program can determine the current state of the Carrier signal for a line by examining the appropriate bit in the high byte of the MSR. It can determine the current state of the Ring signal for a line by examining the appropriate bit in the low byte of the MSR. The program can examine these registers at different times by using move byte or bit test byte instructions, or can examine them as a single 16-bit register by using move word or bit test word instructions. The DZQ11 modem control logic does not interrupt the processor when a Carrier or Ring signal changes state. The program should regularly sample these registers to determine the current status. Sampling at a high rate is not necessary.