EK-DZQ11-TM-001

DZQ11 Asynchronous Multiplexer Technical Manual

digital™

EK-DZQ11-TM-001

DZQ11 Asynchronous Multiplexer Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

First Edition, October 1984

The information in this document is subject to change without notice. Digital Equipment Corporation assumes no responsibility for any errors herein.

Printed in U.K.

The following are trademarks of Digital Equipment Corporation.

digital™

DEC	PDP	RT
DECmate	P/OS	UNIBUS
DECUS	Professional	VAX
DECwriter	Rainbow	VMS
DIBOL	RSTS	VT
MASSBUS	RSX	Work Processor

CONTENTS

CHAPTER 4 PROGRAMMING

CHAPTER 5 TECHNICAL DESCRIPTION

CHAPTER 6 MAINTENANCE

FIGURES

TABLES

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZQ11 is a Q-bus option. Its outline is shown in Figure 1-1. The DZQ11 is an asynchronous multiplexer that interfaces between a Q-bus processor and four asynchronous serial data communication lines. It can be used in many applications such as data concentration, real-time processing, and cluster controlling. The DZQ11 communications interfaces are compatible with RS-232-C (V.28) and RS-423-A (V.10/X.26). There is enough modem control to permit dial-up (auto-answer) operation with full-duplex modems *, such as the Bell models 103, 113, 212, or equivalent. Remote full-duplex working, as a control (master) station over private lines, is also possible for point-to-point or multipoint operation. Figure 1-2 shows some possible applications for the DZQ11 in a Q-bus system.

All the DZQ11 parameters can be easily controlled. These parameters are:

- Baud rate
- Character length
- Number of stop bits for each line
- Odd or even parity for each line
- Transmitter receiver interrupts.

Additional features include:

- Limited modem control
- Zero receiver baud rate
- Break generation and detection
- Silo buffering of received data
- Line turnaround.

The DZQ11 is program-compatible with the Q-bus DZV11 and with the UNIBUS option DZ11-A. The only exception is the number of serial lines supported. The DZQ11 does not support 20 mA operation.

Documents describing the DZQ11 are:

- DZQ11 Asynchronous Multiplexer User's Guide – EK-DZQ11-UG
- DZQ11 Asynchronous Multiplexer Technical Manual – EK-DZQ11-TM
- Field Maintenance Printset – MP01795
- DZQ11 Maintenance Card – EK-DZQ11-MC

* The DZQ11 modem control does not support half-duplex operation or the secondary transmit-and-receive operation available on some modems (such as the Bell 202).

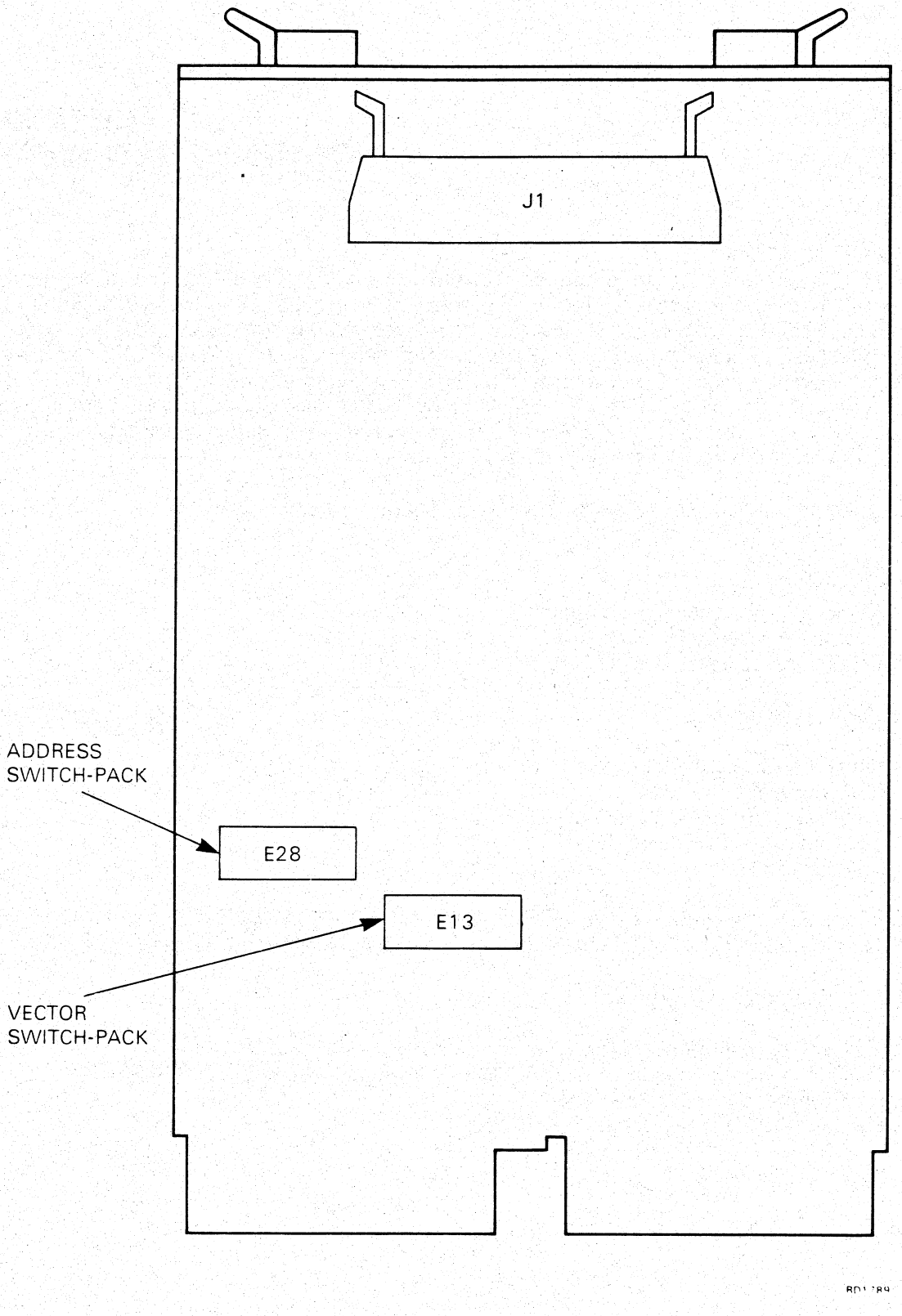


Figure 1-1 M3106 Module

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZQ11 is a Q-bus option. Its outline is shown in Figure 1-1. The DZQ11 is an asynchronous multiplexer that interfaces between a Q-bus processor and four asynchronous serial data communication lines. It can be used in many applications such as data concentration, real-time processing, and cluster controlling. The DZQ11 communications interfaces are compatible with RS-232-C (V.28) and RS-423-A (V.10/X.26). There is enough modem control to permit dial-up (auto-answer) operation with full-duplex modems *, such as the Bell models 103, 113, 212, or equivalent. Remote full-duplex working, as a control (master) station over private lines, is also possible for point-to-point or multipoint operation. Figure 1-2 shows some possible applications for the DZQ11 in a Q-bus system.

All the DZQ11 parameters can be easily controlled. These parameters are:

- Baud rate
- Character length
- Number of stop bits for each line
- Odd or even parity for each line
- Transmitter receiver interrupts.

Additional features include:

- Limited modem control
- Zero receiver baud rate
- Break generation and detection
- Silo buffering of received data
- Line turnaround.

The DZQ11 is program-compatible with the Q-bus DZV11 and with the UNIBUS option DZ11-A. The only exception is the number of serial lines supported. The DZQ11 does not support 20 mA operation.

Documents describing the DZQ11 are:

- DZQ11 Asynchronous Multiplexer User's Guide – EK-DZQ11-UG
- DZQ11 Asynchronous Multiplexer Technical Manual – EK-DZQ11-TM
- Field Maintenance Printset – MP01795
- DZQ11 Maintenance Card – EK-DZQ11-MC

* The DZQ11 modem control does not support half-duplex operation or the secondary transmit-and-receive operation available on some modems (such as the Bell 202).

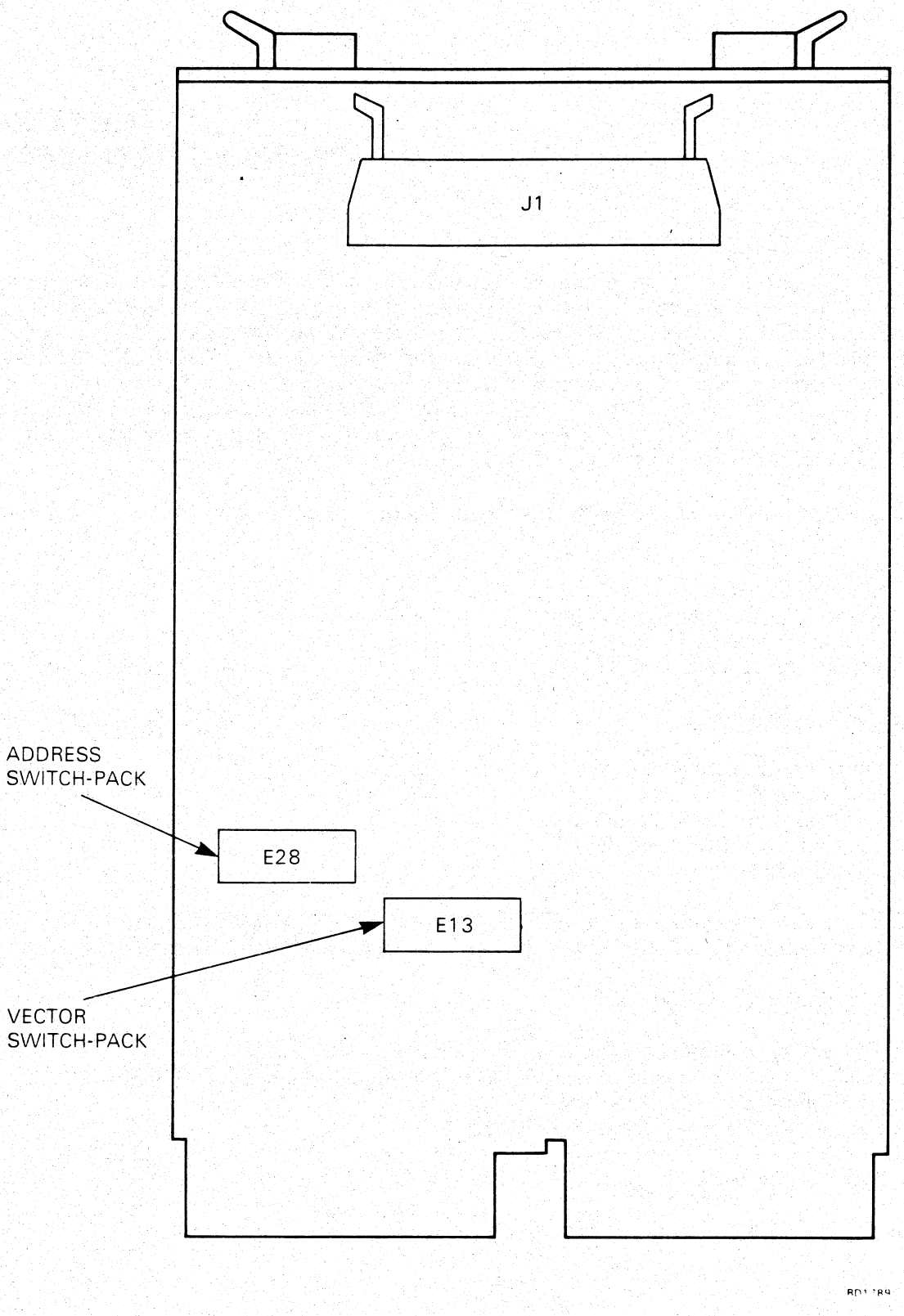


Figure 1-1 M3106 Module

1.2 PHYSICAL DESCRIPTION

The DZQ11 is made up of two components connected by a ribbon cable. The components are:

1. A single dual-height module, 21.6 × 13.2 cm (8.51 × 5.19 inches), called the M3106 module. All input and output connections are available on a Berg * header. This module includes all active circuitry as well as the line drivers and receivers.

2. A distribution panel 6.7 × 8.5 cm (2.6 × 3.3 in) which contains four filtered D-type connectors and a Berg header. This header connects to the M3106 by means of a 40-way ribbon connector.

NOTE

A G7272 Grant Continuity card may be needed. Refer to Section 2.3.2 for an explanation.

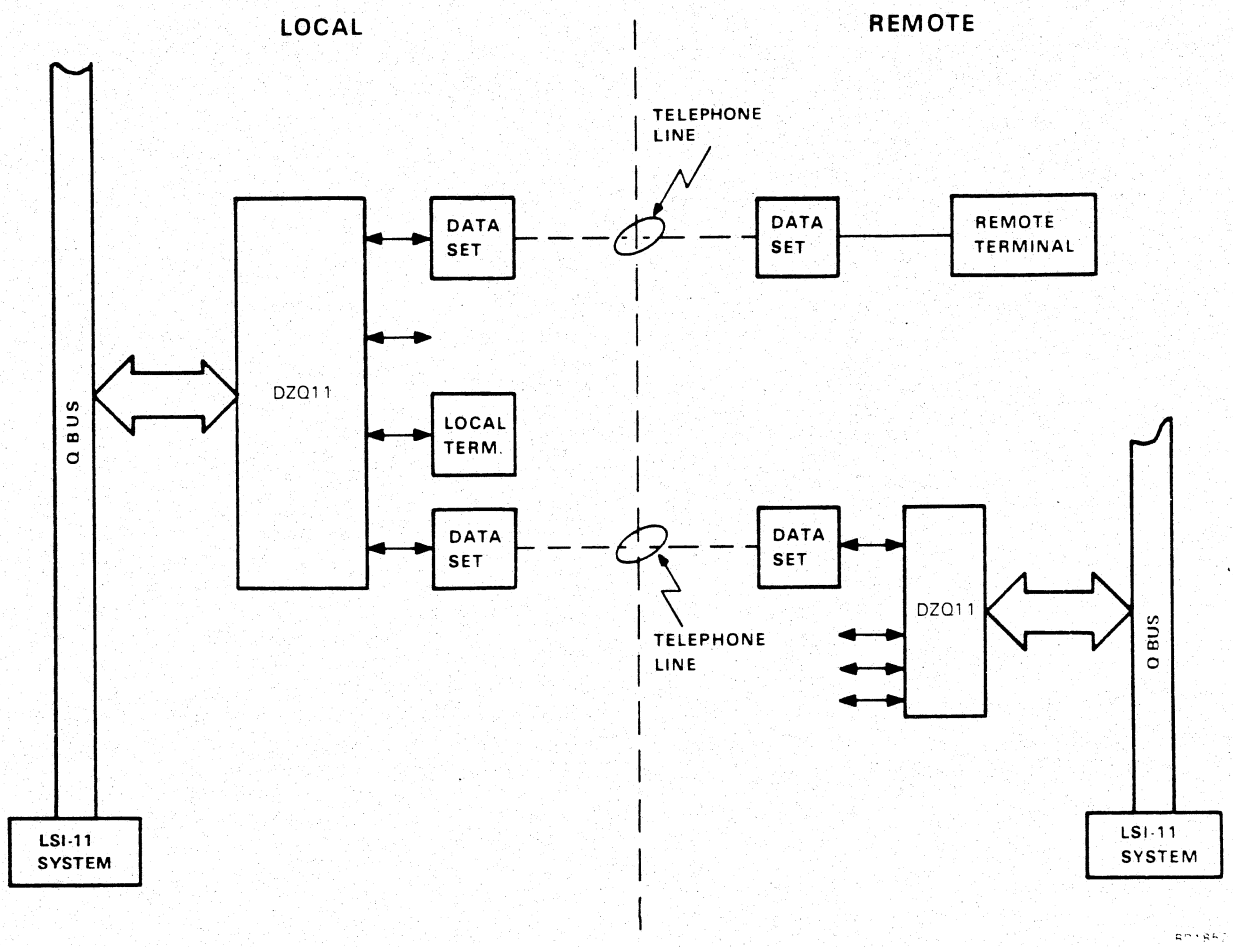


Figure 1-2 DZQ11 System Applications

* Berg is a registered trademark of the Berg Corporation.

1.2.1 DZQ11 Configurations

The basic option supplied is the DZQ11-M and is made up of the following:

1.	Logic Module	M3106
2.	User's Guide	EK-DZQ11-UG
3.	Maintenance Card	EK-DZQ11-MC
4.	Turnaround test connector	H329

The basic option (DZQ11-M) can be supplied with one of five cabinet kits for installation into different systems. These are:

1. CK-DZQ11-DA (21-inch cable), example of use – PDP-11/23S
2. CK-DZQ11-DB (12-inch cable), example of use – Micro/PDP-11
3. CK-DZQ11-DC (30-inch cable), example of use – PDP-11/23+
4. CK-DZQ11-DF (36-inch cable), example of use – PDP-11/83
5. CK-DZQ11-D3 unshielded option (BC11U-25 cable).

The first four cabinet kits are almost identical except for the length of the flat ribbon cables, and the addition of an adapter plate in the CK-DZQ11-DC. They are made up of the following:

1. BC05L-xx cable (see NOTE)
2. H325 line-loopback connector
3. The distribution panel – 70-19964-00
4. Mounting bolts and washers for the distribution panel.

A system integrated DZQ11 option is a DZQ11-DP.

NOTE

The distribution panels provide noise filtering and static discharge protection on the communications lines. The -DC version has an adapter plate which allows the panel to be mounted in the PDP-11/23+.

BC05L-xx cables are supplied in different lengths for each kit as previously specified.

The CK-DZQ11-D3 cabinet kit is a cable assembly made up of four cables, with D-type connectors at one end, and the other end connected to a socket which fits in the module connector. This kit does not provide noise filtering or static discharge protection on the communications lines.

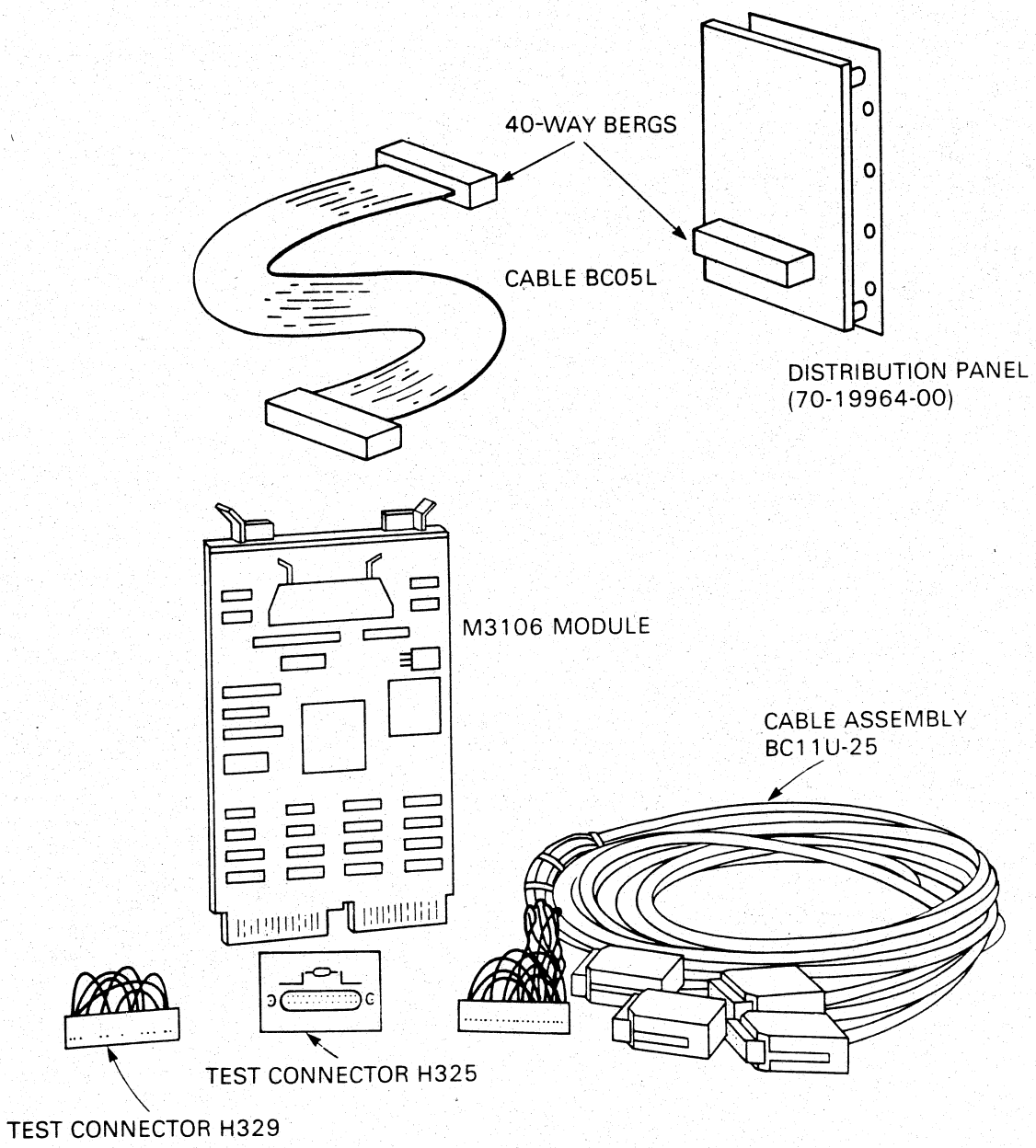


Figure 1-3 Elements of the DZQ11 Option

1.2.2 Interface Cables

The connections from the DZQ11 use 25-pin male subminiature D-type connectors as specified for RS-232-C.

Circuit AA (CCITT* 101)	Pin 1	Protective Ground
Circuit AB (CCITT 102)	Pin 7	Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
Circuit BB (CCITT 104)	Pin 3	Received Data
Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CE (CCITT 125)	Pin 22	Ring Indicator
Circuit CF (CCITT 109)	Pin 8	Carrier

NOTE

Signal ground and protective ground are connected together, through the chassis, by jumper W1 on the 70-19964-00 distribution panel.

1.2.3 Test Connectors

Figure 1-4 shows the two accessory test connectors, H329 and H325.

The H329 plugs into the module I/O connector and connects line 0 to line 1, and line 2 to line 3.

The H325 plugs into an EIA connector on the distribution panel, or BC11U-25 cable assembly, to loopback data and modem signals over a single line. The loopback connections are shown in Figure 1-5.

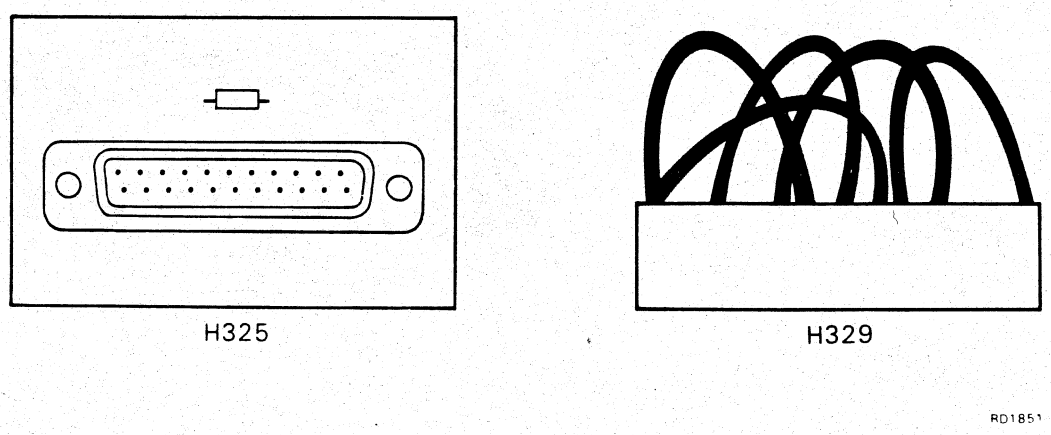


Figure 1-4 Test Connectors H325 and H329

* CCITT – The International Consultative Committee for Telegraphy and Telephony is an advisory committee created under the United Nations to recommend worldwide standards.

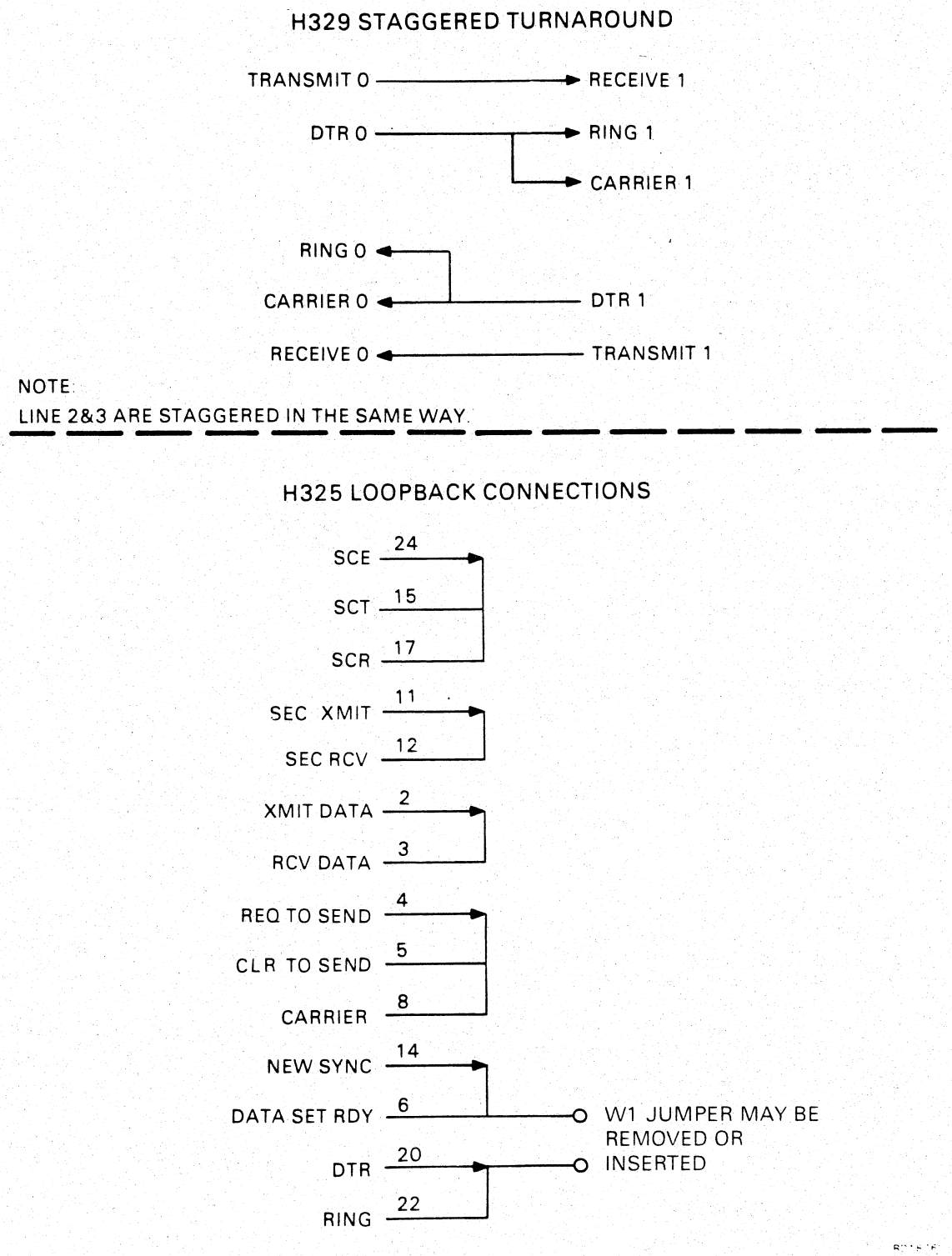


Figure 1-5 Loopback Connection

1.3 SPECIFICATIONS

Environmental, electrical, and performance specifications for the DZQ11 are listed in the following paragraphs.

1.3.1 Environmental

Storage temperature	0 degrees C to 66 degrees C (32 degrees F to 151 degrees F)
Operating temperature	5 degrees C to 60 degrees C (41 degrees F to 140 degrees F)
Relative humidity	10% to 95% non-condensing

1.3.2 Electrical

Power consumption	1.100 A at + 5 V dc typical 0.236 A at + 12 V dc typical
Q-bus loading	Q-bus ac loads – 1.5 ac loads Q-bus dc loads – 1.0 dc loads

1.3.3 Performance

The following paragraphs describe the DZQ11 performance capabilities and restrictions.

1.3.3.1 Interfaces – The DZQ11 interfaces with the host computer bus and also with the four data communication lines.

1. System Bus Interface

   The DZQ11 module interfaces directly to a Q22 or other Q-bus via connectors A and B. The module meets the DIGITAL Q-bus specification.

2. Serial Interfaces

   The DZQ11 serial interfaces comply with a subset of EIA/CCITT standards RS-232-C/V.24. The electrical characteristics are compatible with EIA/CCITT standards RS-232-C/V.28 and RS-423/V.10 (unbalanced interface).

1.3.3.2 Maximum Configurations – The DZQ11 multiplexer is assigned a device address in the floating address space. The floating address space starts at 760010_8 and extends to 763776_8. Maximum configuration of DZQ11s is not limited by floating address space, but is limited by the rules controlling a system configuration of average size.

As the DZQ11 needs one backplane AB slot-pair, it is physically possible to mount:

- Two M3106 modules in a PDP-11/23-S
- Three M3106 modules in a Micro/PDP-11
- Four to five M3106 modules in a PDP-11/23+

These numbers are the absolute maximum, because of the limited number of 70-19964-00 distribution panels that can be installed in the rear panel of the mounting box. These numbers may also be limited by the available capacity of the power supply, if other options are installed in the mounting box.

1.3.3.3 Throughput – Each DZQ11 is capable of a throughput of 10 970 characters per second (chars/s). This rate is computed as follows.

(Bits/s × number of lines × directions) divided by bits/char

(9 600 × 4 × 2)/7 equals 10 970 chars/s, at 5 bits/char with one start and one stop bit and no parity.

The full device throughput can only be maintained when a character service routine takes 100 microseconds or less.

The DZQ11 has a maximum non-standard data rate of 19 800 baud. At this rate the throughput is 22 625 characters per second.

1.3.3.4 Receivers – The receivers perform serial-to-parallel conversion of 5-, 6-, 7-, or 8-level code with one start bit and at least one stop bit. The character length, number of stop bits, parity generation, and operating speed are programmable parameters for each line. Both the receiver and the transmitter of a corresponding line share the same operating speed, and the receiver line can be enabled or disabled.

Each receiver is double buffered and has an acceptable input distortion of 43.75% on any bit. The sum of the character distortion must also not exceed 43.75%. An exception to this is the stop bit. The stop bit can tolerate an error of 50%, that is, the receiver will accept a stop bit as short as one half of a bit period. Break detection is provided on each receiver via a register bit. In addition, the configuration of switchpack E13-9 and E13-10 can cause the processor to boot or halt when a break is detected on line 3.

1.3.3.5 Transmitters – The transmitters provide parallel-to-serial conversion of 5-, 6-, 7- or 8-level code with or without parity. The parity sense, when selected, can be either odd or even. The stop code can be either 1 or 2 units except when 5-level code is selected. When 5-level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks can be transmitted on any line. The maximum start-stop distortion for the output of a transmitter is less than 2.5% for an 8-bit character.

1.3.3.6 Baud-Rate Generator – The baud-rate generators are completely programmable. Each line has an independent generator which can select 1 of 16 baud rates. Speed tolerance for all rates is better than 0.3%. The baud rates are shown in Section 1.3.3.7.

1.3.3.7 Performance Summary – The following list shows the programmable features offered for each line.

Character length	5-, 6-, 7-, or 8-level code
Number of stop bits	1 or 2 for 6-, 7-, or 8-level code. 1 or 1.5 for 5-level code
Parity	Odd, even, or none
Baud rates	50, 75, 110, 134.5, 150, 300, 600, 1 200, 1 800, 2 000, 2 400, 3 600, 4 800, 7 200, and 9 600 (and non-standard 19 800)
Breaks	Can be generated and detected on each line Line 3 has a hardware response to detected breaks which, when enabled, may generate a HALT or RESET. This facility can be selected by switches.

1.3.4 Interrupts

The following interrupts are available on the DZQ11.

1.3.4.1 Receiver-Done Interrupt – The receiver-done interrupt occurs every time a character appears at the output of the receiver buffer register and the silo alarm is disabled. The receiver-done interrupt can be enabled or disabled from the bus.

1.3.4.2 Silo-Alarm Interrupt – The silo-alarm interrupt occurs after 16 entries have been made into the receive buffer register by the scanner. This interrupt disables the receiver-done interrupt, and is armed again when the receive buffer register has been read.

1.3.4.3 Transmit Interrupt – The transmit interrupt occurs every time the scanner finds a buffer-empty condition, and the transmitter control register bit is set for that line. It can be enabled or disabled from the bus.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZQ11 asynchronous multiplexer. It contains information on the following:

- Device and vector address selection
- Recommended cables
- Testing after installation
- Floating address and vector assignment.

2.2 UNPACKING AND INSPECTION

The DZQ11 is packed following normal commercial packing practices. To unpack, first remove all packing material and check the equipment against the shipping list. (Table 2-1 contains a list of supplied items per configuration.) Report any damage or shortages to the shipper immediately and inform the local DIGITAL office. Examine all parts and carefully examine the module for damage, loose components, and breaks in the etched paths.

CAUTION

The M3106 is supplied in a protective sleeve. Do not remove the sleeve until you are about to install the module. Protect the module from static during installation.

WARNING

Procedures which call for the removal of the system covers should be performed by trained personnel only. Information on such procedures is included for user information only.

Table 2-1 Items Supplied per Configuration

DZQ11-M Base Option	
Description	**Quantity**
M3106 module	1
H329 test connector	1
DZQ11 User's Guide (EK-DZQ11-UG)	1

CK-DZQ11-DA/DB/DC/D3/DF Cabinet kits	Quantity				
Description	**DA**	**DB**	**DC**	**D3**	**DF**
70-19964-00 distribution panel	1	1	1	–	1
74-28684-01 adapter plate	–	–	1	–	–
BC05L-1K 21-inch cable	1	–	–	–	–
BC05L-01 12-inch cable	–	1	–	–	–
BC05L-2F 30-inch cable	–	–	1	–	–
BC11U-25 cable assembly	–	–	–	1	–
BC05L-03 36-inch cable	–	–	–	–	1
H325 test connector	1	1	1	1	1
90-06633-00 screws	4	4	8	–	4
90-06021-01 washers	4	4	8	–	4

2.3 INSTALLATION PROCEDURE

The following paragraphs describe the installation of the DZQ11 option in a Q-bus system.

2.3.1 Modem Control Jumpers

There are eight jumpers used for modem control (Figure 2-1). The jumpers labelled W1 to W4 connect the Data Terminal Ready (DTR) circuit to the Request To Send (RTS) circuit. This allows the DZQ11 to assert both DTR and RTS when using modems that need control of RTS. These jumpers must be installed for running the cable and external diagnostic programs. The four jumpers W5 to W8 connect the Forced Busy (FB) circuits to the RTS circuits. When these jumpers are installed, asserting an RTS circuit also places an ON or BUSY level on the corresponding FB circuit. Jumpers W5 to W8 are normally cut out unless they are needed by the modems used. Table 2-2 shows the jumper line assignments.

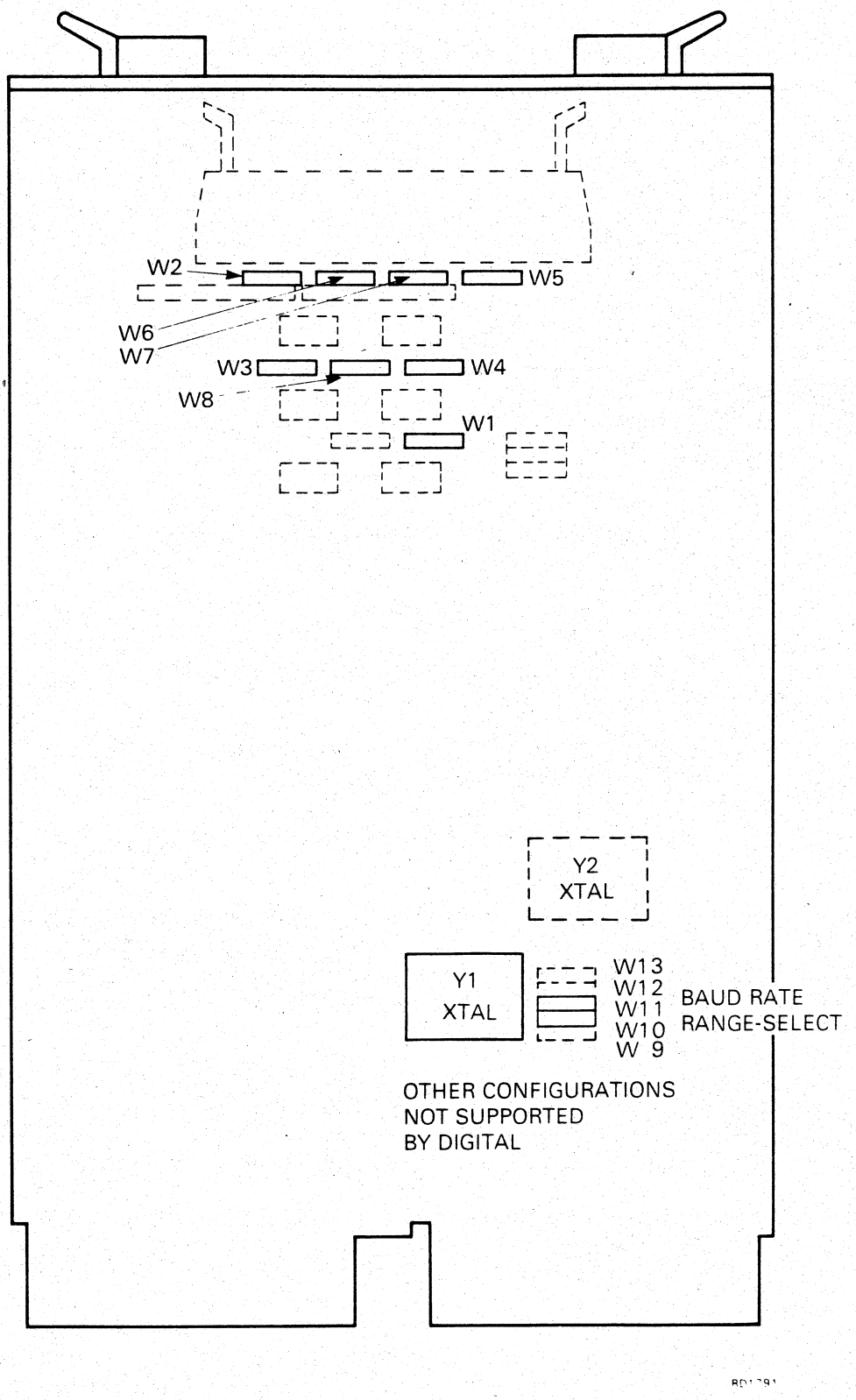


Figure 2-1 Jumper Location on M3106 Module

Table 2-2 Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

2.3.2 Module Installation

To install the M3106 module, perform the following.

NOTE

This checkout procedure should be performed by trained maintenance personnel only.

CAUTION

Switch off power before inserting or removing modules.

The M3106 is a fine-line-etch PCB. Handle it carefully to avoid damaging the etch.

Take anti-static measures to protect the module.

1. The Q-bus Interrupt Acknowledge and the DMA Grant signals are daisy-chained through the AB slots of the Q-bus backplane. If a DZQ11 is followed by a quad-size option in an AB/AB (Q/Q) backplane, it may cause an AB slot-pair to be left vacant. In order to maintain the continuity of the daisy-chained signals, a G7272 Grant Continuity card should be installed in the vacant A slot.

2. Refer to Section 2.4 for descriptions of the address assignments. Set the switches at E28 so that the module responds to its assigned address. When a switch is closed (ON), a binary 1 is encoded. When a switch is open (OFF), a binary 0 is encoded. The switch numbered 1 is connected to address bit 12, 2 is connected to address bit 11, and so on (Table 2-4).

3. The 10-position switch at E13 performs the vector selection. Switch position 7 is not used. Switch position 6 is connected to vector bit 3, 5 is connected to vector bit 4, and so on. When a switch is closed (ON), binary 1 is encoded. When a switch is open (OFF), a binary 0 is encoded (Table 2-5).

4. Position 8 of the vector selection switch is a test switch which can disconnect the DZQ11 oscillator from all circuitry. Make sure that this switch is in the ON position before installation.

5. Positions 9 and 10 of switch E13 control the DZQ11 response to a Break character received on Line 3. There are three valid options: HALT, BOOT, and no response. Table 2-3 lists the switch selections.

Table 2-3 Break Character Response Options

Switch 9	Switch 10	Effect of Break Character on Line 3	
OFF	OFF	No effect	(normal operation)
ON	OFF	Causes Processor to halt	(specific application)
OFF	ON	Causes Processor to boot	(specific application)
ON	ON	Illegal Condition	

6. Make sure that +5 volts is present between AA2 and ground and that +12 volts is present between AD2 and ground. Measure at the nearest accessible point, if the backplane cannot be accessed.

7. Remove power and insert the module in an AB slot of the backplane.

8. Apply power and make sure that the +5 volts and +12 volts is present with the module installed.

CAUTION

Insert and remove modules slowly and carefully to prevent damage to the module components on the card guides, and to avoid changing switch selections in error.

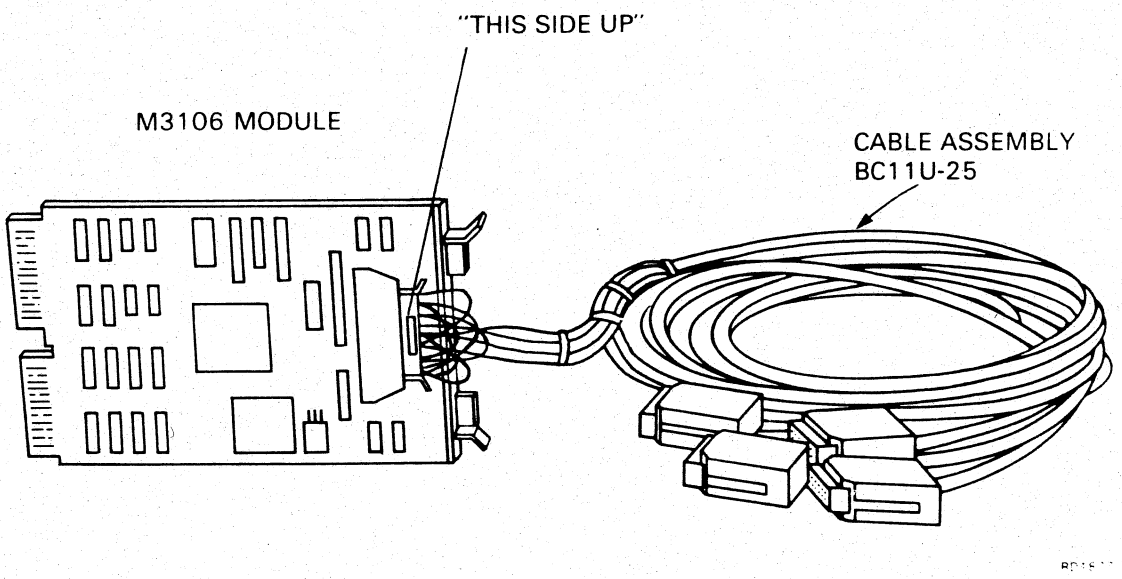
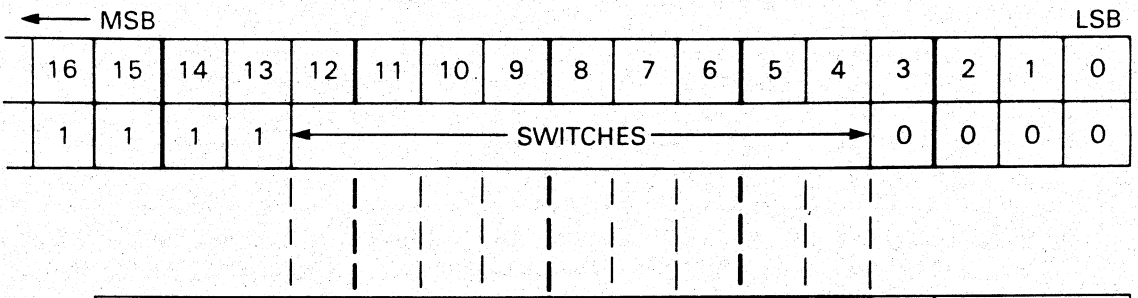


Figure 2-2 DZQ11 Installation (BC11U-25)

Table 2-4 Address Switch Selection



SWITCH NUMBER	E28 1	E28 2	E28 3	E28 4	E28 5	E28 6	E28 7	E28 8	E28 9	E28 10	DEVICE ADDRESS
											17760000
										ON	17760010
									ON		17760020
									ON	ON	17760030
								ON			17760040
								ON		ON	17760050
								ON	ON		17760060
								ON	ON	ON	17760070
							ON				17760100
						ON					17760200
						ON	ON				17760300
					ON						17760400
					ON		ON				17760500
					ON	ON					17760600
					ON	ON	ON				17760700
			ON	ON	ON	ON	ON	ON	ON		17763760
			ON	ON	ON	ON	ON	ON	ON	ON	17763770

ON = SWITCH CLOSED TO RESPOND TO A LOGICAL 1 ON THE BUS

Table 2-5 Vector Switch Selection

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	← SWITCHES →						1/0	0	0

REFER TO SECTION 2.3.2 FOR SETTING OF E13 - 7 TO 10

SWITCH NUMBER	E13 1	E13 2	E13 3	E13 4	E13 5	E13 6	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700
	ON	ON	ON	ON	ON		760
	ON	ON	ON	ON	ON	ON	770

ON = SWITCH CLOSED TO PRODUCE A LOGICAL 1 ON THE BUS

RD-879

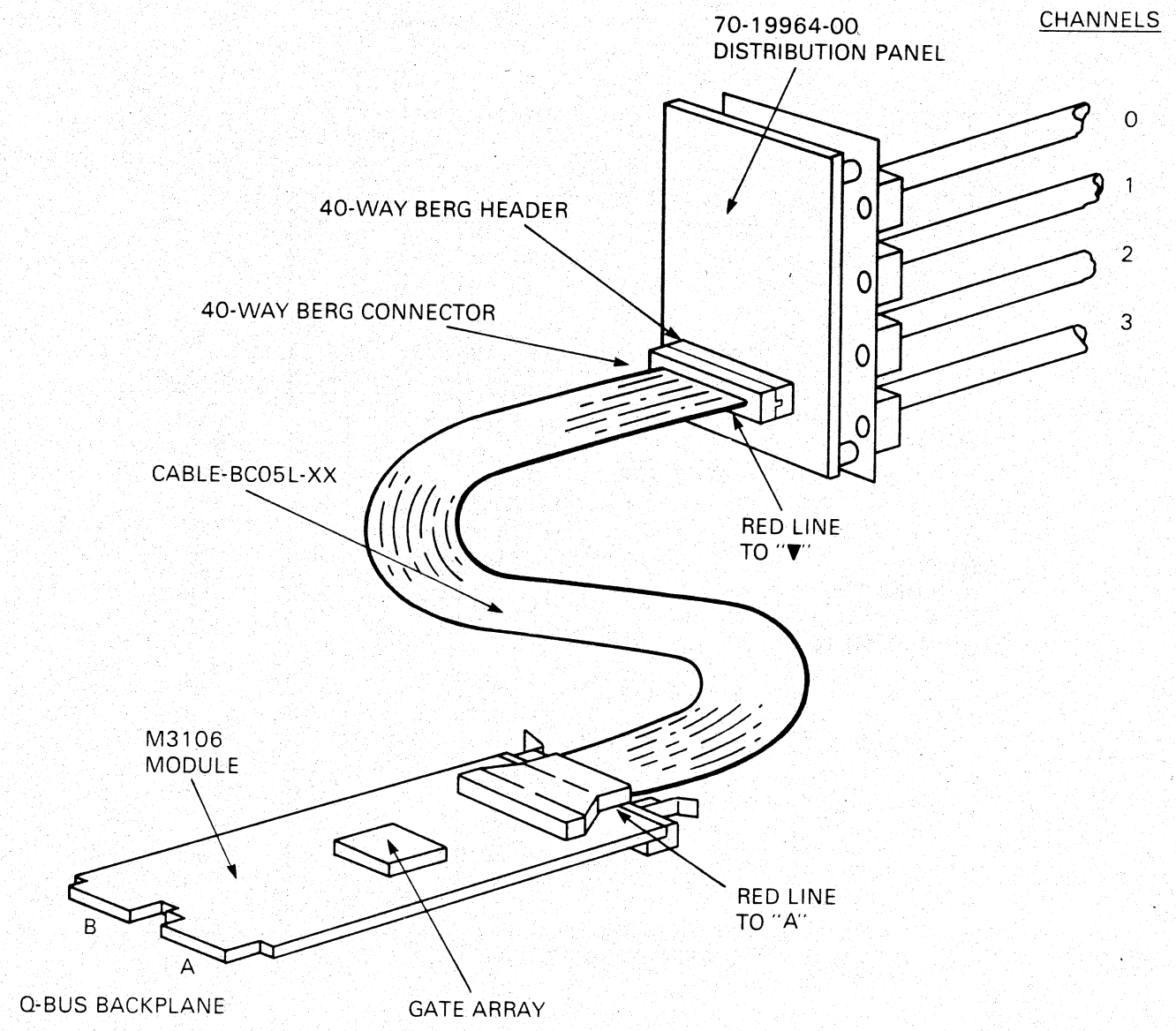


Figure 2-3 DZQ11 Installation (70-19964-00)

2.3.3 Testing DZQ11s in PDP-11 Systems

The following diagnostics are available to test DZQ11s installed in PDP-11 systems. DZITA and DVDZD are only used when a link between two processors is to be tested.

CVDZA	DZV11/DZQ11 Logic Test – Part 1
CVDZB	DZV11/DZQ11 Logic Test – Part 2
CVDZC	DZV11/DZQ11 Cable/Echo Test
CXDZB	DECX/11 Module
DZITA	Interprocessor Test Program (ITEP)
DVDZD	Overlay for ITEP

Test the option as follows.

1. Run diagnostics CVDZA and CVDZB in internal mode, to verify operation. Refer to the listing for more help. Run at least three passes without error.

2. Insert the H329 test connector in J1 with the letter side facing up. J1 is the cable connector at the top of the M3106 module.

   Run CVDZA and CVDZB in the staggered mode, to verify module operation. Refer to the diagnostic listing for the correct procedure. Run at least three passes without error.

3. If the unshielded cab-kit (D3) version is used, replace the H329 test connector with the Berg end of the BC11U cable assembly. Follow the 'This side up' instruction on the assembly. Refer to Figure 2-2 for assembly and interconnection instructions.

4. If the cab-kit versions CK-DZQ11-DA, -DB or -DF are used, feed the cable through the rear of the cabinet and connect the Berg plug to the distribution panel. Mount the distribution panel in the opening at the rear of the cabinet.

   The -DC version is provided with an adapter plate to fit the large opening in a PDP-11/23+. Mount the adapter plate on the distribution panel, with four of the eight screws provided. Mount the distribution panel as described above.

5. Connect the H325 test connector on the first line and run diagnostic CVDZC. Select the cable-test part of the diagnostic. Three passes are needed without error. Repeat this step for each line.

6. Run the DECX/11 system exerciser to verify the absence of Q-bus interference with other system devices.

7. The DZQ11 is now ready for connection to external equipment. If the connection is to a local terminal through either of the two options (BC11U-25 or 70-19964-00), a null modem cable assembly must be used. Use the BC22A, BC22D, or BC03P null modem cables for connection between the option and the terminal. The H312-A null modem unit may also be used in place of the null modem cables.

   Connections between the option and a modem should be made using a BC22E or BC05D cable.

   All of the cables referred to, with the exception of the BC11U-25, must be ordered separately as they are not components of a DZQ11 option.

   If a terminal is available, run the diagnostic CVDZC in echo-test mode to verify the cable connections and the terminal equipment.

2.3.4 Testing in MicroVAX Systems

The following diagnostic tests are available for testing DZQ11s in MicroVAX systems.

EHXDZ	DZV11/DZQ11 Test
EHKMV	Macroverify – MicroVAX System Test

Macroverify is a standalone diagnostic which contains a DZV11/DZQ11 test module.

Refer to the appropriate diagnostic listing, or to Chapters 11 and 14 of the MicroVAX Owner's Guide, for details of how to run EHXDZ and EHKMV.

Test the option as follows.

1. Boot from the MicroVAX system tests diskette (number 2 of 2). Attach and select the DZQ11 that is to be tested.

2. Run EHXDZ for three error-free passes of the internal (default) test.

3. Install the H329 staggered loopback connector on the M3106 module. Run EHXDZ for three error-free passes of the staggered test.

4. Remove the H329. Install the BC05L cable and the distribution panel.

5. If the operation of a terminal link is to be tested, connect the terminal line to the distribution panel. Run the EHXDZ echo test on that line until the link is proven. Depending on the terminal, a null-modem may be needed for this test. Exit echo test by ^Z (CTRL/Z).

6. Remove all external cables and connectors from the distribution panel. Boot the CPU tests diskette (number 1 of 2). The Macroverify diagnostic will run automatically when the boot process is complete. When the test completes, the status of all options will be displayed.

7. If no device has a TEST FAILED status, the DZQ11 is now ready for connection to external equipment. If the connection is to a local terminal, a null modem cable assembly must be used. Use the BC22A, BC22D, or BC03P null modem cables for connection between the option and the terminal. The H312-A null modem unit may also be used in place of the null modem cables.

   Connections between the option and a modem should be made using a BC22E or BC05D cable.

   All of the referenced cables must be ordered separately as they are not components of a DZQ11 option.

2.4 DEVICE ADDRESS ASSIGNMENTS

On UNIBUS and Q-bus systems, a range of addresses ($xxx60010_8$ to $xxx63776_8$) in the top 4K words is assigned as floating address space (xxx means all top address bits = 1).

The first part of the list of options (sufficient to include the DZQ11) which can be assigned floating device addresses is given in Table 2-6. 'Rank' gives the sequence of address assignment for both Q-bus and UNIBUS options.

If addresses are assigned according to defined rules, configuration programs can check which options are installed in a system. Having a combined list allows us to use one set of configuration rules and one configuration program for both Q-bus and UNIBUS systems.

Table 2-6 Floating Address Assignments

Rank	Device	Size (decimal)	Modulus (octal)
1	DJ11	4 words	10
2	DH11	8 words	20
3	DQ11	4 words	10
4	DU11, DUV11*	4 words	10
5	DUP11	4 words	10
6	LK11A	4 words	10
7	DMC11/DMR11	4 words	10
8	DZ11, DZS11, DZQ11*/DZV11* DZ32	4 words	10

* Q-bus device

For example, the address assignment sequences could be:

UNIBUS	Q-bus
DJ11	No Q-bus equivalent of DJ11
DH11	No Q-bus equivalent of DH11
DQ11	No Q-bus equivalent of DQ11
DU11	DUV11
DUP11	No Q-bus equivalent of DUP11
LK11A	No Q-bus equivalent of LK11A
DMC11	No Q-bus equivalent of DMC11
DZ11	DZQ11 and so on.

Devices of the same type are given sequential addresses, therefore all DUV11s in a system will have lower addresses than DZQ11s or DZV11s.

For the purpose of address assignment, DZQ11s and DZV11s are considered as devices of the same type.

The column *Size(decimal)* in Table 2-6, shows how many words of address space are needed for each device. The column *Modulus(octal)* is the modulus used for starting addresses. For example, devices with an octal modulus of 10 must start at an address which is a multiple of 10_8. The same rule is used to select a gap address (see assignment rules) after an option, or for a nonexistent device.

The assignment rules are as follows.

1. Addresses, starting at xxx60010, are assigned according to the sequence of Table 2-6
2. Option and gap addresses are assigned according to the octal modulus as follows.
   a. Devices with an octal modulus of 10 are assigned an address on a 10_8 boundary (the three lowest-order address bits = 0)
   b. Devices with an octal modulus of 20 are assigned an address on a 20_8 boundary (the four lowest-order address bits = 0)
3. Address space equal to the device's modulus must be allowed for each device which is connected to the bus
4. A one-word gap, assigned according to rule 2, must be allowed after the last device of each type. This gap could be bigger when rule 2 is applied to the following rank
5. A one-word gap, assigned according to rule 2, must be allowed for each unused rank on the list if a device with a higher address is used. This gap could be bigger when rule 2 is applied to the following rank

Two examples of address assignment follow. Table 2-7 shows addresses for a system with one DUV11 and one DZQ11. Table 2-8 shows addresses for a system with no DUV11 and two DZQ11s. Note that where there is no Q-bus device at a specific rank, the UNIBUS device parameters must be used to assign the gap. Vector assignments (see Section 2.5) are also shown in these tables.

Table 2-7 is supported by a description of how to apply the assignment rules.

Table 2-7 One DUV11 and One DZQ11

Rank	Address	Designation	Vector
1	xxx60010	DJ11 gap	
2	xxx60020	DH11 gap	
3	xxx60030	DQ11 gap	
4	xxx60040	DUV11	300
	xxx60050	DUV11 gap	
5	xxx60060	DUP11 gap	
6	xxx60070	LK11A gap	
7	xxx60100	DMC11 gap	
8	xxx60110	DZQ11	310
	xxx60120	DZQ11 gap	

The first floating address is 760010. As a DJ11 has a modulus of 10_8, its gap can be assigned to 760010. The next available location becomes 760012.

As a DH11 has a modulus of 20_8, it cannot be assigned to 760012. The next modulo 20 boundary is 760020, so the DH11 gap is assigned to this address. The next available location is therefore 760022.

A DQ11 has a modulus of 10_8. It cannot be assigned to 760022. Its gap is therefore assigned to 760030. The next available location is 760032.

The DUV11 has a modulus of 10_8. It cannot be assigned to 760032. It is therefore assigned to 760040. As the size of DUV11 is four words, the next available address is 760050.

There is no second DUV11, so a gap must be left to indicate that there are no more DUV11s. As 760050 is on a 10_8 boundary. The DUV11 gap can be assigned to this. The next available address is 760052.

And so on.

Table 2-8 Two DZQ11s

Rank	Address	Designation	Vector
1	xxx60010	DJ11 gap	
2	xxx60020	DH11 gap	
3	xxx60030	DQ11 gap	
4	xxx60040	DUV11 gap	
5	xxx60050	DUP11 gap	
6	xxx60060	LK11A gap	
7	xxx60070	DMC11 gap	
8	xxx60100	1st DZQ11	300
8	xxx60110	2nd DZQ11	310
	xxx60120	DZQ11 gap	

2.5 INTERRUPT VECTOR ADDRESS ASSIGNMENTS

Addresses between 300_8 and 774_8 are designated as the floating vector space. These addresses are assigned in sequence as in Table 2-9.

Each Device needs two 16-bit locations for each vector. For example, a device with one receive and one transmit vector needs four words of vector space.

The vector assignment rules are as follows.

1. Each device occupies vector address space equal to 'Size' words. For example, the DLV11-J occupies 16 words of vector space. If its vector was 300_8, the next = available vector would be 340_8.
2. There are no gaps, except those needed to align an octal modulus.

The vector addresses shown in Tables 2-7 and 2-8 are assigned according to these rules.

Table 2-9 First Part of Q-bus Vector Address Assignments List

Device	Size (decimal)	Modulus (octal)
DLV11-J	16	10
DLV11,DLV11-F	4	10
DRV11-B	4	10
DRV11	4	10
DLV11-E	4	10
VSV11	8	10
KWV11	4	10
DUV11	4	10
DZV11/DZQ11	4	10

CHAPTER 3
DEVICE REGISTERS

3.1 SCOPE

This chapter describes the format and bit function of each register in the DZQ11.

3.2 DEVICE REGISTERS

The DZQ11 contains six addressable registers. Figure 3-1 shows the bit assignments of these registers and Table 3-1 lists the registers and related DZQ11 addresses.

Table 3-1 DZQ11 Register Address Assignments

Register Name	Mnemonic	Address	Program Capability
Control and Status Reg.	CSR	76XXX0	Read/Write
Receiver Buffer	RBUF	76XXX2	Read Only
Line Parameter Register	LPR	76XXX2	Write Only
Transmitter Control Reg.	TCR	76XXX4	Read/Write
Modem Status Register	MSR	76XXX6	Read Only
Transmit Data Register	TDR	76XXX6	Write Only

XXX = Selected in agreement with the floating device address system.

3.2.1 Control and Status Register

The control and status register (CSR) can be addressed with a byte or word address. All bits in the CSR are cleared by an occurrence of BINIT, or by setting device Master Clear (CSR<04>). The format is shown in Figure 3-1 and the bit assignments are listed in Table 3-2.

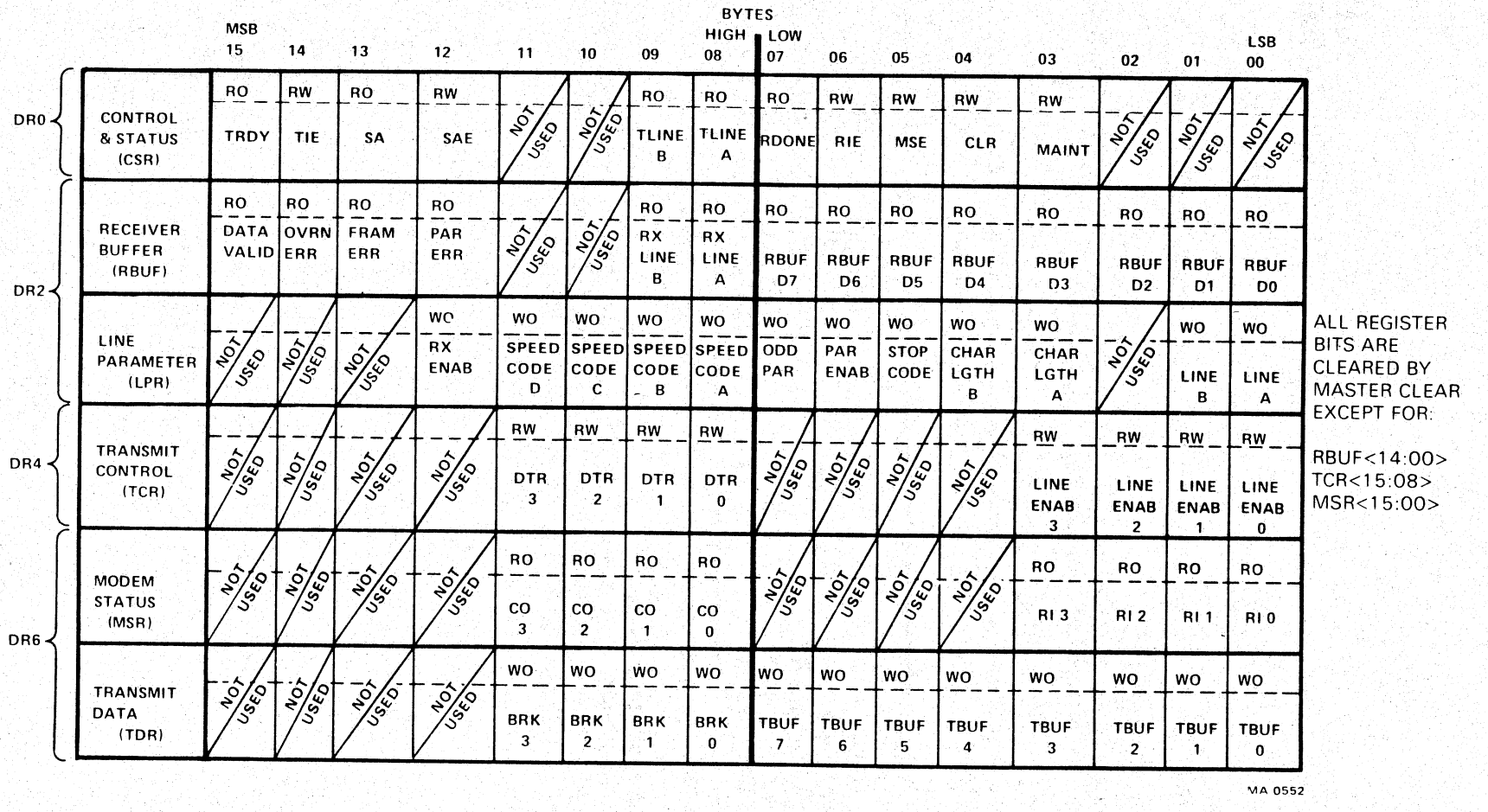


Figure 3-1 Register Bit Assignment

Table 3-2 CSR Bit Assignments

Bit	Title	Function
<02:00>	Not used	
<03>	Maintenance (MAINT)	This is a READ/WRITE bit. When set it loops the serial output connections of the transmitter to the corresponding serial input connections of the receiver at the UART. (Used for loopback test only.)
<04>	Master Clear (CLR)	When written to a 1, this bit generates 'initialize' within the DZQ11. A read-back of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTs are cleared with the following exceptions: 1. Only bit 15 of the receiver buffer register (Data Valid) is cleared; the other bits (<14:00>) are not. 2. The high byte of the transmitter control register is not cleared by Master Clear. 3. The modem status register is not cleared by Master Clear.
<05>	Master Scan Enable (MSE)	This read/write bit must be set to permit the receiver and transmitter control sections to start scanning. When cleared, Transmitter Ready (CSR<15>) is inhibited from setting, and the received character buffers (silos) are cleared.
<06>	Receiver Interrupt Enable (RIE)	This bit permits the generation of an interrupt, when CSR<07> or CSR<13> is set. This bit is read/write.
<07>	Receiver Done (RDONE)	This is a read-only bit that is set when a character appears at the output of the first-in/first-out (FIFO) buffer. For the DZQ11 to run in the interrupt-per-character mode, CSR<06> must be set and CSR<12> must be cleared. With CSR<06> and CSR<12> cleared, character-flag mode is indicated. Receiver Done clears when the receiver buffer register (RBUF) is read or when Master Scan Enable (CSR<05>) is cleared. If the FIFO buffer contains an additional character, the Receiver Done flag stays clear for up to 1 microsecond, while that character bubbles through to the bottom of the FIFO.
<09:08>	Transmitter Line Number (TLINE B and TLINE A)	These read-only bits indicate the line number whose transmit buffer needs servicing. These bits are valid only when Transmitter Ready (CSR<15>) is set, and are cleared when Master Scan Enable is cleared. Bit <08> is the least-significant bit.
<11:10>	Not used	

Table 3-2 CSR Bit Assignments (Cont)

Bit	Title	Function
<12>	Silo Alarm Enable (SAE)	This is a read/write bit. When set, it enables the silo-alarm and prevents RDONE (bit <07>) from causing interrupts. If the receiver interrupt enable bit (bit <06>) is set, SAE enables the silo-alarm (bit <13>) to generate an interrupt after 16 silo entries. If silo-alarm is not set, then SAE may be used as a flag to indicate that 16 or more characters are in the silo.
<13>	Silo Alarm (SA)	This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo Alarm is held cleared when Silo Alarm Enable (CSR<12>) is cleared. This bit is cleared by a read to the receiver buffer register and does not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR<06>) is set, the occurrence of Silo Alarm generates a receiver interrupt request. Flag mode operation of the Silo Alarm bit is permitted with CSR<06> cleared.
<14>	Transmitter Interrupt Enable (TIE)	This is a read/write bit which must be set for Transmitter Ready to generate an interrupt.
<15>	Transmitter Ready (TRDY)	This read-only bit is set by the hardware when the transmitter scanner stops on a line whose transmit buffer may be loaded with another character and whose related TCR bit is set. The transmitter line number, specified in CSR<09:08>, is only valid when Transmitter Ready is set. Transmitter Ready is cleared by any of the following conditions: 1. When Master Scan Enable is cleared. 2. When the related TCR bit is cleared for the line number pointed to in CSR<09:08> If additional transmit lines need service, Transmitter Ready appears again within 1.4 microseconds of the completion of the 'transmit data register load' instruction. When Transmitter Ready occurs with Transmitter Interrupt Enable set, a transmitter interrupt request is generated.

3.2.2 Receiver Buffer

The receiver buffer (RBUF) is a 16-bit read-only register that contains the received character at the output of the FIFO buffer. A read of the register causes the character entry to be removed from the buffer, and all other entries to shift down to the lowest location that is not occupied. Only the Data Valid bit (RBUF<15>) is cleared by BINIT or by setting device Master Clear (CSR<04>). Bits <14:00> are not affected. The bit assignments for the RBUF register are listed in Table 3-3.

Table 3-3 RBUF Bit Assignments

Bit	Title	Function
<07:00>	Received Character (RBUF D<7:0>)	These bits contain the received character, right justified. the least-significant bit is bit <00>. For short characters, bits that are not used are logic low. The parity bit is not shown.
<09:08>	Received Line Number (RX LINE B and RX LINE A)	These bits contain the line number on which the Received Character was received. Bit <08> is the least significant.
<11:10>	Not used	
<12>	Parity Error (PAR ERR)	This bit is set if the sense of the parity of the received character does not agree with the parity defined for that line.
<13>	Framing Error (FRAM ERR)	This bit is set if the received character did not have a stop bit present at the correct time. This bit is usually interpreted as indicating that a break has been received.
<14>	Overrun Error (OVRN ERR)	This bit becomes set when a received character is overwritten in the UART buffer (by a following character), before it has been transferred by the scanner to the FIFO.
<15>	Data Valid (DATA VALID)	This bit, when set, indicates that the data in bits <14:00> is valid. This bit permits the use of a character-handling program which again and again takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit <15> until the program gets a word for which bit <15> is zero.

3.2.3 Line Parameter Register

The line parameter register (LPR) controls the operating parameters related to each line in the DZQ11. The LPR must be addressed with a word address and is a write-only register. The line parameters for all lines must be loaded again following an occurrence of either BINIT or device Master Clear. Table 3-4 lists bit assignments.

Table 3-4 LPR Bit Assignments

Bit	Title	Function
<01:00>	Parameter Line Number (LINE B and LINE A)	These bits specify the line number for which the parameter information (bits <12:3>) is to apply. Bit <00> is the least-significant bit.
<02>	Not used	Must always be written as a zero when specifying the parameter line number. Writing this bit as a one extends the parameter line number field into nonexistent lines. Parameters for lines 00 to 03 are not affected.

Table 3-4 LPR Bit Assignments (Cont)

Bit	Title	Function
<04:03>	Character Length (CHAR LGTH B and CHAR LGTH A)	These bits are set to receive and transmit characters of the length (except parity) shown below.

Bit 04	Bit 03	
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

<05>	Stop Code (STOP CODE)	This bit sets the stop code length; 0 = 1 unit stop, 1 = 2 unit stop (or 1.5 unit stop if a 5-level code is used).
<06>	Parity Enable (PAR ENAB)	If this bit is set, characters transmitted on the line have an appropriate parity bit added, and characters received on the line have their parity checked.
<07>	Odd Parity (ODD PAR)	If this bit is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit <06> is set, characters of even parity are generated on the line, and incoming characters are expected to have even parity. If bit <06> is not set, then the setting of this bit will not have any effect.
<11:08>	Speed code (SPEED CODE D to SPEED CODE A)	The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1 200
1	0	0	0	1 800
1	0	0	0	2 000
1	0	1	0	2 400
1	0	1	1	3 600
1	1	0	0	4 800
1	1	0	1	7 200
1	1	1	0	9 600
1	1	1	1	19 800 *

* Not supported by standard software.

Table 3-4 LPR Bit Assignments (Cont)

Bit	Title	Function
<12>	Receiver Enabled (RX ENAB)	This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit is cleared following a BINIT or device Master Clear.
<15:13>	Not used	

NOTE

The M3106 module can be modified by jumpers W9 to W13, so that code 1111 selects baud rates other than 19 800. This modification is not supported by DIGITAL.

3.2.4 Transmitter Control Register

The transmitter control register (TCR) is a byte- and word-addressable register. The low byte of the TCR contains the transmitter control bits, and must be set to start transmission on a line. Each TCR bit position is related to a line number. For example, TCR<00> is related to line 00, bit <01> to line 01, and so on. Setting a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a 'transmit buffer empty' condition. An interrupt is then generated if Transmitter Interrupt Enable is set. The scanner clock restarts when either the transmit data register (TDR) is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running, (that is, Transmitter Ready is set or Master Scan Enable is cleared).

The line enable bits are represented in TCR<03:00>. These bits are read/write and are cleared by BINIT or device Master Clear. Bits <07:04> are not used, and are read as zero.

The high byte of the TCR register contains the modem control signal that can be written, data terminal ready (DTR). The bits are defined as follows:

Bit	Name
<08>	DTR Line 00
<09>	DTR Line 01
<10>	DTR Line 02
<11>	DTR Line 03
<15:12>	Not used; read as zero

Assertion of a DTR bit creates an ON condition on the appropriate modem circuit for that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the RTS circuits to be asserted using DTR assertions.

3.2.5 Modem Status Register

The modem status register (MSR) is a 16-bit read-only register. A read to this register gives the status of the modem control signals that can be read, Ring and Carrier. The ON condition of a modem control signal is interpreted as a logical one. Bits <07:04> and <15:12> are not used and are read as a zero. The other bits are defined as follows:

Bit	Name	Bit	Name
<00>	Ring Line 00	<08>	Carrier Line 00
<01>	Ring Line 01	<09>	Carrier Line 01
<02>	Ring Line 02	<10>	Carrier Line 02
<03>	Ring Line 03	<11>	Carrier Line 03
<07:04>	Not used; read as zero	<15:12>	Not used; read as zero.

3.2.6 Transmit Data Register

The transmit data register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR<00> is the least-significant bit. Loading of a character should occur only when Transmitter Ready (CSR<15>) is set. The character that is loaded into this register is routed to the line defined in CSR<09:08>. The high byte of the TDR is defined as the break control register.

There is a corresponding break bit for each of the four multiplexer lines. TDR<08> represents the break bit for line 00, TDR<09> for line 01, and so on. TDR<15:12> are not used. Setting a break bit forces the output of that line to space. This register is cleared by BINIT or device Master Clear. The break control register can be used regardless of the state of the Device Maintenance bit (CSR<03>).

CHAPTER 4
PROGRAMMING

4.1 SCOPE

This chapter contains information for programming the DZQ11 in the most efficient way. To do so, the programming controls must be completely understood. The following paragraphs discuss the DZQ11 from the programming point of view and describe recommended programming methods.

4.2 PROGRAMMING FEATURES

The DZQ11 has some programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to get the wanted operating parameters.

4.2.1 Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the way that the DZQ11 receiver interrupts the processor.

If RIE and SAE are both clear, the DZQ11 never interrupts the processor. In this event, the program must regularly check that the data is available in the silo, and empty the silo when data is present. If the program operates from a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety element to cover processor-response delays and time to empty the silo. The Receiver Done (RDONE) bit in the CSR is set when a character is available in the silo. The program can regularly check this bit with a test byte or bit test instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZQ11 interrupts the processor and forces it to the DZQ11 receiver vector address, when RDONE is set. This indicates the presence of a character at the bottom of the silo. The interrupt service routine can get the character by performing a move instruction from the RBUF. If the program then dismisses the interrupt, the DZQ11 interrupts when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Another way is for the interrupt service routine to respond to the interrupt by emptying the silo before it dismisses the interrupt.

If RIE and SAE are both set, the DZQ11 interrupts the processor to the DZQ11 receiver vector when the Silo Alarm (SA) bit in the CSR is set. The SA bit is set when 16 characters have been placed in the silo after the last time the program has accessed the RBUF. Accessing the RBUF clears the SA bit and the related counter. The program should follow the procedure described in Section 4.2.2 to empty the silo completely in response to a Silo Alarm interrupt. This makes sure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each Silo Alarm interrupt, characters coming in while interrupts are being processed build up without being counted by the Silo Alarm circuit. The silo may in the end overflow without the alarm being issued.

If the Silo Alarm interrupt is used, the program will not be interrupted when fewer than 16 characters are received. In order to respond to short messages during periods of medium activity, the program should regularly empty the silo. The scanning period depends on the wanted response time to received characters. While the program is emptying the silo, it should make sure that DZQ11 receiver interrupts are inhibited. This should be done by raising the processor priority. The Silo Alarm interrupt feature can greatly decrease the processor overhead that would be needed by the DZQ11 receiver. This is done by removing the need to enter and exit an interrupt service routine each time a character is received.

The Transmitter Interrupt Enable (TIE) bit controls transmitter interrupts to the processor. If enabled, the DZQ11 interrupts the processor at the DZQ11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set. This indicates that the DZQ11 is ready to accept a character to be transmitted.

Each DZQ11 needs two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests are generated from each section, the receiver section would have priority in placing its vector on the Q-bus. A receiver interrupt to address XX0 is generated from having either a Receiver Done (CSR<07>) or Silo Alarm (CSR<13>) occurrence. A transmitter interrupt to address XX4 is generated by Transmitter Ready (CSR<15>). An additional prerequisite for generating interrupts is that the individual interrupt enable bits are set. The recommended method for clearing interrupt enable bits is first to raise the processor status word to level 4; next, to clear these interrupt enable bits; and then lower the processor status word to zero. Using this method prevents false interrupts from being generated.

4.2.2 Emptying the Silo

The program can empty the silo by performing consecutive move instructions from the RBUF to temporary storage. Each move instruction copies the bottom character in the silo so that it is not lost, and clears out the bottom of the silo, allowing the next character to move down for access by a following move instruction. The program can determine when it has emptied the silo by testing the Data Valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed by branching on the condition code following each move instruction. The test or bit test instruction must not access the RBUF because these instructions cause the next entry in the silo to move down without saving the current bottom character. Also, following a move from the RBUF, the next character in the silo is not available for at least one microsecond. Therefore, on fast CPUs, the program must use enough instructions or no-operation instructions to make sure that consecutive moves from the RBUF are separated by not less than one microsecond. This prevents a false indication of an empty silo.

4.2.3 Transmitting a Character

The program controls the DZQ11 transmitter through four registers on the Q-bus: the control and status register (CSR), the line parameter register (LPR), the transmit control register (TCR), and the transmit data register (TDR).

Following DZQ11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the TIE bit in the CSR if it wants the DZQ11 transmitter to interrupt the processor.

The TCR is used to enable and disable transmission on each line. One bit in this register is related to each line. The program can set and clear bits by using move, move byte, bit set, bit set byte, bit clear, and bit clear byte instructions. (If word instructions are used, the Line Enable bits and the DTR bits are accessed together.)

The DZQ11 transmitter is controlled by a scanner which is continuously looking for an enabled line (Line Enable bit set) which has an empty transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 2-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit allows the scanner to continue its search for lines needing service.

To start transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a move byte instruction. If the interrupts are to be used, a useful way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This occurs if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to RDY, to make sure that it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner in the end finds the line being started. If more than one line needs service, the scanner requests service in priority order as determined by line number. Line 3 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY. Because the transmitters are double buffered, a high-priority line may request two consecutive loads.

To terminate transmission on a line, the program loads the last character normally, and waits for the scanner to request an additional character for the line. The program clears the Line Enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data connection for any line is the one state. The Break (BRK) bits are used to apply a continuous zero signal to the line. One bit in the TDR is related to each line. The line stays in this condition as long as the bit stays set. The program should use a move byte instruction to access the BRK bits.

If the program continues to load characters for a line after setting the BRK bit, transmitter operation appears normal to the program regardless of the fact that no characters can be transmitted while the line is in the continuous zero-sending state. The program may use this facility for sending correctly timed zero signals by setting the BRK bit and using transmit ready interrupts as a timer. The program must also make sure that the line returns to the one state at the end of the zero-sending period before transmitting any additional data characters.

The following procedure does this. When the scanner requests service the first time after the program has loaded the last data character, because the lines are double buffered, the last data character has only started transmission. The program should therefore load an all zero character, and wait for the next service request while the last character is transmitted. When the scanner requests service the second time, the program should set the BRK bit for the line, and the zero character is overwritten. At the end of the zero-sending period, the program should load an all zero character to be transmitted. When the scanner requests service, indicating this character has started transmission, the program should clear the BRK bit and load the next data character.

4.2.4 Data Set Control

The program may sense the state of the Carrier and Ring Indicator signals for each modem and may control the state of the Data Terminal Ready signal to each modem. The program uses two registers to access the DZQ11 modem control logic. There are no hardware interlocks between the modem control logic and the receiver and transmitter logic. Any wanted sequence should be done under program control.

The Data Terminal Ready (DTR) bits in the TCR are read/write bits. Setting or clearing a bit in this register turns the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and Line Enable bits are accessed together.) The DTR bits are cleared by the INIT signal on the Q-bus but are not cleared if the program clears the DZQ11 by setting the CLR bit of the CSR.

The Carrier (CD) and Ring (RI) bits in the MSR are read-only bits. The program can determine the current state of the Carrier signal for a line by examining the appropriate bit in the high byte of the MSR. It can determine the current state of the Ring signal for a line by examining the appropriate bit in the low byte of the MSR. The program can examine these registers at different times by using move byte or bit test byte instructions, or can examine them as a single 16-bit register by using move word or bit test word instructions. The DZQ11 modem control logic does not interrupt the processor when a Carrier or Ring signal changes state. The program should regularly sample these registers to determine the current status. Sampling at a high rate is not necessary.

CHAPTER 5
TECHNICAL DESCRIPTION

5.1 SCOPE

This chapter describes the hardware in more detail, and explains the functional performance of the different circuit elements. It covers the host interface, the multiplexer itself, and the EIA line interface. Signal mnemonics used in this chapter are the same as those used in the field maintenance print set. The prefixes found in the print set, however, are not used here. These prefixes refer to the print sheet number on which a signal originates. For example, D6.DVALD H originates on sheet D6. The print set is useful, but not necessary for understanding this chapter.

Where possible, all figures in this chapter also refer to the sheet number of the field maintenance print set where the full schematic is to be found. An example of this is shown in Figure 5-1.

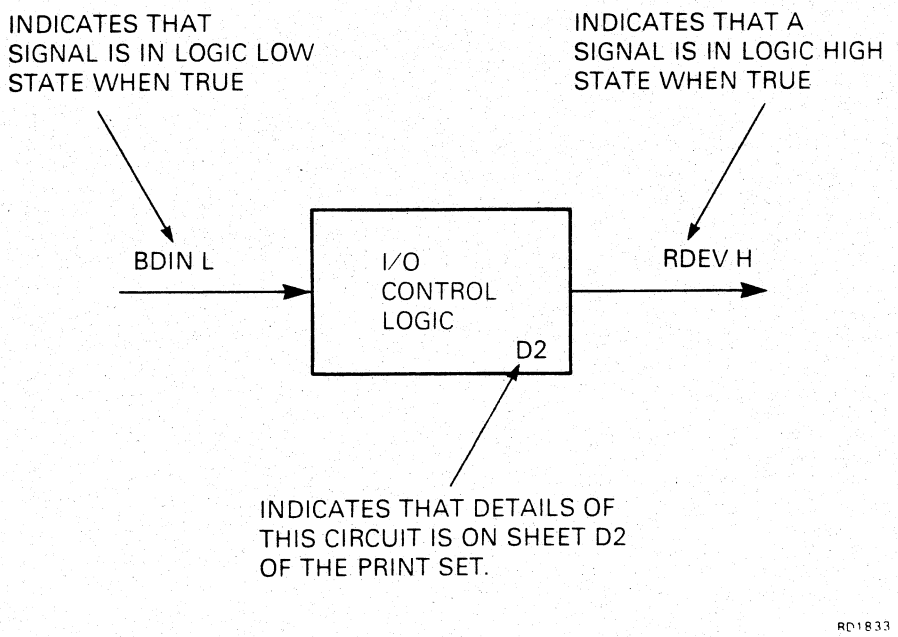


Figure 5-1 Labeling Conventions

Appendix A contains pin-for-pin descriptions of the LSI chips used in the DZQ11. and also the VLSI semi-custom IC (DC367B) which provides most of the functions of the DZQ11.

5.2 CIRCUIT FUNCTIONS

The major functional areas of the DZQ11 circuitry are represented in Figure 5-2. The numbers in the blocks refer to the sections in which the blocks are discussed.

Data to be transmitted on the communications lines moves from the Q-bus through the bus interface to the TDR in the UARTs. There it is converted from parallel to serial form, and sent to the EIA transmitters. These transmitters convert the serial data from TTL levels to EIA levels, and send it to the communications line (or modem). The interrupt logic requests service when a transmitter is empty. The transmitter control determines which of the four specified lines is to be used, indicates which line is selected via two CSR bits, and controls the loading of data.

Data coming from the communications lines is converted from EIA levels to TTL levels by the EIA receivers. It is then converted from serial format into parallel format by the UARTs. The parallel data leaves the UART receiver buffers and is stored in the silo buffer. From there it is transferred to the bus interface. The bus interface places the data on the Q-bus. The interrupt logic requests service when the silo buffer has either 1 or 16 characters of received data, as selected under program control. The receiver control scans the receiver status, and controls the loading and unloading of the silo.

The speed and format control generates clock signals for the UARTs. Under program control, it selects baud rate and stop bit, parity bit, and character-length parameters.

The break logic inhibits output data, so creating a BRK signal. The four lines operate independently and under program control.

The maintenance mode selector provides the facility to switch the data outputs to the data inputs. This is used to verify module operation.

The power supply converts voltages available on the Q-bus backplane to a negative 12 volts as needed by the module.

The different blocks shown in Figure 5-2 are described in more detail in the following sections.

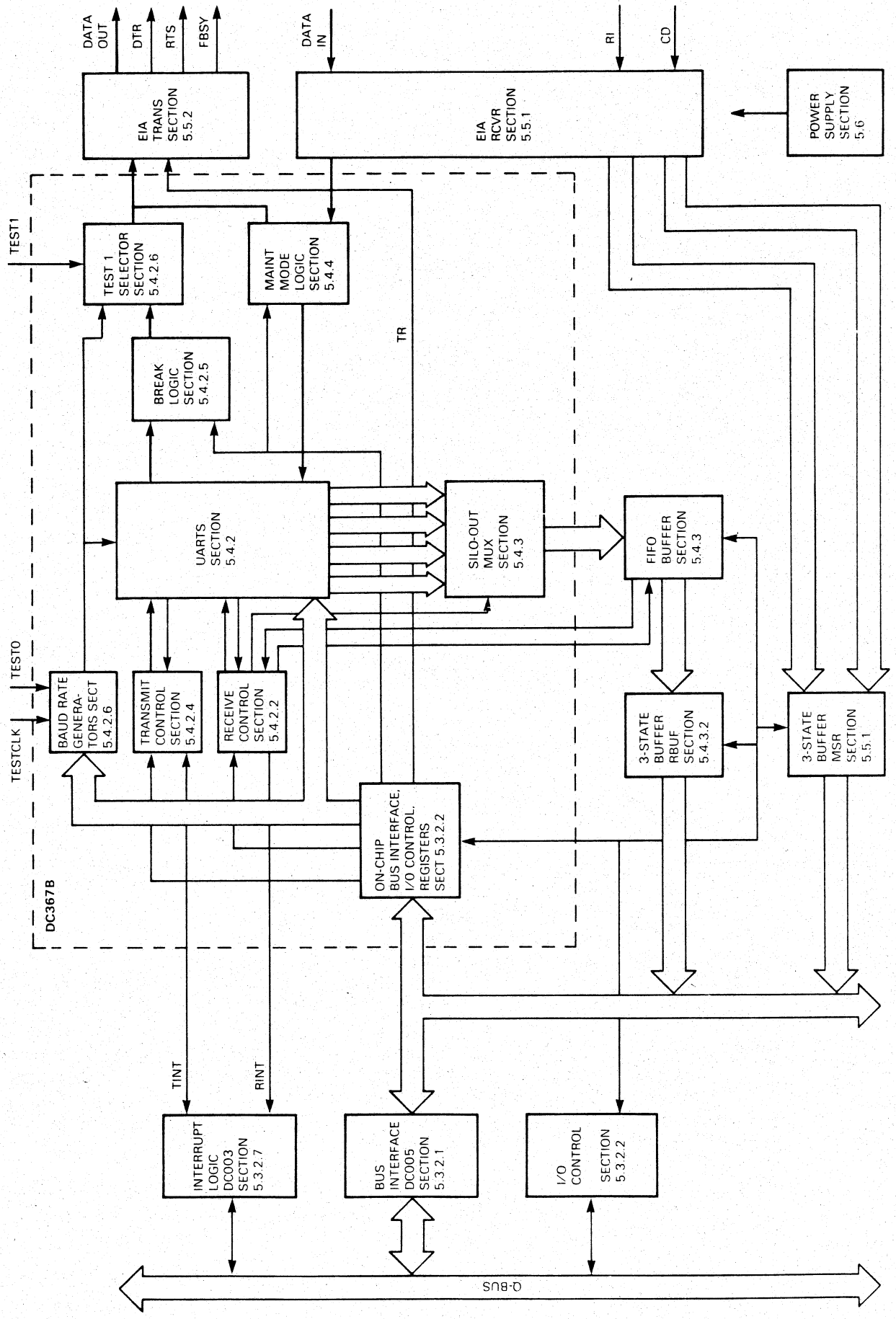


Figure 5-2 Simplified Functional Block Diagram

5.3 DZQ11 TO Q-BUS INTERFACE

5.3.1 Interface Signals

Figure 5-3 shows the signals that interface the DZQ11 to the Q-bus, and Table 5-1 defines these signals.

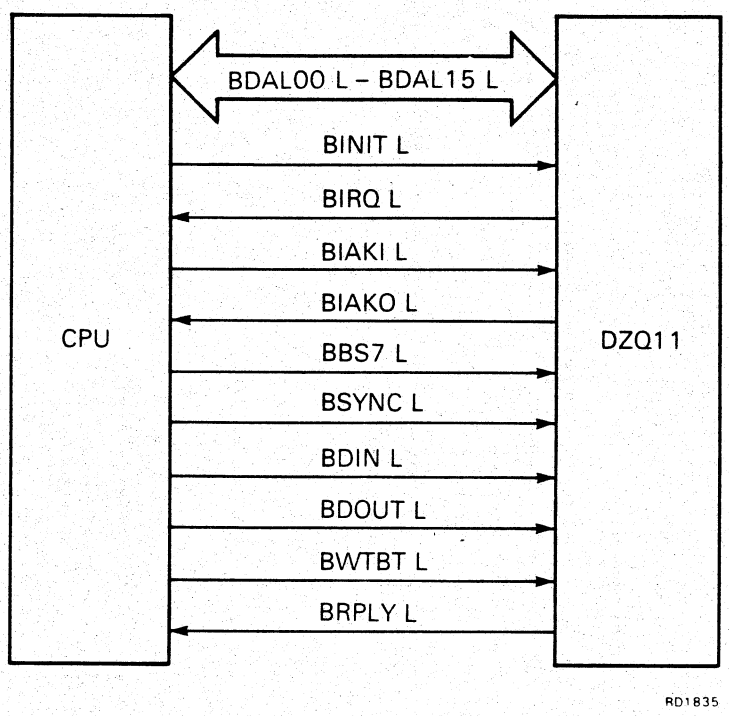


Figure 5-3 DZQ11/Q-bus Interface

Table 5-1 DZQ11/Q-bus Interface Signals

Mnemonic	Description
BINIT L	INITIALIZE – BINIT L is asserted by the processor to initialize or clear all devices connected to the I/O bus. This signal is generated on power-up.
BIRQ L	Interrupt Request – A device asserts this signal when its interrupt-enable and interrupt-request flip-flops are set. If the processor status word PSW<7> is 0, the processor acknowledges the request in response by asserting BDIN L and BIAKO L.
BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output – Interrupt acknowledge signal generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L which is routed to the BIAKI L pin of the first device on the bus. If the device is not asserting BIRQ L, it passes BIAKI L to the next lower priority device in the chain via its BIAKO L pin. Otherwise its BIAKO L output is inhibited.
BBS7 L	Bank 7 Select – The CPU asserts BBS7 L when an address in the upper 4K-word bank of Q-bus address space is placed on the bus. BSYNC L then becomes asserted and BBS7 L stays active for the duration of the addressing cycle.
BSYNC L	Synchronize – BSYNC L is asserted by the CPU to indicate that it has placed an address on BDAL00 1 to BDAL15 L. BSYNC L stays asserted until the transfer is complete.

Table 5-1 DQZ11/Q-bus Interface Signals (Cont)

Mnemonic	Description
BDIN L	Data Input – BDIN L is used for two types of bus operations. 1. When asserted during BSYNC L time, BDIN L indicates an input transfer, and requires a response (BRPLY L). BDIN L is asserted when the CPU is ready to accept data from the DZQ11. 2. When asserted without BSYNC L, BDIN L indicates that an interrupt operation is in progress.
BDOUT L	Data Output – When asserted, BDOUT L indicates that valid data is available on BDAL00 L to BDAL15 L, and that an output transfer is in progress. BDOUT L is deskewed with respect to data on the bus. The DZQ11 must assert BRPLY L to complete the transfer.
BWTBT L	Write/Byte – BWTBT L is used in two ways to control a bus cycle. 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), instead of an input sequence. 2. It is asserted during BDOUT L, in a DATOB cycle, for byte addressing.
BRPLY L	Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during interrupt-acknowledge transactions. It is generated by the DZQ11 to indicate that it has placed its data on the BDAL bus, or that it has accepted output from the bus.
BDAL00 L to BDAL15 L	Data/Address Lines – These lines are the bidirectional bus. First, the CPU places address information on the bus, then, after the needed device has been addressed, the CPU removes the address. Then data is placed on the bus, either by the CPU for an output transfer, or by the DZQ11 for an input transfer.

Transactions between the CPU and the DZQ11 can be program-initiated or interrupt-driven.

An input operation (DATI) is equivalent to a read operation, and an output (DATO) operation is equivalent to a write. A DATOB writes a byte. A DATIO cycle is equivalent to a read-modify-write cycle. First an addressing operation is executed, followed by an input word transfer, in a way similar to the DATI cycle. However, BSYNC L stays in the active state after completing the input data transfer. This causes the addressed device to stay selected. An output data transfer then follows without any addressing. After the completion of the output transfer, the device terminates BSYNC L, completing the DATIO cycle. The output part of this cycle can be a byte transfer. This is a DATIOB.

5.3.2 Circuit Operation

5.3.2.1 Bus Interface – Data and control signals move between the Q-bus and the DZQ11 transmit and receive circuitry through a group of bus transceivers, multiplexers, and latches.

The bus transceivers are made up of four DC005 transceiver chips. These buffer the bus signals BDAL00 to BDAL15 to the device internal data bus lines 00 to 15. The device data lines have three logical states: TTL low, TTL high, and disabled (high impedance).

The DC005 transceiver chips also decode the address and generate the vector. The address is decoded by comparing the state of BDAL03 to BDAL12 with the state of address switches A03 to A12 (switches 1 to 10 on switchpack E28). When a CPU addresses an I/O device, it asserts BBS7 L (bank select 7) during address time. This indicates that the address is in the top 4K words of addressing space, and enables the DC005 transceivers to decode that address. If the address matches the switch selection, the transceivers assert MATCH H to the I/O control logic.

During data time, the transceivers transfer data from the Q-bus to the device data bus lines, if the operation is a data output transfer. If the operation is a data input transfer, the I/O control logic asserts READ L and RDEV H. This switches the transceivers into their opposite direction, where they transfer data from the device data bus to the Q-bus.

Switches V03 to V08 (switches 1 to 6 on switchpack E13) control the generation of vector addresses. The switches control the state of the vector bits 03 to 08 at the time when the interrupt logic enables vector generation. Bit 02, however, is automatically controlled by the interrupt logic, and indicates whether a transmitter or a receiver interrupt is in progress. It is set for a transmitter interrupt, and clear for a receiver interrupt.

When an interrupt occurs, the logic state of the vector switches is placed on the Q-bus lines. The transceivers do this without the need of READ L or RDEV H from the I/O control circuit.

5.3.2.2 I/O Control – This logic controls the flow of status and data bits between the Q-bus and the device registers. It monitors the three least-significant bits of the address word to determine which register is to be read or loaded, and which byte in the register is affected. It monitors BWTBT L (Write Byte) to determine if a byte or a word is being loaded. The CPU can write words or bytes, but reads only words. Control signals BDIN L and BDOUT L indicate whether data is to be moved into the CPU, or out of it.

The major element in the I/O control circuit is a DC004 protocol chip (Figure 5-2). The chip uses bits 01 and 02 of the device data bus to decode the device register address. It then asserts one of the four register select lines. It uses device data bus bit 00 and BWTBT L to select either OUTHB L for a high byte, or OUTLB L for a low byte.

If the operation is an output data transfer (indicated by BDOUT L), circuitry external to the DC367B uses the register-select signals (SEL0 L to SEL6 L) together with:

- OUTLB L to produce load pulse WRLB H
- OUTHB L to produce load pulse WRHB H
- OUTLB L and OUTHB L to produce both load pulses.

This circuitry also encodes the register-select signals to produce RGA and RGB. These signals (WRLB H, WRHB H, RGB and RGA) are connected to the DC367B chip and enable the appropriate byte or bytes of the device data bus to be loaded into the selected register inside the DC367B chip. Table 5-2 shows the register selection.

Table 5-2 Register Selection

DC004 SEL Line (Active Low)						
0	**2**	**4**	**6**	**RGA**	**RGB**	**Selected Register**
L	H	H	H	L	L	CSR
H	L	H	H	H	L	RBUF/LPAR
H	H	L	H	L	H	TCR
H	H	H	L	H	H	MSR/TDR

The DC004 chip is designed to connect directly to the Q-bus, and to decode active LOW signals at the BDAL00 to BDAL02 inputs. In the DZQ11, however, these input pins are connected to the buffered (and inverted) device data bus lines DAL0 to DAL2, to reduce Q-bus loading. Therefore, the decoded outputs SEL0 to SEL6 have their order reversed. So pin 17 of the DC004 is now SEL0 L instead of being SEL6 L, and pin 14 is SEL6 L instead of being SEL0 L, and the same for pins 15 and 16. In the same way OUTLB L and OUTHB L pins are reversed. Pin assignments shown in Appendix A for the DC004 are the standard designated assignments.

The circuitry external to the DC367B also generates two signals named WRCSRLB H and WRCSRHB H. These are used to write interrupt-enable bits into the DC003 chip. These bits are also copied in the DC367B chip via the RGA RGB decoding process, and are available for read-back purposes. WRCSRLB L is also used together with DAL4 (CSR bit 4) to generate Master Clear MCLR L and MCLR H.

If the operation is an input transfer, indicated by BDIN L, the register-select lines are also used to load data from the device data bus to the Q-bus. The I/O control generates a load pulse appropriate to the correct register, and asserts READ L and RDEV H. RDEV H causes the DC367B chip to place the data from the selected register on the device data bus (Table 5-3). RDEV H and READ L together enable the bus transceivers to transfer the data from the device data bus to the Q-bus (Table 5-4). All those bits shown as 'Not Used' in Figure 3-1 are held at zero by the DC367B logic.

Table 5-3 Transceiver Switching

READ L	RDEV H	Mode
H	L	Q-bus to device data bus
H	H	Does not occur
L	L	Q-bus disconnected/device data bus open
L	H	Device data bus to Q-bus

5.3.2.3 Input Operation – An input data transfer (DATI bus cycle) proceeds as follows.

1. The CPU places the device address on Q-bus lines BDAL00 L to BDAL15 L, and asserts BBS7 L. BWTBT L is negated at this time because all input transfers are full words. (Figure 5-4).

2. The bus transceivers are configured to receive from the Q-bus unless switched otherwise. BBS7 L enables the transceivers to decode the address and to assert MATCH H, which enables the I/O control circuit.

3. The CPU asserts BSYNC L. The leading edge of BSYNC L latches the states of MATCH H and device data bus bits 00 to 02 into the protocol chip. These are decoded to produce SEL0 L to SEL6 L.

4. Next, the CPU removes the address from the Q-bus lines, negates BBS7 L, and asserts BDIN L. BDIN L causes the I/O control to generate READ L and RDEV H. These signals place the contents of the selected register on to the device data bus and the Q-bus. BDIN L also generates BRPLY L. This indicates to the computer that the data is on the bus.

5. The computer reads in the data, and then negates BDIN L.

6. The I/O control logic responds to the negation of BDIN L by negating BRPLY L.

7. The CPU terminates the bus cycle by negating BSYNC L.

8. When BSYNC L becomes negated, the protocol chip releases the register selection lines and the READ L and RDEV H signals. The bus interface returns to its normal condition of receiving from the Q-bus and transmitting to the device data bus.

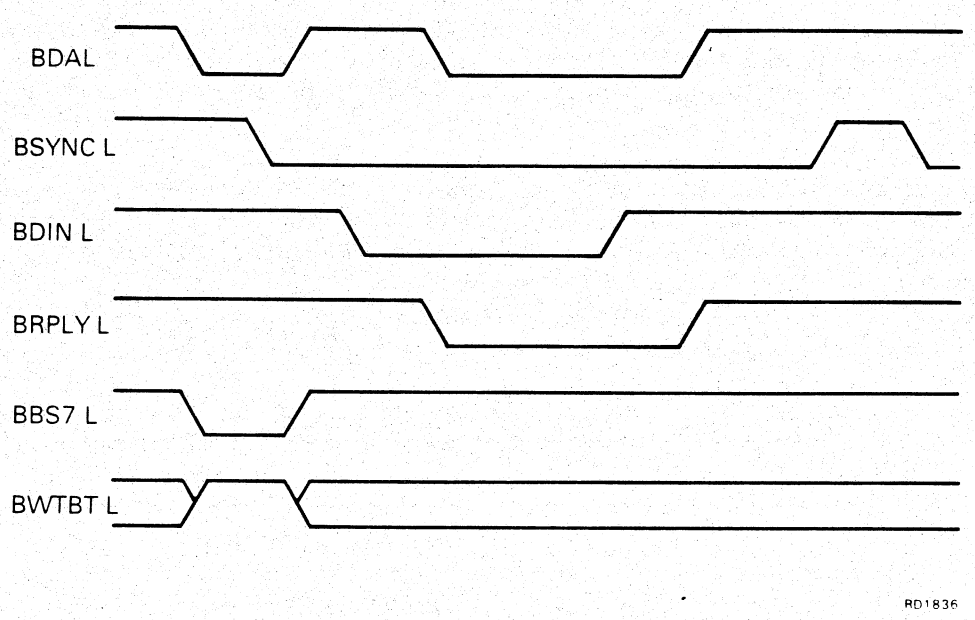


Figure 5-4 Data Input Timing

5.3.2.4 Output Operation – The DZQ11 can accept data from the computer in either bytes or words. To write a word out to the device module, the CPU performs a DATO bus cycle. To write a byte, it performs a DATOB bus cycle (Figure 5-5). An output data transfer proceeds as follows.

1. The CPU places the device address on the Q-bus and asserts BBS7 L and BWTBT L. (During address time, BWTBT L is asserted for an output operation and negated for an input operation.) BBS7 L enables the bus interface to decode the address and assert MATCH H to the I/O control. The bus interface also applies address bits 00 to 02 to the I/O control.

2. The CPU asserts BSYNC L. The leading edge of BSYNC L latches the states of MATCH H and bits 00 to 02 into the DC004 protocol chip. If MATCH H is asserted, the chip decodes the register address and asserts the appropriate select line.

3. The CPU removes the address from the bus lines and negates BBS7 L. If a byte is to be transferred, BWTBT L stays asserted. If a word is to be transferred, BWTBT L is negated.

4. At this time, the CPU asserts BDOUT L, which allows the DC004 protocol chip to decode the states of BWTBT L and the latched-in address bit 00. The DC004 uses the signals to assert either OUTHB L or OUTLB L, or both, for word transfers (Table 5-4). These signals are used with SEL0 L to SEL6 L to write to the appropriate registers.

5. After the DC004 chip receives BDOUT L, it initiates the Bus Reply signal.

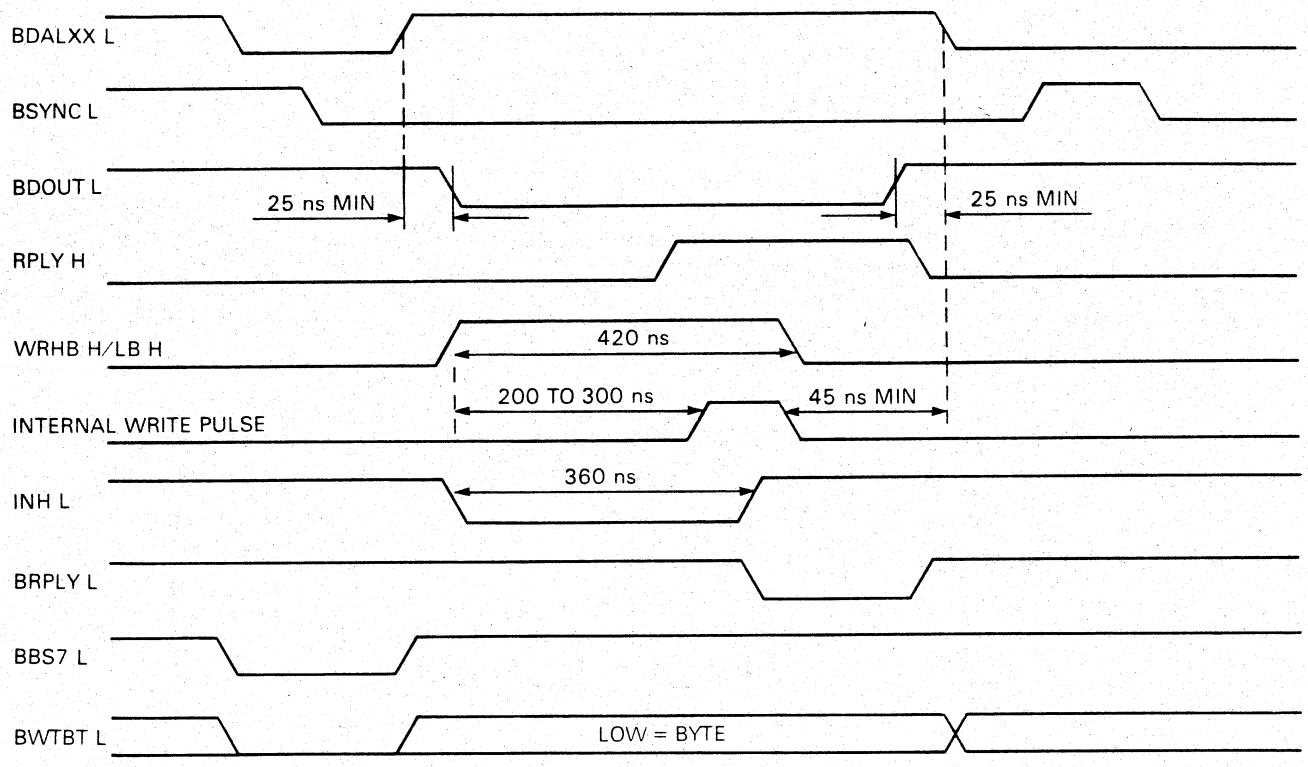


Figure 5-5 Data Output Timing

6. Next, the CPU removes the data from the bus lines and negates BDOUT L.
7. The DC004 chip responds to this by negating BRPLY L.
8. The CPU then terminates the bus cycle by negating BSYNC L and, if applicable, BWTBT L.
9. When BSYNC L is negated, the DC004 chip negates the register select and byte lines.

Table 5-4 Byte Selection (Output Operation Only)

BWTBT L	Internal DAL00	Signals Asserted	Bytes Selected
H	X	OUTLB L and OUTHB L	Both
L	L	OUTLB L	Low
L	H	OUTHB L	High

5.3.2.5 Vector Operation – The I/O control has the additional function of asserting BRPLY L in response to VTB H from the interrupt control circuit. This action is part of the interrupt sequence, and is independent of the BSYNC L and MATCH H. It is discussed in Section 5.3.2.8.

5.3.2.6 Initialize Circuit – External to the DC367B, a write to CSR<4> starts a 2.4 microsecond one-shot which asserts MCLR L (Master Clear) for the DC367B, and also clears the DC003 chip. The Q-bus BINIT L signal also clears the DC003 chip and generates MDMC L (Modem Clear) for the DC367B.

MDMC L is connected to pin 8 of the DC367B chip and directly clears the modem register bits (that is, DTR 0 to 3); MCLR L, connected to pin 7, has no effect on these. Thereafter, both clears are ORed inside the DC367B and synchronized to the system clock to provide a MASTER CLEAR signal for CSR<4> read-back purposes. The resulting read-back pulse is about 2.7 microseconds long (that is, about 300 nanoseconds longer than the original). When this clears itself, initialization is complete on the DZQ11. Figure 5-6 shows details of these signals.

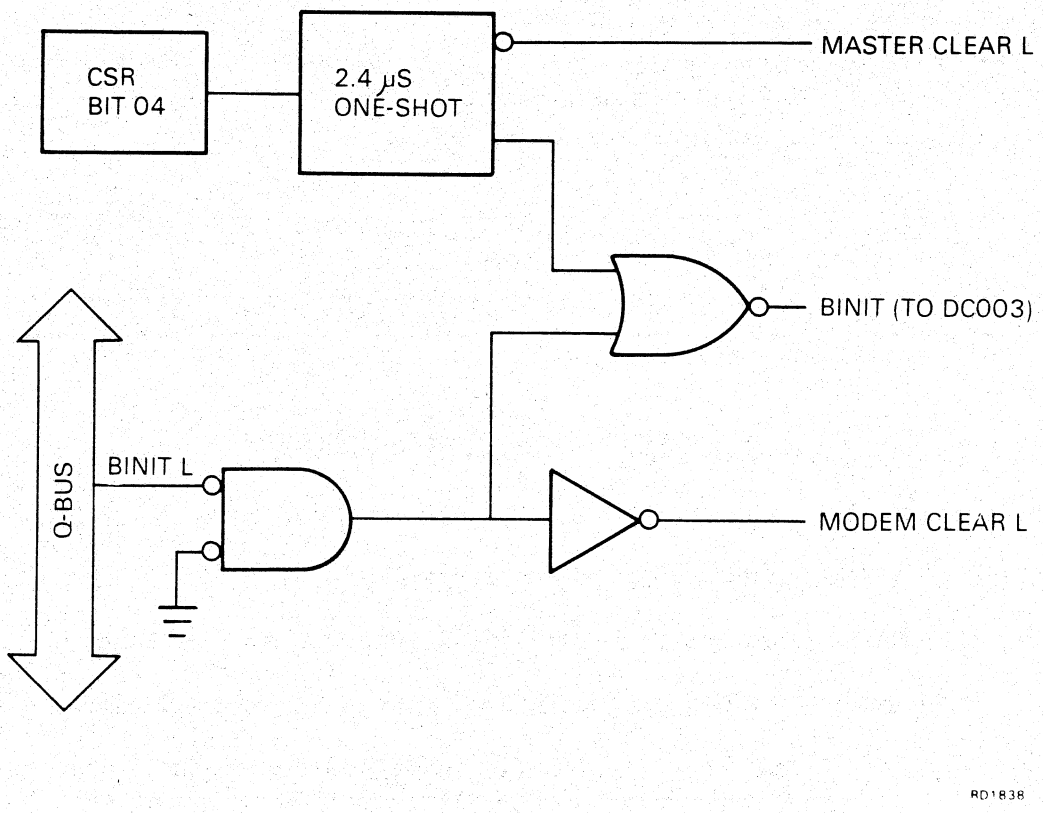


Figure 5-6 Initialization Signals

5.3.2.7 Interrupt Logic – Most of the logic for interrupts is contained in the DC003 interrupt chip (Figure 5-7). The DC003 chip contains two interrupt channels, one for receiver interrupts and one for transmitter interrupts. The circuit generates a receiver interrupt either when the RBUF has 1 character ready for the computer (Receiver Done interrupt), or when the silo buffer has 16 characters ready (Silo Alarm interrupt).

The Receiver Done interrupt is enabled by bit 06 of the CSR. The Silo Alarm interrupt is enabled by setting bit 12. Setting bit 12, however, inhibits the Receiver Done signal from the RBUF. Therefore, Receiver Done interrupts do not occur when Silo Alarm interrupts are enabled.

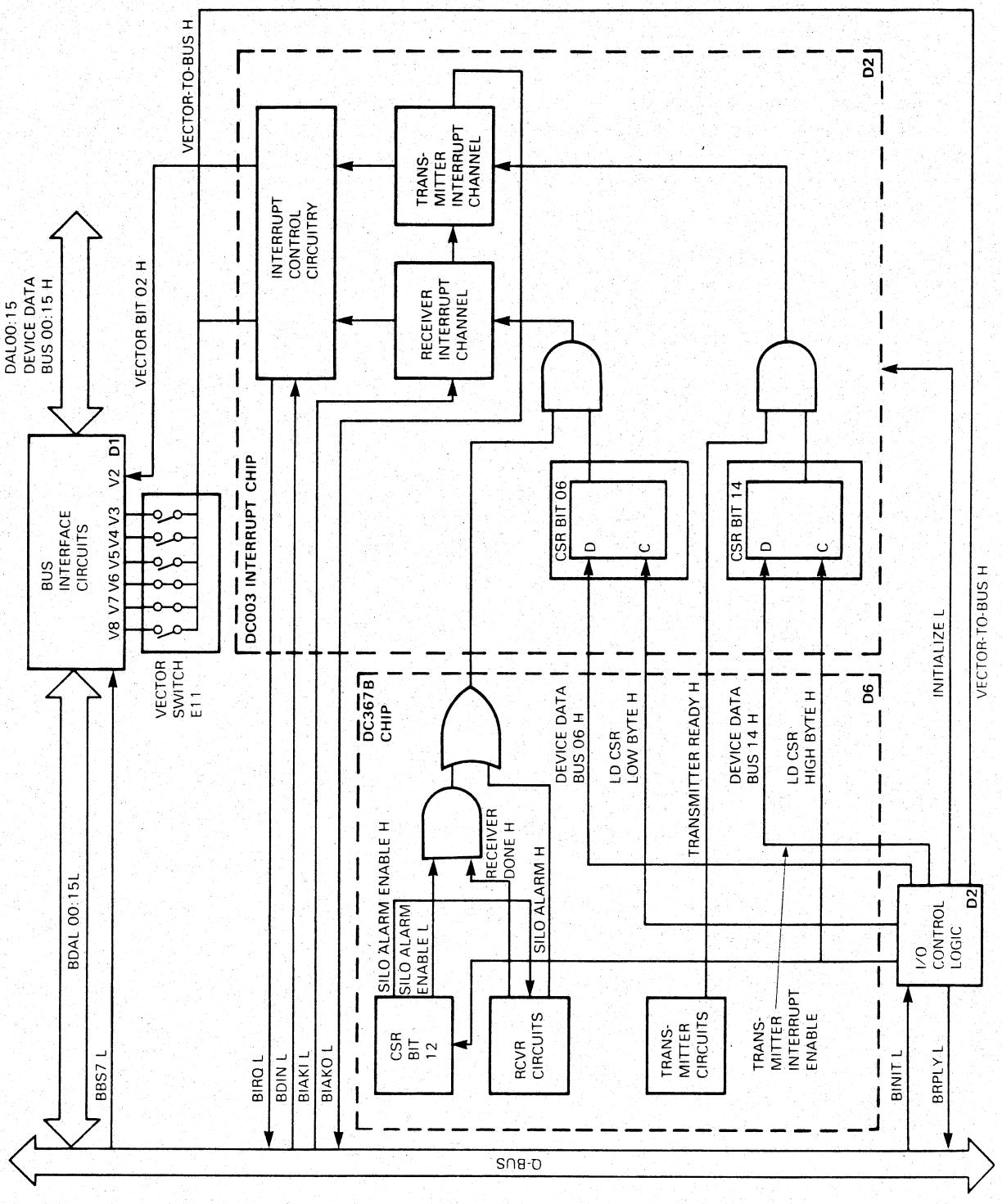


Figure 5-7 Interrupt Logic

The circuit generates a transmitter interrupt when a TDR is empty and ready to accept another data output from the computer. The Transmitter Ready interrupt is enabled by setting CSR bit 14.

Both the Transmitter Interrupt Enable (TIE) and the Receiver Interrupt Enable (RIE) bits are located physically in the DC003 interrupt chip, although they are functionally part of the CSR. Also, for read-back purposes, they are duplicated in the DC367B chip.

The Q-bus Interrupt Acknowledge signal (BIAKI L/BIAKO L) is daisy-chained through the devices on the Q-bus. Device priority is fixed by the position of the device in the Interrupt Acknowledge daisy chain. In the DZQ11 interrupt logic, this chain goes through both the receiver section and the transmitter section of the DC003 chip. It passes through the receiver section first, thereby giving receiver interrupts priority over transmitter interrupts.

5.3.2.8 Interrupt Transactions – When interrupts are enabled and a condition occurs which needs service, the interrupt sequence proceeds as follows.

1. The interrupt logic asserts BIRQ L, the interrupt request line (Figure 5-8).

2. The CPU responds to BIRQ L by asserting BDIN L and then BIAKI L. BIAK is the bussed Interrupt Acknowledge signal. It is passed down the priority chain until it reaches that section of the interrupt chip which initiated the request.

3. When the interrupt logic receives both BDIN L and BIAKI L, it asserts VTB H ('vector to bus') to the vector selection switches. If the interrupt is a transmitter interrupt, the circuit also asserts VBIT2 H. This signal adds four to the base (receiver interrupt) vector that is asserted by VTB H. The circuit also negates BIRQ L.

4. VTB H causes the I/O control logic to issue BRPLY L to the CPU. VTB H causes the bus transceivers to place the selected vector on the Q-bus lines.

5. The computer reads in the interrupt vector, and as a result of receiving BRPLY L, it then negates BDIN L. Shortly after this, it also negates BIAKI L.

6. The interrupt logic negates VTB H and VBIT2 H, if applicable.

7. The negation of VTB H causes the I/O control logic to negate BRPLY L, and the bus transceivers to remove the vector from the Q-bus lines.

An interrupt transaction does not need BBS7 L, MATCH H, BSYNC L, or READ L. The interrupt logic overrides the normal I/O protocol.

A Silo Alarm can be identified from a Receiver Done interrupt by checking the Silo Alarm Enable (SAE) bit (CSR bit 12) when entering a service routine.

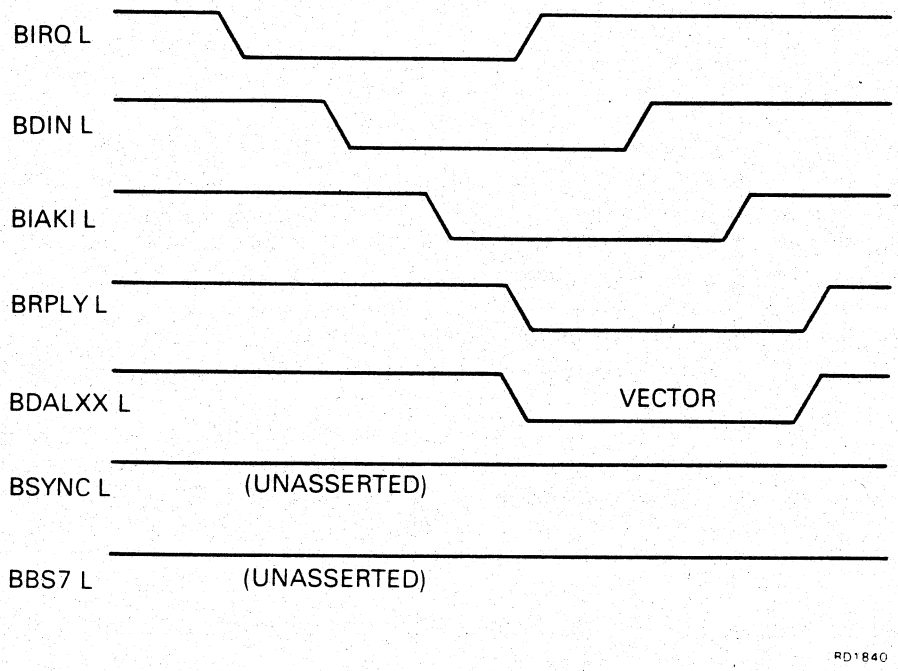


Figure 5-8 Interrupt Timing

5.4 LINE MULTIPLEXER

5.4.1 Hardware Description

All four UARTs, the baud-rate generators, and the control logic are integrated within the DC367B. This is a semi-custom IC contained in a 68-pin plastic leaded chip carrier (PLCC). The Receiver FIFOs are external to the DC367B.

5.4.2 UARTs and Control

5.4.2.1 Receiver Operation – The UART (Universal Asynchronous Receiver/Transmitter) receiver section does the serial-to-parallel assembly of received characters for each line. It also does parity checking, break detection, and overrun detection. Each UART is double buffered, allowing a full character-time to remove the received character to a hardware buffer.

The UARTs are serviced by a sample-and-hold search-priority circuit. Sampling priority of the data-available flags is highest for line 3 and lowest for line 0. Sample and hold times are separated by 100 ns to allow for Priority Selection settling times. When a flag is found, the control logic deposits the character into a 16 x 64 First-In-First-Out (FIFO) buffer.

Serial data coming in is applied to the receiver section of the selected UART, which samples the serial input at the receiver clock rate (16 times the data bit rate). A line is in a continuous marking state when idle. When a start bit arrives, the UART detects the mark-to-space transition. It samples the line again at the time corresponding to the middle of the start bit. If the line is marking, the UART logic assumes that the first sample was noise and continues sampling. If it finds that the line is still spacing, however, the logic assumes it is receiving a start bit, and enters data-entry mode.

In data-entry mode, the UART clocks data bits sequentially into the appropriate bits of the receiving register. If parity has been enabled, the UART checks the total of the received data bits plus the parity bit. (It checks for an even total if even parity has been selected, and an odd total if odd parity has been selected.) A parity error causes the UART to set the parity-error-flag bit in the high byte of the RBUF word.

The UART checks to see if the line is marking at the stop-bit time. If it is marking, the UART logic assumes there is a valid stop bit. If the line is spacing instead, the UART sets the framing-error-flag bit.

About half way through the stop bit time, the UART transfers the received character, the parity-error bit, and the framing-error bit, from the receiving register to the holding register. At the same time, it asserts the Data Available signal to the receiver control logic. If the previous character has not yet been serviced by the receiver control logic, the UART sets the overrun-error-flag bit to indicate that the previous character was lost. It can only be recovered by retransmission.

The receiver control loads the contents of the RBUF (data and status) into the FIFO buffer for transfer to the computer. The receiver control circuit determines when and what type of receiver interrupt to request.

5.4.2.2 Receiver Control – Figure 5-9 shows a block diagram of the receiver control section of the DC367B chip. The function of the control section is to scan the UART status and place UART data together with the line number and error information in the silo buffer. At the same time, it also indicates receiver control status (RDONE and SILO ALARM) to the CPU via the CSR, and, if enabled, receiver interrupt.

The scanning logic is similar to that of the Transmit control logic – it works on a priority basis. Line 3 has the highest priority, and line 0 the lowest.

The following table (Table 5-5) shows the pins of the DC367B chip that are associated with the receiver control function.

Table 5-5 DC367B Receiver Control Signals

Pin	Signal	Description
36	FE3 H	Framing Error Line 3 Output
37	DVALD H	Data Valid Output
38	RINT H	Receiver Interrupt Output
40	SHI23 H	Shift In Pulse 2nd Byte Output
41 to 42	SLD7 H SLD6 H	to Silo Data Bit 7 and Bit 6 Output
45 to 50	SLD5 H SLD0 H	to Silo Data Bit 5 to Bit 0 Output
51	SHI01 H	Shift In Pulse 1st Byte Output
53	IRDY H	In Ready Input
54	ORDY H	Out Ready Input
64	SLCLR L	Silo Clear Output

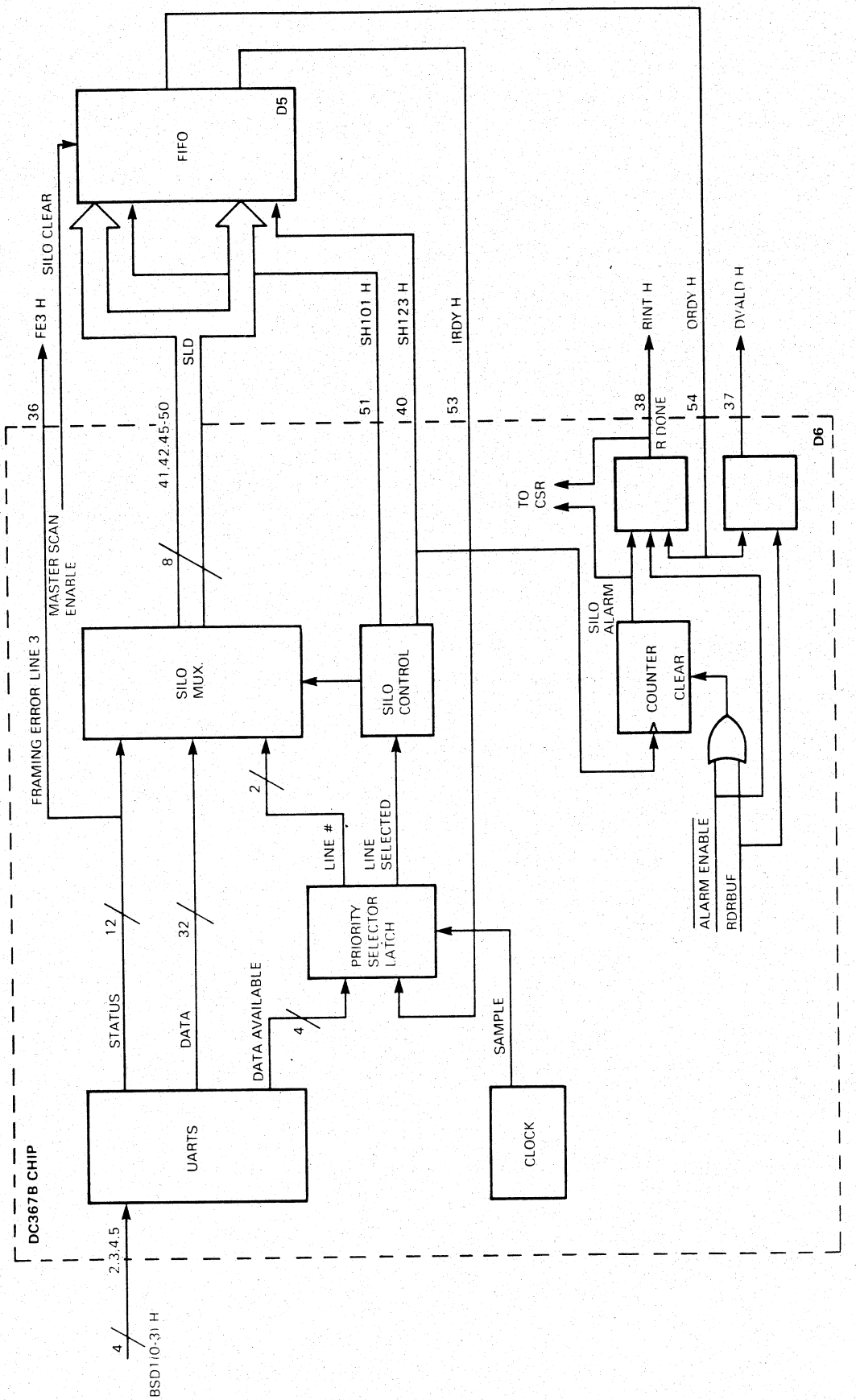


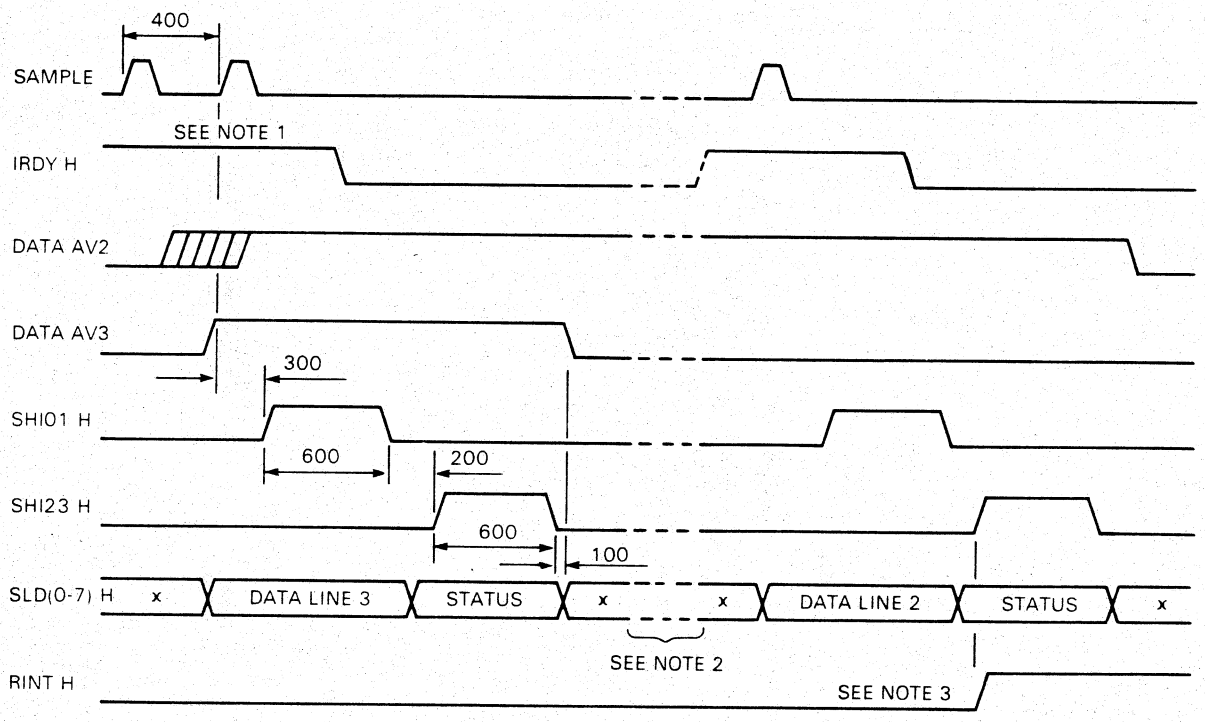
Figure 5-9 Receiver Control Block Diagram

A sample pulse is generated every 400 ns in the DC367B, from an internal clock. The sample pulse strobes the highest-priority active UART which has an assembled character. A shift (SHI01 H) pulse is generated 300 ns after the sample pulse, as long as IRDY is High (the FIFO is not full). SHI01 H can occur as early as 300 ns after the character is assembled, or as late as 700 ns after, because the received character is not synchronized with the internal clock. The SHI01 H pulse loads the data into the FIFO.

The second shift pulse (SHI23 H) is generated 800 ns after the leading edge of SHI01 H. This second pulse loads the status information into the FIFO.

The FIFO buffer is made up of 4-bit-wide chips. Data loaded into each chip starts to 'bubble down' as soon as it is loaded. The FIFO is 16-bits wide; two chips (E10 and E30) are loaded by SHI01 H, and another two (E4 and E17) by SHI23 H. The contents continue to 'bubble down' after the second shift pulse (SHI23). During this time, the chips hold IRDY low and prevent the next UART from being sampled. The worst-case 'bubble-down' time is about 2.0 microseconds, after which IRDY again goes high. Figure 5-10 shows the timing relationship between these signals.

The FIFO buffer is cleared of all data by the signal SLCLR L. The buffer becomes empty, and provides space for 64 characters; IRDY H becomes asserted and ORDY H is cleared. The signal SLCLR L is generated by the register latch which corresponds to the Master Scan Enable bit of the CSR (CSR<05>). So long as CSR<05> stays clear, the FIFO buffer is disabled in the clear condition. Therefore CSR<05> must be set to allow Receive and Transmit control operation. It is automatically cleared by Master Clear and by BINIT L.



NOTE 1. ASSUME LINE 0 AND 1 DISABLED. LINE 3 HAS PRIORITY.
NOTE 2. FIFO "BUBBLE-DOWN" TIME MAY BE UP TO 2.0 MICROSECONDS.
NOTE 3. ASSUME 16TH CHARACTER, AND SILO ALARM ENABLED.

Figure 5-10 Receiver Control Timing Diagram

5.4.2.3 Transmitter Operation – During idle time, the UART transmits a continuous marking signal and holds the Transmitter Ready signal asserted. The transmitter control circuitry uses this signal to determine when to initiate a transmitter interrupt request.

When the computer has data to transmit to a communications line, it uses a DATO or DATOB sequence to address the Transmit Data Register (TDR) and to place the data on the bus lines. The low byte of the TDR word is loaded into the holding register in one of the four UARTs internal to the DC367B.

When the data enters the holding register, the next DC367B internal clock transfers the data – in parallel – from the holding register to a transmitting register. It then produces a start bit, followed sequentially by the data bits from the transmitting register, least-significant bit first. The data bits may be followed by the parity bit, depending on the LPR setting, and then the stop bit(s). These bits are fed via the break/test select logic to the EIA level converters.

The transmitter, like the receiver, is double buffered. Therefore it can be loaded with a second character before the first character has been moved out – so giving continuous transmission.

5.4.2.4 Transmitter Control – The transmitter control circuit checks the transmitter control register (TCR) to determine which lines are enabled. It checks the UARTs to determine which are ready to accept new data for transmission. It also enables the loading of data from the CPU to the highest-priority UART. Table 5-6 shows the pins of the DC367B chip that are associated with the transmitter control function.

Table 5-6 DC367B Transmitter Control Signals

Pin	Signal	Description
32	WRHB H	Write High Byte Input
33	WRLB H	Write Low Byte Input
30	RGB	Select 4 or 6 Input
31	RGA	Select 2 or 6 Input
39	TINT H	Transmitter Interrupt Output
59 to 60	BDTRL0 L BDTRL1 L	Data Terminal Ready Output Line 0 and 1
62 to 63	BDTRL2 L BDTRL3 L	Data Terminal Ready Output Line 2 and 3
65 to 68	BSDO0 H to BSDO3 H	Serial Data Out Output Line 0 to Line 3

Figure 5-11 shows a block diagram of the transmitter control section of the DC367B chip.

An internal clock periodically samples the state of the four Tx Ready lines of the UARTs. This sample, together with the LINE ENABLEs (from the TCR), is applied to a priority selector. This selector chooses the highest-priority line which is both ready and enabled. Any output from the priority selector sets bit 15 in the CSR, and asserts TINT pin 39, which is connected to the DC003 Interrupt chip. This indicates to the CPU that service is needed.

While the CPU is responding to this service request, a UART of a higher-priority line may also become Ready. In order to prevent the priority selector from changing its output before the completion of the service already in progress, the sampling clock is disabled as soon as an output first appears from the priority selector. The sampling clock stays disabled until the service routine loads a new character to the waiting UART transmitter.

The output from the priority selector also gates the load pulse so as to direct the data from the device data bus into that UART which is waiting for service.

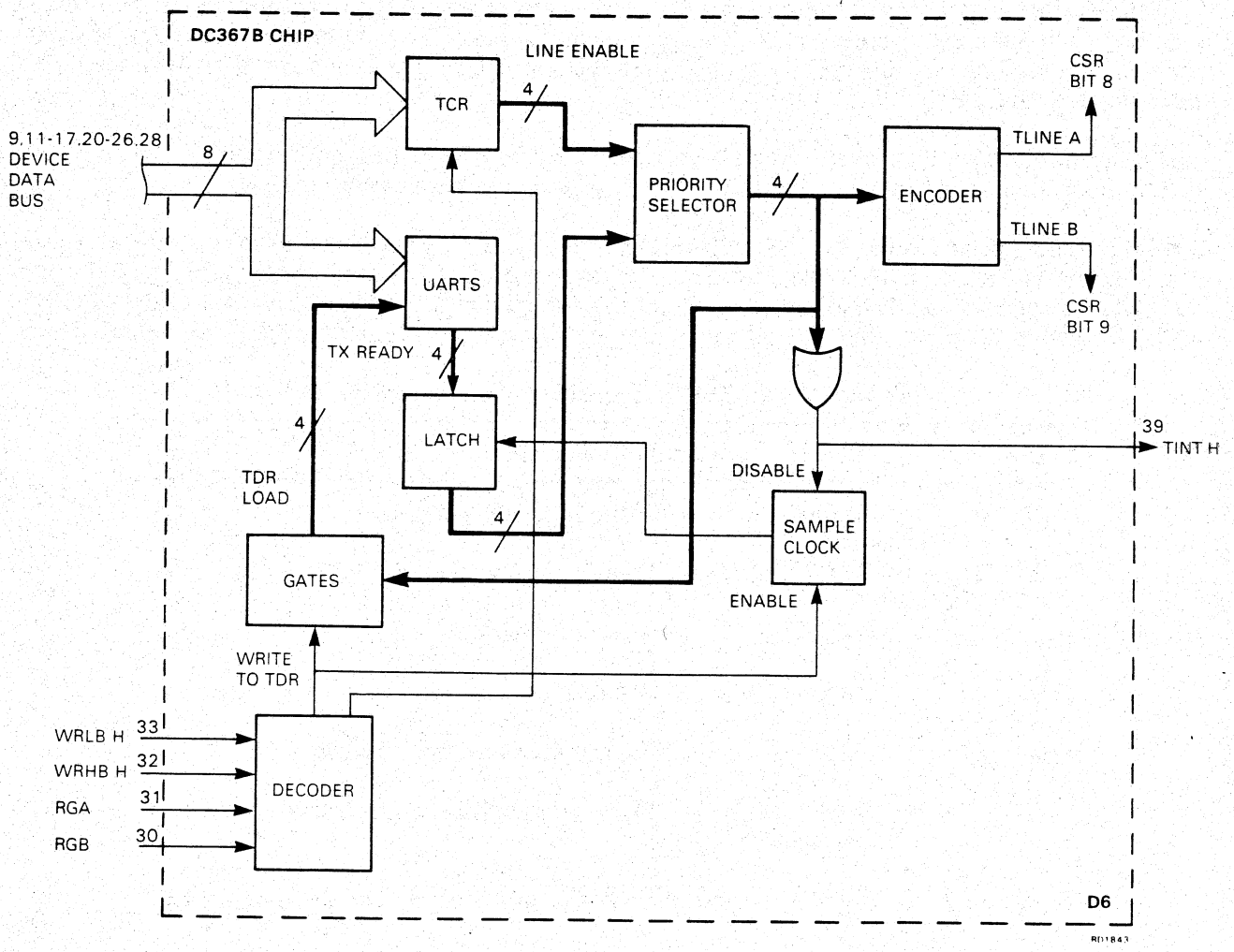


Figure 5-11 Transmitter-Control Block Diagram

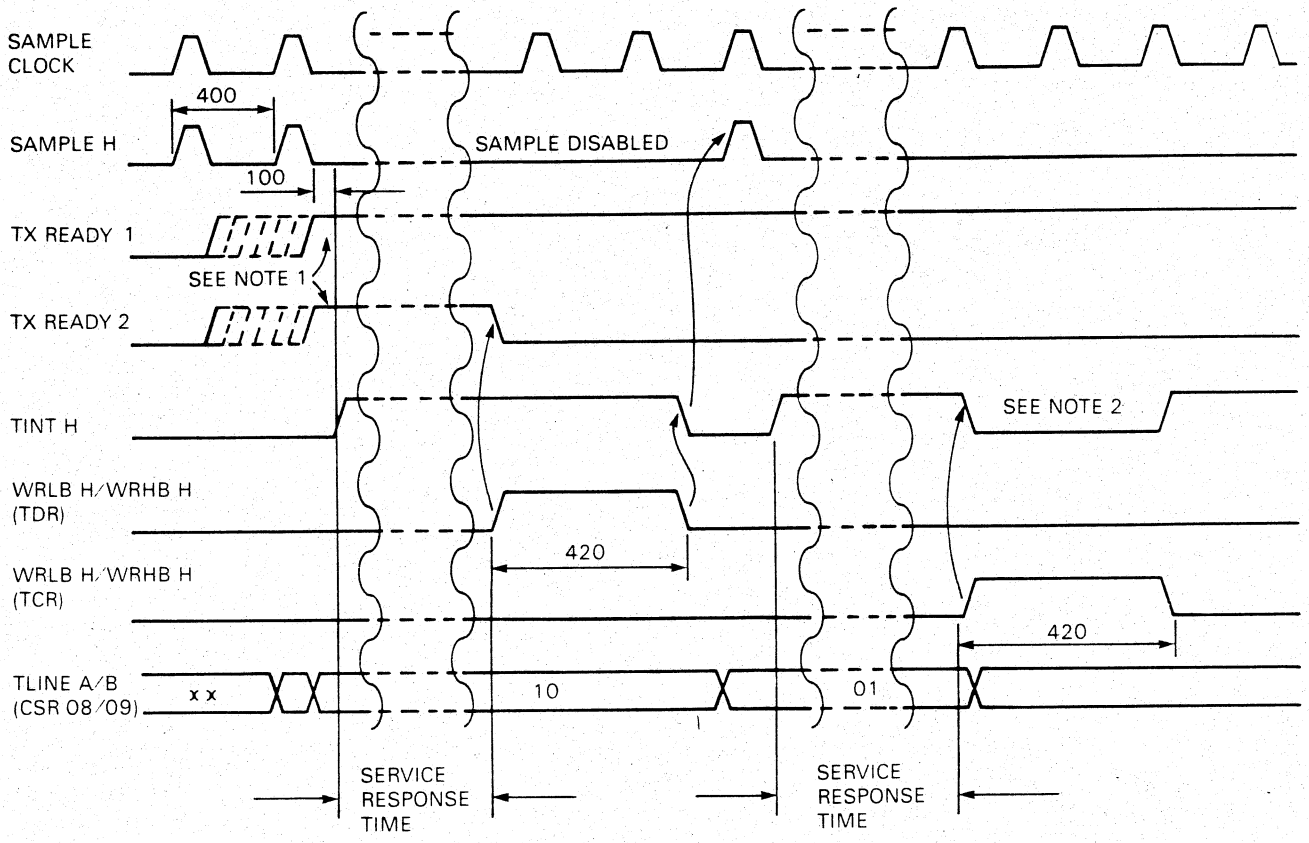
If the service routine disables the line whose UART is waiting for service (when transmission is complete), the sampling clock is again enabled without the need to load a new character. This is done by additional logic, and prevents the service request from permanently staying on that one line.

NOTE

When a LOAD TCR is performed, the TINT H signal is cleared, and is not set again until a new character (or line) needs servicing.

Figure 5-12 shows the timing relationship between the different pins of the DC367B that are associated with the transmitter control function.

Again, as with the Receiver Control circuit, the Transmit Control operation is disabled while the Master Scan Enable (MSE) bit stays clear. Because the MSE bit is cleared on power-up by BINIT L (or on Master Reset), this bit must be set before the Transmit Control operation can start.



NOTE 1 – LINE 2 HAS HIGHER PRIORITY. ASSUME LINE 0 AND 3 DISABLED
NOTE 2 – **TINT** IS HELD **OFF** DURING WRITE TO **TCR** PULSE
NOTE 3 – ALL TIMING EXPRESSED IN NANOSECONDS

Figure 5-12 Transmitter Control Timing Diagram

5.4.2.5 Break (BRK) Bits – The transmission and reception of BRK bits are closely related to the transmission and reception of data. A break signal is a continuous spacing condition in the serial data line. When a UART receives a break signal, it interprets the continuous space as a character with a missing stop bit. Therefore, it sets the framing-error flag. The program then determines how to handle a framing error.

The framing-error bit of channel 3 may be connected (via an 8881 driver and switch setting) to either BHALT L or BDCOK H, to halt or boot the processor. This could also be done by program after normal reading of the framing error via the receiver buffer, but the hardware method gives an immediate response.

A break signal may be transmitted by interrupting the flow of serial data leaving the UART. The high byte of the TDR can be considered as a break register. It contains one BRK bit for each of the four communication channels. Setting one of these bits inside the DC367B will inhibit the flow of data from the UART transmitter to the EIA transmitter, and so cause a Break to be transmitted on the communication line as soon as the break bit is written. Break is removed as soon as the break bit is cleared.

5.4.2.6 Speed and Format Control – The sections controlling speed and format include four line-parameter registers (LPRs), a baud-rate generator with four baud-rate selectors (one for each line), and chip test-select logic which allows an external clock to be used instead of the baud-rate generator.

When the computer writes a word out to the LPR, the following events occur, byte writes having no effect.

1. During address time, the bus interface and I/O control circuitry decode the address and set RGB and RGA to 0 and 1 for the DC367B chip.

2. During data time, data bits 00, and 01 (with bit 02 low) are decoded to enable one of four strobe gates.

3. Bits 03 to 07 are strobed into the appropriate UART to select the number of data bits, the number of stop bits, and odd, even, or no parity.

4. Bits 08 to 11 are strobed into the appropriate baud-rate selector to control the amount by which the 5 MHz oscillator (connected to pin 6) is divided to produce the UART clock signal. Bit 12 is also latched here for the selected line to enable/disable the receiver clock.

In this way the four functional LPRs are partly in the UARTs and partly in the baud-rate generators, all within the DC367B chip.

Input pin 57 on the DC367B (TST0) provides a means of operating the chip at a baud rate of either 19.2K baud, or 38.4K baud. By removing the normally made jumper at W10 and installing a jumper at W9 (so placing a HIGH on the TST0 pin) the internal UART baud-rate input is taken directly from pin 56 (TSTCLK) instead of the 5 MHz input via the internal divider. A crystal oscillator of 3.6864 MHz at Y2 drives a divider chip (74LS92) at E3. Jumper W11 must be removed. With jumper W12 installed, the divider output connects to the TSTCLK input to provide 38.4K baud operation. With jumper W13 connected instead, the divider provides 19.2K baud operation. These speeds can be selected for any line by setting bits 8 to 11 of the appropriate LPR to all 1s. Those lines with a different speed-code selection are not affected. The position of these jumpers can be found from the print set.

NOTE

Neither the 3.6864 MHz crystal oscillator nor the divider chip, 74LS92, are installed or tested at the factory. They must be provided by the user if wanted.

NOTE

Still higher speeds can be obtained by providing external clock sources. The DC367B chip can operate at up to 230.4K baud when pin 56 is connected directly to the oscillator at Y2. This is also not a supported option, and is not factory-tested.

For test purposes, it is possible to select the baud-rate generator output from the DC367B chip instead of the serial data/break output. This can be done by placing a High on the test selector (TEST1 H) which is normally hardwired to ground (de-selected) on the PC board.

5.4.3 FIFO Buffer

5.4.3.1 FIFO Description – The FIFO buffer functions as follows. If space is available in the buffer, a character is written into it. The character then automatically propagates down to the first available open slot. It is stored there until a character is removed from the output side. Remaining characters propagate toward the output. Each character is stored with the following format. The data bits are stored in the low byte or first eight bits, the channel number is stored in two bits, and the status information (parity, overrun, and framing error) is stored in three bits of the high byte. Bit 15, when present, indicates a valid entry.

Once any character reaches the output of the buffer, a Receiver Done occurs. This indicates that a service routine may read the buffer to get the character. When the character has been read, a Shift Out pulse (SHO H) causes the contents of the FIFO buffer to propagate down, so presenting the next character at the output of the buffer.

The Receiver Done flag is serviced by the software either on an interrupt basis, or on a flag-checking basis. Either way, the service routine should process all characters in the FIFO to prevent overheads caused by entering and leaving the service routine. The service routine affects only the output of the FIFO buffer and does not affect the receiver control search logic.

5.4.3.2 FIFO Operation – The silo buffer is made up from four 4-bit × 64 type 3341 serial memory chips. The chips are arranged as a 16-bit 64-word-deep first-in-first-out (FIFO) memory. Data is entered in the 'top' of the memory as described in the previous section. The IRDY H signal indicates that there is a space in the top word of the memory. Also, the ORDY H signal indicates that a word in the 'bottom' of the FIFO is waiting to be shifted out.

The buffer stores full RBUF words. Received character data is stored in the low byte, and receiver status data in the high byte.

As described in Section 5.4.2.2, the DC367B shifts data into the FIFO buffer eight bits at a time. First the low byte (data) is shifted into the chips at E10 and E30 by signal SHI01 H; then the high byte (status) is shifted into the chips at E4 and E17 by the signal SHI23 H. This dual operation multiplexes the 8-bit data bus between the DC367B and the FIFO, so reducing the DC367B pinout.

The total shift-in time is 1.6 microseconds (800 ns per byte). The shift-in pulses are about 600 ns long, leaving 100 ns for data-settling time before the shift-in pulse, and 100 ns data-holding time after the pulse. Refer to Figure 5-10.

Data is shifted out by the CPU as a result of either a Receiver Done interrupt or flag, or a Silo Alarm interrupt or flag. When O/P RDY from each of the FIFO chips is set, ORDY H becomes set. This is applied to the DC367B chip.

Logic inside the DC367B gates ORDY H to the output pin RINT, as long as Silo Alarm Enable is clear. Therefore RINT H follows ORDY H directly. If Silo Alarm Enable is set, however, RDONE is prevented from asserting RINT H. It can only be asserted by Silo Alarm – on the 16th received character.

RINT H goes to the interrupt logic chip DC003, which produces a Receiver Interrupt if the RIE bit is set in the CSR.

Data output from the FIFO buffer is applied to the internal DAL bus (and from there to the BDAL lines of the Q-bus) when RDRBUF L enables the tri-state buffers at E31 and E32. The data is valid only if, at the start of the read time (start of RDRBUF L), ORDY H is set. If not set, it will indicate an empty FIFO. It is possible to read a character too soon after the last read from RBUF, while the next character is still bubbling through. A 2-microsecond gap between consecutive reads is needed to prevent this. The state of ORDY H is latched during the RDRBUF L period, to provide an indication of the valid/invalid condition, and is presented on line DAL15 H. This bit appears in the RBUF register, but is physically generated inside the DC367B chip. The Data Valid bit is generated just as it is read, while the other bits in the RBUF are generated earlier – as the character is received.

The trailing edge of RDRBUF L triggers the one-shot at E9 to produce a shift-out pulse SHO H, but only if the Data Valid bit is set (DVALD H is high). This causes the next character in the FIFO to bubble through to the bottom of the FIFO, ready for the next RDRBUF L signal. If DVALD H is not set, no pulse is generated, and the FIFO is not affected. Also, if the FIFO is empty, no pulse is generated because Data Valid is prevented from being set. The SHO H pulse is about 200 ns wide.

Figure 5-13 shows the timing relationship between the different signals associated with the FIFO buffer.

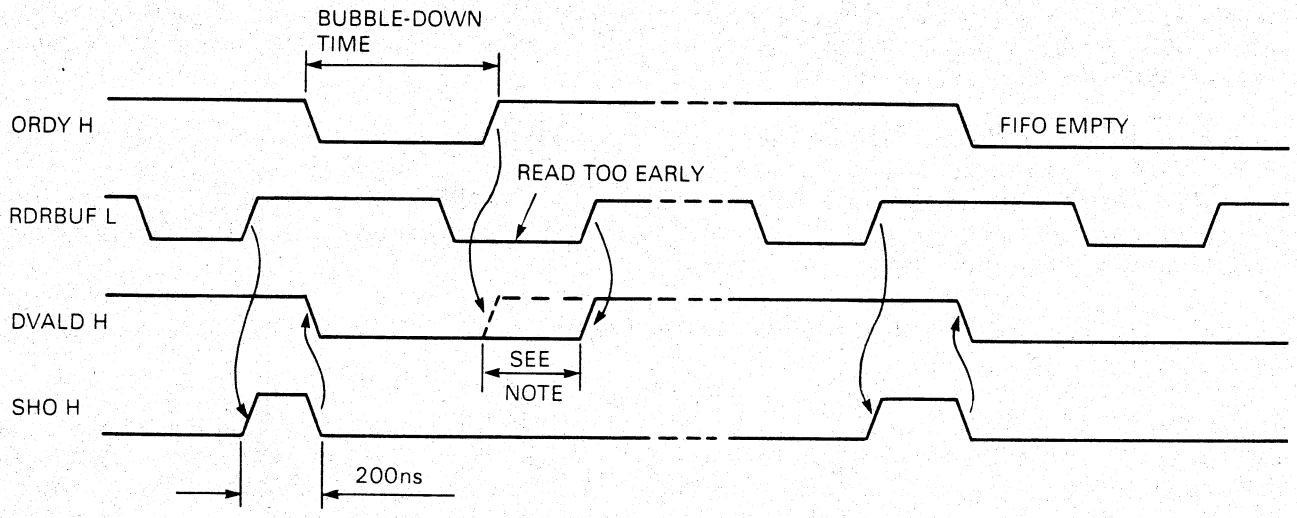


Figure 5-13 FIFO Output Timing

5.4.4 Maintenance Mode

The DZQ11 can be switched to receive the data that is being transmitted. The four serial data lines leaving the UARTs are applied to both a data selector and the EIA transmitters. The data selector controls the inputs to the UART receivers. In the maintenance mode, the data selector ignores the inputs from the EIA receivers, and routes, instead, the output data to the UART receivers. This internal 'wrap-around' feature is enabled by setting the Maintenance bit in the CSR, bit 03. All the appropriate logic is inside the DC367B chip.

5.5 LINE INTERFACE

5.5.1 Description

The DZQ11 line interface is a simple set of level converters. All line input signals are fed into EA9637-type chips at E23, E22, E34, E38, E37, and E35. Each of these chips is a dual-channel receiver designed for EIA-compatible signals. All line output signals are fed to EA9636-type chips at E19, E20, E21, E24, E36, and E39. Each of these chips is a dual-channel transmitter also designed for EIA-compatible signals.

When the DZQ11 is used to interface with a local terminal, it is common practice to make use of only the Transmit Data and the Receive Data circuits. When interfacing with datasets (modems), however, the DZQ11 monitors two other signals, and can control one other signal. The one controlled signal can be jumpered so as to control two additional dataset circuits. The resulting three controlled circuits, however, can only be controlled together and not independently. Table 5-7 defines the modem control and status signals and describes their normal function.

Table 5-7 Modem Control and Status Signals

Signal	Function
Data Terminal Ready	Enables the local modem to be connected to a remote modem. This signal is negated to terminate a call.
Request To Send	Holds the modem in the transmit mode.
Forced Busy	Used with Bell Model 103E and 113B equipment. Signals the modem controller to switch to another channel.
Ring Indicator	Indicates that the local modem is receiving a ringing signal from a remote modem.
Carrier Detect	Indicates that the local modem is receiving (Received Signal a signal from a remote modem, and that the Detector) signal meets the suitability criteria of the local modem.

5.5.2 EIA Receivers

The DZQ11 receives three modem signals for each of the four communications lines that it interfaces. Carrier Detect, Ring Indicator, and Receive Data are received and converted from EIA levels to TTL levels. The Carrier and Ring Status signals go to tri-state buffers, and are placed on the device bus DAL lines to be read as the Modem Status Register (MSR). The Receive Data signals go to the DC367B chip where they connect to the individual UARTs (BSDI0 H to BSDI3 H). Refer to Figure 5-14.

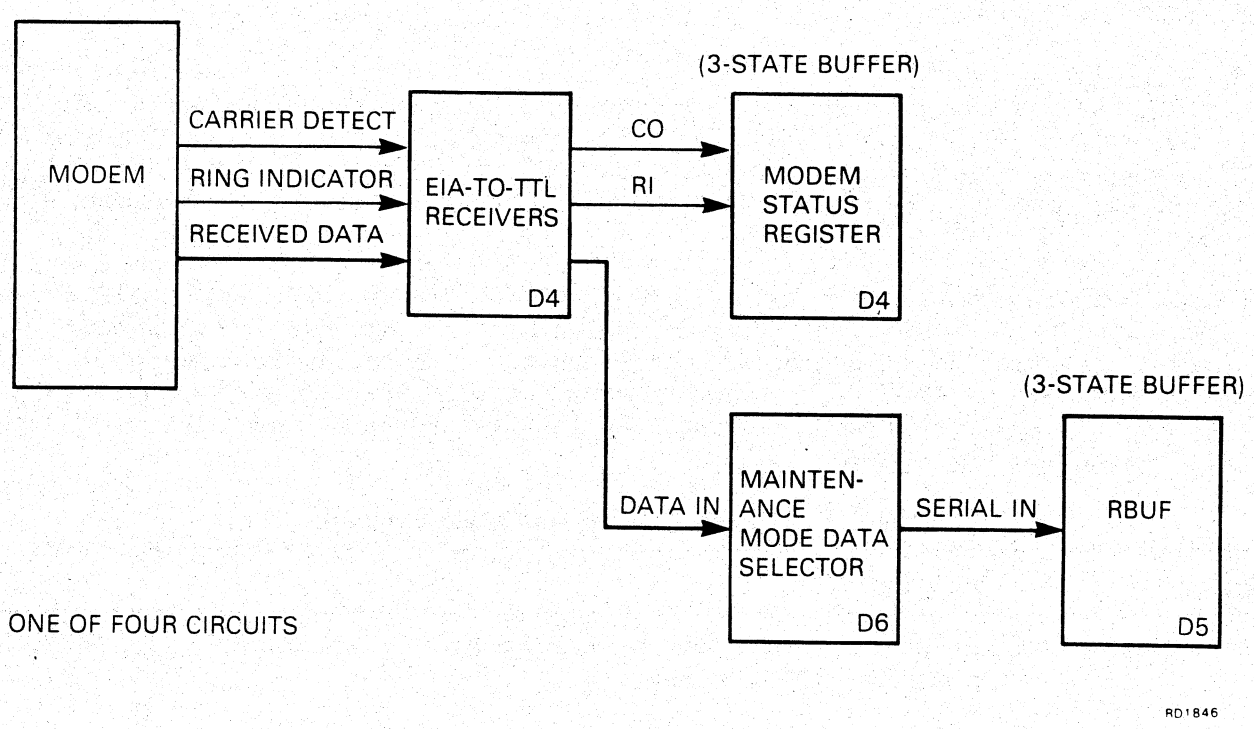


Figure 5-14 EIA Receivers

5.5.3 EIA Transmitters

The DZQ11 has three modem control lines for each of the four communications lines it interfaces. The Transmitter Control Register (TCR) carries a single control bit for each of the four communications lines. This is converted from TTL level to two EIA levels, by means of two converters for each line. One EIA level is always used as the modem Data Terminal Ready (DTR) signal. The second level may be jumpered to provide a modem Request To Send (RTS) signal. The EIA level RTS signal may also be jumpered to provide a Forced Busy signal for use with Bell 103E and 113B modems (or equivalent) if necessary. All three control signals are derived from the single control bit, and are therefore not separately programmable. Refer to Figure 5-15.

The DZQ11 Transmit Data signals are generated by the transmitter UARTs inside the DC367B chip, and the four signals BSDO0 H to BSDO3 H are each converted to EIA levels, and fed to the lines.

5.6 POWER SUPPLY

The DZQ11 uses the +12 V and +5 V available on the Q-bus backplane, and also needs –12 V. This is produced by a switch-mode power supply.

The circuit is built around a TL494 switching regulator which uses pulse-width control to regulate the –12 V output.

Inside the TL494, an oscillator runs at a frequency determined by the time constant of the resistor and capacitor connected to pins 5 and 6. This is about 35 kHz. Pins 8 and 11 drive a power transistor ON and OFF.

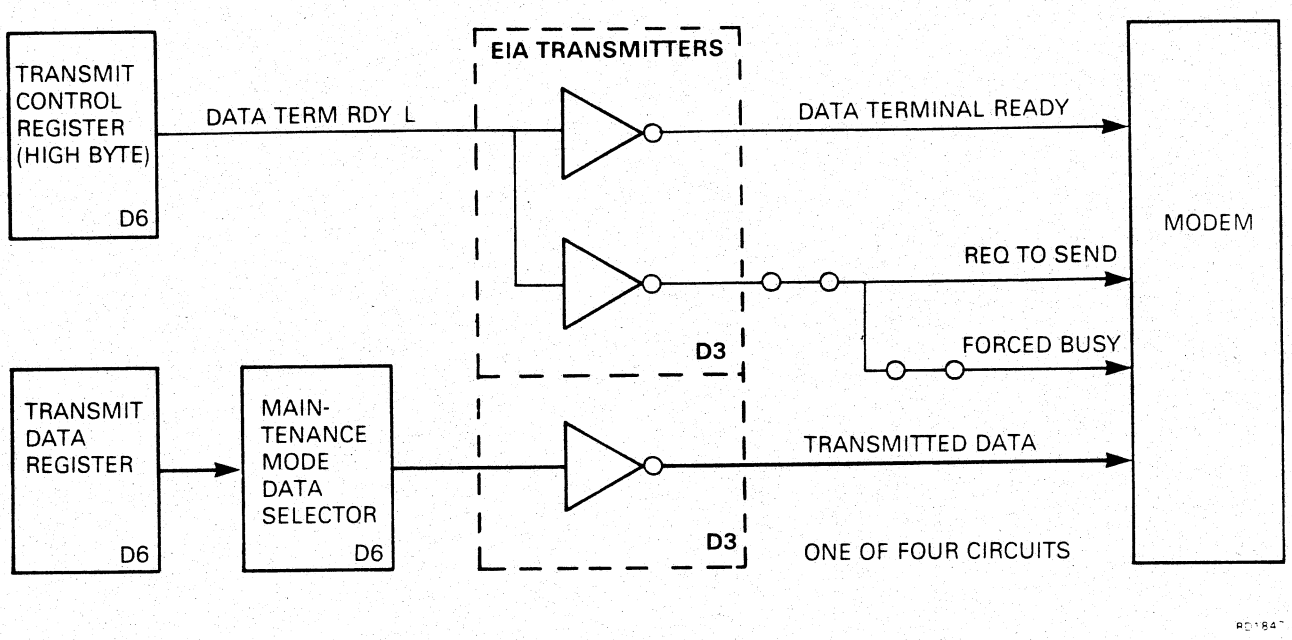


Figure 5-15 EIA Transmitters

When the transistor is ON, its collector is positive and at about +12 V, and the rectifying diode is cut off. Therefore current flows through the 0.39 ohm resistor and the inductor, causing a magnetic field to develop in the inductor. When the transistor is turned OFF, the magnetic field collapses and a self-induced voltage develops across the inductor. This voltage causes power to flow through the rectifying diode, and charge the output smoothing capacitor. Therefore power is transferred from the +12 V supply to the output −12 V line. This line is held at −12 V by means of feedback into the TL494, which changes the width of the pulse that holds the transistor ON. The wider the pulse, the bigger the magnetic field build-up, and the higher the output voltage.

CHAPTER 6
MAINTENANCE

6.1 SCOPE
This chapter explains the maintenance strategy, and how to use the diagnostic programs to find a defective field-replaceable unit (FRU). There is also a troubleshooting flowchart.

6.2 PREVENTIVE MAINTENANCE
No preventive maintenance is planned for the DZQ11. However, if you are servicing the host system, you should check visually for loose connectors and damaged cables.

6.3 CORRECTIVE MAINTENANCE (PDP-11 SYSTEMS)

6.3.1 General
You may recognize the need for corrective maintenance because of a failure during normal operation or because of errors detected during system maintenance. When an error is detected, run the diagnostic programs to isolate the failing FRU. If necessary, refer to Chapter 2 for installation information.

This chapter gives a short description of the diagnostic programs and test modes. For details refer to the program listings.

If it becomes necessary to troubleshoot the DZQ11 to component level, look at the program listing on the use of looping features. By using the program to keep the option in the failing mode, and by using Chapter 5 and the circuit schematics to find the related circuitry, you may be able to isolate the problem to a failing component. This type of maintenance is not recommended if module replacement is possible.

6.3.2 Tools, Test Equipment, and Troubleshooting Aids
The minimum requirements for corrective maintenance are the programs listed in Table 6-1 and, if needed by the system hardware configuration, a screwdriver to remove cover panels. The first two programs can test the DZQ11 using the internal wrap-around feature described in Section 5.4.4.

Table 6-1 Diagnostic Programs

Program Code	Program Title
CVDZA	DZV11/DZQ11 diagnostic, part 1 of 2
CVDZB	DZV11/DZQ11 diagnostic, part 2 of 2
CVDZC	DZV11/DZQ11 cable/echo test
MD-11-DVDZD	DZV11/DZQ11 overlay for ITEP
MD-11-DZITA	Interprocessor test program (ITEP)

You can make better checks by using the H329 and H325 test connectors. The H329 connects data lines and control signals in a staggered loopback configuration. This connector plugs into the Berg J1 on the module, and allows the diagnostic program to check out all the module. The H325 test connector plugs into the modem end of the interface cable. It loops back data lines and control signals without staggering the lines. This allows the program to test both the module and the cable. These test connectors are shown in Figure 1-4 and their part numbers appear in Table 2-1.

If it is necessary to troubleshoot to component level, an ohmmeter, an oscilloscope, and a dual-height extender card are also necessary. Before probing the module, make a good visual inspection for damage to parts or to printed circuits.

6.3.3 DECX/11 Exerciser Program

The DECX/11 system run-time exerciser is made up from different software modules, configured to run interactively. The exerciser is unique to the system it exercises, and must be reconfigured if options are added to the system. The exerciser is different from the diagnostic programs, which test and test the option again in isolation. The exerciser tests the ability of the option to run in the system environment. It does this by performing a sample of the functions of the option while also testing other system components.

The DZQ11 module of DECX/11 is CXDZB DZV11/DZQ11 module test.

6.3.4 XXDP+ Diagnostic Programs

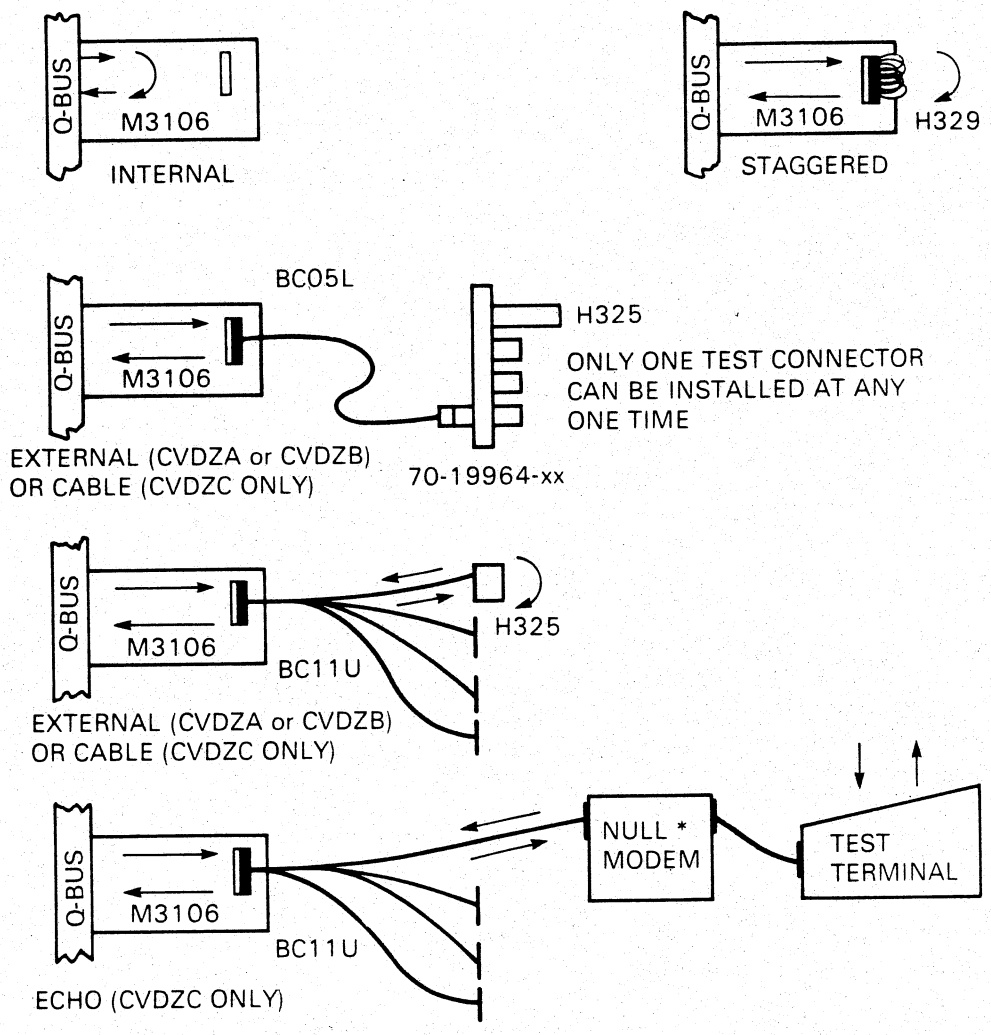
6.3.4.1 General – The diagnostic package has three standalone diagnostics (CVDZA, CVDZB, and CVDZC) and an overlay for the interprocessor test program (DVDZD). To run the interprocessor test, you must first load the ITEP monitor (DZITA). These programs are available on the media listed in Table 6-2. Details of the programs are given in the program listings. This section gives general procedures and information.

Table 6-2 Multimedia Assignments

Media	Title	Part Number
Diskettes	CZZHQnn* DXDP+ 43LSI FLP4	AS-C638n-MC
	CZZMTnn DYDP+ 20LSI-11 #2	BA-F048n-MC
Disk Packs		
(RK05)	CVZZEnn LSI-11 XXDP+ DIAG PKG	AN-T069n-MC
(RK06)	CZZRBnn RK6 DIAG PKG	AM-S469n-MC
(RK07)	CZZSBnn RK7 DIAG PKG	AY-T539n-MC
(RL01)	CZZLDnn RL1 DIAG PKG1	AX-T502n-MC
(RL02)	CSYSAnn 11/23 PLUS SYSTEM CHK	BC-T160n-MC
	CZZLNnn DLDP+ DL2 DIAG PKG	BC-F916n-MC
Tape		
(TU58D)	CXYAEnn DDDP+5 DEVICES	BE-F669n-MC
(TU16)	CZZZ4nn MMDP+ 2400' MT9 1/2	AP-T071n-MC
	CZZZNnn MMDP+ PKG6 MT9	AP-T421n-MC
(TS04)	CZZZ9nn MSDP+ 1600 BPI MT9	BB-F751n-MC
	CZZZVnn TRDP+ TR79 MT	BB-C631n-MC

* The n in the titles and part numbers indicates the revision level, and can change when an update takes place. For example, CZZZVA0 indicates Rev. A, patch 0 of CZZZV. In the same way, BB-C631B-MC indicates Rev. B in the part number.

6.3.4.2 Maintenance Modes – Figure 6-1 shows the data paths for the maintenance modes. The two basic programs (CVDZA and CVDZB) can be run in the internal, staggered, or external modes. The cable and echo test (CVDZC) can be selected either to loop characters from the program out through the test connector and back to the program, or otherwise to loop characters from a test console through the DZQ11 and back out to the test terminal. The interprocessor test program needs another CPU running the test together with the CPU under test. The other CPU may be a local system, or a remote system (such as a turnaround system). Refer to Figure 6-2. In this test, the two processors communicate to check the hardware from end to end. It is possible, however, to operate the program with an H325 loopback connector instead of another processor.



* A NULL MODEM, SUCH AS AN H312, MAY BE NECESSARY, DEPENDING ON THE TERMINAL USED FOR TEST.

Figure 6-1 Maintenance Mode Data Flow

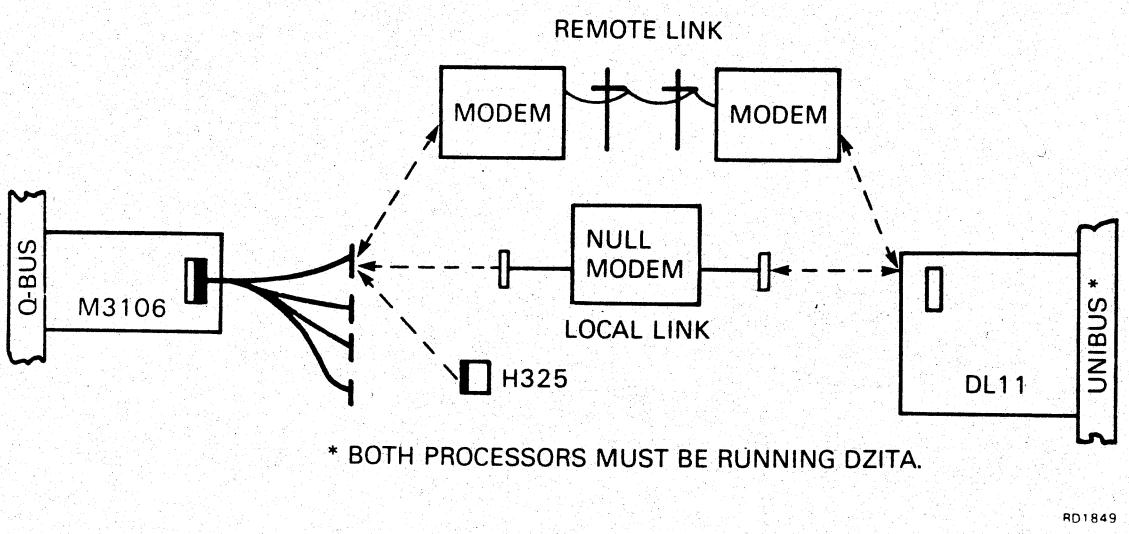


Figure 6-2 Interprocessor Test (ITEP)

6.3.4.3 Setting Up Procedures – Running the internal loopback test needs no setting up. The loopback function is enabled by CSR<03>. The staggered loopback test needs the H329 test connector plugged in J1, in place of the cable. The best method of doing this is to power down the computer, unplug the DZQ11 module, and swap the interface cable for the H329 test connector. Then install the module again, taking care not to damage the components on adjacent modules.

NOTE

You must install jumpers W1 to W4 if either test connector H329 or H325 is used (see Section 2.3.1 in Chapter 2).

To run the external test, disconnect the far end of the BC11U interface cable from the modem or terminal. Plug the H325 test connector into the modem end of the cable. If the 70-19964-00 distribution panel is fitted, plug the H325 into the 25-way D-type connector.

The cable test also needs an H325, as indicated in Figure 6-1. The echo test needs a terminal connected to the DZQ11. This may need a null modem, depending on the type of terminal.

The setting-up procedure for the interprocessor test is different, depending on the equipment available.

6.3.4.4 Software Switch Register – The diagnostic programs use location 176 for a switch register instead of front panel switches. To change the operating parameters, load the program and then use the ODT slash command to open location 176. Refer to the appropriate program listing for a definition of bits. Assemble the corresponding octal number and enter it into location 176. Then start the program at location 200.

NOTE

Memory locations and contents are given in octal notation in this chapter.

The software switch may be accessed while the program is running. Press CTRL/G to stop the program and open the switch register.

6.3.4.5 Auto-Sizing – The two basic tests (CVDZA and CVDZB) have auto-sizing capabilities, and may therefore be run without changing the switch register.

The auto-sizer routine detects all DZQ11 device and vector addresses within the floating address and vector area. The values of the other parameters are by default set for 19 800 baud, internal loopback, and the testing of all four lines. These values are stored in a status table in locations 1500 to 1740 (Table 6-3). They are printed by the console terminal during the test.

Table 6-3 Typical Map of DZQ11 Status*

Location (Octal)	Contents (Octal)	Meaning
1500	160100	CSR address of first DZQ11 in system.
1502	000300	Receiver interrupt vector for first DZQ11 in system.
1504	000017	TCR bit represents the active lines to be tested.
1506	017470	LPR bits representing the following: receiver enabled, 19 800 baud, 8 bits per character, and 2 stop bits.
1510	000000	Indicates the selected maintenance mode, where: 000000 = Internal 000200 = External with H325 100000 = Staggered with H329

* This table is an example. Look at the program listing for details. If a supported baud rate is needed, enter the appropriate value.

6.3.4.6 Parameter Inputs and Dialogue – The CVDZA and CVDZB diagnostics may be run with parameters specified by the operator. To do this, set bit 00 in the software switch register and then start the program at location 200. The program responds with a series of questions.

1ST CSR ADDRESS (160000:167770):

Answer this question by typing in the address of the DZQ11 CSR at which you want testing to start. Press RETURN after all answers.

1ST VECTOR ADDRESS (300:770):

Type the vector of the DZQ11. Note that all the DZQ11s must be contiguous for both address and vector locations.

MAINTENANCE MODE
[EXTERNAL <H325> (E)]
[INTERNAL <DZCSR03 =1>(I)]
[STAGGERED <H329> (S)] :

Press E, I, or S, as appropriate. If running external, all selected lines must be terminated by H325 test connectors.

NOTE

It is not possible to install more than one H325 test connector in the 70-19964-00 distribution panel at any one time. It is necessary to select each line for test, using bit 03 of the software switch register.

OF DZV11/DZQ11'S <IN OCTAL> (1:20):

Type the total number of DZQ11s to be tested.

Other parameters (for example, baud rate) that are not included in the opening dialogue may be entered via the software switch register. All other parameters are assigned to all DZQ11s in the system. The program run time is approximately 1.5 minutes on the first pass and 2.5 minutes on the following passes. Run at least three error-free passes.

Operation of the cable and echo test (CVDZC) always needs an opening dialogue. Special switch selections, however, are not needed for normal operation. Start the program and respond to the questions with an answer followed by RETURN.

VECTOR ADDRESS-

Type the vector of the DZQ11 under test.

CONTROL REGISTER ADDRESS-

Type the CSR address of the DZQ11 under test.

WHICH TEST ? ECHO OR CABLE (E OR C)

Type E or C, as needed

BAUD RATE-

Type one of the following: 50, 75, 110, 135, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, or 9600.

LINE:

Type the number of the line that has the H325 test connector on it. The lines are numbered 0, 1, 2, 3.

At this point, the test starts.

Cable Test
If the cable test (C) was selected, the system prints:

CABLE TEST

The cable test executes in approximately 15 seconds at 9600 baud. It prints an end-of-pass message after each pass. To change lines, press any key on the console terminal while the program is running. The system responds with:

LINE:

At this point, change the H325 test connector to another line and type the new line number. The system prints:

CABLE TEST

and continues.

Echo Test
If you select the echo test (E) when the program asks which test, you should answer the baud rate and line questions in the same way as for the cable test. After the line number is typed, the system prints:

TERMINAL ECHO TEST

on the console terminal, and prints:

THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789

on the DZQ11 terminal. To have this message printed continuously, press CTRL/G on the console terminal while the message is being printed by the DZQ11 terminal. The program prints a prompt character on the console terminal and waits for a new switch register setting. Set the switch register to 377 to have the program output on the 'quick brown fox' message continuously.

To return to the normal flow of diagnostic, press CTRL/G and change the switch register to something other than 377.

The console terminal prints:

TYPE A CHAR. ON DZV11/DZQ11 TERMINAL

Type any printable character on the DZQ11 terminal. It will be echoed back to the terminal.

If you press CTRL/C on the DZQ11 terminal, the program prints the end-of-pass message on the console and then continues with the 'quick brown fox' message on the DZQ11 terminal.

To change lines, type any printable character on the console terminal. The system prints:

LINE:

and waits for a response. Plug the next line into the DZQ11 terminal and continue until all the lines have been tested. Refer to the listing for explanations of error printouts.

6.3.4.7 Functional Description – This section gives a short description of the diagnostic programs used with the DZQ11. For a more details, refer to the program listings.

CVDZA – This is the first of a 2-part series used for basic option checkout. It exercises the read/write bits of the registers, performs simple transmit and receive exercises for each line, and verifies the interrupt capabilities of the option (Table 6-4).

Table 6-4 CVDZA Tests

Test Number (Octal)	Functions
1	Verifies the bus response during a read or write to the following device registers: CSR, RBUF, TCR, and MSR.
2	Verifies that bit CLR can be set, and that it will clear by itself.
3	Verifies that the read/write bits of the CSR can be set. Then verifies that they can be cleared. Also verifies that after being set again, they can be cleared by a Master Clear. The bits tested are MAINT, MSE, SAE, RIE, and TIE.
4	Tests that all of the TCR bits can be set, cleared, and cleared by a Master Clear. Also tests that the DTR bits can be set, cleared, and cleared by a RESET.
5	Verifies that RDONE, TRDY, TLINE B, TLINE A, and SA are read-only. Tests that TRDY is zero until a line is selected and MSE is set.
6	Tests that the following CSR bits are read-write: TIE, SAE, MSE, and MAINT. Checks that setting CLR in the CSR will clear these bits.
7	Performs reset testing. Also tests read-only bits in RBUF and write-only bits in LPR.
10	Performs reset testing. Also tests read-only bits in the MSR and write-only bits in the TDR.
11	Verifies that setting DTR causes CO and RI to set under the following conditions: 1. For the same line if an external mode 2. For the staggered line if in staggered mode Lines are staggered as follows: line 0 with line 1, line 2 with line 3. This test is run only if an H325 or H329 is connected to the DZQ11 under test.
12	Verifies that TRDY is set when a line is ready to be loaded. Verifies that the line specified by TLINE A and TLINE B in the CSR applies to the line selected in the TCR.
13	Transmits one character and receives one character on one line at a time. The character is 252. All selected lines will be turned on. This is the first time any data is checked in the receiver. Using switch 09 with this test makes a tight scope loop that transmits a steady stream of characters.
14	Clears RX ENAB in the LPR for each line to verify that each receiving line can be disabled. This test also verifies that the silo can be emptied by setting CLR in the CSR.
15	Verifies that the transmitter transmits characters and the receiver receives characters. One line at a time is tested, based on valid lines. This is the first point at which all data is tested.

Table 6-4 CVDZA Tests (Cont)

Test Number (Octal)	Functions
16	Exercises one line at a time to verify that: 1. The transmitter BRK bit works 2. The receiver can flag framing errors 3. The receiver can flag parity errors.
17	Verifies that the DZQ11 does not interrupt while the processor status does not allow interrupts. Also checks that the DZQ11 can interrupt when the processor status does allow interrupts.
20	Verifies that the receiver interrupts before the transmitter, even when the transmitter was enabled first.

CVDZB – This program is the second of the two basic option diagnostics. It exercises the transmitters and receivers in all possible operating modes and at all possible data rates. Error conditions are induced and the option is checked for the ability to recognize these errors (Table 6-5).

Table 6-5 CVDZB Tests

Test Number (Octal)	Functions
1	Verifies OVRN ERR and SA one line at a time, based on valid lines. As each of the first 16 characters are sent, Silo Alarm is tested to be cleared. On the 16th character, the program tests for Silo Alarm to set. Then all the silo is filled and an overrun error is expected on the 65th character. Using switch 09 for this test sends 20 characters on the line previously selected. This occurs continuously while SW09 = 1.
2	Tests that SAE inhibits receiver interrupts. Sets RIE and checks that SA causes an interrupt on the 16th character. Tests all selected lines one at a time.
3	Interrupt test on the transmitter and receiver. Runs all qualified lines at maximum speed.
4	DZQ11 relative timing test. Each selected line, one at a time, runs 16 characters at all baud rates, and then the highest baud rate with all character lengths. Each following parameter decreases in time from the previously selected parameter. The time is checked against the previous time. The parameters are: 1. Eight bits per character plus two stop bits at 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600 baud.

Table 6-5 CVDZB Tests (Cont)

Test Number (Octal)	Functions
	2. Five, six, and seven bits per character with two stop bits and at 19.8K baud. Each line completes all of the checks before the next line is tested.
5	Checks parity errors in staggered mode only. All selected lines are enabled at the same time. Tests for even parity on odd lines and odd parity on even lines.

CVDZC – This program verifies the cable interface connection between the module and the EIA connector. The diagnostic includes a cable test, an echo test, and a test of modem control signals.

The cable test transmits a binary count pattern via the test connector to the receivers. The data flow is from the program out through the interface cable to the test connector, and back.

The third test verifies that setting DTR for a given line causes CO and RI to set. Jumpers W1, W2, W3, and W4 must be installed for this test.

6.3.5 Interprocessor Test (ITEP)

The interprocessor test program (ITEP) verifies the operation of the DZQ11 by using it in a communications link with another processor. The other processor may be a system at the same location as the system under test, or it may be in a remote communications test center. DVDZD is the DZV11/DZQ11 overlay of the test program. It must be run together with DZITA-D, the monitor program.

ITEP has the following four testing modes:

1. Internal loopback mode
2. External loopback mode (full-duplex only)
3. One-way-in mode
4. One-way-out mode

6.3.5.1 Starting ITEP – ITEP needs a complete communications loop (Figure 6-2). Make sure that a loop is made with compatible equipment. The variable parameters must be the same in each of the two processors. The mode must be one of the options listed in Table 6-6. The system that is to receive data first should be loaded and started first. If the modem being used on this system has an automatic answer feature, it should be enabled. The system that is to transmit first should then be loaded and the connection made. If the CPU is an LSI-11 and the line clock is to be used, it should be enabled before program execution. The load address is 200.

NOTE

Refer to the program listing for details of restrictions, error messages, and optional selections.

Table 6-6 Valid Mode Combinations

CPU No. 1	CPU No. 2
One-Way-Out	One-Way-In
One-Way-In	One-Way-Out
External Loopback	Internal Loopback
Internal Loopback	External Loopback
External Loopback full-duplex)	External Loopback (full-duplex)
External Loopback (full-duplex with H325 test connector on end of modem cable)	

6.3.6 Manual Tests

This section contains some short tests that can be performed using the hardware ODT commands. The examples given here assume that you are familiar with the use of ODT, and that the DZQ11 CSR address is set for 160100. The letter n is used to indicate a number that may change for different systems. For an explanation of ODT commands, refer to the Microcomputer Handbook.

NOTE

Operator input is underlined in the following dialogues.

1. This test verifies that the CLR bit will clear the CSR and the low byte of the TCR.

@160100/000000 LF	Open the CSR
160102/0nnnnn LF	Open the RBUF
160104/000000 LF	Open the TCR
160106/000000 RET	Open the TDR
@160100/000000 10050 LF	Open CSR; enter bits
160102/0nnnnn LF	
160104/000000 7417 LF	Open TCR; enter bits
160106/000000 RET	
@160100/111450 20 LF	Open CSR; set device clear
160102/0nnnnn LF	

160104/007400 LF	Note that low byte of TCR is cleared
160106/000000 RET	The MSR may contain a value of 007417 if the H329 is connected
@160100/000000	Note that CSR is cleared

2. This test makes a basic check of the transmitter scanner. It performs a Master Clear, sets the TCR bit for line 3, and then verifies that line 3 appears in the CSR. It clears the TCR bit for line 3 and then checks that the line numbers in the CSR are clear.

@160100/000000 20RET	See Master Clear
@/000000 50LF	Set MSE and MAINT
160102/0nnnnn LF	
160104/000000 10^	Set TCR bit 03
160102/0nnnnn ^	
160100/101450 LF	Read CSR for TRDY set and TX line = 3
160102/0nnnnn LF	
160104/000010 0^	Clear TCR bit 03
160102/0nnnnn ^	
160100/000050	Read CSR for TRDY and TLINEs cleared

To perform the same test on line 2, proceed as follows.

@160100/000000 20RET	Set Master Clear
@/000000 50LF	Set MSE and MAINT in CSR
160102/0nnnnn LF	
160104/000000 4^	Set TCR bit 02
160102/0nnnnn ^	
160100/101050 LF	Check CSR for TRDY set and Tx line = 2
160102/0nnnnn LF	
160104/000004 0^	Clear TCR bit 02
160102/0nnnnn ^	
160100/000050	Check CSR for TRDY and TLINEs cleared

To perform the same test on line 1, proceed as follows.

@160100/000000 20(RET)	Set Master Clear
@/000000 50(LF)	Set MSE and MAINT in CSR
160102/0nnnnn (LF)	
160104/000000 2^	Set TCR bit 01
160102/0nnnnn ^	
160100/100450 (LF)	Check CSR for TRDY set and Tx line = 1
160102/0nnnnn (LF)	
160104/000002 0^	Clear TCR bit 01
160102/0nnnnn ^	
160100/000050	Check CSR for TRDY and TLINEs cleared

To perform the same test on line 0, proceed as follows.

@160100/000000 20(RET)	Set Master Clear
@/000000 50(LF)	Set MSE and MAINT in CSR
160102/0nnnnn (LF)	
160104/000000 1^	Set TCR bit 00
160102/0nnnnn ^	
160100/100050 (LF)	Check CSR for TRDY set and Tx line = 0
160102/0nnnnn (LF)	
160104/000001 0^	Clear TCR bit 00
160102/0nnnnn ^	
160100/000050	Check CSR for TRDY and TLINEs cleared

3. This next test checks that line 3 is the highest-priority line when all lines are enabled at once. It checks that line priority goes from 3 to 0.

@160100/000000 20(RET)	Set Master Clear
@/000000 50(LF)	Set MSE and MAINT in CSR
160102/0nnnnn (LF)	
160104/000000 17^	Set TCR bits for lines, 3, 2, 1, and 0

160102/0nnnnn ^

160100/101450 LF — Check CSR for TRDY set and Tx line = 3 (highest priority line)

160102/0nnnnn LF

160104/000017 7^ — Clear only TCR bit 3

160102/0nnnnn ^

160100/101050 LF — Check CSR for TRDY set and Tx line = 2 (next highest priority)

160102/0nnnnn LF

160104/000007 3^ — Clear TCR bit 02

160102/0nnnnn ^

160100/100450 LF — Check CSR for TRDY set and Tx line = 1 (third highest priority)

160102/0nnnnn LF

160104/000003 1^ — Clear TCR bit 01

160102/0nnnnn ^

160100/100050 LF — Check CSR for TRDY set and Tx line = 0 (lowest priority)

160102/0nnnnn LF

160104/000001 0^ — Clear TCR bit 00

160102/0nnnnn ^

160100/000050 — Check CSR for TRDY and TLINEs cleared

4. This test checks the receiver without using the transmitter scanner. The BRK bit is set and the RBUF is tested to see that it contains a null character and a framing error.

@160100/000000 20RET — Set Master Clear

@/000000 50LF — Set MSE and MAINT in CSR

160102/0nnnnn 17470LF — Load LPR with 19.8K baud, 8-level, 2 stop bits, and line 0

160104/000000 LF

160106/000000 400RET — Set Break bit in TDR for line 0

@160100/000250 LF — Read CSR for RDONE set

160102/120000 ^	Check RBUF for Data Valid and FRAM ERR set for RX line = 0, and for all zeros in data bits
160100/000050 (LF)	Check CSR for RDONE cleared
160102/020000	Check RBUF for Data Valid cleared

To perform the same test on line 1, proceed as follows:

@160100/000000 20(RET)	Set Master Clear
@/00000 50(LF)	Set MSE and MAINT in CSR
160102/0nnnnn 17471(LF)	Load LPR with 19.8K baud, 8-level, 2 stop bits, and line 1
160104/000000 (LF)	
160106/000000 1000(RET)	Set Break bit in TDR for line 1
@160100/000250 (LF)	Check CSR for RDONE set
160102/120400 ^	Check RBUF for Data Valid and FRAM ERR set, for RX line = 1, and for all zeros in data bits
160100/000050 (LF)	Check CSR for RDONE cleared
160102/020400	Check RBUF for Data Valid cleared

To perform this test on line 2, proceed as follows:

@160100/000000 20(RET)	Set Master Clear
@/000000 50(LF)	Set MSE and MAINT in CSR
160102/0nnnnn 17472(LF)	Load LPR with 19.8K baud, 8-level, 2 stop bits, and line 2
160104/000000 (LF)	
160106/000000 2000(RET)	Set Break bit in TDR for line 2
@160100/000250 (LF)	Check CSR for RDONE set
160102/121000 ^	Check RBUF for Data Valid and FRAM ERR set, for RX line = 2, and for all zeros in data bits
160100/000050 (LF)	Check CSR for RDONE cleared
160102/021000	Check RBUF for Data Valid cleared

To perform this test on line 3, proceed as follows:

@160100/000000 20(RET)	Set Master Clear
@/000000 50(LF)	Set MSE and MAINT in CSR

160102/0nnnnn 17473LF	Load LPR with 19.8K baud, 8-level, 2 stop bits, and line 3
160104/000000 LF	
160106/000000 4000RET	Set Break bit in TDR for line 3
@160100/000250 LF	Check CSR for RDONE set
160102/121400 ^	Check RBUF for Data Valid and FRAM ERR set. for Rx line = 3, and for all zeros in data bits
160100/000050 LF	Check CSR for RDONE cleared
160102/021400	Check RBUF for Data Valid cleared

5. This test transmits and receives some characters on line 0. It uses 8-level with 2 stop bits at 19.8K baud in maintenance mode.

@160100/000000 20RET	Set Master Clear
@/000000 50LF	Set MSE and MAINT in CSR
160102/0nnnnn 17470LF	Set LPR bits for 19.8K baud, 8-level, 2 stop bits, line 0
160104/000000 1^	Set TCR bit 00
160102/0nnnnn ^	
160100/100050 LF	Check CSR for TRDY set and Tx line = 0
160102/0nnnnn LF	
160104/000001 LF	
160106/000000 377 ^	Load 377_8 into TDR
160104/000001 ^	
160102/100377 ^	Check RBUF for Data Valid set, for OVRN ERR, FRAM ERR, and PAR ERR clear, for Rx line = 0, and for the data to be 377
160100/100050 LF	Check CSR for TRDY set and RDONE cleared
160102/000377 LF	Check RBUF for Data Valid cleared
160104/000001 LF	
160106/000000 252 ^	Load 252_8 into TDR
160104/0000001 ^	
160102/100252 ^	Read RBUF for Data Valid set, the error bits clear, Rx line = 0, and the data to be 252

160100/100050 LF	Check CSR for TRDY set and RDONE cleared
160102/000252 LF	Read RBUF for Data Valid cleared
160104/0000001 LF	
160106/000000 125 ^	Load 125_8 into TDR
160104/000001 ^	
160102/100125 ^	Check RBUF for Data Valid set, no error bits set. Rx line = 0, and the data being 125
160100/100050 LF	Check CSR for TRDY set and RDONE cleared
160102/000125 LF	Read RBUF for Data Valid cleared
160104/000001 LF	
160106/000000 0 ^	Load a 0 into TDR
160104/000001 ^	
160102/100000 ^	Read RBUF for Data Valid set, no errors, Rx line = 0, and the data bits being 0s
160100/100050	Check CSR for TRDY set and RDONE cleared

6. This test sets the maintenance bit but disables the receivers. It then transmits a character and checks to see that it is not received.

@160100/000000 20 RET	Set Master Clear
@/000000 50 LF	Set MSE and MAINT in CSR
160102/0nnnnn 7470 LF	Load the LPR with RX ENAB cleared
160104/000000 1^	Set TCR bit 00
160102/0nnnnn ^	
160100/100050 LF	Check CSR for TRDY set and RDONE cleared
160102/0nnnnn LF	
160104/000001 LF	
160106/000000 377 ^	Load 377 into TDR
160104/000001 ^	
160102/0nnnnn ^	Check RBUF to see that Data Valid did not set
160100/100050	Check CSR to see that RDONE is clear

7. This test sets the line for 5-level code and then tries to transmit and receive 377. Transmitted bits are masked in the process, and a 37 is received. This verifies that the UARTs have switched to 5-level.

@160100/00000020 RET	Set Master Clear
@/000000 50 LF	Set MSE and MAINT in CSR
160102/0nnnnn 17400 LF	Load LPR for 19.8K baud, 5-level line number 0
160104/000000 1^	Set TCR bit 00
160102/0nnnnn ^	
160100/100050 LF	Check CSR for TRDY set and line numbers 0
160102/0nnnnn LF	
160104/000001 LF	
160106/000000 377 ^	Load 377 into TDR
160104/000001 ^	
160102/100037 ^	Read RBUF for Data Valid set, no errors, line = 0, data 37
160100/100050	Check CSR for TRDY set and RDONE cleared

6.4 CORRECTIVE MAINTENANCE (MicroVAX SYSTEMS)

Corrective maintenance is performed when operational failures or diagnostic tests indicate that the DZQ11 is defective. Diagnostic test programs for DZQ11s installed in MicroVAX systems are listed below.

EHKMV	Macroverify – MicroVAX System Test
EHXDZ	DZV11/DZQ11 Tests

6.4.1 The Macroverify Diagnostic

Macroverify is a quick system test which is used:

- As a first-line check before using device diagnostics
- As a confidence check
- To verify the complete system after installation or maintenance

The Macroverify diagnostic runs standalone. It runs automatically when the CPU Tests diskette is booted from one of the RX50 drives. The program, which takes up to four minutes to complete, needs 30K bytes of memory. The testing performed by Macroverify does not destroy information recorded on the disks.

6.4.1.1 Setting-Up Procedures – Power up all devices in the configuration. Set all disk drives for I/O. Place a diskette in each RX50 drive. Disconnect any external cables or test connectors from the DLVJ1 and DZQ11 distribution panels. If the system is not set up correctly, Macroverify will output a TEST FAILED message (see Section 6.4.1.3) for the appropriate device test.

6.4.1.2 Bootstrapping Procedure – To boot Macroverify, mount the CPU Tests diskette in one of the RX50 drives, and type:

```
>>>B DUA1        ;boot from drive 1
```

or:

```
>>>B DUA2        ;boot from drive 2
```

6.4.1.3 Macroverify Operation – Macroverify runs as soon as the boot operation is completed successfully. The program contains routines which check for all possible system configurations.

For each possible device, a test is made to see if the device responds to its assigned Q-bus address. If the device does not respond, the following status message is displayed on the console.

```
DEVICE xxxxx WITH CSR yyyyyy, VECTOR zzz NOT FOUND.
NO TESTING PERFORMED.
```

NOTE

The vector number of devices (such as DZQ11) with floating vectors, will not be displayed.

For each device which responds to its assigned address, a sequence of user-level tests is performed. A TEST SUCCEEDED or TEST FAILED message will be displayed. The time that a successful test should take is also displayed.

An example of a macroverify test report follows. The system that was tested had no DLVJ1 installed and the DEQNA cables were not connected. No diskette was mounted in drive 2.

```
0001C7DB 02

>>>B DUA1

ATTEMPTING BOOTSTRAP


Macroverify V1.4

This MicroVAX 1 is at microcode revision level 5, hardware revision level 0,

and includes support for F-FLOAT and G-FLOAT data types.

                    Time to
Testing           Test (mins)    Comments
-----------------------------------------

Memory                0:30       TEST SUCCEEDED (0.50 Mb)

Disk unit DUA0        0:20       TEST SUCCEEDED (RD51 fixed disk)

Disk unit DUA1        0:20       TEST SUCCEEDED (RX50 floppy disk)

Disk unit DUA2        0:20       TEST FAILED (RX50 floppy disk)
```

```
                                    No floppy diskette is mounted in this drive
                                    or the diskette is mounted improperly.
                                    Please correct and rerun this diagnostic.
DLVJ1                 0:40          DEVICE DLVJ1 WITH CSR 776500
                                    NOT FOUND.  NO TESTING PERFORMED.
DZV11/DZQ11           0:10          TEST SUCCEEDED
DEQNA                 0:10          TEST FAILED
                                    Please verify that the cable from the DEQNA
                                    module to the DEQNA patch panel assembly is
                                    correctly connected. Please verify that the
                                    fuse at the DEQNA patch panel assembly has
                                    not blown.

Macroverify test completed

00000031F 02

>>>
```

6.4.2 DZV11/DZQ11 Diagnostic EHXDZ

Device diagnostics, together with the diagnostic supervisor (VDS), are distributed on the MicroVAX System Tests diskette (number 2 of 2). Run the device diagnostic EHXDZ, which runs under VDS, if an operational failure or the macroverify program indicates a defective DZQ11. Minimum memory requirement is 512K bytes (including VDS).

6.4.2.1 Setting-Up Procedures – Before running the diagnostic, make sure that jumpers W1 to W4 are installed on each DZQ11 under test. The DZQ11 is shipped with these jumpers installed.

Disconnect all external cables from the distribution panel.

6.4.2.2 Bootstrapping Procedure – To boot from the MicroVAX System Test diskette, mount the diskette on one of the RX50 drives and type:

```
>>>B DUA1          ;boot from drive 1
```

or:

```
>>>B DUA2          ;boot from drive 2
```

When the boot process is complete, the VDS prompt (DS>) will be displayed. You can then 'attach' and 'select' the DZQ11, and run EHXDZ by means of the normal VDS commands. That is to say, commands such as START/PASS:n and SET TRACE will function. There are no EVENT flags in EHXDZ.

6.4.2.3 Running EHXDZ – This diagnostic consists of 22 tests which are organized in four parts. These are:

a. Internal loopback tests
b. Staggered loopback tests
c. Modem test
d. Echo test

a. Internal Test – In this series, tests 1 to 19 are performed. The data lines are looped back internally.

Details of tests 1 to 19 follow.

1. CSR Test. This test accesses the CSR and manipulates each register bit.

2. TCR Test. This test accesses the TCR and manipulates each register bit.

3. Transmit Ready Flag Test. This test checks the transmit ready flag. Only one channel is checked.

4. Transmit Interrupt Test. This test verifies that the transmit interrupt occurs and is at the correct priority. Only one channel is checked.

5. Maintenance Mode Test. This test verifies that the maintenance mode loopback works correctly. Only one channel is checked.

6. Receive Interrupt Test. This test verifies that the receive interrupt occurs and is at the correct priority. Only one channel is checked.

7. Interrupt Precedence Test. This test verifies that a receive interrupt will take precedence over a transmit interrupt.

8. Transmit Ready Test. This is the same as test 3 with the exception that all four channels are tested.

9. Transmit Interrupt Test. This is the same as test 4 with the exception that all four channels are tested.

10. Baud Rate Timing Test. This test verifies that increasing the baud rate decreases the interval between transmit interrupts.

11. Maintenance Mode Test. This is the same as test 5 with the exception that all four channels are tested.

12. Receive Interrupt Test. This is the same as test 6 with the exception that all four channels are tested.

13. Character Length Test. This test verifies that all four channels can transmit characters of all four possible bit lengths.

14. Stop Bit Test. This test verifies that all four channels can be set for all three possible stop bit configurations.

15. Parity Bit Test. This test verifies that all four channels can transmit characters for all three possible parity bit settings.

16. Overrun Bit Test. This test verifies that the DZQ11 can detect an overrun condition.

17. LPR Byte Access Test. This test verifies that byte acess to the LPR works correctly.

18. Silo Bit Test. This test verifies that all silo memory bits are functional and the silo alarm will be generated under the right conditions.

19. Dynamic Test. This test verifies that all lines will function at full speed and when dynamic changes are made to programmable line parameters.

b. Staggered Test – This series consists of tests 20 and 21. An H329 staggered loopback connector must be installed in J1.

The H329 connector routes the output of channel 0 to the input of channel 1 and vice versa. Channels 2 and 3 are connected in the same way. All four channels are tested.

Details of tests 20 and 21 follow.

20. Modem Control Test. This test verifies the modem control functions. It needs manual intervention and the H329 connector.

21. Dynamic Test. This test is similar to test 19, with the exception that tests are performed in staggered loopback mode. It needs manual intervention and the H329 connector.

c. Modem Test – Modem Test consists of test 20 only (see Staggered Test). You must install a H329 staggered loopback connector in J1.

d. Echo Test – This test (22) verifies communications between a DZQ11 and a terminal. Characters typed at the terminal are echoed back to the terminal. Echo test has a dialogue which asks the operator for the parameters of the terminal. For example; baud rate, bits/character, parity, line to test.

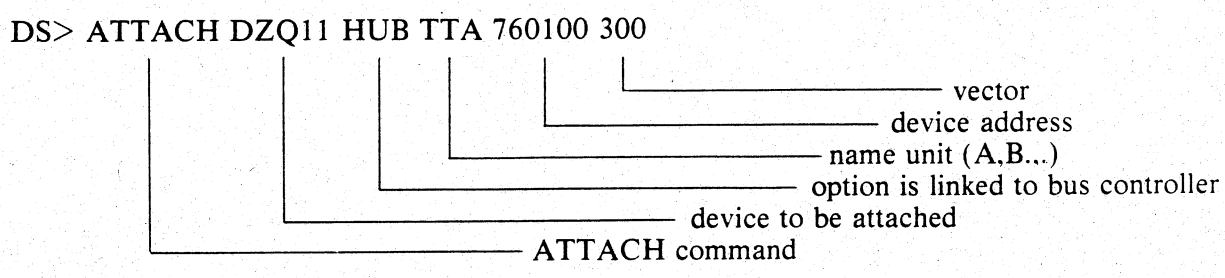
The echo test runs until you deselect it by pressing CTRL/Z.

6.4.2.4 Starting-Up – Once you have booted the MicroVAX System Test diskette, the VDS prompt (DS>) will be displayed. You can then attach the DZQ11 to the bus controller and select it for test. Then you can run EHXDZ. Unless you select a specific test mode, EHXDZ will default to the internal test. An example follows, of a test in the default mode with TRACE set.

```
>>>B DUA1

ATTEMPTING BOOTSTRAP

DIAGNOSTIC SUPERVISOR. ZZ-EHSAA-V6.12-001  1-JAN-1983 00:00:04

DS> attach dzv11 hub tta 760100 300

DS> select tta

DS> set tr

DS> run ehxdz

.. Program: DZV11/DZQ11 Functional Test, ZZ_EHXDZ, revision 1.0, 22 tests,
   at 00:03:09.87.
```

```
Testing:  _TTA
Test 1:  CSR REGISTER TEST
Test 2:  TCR REGISTER TEST
Test 3:  TRANSMIT READY FLAG TEST PART ONE
Test 4:  TRANSMIT INTERRUPT TEST PART ONE
Test 5:  MAINTENANCE MODE TEST PART ONE
Test 6:  RECEIVE INTERRUPT TEST PART ONE
Test 7:  RECEIVE INTERRUPT TEST PART TWO
Test 8:  TRANSMIT READY FLAG TEST PART TWO
Test 9:  TRANSMIT INTERRUPT TEST PART TWO
Test 10: BAUD RATE TIMING TEST
Test 11: MAINTENANCE MODE TEST PART TWO
Test 12: RECEIVE INTERRUPT TEST PART THREE
Test 13: CHARACTER LENGTH TEST
Test 14: STOP BIT TEST
Test 15: PARITY BIT TEST
Test 16: OVERRUN BIT TEST
Test 17: LPR BYTE ACCESS TEST
Test 18: SILO TEST
Test 19: INTERACTION TEST
.. End of run, 0 errors detected, pass count is 1,
   time is 1_JAN-1983 00:03:51.17
DS>
```

The format of the ATTACH command is explained below.



6.4.2.5 Sections – Section is part of the START command. By specifying the section, you can run tests other than 1 to 19.

The sections are:

DEFAULT	– tests 1 to 19	
INTERNAL	– tests 1 to 19	
ALL	– tests 1 to 21	(H329 connector needed)
MODEM	– test 20	(H329 connector needed)
STAGGERED	– tests 20 and 21	(H329 connector needed)
ECHO	– test 22	(test terminal needed)

The following are examples of the use of SECTION.

```
DS> ST/SEC:STAGGERED    ; run tests 20 and 21
DS> ST/SEC:ECHO         ; run test 22
DS> ST/SEC:ALL          ; run tests 1 to 21
```

6.4.2.6 Error Messages – If a diagnostic test detects an error, an error message will be output to the console. Error messages are described in the diagnostic listing for EHXDZ. The error message which follows is from part of a staggered loopback test which was run with the H329 connector removed.

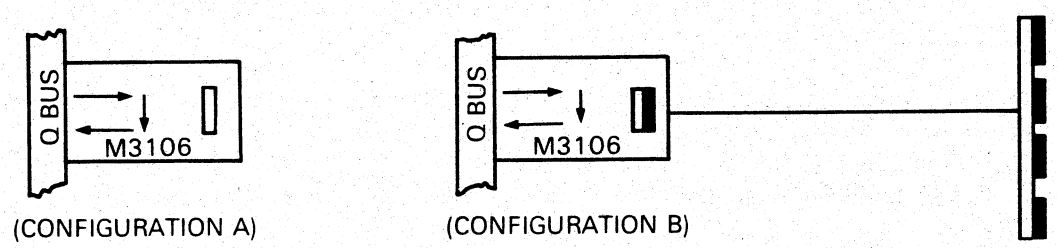
```
DS> st/sec:staggered

..  Program:  DZV11/DZQ11 Functional Test,   ZZ-EHXDZ,   revision  1.0,
    22 tests, at 00:04:15.09.

Testing:  _TTA

Test 20: H329 MODEM CONTROL TEST

********  DZV11/DZQ11 Functional Test, ZZ-EHXDZ - 1.0  ********

  Pass 1, test 20, subtest 0, error 3,  1-JAN-1983 00:04:16.37

  Hard error while testing TTA: MODEM CONTROL TEST

MSR IN ERROR

EXPECTED:0202(X)

RECEIVED:0000(X)

XOR:  0202(X);C01,R11


********  End of Hard error number 3 ********
```

6.4.3 Test Sequence

When a DZQ11 is reported as defective, you have the option of running Macroverify before running EHXDZ. However, if the DZQ11 is clearly indicated as being defective, it would be logical to run EHXDZ first.

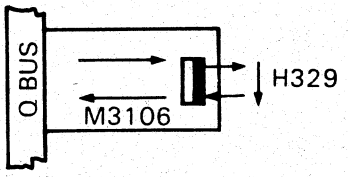
Section ALL selects all tests except the echo test. Therefore, unless the fault symptoms call for repetitive tests of a specific area of logic, section ALL should be selected for initial test. If no errors are detected, but symptoms indicate a defective line, the echo test can be run.

EHXDZ has no specific test for the BC05L cable or the distribution panel.



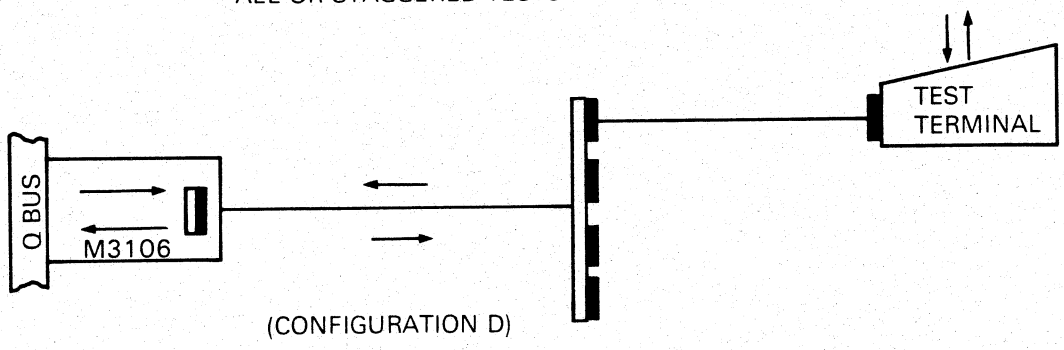
(CONFIGURATION A) (CONFIGURATION B)

INTERNAL OR DEFAULT TESTS



(CONFIGURATION C)

ALL OR STAGGERED TESTS



(CONFIGURATION D)

ECHO TEST

DZQ11 TEST CONFIGURATIONS

RD1882

Figure 6-3 DZQ11 Test Configurations

The recommended test sequence is as follows. See Figure 6-3 for test configurations.

1. Switch off power. Install an H329 staggered loopback connector on J1 (configuration C).
2. Power up (when the system microverify program is complete, the console prompt '>>>' will be displayed).
3. Boot from the system tests diskette.
4. Attach and select the DZQ11 for test.

5. Run EHXDZ for three passes of '/SECTION : ALL'. If there is an error, replace the M3106 module (or the H329).

6. Run ECHO test (configuration D) if needed. If there is an error, replace or repair the terminal, external line, BC05L, or the distribution panel. To deselect ECHO test, press CTRL/Z.

7. Disconnect the terminal from the distribution panel. Remove the diagnostic diskette. Reset the system.

8. Boot from the CPU tests diskette. Macroverify will run automatically. If a defective DZQ11 is indicated, check that the address, vector, and jumpers are correct for the system.

9. If the DZQ11 passes all tests, connect the system for normal operation.

NOTE

For a confidence check of the DZQ11, the internal tests can be run without removing the BC05L cable (configuration B). However, external connections should be removed from the distribution panel.

APPENDIX A
IC DESCRIPTIONS

A.1 SCOPE

This appendix contains data on the LSI chips used in the DZQ11. The smaller common ICs, which are well described in standard reference books, are not included. For information not included in this document, read the appropriate manufacturer's data sheets.

A.2 DC003 INTERRUPT IC

The interrupt controller is an 18-pin DIL device that provides the circuits to perform an interrupt transaction in a computer system that uses a 'pass-the-pulse' type arbitration. The device provides two interrupt channels, A and B, with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or open-collector outputs, which allow the device to be attached directly to the computer system bus. Maximum current taken from the Vcc supply is 140 mA.

Figure A-1 is a simplified logic diagram of the DC003 IC. Timing for the interrupt section is shown in Figure A-2, while Figure A-3 shows the timing for both A and B interrupt sections. Table A-1 describes the signals and pins of the DC003 by pin and signal name.

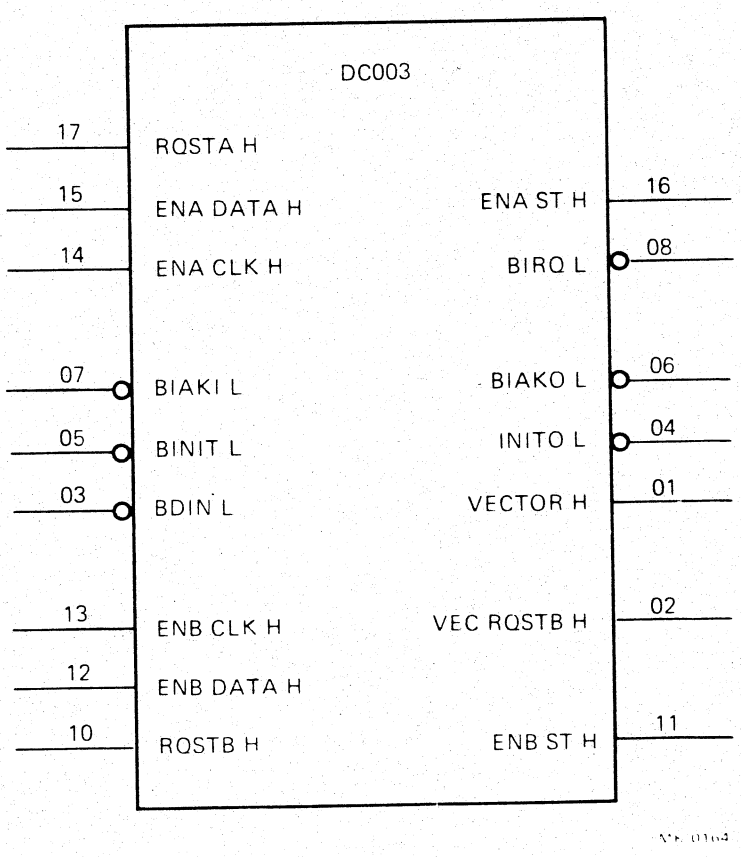


Figure A-1 DC003 Logic Symbol

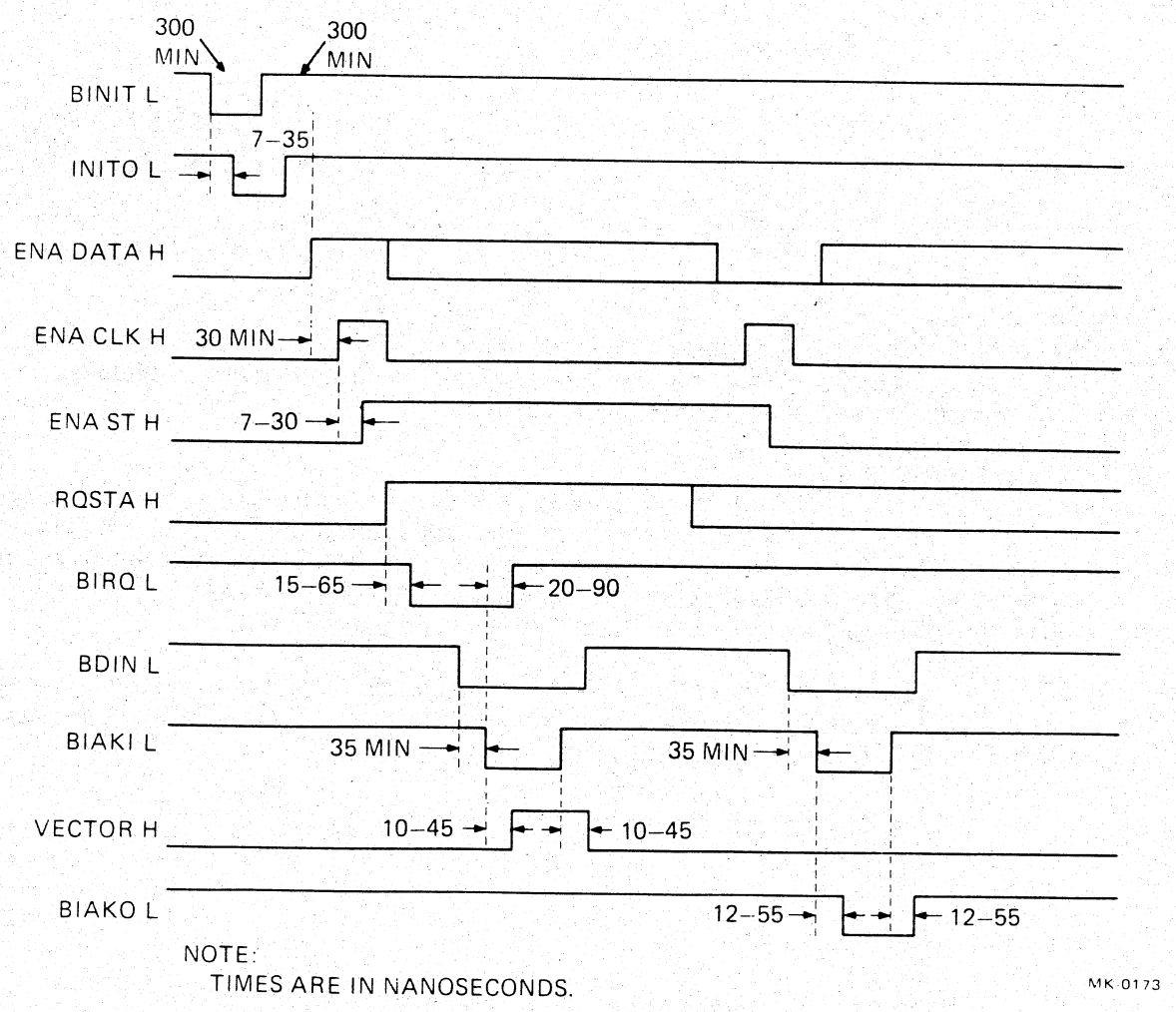
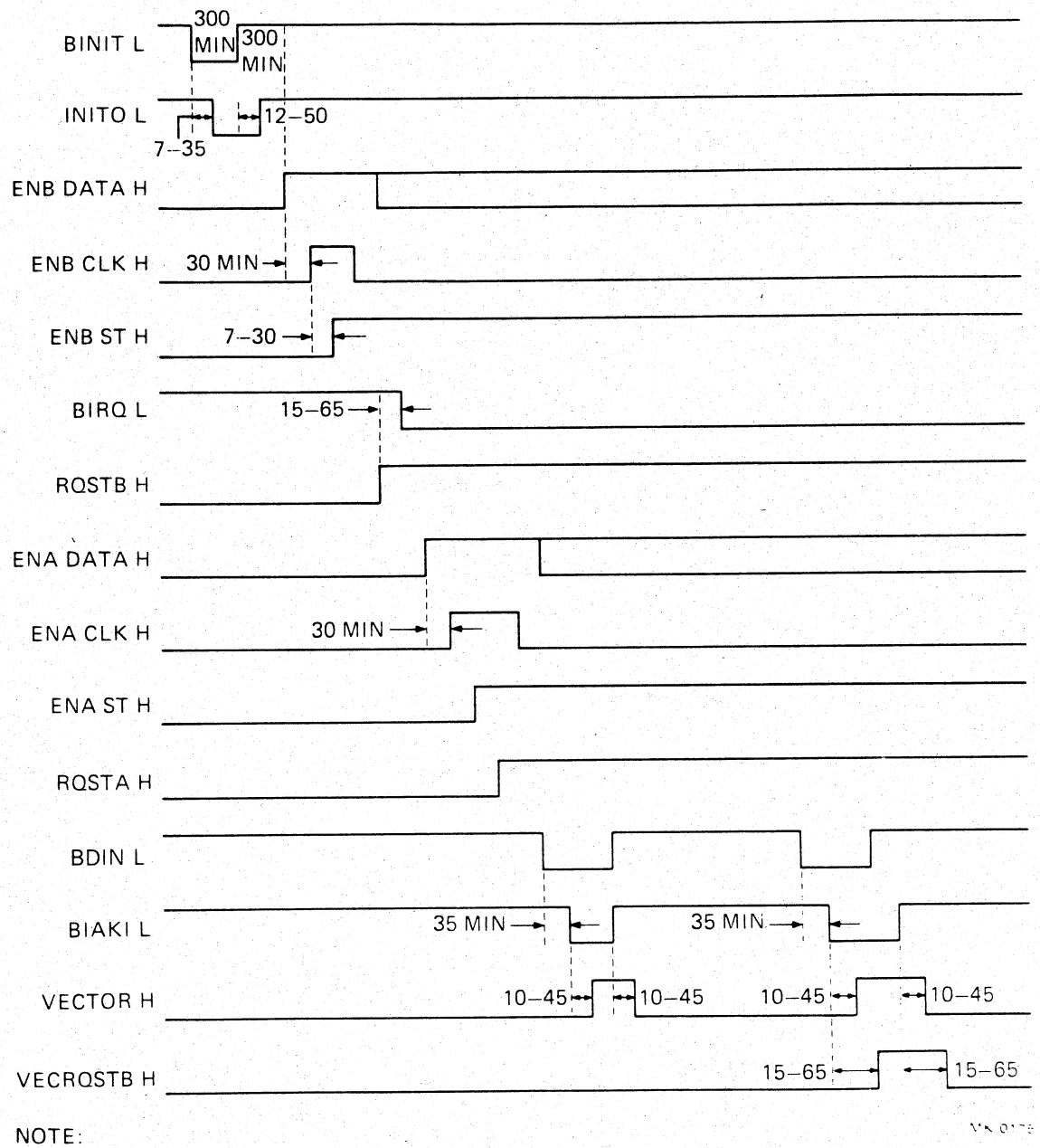


Figure A-2 DC003 A Section Timing



NOTE:
TIMES ARE IN NANOSECONDS.

Figure A-3 DC003 A and B Section Timing

Table A-1 DC003 Signals

Pin	I/O Name	Symbol	Function
1	Interrupt Vector Gating Signal	VECTOR H	This signal gates the appropriate vector address to the bus and forms the bus signal BRPLY L.
2	Vector Request B Signal	VEC RQSTB H	When asserted, this signal indicates RQST B service vector address is wanted. When not asserted it indicates RQST A service vector address is wanted. VECTOR H is the gating signal for the complete vector address; VEC RQST B H is normally bit 2 of the address.
3	Bus Data In	BDIN L	The BDIN signal always precedes a BIAK signal.
4	Initialize Out	INITO L	This is the buffered BINIT L signal used in the device interface for general initialization.
5	Bus Initialize	BINIT L	When asserted, this signal brings all drive lines to their non-asserted state (except INITO L).
6	Bus Interrupt Acknowledge (Out)	BIAKO L	This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must continue to be passed until a new BIAKI L is generated.
7	Bus Interrupt Acknowledge (In)	BIAKI L	This signal is the response of the processor to BIRQ L true. This signal is daisy-chained so that the first requesting device blocks the signal, while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be deasserted by the requesting device.
8	Asynchronous Bus Interrupt Request	BIRQ L	This request is generated when a RQST signal and the appropriate Interrupt Enable signal become valid. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal, or the removal of the appropriate interrupt enable, or by the removal of the appropriate request signal.
17 10	Device Interrupt Request Signal	RQSTA H RQSTB H	When asserted with the enable A/B flip-flop asserted, this signal causes BIRQ L to be asserted on the bus. This signal line normally stays asserted until the request is serviced.
16 11	Interrupt Enable Status	ENA ST H ENB ST H	This signal indicates the state of the interrupt enable A/B internal flip-flop which is controlled by the signal line ENA/B DATA H and the ENA/B CLK H clock line.

Table A-1 DC003 Signals (Cont)

Pin	I/O Name	Symbol	Function
15 12	Interrupt Enable Date	ENA DATA H ENB DATA H	The level on this line, in conjunction with the ENA/B CLK H signal, determines the state of the internal interrupt enable A flip-flop. The output of this flip-flop is monitored by the ENA/B ST H signal.
14 13	Interrupt Enable clock	ENA CLK H ENB CLK H	When asserted (on the positive edge), interrupt enable A/B flip-flop assumes the state of the ENA/B DATA H signal line.

A.3 DC004 PROTOCOL IC

The protocol chip is a 20-pin DIL device that selects the registers, providing the signals necessary to control data flow to and from up to four word registers (eight bytes). Bus signals can be directly attached to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed so that, if close tolerance is not wanted, only an external 1-kilohm (+ or – 20%) resistor is needed. External RCs can be added to change the delay. Maximum current taken from the Vcc supply is 120 mA.

Figure A-4 is a simplified logic diagram of the DC004 IC. Signal timing in relation to different loads is shown in Figure A-5. Signal and pin definitions for the DC004 are shown in Table A-2.

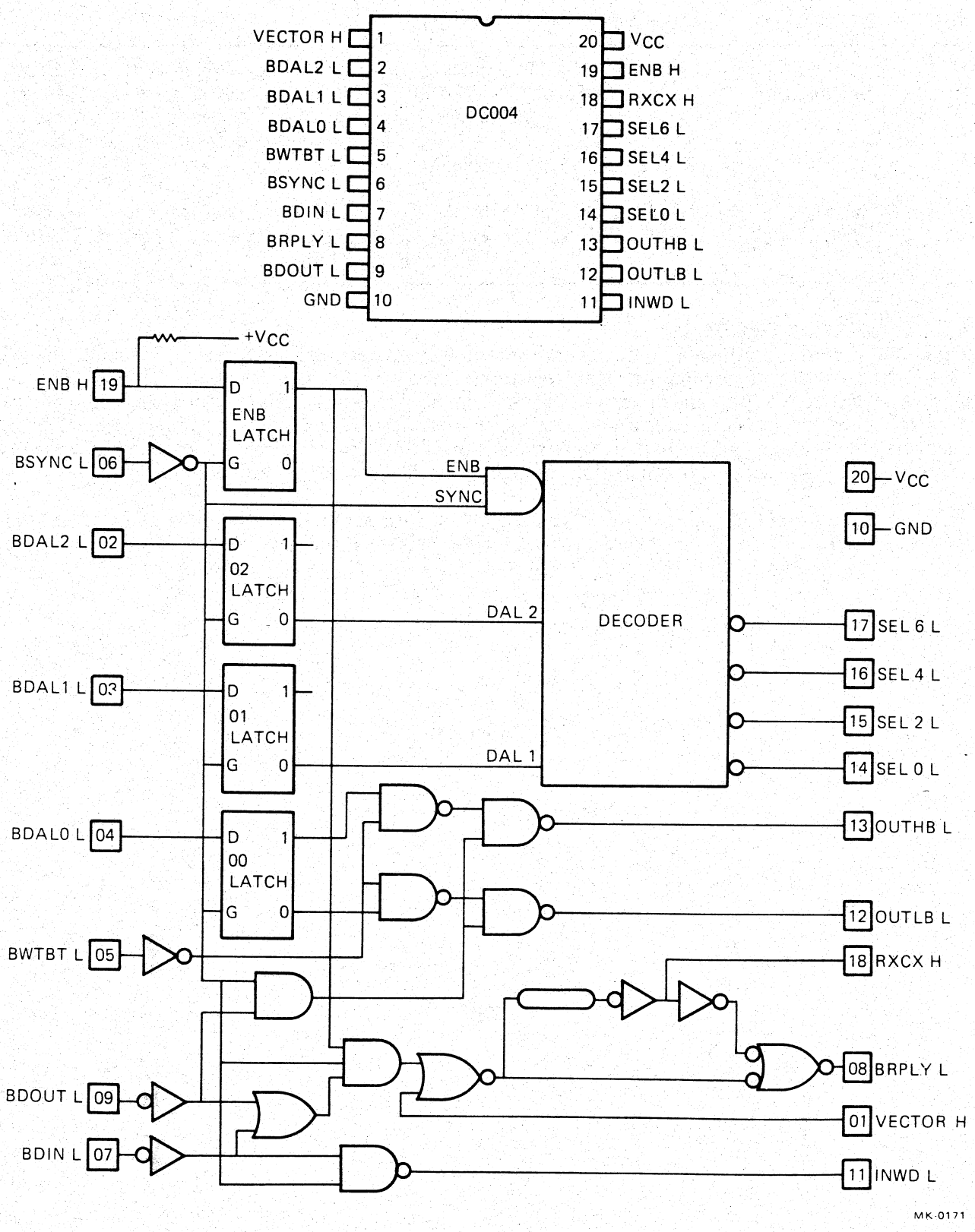
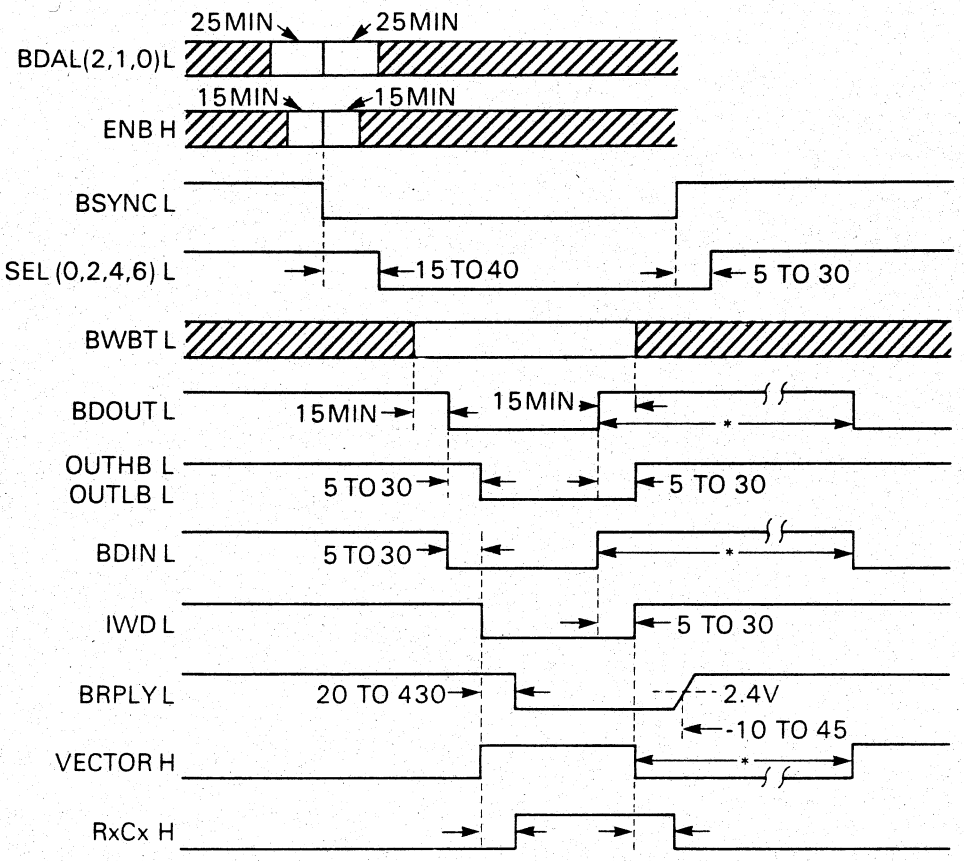


Figure A-4 DC004 Simplified Logic Diagram



* TIME REQUIRED TO DISCHARGE RxCx FROM ANY CONDITION ASSERTED = 150ns

NOTE:

TIMES ARE IN NANOSECONDS

Figure A-5 DC004 Timing Diagram

Table A-2 DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	**Vector** – This input causes BRPLY L to be generated through the delay circuit. It is independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	**Bus Data Address Lines** – These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	**Bus Write Byte** – While the BDOUT L input is asserted, this signal indicates a byte or word operation: asserted = byte, not asserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	**Bus Synchronize** – At the assert edge of this signal, address information is trapped in four latches. When not asserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	**Bus Data In** – This is a strobe signal to effect a data-input transaction. Generates BRPLY L through the delay circuit and INWD L.
8	BRPLY L	**Bus Reply** – This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or BDOUT L, and BSYNC L and latched ENB H.
9	BDOUT L	**Bus Data Out** – This is a strobe signal to effect a data-output transaction. Decoded with BWTBT L and BDAL0 L to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWD L	**In Word** – Used to gate (read) data from a selected register to the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUTLB L OUTHB L	**Out Low Byte, Out High Byte** – Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	**Select Lines** – One of these four signals is true as a function of BDAL2 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and, once asserted, are not deasserted until BSYNC L is deasserted.
18	RXCX	**External Resistor Capacitor Node** – This node is provided to change the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to Vcc and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	**Enable** – This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

A.4 DC005 BUS TRANSCEIVER IC

The 4-bit transceiver is a 20-pin DIL low-power Schottky device for primary use in peripheral device interfaces. It functions as a bidirectional buffer between a data bus and peripheral device logic. In addition to the isolation function, it also provides a comparison circuit for address selection, and a constant generator, useful for interrupt vector addresses. The bus I/O port provides high-impedance inputs and open-collector outputs to allow direct connection to the data bus of a computer. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA tri-state drivers. Data on this port has the opposite polarity to the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs and to generate the signal MATCH. The MATCH output is open-collector, which allows the output of more than one transceiver to be wire-ANDed to form a combined address match signal. The address jumpers can also be put into a third logical state that disconnects that jumper from the address match, allowing for 'don't care' address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant, that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three operation states: receiver data, transmit data, and disable.

Figure A-6 is a simplified logic diagram of the DC005 IC. Timing for the functions is shown in Figure A-7. Signal and pin definitions for the DC005 are given in Table A-3.

Table A-3 DC005 Pin/Signal Descriptions

Pin	Name	Function
12 11 9 8	BUS0 L BUS1 L BUS2 L BUS3 L	**Bus Data** – This set of four lines makes up the bus side of the transceiver. Open-collector outputs; high-impedance inputs; low = 1.
18 17 7 6	DAT0 H DAT1 H DAT2 H DAT3 H	**Peripheral Device Data** – These four tri-state lines carry the inverted received data from BUS<3:0> when the transceiver is in the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS<3:0>. When in the disabled mode, these lines go open (high impedance). High = 1.
14 15 16	JV1 H JV2 H JV3 H	**Vector Jumpers** – These inputs, with internal pull-down resistors, directly drive BUS<3:1>. A low or open on the jumper pin causes an open condition on the corresponding BUS pin if XMIT H is low. A high causes a 1 (low) to be transmitted on the BUS pin. Note that BUS0 L is not controlled by any jumper input.
13	MENB L	**Match Enable** – A low on this line enables the MATCH output. A high forces MATCH low, overriding the match circuit.
3	MATCH H	**Address Match** – When BUS<3:1> matches the state of JA<3:1> and MENB L is low, this output is open; otherwise, it is low.

Table A-3 DC005 Pin/Signal Descriptions (Cont)

Pin	Name	Function
1 2 19	JA1 L JA2 L JA3 L	**Address Jumpers** – A connection to ground on these inputs allows a match to occur with a 1 (low) on the corresponding BUS line. An open allows a match with a 0 (high). A connection to Vcc disconnects the corresponding address bit from the comparison.
5 4	XMIT H REC H	**Control Inputs** – These lines control the operation of the transceiver as follows. **REC XMIT** 0 0 DISABLE: BUS and DAT open 0 1 XMIT DATA: DAT to BUS 1 0 RECEIVE: BUS to DAT 1 1 RECEIVE: BUS to DAT To prevent tri-state overlap conditions an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode, and delays the enabling of tri-state drivers on the DAT lines. This action is independent of the DISABLE mode.

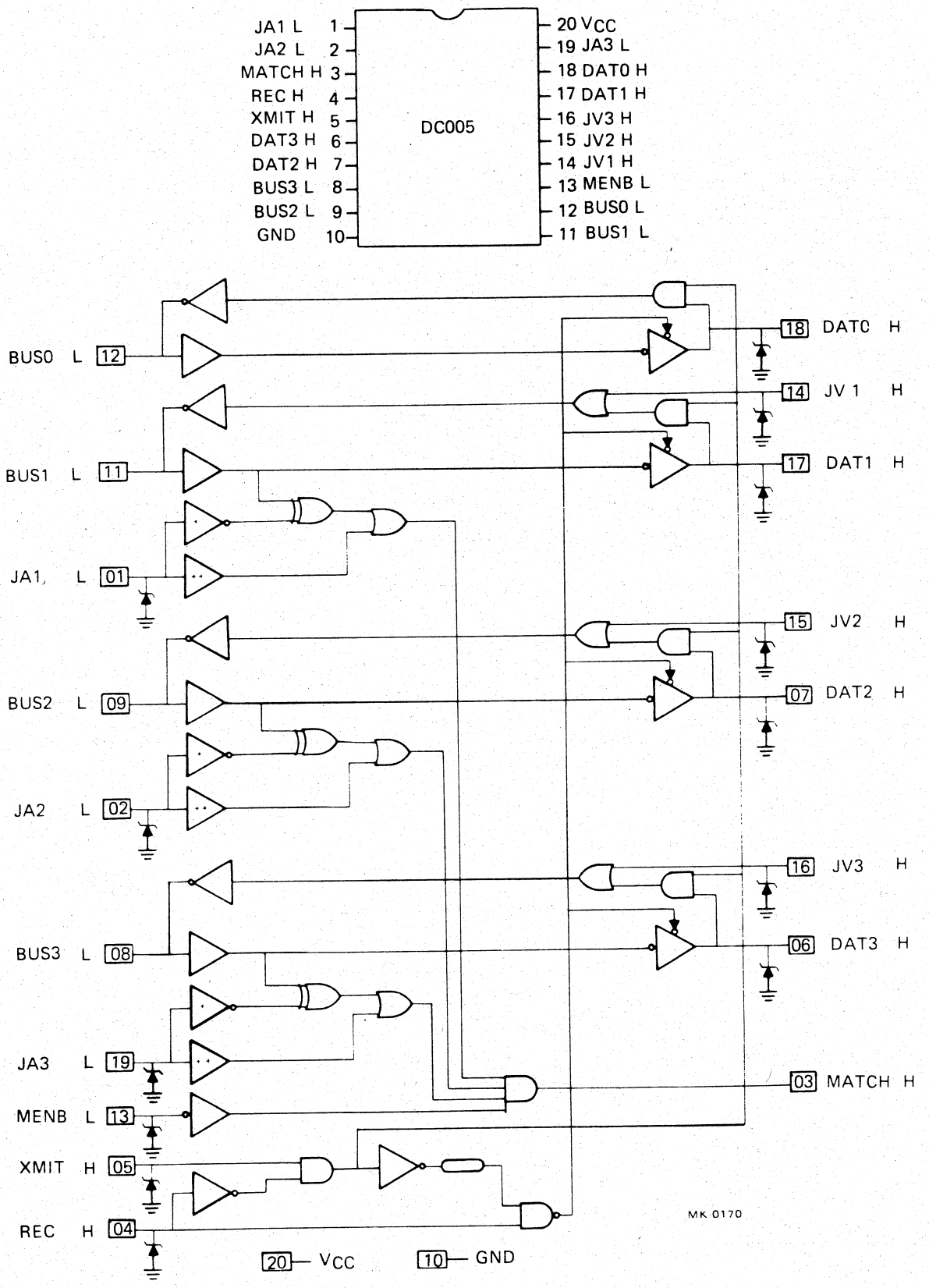


Figure A-6 DC005 Simplified Logic Diagram

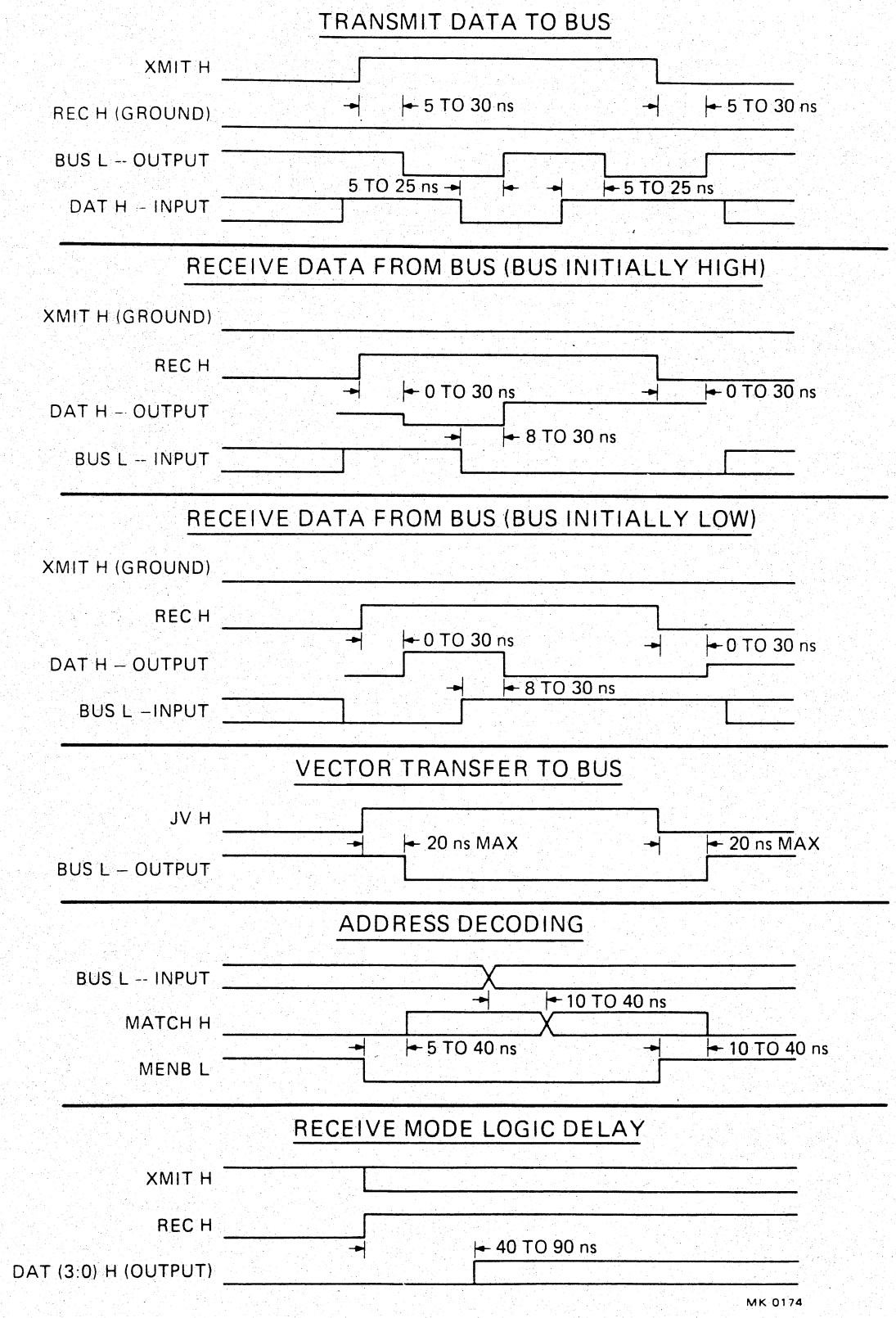


Figure A-7 DC005 Timing Diagram

A.5 DC367B SEMI-CUSTOM VLSI IC

A.5.1 Description

The DC367B is a DIGITAL special VLSI semi-custom IC implemented in CMOS technology. It is packaged in a 68-pin plastic leaded chip carrier (PLCC), and is either socket or surface mounted.

The DC367B contains the following functional items: four UARTs, one 16-output baud-rate generator, all necessary DZQ11 registers, transmit, receive and silo control logic, multiplexers, bi-directional buffers and other logic. Figure 5-10 shows the contents of the device, and Section 5.4 gives a description of the circuitry. Some specifications of the device will be given here, together with a pin description.

A.5.2 Pin Layout

Figure A-8 shows the layout linking pin position to pin numbers and names. Table A-4 lists the names, pin numbers, and describes the function.

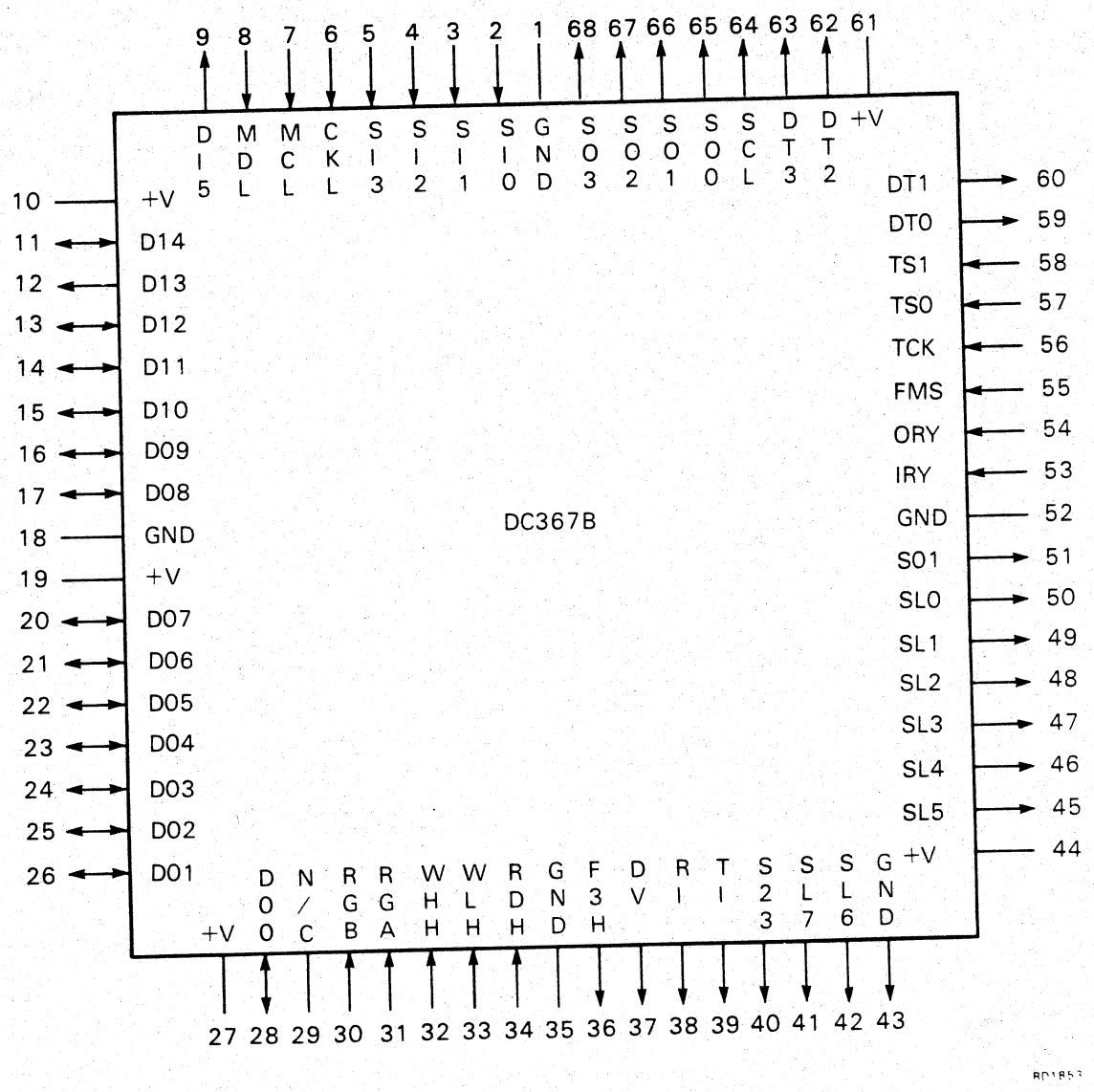


Figure A-8 Pin Layout of the DC367B

Table A-4 DC367B Pin/Signal Descriptions

Pin	Mnemonic	Function
1	GND	**GROUND** – Connects to 0 V
2	SI0	**SERIAL INPUT 0** – Data input line 0
3	SI1	**SERIAL INPUT 1** – Data input line 1
4	SI2	**SERIAL INPUT 2** – Data input line 2
5	SI3	**SERIAL INPUT 3** – Data input line 3
6	CKL	**CLOCK** – 5.0688 MHz clock, active low.
7	MCL	**MASTER CLEAR LOW** – Clears all registers except DTR registers.
8	MDL	**MODEM CLEAR LOW** – Clears all registers including DTR registers.
9	D15	**DATA LINE 15** – Connects to DAL15 H; tri-state output only, not an input.
10	+V	**+5 V** – Connects to +5 V.
11	D14	**DATA LINE 14** – Connects to DAL14 H; bi-directional I/O line.
12	D13	**DATA LINE 13** – Connects to DAL13 H; tri-state output only, not an input.
13 to 17	D12 to D08	**DATA LINES 12/08** – Connects to DAL12 H through to DAL08 H; bi-directional I/O lines.
18	GND	**GROUND** – Connects to 0 V.
19	+V	**+5 V** – Connects to +5 V.
20 to 26	D07 to D01	**DATA LINES 07/01** – Connects to DAL07 H through DAL01 H; bi-directional I/O lines.
27	+V1	**+5 V** – Connects to +5 V.
28	D00	**DATA LINE 00** – Connects to DAL00 H; bi-directional I/O line.
29	N/C	**NOT CONNECTED** – Spare, not connected.
30	RGB	**REGISTER ADDRESS B/A** – RGB and RGA form the address of the
31	RGA	register in read/write operations.
32	WHH	**WRITE HI-BYTE HIGH** – Write strobe to high byte of a register.
33	WLH	**WRITE LO-BYTE HIGH** – Write strobe to low byte of a register.
34	RDH	**READ HIGH** – Read strobe from a register.
35	GND	**GROUND** – Connects to 0 V.

Table A-4 DC367B Pin/Signal Descriptions (Cont)

Pin	Mnemonic	Function
36	F3H	**FRAMING ERROR ON LINE 3 H** – Output indicating a break on channel three; used to halt or boot a system.
37	DV	**DATA VALID** – A high level indicates data at end of silo is valid.
38	RI	**RECEIVER INTERRUPT** – Interrupts CPU if enabled on RDONE, or silo alarm as selected.
39	TI	**TRANSMITTER INTERRUPT** – Interrupts CPU if enabled, on TRDY.
40	S23	**SHIFT-IN SILOS TWO AND THREE** – Shift-in pulse for silo data on the two high-order silo chips.
41 to 42	SL7 to SL6	**SILO DATA 7 to 6** – Silo data lines 7 and 6, data shifted from DC367B into silo.
43	GND	**GROUND** – Connects to 0 V.
44	+V	**+5 V** – Connects to +5 V.
45 to 50	SL5 to SL0	**SILO DATA 5 to 0** – Silo data lines 5 to 0, data shifted from DC367B into silo.
51	S01	**SHIFT-IN SILOS ZERO AND ONE** – Shift-in pulse for silo data on the two low-order silo chips.
52	GND	**GROUND** – Connects to 0 V.
53	IRY	**IN READY** – Signal to the DC367B that all silos are ready for input.
54	ORY	**OUT READY** – Signal to the DC367B that all silos are ready for output.
55	FMS	**FULL MODEM SUPPORT** – An option (not used on DZQ11) which when asserted high forces the DC367B to leave D04 to D07 and D12 to D15 in their high-impedance state during read operations on the MSR. instead of asserting them zero. This allows other modem inputs (CTS and DSR), to be enabled to the DAL bus.
56	TCK	**TEST CLOCK** – Used for chip testing. With TS1 high, this is selected in place of the 19.8K baud internal baud rate.
57	TS0	**TEST 0** – When high, selects the baud rate generator outputs instead of the normal serial data outputs. SI0 and SI1 must be low to read the specific baud rate out. Used for chip testing.
58	TS1	**TEST 1** – When high, selects the TCK input instead of 19.8K baud for any UARTs whose line parameters have selected this baud rate. This allows the use of an external clock, of frequency 16 times the wanted baud rate.

Table A-4 DC367B Pin/Signal Descriptions (Cont)

Pin	Mnemonic	Function
59 to 60	DT0 to DT1	**DATA TERMINAL READY** – Active-low outputs of the DTR registers for lines 0 and 1.
61	+V	**+5 V** – Connect to +5 V.
62 to 63	DT2 to DT3	**DATA TERMINAL READY** – Active-low outputs of the DTR registers for lines 2 and 3.
64	SCL	**SILO CLEAR LOW** – Connects to the clear lines of the silo chips – output of the Master Scan Enable latch.
65 to 68	SO0 to SO3	**SERIAL OUT 0/3** – Active-high serial output lines. Idle state is high.

A.5.3 Specifications of Some Parameters

This paragraph gives specifications of some parameters not given in the main text.

A.5.3.1 Baud-Rate Accuracy – Table A-2 lists the baud rates and their divider ratios with respect to the 5.0688 MHz system clock, and gives the computed deviation from nominal.

Table A-5 Baud Rate Accuracy

LPR bits 11, 10, 09, 08	Baud Rate (in bits per second)	Divisor of 5.0688 MHz clock	% Frequency deviation from nominal
0 0 0 0	50	6336	0%
0 0 0 1	75	4224	0%
0 0 1 0	110	2880	0%
0 0 1 1	134.5	2352	+ 0.144%
0 1 0 0	150	2112	0%
0 1 0 1	300	1056	0%
0 1 1 0	600	528	0%
0 1 1 1	1200	264	0%
1 0 0 0	1800	176	0%
1 0 0 1	2000	158	+ 0.253%
1 0 1 0	2400	132	0%
1 0 1 1	3600	88	0%

Table A-5 Baud Rate Accuracy (Cont)

LPR bits 11, 10, 09, 08	Baud Rate (in bits per second)	Divisor of 5.0688 MHz clock	% Frequency deviation from nominal
1 1 0 0	4800	66	0%
1 1 0 1	7200	44	0%
1 1 1 0	9600	33	0%
1 1 1 1	19800	16	0%(**)

(**) Because the standard is 19200 baud, this option is not supported, as 19800 baud represents a +3.125% deviation which is not acceptable.

A.5.3.2 Receiver Parameters – The receiver will accept an edge misalignment of up to 40% (more accurately 43.75%), which represents one sixteenth of a bit from a 50% deviation (as a result of using a 16× clock). This edge misalignment may be caused by either edge jitter or an accumulation of edge errors caused by an incorrect clock over the full character transmission.

The receiver will also work down to a half stop bit between received characters.

A.5.3.3 Read/Write Pulses and Data Delay – Each write pulse (WHH and WLH) has to be 390 ns minimum. Data may stay unsteady up to 150 ns after the pulse, but must be steady from then until 45 ns after the pulse has been removed. These specifications will guarantee operation in worst-case commercial conditions (0 to 70 degrees centigrade, 4.75 to 5.25 volts).

With read operations, there is a 50 ns delay worst case between RDH being asserted/de-asserted and data being steady or being removed (high impedance) from the I/O lines.

A.6 3341 FIFO SERIAL MEMORY

The 3341 first-in-first-out memory chip asserts Input Ready when it is ready to load data. Each time Shift In is asserted, the chip accepts four bits of parallel data. When the Shift In pin is de-asserted, Input Ready also becomes de-asserted after a short delay. When both pins are Low, data starts to shift to the output end of the 64 × 4-bit register.

When data reaches the output, it asserts Output Ready. When Shift Out is asserted, the chip places the data in the output latches (Figure A-9). When the Shift Out pin is de-asserted, Output Ready also becomes de-asserted after a short delay. When both pins are Low, the next data (if available), 'bubbles' down to the output.

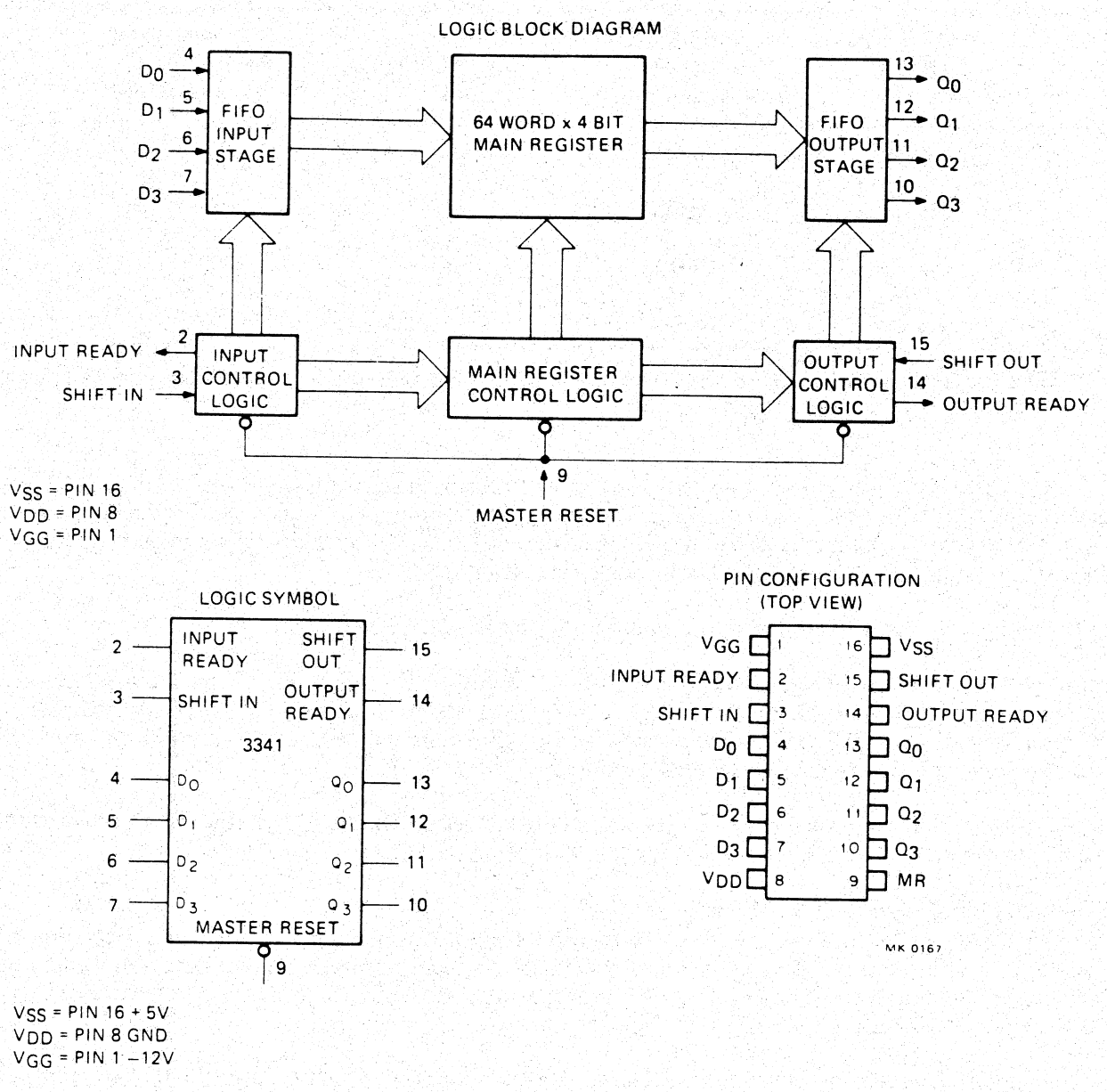


Figure A-9 3341 FIFO Serial Memory

APPENDIX B
GLOSSARY OF TERMS

B.1 SCOPE

This appendix contains a glossary of terms used in this manual. The terms are in alphabetic order for easy reference.

B.2 GLOSSARY

Asynchronous A method of serial transmission in which data is preceded by a start bit and followed by a stop bit. The receiver provides the average timing to identify the data bits.

Auto-answer The facility of a modem or terminal to automatically answer a call.

BDAL Bus data and address line.

Base address The address of the CSR.

CSR Control and status register

CCITT Comite Consultatif International de Telephonie et de Telegraphie. An international standards committee for telephone, telegraph, and data communications networks.

Dataset See modem.

DIL Dual-in-line. The term describes ICs and components with two parallel rows of pins.

DMA Direct memory access. A method which allows a bus master to transfer data to or from system memory without using the host CPU.

Duplex A method of transmitting and receiving on the same channel at the same time.

EIA Electrical Industries of America. An American organization with the same function as CCITT.

EMC Electromagnetic compatibility. The term means compliance with field-strength, susceptibility and static discharge standards.

FCC Federal Communications Commission. An American organization which regulates and licences communications equipment.

FIFO First In First Out. The term describes a register or memory from which the oldest data is removed first. It is often referred to as a silo.

Floating address A CSR address assigned to an option which does not have a fixed address allocated. The address is dependent on other floating address devices connected to the bus.

Floating vector An interrupt vector assigned to an option which does not have a fixed vector allocated. The vector is dependent on other floating vector devices connected to the bus.

FRU Field-replaceable unit.

IC Integrated circuit.

I/O Input/output.

LSB Least-significant bit.

LSI-11 bus Another name for the Q-bus.

Modem The word is an abbreviation of MOdulator DEModulator. A modem interfaces a terminal to a transmission line. A modem is also called a dataset.

MSB Most-significant bit.

Multiplexer A circuit which connects a number of lines to one line.

Null modem A cable which allows two terminals which use modem control signals to be connected together directly. Only possible over short distances.

PCB Printed circuit board.

PLCC Plastic leaded chip carrier.

Protocol A set of rules which define the control and flow of data in a communications system.

Q-bus A global term for a specific DIGITAL bus on which the address and data are multiplexed.

Q22, Q18, and Q16 Terms used to define 22-, 18-, and 16-bit-address versions of the Q-bus.

RFI Radio frequency interference.

SMPS Switch-mode power supply

UART Universal asynchronous receiver transmitter. An IC used to transmit and receive serial asynchronous data on a channel.

Digital Equipment Corporation • Bedford, MA 01730