pdp11

DZ11
asynchronous multiplexer
technical manual

digital

EK-DZ110-TM-002

DZ11
asynchronous multiplexer
technical manual

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZ11 is an asynchronous multiplexer that provides an interface between a PDP-11 processor and eight asynchronous serial lines. It can be used with PDP-11 systems in a variety of applications that include communications processing, time-sharing, transaction processing, and real-time processing. Local operation to terminals or computers is possible at speeds up to 9600 baud using either EIA RS232C interfaces or 20 mA current loop signaling. Remote operation using the public switched telephone network is possible with DZ11 models offering EIA RS232C interfaces. Enough data set control is provided to permit dial-up (auto answer) operation with modems capable of full-duplex* operation such as the Bell models 103 or 113 or equivalent. Remote operation over private lines for full-duplex* point to point or full-duplex* multipoint as a control (master) station is also possible. Figure 1-1 depicts several of the possible applications for the DZ11 in a PDP-11 system.

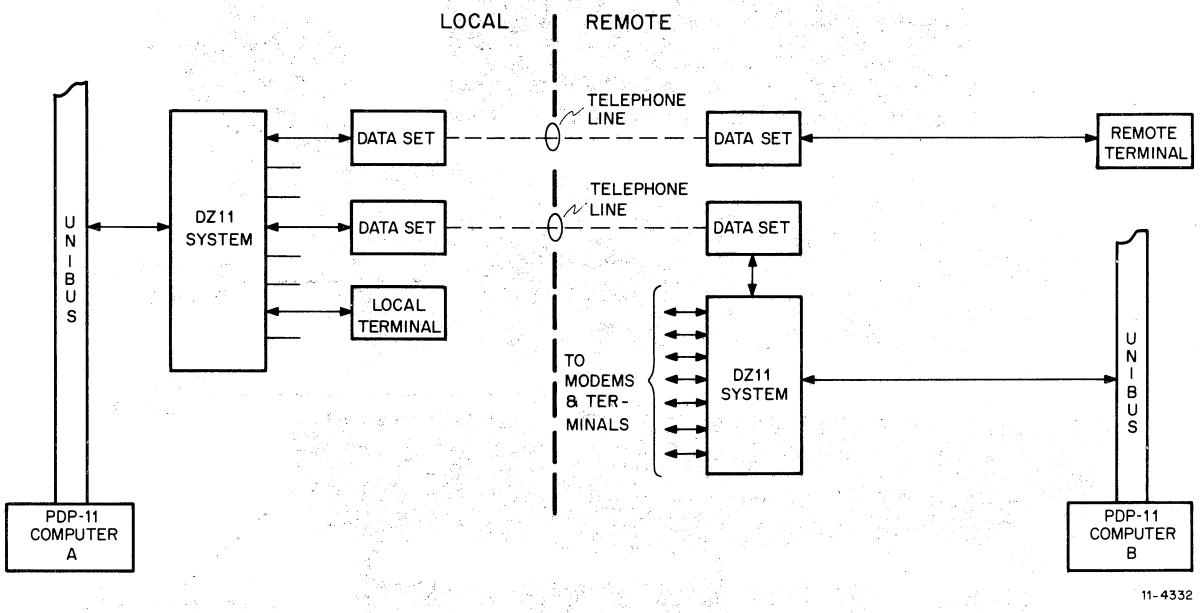


Figure 1-1 DZ11 System Applications

*The DZ11 data set control does not support half-duplex operations or the secondary transmit and receive operations available with some modems such as the Bell model 202, etc.

The DZ11 has several features that provide flexible control of parameters such as baud rate, character length, number of stop bits for each line, odd or even parity for each line, and transmitter-receiver interrupts. Additional features include limited data set control, zero receiver baud rate, break generation and detection, silo buffering of received data, module plug-in to hex SPC slots, and line turnaround.

Each DZ11 module provides for operation of eight asynchronous serial lines. Since the module interfaces to these channels with a 16-line distribution panel, 2 DZ11 modules can be used with 1 panel. Also note that the two versions of the DZ11 (EIA or 20 mA output) consist of different module and panel types. This fact allows a system to mix EIA and 20 mA by using multiple DZ11s.

1.2 PHYSICAL DESCRIPTION

The DZ11 (8-line configuration) comprises a single hex SPC module and a 13.34 cm (5.25 in), unpowered distribution panel, connected by a 4.6 m (15 ft) ribbon cable. Several types of interconnecting cables are used between the distribution panel and the modem or terminal, depending on the device. A 16-line configuration uses two modules and a single distribution panel connected by two ribbon cables. The DZ11 modules, cables, static filters,* and distribution panel are shown in Figures 1-2 and 1-3. The subsequent paragraphs present a detailed description of the physical and electrical specifications of the various DZ11 options and configurations.

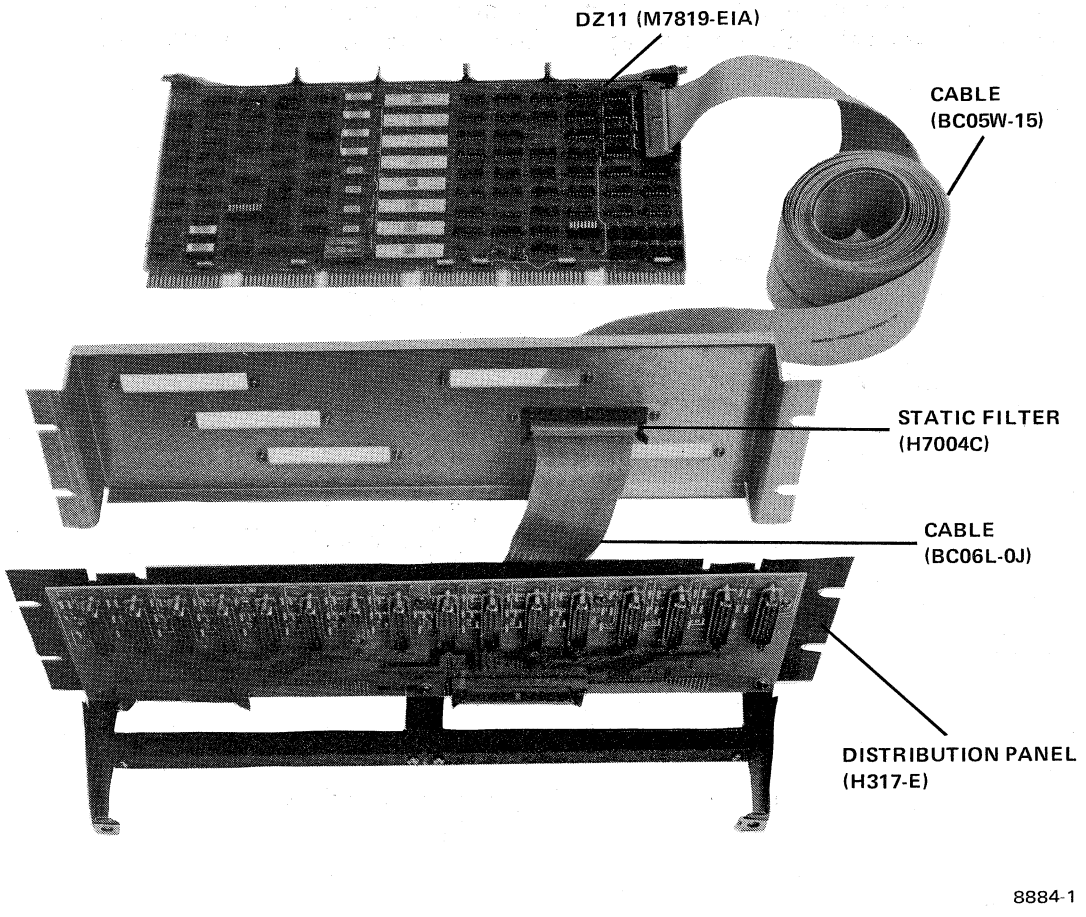


Figure 1-2 DZ11 EIA Module (M7819), Distribution Panel (H317-E), Static Filter (H7004C), and Cables (BC06L-0J and BC05W-15)

*Static filters are not supplied with earlier modules.

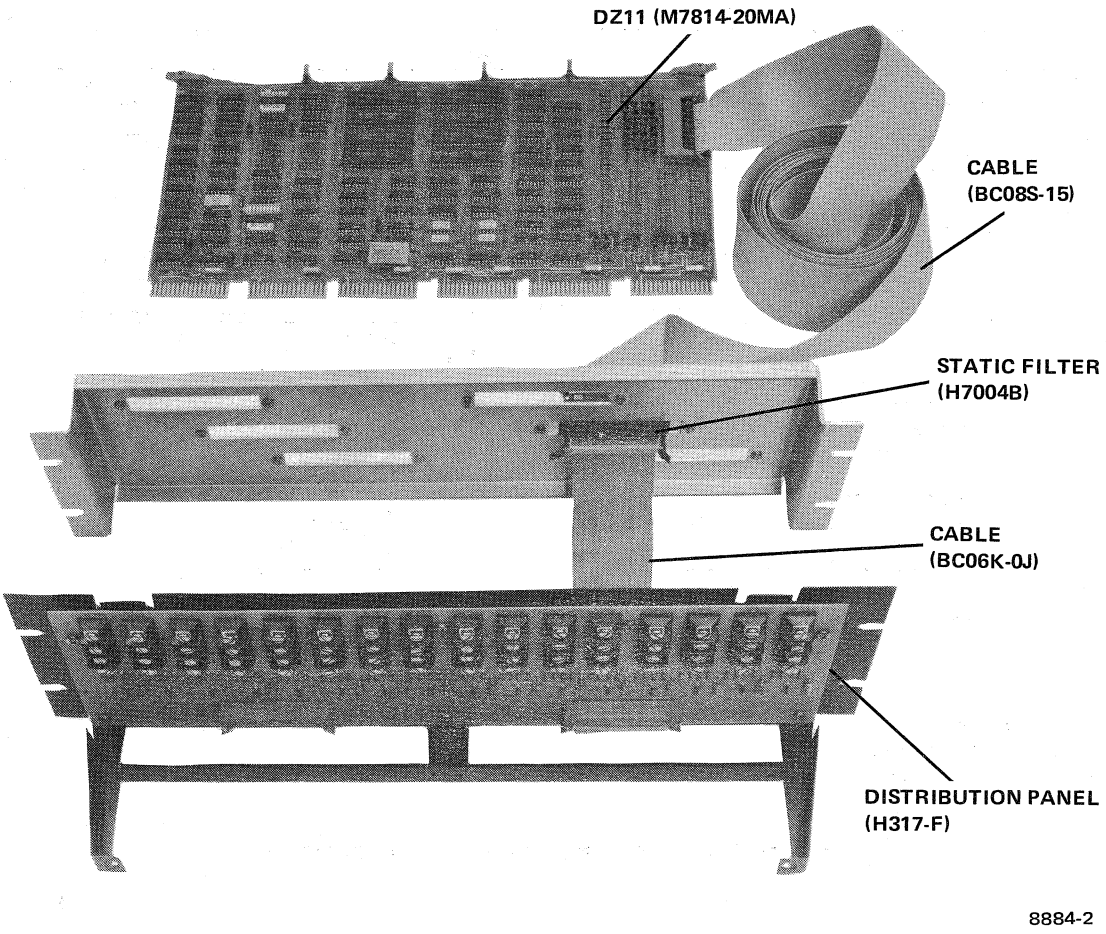


Figure 1-3 DZ11 20 mA Module (M7814), Distribution Panel (H317-F), Static Filter (H7004B), and Cables (BC06K-0J and BC08S-15)

1.2.1 DZ11 Configurations

The DZ11 can be supplied in six different configurations, each designated by a suffix letter (A–F). The DZ11-A and the DZ11-B options are EIA devices with partial modem control. The DZ11-E is the combination of a DZ11-A and a DZ11-B. The DZ11-C and the DZ11-D are 20 mA loop output versions. The DZ11-F is the combination of a DZ11-C and a DZ11-D. Table 1-1 lists the various option configurations and Figure 1-4 shows the required hardware for the various configurations.

The DZ11-A and DZ11-B each use an M7819 module that plugs into slot 2 or 3 of a DD11-B or any system unit with a hex SPC slot; however, slots in the PDP-11/20 BA11 box cannot be used. The H317-E distribution panel provides 16 communication lines from 2 M7819 modules (8 lines per module) and is included with the DZ11-A and DZ11-E configurations. The H317-F distribution panel provides 16 lines for the DZ11-C and DZ11-F configurations, which use the M7814 modules (20 mA system). The distribution panels require no power and can be mounted in an H960 48.26 cm (19 in) cabinet. Static filters (H7004C, EIA, and H7004B, 20 mA) are used to prevent problems caused by electrostatic discharge. A 50-conductor, flat, shielded cable, BC05W-15, connects from the M7819 module to the static filter. Cable BC06L-0J connects the static filter to the EIA distribution panel. A 40-conductor, flat, shielded cable, BC08S-15, connects from the M7814 module to the static filter. Cable BC06K-0J connects the static filter to the 20 mA distribution panel.

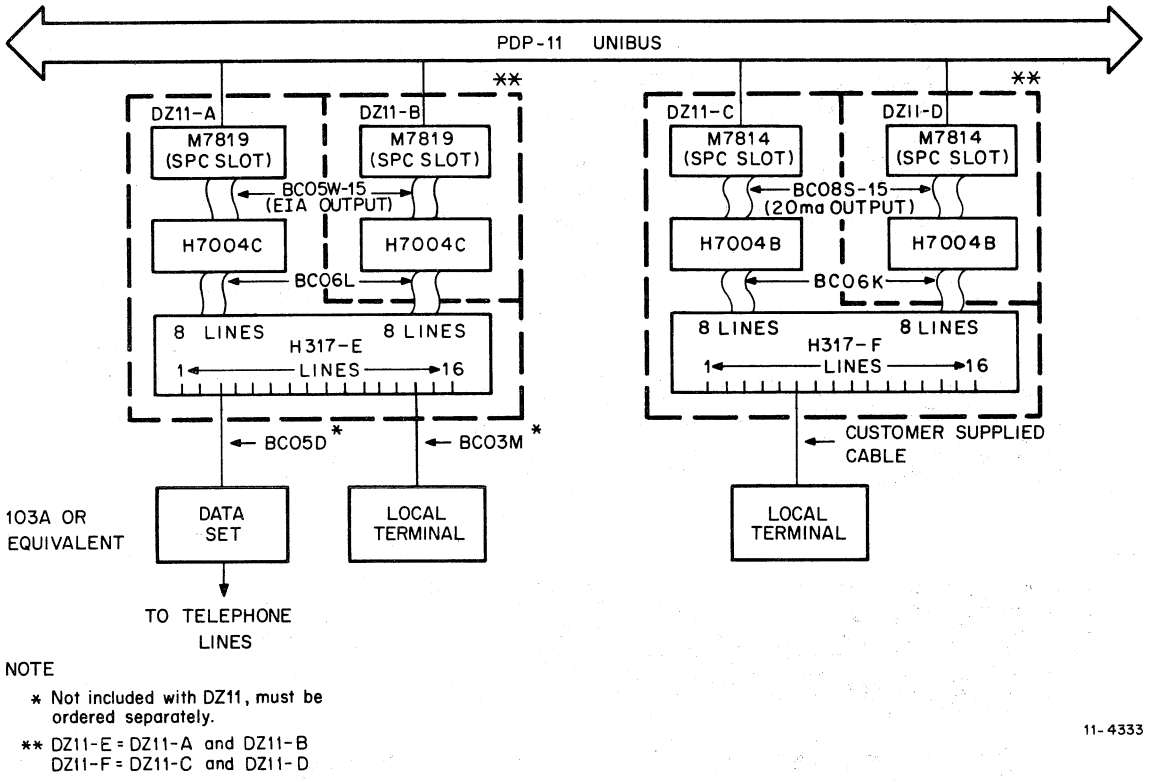


Figure 1-4 DZ11 Hardware Interconnections

Table 1-1 DZ11 Model Configurations

Model	Output	Module	Panel	Test Connector	Cables	Static Filter
DZ11-A	EIA	M7819	H317-E	H325/H327	BC05W, BC06L	H7004C
DZ11-B	EIA	M7819		H327	BC05W, BC06L	H7004C
DZ11-E	EIA	M7819 (2)	H317-E	H325/H327	BC05W (2), BC06L (2)	H7004C
DZ11-C	20 mA	M7814	H317-F	H3190	BC08S, BC06K	H7004B
DZ11-D	20 mA	M7814		H3190	BC08S, BC06K	H7004B
DZ11-F	20 mA	M7814 (2)	H317-F	H3190	BC08S (2), BC06K (2)	H7004B

NOTES

H327 will be replaced by H3271 in later units. H3190 is not supplied with early units. The shipping list will indicate which test connector, if any, is supplied.

H7004C, H7004B, BC06L, and BC06K are not supplied with early units. The shipping list will indicate which static filter and cable, if any, are supplied.

Modems or terminals are connected to the H317-E EIA panel by cables that attach to 16 DB25P cinch connectors. These cables are not provided with the DZ11. The BC05D-25 cable is recommended for data set interconnections, and the BC03M cable is recommended for local terminal interconnections. The BC05W-15 cable carries the data and control signals for all eight lines. Connections between terminals and the H317-F 20 mA panel are by customer-supplied cables to 16 (4-screw) terminal strips. The data signals for all eight lines are carried to the distribution panel by the BC08S-15 cable.

Two accessory test connectors, H325 and H3271*, are provided with each DZ11-A. The H325 plugs into an EIA connector on the distribution panel or on the end of the BC05D cable to loop back data and modem signals onto a single line. The H3271 connects to the module with the BC05W cable (two M7819 modules can be connected to one H3271) and staggers the data and modem lines as shown in Figure 1-5. The connectors are shown in Figure 1-6.

The 20 mA (M7814 module) options also have a staggered turnaround connector (H3190†). The H3190 connects to the M7814 using the BC08S cable and staggers the lines as shown in Figure 1-7.

A priority level 5 insert plugs into a socket on the M7819 or M7814 module to establish interrupts at level 5 on the Unibus.

Maximum configuration allows 16 DZ11 modules per Unibus.

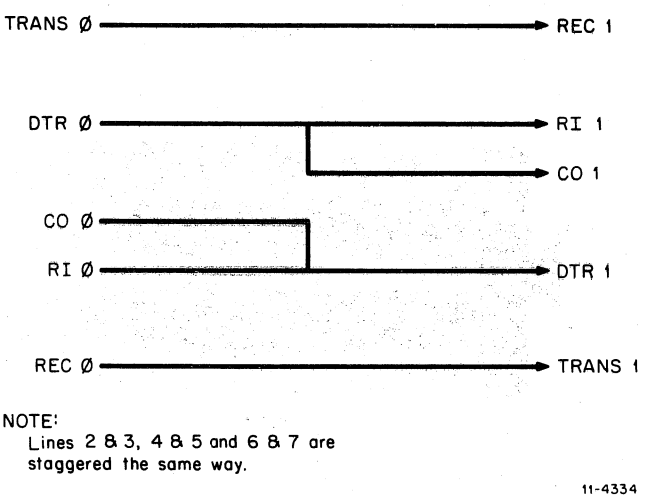
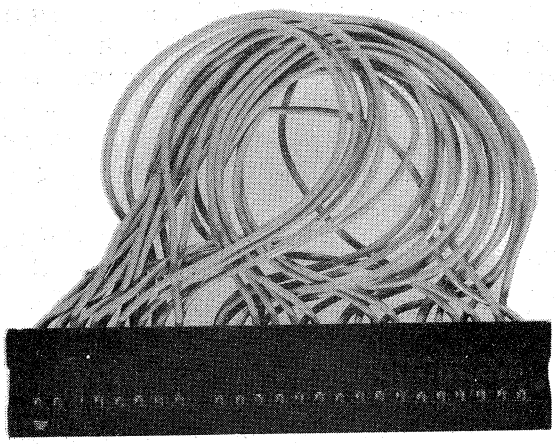


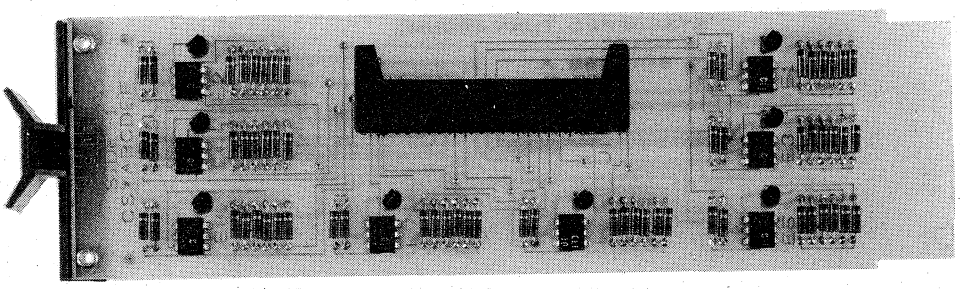
Figure 1-5 H3271 or H327 Turnaround

*This is a new item replacing the H327. The H327 may be used until the H3271 becomes available. The H327 plugs directly into J1 on the M7819 module.

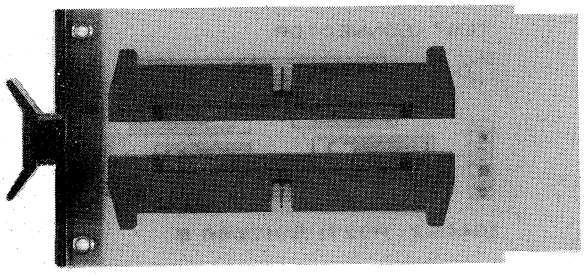
†This is a new item; check the shipping list for availability.



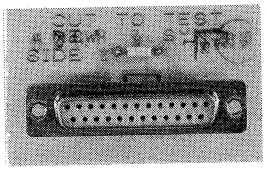
H327



H3190



H3271



H325

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Figure 1-6 Test Connectors H327, H3190, H3271, and H325

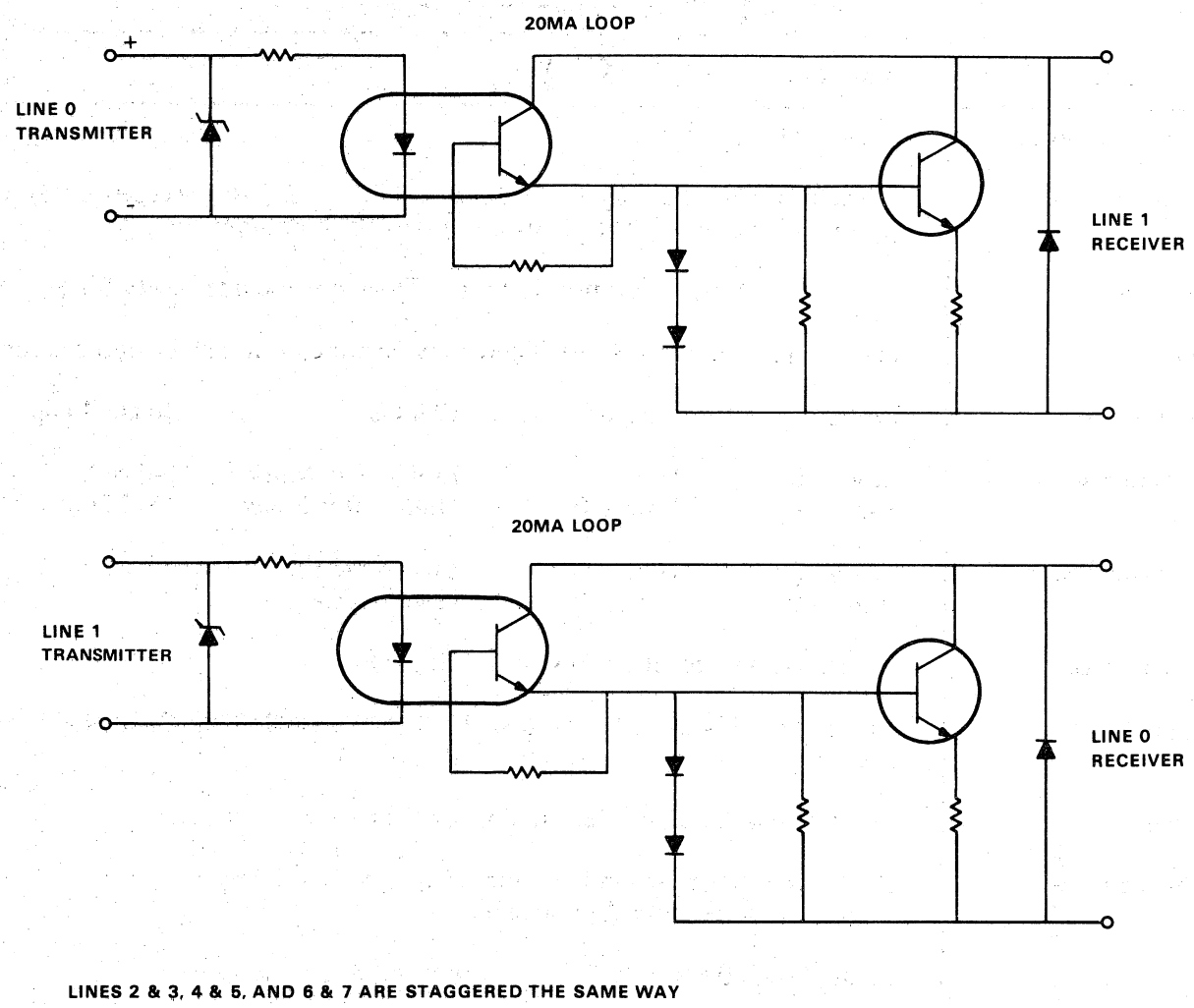


Figure 1-7 H3190 Staggered Line Turnaround

1.3 GENERAL SPECIFICATIONS

The following paragraphs contain electrical, environmental, and performance specifications for all DZ11 configurations. Table 1-2 lists the performance parameters of the DZ11.

Table 1-2 DZ11 Performance Parameters

Parameter	Description			
Operating Mode	Full-Duplex			
Data Format	Asynchronous, serial by bit, 1 start and 1, 1-1/2 (5-level codes only), or 2 stop bits supplied by the hardware under program control			
Character Size	5, 6, 7, or 8 bits; program-selectable. (Does not include parity bit.)			
Parity	Parity is program-selectable. There may be none, or it may be odd or even.			
Bit Polarities	**Unibus**	**Interface**	**EIA Out**	**20 mA Loop**
Data Signal	Low = 1 High = 0	High = 1 Low = 0	Low = 1 = Mark High = 0 = Space	0–5 mA 15–20 mA
Control Signal	Low = 1 High = 0	High = 1 Low = 0	Low = OFF High = ON	
Order of Bit	Transmission/reception low-order bit first			
Baud Rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600			
Breaks	Can be generated and detected on each line			
Throughput	21,940 characters/second = (bits/second × No. Lines × direction)/(Bits/Character) Example: (9600 × 8 × 2)/7 = 21,940 characters/second **NOTE** **The theoretical maximum is 21,940. Actual throughput depends on other factors such as type of CPU, system software, etc.**			

1.3.1 Outputs

1.3.1.1 DZ11-A, -B, and -E – Each line provides voltage levels and connector pinnings that conform to Electronic Industries Association (EIA) standard RS232C and CCITT recommendation V.24. The leads supported by this option are:*

Circuit AA (CCITT 101)	Pin 1	Protective Ground
Circuit AB (CCITT 102)	Pin 7	Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
Circuit BB (CCITT 104)	Pin 3	Received Data
Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CE (CCITT 125)	Pin 22	Ring Indicator
Circuit CF (CCITT 109	Pin 8	Carrier

NOTE
Signal ground and protective ground are connected.

1.3.1.2 DZ11-C, -D, and -F – Each line is a 20 mA current loop used for connection to local terminals. (No data set control is provided.) All lines are active and, therefore, can only drive a passive device. However, a pair of H319 20 mA receivers for each line may be used to convert from active to passive operation in order to allow the DZ11 to drive an active device. Refer to Appendix A for connection details.

1.3.2 Inputs

The PDP-11 Unibus is the input for all DZ11s. The DZ11-A, -B, -C, and -D present one unit load to the Unibus and the DZ11-E and -F present two unit loads to the Unibus. Four ac loads per module are presented to the Unibus in the EIA version and five ac loads per module are presented in the 20 mA version.

1.3.3 Power Requirements, DZ11-A, -B, and -E†

Typical (A)	Maximum (A)	
2.2	2.5	at +5.0 Vdc
0.13	0.15	at -15.0 Vdc
0.1	0.13	at +15.0 Vdc

1.3.4 Power Requirements, DZ11-C, -D, and -F†

Typical (A)	Maximum (A)	
2.1	2.3	at +5.0 Vdc
0.4	0.42	at -15.0 Vdc
0.12	0.15	at +15.0 Vdc

*Circuit CA (CCITT 105 – Request to Send) is connected to circuit CD (DTR) through a jumper on the distribution panel. This allows control of the Request to Send line for full-duplex modem applications that use the RTS circuit.

†DZ11-E and DZ11-F are twice the above given values.

1.3.5 Environmental Requirements – All DZ11s

Class C Environment Operating Temperature	5° to 50° C* (41° to 122° F)
Relative Humidity	10 to 95%, with a maximum wet bulb of 32° C (90° F) and a minimum dewpoint of 2° C (36° F)
Cooling	
DZ11-A, -B, -C, and -D	Air flow 1.416 l/second (3 cu. ft/min)
DZ11-E and -F	Air flow 2.832 l/second (6 cu. ft/min)
Heat Dissipation	
DZ11-A and -B	3.99 g·cal/second (57 Btu/hr)
DZ11-E	7.98 g·cal/second (114 Btu/hr)
DZ11-C and -D	3.85 g·cal/second (55 Btu/hr)
DZ11-F	7.7 g·cal/second (110 Btu/hr)

1.3.6 Distortion – DZ11-A, -B, and -E

The maximum "space to mark" and "mark to space" distortion allowed in a received character is 40 percent.

The maximum speed distortion allowed in a received character for 2000 baud is 3.8 percent. All other baud rates allow 4 percent. The maximum speed distortion from the transmitter for 2000 baud is 2.2 percent. All other baud rates have less than 2 percent.

1.3.7 Interrupts

RDONE	Occurs each time a character appears at the silo output.
SA	Silo Alarm. Occurs after 16 characters enter the silo. Rearmed by reading the silo. This interrupt disables the RDONE interrupt.
TRDY	Occurs when the scanner finds a line ready to transmit on.

NOTE
There are no modem interrupts.

Normally, a level 5 priority plug is supplied. The interface level can be modified to level 4, 6, or 7 by using the proper priority plug.

1.3.8 Line Speed

The baud rate for a line (both transmitter and receiver) is program-selectable. Also, the receiver for each line can be individually turned on or off under program control. (See Table 1-2 for a list of available baud rates.)

*Maximum operating temperature is reduced 1.8° C per 1000 meters (1.0° F per 1000 feet) for operation at altitudes above sea level.

1.3.9 Distance (DZ11-A, -B, and -E)

The recommended distance from computer to DZ11 is 15 m (50 ft) at up to 9600 baud with a BC05D cable or equivalent. Operation beyond 15 m (50 ft) does not conform to the RS232C or CCITT V.24 specifications. However, operation will often be possible at greater distance depending on the terminal equipment, type of cable, speed of operation, and electrical environment. Reliable communication over long cables depends on the absence of excessive electrical noise. For these reasons, DIGITAL cannot guarantee error-free communication beyond 15 m (50 ft). However, the EIA versions of the DZ11 may be connected to local DIGITAL terminals and most other terminals at distances beyond 15 m (50 ft) with satisfactory results if the terminal and computer are located in the same building, in a modern office environment. Shielded twisted pair wire (Belden 8777 or equivalent) is recommended and is used in the BC03M null modem cable.

With cables made with shielded twisted pair wire, such as the Belden 8777, the following rate/distance table may be used as a guide. This chart is for informational purposes only and is not to be construed as a warranty by Digital Equipment Corporation of error-free DZ11 operation at these speeds and distances under all circumstances.

90 m (300 ft) at 9600 baud
300 m (1000 ft) at 4800 baud
300 m (1000 ft) at 2400 baud
900 m (3000 ft) at 1200 baud
1500 m (5000 ft) at 300 baud

NOTE

The ground potential difference between the DZ11 and terminal must not exceed 2 V. This requirement will generally limit operation to within a single building served by one ac power service. In other cases, or in noisy electrical environments, 20 mA operation should be used.

1.3.10 Distance (DZ11-C, -D, and -F)

The length of cable that may be used reliably is a function of electrical noise, loop resistance, cable type, and speed of operation. The following chart is given as a guide; however, there is no guarantee of error-free operation under all circumstances.

Speed (Baud)	Belden 8777, 22 AWG, shielded, twisted pairs (shields floating) (DEC P/N 9107723)	22 AWG, 4 conductor inside station wire (DEC P/N 9105856-4)
9600	150 m (500 ft)	300 m (1000 ft)
4800	300 m (1000 ft)	540 m (1800 ft)
2400	600 m (2000 ft)	900 m (3000 ft)
1200 and below	1200 m (4000 ft)	1500 m (5000 ft)

1.4 FUNCTIONAL DESCRIPTION

The following paragraphs present a general description of DZ11 operation. Figure 1-8 is a general functional block diagram that divides the DZ11 into three basic components: Unibus interface, control logic, and line interface.

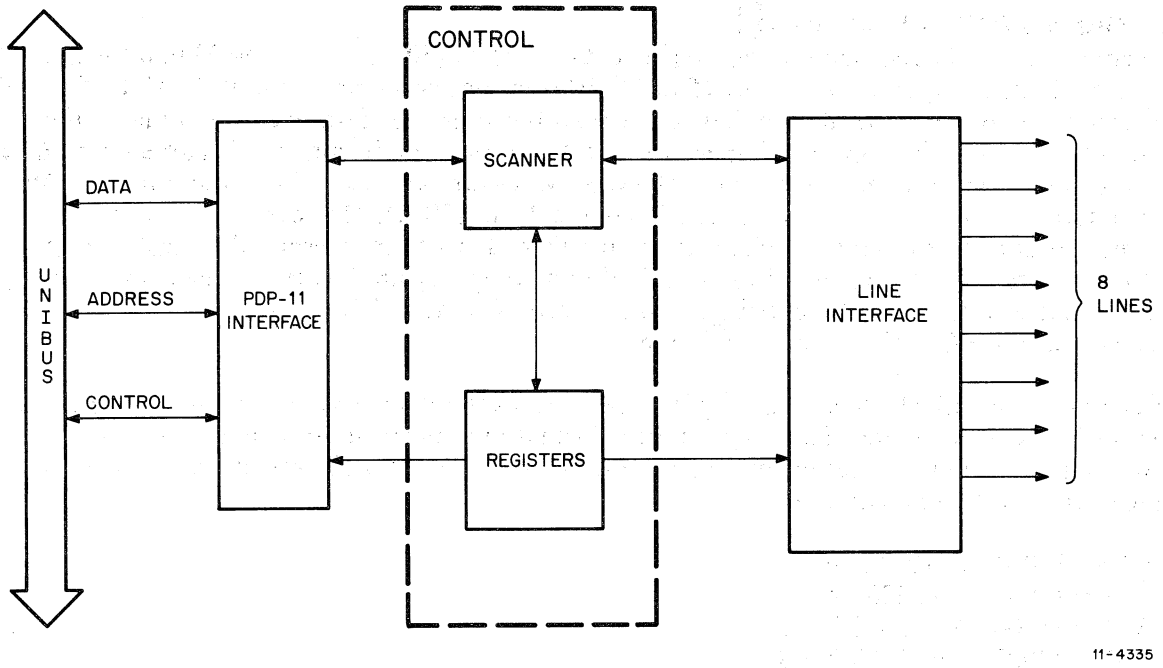


Figure 1-8 General Functional Block Diagram

1.4.1 PDP-11 Unibus Interface

The PDP-11 Unibus interface component of the DZ11 handles all transactions between the Unibus and the DZ11 control logic. The Unibus interface performs three functions: data handling, address recognition, and interrupt control. In its data handling function, the interface routes data to and from the various registers in the control logic and provides the voltage conditioning necessary to transmit and receive data to and from the PDP-11 Unibus. The address recognition and control logic activates the proper load and read signals when it recognizes its preselected address on the Unibus. These signals are used by the data handling function to route the incoming and outgoing data to the desired locations. The interrupt control function initiates and controls interrupt processing between the DZ11 and the PDP-11 processor.

1.4.2 Control Logic

The control logic provides the required timing and control signals to handle all transmitter and receiver operations. The control logic can be divided into two major sections: the scanner and the registers.

The scanner continuously examines each line in succession and, based on information from the line interface and the registers, generates signals that cause data to flow to or from the appropriate line. The scanner comprises a 5.068 MHz oscillator (clock), a 64-word FIFO receiver buffer, a 4-phase clocking network, and other control generating logic.

The DZ11 uses four device registers in a manner that yields six unique and accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input and output data, monitor control signal conditioning, and establish DZ11 operating status. Depending on their functions, some of the registers are accessible in bytes or words; others are restricted to word-only operation. Registers can be read or loaded (written), depending on the operation. The ability to read or write a register allows the use of two of the device registers as four independent registers.

1.4.3 Line Interface

Two of the most important operations in the DZ11 are the conversions from serial-to-parallel and parallel-to-serial data formats. These conversions are required since the DZ11 is located between the PDP-11 Unibus (a parallel data path) and either local terminals or telephone lines (serial data paths). Conversions for each line in the DZ11 are performed by independent universal asynchronous receiver-transmitter (UART) integrated circuits. Another component of the line interface, the line receiver or driver, converts the TTL voltage levels in the DZ11 so that they correspond to those in the external device input lines (modem or terminal).

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZ11 Asynchronous Multiplexer.

2.2 CONFIGURATION DIFFERENCES

The DZ11 can be supplied with or without a distribution panel. The DZ11-B and -D do not have distribution panels. The following list describes the variations.

DZ11-A	EIA level conversion with distribution panel (8 lines)
DZ11-B	EIA level conversion without distribution panel (8 lines)
DZ11-C	20 mA loop conversion with distribution panel (8 lines)
DZ11-D	20 mA loop conversion without distribution panel (8 lines)
DZ11-E	DZ11-A and DZ11-B (16 lines)
DZ11-F	DZ11-C and DZ11-D (16 lines)

2.3 UNPACKING AND INSPECTION

The DZ11 is packaged in accordance with commercial packaging practices. First, remove all packing material and check the equipment against the shipping list. (Table 2-1 contains a list of supplied items per configuration.) Report damage or shortages to the shipper immediately and notify the DIGITAL representative. Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths.

2.4 INSTALLATION PROCEDURE

The following paragraphs should be followed to install the DZ11 option in a PDP-11 system.

2.4.1 H317 Distribution Panel and Static Filter Installation

Install the H317 distribution panel and static filters according to unit assembly drawing D-UA-DZ11-0-0.

2.4.1.1 EIA Option – For the DZ11-A or DZ11-E option, check to ensure that all of the machine-insertable jumpers on the distribution panel are in place. (See Drawing E-UA-5411928-0-0 for jumper locations.) These jumpers are in anticipation of future use of the DZ11 with modems other than the 103; however, two of the jumpers are now functional. The jumper labeled DTR (refer to D-CS-5911928-0-1) connects DTR to pin 4 or Request to Send. This allows the DZ11 to assert both DTR and RTS if using a modem which requires control of RTS. The jumper labeled BUSY is also connected to the DTR lead for use in modems that implement the Force Busy function. This jumper should normally be cut out unless the modem has the Force Busy feature and the system software is implemented to control it.

Table 2-1 Items Supplied Per Configuration

Quantity	Description	A	B	E	C	D	F
1	M7819 module	X	X	*			
1	H7004C static filter (EIA)	X	X	*			
1	H3271 test connector†	X		X			
1	BC06L-0J filter cable (EIA)	X	X	*			
1	H317-E distribution panel assembly	X		X			
1	H325 test connector	X		X			
1	BC05W-15 cable	X	X	*			
1	Print set (B-TC-DZ11-0-6) DZ11, A, B, and C order number MP00132	X	X	X			
1	Software kit	X		X	X		X
1	Panel and static filter mounting hardware set	X		X	X		X
1	Priority insert (5)	X	X	*	X	X	*
1	DZ11 User's Manual (EK-DZ110-OP-01)	X		X	X		X
1	M7814 module				X	X	*
1	H7004B static filter (20 mA)				X	X	*
1	BC08S cable				X	X	*
1	BC06K-0J filter cable (20 mA)				X	X	*
1	H317-F distribution panel assembly				X		X
1	Print set (B-TC-DZ11-0-11) DZ11, C, D, and F order number MP00253				X	X	X
1	H3190 test connector‡				X	X	*

*Shipment contains two of the items listed.

†*New item:* An H327 will be shipped with each M7819 unit until the H3271 becomes available. The shipping list will indicate which test connector is supplied.

‡*New item:* The shipping list will include the H3190 test connector when supplied.

2.4.1.2 20 mA Option – For the DZ11-C or DZ11-F option, refer to D-UA-5411974-0-0. Each line has a jumper on the distribution panel (W1 through W16) which should be in if the terminal operates at 300 baud or less. The jumper should be removed for higher baud rates.

2.4.2 M7819 Module Installation

To install the M7819 module, perform the following procedure.

1. Ensure that the priority insert (level 5) is properly seated in socket E52 on the M7819 module(s). (Refer to drawing D-UA-M7819-0-0.)

2. Refer to Paragraph 3.1.1 for descriptions of the address assignments. Set the switches at E81 so that the module will respond to its assigned address. When a switch is closed (on), a binary 1 is decoded. When a switch is open (off), a binary 0 is decoded. Note that the switch labeled 1 corresponds to bit 3, 2 corresponds to bit 4, etc. (See Figure 2-1.)

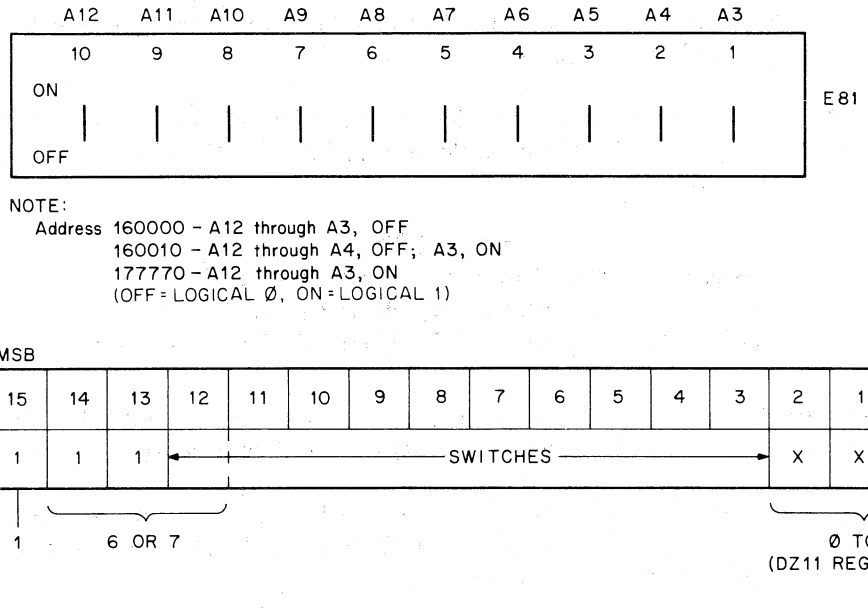


Figure 2-1 M7819 Address Selection

3. Vector selection is accomplished by the 8-position switch at E11. Switch positions 1 and 8 are not used. Switch position 2 corresponds to vector bit 3, 3 corresponds to vector bit 4, etc. When a switch is closed (on), a binary 0 is decoded. When a switch is open (off), a binary 1 is decoded. Note that this is opposite of the address switch decoding. (See Figure 2-2.)

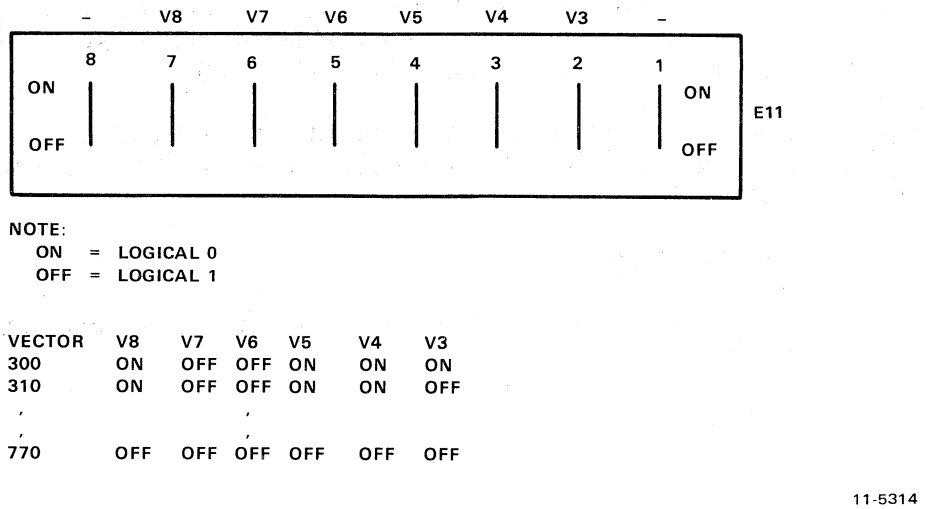


Figure 2-2 M7819 Vector Selection

4. If the DZ11 is supplied with the H3271 test connector, perform step 4. If the H327 test connector is supplied, go to step 5.

   a. Insert the module(s) into an SPC slot and connect the flat shielded cable (BC05W-15), ribbed side up, to J1 on the module(s). Connect the other end of the cable, ribbed side up, to the H3271.*

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

   b. Run the DZ11 diagnostic in staggered mode to verify module operation. Refer to MAINDEC-11-DZDZA, the diagnostic listing. Run at least two passes without error.

   c. Remove the BC05W-15 cable(s) from the H3271 and install the cable(s) (with smooth side up) to the static filter socket(s) on the back of the H317-E distribution panel. Refer to D-UA-DZ11-0-0 and Figure 2-3.

   d. Proceed to step 8.

5. Install the H327 test connector in J1 (the cable connector at the top of the M7819) and align arrows for proper connection.

6. Insert the M7819 in its SPC slot and run the DZ11 diagnostic in the staggered mode to verify module operation. Refer to MAINDEC-11-DZDZA, the diagnostic listing for the correct procedure. Run at least two passes without error.

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

7. Replace the H327 test connector with the BC05W-15 cable and observe the same caution as in step 6. Install the other end of the cable at the static filter socket on the back of the distribution panel. Refer to Figure 2-3 and D-UA-DZ11-0-0.

8. Connect the H325 (or H315) test connector on the first line and run the diagnostics in external mode. The test connector may be installed on the H317-E distribution panel or on the end of a BC05D cable.

   Repeat this step for each line.

9. Run DEC/X11 system exerciser to verify the absence of Unibus interference with other system devices.

*The H3271 has connections for two H7819 cables.

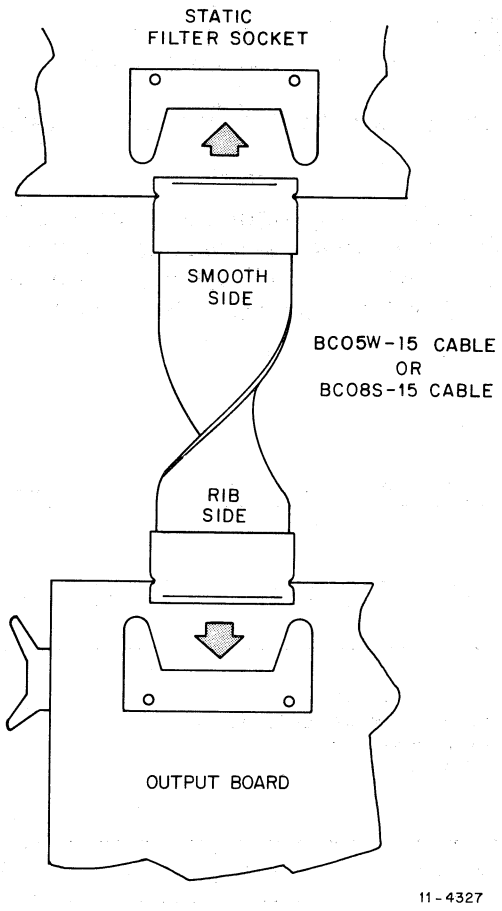


Figure 2-3 BC05W-15 and BC08S-15 Interconnection

10. The DZ11 is now ready for connection to external equipment. If the connection is to a local terminal, a null modem cable must be used. Use the BC03M or BC03P null modem cables for connection between the distribution panel and the terminal. The H312-A null modem unit may also be used with two BC05D EIA cables (one on each side of the null modem unit). If connection is to a Bell 103 or equivalent modem, a BC05D cable is required between the distribution panel and the modem. All of the cables mentioned must be ordered separately as they are *not* components of a standard DZ11 shipment. When possible, run the diagnostic in echo test mode to verify the cable connections and the terminal equipment.

2.4.3 M7814 Module Installation

To install the M7814 module, perform the following procedure.

1. Ensure that the priority insert (level 5) is properly seated in socket E41. Refer to D-UA-M7814-0-0.

2. Refer to Paragraph 3.1.1 for a description of address assignments. Set the switches at E72 so that the module will respond to its assigned address. When a switch is closed (on), a binary 1 is decoded. When a switch is open (off), a binary 0 is decoded. Note that the switch labeled 1 corresponds to bit 3, 2 to bit 4, etc. (See Figure 2-4.)

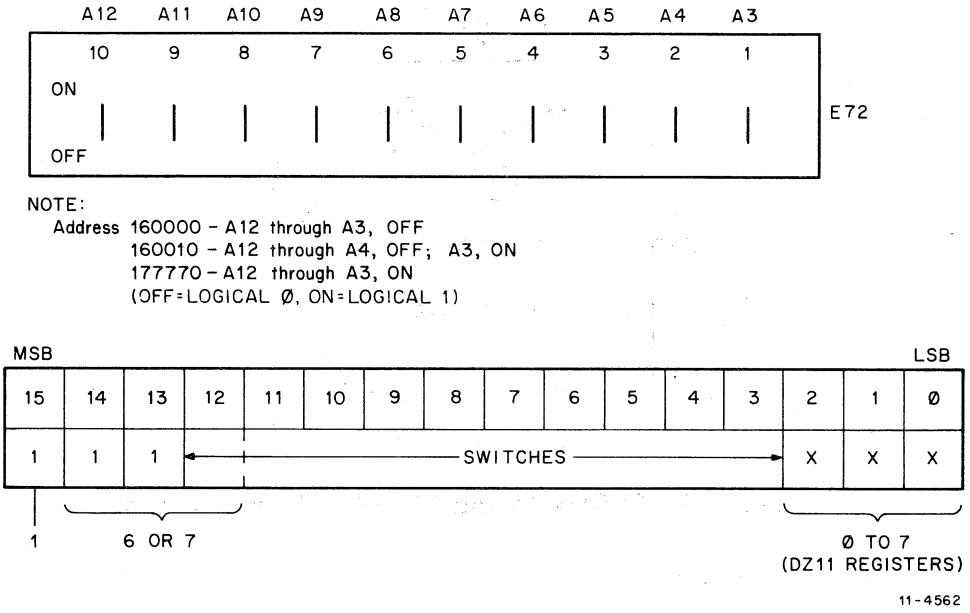
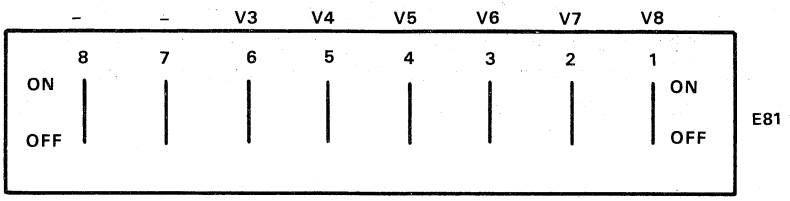


Figure 2-4 M7814 Address Selection

3. Vector selection is accomplished by an 8-position switch at E81 on the module(s). When a switch is closed (on), a binary 0 is decoded. When a switch is open (off), a binary 1 is decoded. Note that this is the opposite of the address switch decoding. Also, note that switch positions 7 and 8 are not used and switch 6 corresponds to bit 3, 5 to bit 4, etc. (Refer to Figure 2-5.)

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.



NOTE:
ON = LOGICAL 0
OFF = LOGICAL 1

VECTOR	V8	V7	V6	V5	V4	V3
300	ON	OFF	OFF	ON	ON	ON
310	ON	OFF	OFF	ON	ON	OFF
,			,			
,			,			
770	OFF	OFF	OFF	OFF	OFF	OFF

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Figure 2-5 M7814 Vector Selection

4. Insert module(s) into their assigned SPC slot(s). Connect the BC08S cable, with ribbed side up, to J1 on the module(s).

5. Skip this step if you have an H3190 test connector; otherwise perform the following.

   a. Connect the other end of the BC08S cable to the static filter on the back of the distribution panel (H317-F) with smooth side up. Refer to Figure 2-3 and D-UA-DZ11-0-0.

   b. Run the DZ11 diagnostic in internal (maintenance) mode for two error-free passes. Refer to MAINDEC-11-DZDZA, the diagnostic listing, for the proper procedure.

   c. Proceed to step 9.

6. Connect the other end of the BC08S cable, with smooth side up, to the H3190 test connector.

7. Run the DZ11 diagnostic in staggered mode for two error-free passes. Refer to MAINDEC-11-DZDZA, the diagnostic listing, for the correct procedure.

8. Remove the BC08S cable from the H3190 test connector and plug it into the static filter socket on the back of the distribution panel (H317-F) with smooth side up. Refer to Figure 2-3 and D-UA-DZ11-0-0.

9. Run the DEC/X11 system exerciser to verify the absence of Unibus interference with other system devices.

10. The DZ11 is now ready for connection to passive external equipment. This is accomplished with a customer-supplied cable. Most DIGITAL terminals use a BC04R cable as shown in Figure 2-6. Table 2-2 shows terminal connections for connecting a VT05, LA30, or LA36 to the DZ11 and Figure 2-7 shows the H317F distribution panel for terminal reference. Run an echo test to verify terminal connections.

NOTE

For customer terminals that can only transmit or receive in a single direction, the echo test cannot be run.

If the DZ11 is to be connected to an active device, a pair of H319s are required. Refer to Appendix A for details on this connection.

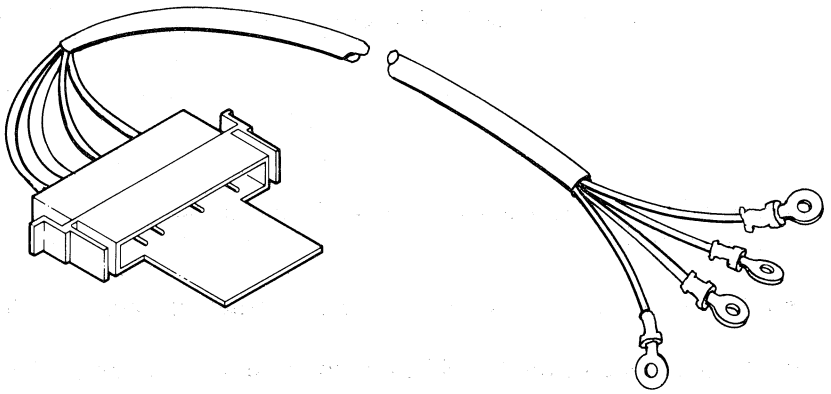

Figure 2-6 BC04R Cable

Table 2-2 DZ11 to Terminal Wiring (Using BC04R Cable)

VT05 Wiring			
Mate-N-Lok	**VT05 Signal**	**Color**	**DZ11 Terminal No.**
5	Terminal +RCV	Black	4 (XMIT+)
2	Terminal −RCV	White	3 (XMIT−)
3	Terminal −XMIT	Green	2 (REC−)
7	Terminal +XMIT	Red	1 (REC+)

Table 2-2 DZ11 to Terminal Wiring (Using BC04R Cable) (Cont)

LA30, LA36 Wiring			
Mate-N-Lok	LA30, LA36 Signal	Color	DZ11 Terminal No.
5	Terminal +XMIT	Black	1 (REC+)
2	Terminal −XMIT	White	2 (REC−)
3	Terminal −REC	Green	3 (XMIT−)
7	Terminal +REC	Red	4 (XMIT+)

NOTE

Terminal RCV is connected to DZ11 XMIT. Terminal XMIT is connected to DZ11 RCV. Polarity should always be + to + and − to − for both XMIT and RCV.

In addition, post 1 is located at the top of the terminal block on the distribution panel and goes in sequence to post 4 at the bottom of the terminal block.

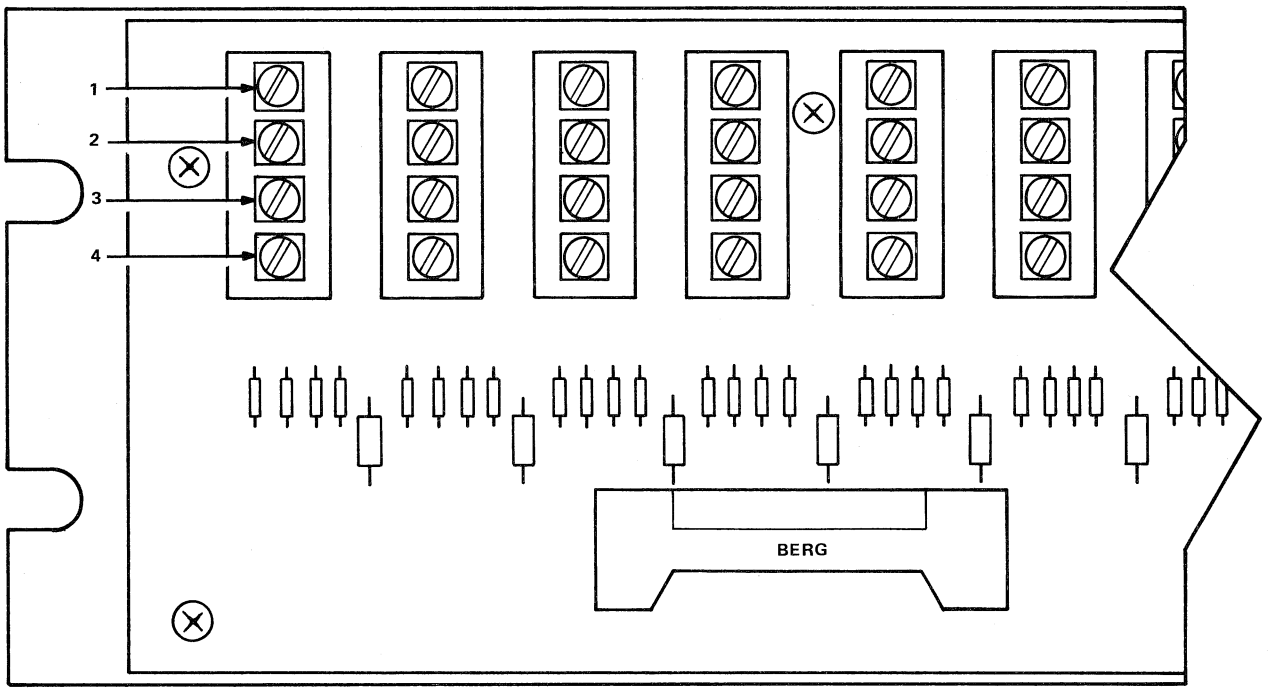

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Figure 2-7 H317F Distribution Panel Terminal Reference

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter provides basic information for programming the DZ11. A description of each DZ11 register, its format, programming constraints, and bit functions are presented to aid programming and maintenance efforts. Special programming features are also presented in this chapter.

3.1.1 Device and Vector Address Assignments

The DZ11's device and vector addresses are selected from the floating vector and device address space.

NOTE

The device floating address space is 160010_8 to 163776_8. The vector floating address space is 300_8 to 776_8.

Its floating address space follows the DJ11, DH11, DQ11, DU11, DUP11, LK11, and DMC11.

Its floating vector space follows the DC11; KL11/DL11-A, -B; DP11, DM11-A; DN11; DM11-BB and other modem control vectors; DR11-A; DR11-C; PA611 reader, PA611 punch; DT11; DX11; DL11-C, -D, -E; DJ11; DH11; GT40; LPS11; DQ11; KW11-W; DU11; DUP11; DV11; LK11-A; DWUN; and DMC11. If a DZ11 is installed in a system with any of the above listed options, then its assigned vector and device address should follow the vector and device address of the other options.

Two examples follow. First, the simplest case where there is only one DZ11.

Option	Address	Vector	Comment
GAP	160010		No DJ11s
GAP	160020		No DH11s
GAP	160030		No DQ11s
GAP	160040		No DU11s
GAP	160050		No DUP11s
GAP	160060		No LK11s
GAP	160070		No DMC11s
DZ11	160100	300	
GAP	160110		No more DZ11s

Next, a system with one DJ11, one DH11, one GT40, one KW11-W, and two DZ11s.

Option	Address	Vector	Comment
DJ11	160010	300	
GAP	160020		No more DJ11s
GAP	160030		DH11 must start on an address boundary that is a multiple of 20.
DH11	160040	310	
	160050		
GAP	160060		No more DH11s
GT40		320	GT40 address is not in the floating address space.
KW11-W		330	KW11-W address is not in the floating address space.
GAP	160070		No DQ11s
GAP	160100		No DU11s
GAP	160110		No DUP11s
GAP	160120		No LK11s
GAP	160130		No DMC11s
DZ11	160140	340	
DZ11	160150	350	
GAP	160160		No more DZ11s

3.2 REGISTER BIT ASSIGNMENTS

A comprehensive pictorial of all register bit assignments is shown in Figure 3-1. The four device registers (DR0, DR2, DR4, and DR6) are subdivided to form six unique registers. This subdivision is accomplished in DR2 and DR6 by assigning read-only (RO) or write-only (WO) status to each register. Since the reading and writing of DR2 and DR6 accesses two registers, PDP-11 processor instructions that perform a read-modify-write (DATIP) bus cycle cannot be used with DR2 or DR6. Also, DR2 permits only word instructions, but either byte or word instructions may be used with DR6. DR0 and DR4 have no programming constraints. In all register operations, the following applies: read-only bits are not affected by an attempt to write, and write-only and "not-used" bits appear as a binary 0 if a read operation is performed. Specific programming constraints for each register are discussed in the following paragraphs. A description of each bit function is presented in Tables 3-1 through 3-3.

3.2.1 Control and Status Register (CSR)

The control and status register (CSR) contains the states of flags and enable bits for scanning, processor interrupts, clearing, and maintenance. The 16-bit CSR has no programming constraints. The format is depicted in Figure 3-1, and bit functions are described in Table 3-1. Write-only and "not-used" bits are read as zeros by the Unibus, and read-only bits are not affected by write attempts.

		BYTES HIGH								LOW							
		MSB 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	LSB 00
DR0	CONTROL & STATUS (CSR)	RO TRDY	RW TIE	RO SA	RW SAE	NOT USED	RO TLINE C	RO TLINE B	RO TLINE A	RO RDONE	RW RIE	RW MSE	RW CLR	RW MAINT	NOT USED	NOT USED	NOT USED
DR2	RECEIVER BUFFER (RBUF)	RO DATA VALID	RO OVRN	RO FRAM ERR	RO PAR ERR	NOT USED	RO RX LINE C	RO RX LINE B	RO RX LINE A	RO RBUF D7	RO RBUF D6	RO RBUF D5	RO RBUF D4	RO RBUF D3	RO RBUF D2	RO RBUF D1	RO RBUF D0
	LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	WO RX ON	WO FREQ D	WO FREQ C	WO FREQ B	WO FREQ A	WO ODD PAR	WO PAR ENAB	WO STOP CODE	WO CHAR LGTH B	WO CHAR LGTH A	WO LINE C	WO LINE B	WO LINE A
DR4	TRANSMIT * CONTROL (TCR)	RW DTR 7	RW DTR 6	RW DTR 5	RW DTR 4	RW DTR 3	RW DTR 2	RW DTR 1	RW DTR 0	RW LINE ENAB 7	RW LINE ENAB 6	RW LINE ENAB 5	RW LINE ENAB 4	RW LINE ENAB 3	RW LINE ENAB 2	RW LINE ENAB 1	RW LINE ENAB 0
DR6	MODEM * STATUS (MSR)	RO CO 7	RO CO 6	RO CO 5	RO CO 4	RO CO 3	RO CO 2	RO CO 1	RO CO 0	RO RI 7	RO RI 6	RO RI 5	RO RI 4	RO RI 3	RO RI 2	RO RI 1	RO RI 0
	TRANSMIT DATA (TDR)	WO BRK 7	WO BRK 6	WO BRK 5	WO BRK 4	WO BRK 3	WO BRK 2	WO BRK 1	WO BRK 0	WO TBUF 7	WO TBUF 6	WO TBUF 5	WO TBUF 4	WO TBUF 3	WO TBUF 2	WO TBUF 1	WO TBUF 0

*The high byte of the TCR (Data Terminal Ready) and the MSR are not used with the 20 mA options.

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Figure 3-1 Register Bit Assignments

Table 3-1 CSR Bit Functions

Bit	Title	Function
00–02	Not used	
03	Maintenance (MAINT)	A read/write bit that, when set, causes the serial output data from the transmitter to be fed back as serial input data to the receiver. All lines are turned around. Cleared by BUS INIT and CLR.
04	Clear (CLR)	A read/write bit that fires a one-shot to generate a 15 μs reset which clears the receiver silo, all UARTs, and the CSR. After a CLR is issued, the CSR and line parameters must be set again. CLR in progress is indicated by CLR = 1. Modem control registers are not affected, nor are bits 00 through 14 of RBUF.
05	Master Scan Enable	A read/write bit that activates the scanner to enable the receiver transmitter and silo. Cleared by CLR and BUS INIT.
06	Receiver Interrupt Enable	A read/write bit that enables the receiver interrupt. Cleared by CLR and BUS INIT.
07	Receiver Done (RDONE)	A read-only bit (hardware set) that generates RCV INT if bit 06 = 1 and bit 12 = 0. The bit clears when the RBUF is read and resets when another word reaches the output of the silo (RBUF). If bit 06 = 0, RDONE can be used as a flag to indicate that the silo contains a character. If bit 12 = 1, RDONE does not cause interrupts but otherwise acts the same.
08–10	Transmit Line A–C (TLINE)	When bit 15 = 1, these three read-only bits indicate the line that is ready to transmit a character. Bit 15 clears when the character is loaded into the transmit buffer, but sets again if another line is ready. A new line number could appear within a minimum of 1.9 μs. Bits 08–10 return to line 0 after a CLR or BUS INIT. These bits are meaningful only when bit 15 (TRDY) is true.
11	Not used	
12	Silo Alarm Enable (SAE)	A read/write bit that enables the silo alarm and prevents RDONE from causing interrupts. If bit 06 = 1, the SAE allows the SA (bit 13) to cause an interrupt after 16 entries in the silo. If bit 06 = 0, the SA can be used as a flag. The bit is cleared by CLR and BUS INIT.

Table 3-1 CSR Bit Functions (Cont)

Bit	Title	Function
13	Silo Alarm (SA)	A read-only bit set by the hardware after 16 characters enter the silo. It causes an interrupt if bit 06 = 1 and is cleared by CLR, BUS INIT, and reading the RBUF. When the silo flag occurs (SA = 1), the silo must be emptied because the flag will not be set again until 16 additional characters enter the silo.
14	Transmitter Interrupt Enable (TIE)	A read/write bit that allows an interrupt if bit 15 (TRDY) = 1.
15	Transmitter Ready (TRDY)	A read-only bit that is set by hardware when a line number is found that has its transmit buffer empty and its LINE ENAB bit set. It is cleared by CLR, BUS INIT, and by loading the TBUF register.

3.2.2 Receiver Buffer (RBUF)

The receiver buffer (RBUF) register contains the received character bits, with line identification, error status, and data validity flag. As one of two registers in DR2 (RBUF and LPR), RBUF is accessed when a read operation is performed (write operation accesses the LPR). The programming constraints for the RBUF register are as follows.

1. Byte instructions cannot be used.
2. It is a read-only register.
3. TST or BIT instructions cannot be used because they cause the loss of a character.
4. The register requires master scan enable (CSR, bit 05) to be set in order to be functional. When this bit is off, bits 00 to 14 of the RBUF become invalid regardless of the state of bit 15 (data valid) and the silo is held empty. The register format of RBUF is depicted in Figure 3-1 and bit functions are described in Table 3-2. Each reading of the RBUF register advances the silo and presents the next character to the program. Bits 00 through 14 do not go to zero after a CLR or BUS INIT; however, they become invalid and the silo is emptied. Bit 15 (data valid) does clear to zero. (See Table 3-2.)

Table 3-2 RBUF Bit Functions

Bit	Title	Function
00–07	Received Character	These bits contain the received character. If the selected code level is less than eight bits wide, the high-order bits are forced to zero.
08–10	Line Number	These bits present the line number on which the character was received.
11	Not used	
12	Parity Error	This bit indicates whether the received bit had a parity error. The parity bit is generated by hardware and does not appear in the RBUF word.
13	Framing Error	This bit indicates improper framing (stop bit not a mark) of the received character and can be used for break detection.
14	Overrun	This bit indicates receiver buffer overflow. The result is a received character which is replaced by another received character before storage in the silo. A character is lost but the received character put in the silo is valid.
15	Data Valid	This bit indicates that the character read from the silo (RBUF) is valid. The RBUF is read until the data valid bit = 0, indicating an invalid character and empty silo. Cleared by CLR and BUS INIT.

3.2.3 Line Parameter Register (LPR)

The line parameter register (LPR) is a 16-bit register that sets the parameters (character and stop code lengths, parity, speed, and receiver clock) for each line (Table 3-3). Bits 00–02 select the line for parameter loading. Line parameters for each line must be reloaded after a CLR (bit 04 of CSR) or BUS INIT operation. The programming constraints for the LPR are as follows.

1. It is a write-only register.
2. BIS or BIC instructions are not allowed.
3. Byte operations cannot be used.

Table 3-3 LPR Bit Functions

Bit	Title	Function
00–02	Line Number	These bits select the line for parameter loading
03–04	Character Length	These bits set the character length for the selected line. The parity bit is not part of the character length. **04 03** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits
05	Stop Code	This bit sets the stop code length (0 = 1-unit stop, 1 = 2-unit stop or 1.5-unit stop if a 5-level code is employed).
06	Parity	This bit selects the parity option (0 = no parity check, 1 = parity enabled on TRAN and RCV).
07	Odd Parity	This bit selects the kind of parity (0 = even parity select, 1 = odd parity select). Bit 06 must be set for this bit to have effect.
08–11	Speed Select	These bits select the TRAN and RCV speed for the line selected by bits 00–02. Refer to Table 3-4 for a list of available baud rates.
12	Receiver On	This bit must be set when loading parameters to activate the receiver clock. (Transmitter clock is always on.) A CLR or BUS INIT turns the receiver clock off.

3.2.4 Transmit Control Register (TCR)

The transmit control register contains 16 bits for the EIA options (M7819 module) and 8 bits for the 20 mA option (7814 module). The difference is that the data terminal ready (DTR) lines that make up the high byte (bits 08 through 15) of the TCR are not used by the 20 mA options because they do not have modem control capabilities.

The high byte (M7819 only) contains a read/write DTR bit for each line. This byte is cleared by BUS INIT only, not by CLR. When the high byte is not used (M7814 only), it reads back to the Unibus as all zeros. Attempts to write into it will have no effect. The low byte contains a read/write line enable bit for each line. A set bit allows transmission on the corresponding line. Paragraph 3.3.7 explains how to properly use this bit. This byte is cleared by CLR and BUS INIT.

3.2.5 Modem Status Register (MSR)

This is a 16-bit register used only with the EIA options (M7819 module). The 20 mA options (M7814 module) do not have modem control capabilities. When not used, this register reads all zeros to the Unibus.

The MSR consists of two bytes: the low byte (bits 00–07) and the high byte (bits 08–15). The low byte monitors the state of each line's ring indicator (RI) lead; the high byte monitors the state of each line's carrier (CO) lead. The MSR is the read-only portion of DR6 and has the following programming characteristics.

1. It is a read-only register.
2. CLR and BUS INIT have no effect.
3. Bit format is shown in Figure 3-1.

3.2.6 Transmit Data Register (TDR)

The TDR consists of two 8-bit bytes. The low byte is the transmit buffer (TBUF) and holds the character that is to be transmitted. The high byte is the break register with each line controlled by an individual bit. When a break bit is set, the line associated with that bit starts sending zeros immediately and continuously. The TDR is the write-only portion of DR6 and has the following programming characteristics.

1. It is a write-only register.
2. BIS or BIC instructions cannot be used.
3. For character lengths less than 8 bits, the character loaded into the TBUF must be right justified because the hardware forces the most significant bits to zero.
4. The break register has no effect when running in the maintenance mode (i.e., CSR bit 03 = 1).
5. It is cleared by CLR and BUS INIT.
6. Bit format is shown in Figure 3-1.

3.3 PROGRAMMING FEATURES

The DZ11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

3.3.1 Baud Rate

The selection of the desired transmission and reception speed is controlled by the conditions of bits 08 through 11 of the LPR. Table 3-4 depicts the required bit configuration for each operating speed. The baud rate for each line is the same for both the transmitter and receiver. The receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 3-4 Baud Rate Selection Chart

Bits				Baud Rate
11	10	09	08	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not used

3.3.2 Character Length

The selection of one of the four available character lengths is controlled by bits 03 and 04 of the LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5-level), 01 (6-level), 10 (7-level), and 11 (8-level). For character lengths of 5, 6, and 7, the high-order bits are forced to zero.

3.3.3 Stop Bits

The length of the stop bits in a serial character string is determined by bit 05 of the LPR. If bit 05 is a zero, the stop length is one unit; bit 05 set to a one selects a 2-unit stop unless the 5-level character length (bits 03 and 04 at zero) is selected, in which case the stop bit length is 1.5 units.

3.3.4 Parity

The parity option is selected by bit 06 of the LPR. Parity is enabled on transmission and reception by setting bit 06 to a one. Bit 07 of the LPR allows selection of even or odd parity, and bit 06 must be set for bit 07 to be significant. The parity bit is generated and checked by hardware, and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character has a parity error.

3.3.5 Interrupts

The receiver interrupt enable (RIE) and silo alarm enable (SAE) bits in the CSR control the circumstances upon which the DZ11 receiver interrupts the PDP-11 processor.

If RIE and SAE are both clear, the DZ11 never interrupts the PDP-11 processor. In this case, the program must periodically check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZ11 will interrupt when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Alternatively, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt.

If RIE and SAE are both set, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector when the silo alarm (SA) bit in the CSR is set. The SA bit will be set when 16 characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described in Paragraph 3.3.6 to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity, the PDP-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo, it should ensure that DZ11 receiver interrupts are inhibited. This should be done by raising the PDP-11 processor priority. The silo alarm interrupt feature can significantly reduce the PDP-11 processor overhead required by the DZ11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The transmitter interrupt enable bit (TIE) controls transmitter interrupts to the PDP-11 processor. If enabled, the DZ11 will interrupt the PDP-11 processor to the DZ11 transmitter interrupt vector when the transmitter ready (TRDY) bit in the CSR is set, indicating that the DZ11 is ready to accept a character to be transmitted.

3.3.6 Emptying the Silo

The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the silo so it will not be lost and will clear out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the data valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. A TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the silo to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo will not be available for at least 1 μs. Therefore, on fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of 1 μs. This will prevent a false indication of an empty silo.

3.3.7 Transmitting a Character

The program controls the DZ11 transmitter through five registers on the Unibus: the control and status register (CSR), the line parameter register (LPR), the line enable register, the transmitter buffer (TBUF), and the break register (BRK).

Following DZ11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the master scan enable (MSE) bit in the CSR. The program should set the transmitter interrupt enable (TIE) bit in the CSR if it wants the DZ11 transmitter to operate on a program interrupt basis.

The line enable register is used to enable and disable transmission on each line. One bit in this 8-bit register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC, and BICB instructions. (If word instructions are used, the line enable register and the DTR registers on M7819 modules are simultaneously accessed.)

The DZ11 transmitter is controlled by a scanner which is constantly looking for an enabled line (line enable bit set) which has an empty UART transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 3-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the PDP-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 7 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the line enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data lead for any line is the 1 state. The break register (BRK) is used to apply a continuous zero signal to the line. One bit in this 8-bit register is associated with each line. The line will remain in this condition as long as the bit remains set. The program should use a MOVB instruction to access the BRK register. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous zero sending state. The program may use this facility for sending precisely timed zero signals by setting the break bit and using transmit ready interrupts as a timer.

It should be remembered that each line in the DZ11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the 1 state at the end of the zero sending period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the zero sending period, the program should load an all-zero character to be transmitted. When the scanner requests service, indicating this character has begun transmission, the program should clear the BRK bit and load the next data character.

3.3.8 Data Set Control

DZ11 models with EIA interfaces include data set control as a standard feature. The program may sense the state of the carrier and ring indicator signals from each data set and may control the state of the data terminal ready signal to each data set. The program uses three 8-bit registers to access the DZ11 data set control logic. One bit in each register is associated with each of the eight lines. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The data terminal ready (DTR) register is a read/write register. Setting or clearing a bit in this register will turn the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and line enable registers will be simultaneously accessed.) The DTR register is cleared by the INIT signal on the Unibus but is not cleared if the program clears the DZ11 by setting the CLR bit of the CSR.

The carrier register (CAR) and ring register (RING) are read-only registers. The program can determine the current state of the carrier signal for a line by examining the appropriate bit of the CAR register. It can determine the current state of the ring signal by examining the appropriate bit of the ring register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16-bit register by using MOV or BIT instructions. The DZ11 data set control logic does not interrupt the PDP-11 processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

3.4 PROGRAMMING EXAMPLES

The following six examples are sample programs for the DZ11 option. These examples are presented only to indicate how the DZ11 can be used.

Example 1 – Initializing the DZ11

The DZ11 is initialized by a power-up sequence, a reset instruction, or a device clear instruction.

Device Clearing the DZ11

```
001000  012737  START:  MOV #20, DZCSR    ;Set bit 4 in the
001002  000020                           ;DZ11 control and
001004  160100                           ;status register.
001006  032737  1$:     BIT #20, DZCSR    ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$            ;If bit 4 is still
                                          ;set, the branch
                                          ;condition is true
                                          ;and the device clear
                                          ;function is still in
                                          ;progress.
001016  000000          HALT              ;The device clear
                                          ;function is complete
                                          ;and the DZ11 has been
                                          ;cleared.
```

DZCSR = Control and Status Register Address = 160100.

Example 2 – Transmit Binary Count Pattern on One Line

```
001000  012737  START:  MOV #20, DZCSR    ;Set bit 4 in the DZ11
001002  000020                           ;control and status
                                          ;register.
001004  160100
001006  032737  1$:     BIT #20, DZCSR    ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$            ;If bit 4 is still set,
                                          ;the branch condition
                                          ;is true and the device
                                          ;clear function is still
                                          ;in progress.
001016  012737          MOV #n, DZLPR     ;Load the parameters
001020  001070                           ;for line 0: 8-bit
001022  160102                           ;character; 2 stop bits;
                                          ;110 baud
001024  012737          MOV #1, DZTCR     ;Enable line 0
                                          ;transmitter.
```

```
001026  000001
001030  160104
001032  012737          MOV #m, DZCSR       ;Set scanner enable bit
001034  000040                              ;5 in the control and
001036  160100                              ;status register.
001040  005000          CLR R0              ;Set binary count
                                            ;pattern to zero.
001042  005737  2$:     TST DZCSR           ;Test the transmitter
001044  160100                              ;ready flag (bit 15).
001046  100375          BPL 2$              ;If branch condition
                                            ;is false, continue;
                                            ;otherwise test again.
001050  110037          MOVB R0, DZTDR      ;Load character to be
001052  160106                              ;transmitted.
001054  105200          INCB R0             ;Increment binary count.
001056  100371          BPL 2$              ;If branch condition is
                                            ;false, the binary count
                                            ;pattern is complete.
001060  000000          HALT
```

R0 = Register 0 = Binary Count Pattern
DZCSR = DZ11 Control and Status Register Address = 160100
DZLPR = DZ11 Line Parameter Register Address = 160102
DZTCR = DZ11 Transmit Control Register Address = 160104
DZTDR = DZ11 Transmit Data Register Address = 160106

Example 3 – Transmit a Binary Count in Maintenance Loopback Mode, with the Receiver "On" in the Interrupt Mode

Output Received Data to Console

```
001200  005000          CLR R0              ;Set binary count
                                            ;to zero.
001202  012701          MOV 1400, R1        ;Set R1 to first
001204  001400                              ;address of data
                                            ;buffer.
001206  012706          MOV #SP, R6         ;Initialize stack
001210  001100                              ;pointer.
001212  012737          MOV #INT, RVEC      ;Set DZ11 vector
001214  001304                              ;address to start of
001216  000300                              ;receiver interrupt
                                            ;routine.
001220  005037          CLR (RVEC+2)        ;Set up processor
001222  000302                              ;status word for DZ11
                                            ;receiver interrupt.
001224  012737          MOV #20, DZCSR      ;Set bit 4 in the
001226  000020                              ;DZ11 control and
                                            ;status register.
```

```
001230  160100
001232  032737  1$:     BIT #20 DZCSR       ;Test bit 4.
001234  000020
001236  160100
001240  001374          BNE 1$              ;If bit 4 is still
                                            ;set, the branch
                                            ;condition is true
                                            ;and the device clear
                                            ;function is still in
                                            ;progress.
001242  012737          MOV #PAR, DZLPR     ;Load the parameters
001244  011070                              ;for line 0: 8-bit
001246  160102                              ;character; 2 stop bits;
                                            ;110 baud; no
                                            ;parity; receiver on.
001250  012737          MOV #1, DZTCR       ;Enable line 0
                                            ;transmitter.
001252  000001
001254  160104
001256  012737          MOV #150, DZCSR     ;Turn scanner on,
001260  000150                              ;enable receiver
001262  160100                              ;interrupts, and loop
                                            ;lines back on themselves.
001264  005737  2$:     TST DZCSR           ;Test the transmitter
001266  160100                              ;ready flag.
001270  100375          BPL 2$              ;If branch condition is
                                            ;false, continue;
                                            ;otherwise test again.
001272  110037          MOVB R0, DZTBUF     ;Load character to be
001274  160106                              ;transmitted.
001276  105200          INCB R0             ;Increment binary count.
001300  001371          BNE 2$              ;If branch condition is
                                            ;false, the binary count
                                            ;pattern is complete.
001302  000777          BR.                 ;Wait for last character
                                            ;transmitted to be
                                            ;received.
```

Receiver Interrupt Service Routine

```
001304  013711          MOV DZRBUF, (R1)    ;Store received
001306  160102                              ;character in memory
                                            ;table.
001310  022721          CMP #100377,        ;Check for last
001312  100377          (R1)+               ;character.
001314  001401          BEQ .+2             ;Branch condition is
                                            ;true when last
                                            ;transmitted character
                                            ;is received.
001316  000002          RTI                 ;Exit routine.
001320  012701          MOV #1400, R1       ;Initialize pointer
001322  001400                              ;to start of received
                                            ;data buffer in memory.
001324  105737  3$:     TSTB TPS            ;Test to see if console
001326  177564                              ;is ready.
001330  100375          BPL 3$              ;Wait, and test again.
                                            ;If condition is met,
001332  111137          MOVB (R1), TPB      ;transfer character
001334  177566                              ;to console.
001336  022721          CMP #100377,        ;Check for last
001340  100377          (R1)+               ;character.
001342  001370          BNE 3$              ;Not finished if
                                            ;condition is true.
001344  000000          HALT                ;finished.
```

RVEC = DZ11 Receiver Interrupt Vector Address
DZCSR = DZ11 Control and Status Word Address
DZLPR = DZ11 Line Parameter Register (Write-Only) Address
DZTCR = DZ11 Transmit Control Register Address
DZTBUF = DZ11 Transmit Buffer Address
DZRBUF = DZ11 Receiver Buffer Address (Read-Only Register)
TPS = Teletype® Punch Status Register Address
TPB = Teletype Punch Data Register Address

®Teletype is a registered trademark of Teletype Corporation.

Example 4 – Transmit and receive in Maintenance Mode on a Single Line
The switch register bits (SWR00–SWR07) hold the desired data pattern (character).

```
001000  012737  START:  MOV #LINE, DZTCR  ;Select the line for
001002  000002                           ;transmitting on.
                                         ;Choose one of eight.
001004  160104                           ;Line #1 selected.
001006  012737          MOV #PAR, DZLPR  ;Select desired line
001010  017471                           ;parameters for
                                         ;transmitting line
001012  160102                           ;and turn on receiver
                                         ;for that line.
                                         ;8-level code, 2 stop
                                         ;bits, and no parity
                                         ;selected.
                                         ;19.2K baud selected
                                         ;Note: 19.2K baud is
                                         ;not used by the
                                         ;customer but can be
                                         ;used for diagnostic
                                         ;purposes to speed up
                                         ;the transmit-receive
                                         ;loop to make it easier
                                         ;to scope.
001014  012737          MOV #N, DZCSR    ;Start scanner and set
001016  000050                           ;maintenance bit 3.
001020  160100
001022  005737  Test 1:  TST DZCSR        ;Test for bit 15
001024  160100                           ;(transmitter ready).
001026  100375          BPL Test 2       ;If the branch condition
                                         ;is false, the transmitter
                                         ;is ready; if true, go
                                         ;back and test again.
001030  113737          MOVB SWR,        ;Load the transmit
001032  177570          DZTBUFF          ;character from the
001034  160106                           ;switch register.
001036  000240          NOP              ;No operation. This
                                         ;location can be changed
                                         ;to a branch instruction
                                         ;if only test 1 is
                                         ;desired (replace 000240
                                         ;with 000771).
001040  012701          MOV #DEL, R1     ;Delay equals a
        177670                           ;constant that will
                                         ;allow enough time for
                                         ;the receiver done
                                         ;flag to set before
                                         ;recycling the test.
                                         ;The value will change
                                         ;with baud rate and
                                         ;processor. The
                                         ;constant given is
                                         ;good for 19.2K baud
                                         ;on a PDP-11/05.
```

```
001042  105737  Test 2:  TSTB DZCSR      ;Test bit 2 (receiver
001044  160100                           ;done flag).
001046  100402           BMI 1$          ;When the branch
                                         ;condition is true,
                                         ;the receiver done
                                         ;flag is set.
001050  005201           INC R1          ;Increment delay.
001052  001373           BNE TEST 2      ;If the branch
                                         ;condition is true, the
                                         ;delay is not finished.
001054  013700  1$:      MOV DZRBUF, R0  ;Read the DZ11
001056  160102                           ;receiver buffer to
                                         ;register 0.
001060  000760           BR TEST 1       ;Loop back and
                                         ;test again.
```

Example 5 – Transmit and Receive on a Single Line Using Silo Alarm in Maintenance Mode

```
001200  012706           MOV #1100, R6   ;Initialize stack
001202  001100                           ;pointer.
001204  012737           MOV #3$, TVEC   ;Initialize transmitter
001206  001274                           ;vector address.
001210  000304
001212  005037           CLR TVEC+2      ;Initialize transmitter
001214  000306                           ;vector processor status
                                         ;word.
001216  012700           MOV #DBUF, R0   ;Set first address of
001220  001304                           ;input data table
                                         ;into R0.
001222  012737           MOV #1, DZTCR   ;Enable line 0
                                         ;transmitter.
001224  000001
001226  160104
001230  012737           MOV #17470,     ;Set up line parameters
001232  017470           DZLPR           ;and turn on the receiver
001234  160102                           ;clock for line 0.
001236  012737           MOV #50050,     ;Enable transmitter
001240  050050           DZCSR           ;interrupt and silo
001242  160100                           ;alarm. Turn on
                                         ;scanner and maintenance
                                         ;mode.
001244  032737  1$:      BIT #20000,     ;Test for silo alarm
001246  020000           DZCSR
001250  160100
001252  001774           BEQ 1$          ;Loop until silo alarm
                                         ;flag sets.
001254  013720  2$:      MOV DZRBUF,     ;Read DZ11 silo
001256  160102           (R0)+           ;receiver buffer output.
001260  000240           NOP             ;Delay to allow next
001262  000240           NOP             ;word in silo to filter
                                         ;down to the silo
                                         ;output.
```

```
001264   100773          BMI 2$          ;Data valid set says
                                         ;that word is good,
                                         ;go back for more.
001266   012700          MOV #DBUF, R0   ;Silo has been emptied.
001270   001304                          ;Reinitialize data
                                         ;table address pointer.
001272   000764          BR 1$           ;Do it again.
```

Transmitter Interrupt Service Routine

```
001274   112737   3$     MOVB DAT, DZTBUF    ;Transmit
001276   000252                              ;character 252
001300   160106
001302   000002          RTI
```

Data Table

```
1304     100252    ;Word 1
1306     100252
```

.

.

.

.

.

.

```
1340     100252    ;Word 16
1342     000252    ;Data valid
                   ;not set
                   ;character is
                   ;invalid
```

NOTE

It is possible to get more than 16 words because they are being put into the silo simultaneously with the reading of the silo.

Example 6 – Echo Test on a Single Line (Transmit Received Data)

```
001000  012737  START  MOV #PAR, DZLPR  ;Load line parameters
                                        ;for line being used.
001002  011073                          ;Line 3, 8-bit
001004  160102                          ;character, 2 stop
                                        ;bits, no parity,
                                        ;110 baud, and receiver
                                        ;clock on.
001006  012737         MOV #LINE, DZTCR ;Turn line 3
001010  000010                          ;transmitter on.
001012  160104
001014  012737         MOV #n, DZCSR    ;Turn scanner on
001016  000040                          ;(set CSR-5)
001020  160100
001022  105737  1$:    TSTB DZCSR       ;Test (bit 7) for
001024  160100                          ;RDONE
001026  100375         BPL 1$           ;If bit 7 is not set,
                                        ;go back and test again.
001030  005737  2$:    TST DZCSR        ;Test (bit 15) for
001032  160100                          ;TRDY
001034  100375         BPL 2$           ;If bit 15 is not set
                                        ;go back and test again.
001036  013700         MOV RBUF, R0     ;Read received data
001040  160102                          ;word into R0
001042  110037         MOVB R0, DZTDR   ;Load character
001044  160106                          ;into DZ11 TBUF
                                        ;register for
                                        ;transmitting.
001046  000765         BR 1$            ;Repeat.
```

CHAPTER 4
DETAILED DESCRIPTION

4.1 SCOPE

This chapter contains detailed descriptions of DZ11 circuit operation and signal flow; it also describes the DZ11's interaction with external devices and how it operates as a component of a PDP-11 system. The text is supplemented by references to DIGITAL engineering drawings and specifications, simplified diagrams, and appendices.

The DZ11 supports two types of output line interfaces: EIA and 20 mA loop. Each has a separate module with the following differences.

1. The M7819 module (EIA) supports three modem control leads (data terminal ready, carrier, and ring indicator). The M7814 module (20 mA loop) does not support these signal leads.

2. The receivers and output drivers are different for each type.

3. The line interface cable, turnaround connector, and distribution panel are different for each type.

Despite these differences, the Unibus interface logic, scanner logic, and output control logic are identical and these areas will therefore be discussed once for both modules.

4.2 LINE-TO-UNIBUS OVERALL DATA FLOW (RECEIVE)

When receiving data from a terminal or modem, the DZ11 module interprets a serial data stream and performs a serial-to-parallel conversion before transferring the data to the Unibus. (Refer to Figure 4-1.) Each serial line, REC (07:00), connects through the distribution panel to connector J1. The receivers match the incoming signal levels to that of the DZ11, and the data is fed to the receiver control logic, where it passes through a maintenance control circuit which allows the DZ11 to "receive" its own transmissions during maintenance tests.

From the receiver control logic, the data is fed into the appropriate UART for the serial-to-parallel conversion. A parallel data format, corresponding to its serial input, is moved to a FIFO storage "tank," called a silo, which has a 64-character capacity. When requested by the processor, each character is read from the bottom of the silo (RBUF). The remaining characters shift one position downward and the read character is multiplexed through the bus drivers to the Unibus. For the M7819 module (EIA), the modem control signals (RI and CO) for each line are routed directly to the output multiplexer.

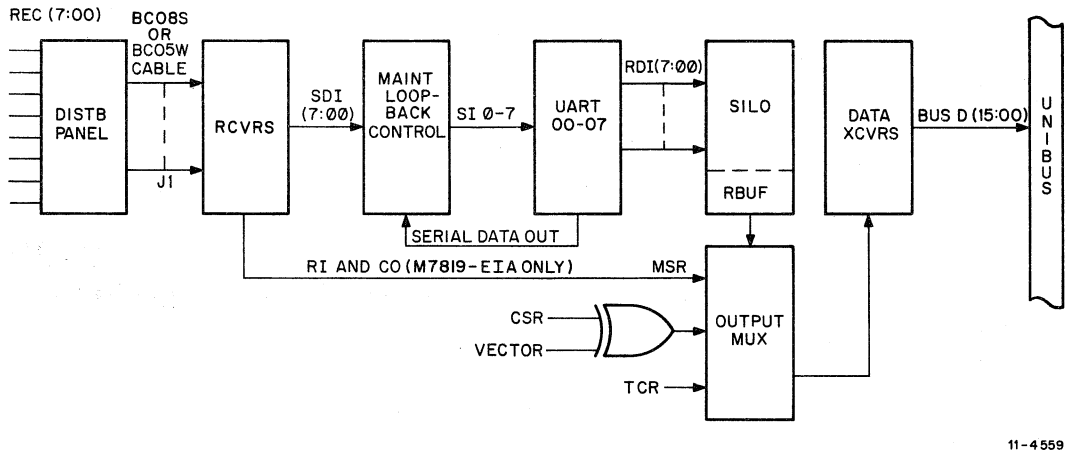


Figure 4-1 Line-to-Unibus Data Flow (Receive)

4.3 UNIBUS-TO-LINE OVERALL DATA FLOW (TRANSMIT)

During a transmit cycle, parallel data is brought in from the Unibus for transmission to one of the eight terminals (or modems). (Refer to Figure 4-2.) The 16 bus lines, BD (15:00), are fed through data transceivers and distributed to the device registers and UARTs. When the DZ11 is ready to transmit, a character is read from the TBUF and loaded into the appropriate UART for the line. The UART then performs the parallel-to-serial data conversion, adds the desired character control bits, and sends the data to the selected transmission line through a line driver, and subsequently to the modem or terminal connected to that line. The break register connects directly to the drivers. Setting the break forces the drivers into a continuous "zero sending" condition. The DTR modem control lines (M7819 only) go directly to the EIA drivers.

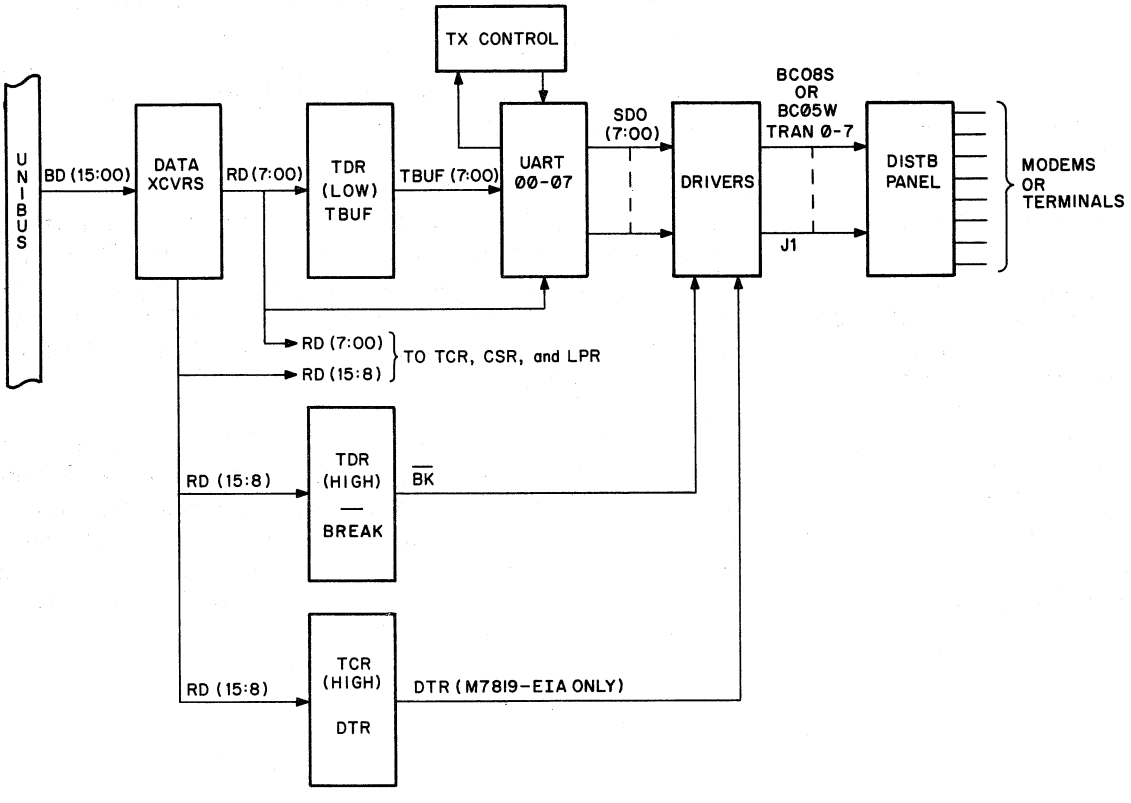


Figure 4-2 Unibus-to-Line Data Flow (Transmit)

4.4 FUNCTIONAL BLOCK DESCRIPTION

4.4.1 Unibus Interface

The DZ11 Unibus interface provides access for the DZ11 system to the PDP-11 Unibus. All signals that pass between the Unibus and the DZ11 are routed through the interface. This logic can be divided into three major areas: address selection, data transceiving and multiplexing, and interrupt control. These are shown in Figure 4-3. The interface logic performs the following functions:

1. Selection and recognition of the DZ11 addresses and device registers
2. Determination of the DZ11 mode of operation with the PDP-11 processor (DATI or DATO word or byte)
3. Handling of data to and from the device registers and other DZ11 control elements
4. Controlling interrupts between the DZ11 and PDP-11 processor.

4.4.1.1 Address Selection – The address selection logic determines the DZ11 device address and recognizes that address when it appears on the Unibus. A recognized address indicates that the DZ11 has been selected by the processor or another bus "master."

The desired address is selected by switches that correspond to Unibus address bits 03 through 12 (Figure 4-4). Bits 13 through 17 are always decoded as binary 1s (Figure 4-5). Bits 00 through 02 determine which device register is to be selected. This bit scheme allows device addresses from $16000X_8$ to $17777X_8$. However, the DZ11 uses only the floating address space from 160010_8 to 163770_8. A detailed description of DZ11 address assignments is presented in Chapter 3.

4.4.1.2 Interrupt Control – The interrupt control logic handles the processor to Unibus to DZ11 dialogue to permit processor interrupts. The logic generates the vector address and receives interrupt commands from the CSR. The DZ11 operates at priority levels 5A (receiver) and 5B (transmitter). When two DZ11 modules are used, the first module (slot 1) has priority over the second (slot 2). The priority insert establishes the DZ11 priority level by directing the Unibus request and grant signals from the appropriate Unibus lines to the DZ11. A series of switches permit alteration of the vector address to suit programming requirements. Refer to Chapter 3 of this manual for vector selection and assignment.

4.4.1.3 Data Transceivers and Output Multiplexers (Figure 4-6) – The data transceivers and output multiplexers control data flow to and from the Unibus. The 4:1 multiplexers select the contents of the CSR, RBUF, TCR, and MSR (MSR not used in M7814) for transmission to the Unibus. The vector bits are also transferred to the Unibus by the same logic.

4.4.2 Scanner

The scanner generates timing signals for transmission and reception of data between the Unibus and UARTs. The scanner timing signals originate at the 5.068 MHz clock, a continuously running signal that is inverted twice to yield MASTER CLK L and MASTER CLK H pulses. These pulses control the baud rate logic, and a divide-by-five counter uses the pulses to generate the CLK H pulses that drive the phase generator logic. Line sampling occurs during a 4.0 μs period, which is divided into four equal phases. Phase 1 triggers a line counter, which produces the SCAN A, B, and C line-select signals. Each line is sampled sequentially. (Refer to Figure 4-7.) Phases 2, 3, and 4 are used in the receiver and transmit control sections and are discussed in detail in Paragraphs 4.5.6 and 4.5.7.

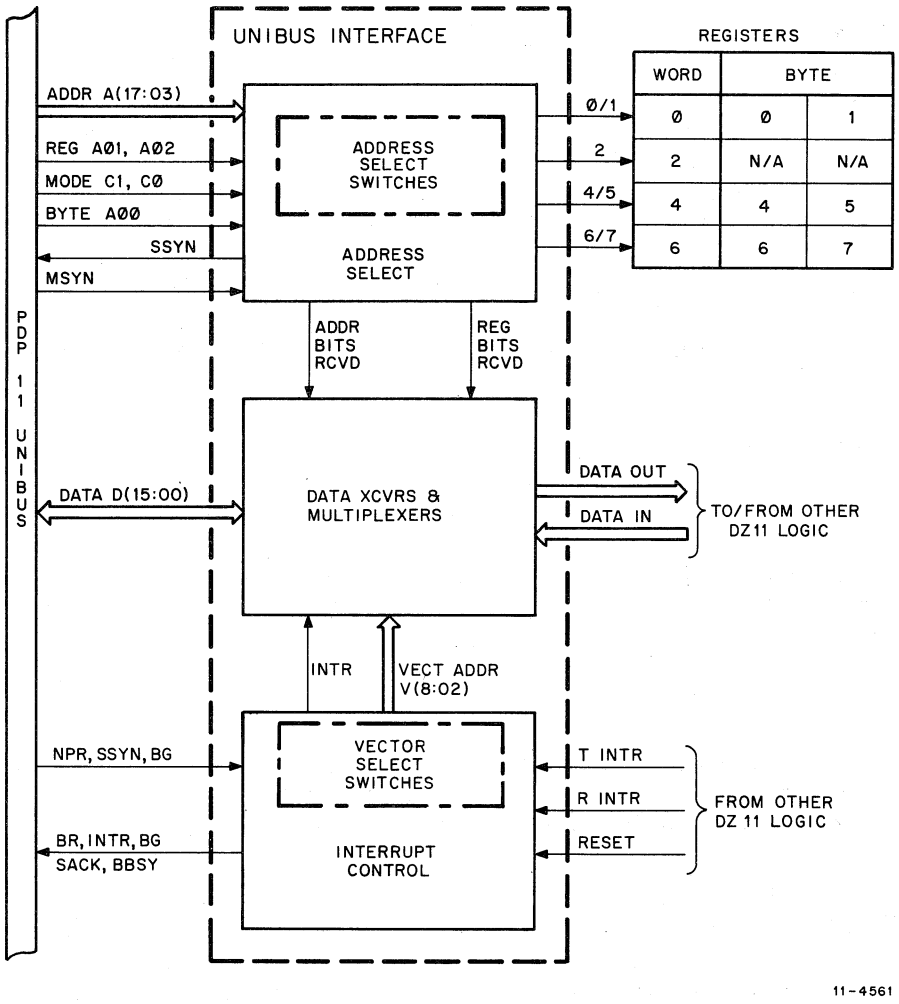
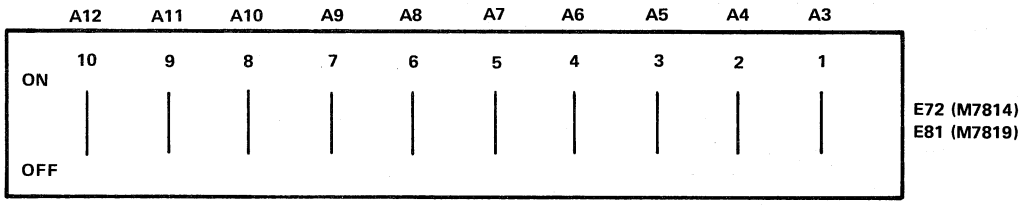


Figure 4-3 Unibus Interface Block Diagram



NOTE:
ADDRESS 160000 - A12 THROUGH A3, OFF
160010 - A12 THROUGH A4, OFF, A3, ON
177770 - A12 THROUGH A3, ON
(OFF = LOGICAL 0, ON = LOGICAL 1)

MA-0803

Figure 4-4 Address Selection Switches

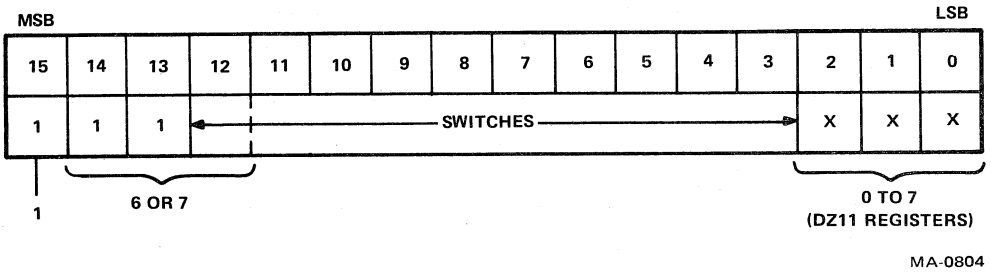


Figure 4-5 Address Word Format

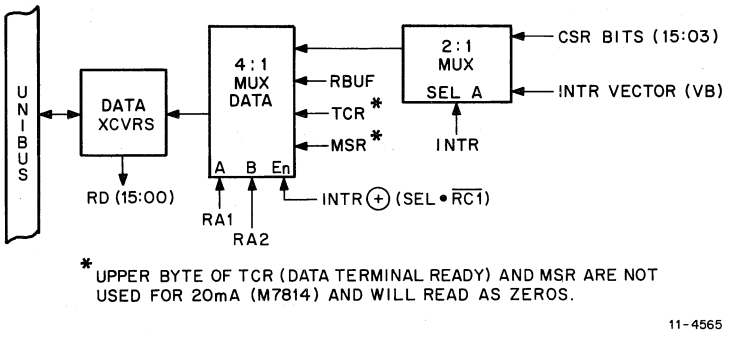


Figure 4-6 Output Data Multiplexer Bit Correlation

4.4.3 Universal Asynchronous Receiver-Transmitter (UART)

The UART is a complete integrated circuit subsystem that transmits and receives asynchronous data in duplex/half-duplex operation. The transmitter and receiver operate independently and thus can operate simultaneously. The transmitter accepts parallel binary-coded characters and converts them to serial formats, and the receiver performs the reverse operation (serial-to-parallel). The UART requires several control signals to properly time its operation with that of the remaining DZ11 circuitry. Each UART is a 1602 integrated circuit, and one chip is used for each line. The baud rate, character length, parity mode, and number of stop bits are selected external to the UART. Figure 4-8 presents a block diagram of UART operation; a more detailed description of the UART is presented in Appendix B.

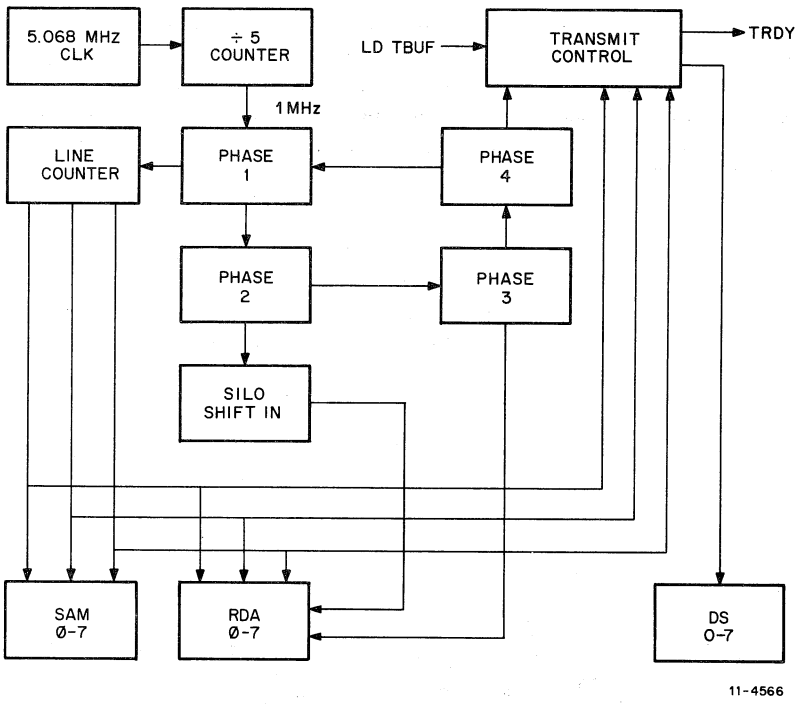


Figure 4-7 Scanner Block Diagram

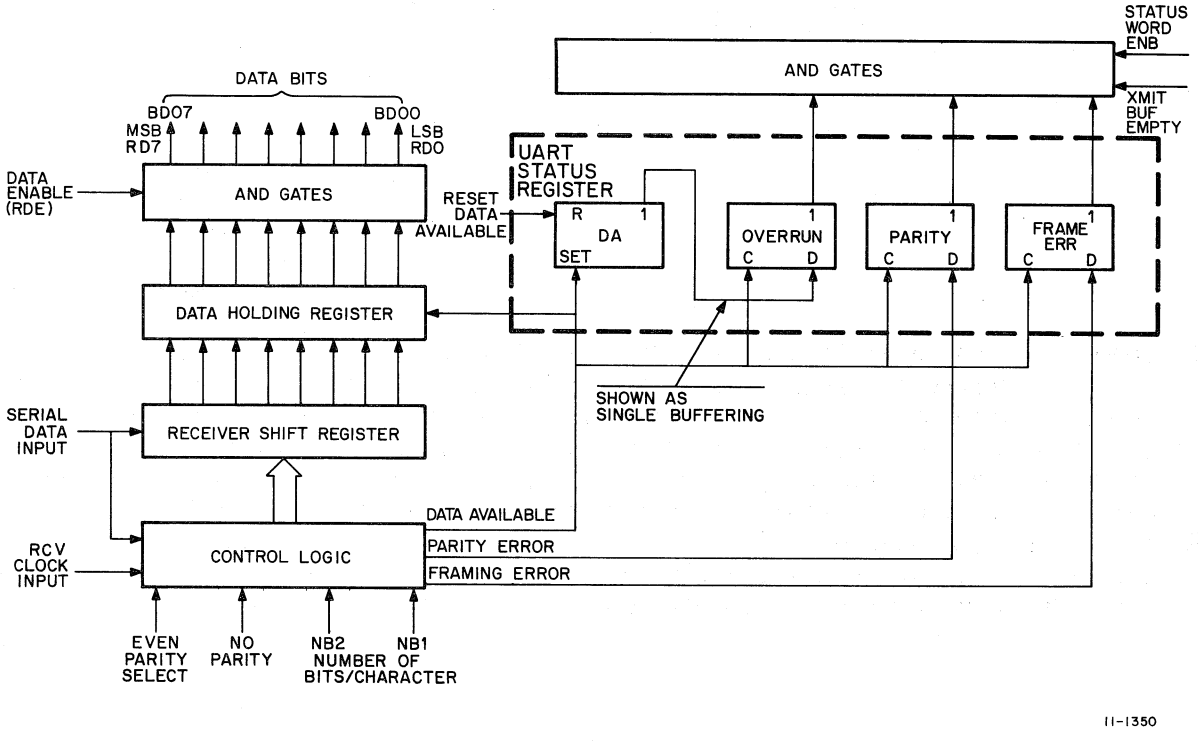


Figure 4-8 UART Block Diagram

4.5 DETAILED FUNCTIONAL DESCRIPTION

4.5.1 Address Selection Logic (Figure 4-9)

The switches and resistor network (shown at the left of Figure 4-9) provide a reference voltage to be used by the voltage comparators. These voltages are compared with Unibus address bits A03 through A12. When a switch is open, a high-level voltage is compared to the incoming address bit; when a switch is closed, a low-level voltage is compared. The outputs of the voltage comparators are wire-ANDed to provide a single output that is at a high level when the device is selected. This only happens when the voltages on all three voltage comparators match; otherwise, the output remains low and the device will not respond. For example, if BUS A03 through BUS A10 are at a high level and BUS A11 and BUS A12 are at a low level, a match only occurs if switches 1 through 8 are closed and switches 9 and 10 are open. From the voltage comparator circuitry, the output is inverted and used by the device response logic and the register select and control logic, and is also sent to the multiplexer control logic (Paragraph 4.5.5).

The device response logic provides a delay to slave sync to allow for decoding and strobing data. LD DATA H is delayed an additional 100 ns to allow the UARTs to decode input data lines. Control signals from the Unibus are gated to select register load commands in the register select and control logic. The output of the voltage comparators enables the register load signal output.

4.5.2 Receiver Interrupt Control (Figure 4-10)

The receiver interrupt signals the processor when the DZ11 receives a character from the terminal and stores the character in the RBUF (silo buffer). After processing by the UART, the character is loaded into the silo, and CSR bit 07 (RDONE) is set; RDONE causes generation of the RINT signal. RINT is fed to the receiver interrupt logic and the BR signal is transmitted to the processor via the Unibus at priority level 5. When the processor status goes below level 5, a BG5 signal is routed through the priority insert (on the DZ11 module) to the BG IN input of the receiver interrupt chip, causing generation of MASTER, BUS SACK, and BUS BBSY. The MASTER signal is inverted and gated to create BUS INTR for transmission to the Unibus. The receiver interrupt is also caused by silo alarm. INTR is created to strobe the vector address to the Unibus from the output data multiplexer.

4.5.3 Transmitter Interrupt Control (Figure 4-10)

The transmitter interrupt occurs when the DZ11 is engaged in character transmission and the processor must be interrupted to request additional data for transmission. The interrupt sequence begins with assertion of TRDY with TIE set, which generates the TINT pulse. TRDY is the result of the line being enabled and the transmit buffer for that line being able to accept a character. The TINT signal begins the processor-DZ11 interrupt dialogue via the Unibus. The transmitter interrupt priority is less than that of the receiver; therefore, bus grants are received only when a receiver interrupt is not in process. The transmitter interrupt logic causes generation of the same signals as the receiver logic, including strobing the vector address; however, the transmitter vector is located two words after the receiver vector. For example, a receiver vector of 300 automatically places the transmitter vector at 304.

4.5.4 Data Transceivers (Figure 4-11)

The data transceivers allow the data to flow directly to and from the Unibus. Lines BUS D (15:00) convert information and control data on the Unibus to the proper levels used by the DZ11 and are sent to the device registers by way of RD (15:00). Information back to the Unibus is presented to the transceivers along lines D (15:00), which come from the output data multiplexer.

4.5.5 Output Multiplexers (Figure 4-11)

This logic controls the flow of information (data and interrupt vector) to the data transceivers for output to the processor via the Unibus. The interrupt control logic sends INTR to control whether the vector bits or data are to be sent to the data transceivers. The INTR pulse goes low to send vector bits. The processor sends two lines, BUS A01 and BUS A02; these are inverted to become RA1 and RA2, which drive the multiplexers' select lines. When a match condition exists in the voltage comparators of the address selection logic, signal SEL is created. This signal, ANDed with RC1 – the inverted BUS C1 signal from the processor (DATI bus cycle) – gates the selected register to the Unibus data transceivers.

4.5.6 Receiver Control Logic (Figure 4-12)

The operation of loading a character into the silo and reading the RBUF is timed by the scanner. As shown in Figure 4-13, at the trailing edge of phase 4 (leading edge of phase 1), the scanner is incremented to the next line for sampling. During phase 1, the data available (DA) flag is sampled. If the flag is set and the silo is not full, a shift-in (SHI) pulse (leading edge of phase 2) moves a character from the UART for that line to the silo. At the trailing edge of phase 2 (start of phase 3), the reset data available (RDA) pulse resets the DA flag if SHI occurred during phase 2. Phase 4 terminates the RDA pulse. The Unibus initiates a character shift out of the silo by reading the RBUF (Figure 4-14).

4.5.7 Transmit Control Logic (Figure 4-15)

The transmission of a character from the DZ11 is primarily controlled by a network of logic circuits called the transmit control section. This network generates the timing signals for line selection, UART control, and data transfer to the modem or terminal connected to the DZ11.

When the TBMT signal goes high, it indicates that the transmitter buffer for the UART being sampled is empty. TBMT is inverted and strobes the appropriate line enable (LINE 0–7) signal through the logic. This occurs under the control of signals SCAN A, B, and C, which provide the proper selected line. The transmitter control operates in four phases (Figure 4-16). The phase 1 pulse is delayed 50 ns to allow propagation time through the circuit and to avoid race conditions. As phase 1 ends and phase 2 begins, the delay ensures that the proper line is latched up at the 8-bit addressable latch before data changes. After passage through D-type flip-flop chips, the line select data reaches the priority encoder. The priority encoder outputs signals TLINE A, B, and C, which are sent to the output data multiplexers. Signals from the priority encoder inhibit gates feeding the clock for the D-type flip-flop chips. This prevents the inputs to the priority encoder from changing until the line has been serviced or disabled by the programmer.

Character transmission is allowed for the first 400 ns of phases 2, 3, and 4 during CLK H pulses only. During phase 1, transmission is inhibited to allow sampling of line enable bits. Outputs from the Character Loaded flip-flop and priority encoder are used to generate the transmit ready (TRDY H) pulse, which signifies that a line is available for transmission. Transmission is initiated by loading the transmit buffer register (TBUF). This causes the Character Loaded flip-flop to set; TRDY H drops and cannot be asserted again until this flip-flop is cleared. If all conditions for transmission are satisfied, a 300 ns one-shot allows data strobe (DS) to the UART. DS loads the contents of the TBUF into the UART and transmission starts. The correct DS pulse is a function of the TLINE outputs from the priority encoder. Priority level is achieved in the priority encoder by having each ascending numbered input take priority over the input with the lower number. The 300 ns pulse is also gated to pin 14 of the 8-bit addressable latch and opens the latch selected by input pins 1, 2, and 3. During phases 2, 3, and 4, these inputs are the TLINE bits from the priority encoder; the data input (pin 13) is at ground level, so that the latch for this line is cleared. In addition, the pulse causes the priority encoder to turn off after it times out. This makes pin 14 of the priority encoder go high and causes a clock output from pin 11, G3. This output updates the 8-bit register from the addressable latch outputs and presents a new set of inputs to the priority encoder. Pin 11 of G3 also triggers a 150 ns one-shot, which allows for propagation delay and data settling time at the priority encoder inputs. When this delay times out, flip-flop G1, pin 5, is cleared and G2, pin 4, is disabled. The output of this gate goes low and turns the priority encoder on.

The output of E2, pin 6, gates the reset for the Character Loaded flip-flop to clear for the next transmission. If another line is ready to transmit, pin 14 of the priority encoder will go low and the TRDY signal will be reasserted. The TLINE signals will contain the value of the next line ready for transmission. If the line enable bit is turned off, the 300 ns pulse occurs but no DS will be sent to the UART because pin 5 of G4 is low and disables G5.

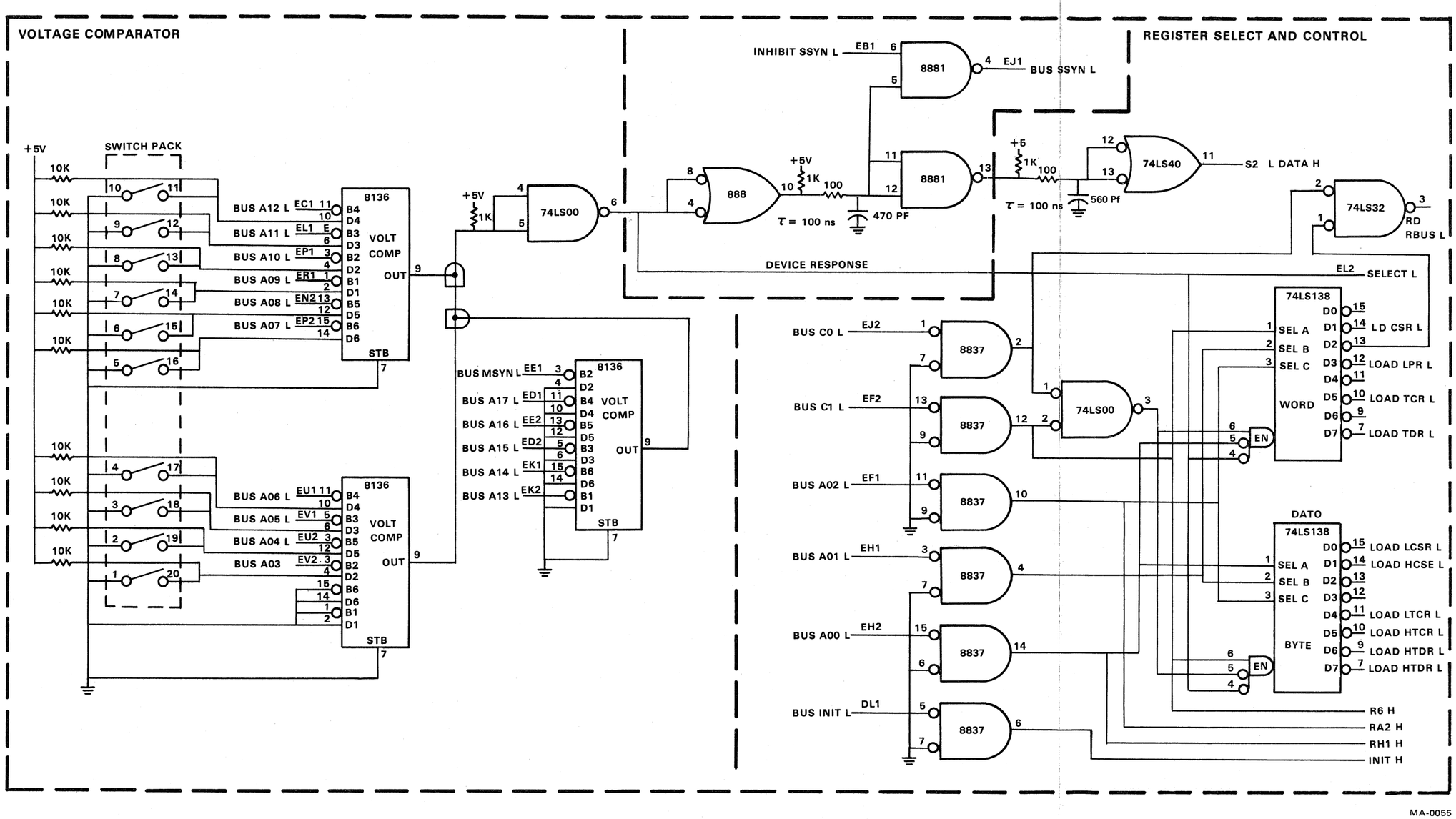


Figure 4-9 Address Selection Logic

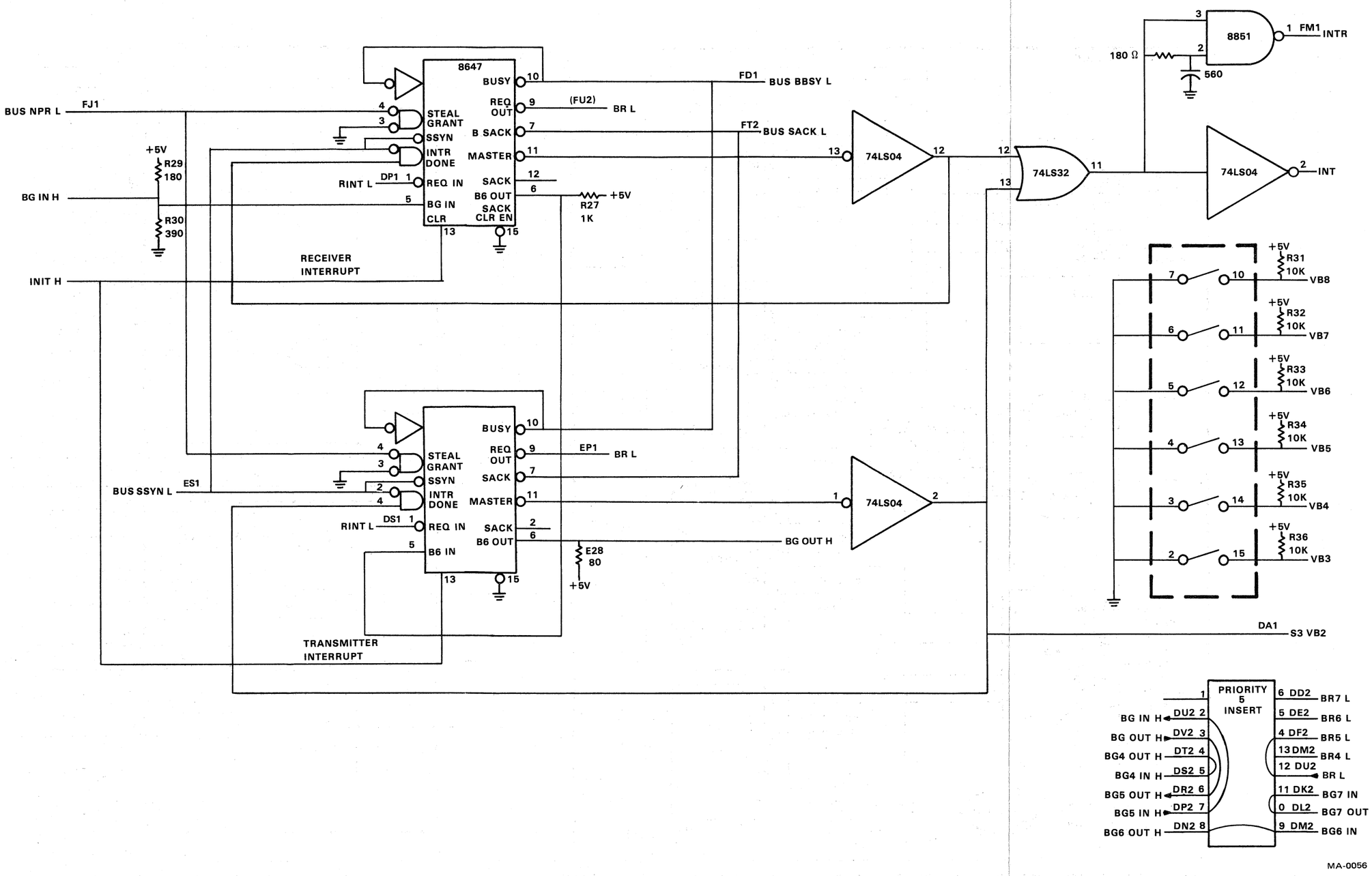


Figure 4-10 Interrupt Control Logic

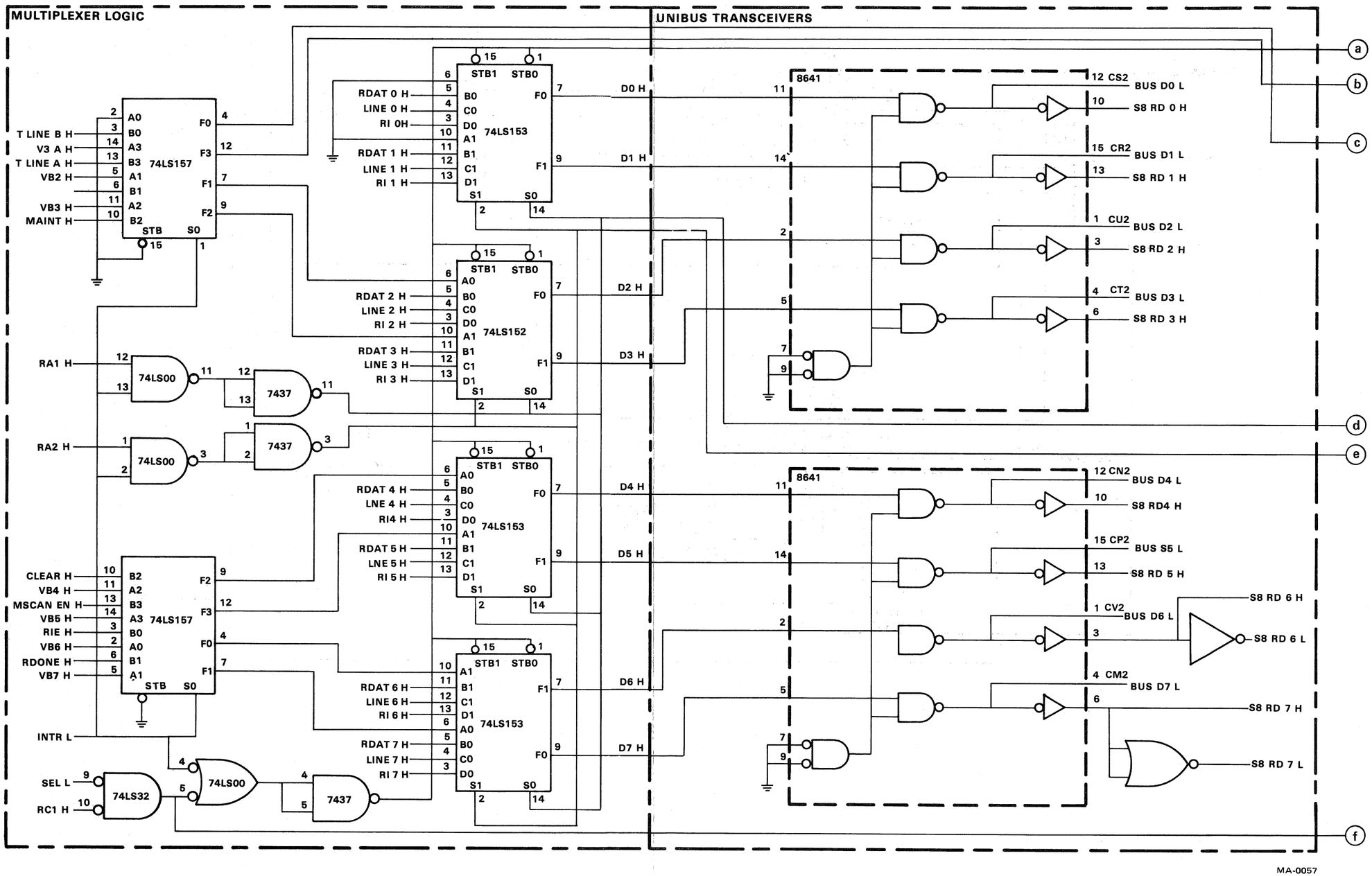


Figure 4-11 Unibus Data Flow
(Sheet 1 of 2)

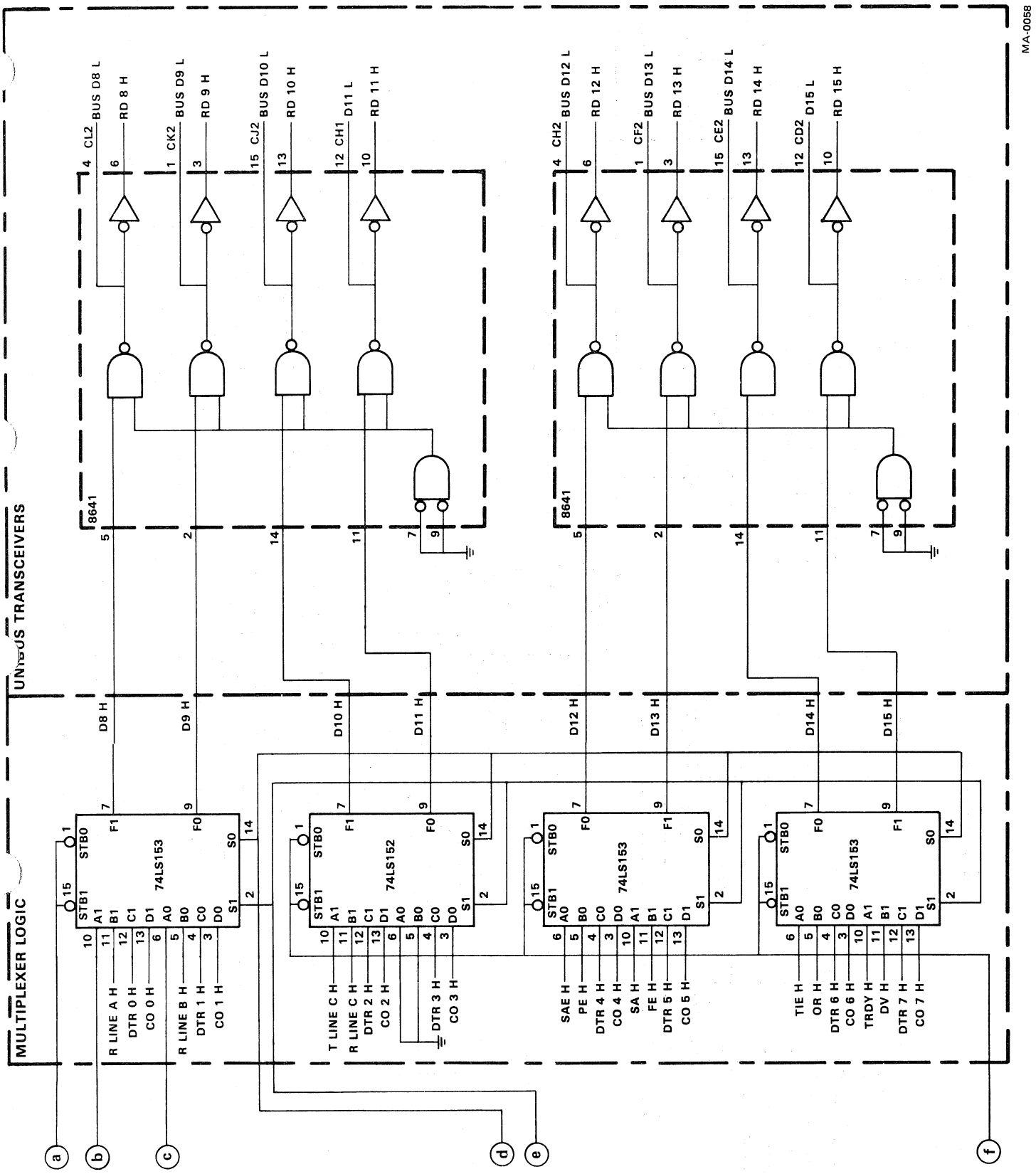


Figure 4-11 Unibus Data Flow
(Sheet 2 of 2)

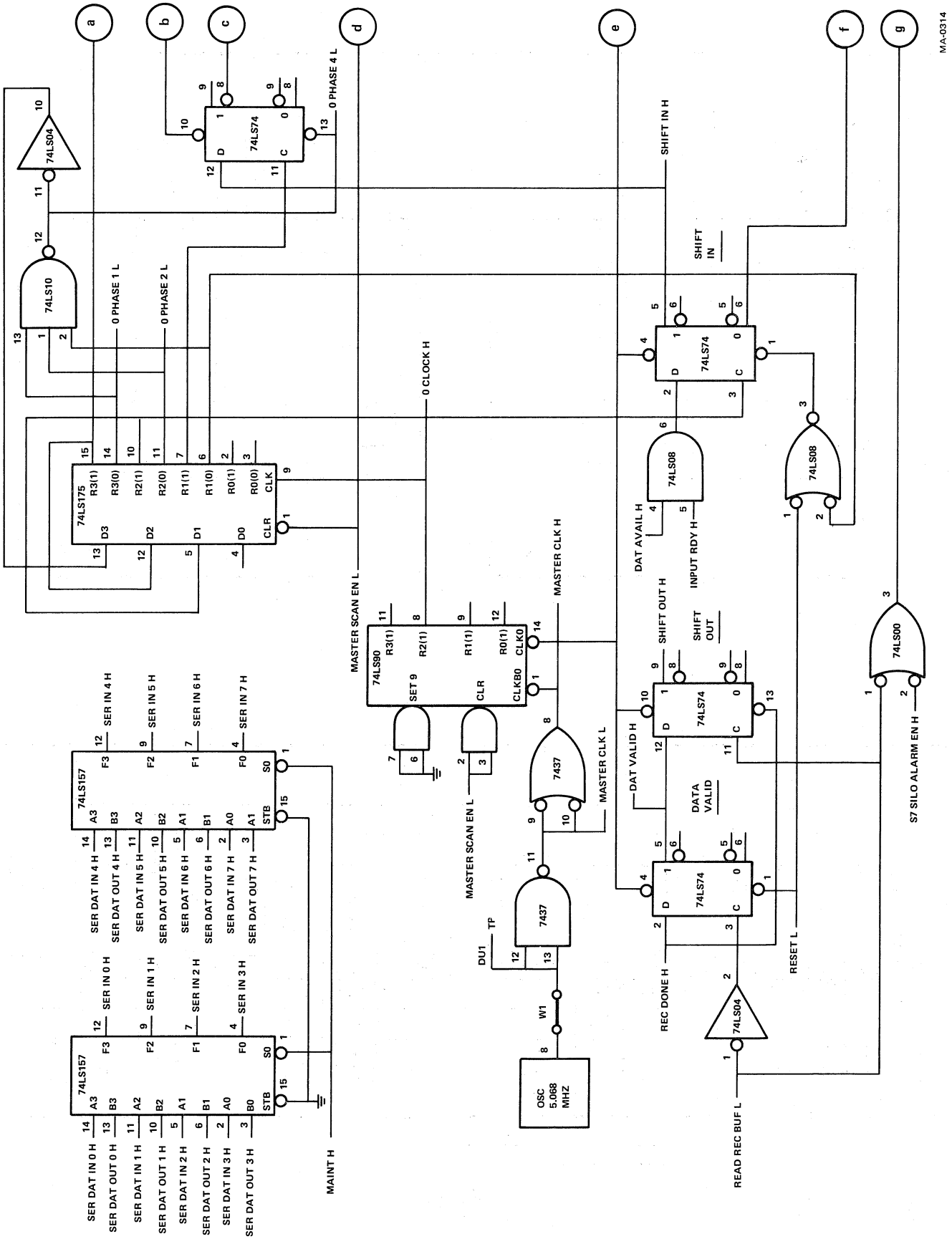


Figure 4-12 Receiver Control Logic
(Sheet 1 of 2)

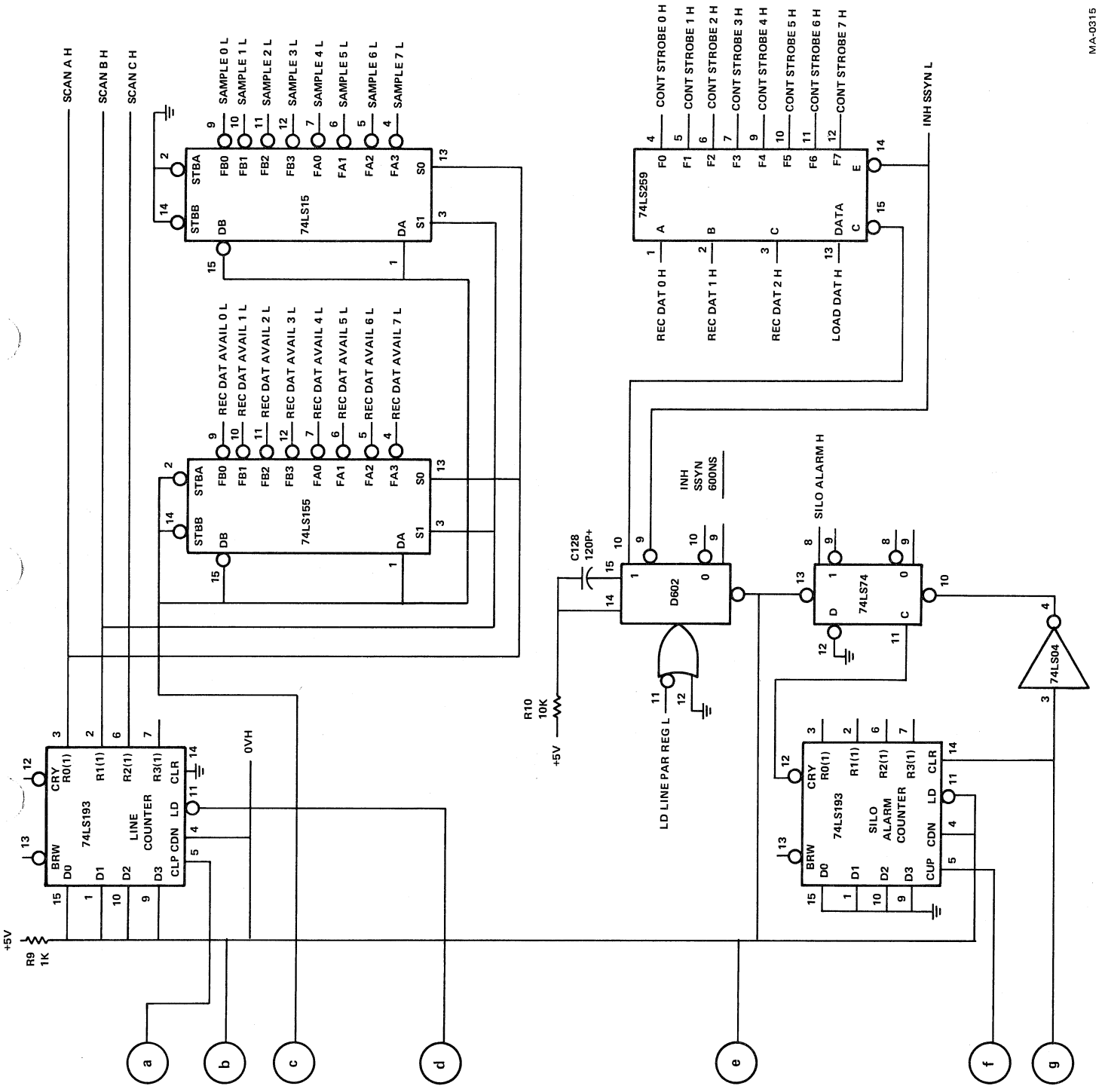


Figure 4-12 Receiver Control Logic
(Sheet 2 of 2)

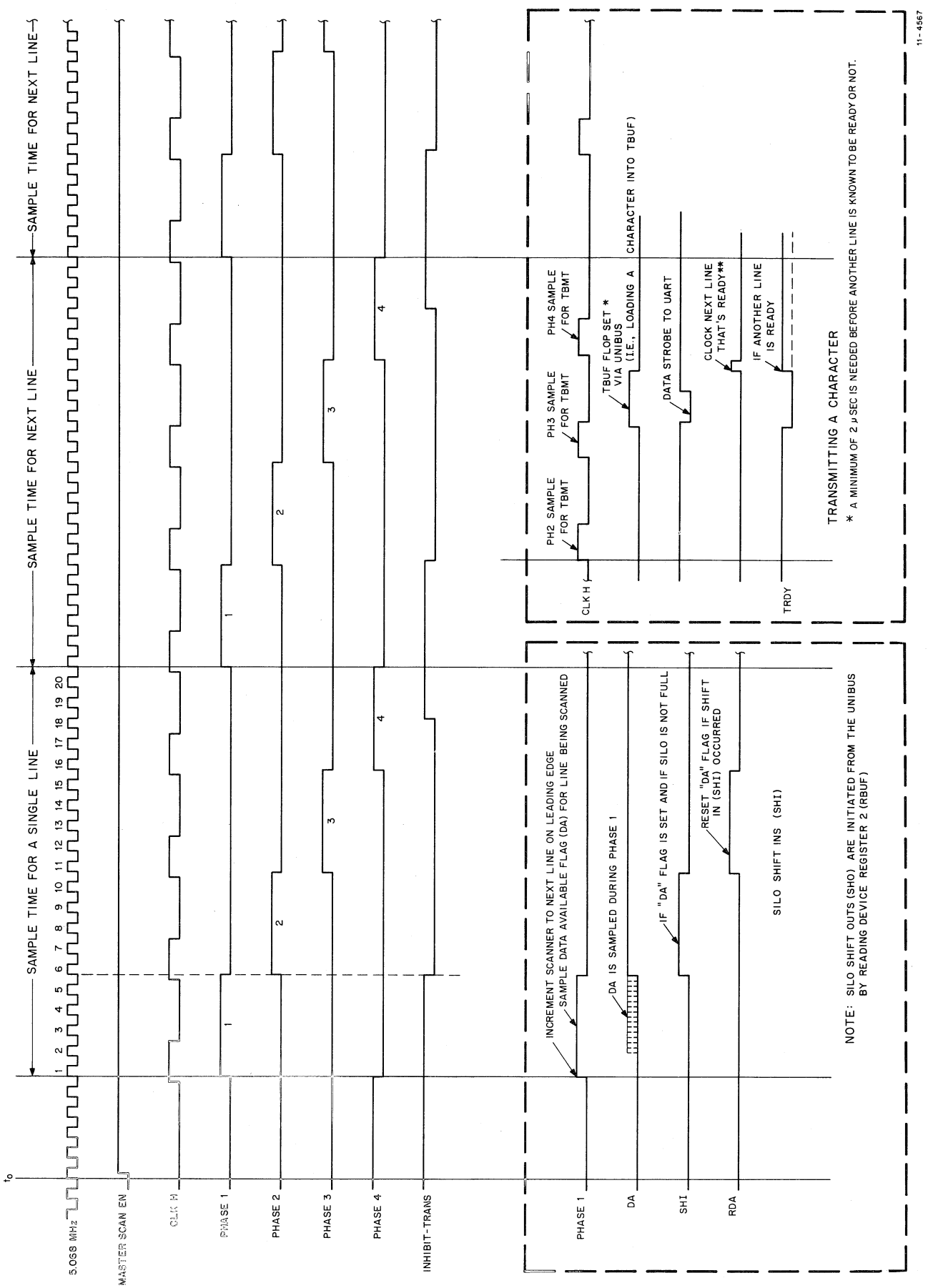


Figure 4-13 DZ11 Scanner Timing

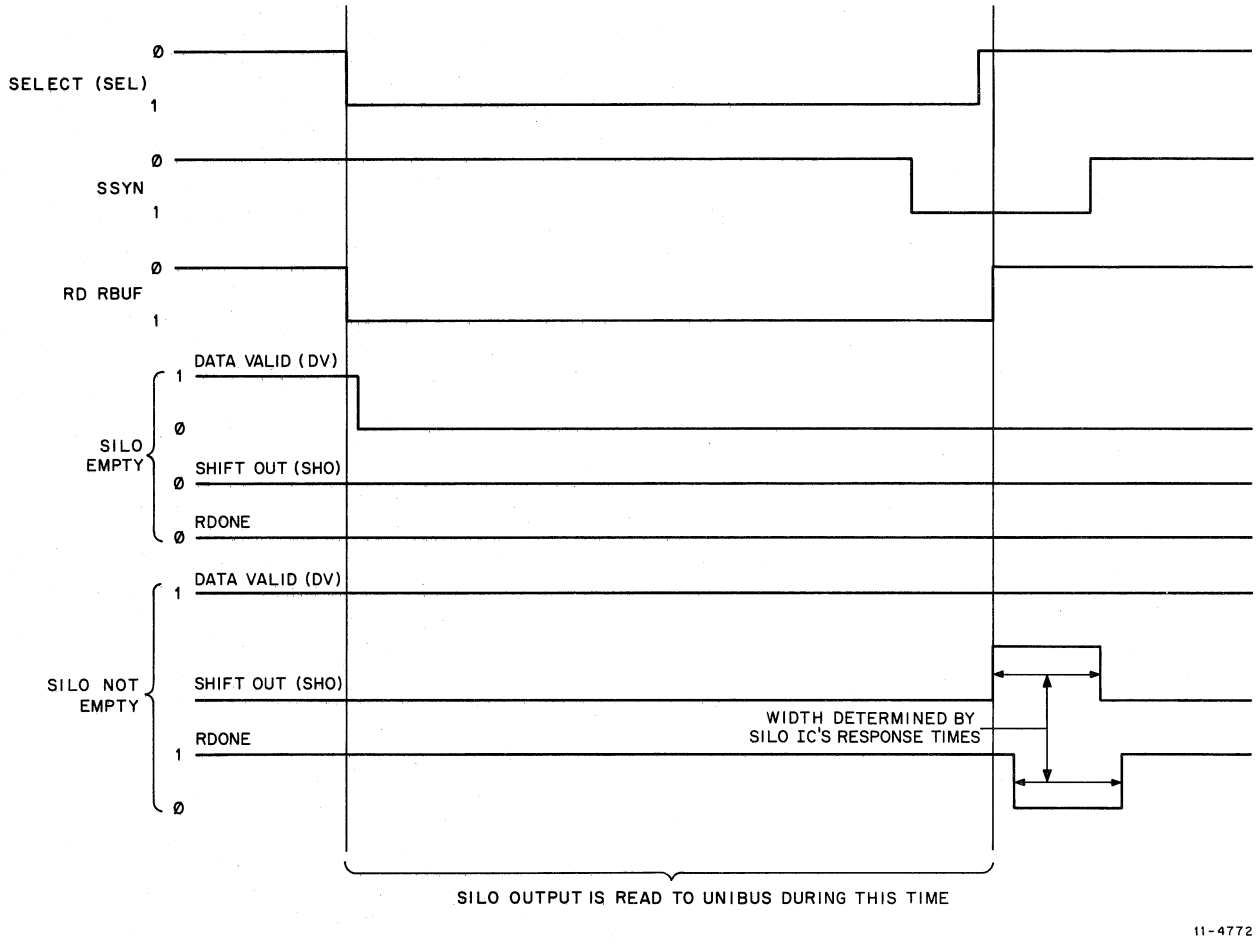


Figure 4-14 Silo Character Shift Out Timing Diagram

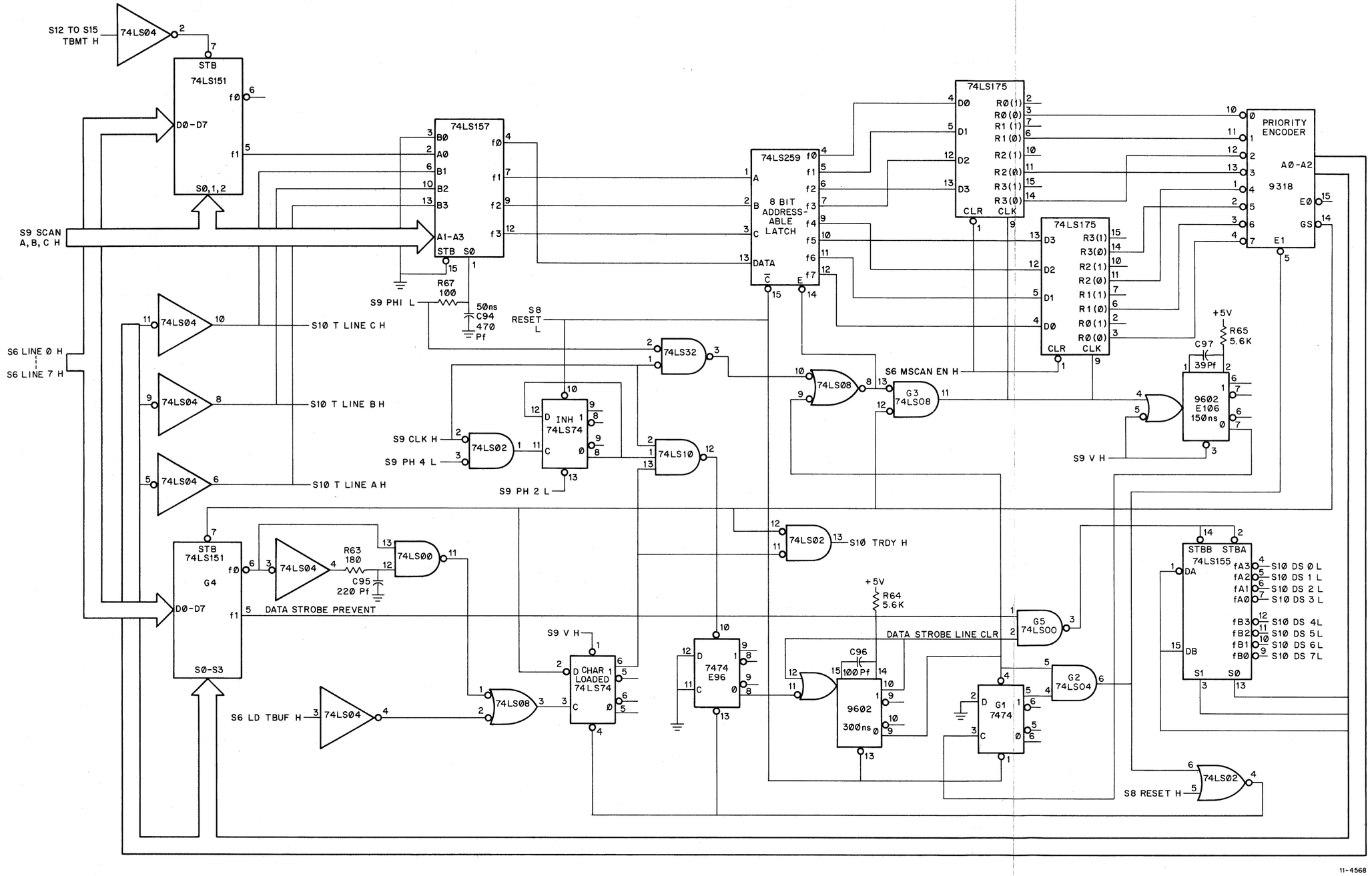


Figure 4-15 Transmit Control Logic

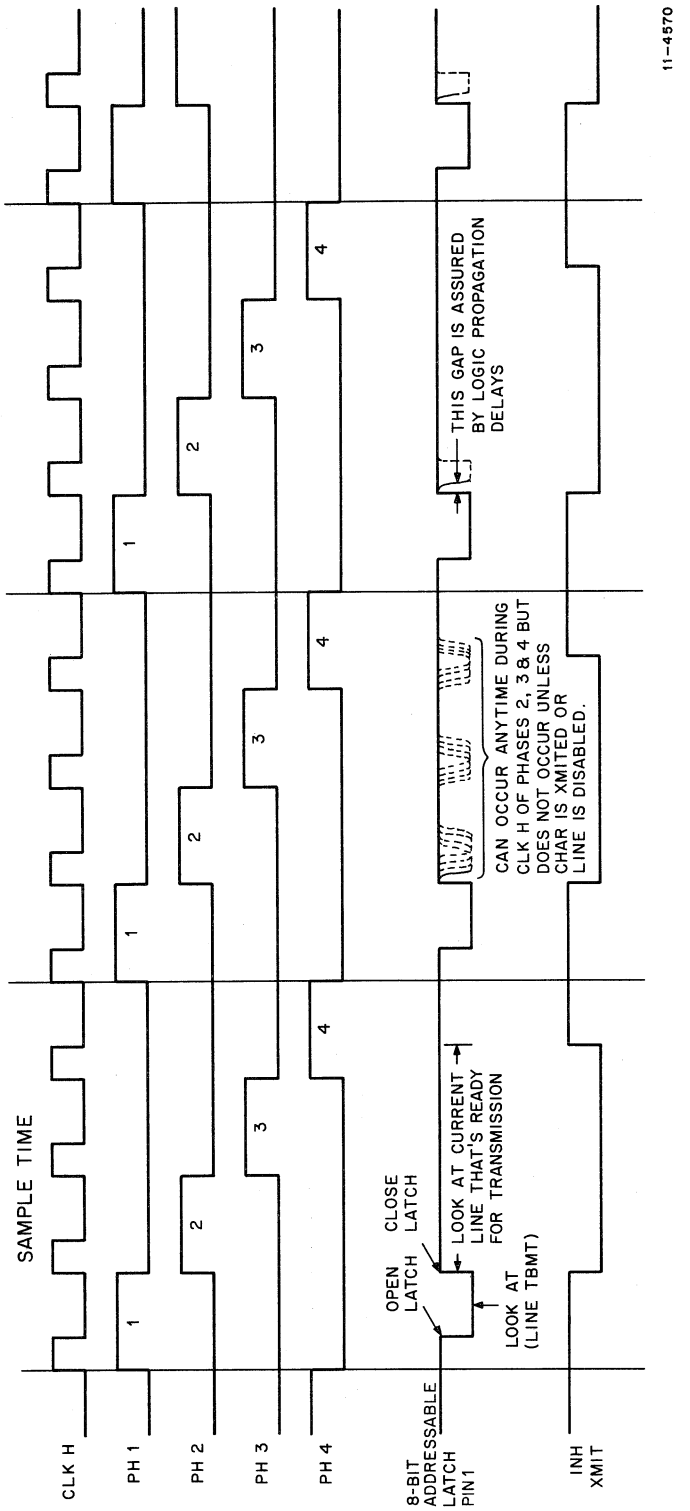


Figure 4-16 Transmit Control Timing

4.5.8 Registers

The DZ11 uses four device registers in a manner that yields six uniquely accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input/output data, establish DZ11 operating status, and monitor control signal conditioning. Depending on the function of the register, some are accessible in bytes or words; others are restricted to word-only operations. Since registers can be read or written into, the selection of either a read or write operation allows two of the device registers to function as four independent registers.

The subsequent paragraphs describe the operation of each DZ11 register. Refer to Chapter 3 of this manual for additional information regarding register bit assignments, bit functions, and programming techniques.

4.5.8.1 Control and Status Register – The control and status register (CSR) comprises two 74LS175 chips (Figure 4-17). Additional gates are used to control the register and generate signals that are CSR bits but are not stored in the 74LS175 chips. The Unibus lines, after routing through the DZ11 bus transceivers, direct the operation of the DZ11 in accordance with the PDP-11 system requirements. Bits RD (03:06), RD12, and RD14 are stored in the CSR chips since they are read or write bits. The CSR is controlled by LD HCSR, LD LCSR, and LD CSR signals from the address selection logic. These signals are gated to the CSR chips to yield selection of the upper (HCSR) or lower (LCSR) portions of the register. The RINT and TINT signals are produced by the outputs of the CSR and other logic that receive signals required to generate receiver and transmitter interrupt commands. TheCSR is reset by a RESET L pulse to the CLR input of the chips. The LD CSR signal activates both CSR bytes and accomplishes the loading of the entire CSR. Several bits (00, 01, 02, and 11) are not used and have no effect on DZ11 operation.

4.5.8.2 Receiver Buffer – The receiver buffer (RBUF) is a read-only register that contains the received character (lower byte), the receiver line number (bits 08–10), and four character-condition signals relating to errors in reception (bits 12–15). Bit 11 is not used in the RBUF. The RBUF read command is generated in the address select logic. The RD RBUF signal is inverted and fed to the receiver control logic to cause the first-in character of the silo to be read from the "bottom" (RBUF) of the silo. The trailing edge of the RD RBUF command causes a SHO H signal to be sent to the silo to shift the next character down through the 16-character positions. (Refer to sheet 11 of engineering drawing M7819-0-1 or sheet 12 of M7814.)

4.5.8.3 Line Parameter Register – The line parameter register (LPR) is a write-only segment of device register 2 (Figure 4-18). The LPR contains various line parameters such as line number, character length, stop code, parity, DZ11 baud rate, and a receiver-on bit. Bits 13–15 are not used. The LD LPR signal is generated by the address select logic and fed to a 500 ns one-shot that drives an 8-bit addressable latch and inhibits SSYN from being asserted on the Unibus. The latch is open and the LD DATA L signal is gated to the proper UART, selected by RD (02:00). This is the control strobe (CS) signal that loads the line parameter data for that line (e.g., character length, stop bits, and parity). The CS signal occurs approximately midway into the inhibit SSYN signal; this allows proper data setup time for the UART inputs. Refer to Figure 4-19 for the timing of the CS signal.

The second latch records bit 12 and turns on the receiver clock (RCLK) for the selected line. Bits 08 through 11 are strobed into the baud rate generator chips by the CS pulse. The output of this chip is the transmitter clock (XCLK), which is gated by the condition of the output from the second latch to give the RCLK for the UART.

4.5.8.4 Transmit Control Register (Refer to Engineering Drawing M7819-0-1, sheets 5 and 6, or M7814-0-1, sheets 6 and 7) – The transmit control register (TCR) is a read/write register that comprises four 74LS175 chips, two for the low byte (line transmission enable) and two for the high byte. The high byte is used on the EIA version only and contains the data terminal ready (DTR) flags. Setting or clearing a bit in this byte will turn the appropriate DTR signal on or off. The low byte contains a line

enable bit for each line. A set bit allows transmission on the corresponding line. The register is controlled by LD TCR, LD LTCR, and LD HTCR signals from the address select logic. The inputs to the register originate from the Unibus lines and pass through the bus transceivers. The low byte of the TCR is cleared by RESET L and the high byte is cleared by INIT L.

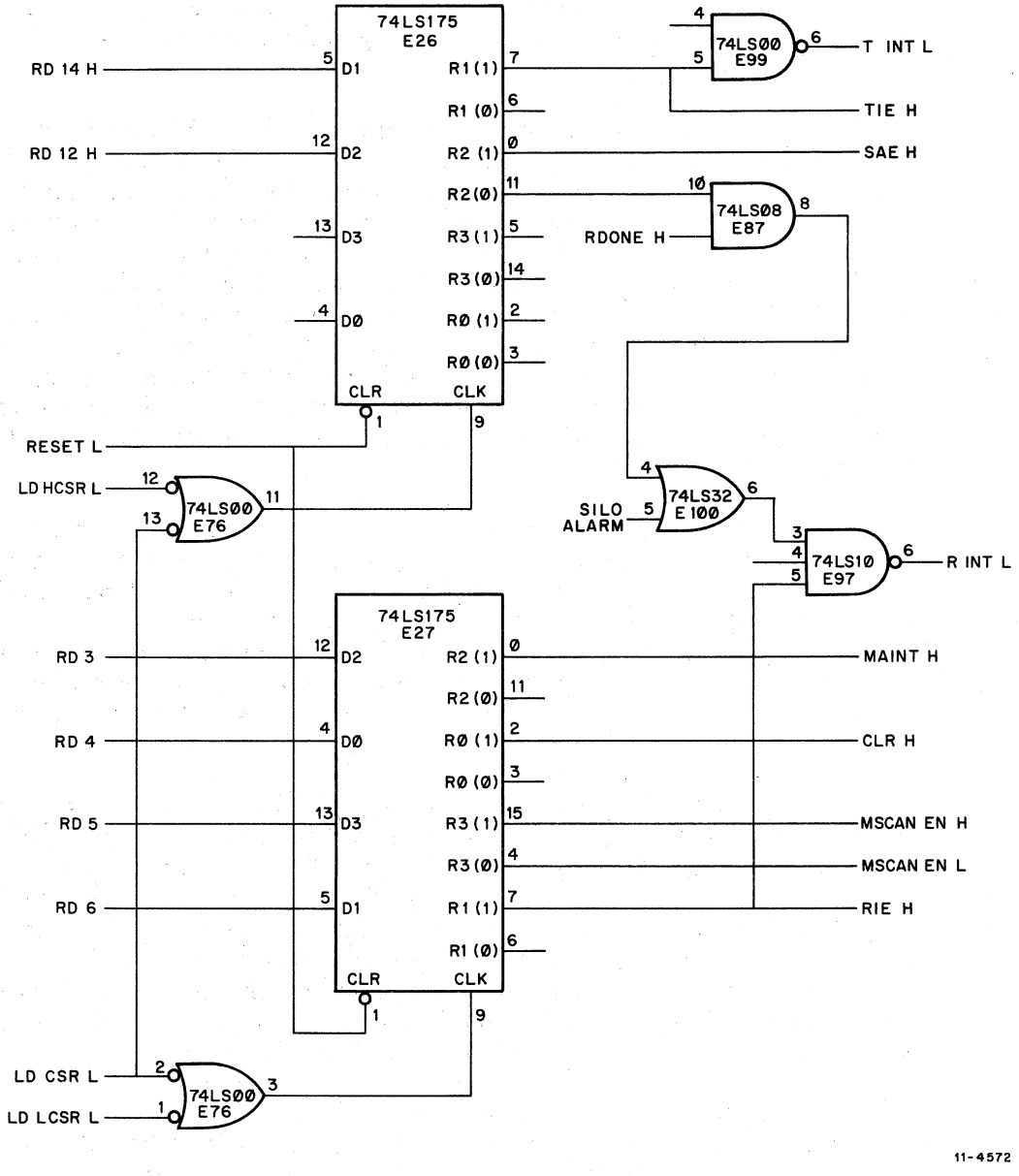


Figure 4-17 CSR Diagram

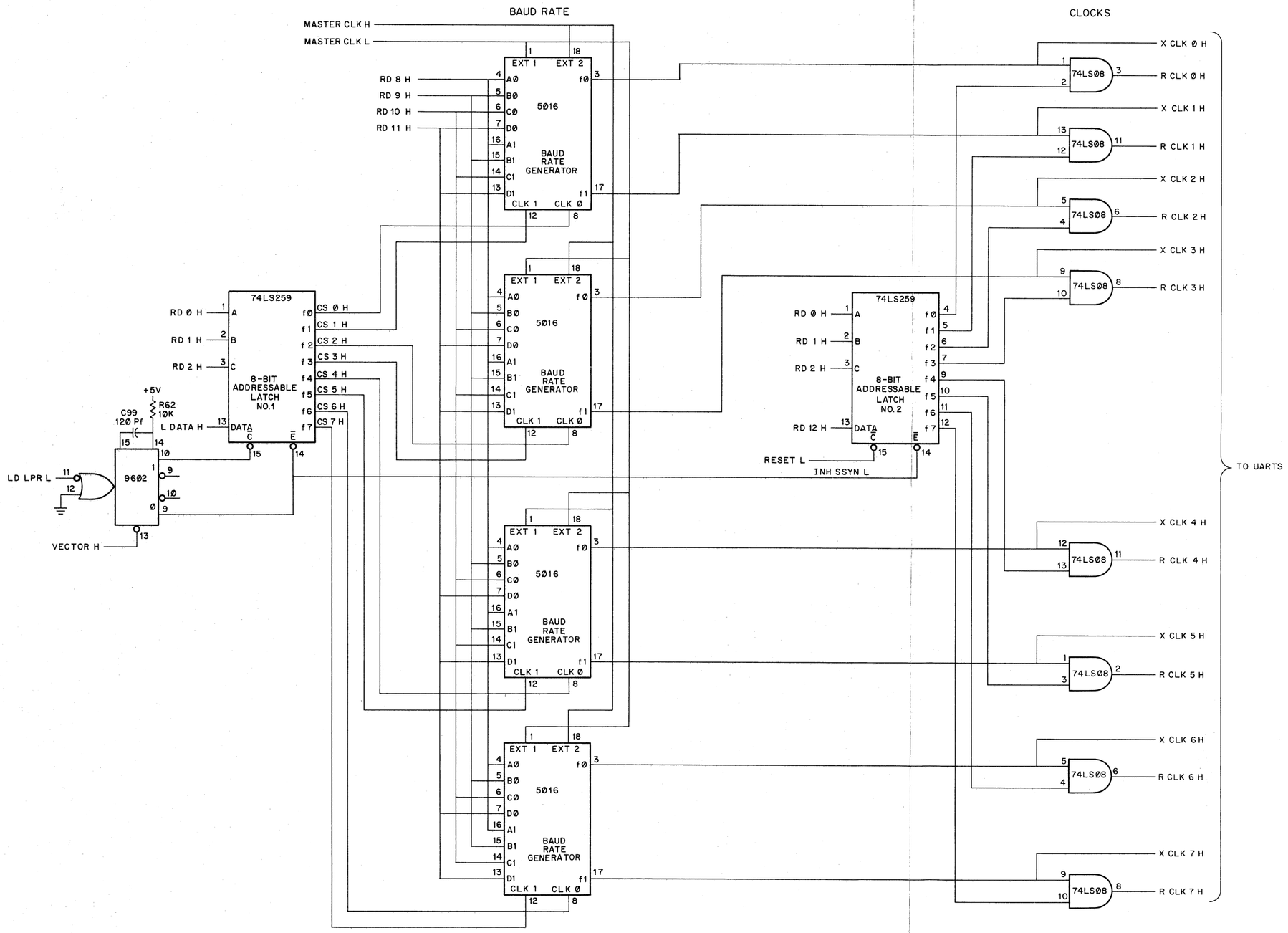


Figure 4-18 LPR Diagram

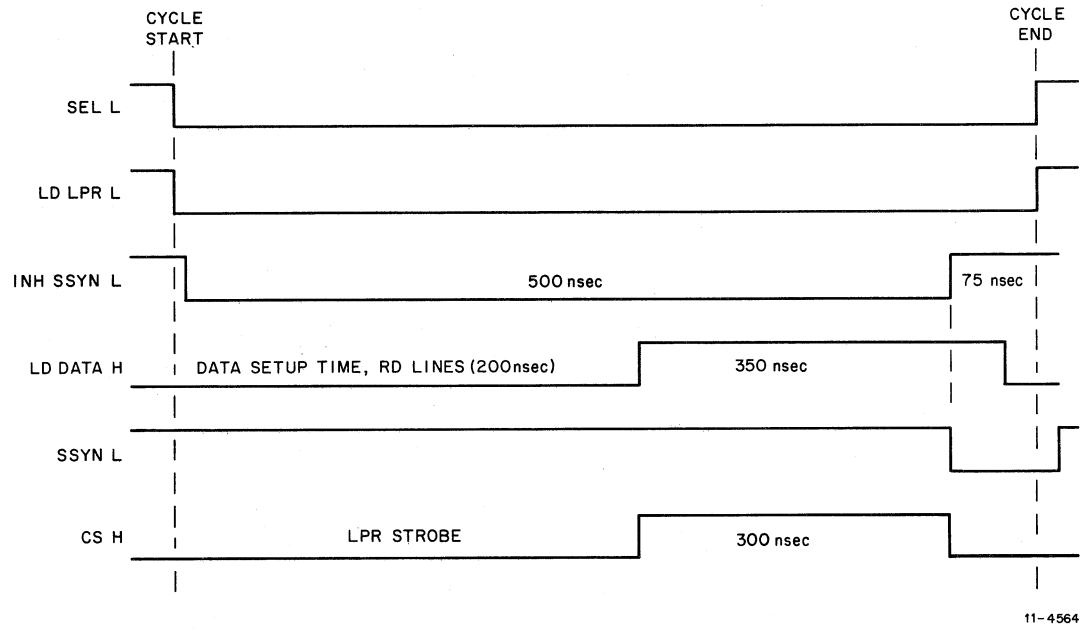


Figure 4-19 Line Parameter Loading

4.5.8.5 Modem Status Register (Not Used for 20 mA Version) – The modem status register (MSR) is a read-only segment of device register 6. The MSR shown in Figure 4-20 examines data relative to the status of modem operation on each line, such as ring indication (low byte) and carrier-on flags (high byte). The register is dynamic in that it represents the current state of these lines. These lines must be continuously monitored as transitions on them do not cause interrupts.

4.5.8.6 Transmit Data Register (Refer to Engineering Drawing M7819-0-1, sheets 5 and 6, or M7814, sheets 6 and 7) – The transmit data register (TDR) is a write-only segment of device register 6. The TDR, using four 74LS175 chips, comprises two bytes; the low byte contains the character (TBUF) to be transmitted, and the high byte contains the break (BRK) bits for each line. When the BRK bit is set, the line transmits zeros continuously. This is accomplished by a NAND gate for each line that requires the BRK signal and SDO (serial data out) to produce the TRANS 0–7 L signals. The TDR is cleared by the RESET L pulse; for character lengths less than eight bits, the character must be right-justified, as the most significant bits are forced to zero. The TDR is controlled by LD HTDR, LD LTDR, and LD TDR commands from the address select logic.

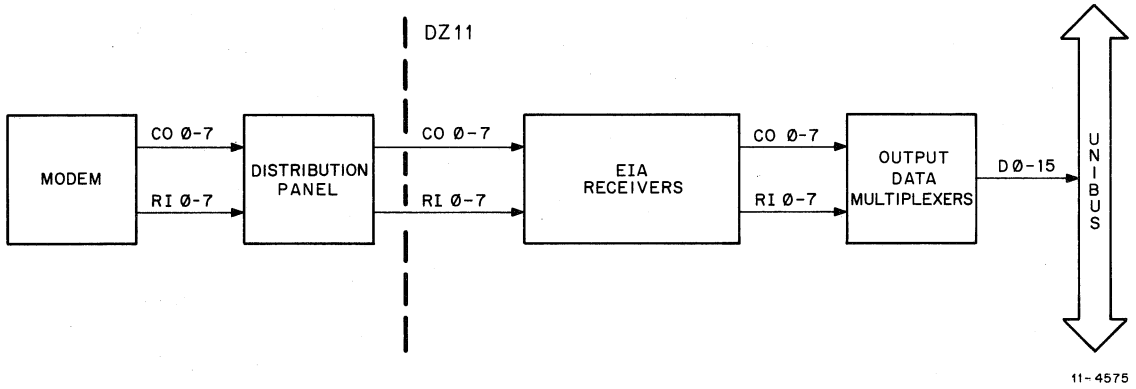


Figure 4-20 MSR Diagram

CHAPTER 5
MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

The DZ11 maintenance philosophy assumes that proper and regular preventive maintenance can eliminate most equipment failures before they occur. The DZ11 module is designed so that module replacement can restore the system to operating status in minimum time. The corrective maintenance procedures contained in this manual are designed to assist Field Service personnel in detecting component malfunctions on the DZ11 module and ensuring proper DZ11 operation within the integrated system. Prior to performing the procedures outlined in this chapter, the material presented in the previous chapters should be thoroughly understood.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of running diagnostics, visual inspection, operational checks, adjustments, and replacement of marginally operating components. The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Normally, preventive maintenance consists of inspection and cleaning after every 600 hours of operation or every 4 months, whichever occurs first. For extreme conditions of temperature, humidity, or dust, and with abnormally heavy workloads, more frequent maintenance may be necessary. It is recommended that the DZ11 diagnostic (MAINDEC-11-DZDZA-REV-PB) be run once a week as part of the normal preventive maintenance schedule.

5.3 TEST EQUIPMENT REQUIRED

Maintenance procedures for the DZ11 require the test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes.

Table 5-1 Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 454 or equivalent
Module Extender	DIGITAL	W904 Hex double-sided
Modem Control Connector	DIGITAL	H315 or 325
Diagnostics	DIGITAL	MAINDEC-11-DZDZA MAINDEC-11-DXDZA MAINDEC-11-DZDZB
Staggered Turnaround Connector	DIGITAL	H3271* or H3190

*H327 may be used in place of H3271.

5.4 DZ11 MAINTENANCE SOFTWARE

The DZ11 makes use of three different software packages which diagnose problems at the module level; verify operation at the system level; and verify operation over a communication's network channel. This software includes:

1. The DZ11 diagnostic (MAINDEC-11-DZDZA)
2. The DZ11 system software exerciser module (MAINDEC-11-DXDZA)
3. The interprocessor test program (ITEP) overlay (MAINDEC-11-DZDZB).

5.5 CORRECTIVE MAINTENANCE

The corrective maintenance procedures are designed to aid the maintenance technician in isolating and repairing faults within the DZ11 module. The technician must therefore be equipped to determine that the DZ11 is, in fact, at fault.

The diagnostic programs comprise the basic tool used by the technician to isolate faults. The diagnostics exercise the DZ11 in four distinct maintenance modes and provide printouts indicating the results. The printouts point the technician to a particular logic area. The technician then uses standard test equipment (oscilloscope and probe) to further isolate the fault to a specific circuit component.

The four maintenance modes are:

1. Internal Loopback
2. Staggered Loopback
3. External (EIA only)
4. On-Line with Terminal

5.5.1 Internal Loopback Mode

This mode is run first because it is the simplest. Bit 03 of the control and status register (CSR) is set. The output serial data from the UARTs are turned around into their respective serial data inputs. All lines are turned around simultaneously, but bypass the EIA level converters (or 20 mA loop circuits).

5.5.2 Staggered Loopback Mode

This mode utilizes test connector H3271* for the EIA version, or H3190 for the 20 mA loop version. The staggered loopback is designed to test the output level converters (EIA) and to check all UART parameters.

When the staggered loopback mode is run, bit 03 of the CSR must not be set. The lines are turned around as follows: line 0 transmits to line 1, line 1 transmits to line 0. The remaining lines are similarly paired (i.e., lines 2 and 3, 4 and 5, 6 and 7).

5.5.3 External Mode

This maintenance mode is used in the EIA version only. An H315 or H325 loopback connector is attached to the customer end of the BC05D cable that originates at the distribution panel.

When exercising the external mode, the lines are run to the point where the customer or user connects.

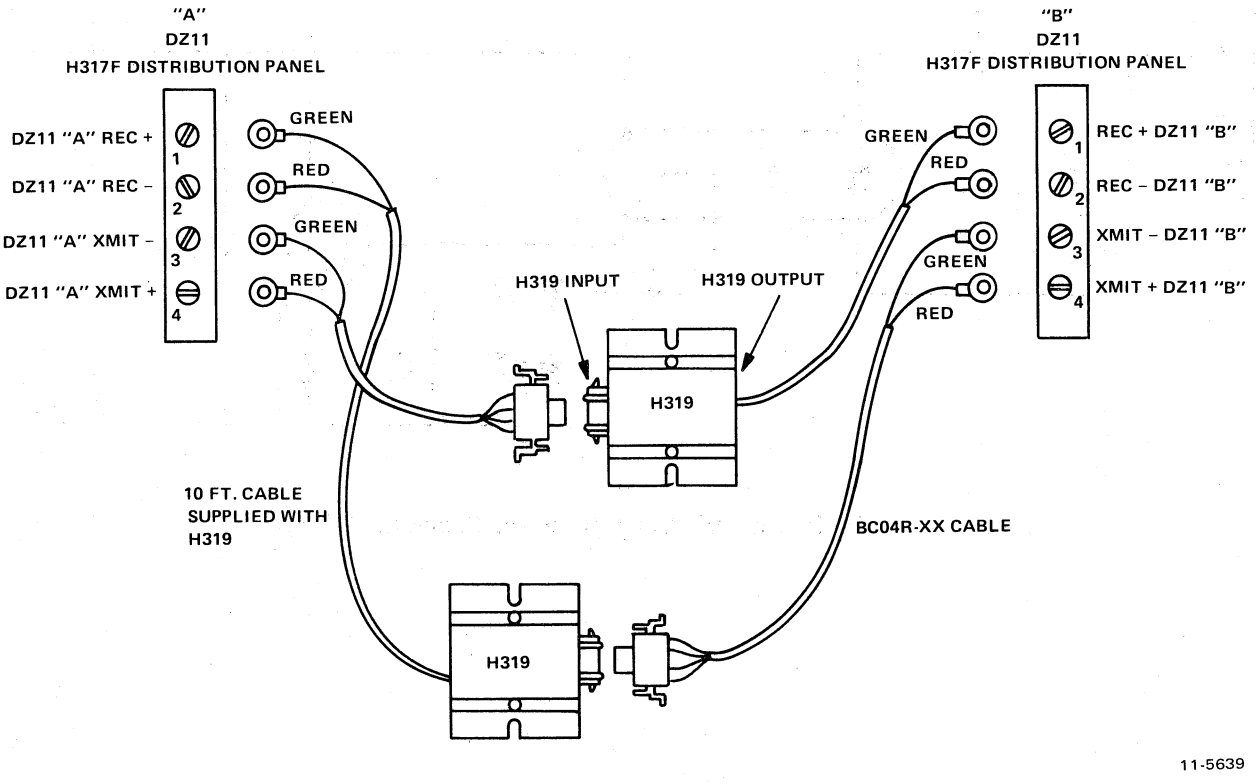
5.5.4 On-Line with Terminal

During this test, a 20 mA or EIA terminal is connected to a single line on the distribution panel. All lines are checked individually by means of an ECHO test which is part of the diagnostics.

*H327 may be used in place of H3271.

APPENDIX A
DZ11 (M7814) TO AN ACTIVE DEVICE INSTALLATION

When a 20 mA DZ11 is used with another active device, two H319 current loop receivers must be used. Figure A-1 provides an example of the connections involved when the DZ11 is used with another active device, in this case another DZ11. A schematic of the H319 is shown in Figure A-2.



NOTE: THE CABLE ATTACHED TO THE H319 SHOULD HAVE THE CONNECTOR REMOVED AND RING LUGS ATTACHED TO THE RED AND GREEN LEADS AS SHOWN.
THE BLACK AND WHITE LEADS IN THE H319 CABLE AND BC04R CABLE ARE NOT USED.

Figure A-1 DZ11 (M7814) to Active Device Connection

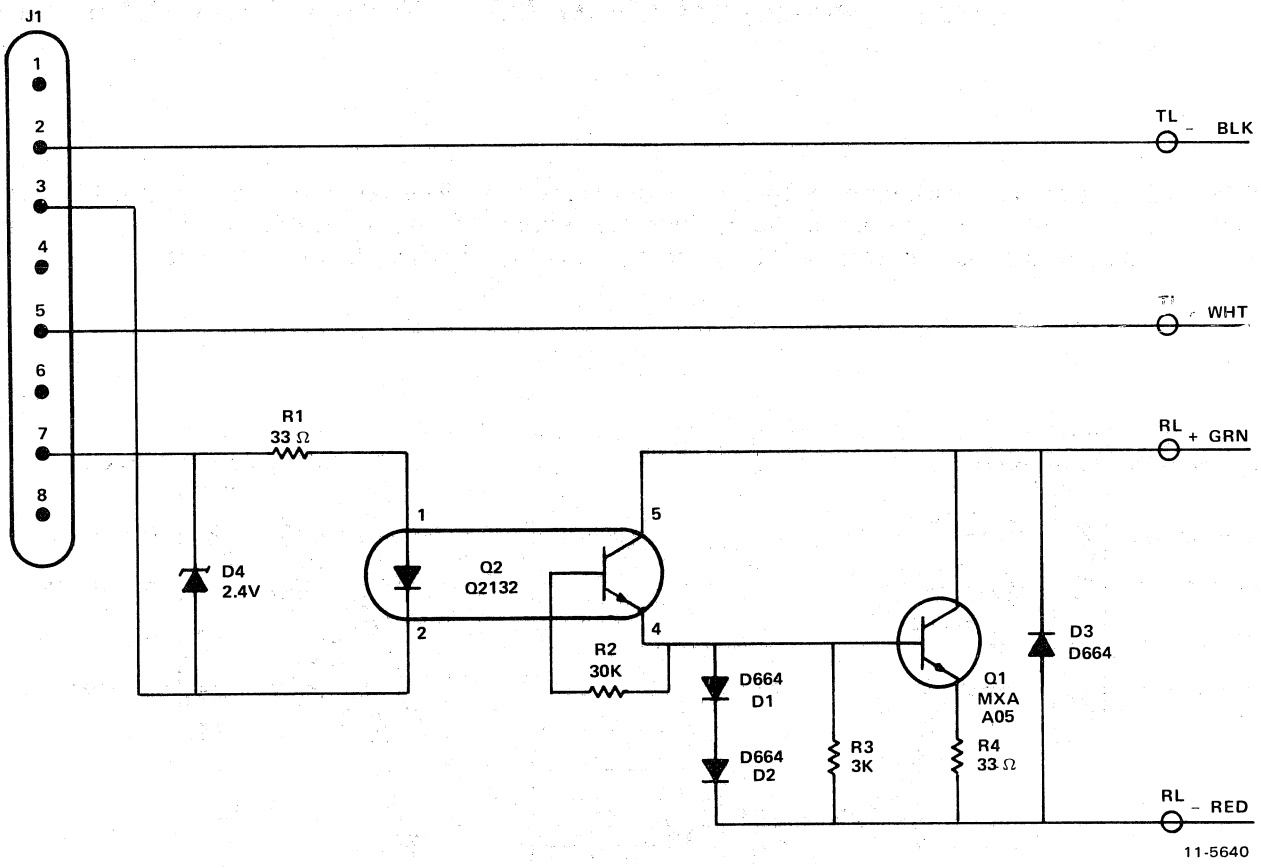


Figure A-2 H319 Current Loop Receiver Schematic Diagram

APPENDIX B
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The UART is a MOS/LSI device packaged in a 40-pin DIP. It is a complete subsystem that transmits and receives asynchronous data in duplex or half-duplex operation. The receiver and transmitter can operate simultaneously. The transmitter accepts parallel binary characters and converts them to a serial asynchronous output. The receiver accepts serial asynchronous binary characters and converts them to a parallel output. The receiver and transmitter clocks are separate and must be 16 times the desired baud rate. The allowable clock rate is dc to 160 kHz.

Control bits are provided to select: character length of 5, 6, 7, or 8 bits (excluding parity), odd or even parity; and one or two stop bits for 6-, 7-, or 8-bit characters. For 5-bit characters, 1 or 1-1/2 start bits are used. The format of a typical input/output serial word is shown in Figure B-1. Both the receiver and transmitter have double character buffering so that at least one complete character is always available. A register is also provided to store control information.

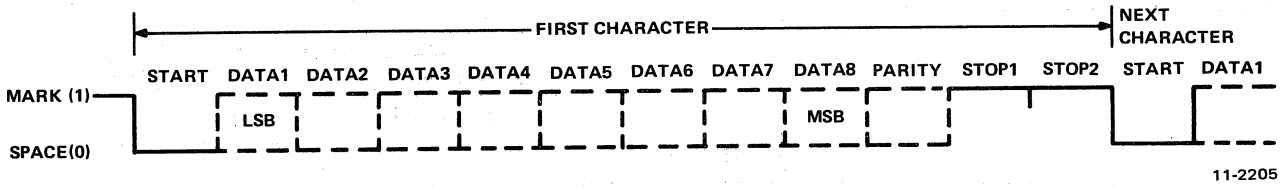
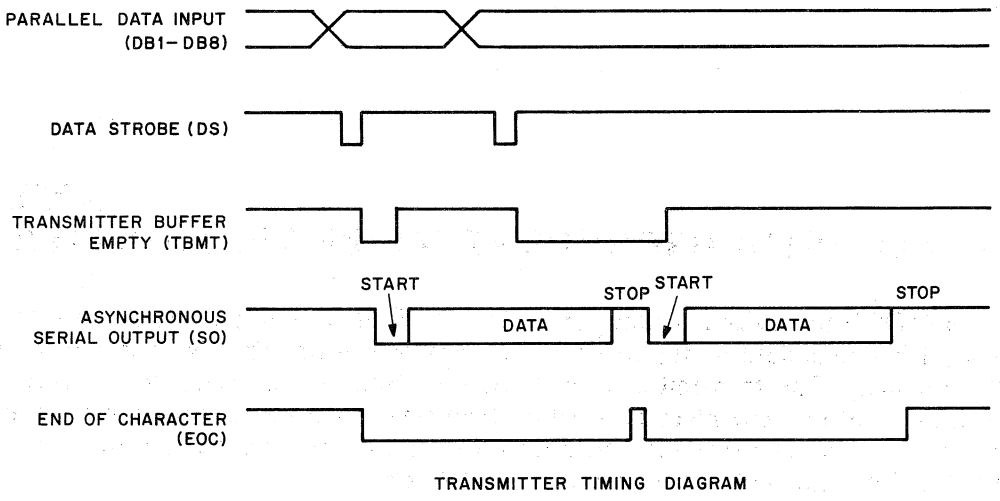


Figure B-1 Format of Typical Input/Output Serial Character

A block diagram and simplified timing diagram for the UART transmitter are shown in Figure B-2. The transmitter data buffer (holding) register can be loaded with a character when the transmitter buffer empty (TBMT) line goes high. Loading is accomplished by generating a short negative pulse on the data strobe (DS) line. The positive-going trailing edge of the DS pulse performs the load operation. The character is automatically transferred to the UART transmitter shift register when this register becomes empty. The desired start, stop, and parity bits are added to the data and transmission begins. One-sixteenth of a bit time before a complete character (including stop bits) has been transmitted, the end-of-character (EOC) line goes high and remains in this state until transmission of a new character begins.

A block diagram and simplified timing diagram for the UART receiver are shown in Figure B-3. Serial asynchronous data is sent to the serial input (SI) line. The UART searches for a high-to-low (mark-to-space) transition on the SI line. If this transition is detected, the receiver looks for the center of the start bit as the first sampling point. If this point is low (space), the signal is assumed to be a valid start bit and sampling continues at the center of the subsequent data and stop bits. The character is assembled bit by bit in the receiver shift register in accordance with the control signals that determine the number of data bits and stop bits and the type of parity, if selected. If parity is selected and does not check, the receiver parity error (PER) line goes high. If the first stop bit is low, the framing error (FER) line goes high. After the stop bit is sampled, the receiver transfers in parallel the contents of the



TRANSMITTER TIMING DIAGRAM

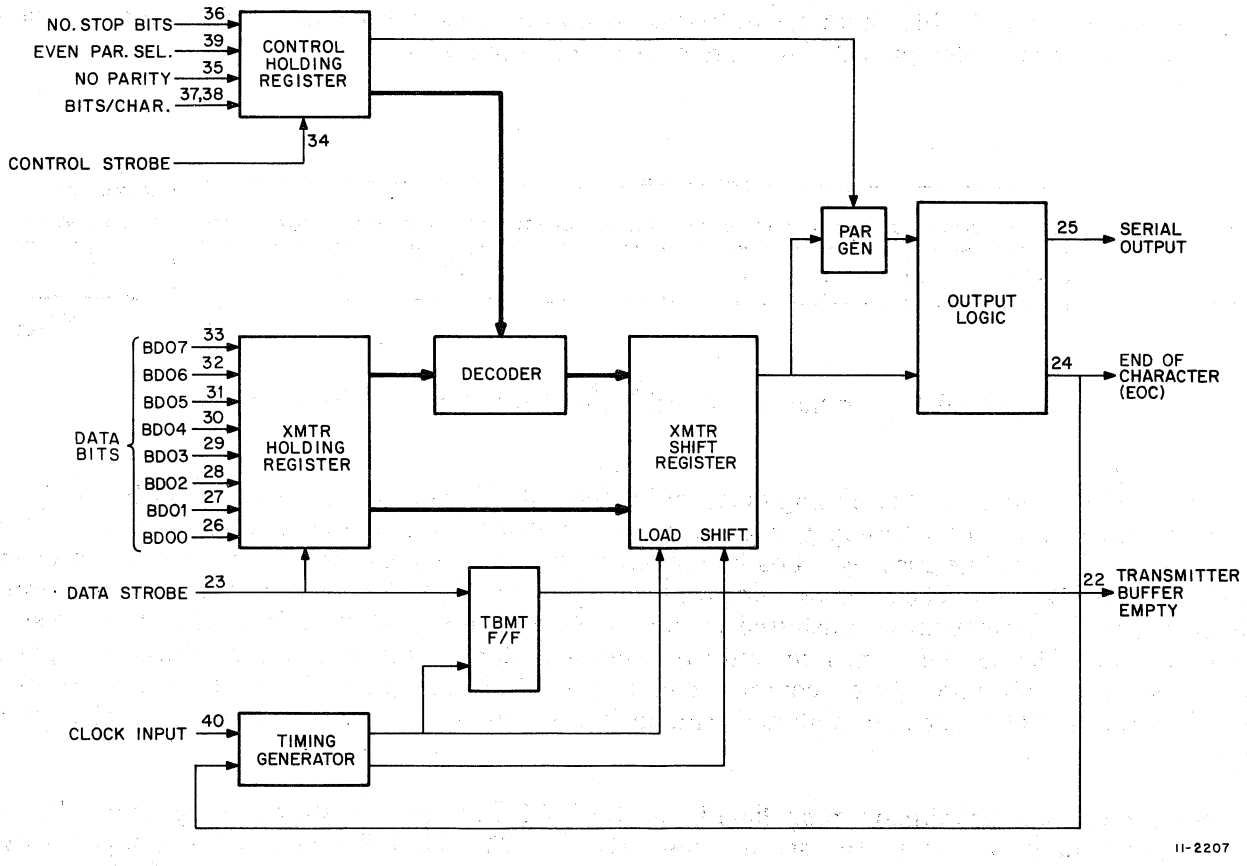
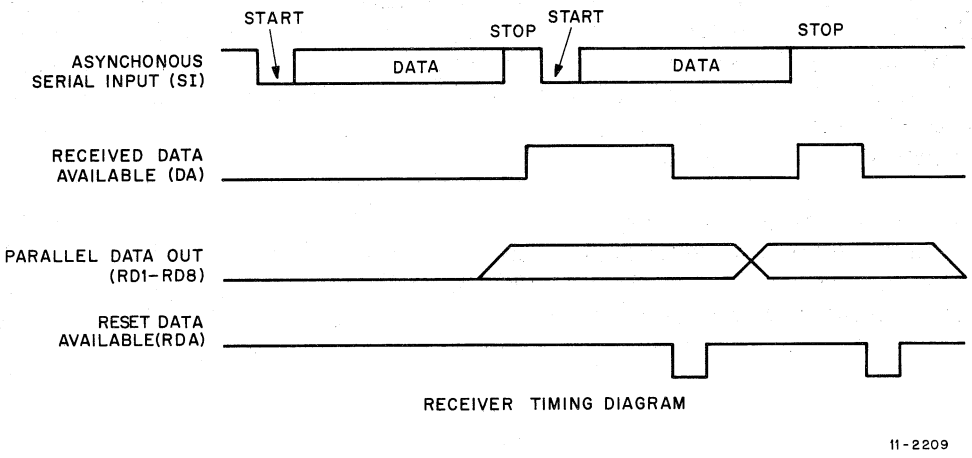


Fig.B-2 UART Transmitter Block Diagram and Simplified Timing Diagram



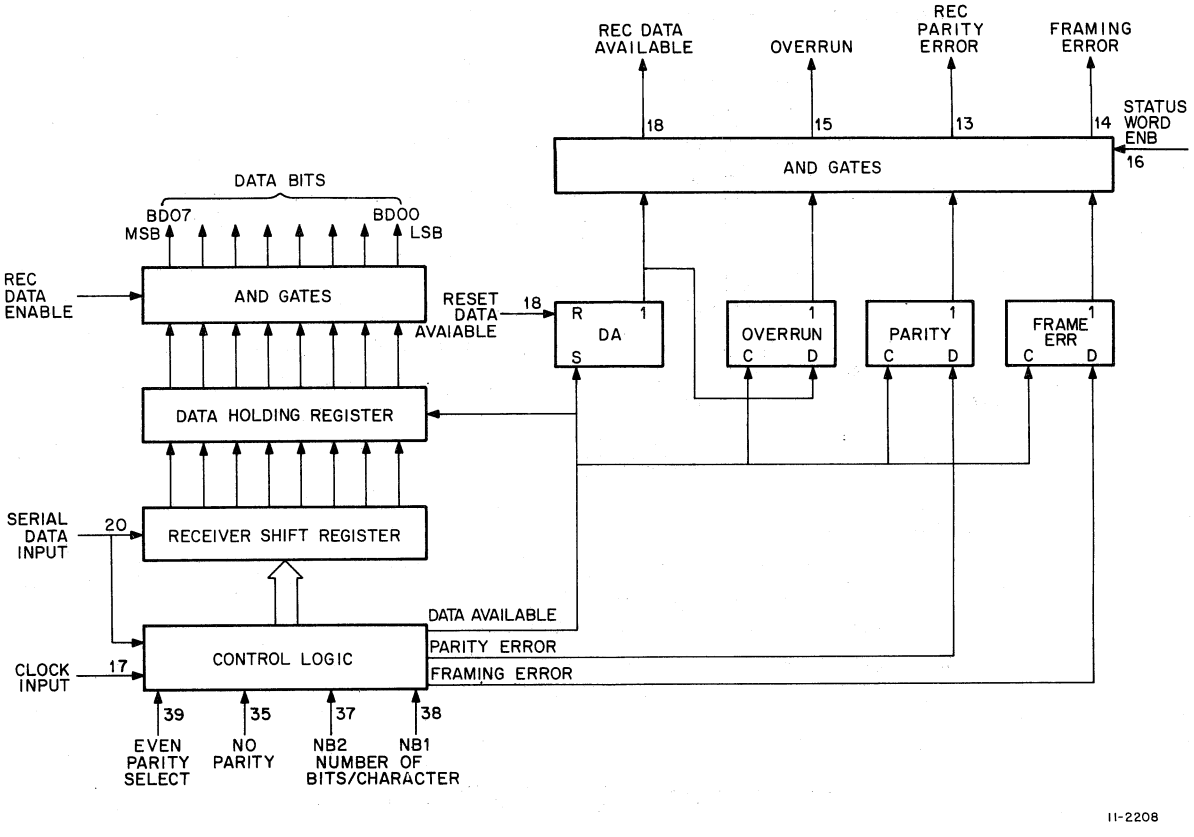


Figure B-3 UART Receiver Block Diagram and Simplified Timing Diagram

receiver shift register into the receiver data buffer (holding) register. The receiver then sets the received data available (DA) line and transfers the state of the framing error and parity error to the status holding register. When the DZ11 accepts the receiver output, it drives the reset data available (RDA) line low, which clears the DA line. If this line is not reset before a new character is transferred to the receiver holding register, the overrun (OR) line goes high and is held there until the next character is loaded into the receiver holding register.

Figure B-4 is a pin/signal designation diagram for the UART. The function of each signal is given in Table B-1. In the Function column, the references to high and low signals are with respect to the pins on the UART. This information is used during servicing of the device. Programmers should refer to the DZ11 register descriptions (Chapter 3) for information concerning the function of these signals.

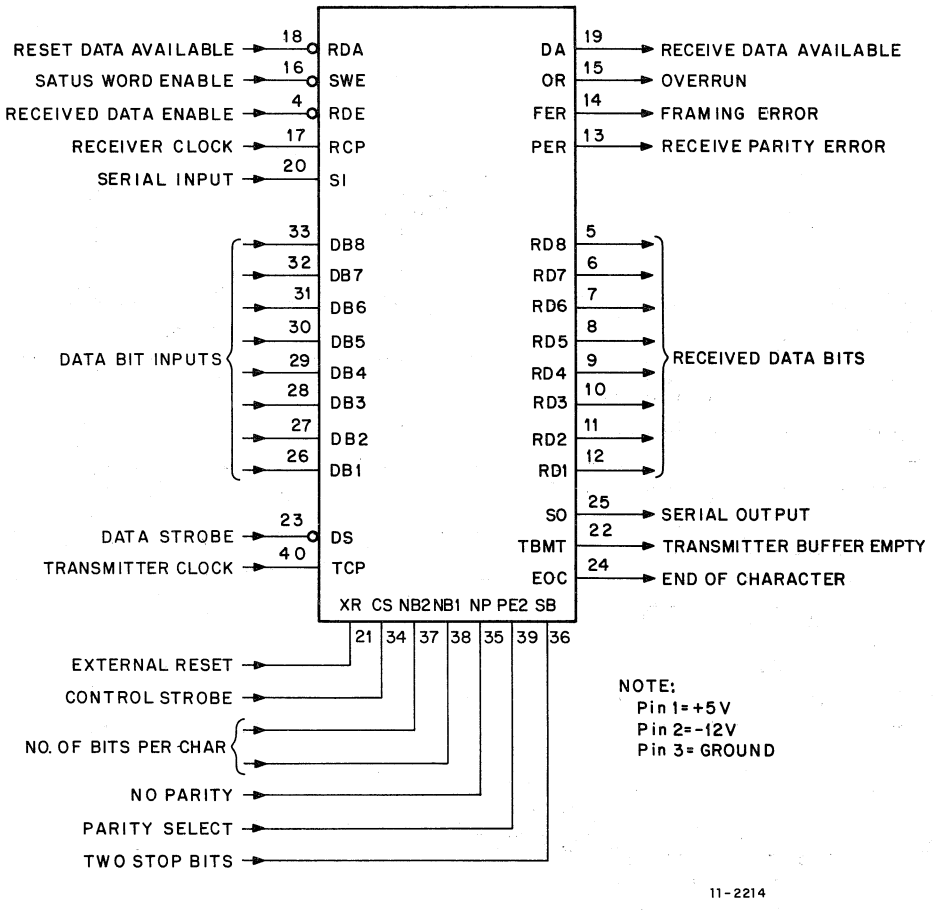


Figure B-4 UART Signal/Pin Designations

Table B-1 UART Signal Functions

Pin No.	Mnemonic	Name	Function
5–12	RD1–RD8	Received Data	Eight data out lines that can be wire ORed. RD8 (pin 5) is the MSB and RD1 (pin 12) is the LSB. When 5-, 6-, or 7-bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PER	Receive Parity Error	Goes high if the received character parity does not agree with the selected parity.
14	FER	Framing Error	Goes high if the received character has no valid stop bit.
15	OR	Overrun	Goes high if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	SWE	Status Word Enable	When low, places the status word bits (PE, OR, TBMT, FE, and DA) on the output lines.
17	RCP	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver baud rate.
18	RDA	Reset Data Available	When low, resets the received data available (DA) line.
19	DA	Received Data Available	Goes high when an entire character has been received and transferred to the receiver holding register.
20	SI	Serial Input	Input for serial asynchronous data.
21	XR	External Reset	After power is turned on, this line should be pulsed high which resets all registers, sets serial output line high, sets end of character line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter data holding register may be loaded with another character

Table B-1 UART Signal Functions (Cont)

Pin No.	Mnemonic	Name	Function
23	DS	Data strobe	Pulsed low to load the data bits into the transmitter data holding register during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Goes high each time a full character, including stop bits, is transmitted. It remains high until transmission of the next character starts. This is defined as the mark (high) to space (low) transition of the start bit. This line remains high when no data is being transmitted. When full speed transmission occurs, this lead goes high for 1/16 bit time at the end of each character.
25	SO	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26–33	DB1–DB8	Data Input	Eight parallel data in lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5-, 6-, or 7-bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	When high, places the control bits (POE, NP, SB, NB1 and NB2) into the control bit holding register.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error (PER) line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the parity bit. A low inserts 1 stop bit and a high inserts 2 stop bits.

Table B-1 UART Signal Functions (Cont)

Pin No.	Mnemonic	Name	Function
37,38	NB2, NB1	Number of Bits per Character (Excluding Parity)	Selects 5, 6, 7, or 8 data bits per character as follows. **Bits Char** / **NB2 (37)** / **NB1 (38)** 5 / L / L 6 / L / H 7 / H / L 8 / H / H
39	POE	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	TCP	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desired transmitter baud rate.

APPENDIX C
DUAL BAUD RATE GENERATOR (COM5016)

The dual baud rate generator/programmable divider (COM5016) is an N-channel MOS/LSI device capable of generating 32 externally selectable frequencies from either an on-chip oscillator or an external input frequency. The unit generates 16 synchronous/asynchronous frequencies as shown in Table C-1. Four address inputs select one of 16 independent receiver or transmitter frequencies (Figure C-1).

The dual baud rate generator is essentially a programmable 15-stage feedback register. An internal reprogrammable ROM permits the generation of the frequency scheme from an internal crystal clock or via an external input frequency. Address inputs may be strobed or dc loaded. Full duplex (independent receive and transmit frequencies) operation is possible with the COM5016.

Utilization of one of the frequency outputs permits generation of additional divisions of the master clock frequency by cascading COM5016s. This may be accomplished by feeding frequency outputs into the XTAL/EXT input on a subsequent device.

The COM5016 may be driven either by an external crystal or TTL logic level inputs. COM5016 pin assignments are shown in Figure C-2; pin functions are described in Table C-2.

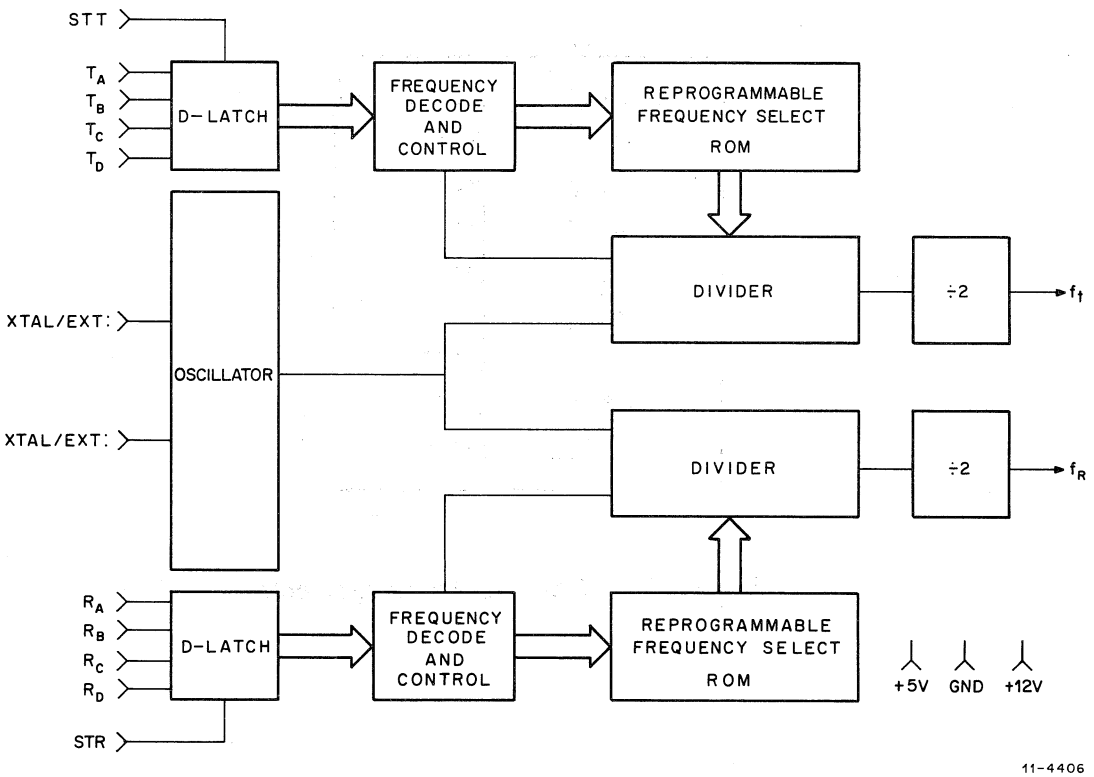


Figure C-1 Dual Baud Rate Generator Block Diagram

Table C-1 Dual Baud Rate Generator Address/Frequency Assignments

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock (kHz)	Actual Frequency 16X Clock (kHz)	Percent Error	Duty Cycle (%)	Divisor
D	C	B	A						
0	0	0	0	50	0.8	0.8		50/50	6336
0	0	0	1	75	1.2	1.2		50/50	4224
0	0	1	0	110	1.76	1.76		50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4		50/50	2112
0	1	0	1	300	4.8	4.8		50/50	1056
0	1	1	0	600	9.6	9.6		50/50	528
0	1	1	1	1200	19.2	19.2		50/50	264
1	0	0	0	1800	28.8	28.8		50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4		50/50	132
1	0	1	1	3600	57.6	57.6		50/50	88
1	1	0	0	4800	76.8	76.8		50/50	66
1	1	0	1	7200	115.2	115.2		50/50	44
1	1	1	0	9600	153.6	153.6		48/52	33
1	1	1	1	19200	307.2	316.8	3.125	50/50	16

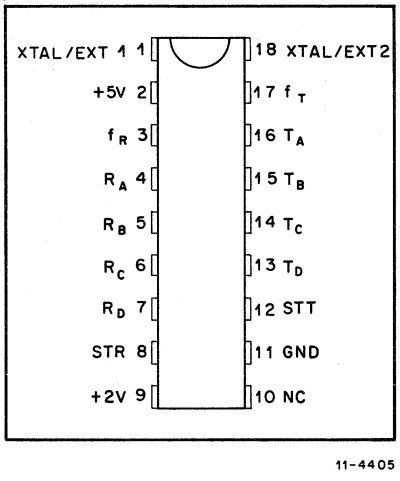


Figure C-2 COM5016 Pin Assignments

Table C-2 Dual Baud Rate Generator Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5V supply
3	f_R	Receiver Output Frequency	This output runs at a frequency as selected by the receiver address
4–7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs, as shown in Table C-1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to a high level.
9	V_{DD}	Power Supply	+12 V supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to a high level.
13–16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table C-1 selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency as selected by the transmitter address.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

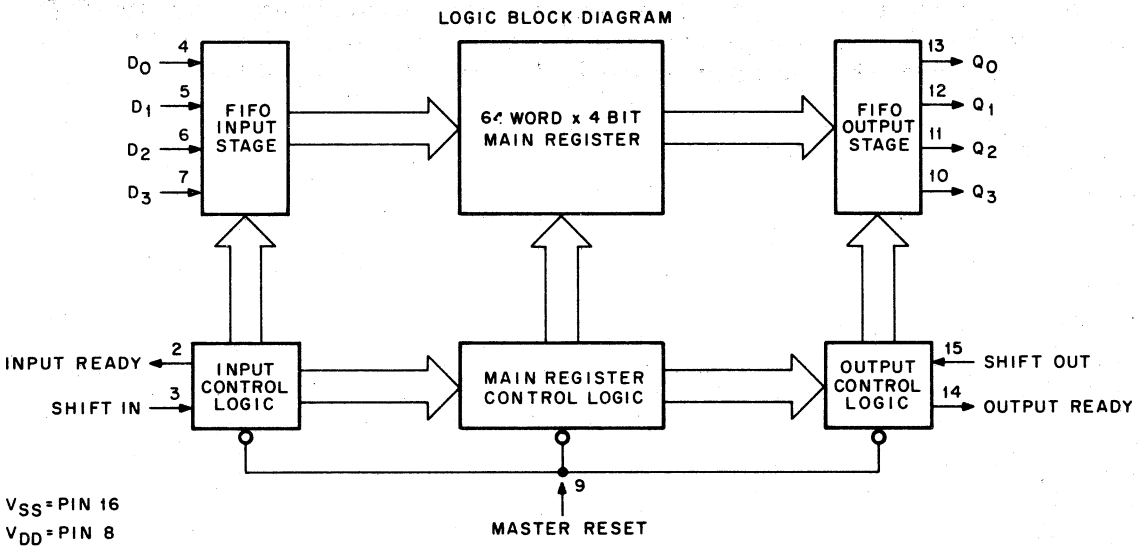
APPENDIX D
INTEGRATED CIRCUITS

The following pages contain reference information for integrated circuits used within the DZ11. Logic diagrams and truth tables (where applicable) are shown. In some cases a pictorial of the chip with pin designations is provided. The integrated circuits in this appendix are listed below:

3341
8136
8641
8647
9318
9602
74LS74
74LS90
74LS138
74LS151
74LS153
74LS155
74LS157
74LS175
74LS193
74LS259

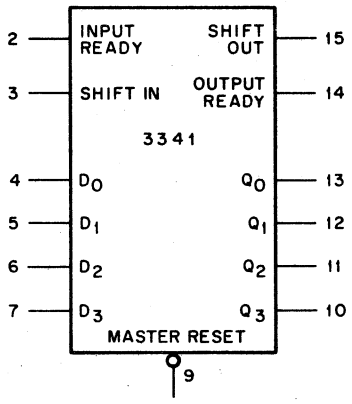
3341 FIFO SERIAL MEMORY

LOGIC BLOCK DIAGRAM



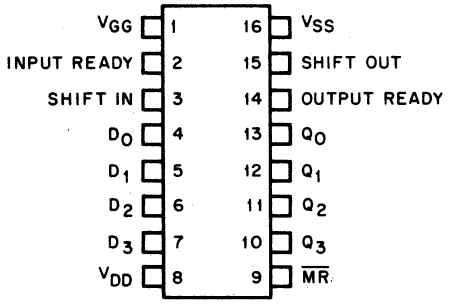
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC SYMBOL



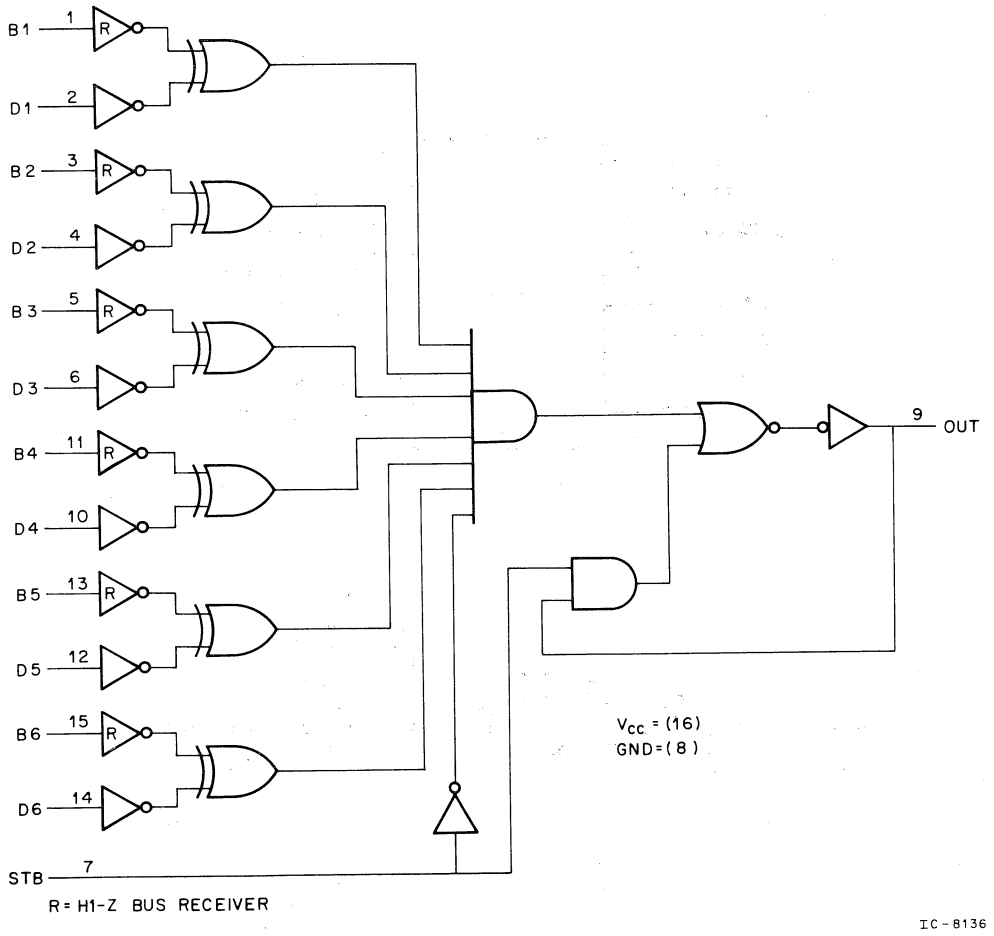
V_{SS} = PIN 16 +5V
V_{DD} = PIN 8 GND
V_{GG} = PIN 1 -12V

PIN CONFIGURATION
(TOP VIEW)



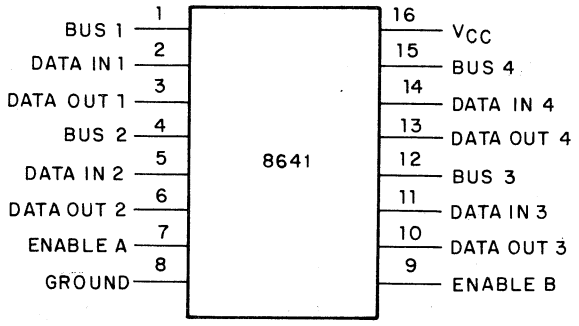
8136 6-BIT, UNIFIED-BUS COMPARATOR

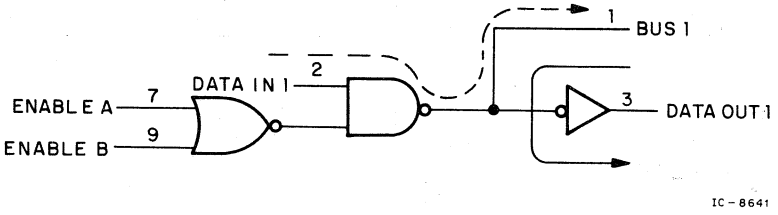
The 8136 compares two binary words (from 2 to 6 bits in length) and indicates matching bit-for-bit of the two words. Inputs for one word are TTL, while those of the second word are high impedance receivers driven by a terminated data bus. The transfer of information to the output occurs as long as the STB input is logic 0. Inputs may be changed while the STB input is at the logic 1 level without affecting the state of the output.



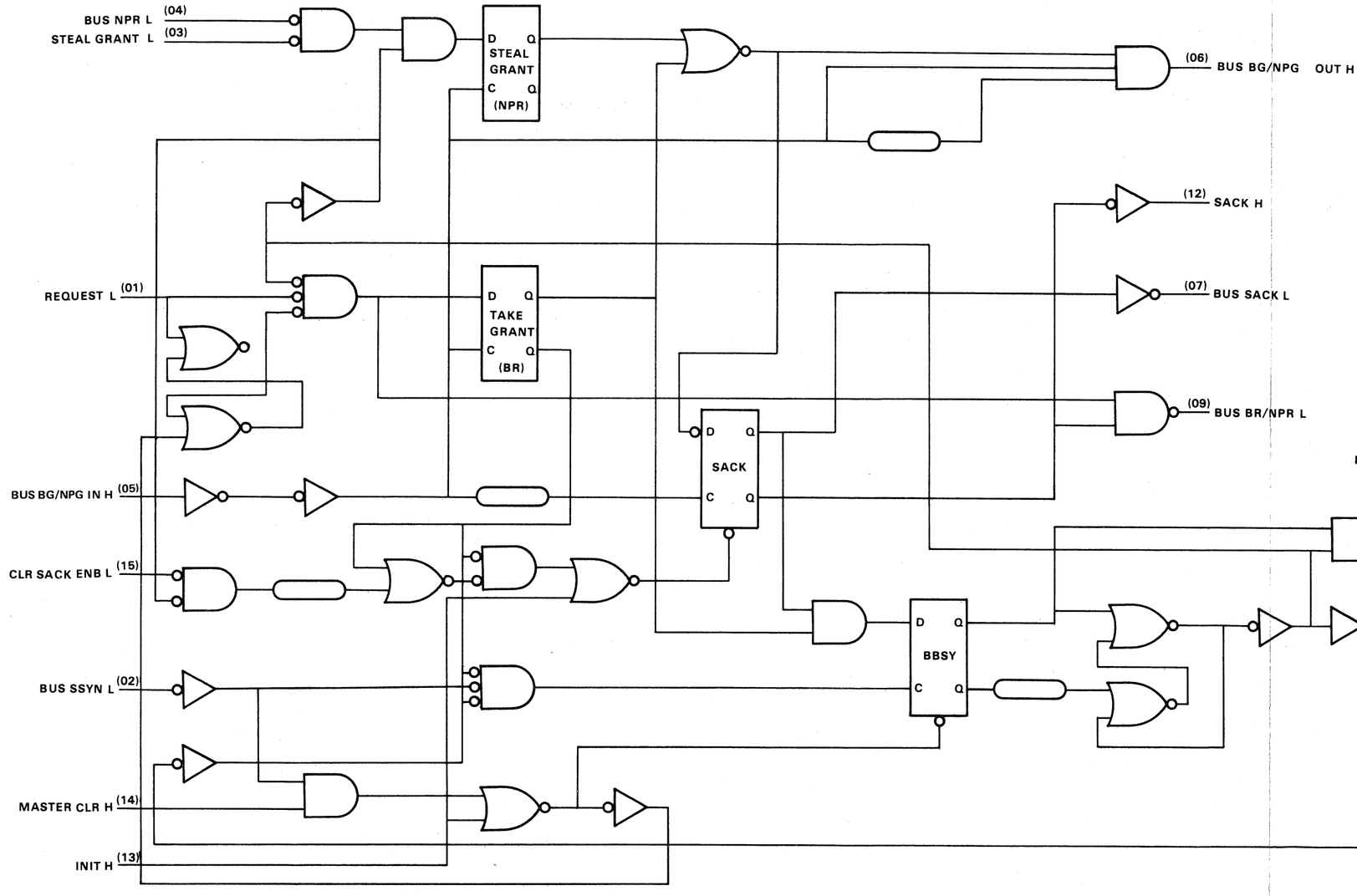
8641 QUAD BUS TRANSCEIVER

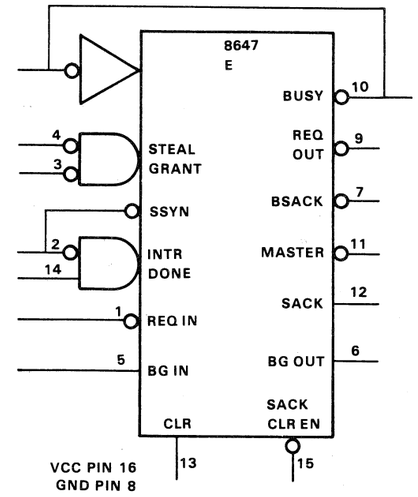
The 8641 consists of four identical receiver/drivers and a single enabling gate in one package for interfacing with the PDP-11 Unibus. The transceiver drivers are enabled when ENABLE A and ENABLE B are both low. The other input of each driver is connected to the data to be sent to the Unibus. For example, when enabled, DATA IN 1 (pin 2) is read to the Unibus via BUS 1 (pin 1). During a write operation, data comes from the Unibus as BUS 1 (pin 1) and is passed through the receiver to the device as DATA OUT 1 (pin 3).



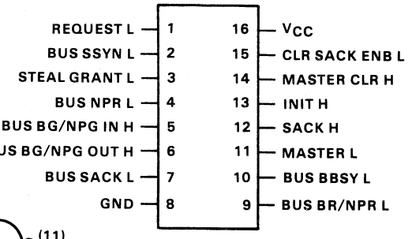


8647 UNIBUS CHIP





PIN CONNECTION DIAGRAM



Pin 8 = GND

Pin 16 = V_{CC}

IC-8647

9318 PRIORITY ENCODER

The 9318 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

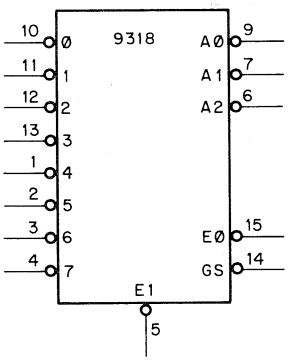
A HIGH on the Input Enable (EI) will force all outputs to the inactive (HIGH) state and allow new data to settle wthout producing erroneous information at the outputs.

A Group Signal output (GS) and an Enable Output (EO) are provided with the three data outputs. The GS is active level LOW when any input is LOW; this indicates when any input is active. The EO is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both EO and GS are inactive HIGH when the input enable is HIGH.

TRUTH TABLE

$\overline{E1}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

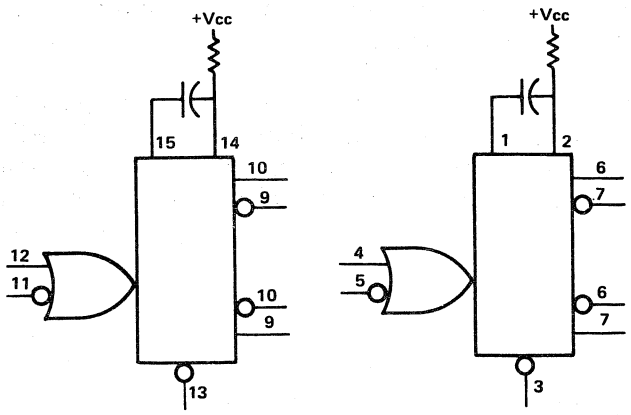
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



GND = PIN Ø8
VCC = PIN 16

IC-9318

9602 MONOSTABLE MULTIVIBRATOR



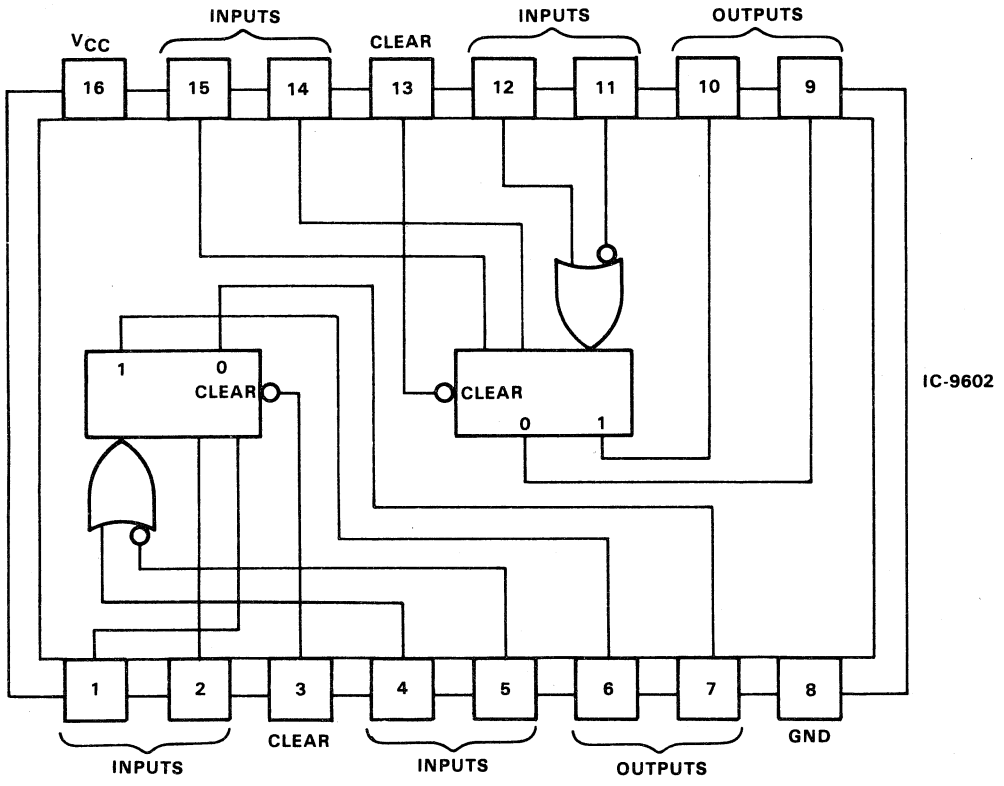
INPUT PIN NO.		OUTPUT PIN NO.	
05/11	04/12	06/10	07/09
H	↑	⊓	⊓
↓	L	⊓	⊓

H=HIGH LEVEL

L=LOW LEVEL

↑=LOW TO HIGH TRANSITION

↓=HIGH TO LOW TRANSITION



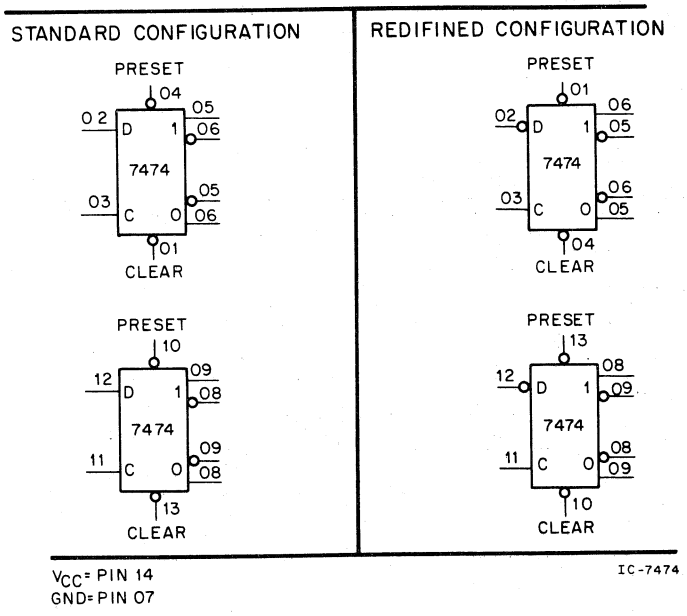
IC-9602

74LS74 DUAL FLIP-FLOP

TRUTH TABLE FOR
7474 STANDARD CONFIGURATION
(EACH FLIP-FLOP)

t_n			t_n+1	
Preset Pin 4(10)	Clear Pin 1(13)	D Input Pin 2(12)	1 Side Pin 5	0 Side Pin 6
High	High	Low	Low	High
High	High	High	High	Low
High	Low	X	Low	High
Low	High	X	High	Low
Low	Low	X	High	High

t_n = bit time before clock pulse.
t_n+1 = bit time after clock pulse.
X = irrelevant



NOTE
IC 7474 is shown. "LS" only signifies low-power Schottky.

74LS90 DECADE COUNTER

The 74LS90 decade counter consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the CLKB0 input must be externally connected to the R0(1) output. The CLK0 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown below.

2. If a symmetrical divide-by-ten count is desired, the R3(1) output must be externally connected to the CLK0 input. The input count is then applied at the CLKB0 input and a divide-by-ten square wave is obtained at output R0(1).

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The CLKB0 input is used to obtain binary divide-by-five operation at the R1(1), R2(1), and R3(1) outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

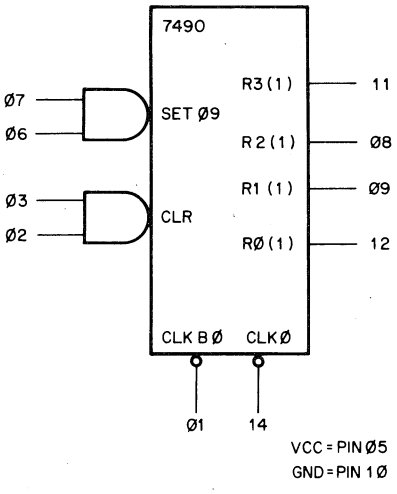
TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT			
	R3(1)	R2(1)	R1(1)	RØ(1)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT			
02	03	06	07	R3(1)	R2(1)	R1(1)	RØ(1)
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

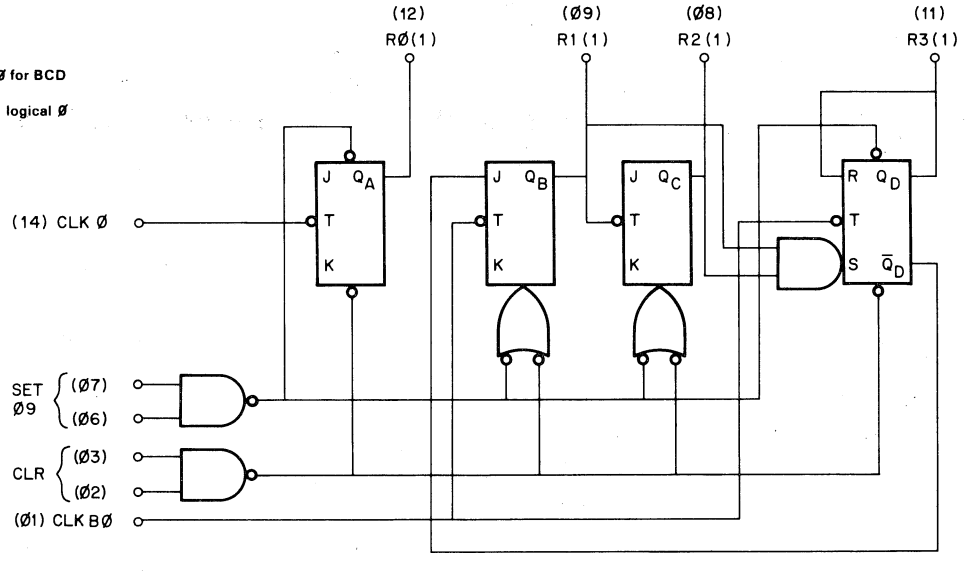


NOTES:

1. Output RØ(1) connected to input CLKBØ for BCD count.
2. X indicates that either a logical 1 or a logical Ø may be present.

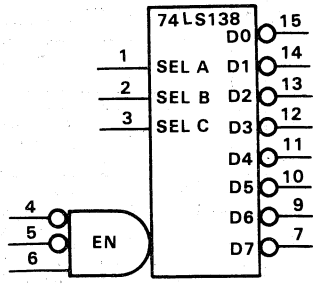
NOTE

IC 7490 is shown. "LS" only signifies low-power Schottky.



IC-7490

74LS138 DECODER/DEMULTIPLEXER

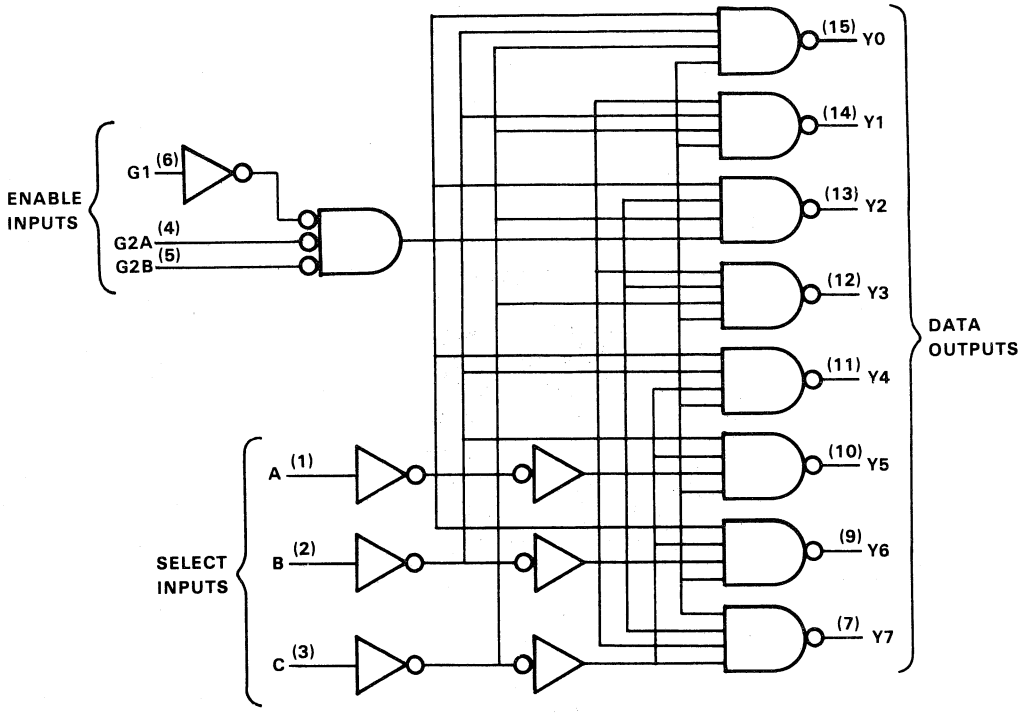


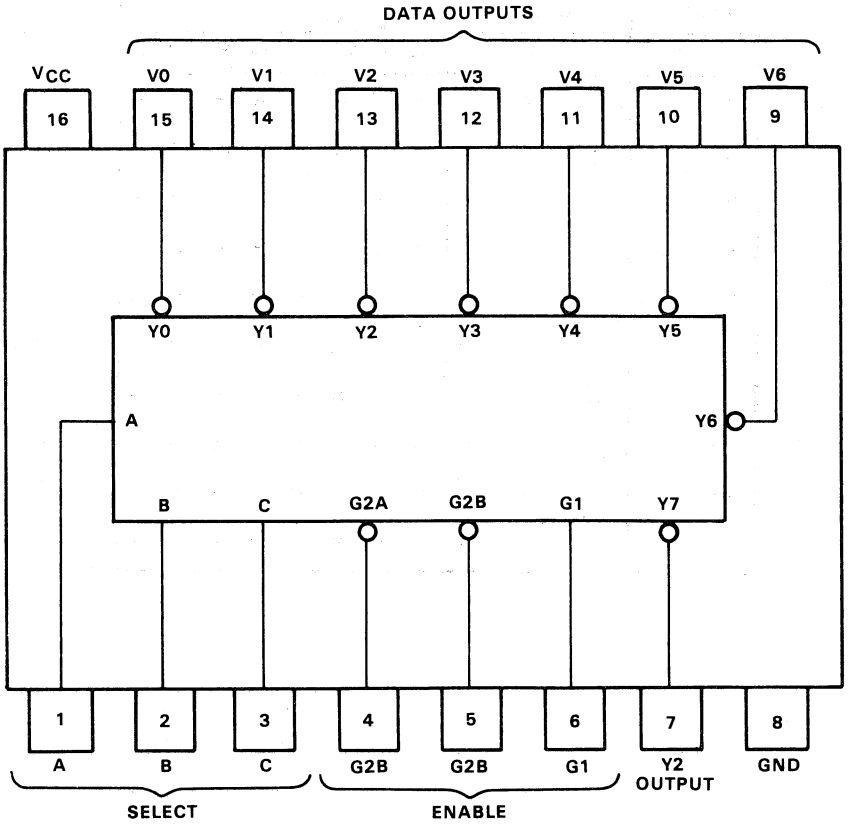
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

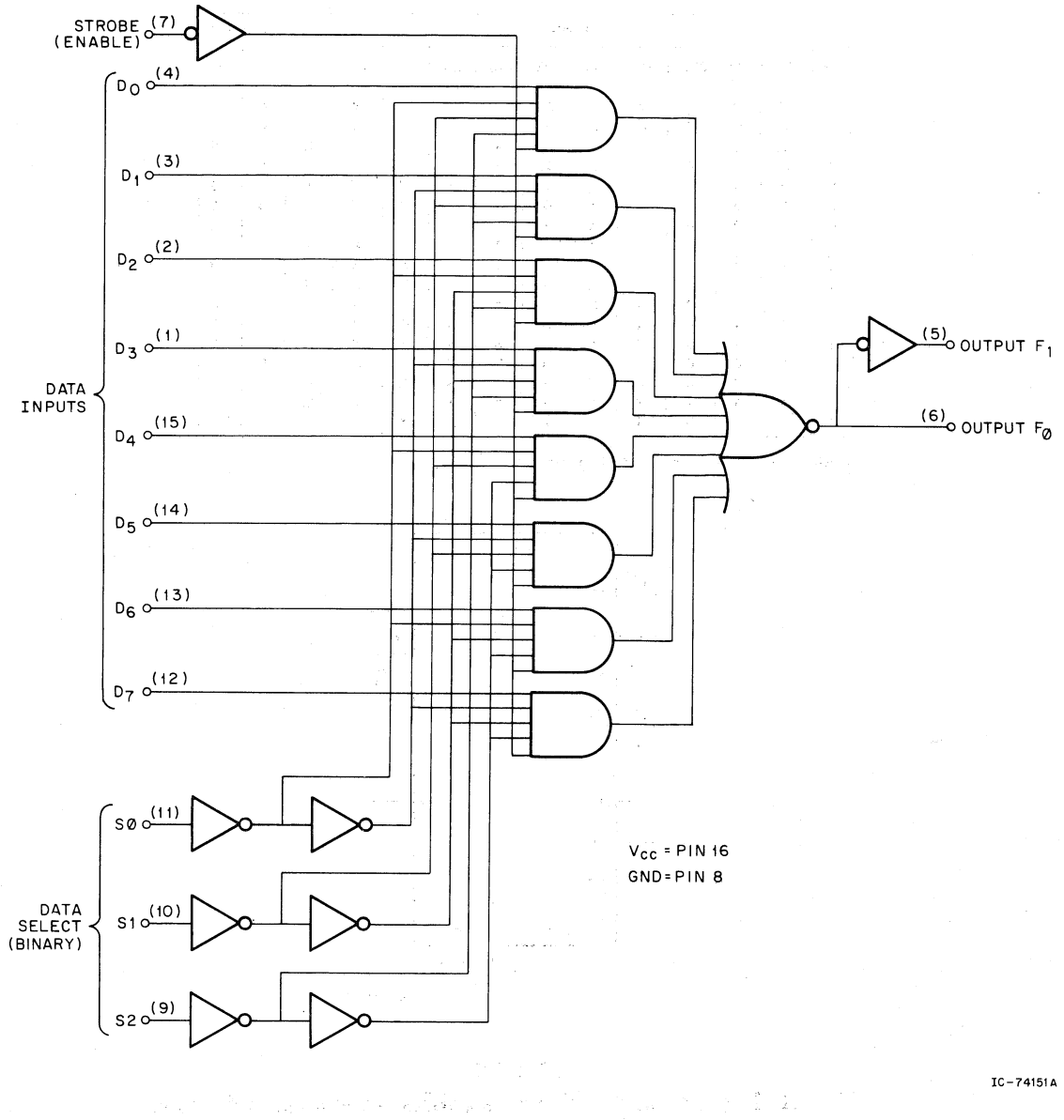
IC-74LS138

74LS138 DECODER/DEMULTIPLEXER (Cont)





74LS151 8-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER

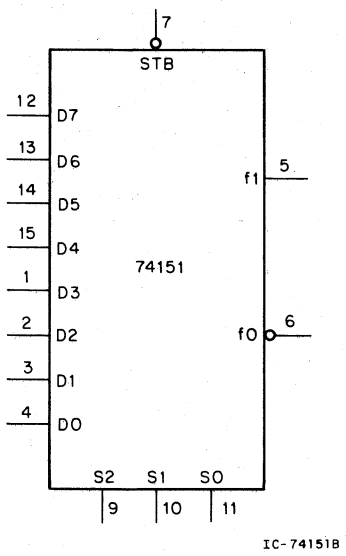


NOTE
IC 74151 is shown. "LS" only signifies low-power Schottky.

74151 TRUTH TABLE

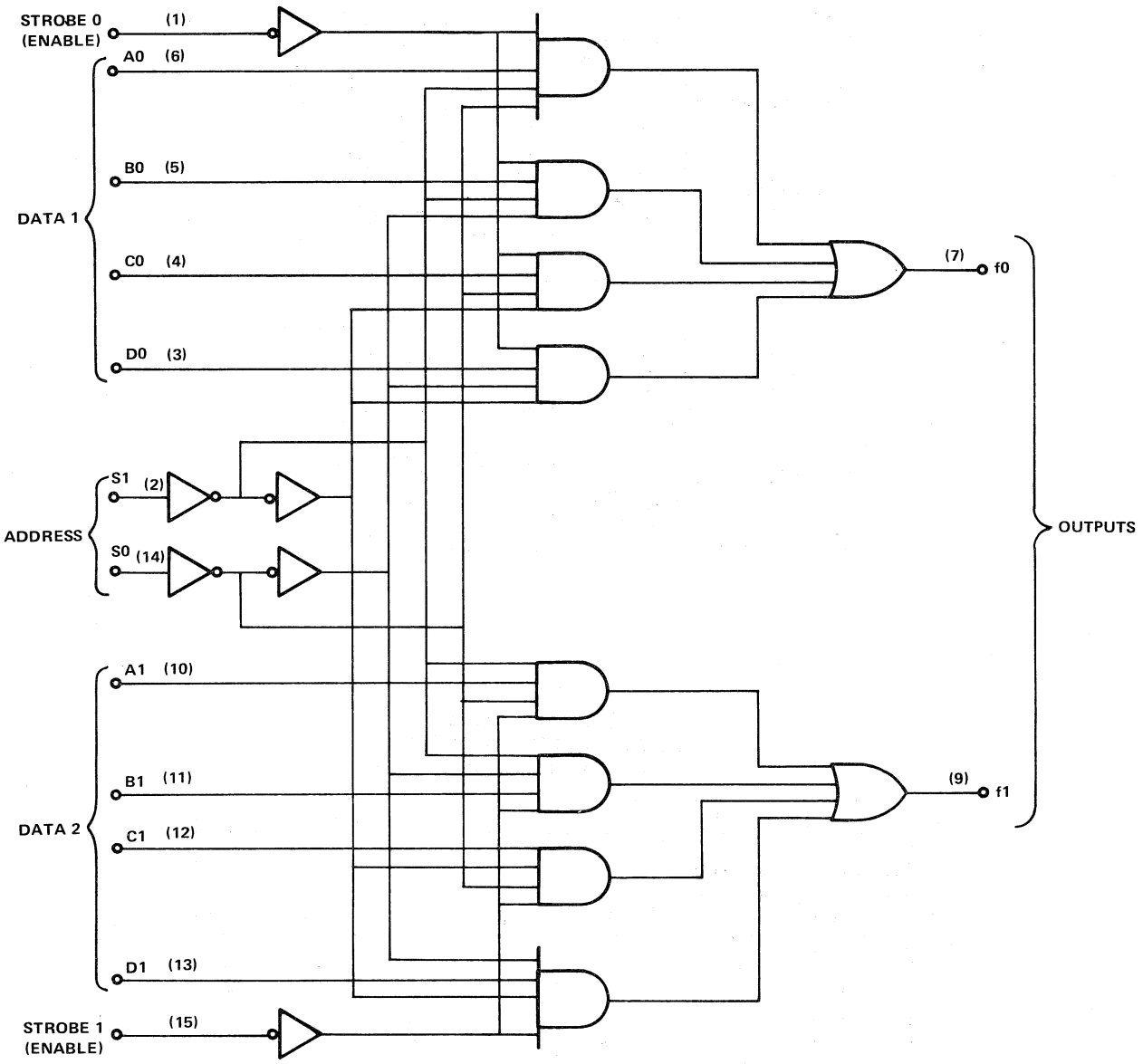
Inputs												Outputs	
S2	S1	S0	STB	D0	D1	D2	D3	D4	D5	D6	D7	f1	f0
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.



NOTE
IC 74151 is shown. "LS" only signifies low-power Schottky.

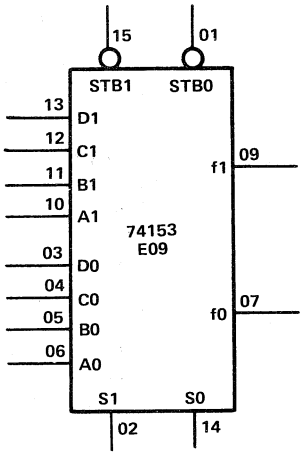
74LS153 DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER



V_{CC} = PIN 16
GND = PIN 08

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
S1	S0	A	B	C	D	STB	f
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

ADDRESS INPUTS S0 AND S1 ARE COMMON TO BOTH SECTIONS : H=HIGH LEVEL, L=LOW LEVEL , X= IRRELEVANT.

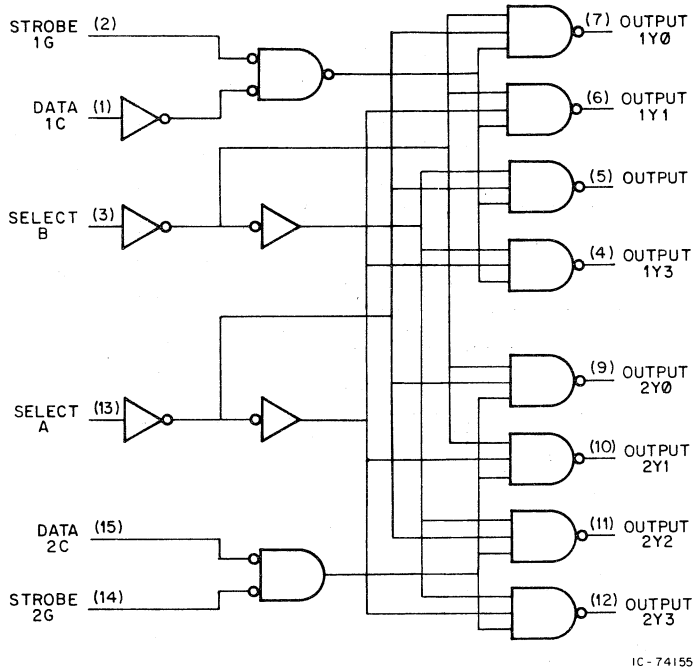


IC-74153

NOTE

IC 74153 is shown. "LS" only signifies low-power Schottky.

74LS155 DUAL 2-LINE-TO-4-LINE DECODER



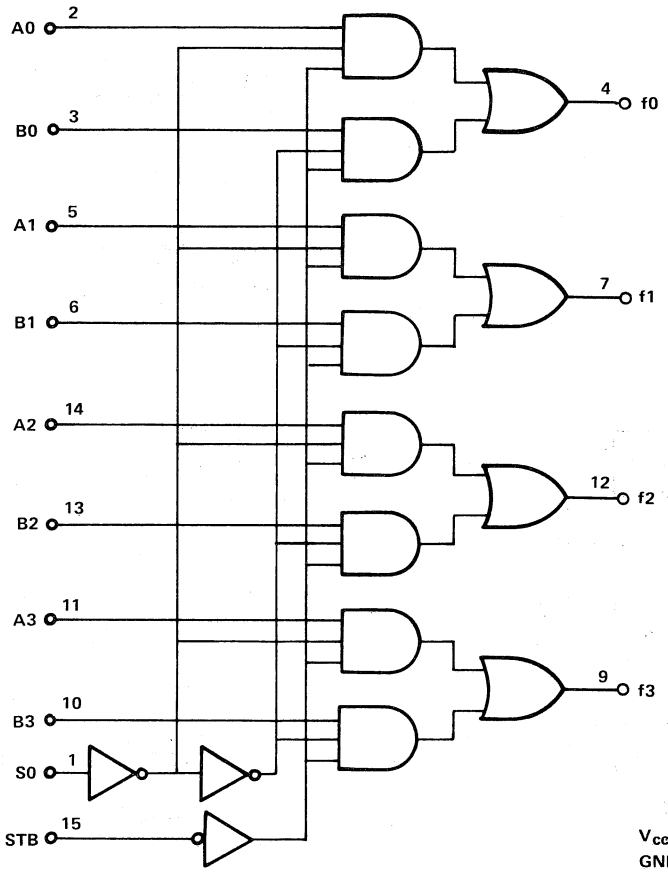
FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

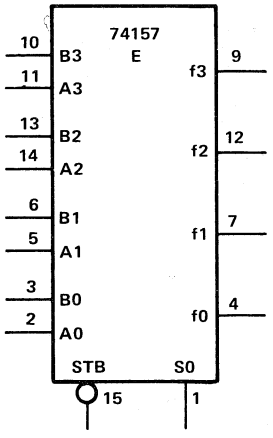
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

NOTE
IC 74155 is shown. "LS" only signifies low-power Schottky.

74LS157 QUADRUPLE 2-LINE-TO-1-LINE MULTIPLEXER





INPUTS			OUTPUT
STROBE	SELECT	A B	
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

IC-74157

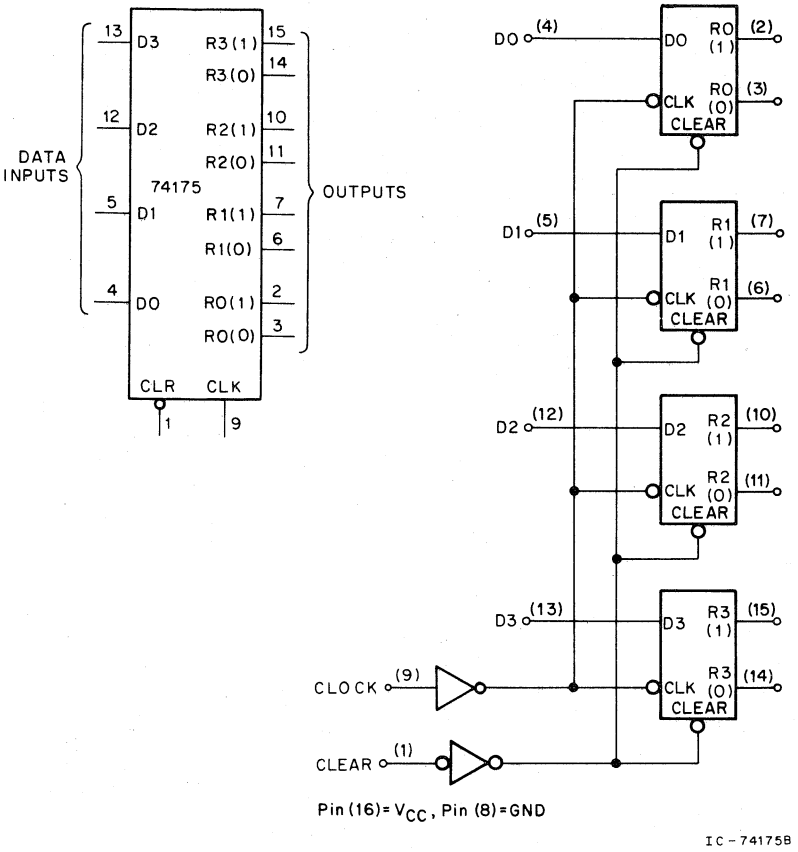
NOTE
IC 74157 is shown. "LS" only signifies low-power Schottky.

74LS175 QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOP

TRUTH TABLE

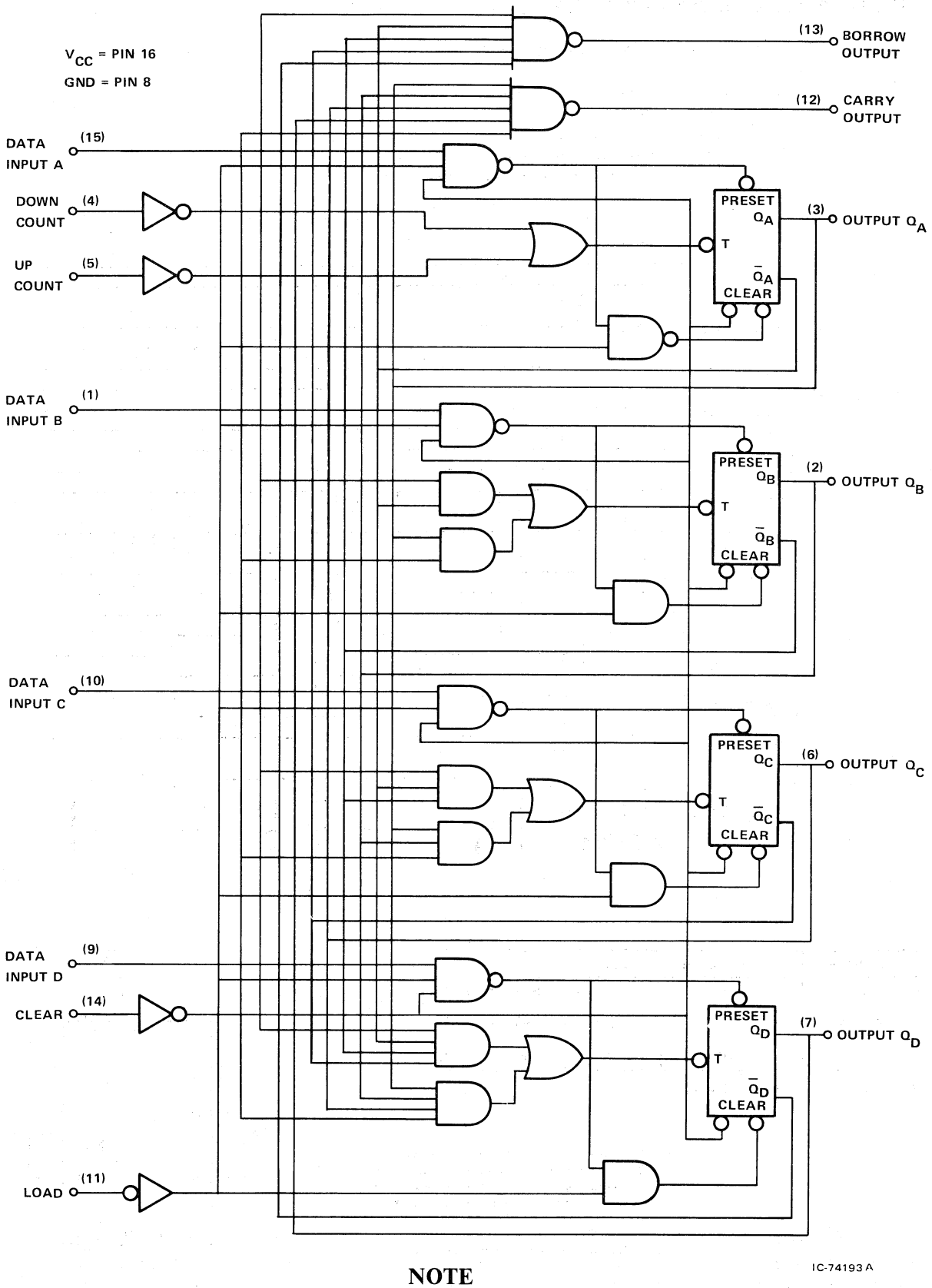
INPUT t_n	OUTPUTS t_{n+1}
D	R(1) R(0)
H	H L
L	L H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



NOTE
IC 74175 is shown. "LS" only signifies low-power Schottky.

74LS193 4-BIT BINARY COUNTER



NOTE

IC 74193 is shown. "LS" only signifies low-power Schottky.

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