Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-8 Family
Maintenance Manual

DF32-D,E

Disk File and Control

FS-59-020 11-18-75

RECOMMENDED SPARES LEVEL

ORIGINAL DATE :11-05-74
REVISION DATE :11-13-75

OPTION : DF32-D
DESCRIPTION : 32K 12 BIT DEC DISK & CONT

DEC PART NO.	DESCRIPTION	VENDOR#	COST PRICE	IN STOCK LEVEL OF SERVICE 98%	95%	90%	80%	70%	50%	C.I.
0G294-00	DISC WRITER		8.87	1						
0G295-00	SERIES SWITCH		11.34	1						
0G296-00	CENTER TAP SELECTOR		12.70	1	1					.01
0M101-00	BUS DATA INTERFACE		5.60	1	1	1				.04
0M103-00	DEVICE SELECTOR		6.68	1						
0M111-00	INVERTER		5.92	1						
0M112-00	NOR GATE		6.38	1	1	1				.04
0M113-00	10-2 INPUT NAND GATE		4.72	1						
0M115-00	INPUT NAND GATE		5.13	1	1	1				.05
0M117-00	INPUT NAND GATE		4.81	1						
0M160-00	EXPANDER		4.71	1						
0M205-00	50 FLIP FLOP		4.26	1	1	1	1	1	1	.12
0M206-00	SIX FLIP FLOPS		6.63	1	1					.01
0M233-00	DISK SHAFT REG.		5.37	1	1	1				.05
0M302-00	ONE SHOT DELAY		16.84	1	1					.05
0M310-00	DELAY LINE		15.48	1						
0M602-00	PULSE GENERATOR		7.28	1	1	1	1			.01
0M617-00	INPUT NAND GATE BUFFER		6.51	1						.08
0M623-00	BUS DRIVER		10.89	1						
0M902-00	RESISTOR TERMINATOR		4.99	1						
0M906-00	CABLE TERMINATOR		9.43	1						
G0850-00	DISC READ AMP & SLICE		26.30	1	1	1	1			.15
10-05767-00	10 MFD 330V 10%/DO NOT USE IN NEW DESI		4.78	1						
12-01434-00	RLY,G.P.,115V COIL,DPDT, 2A,OCTAL		8.45	1						
12-05358-00	DISK-10 INCH NICKEL COBALT		322.40	1	1	1	1	1		.55
30-05359-00	HEAD, FLYING 4 TRACK		42.67	1	1	1	1	1	1	.96
70-05315-01	MOTOR+HUB 60CY DF32		95.98	1	1	1	1			.36
70-05315-02	MOTOR+HUB 50CY DF32		97.03	1						.04
74-06308-00	DATA HEAD HARNESS		50.09	1						.01
		TOTAL COST		812.24	557.54	521.37	498.89	369.33	46.93	

MISCELLANEOUS PARTS AND SPECIAL TOOLS

10-02938-00	.01 MFD 600V 10% 663UW M -M	(10	.21
11-00113-00	D 662 OS 600PCB(STABISTOR)		.05
13-00496-00	15 K 1/4W 5% CC	(13-00	.02
15-02979-00	DEC3638a PNP 300MW SI 25 P		.12
15-03100-00	DEC3009B NPN 200MW SI 20 25 P		.11
19-05576-00	DEC 7410 NAND GATE-TRIPLE 3IN		.14

DEC-00-DF32-D/E

PDP-8 FAMILY
DF32-D,E DISK FILE AND CONTROL MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing August 1970
2nd Printing August 1971
3rd Printing July 1972

Copyright © 1970, 1971, 1972 by Digital Equipment Corporation

The material in this manual is for information purposes and is subject to change without notice.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	PDP
FLIP CHIP	FOCAL
DIGITAL	COMPUTER LAB

CONTENTS

		Page
CHAPTER 1	INTRODUCTION	
1.1	Scope	1-1
1.2	Equipment Application	1-2
1.3	DF32-D,E Description	1-2
1.3.1	Disk Assembly	1-5
1.3.2	Logic Module Assembly	1-6
1.4	DS32-D,E Description	1-6
CHAPTER 2	INSTALLATION	
2.1	Cabinet Installation	2-1
2.2	Power Requirements	2-1
2.3	Cable Requirements	2-2
CHAPTER 3	OPERATION AND PROGRAMMING	
3.1	Operation	3-1
3.2	Programming	3-3
CHAPTER 4	THEORY OF OPERATION	
4.1	General	4-1
4.1.1	Write Operation	4-5
4.1.2	Read Operation	4-5
4.2	Disk	4-9
4.2.1	Disk Format	4-9
4.2.2	Disk Timing	4-12
4.2.3	Disk Recording Technique	4-14
4.3	Logic Circuits	4-14
4.3.1	Logic Timing	4-14
4.3.2	Search Operation	4-17
4.3.3	Write Operation	4-21
4.3.4	Read Operation	4-23
4.3.5	Data Track Selection and Lock-Out Switches	4-26
4.3.6	Disk Expander Operation	4-31
4.3.7	Error Flags	4-31

CONTENTS (Cont)

		Page
CHAPTER 5	MAINTENANCE	
5.1	General	5-1
5.2	Procedure for Cleaning the Disk and Heads	5-1
5.2.1	Preliminary Action	5-1
5.2.2	Disk Removal and Cleaning	5-1
5.2.3	Head Cleaning	5-2
5.2.4	Disk Replacement	5-2
5.2.5	Final Check	5-4
5.3	Adjustments	5-5
5.4	Troubleshooting	5-9
5.5	Module List	5-11
CHAPTER 6	ENGINEERING DRAWINGS	6-1
APPENDIX A	TIMING TRACK WRITER	
A.1	Introduction	A-1
A.2	Operation	A-1
A.3	Operating Switches	A-2
A.4	Theory of Operation	A-2
A.4.1	General	A-2
A.4.2	Detailed Logic Discussion	A-4
A.5	Adjustment Procedure	A-11

ILLUSTRATIONS

Figure No.	Title	Art No.	Page
1-1	Disk and Logic Module Assembly	5077-2	1-3
1-2	Disk Assembly with Top Dust Cover Removed	3490-3	1-5
1-3	Disk Assembly with Disk Removed and Recording Heads Exposed	3490-1	1-6
2-1	DF32-D/DS32-D Mounting Locations	08-0578	2-2
3-1	DF32-D Front Panel	5022-3	3-2

ILLUSTRATIONS (Cont)

Figure No.	Title	Art No.	Page
3-2	DS32-D Front Panel	5151-2	3-2
3-3	IOT Instructions	08-0539	3-3
3-4	Programming Example		3-8
4-1	DF32-D Block Diagram, Write and Read Operations	08-0538	4-4
4-2	Flow Diagram	08-0544	4-7
4-3	Disk Track Order	08-0541	4-9
4-4	Disk Format	08-0540	4-10
4-5	Search/Transfer Operation Timing	08-0545	4-11
4-6	Disk Track Timing	08-0548	4-13
4-7	Basic Timing Signals	08-0525	4-15
4-8	Basic Timing Logic	08-0546	4-16
4-9	GAP Timing	08-0533	4-17
4-10	Address Search, Simplified Logic Block Diagram	08-0547	4-18
4-11	DMA Incrementation and Timing	08-0532	4-20
4-12	Write Operation Simplified Logic - Block Diagram	08-0535	4-22
4-13	Read Operation Simplified Logic - Block Diagram	08-0534	4-24
4-14	DB Loading of Data Word - Timing Diagram	08-0526	4-25
4-15	Read/Write Termination	08-0523	4-27
4-16	Last Word/Last Disk Timing Diagram	08-0524	4-28
4-17	Unit Select Circuit	08-0536	4-29
4-18	Lock-Out Select	08-0537	4-30
5-1	Disk Removal	3490-2	5-3
5-2	Head Cleaning	3490-4	5-4
5-3	Output Signal at Pin AT (CT)	08-0518	5-7
5-4	Output Signal at Pin BD (DD)	08-0519	5-7
5-5	Slice Level Obtained by Combining Outputs from Pins (CT) AT and (DD) BD	08-0520	5-7
5-6	TTA and TTB Pulse	08-0521	5-8
5-7	TTAD Pulse and Associated Data Pulse	08-0522	5-8

ILLUSTRATIONS (Cont)

Figure No.	Title	Art No.	Page
A-1	DF32-D-15 Timing Track Writer	5391-1	
A-2	TTW Block Diagram	08-0555	A-3
A-3	Timing Diagram	08-0529	A-5
A-4	Address Word Incrementation	08-0528	A-8
A-5	Address Increment	08-0543	A-9
A-6	Last TTB Generation	08-0531	A-9
A-7	Alternate Address Logic	08-0542	A-10
A-8	Timing Write Cycle (Test)	08-0527	A-11
A-9	LA-LB Relationship	08-0530	A-12
A-10	Timing Track Writer		A-13

ENGINEERING DRAWINGS

Drawing No.	Title	Page
D-BS-DF32-DP-04	Interface (3 sheets)	6-3
D-BS-DF32-DN-04	Interface (3 sheets)	6-9
D-BS-DF32-DP-05	Disk Control (3 sheets)	6-15
D-BS-DF32-DP-02	Disk Memory and Address Search (2 sheets)	6-21
D-BS-DF32-DP-03	Data Logic and Head Matrix (3 sheets)	6-25
D-MU-DF32-DP-06	Module Utilization	6-31
D-MU-DF32-DN-06	Module Utilization	6-33
D-BS-DS32-D-03	Disk Expander (2 sheets)	6-35
D-MU-DS32-D-02	Module Utilization	6-39
C-CS-G085-0-1	Disk Read Amplifier and Slice Rectifier	6-41
B-CS-G294-0-1	Disk Writer	6-42
B-CS-G295-0-1	Series Switch	6-42
B-CS-G296-0-1	Center Tap Selector	6-43
B-CS-M233-0-1	Disk Shift Register	6-43

TABLES

Table Number	Title	Page
1-1	Reference Publications	1-1
1-2	Operating and Maintenance Programs	1-1
1-3	DF32-D,E Subsystem Specifications	1-3
2-1	Cable Requirements	2-3
2-2	DF32-D/Computer Cable Connections	2-3
2-3	DF/DS32-D Cable Connections	2-4
3-1	DF32-D Operating Control Functions	3-1
3-2	DS32-D Operating Control Functions	3-3
3-3	DF32-D Instructions	3-4
3-4	IOT Instructions	3-5
4-1	DF32-D/DS32-D Signal Mnemonics	4-1
5-1	Module List	5-12
A-1	TTW Operating Switches	A-2

Chapter 1
Introduction

1.1 SCOPE

This manual describes the DF32-D,E Disk File and Control Unit and the DS32-D,E Disk Extender Unit. The information is intended primarily for maintenance personnel familiar with the DEC PDP-8 family of computers. Table 1-1 lists supplementary publications and Table 1-2 lists operating and maintenance programs available for use with the disk file system.

Table 1-1
Reference Publications

Title	Description
Logic Handbook	Function and specifications of FLIP CHIP® modules, cabinets, power supplies and accessories.
PDP-8 Maintenance Manual	Theory, operation and maintenance information on the PDP-8.
PDP-8/I Maintenance Manual	Theory, operation and maintenance information on the PDP-8/I.
PDP-8/L Maintenance Manual	Theory, operation and maintenance information on the PDP-8/L.
Small Computer Handbook	Operation and programming of PDP-8/L and PDP-8/I computers and peripheral equipment.

Table 1-2
Operating and Maintenance Programs

Program	Description
DF32-D Software Package	Perforated program tapes, symbolic assembly, assembly language, and utility subroutines.
DF32-D Diskless Logic Tests (Maintenance) MAINDEC-8I-D5FA	Tests master logic without the disk in operation.

Table 1-2 (Cont)
Operating and Maintenance Programs

Program	Description
DF32/DF32-D Disk Data Mini Disk, Interface Address, Data Test MAINDEC-08-D5CD	Tests master logic with the disk in operation.
DF32/DF32-D Multi Disk Exerciser MAINDEC -08-D5DB	Tests master disk and up to three slave disks.

1.2 EQUIPMENT APPLICATION

The DF32-D,E subsystem is comprised of the DF32-D,E Disk File and Control and as many as three DS32-D,E Disk Extenders. This subsystem is part of a major system built around either a PDP-8, PDP-8/I, or PDP-8/L computer. The subsystem expands the memory capacity of the particular computer by providing a quickly-accessed storage facility. The subsystem stores information transferred from the computer memory and returns this information on command. The DF32-D,E and each DS32-D,E store up to 32,768 13-bit words. The subsystem can thus expand the computer memory by as many as 131,072 words.

1.3 DF32-D,E DESCRIPTION

The DF32-D,E Disk File and Control Unit can be used with either 60- or 50-Hz primary power, and with either a positive or negative computer bus. Thus, four distinct units are available. The complete nomenclature of a particular unit is one of the following:

DF32-DP ..... 115V, 60 Hz, positive bus
DF32-DN..... 115V, 60 Hz, negative bus
DF32-EP ..... 115V, 50 Hz, positive bus
DF32-EN ..... 115V, 50 Hz, negative bus

NOTE

All of the above can be used in 230V systems. A multi-tap transformer (DEC P/N 16-2283) can be provided for this purpose.

For convenience, the nomenclature DF32-D will be cited, except where basic differences must be noted.

The DF32-D is a random access, bulk storage device that uses a magnetic recording process to record information on an aluminum disk. The unit consists of two assemblies: the disk assembly and the

logic module assembly (see Figure 1-1). The disk assembly is mounted on shock-absorbing columns at the rear of the frame. The logic modules are inserted in mounting connectors at the front. The wiring side of the connectors faces the front of the unit. The frame is equipped with track slides for easy access and can be installed in any 19-in. equipment rack. The frame is 10-1/2 in. high, 19 in. wide, and 23-1/4 in. deep from the mounting surface, with a 2-3/8 in. extension in front of the mounting surface. (Refer to Table 1-3 for subsystem specifications.)

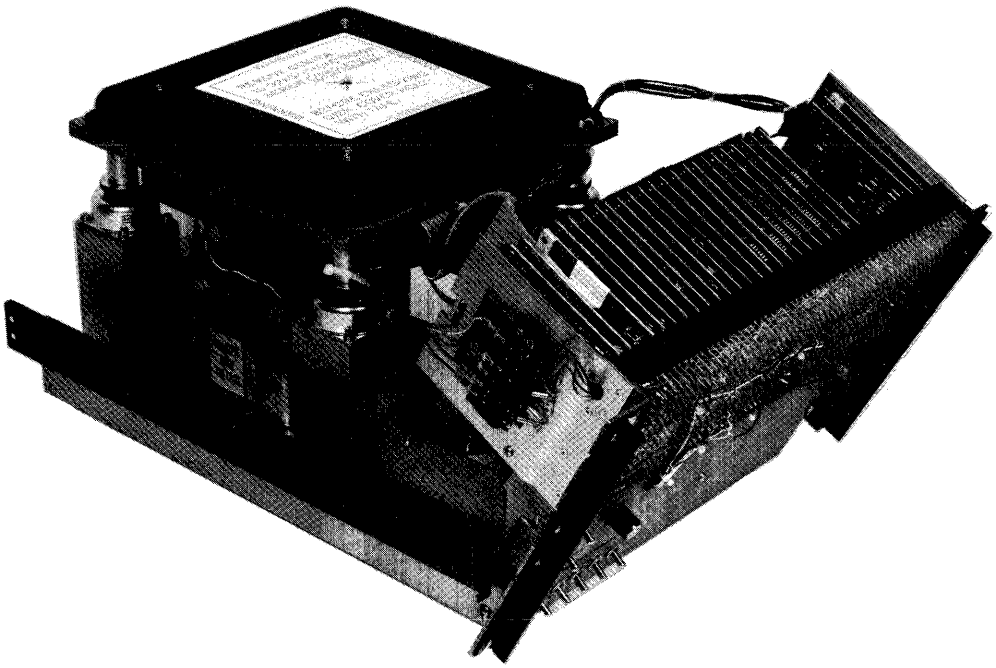


Figure 1-1 Disk and Logic Module Assembly

Table 1-3
DF32-D,E Subsystem Specifications

Storage Capacity	DF32-D,E: 32,768 13-bit words DS32-D,E: 32,768 13-bit words Three DS32-D,E extender disks may be used with each DF32-D,E master unit, resulting in a system capacity of 131,072 13-bit words.
Data Transfer Rate	DF32-D: 32 μs/word DF32-E: 39 μs/word
Access Time Average	DF32-D: 16.67 ms DF32-E: 20.00 ms
Maximum	DF32-D: 33 ms DF32-E: 40 ms

Table 1-3 (Cont)
DF32-D,E Subsystem Specifications

Bit-to-Bit Transfer Rate	DF32-D: 1.10 μs serial DF32-E: 1.33 μs serial
Addressing Scheme	Random or absolute addressing from 0 to 32,768 words; variable block size: from 1 to 4096 words.
Data Assembly	Internal read/write, serial; external transfer, parallel, 12 bits per word
Recording Medium	Nickel-cobalt, rhodium plated surface of a 10-in. diameter aluminum disk
Recording Method	Non-Return to Zero Inhibit (NRZI)
Number of Disk Data Tracks	16
Data Words per Track	2048
Bit Density	1170 BPI, maximum
Number of Disk Timing Tracks	Two, plus spare for each: all prerecorded
Tracks per Inch	30
Track Width	0.020
Special Features	Write inhibit of lower/upper 16K of any 32K disk surface: inhibit of one or more 32K disks of an expanded configuration
Number of Recording Heads	20, in groups (pads) of four
Power Requirements	
ac	DF32-D: 115V, 60 Hz, single phase DF32-E: 115V, 50 Hz, single phase
dc	DF32-D,E +20V, 300 mA +10V, 65 mA +5V, 3.6 mA -15V, 702 mA DS32-D,E +20V, 300 mA +10V, 35 mA +5V, 677 mA -15V, 377 mA NOTE +20V, +10V: requirements for one DF32-D,E and three DS32-D,E provided by one DEC type 705B or H709/H709B Power Supply +5V, -15V: one H716 required for DF32-D,E and one H716 required for the three DS32-D,E
Recommended Environment	70 to 80°F, 20 to 80% relative humidity

Table 1-3 (Cont)
DF32-D,E Subsystem Specifications

Physical Characteristics	
Height	10-1/2 in.
Width	19 in.
Depth	21-1/4 in. from mounting surfaces; 2-3/8 in. extension in front of mounting surface
Weight	65 lb, approximate

1.3.1 Disk Assembly

The disk assembly includes a 10-in. diameter aluminum disk, 20 recording heads, and a drive motor mounted on a base plate, supported by four shock-absorbing columns. Top and bottom dust covers protect the disk and heads. Electrical signals are sent through two connector cards that plug into the logic module assembly. Figure 1-2 is the disk assembly with the top dust cover removed. Figure 1-3 is the assembly with the disk removed and recording heads exposed. Note that there are four heads on each head shoe.

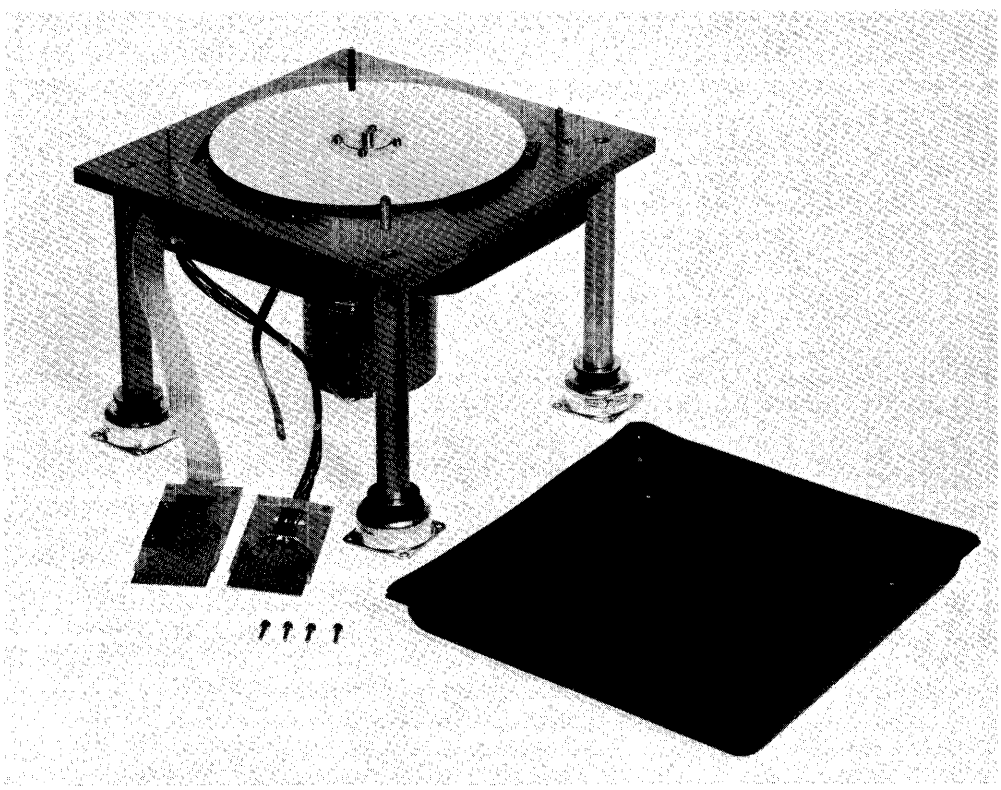


Figure 1-2 Disk Assembly with Top Dust Cover Removed

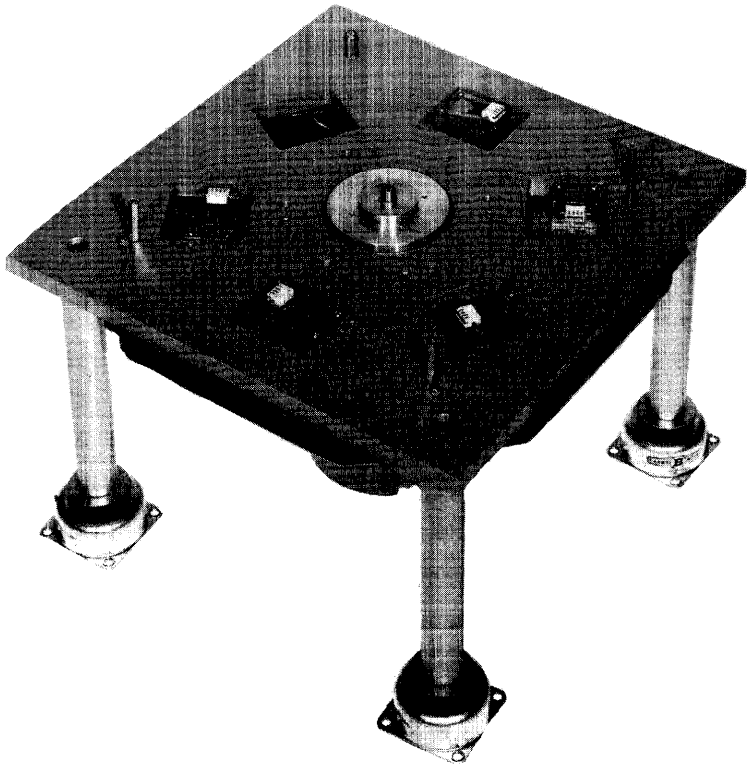


Figure 1-3 Disk Assembly with Disk Removed and Recording Heads Exposed

1.3.2 Logic Module Assembly

The logic module assembly includes the logic modules, the module mounting panels, controls, and switches. The logic for the DF32-D is contained on DEC logic modules, which are inserted in the mounting connectors. Connections between the modules are made by wiring the connector pins. The modules consist of G-series (discrete components) and M-series (integrated circuit) modules. The majority of these modules are the M-series, which use high speed TTL integrated circuits to implement the logic. Table 5-1 lists the DEC modules in the DF32-D. Drawing DF32-DP-06 (Section 6) shows the location of each module in the connector blocks, and the identity of the signals furnished by each module.

1.4 DS32-D,E DESCRIPTION

The disk extender (as well as the master controller) can be used with either 60- or 50-Hz power, and with either a positive or negative bus. The following extender units are available:

DS32-D.....115V, 60 Hz, positive and negative bus
DS32-E.....115V, 50 Hz, positive and negative bus

For convenience, the short nomenclature, DS32-D, will be used.

The DS32-D is similar to the DF32-D in appearance and in overall dimensions. The disk assembly is identical to that of the DF32-D; however, the logic module assembly is significantly different. The logic module assembly contains fewer logic modules because the DS32-D operation is controlled by the DF32-D control circuits. A completely extended DF32-D subsystem consists of one DF32-D Disk File and Control, three DS32-D Disk Extenders, a DEC Type 705B or H709/H709B Power Supply, two DEC Type H716 Power Supplies, and a power control panel.

Chapter 2
Installation

2.1 CABINET INSTALLATION

The DF32-D subsystem will normally be an addition to a system built around a PDP-8, PDP-8/I, or PDP-8/L computer. This computer will be either pedestal or rack mounted. If other peripheral equipment is rack mounted in a DEC standard computer cabinet, it may be possible to incorporate the DF32-D subsystem into the existing mounting configuration. Refer to the appropriate computer maintenance manual for a discussion of mounting arrangements in the DEC cabinet.

Additional cabinet space may be required if the DF32-D subsystem includes disk extenders. In this event, the DF32-D should be mounted at the top with the extender disks mounted below. Cables must be kept as short as possible; therefore, all extender units should be mounted in the same cabinet as the DF32-D. Although any 19-in. equipment rack can be used, a DEC standard computer cabinet is suggested for convenience and appearance. Various panel doors and cover plates can be purchased along with the basic 19-in. frame. A typical system is shown in Figure 2-1. Refer to the Logic Handbook for a guide to available cabinet hardware.

If the DF32-D is to be installed in a cabinet of an existing system in the field, it may be necessary to install the cabinet portion of the track slide assembly. Two types of track slides are used, depending upon the type of DEC cabinet in which the equipment is being mounted. DEC Type CAB8 Cabinets use Chassis Track Slides (C300-S-20), while the new DEC H960 and H961 Cabinets use Slides 12-91-54. When the cabinet location of the equipment has been selected, the track slide housing should be mounted with four No. 10-32 Rivinuts.

2.2 POWER REQUIREMENTS

The DF32-D/E requires a 115V ac, single-phase power source. The DF32-D is designed for 60-Hz operation; the DF32-E is designed for 50-Hz operation. AC connections are made directly to the dc power supplies listed in Table 1-3. DC power connections to the logic modules are made at a power end panel located on the left side of either DF32-D or DS32-D.

NOTE

The disk motor should not be turned on and off any more than is absolutely necessary. There is contact between the disk and the heads when the disk is stopped. Excessive starting and stopping creates excessive wear on both disk and heads. The disk motor ac power should, therefore, be supplied directly from a power source and not from the power control switch.

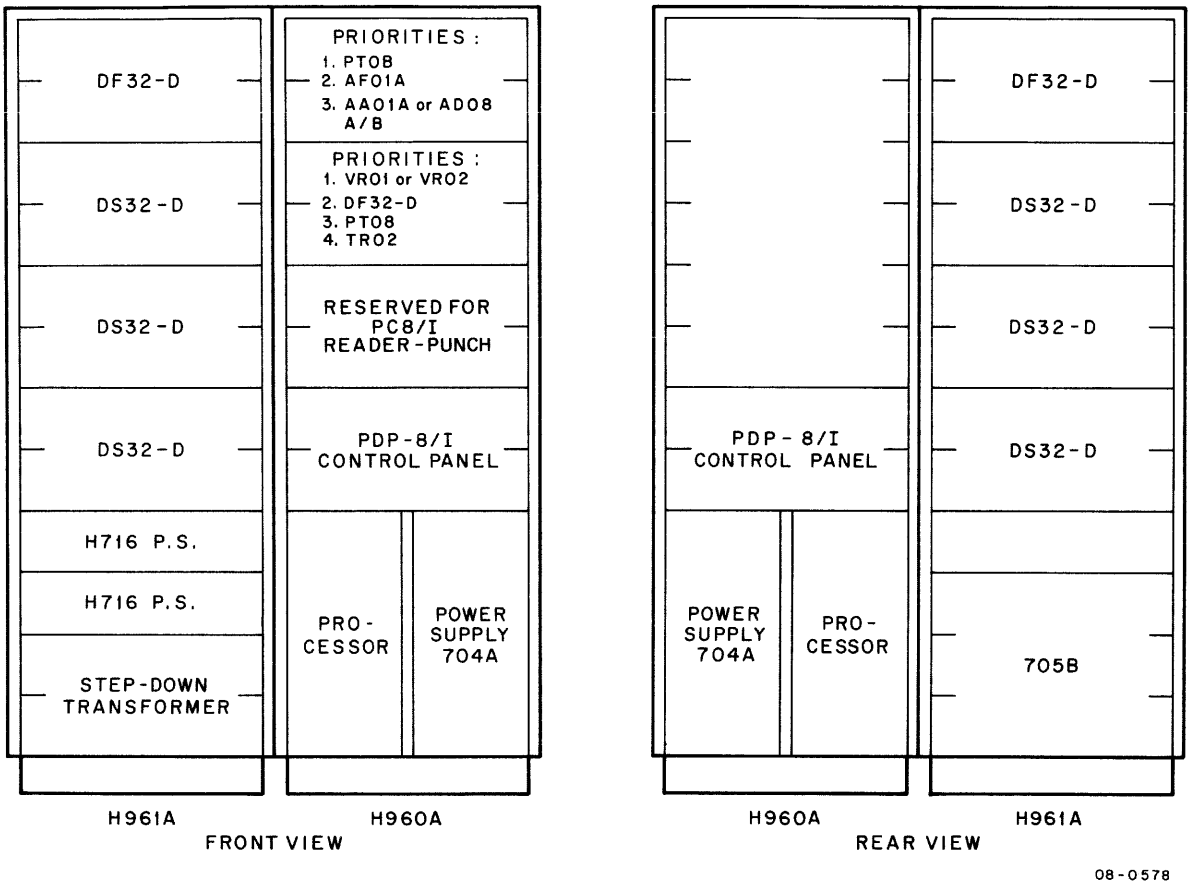


Figure 2-1 DF32-D/DS32-D Mounting Locations

2.3 CABLE REQUIREMENTS

Connections between the computer and the DF32-D are made by shielded mylar interfacing cable, terminated on either end by single- or double-sided connector boards. Cable requirements are shown in Table 2-1 for each combination of DF32-D and computer.

Table 2-1
Cable Requirements

Computer	Type of DEC Standard Interface Cable Needed	Number of Cables Needed	Cable Components
PDP-8	BC08C-5	5	5 ft. 1-1/4 in. mylar M903 to 2 W031
		1	5 ft. 1-1/4 in. mylar W021 to W021
PDP-8/I	BC08C-5	5	5 ft. 1-1/4 in. mylar M903 to 2 W031
PDP-8/L	BC08A-5	5	5 ft. 1-1/4 in. mylar M903 to M903

Table 2-2 gives cable connections between the DF32-D and associated computer.

Table 2-2
DF32-D/Computer Cable Connections

DF32-D Receptacle Connector	Computer Receptacle Connector		
	PDP-8 (W031)	PDP-8/I (W031)	PDP-8/L (M903)
A25 (M903)	ME-34 MF-34	J01 J02	D36
A26 (M903)	ME-35 MF-35	J03 J04	D35
A27 (M903)	PE-02 PF-02	J05 J06	D34
A28 (M903)	PE-03 PF-03	J07 J08	C36
A29 (M903)	PE-04 PF-04	J09 J10	C35
B02 (W031)	ME-30	J11 (Negative bus only)	

Connections between the DF32-D and DS32-D are also made by standard DEC interfacing cable. Table 2-3 gives cable requirements and cable connections for DF/DS32-D combinations.

Table 2-3
DF/DS32-D Cable Connections

Cable	Number Required	From	To
BC03D-5	1	DF32-D, B03 (W021 Connector)	DS32-D, C10 (W021 Connector)
BC08A-5	1	DF32-D, A03 (M903 Connector)	DS32-D, D09 (M903 Connector)

Chapter 3
Operation and Programming

3.1 OPERATION

No special operating procedures are required for the DF32-D or the DS32-D. The DF32-D front panel is shown in Figure 3-1; the DS32-D front panel is shown in Figure 3-2. The DF32-D operating controls are described in Tables 3-1 and 3-2.

Table 3-1
DF32-D Operating Control Functions

Control	Function
UNIT SELECT	Assigns disk selection number.
UPPER 16K	When in the ON position, inhibits writing on the upper 16K word positions of the DF32-D if write lockout is enabled.
LOWER 16K	When in the ON position, inhibits writing on the lower 16K word positions of the DF32-D if write lockout is enabled.
OPR/MAINT	Normally in the OPR position; when in the MAINT position, enables maintenance IOT instructions (for diskless diagnostic test).
DISK 0 WRITE LOCKOUT	When in the ON position, enables write lockout selection on unit 0.
DISK 1 WRITE LOCKOUT	When in the ON position, enables write lockout selection on unit 1.
DISK 2 WRITE LOCKOUT	When in the ON position, enables write lockout selection on unit 2.
DISK 3 WRITE LOCKOUT	When in the ON position, enables write lockout selection on unit 3.

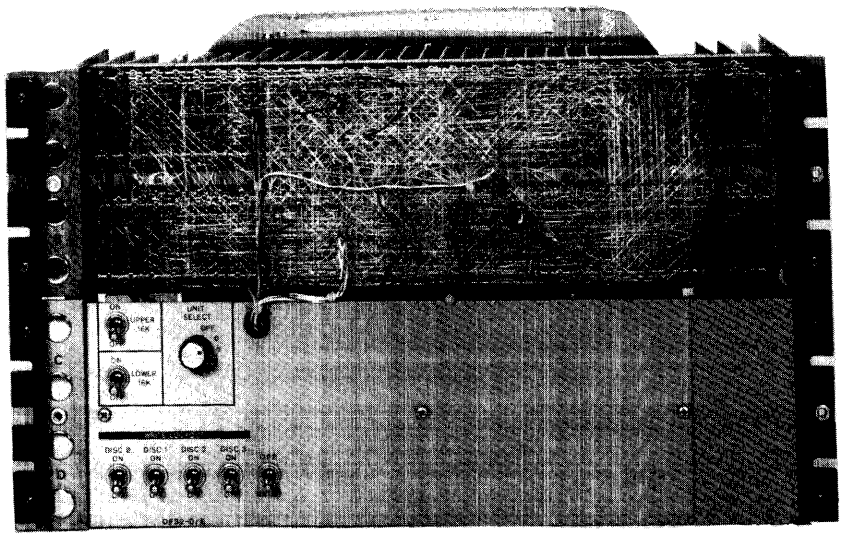


Figure 3-1 DF32-D Front Panel

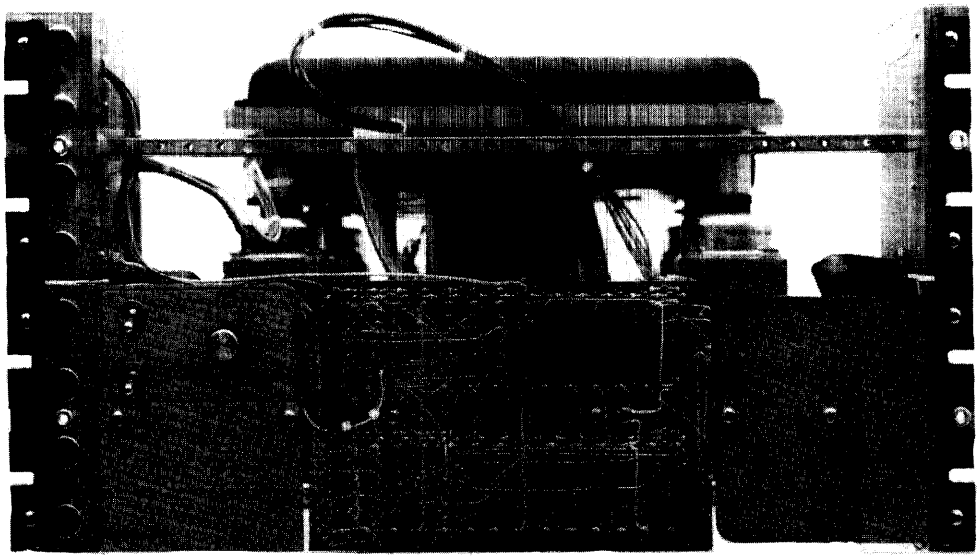


Figure 3-2 DS32-D Front Panel

Table 3-2
DS32-D Operating Control Functions

Control	Function
UNIT SELECT	Assigns disk selection number.
UPPER 16K	When in the ON position, inhibits writing on the upper 16K word positions of the DS32-D if write lockout is enabled.
LOWER 16K	When in the ON position, inhibits writing on the lower 16K word positions of the DS32-D if write lockout is enabled.

3.2 PROGRAMMING

The programming of the DF32-D is typical of an input/output (I/O) device attached to a PDP-8 family computer. Input/output transfer (IOT) instructions control device operation. The 3-cycle data break facility of the computer is used to transfer data between core memory and the DF32-D. The word count (WC) register (memory address 7750) of the data break facility specifies the number of word transfers, and the current address (CA) register (memory address 7751) of the data break facility specifies the starting address of the transfer. The DF32-D contains a disk buffer (DB) register to buffer the data between core memory and the disk; a disk memory address (DMA) register to specify the disk data address; an extended memory address (EMA) register to specify the disk and track; and an extended address (EA) register to specify the core memory field when the computer memory capacity has been expanded.

The IOT instructions initiate a data transfer and provide the DF32-D with the information it needs to take part in the transfer (see Figure 3-3). Bits 0, 1, and 2 represent the operation code. When the computer recognizes operation code 6, indicating an IOT instruction, the computer generates an IOP pulse. IOP1 is generated if a 1 is present in bit 11 of the IOT instruction; IOP2 is generated if a 1 is present in bit 10 of the IOT instruction; IOP4 is generated if a 1 is present in bit 9 of the IOT instruction. These IOP pulses are sent to the peripheral device designated by bits 3 through 8 of the IOT. Selection circuits within the device then generate IOT pulses, which specify device control operations. The IOT instructions that apply to the DF32-D are listed in Tables 3-3 and 3-4.

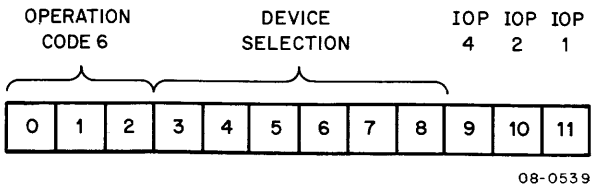


Figure 3-3 IOT Instructions

Table 3-3
DF32-D Instructions

Mnemonic	Octal	Operation
DCMA	6601	Clear the disk memory address register, parity error, and completion flags. This instruction clears the disk memory request flag and interrupt flags.
DMAR	6603	Load the disk memory address register with the information (initial address) stored in the accumulator (AC). Then clear the AC. Begin to read information from the disk into the specified core location. Clear parity error and completion flags. Clear interrupt flags. $AC_{0-11} \rightarrow DMA_{0-11}$
DMAW	6605	Load the disk memory address register with the information (initial address) stored in the accumulator (AC). Begin writing information onto the disk from the specified core location. A data break must be allowed to occur within 64 μs after this instruction is issued. Clear parity error and completion flags. Clear interrupt flags. $AC_{0-11} \rightarrow DMA_{0-11}$
DCEA	6611	Clear the disk extended address and memory address extension register. $0 \rightarrow EMA_{5-1}$ $0 \rightarrow EA_{3-1}$
DSAC	6612	Skip the next instruction if the address confirmed flag is a 1. This flag is set for 16 μs (AC is cleared). $0 \rightarrow AC$
DIEF	6614	Load the following information into the accumulator: Gap (Simulated photocell) flag $\rightarrow AC_0$ $EMA_{5-1} \rightarrow AC_{1-5}$ $EA_{3-1} \rightarrow AC_{6-8}$ data late flag $\rightarrow AC_9$ write lockout flag $\rightarrow AC_{10}$ } error flags parity error flag $\rightarrow AC_{11}$
DEAL	6615	Clear the disk extender address and memory address extension registers. Then load the disk extender address and memory address extension registers with the track address data held in the accumulator. $AC_{6-8} \rightarrow EA_{3-1}$, core memory extension $AC_{1-5} \rightarrow EMA_{5-1}$, disk address extension (128, 96, 64, 32K) $AC_{0;9-11}$, used with DEAC instruction
DEAC	6616	Clear the accumulator, then load the contents of the disk extended address register into the accumulator to allow program evaluation. Skip the next instruction if address confirmed flag is a 1.

Table 3-3 (Cont)
DF32-D Instructions

Mnemonic	Octal	Operation
DEAC (Cont)		128, 96, 64, 32K: $EMA_{5-1} \rightarrow AC_{1-5}$ Computer memory $EA_{3-1} \rightarrow AC_{6-8}$ Simulated photocell sync mark $\rightarrow AC_0$ Data request late flag $\rightarrow AC_9$ Nonexistent disk flag or write lock switch "on" $\rightarrow AC_{10}$* Parity errors $\rightarrow AC_{11}$
DFSE	6621	Skip next instruction if the parity error, data request late, or write lock switch flag is a 1 (no error).
DFSC	6622	Skip next instruction if the completion flag is a 1 (data transfer is complete).
DMAC	6626	Clear the accumulator, then load the contents of the disk memory address register into the accumulator to allow program evaluation. $DMA_{0-11} \rightarrow AC_{0-11}$

NOTE

1. During read the final address will be the last address transferred +1.
2. During write the final address will be the last address transferred.
3. The nonexistent disk condition will appear following the completion of a read data transfer if the address acknowledged was the last address of a disk and the next word to be addressed falls within a nonexistent disk. The completion flag for this data transfer is set by the nonexistent disk condition.

*Write lock switch status is true only when the disk module contains a write command.

Table 3-4
IOT Instructions

Instruction	Description
6601: DCMA	1. Generates SCL (start clear), which clears: a. TRC FF (transfer complete) b. NED FF (nonexistent disk) c. MRS FF (memory request sync)

Table 3-4 (Cont)
IOT Instructions

Instruction	Description
6601 (Cont)	d. ADC FF (address confirmed) e. DRL FF (data request late) f. PER FF (parity error) 2. Generates DTC (disk time clear) which clears: a. SEN FF (search enable) b. TCA FF (time counter "A") c. TCB FF (time counter "B") 3. Clears the disk memory address register
6602:	1. Clears the accumulator. 2. Clears the WRITE FF (setting transfer direction to read). 3. Generates LAD (load address), which: a. Causes a jam transfer from the accumulator to the disk memory address register by generating LAP and IOT 60. b. Clears WCO FF (word count overflow). c. Sets MRS FF (memory request sync).
6604:	1. Clears the accumulator. 2. Sets the R/W FF, setting transfer direction to write. 3. Generates LAD. 4. Sets DBR FF (data break request). NOTE Combinations of the 660X IOT are: 6603 DMAR (read) 6605 DMAW (write)
6611: DCEA	1. Clears disk extended memory address register. $0 \rightarrow EMA_{5-1}$ 2. Clears extended address register (for extended memory in computer). $0 \rightarrow EA_{3-1}$
6612: DSAC	1. Skip on address confirmed flag (used primarily in diagnostic programming). 2. Clears the accumulator.
6614: DIEF	1. Causes a transfer of 1s from the disk status register to accumulator bits 0 through 11 as follows: $GAP \rightarrow AC_0$ $EMA_{5-1} \rightarrow AC_{1-5}$ $EA_{3-1} \rightarrow AC_{6-8}$

Table 3-4 (Cont)
IOT Instructions

Instruction	Description
6614 (Cont)	DRL flag $\rightarrow AC_9$ WLO flag $\rightarrow AC_{10}$ } error flags PER flag $\rightarrow AC_{11}$ 2. Causes a jam transfer from accumulator bits 1 through 5 to the disk extended address register. $AC_{1-5} \rightarrow EMA_{5-1}$ NOTE Combinations of 661X IOTs are: 6615 DEAL (clear and load disk EMA register) $AC_{6-8} \rightarrow EA_{3-1}$ $AC_{1-5} \rightarrow EMA_{5-1}$ 6616 DEAC (0 $\rightarrow$AC, load AC with disk EMA)
6621: DFSE	1. Enables skip bus if no error flags are up (skip on no error).
6622: DFSC	1. Enables skip bus if the TRC FF is set and computer MB bit 9 is a 0 (IOT 6622 used alone). 2. Enables clear bus if computer MB bit 9 is a 1 (IOT 6622 used with IOT 6624).
6624:	1. Causes a transfer of 1s from disk memory address register to accumulator bits 0 through 11. $DMA_{0-11} \rightarrow AC_{0-11}$ NOTE Combinations of 662X IOTs are: 6626 DMAC (0 $\rightarrow$AC and load AC with DMAR)
	Maintenance IOT Instructions
6631: TAS (TTA simulator)	Generates false TTA pulses for static logic test.
6632: TBS (TTB simulator)	Generates false TTB pulses for static logic test.
6634: DBRS	Sets data break request FF static logic test. NOTE For maintenance, the MAINT-OPR switch must be turned to MAINT.

A typical computer program (Figure 3-4) illustrates the writing of a block of data onto the disk. The calling subroutine must be set up so the subsequent locations to SUB (SUB+1, SUB+2, etc.) contain the parameters shown in the comments column. The format of location SUB+3 must conform to that of the DEAC instruction in Table 3-3.

```
          /CALLING SEQUENCE
SUE,        JMS       WRT        /JUMP TO WRITE SUBROUTINE
             Ø                  /CONTAINS WORD COUNT
             Ø                  /CONTAINS INITIAL CORE MEMORY ADDRESS
             Ø                  /CONTAINS TRACK AND UNIT NUMBER
             Ø                  /CONTAINS TRACK ADDRESS
            XXX                 /CONTINUE WITH MAIN PROGRAM

          /WRITE SUBROUTINE
WRT,         Ø                  /ENTER WRITE SUBROUTINE
           TAD I     WRT        /FETCH WORD COUNT
           DCA       WC         /DEPOSIT IN WORD COUNT REGISTER
           ISZ       WRT        /INCREMENT POINTER
           TAD I     WRT        /FETCH INITIAL CORE MEMORY ADDRESS
           DCA       CA         /DEPOSIT INTO CURRENT ADDRESS REGISTER
           ISZ       WRT        /INCREMENT POINTER
           TAD I     WRT        /FETCH TRACK AND UNIT NUMBER
           DEAL                 /DEPOSIT INTO REGISTER IN DF32-D CONTROL
           CLA                  /CLEAR AC
           ISZ       WRT        /INCREMENT POINTER
           TAD I     WRT        /FETCH TRACK ADDRESS
           DMAW                 /TRACK ADDRESS TO DMA IN DISK; START
                                /WRITE OPERATION
           DFSC                 /JOB DONE
           JMP -1               /NO, WAIT
           DFSE                 /ANY ERRORS?
           JMP       ERR        /YES, GO TO ERROR SUBROUTINE
           ISZ       WRT        /NO, INCREMENT POINTER TO EXIT ADDRESS
           JMP I     WRT        /EXIT PROGRAM
```

Figure 3-4 Programming Example

Continuing with the program, the JMS WRT instruction causes a subroutine jump to location WRT, with the contents of the PC+1 (which contains symbolic address SUB+1) deposited into location WRT. Because location WRT contains SUB+1, the first instruction of the subroutine (TAD I WRT) loads the AC with the contents of SUB+1, the word count. The word count is then deposited into the WC register. The initial address is deposited in a similar manner into the CA register. The program then proceeds to set up the EMA and DMA registers and start the write operation. After the DMAW instruction is issued, the data transfer operation begins and continues independently of the program; the DF32-D operates under control of the data break facility while transferring data. When the transfer is complete, the transfer complete (TRC) flag raises and, when sensed by the DFSC control, causes the program to pass to the DFSE instruction. DFSE then senses for errors; if any errors are sensed, control jumps to an error or diagnostic routine. If no errors are sensed, control exits from

the subroutine, returns to the main program, and resumes main processing. The data transfer operates independently of the program; therefore, the subroutine could be exited following the DMAW instruction. An interrupt subroutine could handle the post-data transfer processing because the TRC flag generates an interrupt. An identical program could handle data transfers for a read operation if the DMAW instruction is replaced by the DMAR instruction.

Chapter 4
Theory of Operation

4.1 GENERAL

The mnemonics that represent the DF32-D and DS32-D signals are listed in Table 4-1. The control unit and the expander unit use the same mnemonics, but mnemonics representing signals generated by an expander unit are subscripted (e.g., SEL_1 indicates that the select signal was generated by expander unit 1).

Table 4-1
DF32-D/DS32-D Signal Mnemonics

Mnemonics	Description
ABD	Address Bit Detector
AC BUS*	
AC CLEAR*	
ACE	Address Compare Error
ADC	Address Confirmed
ADD ACCEPT*	Address Accept
A GND	Analog Ground
B AC*	Buffered Accumulator Bits
B ADC	Buffered Address Confirmed
B INITIALIZE*	
B IOP*	Buffered Input/Output Pulse
B RUN	Buffered Run
B WRITE	Buffered Write
BEM 0,1,2,3	Buffered Extended Disk Memory Units
BEMA	Buffered Extended Memory Address (disk)
BMB*	Buffered Memory Buffer Bits
BREAK*	Break Cycle
BRK RQST*	Break Request
BTS1*	Buffered Time State 1
BTS3*	Buffered Time State 3
BWC OVERFLOW*	Buffered Word Count Overflow
BWFF**	Buffered Write Flip-Flop (for writing in NRZI)

*Signals between computer and disk logic.
**Signals between extenders and disk logic.

Table 4-1 (Cont)
DF32-D/DS32-D Signal Mnemonics

Mnemonic	Description
BWLO	Buffered Write Lock-Out
C0-C7	Center Tap Selection 0 to 7
CARRY	Carry Flip-Flop (for address increment in DMA)
CBR	Clear Break Request
CEMA	Clear Extended Memory Register
CLA	Clear Accumulator
CLCP	Clear Carry Pulse
CSEN	Clear SEN Flip-Flop
DATA ADD*	Disk Address (7750)
DATA IN*	Direction of Information Flow into Computer During Break
DATA 00-11	Data Bits to Computer
DB 00-11	Data Bits Register in Disk Control
DBR	Data Break Flip-Flop
DCH	Disk or Track Change
DDI	Disk Data In (for assembly)
DEND	Data End (for address n if searching for n + 1)
DEP	Data End Pulse (for address n + 1 if searching for n + 1)
DMA	Disk Memory Address Register
DMA IN	Clocking Signal for Data into DMA Register
DOP	Data Ones Pulses
DRL	Data Request Late
DSL (+), (-)	Data Sense Lines
DTC	Disk Timer Clear (4 words)
EA 1,2,3	Extended Address
EDOP**	External Data Ones Pulses
EMO 1,2,3	Extended Disk Memory Units 0 to 3
EMA 1-5	Extended Memory Address Register (disk)
ERROR	Error in Search of Address
ETTAP**	External TTA Pulse
ETTBP**	External TTB Pulse
EUSS**	External Unselected Switch
EWL**	External Write Lock-Out from EA
EXT DATA ADD 0-2	Extended Address Bits Reversed
GAP	Flip-Flop Set During Time Between Address 4000 and Address 0
INITIALIZE*	Pulse from Computer to Reset Control Logic
INT	Interrupt to Computer
INT RQST BUS*	
IOT 60	Decoded Signal for Disk Input/Output Transfer
IOT	Input/Output Transfer Instruction
LAD	Load Address IOT
LAP	Load Address Pulse
LD ENABLE	Load Enable (for shift register M233)
MB INC	Increment MB
MB00-11	Memory Buffer Bits

*Signals between computer and disk logic.

**Signals between extenders and disk logic

Table 4-1 (Cont)
DF32-D/DS32-D Signal Mnemonics

Mnemonic	Description
MBC	Disk Memory Buffer Clear
MRS	Memory Request Synchronization
NED	Nonexistent Disk Flip-Flop
NEX	Nonexistent Disk
OPTION SELECT	Disk (option) Selected During In/Out Instruction
PAR	Parity Flip-Flop (even parity during read)
PER	Parity Error
SADC	Set ADC Flip-Flop
SAP	Shift Address Pulse
SBR	Set Break Request Flip-Flop
SCL	Start Clear
SEN	Search Enable
SKIP BUS*	Skip Next Instruction
SLT	Select
SNE	Status - No Error in WLO, EWL
SPW	Bit for Special Word (4000)
STATUS	Status of WLO, EWL, NEX
SYNC P	Synchronizing Pulse (end of address 4000)
SYNC	Flip-Flop to Synchronize with Addressing on Disk
TCA	Time Counter A
TCB	Time Counter B 4 Word Hold Before Setting SEN
TCX	Time Counter X
TP1	Time Pulse 1
TRC	Transfer Complete
TRK INC	Track Increment (during search)
TS3	Time State 3
TS3B	Time State 3 of Break Cycle
TTA	Timing Track A (timing)
TTB	Timing Track B (addressing)
TTA D1	Strobed Analog Signal TTA from Disk
TTA D2	
TTA 1	TTA Delayed for DDI
TTA 2	TTA Delayed for ABD Resetting
TTAD	TTA Delayed for Strobing Data
TTA, ADC + TS3B	For Clocking Data Shift Register
USS	Unselected Switch (disk units)
WC OVERFLOW	Word Count Overflow
WCO	Word Count Overflow Flip-Flop
WFF	Write Flip-Flop (for NRZI writing)
WIA	Inhibit Writing on Upper 16K of Memory
WIB	Inhibit Writing on Lower 16K of Memory
WLO	Write Lock-Out
WRITE	Write on Disk Flip-Flop (READ if flip-flop reset)
X0-X7	Selection Levels for Disk Heads
3 CYCLE	3-Cycle Break

*Signals between computer and disk logic.

**Signals between extenders and disk logic.

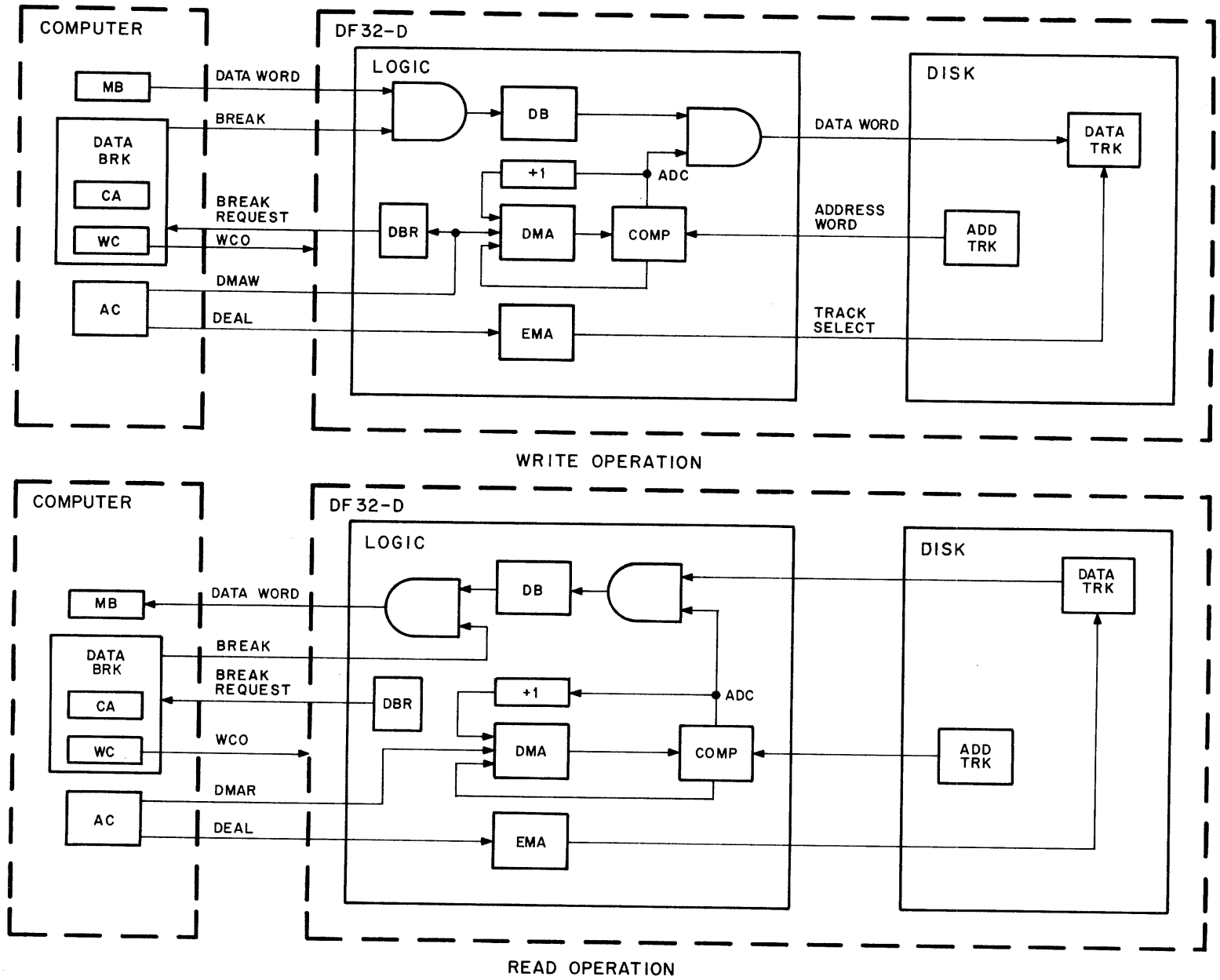


Figure 4-1 DF32-D Block Diagram, Write and Read Operations

A write operation and a read operation are shown in Figure 4-1. Although the two block diagrams are similar to a great extent, the operations have been presented separately to avoid confusing overlap of signal directions. The DF32-D can be represented by two large blocks (the logic circuits and the disk) and each operation involves a transfer of a data word, an address word, and a track selection signal between these two blocks. Also note that only the data word changes direction when the operation changes from write to read.

4.1.1 Write Operation

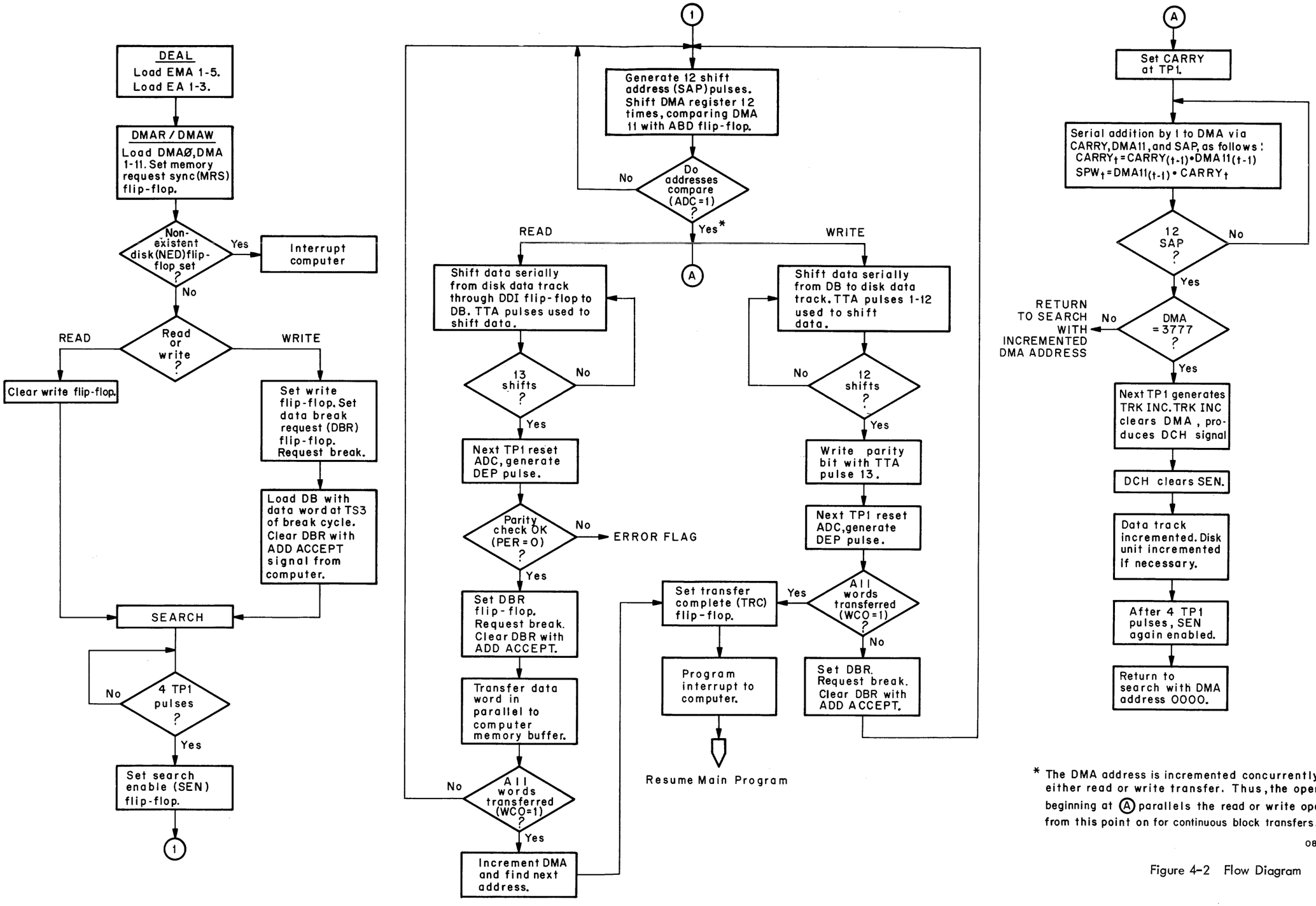
When the program has loaded the WC and CA registers, it sets up the AC with the unit number (DF32-D or one of the extender disks) and the disk data track number. The DEAL instruction transfers this information to the DF32-D extended memory address (EMA) register, which selects 1 of 16 data tracks. When the data track has been selected, the program loads the AC with the initial address. DMAW transfers this address from the AC to the disk memory address (DMA) register, and, at the same time, sets the data break request (DBR) flip-flop. The DBR flip-flop sends a break request signal to the data break facility. The facility responds with a BREAK signal, which, at time state 3 (TS3) of the computer break cycle, enables a parallel transfer of the data from the computer memory buffer (MB) register to the disk buffer (DB) register.

The data word stored in the DB register must be written on the disk in the correct data track location. The data track has already been selected. The DMA contains the address of the track location where the data should be written. To indicate when the correct location is passing over the recording heads, an address track is included on the disk. For each address on this track, there is a corresponding data word location on the data track. If the two differ, the address in the DMA is circulated and compared to the next address from the track. This comparison continues until the two addresses match (i.e., the correct address on the track has been found). An address confirmed (ADC) signal, developed in the comparator, indicates that the desired location on the data track is passing over the recording head.

The data word is now serially shifted from the DB to the disk data track. When the addresses match, the DMA address is again circulated, but in this case it is also incremented. The new address indicates the data track location of the next data word. The comparison is repeated for this address and for each succeeding incremented address. When the last word of the block has been transferred from the MB to the disk, the WC register sends a word count overflow (WCO) signal to the logic, and the operation ends.

4.1.2 Read Operation

Like the write operation, the read operation begins with an address search. DMAR transfers the initial address to the DMA but does not request a break (in the write operation the DMAW requests a break).



* The DMA address is incremented concurrently with either read or write transfer. Thus, the operation beginning at (A) parallels the read or write operation from this point on for continuous block transfers.

08-0544

Figure 4-2 Flow Diagram

Instead, a break is requested only after the initial address has been found and the data word has been loaded into the DB. Then, the computer responds with the BREAK signal, transferring the data word to the MB.

The search, read, and write operations, and the disk are described in detail in succeeding paragraphs. However, before proceeding to the discussion, refer to Figure 4-2. Some features of this diagram are beyond the level of information already presented in the manual; however, a careful study of this diagram will provide further insight to the general operation of the DF32-D. The flow diagram is useful as an aid to understanding the detailed discussions, and should be consulted frequently.

4.2 DISK

Figure 4-1 is divided into two large components: the logic circuits and the disk. The disk is a major component of the DF32-D and is discussed in detail in the following paragraphs.

4.2.1 Disk Format

The disk is a 10-in. diameter aluminum plate, covered first with a thin nickel-cobalt layer and then with a hard rhodium plating. A 0.95-in. wide ring at the outside edge of either surface is used for recording. Within this ring, 16 data tracks and 4 timing tracks can be recorded (see Figure 4-3). The first track is the TTA timing track and the fourth is the spare TTA. The seventh track is the TTB address track and the tenth is the spare TTB. The remaining 16 tracks, numbered 0_8 through 17_8, are reserved for data recording.

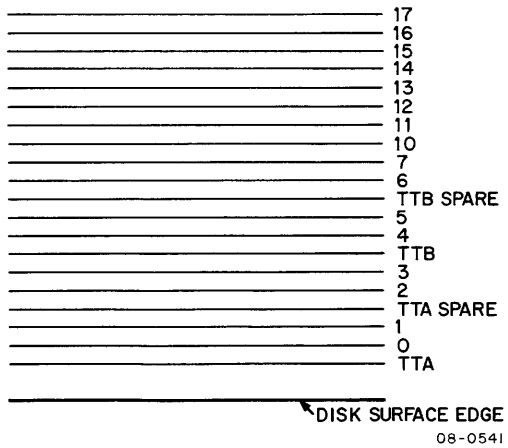


Figure 4-3 Disk Track Order

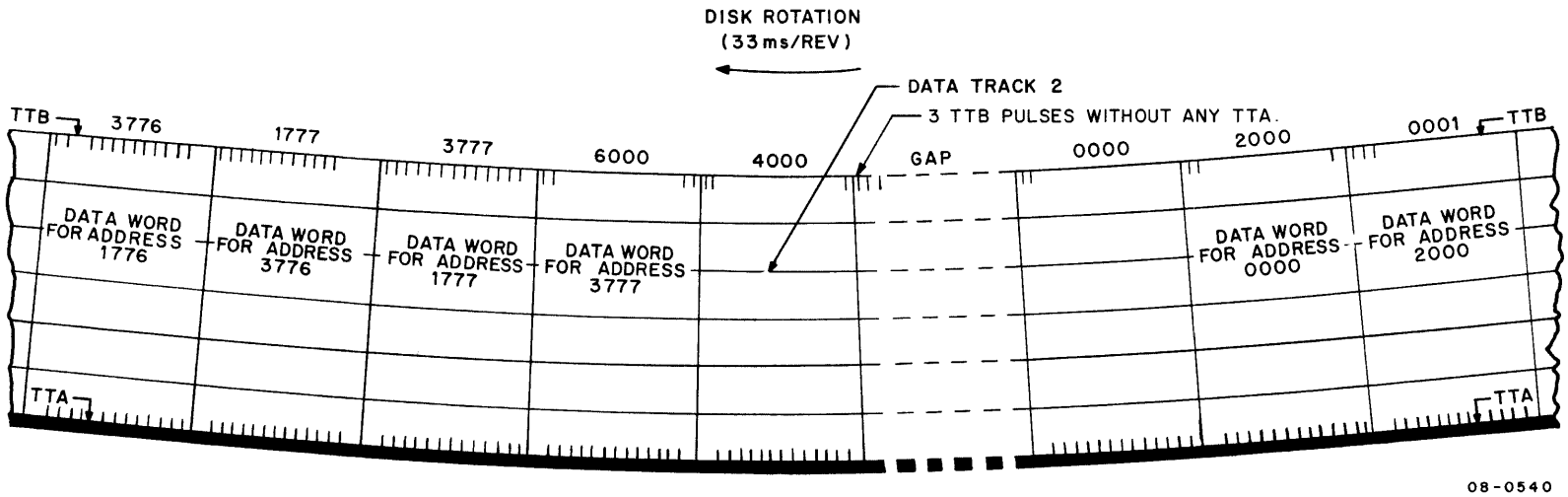


Figure 4-4 Disk Format

The timing track, the address track, and the two spares, are recorded on the disk at the factory. If the main tracks are accidentally destroyed, the spare TTA and TTB tracks can be used. In the unlikely event that the entire disk is erased, a DF32-D-15 Timing Track Writer can be used for field recording of the timing and address tracks. Appendix A contains a detailed discussion of the timing track writer.

Figure 4-4 is a portion of the recorded surface of the disk (TTA, TTB, and data track 2); for clarity, the remaining tracks are not identified. A total of 2050 12-bit addresses are recorded on TTB. Two addresses, 6000_8 and 4000_8, are used for timing. Each of the remaining 2048 addresses, from 0000_8 through 3777_8, is used to locate a 13-bit data track word. There are 16 data tracks and only one track at a time is used; therefore, there are 16 times 2048, or 32,768 data word locations.

Addresses 6000_8 and 4000_8 are used only for timing and have no corresponding data words on the data tracks, thus, the data track is blank from the end of address 6000_8 to the beginning of address 2000_8. This interval, specifically the group of three TTB pulses appearing after address 4000_8, is used to synchronize the disk tracks with the control logic. Synchronization is discussed in detail in Paragraph 4.3. The data word for each address is located in the interval immediately following that address. A search process takes place prior to a read or write operation, and TTB addresses are compared to an address contained in the DMA. An address match is recognized only after the complete address has been examined; therefore, the data word for the address must be placed in the location following the address.

The recording of an address on the disk is also shown in Figure 4-4. Rather than being consecutive from 0000_8, the addresses alternate in the following manner: 0000_8, 2000_8, 0001_8, 2001_8, 0002_8, 2002_8, 0003_8, etc. Figure 4-5 illustrates the reason for this particular scheme. Assume that address 0000_8 is stored in the DMA. An address search begins and later, 0000_8 from the TTB track is compared to 0000_8 in the DMA. This comparison occurs during period 5 (Figure 4-5). At the end of period 5, the ADC signal enables the serial shift of the data word to the disk data track, if a write operation is performed.

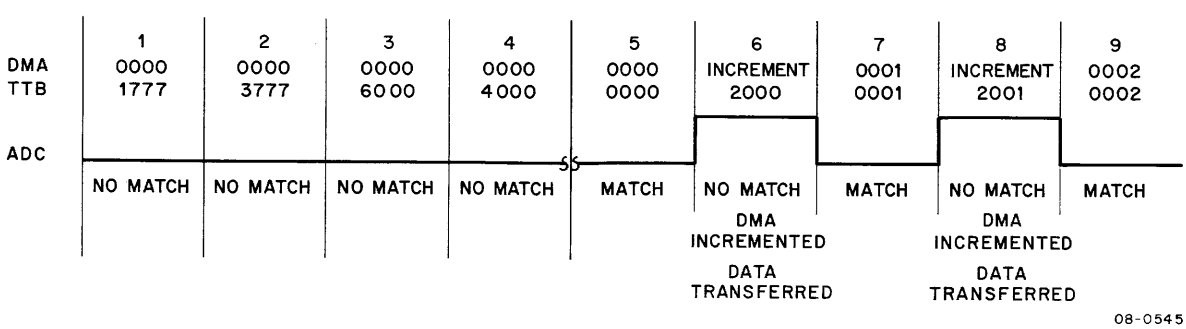


Figure 4-5 Search/Transfer Operation Timing

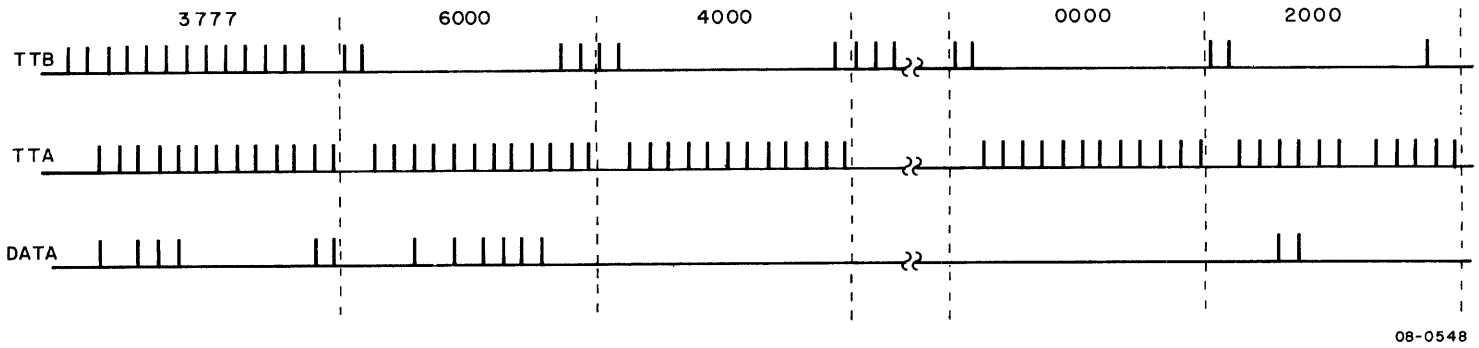


Figure 4-6 Disk Track Timing

The shift occurs and the DMA is incremented during period 6; thus, at the beginning of period 7, the DMA contains 0001_8 and this same address is beginning to be read from the TTB track. Another match occurs and a transfer takes place in period 8. An address match occurs in each succeeding odd period until the end of the block transfer. The particular addressing scheme of the TTB track thus results in an optimum data transfer rate.

NOTE

(1) The address sequence described is the one normally recorded on the disk. Many other schemes are possible but this particular scheme results in rapid data transfers and is preferable in most instances.

(2) In at least one instance, another scheme may be more desirable to the DF32-D user. Users who previously incorporated the DF32 into their systems, and who have compiled large software files based on the address sequence employed in the DF32, may wish to continue with this sequence. Digital Equipment Corporation has considered this and will record the address sequence familiar to these users.

(3) To first-time users of the disk file system, DEC recommends using the normal address scheme of the DF32-D. The alternate address scheme is described in Appendix A for those who wish to compare the two. Note that the sequence of the DF32-D allows the user to transfer an entire data track in only two revolutions of the disk; this is twice as fast as the scheme used by the DF32.

4.2.2 Disk Timing

The relative timing of the three disk tracks is illustrated in Figure 4-6, covering addresses 3777_8 through 2000_8. Each track has 14 bit positions per address word period. The first two TTB bit positions are always occupied by timing pulses. The remaining 12 positions contain 1s or 0s depending on the address word for that period. Refer to address 6000_8. The first two TTB pulses are the timing pulses. The next TTB bit position (the third) is reserved for the least-significant bit (LSB) of the address. The bit positions increase in significance while proceeding to the right; thus, the most-significant bit (MSB) would appear in position 14, as is the case with 6000_8. In other words, the addresses and data words are recorded backwards on the disk.

TTA is characterized by one 0 and thirteen 1s during each period. Note that the TTA bit positions are out of phase with the TTB positions; the significance of this phase difference becomes apparent when the logic timing is discussed.

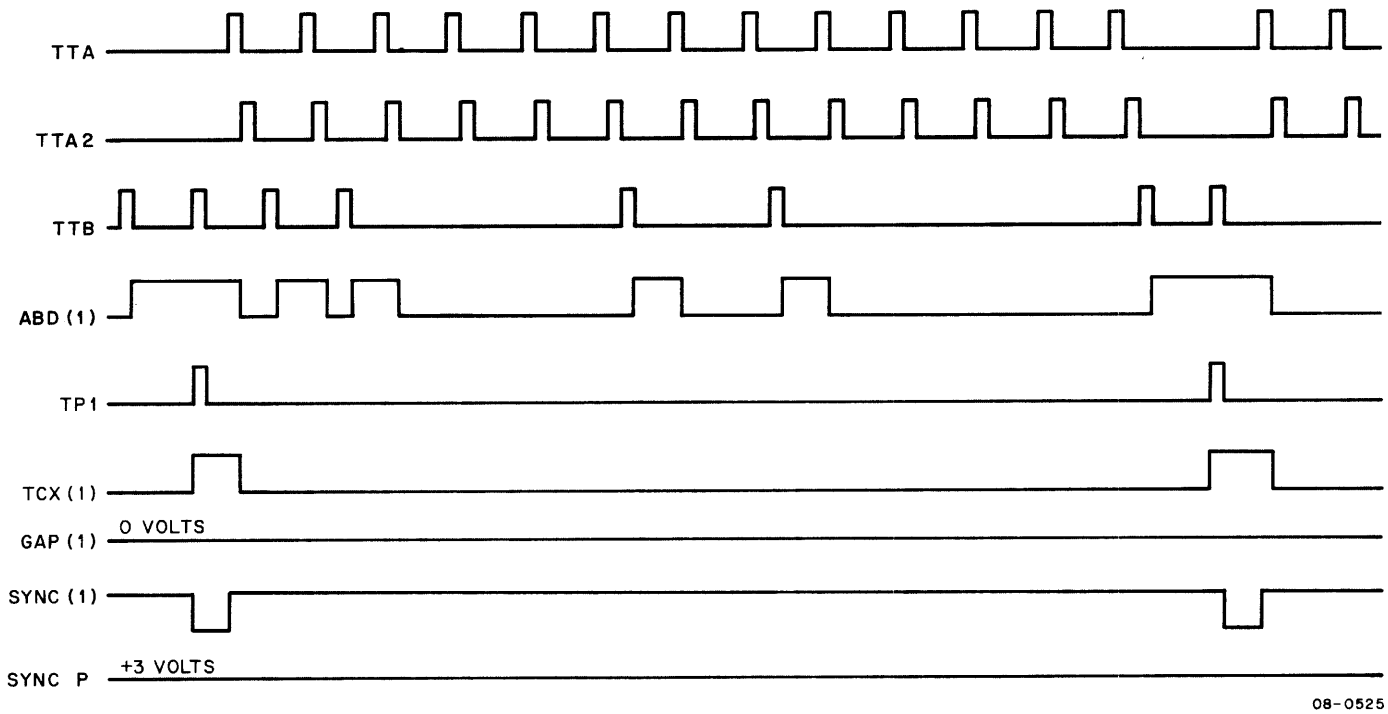


Figure 4-7 Basic Timing Signals

Each data track (only one is represented in Figure 4-6) contains 4000_8 data words. Data word bit positions are in phase with those of TTA and contain 1s or 0s. The first twelve bits from the left represent the data (the data word is backwards). Bit 13, a parity bit position, contains a 1 when the data word contains an odd number of 1s.

4.2.3 Disk Recording Technique

Various tracks are represented as containing 1s and 0s, pulses and no pulses; however, during any bit position, a magnetic flux pattern, recorded by a non-return to zero inhibit (NRZI) technique, is physically present. In NRZI, a 1 is represented by a change in the direction of magnetic flux, and a 0 is represented by no change.

In the write operation, a flip-flop is used to control the polarity of the recording head magnetizing current. When the flip-flop is set, current flows through the head coil in one direction; clearing the flip-flop reverses the current flow and the direction of the magnetic flux lines. A 1 is recorded. In the read operation, the head senses the flux changes and produces bipolar pulses, which are rectified and shaped to produce data pulses.

4.3 LOGIC CIRCUITS

The DF32-D logic circuits are discussed in detail in the following paragraphs.

4.3.1 Logic Timing

The block diagrams of the read and write operations are similar in most respects. The greater part of the logic hardware is used in searching for the correct address. Each operation (read or write) is preceded by an address search. To aid in understanding the address search, certain aspects of operation timing will first be discussed.

As noted earlier, the computer program provides instructions which initiate the DF32-D address search; however, the DF32-D is not inactive before the program begins an address search. Instead, the disk motor is turned on, the disk is rotating, TTA and TTB pulses are read from their respective tracks, and certain timing pulses are generated by the logic circuits. Figure 4-7 shows basic timing signals, and Figure 4-8 shows the logic elements used to generate the signals.

Recall that each address word period contains 13 TTA pulses and as many as 14 TTB pulses, and that the first two TTB pulses are always present. These two TTB pulses are used to produce one TP1 pulse at the beginning of each address word period. The first TTB pulse sets the address bit detector (ABD) flip-flop and the second TTB is NANDed with ABD(1) to produce TP1. ABD is then reset by the first TTA2 pulse. Each succeeding TTB pulse sets ABD, which is then cleared by the next TTA2 pulse. Thus, the

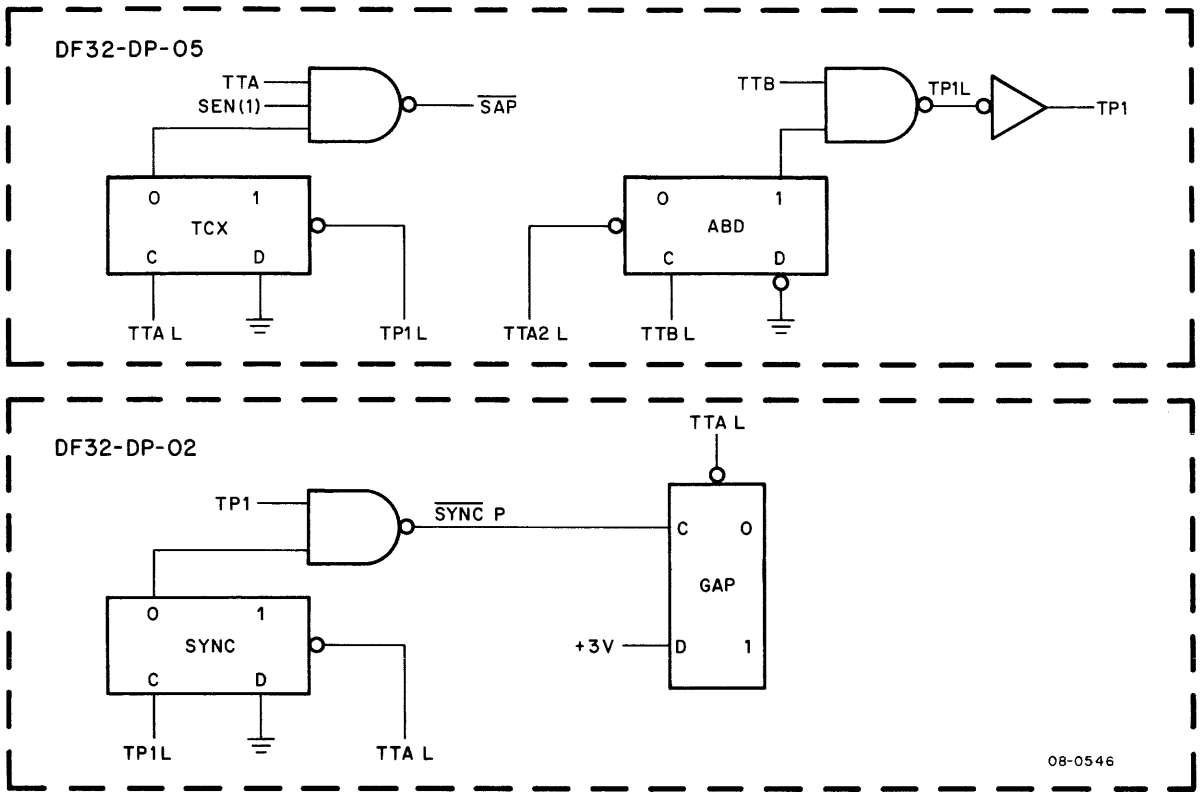


Figure 4-8 Basic Timing Logic

ABD signal represents the address contained in the TTB track, and performs an important function during the address comparison process. Each TP1 pulse sets the time counter X (TCX) flip-flop. TCX is reset by the trailing edge of the first TTA pulse. In Figure 4-8, TCX(0) is NANDed with TTA and SEN(1) to produce shift address (SAP) pulses. SEN(1) represents the set state of the search enable flip-flop, and is introduced at this time to demonstrate the application of the TCX flip-flop (i.e., masking of the first TTA pulse). The masking process results in the generation of 12, rather than 13, SAP pulses. The SAP pulses are used to serial shift the addresses through the DMA. Thus, only 12 pulses are required.

The signals representing the GAP flip-flop and the SYNC flip-flop are used primarily between addresses 4000_8 and 0000_8. In Figure 4-4, address 4000_8 is followed by three TTB pulses. The TTB pulses are followed by a 2-ms gap (approximate) during which the disk address and timing tracks are blank. The gap period is indicated as discontinuous due to the extreme difference in duration between this period and a 15-μs address word period (refer to Appendix A for signal duration details). The timing related to this gap is shown in Figure 4-9. The signals are generated continuously while the disk is rotating, even when no data transfer has been programmed. The signals have little significance until a data transfer begins; therefore, these signals will be discussed from that standpoint.

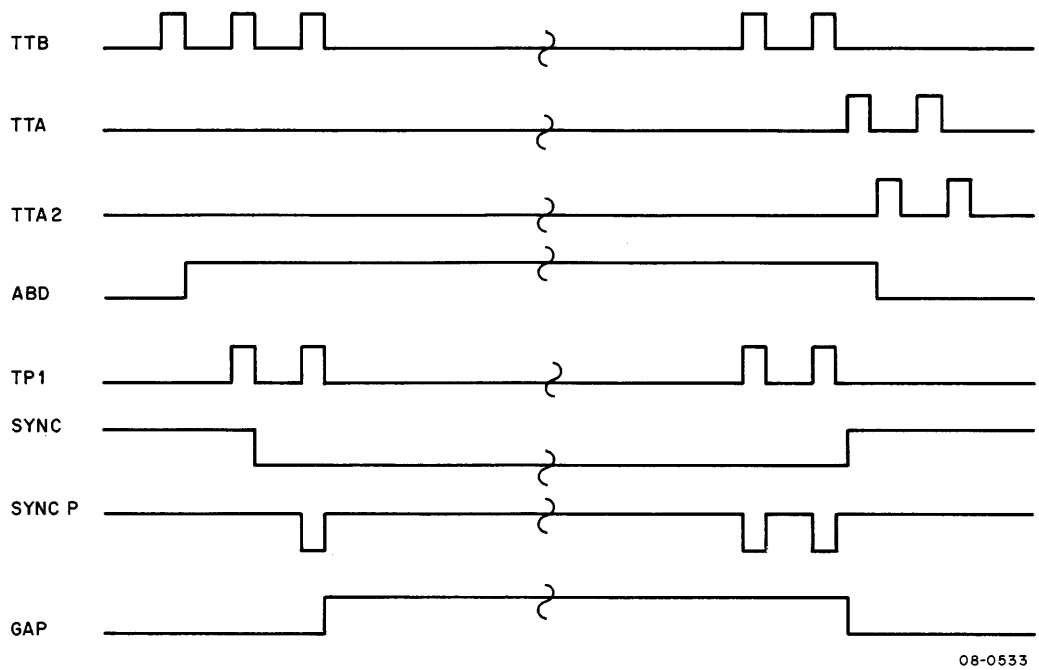


Figure 4-9 GAP Timing

A write operation, for instance, could involve a block of 2060 data words. The block cannot be contained in one data track because each track has only 2048 word locations; therefore, two data tracks are used. When one is filled, the EMA register, which selects data tracks, is incremented and the remaining words are written on the second track. The EMA is incremented at the end of address 6000_8. At the same time, the search process is disabled and remains disabled during the transition period. The search must be reinitiated before address 0000_8 is read from the TTB track. Four TP1 pulses are required to begin the search. The ABD flip-flop remains high through the gap, as shown; therefore, these four TP1 pulses are produced.

The GAP flip-flop likewise remains set throughout the gap, and the trailing edge of the GAP signal is used to clear the CARRY flip-flop (not shown) before address 0000_8 is read from the TTB track. If CARRY is not cleared, the DMA is prematurely incremented from 0000_8 to 0001_8.

4.3.2 Search Operation

During the cycle of these basic timing signals, the program will issue an IOT instruction and the DF32-D device selector will provide a signal that initiates operation. Drawing DF32-DP-05 (Section 6) shows the disk control logic; locate the shift enable (SEN) flip-flop. The SEN signal, one of the more important enabling signals used in SAP generation, provides the shift enable signal for the DMA register. SEN must be set before a search can begin. The following paragraphs explain how this signal is produced.

Either DMAR or DMAW will initiate a search. Both instructions produce:

1. The start clear (SCL) signal
2. The load address (LAD) signal

SCL clears the following flip-flops: memory request sync (MRS), time count A (TCA), time count B (TCB), and SEN. LAD then sets MRS which enables TP1 to clock the 3-stage counter consisting of TCA, TCB, and SEN. The fourth TP1 pulse sets SEN, which then resets MRS, preventing further clocking of the 3-stage counter. The delay between issuing DMAW or DMAR and the setting of SEN ensures that the correct data track heads are selected. In addition, the delay permits stabilization of the logic modules that depend on the direction of information transfer (e.g., the disk amplifier module).

The major component in the logic elements used in address search is the DMA register, a 12-bit shift register that is capable of serial and parallel load (see Figure 4-10). If the SEN signal is present on the SHIFT line, SAP pulses will shift in the information present on the SERIAL IN line. If, instead, an IOT 660X instruction is present on the LOAD line, a LAP pulse clocks in the information present on the 11 inputs designated AC1 through AC11.

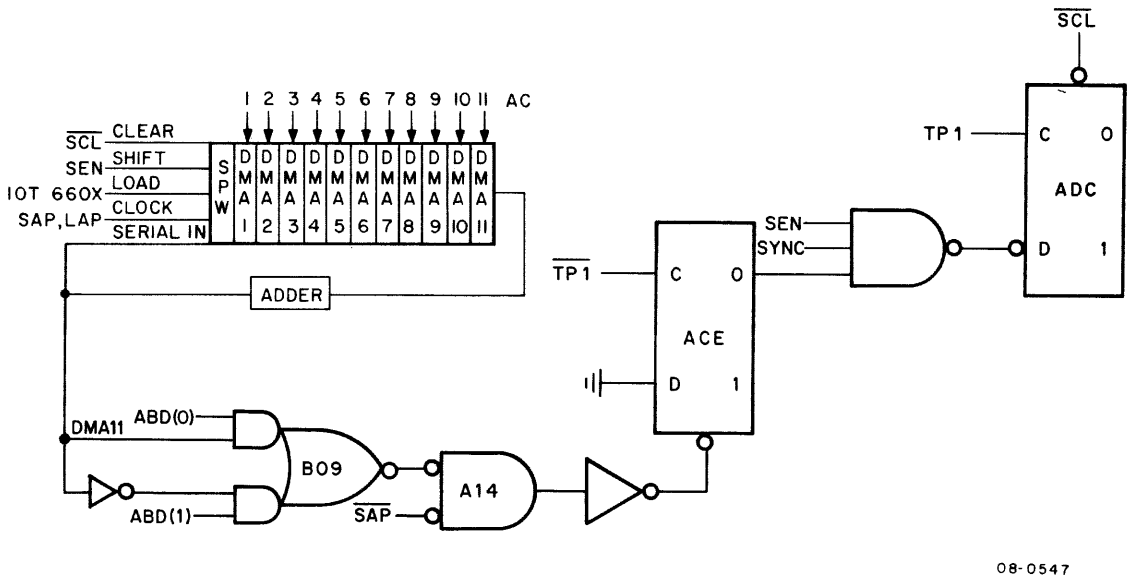


Figure 4-10 Address Search, Simplified Logic Block Diagram

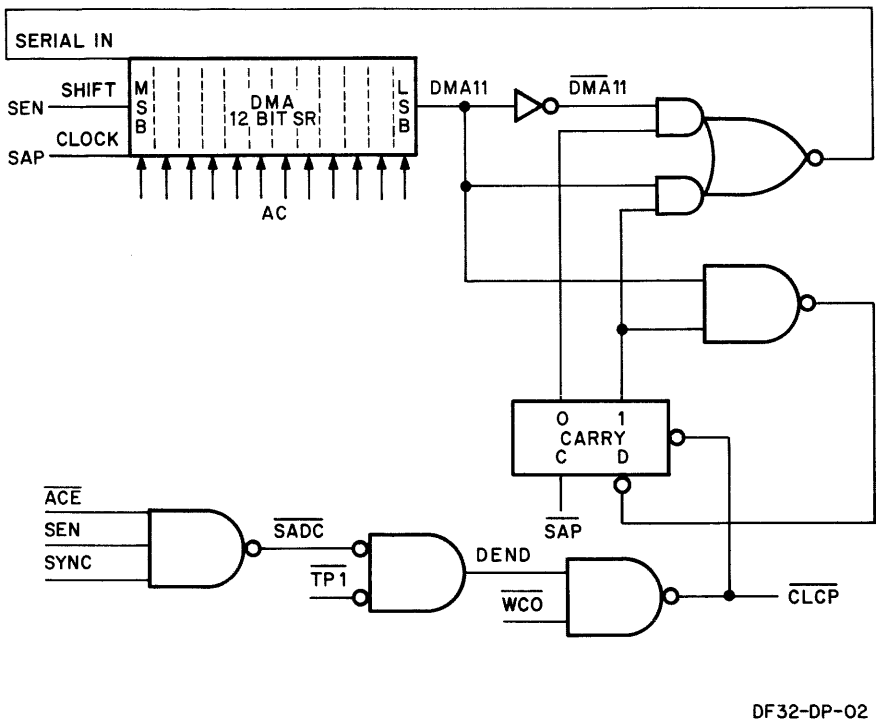
The latter process, the parallel load, is accomplished by either the DMAR or the DMAW instructions. Recall that the initial address is transferred by the program from computer memory to the AC. When the LAD signal is generated by DMAR or DMAW, LAP pulse is produced. Because the DMA LOAD is

enabled, the LAP pulse clocks in the information from the AC. Therefore, when the SEN signal is generated by TP1, the initial address is present in the DMA. SAP pulses applied to the CLOCK line shift in the information on SERIAL IN. This information is the output of the DMA (12th bit, or DMA11) fed back through an adder network. For the moment, assume that DMA11 is tied directly to SERIAL IN. The first SAP pulse shifts the DMA to the right by one bit position (bit 12 of the initial address is shifted into SPW, bit 11 is shifted into DMA11). Twelve SAP pulses will shift the DMA completely around. As each SAP pulse shifts the DMA, the new content of DMA11 is compared with the ABD signal. Recall that the ABD flip-flop represents the address bit on the TTB track. The 12 bits of the initial address are thus compared with the 12 bits of an address from the TTB track. If the two addresses compare, bit by bit, the output of the AND/NOR gate, B09, remains true and the address compare error (ACE) flip-flop, initially cleared by TP1, remains clear for the entire address word period. Data input to the address confirmed (ADC) flip-flop is false when the next TP1 is applied to the ADC clock input. ADC is then set by TP1. ADC enables the DB to shift the data word in the direction of transfer.

If the two addresses do not match, the output of gate B09 drops low. The negative-going signal at the DC-set input of ACE sets the flip-flop. The ADC signal is not produced and the data word remains in the DB. Each succeeding address from the TTB track is compared with the initial DMA address, until the correct address on the track is found.

The DMA initial address represents the data track location from or to which only the first data word is transferred. After the transfer of the first data word, the initial address must be incremented, in order to represent the location of the second word of the group. Each time a word is transferred, the DMA is incremented to indicate the intended location of the next data word. The DMA address is incremented by the adder network (see Figure 4-10).

This adder network (shown in detail in Figure 4-11) and the accompanying timing diagram illustrate DMA incrementation. The timing diagram represents an incrementation from address 3503_8 to address 3504_8, as an example. The SAP pulses are again used to circulate the address through the DMA; however, during this circulation, a 1 is added to the address by the CARRY flip-flop. The CARRY flip-flop will be set by the $\overline{\text{CLCP}}$ pulse at the beginning of the address word period if the address is to be incremented. $\overline{\text{CLCP}}$ is produced by TP1, providing the ACE flip-flop has not been set during the address search and there is no word count overflow (WCO) signal. If the ACE flip-flop has been set, indicating that the DMA address and the TTB track address were different, the DMA address is circulated without being incremented.



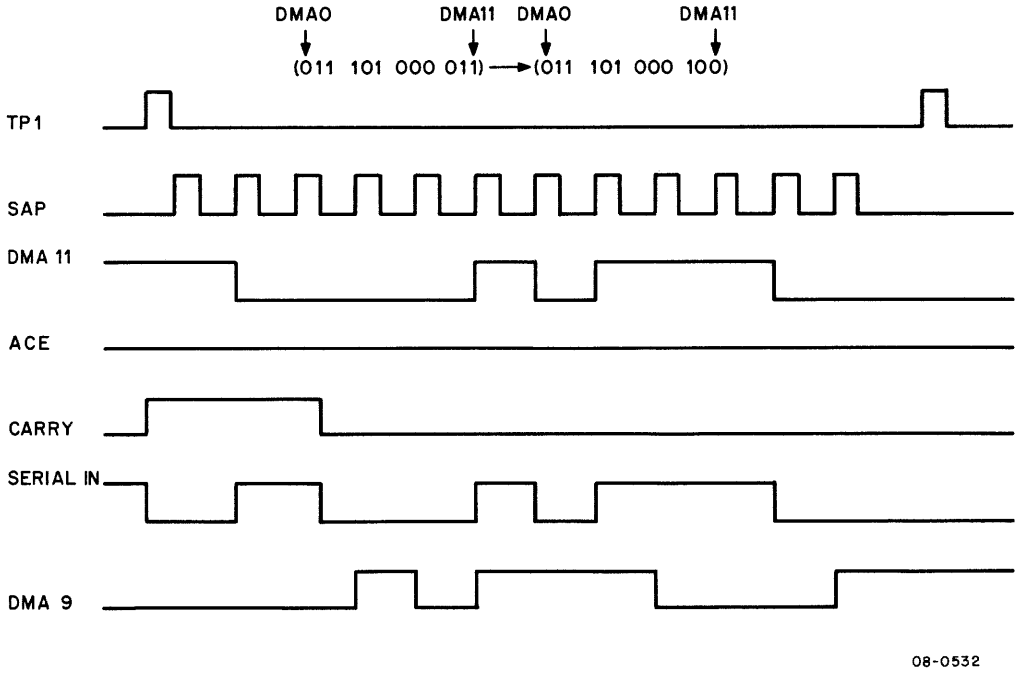


Figure 4-11 DMA Incrementation and Timing

In the above example, CARRY is set by $\overline{CLCP}$ and remains set until cleared by SAP pulse 3. SAP pulse 3 also shifts a 1 into the DMA MSB. The 1 is shifted one bit position to the right by each succeeding SAP pulse. After 12 SAP pulses, DMA9 contains a 1 and the new address in the DMA is 3504_8. The comparison process is repeated and the DMA is incremented again, this time to 3505_8. When address 3777_8 appears in the DMA, special logic is employed to ensure correct operation. A number of objectives must be met when 3777 is incremented. First, the logic must be reset so a search can begin with address 0000_8. Second, the DMA must be cleared to 0000_8. Third, the data track count in the EMA must be incremented.

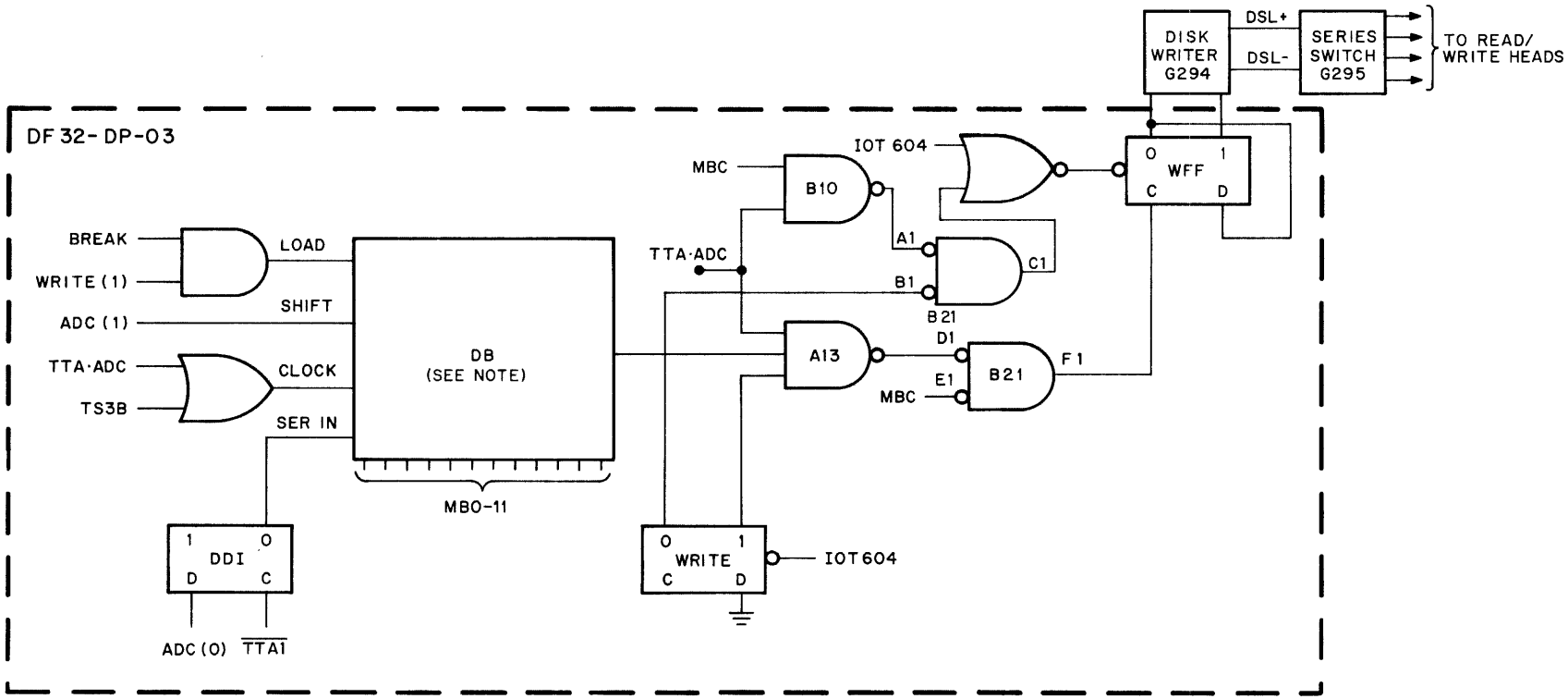
All the objectives are essentially met by the signal $\overline{\text{TRK INC}}$. Drawing DF32-DP-02 (Section 6) shows that this signal is produced by TP1 when 3777_8 is incremented to 6000_8 (6000_8 and 4000_8 are the only addresses that produce a 1 in SPW of the DMA). $\overline{\text{TRK INC}}$ is applied to the EMA register, advancing it to the next data track, and to the DMA register, resetting it to 0000. At the same time, $\overline{\text{TRK INC}}$ produces a DCH pulse, which is applied to the control logic (Drawing DF32-DP-05). The DCH pulse produces the disk timer clear (DTC) signal, which clears the SEN flip-flop and sets the MRS flip-flop. SEN will be reset only after four TP1 pulses have been produced. These TP1 pulses are produced between addresses 4000_8 and 0000_8 of the TTB track (refer to Figure 4-9 and the accompanying discussion of the gap period).

4.3.3 Write Operation

The major component of the write operation (as in the search operation) is a 12-bit shift register capable of serial and parallel transfers (see Figure 4-12).

The state of the WRITE flip-flop depends on the operation performed: read or write. IOT 6604 in addition to setting the WRITE flip-flop, which indicates a write operation, also sets the DBR flip-flop, thereby requesting a BREAK signal from the computer. The BREAK signal and the WRITE signal provide a LOAD enable for the DB register. When the TS3B signal, indicating time state 3 of the computer break cycle, is applied to the DB clock line, the data word is transferred in parallel from the memory buffer.

Following a successful address search, this data word must be shifted from the DB to the specified data track. TTA pulses are used to shift the data word, bit by bit, and the ADC signal is used to enable the shift operation. Each TTA pulse is NANDed in gate A13 with the content of DB11. When DB11 contains a 1, the WFF flip-flop is complemented by a pulse on the clock input; a 0 in DB11 leaves WFF unchanged. Each time WFF is complemented, the disk writer, G294, will record a 1 on the data track (as noted earlier, this recording technique is called NRZI).



NOTE
The DB register is being used in its complemented state for data.

08-0535

Figure 4-12 Write Operation Simplified Logic - Block Diagram

Although the DB contains only a 12-bit data word, there are 13 TTA pulses generated during each word period. The first 12 are used to shift the 13-bit data word. The 13th TTA pulse is used to write a parity bit if one is necessary. Note that WFF can be clocked or DC-reset, and that each operation can be essentially performed by TTA. Whether WFF is clocked or DC-reset depends on the memory buffer clear (MBC) signal. This signal is false when the first 12 TTA pulses are shifting the DB. Thus, B21 is enabled and B10 is inhibited. TTA pulses then clock WFF, complementing it each time a 1 appears in DB11.

After the twelfth TTA pulse, but before the thirteenth, MBC becomes true. B21 is disabled, when B10 is enabled. The thirteenth TTA pulse resets WFF. If the data word contains an odd number of 1s, WFF is set (notice that WFF is initially reset by IOT 6604). The thirteenth TTA pulse then resets WFF and this transition is written on the data track as the parity bit. However, if parity existed in the data word, WFF would already be reset after the twelfth TTA pulse and, since no transition would be effected by TTA13, a 0 would be written in the parity bit position.

The state of MBC is determined as follows (see Drawing DF32-DP-03). Modules A13, A18, and B18 produce the MBC signal. MBC remains false during the 12 data bits by NANDing $\overline{DB00}$ through $\overline{DB10}$ and $\overline{DDI}$, as shown. DDI begins in the set state, and the first TTA pulse therefore shifts a 0 into DB0. DDI is then reset by TTA1 and remains in this state for the rest of the data word. TTA pulses 2 through 13 shift 1s into DB0. The 0 shifted into DB0 by TTA pulse 1 is shifted out of DB10 by TTA pulse 12. Therefore, after 12 TTA pulses, all the inputs of A13 are true, and MBC becomes true. TTA pulse 13 writes a parity bit if one is necessary.

When the data word has been written on the disk, the DEP produced when TP1 resets the ADC flip-flop is applied to the DBR flip-flop. If more data is to be transferred, DBR requests a break cycle, as before. When the last data word has been transferred, the WCO flip-flop prevents the DBR from requesting a break; instead, the TRC flip-flop will be set by the DEP pulse. This flip-flop then generates an interrupt, notifying the program that the transfer operation has ended.

4.3.4 Read Operation

The DB is used to transfer the read operation information from the disk data track to the computer memory buffer (see Figure 4-13).

The WRITE flip-flop is reset by IOT 6602, indicating a read operation. As in the write operation, TTA is used to shift the DB, and ADC is used to enable this shift. The DDI flip-flop performs a more important function in the read operation than it did in the write operation by providing the DB with a 1 or a 0 at the SERIAL IN line, in response to a 1 or a 0 in the data word.

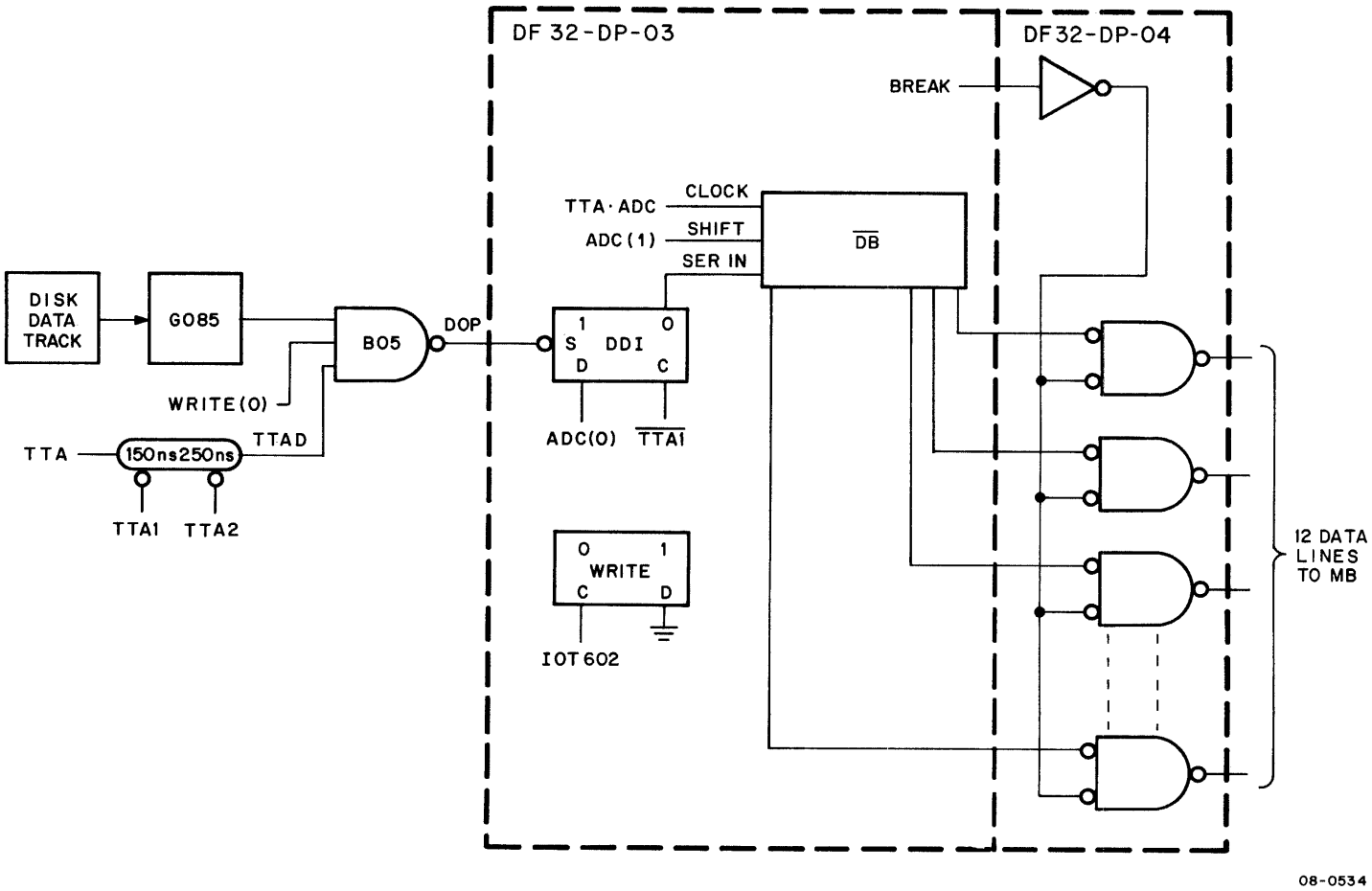


Figure 4-13 Read Operation Simplified Logic - Block Diagram

Following a successful address search, the data word must be shifted from the specified data track to the DB. Each time the amplifier and detector module, G085, detects a 1 in the data word, it provides a true sliced signal to one of the inputs of NAND gate B05. The TTAD pulse strobes the true level to produce a DOP pulse. Each DOP pulse sets the DDI flip-flop. A TTA pulse then shifts a 0 into $\overline{DB0}$. (Refer to Figure 4-14.)

Note that TTA pulse 1 clocks the DB before a DOP pulse is produced. The state represented by DDI(0) is shifted into DB0. It makes no difference if a 1 or a 0 is shifted in because the thirteenth TTA pulse will shift the bit out of the DB. Each DOP sets DDI; each TTA1 pulse resets DDI. TTA pulses 2 through 13 shift the 12-bit data word into the register. When the entire data word is shifted in, various AND gates of the B24 module are qualified. If a BREAK signal is received from the computer, the data word will be transferred; however, before the transfer, the disk logic checks the data word for parity (see Drawing DF32-DP-03). The parity (PAR) flip-flop is reset by the CLCP pulse prior to generation of DOP pulses. Each DOP pulse complements the PAR flip-flop; therefore, an even number of DOP pulses leaves the PAR flip-flop in its original state (i.e., reset). When the DEP is applied to NAND gate B11, it produces a clock pulse for the parity error (PER) flip-flop. If PAR is set by an odd number of DOP pulses, the clock pulse sets PER. This error signal is sensed by IOT 6621 in the program, and a program error subroutine may be entered.

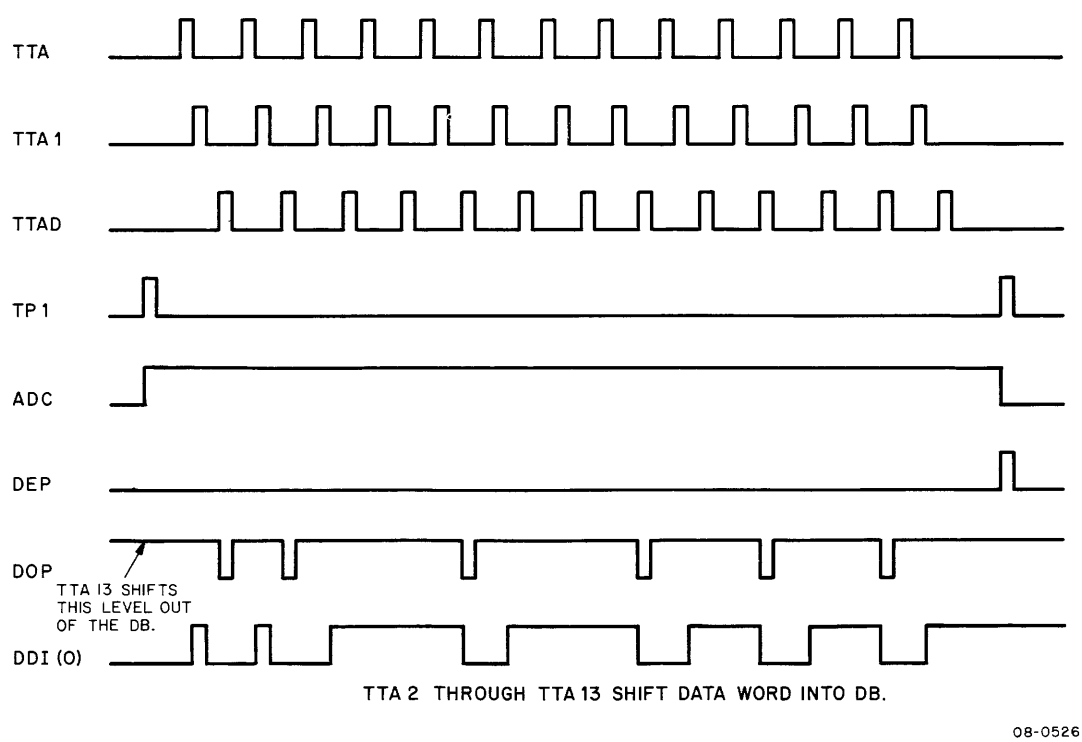


Figure 4-14 DB Loading of Data Word - Timing Diagram

In addition to providing a PER flip-flop clock pulse, the DEP sets the DBR flip-flop, which then requests a data break cycle from the computer. During the address word period following the DEP pulse, the BREAK signal sent by the computer enables the previously qualified B24 AND gates. The data word is transferred to the computer memory buffer. If the transfer involves more than one word, the search/transfer process is repeated until the last word of the block has been processed.

As noted in Paragraph 4.3.3, a write operation is terminated when the DEP pulse sets the TRC flip-flop. The same basic procedure is followed for a read operation; however, a significant difference is apparent upon examining Figure 4-15, which shows the termination of a read and a write operation, with the last data word location of each transfer represented by address 1001_8.

In the write operation, the data word corresponding to address 1001_8 is transferred from the computer memory buffer to the disk MB when the DMA and the TTB track are being compared (period 3 on Figure 4-15). This is the last word of the transfer; therefore, WCO is set during this period. When the DEP pulse is produced after period 4, the TRC flip-flop is set and operation ceases. However, in the read operation, the data word corresponding to 1001_8 is transferred from the disk MB to the computer memory buffer during period 5. This is the last word; therefore, WCO is set during this period. One additional DEP pulse, which is required to set the TRC flip-flop, is obtained at the end of period 6. Note that although the data word corresponding to address 1002_8 is placed in the disk MB, it is not transferred since a break request is not generated by the last DEP. If n words are transferred starting at address N, the DMA contains (N + n) at the conclusion of a write operation and (N + n + 1) at the conclusion of a read operation. For example: if the starting address is 1000 (N) and 5 (n) words are transferred, then the DMA contains 1005 for a write operation or 1006 for a read operation.

Another special procedure is necessary during a read operation when a block transfer ends with the data word represented by address 3777_8 of the data track 16 (the last word on the disk). The TRK INC signal generated after address 6000_8 causes an incrementation of the EMA register. If another disk is available, it is selected when the EMA is incremented. The new disk provides the extra DEP pulse that is required to set the TRC flip-flop for the read operation. If no other disk is available, the procedure in Figure 4-16 provides this DEP pulse. When the EMA is incremented, the nonexistent disk (NEX) signal is generated. TS3 of the break cycle sets the nonexistent disk (NED) flip-flop, which produces the needed DEP pulse. The TRC flip-flop is set by DEP and operation ceases.

4.3.5 Data Track Selection and Lock-Out Switches

The EMA register is loaded by the program with the disk and data track selection information. Specifically, EMA1 through EMA3, along with DMA0, select the data track, while EMA4 and EMA5 select the disk. Drawing DF32-DP-03, sheet 3, shows the disk head and matrix, the data track selection circuits, and the lock-out switches.

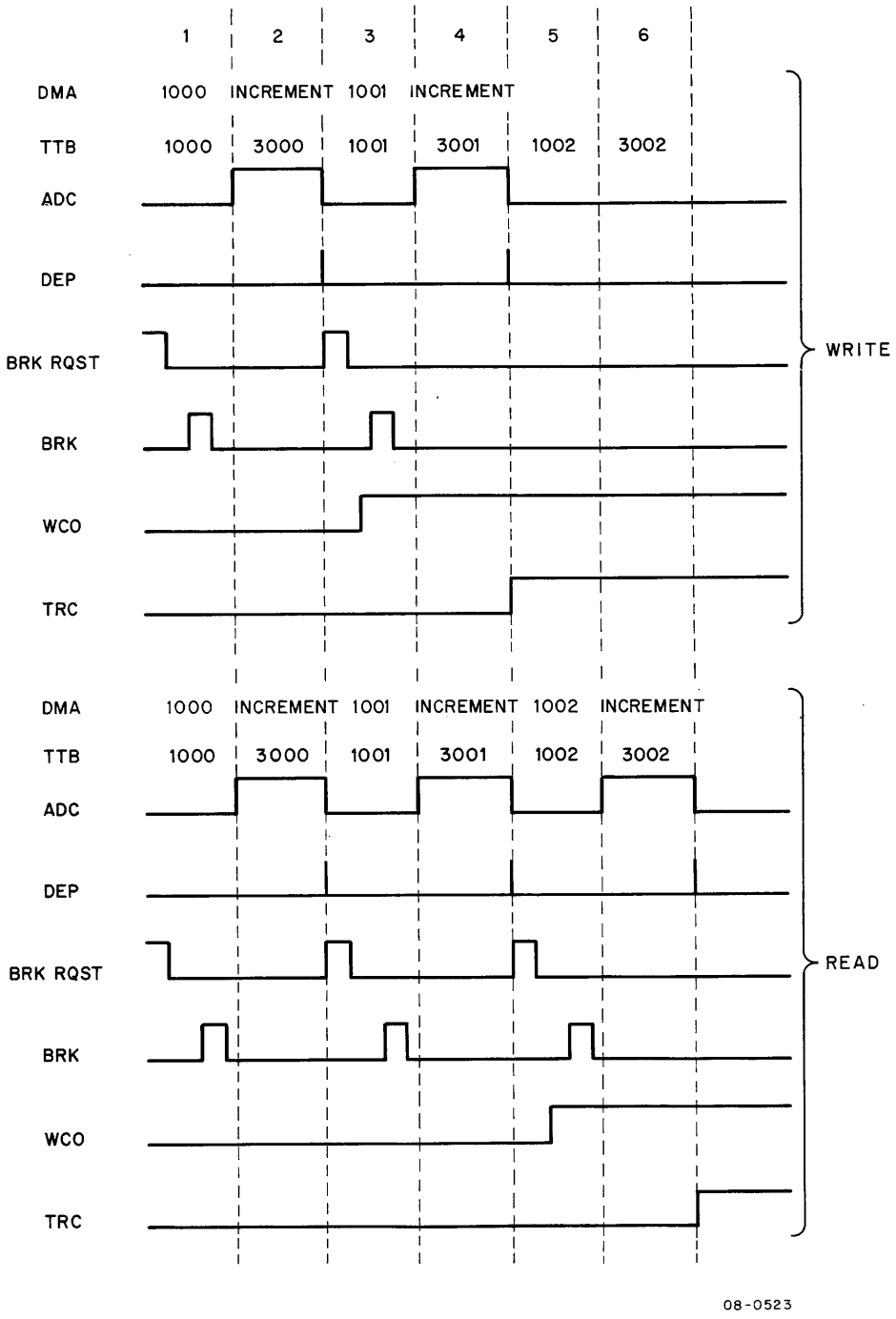


Figure 4-15 Read/Write Termination

The disk contains 16 data tracks. The 4-stage counter consisting of DMA0 (the LSB), EMA1, EMA2, and EMA3 (the MSB) (see Drawing DF32-DP-02) represent any 1 of the 16 tracks. For instance, the count 0000 represents data track one; 1000 represents data track nine. Note that the difference between these two numbers is the state of EMA3. DMA0, EMA1, and EMA2 select tracks 1 through 8 when EMA3 contains a 0, and tracks 9 through 16 when EMA3 contains a 1.

On Drawing DF32-DP-03, DMA0, EMA1, and EMA2 are applied to the A08 module, a binary-to-decimal decoder. The A08 module produces a signal on one of its eight output lines, which is applied to one of the center tap selector modules. This module provides a biasing signal for two recording heads. EMA3 will then select one of the two heads for recording. For example, assume that the count is 0011. This count is decoded and a signal is sent to A06, which provides bias for heads 3_8 and 13_8. EMA3 is a 0; therefore, NAND gate B18 produces a positive level at pin N1. This signal, applied through the series switch, selects head 3_8 for recording. Data track 4 is then recorded. If the count is 1011, head 13_8 is selected and track 12 is recorded.

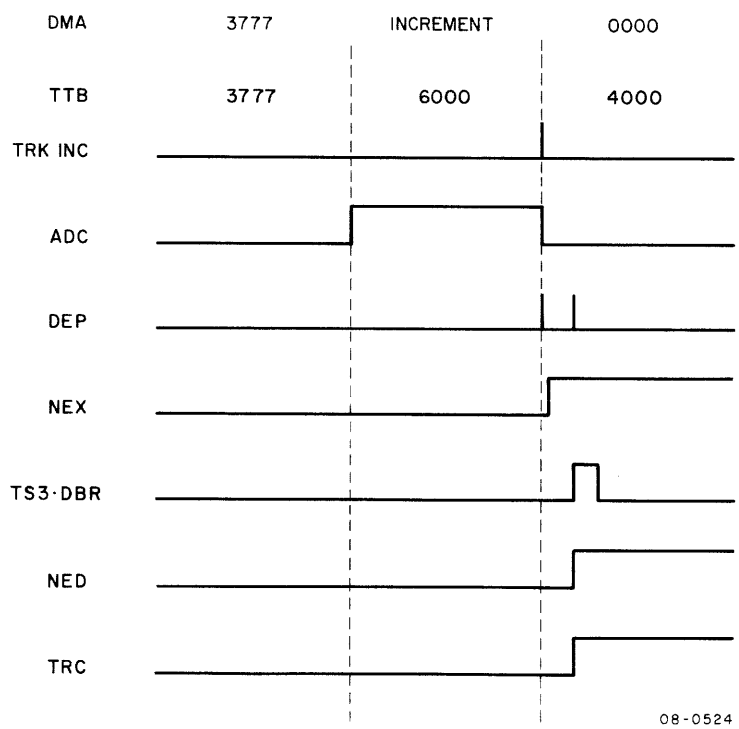


Figure 4-16 Last Word/Last Disk Timing Diagram

This method of track selection permits the write lock-out of either the upper (9 through 16) or the lower (1 through 8) data tracks (or upper and lower 16K word positions). To understand this write lock-out feature, the concept of disk selection must be understood. This concept is discussed in the following paragraphs.

As stated earlier, EMA bits 04 and 05 select either the DF32-D control unit or one of the DS32-D expander disks for a data transfer (see Figure 4-17). The binary count in EMA4 and EMA5 is decoded by a binary-to-decimal decoder to produce one of the following signals: EM0 through EM3. The particular EM signal produced by the decoder is applied to the UNIT SELECT switch of the control unit and each expander unit. The unit is selected as illustrated in Figure 4-17. If EM0 is decoded by A08, the control unit is selected for a data transfer (Figure 4-17). If EM1 is decoded, the expander disk is selected. If only these two disks are used, and EM3 is decoded, NEX is produced and the NED flip-flop is set to interrupt program operation.

In Drawing DF32-DP-03, locate the upper and lower write lock-out switches. When the switches are in the OFF position, the normal write operation is carried out. When either switch is in the

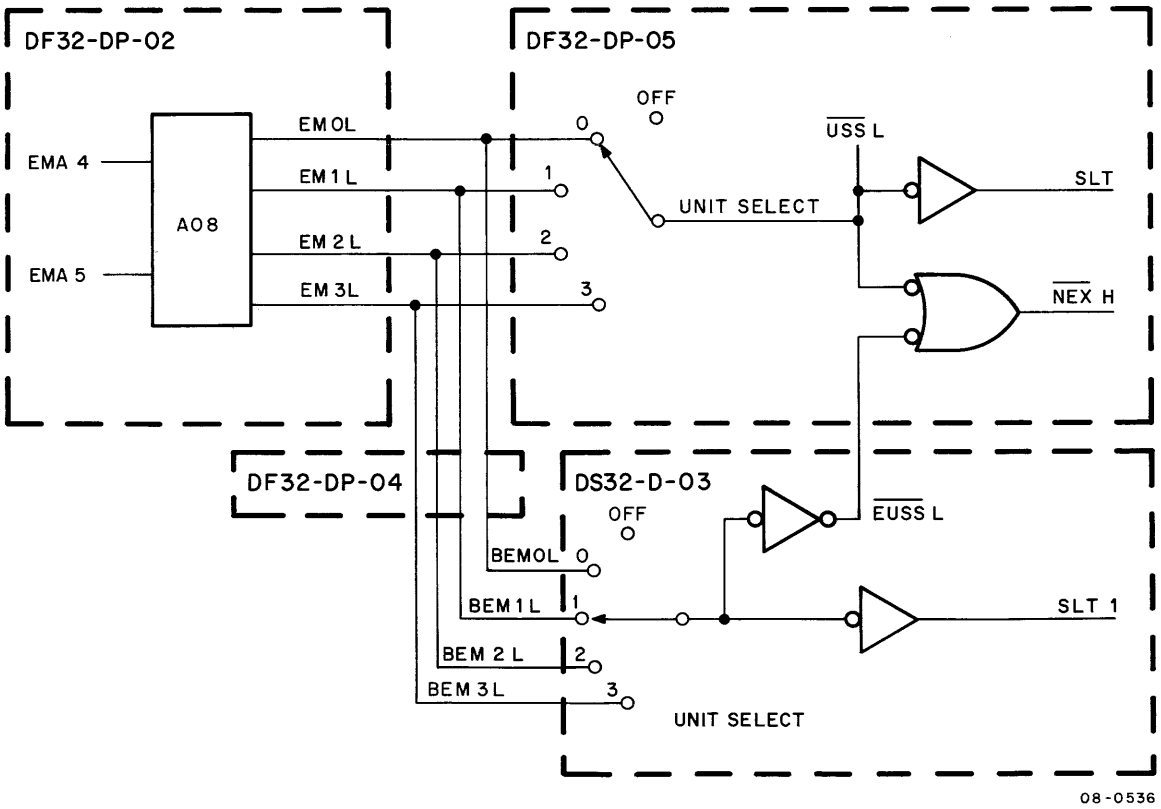


Figure 4-17 Unit Select Circuit

lock-out (ON) position, one of the B18 NAND gates is inhibited, if pin F1 of B10 is at a positive level, and if either the upper or lower 16K word positions are locked out. This last provision is met if the DISK LOCKOUT 0 switch is in the lock-out (ON) position (using the control disk as the selected unit). See Figure 4-18 for operation of the DISK LOCKOUT switches.

As another example, if EM1 has been decoded and the extender disk is to be locked out, the DISK LOCKOUT 1 switch must be set to the lock-out position. Lock-out of the extender is not possible with the conditions in Figure 4-18. Thus, the control unit determines which disk units are available for a write lock-out.

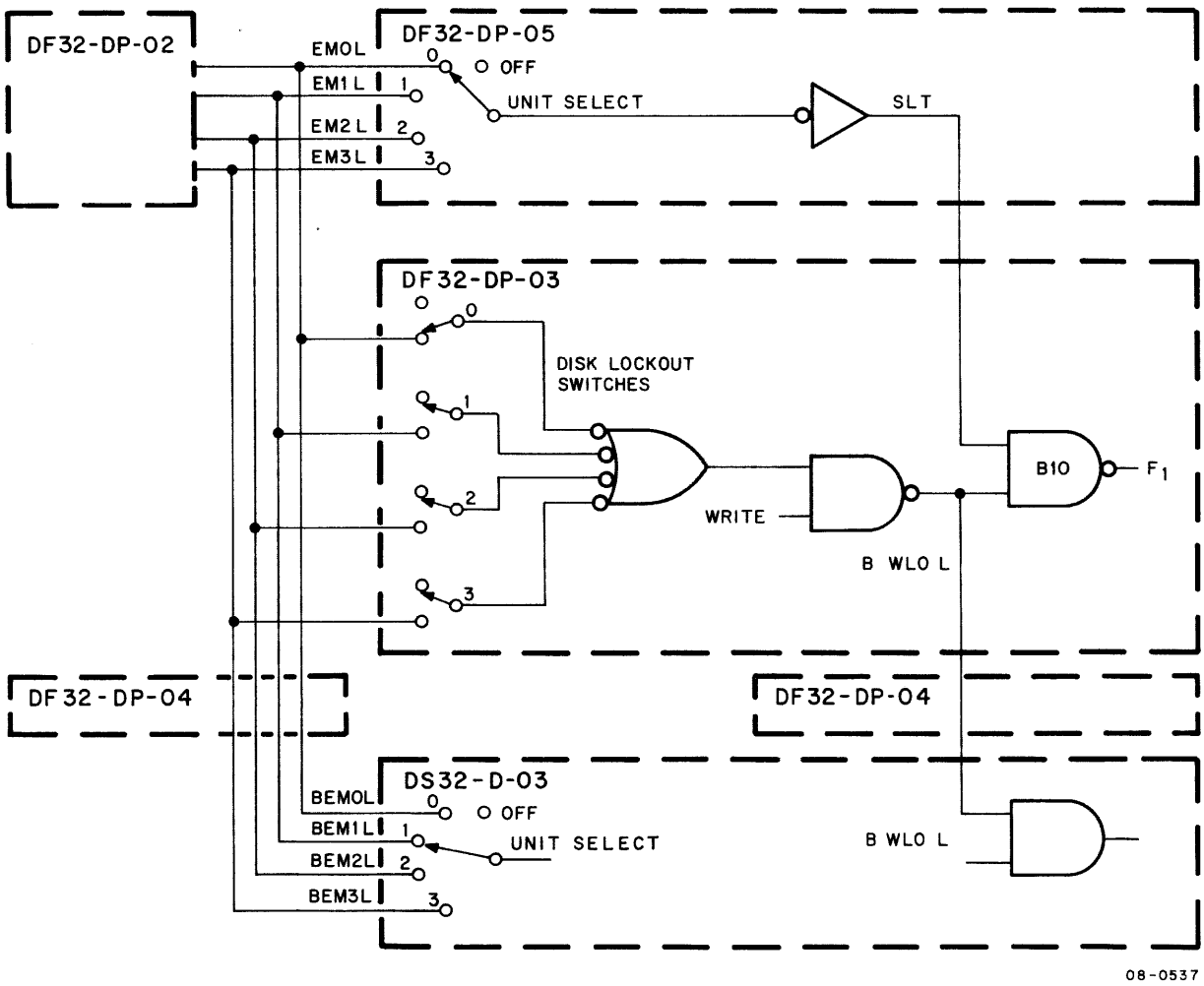


Figure 4-18 Lock-Out Select

4.3.6 Disk Expander Operation

Disks are selected for transfer as discussed in the previous section. In Drawing DS32-D-03, sheet 2, if disk number 1 is assigned to the extender, then subscript 1 mnemonics refer exclusively to this unit.

Thus, when signal EM1 is transferred to the UNIT SELECT switch SLT1 is produced. This signal is applied to NAND gates D14 (sheet 1). The TTA and TTB signals from the disk of this unit are thus transferred, as ETTAP and ETTBP, to the DF32-D where they control the read/write operation.

These two operations proceed as described for the DF32-D. The control unit transfers the B WRITE, B WFF, B ADC, and B WLO signals so the extender disk writer module can record the extender disk data tracks. DOP pulses produced by the extender amplifier and slice rectifier are transferred to the control unit for application to the DDI flip-flop.

4.3.7 Error Flags

Three error flags sensed by the IOT 6621 instruction are: parity error flag (PER), data request late flag (DRL), and write lock switch flag (either WIA, WIB, or EWL). The parity error flag occurs during the read operation and has been discussed. The DRL error flag is set by a DEP pulse when the DBR flip-flop is set. DBR is set if no address accepted signal is received from the computer. WIA is set when a write operation is attempted on the upper 16K word positions while these positions have been selected for lock-out. WIB indicates the same condition for the lower 16K word positions. The EWL flag is a combination of WIA and WIB flags from all disk expanders.

Chapter 5
Maintenance

5.1 GENERAL

The information in this chapter will help the user service the DF32-D Disk File and Control. Proper maintenance requires an understanding of the operation of the Disk File with the PDP-8, PDP-8/I, and PDP-8/L Processors. Maintenance procedures for these and other DEC products are contained in manuals and handbooks available from DEC (refer to Table 1-1).

5.2 PROCEDURE FOR CLEANING THE DISK AND HEADS

NOTE

The cleaning procedure should be performed in a controlled environment.

5.2.1 Preliminary Action

To prepare the disk and heads for cleaning, perform the following:

Step	Procedure
1	Turn off all power switches.
2	Pull the unit forward on the track slides.
3	Remove the top dust cover.

5.2.2 Disk Removal and Cleaning

To remove and clean the disk, perform the following:

Step	Procedure
1	Put on cotton or nylon gloves before handling the disk and heads and be careful when handling either.
2	Read completely each instruction step before performing the step.

Step	Procedure
3	To remove the four disk mounting screws, brace the disk gently with one hand so it does not turn. If the disk turns, it might wear on one or more of the heads, perhaps causing damage to head or disk.
4	When the screws have been removed, lift the disk from the hub.
	NOTE The disk surface that is on the top before the disk is removed must be on the top after the disk is replaced.
5	Place your hands on opposite edges of the disk (see Figure 5-1) and lift with a slight turning motion. Try not to tilt the disk while lifting. Place the disk on clean paper towels on a smooth surface. (Towels are supplied in the Potter cleaning solvent kit.)
6	To clean the disk surfaces, moisten a towel with cleaning solvent and wipe the surfaces. Then, cover the disk with a towel.

5.2.3 Head Cleaning

To clean the head shoes, perform the following:

Step	Procedure
1	The head shoes are mounted on gimbals. Support the gimbal unit gently with one hand (see Figure 5-2) and clean the head surfaces with a cotton swab dipped in magnetic head cleaning solvent.
2	Wipe the shoe surface with soft tissue paper to remove film.
3	Repeat the procedure for the remaining head shoes.

5.2.4 Disk Replacement

To replace the disk, perform the following:

Step	Procedure
1	Before replacing the disk, clean the top of the disk table with a paper towel moistened with cleaning solvent. Try not to hit any of the shoe/gimbal units.
2	Hold the disk as instructed in the removal operation and replace it on the hub. Try not to tilt the disk while letting it down on the hub.
3	Turn down, but do not tighten, the four mounting screws.
4	Use the following procedure to center the disk on the hub. a. Insert strips of paper between the hub and disk at three points equally spaced around the circumference of the hub With a screwdriver, tighten the screws while bracing the disk so that it will not turn.

Step	Procedure
4 (Cont)	b. With all four screws snug, place a pencil, eraser down, on the table very close to the outside edge of the disk. Closely watch the clearance between the pencil and the disk while you rotate the disk by hand in a clockwise direction.
	c. If the gap appears to remain constant, remove the paper and tighten the four mounting screws, taking care that the disk does not rotate while the screws are being tightened.

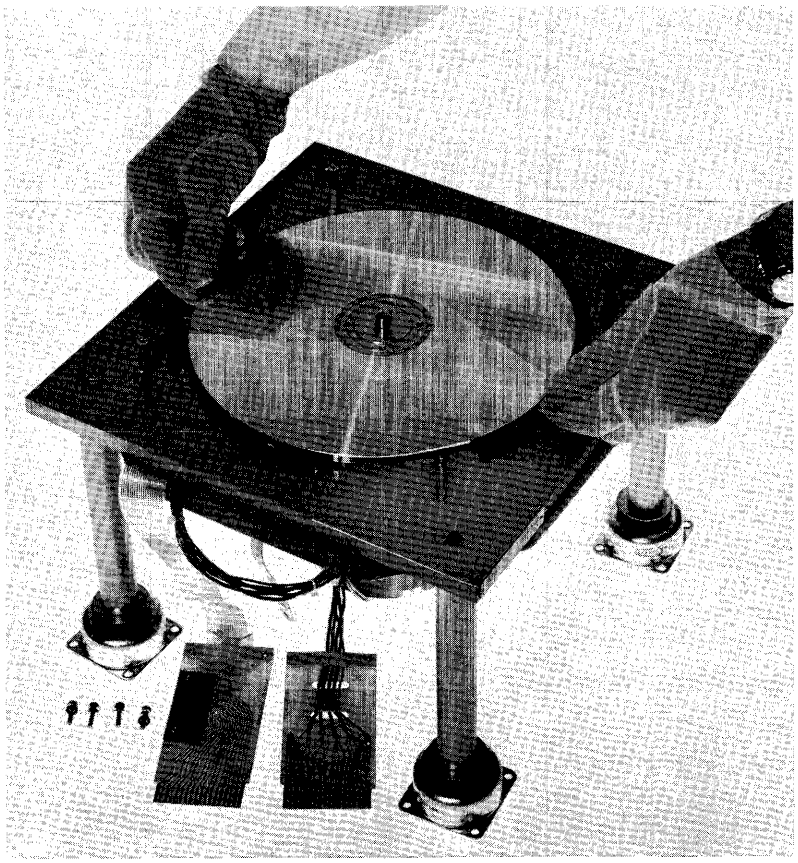


Figure 5-1 Disk Removal

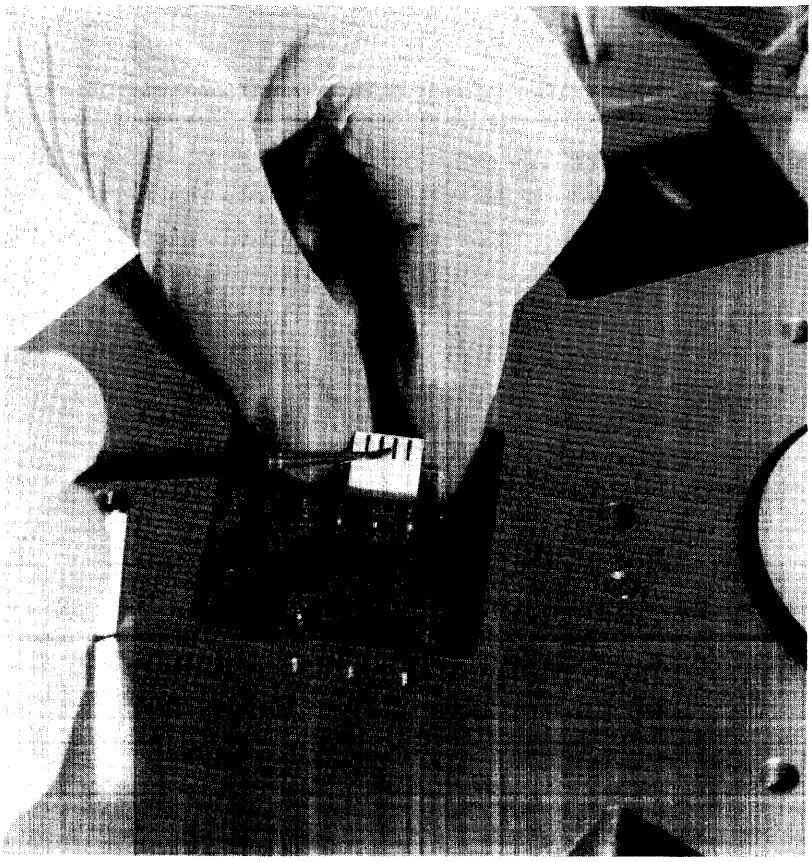


Figure 5-2 Head Cleaning

5.2.5 Final Check

When the procedures above have been accomplished, perform the following:

Step	Procedure
1	Clean the inside of the top dust cover with a paper towel moistened with cleaning solvent. Replace the cover and check that the seal is tight.
2	Turn on the motor and listen for any unusual sound. If an unusual sound is detected, turn off the motor and check the physical alignment of the disk and heads.
3	Slide the unit back into the cabinet.

5.3 ADJUSTMENTS

The DF32-D/DS32-D adjustments are performed on the G085 modules (read amplifier and slice rectifier). Three such modules are used in the DF32-D and in each DS32-D. One module converts the disk TTA track recorded flux pattern into TTA pulses; another converts the TTB track flux pattern into TTB pulses; the third converts the flux pattern of the data tracks into data pulses. To ensure that the TTA, TTB, and data pulses are correctly shaped, two adjustments must be made on each G085.

NOTE

The adjustment procedure that follows is for a typical disk. Each disk has different electromechanical characteristics; therefore, the voltage and slice levels may vary slightly from those given in the adjustment procedure. These variations are specified in the Disk Identification Margin Sheet supplied with the system.

Refer to Drawing C-CS-G085-0-1, Section 6. Locate pins AU and AT on the collectors of Q5 and Q7, respectively. These pins are the outputs of the amplifier portion of the module (AU being the inverse of the signal at AT). The output signal at AT is represented in Figure 5-3. Locate pins BE and BD on the collectors of Q15/Q17 and Q14/Q16, respectively. These pins are the outputs of the slice rectifier portion of the module (BE being the inverse of the signal at BD). The output signal at BD is represented in Figure 5-4. The adjustments affect, first, the peak-to-peak voltage of the waveform in Figure 5-3, and, second, the pulse width of the waveform in Figure 5-4. The adjustment procedure follows:

Step	Procedure
1	If the adjustment is made in the DF32-D, A,B30 and A,B31 are the TTA and TTB modules, respectively; A,B1 is the data module. If the DS32-D modules are adjusted, C,D22 and C,D23 produce TTA and TTB, respectively; C,D17 produces data.
2	The TTA and TTB modules must be adjusted before the data modules. Either TTA or TTB may be adjusted first; the procedure is the same for each.
3	Release the captive screws on the front panel of the disk unit and tilt the panel, exposing the logic modules. Locate the desired G085 module.
4	Each G085 contains two 500-ohm potentiometers, which are accessible from the rear of the module deck. The upper potentiometer, R21, of the module affects the peak-to-peak voltage, while the lower potentiometer, R32, affects the slice threshold and thus the pulse width. The upper potentiometer must be adjusted first.

Step	Procedure
5	Connect a vertical input of an oscilloscope (Tektronix Type 545, or equivalent, equipped with a dual-trace plug-in module) to pin AT2 (CT2)* of the module connector. The waveform should resemble that of Figure 5-3.
6	Adjust R21 to obtain a peak-to-peak amplitude of 10V.
7	Connect the second vertical input of the oscilloscope to pin BD2 (DD2). Ensure that the oscilloscope vertical input polarity switches are set to positive polarity. The waveform at BD2 (DD2) should resemble that of Figure 5-4.
8	Adjust R32 until the duration of the negative pulse is 600 ns.
	NOTE If you cannot make this adjustment, or the one in Step 10, ground pins BS2, BT2, BU2, and BV2 (DS2, DT2, DU2, and DV2). Do not remove the grounds when finished with the adjustments.
9	Using the polarity switch, invert the polarity of this pulse.
10	Using the vertical positioning controls, align the two waveforms as shown in Figure 5-5. The slice level, represented by "a", should be a minimum of 2V.
11	If "a" is less than 2V, make it exactly 2V by readjusting R32. This will decrease the duration of the pulse. A 10 percent decrease is acceptable.
12	Remove the oscilloscope lead from pin AT2 (CT2) and connect it to A18, pin D2 (C11, pin D1). Remove the lead from pin BD2 (DD2) and connect it to A18, pin B1 (C11, pin E1). Use the vertical positioning controls to align the waveforms as shown in Figure 5-6. The positive pulses are TTA pulses, the negative are TTB pulses. Verify that the values of t and T are as noted in Figure 5-6.
13	After TTA and TTB have been adjusted, verify that the address test of the disk data diagnostic is satisfactorily performed. If it is not, recheck the waveforms and, if necessary, proceed to the troubleshooting section.
14	If Step 13 is completed satisfactorily, use the disk data diagnostic to provide all 1s on the data tracks. Adjust the data G085 module by repeating Steps 3 through 7. When Step 7 is completed, return to Step 15.
15	Adjust R32 until the duration of the negative pulse is 500 ns.
	NOTE If you cannot make this adjustment, ground pins BS2, BT2, BU2, and BV2 (DS2, DT2, DU2, and DV2). Do not remove the grounds when finished with the adjustment.

*DS32-D connections are indicated in parentheses.

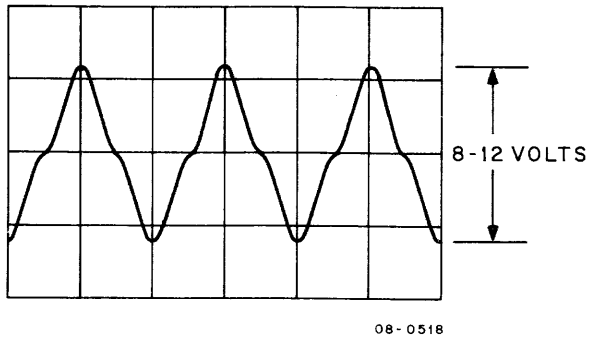


Figure 5-3 Output Signal at Pin AT (CT)

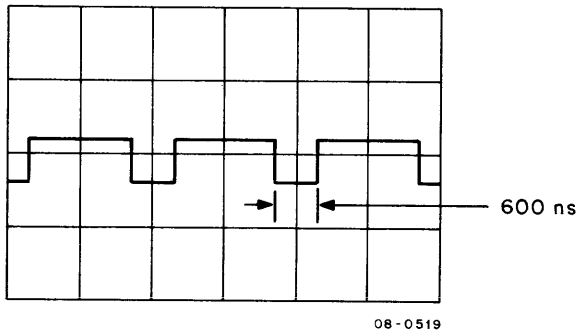


Figure 5-4 Output Signal at Pin BD (DD)

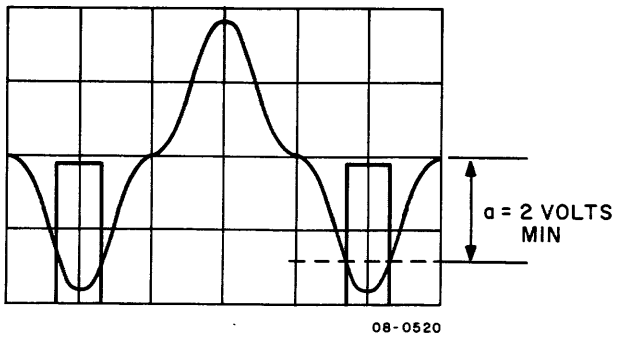


Figure 5-5 Slice Level Obtained by Combining Outputs from Pins (CT) AT and (DD) BD

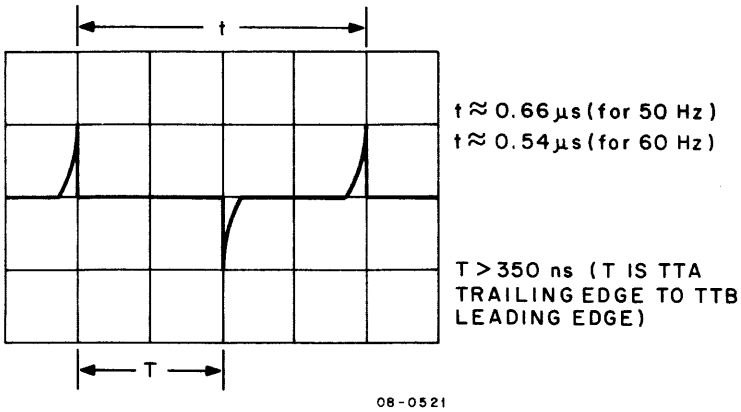


Figure 5-6 TTA and TTB Pulses

Step	Procedure
16	Repeat Steps 9, 10, and 11.

NOTE

If you cannot make the adjustment in Step 10, ground pins BS2, BT2, BU2, and BV2 (DS2, DT2, DU2, and DV2). Do not remove the grounds when finished with the adjustment.

17 Remove the lead from pin AT2 (CT2) and connect it to B08, pin J1 (D15, pin J1), the TTAD pulse, which strobes the data pulse. Align the two waveforms and measure t_d. See Figure 5-7 for a representation of these waveforms. Verify that t_d is 500 to 600 ns.

NOTE

If the disk unit is the DF32-D, there is no adjustment for t_d. Refer to Paragraph 5.4 if difficulty is encountered. If the disk unit is the DS32-D, additional delay may be selected, in 50-ns steps, to achieve the required delay. (See note 3 of Drawing D-BS-DS32-D-03, sheet 1.)

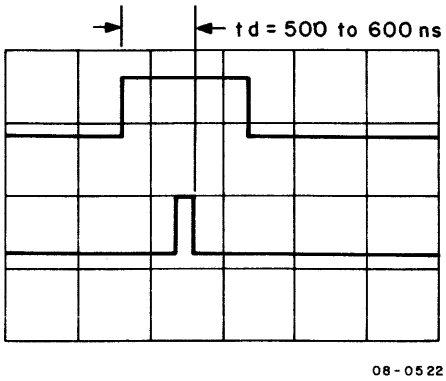


Figure 5-7 TTAD Pulse and Associated Data Pulse

5.4 TROUBLESHOOTING

The following list of potential failures will help to isolate malfunctions in the disk/logic.

1. If an error typeout indicates one address failure within the whole disk, the following possible conclusions can be drawn:
   a. A spot on the disk surface is beginning to corrode.
   b. The data read preamp output has dropped marginally enough to pick up this address failure.
   c. The head flying characteristics have changed.
   d. The write current has deteriorated.
   e. Dust or other surface contamination of the disk has occurred in one small spot.
2. When a series of address failures appear relative to the disk position, the following possible conclusions can be drawn:
   a. A scratch has appeared on the disk.
   b. Either the timing or address track has been destroyed at this point on the disk.
   c. A large area of contamination has occurred.
   d. The timing or address track preamps have deteriorated.
   e. The timing address head has changed aerodynamically.
   f. A SAP failure has occurred.
3. When any particular address on all data tracks fails relative to a certain position on the address track or the data words in four tracks near this address fail, the following conclusions may be drawn:
   a. A scratch has appeared on the disk.
   b. Timing relationships have changed on the timing and address tracks from write to read.
   c. A disk coating variation is apparent.
   d. Address search logic (CARRY, shift register DMA) fails for this address possibly due to timing TTA, TTB variation.
4. When a series of data words fails relative to a particular track, the following conclusions can be drawn:
   a. The flying characteristics of the shoe pad associated with the addressed track are unstable.
   b. The head involved has different playback characteristics than the others within the shoe or system.
   c. A surface scratch has appeared only under this track.
   d. The data read amplifier acceptance level is marginal for this track.
   e. The combination of low amplitude playback and surface contamination causes track failure.

f. The data strobe window pulse is not centered to the peaks of the playback signal on the track.

g. The power supply level has dropped.

5. When nonconsecutive addresses fail, but do not repeatedly fail, it is considered a random address failure and the following conclusions can be drawn:

   a. A dust speck appeared instantaneously.

   b. The disk and head assemblies received a momentary shock or vibration.

   c. A line transient is causing either electrostatic or electromagnetic fields.

   d. A poor connection exists in the logic system.

   e. A circuit component has deteriorated to the marginal point.

   f. Assuming all random data is stored, a worst case pattern exists during playback causing a marginal failure.

   g. TRK, INC generated for an address other than address 4000 on the disk, is randomly causing partial selection of the next track.

6. When a data failure follows a certain pattern, the following conclusions may be drawn:

   a. The head to disk flying characteristics have changed causing a drop in head resolution.

   b. The disk surface is dirty.

   c. Cabling, the head, or read preamp have changed characteristics.

   d. Deterioration of the read amplifiers for only the data track is causing a drop of bits.

   e. The data strobe delay is not centered over the playback peaks.

   f. The data buffering logic is sensitive to a certain pattern of data.

   g. Data surface wear is causing data dropouts.

7. When the disk logic hangs in a loop looking for an address, the following conclusions may be drawn:

   a. A portion of the timing or address track is erased.

   b. The amplitude adjustment of TTA/TTB is not correct.

   c. The timing relationship between TTA and TTB is such that a particular address cannot be found. TTA- to TTB-gap should normally be increased.

   d. A logic failure is apparent either in the address register or the associated control logic.

8. When addressing works well, but data errors are considerable, the following conclusions may be drawn:

   a. One of the matrix circuits is failing.

   b. The data preamp or rectifying slicer circuits are failing.

   c. Poor write current rise time is causing poor playback signals.

   d. There is an aerodynamic failure in the head-to disk-relationship.

e. There is a complete lack of data playback due to a short or open circuit in the read/write logic.

9. When data parity errors (but no data errors) appear, the following conclusions may be drawn:

   a. The write flip-flop and associated clear logic is faulty.

   b. The read parity detection logic is not complementing correctly.

   c. At parity strobe time, a data signal noise bit is detected.

   d. The timing strobe for the parity bit is offset due to a poor resolution head causing peak shift.

10. Disk Head Alignment

    If failures occur during readcheck, but not during the read-after-write, there may be an overlap of tracks on the disk.

    a. The all 1s data test in the Disk Data Program is used to detect an overlay of tracks by comparing the readcheck with the read-after-write, while observing the output of the data amplifier. For example, assume that head 11 is misaligned beneath track 7. The all 1s data test yields the following analysis: each read-after-write appears good until track 7 is written; as track 7 is written, the previous history is seen to be the result of track 11; when track 7 is completely written with 1s, the read cycle playback is good; the same signal envelope, which resembles extremely low amplitude signals resulting from electrical noise, appears when track 11 is written; the read cycle playback of track 11 is also good; the readcheck of track 7 shows that no signal is present or that an out-of-phase signal, created by track 11, has been added to the signal written on track 7; track 11 readcheck shows that this track is operational.

    b. Three possible failures are associated with the preceding analysis. First, the matrix selection circuits in the logic could have failed. The light-board test can isolate or eliminate this possibility. Second, a short circuit or an open connection could have developed in the head and matrix cable connecting the logic to the disk. The matrix-head cable tester can be used to isolate or eliminate this possibility. Third, pad 4 could be misaligned. This possibility can be isolated or eliminated by using a program that writes the address of each track on that particular track, and then reads back each track. If the ADC flip-flop is used as the synchronizing point, an observer can readily determine if an overlay of tracks exists.

5.5 MODULE LIST

All DEC module types used in the DF32-D are listed in Table 5-1. One module of each type, stocked as a spare, helps minimize equipment downtime.

Table 5-1
Module List

Module Name	Type Number
Disk read amplifier and slice rectifier	G085
Disk writer	G294
Series switch	G295
Center tap selector	G296
15 loads	M002
Inverter	M111
NOR gates	M112
NAND gates	M113
NAND gates	M117
AND/NOR gates	M121
Gate module	M160
Dual binary-to-decimal decoder	M163
D flip-flops	M205
Flip-flops	M206
Shift register	M233
Delay line	M310
Negative input converter	M506
Pulse generator	M602
NOR buffers	M617
Bus driver	M624
Bus data interface*	M101
Device selector*	M103
Bus drivers*	M623
Bus data interface†	M100
Device selector†	M102
Bus drivers†	M633
Clamped loads†	W005

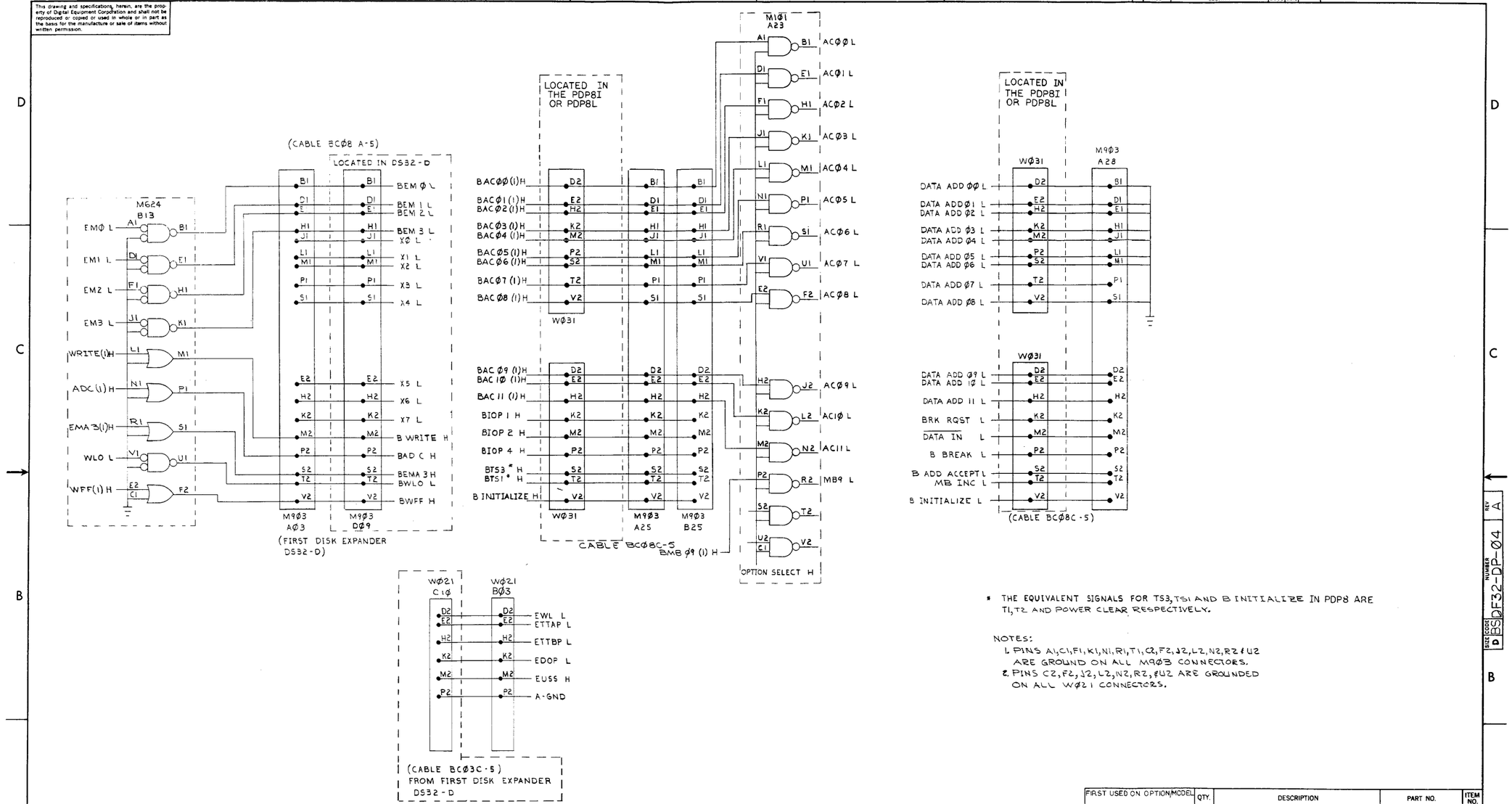
*Used only in positive bus unit (DF32-DP,EP).
†Used only in negative bus unit (DF32-DN,EN).

Chapter 6
Engineering Drawings

The following engineering drawings and circuit schematics are necessary for understanding and maintaining the DF32-D, E Disk File and Control and the DS32-D, E Disk Extender.

Drawing No.	Revision	Title	Page No.
D-BS-DF32-DP-04	A	Interface (3 sheets)	6-3
D-BS-DF32-DN-04		Interface (3 sheets)	6-9
D-BS-DF32-DP-05	A	Disk Control (3 sheets)	6-15
D-BS-DF32-DP-02	A	Disk Memory and Address Search (2 sheets)	6-21
D-BS-DF32-DP-03	A	Data Logic and Head Matrix (3 sheets)	6-25
D-MU-DF32-DP-06	A	Module Utilization	6-31
D-MU-DF32-DN-06	A	Module Utilization	6-33
D-BS-DS32-D-03		Disk Expander (2 sheets)	6-35
D-MU-DS32-D-02		Module Utilization	6-39
C-CS-G085-0-1	D	Disk Read Amplifier and Slice Rectifier	6-41
B-CS-G294-0-1	A	Disk Writer	6-42
B-CS-G295-0-1		Series Switch	6-42
B-CS-G296-0-1	A	Center Tap Selector	6-43
B-CS-M233-0-1		Disk Shift Register	6-43

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



* THE EQUIVALENT SIGNALS FOR TS3, TS1 AND B INITIALIZE IN PDP8 ARE T1, T2 AND POWER CLEAR RESPECTIVELY.

NOTES:

1. PINS A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2 & U2 ARE GROUND ON ALL M9Ø3 CONNECTORS.
2. PINS C2, F2, J2, L2, N2, R2, & U2 ARE GROUNDED ON ALL WØ21 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.		DATE 11-8-69
CHK'D.		DATE 1-20-70
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE 1-28-70

NEXT HIGHER ASSY. A-ML-DF32-DP/EP

SCALE NONE

SHEET 1 OF 3

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE INTERFACE

SIZE	CODE	NUMBER	REV.
D	BS	DF32-DP-Ø4	A

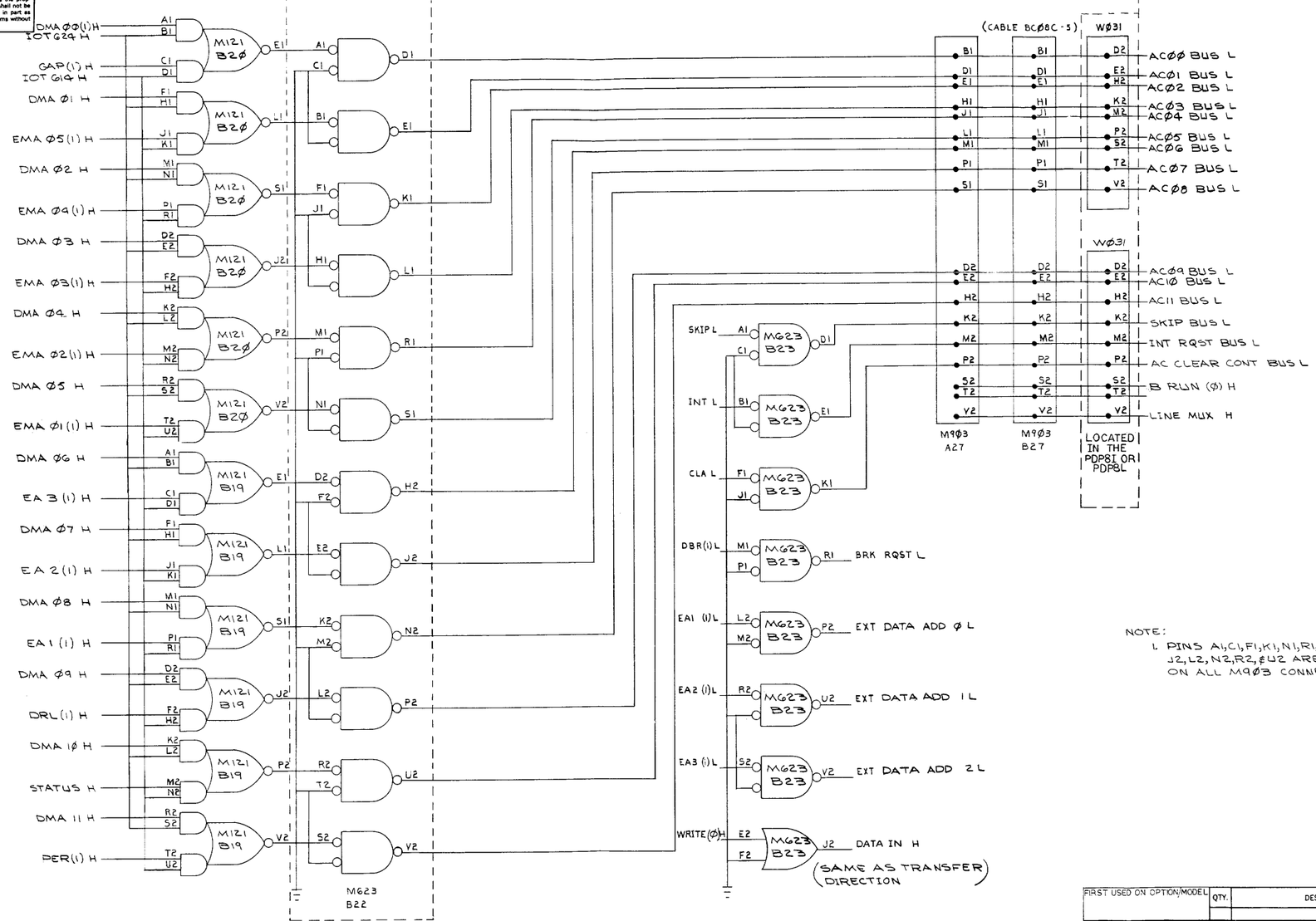
DIST.

REVISIONS

CHK	CHANGE NO.	REV

DEC FORM NO ORD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



NOTE:
1. PINS A1,C1,F1,K1,N1,R1,T1,C2, F2, J2,L2,N2,R2,&U2 ARE GROUNDED ON ALL M9Ø3 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. F. Green DATE 11-10-69
CHK'D. DATE 1-22-70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 1-22-70

NEXT HIGHER ASSY A-ML-DF32-DP/EP
SCALE NONE
SHEET 2 OF 3

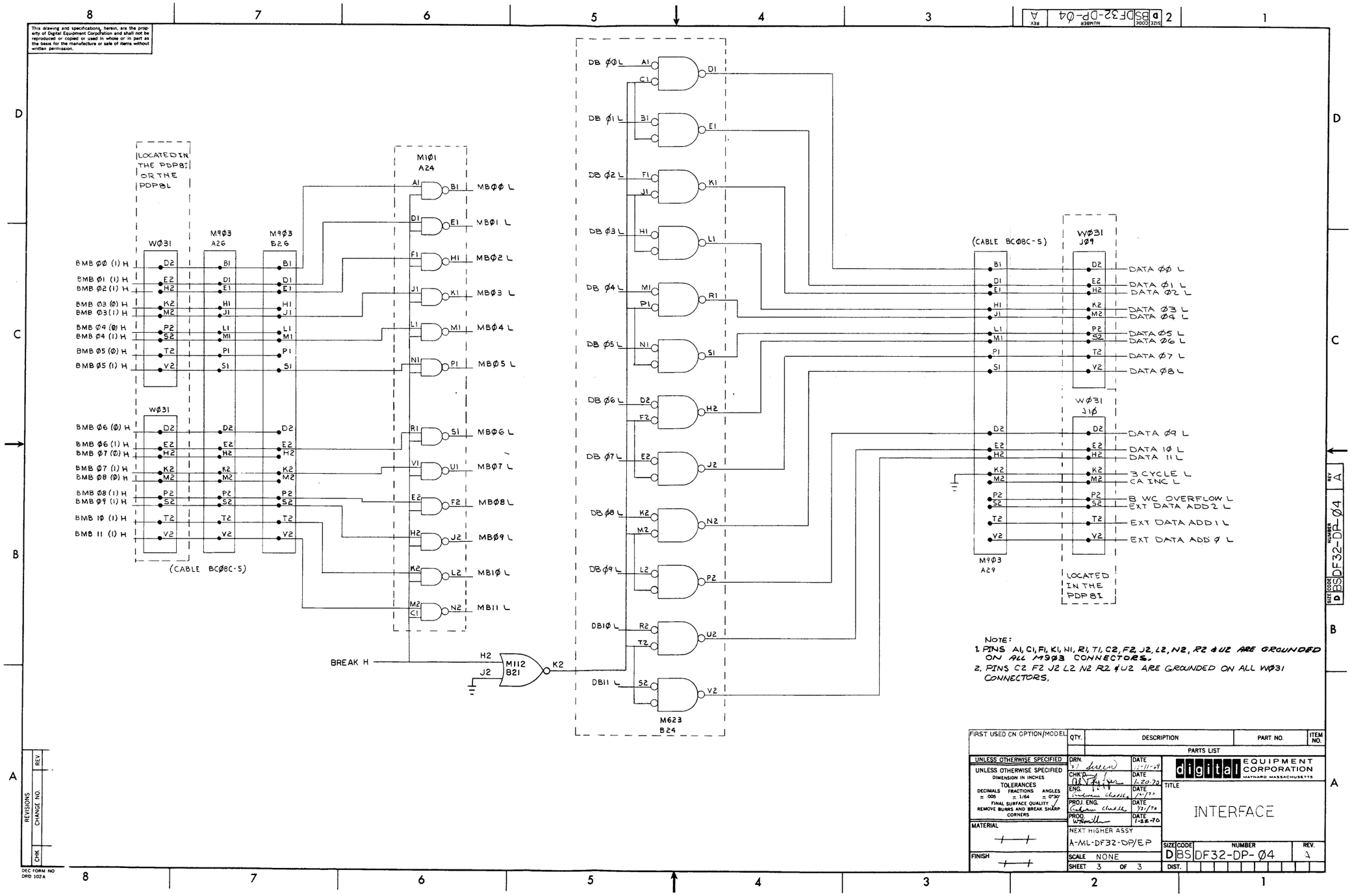
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE INTERFACE

SIZE D CODE BS NUMBER DF32-DP-Ø4 REV. A
DIST.

REVISIONS REV. CHANGE NO. CHK

DEC FORM NO DRD 102A



NOTE:
1. PINS A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2 & U2 ARE GROUNDED ON ALL M903 CONNECTORS.
2. PINS C2 F2 J2 L2 N2 R2 & U2 ARE GROUNDED ON ALL W031 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. [signature] DATE 11-11-69
CHK'D. [signature] DATE 1-20-70
ENG. [signature] DATE 1/21/70
PROJ. ENG. [signature] DATE 1/21/70
PROD. [signature] DATE 1-22-70

NEXT HIGHER ASSY A-ML-DF32-DP/EP
SCALE NONE
SHEET 3 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE INTERFACE

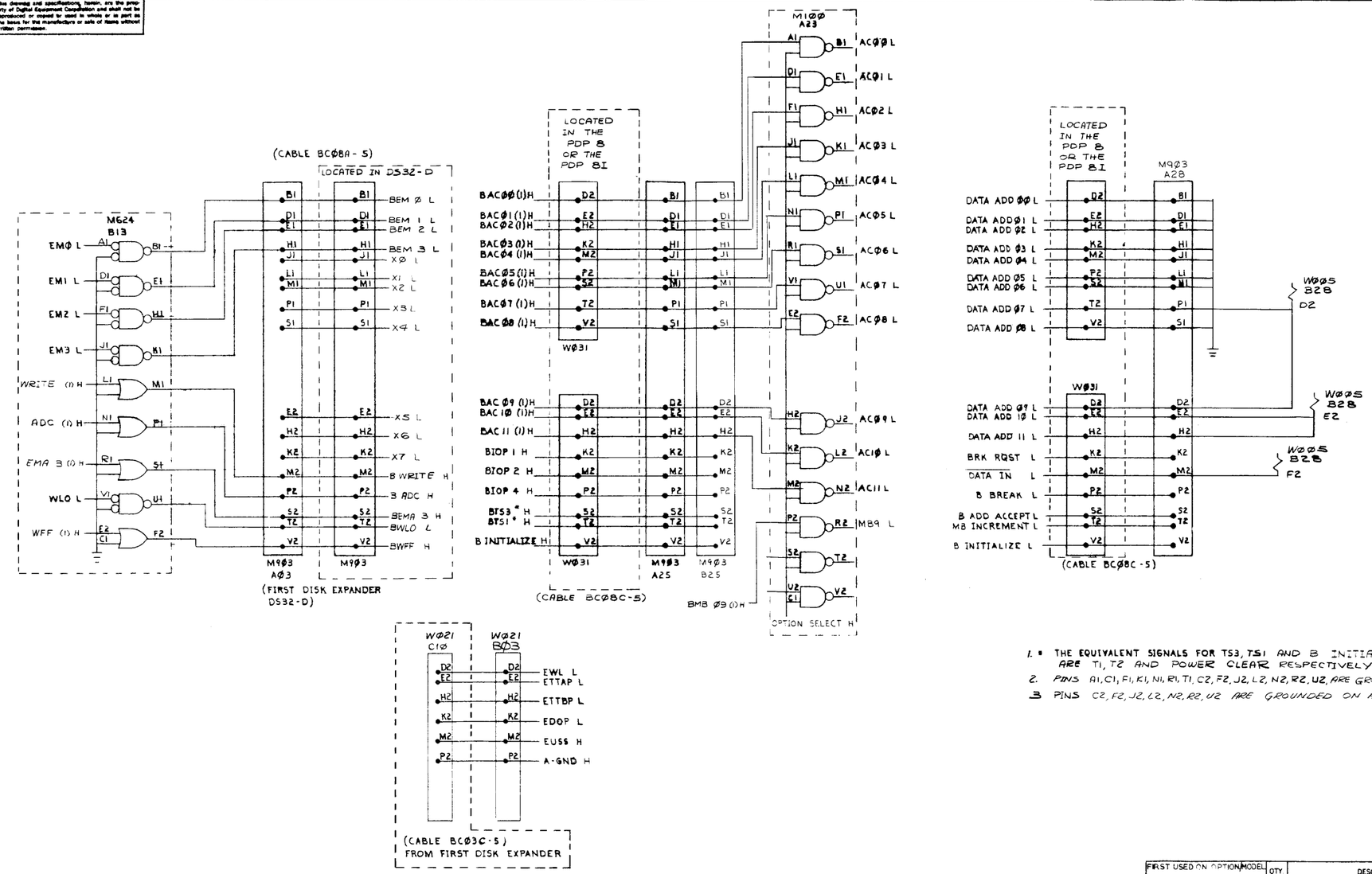
SIZE D CODE BS NUMBER DF32-DP-04 REV. A
DIST.

REVISIONS CHANGE NO. REV CHK

DEC FORM NO DRD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



1. * THE EQUIVALENT SIGNALS FOR TS3, TS1 AND B INITIALIZE IN PDP 8 ARE T1, T2 AND POWER CLEAR RESPECTIVELY.
2. PINS A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, U2, ARE GROUNDED ON ALL M9Ø3 CONNECTORS.
3. PINS C2, F2, J2, L2, N2, R2, U2 ARE GROUNDED ON ALL WØ21 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. Green DATE 11-5-69
CHK'D DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE

NEXT HIGHER ASSY. A-ML-DF32-DN/EN
SCALE NONE
SHEET 1 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE INTERFACE

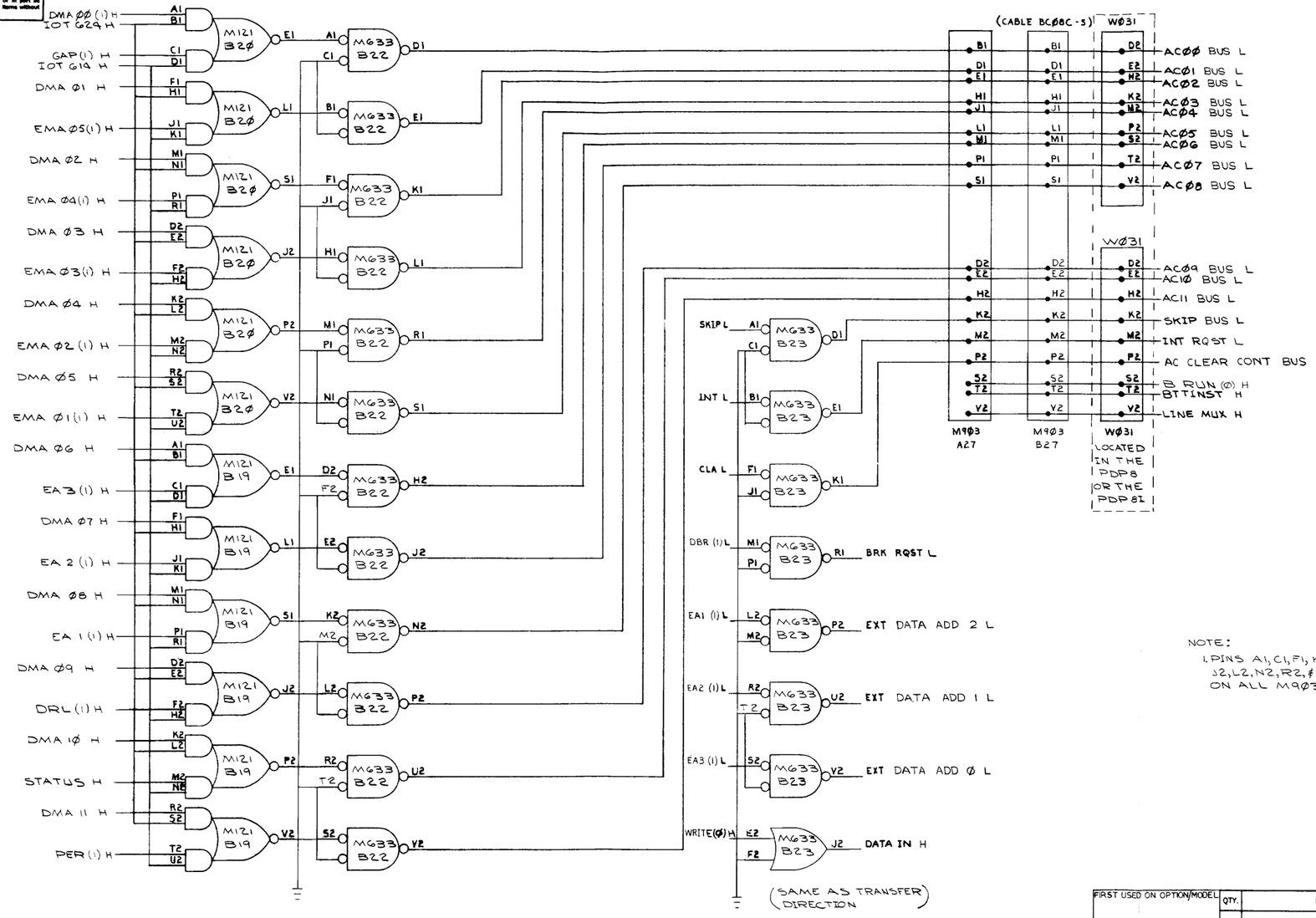
SIZE CODE D NUMBER BS DF32-DN-Ø4 REV.
DIST.

REVISIONS REV. CHANGE NO. CHK

DEC FORM NO DRD 102A

SIZE CODE D BS NUMBER DF32-DN-Ø4 REV A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



NOTE:
1. PINS A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, & U2 ARE GROUNDED ON ALL M9Ø3 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. DATE
CHK'D DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE

NEXT HIGHER ASSY A-ML-DF32-DN/EN

SCALE NONE
SHEET 2 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

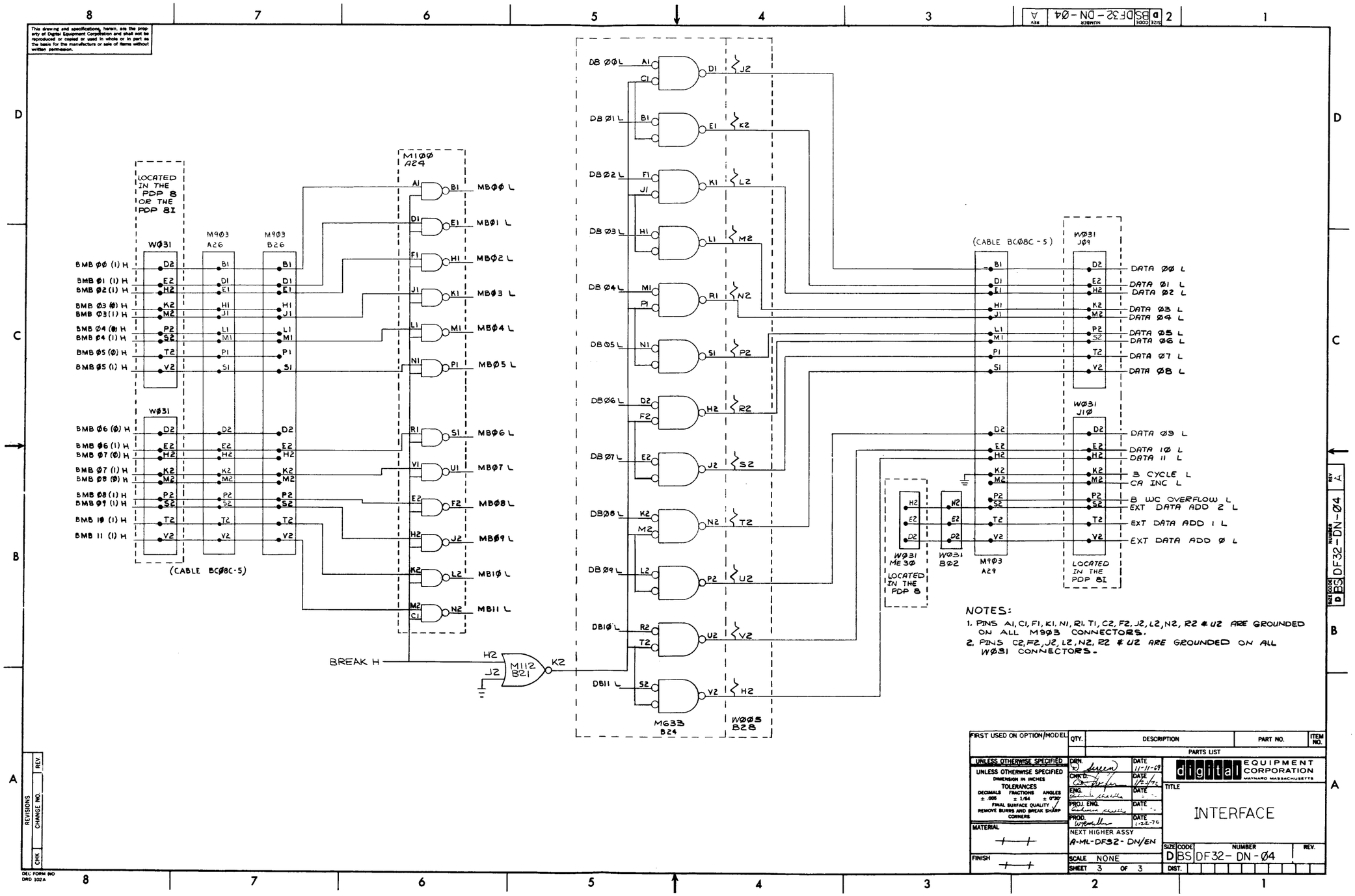
TITLE INTERFACE

SIZE D CODE BS NUMBER DF32-DN-Ø4 REV

DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO DRD 102 A



NOTES:

1. PINS A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2 & U2 ARE GROUNDED ON ALL M903 CONNECTORS.
2. PINS C2, F2, J2, L2, N2, R2 & U2 ARE GROUNDED ON ALL W031 CONNECTORS.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. DATE 11-11-69
CHK'D. DATE 1/22/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 1-22-70

NEXT HIGHER ASSY
A-ML-DF32-DN/EN

SCALE NONE
SHEET 3 OF 3

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

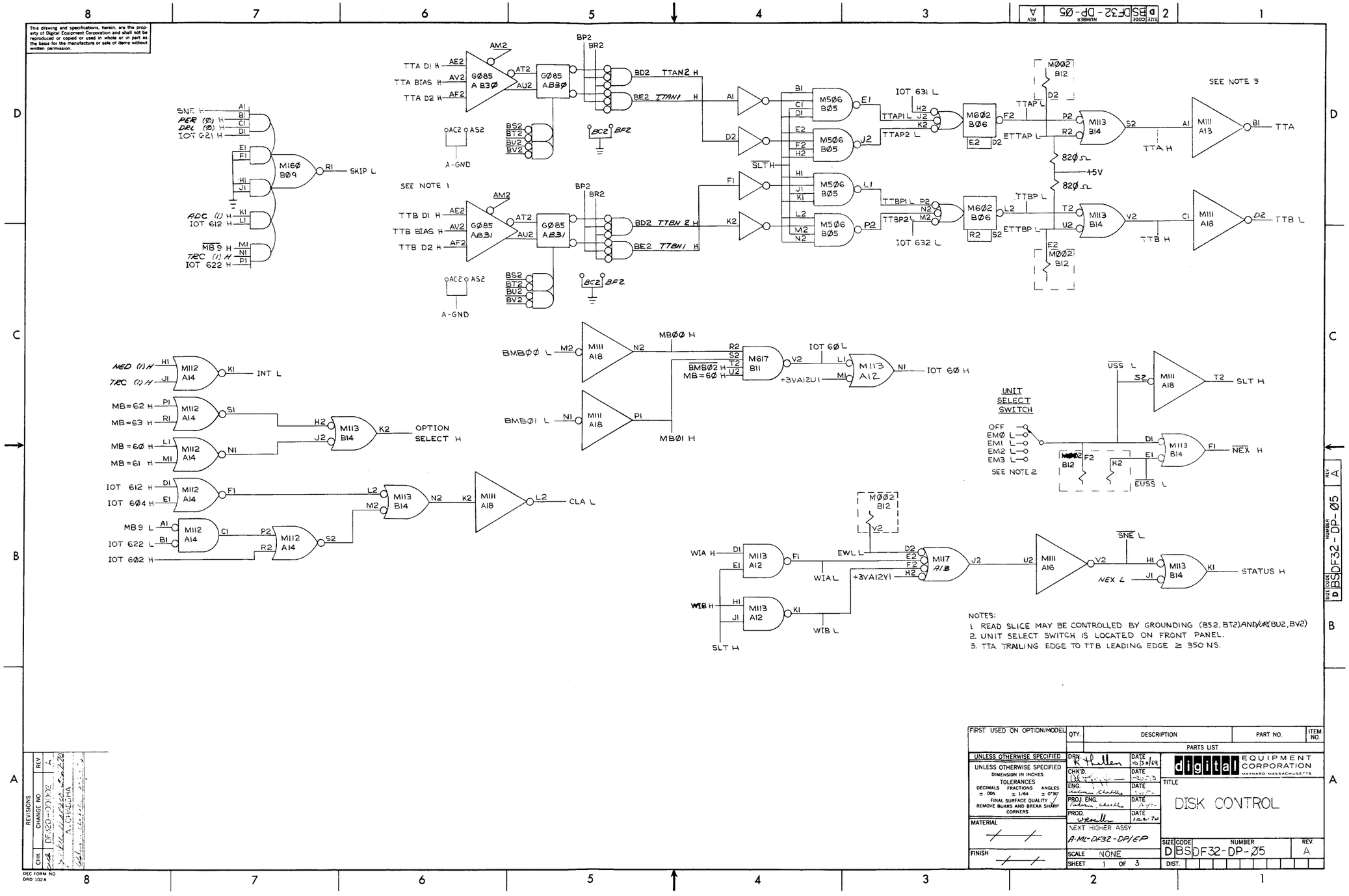
TITLE
INTERFACE

SIZE D CODE BS NUMBER DF32-DN-04 REV.

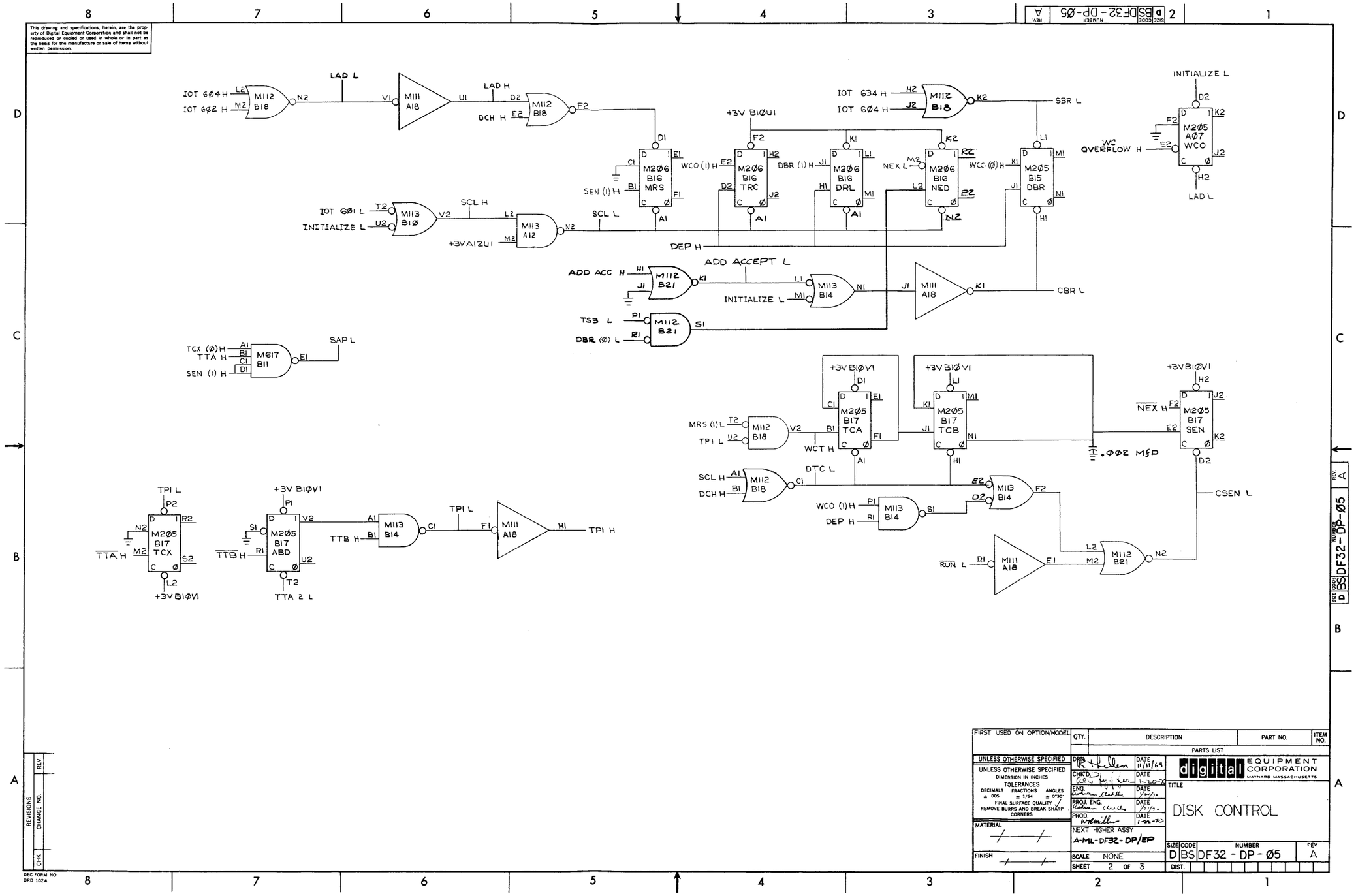
DIST.

REVISIONS
CHK CHANGE NO. REV.

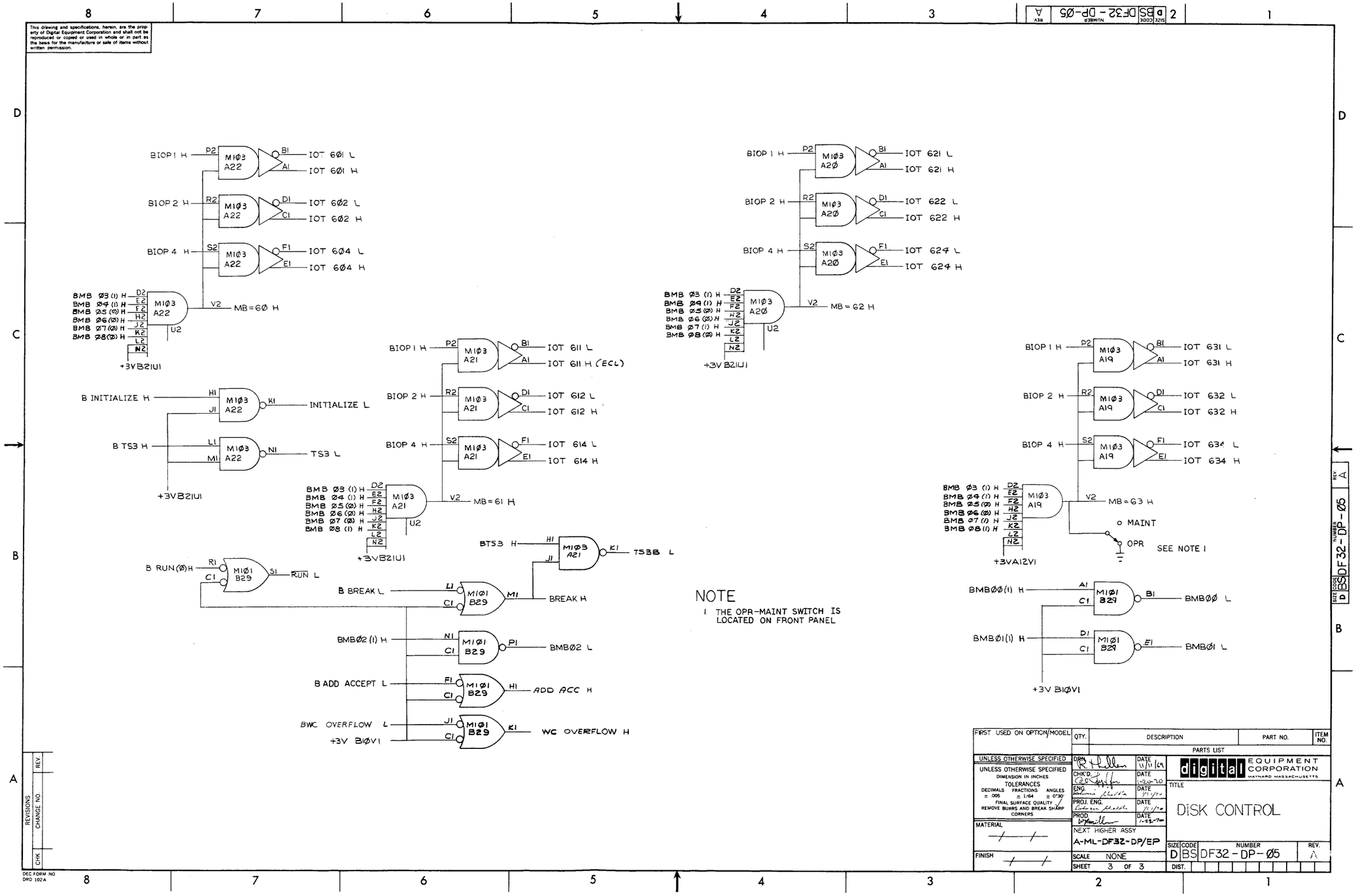
DEC FORM 840
DRD 102A



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
SEE NOTE 1
SEE NOTE 2
SEE NOTE 3
UNIT SELECT SWITCH
OFF
EM0 L
EM1 L
EM2 L
EM3 L
SKIP L
INT L
OPTION SELECT H
CLA L
STATUS H
TTA
TTB L
SLT H
NEX H
NEX L
SNE L
WIA H
WIB H
WIA L
WIB L
+5V
+3VA12V1
A-GND
NOTES:
1. READ SLICE MAY BE CONTROLLED BY GROUNDING (BS2, BT2) AND/OR (BU2, BV2)
2. UNIT SELECT SWITCH IS LOCATED ON FRONT PANEL.
3. TTA TRAILING EDGE TO TTB LEADING EDGE ≥ 350 NS.
FIRST USED ON OPTION/MODEL
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
NEXT HIGHER ASSY
A-ML-DF32-DP/EP
SCALE NONE
SHEET 1 OF 3
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
DISK CONTROL
SIZE D
CODE BS
NUMBER DF32-DP-Ø5
REV. A
DIST.
REVISIONS
CHANGE NO.
REV
CHK
DEC FORM NO DRD 102A



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
IOT 6Ø4 H
IOT 6Ø2 H
M112 B18
LAD L
M111 A18
LAD H
DCH H
M112 B18
IOT 634 H
IOT 6Ø4 H
M112 B18
SBR L
INITIALIZE L
M2Ø5 AØ7 WCO
WC OVERFLOW H
LAD L
+3V B1ØU1
M2Ø6 B16 MRS
SEN (1) H
WCO (1) H
M2Ø6 B16 TRC
DBR (1) H
M2Ø6 B16 DRL
NEX L
M2Ø6 B16 NED
WCO (Ø) H
M2Ø5 B15 DBR
IOT 6Ø1 L
INITIALIZE L
M113 B1Ø
SCL H
+3VA12U1
M113 A12
SCL L
DEP H
ADD ACC H
M112 B21
ADD ACCEPT L
INITIALIZE L
M113 B14
M111 A18
CBR L
TSB L
DBR (Ø) L
M112 B21
TCX (Ø) H
TTA H
SEN (1) H
M617 B11
SAP L
+3V B1ØV1
M2Ø5 B17 TCA
+3V B1ØV1
M2Ø5 B17 TCB
+3V B1ØV1
M2Ø5 B17 SEN
NEX H
MRS (1) L
TP1 L
M112 B18
WCT H
.ØØ2 MFD
SCL H
DCH H
M112 B18
DTC L
M113 B14
CSEN L
WCO (1) H
DEP H
M113 B14
RUN L
M111 A18
M112 B21
TP1 L
M2Ø5 B17 TCX
TTA H
+3V B1ØV1
+3V B1ØV1
M2Ø5 B17 ABD
TTB H
TTA 2 L
M113 B14
TTB H
TP1 L
M111 A18
TP1 H
FIRST USED ON OPTION/MODEL
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN
DATE 11/11/69
CHK'D
DATE 1-20-70
ENG.
DATE 1/20/70
PROJ. ENG.
DATE 1/21/70
PROD.
DATE 1-22-70
NEXT HIGHER ASSY
A-ML-DF32-DP/EP
SCALE NONE
SHEET 2 OF 3
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
DISK CONTROL
SIZE D
CODE BS
NUMBER DF32 - DP - Ø5
REV A
DIST.
REVISIONS
REV.
CHANGE NO.
CHK
DEC FORM NO DRD 102A



NOTE

1 THE OPR-MAINT SWITCH IS LOCATED ON FRONT PANEL

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R. Fuller DATE 11/11/69
CHK'D. DATE 1-20-70
ENG. DATE 1/21/70
PROJ. ENG. DATE 1/21/70
PROD. DATE 1-22-70

NEXT HIGHER ASSY A-ML-DF32-DP/EP

SCALE NONE
SHEET 3 OF 3

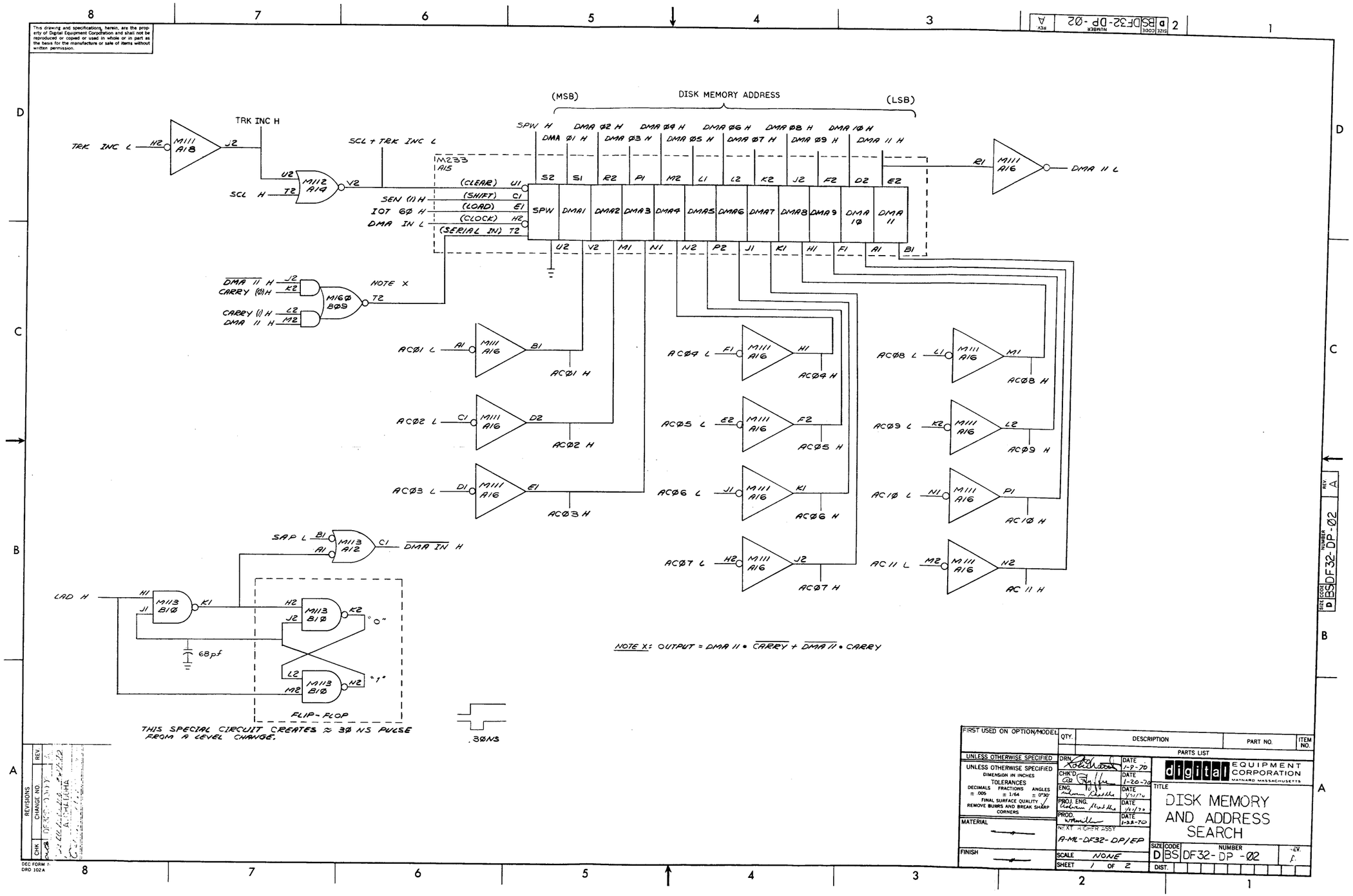
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE DISK CONTROL

SIZE D CODE BS NUMBER DF32-DP-Ø5 REV. A

REVISIONS CHANGE NO. REV. CHK

DEC FORM NO DRD 102A



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.	DATE	1-9-70
CHK'D.	DATE	1-20-70
ENG.	DATE	1/21/70
PROJ. ENG.	DATE	1/21/70
PROD.	DATE	1-28-70

NEXT HIGHER ASSY: A-ML-DF32-DP/EP

SCALE: NONE

SHEET 1 OF 2

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

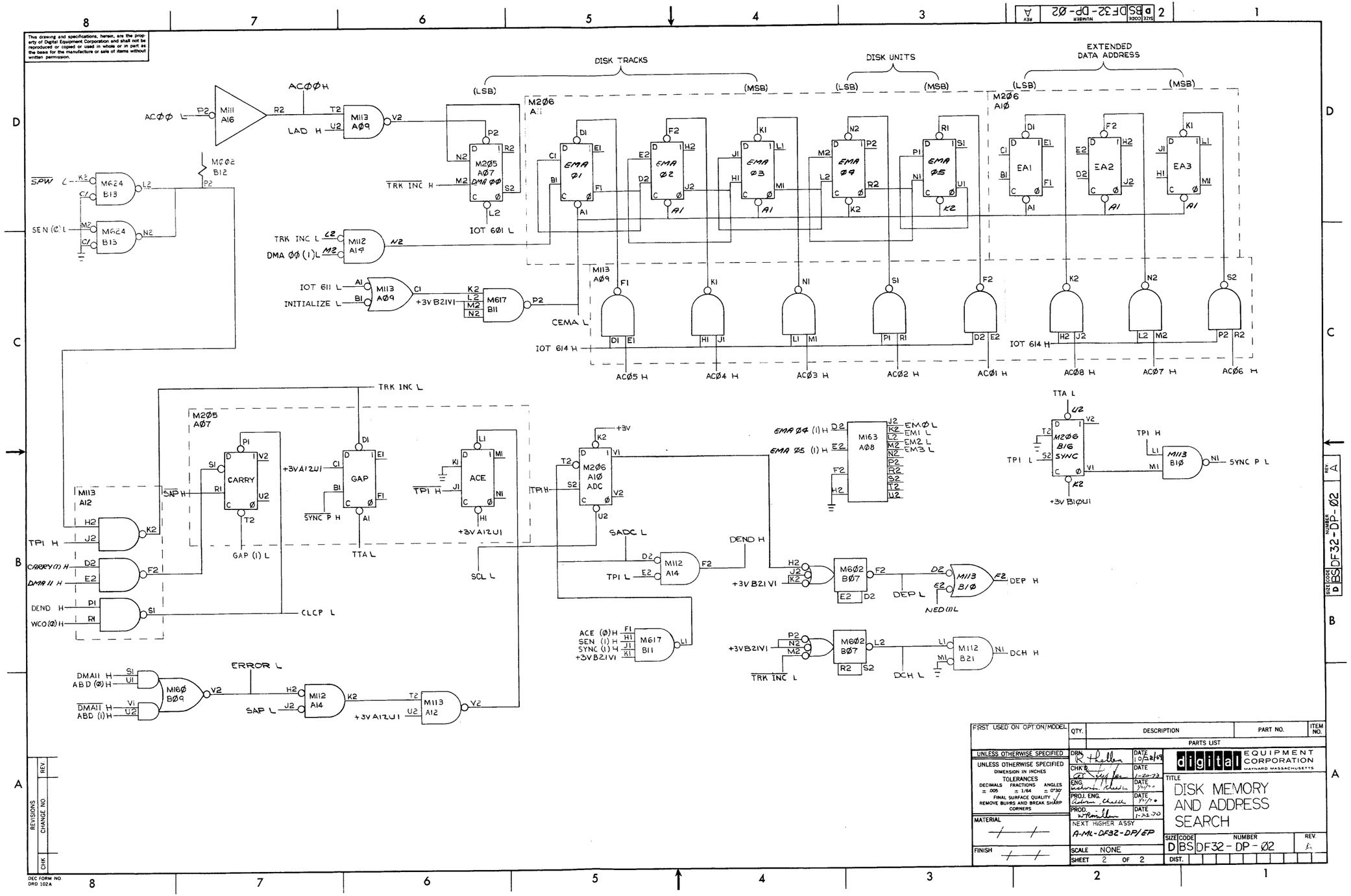
TITLE: DISK MEMORY AND ADDRESS SEARCH

SIZE D CODE BS NUMBER DF32-DP-Ø2 REV. A

DIST.

REVISIONS: CHK | CHANGE NO. | REV.

DEC FORM 1 DRD 102A



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R. Thellen DATE 10/28/69
CHK'D. DATE 1-20-73
ENG. DATE 1/21/70
PROJ. ENG. DATE 1/21/70
PROD. DATE 1-22-70

NEXT HIGHER ASSY
A-ML-DF32-DP/EP

SCALE NONE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

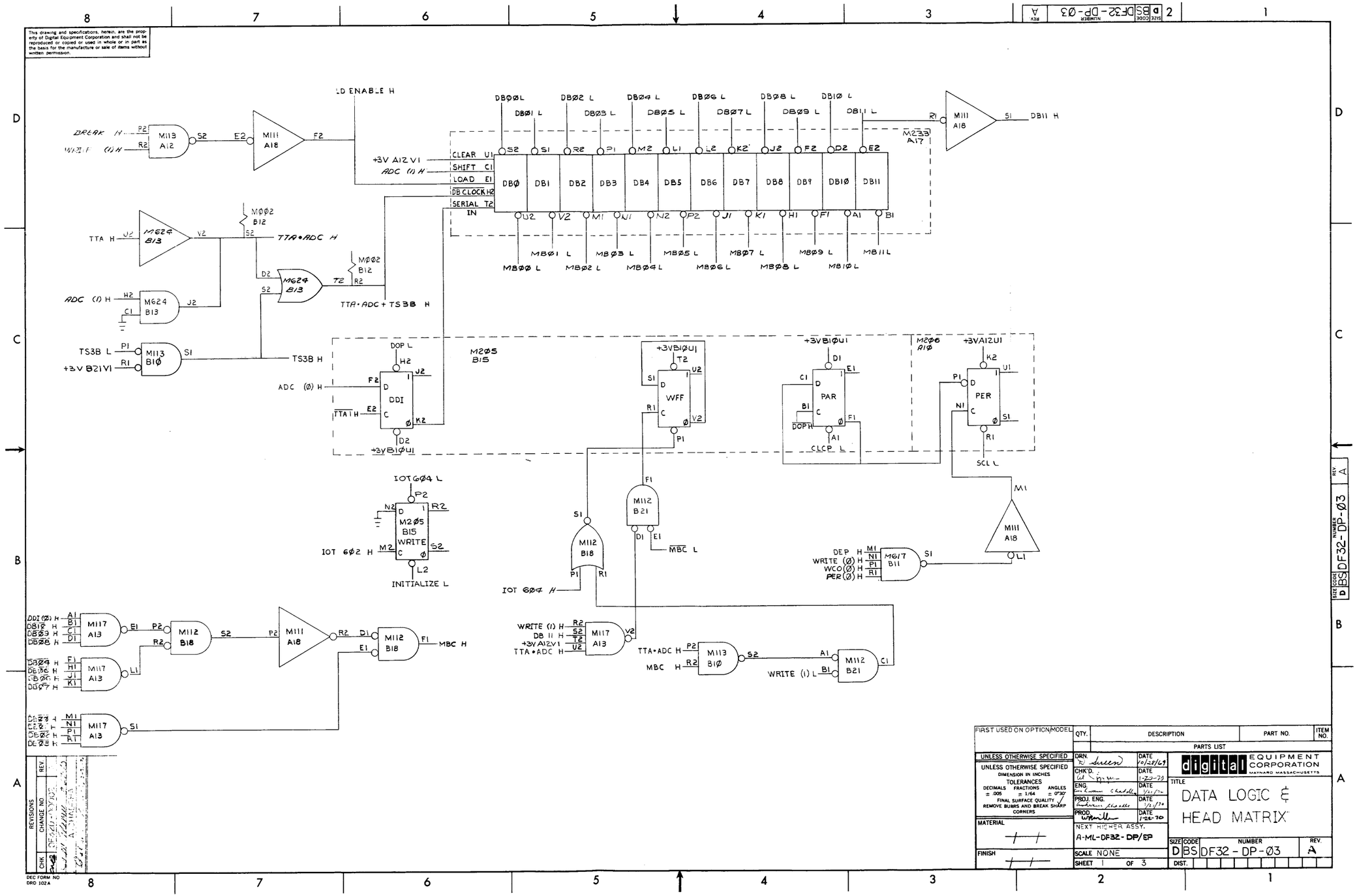
TITLE
DISK MEMORY AND ADDRESS SEARCH

SIZE D CODE BS NUMBER DF32 - DP - Ø2 REV. A
DIST.

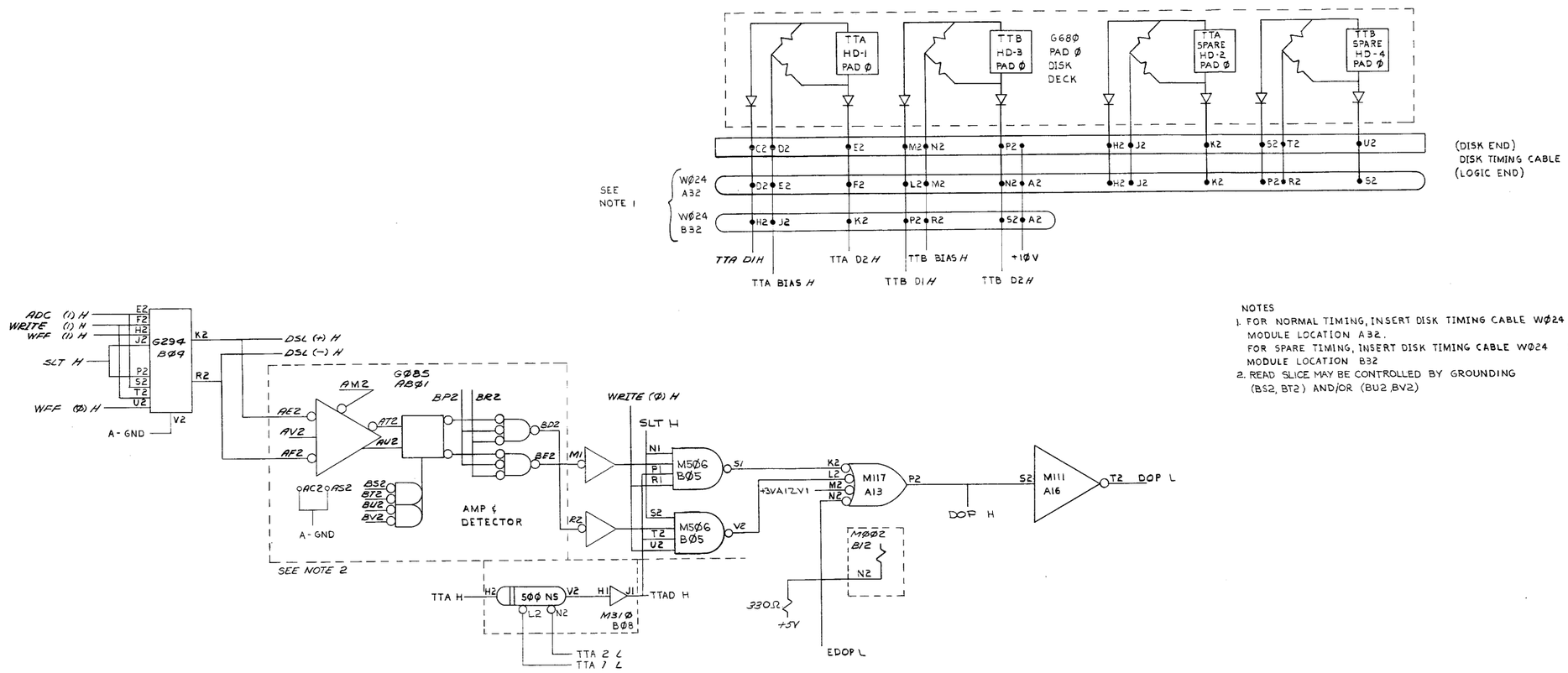
REVISIONS | CHANGE NO. | REV. | CHK

DEC FORM NO. DRD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



NOTES
1. FOR NORMAL TIMING, INSERT DISK TIMING CABLE WØ24 IN MODULE LOCATION A32.
FOR SPARE TIMING, INSERT DISK TIMING CABLE WØ24 IN MODULE LOCATION B32
2. READ SLICE MAY BE CONTROLLED BY GROUNDING (BS2, BT2) AND/OR (BU2, BV2)

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. [signature] DATE 10/30/69
CHK'D. [signature] DATE 12-0-70
ENG. [signature] DATE 1/2/70
PROJ. ENG. [signature] DATE 1/21/70
PROD. [signature] DATE 1-22-70

NEXT HIGHER ASSY A-ML-DF32-DP/EP
SCALE NONE
SHEET 2 OF 3

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

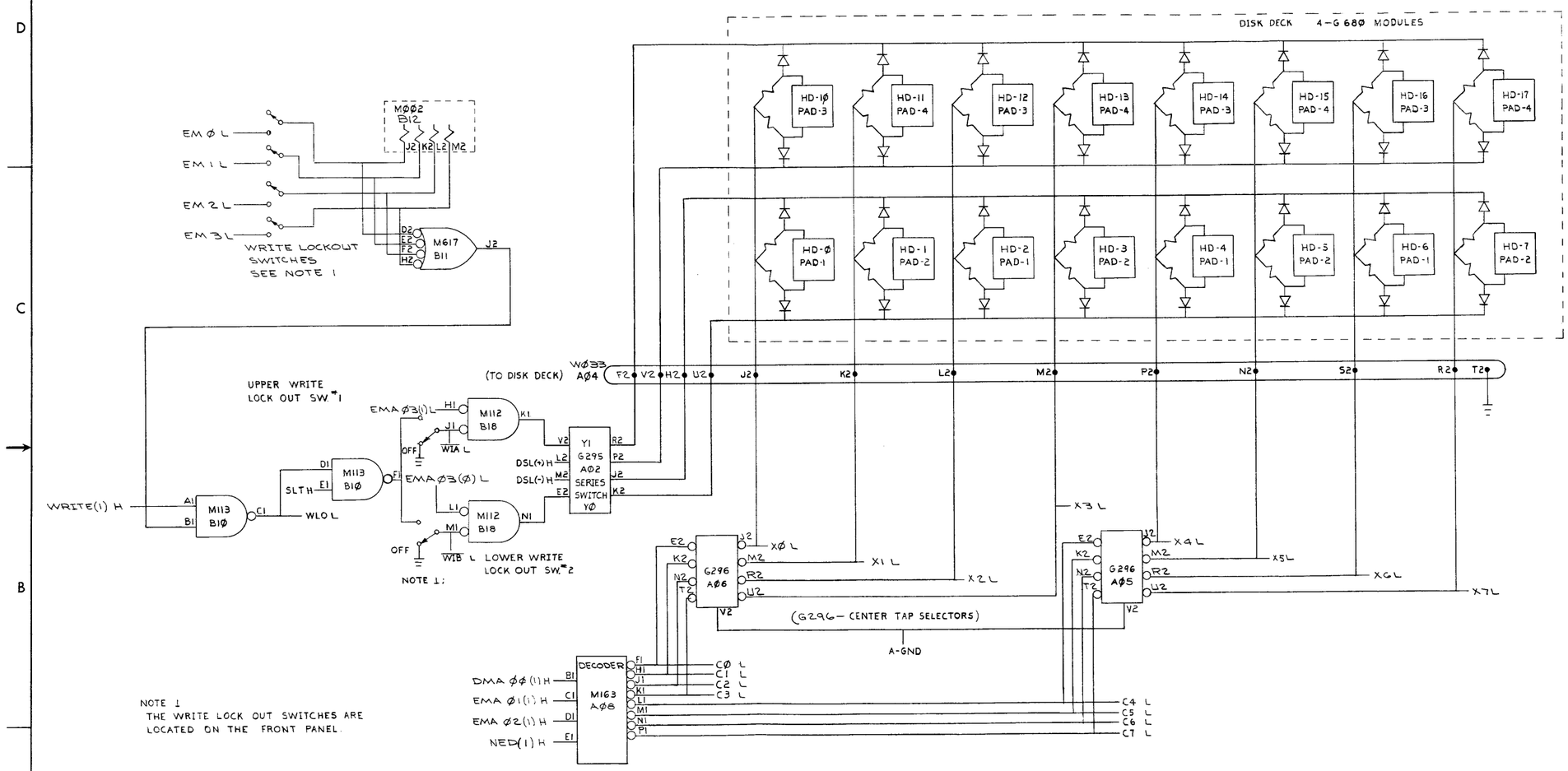
TITLE DATA LOGIC & HEAD MATRIX

SIZE D CODE BS NUMBER DF32-DP-Ø3 REV A
DIST.

REVISIONS | CHANGE NO. | REV | CHK

DEC FORM NO DRD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN.		DATE
CHK'D.		DATE 1-20-70
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE 1-22-70

NEXT HIGHER ASSY
A-ML-DF32-DP/EP
SCALE NONE
SHEET 3 OF 3

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
DATA LOGIC & HEAD MATRIX

SIZE D CODE BS NUMBER DF32-DP-03 REV A
DIST.

REVISIONS
CHK | CHANGE NO | REV

DEC FORM NO DRD 102A

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Module	G085	G295	M903	W033	G296	G296	M205	M163	M113	M206	M206	M113	M117	M112	M233	M111	M233	M111	M103	M103	M103	M103
USAGE			CABLE	CABLE																		
A	DOP	Y0 & Y1 SERIES SWITCH	BEM 0 TO BEM 3 X0 TO X4	X5 TO X7 B WRITE BADC BEMA 3 BWLO BWFF	DISK HEAD CABLE X0 THPU X7	X4 THRU X7	X0 THRU X3	GAP ACE	WCO DMA0 CARRY	C0 THRU C7	EM0 THRU EM3	EA1 EA3 PER	EA2 ADC	EMA1 EMA3 EMA5	EMA2 EMA4	DMA IN W1A W1B IOT 60 CLCP	CARRY TRK INC SCL LD ENAB ACE SET	WFF WFF	SNE DOP WFF	CLA INT OPTION SELECT	DEND ACE SET EMA1 SCL + TRK INC	DMA Ø5 DMA Ø3 DMA Ø1	DMA11 DMA10 DMA09 DMA08 DMA07 DMA06 DMA04 DMA02 SPW
B	DOP		EXT DATA ADD 0 THRU 2	EWL ETTAP ETTEP EDOP EUSS A-GND	DSL (+) DSL (-)	TTAP TTBP	DEP DCH	TTAD TTAD	SKIP	SERIAL IN ERROR	WLO WLO & STL LAD SYNC P TS3B	DEP DMA IN WFF CLR SCL	SAP SADC PER	WLO CEMA IOT 60	D E F H J K L M N P R S	BEM 0 BEM 1 BEM 2 BEM 3 B WRITE B ADC BEMA 3 BWLO	BWFF TTA & ADC TRK INC TTA & ADC + TS3B TTA & ADC	TPI NEX STATUS CBR CSEN TTA	CSEN OPTION SELECT CLA TTA TTB	PAR DBR	DDI WRITE WFF	MRS DRL SYNC	TRC NED	TCA TCB	SEN TCX ABD

Slot	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
Module	M101	M101	M903	M903	M903	M903	M903	G085	G085	W024 *												
USAGE			CABLE	CABLE	CABLE	CABLE	CABLE			CABLE												
A	AC00 AC01 AC02 AC03 AC04 AC05 AC06 AC07	AC08 AC09 AC10 AC11 MB9 MB00 MB01 MB02 MB03 MB04 MB05 MB06 MB07	BAC 00 (1) TO BAC 08 (1) BAC 09 (1) TO BAC 11 (1) BIOP1 BIOP2 BIOP4 BTS3 BTS1 B INIT	BMB 00 (1) THRU BMB 05 (1) BMB 06 (0) THRU BMB 11 (1)	AC00 BUS TO AC08 BUS AC09 BUS TO AC11 BUS SKIP BUS INT RQST BUS AC CLR BUS BRUN BTT INST LINE MUX	DATA ADD 00 TO 08 DATA ADD 09 TO 11 BRK RQST DATA IN B BREAK B ADD ACCEPT MB INC B INIT	DATA 00 TO DATA 08 DATA 09 TO DATA 11 3 CYCLE CA INCR BWC OVFL EXT DATA ADD 2 EXT DATA ADD 1 EXT DATA ADD 0		TTAN 2	TTBN 2	+10V TTA D1 TTA BIAS TTA D2 TTB D1 TTB BIAS TTB D2										
	M623	M623	M903	M903	M903		M101			W024 *												
USAGE			CABLE	CABLE	CABLE					CABLE												
B	SKIP BUS INT RQST BUS AC CLR BUS BRK RQST	DATA IN EXT ADD 2 EXT ADD 1 EXT ADD 0	DATA 00 DATA 01 DATA 02 DATA 03 DATA 04 DATA 05 DATA 06 DATA 07 DATA 08 DATA 09 DATA 10 DATA 11	BAC 00 (1) TO BAC 08 (1) BAC 09 (1) TO BAC 11 (1) BIOP1 BIOP2 BIOP4 BTS3 BTS1 B INIT	BMB 00 (1) THRU BMB 05 (1) BMB 06 (0) THRU BMB 11 (1)	AC00 BUS TO AC08 BUS AC09 BUS TO AC11 BUS SKIP BUS INT RQST BUS AC CLR BUS BRUN BTT INST LINE MUX	BMB00 BMB01 ADD ACC BWC OVER BREAK BMB02 RUN(1)		TTAN 1	TTBN 1	+10V TTA D1 TTA BIAS TTA D2 TTB D1 TTB BIAS TTB D2										

NOTES:
* FOR NORMAL TIMING INSERT DISK TIMING CABLE IN LOCATION A32. FOR SPARE TIMING INSERT CABLE IN LOCATION B32.
** CABLE USED IN THE PDP 8 SYSTEM ONLY.

FIRST USED ON OPTION/MODEL

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN. H. Rosenberg DATE 12-18-69
CHK'D. W. Thelin DATE 1-20-70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 1-22-70
NEXT HIGHER ASSY A-ML-DF32-DP/EP
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE MODULE UTILIZATION

SIZE D CODE MU NUMBER DF32-DP-06 REV. A
DIST.

REVISIONS
REV.	CHANGE NO.	CHK
A	DF32-0000	

DEC FORM NO. DRD 112

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

MODULE UTILIZATION

Rows A and B (Usage, side 1 / side 2):

Slot	A Module	A Usage (1 / 2)	B Module	B Usage (1 / 2)
1	G085	— / DOP		— / DOP
2	G295	— / YØ & Y1 SERIES SWITCH	W031 CABLE	— / EXT DATA ADD Ø THRU 2
3	M903 CABLE	BEM Ø TO BEM 3, XØ TO X4 / X5 TO X7, B WRITE, BADC, BEMA 3, BWLO, BWFF	W021 CABLE	— / EWL, ETTAP, ETTBP, EDOP, EUSS, A-GND
4	W033 CABLE	— / DISK HEAD CABLE XØ THRU X7	G294	— / DSL (+), DSL (−)
5	G296	— / X4 THRU X7	M506	TTAP1, TTBP1, DOP / TTAP2, TTBP2, DOP
6	G296	— / XØ THRU X3	M602	— / TTAP, TTBP
7	M205	GAP, ACE / WCO, DMAØ, CARRY	M602	— / DEP, DCH
8	M163	CØ THRU C7 / EMØ THRU EM3	M310	TTAD / TTAP
9	M113	CEMA, EMA1 SET, EMA2 SET, EMA3 SET, EMA4 SET / EMA5 SET, EA1 SET, EA2 SET, EA3 SET, DMAØ SET	M160	SKIP / SERIAL IN, ERROR
10	M206	EA1, EA3, PER / EA2, ADC	M113	WLO, WLO & STL, LAD, SYNC P, TS3B / DEP, DMA IN, WFF CLR, SCL
11	M206	EMA1, EMA3, EMA5 / EMA2, EMA4	M617	SAP, SADC, PER / WLO, CEMA, IOT 6Ø
12	M113	DMA IN, WIA, WIB, IOT 6Ø, CLCP / CARRY, TRK INC, SCL, LD ENAB, ACE SET	M002	— / D, E, F, H, J, K, L, M, N, P, R, S
13	M117	WFF / SNE, DOP, WFF	M624	BEM Ø, BEM 1, BEM 2, BEM 3, B WRITE, B ADC, BEMA 3, BWLO / BWFF, TTA & ADC, TRK INC, TTA & ADC + TS3B, TTA & ADC
14	M112	CLA, INT, OPTION SELECT / DEND, ACE SET, EMA1, SCL + TRK INC	M113	TPI, NEX, STATUS, CBR, CSEN / CSEN, OPTION SELECT, CLA, TTA, TTB
15	M233	DMA Ø5, DMA Ø3, DMA Ø1 / DMA11, DMA1Ø, DMAØ9, DMAØ8, DMAØ7, DMAØ6, DMAØ4, DMAØ2, SPW	M205	PAR, DBR / DDI, WRITE, WFF
16	M111	ACØ1, ACØ3, ACØ4, ACØ6, ACØ8, AC1Ø, DMA11 / ACØ2, ACØ5, ACØ7, ACØ9, AC11, ACØØ, DOP, SNE	M206	MRS, DRL / TRC, NED, SYNC
17	M233	DBØ5, DBØ3, DBØ1 / DB11, DB1Ø, DBØ9, DBØ8, DBØ7, DBØ6, DBØ4, DBØ2, DBØØ	M205	TCA, TCB / SEN, TCX, ABD
18	M111	TTA, RUN L, TPI, CBR, PER, MBØ1, DB11, LAD / TTB, LD ENAB, TRK INC, CLA, MBØØ, MBC, SLT	M112	DTC, MBC, SERIES SW, YØ & Y1, WFF CLR / MRS SET, SBR, LAD, MBC, WCT
19	M102	IOT 631, IOT 632, IOT 634 / MB= 63	M121	ACØ6 BUS, ACØ7 BUS, ACØ8 BUS / ACØ9 BUS, AC1Ø BUS, AC11 BUS
20	M102	IOT 621, IOT 622, IOT 624 / MB= 62	M121	ACØØ BUS, ACØ1 BUS, ACØ2 BUS / ACØ3 BUS, ACØ4 BUS, ACØ5 BUS
21	M102	IOT 611, IOT 612, IOT 614, TS3B / MB= 61	M112	WFF CLF, WFF, ADD ACC, DCH, NED / ADDR ACCEPT, BREAK
22	M102	IOT 6Ø1, IOT 6Ø2, IOT 6Ø4, INIT, TS3 / MB= 6Ø	M633	ACØØ BUS, ACØ1 BUS, ACØ2 BUS, ACØ3 BUS, ACØ4 BUS, ACØ5 BUS / ACØ6 BUS, ACØ7 BUS, ACØ8 BUS, ACØ9 BUS, AC1Ø BUS, AC11 BUS
23	M100	ACØØ, ACØ1, ACØ2, ACØ3, ACØ4, ACØ5, ACØ6, ACØ7 / ACØ8, ACØ9, AC1Ø, AC11, MB9	M633	SKIP BUS, INT RQST BUS, AC CLR BUS, BRK RQST / DATA IN, EXT ADD 2, EXT ADD 1, EXT ADD Ø
24	M100	MBØØ, MBØ1, MBØ2, MBØ3, MBØ4, MBØ5, MBØ6, MBØ7 / MBØ8, MBØ9, MB1Ø, MB11	M633	DATA ØØ, DATA Ø1, DATA Ø2, DATA Ø3, DATA Ø4, DATA Ø5 / DATA Ø6, DATA Ø7, DATA Ø8, DATA Ø9, DATA 1Ø, DATA 11
25	M903 CABLE	BAC ØØ (1) TO BAC Ø8 (1) / BAC Ø9 (1) TO BAC 11 (1), BIOP1, BIOP2, BIOP4, BTS 3, BTS 1, B INIT	M903 CABLE	BAC ØØ (1) TO BAC Ø8 (1) / BAC Ø9 (1) TO BAC 11 (1), BIOP1, BIOP2, BIOP4, BTS 3, BTS 1, B INIT
26	M903 CABLE	BMB ØØ (1) THRU BMB Ø5 (1) / BMB Ø6 (Ø) THRU BMB 11 (1)	M903 CABLE	BMB ØØ (1) THRU BMB Ø5 (1) / BMB Ø6 (Ø) THRU BMB 11 (1)
27	M903 CABLE	ACØØ BUS TO ACØ8 BUS / ACØ9 BUS TO AC11 BUS, SKIP BUS, INT RQST BUS, AC CLR BUS, BRUN, BTT, INST LINE MUX	M903 CABLE	ACØØ BUS TO ACØ8 BUS / ACØ9 BUS TO AC11 BUS, SKIP BUS, INT RQST BUS, AC CLR BUS, BRUN, BTT, INST LINE MUX
28	M903 CABLE	DATA ADD ØØ TO Ø8 / DATA ADD Ø9 TO 11, BRK RQST, DATA IN, B BREAK, B ADD ACCEPT, MB INC, B INIT	W005	— / D, E, F, H, J, K, L, M, N, P, R, S, T, U, V
29	M903 CABLE	DATA ØØ TO DATA Ø8 / DATA Ø9 TO DATA 11, 3 CYCLE CA INCR, BWC OVFL, EXT DATA ADD 2, EXT DATA ADD 1, EXT DATA ADD Ø	M100	BMBØØ, BMBØ1, ADD ACC, BWC OVER, BREAK, BMBØ2, RUN(1) / —
30	G085	— / TTAN 2		— / TTAN 1
31	G085	— / TTAN 2		— / TTBN 1
32	W024 * CABLE	— / +10V, TTA D1, TTA BIAS, TTA D2, TTB D1, TTB BIAS, TTB D2	W024 * CABLE	— / +1ØV, TTA D1, TTA BIAS, TTA D2, TTB D1, TTB BIAS, TTB D2
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
44				

NOTES:
* FOR NORMAL TIMING INSERT DISK TIMING CABLE IN LOCATION A32.
FOR SPARE TIMING INSERT CABLE IN LOCATION B32.

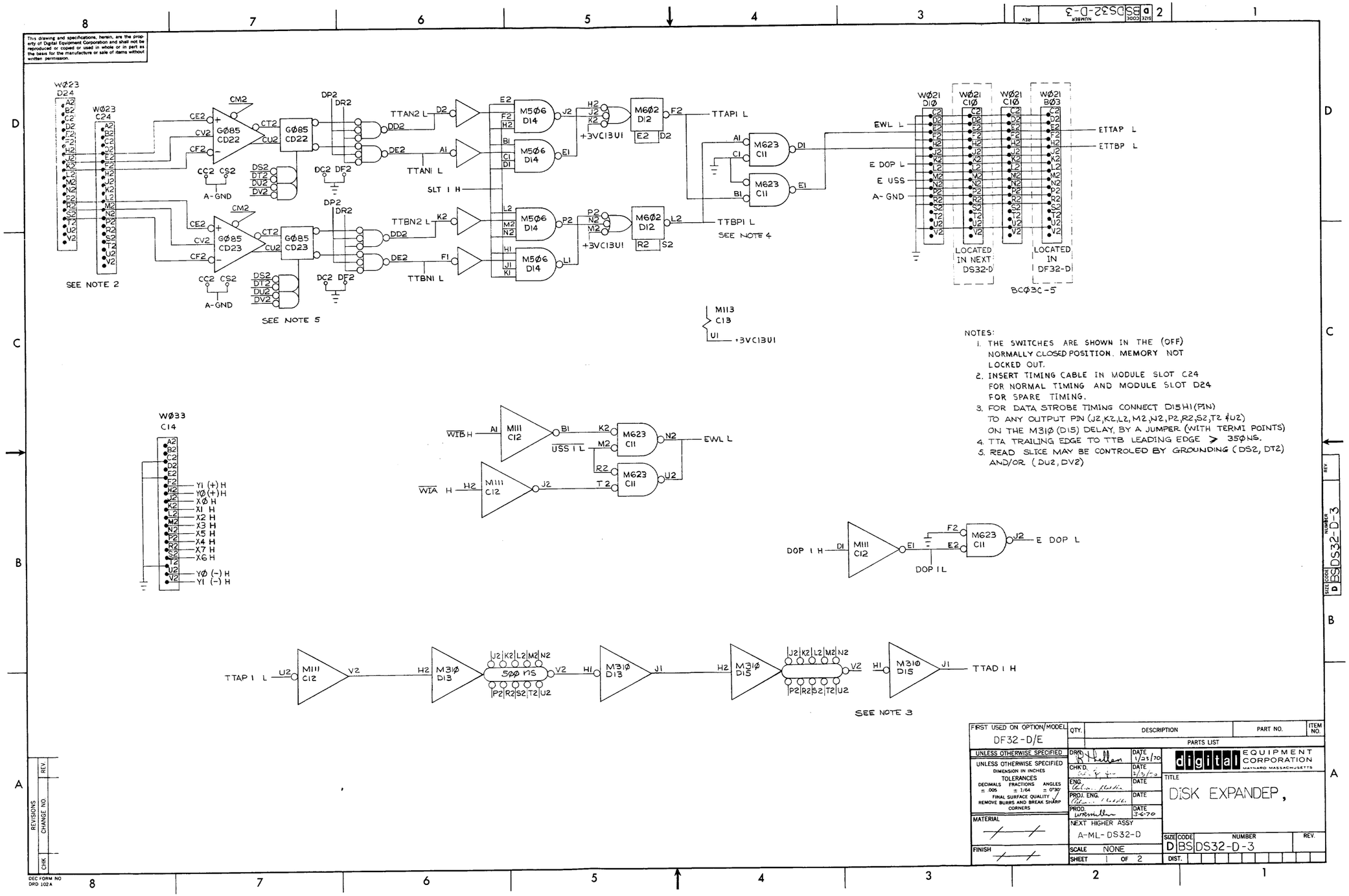
FIRST USED ON OPTION/MODEL	
DO NOT SCALE DRAWING	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY √ REMOVE BURRS AND BREAK SHARP CORNERS	
MATERIAL	
FINISH	
DRN.	DATE 1/14/70
CHK'D.	DATE 1/20/70
ENG.	DATE
PROJ. ENG.	DATE
PROD.	DATE 1-23-70
NEXT HIGHER ASSY	A-ML-DF32-DN/EN
SCALE	
SHEET 1 OF 1	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

SIZE D CODE MU NUMBER DF32-DN-Ø6 REV A

DEC FORM NO. DRD 112



NOTES:

1. THE SWITCHES ARE SHOWN IN THE (OFF) NORMALLY CLOSED POSITION. MEMORY NOT LOCKED OUT.
2. INSERT TIMING CABLE IN MODULE SLOT C24 FOR NORMAL TIMING AND MODULE SLOT D24 FOR SPARE TIMING.
3. FOR DATA STROBE TIMING CONNECT D15H1(PIN) TO ANY OUTPUT PIN (J2,K2,L2,M2,N2,P2,R2,S2,T2 & U2) ON THE M31Ø (D15) DELAY, BY A JUMPER (WITH TERMI POINTS)
4. TTA TRAILING EDGE TO TTB LEADING EDGE > 35ØNS.
5. READ SLICE MAY BE CONTROLED BY GROUNDING (DS2, DT2) AND/OR (DU2, DV2)

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DF32-D/E		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. R. Phelan DATE 1/23/70
CHK'D. DATE 2/3/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 3-6-70
NEXT HIGHER ASSY A-ML-DS32-D
SCALE NONE
SHEET 1 OF 2

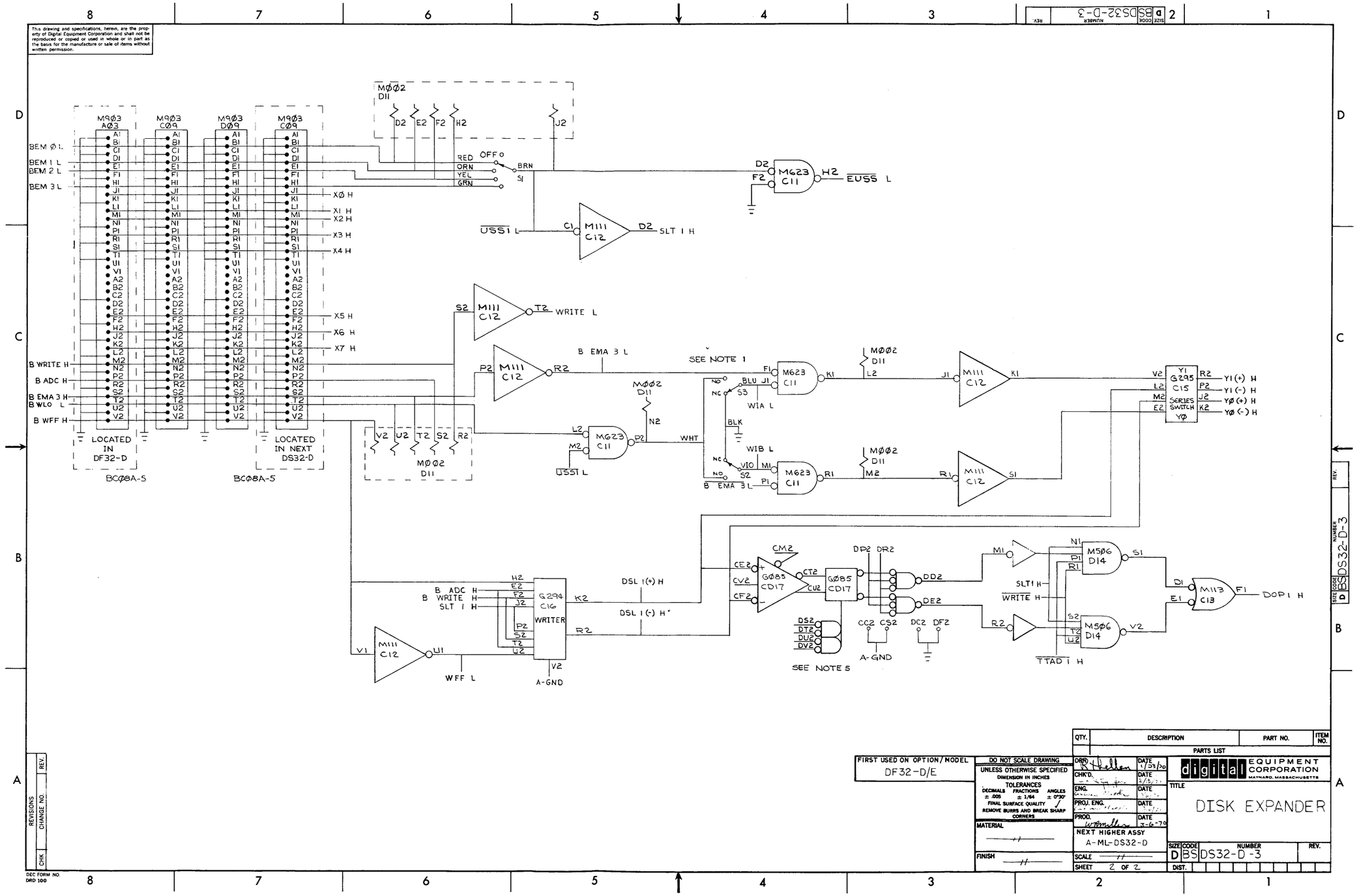
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE DISK EXPANDER,

SIZE D CODE BS NUMBER DS32-D-3 REV.
DIST.

REVISIONS CHANGE NO. REV. CHK

DEC FORM NO DRD 102A



QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

FIRST USED ON OPTION/MODEL: DF32-D/E

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —//—

FINISH —//—

DRN. DATE 1/23/70
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 3-6-70

NEXT HIGHER ASSY A-ML-DS32-D

SCALE —//—

SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

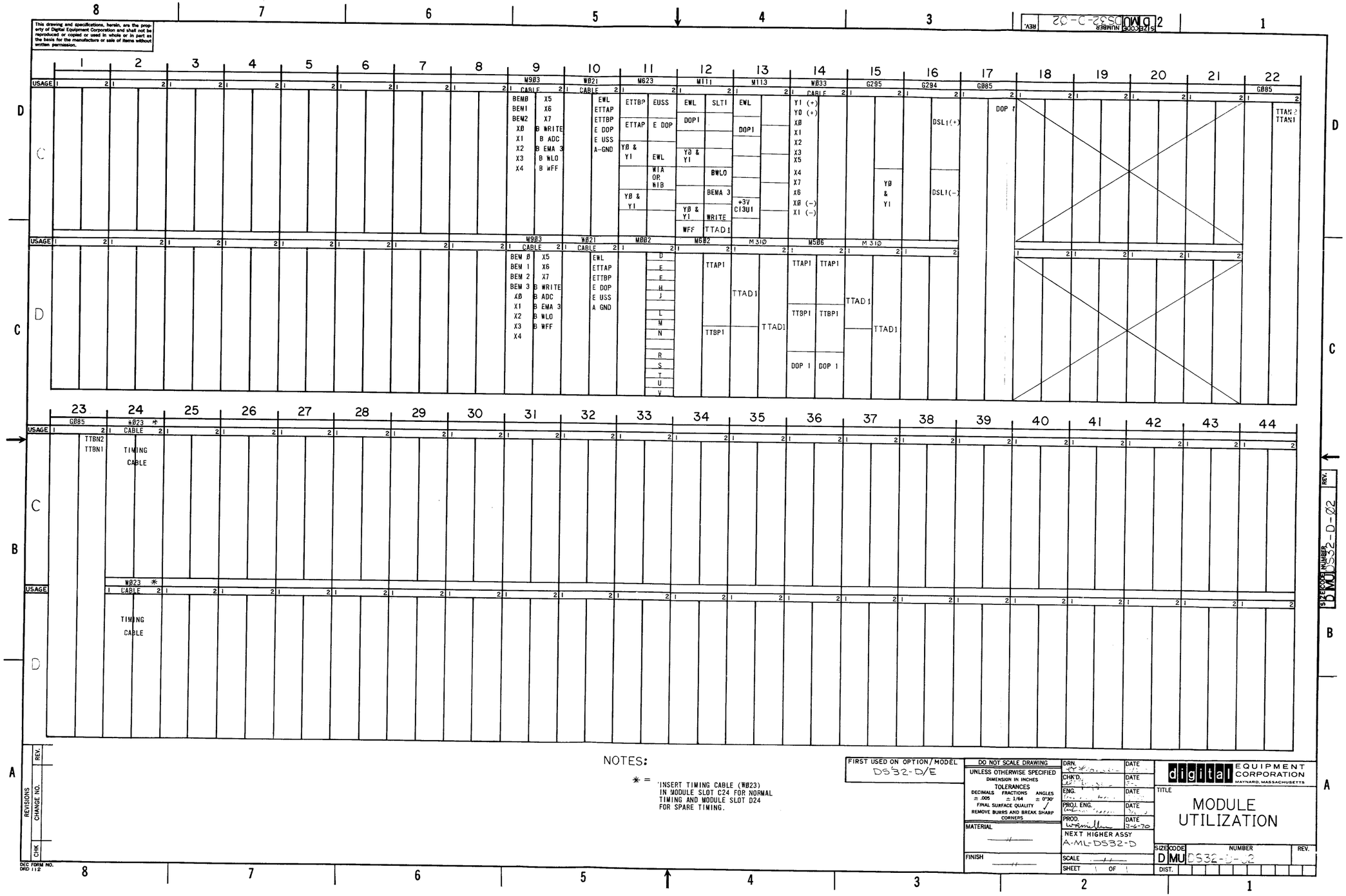
TITLE: DISK EXPANDER

SIZE D CODE BS NUMBER DS32-D-3 REV.

DIST.

REVISIONS: CHK | CHANGE NO. | REV.

DEC FORM NO. DRD 100



NOTES:

* = INSERT TIMING CABLE (W023) IN MODULE SLOT C24 FOR NORMAL TIMING AND MODULE SLOT D24 FOR SPARE TIMING.

FIRST USED ON OPTION/MODEL DS32-D/E

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —//—
FINISH —//—

DRN. DATE
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 3-6-70
NEXT HIGHER ASSY A-ML-DS32-D
SCALE —//—
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE MODULE UTILIZATION

SIZE D CODE MU NUMBER DS32-D-02 REV.

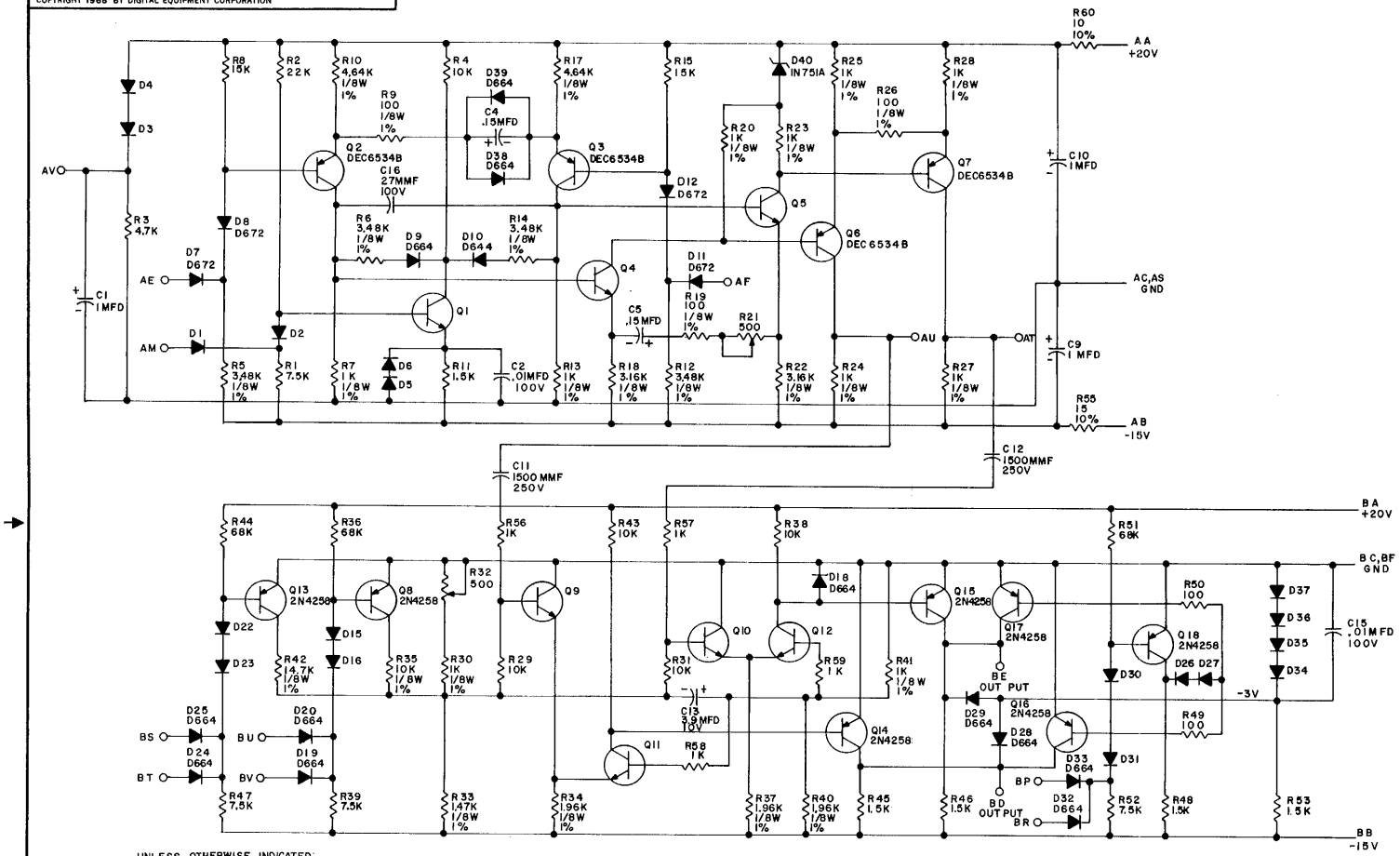
DIST.

REVISIONS CHANGE NO. REV. CHK

DEC FORM NO. DRD 112

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1968 BY DIGITAL EQUIPMENT CORPORATION



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 35V
RESISTORS ARE 1/4W, 5%
DIODES ARE D662
TRANSISTORS ARE DEC3009B
R21, R32 ARE POTS 76 PR 500 HELITRIM
1/8W, 1% RESISTORS ARE 100MF

REVISIONS		
CHK	CHG NO.	REV
MM	00001	A
	REV. & REQR.	
	00002	D
	00003	

DRN.	M. HALLER	DATE 10-23-68
CHK'D	MULLEN	DATE 10-24-68
ENG.	S. SAMBERT	DATE 1-10-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606	DEC6534B	MPS6534B
D662	IN645	IN751A	SAME
D672	IN3653		
2N4258	NONE		
DEC3009B	2N3009B		

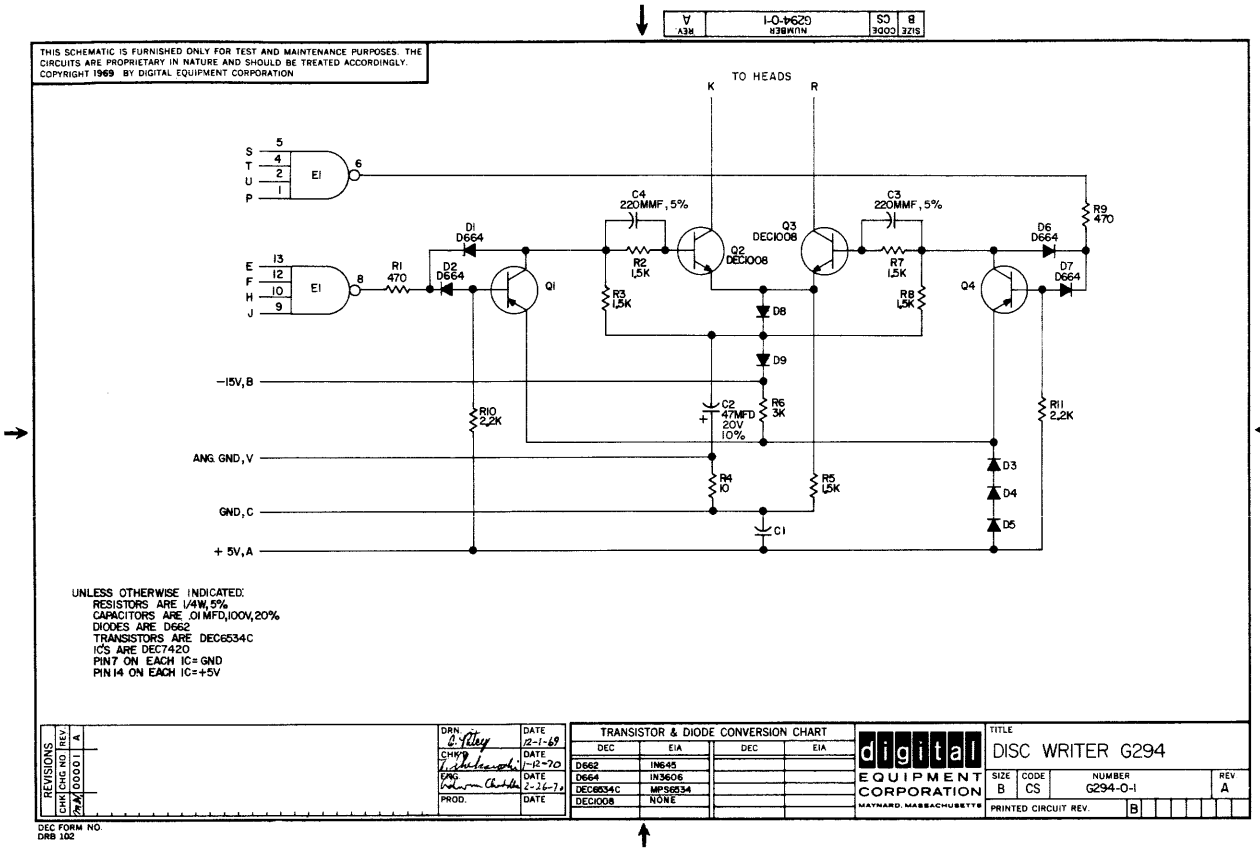
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

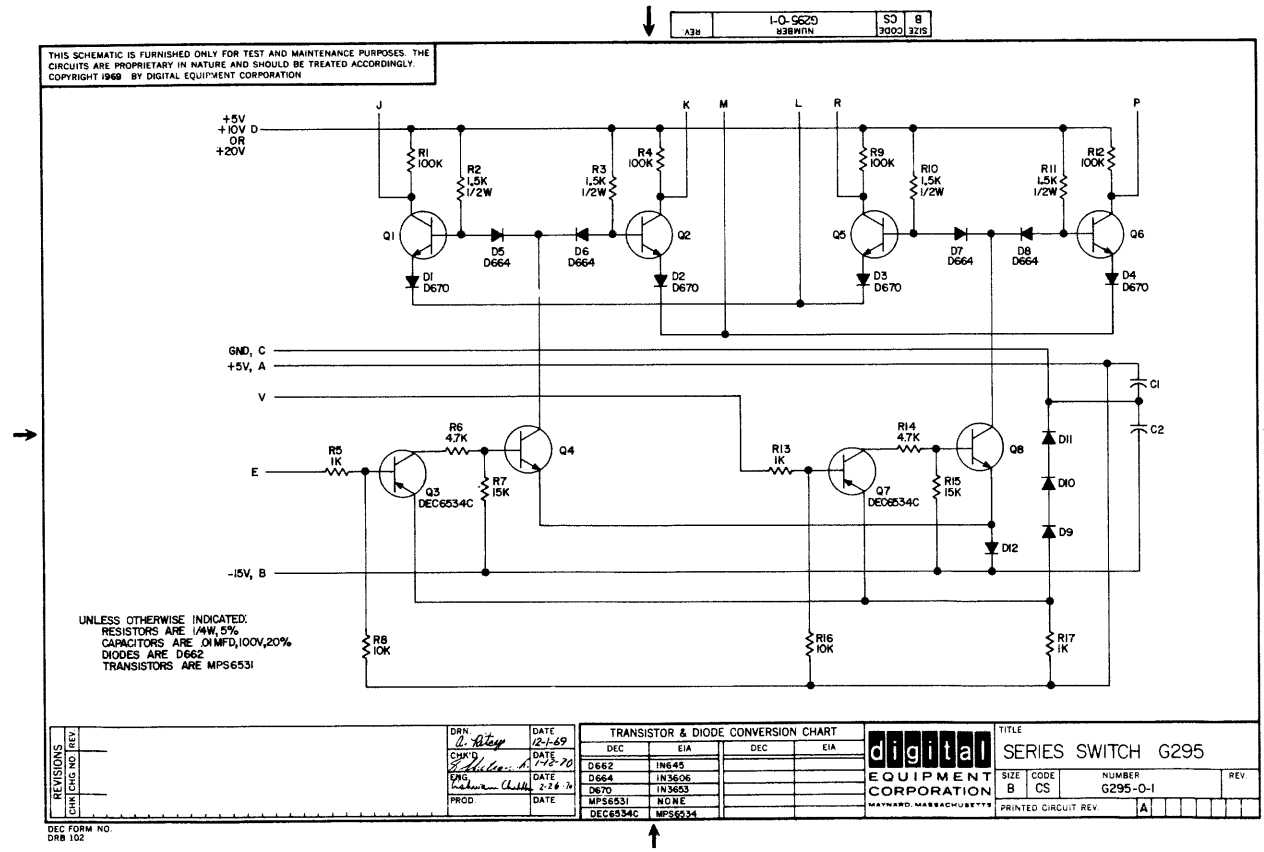
TITLE: DISC READ AMP AND SLICE G085

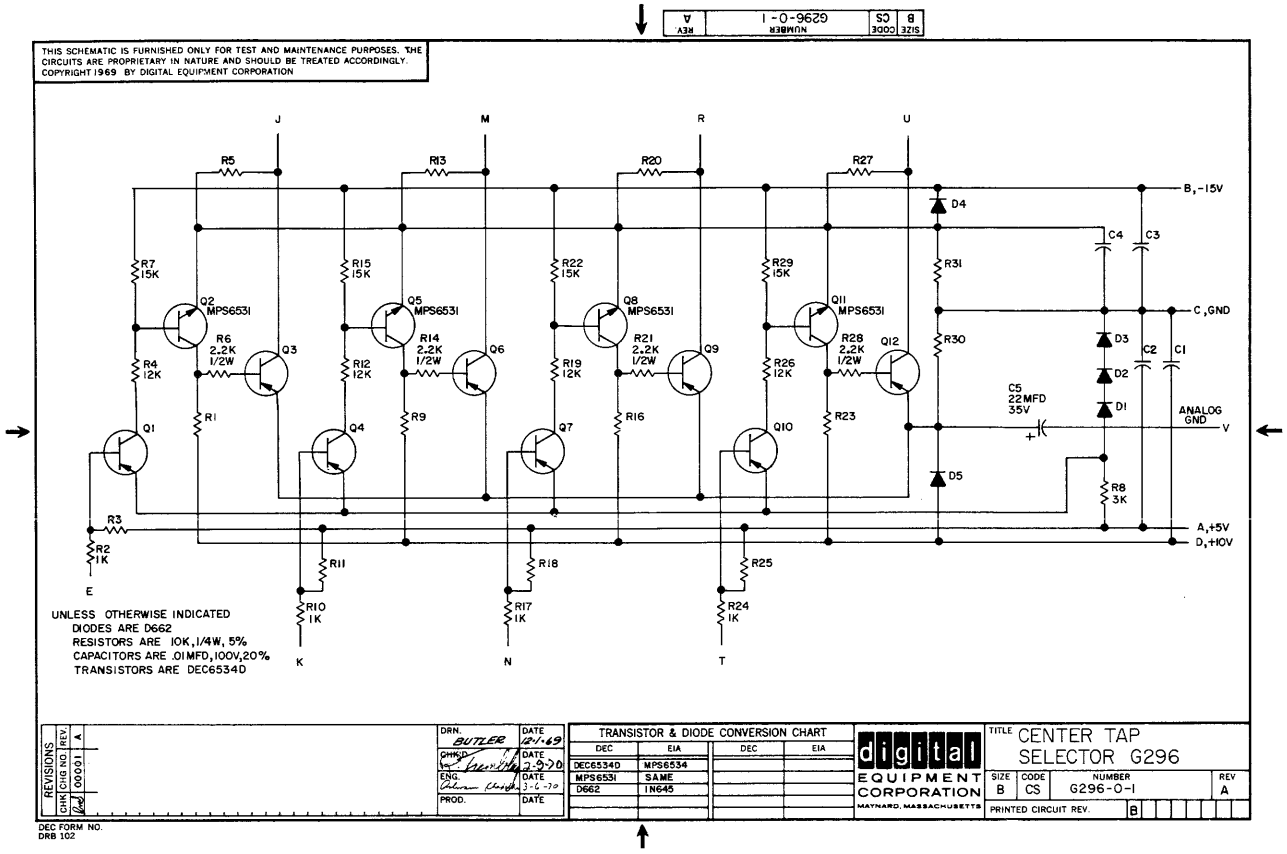
SIZE	CODE	NUMBER	REV.
C	CS	G085-0-1	D

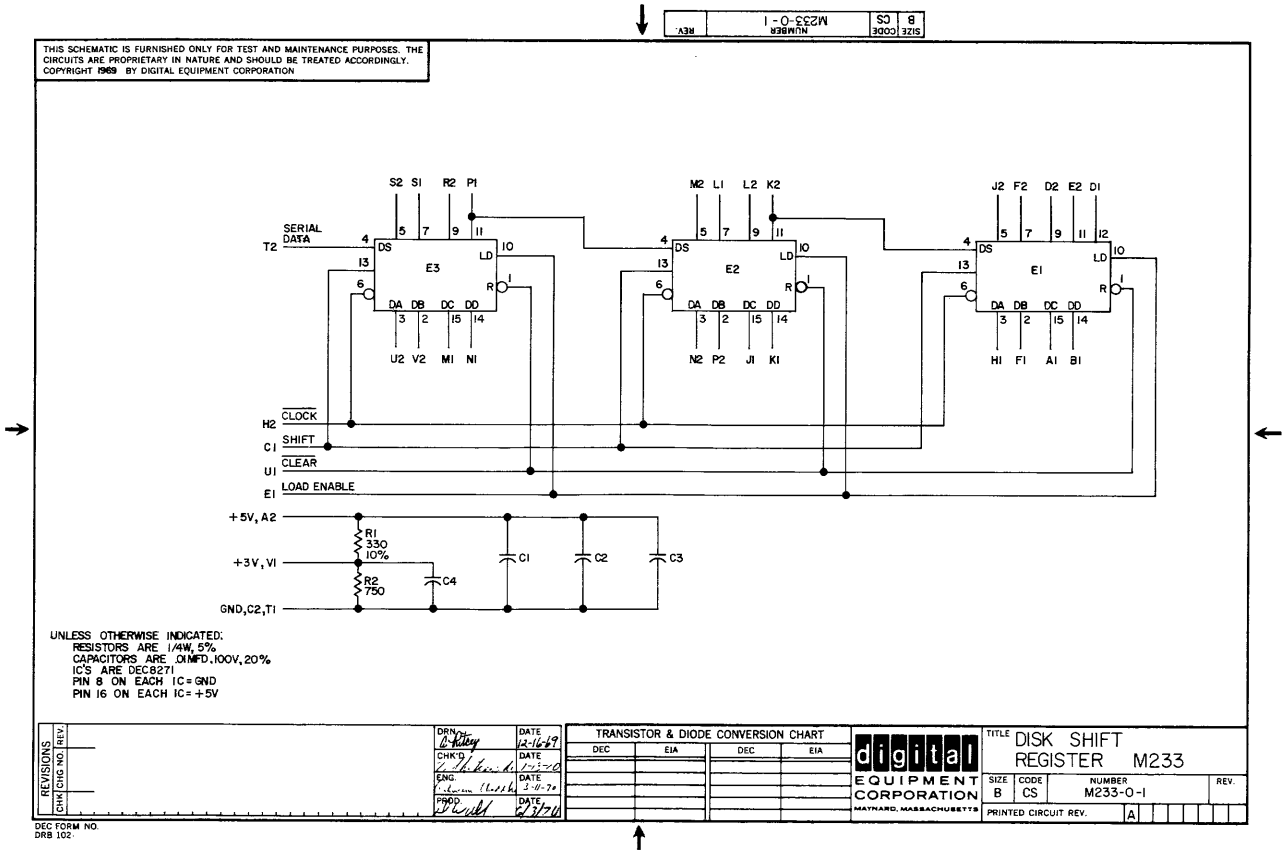
PRINTED CIRCUIT REV. D

DEC FORM NO. DRC 102


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
TO HEADS
K
R
S
T
U
P
E
F
H
J
E1
C4 220MMF, 5%
C3 220MMF, 5%
Q1
Q2 DEC1008
Q3 DEC1008
Q4
D1 D664
D2 D664
D6 D664
D7 D664
R1 470
R2 1.5K
R3 1.5K
R7 1.5K
R8 1.5K
R9 470
D8
D9
-15V, B
R10 2.2K
C2 47MFD 20V 10%
R6 3K
R11 2.2K
ANG. GND, V
R4 10
R5 1.5K
D3
D4
D5
GND, C
C1
+ 5V, A
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD, 100V, 20%
DIODES ARE D662
TRANSISTORS ARE DEC6534C
IC'S ARE DEC7420
PIN 7 ON EACH IC= GND
PIN 14 ON EACH IC=+5V
REVISIONS
CHK CHG NO REV
DRN. 12-1-69
CHK'D 1-12-70
ENG. 2-26-70
PROD.
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D662 IN645
D664 IN3606
DEC6534C MPS6534
DEC1008 NONE
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DISC WRITER G294
SIZE B CODE CS NUMBER G294-0-1 REV A
PRINTED CIRCUIT REV. B
DEC FORM NO. DRB 102


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
J
K
M
L
R
P
+5V +10V D OR +20V
R1 100K
R2 1.5K 1/2W
R3 1.5K 1/2W
R4 100K
R9 100K
R10 1.5K 1/2W
R11 1.5K 1/2W
R12 100K
Q1
Q2
Q5
Q6
D5 D664
D6 D664
D7 D664
D8 D664
D1 D670
D2 D670
D3 D670
D4 D670
GND, C
+5V, A
V
C1
C2
E
R5 1K
R6 4.7K
R7 15K
Q3 DEC6534C
Q4
R13 1K
R14 4.7K
R15 15K
Q7 DEC6534C
Q8
D11
D10
D9
D12
-15V, B
R8 10K
R16 10K
R17 1K
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD, 100V, 20%
DIODES ARE D662
TRANSISTORS ARE MPS6531
REVISIONS
CHK CHG NO REV
DRN. 12-1-69
CHK'D 1-12-70
ENG. 2-26-70
PROD.
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
D662 IN645
D664 IN3606
D670 IN3653
MPS6531 NONE
DEC6534C MPS6534
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE SERIES SWITCH G295
SIZE B CODE CS NUMBER G295-0-1 REV.
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
SIZE B CODE CS NUMBER G296-0-1 REV A
J
M
R
U
R5
R13
R20
R27
B,-15V
D4
C4
C3
R7 15K
R15 15K
R22 15K
R29 15K
R31
Q2 MPS6531
Q5 MPS6531
Q8 MPS6531
Q11 MPS6531
C,GND
R6 2.2K 1/2W
R14 2.2K 1/2W
R21 2.2K 1/2W
R28 2.2K 1/2W
R30
D3
C2
C1
R4 12K
R12 12K
R19 12K
R26 12K
D2
C5 22MFD 35V
D1
ANALOG GND
V
Q1
Q3
Q4
Q6
Q7
Q9
Q10
Q12
R1
R9
R16
R23
D5
R8 3K
R3
R2 1K
A,+5V
D,+10V
R11
R18
R25
E
R10 1K
R17 1K
R24 1K
K
N
T
UNLESS OTHERWISE INDICATED
DIODES ARE D662
RESISTORS ARE 10K,1/4W, 5%
CAPACITORS ARE .01MFD,100V,20%
TRANSISTORS ARE DEC6534D
REVISIONS
CHK CHG NO. REV.
00001 A
DRN. BUTLER DATE 12-1-69
CHK'D DATE 2-9-70
ENG. DATE 3-6-70
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
DEC6534D MPS6534
MPS6531 SAME
D662 1N645
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE CENTER TAP SELECTOR G296
SIZE B CODE CS NUMBER G296-0-1 REV A
PRINTED CIRCUIT REV. B
DEC FORM NO. DRB 102


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
SIZE B CODE CS NUMBER M233-0-1 REV.
S2 S1 R2 P1
M2 L1 L2 K2
J2 F2 D2 E2 D1
SERIAL DATA
T2
E3
E2
E1
DS
LD
R
DA DB DC DD
U2 V2 M1 N1
N2 P2 J1 K1
H1 F1 A1 B1
H2 CLOCK
C1 SHIFT
U1 CLEAR
E1 LOAD ENABLE
+5V, A2
+3V, V1
GND, C2, T1
R1 330 10%
R2 750
C1
C2
C3
C4
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01MFD.100V,20%
IC'S ARE DEC8271
PIN 8 ON EACH IC=GND
PIN 16 ON EACH IC=+5V
REVISIONS
CHK CHG NO. REV.
DRN. DATE 12-16-69
CHK'D DATE 1-23-70
ENG. DATE 3-11-70
PROD. DATE 12/3/70
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DISK SHIFT REGISTER M233
SIZE B CODE CS NUMBER M233-0-1 REV.
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102

APPENDIX A

TIMING TRACK WRITER

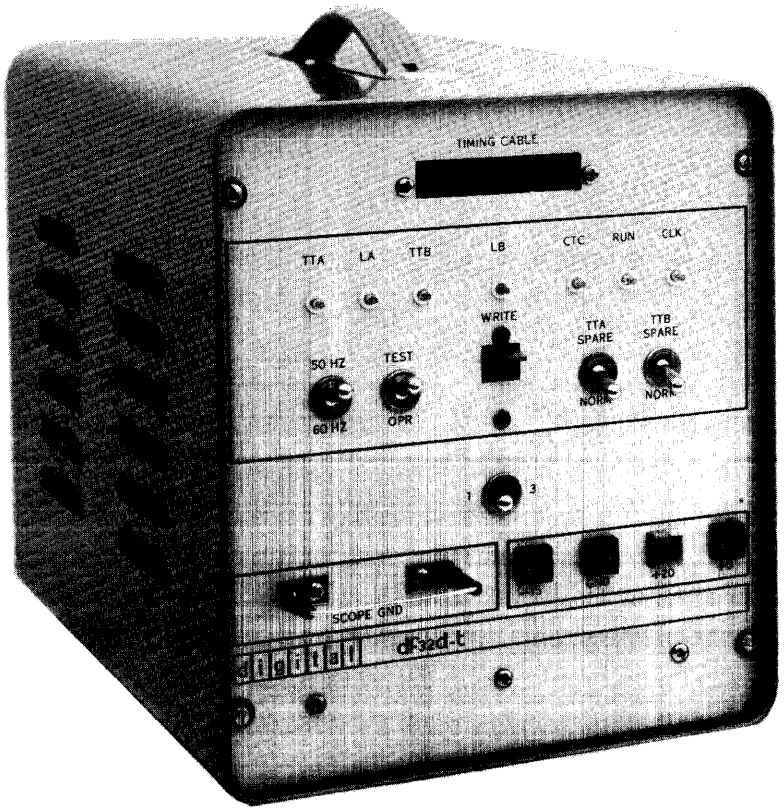


Figure A-1 DF32-D-15 Timing Track Writer

Appendix A
Timing Track Writer

A.1 INTRODUCTION

This appendix describes the DF32-D-15 Timing Track Writer (see Figure A-1). The timing track writer (TTW) is used to record the timing track and the address track on the disks of a DF32-D, E subsystem. The timing track (TTA), the address track (TTB), and a spare track for each are recorded magnetically on each disk shipped by DEC. The TTW is for field use in the unlikely event that any of the above tracks are partially or completely destroyed.

A.2 OPERATION

If the TTW is operational, use the procedure beginning with Step 1 below to record a disk. Otherwise, proceed to the TTW adjustment procedure, Paragraph A.5.

Step	Procedure
1	Turn off disk power (motor power included).
2	The TTW is a portable unit requiring only dc power, which is supplied by the DF32-D or the DS32-D. Connect power jumper cables between the disk unit power end panels and the TTW power inputs.
3	Remove the disk timing track cable from slots A32 or B32 (whichever slot it is in) of the disk unit and plug it into the TTW slot provided.
4	Set the TTW frequency switch to 50 or 60 Hz as required.
5	Set the TTW OPR/TEST switch to OPR.
6	Set the INTERLACE switch to the 1 or 3 position.
7	Turn on disk power (motor power included). Wait 2 minutes.
8	Depress the TTW WRITE switch.
9	Turn off the disk motor ac power. Wait 2 minutes.
10	Turn off the disk motor dc power.
11	Remove the disk timing cable from the TTW slot and return it to slot A32 or B32 of the disk unit.
12	Remove the dc power jumper cables.

A.3 OPERATING SWITCHES

Table A-1 lists the TTW operating switches.

Table A-1
TTW Operating Switches

Switch	Function
50 Hz/60 Hz	Selects 50- or 60-Hz operation. (TTW internal clock repetition rate differs with primary power frequency.)
TEST/OPR	Switch normally in OPR position; when in TEST position, permits repetitive cycling of the writing operation to facilitate testing and maintenance.
WRITE	Initiates a writing cycle when depressed.
SPARE/NORM	Selects either the normal TTA and TTB signals or the spare TTA and TTB signals for monitoring at the front panel TTA and TTB test points.
1/3	Selects address sequence on TTB track. When in the 1 position, the normal sequence will be recorded.

A.4 THEORY OF OPERATION

A.4.1 General

After the timing track writer has been connected into the disk system as outlined in the operating procedure, the operator depresses the front panel WRITE switch to record the TTA and TTB tracks (see Figure A-2).

When the WRITE switch is depressed, a 40-ms monostable multivibrator is enabled, and the $\overline{CLP}$ pulse is generated. $\overline{CLP}$ sets the write enable (WEN) flip-flop and clears the remaining flip-flops, the 5-stage counter, and the 12-bit shift register. During the 40 ms period in which the one-shot multivibrator is set, the disk TTA and TTB tracks are erased. When the one-shot returns to its stable state, an astable multivibrator begins to produce clock pulses (TCP). The TCP pulses are applied to the 5-stage binary counter.

Various stages of this counter are used, along with TCP pulses, to produce LA pulses. Each LA pulse complements the WFA flip-flop. WFA is applied to a disk writer module, along with the WEN signal. Recording is accomplished by the NRZI technique; therefore, a TTA pulse is recorded each time WFA is complemented.

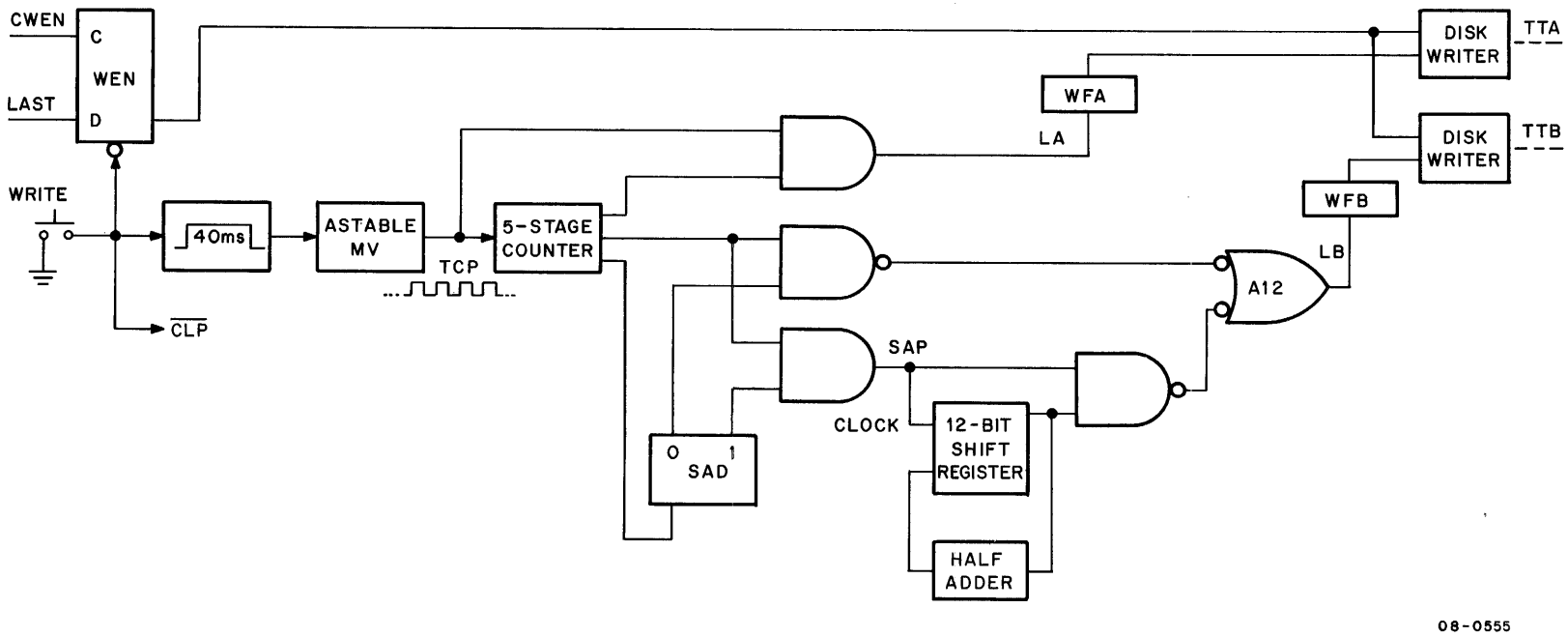


Figure A-2 TTW Block Diagram

The generation of TTB signals is more complicated than that of TTA. LB pulses are produced to complement the WFB flip-flop. LP pulses are produced in the two ways indicated by the NOR gate A12. One path is used to produce the two TTB timing pulses that are present at the start of each address word. The other path is used to produce the TTB pulses that constitute the address word, and that vary in number from 0 to 12.

The first two LB pulses are generated by various outputs of the 5-stage register, along with the 0-side of the shift address (SAD) flip-flop. The remaining LB pulses are produced by the shift address (SAP) pulses and the output from the 12-bit shift register. This procedure is described in the following section.

A.4.2 Detailed Logic Discussion (see Figure A-10)

When the WRITE switch is pressed, the generated $\overline{\text{CLEAR}}$ signal triggers a pulse amplifier (B09) and a monostable multivibrator (B11). The pulse amplifier provides the clear pulse, $\overline{\text{CLP}}$. $\overline{\text{CLP}}$ sets the write enable (WEN) flip-flop, and clears the remaining flip-flops and the 12-bit shift register, A07.

B11 generates the start run signal, $\overline{\text{SRUN}}$ 40 ms later. $\overline{\text{SRUN}}$ sets the RUN flip-flop and $\overline{\text{RUN}}$ triggers the variable clocks, B07 and B10. These clocks provide timing pulses TCP1 and TCP2 and their complements. The frequency select switch selects TCP1 and $\overline{\text{TCP1}}$ for a 60-Hz power source, or TCP2 and $\overline{\text{TCP2}}$ for a 50-Hz power source. The selected signal is then the basic timing pulse, TCP, and its complement, $\overline{\text{TCP}}$.

$\overline{\text{TCP}}$ clocks the binary counter, TC0 through TC4. The five stages of this counter are used to gate the TCP pulses through various NAND gates. TCP, thus, directly produces the following control pulses: $\overline{\text{CTC1}}$ (from NAND gate A09), which is used as a clock pulse for the shift register; $\overline{\text{LA}}$ (from NAND gate A08), which is used to complement the WFA flip-flop; and $\overline{\text{WAP}}$ (from NAND gate A12), which is used with the SAD flip-flop to provide either LB pulses or SAP pulses.

Consider first, NAND A08, which provides $\overline{\text{LA}}$ at pin S2. LA complements WFA (see Figure A-3) and each time WFA is complemented a TTA pulse is recorded on the disk. As shown on the diagram, every even TCP pulse, except number two, produces an LA pulse. The second TCP pulse is prevented from doing so by the F-BIT signal. Each timing period thus produces 13 LA pulses to complement WFA. WFA is applied to the G294 Disk Writers, A3 (for recording the spare TTA track) and A4 (for recording the main TTA track).

NAND A12 provides $\overline{\text{WAP}}$ at pin S2. When the SAD flip-flop is cleared, WAP and $\overline{\text{SAD}}$ produces LB pulses at A12, pin C1. If SAD is set, however, SAP pulses are produced by WAP, and the output of the shift register (MA11) must produce LB pulses.

The number of LB pulses varies from a minimum of two up to a maximum of 14 during each timing period (see Figure A-3). The first two LB pulses are always present. Each of the remaining 12 pulse positions

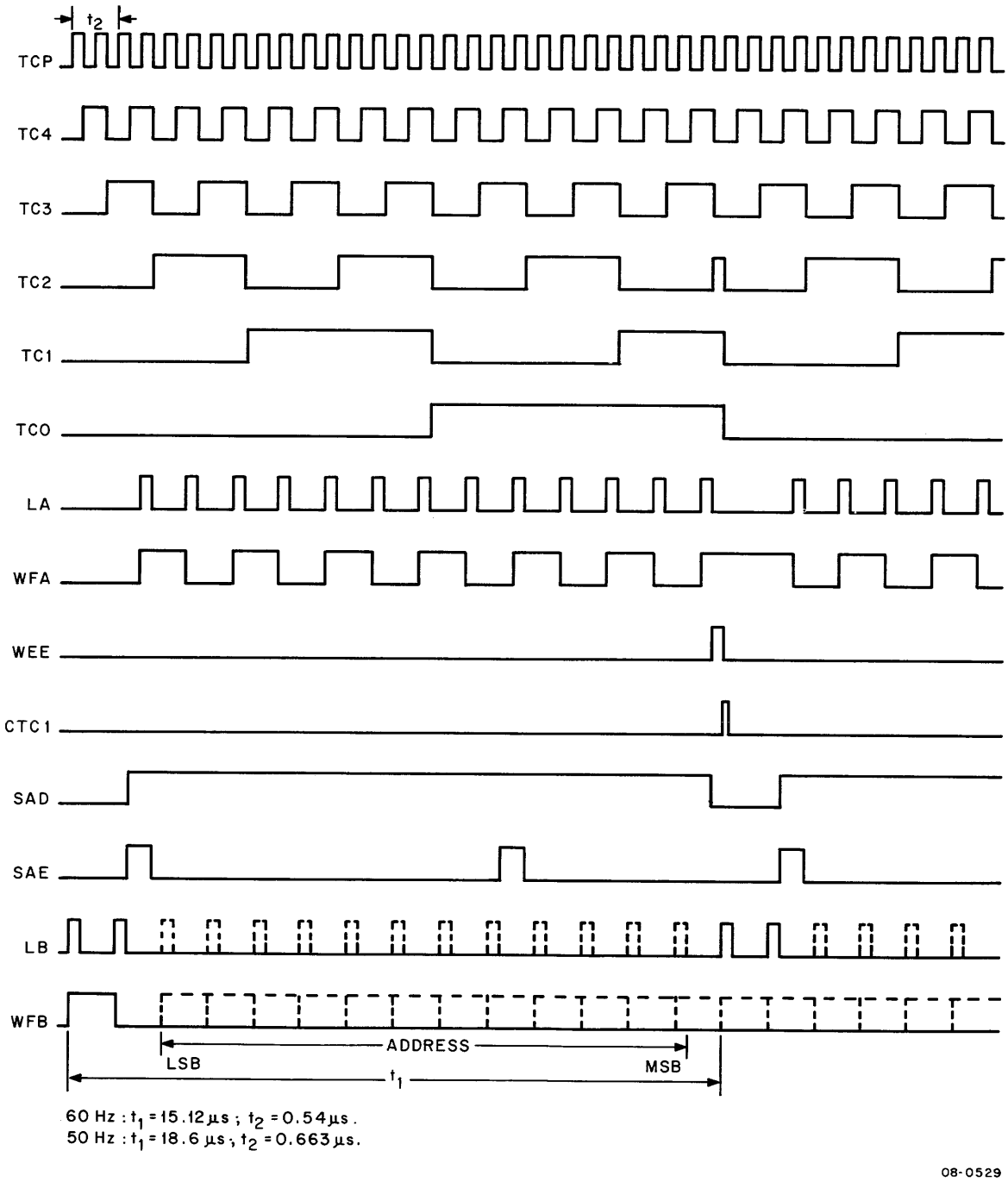


Figure A-3 Timing Diagram

represents a bit in a 12-bit binary address; therefore, the number of pulses depends upon the address represented. For example, if the octal address 0001 (binary 000 000 000 001) is to be written, LB pulse position three will be occupied; or if the address 0027_8 (000 000 010 111) is to be written, positions 3, 4, 5, and 7 will be occupied.

The first two LB pulses are produced by WAP. When SAD is set by the shift pulse $\overline{(SP)}$, the SAP pulses produce the 12 LB pulses that represent the address. Each SAP pulse generates an LB when a 1 is present in bit 12 (MA11) of the shift register, A07.

The shift register is initially cleared by $\overline{CLP}$. The first address to be written on an address track is 0000_8. When the first SAP is produced, MA11 contains a zero. LB pulse position three remains empty, WFB is not complemented, and a zero is written on the address track. This first SAP pulse also shifts the information in the register one stage to the right. Therefore, when SAP pulse two is produced, MA11 contains the information that was originally in MA10, in this case another 0. Each SAP pulse, 1 through 12, in effect, examines a stage of the shift register and produces an LB pulse when a 1 is present. The information in the shift register is circulated, rather than shifted out and lost. As a bit is shifted out of MA11, it is shifted into SPW through an adder network, which increments the address when necessary. In the case of address 0000_8, incrementation is not necessary and SAP pulse 12 returns the register to its initial count of 0000_8.

The address sequence determines which addresses are incremented. Two different sequences can be recorded on the disk. The desired sequence is selected by the INTERLACE switch, located on the front panel. The normal sequence, which will be the more desirable for most users, is selected when the switch is in the 1 position. This sequence is 0000_8, 2000_8, 0001_8, 2001_8, . . . , 1776_8, 3776_8, 1777_8, 3776_8, 6000_8, 4000_8. The alternate sequence is obtained with the switch in the 3 position. This sequence is 0000_8, 1000_8, 2000_8, 3000_8, 0001_8, 1001_8, . . . , 0777_8, 1777_8, 2777_8, 3777_8, 5000_8, 7000_8. The normal sequence will be discussed first, with all concepts explored in detail. The alternate sequence will be presented only when it differs from the normal scheme.

Consider, then, the normal sequence of addresses. The second address to be written on the track is 2000_8. Note that this count can be obtained merely by complementing stage two $\overline{(MA1)}$ of the register, which now contains address 0000_8. Stage two is complemented by parallel loading of MA1 prior to the next address period. The word end enable (WEE) pulse, in addition to clearing SAD and enabling the parallel loading of the register, enables TCP to produce $\overline{CTC1}$. $\overline{CTC1}$ then clocks in the complement of MA1. MA1 is complemented at the end of each address word period.

Note the address sequence again. Observe that some addresses, in addition to having their MA1 bits complemented, are incremented. For example: 2000_8 must be incremented and its MA1 bit complemented to obtain 0001_8; likewise with 2001_8 to obtain 0002_8. See Figure A-4. To change the address

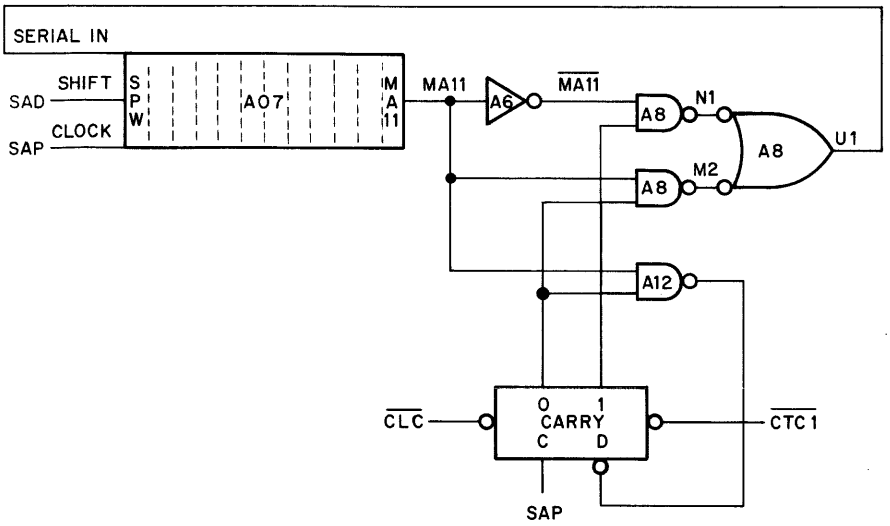
from 2000_8 at t_1 to 0001_8 at t_2, a 1 must be added to MA11. If the 1 is added prior to SAP pulse one, it will be shifted to the right by each SAP pulse until it comes to rest in MA11. As shown in Figure A-4, $\overline{\text{CTC1}}$ sets the CARRY flip-flop. The adder circuit, A8, provides a 1 for the SERIAL IN line of A07. SAP pulse one shifts the 1 into SPW, and resets CARRY at the same time. The 1 is shifted right by each SAP pulse, and SAP pulse 12 shifts it into MA11. At this point, the register contains 2001_8. At time t_2, CTC1 complements MA1 and the address becomes 0001_8.

At time t_2, CARRY is again set by $\overline{\text{CTC1}}$. The next address to be written is 2001_8, which is obtained by complementing MA1 of address 0001_8. Thus, CARRY must be reset before the next SAP pulse one, to prevent a 1 from being added to 0001_8. The reset is accomplished by $\overline{\text{CLC}}$, which is produced at the beginning of alternate timing periods (see Figure A-4).

See Figure A-5. To increment an address, NAND gate A08 is inhibited by driving pin F2 low (assume CCP and TC3 are high). To increment 2000_8, for instance, MA1 of address 2000_8 is 1, while SPW is 0. NAND gates B08 are inhibited. Therefore, pin F2 of A08 is low and the address is incremented. Conversely, 0001_8 is not to be incremented. Both SPW and MA1 of this address are 1s. NAND gate B08B is enabled; therefore, pin F2 of A08 is high. CLC is produced, clearing the CARRY flip-flop and thus preventing incrementation. One of the B08 NAND gates must be enabled if an address is to be incremented, although B08A is enabled only once, when address 6000_8 appears in the register. The addresses incremented are $3XXX_8$ and $4XXX_8$. The addresses not incremented are $0XXX_8$, $1XXX_8$, and $6XXX_8$.

After 4000_8 is recorded, the TTW must write three TTB pulses and end the writing operation. These pulses signify the beginning of the gap, the blank space on the disk between address 4000_8 and address 0000_8. The disk completes one revolution in approximately 33 ms (for 60-Hz operation). The TTW records the TTB track in approximately 31 ms, leaving a 2-ms gap. The DF32-D logic uses the 3 TTB pulses in timing operations involving this gap. When address 4000_8 is incremented and its MA1 bit is complemented, the result is 6001_8. The first two LB pulses of this address period produce two of the required three TTB pulses. The third is produced as follows.

In Figure A-10, locate the A12 NAND gate, pins D2, E2, and F2. The gate inputs are SPW and MA11. When 4000_8 is incremented and its MA1 bit complemented, SPW and MA11 become true (4000_8 becomes 6001_8). The signal $\overline{\text{LAST}}$ is produced. This is applied to the data inputs of the RUN and WEN flip-flops. If a pulse is applied to the clock lines of these flip-flops, they are cleared and the writing operation ceases. The SAE pulse, used for this purpose, is produced by NAND gate A09 at pin J2. Note on Figure A-3, this pulse is produced immediately after the first two LB pulses, thus, the writing operation ends before any address bits are recorded. The writing operation seems to end before the third TTB



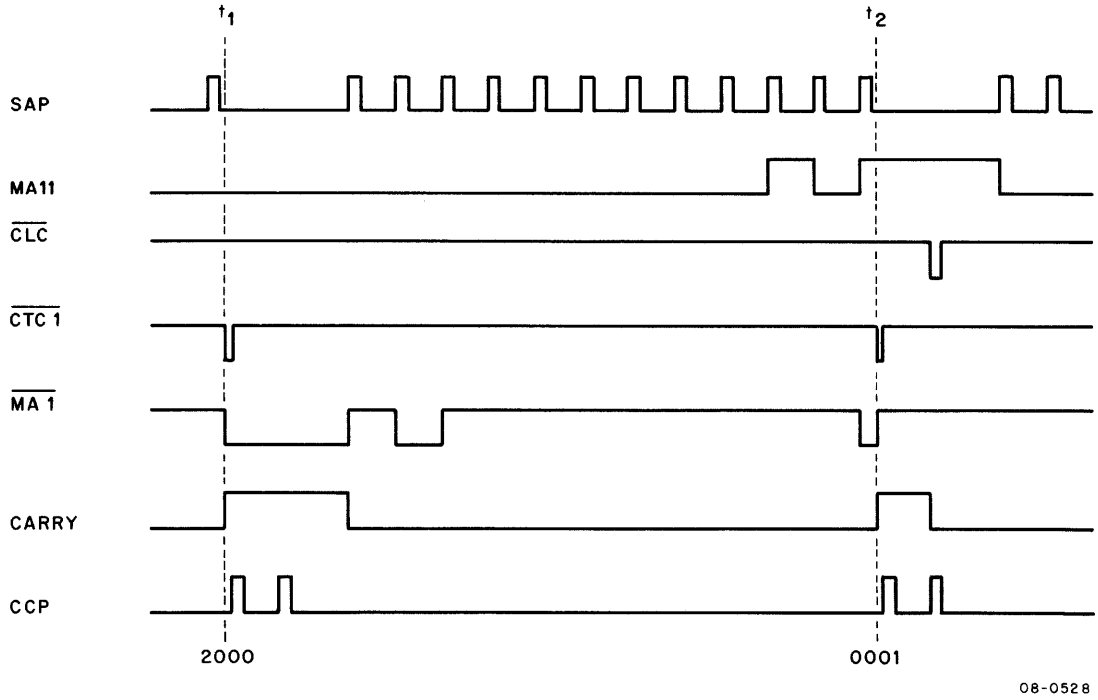


Figure A-4 Address Word Incrementation

pulse is generated; however, note that when WEN is cleared by SAE, WFB is cleared by the resulting negative transition on the WFB DC-clear line. Note also, that the 0.027-μF capacitor on the output pin, V2, of NAND gate B08, produces an exponential decay of the WEN H signal. Thus, the TTB disk writer module is still enabled when WFB undergoes its last transition, and the third TTB pulse is recorded (see Figure A-6).

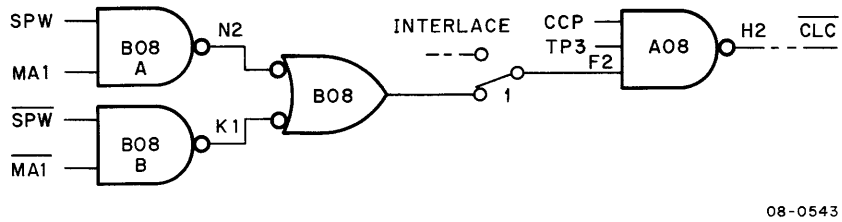


Figure A-5 Address Increment

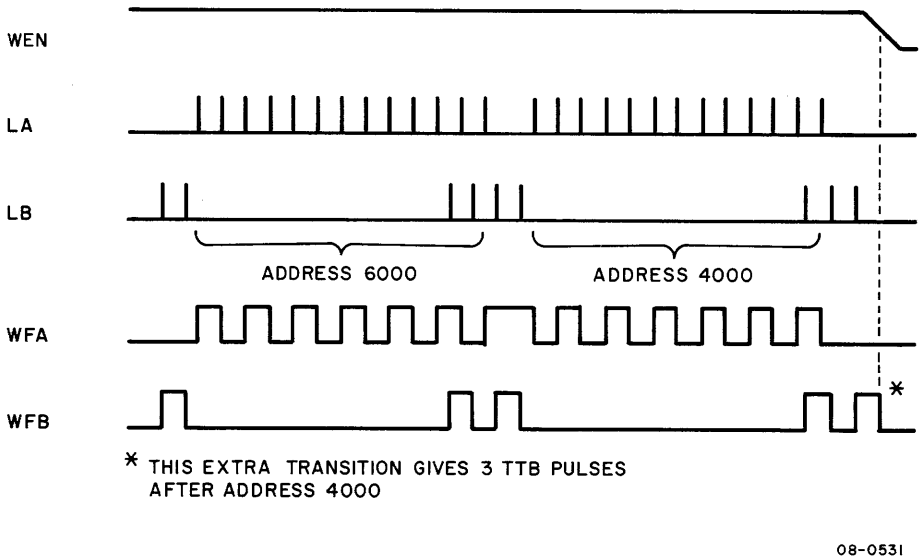


Figure A-6 Last TTB Generation

The same procedure is used when the alternate address sequence is recorded. There is very little additional logic required to produce this sequence. Recall that the address sequence is 0000_8, 1000_8, 2000_8, 3000_8, 0001_8, 1001_8, . . . ,0777_8, 1777_8, 2777_8, 3777_8, 5000_8, 7000_8. The first four addresses differ only in the bit values assigned to MA1 and MA2. For instance, both bits are 0 in address 0000_8; both are 1 in address 3000_8. These two bit positions are controlled by the logic circuits represented in Figure A-7.

Figure A-7 shows the INTERLACE switch in the 3 position. Address 0000_8 is recorded as described for the normal sequence. Next, the content of the register is converted from 0000_8 to 1000_8 by complementing the MA2 bit. The MA2 bit is complemented by inverting the MA2 bit in NOR gate B12A and applying it to the parallel load input. Then, the complement is clocked in by the CTC1

pulse, as in the normal address sequence. Address 1000_8 is recorded. To convert from 1000_8 to 2000_8, MA2 is again complemented. In addition, MA1 is complemented, using the half-adder circuit. To convert from 2000_8 to 3000_8 only MA2 is complemented. As a result, 3000_8 is stored in the register. The next address to be recorded is 0001_8. To obtain this address, MA1 and MA2 are complemented as before, and 3000_8 is incremented (remember that an address is incremented before being complemented) via gates B12E and B12F.

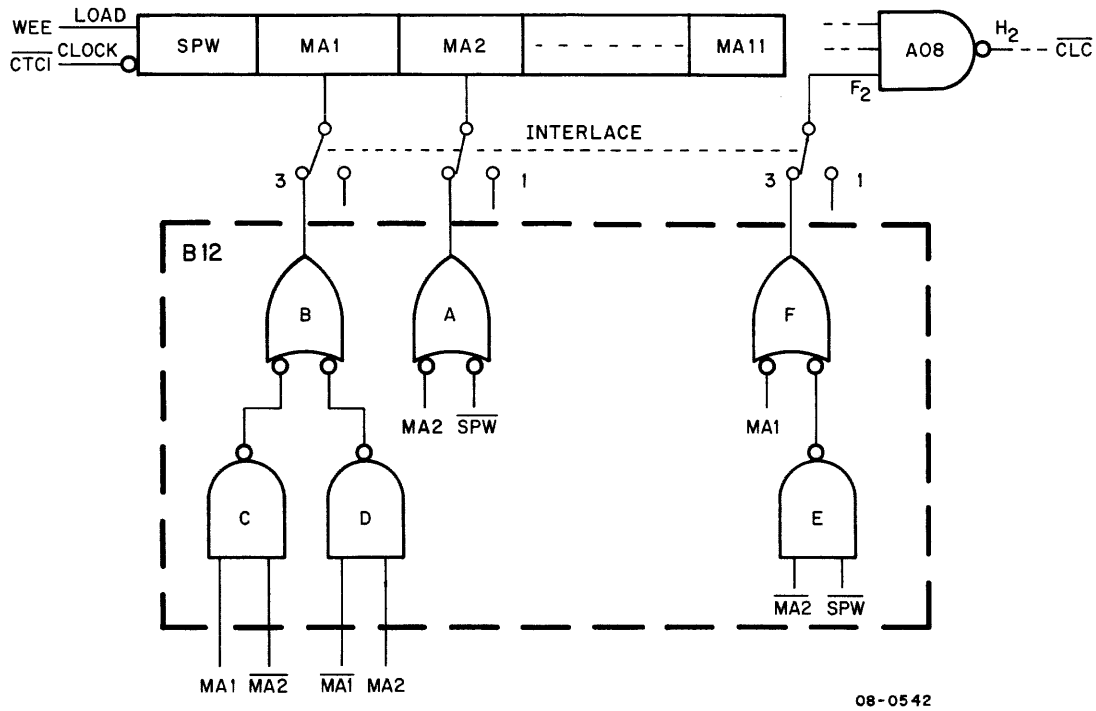


Figure A-7 Alternate Address Logic

In Figure A-4 $\overline{CLC}$ is used to reset the CARRY flip-flop. If $\overline{CLC}$ is not generated, the address currently in the register will be incremented (i.e., 2000_8). NOR gate B12F inhibits NAND A08 when MA1 and MA2 are 1. CLC is not produced, consequently, each $3XXX_8$ address is incremented. To convert from 3000_8 to 0001_8, the address is first incremented from 3000_8 to 3001_8, both MA1 and MA2 are complemented. The series of addresses from 0001_8 to 3000_1 is produced in exactly the same way as the series 0000_8 to 3000_8. This process continues through address 7000_8. Since both MA1 and MA2 of address 7000_8 are 1, the address is incremented and complemented. Address 6001_8 is produced in the register, but before it can be recorded, LAST is generated as described for the normal sequence.

The entire writing operation requires less than 80 ms. The operation is completed in one cycle; therefore, provision must be made for repetitive cycling to facilitate testing and maintenance. Thus,

the OPR/TEST switch and the second 40-ms monostable multivibrator are included. Figure A-8 shows how the writing cycle is made repetitive. The first 40 ms of the cycle are used to clear the TTA and TTB tracks, the second 40 ms (only 31 ms are needed) are used to record the tracks.

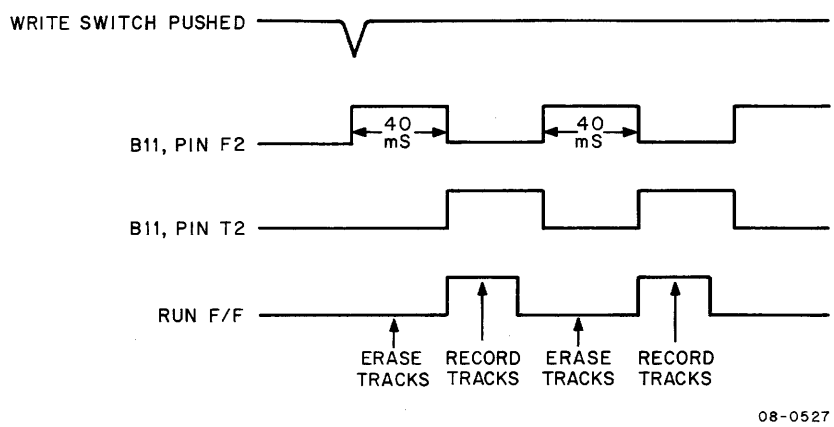


Figure A-8 Timing Write Cycle (Test)

A.5 ADJUSTMENT PROCEDURE

The following procedure is recommended if the timing track writer has not been adjusted or checked:

Step	Procedure
1	Turn off dc power.
2	Remove TTW from case. Connect power to the TTW using dc power jumper cables between DISK power end panel tabs and TTW power inputs.
3	Turn on dc power.
4	Turn frequency switch to 60 Hz or 50 Hz as required. Turn TEST/OPR switch to TEST.
5	Put the NORM/SPARE switch in the NORM position.
6	Using an oscilloscope equivalent to a Tektronix Type 543A, plug the scope sync lead into the RUN plug.
7	Use channels A and B to observe LA and LB (front panel of TTW). Adjust word length time between a set of 15 LB pulses (or 15 LA pulses) to t_1 for: 60 Hz: $15\ \mu s \leqslant t_1 \leqslant 15.5\ \mu s$, ideally $t_1 = 15.12\ \mu s$ 50 Hz: $18\ \mu s \leqslant t_1 \leqslant 19\ \mu s$, ideally $t_1 = 18.6\ \mu s$ This adjustment is made by potentiometer adjustment of M401 modules in slot B10 for 60 Hz, and slot B07 for 50 Hz. An approximate check may be made on t_2.

Step	Procedure
7 (Cont)	60 Hz: $t_2 = 0.54\ \mu s$ (See Figure A-3) 50 Hz: $t_2 = 0.66\ \mu s$
8	Observe LA and LB on channels A and B of the scope. The relationship for the first two addresses is shown in Figure A-9. The addressing sequence should be 0000, 2000, 0001, 2001, etc.
9	Use the delayed sweep to observe the trailing edge of WEN (A3H2) and WFB (A11E1) on two channels. The waveforms should appear as in Figure A-6.

CAUTION

If Step 9 is performed with the timing cable plugged in, the TEST/OPR switch MUST be in OPR position. The WRITE pushbutton should be depressed.

10	TTA and TTB can be observed on channel A and channel B of the scope by turning the NORMAL/SPARE switch as desired. The relationship of the waveforms should be similar to the LA/LB relationship. This verifies the operation of G294 modules and G085 modules. To isolate a problem, the outputs of the writer can be observed. These outputs should appear the same as respective inputs WFA or WFB except the swing should be between +18V and -15V (differential) when the timing head cable is connected. If the writer outputs appear to be correct, and TTA/TTB do not, then the G085 modules need potentiometer adjustment of the gain and slice levels.

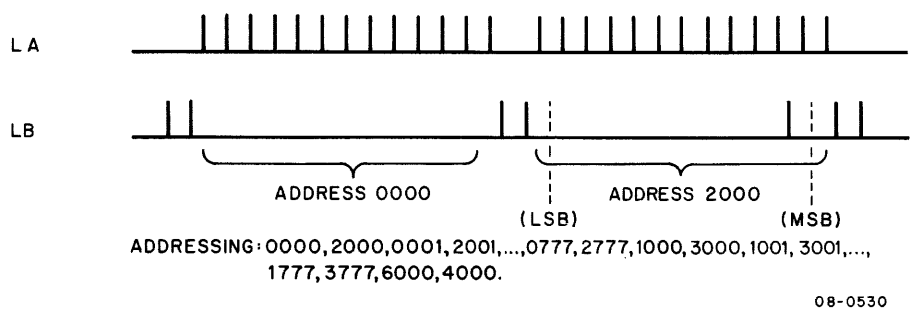


Figure A-9 LA-LB Relationship

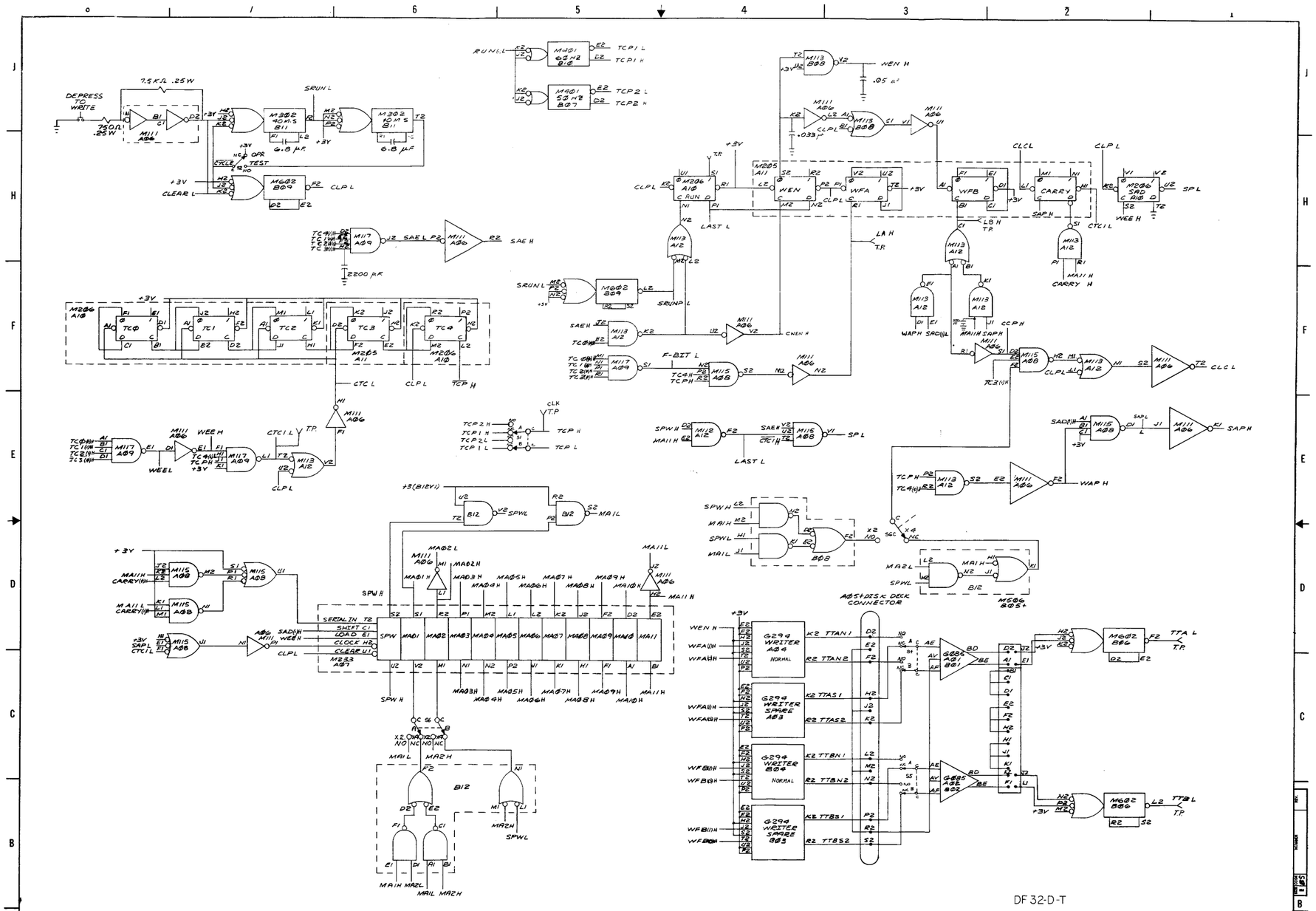


Figure A-10 Timing Track Writer

Digital Equipment Corporation
Maynard, Massachusetts

printed in U.S.A.