EK-DYS50-TM-001

DYS50

Technical Manual

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of
Digital Equipment Corporation

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PREFACE

This hardware technical manual, like most technical manuals, tends to be all-inclusive. The information is not restricted to a single audience. It is addressed instead to several audiences -- none of which is expected to be interested in the entire document. Individual chapters, however, are audience-specific. For those who want to know what to read, and what not to read, the following describes the chapters.

Chapter 1 Introduction
This chapter defines the DYS5Ø. The chapter is for the individual who wants a quick summary of: the DYS5Ø's function, its relationship to the DECdataway, and its available options.

Chapter 2 Installation
This chapter contains the information and level-of-detail needed by individuals who do the installation. It tells how to unpack, inspect, mount, and power-up the DYS5Ø. It also tells how the unit should operate when first turned on, and how to implement some of its interfaces.

Chapter 3 Maintenance
This chapter is for the Field Service or other maintenance person who troubleshoots and repairs a failed DYS5Ø. It tells how to isolate a faulty Field Replaceable Unit (FRU), and, once found, how to replace it with a new FRU.

Chapter 4 ISV11-B Description
The first few paragraphs of this chapter are of general interest. They contain a short functional description of the ISV11-B. The remainder of the chapter contains a detailed description of the ISV11-B logic as shown in the field maintenance print set. It is included so that engineers and component-level service technicians will have a permanent record of this information.

Chapter 5 BA11-Y Power System Description

This chapter contains a complete physical and electrical description of the BA11-Y mounting box. That is, the box that the DYS5Ø modules are plugged into. It describes in detail: all power supply circuits, power distribution, and all backplane and chassis wiring for the entire BA11-Y box. It is included here for reference, and so that engineers and component-level troubleshooting technicians will have a permanent record of this information.

CHAPTER 1
INTRODUCTION

1.1 DEFINITION AND SCOPE

The DYS5Ø is an LSI-11/23B microcomputer with a DECdataway network interface. This configuration is called a DECdataway Intelligent Subsystem (DIS). The DYS5Ø functions as a fully programmable DECdataway network node. It operates in an execute-only environment under the RSX11-S operating system. It is not a development subsystem.

The DYS5Ø is a product of DIGITAL's Manufacturing Distribution and Control (MDC) group. This group designs hardware and software for industrial local-area networks called DECdataway (DY) systems. DYS5Øs are the intelligent elements in these networks.

The DECdataway also supports other devices besides DYS5Øs, but these are fully described in their own manuals. This manual is about the DYS5Ø only. Moreover, it is strictly a hardware manual. It tells what a DYS5Ø is, and how to install, operate, troubleshoot, and maintain it. It contains functional and physical descriptions of the DYS5Ø subsystem and a detailed description of its DECdataway interface, the ISV11.

Where appropriate, some ancillary topics are discussed, but not in any depth. For example, this manual does not fully describe: the DECdataway, the DYS5Ø's processor, its memory, or its peripherals. These devices are not unique to the DYS5Ø. Their detailed descriptions are contained in separate manuals. Neither does this manual describe DYS5Ø operating or maintenance software. These subjects also are fully discussed in separate manuals.

Finally, a DYS5Ø installation presumes a DY network installation. This manual is, therefore, just a small part of your total system documentation package. The total package includes not only all documents for your particular DY system's hardware complement, but several DY system operating and maintenance software documents as well. Paragraph 1.6 lists several existing documents that specifically address these topics.

1.2 INTRODUCTION

Figure 1 shows a DYS5Ø with its front door removed and module cover cut away. It consists of a mounting box and four modules. From the top, the four modules are: a processor, memory, and DECdataway interface (2 modules). The following describes the modules further.

BA11-YA	Mounting box with power supply, backplane, and front panel controls
KDF11-BB	Processor (M8189 module)
MSV11-PK	256 KB memory (M8Ø67-KA module)
ISV11-B	DECdataway interface (consisting of an M8Ø8Ø module, an M8Ø84 module, and an interconnecting cable)

There are five empty slots for peripheral interface options.

1.3 FEATURES

Components of the DYS5Ø have a number of significant features that, taken together, make it an efficient and versatile performer in most any distributed processing application. A brief summary of the important features follows.

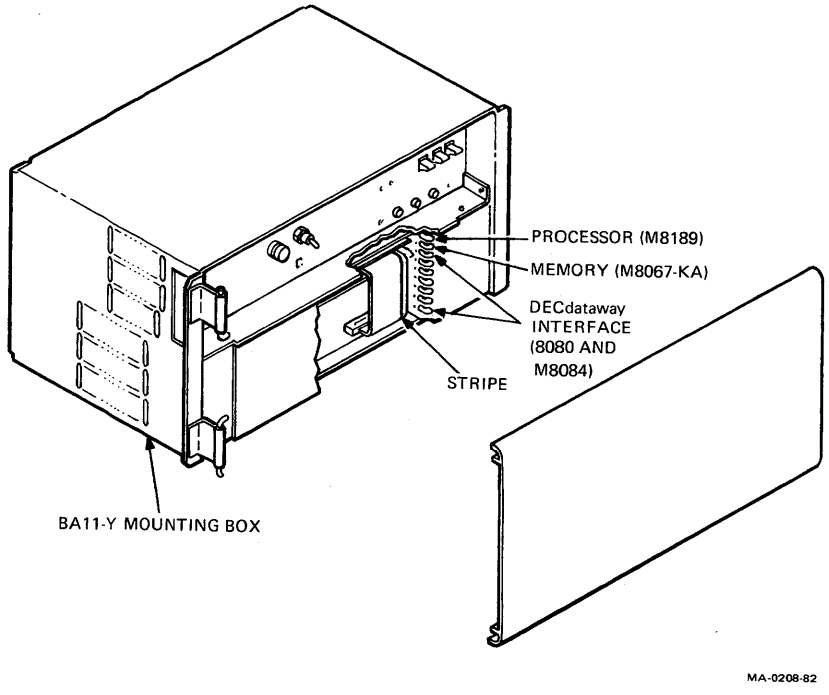


Figure 1-1 Basic DYS5Ø

1.3.1 KDF11-BB Processor (M8189)

This quad-height module contains: a central processor, memory management, line frequency clock, BDV11 compatible bootstrap and diagnostic ROM, two serial line units, floating point, and 22-bit addressing.

1.3.2 MSV11-PK Memory (M8Ø67-KA)

This quad-height module contains 128K words of metal oxide semiconductor (MOS) random access memory (RAM). Words are 18-bits -- 16 data and 2 parity.

1.3.3 ISV11-B DECdataway Interface

This unit consists of two modules: the M8Ø8Ø and the M8Ø84. They are connected together with a short ribbon cable. The ISV11-B is the DYS5Ø's interface to the DECdataway and the host computer. It has in it a microcomputer that is programmed to manage communications between the host and the DYS5Ø's LSI-11/23B. It starts, stops, boots, and runs power-up diagnostics on the DYS5Ø. Chapter 4 contains a complete description of the ISV11-B.

1.3.4 BA11-Y Mounting Box

This is the DYS5Ø enclosure (Figure 1-2). It contains an H9276 nine-slot, extended (22-bit) LSI-11/23 backplane, and an H7861 power supply that provides +5 volt, and +12 volt power to the backplane. The BA11-Y is just 26.67 cm (1Ø.5 inches) high, and only 27.94 cm (11 inches) deep. All modules, cables, controls, adjustments, and test points are front-accessible, which makes the DYS5Ø very easy to service. The BA11-Y is equipped for easy mounting in either a NEMA-12 industrial type enclosure, or in a standard cabinet. Both the backplane and power supply are Field Replaceable Units (FRUs); they can be swapped in a matter of minutes.

1.4 GENERAL DESCRIPTION

The best way to understand how a DYS5Ø works is to look at its relationship to the DY system of which it is a part. For that reason, we will begin with just a brief, and much simplified description of how a DY system works. Readers interested in a comprehensive treatment should consult the references listed in Paragraph 1.6.

1.4.1 DY Systems

In its simplest form, a DY network has a centrally-located (host) computer, and multiple, remotely-located, smaller computers. The remotes can be placed anywhere in the local area where dedicated processing is needed. Completing the network is a communication channel called the DECdataway, which connects the host and all remotes together (Figure 1-3).

As the figure shows, DYS5Øs are the distributed elements of the network. The host system can be either a VAX/VMS or PDP-11 computer, running RSX11-M or RSX11-M PLUS.

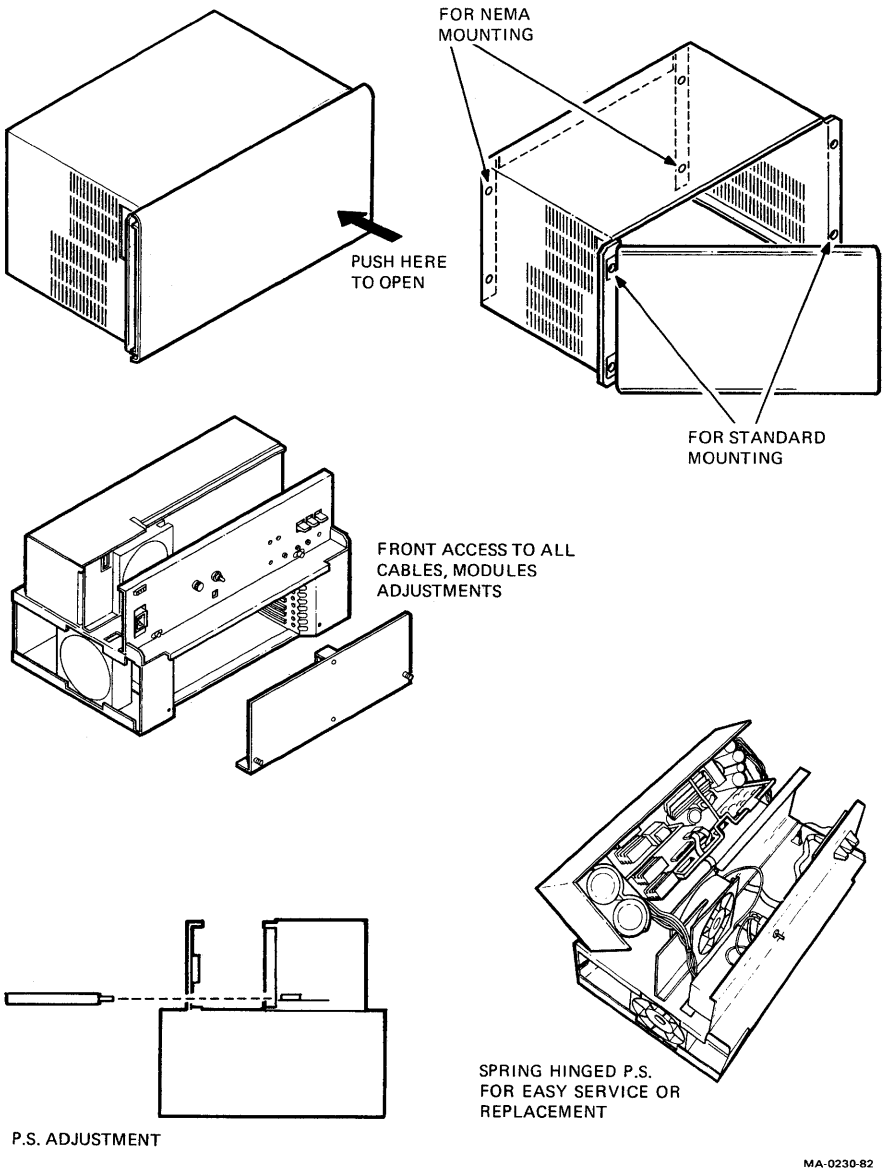


Figure 1-2 DYS5Ø Enclosure Features

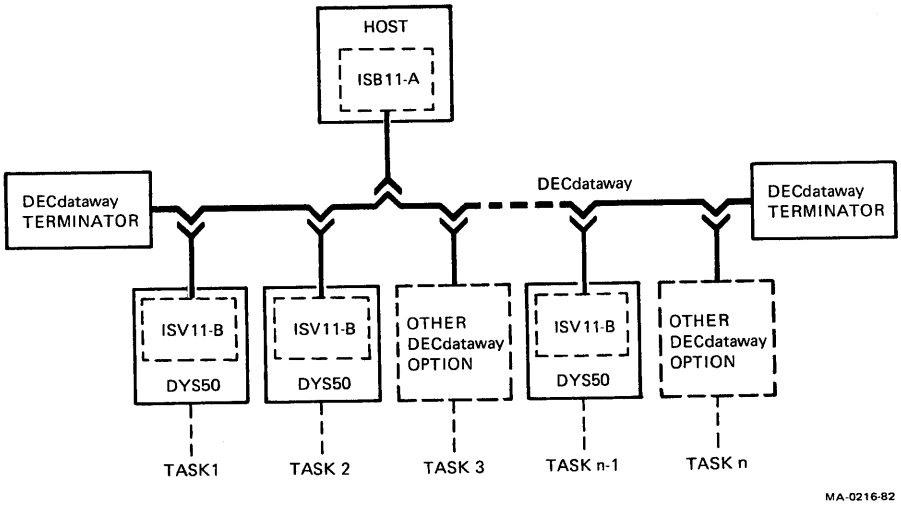


Figure 1-3 A Typical DY System

Because they are linked by the DECdataway, DYS5Øs are DECdataway subsystems, and because they are programmable they are called intelligent subsystems. Thus the name: DECdataway Intelligent Subsystem (DIS).

DYS5Øs are fully programmable and are therefore not dependent on the host for performance at their dedicated functions. What role does the host play? The host is able to communicate with all DYS5Øs via the DECdataway. It can, therefore, effect communications between tasks in different parts of the network.

It can also start, stop, and monitor the progress of each DYS5Ø task so that a large system can be sensibly managed by controlling all its subsystems in a manner that optimizes total system output and economy.

The economies are of several types. For example, DYS5Øs are fully programmable, but they serve local processing needs in an execute-only mode. They do this by running programs that have been developed at the host and down-line loaded to them via the DECdataway. Thus the additional hardware and software tools normally needed for program development are required only at the host -- a considerable economy in a large system.

Other economies are achieved because the host can also share its database or mass-storage devices with the remote systems. All this is in addition to the fact that distributing the processing power in the first place breaks an entire project into smaller, more manageable tasks, and in so doing it achieves economies of convenient location, reduced wiring costs, modularity, and improved response.

Finally then, although DY system implementations may vary considerably from one application to another, they have in common a major attribute: they modularize a large task into several smaller, more manageable ones, which can be physically dispersed for optimum convenience and efficiency. And the DYS5Ø is the principal means of accomplishing this modularization.

1.4.2 DYS5Ø Functional Description

Recall that a DYS5Ø runs its own local programs, and that the DECdataway network host relates to it and all other DECdataway devices as a sort of manager. Figure 1-4 shows the physical relationship between a single DYS5Ø and: the DECdataway, the host, and the local task. From this figure it can be implied that the DYS5Ø needs at least three things: a DECdataway interface, a local task interface, and a computer to run the programs.

A block diagram of the DYS5Ø only (Figure 1-5) shows this in more detail. The figure is a familiar enough looking LSI-11 computer block diagram with the exception of the block labeled DECdataway interface, which makes the DYS5Ø functionally unique. It is the only part of that figure that requires further discussion in this manual, and a complete description of it is presented in Chapter 4. Discussions of the LSI-11/23B computer and its various I/O options are contained in the references.

The ISV11-B takes DECdataway serial-type messages, which are in DIGITAL serial bus control (DSBC) protocol format, and converts them to LSI-11 bus-compatible parallel address and data format.

It then makes a DMA transfer of this data to the DYS5Ø's LSI-11 memory. It performs the reverse of this process when transferring DYS5Ø data to the DECdataway.

The DYS5Ø normally serves its local function by running its program and processing interrupts until it receives a message from the host via the DECdataway. The message may contain a command for the DYS5Ø to start, or halt, or perhaps simply receive or transmit some data. The DYS5Ø responds as it would to any other device in its I/O page. Of course, in addition to the hardware, there is network software that must be in place (both in the host and the DYS5Ø) to make it all work. These matters are the subject of several references listed in Paragraph 1.6.

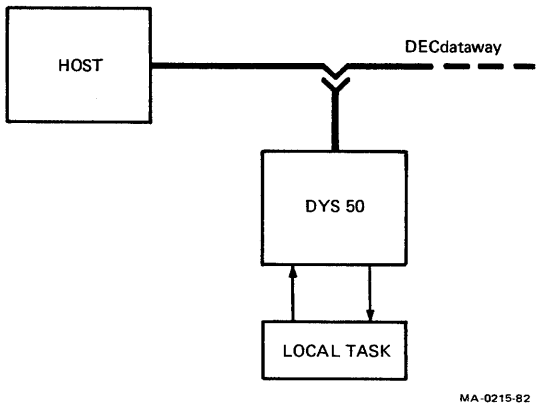


Figure 1-4 A Single DYS5Ø

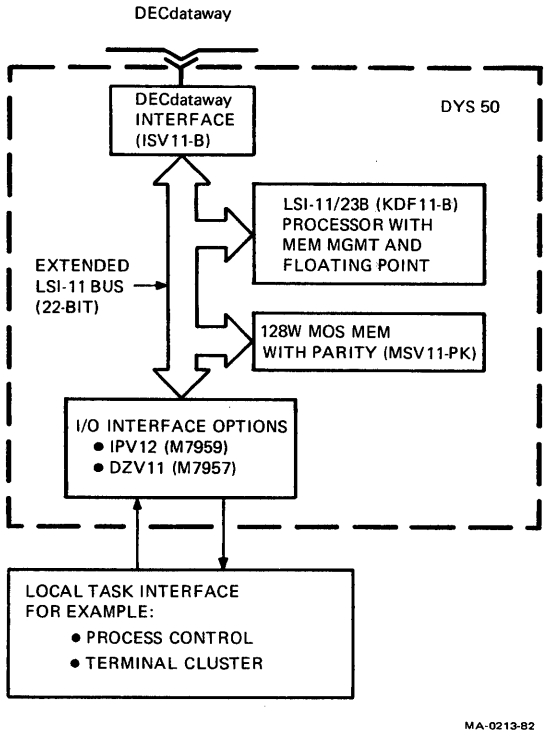


Figure 1-5 DYS5Ø Block Diagram

1.5 TYPICAL DYS5Ø CABINET CONFIGURATIONS

Figures 1-6 and 1-7 show some typical configurations for H9646 cabinets. These figures show equipment that would be used with the DYS5Ø in a process control application. Figures 1-8 and 1-9 show similar equipment configured in an H96Ø cabinet.

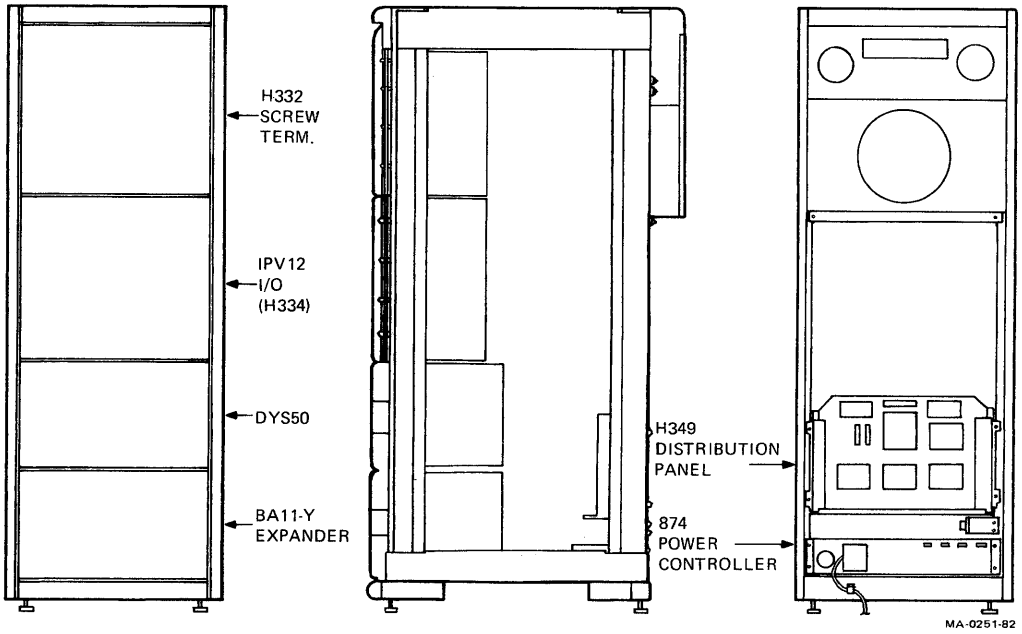


Figure 1-6 H9646 Cabinet Configuration

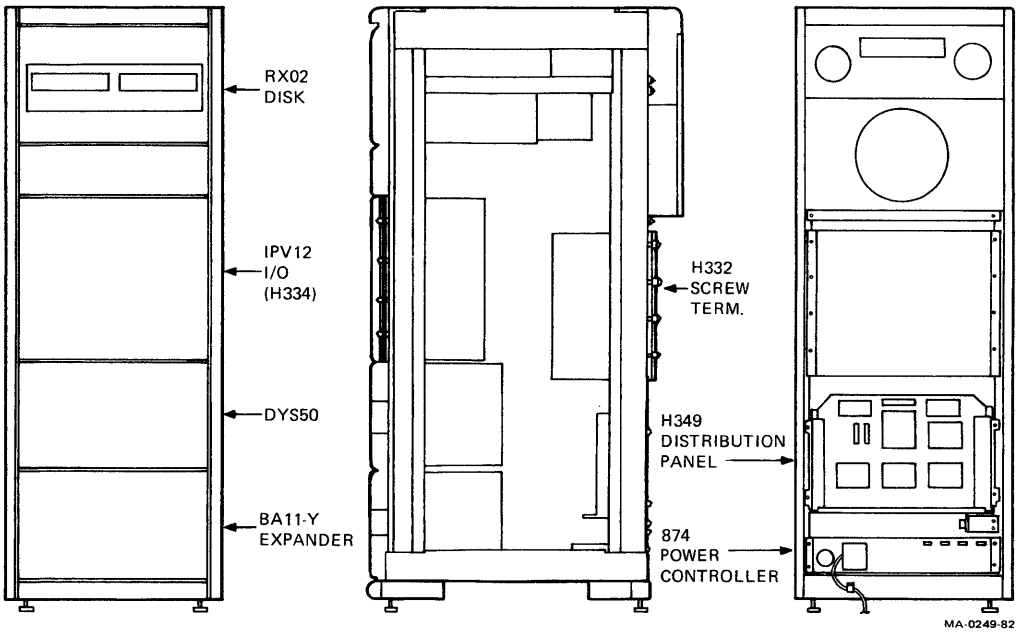


Figure 1-7 H9646 Cabinet Configuration

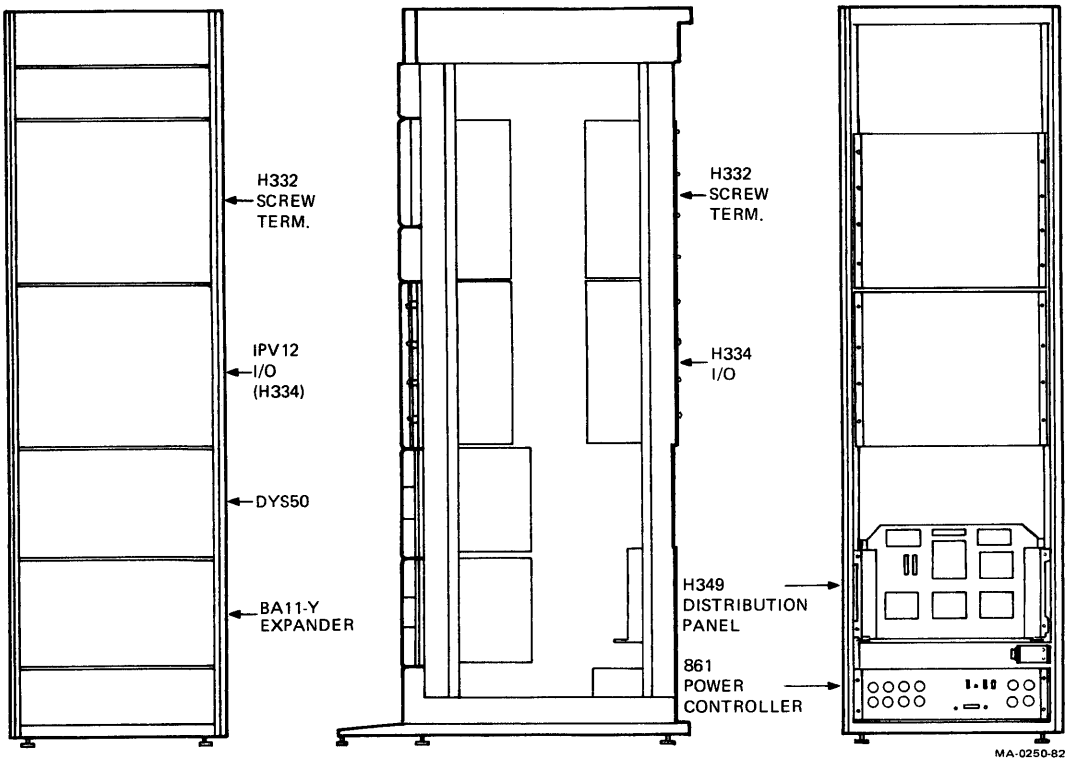


Figure 1-8 H960 Cabinet Configuration

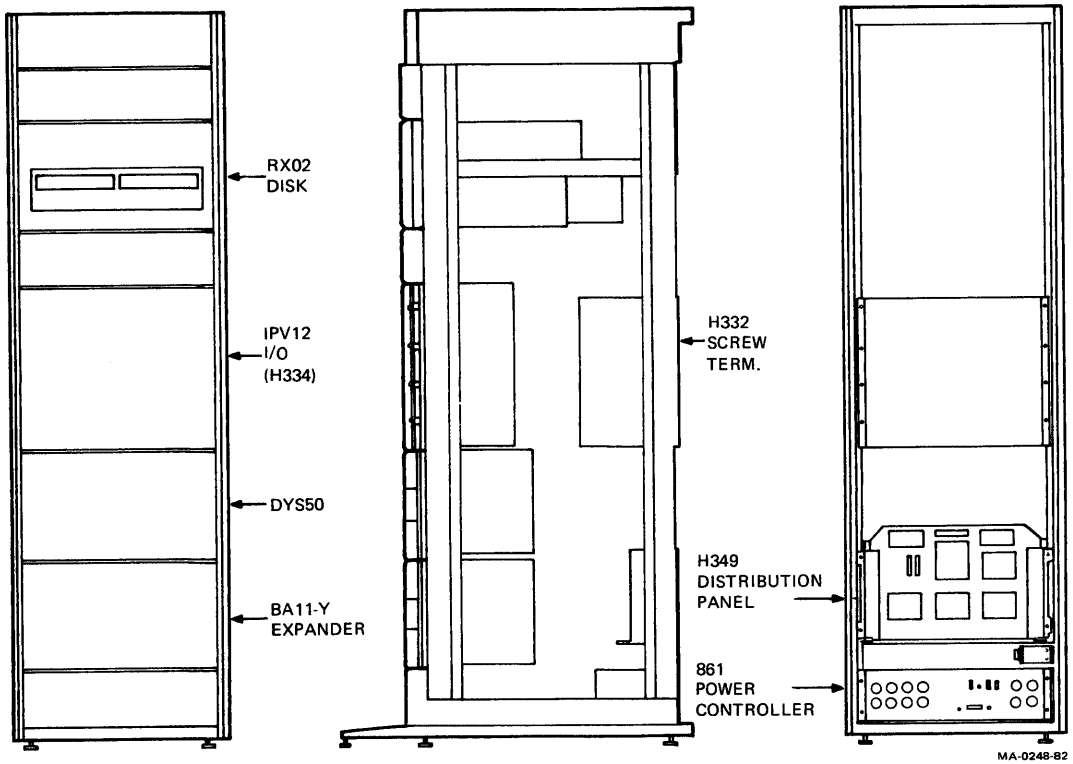


Figure 1-9 H960 Cabinet Configuration

1.6 RELATED DOCUMENTS

The following documents are shipped with your DYS5Ø.

Title	Document Number
DYS5Ø Technical Manual	EK-DYS5Ø-TM
DYS5Ø Pocket Service Card	EK-DYS5Ø-PC
KDF11-BA CPU Module User's Guide	EK-KDFEB-UG
MSV11-P User Guide	EK-MSVQP-UG
DYS5Ø Field Maintenance Print Set	MP-Ø1403
KDF11-BA Field Maintenance Print Set	MP-Ø2136
MSV11-P Field Maintenance Print Set	MP-Ø1239
ISV11-B Field Maintenance Print Set	MP-ØØ6Ø9
BA11-Y Field Maintenance Print Set	MP-Ø1402
Microcomputer Interfaces Handbook	EB-2Ø175-2Ø/8Ø

The following related documents can be ordered from:

Digital Equipment Corporation
Accessories and Supplies Group
P.O. Box CS2ØØ8
Nashua, New Hampshire Ø3Ø61

Title	Document Number
Digital Site Preparation Guide	EK-OCORP-SP
I/O Subsystem User Guide	EK-ØPIOS-UG
DECdataway User Guide	EK-ISB11-UG
DPM Diagnostic User Guide	EK-DPMØØ-DM
VAX-11 DY32 Hardware Installation and Diagnostic User Guide	EK-ØDY32-UG
Serial Bus Exerciser Write Up	MD-11-CZKCH-D
Remote Terminal Tester Write Up	MD-11-CZKCI-D
Diagnostic Monitor Write Up	MD-11-CZKMP-D
DPM/DPM-PLUS Documentation Set consisting of the following:	
DPM/DPM-PLUS Dataway Intelligent Subsystem User Guide	AA-J529B-TC
DPM/DPM-PLUS Terminal User Guide	AA-J53ØB-TC
DPM/DPM-PLUS System Generation and Management Guide	AA-J531C-TC
DPM/DPM-PLUS Release Notes	AA-K16ØB-TC
DPM/DPM-PLUS Mini-reference	AV-M195A-TC

In addition to documentation, DYS5Ø maintenance training is also available from DIGITAL. Contact your local DIGITAL representative for details.

1.7 SPECIFICATIONS

The following are the specifications for the DYS5Ø.

CPU	KDF11-BB
Memory	128K words MOS memory
Voltage/Current	
DYS5Ø A/D	6 A maximum at 115 V 3 A maximum at 23Ø V
Frequency	47 Hz to 63 Hz
Power	69Ø VA, PF=Ø.6 minimum
Ride-through	15 milliseconds minimum
Input protection	Fast-blow fuse: 1Ø A for 115 V operation, 5 A for 23Ø V operation

Environmental

NOTE

When other equipment is mounted in the same cabinet as a DYS5Ø, use the environmental limits of the product with the minimum environmental capability.

Temperature	
Operating	5° to 5Ø° C ambient (41° to 122° F)
Nonoperating	-4Ø° to 66° C ambient (-4Ø° to 151° F)

NOTE

The maximum allowable operating temperature is based on operation at sea level. The maximum allowable operating temperature is reduced by a factor of 1.8° C/1ØØØ m (1.Ø° F/1ØØØ ft) for operation at high altitudes.

Humidity	
Operating	1Ø percent to 95 percent RH 32° C (89.6° F) maximum wet bulb 2° C (35.6° F) minimum dew point
Nonoperating	1Ø percent to 95 percent RH (noncondensing)
Altitude	
Operating	2.4 km (8,ØØØ ft)
Nonoperating	9.1 km (3Ø,ØØØ ft)

Physical		
Height		26.416 cm (10.4 in)
Width		48.26 cm (19 in)
Depth	(with door)	32.537 cm (12.81 in)
	(without door)	29.464 cm (11.6 in)
Weight		20.9 kg (46 lbs)

ADDITIONAL SPECIFICATIONS

Specifications for all LSI-11 microcomputer components contained in the DYS50 are provided in the Microcomputer Processor Handbook and the Microcomputer Interfaces Handbook.

Specifications for the remaining DYS50 components, except the ISV11-B, are provided in their respective user guides. The appropriate manuals are shipped with each system. Specifications for the ISV11-B are listed in Chapter 4.

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter tells how to install the DYS5Ø. Included are instructions for unpacking, inspecting, interfacing, connecting primary power, and preparing the system for operation. Finally, there is a short checkout procedure that establishes whether or not the basic DYS5Ø is operational.

The chapter does not cover installation of peripheral devices that interface with the DYS5Ø. It covers only: installation of the basic DYS5Ø, its interfaces, and some guidelines for its expansion. Peripheral devices for the DYS5Ø are installed per instructions in their respective manuals, one of which is included with each device. These manuals are referenced where appropriate. Chapter 1 includes a list of documents shipped with the basic DYS5Ø.

2.2 SITE PREPARATION

The DYS5Ø is only one of several devices that can be connected to the DECdataway, and is only one part of a larger host-based system. This means that its site preparation is provided for in the preparations for the DECdataway. Therefore its assigned location should have a DECdataway remote device interface connector and the appropriate primary power receptacles.

Final positioning of a DYS5Ø cabinet must allow sufficient clearance from any obstruction that might hinder air flow to the cabinet, or easy access by service personnel.

CAUTION

To maintain stability in operating and servicing positions, DYS5Ø cabinet configurations must be secured to the floor or an adjacent cabinet.

2.2.1 Site Power Requirements

Site Power Receptacles do not necessarily mate directly with the DYS5Ø. And which receptacles are required depends not only on whether the DYS5Ø is 115 Vac or 23Ø Vac, but also on whether or not a cabinet power controller is being used. The power controller requirements are different because, since it usually powers more than one device, its current rating is higher.

For example, if the DYS5Ø is going to plug directly into a site power receptacle, then that receptacle must be, for example, either a type A or type B (for 115 Vac or 23Ø Vac operation respectively). If, on the other hand, the DYS5Ø is going to plug into a cabinet power controller, the power controller must have type A or B receptacles for the DYS5Ø, but the power controller itself requires a type C or D site power receptacle because of its higher current rating. Refer to Figure 2-1.

Note that two power cords are provided with the DYS5Ø. One is for 115 Vac service and the other for 23Ø Vac service as shown in Figure 2-1. Use the one you need and discard the other.

Verify that the site power receptacle is the correct one, that it is wired correctly, that the voltage is correct, and that the receptacle is properly grounded. For a more complete discussion of these matters, refer to the Digital Site Preparation Guide (EK-OCORP-SP).

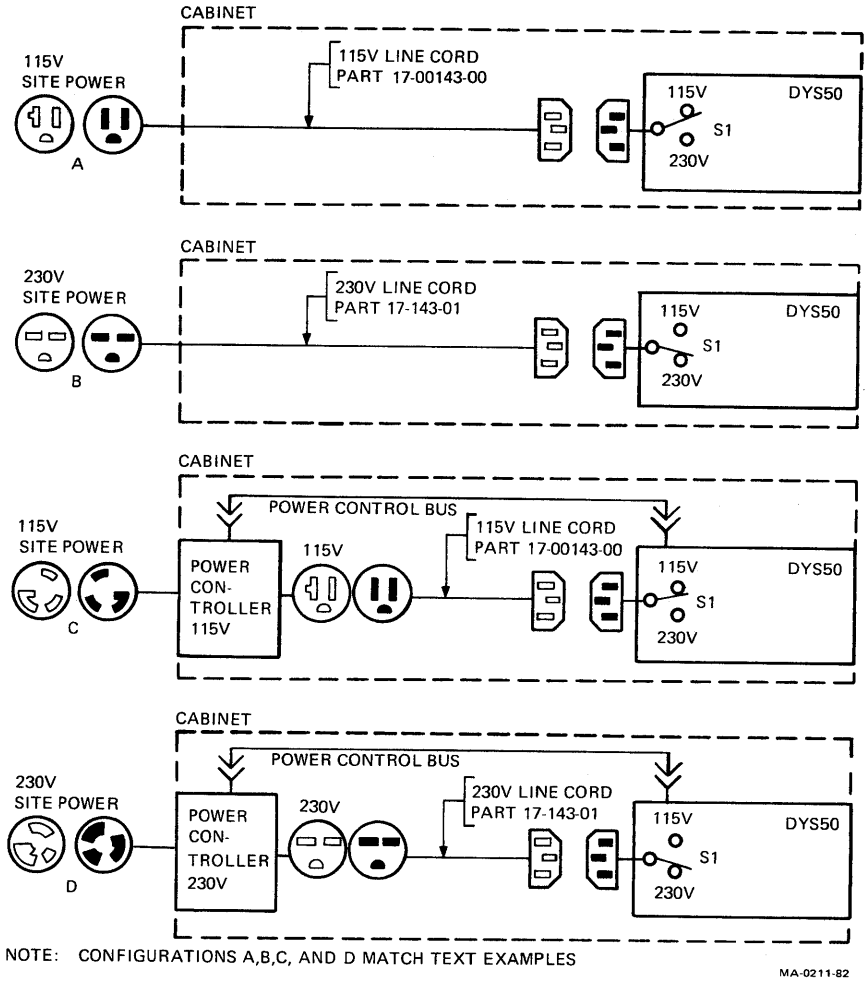


Figure 2-1 Site Power

2.2.2 NEMA Enclosure Requirements

If the DYS5Ø is to be installed in a NEMA enclosure, the customer must do some advance planning. DIGITAL does not sell NEMA type enclosures; they must be provided by the customer. Moreover, the customer must define the equipment configuration that goes into that cabinet. When specifying that configuration, the customer must make allowances for: heat dissipation, primary power, and I/O cabling. Refer to Paragraph 2.6.1 for NEMA enclosure mounting instructions and dimensions.

2.3 DYS5Ø UNPACKING AND INSPECTION

Some DYS5Øs are shipped separately and some are already mounted in cabinets with their customer chosen peripherals. If your's is a separate unit skip to Paragraph 2.3.2. If it is mounted in a cabinet continue.

NOTE

To protect the warranty, the customer must not unpack the system unless a DIGITAL representative is present.

2.3.1 Factory Configured Units

Perform the following unpacking and inspection procedure for all single and multicabinet systems.

2.3.1.1 Unpacking -- If the shipment must be moved from the receiving area, make sure doorways and passageways are wide enough to accommodate cabinet pallets before trying to move equipment to its selected location. Regardless of where unpacking and inspection is done, do not remove containers from the pallets until the shipment is examined for possible damage. (Reimbursement for damaged goods removed from the pallet is difficult.)

Perform the following unpacking procedure.

1. Make sure all containers are sealed. If any container is open, record it on the Installation Report or Field Service Report.

2. Check the shipment against the packing list to make sure you have received the correct number and type of containers. If the shipment is incorrect, notify the salesman and/or customer, and the Branch Service Manager. The customer should check with the carrier to locate any missing items.

3. Check all containers for external damage. Look for dents, protrusions, holes, and smashed corners. Note any damage and record it on the Installation Report or Field Service Report.

4. Open each container starting with the one marked "OPEN ME FIRST." Locate the packing slip and check the contents of each container against its respective slip. Identify any missing items on the Installation Report. Save any ramps that might come with pallet-mounted equipment.

5. If reshipment is a possibility, retain packing materials such as foam fillers and plastic inserts. In any case, retain the plastic (antistatic) bags in which any individual modules are shipped.

2.3.1.2 Inspection -- Perform the following inspection procedure.

1. Inspect the outside of the equipment and/or cabinet(s) for damage such as scratches, broken switches, and broken stabilizer feet.

2. Inspect inside the equipment and/or cabinet(s) for damaged components such as switches and indicators, or for loose and broken cable connections. Make sure all modules are securely seated in their connectors.

3. Note any damage found and record it in the Installation Report. Notify the Branch Service Manager immediately of any damage found.

4. Inspect each cabinet and freestanding peripheral to make sure it contains the items listed on the transfer sheet. Check the engineering change order revision (ECO REV) level and serial numbers against the transfer sheet or ECO status sheets. Record any missing items, incorrect serial numbers, or incorrect revision levels on the Installation Report.

5. When inspection is complete, remove the equipment and cabinet(s) from the shipping pallet. Remove the cabinet(s) as follows.

   a. Unbolt cabinet(s) from the shipping pallet. The bolts are on the lower supporting side rails of an H96Ø cabinet, or at the four corners of an H9646 cabinet, and can be reached from inside the cabinet.

   b. Raise stabilizing feet above the level of the casters.

   c. Attach enclosed ramp or use wooden blocks and planks to form a ramp from pallet to floor. Carefully roll cabinet(s) onto floor.

   d. Install front stabilizer feet with hardware provided.

2.3.2 Separate Units

All components of the basic DYS5Ø are shipped in a single carton. Optional devices are shipped in separate containers, and may require special unpacking procedures. Consult each option's own documentation for details.

Perform the following unpacking procedure for the DYS5Ø.

1. Inspect the DYS5Ø package for any external indication of shipping damage. Record any such indication on your Field Service report.

2. Open the package and remove the contents. Compare the contents with Figure 2-2 and Table 2-1 and verify that all items have been received. Check all items for damage. Record any shortages or damage on your Field Service report.

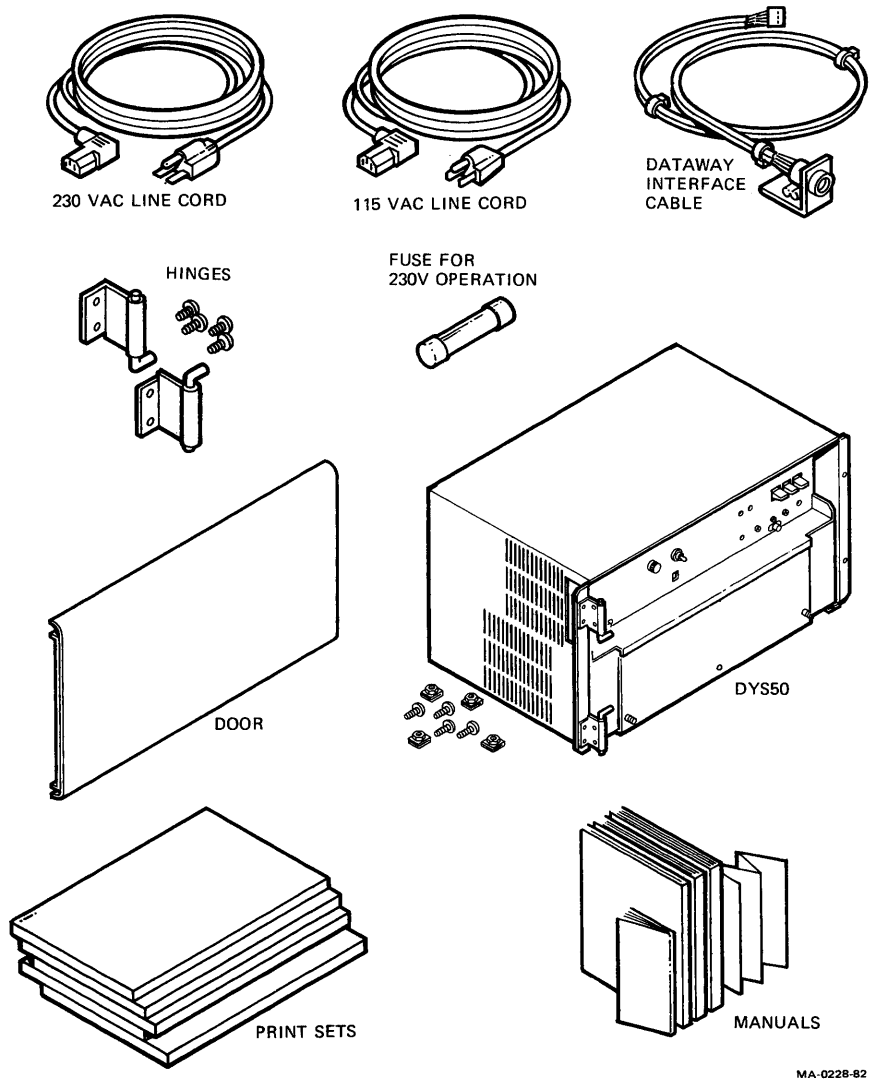


Figure 2-2 DYS5Ø and Accessories

Table 2-1 Box Contents

Quantity	Description
1	DYS5Ø (with KDF11-BB, MSV11-PK, ISV11-B)
1	Door
1	Top hinge
1	Bottom hinge
1	12Ø Vac power cord
1	24Ø Vac power cord
1	DECdataway interconnect cable
1	Fuse 5A/25Ø V
4	Hinge mounting screws phl pan sems
4	DYS5Ø mounting screws trus phl sem 1Ø-32 X 1/2
4	DYS5Ø mounting nuts, tinnerman, 1Ø-32
5	Field Maintenance Print Sets (DYS5Ø, BA11-Y, KDF11-B, MSV11-P, ISV11-B)
3	Technical Manuals or User Guides (DYS5Ø, KDF11-B, MSV11-P)
1	DYS5Ø Pocket Service Card

NOTE

An expander box has two 5 foot cables (BCØ2D-Ø5). A second expander box requires two 1Ø foot cables (BCØ2D-1Ø), which must be ordered separately. See Appendix C for details.

3. Save the shipping container and all packing materials until certain that return or reshipment to another location is not necessary.

4. Place the DYS5Ø on a bench so that its front hangs over the edge of the bench about 4 cm (1.5 inches). Remove the front module cover by loosening the two knurled, captive screws near the bottom of the unit and pulling out and down (Figure 2-3). Slide the unit back on the bench.

5. Without removing any modules, inspect for any bent or broken indicators, connectors, or any other obvious damage. The module configuration should match that shown in Figure 2-4. Do not add any modules at this time. Record any damage or shortages on the Field Service report.

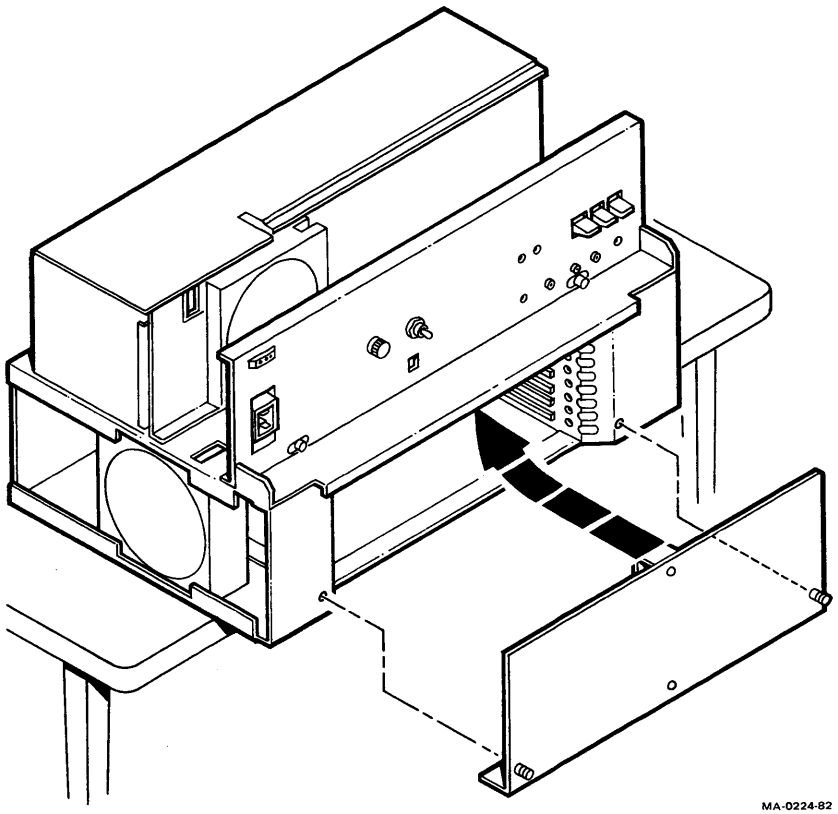


Figure 2-3 Module Cover

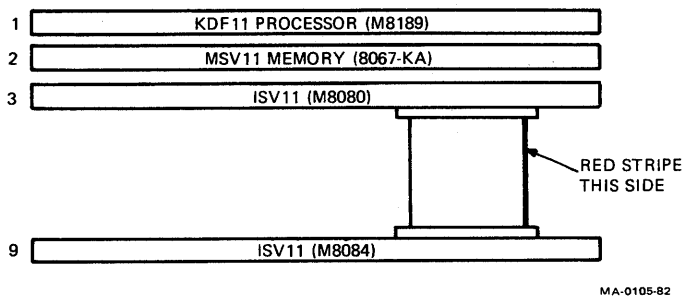


Figure 2-4 DYS5Ø Modules

6. Place the DYS5Ø about 3Ø cm (12 inches) back from the edge of the work bench and remove the cover as follows.

   a. Remove the two retaining screws, just forward of and at either end of the front panel, that fasten the DYS5Ø to its cover. One of these is shown in Figure 2-5.

   b. Using both hands, place your thumbs against the top front edge of the DYS5Ø, just above the cover lock-release levers, as shown in the boxes in Figure 2-5. Place your index fingers against the release levers, and your middle fingers under the lip just above the modules.

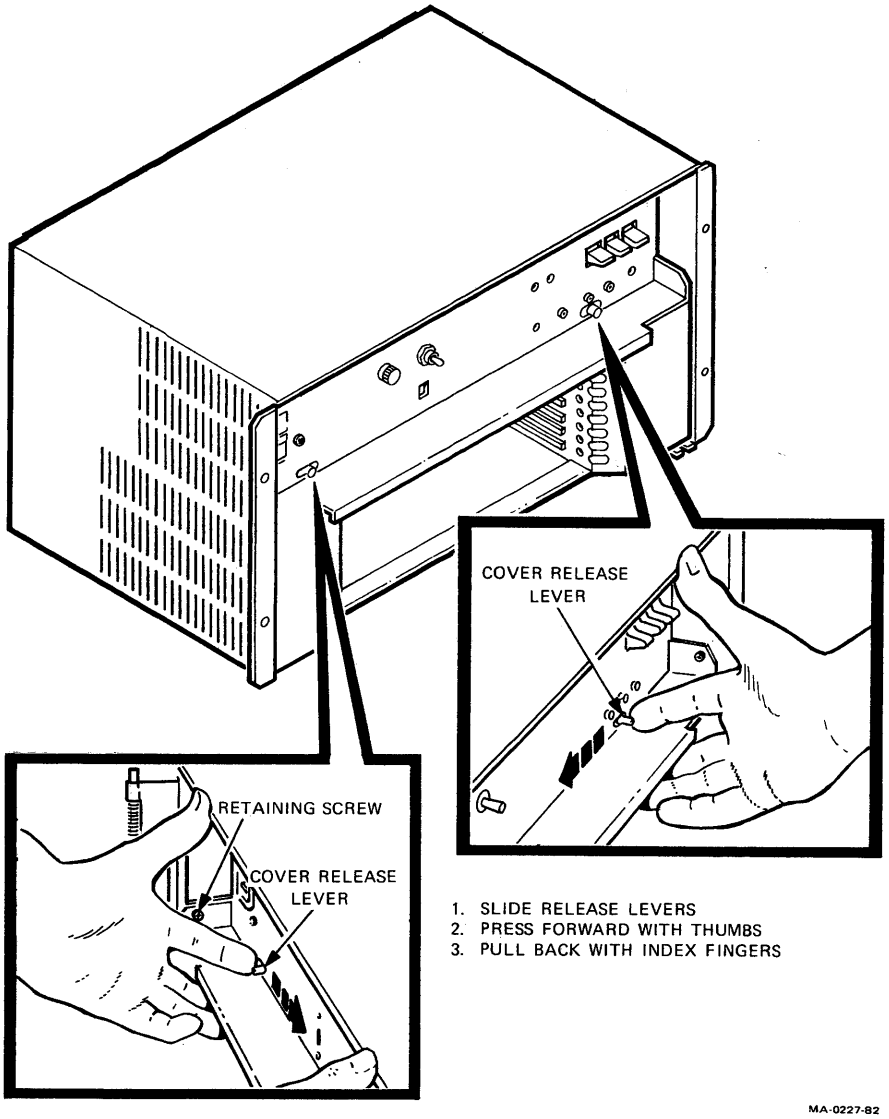


Figure 2-5 Cover Removal

c. Push on the release levers, sliding both of them toward the center of the front panel. While holding the levers in that position, press forward with your thumbs, and pull back with your middle fingers. The DYS5Ø should release and slide a little way out of the cover.

d. Complete cover removal by gripping the lip above the modules with one hand and pulling toward you, while, with the other hand, holding the top rear edge of the cover.

2.4 DYS5Ø SWITCHES AND INDICATORS

Before proceeding any further, study Figure 2-6 and Table 2-2. Become familiar with the locations and functions of the basic DYS5Ø switches and indicators.

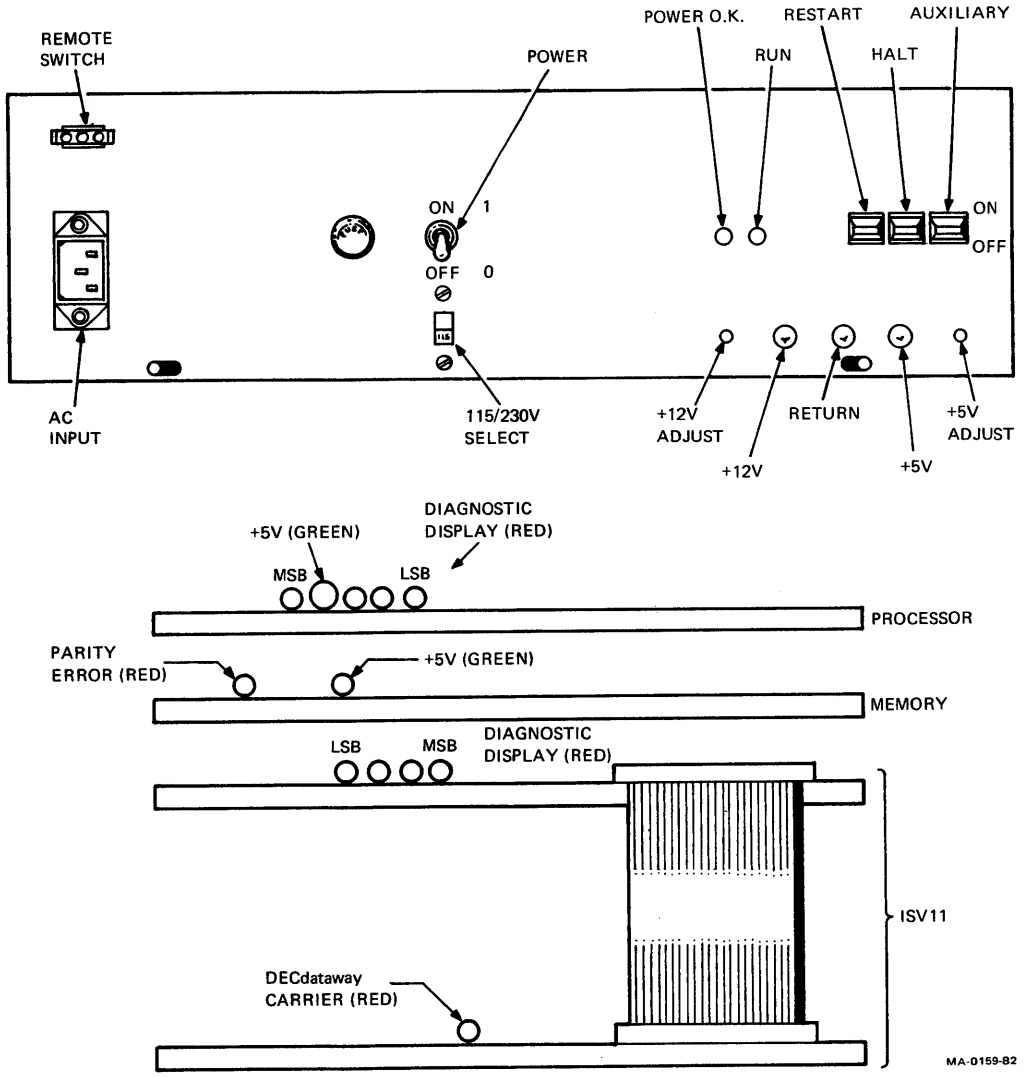


Figure 2-6 Switches and Indicators

Table 2-2 DYS5Ø Switches and Indicators

Switch or Indicator	Location	Function
DYS5Ø primary power switch	Front panel	When in the ON or 1 position, this switch connects ac power to the DYS5Ø power supply and cooling fans.
115/23Ø Vac select switch	Front panel	When the 115 legend on this switch is visible, the DYS5Ø is configured to operate on 115 Vac primary power. When the 23Ø legend is visible, the DYS5Ø is configured for 23Ø Vac primary power. To change the switch setting place the tip of a ballpoint pen in the depression on the front of the switch and push up or down. (Note that the fuse and power cord must also be changed.)
AUX ON/OFF	Front panel	A cable connects this switch to the cabinet power controller. Since all cabinet equipment is powered from the power controller, this switch serves as the master on/off switch for the entire cabinet.
HALT	Front panel	In the down position, this switch halts program execution by the DYS5Ø processor. In the up position, program execution is enabled but does not start automatically. A downline loading procedure from the dataway host normally starts the DYS5Ø.
RESTART	Front panel	When this momentary-contact switch is moved to the up position and released, it causes the DYS5Ø to do a power-up sequence. If the HALT switch is up, the processor can start executing a program. If the HALT switch is down, the processor enters ODT mode, and responds to ODT commands from a console terminal.
PWR OK	Front panel	This indicator lights when power supply dc voltages are present.

Table 2-2 DYS5Ø Switches and Indicators (Cont)

Switch or Indicator	Location	Function
RUN	Front panel	This indicator lights when the processor is executing programs.
DECdataway interface diagnostic display	ISV11 M8Ø8Ø module	At power-up, when one of the twelve ISV11-B ROM-resident diagnostics is running, these indicators display its number (in octal MSB at the right) An error in any one of the first nine (hardcore) tests causes its number to be displayed continuously. An error in any of the last three (softcore) tests causes its number to flash on and off for ten seconds.
DECdataway carrier indicator	ISV11-B M8Ø84 module	When the dataway is connected, this indicator is on when there is dataway activity. It is off if there is no activity or if the dataway is not connected.
Processor diagnostic display	KDF11 M8189 module	These indicators are normally on. They are not used for processor diagnostics in the DYS5Ø because the processor is configured for power-up-mode zero.
Processor PWR OK	KDF11 M8Ø89 module	This indicator lights when +5 V is present on the processor module.
Memory parity	MSV11 M8Ø67 module	This indicator lights when a parity error has been detected.
Memory PWR OK	MSV11 M8Ø67 module	This indicator lights when +5 V is present on the memory module.

2.5 PRELIMINARY CONFIGURATION

Configure DYS5Ø switches and jumpers as follows.

DYS5Ø Primary Power Switch	OFF or zero position
Restart	OFF
HALT	OFF
Auxiliary	OFF

115/23Ø Vac Select Switch -- Make sure the position of this switch matches the voltage being used at your site.

Fuse -- Two fuses are shipped with each DYS5Ø -- one in the fuse holder, and one loose. Make sure the correct one is in the fuseholder. The 1Ø A fuse is for 115 Vac operation. The 5 A fuse is for 23Ø Vac operation.

Backplane Jumpers -- The usual configuration for these jumpers is shown in Figure 2-7. Make sure that at least W1 is installed. W2 and W3 are not needed but do no harm if present. Backplane jumper functions are explained in Table 2-3.

Bezel Assembly Jumpers -- These jumpers are normally factory configured as shown in Figure 2-8. Make sure W1, W2, and W3 are out, and W4 is in. Jumper functions are explained in Table 2-4. Alternative configurations of these jumpers are explained in Chapter 5, Paragraph 5.2.4.

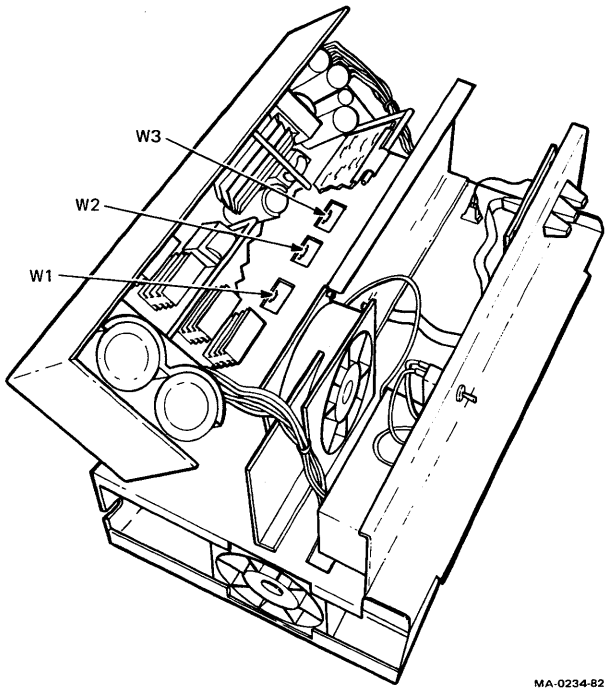


Figure 2-7 Backplane Jumpers

Table 2-3 Backplane Factory Jumper Configuration

Jumper	Jumper State	Function
W1*	In	The H7861 power supply generated LTC signal is used to assert BEVNT L signal.
W2, W3	Out	These jumpers have no effect on DYS5Ø operation.

* W1 must be removed from all expander boxes in a multiple-box system since only the box containing the KDF11-BB (M8189) module must be the source of the LTC signal.

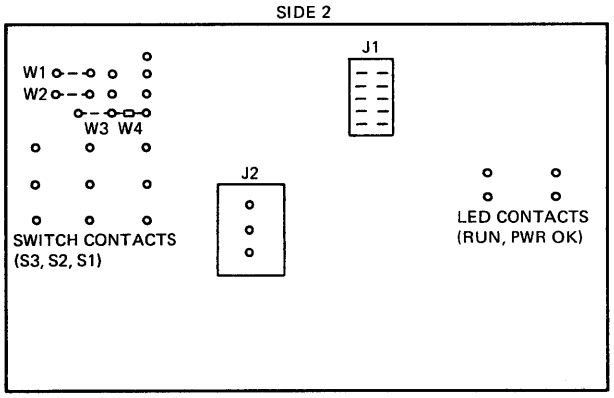


Figure 2-8 Front Bezel Jumpers

Table 2-4 Bezel Assembly Factory Jumper Configuration

Jumper	Jumper State	Function
W1, W2	Out	These jumpers allow the AUX ON/OFF switch to turn the system power on and off.
W3	Out	CPU is mounted in this backplane.
W4	In	This jumper enables the RUN indicator because the CPU is mounted in this backplane.

2.6 MOUNTING THE DYS5Ø

If your system was factory configured in a cabinet, skip to Paragraph 2.7.

2.6.1 Non-standard Enclosure Mounting

If your DYS5Ø is being installed in a special industrial enclosure, the following installation procedure must be modified to suit that enclosure's configuration. Study the procedure and become familiar with its requirements. Although DIGITAL does not provide industrial enclosures for DYS5Øs, or specify their configuration, the DYS5Ø is designed to simplify such installations.

Specifically, the DYS5Ø (without its front door or hinges) fits in a NEMA type-12 industrial cabinet. (NEMA stands for National Electrical Manufacturing Association.) A NEMA type-12 cabinet is 3Ø.48 cm (12 in) deep. The DYS5Ø cover has rear mounting holes for mounting on the rear wall in a NEMA type enclosure (Figure 2-9). Since all DYS5Ø modules, switches, indicators, and adjustments are front accessible, it is well suited for this type of installation. For more information about NEMA enclosures, refer to DIGITAL brochure ED Ø1315-126.

For examples of this type of installation, refer to the I/O Subsystem User Guide EK-ØPIOS-UG.

2.6.2 Standard Cabinet Mounting

Perform the following if you are installing the DYS5Ø in a standard cabinet.

1. Install the power cord in the cabinet as shown on unit assembly drawing E-VA-DYS5Ø-ØØ.

2. Mount the hinges (as shown in Figure 2-1Ø) with hardware provided.

3. Install the DYS5Ø cover in the cabinet (as shown in Figure 2-11) with hardware provided. Do not tighten the mounting screws at this time.

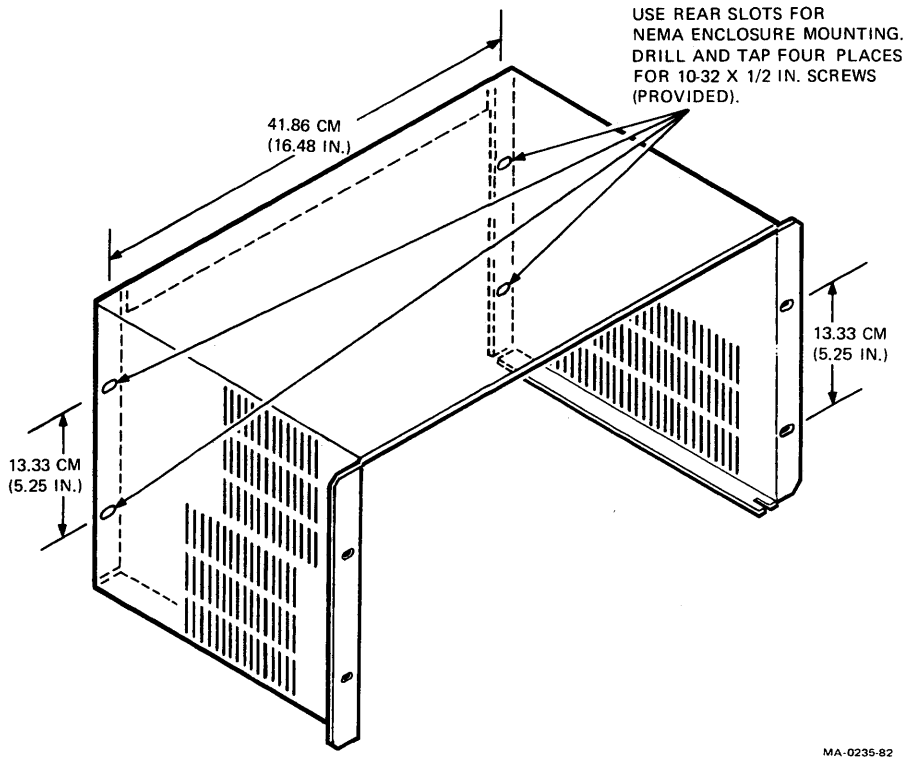


Figure 2-9 NEMA Mounting

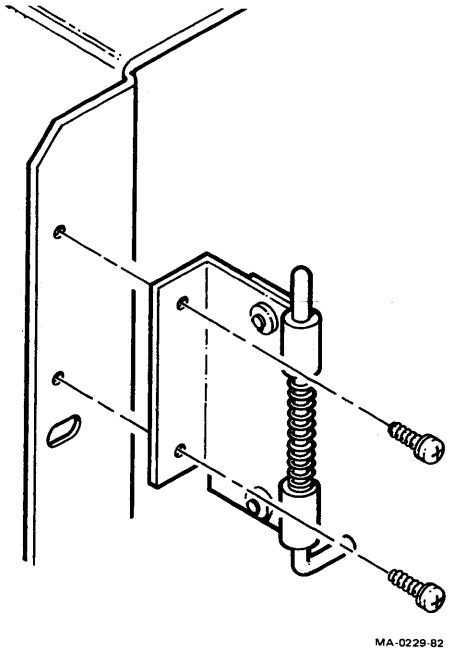


Figure 2-10 Hinge Mounting

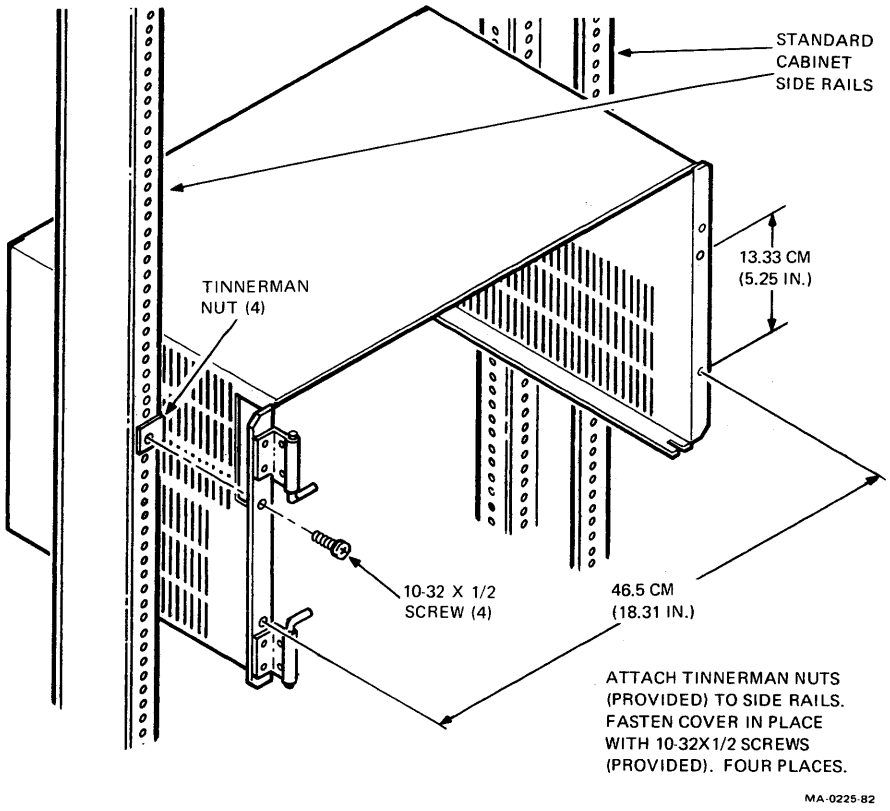


Figure 2-11 Standard Mounting

4. Slide the DYS5Ø into the cover until it is stopped by the locking bolts. Momentarily press the lock-release levers to allow the DYS5Ø to go in the rest of the way, and slide it in until it locks. Now, tighten the four mounting screws.

WARNING

Note that the DYS5Ø has no restraining mechanism to prevent its being pulled all the way out of its mounting cover, once its locking bolts have been released. Therefore, when removing it from its mounting cover, use extreme caution to avoid dropping it.

5. Leave the module cage cover off at this time, so that the LED indicators are visible during test.

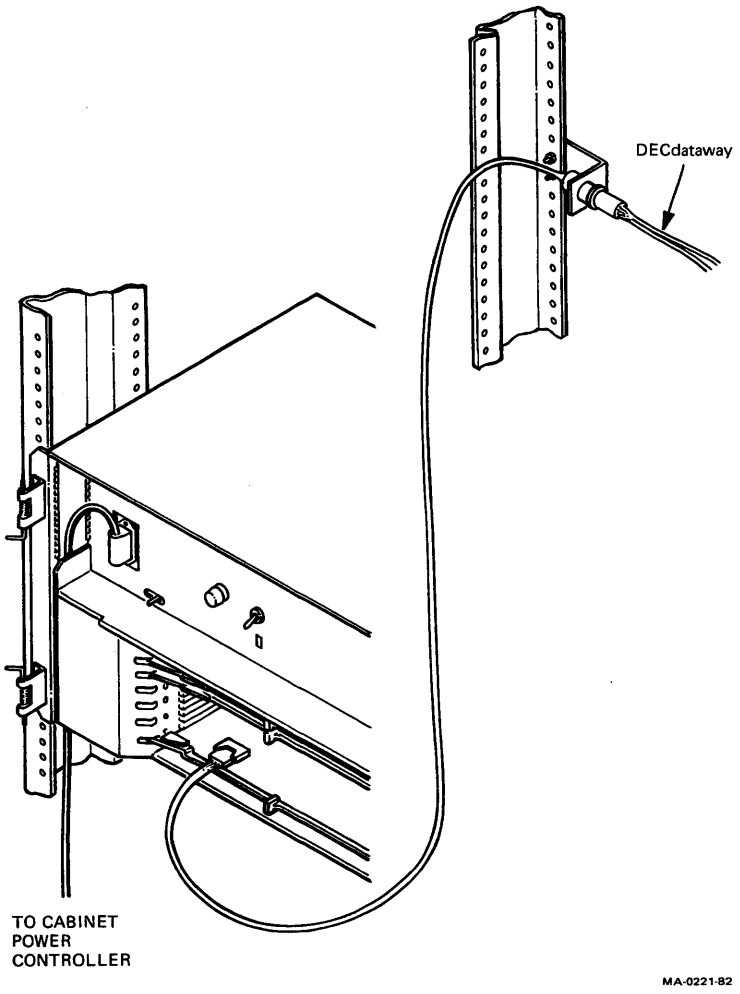


Figure 2-12 DECdataway and Power

6. Install the power cord and DECdataway interface cable (as shown in Figure 2-12) with hardware provided. Do not connect the DECdataway at this time.

7. Place the DYS5Ø front panel power ON/OFF switch (located at approximately the center of the front panel) in the 1 (ON) position.

2.7 CABINET AC POWER CHECK

All units in the DYS5Ø cabinet get their ac power from the 874 power controller. Remove the cabinet rear panel and use the following procedure to make sure that cabinet power is configured properly.

1. At the rear of the cabinet, set the power controller main power circuit breaker switch to Ø (OFF).

2. Set the power controller REMOTE/OFF/LOCAL switch to OFF.

3. Plug the cabinet ac power cord into its proper receptacle. The ac power indicator (to the upper right of the main power circuit breaker) should go on.

4. Set the power controller MAIN POWER circuit breaker switch to 1 (ON).

5. Set the REMOTE/OFF/LOCAL switch to LOCAL. All cabinet equipment should go on, and the DYS5Ø front panel PWR OK indicator should go on. The DYS5Ø fans should operate.

6. Set the REMOTE/OFF/LOCAL switch to REMOTE. All cabinet equipment should go off.

7. At the front of the cabinet, set the DYS5Ø AUX ON/OFF switch to ON. All cabinet equipment should go on as before.

8. Set the AUX ON/OFF switch to OFF.

2.8 DC VOLTAGE MEASUREMENT

Turn on the DYS5Ø using the AUX ON/OFF switch on the front panel (Figure 2-6).

The +5 Vdc and +12 Vdc regulated voltages must be measured with a calibrated digital voltmeter. Test points for this purpose are located at the lower right of the front panel also shown in Figure 2-6. If these measurements are not within the limits given, do not try to adjust the power supply until you first refer to Chapter 5. That chapter contains the correct adjustment procedure, along with some precautions that must be observed.

2.8.1 Measurement of +5 Vdc

Use the following procedure to measure +5 Vdc voltage.

1. Attach the voltmeter leads as follows.
   The plus lead to the plus 5 V test point
   The minus lead to the return test point

2. The correct reading is +5 V $\pm$ Ø.15 V.

2.8.2 Measurement of +12 Vdc

Use the following procedure to measure +12 Vdc voltage.

1. Move the plus voltmeter lead to the +12 V test point.

2. The correct reading is +12 V + Ø.36 V.

2.9 OFF-DATAWAY OPERATION

For this procedure you need to use one of the DYS5Ø-site terminals as a console device. Refer to that terminal's user guide to determine its interface requirements, and connect it to J1 of the processor. (This is the console interface; it is normally configured at the factory for 96ØØ baud).

Next, turn on the terminal and place the DYS5Ø HALT switch in the up position. Then, turn on the DYS5Ø using the AUX ON/OFF switch on the front panel.

When power is turned on, the ISV11-B internal diagnostics keep repeating and produce the following display on the DYS5Ø console. The explanatory comments in the right column are not part of the display.

```
@                       ODT prompt

Ø Ø Ø 6 7 6             Interrupt test successful

@                       ODT prompt

Ø Ø 1 1 3 4             LSI-11 Instruction test successful

@                       ODT prompt
```

The display repeats continuously about every 1Ø seconds.

Observe the ISV11-B indicator LEDs and confirm the following.

1. The ISV11 (M8Ø8Ø module) diagnostic indicators display the number of the diagnostic (in octal, LSB at the left) being executed. These indicators cycle as the diagnostics repeat, but the on/off pattern appears random because all tests do not have the same duration. However, test 13 (octal) is about ten seconds long and is noticeable.

2. The ISV11 (M8Ø84 module) carrier indicator is off.

2.10 DYS50 TO DECdataway INTERFACE

The communications link between the DYS50 and its host PDP-11 computer is the DECdataway. This should already be installed. If not, its installation is covered in the DECdataway User Guide (EK-ISB11-UG).

Part of that installation is selecting the DECdataway port address for each connected device (by configuring jumpers at each port connector). The DYS50 uses two port addresses; the lowest numbered address is marked on the port connector at the DYS50 site location. Check with the site manager to see if the address marked on the connector is the correct one for this installation.

To interface the DECdataway to the DYS50, simply mate the DECdataway connector with its receptacle inside the DYS50 cabinet (Figure 2-12).

2.11 ON-DATAWAY OPERATION

When the dataway is connected, observe the terminal display again.

- The terminal display stops repeating.

Observe the ISV11 indicators.

- The ISV11 (M8080 module) diagnostic indicators display a zero cycling from left to right through a field of ones.
- The ISV11-B (M8084 module) carrier indicator lights when there is dataway activity.

Any variation from the above results indicates a fault in the basic DYS50 system. As an aid to isolating the fault, refer to Chapter 3 (Maintenance), which presents a detailed discussion of the ISV11-B internal diagnostics and the significance of variations from the above results.

2.12 DYS50 PERIPHERAL INTERFACES

The following paragraphs discuss interfaces for some common DYS50 peripherals.

2.12.1 Standard Interfaces

The DYS50 processor is an LSI-11 device. Its peripherals interface to the LSI-11 bus via control modules. These modules plug into the bus and connect to the peripheral devices via one or more cables. The various control modules and their cabling requirements are discussed at length in the Microcomputer Interfaces Handbook. A user guide with additional interface information comes with each peripheral; sometimes additional cables are included.

2.12.2 Filtered Interfaces

In any electrical system, cables that connect pieces of electrical equipment carry signals that may radiate enough electrical energy to cause objectionable amounts of electromagnetic interference (EMI) in the local environment. Conversely, any EMI in the local environment can be conducted into a cabinet on its interfacing cables. If that cabinet happens to contain sensitive circuits, this interference may cause them to malfunction. To minimize the possibility of either problem occurring with the DYS5Ø, all signal cables leaving or entering a DYS5Ø cabinet, do so through specially constructed cable assemblies that have filtered connectors. These connectors are mounted on an H349 distribution panel. An example of this type of interface is shown in Figure 2-13.

2.12.3 H349 Distribution Panel

This panel is provided with all DYS5Ø cabinet assemblies. The panel provides simple and convenient means of interfacing peripheral equipment with the DYS5Ø.

This 28.32 cm (11.15 in) by 44.1Ø cm (18 in) hinged panel is held in its vertical position by two quarter-turn captive screws.

The H349 panel has ten mounting locations (J1 through J15) for mounting up to fifteen connector cable assemblies, as shown in Figure 2-14. Eleven cable assemblies contain 1 X 4 slots (J1 through J11) and four contain 4 X 4 slots (J12 through J15). An adapter is available to transform four of the 1 X 4 slots (J8 through J11) into a 4 X 4 slot. When mounted, each cable assembly is connected to the DYS5Ø subsystem by ribbon cables. As Figure 2-14 shows, the J6 and J7 positions are normally used for the two SLU interfaces on the DYS5Ø's processor: J6 for the console interface and J7 for a standard terminal.

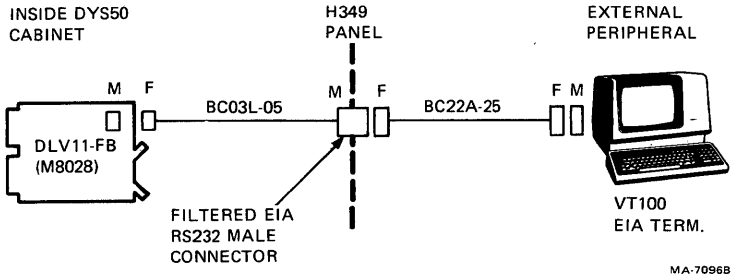


Figure 2-13 Filter Placement

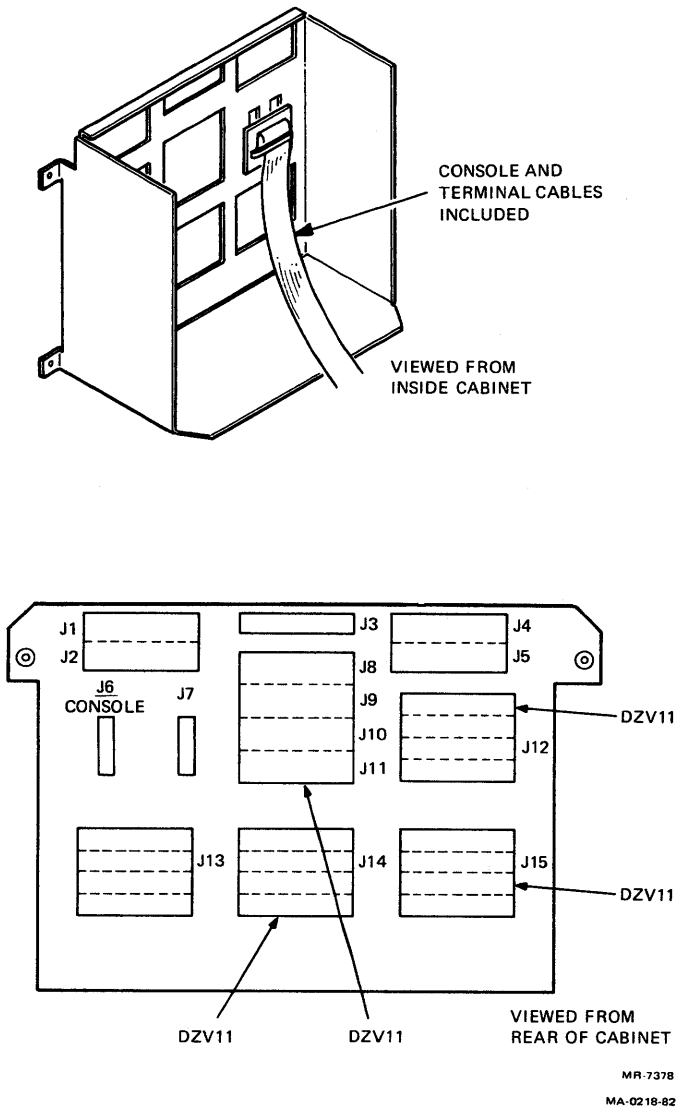


Figure 2-14 H349 Distribution Panel

2.12.4 DYS5Ø to I/Ø Subsystem Interface

For process I/O applications, the DYS5Ø must contain an M7959 I/O control module (IOCM). This module provides an interface between the DYS5Ø LSI-11 bus and the I/O subsystem D-bus.

The interface is completed via a BCØ8R cable that plugs into J1 of the M7959 module at one end, and the D-bus-in connector of the I/O subsystem H334 chassis at the other end (Figure 2-15). The figure shows the correct way to install this cable by observing proper orientation of the stripe on the side of the cable. Additional information about the I/O subsystem is contained in the I/O Subsystem User Guide (EK-ØPIOS-UG).

2.13 EXPANDING AN EXISTING SYSTEM

If an existing DYS5Ø system needs more peripherals to meet increased demands, interface modules for the new peripherals must be added to the LSI-11/23B bus. The following paragraphs tell how to add new modules to existing spare bus slots, and how to expand the bus if there are no spare slots.

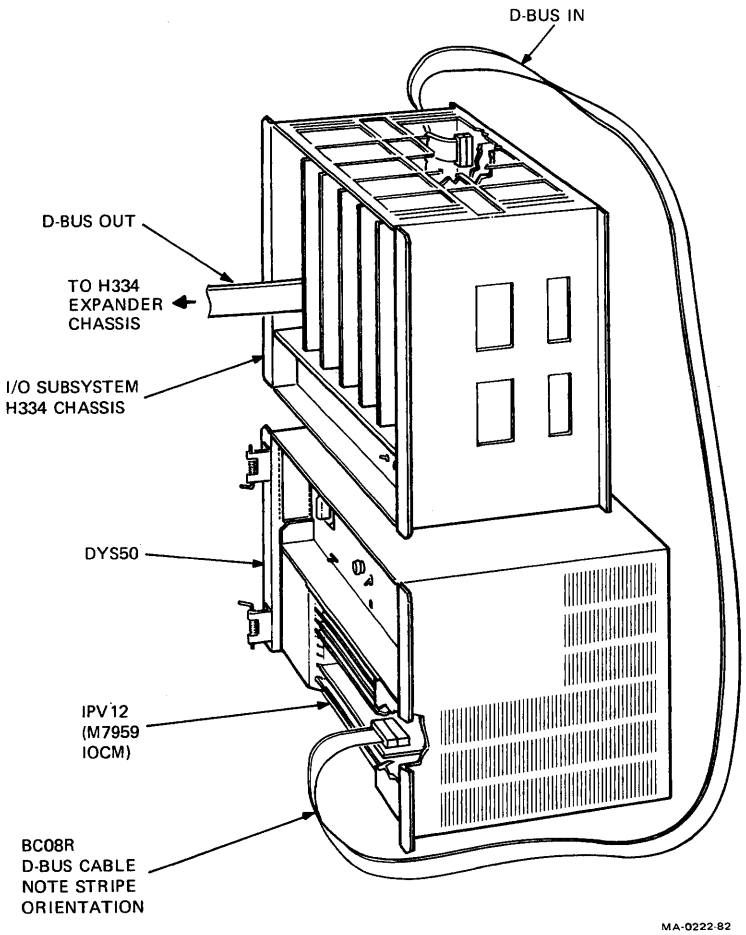


Figure 2-15 I/O Subsystem Interface

2.13.1 Adding New Modules

If there is a spare slot on the LSI-11/23B bus, it is easy to add a new peripheral device to the DYS5Ø. While observing LSI-11/23 bus rules, (as explained in Appendix C) configure the new peripheral's interface module address, vector, and other options (if any); plug the module into the spare bus slot, and connect it to the peripheral with the appropriate cable. First consult each device's user manual to determine if there are any restrictions and what cables can be used. In addition, the DYS5Ø imposes the following restrictions for adding new modules.

1. The ISV11-B M8Ø8Ø module must be moved to the slot following the new interface module.

2. The ISV11-B M8Ø84 module must remain in slot 9.

3. The DZV11 vector space is from 3ØØ to 777. Vectors 3ØØ and 3Ø4 cannot be used because they conflict with the ISV11-B.

2.13.2 Adding an Expansion Chassis

If the original DYS5Ø chassis does not have enough room for expansion, you can extend the bus by adding a BA11-YC expander box. The rules for adding new modules to the first box must also be applied to the second box. In addition, the expansion bus must connect to the first bus via two BCØ2D cables. These cables interface to the first chassis via an M94Ø4-ØØ module in the last usable slot, and to the second chassis via an M94Ø5-YA module in slot 1 (refer to Appendix C). (The option consists of the two cables and two modules.) Note that when adding an expander box, the ISV11-B moves to the expander box.

2.14 PERFORMANCE VERIFICATION

You can verify the performance of the DYS5Ø and its peripherals once communication is established between the DYS5Ø and host computer via the DECdataway. When this is done, the host can down-line load diagnostic software to the DYS5Ø. Then, using only a local console terminal, you can verify that all DY subsystem units are operational by running these diagnostic programs. Each program exercises some integral unit of the system and provides feedback via displays or printouts about the unit's performance.

CHAPTER 3
MAINTENANCE

3.1 OVERVIEW

Corrective maintenance of the basic DYS5Ø is relatively simple. It is a modular device; if it fails, just identify and replace the failed module.

Identification of the failed module is sometimes difficult, but there are tools to help you do that. All that is needed is some system knowledge and a logical approach to each problem.

The logical approach is not possible without the system knowledge. You must be aware of, and clearly understand, the DYS5Ø's relationship to the system of which it is a part (the DY system). For example, if you want to troubleshoot a DYS5Ø from the host, you must first establish that the host itself is operational, and that the DECdataway is working properly. You must also determine that the DYS5Ø's interface to the DECdataway (the ISV11) is working. Read the related material and references in Chapter 1, and become totally familiar with DY system concepts.

This chapter describes DYS5Ø maintenance only. You can find hardware maintenance information for optional units of a DYS5Ø subsystem in their respective user guides. These user guides are included in the documentation package shipped with the DYS5Ø. In addition to maintenance information, these user guides describe optional configurations of these units, which may or may not be incorporated in a given DYS5Ø. For example, many peripheral interface modules have jumpers and/or switches used to select addresses, vectors, etc. All modules in a DYS5Ø are configured before shipment. However, factory configurations of user selected options may not match site requirements in all cases, so if a module appears to have failed at installation time, check its configuration. Even when a previously working module fails and is replaced by a new one, verify that it is properly configured by consulting the appropriate user guide.

As for the standard modules comprising the basic DYS5Ø, if there is ever any doubt about their original factory configurations, they are listed in Appendix A for reference.

The United States Area Support Group is chartered to provide all levels of support, including Field Service training for U.S. Area Support personnel. Support and training in European areas is provided by European Regional Support.

3.2 TROUBLESHOOTING TOOLS

It is impossible to describe all the ways that a DYS5Ø failure can affect a DY system. Some failures are easily isolated and corrected; others require all the troubleshooting resources and expertise at your command. The exact nature of a failure and its attendant symptoms will, to a large extent, dictate your troubleshooting approach. Nevertheless, a logical beginning and a thorough knowledge of troubleshooting tools can greatly reduce the time spent in the effort.

The following is a brief description of the DYS5Ø's hardware and software troubleshooting tools. They have a top-down structure that, if used intelligently, will help you quickly zero-in on even the most obscure failure causes.

WARNING

If the DYS5Ø is used as an industrial process controller, do not initiate any maintenance procedures or diagnostic programs without first checking with local site personnel for any required safety precautions and/or operating restrictions. Certain of these processes, if interfered with in any way, can pose extreme hazards to site personnel, and may even have far-reaching and dire consequences beyond their immediate vicinity.

3.2.1 Maintenance Software (Diagnostics)

The following is a brief discussion of what maintenance software will do for you. How to run and interpret system-level and standalone diagnostics are the subjects of other documents. Which documents, depends on which host computer is used in your system. These are listed in Chapter 1.

3.2.1.1 System Level Diagnostics -- These diagnostics are run at the host. In the event of a DYS5Ø caused system failure, isolation of that failure to a specific DYS5Ø, if not immediately obvious, is usually achieved by logical system-level fault analysis -- that is, by running the system-level diagnostics and interpreting the results. One of these diagnostics tests the ISB11 controller; another, (called the DECdataway exerciser) establishes the soundness of communications between the host and the DYS5Øs.

3.2.1.2 Standalone Diagnostics -- Further isolation of a failure to a specific field replaceable unit (FRU) in the DYS5Ø is done by running standalone diagnostics in the DYS5Ø. These are down-line loaded to the DYS5Ø's LSI-11/23B computer by CZKMP, a diagnostic monitor in the host. (CZKMP also down-line loads part of itself to the ISV11's RAM memory. From there it monitors the down-line loaded, standalone diagnostics and communicates with the operator.) Once down-line loaded, standalone diagnostics are run by the DYS5Ø's LSI-11/23B computer. They can be monitored remotely at the host in two different modes (host and communication), or locally (in local mode) at the DYS5Ø if it has a console terminal.

3.2.2 Hardware Troubleshooting

Before running any diagnostics, perform a quick visual inspection of the DYS5Ø for any obvious signs of trouble. The following are things to look for.

- Are both ends of the power cord plugged in?
- Is the fuse okay?
- Are both fans operating?
- Is the power ON/OFF switch on?
- Is the 115/23Ø volt select switch in the correct position?
- Is the power control cable connected?
- Are the HALT, RESTART, and AUXILIARY switches in the correct positions?
- Do the POWER OK and RUN indicators light?
- Are all cables in good condition and their connectors firmly seated?

3.2.3 Built-In Diagnostics

Aside from system level and standalone diagnostics, there are on-board diagnostics contained in the ISV11's ROM memory. These are a series of twelve tests (numbered one through fourteen, octal) that run automatically every time the DYS5Ø is turned on. If the DECdataway is connected, these tests run only once, otherwise they repeat continuously (except in the case of some error conditions). The tests are also run once by one of the system-level diagnostics: the DECdataway exerciser. Associated with the built-in diagnostics is a display, consisting of four LEDs, that indicates the number of the test being run. The tests are of two types: hardcore and softcore.

3.2.3.1 Hardcore Tests -- The first nine tests (1 to 11 octal) are called hardcore because they test basic characteristics of the ISV11-B. An error in any of these nine tests causes the eight-bit microprocessor to loop within the test, thus continuously displaying the number of the first failed test. A hardcore error also means that the DYS50's communication interface is not functioning properly. It is, therefore, prevented from trying to communicate, so that it does not impair the communications of other devices on the DECdataway. Table 4-1 (Chapter 4) describes the hardcore tests.

3.2.3.2 Softcore Tests -- The last three tests (12, 13, and 14, octal) of the ISV11-B ROM-resident diagnostic tests are called softcore because they do not stop the ISV11-B from communicating with the host. These tests check the operation of the LSI-11/23B CPU (processor and memory). Test 13 takes about 11 seconds, but 12 and 14 are so fast their numbers may not be noticed in the LEDs. A softcore error causes the failed test number to be displayed flashing in the LEDs for 10 seconds. The error number (in decimal) is also displayed at the operator's terminal. Table 4-2 (Chapter 4) describes the softcore tests.

3.2.4 ISV11 Indicators

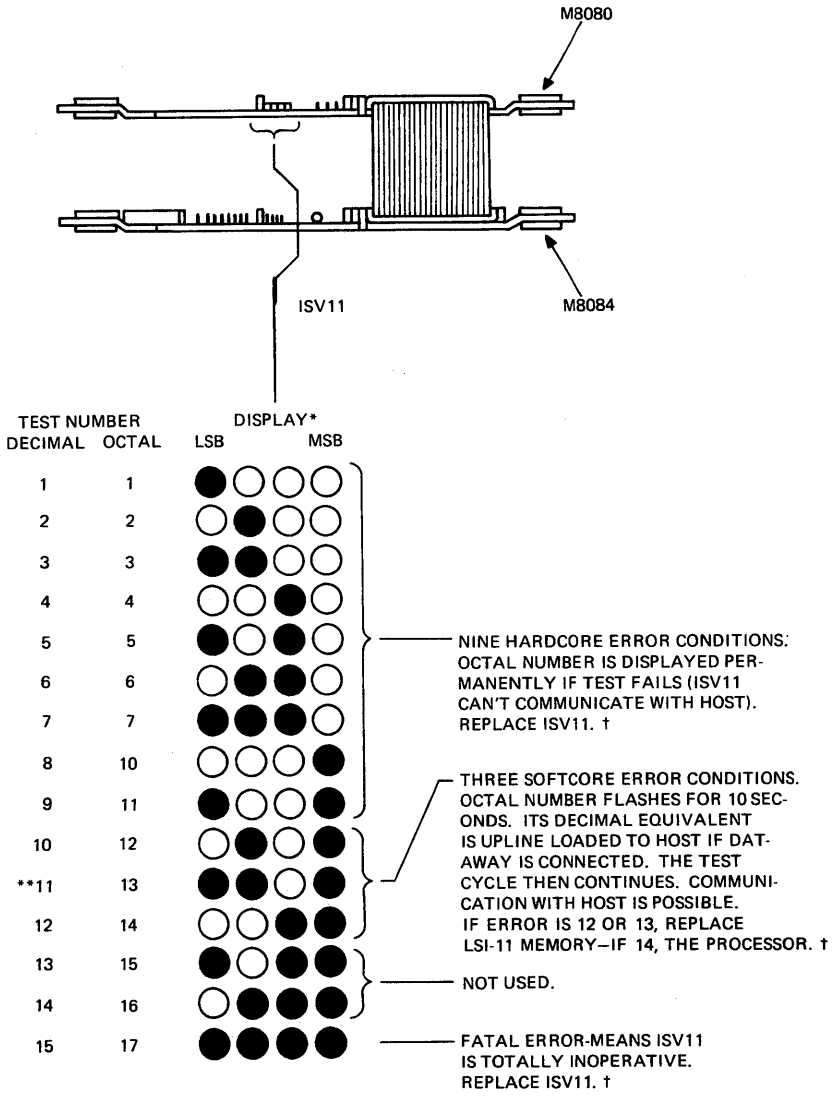
The LED display for the built-in diagnostics, located on the edge of the ISV11-M8080 board, provides much helpful information for DYS50 fault analysis. Figure 3-1 summarizes the interpretation of this display.

A LED on the ISV11-M8084 board flashes when a carrier is present on the DECdataway. It flashes at a slower rate as carrier activity increases.

3.2.5 DYS50 Troubleshooting Flowchart

It cannot be overemphasized that you must always be aware of the total system when troubleshooting devices on the DECdataway. Do not troubleshoot the DYS50 until it has been verified that the problem is not in the host or DECdataway. The strategy for doing that is the subject of system level documents listed in Chapter 1.

When through direct observation or system trouble analysis you have isolated a particular DYS50 as the source of a problem, you can then pursue a troubleshooting strategy to further isolate it to the lowest field replaceable unit (FRU) in the DYS50. The strategy is outlined in flowchart form in Figure 3-2. The figure is not meant to be an exhaustive treatment of all possible failures. It is merely a helpful guide. Troubleshooting strategies change as more is learned about the problem, but if you begin with the approach indicated in Figure 3-2, it should prevent you from wasting valuable time misreading the symptoms.



*BLACK = ON

** TEST 13 (OCTAL) LASTS ABOUT 11 SECONDS. ITS NUMBER IS DISPLAYED ALL DURING THE TEST, BUT UNLESS IT IS FLASHING, THE TEST HAS NOT FAILED.

† MODULE REPLACEMENT SUGGESTIONS ARE FOR MOST PROBABLE FAILURES. OTHER FAILURES MAY SHOW THE SAME SYMPTOMS.

NOTE: THERE ARE TWO NO-ERROR DISPLAY CONDITIONS

1. IF THERE ARE NO FAILURES, AND THE DATAWAY IS CONNECTED, THE LEDS DISPLAY A ZERO CYCLING FROM LEFT TO RIGHT THROUGH A FIELD OF ONES.
2. IF THERE ARE NO FAILURES, AND THE DATAWAY IS NOT CONNECTED, THE ON-BOARD DIAGNOSTICS KEEP REPEATING. THE LEDS DISPLAY EACH TEST NUMBER AS IT RUNS, BUT 13 (OCTAL) IS THE ONLY ONE OF SUFFICIENT DURATION TO BE READ EASILY.

MA-0104-82

Figure 3-1 ISV11 Display

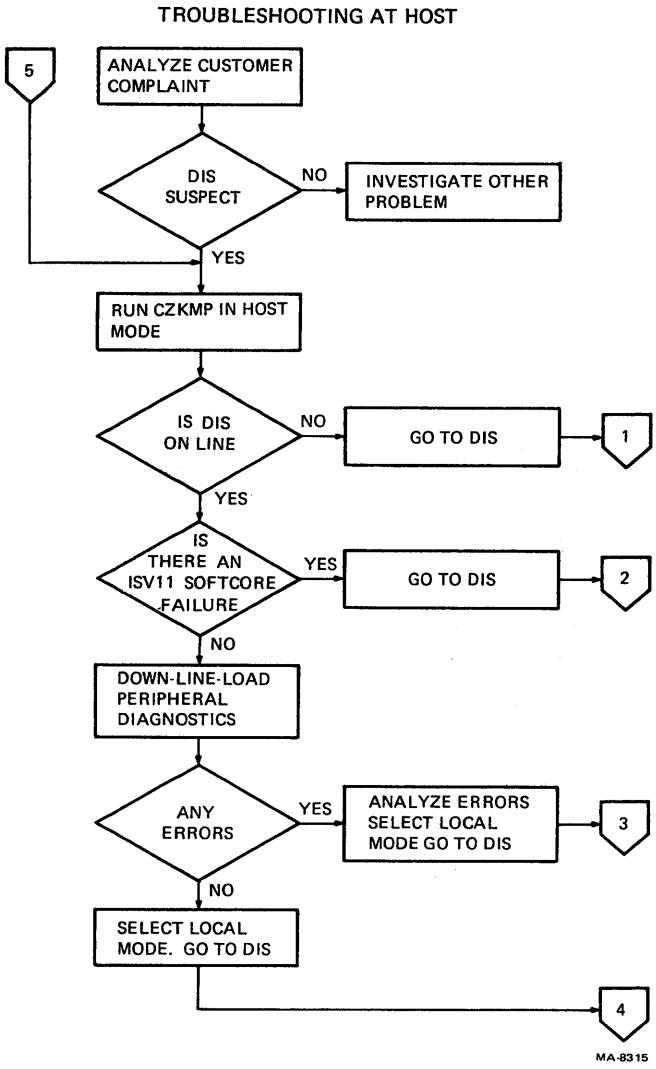


Figure 3-2 DYS5Ø Troubleshooting (Sheet 1 of 2)

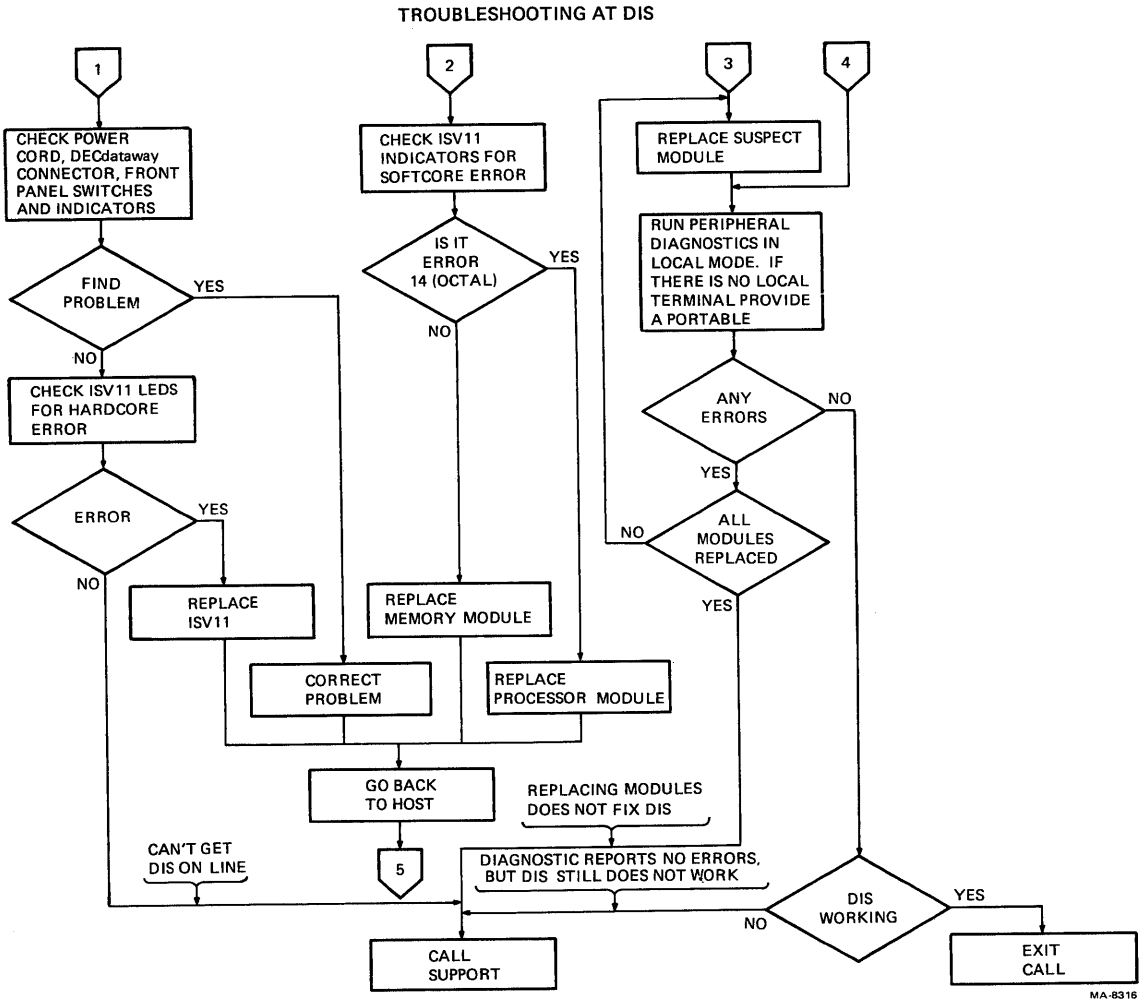


Figure 3-2 DYS5Ø Troubleshooting (Sheet 2 of 2)

3.3 ISV11-B TROUBLESHOOTING

Maintenance philosophy for the ISV11-B is option replacement (both modules). However, careful analysis of faults using diagnostics and available test points should permit service personnel to isolate a problem to one of the two modules. Chapter 4 contains a troubleshooting procedure for doing this. Note that the ISV11-B operates only as a unit, that is, with the M8Ø8Ø and M8Ø84 modules connected together. However, they are not a matched set; a single module can be replaced if necessary.

3.4 ROUTINE MAINTENANCE

Routine maintenance procedures (when and if required) for integral units of a DYS5Ø subsystem are found in their respective user guides (Paragraph 1.6). Most maintenance procedures can be performed by removing the rear panel and/or sliding out one of the drawers.

3.5 UNIT REMOVAL AND REPLACEMENT

Once identified, a faulty unit in a DYS5Ø is easily replaced using one of the following procedures. Field replaceable units (FRUs) include the following:

- Entire DYS5Ø box (the BA11-Y)
- Any plug-in module
- Fans
- Power supply
- Control panel module (bezel module)
- Backplane

WARNING

Note that the DYS5Ø has no restraining mechanism to prevent its being pulled all the way out of its mounting cover, once its locking bolts have been released. Therefore, when removing it from its mounting cover, use extreme caution to avoid dropping it.

3.5.1 Replacement of the BA11-Y Box

Use the following procedure to remove the DYS5Ø.

1. Place the AUX ON/OFF switch in the OFF position.

2. Place the ac power 1/Ø (ON/OFF) switch in the zero (OFF) position.

3. Unplug the power-control cable (if used), and the ac power cord from their sockets at the left end of the front panel. Place these out of the way by tucking them into the rectangular opening just to the left of the front panel. Put the power-control cable in first. It will be held in place by the power-cord plug, which will be held neatly in place if you tuck it into the front part of the opening. There is a channel the right size for it (Figure 3-3).

4. Loosen the two knurled-captive screws near the bottom of the DYS5Ø. Remove the module cover by pulling out at the bottom and then down.

5. Remove any cables attached to the modules. Do this carefully, taking special note of the position of each connector, and of its orientation (some connectors are not mechanically keyed and can be plugged in backwards unless you pay attention to this). Also note the routing of these cables so that you can put them back neatly when reinstalling the DYS5Ø.

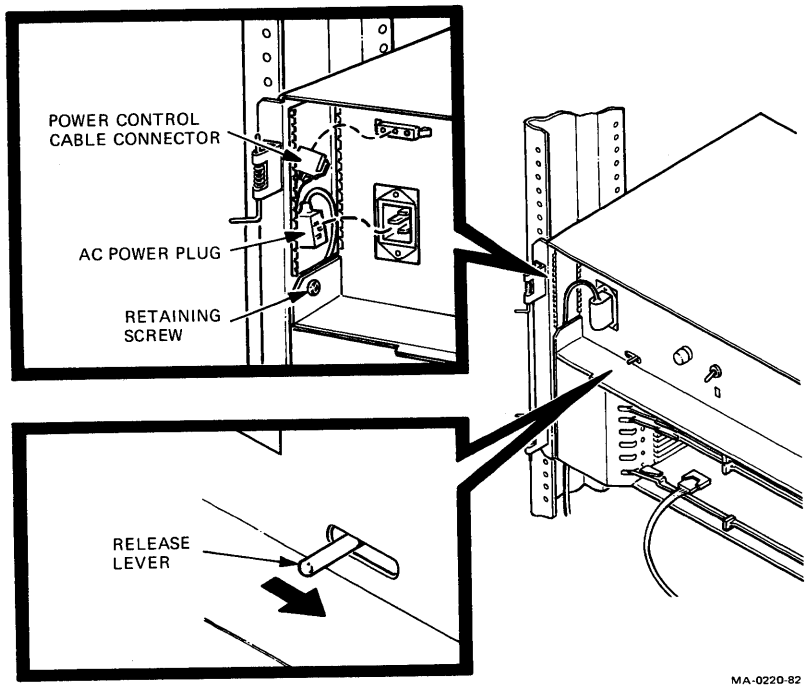


Figure 3-3 DYS5Ø Chassis Removal

6. Remove the two retaining screws that fasten the DYS5Ø in place. There is one at each end of, and just forward of the front panel (Figure 3-3).

7. Release the DYS5Ø from its mounting cover and pull it out only about two inches. This is done by pressing the release levers with your index fingers, while pulling with your middle fingers hooked under the lip just over the module cage. Keep in mind that the DYS5Ø is not restrained in its mounting cover in any way, slide it the rest of the way out of the cover very carefully, supporting it with your hands on both sides.

The replacement procedure for the DYS5Ø is nearly the reverse of the removal procedure -- except for the release levers. These will prevent you from sliding the DYS5Ø all the way back into its mounting cover. Press the release levers and push the DYS5Ø past that point. Then push the DYS5Ø in until you hear them lock.

3.5.2 Module Insertion and Removal

CAUTION

Modules and/or the backplane assembly might be damaged if modules are inserted or removed with power on, or if inserted upside down.

It is absolutely imperative that you turn the power off before trying to insert or remove any DYS5Ø module. Use the ac 1/Ø (ON/OFF) switch to turn off a DYS5Ø or expander box only. If your system has a power controller, and if its remote ON/OFF feature has been implemented on your DYS5Ø, you can use the AUX ON/OFF switch to turn off the entire system.

Your DYS5Ø may have both quad modules and dual modules. Dual modules go only in the left side of the module cage (Figure 3-4). All modules are installed component side up.

All modules must be inserted or removed with extreme caution, to prevent damage to any of their components or to the components of adjacent modules. Do not grab a module by its handle(s) and yank it out of the card cage. Module removal is really a two step process: First pull with only enough force to release it from its connector, and then carefully guide it out of its slot. This prevents damage to components, as well as the unintentional changing of any switch settings on the module itself or the one below it.

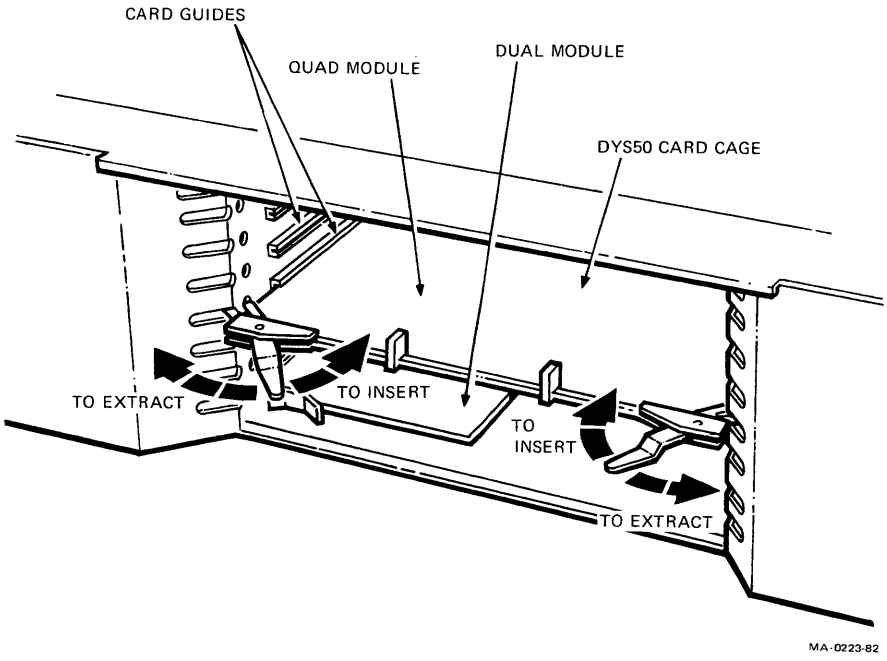


Figure 3-4 Module Replacement

Most quad modules are equipped with extractor-type handles that help with module insertion and removal. Pulling back on both of these handles at the same time releases the module from its connector, making removal easy. To reinstall one of these modules, carefully guide it into its slot, making sure that it is in its proper card guide on both sides. With the extractor handles extended outward, you will be able to guide the card far enough into its connector for the forked ends of the handles to engage the slots on the sides of the card cage entrance (Figure 3-4).

Insertion is completed by pressing on both handles until they are parallel to the card end.

3.5.3 Fan Removal and Replacement

The DYS5Ø has two cooling fans: one for the modules, and another for the power supply. To replace either fan, you must first turn off the power and remove the DYS5Ø from its mounting cover in the manner previously discussed.

Use the following procedure to remove the power supply fan.

1. Unplug the ac cord on the right side of the fan.

2. Remove the four screws that fasten the power supply bracket, fan, and fan bracket to the DYS5Ø chassis, and remove that entire assembly (Figure 3-5).

Use the following procedure to replace the power supply fan.

1. Check the arrow on the side of the new fan for proper air-flow direction, and also orient the fan so the ac plug is in the correct position.

2. Attach the brackets to the new fan and reinstall the assembly.

3. Plug in the ac cord.

The logic assembly fan appears difficult to remove but is really quite easy with the following procedure.

Use the following procedure to remove the logic assembly fan.

1. Unplug the ac cord on the right side of the fan.

2. Remove the four mounting screws.

3. Push the fan back as far as it will go and tip the top forward. By sliding the fan to one side, you will be able to slide out one top corner and then the other to remove the fan (Figure 3-5).

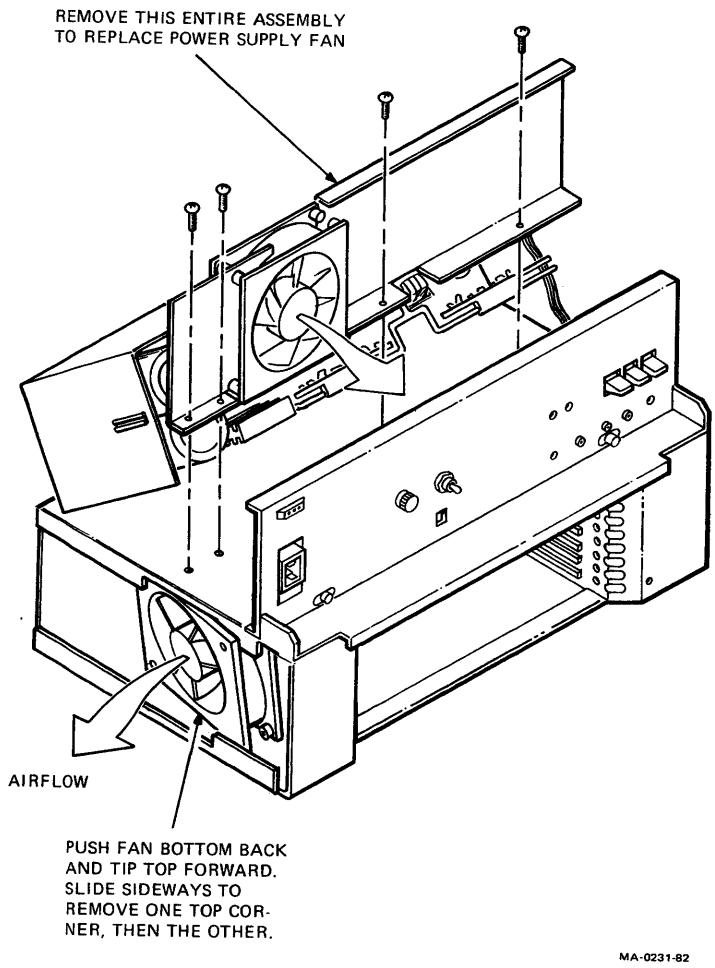


Figure 3-5 Fan Replacement

Use the following procedure to replace the logic assembly fan.

1. Check the arrow on the side of the new fan for proper air-flow direction, and also orient the fan so the ac plug is in the right position.

2. Install the new fan in the chassis by putting the bottom in first and then sliding the top corners in one at a time.

3. Finally, fasten the four mounting screws, and plug in the ac cord.

3.5.4 Power Supply Removal and Replacement

Use the following procedure to remove the power supply.

1. Turn off power.
2. Remove cover.
3. Remove two screws on top of supply and tip back.
4. Unplug J1 (ac power harness).
5. Loosen the screws of the dc harness terminal strip and disconnect it (Figure 3-6).
6. Unplug the control board (the small pc board on the left Figure 3-6) to access J5 and J6. Unplug J5 and J6.
7. Tip supply down to normal position.
8. Unlock hinges (Figure 3-6).
9. Lift supply out.

Use the following procedure to replace the power supply.

1. Make sure the power supply hinges are in the unlocked position; set it in place, and lock the hinges.
2. Replace: J5 and J6, the power supply control module, the dc harness terminal strip, the ac power harness, and the two screws.
3. Reinstall the DYS5Ø in its mounting cover.

3.5.5 Control Module Replacement (Bezel)

This is a 7.6 X 11.4 cm (3 X 4.5 in) printed circuit module. It is mounted on standoffs, and is located just behind the front panel (Figure 3-7).

Use the following procedure to remove the control module.

1. Turn off power.
2. Remove cover.
3. Unplug the two cables that plug into the control module.
4. Remove the four mounting screws that attach the module to the standoffs, and remove the module.

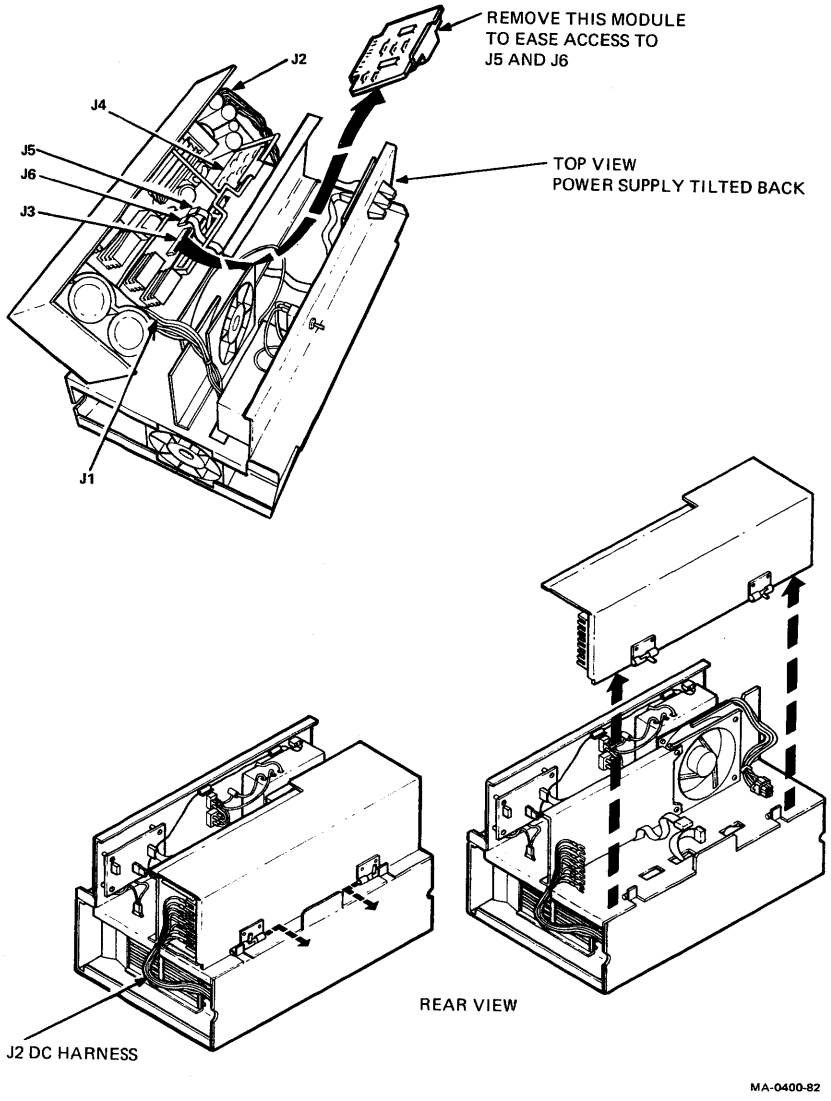


Figure 3-6 Power Supply Replacement

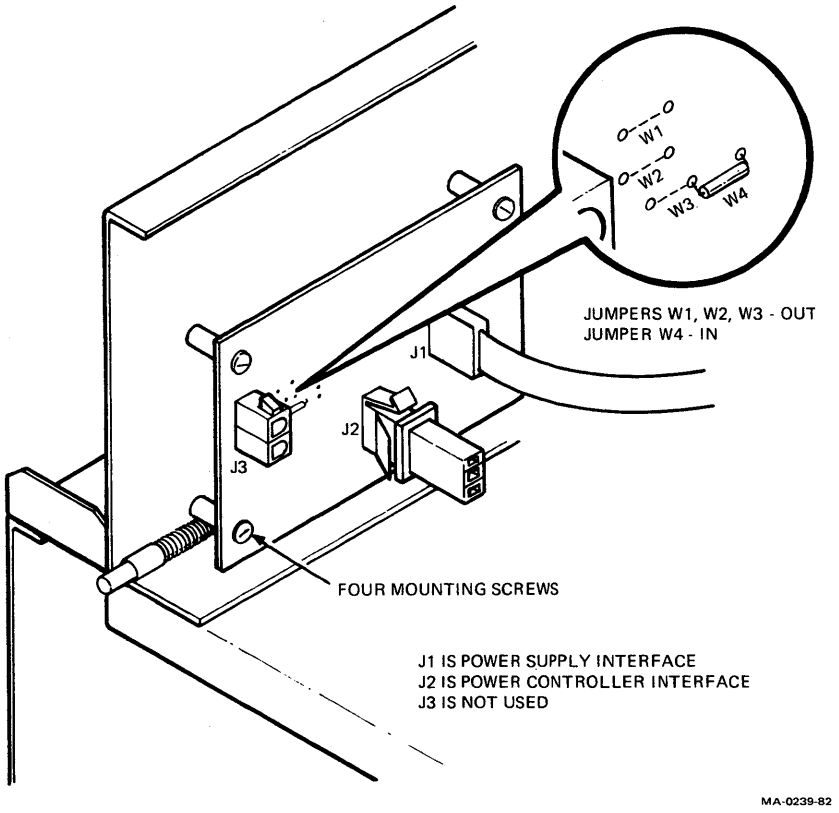


Figure 3-7 Front Panel Bezel Module Replacement

Use the following procedure to replace the control module.

1. Check jumpers W1 through W4. Normally, jumpers W1, W2, and W3 should be out; W4 should be in. However, there are other configuration options as explained in Chapter 5, so configure the new module like the old one unless directed to do otherwise by the site manager.

2. Install the module on the standoffs as shown in Figure 3-7, and fasten with the four mounting screws.

3. Reconnect the cables to J1 and J2 (J3 is not used).

4. Reinstall the DYS5Ø in its mounting cover.

3.5.6 Backplane Replacement

To replace the backplane, first turn off power and remove the DYS5Ø from its mounting cover in the manner previously described. Having done that, remove the backplane as follows.

1. Remove all modules plugged into the backplane.

2. Disconnect the dc harness at the backplane end. Loosen the screws to disconnect the harness.

3. Disconnect the backplane signal cable at the backplane end.

4. Remove the bottom two mounting screws of the card-cage cooling fan.

5. At the rear of the power supply (Figure 3-8), remove the three screws that fasten the rear of the backplane enclosure to the DYS5Ø.

6. On the bottom of the DYS5Ø, remove the six screws that fasten the bottom cover to the module cage. This frees the L-shaped, bottom-and-back cover from the DYS5Ø. The backplane, which is mounted to the back part of this cover, is now accessible.

7. Remove the four screws that fasten the backplane in place, and remove the backplane.

Use the following procedure to replace the backplane.

1. Verify that jumpers W1, W2, and W3, on the front of the new backplane are configured correctly.

2. Fasten the new backplane to the cover with the four screws removed from the old one.

3. Reassemble the DYS5Ø, following the previous procedure in reverse.

3.6 DC VOLTAGE MEASUREMENT AND ADJUSTMENT

If the +5 Vdc and +12 Vdc regulated voltages appear to be out of limits, do not try to adjust them without first remeasuring as directed here. Furthermore, if adjustment is indeed necessary, you must use the exact procedure and precautions given here.

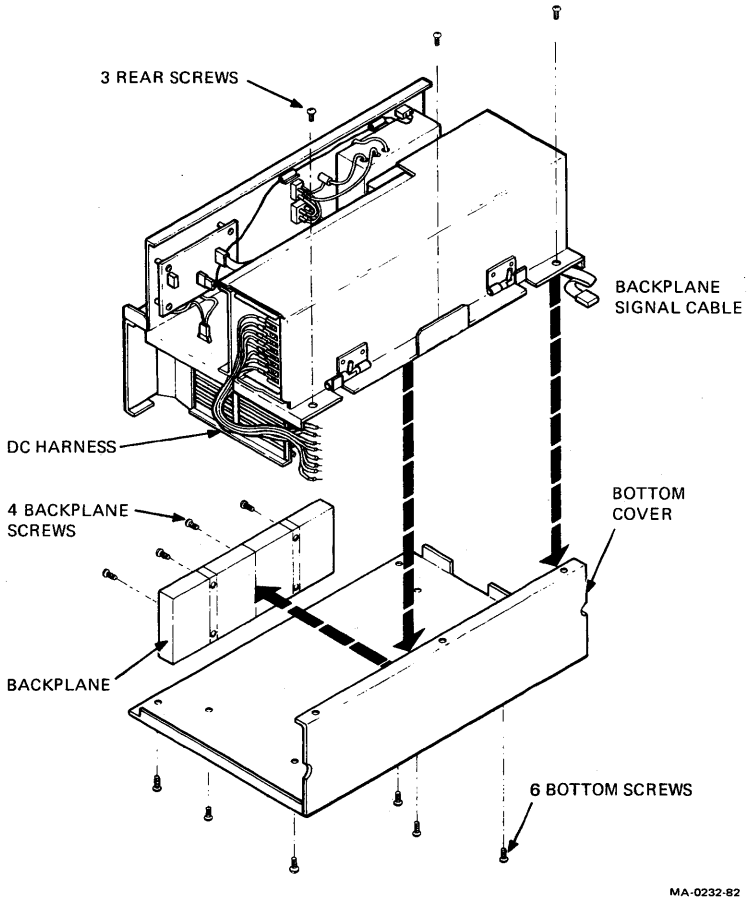


Figure 3-8 Backplane Replacement

3.6.1 Measurement

Use a calibrated digital voltmeter to measure the voltages under typical conditions.

NOTE

Do not measure the dc voltages without a load on the power supply (at least 2 amps). If you do, you will get incorrect readings.

Use the test points provided at the lower right of the front panel to measure the voltages (Figure 3-9). The +5 Vdc output should be between 4.85 V and 5.15 V. The +12 Vdc output should be between 11.64 V and 12.36 V. If either voltage is out of tolerance, use the following adjustment procedure.

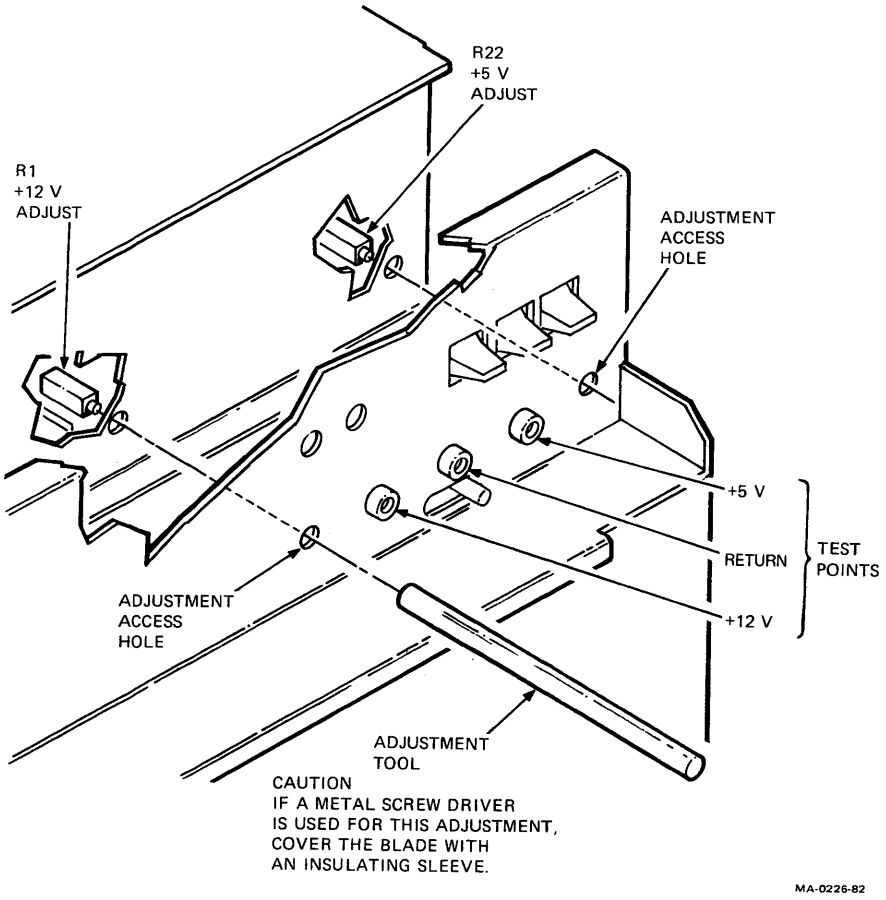


Figure 3-9 DC Voltage Adjust

3.6.2 Adjustment

Voltage adjustment potentiometers are located on the control board inside the power supply (Figure 3-9). Access to these adjustments is possible through holes in the front panel.

NOTE

If both voltages need adjustment, adjust the +5 Vdc supply first. Adjusting the +12 Vdc supply first -- beyond its range -- may cause crowbarring.

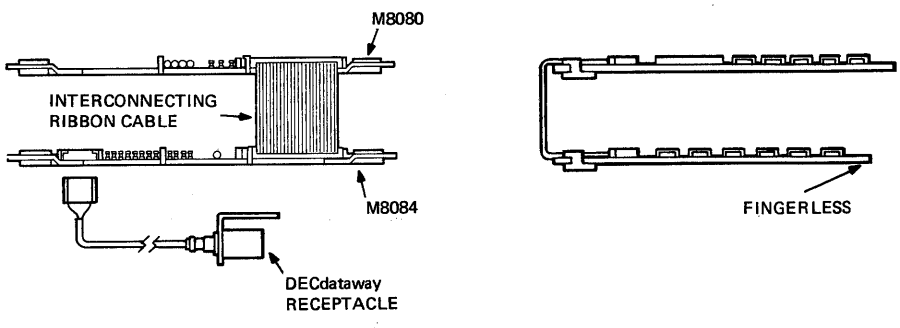
The correct output is reached when a potentiometer is near its midrange position. If it must be turned to near an extreme position to reach tolerance limits, there may be a problem in the regulator. If the output cannot be brought within limits, replace the power supply control board.

CHAPTER 4
ISV11-B DESCRIPTION

4.1 INTRODUCTION

The ISV11-B is a device that interfaces LSI-11 computers to the DECdataway. That is, an LSI-11 computer equipped with an ISV11-B can be attached to a DECdataway network. An LSI-11 computer so equipped is called a Distributed Intelligent Subsystem (DIS). The ISV11-B works with all current versions of the LSI-11 family of computers.

The ISV11-B consists of two quad-height modules: the M8080 and the M8084 (Figure 4-1). These are connected together with a short ribbon cable. One of the modules, the M8080, interfaces with the LSI-11 bus via its etched edge connector when it is plugged into an LSI-11 backplane. The other module, the M8084, does not plug into the backplane at all; it has no edge connector. It does, however, occupy a slot in the module cage. It interfaces with the DECdataway cable connector via a one meter (3.3 ft) serial-bus cable. This cable and the ribbon cable that interconnects the two modules are part of the ISV11-B option.



NOTE: THE M8080 MODULE IS ALWAYS ASSIGNED AS THE LAST OPTION ON THE LSI-11 BUS. THE M8084 IS ALWAYS ASSIGNED TO THE LAST AVAILABLE SLOT IN THE MODULE ASSEMBLY AND DOES NOT PLUG INTO THE BUS. THERE CAN BE EMPTY SLOTS BETWEEN THE TWO MODULES.

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Figure 4-1 ISV11-B Option -- DECdataway to LSI-11 Bus Interface

4.2 ISV11-B APPLICATION

Recall that an ISV11-B plugged into an LSI-11 computer creates a DIS. A DIS fulfills a modular function in a class of computer communication networks called DY (DECdataway) systems. These systems are local area networks that implement distributed processing in industrial complexes. To see how an ISV11-B works in one of these systems, we must first see how a typical DY system works.

4.3 TYPICAL DY SYSTEM

In its simplest form, a DY network has a centrally-located (host) computer, and multiple, remotely-located, smaller computers. The remotes are deployed throughout the site wherever dedicated processing is needed. Completing the network is a communication channel called the DECdataway, which connects the host and all remotes together (Figure 4-2).

As Figure 4-2 shows, LSI-11s (the DISs) are the distributed elements of the network, and ISV11-Bs are their network interfaces. Because they are linked by the DECdataway, the LSI-11s are DECdataway subsystems, and because they are programmable they are called intelligent subsystems. Thus the name, DECdataway Intelligent Subsystem (DIS).

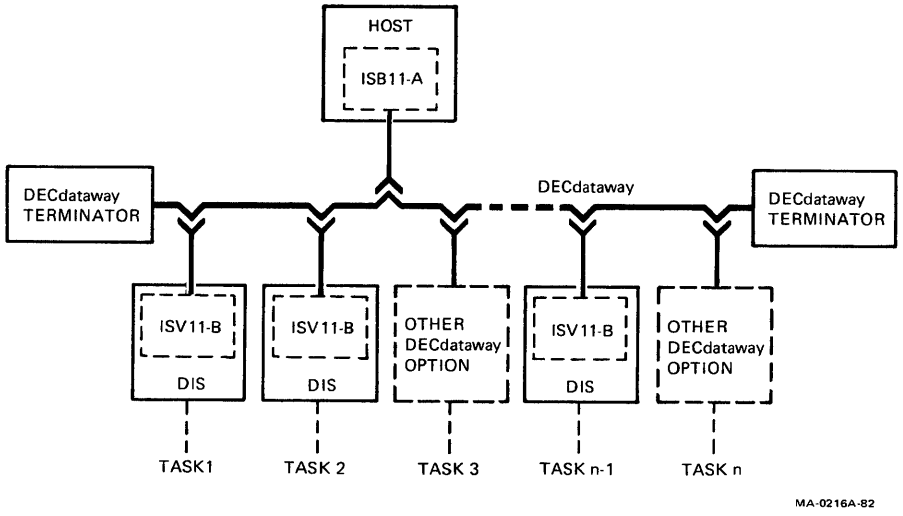


Figure 4-2 A Typical DY System

4.3.1 DY System Host

The host computer of a DY system local-area network can be either a PDP-11, or VAX/VMS computer. The same DECdataway hardware is used in either case, but the software is different. Moreover, the host operating system can regard all units of a local area as belonging to the same network even though more than one DECdataway may be used to connect all of them to the host. Different hosts can support different numbers of DECdataways and each DECdataway needs a separate ISB11 DECdataway Controller.

By the way, the host and its ISB11 DECdataway controller are not restricted to any particular network node; they can be at one end of the DECdataway or at any node along the entire cable. The host's node, however, does need an ISB11-unique DECdataway connector.

4.3.2 DY System Communication Link

A DECdataway consists of more than only a cable. The DECdataway controller, its connectors, and its two cable-terminating resistors, as well as the cable, are all part of the DECdataway (Figure 4-2). Each of these is described briefly.

4.3.2.1 DECdataway Cable -- This cable is a shielded, twisted pair. It can be up to 4572 m (15,000 ft) long.

4.3.2.2 DECdataway Controller (ISB11) -- One of the DECdataway nodes plugs into the ISB11 DECdataway controller, which in turn, plugs into the host computer. This controller manages all communications between the host and any remote devices attached to its DECdataway cable. The controller supports up to 63 remote-device addresses.

Communication over the DECdataway is synchronous serial at 55,556 bits per second, and is carried out in a block or message-oriented fashion. Most communications are two-part transactions: (1) a command message from the host to a remote and, (2) a response message from the remote back to the host. Excepted are communications from the host to address zero. This address functions as a broadcast channel for sending command messages from the host to all remotes at the same time. Remotes are not allowed to respond to these messages.

All messages on the DECdataway are formatted in DIGITAL Serial Bus Control (DSBC) protocol, which makes sure that message content is not modified during transmission.

4.3.2.3 DECdataway Connectors -- Each DECdataway has one controller connector, and from one to 63 remote-device connectors. The controller connector has only four pins; remote-device connectors have sixteen.

During installation, the extra pins in the remote connectors are configured with jumpers that define a device's DECdataway address. Connectors of devices that use more than one DECdataway address are configured with that device's lowest address.

4.3.2.4 DECdataway Terminators -- The two DECdataway cable ends are always terminated in the cables characteristic impedance (200 ohms).

4.3.3 DY System Remote Devices

Although we are not concerned with them here, it should be mentioned that other devices besides DISs attach to the DECdataway. This was indicated in Figure 4-2.

If there were nothing but DISs on the DECdataway, we could say that since a DIS uses two addresses, the DECdataway accommodates 31 of them. But this, in fact, may not be true. Other devices may be present, and since these other devices also have varying numbers of addresses, the number of DISs that can be attached to the DECdataway is not always that straightforward.

Since the ISV11-B is our concern here, and since it is a DIS's interface to the DECdataway, we will briefly discuss a typical DIS.

4.3.3.1 Typical DIS -- Figure 4-3 shows a typical DIS. If you ignore the block labelled: DECdataway Interface (ISV11-B), it is an ordinary computer block diagram. It has: a memory to store programs, a processor to run the programs, and I/O devices to receive and dispatch data. But a few things are missing: there is no console, and there are no mass storage or boot devices. That is where the ISV11-B comes in; it takes the place of the extra devices that would be needed if the DIS were not part of a network.

So, to repeat what we said at the outset, a DIS is an LSI-11 computer with a DECdataway interface. How that interface works is the next subject for discussion.

4.4 FUNCTIONAL DESCRIPTION OF THE ISV11-B

As Figure 4-3 shows, the ISV11-B is itself a computer: it has a processor, a memory, and two I/O interfaces. One interface is to the DECdataway; the other is to the LSI-11 bus.

4.4.1 ISV11-B Processor and Memory

The processor is an 8080, and the memory is a combination of ROM and RAM.

4.4.2 ISV11-B to DECdataway Interface

This interface consists of a Universal Synchronous Receiver Transmitter (USYNRT) chip, and a modem. It responds to commands from a looping routine in the 8080.

Its function is to accept a serial, analog signal from the DECdataway, and: demodulate it, digitize it, disassemble it from its DSBC format, and reassemble it into 8-bit 8080 bus format. It also does the reverse of this process.

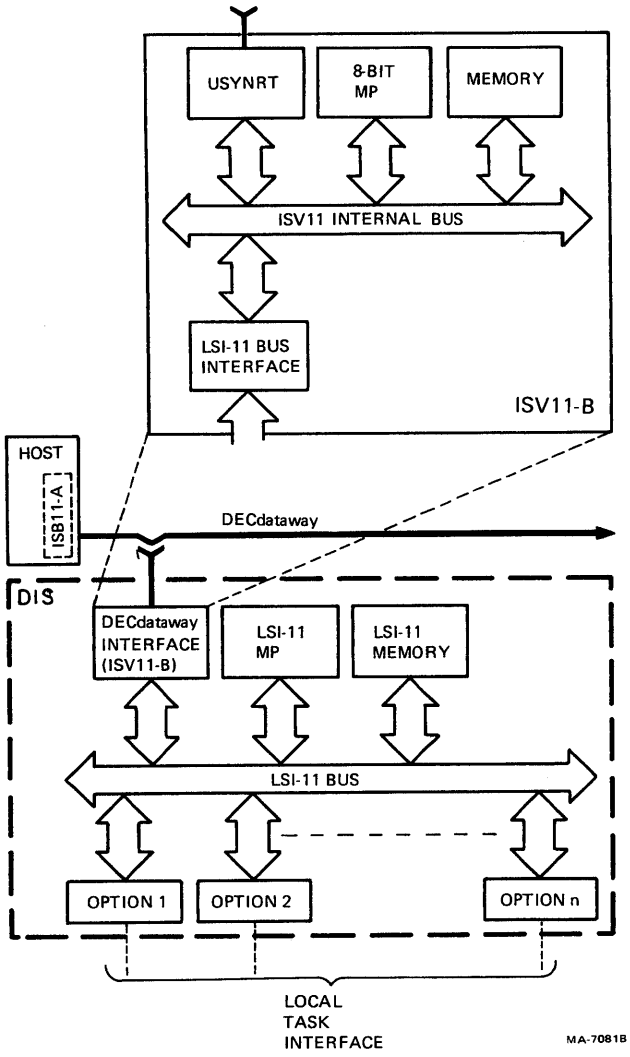


Figure 4-3 DIS with ISV11-B Interface

4.4.3 ISV11-B to LSI-11 Interface

This interface consists of: address decoders, data registers, CSRs and multiplexers. It responds to commands from either the LSI-11 bus or the 8080 bus.

Its function is to accept 16-bit format LSI-11 bus data, and convert it to 8080 bus 8-bit format. It also does the reverse of this process.

4.4.4 ISV11-B Operation

Upon decoding a specific command in its received message stream from the DECdataway, the ISV11-B's microprocessor executes one of the programs stored in the ISV11-B's memory. Among the things that these various programs cause the ISV11-B to do, are the following.

1. Down-line load programs from the host to LSI-11 Memory (including application programs, operating systems, and diagnostics)

2. Down-line load blocks of data from the host to LSI-11 memory

3. Boot the LSI-11

4. Halt the LSI-11

5. Run its own ROM-resident diagnostics (These also run automatically when the power is turned on.)

4.5 ISV11-B MAINTENANCE

Maintenance philosophy for the ISV11-B is option replacement (both modules). However, careful analysis of faults using diagnostics and available test points should permit service personnel to isolate a problem to one of the two modules. Note that the ISV11-B operates only as a unit, that is, with the M8080 and M8084 modules connected together. However, they are not a matched set; a single module can be replaced if necessary.

4.5.1 Built-In Diagnostics

There are on-board diagnostics contained in the ISV11's ROM memory. These are a series of twelve tests (numbered one through fourteen, octal) that run automatically every time the DIS is turned on. If the DECdataway is connected, these tests run only once, otherwise they repeat continuously (except in the case of some error conditions). The tests are also run once by one of the system-level diagnostics: the DECdataway exerciser. Associated with the built-in diagnostics is a display, consisting of four LEDs, that indicates the number of the test being run. There are two types of tests: hardcore and softcore.

4.5.1.1 Hardcore Tests -- The first nine tests (1 to 11 octal) are called hardcore because they test basic characteristics of the ISV11-B. An error in any of these nine tests causes the ISV11-B's microprocessor to loop within the test, thus continuously displaying the number of the first-failed test. A hardcore error also means that the DIS's communication interface is not functioning properly. It is, therefore, prevented from trying to communicate, so that it will not impair the communications of other devices on the DECdataway. Table 4-1 describes the hardcore tests.

Table 4-1 Hardcore Tests

Test	Module	Description
1	M8080	This test checks power-up configuration of 8080 I/O registers 1 and 2, and does basic 8080 instruction test.
2	M8084	This test does individual cyclic redundancy check on each 8080 ROM.
3	M8084	This test checks writing and reading in the 8080 RAM and checks out RAM addresses.
4	M8084	This test checks transmission and reception in USYNRT communications chip, using maintenance mode.
5	M8084	If the dataway connector is unplugged (i.e., address 77 is read), this test checks transmission and reception in the USYNRT through the modem; otherwise the test is skipped.
6	M8084	This test checks ISV11-B interrupt system.
7	M8080	This test checks 8080 I/O register 2 and 8080 I/O registers (3--5) that are common with LSI-11 control and status registers (CSR2 and CSR4).
10	M8080	This test checks time-out feature of DMA logic for access to LSI-11 memory.
11	Both	This test checks LSI-11 interrupt circuit in ISV11-B.

4.5.1.2 Softcore Tests -- The last three tests (12, 13, and 14, octal) of the ISV11-B ROM-resident diagnostic tests are called softcore because they do not stop the ISV11-B from communicating with the host. These tests check the operation of the LSI-11 CPU (processor and memory). Test 13 takes about 11 seconds, but 12 and 14 are so fast their numbers may not be noticed in the LEDs. A softcore error causes the failed test number to be displayed flashing in the LEDs for 10 seconds. The error number (in decimal) is also displayed at the operator's terminal. Table 4-2 describes the softcore tests.

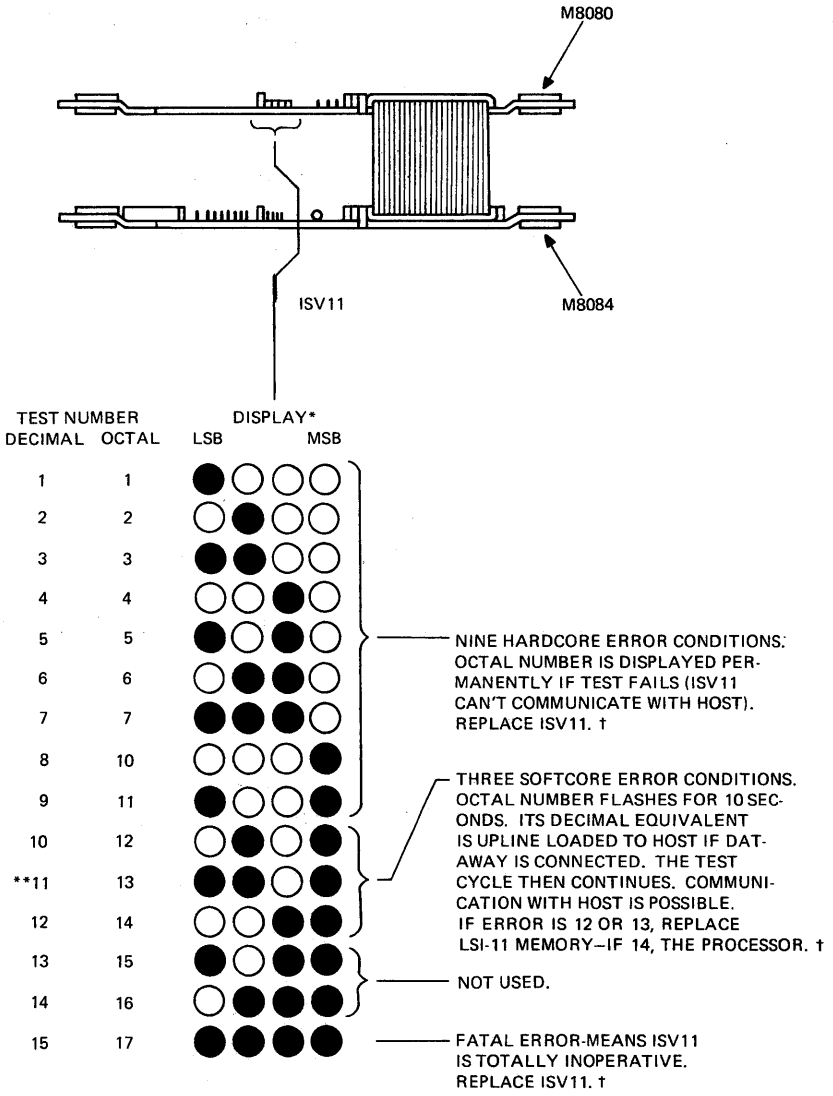
4.5.2 ISV11 Indicators

The LED display for the built-in diagnostics, located on the edge of the ISV11-M8080 board, provides much helpful information for DYS50 fault analysis. Figure 4-4 summarizes the interpretation of this display.

A LED on the ISV11-M8084 board flashes when a carrier is present on the DECdataway. It flashes at a slower rate as carrier activity increases.

Table 4-2 Softcore Tests

Test	Module	Description
12	LSI-11	This test loads a program into LSI-11 memory and then boots the LSI-11; this checks ability of ISV11-B to interrupt the LSI-11 and vice versa.
13	MSV11	This test runs address and data tests on 28K words of LSI-11 memory.
14	LSI-11	This test runs LSI-11 instruction test by loading it into LSI-11 memory and booting the LSI-11 to run it.



*BLACK = ON

** TEST 13 (OCTAL) LASTS ABOUT 11 SECONDS. ITS NUMBER IS DISPLAYED ALL DURING THE TEST, BUT UNLESS IT IS FLASHING, THE TEST HAS NOT FAILED.

† MODULE REPLACEMENT SUGGESTIONS ARE FOR MOST PROBABLE FAILURES. OTHER FAILURES MAY SHOW THE SAME SYMPTOMS.

NOTE: THERE ARE TWO NO-ERROR DISPLAY CONDITIONS

1. IF THERE ARE NO FAILURES, AND THE DATAWAY IS CONNECTED, THE LEDS DISPLAY A ZERO CYCLING FROM LEFT TO RIGHT THROUGH A FIELD OF ONES.
2. IF THERE ARE NO FAILURES, AND THE DATAWAY IS NOT CONNECTED, THE ON-BOARD DIAGNOSTICS KEEP REPEATING. THE LEDS DISPLAY EACH TEST NUMBER AS IT RUNS, BUT 13 (OCTAL) IS THE ONLY ONE OF SUFFICIENT DURATION TO BE READ EASILY.

MA-0104-82

Figure 4-4 ISV11 Display

4.5.3 Test Points

This paragraph identifies the locations and functions of ISV11-B test points. This information helps when troubleshooting the ISV11-B.

Lugs for the test points appear near the LEDs in Figure 4-5. On the M8080, the three test points are to the right of the LEDs and are numbered 4 to 6 from left to right. On the 8084, the test points are to the left of the LED and are numbered 1 to 13 from right to left.

4.5.3.1 M8080 Test Point Description -- Refer to Figure 4-6 for M8080 module test point locations.

Point	Signal	Meaning
TP4	DMR H	Internal DMA request
TP5	FRPLY H	Failed to receive DMA reply
TP6	WAIT L	Force 8080 wait state

4.5.3.2 M8084 Test Point Description -- Refer to Figure 4-7 for M8084 module test point locations.

Point	Signal*	Meaning
TP1	PCS2 BUS MEMR L	8080 memory read
TP2	SL5 T DATA H	USYNRT serial output to modem
TP3	+12 V	--
TP4	SL5 T ENA H	USYNRT transmit enable to modem
TP5	-5 VB	--
TP6	-12 V	--
TP7	+5 V	--
TP8	-5 VA	--
TP9	GND	--
TP10	SL1 DROPOUT H	No signal on dataway
TP11	SL1 R DATA H	Received data to USYNRT
TP12	SL1 T CLOCK H	Transmitter clock from Ø2 (55.556 KHz)
TP13	SL1 R CLOCK H	Receiver clock to USYNRT

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* Includes print on which it appears.

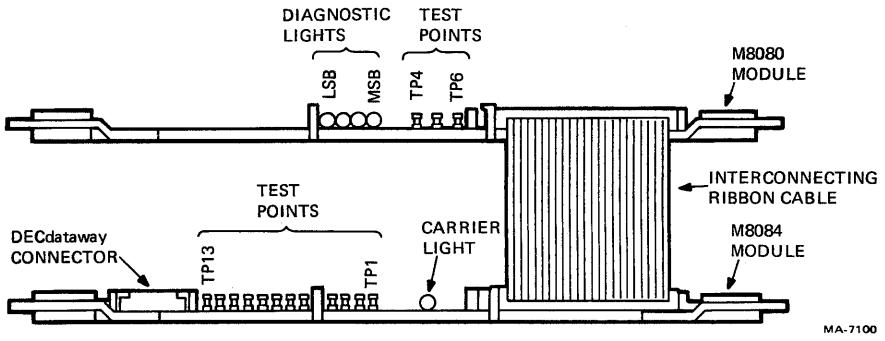


Figure 4-5 ISV11-B Modules (Edge-On)

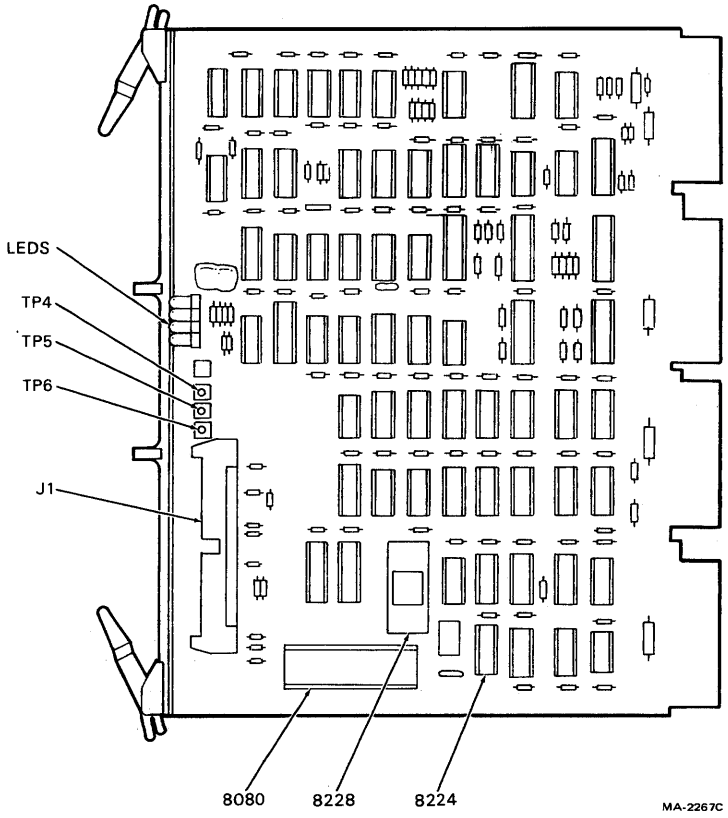


Figure 4-6 M8080 Module

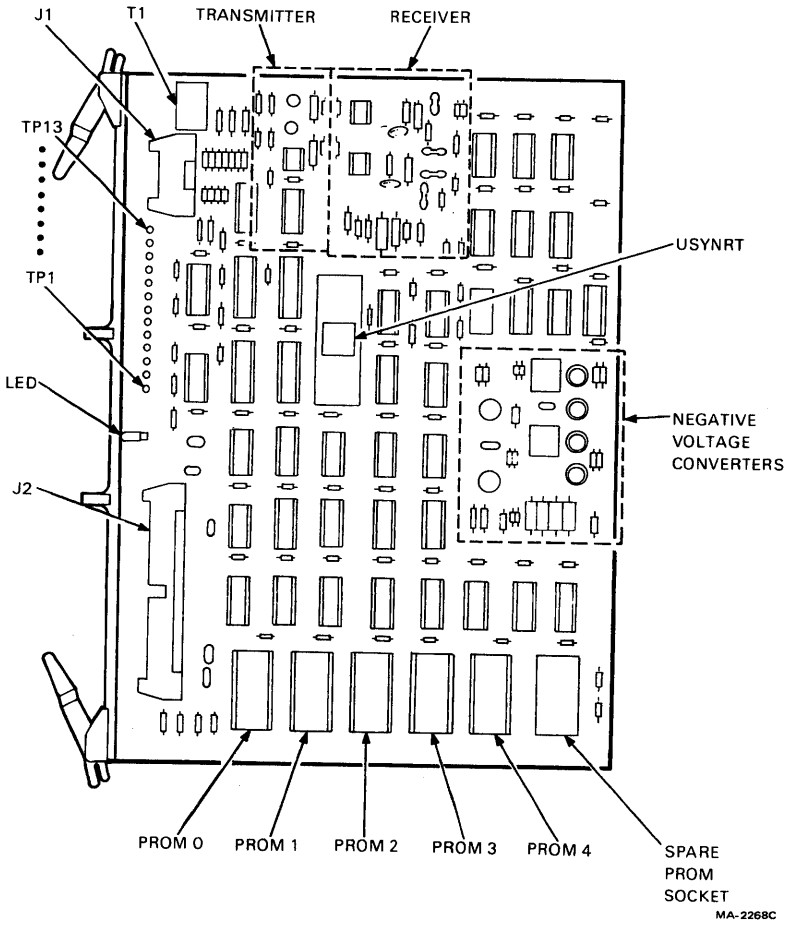


Figure 4-7 M8Ø84 Module

4.5.4 Module Troubleshooting

Use the following procedures to troubleshoot an ISV11-B to one of its two modules.

Service personnel can perform most ISV11-B checks with the modules installed because all test points and LEDs are located at the module edge. However, when it is necessary to access internal points on the module, use the following set-up procedure.

1. Remove the ISV11-B module set.
2. Install a quad-height module extender (W987).
3. Plug the M8Ø8Ø into the module extender.
4. Let the M8Ø84 hang by the interconnecting cable.

CAUTION

Be careful that the M8Ø84 touches nothing that will short any of its components.

4.5.4.1 Quick Check for Major Problems -- These tests check the basic functions of ISV11-B modules. They are particularly useful if the 8080 does not run. (All maintenance LEDs are on.) Unless otherwise indicated, all test points are on the outside edge of the M8084. Testing requires a voltmeter and an oscilloscope (preferred) or logic probe.

NOTE

TP7 (+5 V) and TP9 (GND) can be used to power the logic probe.

1. Using TP9 as a ground reference, make sure that the following supply voltages are present.

   +5 V ± 5% at TP7
   +12 V ± 5% at TP3
   -12 V ± 10% at TP6
   -5 VA ± 5% at TP8
   -5 VB ± 5% at TP5

2. Check that the modem transmitter clock, T CLOCK H, is present on TP12. It is a square wave with period 18 us. This test also verifies that the 8080 clock generator is working.

3. Check that 8080 memory read pulses, BUS MEMR L, are present on TP1. This verifies that the 8080 is fetching instructions and running. If not, verify on the M8080 that BPOK H (E14-12) and READY H (E70-23) are asserted. Then replace the 8080 (E70).

4. The carrier-detected LED should turn on (dim or bright glow) when a running dataway is connected, and turn off when the dataway is removed. If the LED stays on, check that T ENA L (TP4) is high. If T ENA L is asserted, the USYNRT chip (E20 on the M8084) or the 8080 program flow is defective.

4.5.4.2 Manual Modem Test -- Perform this test if test 5 (modem test) in the power-up diagnostics fails. Test 5 does not execute unless the dataway is disconnected. Furthermore, do not perform this manual test unless the dataway is disconnected, to prevent disruption of its ongoing activity.

The test checks out most of the circuitry interfacing the USYNRT chip to the dataway. In particular, it verifies the following items.

1. The transmitter turns on and off.
2. The transmitter transmits ones and zeros.
3. The modem analog circuits transmit and receive data.
4. The receiver decodes ones and zeros.
5. The receiver detects the sync pattern (two successive zeros following a one) that locks in carrier detected.
6. The receiver detects the pattern that drops carrier detected (absence of any transition for 1 to 1.5 bit times).

NOTE

There may be subtle failures in either the analog or digital circuitry of the receiver; these can cause occasional CRC errors or other problems. However, these failures may not be detected by this test or test 5. If such a failure is suspected, replace the ISV11-B.

The following tools are required to perform this test.

- Two 6-inch jumpers with alligator clips or miniclips at each end
- Oscilloscope (or logic probe)

Observe the carrier-detected LED after each step to determine success or failure.

Step		Effect	LED
1	Power up ISV11-B with dataway.	Transmitter idle	Off
2	Connect jumper 1 from TP4 (E ENA L) to TP9 (GND).	Transmit 1s	Off
3	Connect jumper 2 from TP2 (T DATA H) to TP9 (GND).	Transmit Øs	On
4	Disconnect jumper 1.	Transmit 1s	On
5	Disconnect jumper 2.	Transmitter idle	Off

If the test fails, repeat it, observing these points with the scope after each step.

Step	R CLOCK H (TP13)	R DATA H (TP11)
1	Logic Ø	Logic 1
2	Logic Ø	Square wave (18 us)
3	Square wave (18 us)	Logic Ø
4	Square wave (18 us)	Square wave (18 us)
5	Logic Ø	Logic 1

4.6 ISV11-B DETAILED DESCRIPTION

The ISV11-B option consists of two quad-height printed circuit boards. It is built around two large-scale monolithic integrated circuits: an 8080 microprocessor, and an LSI synchronous communications device (USYNRT). To understand how the hardware functions, you must be familiar with the operation of these two circuits as explained in the vendor manuals. A signal name glossary appears at the end of this chapter.

Figure 4-8 is a block diagram showing the logical organization of the hardware on the M8080 ISV11-B microprocessor and the M8084 serial line unit. Logically the system has three major subdivisions organized around two internal buses, one of which is simply an extension of the LSI-11 bus. The processing unit (upper left in Figure 4-8) consists of elements of both boards. It includes the 8080 microprocessor, its associated clock and gating circuits, and local memory.

Communication between microprocessor and local memory is over the 8080 bus. This bus runs through both boards, connecting the processing unit to the other two major parts of the logic. The interface between the 8080 bus and the DECdataway (upper right in Figure 4-8) is entirely on the M8084 module. This subsystem is based on the USYNRT communications chip and connects to the dataway by a modem. The remaining hardware (lower half of Figure 4-8) is on the M8080 module. It includes registers, decoders, and other minor logic elements that connect the 8080 bus to the LSI-11 bus. The LSI-11 bus in turn connects to the LSI-11, its memory, and peripheral equipment.

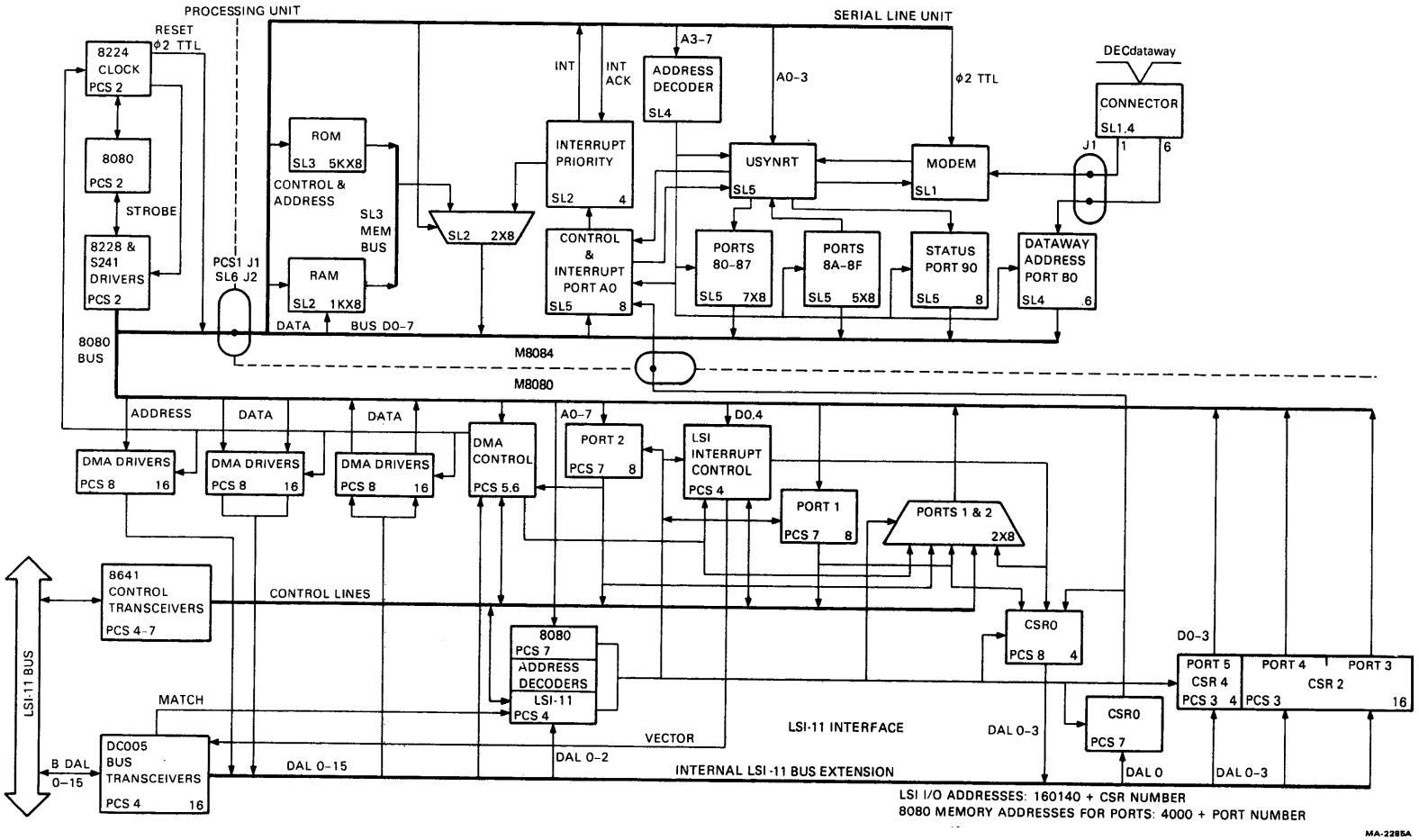


Figure 4-8 ISV11-B Logical Organization

The hardware on each module appears in a set of circuit schematics, code CS. Each set has a drawing number in the form X-Ø-1. (X is the board designation.) A revised schematic has a revision letter to the right of the drawing number. The individual sheets of each drawing set are labeled for convenient referencing. For example, the labels on the six sheets of 54-13290-Ø-1 (M8Ø84 module) are SL1 to SL6, and those on the eight sheets of M8Ø8Ø-Ø-1 are PCS1 to PCS8. These labels serve as prefixes in signal names to indicate signal origin. They also appear in the text and block diagrams for referencing individual prints.

In Figure 4-8 these labels appear in the lower left corners of each block to indicate which print contains the logic represented by the block. Parts of a print are indicated by combining the letters and numbers along the edges. Paragraphs 4.7 through 4.9 give a detailed description of the hardware on the two modules. Discussion is geared to the prints, but you should also refer to Figure 4-8 whenever necessary.

Some logic signals on the boards are available at test sockets shown in the lower left on SL6 and the upper right on PCS6. In some cases the lines to these test pins are not true logic signals at all, but gate inputs tied to +5 V. Therefore, they play no real role in system operation; but they can be pulled low to disable various parts of the logic for GR test purposes. These pseudo signals are identified on the prints by the word test.

4.7 PROCESSING UNIT

This unit occupies part of both boards and appears on three prints: PCS2, SL2, and SL3. PCS2 shows the 8Ø8Ø microprocessor with its clock and gating circuits. The 8228 has bidirectional drivers for the 8 data lines in the 8Ø8Ø bus; the two 74S241s below it provide unidirectional driving for the 16 address lines. The 8224 clock circuit at the left supplies the Ø1 and Ø2 clocks for the microprocessor chip, and the Ø2 TTL clock for the serial line unit. (All clocks are 2 MHz.)

At the beginning of every microprocessor machine cycle, the 8Ø8Ø places status information identifying the use of the cycle on its D outputs; it also sends a sync signal to the 8224. The 8224 responds by sending a strobe to the 8228, causing it to load status into a set of latches. This frees the data lines for transfers during the cycle. The status information indicates the kinds of events that occur during the cycle. From the latched status bits and 8Ø8Ø control signals WR (write) and DBIN (data bus in), 8228 sets up memory, I/O control signals, and interrupt acknowledgement for the cycle.

A memory read can fetch an instruction, an operand, or an item from the stack; writing in memory can be for an operand or a stack item. Bus I/O control signals (in field DI on the print) are produced by the 8228 I/O outputs. However, they are also asserted by the memory control signals when the address is in the 4ØØØ to 7FFF range (the area of the ISV11-B address space reserved for I/O registers).

The ready input to the 8080 through the 8224 is high, except when a wait is needed for a DMA operation. ENA DMA enables the 8093 so that WAIT goes low; when the acknowledgement appears, READY goes high and the 8080 continues. But, the DMA signals have no effect when I/O WR is true. This prevents an unwanted wait from hanging up the 8080 if DMA signals are generated inadvertently because an I/O operation looks like a DMA operation to DMA logic. When the 8080 does an input or output instruction, it puts the one-byte address on both the upper and lower half of the address lines. Therefore, an I/O port address of 80 or above puts a one on line 15, which may generate ENA DMA. The I/O WR prevents any wait during an IN instruction; however, the I/O WR occurs later during an OUT, and the 8080 may enter the wait state for a single cycle.

The RAM and ROM that constitute local memory are on SL2 and SL3 respectively. The RAM is made up of eight 1K X 1 chips, each storing a single bit of each byte in the 1K. The ROM is made up of five 1K X 8 chips (with space for a sixth), each storing the entire byte for 1K locations. Logic gates at the upper left on SL2 produce a memory select when the 8080 calls for a memory read or write with an address in the 0 to 1FFF range. The select, in turn, enables the decoding of address bits 10 to 12 at the lower left on SL3 to select a single ROM chip or the set of eight RAM chips. The 10 least significant address bits are applied to the address inputs of all chips to select the individual location.

When the RAM is selected and the function is write, bits from the eight data lines are written into the eight RAM chips. The output of the selected ROM, or set of RAMs, is available on the SL3 memory bus. During a read, the data is placed on the 8080 bus via the multiplexer at the upper right on SL2. Drawing TD-ISV11A-0-7 shows the timing of the signals involved in the 8080 reading and writing memory.

4.8 SERIAL LINE UNIT

The heart of this unit is the USYNRT synchronous communications chip at the left on SL5. It is set up for byte operation by a high level at pin 22 and connects corresponding pins for the left and right bytes of its 16 data inputs-outputs. These connect to the eight data lines of the 8080 bus. The 8080 governs the device by supplying control bytes and reading status. The USYNRT in turn uses the modem for handling communication over the serial DECdataway. Serial data received from the modem at RSI is assembled into bytes, and available to the processing unit via the eight data lines. Transmit bytes supplied over data lines are passed on serially to the modem from TSO.

The 8080 moves bytes to and from the interface via its I/O ports. Port selection is made by the address decoder at the right on SL4. The number of ports is small, and an I/O bus control signal is generated by either an I/O transfer or memory access in the appropriate address range. Therefore, decoding a few address bits

and the I/O signals is sufficient to select among ports 90, A0, B0, and the USYNRT registers. From port B0 the 8080 can learn its own dataway port address, wired into the DECdataway connector and available through the gates at the left. SEL 8X enables the USYNRT data lines.

Selection among various registers is made by address bits 0 to 2, applied to the USYNRT address inputs on SL5. Register reading and writing uses separate addresses, so A03 is connected to the USYNRT write input. A one enables writing and drives the USYNRT data lines from the 8080 bus through the two 74S241s at the lower right. When a zero places a register on the data lines, READ 8X from the address decoder drives the 8080 bus from them. The E30 gate below the decoder on SL4 prevents any register selection if the 8080 should give a read function for a write port.

The remaining two ports are at the upper right on SL5, where address 90 reads status bits from the USYNRT and modem, and the LSI-11 interrupt request through E22. Address A0 loads a byte from the 8080 bus into the register in E27. The control bits supplied include enables for transmitter and receiver in the USYNRT maintenance mode, and for various conditions that can request interrupts through gates at the upper right.

Selecting maintenance mode inhibits generation of the transmit enable to the modem (T ENA at CI), even if the USYNRT transmitter is active (TX ACT). The interrupt request levels are applied to the latch and priority network at the upper left on SL2. Any interrupt request produces the INT signal, which goes to the 8080. An acknowledgement from the 8080 latches the current request, enables the multiplexer for the SL2 bus (8080 bus data lines), and selects as multiplexer input an RST instruction encoded from the number of the highest priority request. The 8080 then executes the RST as a call to the corresponding location (as listed in the table at the lower right on SL5).

4.8.1 Serial Transmitter-Receiver

The modem for the serial line unit takes up most of SL1. The basic time reference is the 02 TTL clock supplied by the 8224 clock circuit associated with the 8080 microprocessor. This clock drives the receiver directly. For the transmitter, the exclusive OR gate at A7 (with the delay introduced by two inverters at one of its inputs) acts as an edge detector to multiply the basic clock to 4 MHz. From this, the E28 counter produces the 8X clock by dividing by nine. This is accomplished by loading 7 at the clock following the carry out produced by a count of 15. The 8X clock counts the E23 counter, which runs on a continuous 16-count cycle so that its two middle bits provide division by 4 and 8. The T (1X) clock drives the USYNRT transmitter and shifts out the data; the 1X and 2X clocks together are used for biphase encoding of data transmitted over the dataway. Table 4-3 lists characteristics of the various clocks.

Table 4-3 Clock Characteristics

Clock	Period (us)	Frequency
ø2 TTL	Ø.5Ø	2 MHz
8X CLK	2.25	444.444 KHz
2X CLK	9.ØØ	111.111 KHz
T CLOCK	18.ØØ	55.555 KHz

The modem is coupled to the DECdataway by transformer T1; its secondary winding connects the serial line at pins 9 and 1Ø of the internal dataway connector. The transformer is the 1-1-1 type. A pulse train in from the line generates two output trains, one positive and the other negative; both have the same amplitude as the input. The transmitter uses only one primary coil each way, so the output is a 5 V signal, either positive or negative.

The two Zener diodes back-to-back (shown at the left of the connector) draw no current until the potential reaches 9 V; then they draw a great deal. This prevents a surge on the dataway from burning out the operational amplifiers. During transmission the Zeners limit output to 9 V, even though the transmitter circuit output is about 12 V. There is an effective 1ØØ ohm load with the dataway connected. This is due to either the 2ØØ ohm terminating resistor being in parallel with the cable or mounted in the middle of the 2ØØ ohm cable. Therefore, the line is actually driven at about 5 V.

The only control signal supplied by the USYNRT to the modem is T ENA at D8. When this signal is true, the T1 primary can be driven at one side or the other to drive the serial line. When T ENA is false, the transmitter is disabled, and the receiver picks up any data coming from the DECdataway.

The disable and external inputs, as well as various circuit outputs, are available at the test socket on SL6. Test inputs allow for disabling the clock and the raw received data; then external inputs can be substituted for them. Conversely, without the disables, the external connections make the internal clock and raw data available at the test socket.

4.8.1.1 Transmitter -- Data from the USYNRT enters the transmitter circuit at E31-13 (C8), ANDed with the T clock. The gate keeps the J and K inputs to the E12-5 flip-flop high, except when the data bit is one and T clock is high. Therefore, a zero enables JK for the whole bit period, and a one enables it for half the bit period. You can see this in Figure 4-9, which shows the relationship between data, flip-flop signals, and transmitter clocks. The flip-flop toggles twice during a zero bit, but only once during a one. The state of the flip-flop drives one side or the other of the T1 primary. Therefore, there are two zero-crossings during transmission of a zero on the dataway, but only one during a one. This is the so-called biphase modulation technique of data transmission.

The circuit in D8 senses the +5 V. Should the voltage drop slightly, Q4 conducts and disables T ENA. Therefore, if the power is failing, the transmitter is disabled even if the USYNRT is sending data (which may be invalid).

4.8.1.2 Receiver -- Changes in current flow through the T1 primary are sensed by the receiver circuit (shown at top-center on SL1). A switch in direction, caused either by the serial line (secondary) or transmitter, reverses the state of the raw data outputs (shown at the upper right). A string of logic components is shown from left to right, across the center, and in the lower right of the print. These logic components process this raw data to detect the start of message, derive data bits and a clock to pass on to the USYNRT, and detect a dropout of the received signal. The logic is driven by the 2 MHz Ø2 TTL clock, which runs at 36 times the bit rate of the dataway. Therefore, the clock not only synchronizes the raw data to the ISV11-B, but also provides a finer resolution for sampling it.

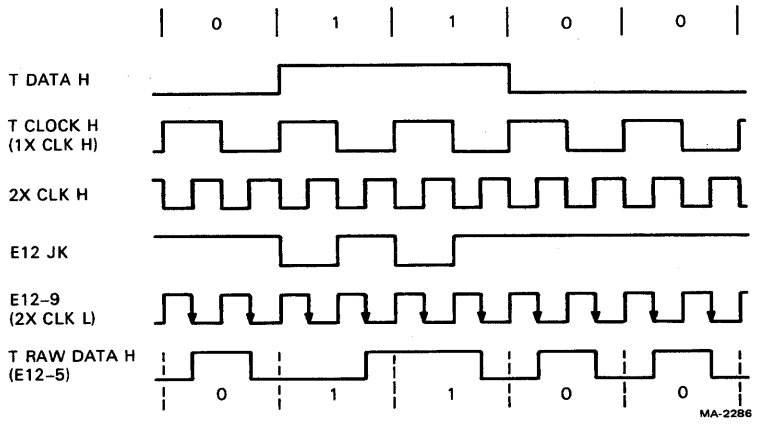


Figure 4-9 Transmitter Timing

Figure 4-10 is a simplified diagram of the receiver with most components in the same relative position as they appear on the print. The dual signal generated by the T1 primary from the dataway is applied to a pair of operational amplifiers. These have gain +1 and high input impedance for isolation. The 56K input resistors prevent a power turn-off in the ISV11-B receiver from dragging down the dataway. The bandpass of the filters at the amplifier outputs eliminates both high and low frequency noise, but it attenuates the signal to about one third.

For generating raw data, the threshold comparator uses a reference of 50 mV; this guarantees the spec of 100 mV, one-third of the 300 mV minimum dataway signal. A switch in the comparator outputs occurs only when the signal goes above the positive threshold after having been negative, or below the negative threshold after having been positive. Changes in the raw data are synchronized to the clock by a flip-flop.

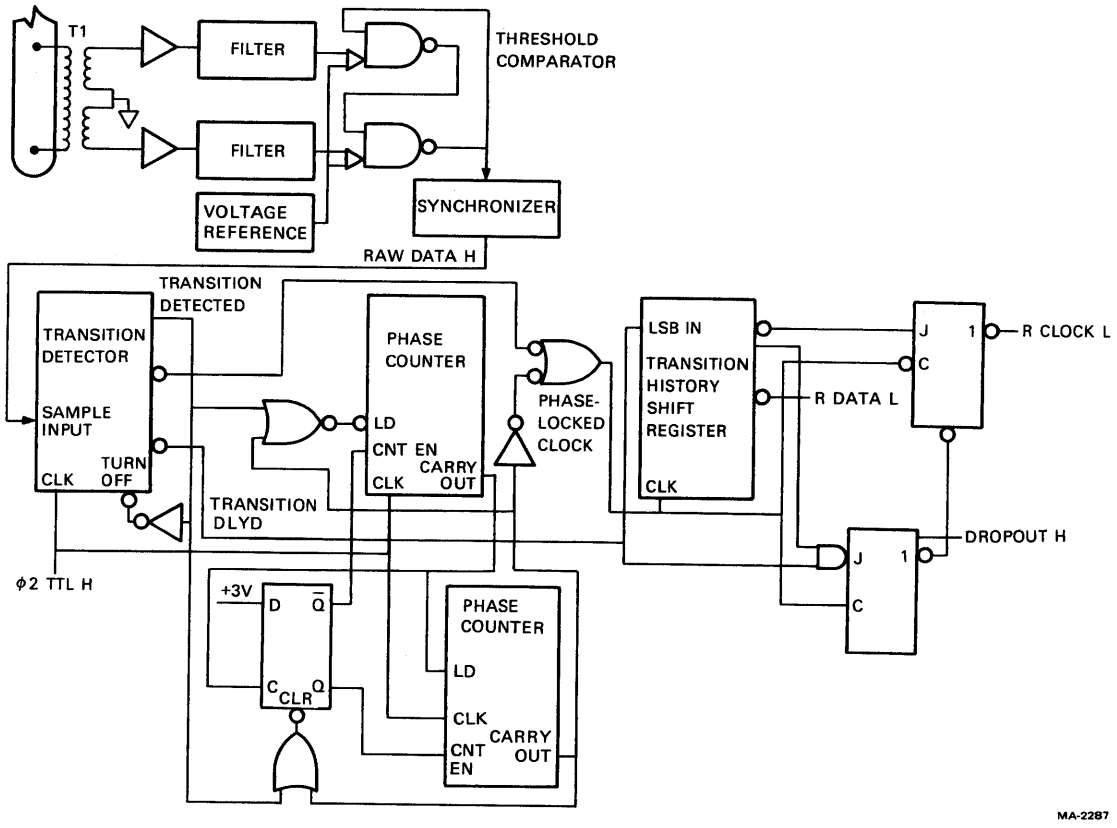


Figure 4-10 Receiver Simplified Block Diagram

The logic shown across the lower part of Figure 4-1Ø contains three main parts: a transition detector at the left, a phase-locked clock generator, and a shift register for recording recent transition history in raw data from the receiver circuit. This history is necessary for recognizing the start of message and modem dropout. It also distinguishes between zeros and ones in the received data it supplies to the USYNRT. Figure 4-11 shows the timing of major signals associated with this transition processing logic.

A message always starts with several ones followed by at least two zeros for synchronization. Figure 4-11 shows signal configuration for a message beginning with 1ØØ, followed by several arbitrary bits, and then a modem dropout. The transition detector generates three signals associated with a transition in the raw data.

Following synchronization of a transition, the first 2 MHz clock produces the transition-detected signal. This is on for two clock periods; during that time it turns off the detector to inhibit further sampling of the raw data. This filters out noise near the modem comparator threshold, preventing any noise surrounding a transition from being mistaken for another transition. The second signal, transition delayed, has the same form as transition detected; however, it has opposite polarity and is offset by one clock period.

The difference in these two signals is that transition detected inhibits the detector (resetting the phase counter), and transition low actually represents the transition for processing by the remaining logic. The third signal from the detector produces the phase-locked clock, which occurs at the end of transition detected.

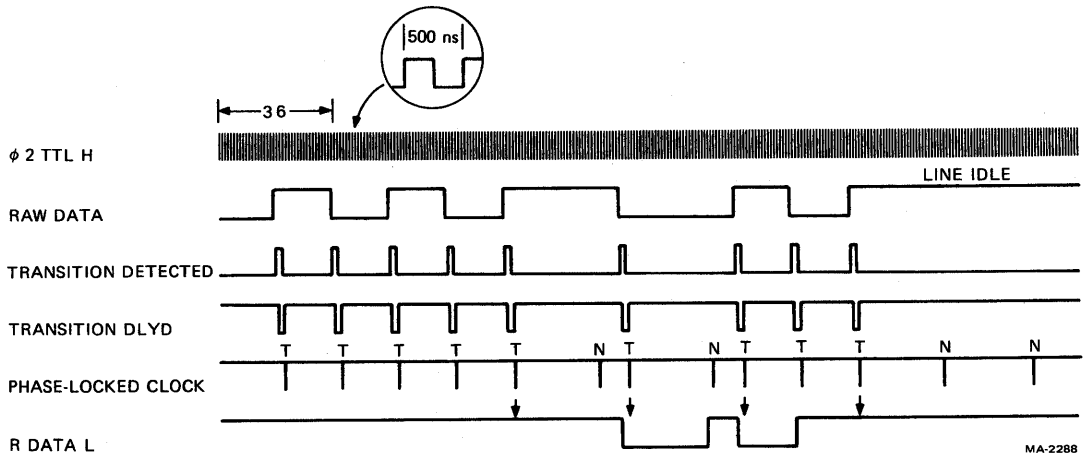


Figure 4-11 Receiver Timing

The phase counter is reset at every transition, but in the absence of transitions it simulates the phase-locked clock every time it reaches 3Ø. The Ts and Ns in the timing diagram distinguish phase-locked clocks produced by transitions (T) from those that are not (N). Figure 4-11 illustrates the exact theoretical timing for a serial signal from the bus. In a real situation, transitions can be quite late without adversely affecting reception.

Each phase-locked clock shifts the transition history. Where the bit shifted into the register reflects transition low, detection of a transition causes a zero to be entered. After the line has been idle, the phase-locked clock that occurs at the fifth consecutive transition (a one succeeded by two zeros) clears the dropout flag, turning on the LED. From that point on, the data represented by the bottom line in the diagram is available to the USYNRT from the second bit position in the history shift register. The USYNRT samples incoming data at the R clock, which is represented by arrows and occurs at the trailing edge of the phase-locked clock. The absence of two transitions in a row sets the dropout flag, turning off the receiver clock.

The above discussion should provide a basic understanding of what the receiver does, and how the incoming data is supplied to the USYNRT. But to understand in detail how the logic works, turn to the circuit schematic (print SL1) and the complete timing diagram (TD-ISV11A-Ø-8), which show all associated signals. Raw data synchronization is provided by flip-flop E8-9 located at B3 on the print. The transition detector at the left is made up of a shift register and three exclusive OR gates. When pin 9 of E11 is high, each clock shifts the register, sampling the raw data at the LSB. When pin 9 is low, each clock loads the register from the data inputs; but these are connected so the register still shifts, ignoring the raw data. Therefore, each transition is shifted through the register, giving a sequence of signals through the exclusive OR gates.

E9-11 and E9-6 are transition detected and transition delayed. These gates are driven from pins 13 and 15, and 11 respectively (not 14 of E11), so they generate signal trains with on times of two clock periods (E9-6 offset by one period). E9-8, which generates the phase-locked clock, is fed from E11-13 and 11, and thus occupies the second half of the transition-delayed on time.

Binary counters E3 and E1 are configured for a count of 3Ø, 17 in E3 plus 13 in E1. Detection of a transition clears E3 and sets an enable-disable flip-flop (E8-5). This allows E3 to count the 2 MHz clock after transition detected goes off, but inhibits E1 from doing so. When E3 counts to 15, the carry out loads three into E1 and sets the flip-flop. This disables E3 and enables E1, which can then continue the count. When E1 reaches 15 (total 3Ø), the carry out produces a phase-locked clock and clears the flip-flop; the next 2 MHz clock clears E3 to restart the count. Therefore, a phase-locked clock occurs at each transition, and also when there is a count of 3Ø without a transition. E15 is the history shift register.

Initially the E11 bits are alike: E9-11 is low, which causes the 2 MHz clock to shift E11; E9-8 is high, so the phase-locked clock is low; and E9-6 is also high. When the raw data changes, the next 2 MHz clock shifts E11. This causes pin 15 to differ from the other three outputs. In particular, pin 15 differs from pin 13, so E9-11 goes high, enabling the load function at both E11 and E3.

The first clock after detection of the transition loads zero into E3 and shifts E11 without sampling the raw data. That is, pin 15 remains the same and the transition lies between pins 14 and 13. With this change, E9-6 supplies a low input to E15 DØ and E2 J. The second clock loads again, moving the transition between pins 13 and 11. This causes E9-8 to drop, producing a phase-locked clock which shifts E15 and loads zero into E15 RØ since E9-6 is still low.

E9-11 also drops, which reenables shifting and counting. The third clock then counts E3 to one and shifts E11, resampling the raw data and shifting out the preceding transition. This raises both E9-6 and E9-8, dropping the phase-locked clock. If a transition were detected, E9-11 would again go high and start the whole sequence over.

Serial line transmission always begins with a few ones followed by at least two zeros. The final one and the two zeros provide a string of five transitions, a half bit time apart. Following the just defined procedure, you can see that the first four transitions result in four zeros being shifted into E15. This enables the AND gates at the clear input to the dropout flip-flop E2. At the fifth transition, the phase-locked clock clears E2. This removes both the dropout signal to the USYNRT and the hold-clear on flip-flop E12-3, generating the R clock for the USYNRT receiver.

Once the system is synchronized to the incoming serial signal, a transition that occurs before a count of 3Ø following a preceding transition produces a phase-locked clock that loads a zero into E15. If there is no transition by clock 29, clock 3Ø counts E3 to 15, and the carry out produces a phase-locked clock that loads a one into E15 (since E9-6 is high). But subsequent detection of a transition before the next 29 count (restarting the count with no transition detected ships the extra load) generates a phase-locked clock that loads a zero into E15. Therefore, a zero data bit causes the loading of two successive zeros into the first two stages of E15. A one results in a zero in RØ and a one in R1 following a pair of shifts. Thus, at the end of each bit time, the state of R1 represents the received data.

Since at this time RØ is zero for either a zero or a one data bit, the trailing edge of the phase-locked clock sets E12-3 to start a cycle of the R clock. Since the K input is held high, the flip-flop clears in the middle of the next bit time regardless of what the first phase-locked clock brings into RØ. The first data bit the USYNRT actually reads is the second zero in the sync pair.

If no transition is detected through the fifty-eighth clock, the fifty-ninth counts E3 to 15 a second time. This produces a second nontransition phase-locked clock. With E9-6 still high and a one already in E15 RØ, this sets E2, indicating a modem dropout and disabling the receiver clock.

4.8.1.3 Negative Voltage Converters -- The circuit at the left on SL6 provides one -12 V and two -5 V supplies from +5 V. Two separate -5 V supplies are necessary for handling the large power requirements of the PROMs.

Each -5 V converter consists of an inverter oscillator using a saturable core transformer, a negative rectifier, a filter, and a three-terminal regulator chip that produces the regulated -5 V. Oscillator frequency is about 4Ø KHz. The transformer primary has a 9 V square wave centered at +5 V; the secondary has an 18 V square wave centered at ground. Filter output to the regulator is approximately -8 V.

The -12 V converter uses the 9 V square wave across the T3 primary to drive a charge pump (C55, D1Ø, D11, C56). The pump output is superimposed on the -8 V rectified secondary output to produce an unregulated -17 V; this is converted to a regulated -12 V by Zener diode D12.

To prevent large instantaneous switching currents in the oscillators from coupling into the main +5 V supply, they have separate, inner layer ground and V_{cc} planes. The separate V_{cc} plane is decoupled from the main plane by an LC filter, and the separate ground plane is connected to the main ground plane at a single point.

4.9 LSI-11 BUS INTERFACE

This unit handles all communication (programmed transfers, DMA transfers, and interrupts) between the ISV11-B and the LSI-11 processor and memory. The bidirectional LSI-11 internal bus extension (PCS4 DAL) interfaces to the bidirectional LSI-11 bus data and address lines (B DAL) via the DCØØ5 transceivers at the left on PCS4.

The XMIT input is enabled for driving the LSI-11 bus from its extension during one of two events: when the LSI-11 is reading a control status register (CSR), or when the ISV11-B is sending DMA address or data to the LSI-11 memory or I/O bank. At all other times the REC input is enabled, driving the extension from the LSI-11 bus. However, enabling REC also allows high levels at the JAV inputs to drive the LSI-11 bus lines independently. These inputs are connected for VECTOR to place an interrupt vector on the B DAL lines, where a jumper in is a one.

When the I/O bank select signal BS7 is true at E23-13, the JA inputs are compared with levels on certain LSI-11 bus lines. The lines are not connected to the chips in order; this allows a comparison between JA inputs and bus lines 3 to 12. The match output is true when BS7 is true and bus lines 3 to 12 contain the address of the ISV11-B CSRs set into the JA jumpers. A jumper in is a one.

Type 8641 transceivers are used for interfacing to LSI-11 bus control signals (usually bidirectional). These transceivers appear on various prints, next to the logic with which they are associated.

4.9.1 Port Transfers

Programmed transfers are handled through what are regarded as 16-bit control status registers from the LSI-11, and 8-bit ports from the 8080 microprocessor in the ISV11-B. Furthermore, since addressing is from different buses and the I/O banks occupy different parts of the processor's address spaces, there are two completely separate address decoders.

The LSI-11 decoder is a standard DC004 (PCS4 right) enabled by matching the ISV11-B CSR jumper address with the address supplied on the B DAL lines. Bus control signals come to the DC004 via the transceivers on PCS6, since the same signals are also involved in DMA control. The sync latches the three least significant address bits, which are decoded for selecting the CSRs. (Select signals are backward, since high levels are applied to the DAL inputs.) For output, DOUT generates a high or low byte strobe, or both, depending on DAL 0 and whether WTBT selects a byte or whole word. For input, DIN gives an INWD strobe. Both the address latch and the data strobe produce a bus reply through the 8641.

The LSI-11 supplies the address of the transfer control block (TCB) via the CSRs on PCS3. The only other data comes to the ISV11-B via CSR0, when a one on DAL 0 sets the flip-flop in the lower right corner on PCS7 to request an 8080 interrupt. The gate just above provides a read strobe for CSR0, allowing the LSI-11 to read its own interrupt request and other status information via the 74LS367 (E7) at the lower left corner on PCS8. For test purposes the ISV11-B can load the CSRs via the I/O page in LSI-11 address space.

Decoding addresses of 8080 ports in the LSI-11 bus interface is accomplished by the logic at the top on PCS7. There, address bits 0 to 2 are decoded to select the port on an I/O function when bits 3 to 7 are all zero. Only ports 1 and 2 (the E39 and E36 registers below the decoder) can be written by the 8080, and for these the select lines also generate write signals on an I/O write. From these two ports, the only bit the LSI-11 can read is boot status (port 1 bit 1) through CSR0. Setting and clearing port 1 bit 7 boots the LSI-11 by simulating a power-up signal on the DCOK line of the LSI-11 bus. To halt the LSI-11, port 1 bit 6 is handled by a separate flip-flop, so it can also be set by a power failure.

Port 2 bit 5 is not included in the register, because it is used to clear the LSI interrupt request flip-flop at the lower right. Port 1 bit Ø and port 2 bit 4 do not show up here at all; they are used to request interrupts at the LSI-11 as described in the following discussion.

The 8Ø8Ø can read most of what it supplies to ports 1 and 2, plus a few other bits from interrupt and DMA control, via the E38 and E4Ø multiplexers at the left. Port Ø is not used; ports 3, 4, and 5 correspond to the three bytes of the TCB address in CSR2, CSR3, and CSR4 (PCS3).

4.9.2 LSI-11 Interrupt Control

Interrupt requests from the 8Ø8Ø to the LSI-11 are handled by the standard DCØØ3 dual-interrupt circuit at the upper right on PCS4. The 8Ø8Ø can make requests on two levels, A and B, associated with vector locations 3ØØ and 3Ø4 respectively in the LSI-11. Request inputs to the DCØØ3 are held high, so making and dropping requests on levels A and B respectively, are under writing control in port 1 bit Ø and port 2 bit 4. Status of current interrupt requests (LSI-11 bus A and B) is available to the LSI-11 via CSRØ, and to the M8Ø8Ø via ports 1 and 2.

A request made on either level asserts the BIRQ signal to the LSI-11. Once the LSI-11 responds with DIN and the acknowledgement BIAKI, the DCØØ3 disables BIRQ and asserts VECTOR. This produces a bus reply through the DCØØ4 below and places the vector address on the LSI-11 bus via the DCØØ5 JAV inputs at the left. The signal VEC RQST B puts a zero or one on line two, depending on whether the interrupt is on level A or B.

4.9.3 DMA Transfers

The upper 32K-byte half of the 8Ø8Ø address space is used for referencing any 32K-byte section of the LSI-11 address space by means of DMA transfers. Before initiating any DMA operation with a 28K memory, the 8Ø8Ø must set up AD 15, which is port 2 bit Ø (PCS7 B4), as address bit 15 on the LSI-11 bus. This indicates which half of the LSI-11 address space is referenced when A15 on the 8Ø8Ø bus is one. Then, the 8Ø8Ø simply makes a memory reference in the upper half of its own space, to reference the selected half of the LSI-11 space, using DMA request and control logic on PCS5 and PCS6. (A 124K memory would require that AD 16 and AD 17 be set up as well.) The 8Ø8Ø must also set BS7 (port 2 bit 3) if the address location lies in the I/O bank. Two timing diagrams, TD-ISV-11A-Ø-5 and TD-ISU-11A-Ø-6, show the relationships among the various quantities involved in output and input DMA transfers: LSI-11 bus signals, control signals for the 8Ø8Ø, the 8Ø8Ø clocks, and machine states. An R or T in parentheses next to a signal name means it is received or transmitted by the ISV11-B over the LSI-11 bus.

Addresses and data move between the two buses via the 74LS367 drivers on PCS8. The signal T ADDR EN places the address on the

LSI-11 bus through parts of the driver chips at the left. However, only 15 bits come from the 8080 bus address lines; bit 15 (A8) comes from port 2 instead. Each data transfer is a single byte, with the low or high position on the DAL lines selected by A00. Data is gated from the 8080 bus to LSI-11 bus by T DATA EN, with the low byte handled by E60 and part of E46, and the high byte by E59 and part of E51. Gating from the LSI-11 bus to 8080 bus is controlled by a DMA signal derived directly from the 8080 memory read, with the low byte handled by E61 and part of E7, and high byte by E52 and part of E51.

An 8080 memory reference in the 8000 to FFFF range produces ENA DMA at the upper left on PCS5. This causes the 8080 to wait by pulling down the 8224 ready input on PCS2. On PCS5 it generates the appropriate DMA memory read or write level, and a DMA request that goes out on the LSI-11 bus and also clears flip-flop E15-9 at the lower left. When the LSI-11 sends the DMA grant in, E12-5 sets, preventing the grant from passing out to the next device. With the grant on, negation of both the sync and the reply at the end of the current bus cycle sets E12-9. This generates SACK on the LSI-11 bus to acknowledge that the ISV11-B has become bus master; it also drops the request, following which the LSI-11 drops the grant.

The acknowledgement also triggers a timing circuit based on shift register E9 at the upper left on PCS6. SACK sets E19-5 to feed a one into the LSB register and causes the output of the E17-8 AND gate to go low. The output of this gate is fed back to one of its inputs. This makes the output oscillate, which supplies a rising-edge clock with a period of 110 ns beginning about half a period after SACK goes true. Since the setting of E9 R0 clears E19-5, the clock provides timing for the transfer by passing a single one through the shift register.

This moving one, in turn, controls the column of flip-flops shown at the center of the drawing. A1 in R0 sets T ADDR EN to place the address on the LSI-11 bus, and to gate the state of BS7 from port 2 onto the B BS7 line. This indicates whether the transfer is for memory or the I/O bank. At the same time a write function turns on T WTBT to specify an output byte. Time 330 turns on T SYNC, and time 440 clears T ADDR EN. For writing, 440 also sets T DATA EN to gate the byte onto the LSI-11 bus, and 550 turns on T DOUT to make the slave accept it. But for reading, 550 turns on T DIN to tell the slave to send data; the read level itself gates the DAL lines onto the 8080 bus, with the transfer time determined by the slave.

With SACK still asserted, the reply from the slave produces the DMA acknowledgement (C7) that frees the 8080. The freed 8080 negates the memory signals, negating DMR (PCS5). DMR then cancels either T DOUT or T DIN, whichever is on. Finally the trailing edge of RRPLY triggers an identical reset timer based on shift register E10. Reset time R110 turns off T SYNC, T DATA EN, and T WTBT (if on); it also sets E15-9 (at the lower left on PCS5) to turn off SACK.

Each request triggers the 39 us one-shot in the time-out circuit at the bottom on PCS6. Completion of a transfer clears it and prevents the clearing from affecting the E15-5 flip-flop at the right. However, should the one-shot time out, it indicates failure of the slave to reply in a reasonable time; then the flip-flop sets to generate FRPLY. This signal produces the DMA ACK to free the 8080. When DMR subsequently goes off, it clears FRPLY but also sets E19-9, triggering the reset time to clear the DMA logic.

4.10 FUNCTIONAL FLOWS

Figures 4-12 through 4-17 show the system's major operations in terms of functional flow, that is, as the signal paths and logic elements that enter into their execution. All logic elements are labeled for the circuit schematics on which they appear. To help pinpoint the trouble, the figures identify all significant elements that play a role in a given operational sequence. You can then turn to the referenced schematics for details of circuit, signals, and pin connections.

These flows are meant to stand alone; no written description accompanies them since the detailed description of the logic, geared to schematics, has already been presented. All lines are labeled with the actual signal names from the schematics; wherever possible the logic elements are represented by the symbols in the schematics. It has, however, been necessary in some cases to use ordinary blocks as logic elements. These are easily identified because the signal lines entering them have arrowheads.

None of the diagrammed operations comprise only a single sequence of events. Rather, each is made up of several logically distinct but interdependent sequences, such as an 8080 instruction followed in order by an interrupt and another 8080 instruction. Another sequence is an 8080 instruction followed in order by a response from the LSI-11 and an action by the ISV11-B. The numbers in circles indicate the order in which the hardware parts are employed for these sequences. Sections of the hardware tested by power-up diagnostics are labeled with test numbers.

The six flows are in three pairs, and all operations shown involve the microprocessor. The first two drawings show the movement of information in either direction through the serial line unit. The next pair show DMA transfers through the LSI-11 bus interface. Figure 4-16 shows an ISV11-B interrupt request to the LSI-11. Figure 4-17 shows an interrupt request in the opposite direction, the only operation that uses elements of both interfaces in the ISV11-B. There are many other minor operations, such as the 8080 reading or writing a port, and the LSI-11 making a CSR transfer. You can easily identify components that enter into these simpler operations directly from the circuit schematics.

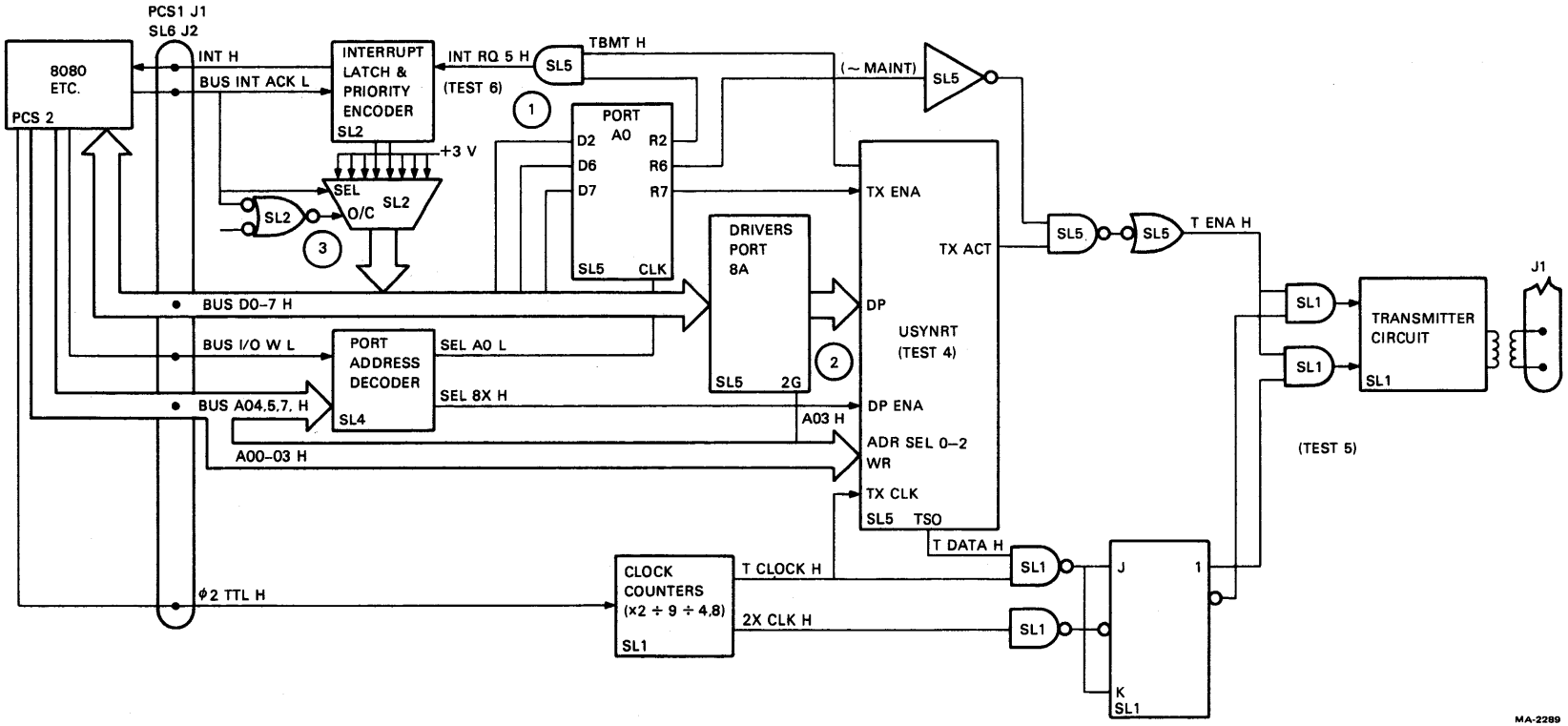


Figure 4-12 Serial Line Out

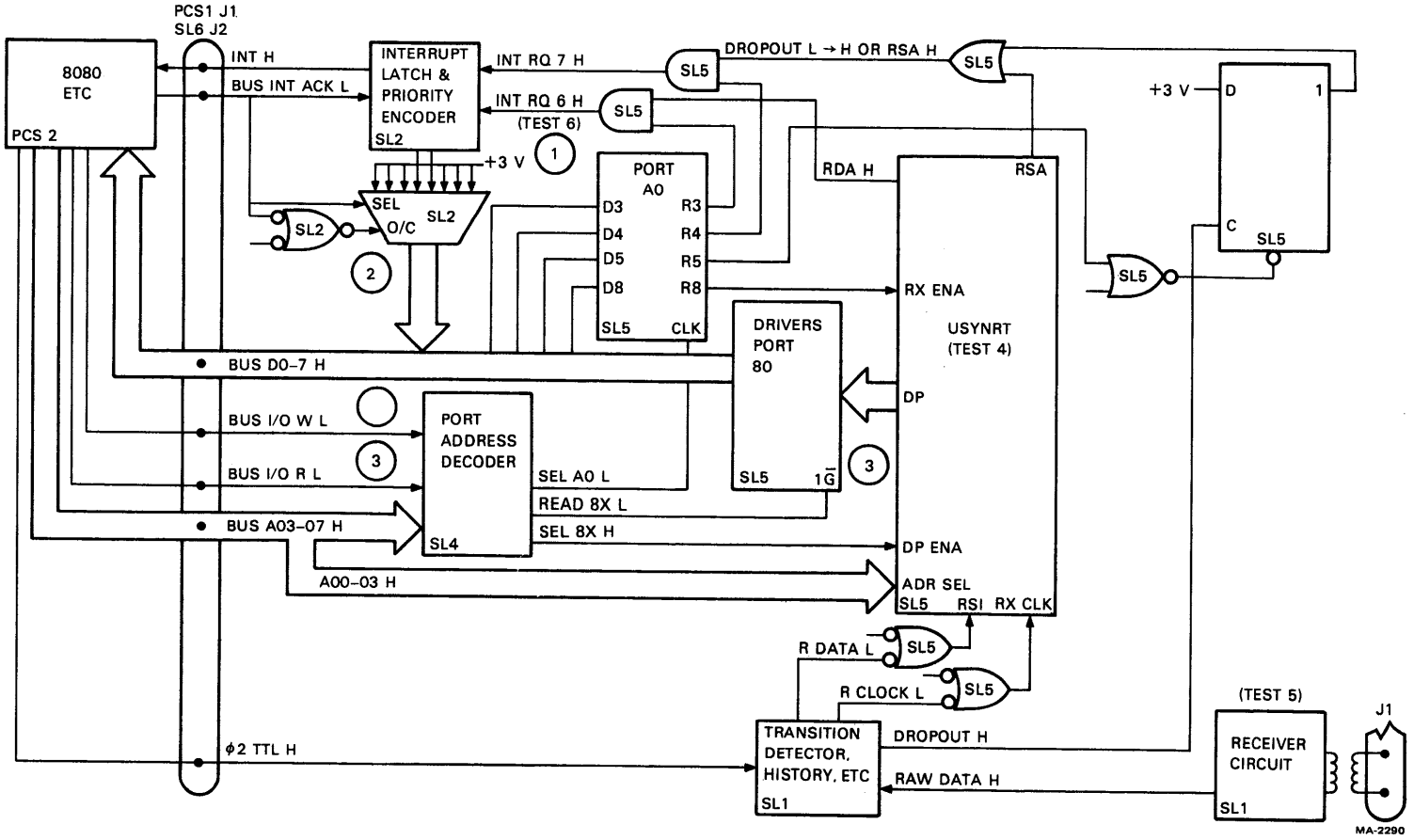


Figure 4-13 Serial Line In

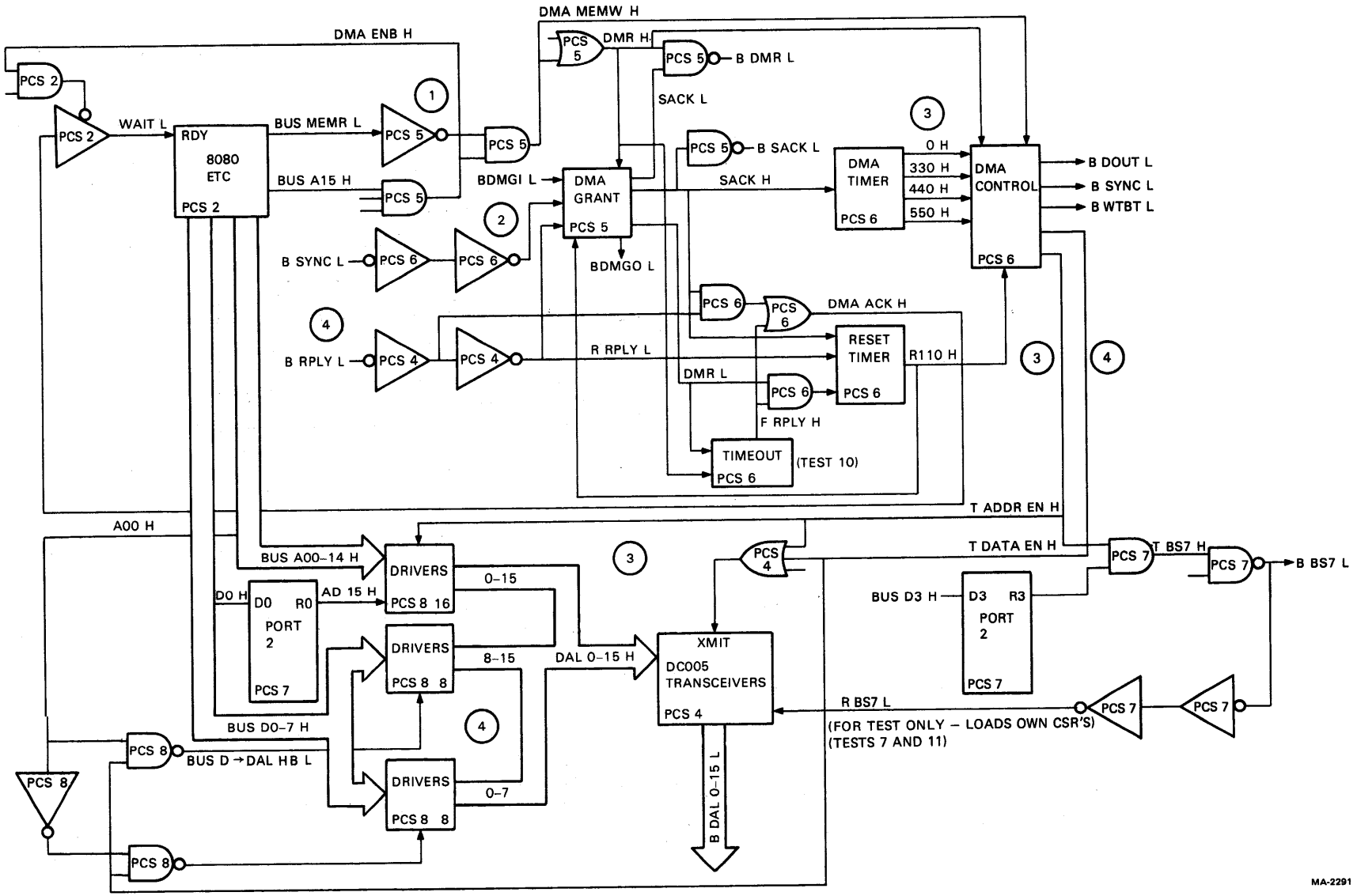


Figure 4-14 DMA Transfer Out

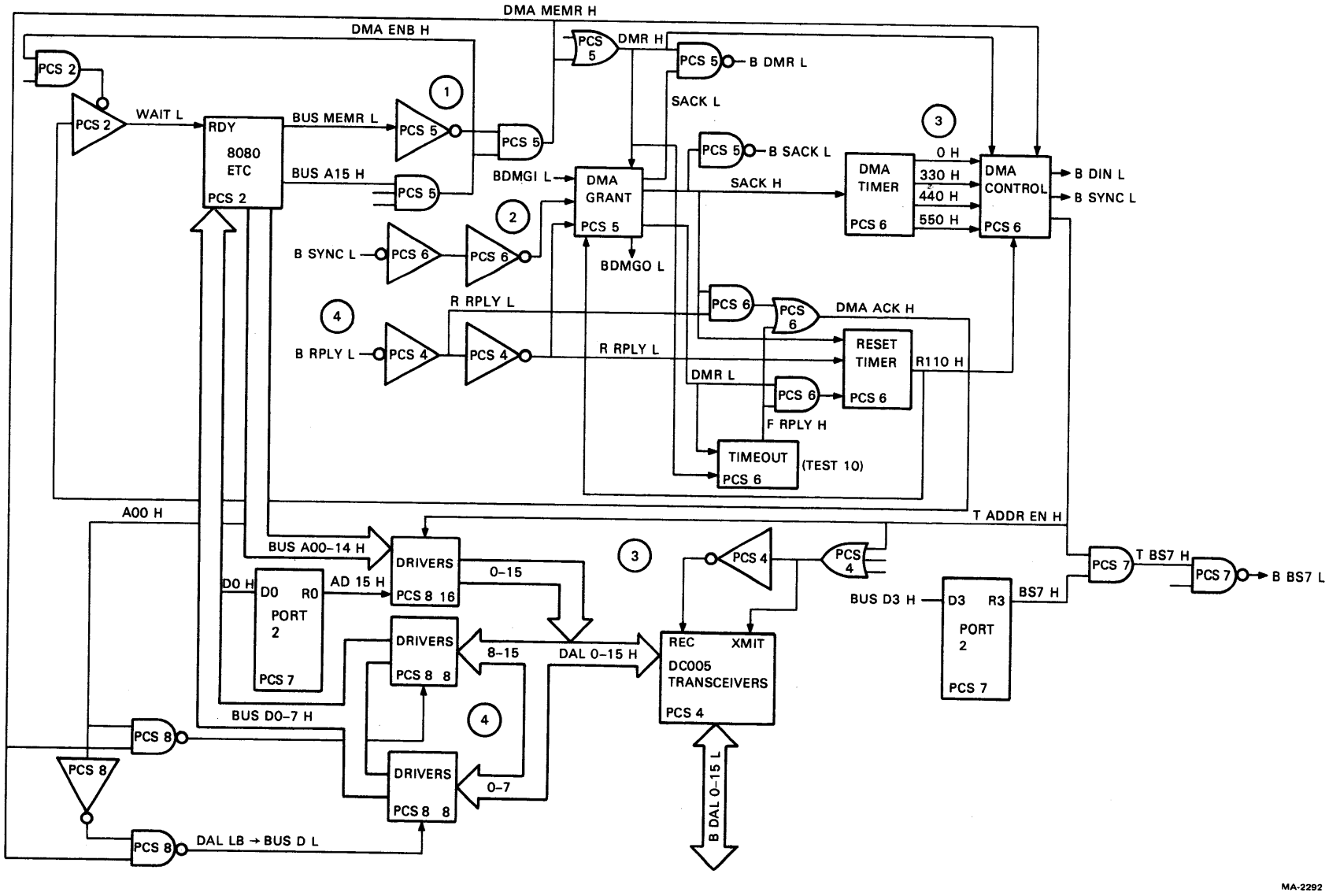


Figure 4-15 DMA Transfer In

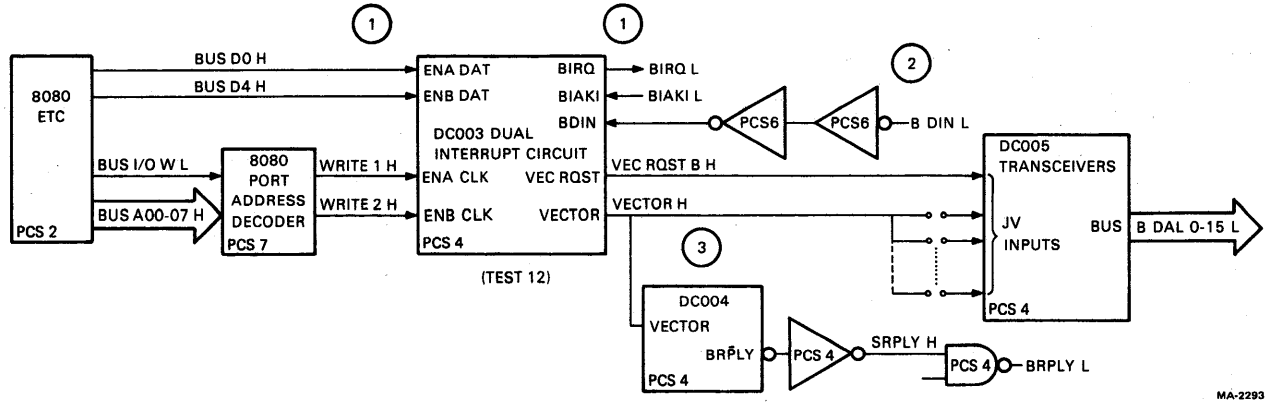


Figure 4-16 ISV11-B Interrupt Request to LSI-11

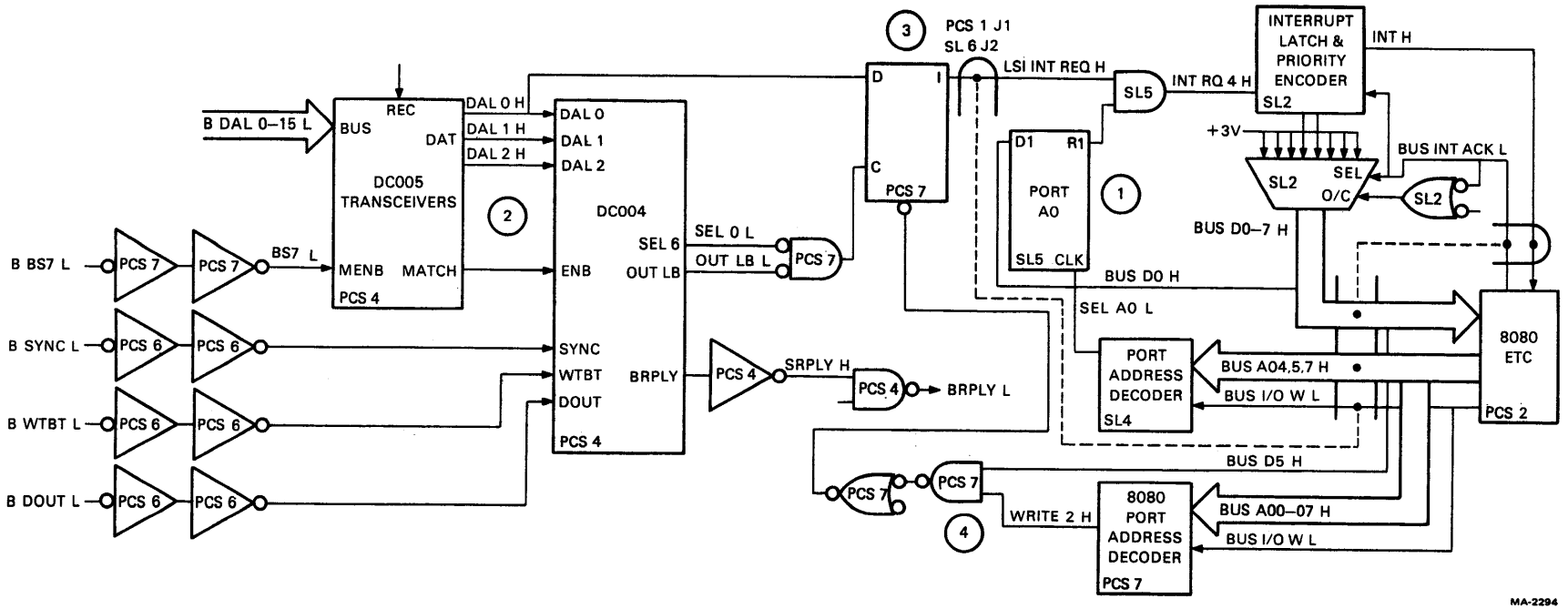


Figure 4-17 LSI Interrupt Request

4.11 SPECIFICATIONS

The ISV11-B places one dc unit load and four ac unit loads on the LSI-11 bus, and has the following dc current requirements.

+5 V	3.Ø A maximum
+12 V	Ø.37 A maximum
LSI-11 Interface	
CSRs	16Ø14Ø, 16Ø142, 16Ø144
Interrupts	3ØØ, 3Ø4
DECdataway Interface (modem)	
Port addresses	Two consecutive, lower wired into connector
Operating mode	Half-duplex
Data format	Synchronous, serial, LSB first (DSBC)
Character size	8 bits plus Ø to 2 stuffing bits
Data rate	55,556 bits per second
Transmission technique	Biphase modulation
Transmitter timing	Crystal clock
Receiver timing	From received signal
Line interface	Transformer coupled
Transmitted signal	5 V peak-to-peak into terminated 2ØØ ohm cable
Receivable signal threshold	15Ø mV peak-to-peak minimum
Error-free signal level	3ØØ mV peak-to-peak minimum
Common mode isolation	35Ø Vac rms, 5ØØ Vdc
Receiver bandpass	6 KHz to 13Ø KHz (-3 dB points)

4.12 ISV11-B Signal Glossary

This glossary lists all signals that appear on the circuit schematics for the M8080 and M8084 modules, as well as the print on which each appears. Some bus signals are generated on several prints. Many LSI-11 bus signals originate outside the ISV11-B as well as inside. A print designation in parentheses indicates a signal that appears on that print as an input but is never generated by the ISV11-B.

Signal	Print	Definition
ø1,2, CLOCK H	PCS2	2 MHz clocks generated by the 8224 for the 8080.
ø2 TTL H	PCS2	2 MHz clocks generated by the 8224 for the USYNRT.
1X CLK H	SL1	Equals T CLOCK H.
2X CLK H	SL1	For biphase encoding, this clock has twice the frequency of T CLOCK.
8X CLK H,L	SL1	Intermediate signal in transmitter clock (eight times dataway bit rate).
ø H 330 H 440 H 550 H	PCS6	Timing signals for DMA.
AD 15-17 H	PCS7	High-order address bits for DMA.
BAD 16,17 L	PCS7	Expansion address bits for LSI-11 bus.
B BS7 L	PCS7	Bank select 7 -- LSI-11 bus signal to select I/O page in LSI-11 address space.
B DAL ø-15 L	PCS4	LSI-11 bus data and address lines.
B DCOK H	PCS7	LSI-11 bus dc power okay.
B DIN L	PCS6	LSI-11 bus - master requesting input, or LSI-11 getting vector address in response to interrupt.
BDMGI L	(PCS5)	LSI-11 bus DMA grant in.
BDMGO L	PCS5	LSI-11 bus DMA grant out.

Signal	Print	Definition
B DMR L	PCS5	LSI-11 bus DMA request.
B DOUT L	PCS6	LSI-11 bus -- master has data available for output.
B HALT L	PCS7	LSI-11 bus -- halt processor.
BIAKI L	(PCS4)	LSI-11 bus interrupt acknowledge in.
BIAKO L	PCS4	LSI-11 bus interrupt acknowledge out.
B INIT L	(PCS4)	LSI-11 bus -- in ISV11-B initializes only interrupt control.
BIRQ L	PCS4	LSI-11 bus interrupt request (to LSI-11).
BOOT LSI H	PCS7	Boots LSI-11 by simulating power up (through control of B DCOK).
BPOK H	(PCS5)	LSI-11 bus ac power okay.
BRPLY L	PCS4	LSI-11 bus reply.
BS7 H	PCS7	Bank select 7 for I/O page -- conditions TBS7 when address placed on LSI-11 bus.
B SACK L	PCS5	LSI-11 bus -- acknowledges that ISV11-B has been granted master status in DMA operation.
B SYNC L	PCS6	LSI-11 bus -- master has placed address on bus.
BUS AØØ L	PCS7	From BUS AØØ H.
BUS AØØ-15 H	PCS2	8Ø8Ø bus address lines.
BUS DØ-7 H	PCS2,3,7 SL2,4	8Ø8Ø bus data lines.
BUS D^2 DAL HB L	PCS8	8Ø8Ø data to LSI-11 bus high byte.
BUS INT ACK L	PCS2	8Ø8Ø interrupt acknowledge.
BUS I/O R L	PCS2	8Ø8Ø reading an I/O register (port).

Signal	Print	Definition
BUS I/O W L	PCS2	8080 writing an I/O register (port).
BUS OUT EN L	SL2	8080 reading local memory or receiving interrupt RST.
BUS MEMR L	PCS2	8080 reading memory or I/O register addressed as memory.
BUS MEMW L	PCS2	8080 writing memory or I/O register addressed as memory.
B WTBT L	PCS6	LSI-11 bus write/byte.
CARRIED LED	SL1	Controls carrier-detected LED.
CPU SYNCH H	PCS2	8080 signal to 8224 to indicate first state in each machine cycle.
DAL 0-15 H	PCS4, 7	Data and address lines on LSI-11 bus extension.
DAL LB^2 BUS D L	PCS8	LSI-11 bus data low byte to 8080.
DIN L	PCS6	Received B WTBT.
DIS 8X CLK L	SL6	GR test disable for 8X CLK.
DIS I/O L	SL6	GR test disable for 8080 I/O address decoder.
DIS MEM L	SL6	GR test disable local memory.
DIS RAW DATA L	SL6	GR test disable receiver.
DMA ACK H	PCS6	DMA request has been acknowledged by LSI-11 bus.
DMA MEMR H	PCS5	8080 reading in LSI-11 address space.
DMA MEMW H	PCS5	8080 writing in LSI-11 address space.
DMR H,L	PCS5	DMA request -- generates B DMR for 8080 to access LSI-11 address space.
DOUT L	PCS6	Received B DOUT.
DROPOUT H,L	SL1	Dataway signal absent.

Signal	Print	Definition
DROPOUT L^2 H OR RSA H	SL5	Dataway signal dropped out (1.5 bit times without transition) or USYNRT receiver status available.
ENA DMA H	PCS5	8080 addressing LSI-11 space.
EXT 8X CLK L	SL6	8X CLK at test socket; or can be used for external clock if DIS 8X CLK.
EXT RAW DATA H	SL6	RAW DATA at test socket; or can be used for external data if DIS RAW DATA.
EXT R CLOCK L	SL6	External test receiver clock for USYNRT.
EXT R DATA L	SL6	External test received data for USYNRT.
FRPLY H,L	DCS6	Forced bus reply.
HALT LSI H	PCS7	Generates B HALT.
INT H	SL2	Interrupt to 8080.
INT Q BUS A H	PCS4	LSI-11 bus interrupt control waiting for interrupt on A level, or has vector 300 on B DAL lines.
INT RQ 4-7 H	SL5	Interrupt requests to 8080.
INWD L	PCS4	From B DIN sent by LSI-11 for CSR.
I/O PAGE L	PCS2	8080 addressing I/O register as memory location.
I/O R L	PCS2	8080 IN instruction (I/O read).
I/O W L	PCS2	8080 OUT instruction (I/O write).
I/O WR H	PCS7	Equals I/O R "OR" I/O W.
JA	PCS4	Jumper address inputs to DC005s.
JAV	PCS4	Jumper vector address inputs to DC005s.
LITE 1-4 L	PCS7	Control M8080 LEDs.

Signal	Print	Definition
LSI INT REQ H	PCS7	Equals CSR Ø bit Ø; this is an LSI-11 request for an 8Ø8Ø interrupt.
MARGIN -5 V	SL6	GR test margin for -5 V for PROMs.
MATCH	PCS4	Address on B DAL equals jumper address (JA) on DCØØ5s (LSI-11 addressing ISV11-B CSRs).
MEM BUS DØ-7 H	SL2,3	Data bus for output from local memory.
MEMR H	PCS5	Equals BUS MEMR.
MEMW H	PCS5	Equals BUS MEMW.
MEM SEL L	SL2	8Ø8Ø accessing local memory.
MENB	PCS4	Enables match with JA in DCØØ5s.
OUT HB H	PCS3	From OUT HB 1.
OUT HB L	PCS4	LSI-11 loading CSR high byte.
OUT LB H	PCS3	From OUT LB L.
OUT LB L	PCS4	LSI-11 loading CSR low byte.
PHASE-LOCKED CLK H	SL1	A clock (train) geared to last signal transition detected on dataway.
PORT ADDR 1-6 H	(SL4)	Port address wired into dataway connector.
R11Ø H	PCS6	Reset time for DMA.
RAM SEL L	SL3	8Ø8Ø accessing the RAM.
RAW DATA L	SL1	Output of modem receiver circuit.
R BS7 L	PCS7	Received B BS7.
R CLOCK H,L	SL1	Receiver clock derived from incoming bit stream.
RDA H	SL5	USYNRT output -- received data available.

Signal	Print	Definition
R DATA H,L	SL1	Modem received data output to USYNRT.
R DCOK L	PCS7	Received B DCOK.
READ 8X L	SL4	8080 reading I/O register in address range 80--87.
READ CSR L	PCS7	LSI-11 reading CSR 0.
READY H	PCS2	Pulled down by the 8224 on a wait to idle the 8080.
REC H	PCS4	ISV11-B is not now sending information on LSI-11 bus B DAL lines.
RESET 1 H	PCS2	Generated by 8224 when BPOK H goes down.
RESET H,L	PCS2	Equals RESET 1.
RESET H,L	SL6	M8084 reset from PCS2 RESET L.
R HALT H	PCS7	Received B HALT.
RPOK L	PCS5	Received BPOK.
RRPLY H,L	PCS4	Received BRPLY.
RSA H	SL5	USYNRT output -- receiver status available.
RX ACT H	SL5	USYNRT receiver active.
SACK H	PCS5	Send B SACK for DMA.
SEL 0,2,4 L	PCS4	CSR address decoder outputs.
SEL 8X H	SL4	8080 accessing I/O register in address range 80--87.
SEL 90 L	SL4	8080 reading I/O register 90 (USYNRT status).
SEL A0 L	SL4	8080 writing I/O register A0 (USYNRT control).
SEL B0 L	SL4	8080 reading I/O register B0 (port address).

Signal	Print	Definition
SELECT 1-5 L	PCS7	Address decoder outputs for 8080 I/O registers in LSI-11 bus interface.
SRPLY H	PCS4	Send BRPLY.
STROBE	PCS2	Send 8224 to 8228 in response to CPU SYNC; latches 8080 cycle status in 8228.
SYNC L	PCS6	Received B SYNC.
T ADDR EN H,L	PCS6	Transmit address on B DAL for DMA.
TBMT H	SL5	USYNRT transmit buffer empty.
TBS7 H	PCS7	Transmit B BS7.
T CLOCK H	SL1	Transmitter clock -- 55,556 KHz.
T DATA H	SL5	USYNRT serial data output.
T DATA EN H,L	PCS6	Transmit data on B DAL for DMA.
T DIN H	PCS6	Transmit B DIN for DMA.
T DOUT H	PCS6	Transmit B DOUT for DMA.
T ENA H,L	SL5	Enable modem transmitter (when USYNRT transmitter active but not in maintenance mode).
TEST DISABLE 8080 L	PCS6	GR test disable 8080 operation.
TEST DISABLE I/O L	PCS6	GR test disable 8080 I/O register addressing.
TME H	PCS7	Time-out enable for DMA.
TMO H	PCS7	DMA time-out.
TMO ERR H	PCS7	Time-out error status bit (8080 to LSI-11).
TRANSITION DETECTED H	SL1	Receiver detected a zero-crossing.
TRANSITION DLYD L	SL1	Transition detected inverted and delayed 500 ns.

Signal	Print	Definition
T RAW DATA H	SL1	Flip-flop biphase-encoded data signal applied to transmitter circuit.
T SYNC H	PCS6	Transmit B SYNC for DMA.
T WTBT H	PCS6	Transmit B WTBT for DMA.
TX ACT H	SL5	USYNRT transmitter active.
VEC RQST B H	PCS4	Makes vector jumper address 304 when VECTOR is true.
VECTOR H	PCS4	Places vector jumper address (JAV) on B DAL when the 8080 interrupts the LSI-11.
WAIT L	PCS2	Puts 8080 in wait state until DMA acknowledged.
WRITE 1,2 H	PCS7	Select 8080 I/O registers 1 and 2 for writing.
WTBT L	PCS6	Received B WTBT.

5.1 INTRODUCTION

The BA11-Y power system has four major assemblies.

1. Power supply (H7861)
2. Backplane (H9276)
3. Module cage
4. AC input panel (front panel)

These are identified in Figure 5-1, which shows the BA11-Y with its cover removed. In addition to the major assemblies, the figure shows the locations of several subassemblies that are of interest to anyone servicing the unit. These are:

1. Module-assembly and power-supply fans.
2. AC and dc harnesses.
3. Bezel PC board assembly.
4. Power supply control and power-monitor boards.

Figure 5-2 links these components functionally.

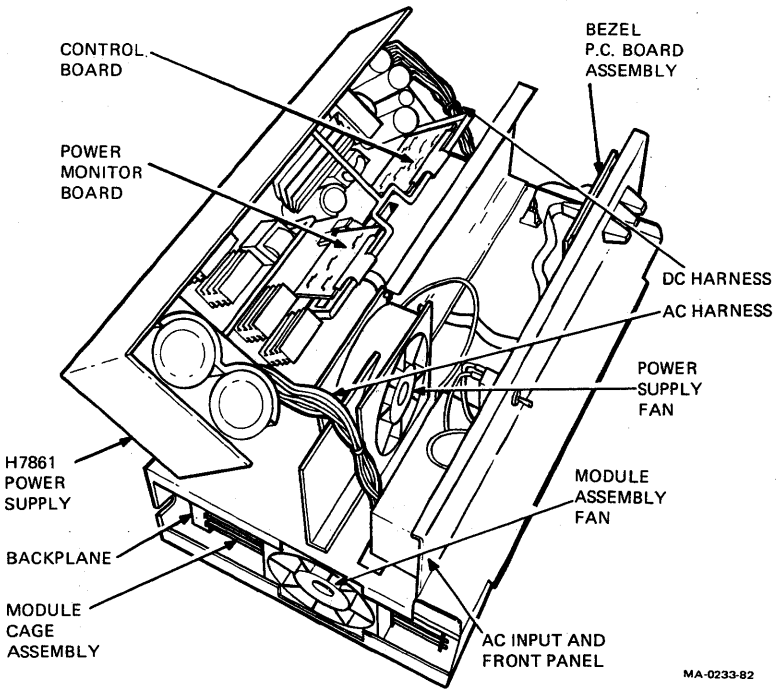


Figure 5-1 BA11-Y Major Assemblies

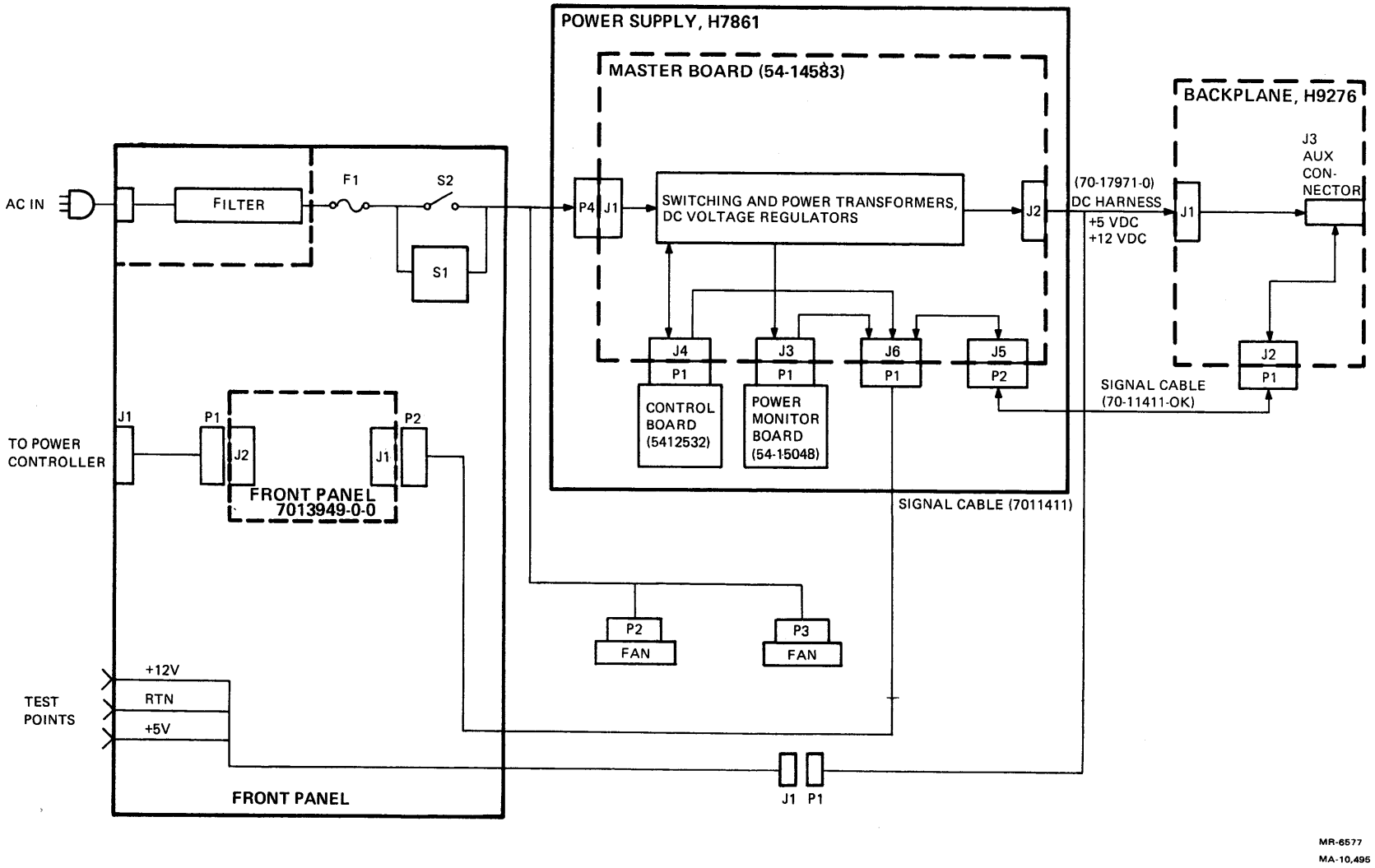


Figure 5-2 BA11-Y Functional Block Diagram

5.1.1 AC Input Panel

The ac input panel is also the front panel. Power is provided to the panel from the ac mains by either a 120 V line cord or a 240 V line cord.

The panel includes an ac input connector, a line filter, a fuse, an ON/OFF switch, and a switch that makes the correct connections to the fans and the power supply for both 120 Vac and 240 Vac line voltages.

The output of the panel is taken to the fans and the power supply by an ac power harness. Connector P1 of the harness is a Mate-N-Lok connector (9-pin), while P2 and P3 are molded ac plugs that break out of the harness to plug into terminals on the fans.

5.1.2 H7861 Power Supply

The H7861 power supply occupies the upper, rear quarter of the DYS50 space. It is attached to the logic cover assembly with two releasable hinges. It is fastened to the power supply bracket with two screws. When the two screws are removed, the supply can be tipped back to allow service access. The entire power supply can be removed easily by removing the two screws, unlatching the two hinges, and disconnecting four cables.

Three printed circuit boards contain all the power supply components. The control board and the power monitor board are inserted in connectors that are mounted on the master board. The regulated dc voltages generated on the master board are sent to the H9276 backplane by a dc harness that connects on both ends to screw terminals. The signals generated on the control board are applied to the backplane and to the front panel by two different signal cable assemblies.

5.1.3 H9276 Backplane

The H9276 is a 9 X 4 backplane, i.e., nine slots of four rows each; both double and quad modules can be inserted. Rows A and B of each slot supply the extended LSI-11 bus signals; these signals are bused to each of the nine slots.

The pins of the C and D rows are not bused; however, the pins of adjacent slots are connected. This not only precludes the necessity of top connectors, but also provides the means for designing buses whose lengths are determined by the number of modules in a set. The C and D rows of the backplane are referred to collectively as the CD bus.

5.1.4 Front Bezel Assembly

The front panel can be blank or it can be equipped with switches and indicators. The switches allow an operator to turn the power on and off (only when connected to a power controller), to reboot the CPU, and to suspend the CPU's usual program execution. The indicators, when lit, tell the operator that the power supply voltages are enough for operation and the CPU is running. The front panel is connected to the power supply master board by a signal cable and, if appropriate, to a power controller by a twisted-pair cable that can be provided.

5.2 DETAILED DESCRIPTION

A detailed description of each component of the power system follows. Figure 5-3 is a unit assembly drawing that shows details of the power system interconnections.

5.2.1 AC Input Panel

Figure 5-4 is a schematic of the ac input panel. The fans and part of the power supply master board are shown to present the primary power connections. T4 of the master board is the +12 V start-up transformer; D1, C2, and C1 convert the ac voltage to nonregulated dc voltage, as described in Paragraph 5.2.2.1.

The line cord that supplies primary power is inserted in the male connector, FL1. The line voltage is controlled by SW2, which is used as an ON/OFF switch when a power controller is not used. When SW2 is closed, the line voltage is applied through F1 and the line filter to the voltage selection switch, SW1. This switch is mounted below SW2 on the front panel and is in the correct position when the printing over the switch lever agrees with the line voltage being used. SW1 allows the system to run on 120 Vac or 240 Vac by connecting the line to the power supply input and the two fans. For example, the fans are provided with 120 Vac, even when the line voltage is 240 Vac.

5.2.2 H7861 Power Supply

Figure 5-5 is a block diagram of the H7861 power supply. All of the power supply components are mounted on three printed circuit boards -- a master board, a control board, and a power monitor board.

The master board consists of an ac input circuit, the +5 V and +12 V regulators, and a +12 V start-up supply. The ac input includes a thermostat that protects the supply from too much heat. The thermostat switch opens, disconnecting the ac input, when the ambient temperature reaches 85° C (185° F); the switch closes automatically when the temperature returns to 64.4° C (148° F). The ac input circuit converts the 120 Vac or 240 Vac input to raw dc voltage. This dc voltage is applied to a power converter circuit that is switched on and off to produce rectangular-wave voltages that are applied to the regulator circuits. The rectangular-wave input to each switching regulator has a duty cycle that differs with the level of the unregulated input voltage. If, for example, the input voltage decreases, the 5 V control circuit on the control board causes the power converter circuit to increase the duty cycle of the rectangular wave. Therefore, the output voltage is maintained at its correct level. The 12 V circuit has a switching transistor in series with the inverter circuit output. This switch corrects the converter output pulse to maintain a duty cycle that will average 12 V.

Each regulator circuit is a switching regulator with an averaging filter and includes overvoltage and overcurrent circuits that protect the supply against overload conditions. The regulated outputs are monitored by the control board. The outputs are also applied to the H9276 backplane.

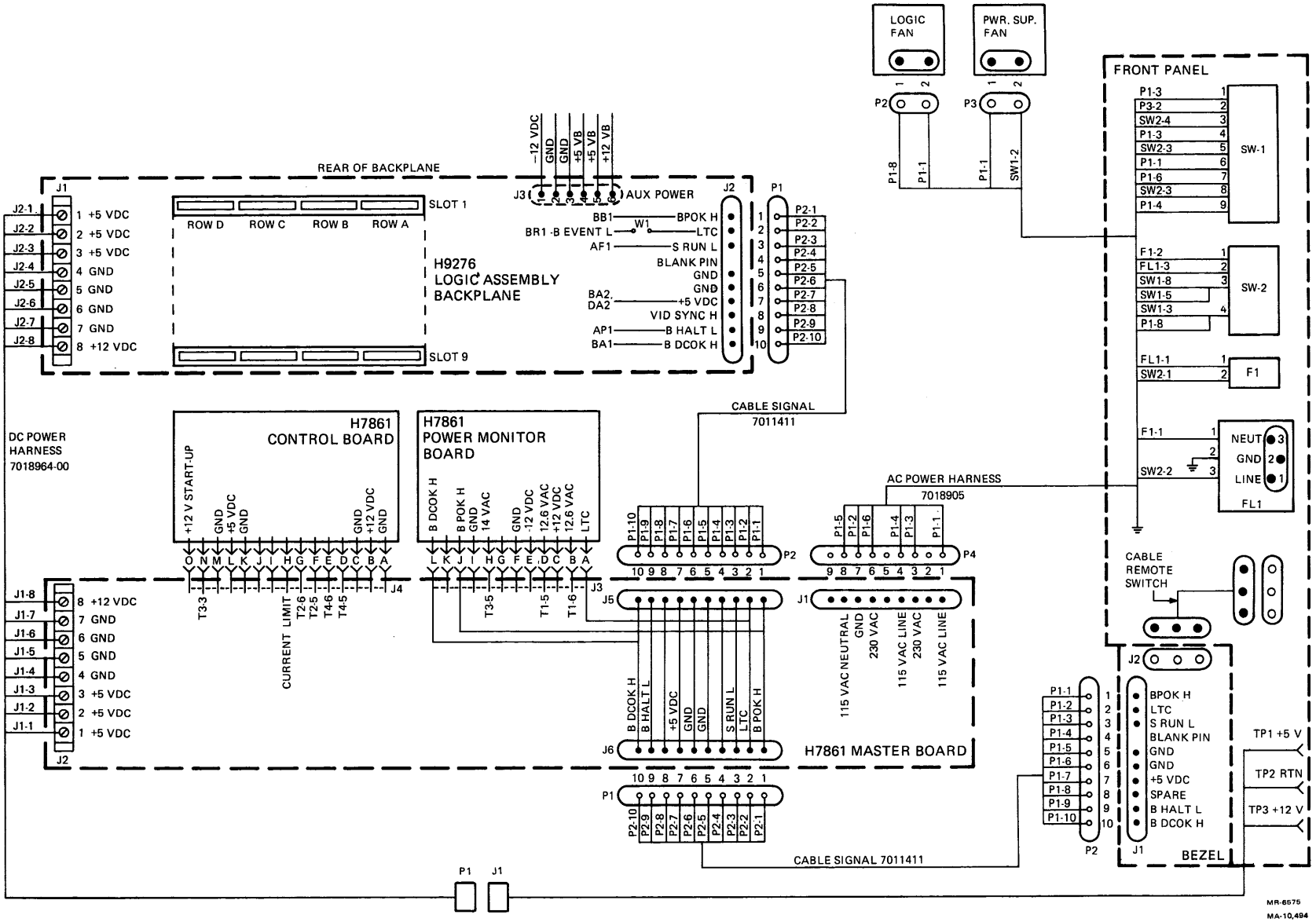


Figure 5-3 BA11-Y Interconnections

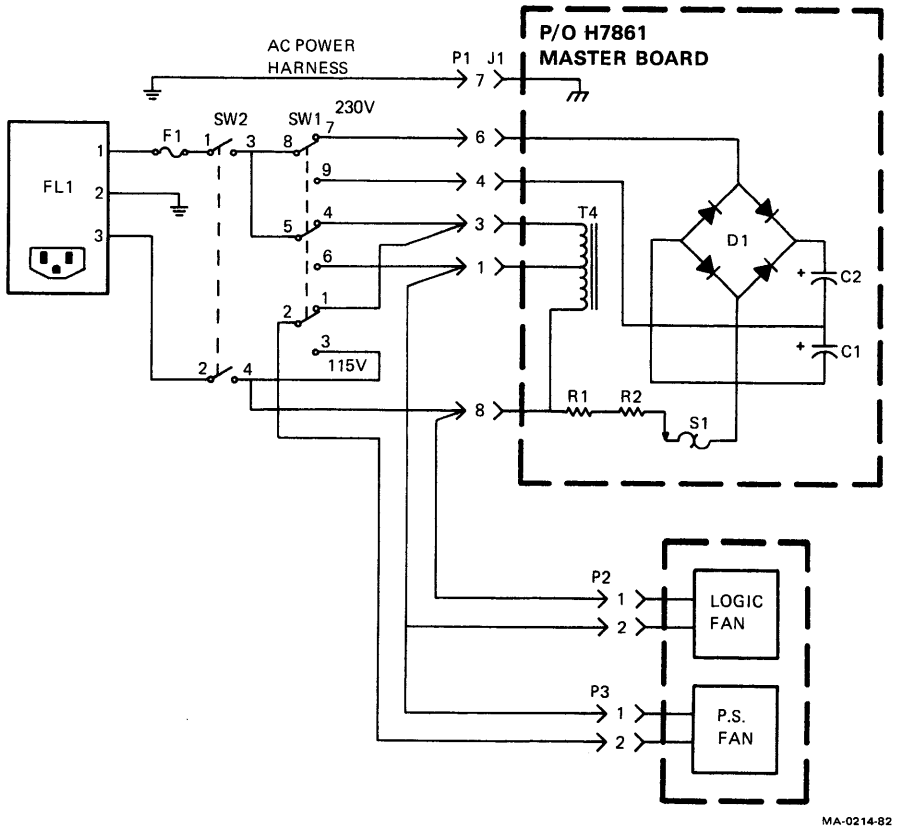


Figure 5-4 AC Input Schematic

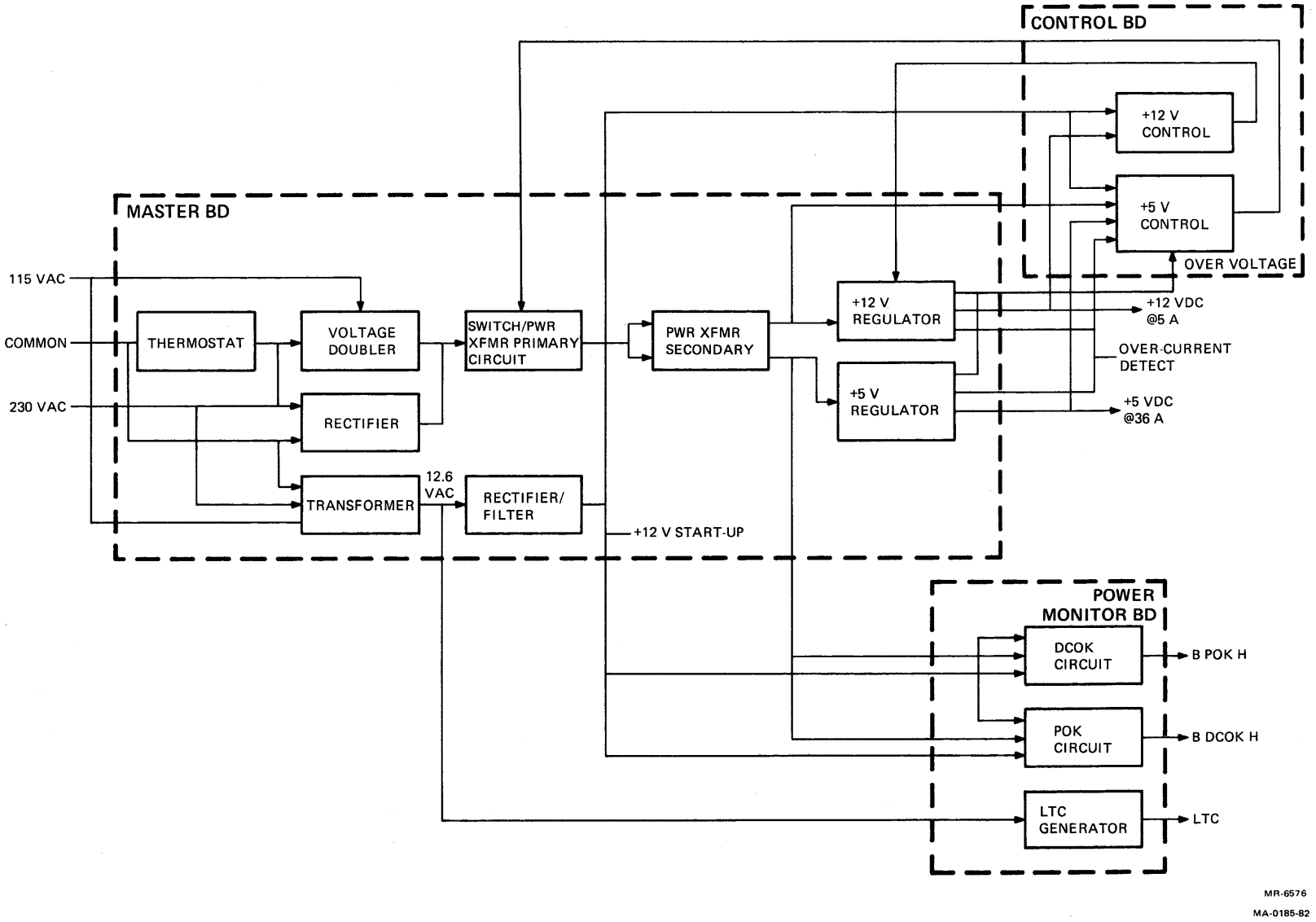


Figure 5-5 H7861 Block Diagram

The +12 V start-up supply produces a dc voltage that is necessary during start-up operations. When steady conditions are attained, the +12 V regulated output takes over for the start-up voltage. If the +12 V regulated output should be lost during operation, the start-up voltage is available to keep the control board and power monitor board circuits operating.

The control board circuits monitor the regulated output voltages, comparing them to control board-generated reference voltages, and feed them back to the main converter. When either regulated voltage varies from its prescribed value, the appropriate control circuit varies the duty cycle of the rectangular-wave as needed. This forces the output to return to the correct value. Adjustment potentiometers are provided in each control circuit, enabling the output voltages to be adjusted to account for initial tolerances of circuit components.

The power monitor board generates two signals -- BPOK H and BDCOK H -- that enable the CPU to carry out specific power-up and power-down operations. The signals are asserted in a set sequence both when the power is turned on and when the power is turned off or lost because of failure (the sequence is described in Paragraph 5.2.2.5). Also included on the board is a clock generator that produces a line-time clock (LTC) signal. This signal is applied at the CPU, where it generates vectored interrupts at the line frequency.

5.2.2.1 AC Input Circuit -- Figure 5-6 shows the ac input circuit of the power supply. The ac input voltage is converted to dc voltage by bridge rectifier D1 and capacitors C1 and C2. When the input is 240 Vac, D1 corrects the ac voltage, and C1 and C2 smooth the ripple that appears on the dc output of the rectifier. However, when the input is 120 Vac, D1, C1, and C2 become a voltage doubler. Therefore, the dc voltage produced is approximately the same for both line voltages and can change between 200 and 375 Vdc.

This dc voltage is applied to a switching circuit that includes transistors Q1 and Q2 and transformer T1. Q1 and Q2 are switched on and off at 30 kHz. The duty ratio is determined by the +5 V control circuit on the control board. When the transistors are on, the corrected dc voltage appears across the primary of transformer T2 (pins 1-2) and is combined with each secondary of T2. The dots on the windings of T2 (Figure 5-6) represent the more positive side of each winding at this time. When the transistors are switched off, the voltage across the primary of T2 reverses its polarity instantaneously. The same polarity reversal occurs in the secondaries of T2; then, an alternating wave is generated at the secondaries of T2. Each regulator uses the positive half cycle of the secondary voltage to produce a positive dc voltage. The +5 V regulator winding also uses the negative half-cycle of the secondary voltage to produce a nonregulated, negative dc voltage (-12 Vdc), which is used to bias ICs on the power monitor board.

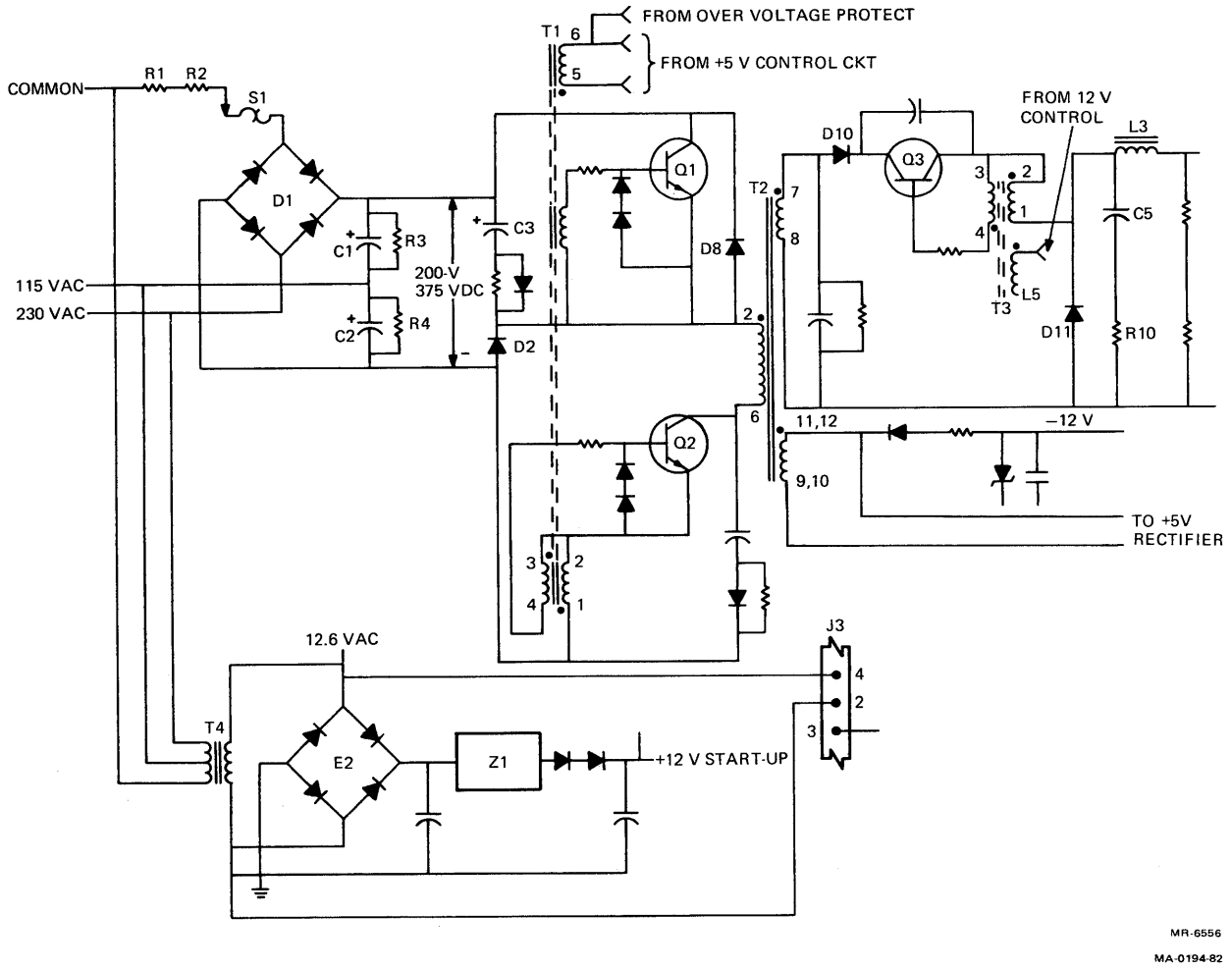


Figure 5-6 Inverter Circuit

The rest of this section expands the preceding short description by focusing on the current and voltage relationship in transformer T2. Figure 5-7 links the current and voltage waveforms in the primary and secondary windings of T2. At time A, transistors Q1 and Q2 are off. During this time, a steady current is moving through the secondary winding of transformer T1 from pin 5 to pin 6 (Figure 5-6). At time B, the +5 V control circuit causes the current in winding 5-6 to stops moving. A voltage that opposes the decrease in current (i.e., a counter-EMF) is produced across winding 5-6; thus, pin 5 becomes negative with respect to pin 6. Voltages having the same polarity are induced in the other secondaries and the primary of T1. These voltages forward-bias the emitter-base junction of both Q1 and Q2, turning on the transistors. Collector current starts to flow from Q1 through the primary of T2 from pin 2 to pin 6, through Q2, and through secondary winding 2-1 of T1. Then, the corrected dc voltage appears across the primary of T2, pin 2 being the more positive side of the winding.

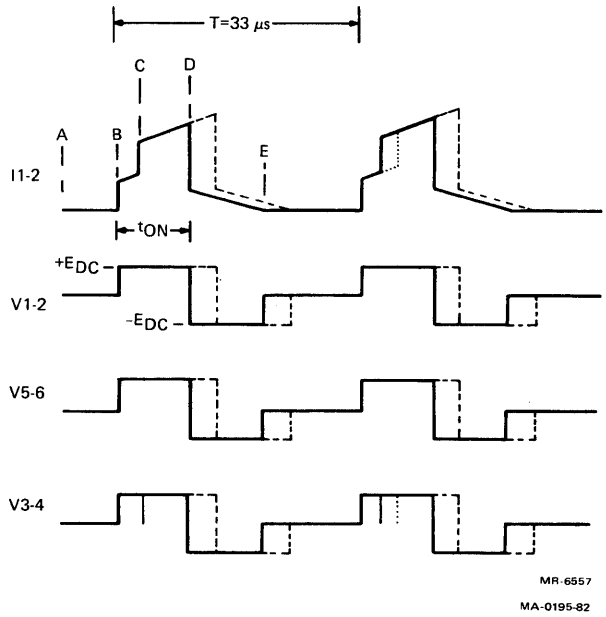


Figure 5-7 Current/Voltage Relationship in T3

The current moving in the primary of T2 is determined by the load on each secondary winding. At time B, a steady current is moving in the primary of transformer T3 from pin 6 to pin 5, and transistor Q3, which is part of the +12 V regulator circuit, is not conducting. Then, there is no load on secondary winding 7-8 of T2, and the primary current of T2 is a function of only the +5 V regulator. At time C, the +12 V control circuit causes the current in winding 5-6 of T3 to stop moving. The counter-EMF generated across the primary winding is coupled to both secondaries of T3, and the polarity of the induced voltage forward-biases the emitter-base junction of Q3. The +12 V regulator starts to operate and the current drawn from the secondary of T2 is echoed back to the primary of that transformer. Then, the total current in the primary of T2 quickly grows, as shown by the current waveform in Figure 5-7.

After the sudden increase at time C, the primary current begins a more gradual, linear increase, resulting from a constant voltage across the primary winding. At time D, the +5 V control circuit causes a steady current to start moving once more in winding 5-6 of transformer T1. The bias voltage is removed from Q1 and Q2, turning them off. As the current through the primary of T2 starts to decrease, the primary voltage reverses polarity to oppose the changing current. Now pin 6 becomes the more positive side of winding 2-6. The charging path is from pin 6, through diode D8 capacitors C2 and C1, and diode D2 back to pin 2 of the winding. The $-E_{DC}$ voltage is clamped across the primary winding; then the primary current decays linearly toward zero. When this value is attained, the primary voltage drops to zero, and the cycle is repeated.

As Figure 5-7 indicates, the frequency of the voltage waveforms is constant. This frequency is determined by circuit components in the +5 V control circuit. However, the duty cycle of the voltage pulses can change to show the condition of the controlled dc voltages. (The duty cycle is defined as the ratio t_{ON}/T and has a maximum value of 50 percent.) For example, if the load on the +5 V output increases, the +5 V control circuit causes switching transistors Q1 and Q2 to stay on for a longer period of time to make up for increased voltage drops due to circuit resistance. That is, point D and point E in Figure 5-7 move to the right, as indicated by the dashed lines. Then, the average value of the input to the +5 V regulator increases; this increase forces the output back to its original value.

The increased duty cycle forces up the +12 Vdc controlled output, as well. Because this output was at the proper value (we assume), any increase is false. Therefore, the +12 V control circuit causes Q3 to switch on later to lower the average value of the input to the +12 V regulator. The result of this on the waveforms in Figure 5-7 is shown as a dotted line.

5.2.2.2 +5 V Control Circuit -- Figure 5-8 shows the +5 V control circuit. The circuit monitors the +5 Vdc controlled output and, by turning Q2 on and off, controls the flow of current in winding 5-6 of transformer T1.

To monitor the controlled voltage, the circuit includes a 3524 integrated circuit (IC) -- a controlled pulse-width modulator. Figure 5-9 shows a block diagram of this IC. When the 3524 is used in the +5 V control circuit, the +5 Vdc controlled output is applied to one input of the error amplifier. The other input of the error amplifier is connected to an internally generated +5 V reference (pin 16). The error signal developed at pin 9 is applied to a comparator together with an internally generated sawtooth waveform (the outputs from the internal oscillator are set by external components at pins 6 and 7). The comparator output is a pulse whose width depends on the level at which the error signal slices the sawtooth. This pulse is applied to NOR gates along with the internal oscillator output and both sides of the internal flip-flop. The resulting output signals at pins 12 and 13 are used in both the +5 V control circuit and the +12 V control circuit.

These output signals from the 3524 IC are related to the internal signals by the waveforms in Figure 5-10. The circuit components connected to pins 6 and 7 result in an oscillator output for a period of 16.5 us. The oscillator output pulses (the top line) clock the internal flip-flop, one output of which is shown in the second line. The third line shows the sawtooth signal being sliced by the error signal, which is represented by the horizontal solid line (the dashed line will be explained later); line 4 shows the resulting comparator output. When the signals shown on lines 1, 2, and 4 are NORed, they produce the output signals shown on lines 5 and 6.

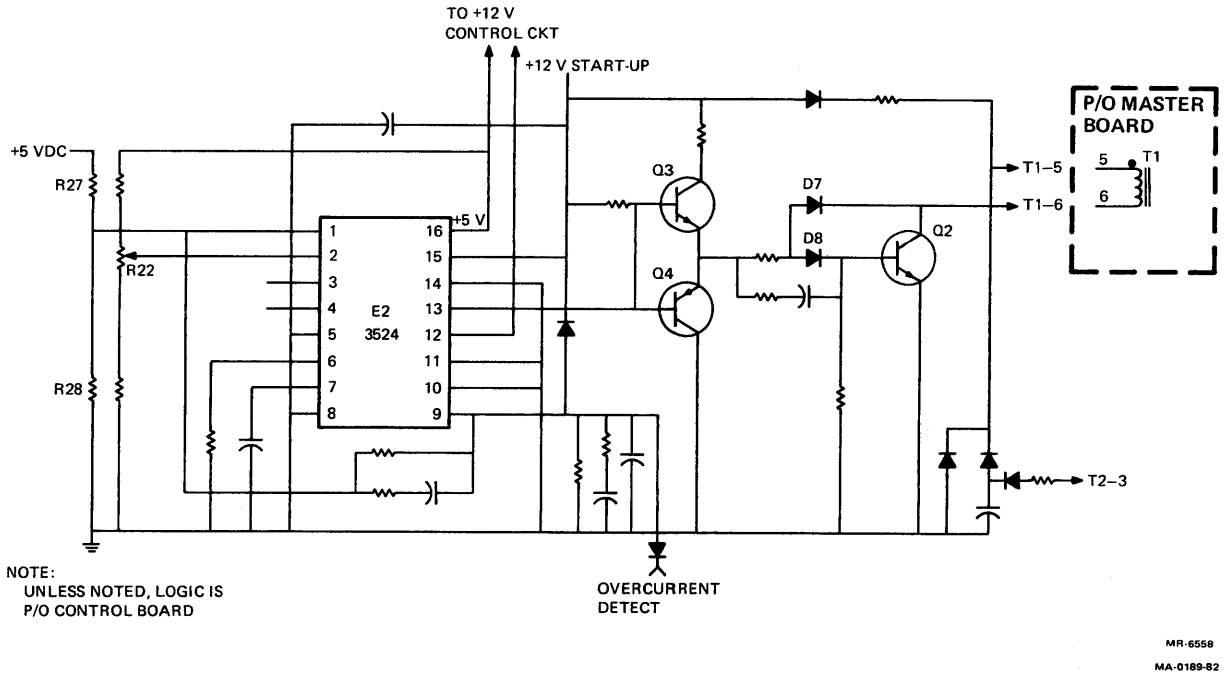


Figure 5-8 +5 V Control Circuit

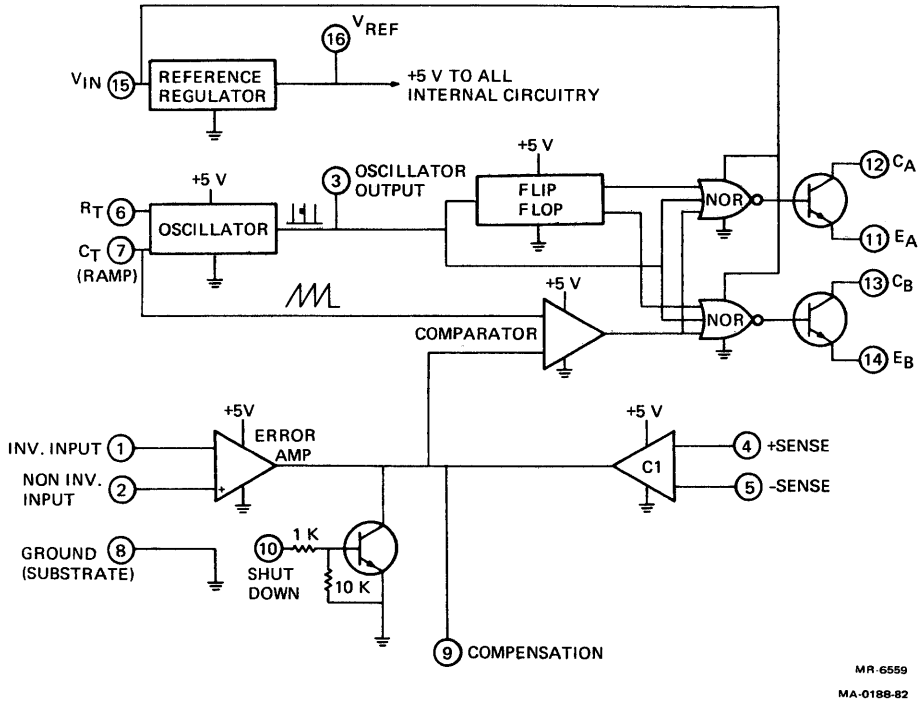


Figure 5-9 3524 IC Block Diagram

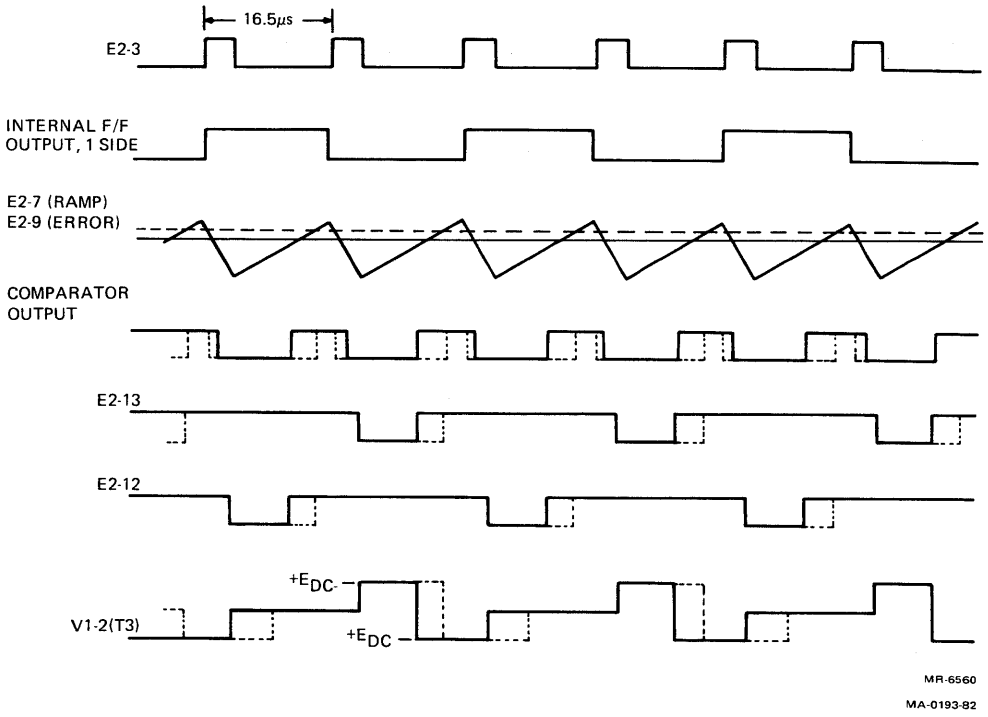


Figure 5-10 Timing, +5 V Control Circuit

The output from pin 12 of Z1 is used in the +12 V control circuit. The output from pin 13 is applied to transistor pair Q3/Q4 in the +5 V control circuit. When pin 13 goes low, Q4 is turned on and Q3 is turned off. Q2 turns off and the current that had been moving in transformer T1 begins to decrease. The counter-EMF induced in the windings of T1 forward-biases switches Q1 and Q2 in the ac input circuit. Then, Q1 and Q2 switch on and E_{DC} is applied to the primary of power transformer T2, as shown by the signal of line 7. When pin 13 of E2 goes high, Q3 is turned on and Q4 is turned off. Therefore, Q2 conducts and steady current again moves through T1. Switches Q1 and Q2 in the ac input circuit turn off, and the primary voltage of T2 reverses polarity. When the primary current of T2 has decayed to zero, the voltage returns to zero and the cycle is repeated.

The dashed lines show what occurs, for example, when the +5 Vdc controlled output tends to decrease. The error signal in the 3524 IC increases, narrowing the output of the IC's comparator. As a result, switches Q1 and Q2 in the ac input conduct for a longer period of time. The increased duty cycle of the voltages across the windings of T2 counteracts the threatened decrease of the +5 Vdc controlled output.

Both regulator circuits are equipped with overcurrent detectors. When such a condition results in either regulator, pin 9 of Z1 is taken near ground and the comparator output pulse width reaches a maximum. Then, the duty cycle of the power transformer voltages is lowered to a minimum.

5.2.2.3 +12 V Control Circuit -- The +12 V control circuit is represented in Figure 5-11. The circuit monitors the +12 Vdc controlled output and, by turning Q1 on and off, controls the movement of current in winding 5-6 of transformer T3. The control circuit includes an operational amplifier, E1, and an NE555 timer, E3.

A simple block diagram of the timer is shown in Figure 5-12 (Q5 and C13 are part of the +12 V control circuit). A trigger pulse applied to comparator B causes both the output phase to generate a gate and the internal transistor to turn off. The external capacitor, C13, starts to charge at a rate determined by the amount of current provided by Q5. When the charge voltage on C13 reaches the threshold level started by the control input (pin 5), comparator A causes both the output phase to terminate the gate and the internal transistor to turn on. C13 discharges through the internal transistor to ground, and the cycle repeats when the next trigger pulse is applied.

The dashed lines in Figure 5-13 represents what occurs, for example, when the +12 Vdc controlled output decreases. The output of the operational amplifier in the control circuit increases. Therefore, Q5 supplies a larger amount of current to C13, which charges at a more rapid rate. Transistor Q1 turns on earlier to increase the duty cycle of the secondary voltage of T2 and, thereby, to aid the slight decrease in the output voltage.

5.2.2.4 +12 V/+5 V Regulators -- The +12 V regulator is shown in Figure 5-14. The circuit includes a switching regulator, an overcurrent sensor, and an overvoltage detector. The main components of the switching regulator are diode D11, choke coil L3, and filter capacitor C5. When Q3 is turned on by the +12 V control circuit, the voltage at the secondary of T2 is applied across D11, at the input of the LC filter. The constant voltage across L3 results in a linear current buildup, which is absorbed by the output capacitance. Therefore, the +12 Vdc output tends to rise. When the +12 V control circuit turns off Q3, the voltage across L3 reverses polarity, and L3 discharges through D11 into C5 and the load. The +12 Vdc output decreases until Q3 is turned on again. This cycle repeats, with the period either increasing or decreasing, depending on the level of the controlled output; therefore, the output is a ripple centered at the +12 V level.

Overcurrent sensing is accomplished by comparator E1. When the current drawn from the supply reaches 7 A, the voltage at the inverting input of E1 predominates and the output of E1 goes to ground. This ground is applied to the +5 V control circuit, causing it to decrease the duty cycle of the power transformer voltages to a minimum. Then, the output voltage is decreased to make sure the current is kept below 7 A. When the overload condition is removed, typical regulator operation continues.

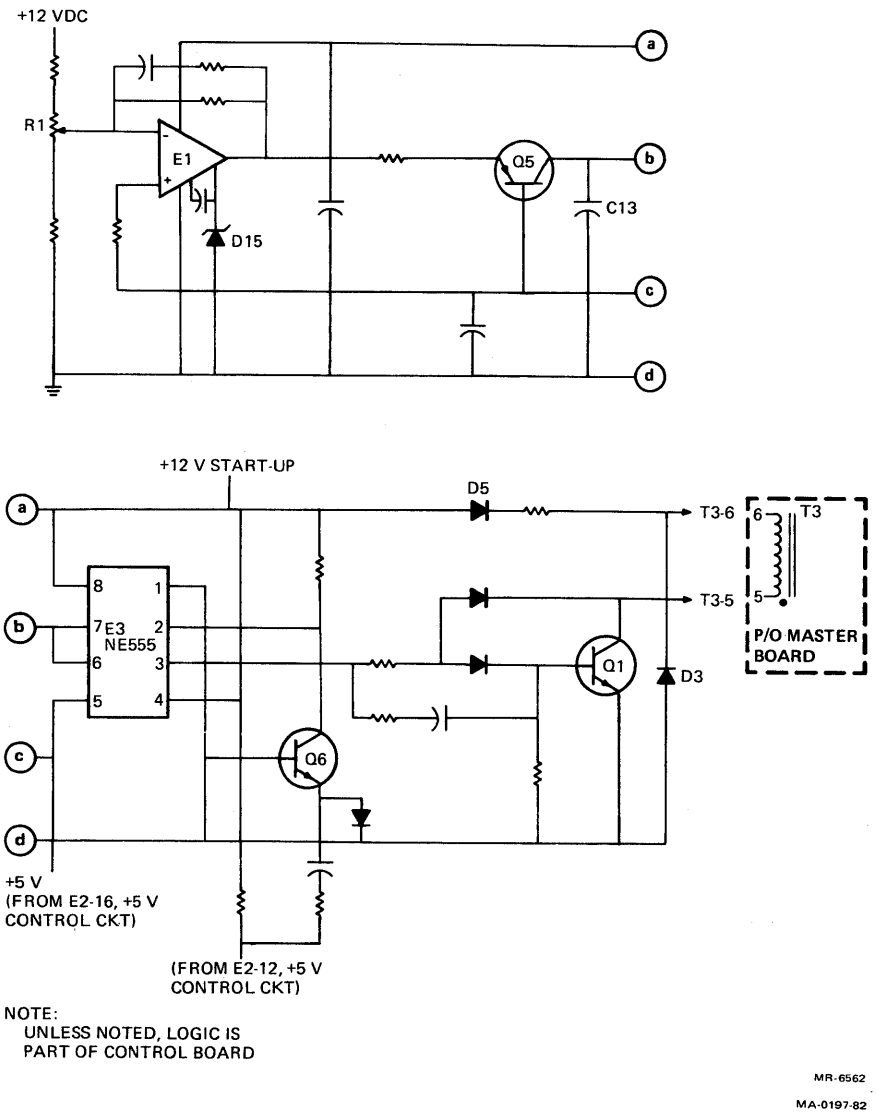


Figure 5-11 +12 V Control Circuit

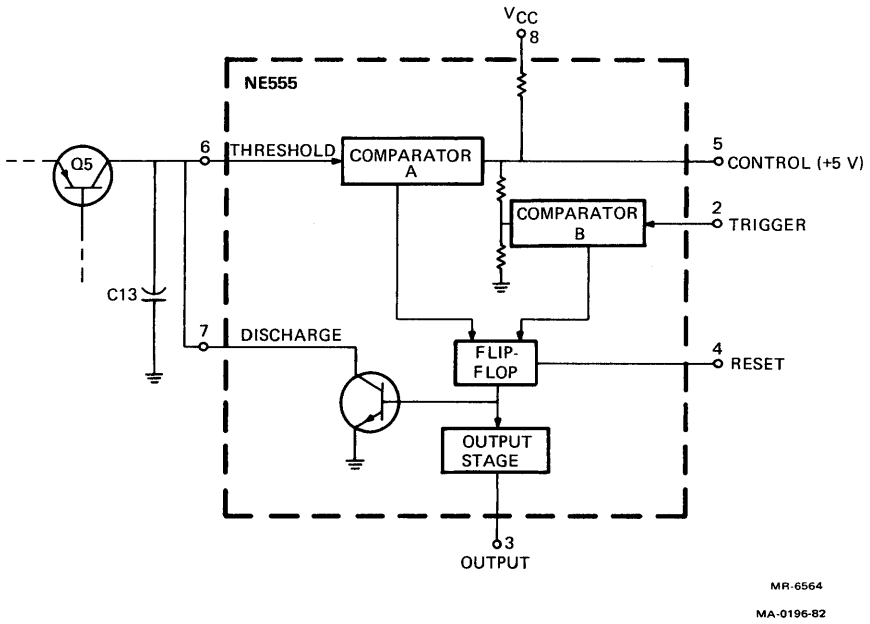


Figure 5-12 Block Diagram, NE555

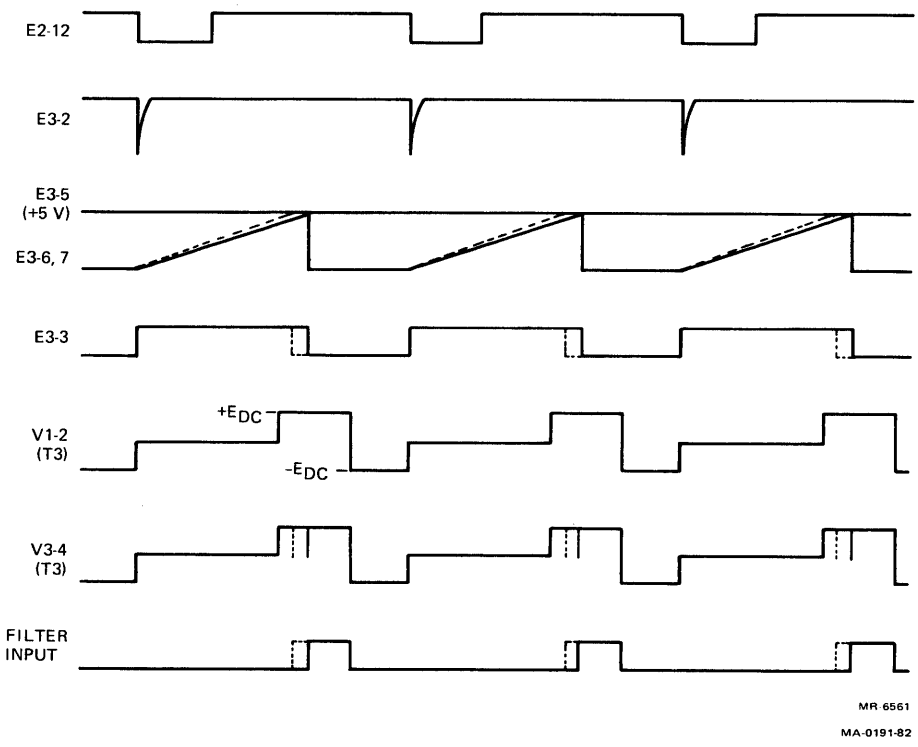


Figure 5-13 Timing, +12 V Control Circuit

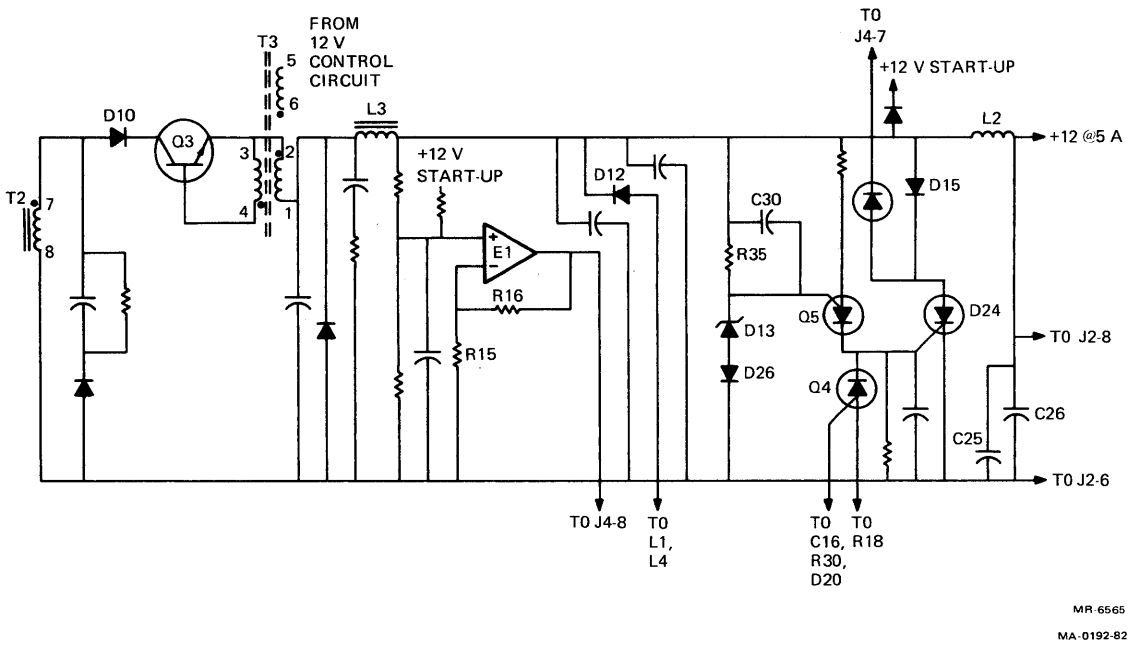


Figure 5-14 +12 V Regulator

Overvoltage protection is provided by the circuitry centered on D2Ø, Q5, Q6, and D24. If the output voltage approaches 14 Vdc, Zener diode D2Ø conducts, turning on unijunction transistor Q5. Q5 provides gate current for SCR Q6, which triggers on. A near-ground voltage is applied through D24 to pin 6 of transformer T1 in the ac input circuit. Hence, the transistor switches in the ac input circuit are turned off, and the voltage on the power transformer goes to zero. Normal operation resumes only when the overvoltage condition is corrected and the power is switched off.

The +5 V regulator is shown in Figure 5-15. Like the +12 V regulator, this circuit includes a switching regulator, an overcurrent sensor, and an overvoltage detector. Each of these works exactly as its equal in the +12 V regulator, except that the voltage and current limits are different; i.e., the overcurrent starts to operate before 48 A and the overvoltage circuit starts to operate at 5.7 V. Also present in the +5 V regulator is the -12 Vdc generator, which is, basically, diode D17 and Zener diode D23.

5.2.2.5 POK/DCOK Circuits -- The power monitor circuits control two signals, BPOK H and BDCOK H. These signals are asserted when the power is turned on or off, or when a power failure occurs. They cause the CPU to carry out specific power-up and power-down operations. Figure 5-16 shows the bus timing specification that BDCOK H and BPOK H must meet; these minimum timing requirements are met by the circuits shown in Figure 5-17.

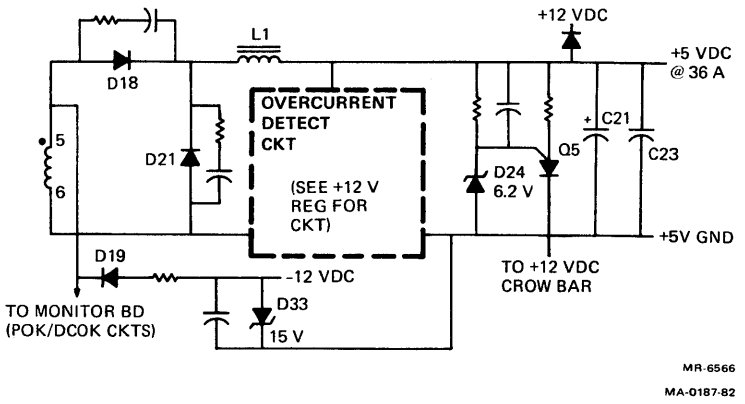


Figure 5-15 +5 V Regulator

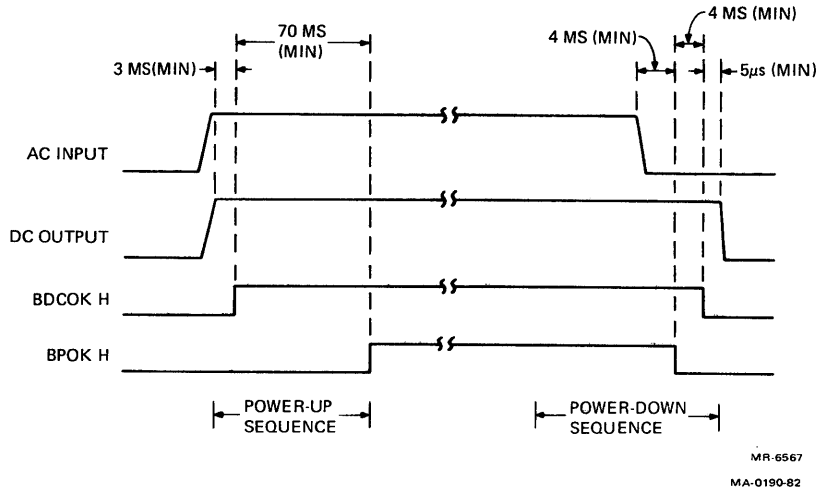


Figure 5-16 Power-Up/Power-Down Timing

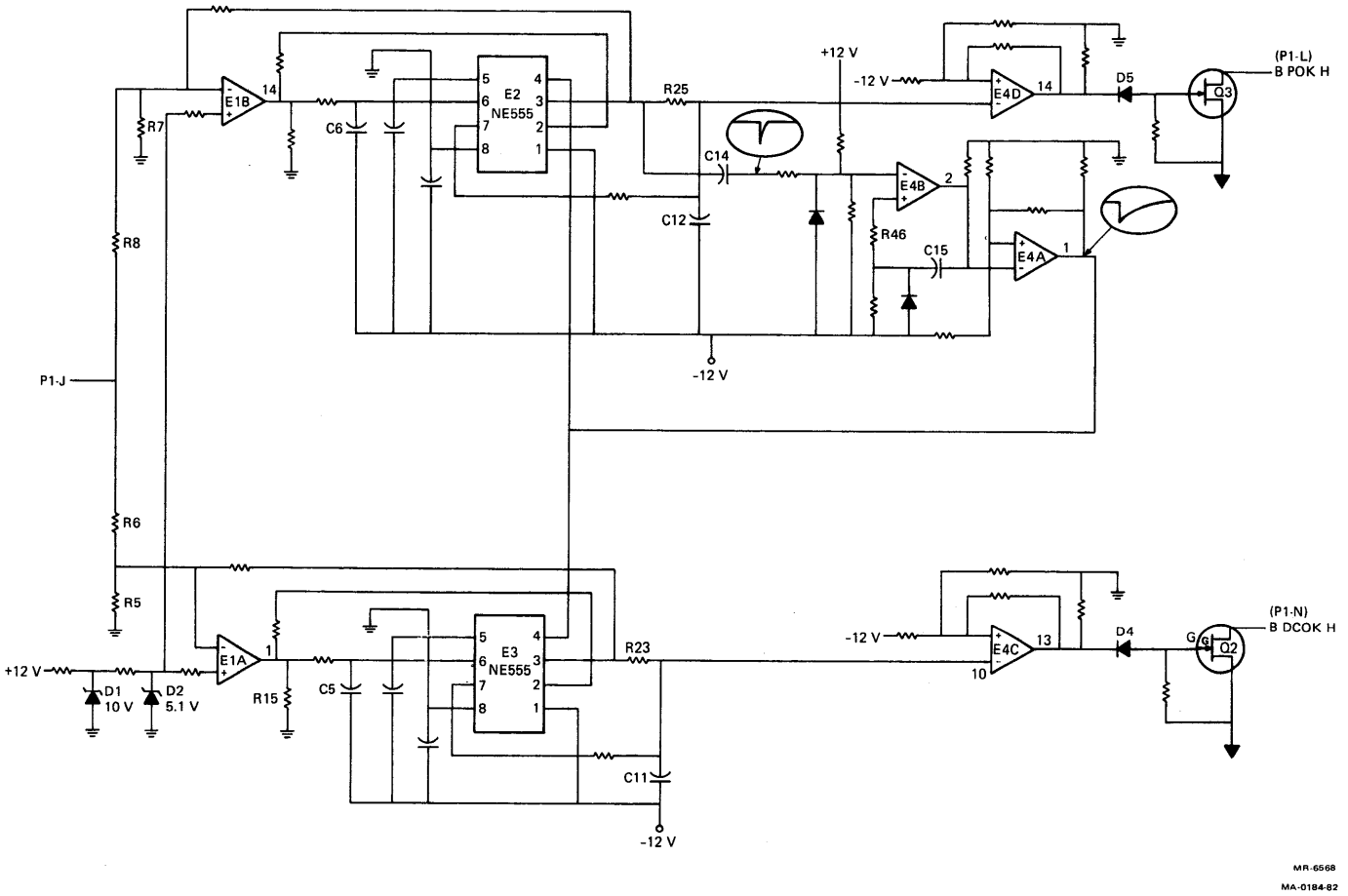


Figure 5-17 POK/DCOK Circuits

The POK circuit and the DCOK circuit work the same way during a power-up sequence. Figure 5-18 presents the timing of significant signals in the DCOK circuit during such a sequence. The signal at P1-J is from the secondary of power transformer T3 in the ac input circuit. When the dc start-up supply voltages have attained a level that is enough to operate the logic, the signal at P1-J is compared to a reference level by voltage comparator E1A. The output of E1A, pin 1, is high when the reference level at the noninverting input is higher than the signal level at the inverting input. When the signal at E1-1 goes high, capacitor C5 charges; when the signal goes low, C5 discharges through R15 to ground. If the peak voltage of the signal at P1-J often rises above 14.5 V, E1-1 goes low occasionally; therefore, C5 charges and discharges repeatedly.

After the circuit starts to operate, the first negative change at E1-1 triggers the timer, E3, and pin 3 goes high. As long as the voltage at pin 6 of the timer stays below the threshold at pin 5, pin 3 stays high. The timer output is applied to comparator E4C, the leading edge of the output being integrated by R23 and C11. When E3-3 goes high, the output at E4-13 also goes high; therefore, D4 is turned off and Ø V are applied to the gate (G) of Q2, a field-effect transistor (FET). Q2 conducts, holding the BDCOK H signal near ground level.

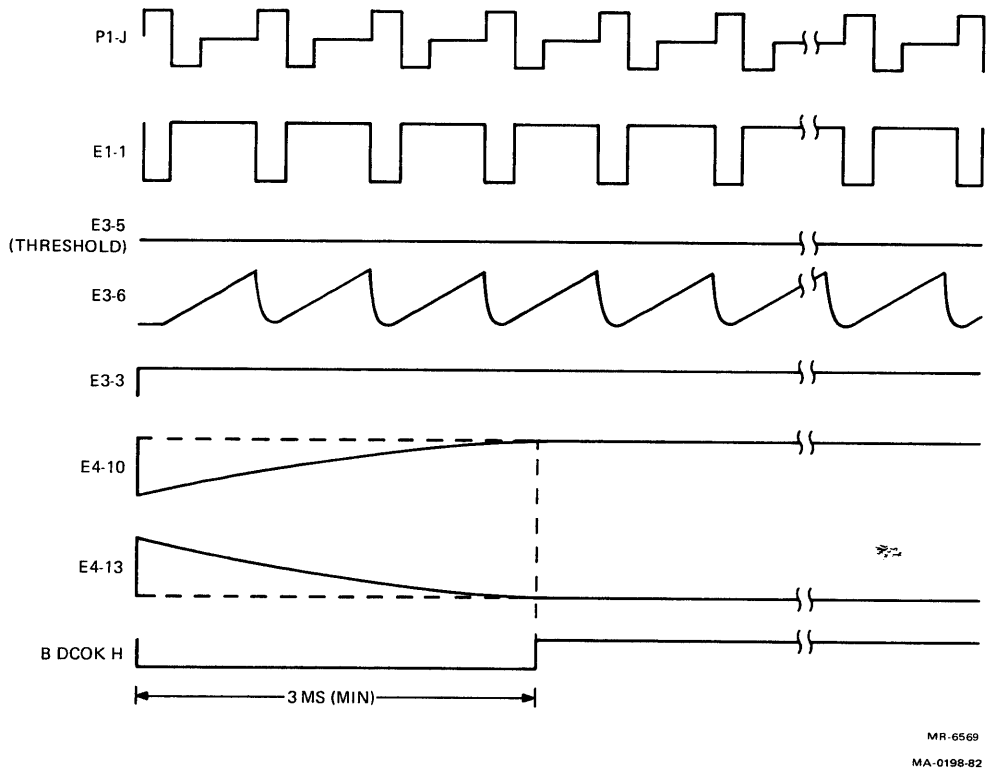


Figure 5-18 DCOK Power-Up Timing

When the signal at E4-13 starts to drop, D4 conducts and a negative voltage is applied to the gate of Q2; ultimately, this voltage becomes negative enough to turn off Q2. At this time BDCOK H is asserted. The time constant of R23/C11 is such that at least 30 ms elapse from the time dc voltages become active to the time that BDCOK H is asserted.

The same type of circuit causes the BPOK H signal to be asserted during the power-up sequence. However, the time constant of R25/C12 at the output of timer E2 is such that at least 100 ms elapse from the time BDCOK H goes high to the time that BPOK H does so. In addition, the POK circuit makes up circuit components that have no counterparts in the DCOK circuit. These components include equals E4A and E4B, which set the circuit timing during a power-down sequence.

Figure 5-19 shows the relationship of significant signals in the POK/DCOK circuits during a power-down sequence. This sequence is started when the ac input at P1-J (Figure 5-17) drops below a predetermined minimum. If the input signal decreases greatly (to below 14.5 V), both the POK circuit and DCOK circuit cause their respective inputs to be asserted. However, the input can decrease just enough to cause only the POK circuit to be turned off (to below approximately 17 V). In this instance, the POK circuit forces the BDOK H signal to go low; so, the result is as if the DCOK circuit had been turned off.

Figure 5-19 shows this condition. That is, the input signal, P1-J, has decreased so that the inverting input of comparator E1B does not rise above the reference level at the noninverting input. Then, the output of E1B fails to go low to discharge capacitor C6 before the threshold level is reached. However, the voltage divider at the inverting input of E1A (R5/R6) differs from its equal at E1B (R7/R8). The voltage at the inverting input of E1A is still enough (in this example) to cause the output of E1A to go low occasionally; therefore, capacitor C5 is repeatedly discharged before reaching the threshold level.

When the voltage at pin 6 of timer E2 reaches the threshold level, the output of E2 (pin 3) goes low. The output of comparator E4D goes high, closing off D5 and causing Q3 to conduct; thus, the BPOK H signal is negated. Now the POK circuit uses comparators E4A and E4B to force the BDCOK H signal low. The output of timer E2 is applied through the comparators to the reset input (pin 4) of each timer, E2 and E3. This causes the output of E3 to go low and holds both timer outputs low regardless of what occurs at the timer inputs. When E3-3 goes low, the output of E4C goes high, closing off D4, Q2 turns on, negating the BDCOK H signal.

If the input signal, P1-J, experiences only a momentary fault, as shown in Figure 5-19, the power-up sequence starts automatically when the timer reset inputs are allowed to go high. The BDCOK H signal is asserted 30 ms after E3-3 goes high, while the BPOK H signal is canceled some 100 ms later.

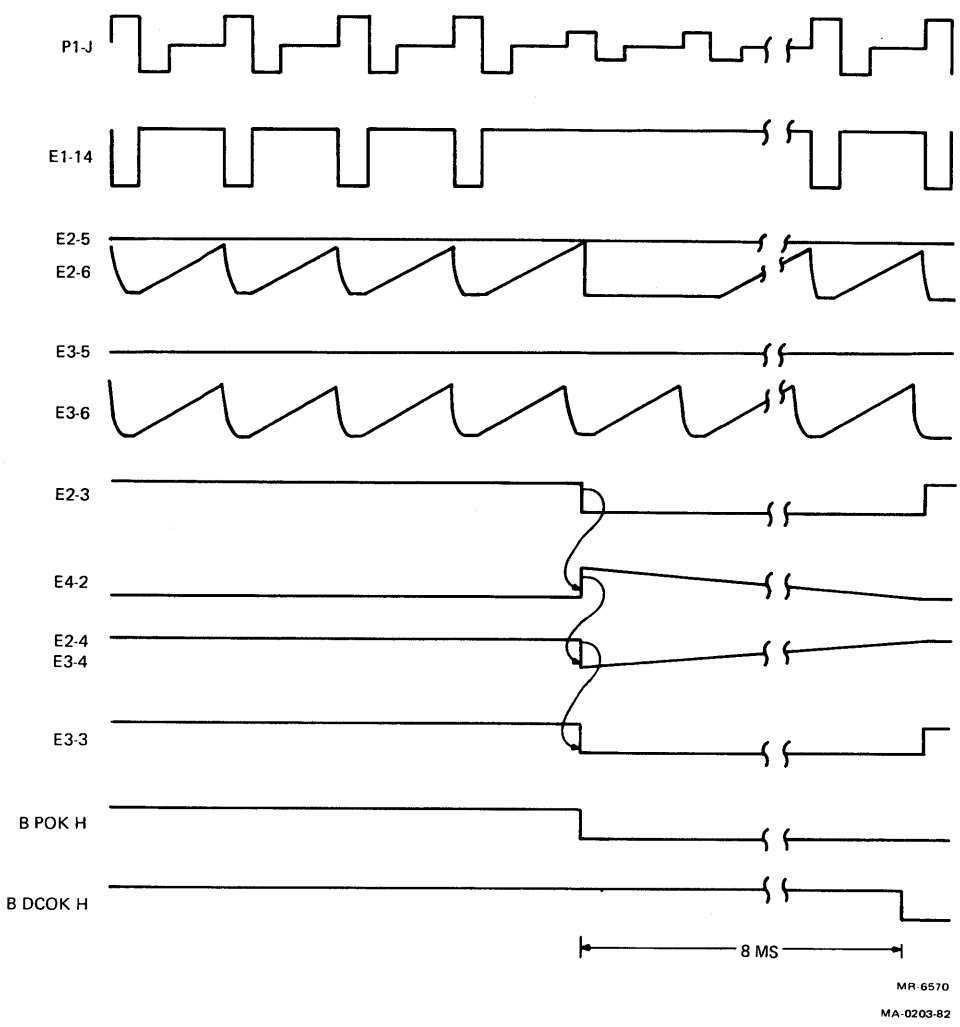


Figure 5-19 Power-Down Timing

5.2.2.6 LTC Generator -- Figure 5-2Ø shows the circuit that generates the LTC signal. The 12.6 Vac output of transformer T1 is applied to both inputs of comparator E1. The waveforms represent how the comparator output controls transistor Q1 to generate LTC.

5.2.3 H9276 Backplane

The BA11-Y backplane is a 9 X 4 backplane that accepts both double-height and quad-height modules. The backplane structure is unique, providing two separate buses, the extended LSI-11 bus and the CD bus. These two buses are shown in Figure 5-21, which also shows the backplane and points out the power and signal connectors (J1--J3). Modules are inserted in slots 1 through 9 of the backplane. The extended LSI-11 bus signals appear on rows A and B; the CD bus signals appear on rows C and D.

The paragraphs that follow include information that is necessary when designing modules for the two buses.

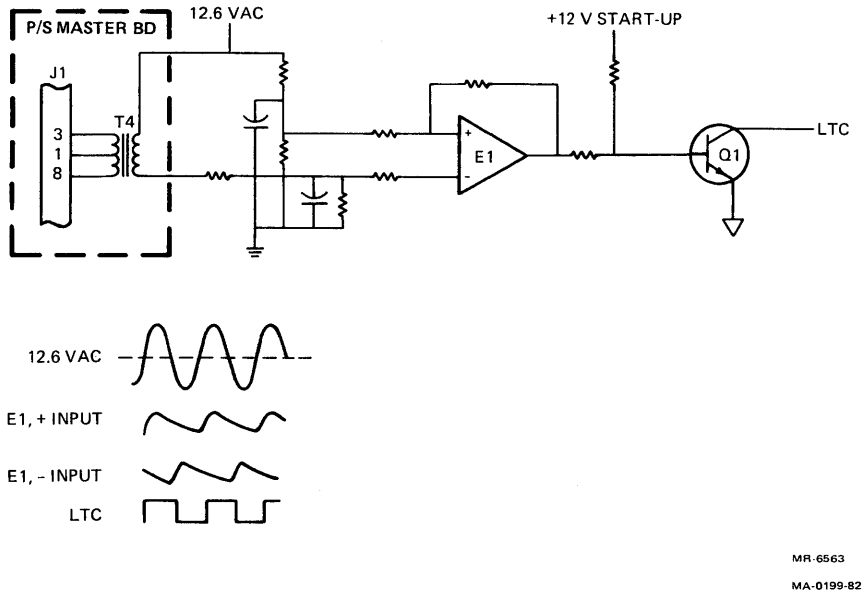


Figure 5-2Ø LTC Generator

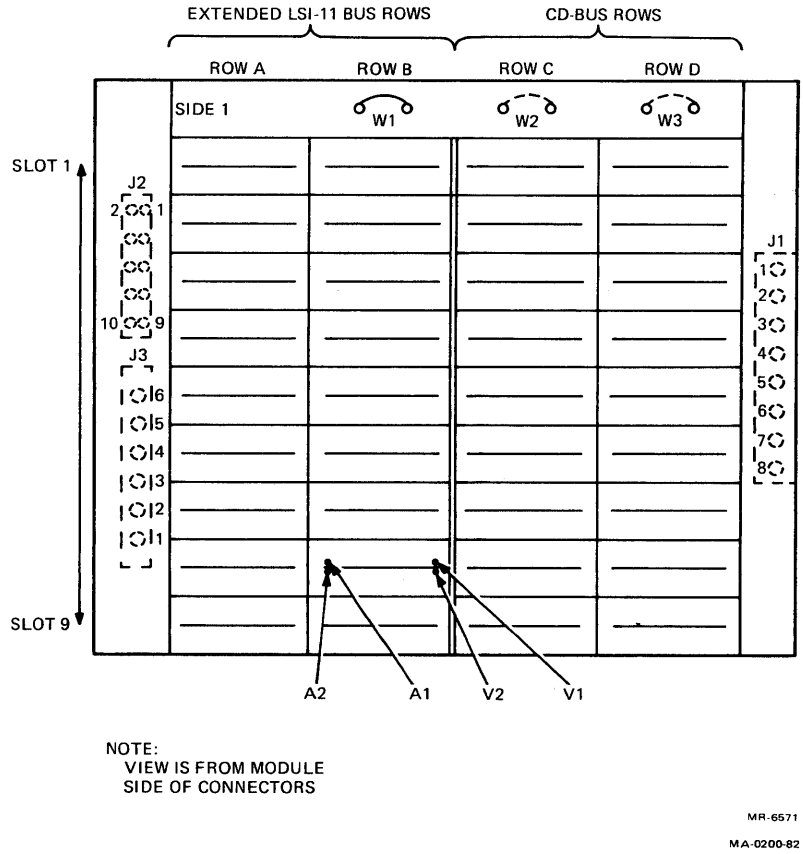


Figure 5-21 H9276 Backplane

5.2.3.1 **Extended LSI-11 Bus Signals** -- The extended LSI-11 bus signals in the H9276 backplane are provided by rows A and B. Most of these signals are bused to the same pin in all nine slots of the backplane. Certain defined spare pins are not bused. Also, interrupt acknowledge and bus grant signals (BIAKO L, BIAKI L, BDMGO L, amd BDMGI L) are not bused, being connected, instead, as shown in Figure 5-22. The interrupt acknowledge and bus grant signals are passed from module to module by etch jumpers that connect pin M2 to pin N2 and pin R2 to pin S2 on connector A of the module. Therefore, there can be no empty module positions between the CPU (which occupies slot 1) and an I/O device option that uses these signals.

If the extended LSI-11 bus is to be continued to a second backplane, an M9404 connector module is inserted into connectors A and B of the last usable slot in the first backplane, while an M9405 connector module is inserted into slot 1 (rows A and B) of the second backplane (refer to Paragraph 2.13.2 and Appendix C for details). A pair of BC02D-05 cables are used with these modules to connect one H9276 backplane to another.

Table 5-1 lists the extended LSI-11 bus signals and the assigned pin numbers.

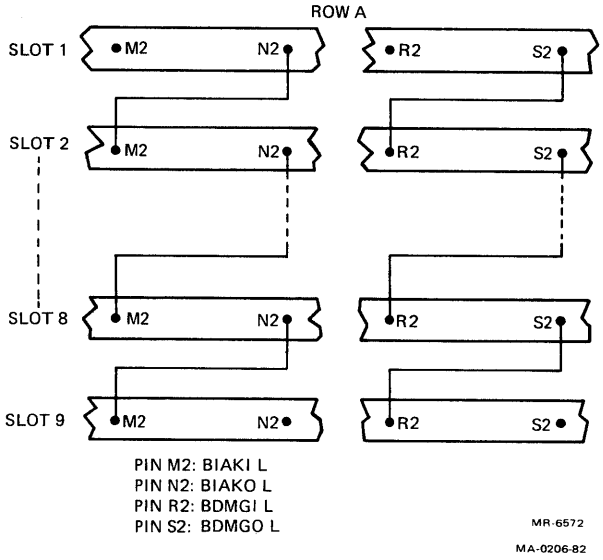


Figure 5-22 Interrupt Acknowledge and Bus Grant Signal Interconnection, H9276 Backplane

Table 5-1 Extended LSI-11 Bus Signal Pin Assignments

Slot, Side	A1	A2	B1	B2
Pin				
A	BIRQ 5 L*	+5	BDCOK H	+5
B	BIRQ 6 L*	-12	BPOK H	-12
C	BDAL 16 L	GND	BDAL 18 L*	GND
D	BDAL 17 L	+12	BDAL 19 L*	+12
E	SSPARE 1+	BDOUT L	BDAL 20 L*	BDAL 2 L
F	SSPARE 2	BRPLY L	BDAL 21 L*	BDAL 3 L
H	SSPARE 3	BDIN L	SSPARE 8	BDAL 4 L
J	GND	BSYNC L	GND	BDAL 5 L
K	MSPARE A	BWTBT L	M SPARE B	BDAL 6 L
L	MSPARE A	BIRQ L	M SPARE B	BDAL 7 L
M	GND	BIAKI L	GND	BDAL 8 L
N	BDMR L	BIAKO L	BSACK L	BDAL 9 L
P	BHALT L	BBS7 L	BSPARE 5	BDAL 10 L
R	BREF L	BDMGI L	BEVENT L	BDAL 11 L
S	+12 B	BDMGO L	+12 B	BDAL 12 L
T	GND	BINIT L	GND	BDAL 13 L
U	PSPARE 1	BDAL0 L	P SPARE 2	BDAL 14 L
V	+5B	BDAL1 L	+5	BDAL 15 L

* Extended LSI-11 bus pins.

† Some memory module types may require +5 VB to be jumpered from connector pins AV1 to AE1 on the extended LSI-11 bus rows A and B slots (2 through 9 only) for that module.

5.2.3.2 CD Bus Signals -- Rows C and D supply the CD bus signals. Figure 5-23 shows the connections to the CD bus. Clearly, only five of the nine slots are pictured. The +5 V supply is bused to all slots on pin A2 of rows C and D (i.e., pins CA2 and DA2). Also, ground connections on pins CC2, CT1, DC2, and DT1 are bused to all slots. All other pins connect only to an adjacent slot. For example, pin CF2 of any slot connects only to pin CF1 of the adjacent higher numbered slot. Pins on side 2 of the row (B2, C2, etc.) connect at the adjacent higher numbered slot (except DT2, which connects to CT2 of the adjacent lower numbered slot), while pins on side 1 of the row (B1, C1, etc.) connect to the adjacent lower numbered slot (except pin A1, which connects to C1 of the adjacent higher numbered slot). Then, each slot, except 1 and 9, has 33 signal connections (i.e., connections other than +5 V and ground) to both the adjacent higher numbered slot and the adjacent lower numbered slot. To help reference to these two groups of 33 signals, group 1 is defined as making up the signals connecting a slot (slot X) to its adjacent lower numbered slot (slot X-1), while group 2 is defined as making up the signals connecting a slot to its adjacent higher numbered slot (slot X+1). This group distinction is maintained in Table 5-2, which lists row C and D pins for slot X and assigns signal names to each pin. Generally, group 1 signals are found on side 1 pins, while group 2 signals are found on side 2 pins.

NOTES

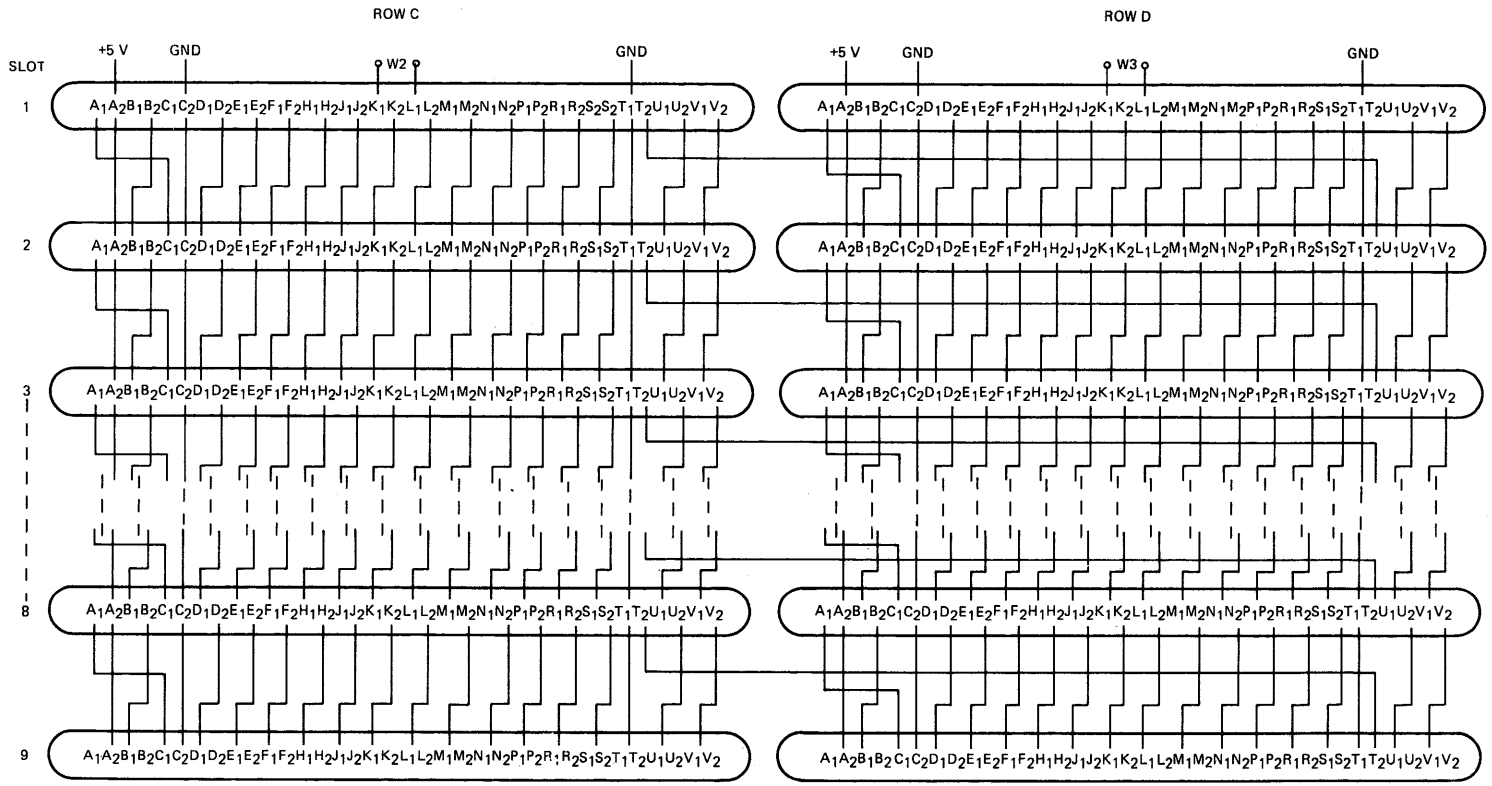
1. **Bus pins are called out as AK1, AS1, BC2, etc. A callout such as AS1, for example, means row A, pin S, side 1.**

2. **The following spare pins are not bused: S SPARE 1 - S SPARE 8; M SPARE A and M SPARE B (in each slot, AK1 is connected to AL1 and BK1 is connected to BL1); P SPARE 1 and P SPARE 2. The following signals are not bused: BIAKI L, BIAKO L, BDMGI L, and BDMGO L.**

3. **If a CPU is installed in slot 1, pin AF1 of slot 1 (formerly a spare) becomes S RUN L.**

Descriptions of these signals can be found in the 1979--1980 Microcomputer Processor Handbook.

W1, W2, and W3 backplane jumpers are removed when the BA11-Y mounting box is used as an expander box (without a CPU module). Otherwise, these jumpers short together pins in the first backplane slot C01KI to C01LI and D01KI to D01LI, respectively.



NOTE:
WITH SOME PROCESSORS, W2 AND W3 INSTALLED ENABLE THE CPU TO OPERATE IN SLOT 1. IF THE BACKPLANE IS BEING USED AS AN EXTENDED BUS, REMOVE THE JUMPERS (THE CPU MUST BE PLACED IN SLOT 1 OF THE MAIN BOX ONLY). IN THE DYS50, JUMPERS W2 AND W3 HAVE NO FUNCTION. THEY ARE NOT CONNECTED TO ANYTHING.

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Figure 5-23 CD Bus Interconnections

Table 5-2 CD Bus Signal Pin Assignments

Row	Pin	Side 1	Side 2
C	A	INTCON 1, Group 2	+5 V
	B	INTCON 2, Group 1	INTCON 2, Group 2
	C	INTCON 2, Group 1	GND
	D	INTCON 3, Group 1	INTCON 3, Group 2
	E	INTCON 4, Group 1	INTCON 4, Group 2
	F	INTCON 5, Group 1	INTCON 5, Group 2
	H	INTCON 6, Group 1	INTCON 6, Group 2
	J	INTCON 7, Group 1	INTCON 7, Group 2
	K	INTCON 8, Group 1	INTCON 8, Group 2
	L	INTCON 9, Group 1	INTCON 9, Group 2
	M	INTCON 10, Group 1	INTCON 10, Group 2
	N	INTCON 11, Group 1	INTCON 11, Group 2
	P	INTCON 12, Group 1	INTCON 12, Group 2
	R	INTCON 13, Group 1	INTCON 13, Group 2
	S	INTCON 14, Group 1	INTCON 14, Group 2
	T	GND	INTCON 33, Group 2
	U	INTCON 15, Group 1	INTCON 15, Group 2
	V	INTCON 16, Group 1	INTCON 16, Group 2
D	A	INTCON 17, Group 2	+5 V
	B	INTCON 18, Group 1	INTCON 18, Group 2
	C	INTCON 17, Group 1	GND
	D	INTCON 19, Group 1	INTCON 19, Group 2
	E	INTCON 20, Group 1	INTCON 20, Group 2
	F	INTCON 21, Group 1	INTCON 21, Group 2
	H	INTCON 22, Group 1	INTCON 22, Group 2
	J	INTCON 23, Group 1	INTCON 23, Group 2
	K	INTCON 24, Group 1	INTCON 24, Group 2
	L	INTCON 25, Group 1	INTCON 25, Group 2
	M	INTCON 26, Group 1	INTCON 26, Group 2
	N	INTCON 27, Group 1	INTCON 27, Group 2
	P	INTCON 28, Group 1	INTCON 28, Group 2
	R	INTCON 29, Group 1	INTCON 29, Group 2
	S	INTCON 30, Group 1	INTCON 30, Group 2
	T	GND	INTCON 33, Group 1
	U	INTCON 31, Group 1	INTCON 31, Group 2
	V	INTCON 32, Group 1	INTCON 32, Group 2

5.2.3.3 Module Requirements for H9276 Capability -- Modules used in the BA11-Y box are of two classes: those that function with 18-bit addressing and those that function with 22-bit addressing.

A double-height module that has been designed for 18-bit addressing capability can be used with both the KDF11-A and the KDF11-B processor modules. Such a system is limited to 256 Kb of memory; however, both the KDF11-A Rev C and later and the KDF11-B function use a 22-bit addressing system. A double-height module designed for the CD bus can only be inserted into the H9276 backplane CD bus rows. Table 5-3 lists the compatible CD bus signals.

Quad modules designed to be used with an H9273 backplane, are compatible with the H9276 backplane as long as they do not use BDAL 18--21 for another reason. Both backplanes have etch jumpers connecting pin M2 to pin N2 and from pin R2 to pin S2 on the module connector A only. Also, these jumpers permit passage of the BIAK and BDMG signals.

Figure 5-24 shows a portion of each backplane to show the differences between the wiring of pins M, N, R and S in rows A and C of both the H9273 and H9276 backplanes.

Table 5-3 CD Bus Signals for H9276 Compatible Quad Modules

CD Bus Signal	Pin Number
+5 V	CA2, DA2
GND	CT1, CC2, DT1, DC2
INTCON 4, Group 1	CE1
INTCON 5, Group 1	CF1
INTCON 6, Group 1	CH1
INTCON 10, Group 2	CM2*
INTCON 11, Group 2	CN2*
INTCON 13, Group 2	CR2*
INTCON 14, Group 2	CS2*
INTCON 17, Group 1	DC1
INTCON 19, Group 1	DD1
INTCON 20, Group 1	DE1
INTCON 21, Group 1	DF1
INTCON 22, Group 1	DH1

* Etch jumpers between CM2 and CN2, CR2 and CS2, respectively, must be placed on modules used in an H9270 backplane to allow passage of the BIAK and BDMG signals.

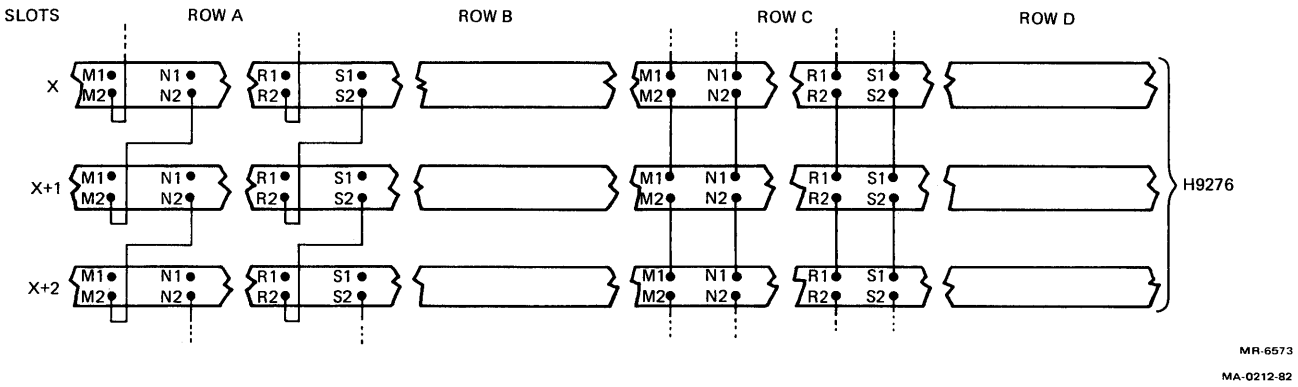


Figure 5-24 H9276 Backplane Wiring (Rows A and C)

5.2.3.4 Modules Designed for the H9276 Backplane Only -- Modules can be used in the H9276 backplane either singly or in sets. The single, or standalone, module communicates with other modules only through the extended LSI-11 bus. A double-height, standalone module is inserted into extended LSI-11 rows A and B. A quad-height, standalone module can use the group 1 INTCON signals but cannot use the group 2 signals.*

A module set is made up of more than one module. The module occupying the highest numbered slot of the set must not use the group 2 INTCON signals. All other modules of the set can use both the group 1 and group 2 INTCON signals. The module in the lowest numbered slot can use the group 1 signals as test points;* its group 2 signals communicate with the second module of the set. Each module after the first communicates with its neighbors with both the group 1 and group 2 signals except, of course, the last module of the set, which does not use the group 2 signals.

A bus can be created for each module set by connecting group 1 pins to group 2 pins on each center module. For example, if you have a four-module set, you can create an INTCON 4 bus by connecting pin CE1 to pin CE2 on both the second and third modules of the set.

Module sets can be expanded at any time. However, the set can be expanded upward, only. That is, if a module is added to an existing set, it must occupy the lowest numbered slot of the new set.

---

* A standalone module might have INTCON 1Ø, group 1, shorted to INTCON 11, group 1, and INTCON 13, group 1, shorted to INTCON 14, group 1. Refer to Paragraph 5.2.3.3 for an explanation.

5.2.3.5 Electrical Protection for Quad-Height and Double-Height Module -- Use only quad-height modules that have extractor-type handles in the H9276 backplane. (The extractor-type handle is shown in Figure 3-4). These handles help you to insert and extract the module. More importantly, the card frame of the BA11-Y is designed so that these handles prevent a module from being inserted upside down. If a quad module having plastic U-shaped handles must be used, confirm that the module is inserted correctly; i.e., the component side of the module must be on top.

Double modules have only plastic U-shaped handles. These modules can be inserted in backplane rows A and B or C and D, depending on whether they are designed to use the extended LSI-11 bus or the CD bus, in order. Obviously, it is possible to insert these modules not only backwards but also in the wrong bus. Therefore, electrical protection must be included in the design of double modules; i.e., the assignment of supply voltages to connector pins must be done so that if a module is incorrectly inserted in the backplane, supply voltage will not be applied to signal pins.

Electrical protection for extended LSI-11 bus double modules is afforded by the design of the H9276 backplane. A double module designed to be inserted in the extended LSI-11 rows (A and B) can be inserted upside down with no damage to power supply voltages. That is, a module pin that is supposed to receive +12 Vdc, gets +12 Vdc whether the module is right-side up or upside down. The same protection is afforded if the module is inserted in the CD bus, right-side up or upside down. Of course, an incorrectly inserted module will not work correctly. If the system fails to operate (either totally or in a specific area) after module installation or replacement, be sure that all modules are inserted correctly in the backplane before trying other troubleshooting methods.

Unfortunately, the backplane cannot provide protection for modules designed to use the CD bus. Therefore, the protection must be designed into the module itself. The pins listed in Table 5-4 are those that must be protected from incorrect placement of the CD bus module (the double-module connectors are labeled A and B even though they are inserted in CD bus rows C and D, in order). For example, a module designed for the CD bus receives +5 Vdc from backplane pins CA2 and DA2, and no other voltage. If the module was inserted in the extended LSI-11 bus (A and B), it would receive +5 Vdc, -12 Vdc and +12 Vdc on the pins listed in Table 5-4.

Table 5-4 Vulnerable CD Bus Double Module Connector Pins

Module Pin	Voltage to Which Pin Might Be Exposed
AV1, BV1, AE1*	+5 V, +5 VB
AB2, AU1, BB2, BU1	-12 V
AD2, AS1, BD2, BS1	+12 V, +12 VB

5.2.4 Front Bezel Assembly

Figure 5-25 represents the logic linked with the front panel switches and indicators. (Paragraph 2.4 tells how to use the switches and how to interpret the indicators.) The logic components are mounted on a printed circuit board that is attached to the rear of the front panel. A signal cable that plugs into J1 of the printed circuit board carries the signals between the front panel and the power supply master board. J2 is cabled to the remote switch connector on the front panel.

Indicator lights D1 and D2 light when the power supply is operating correctly and when the CPU is running. D1, the PWR OK indicator, lights when the B POK H signal from the power supply is asserted. D2, the RUN indicator, lights as long as the CPU generates the signal S RUN L. This signal is applied to the positive trigger input of retriggerable one-shot multivibrator E3A. The basic pulse width of E3A is greater than the period (t) of S RUN L (Figure 5-26); therefore, E3A is continually retriggered by S RUN L and stays on until S RUN L is negated. The 1 output of E3A causes the RUN indicator to light (the jumper in W4 is in place when the CPU is inserted into the backplane).

In meeting its more obvious function, switch S2 grounds the B HALT L signal when it is moved to the HALT position (down). Then, the CPU can be forced to halt typical program execution from the front panel of either the main box or an expander box. To continue operation after using the HALT switch, return the HALT switch to the enable position (up) and enter a P command from the console terminal. (Refer to Chapter 4 of the 1979-1980 Microcomputer Processor Handbook for a description of console ODT command usage.)

Not only can you halt the CPU from the front panel, but you can also reboot it. When you lift and release the momentary RESTART switch, S1, the CPU halts and then automatically carries out a power-up sequence. Figure 5-25 shows switch S1 in the typical operating position (down). When the operator lifts and then releases S1, allowing it to return to the down position, a positive-to-negative change is applied to the negative-trigger input of one-shot multivibrator E3B. This negative change causes the one-shot to generate a gate of 1 us (minimum) duration; this gate first negates BDCOK H and then permits it to be reasserted to complete the reboot operation.

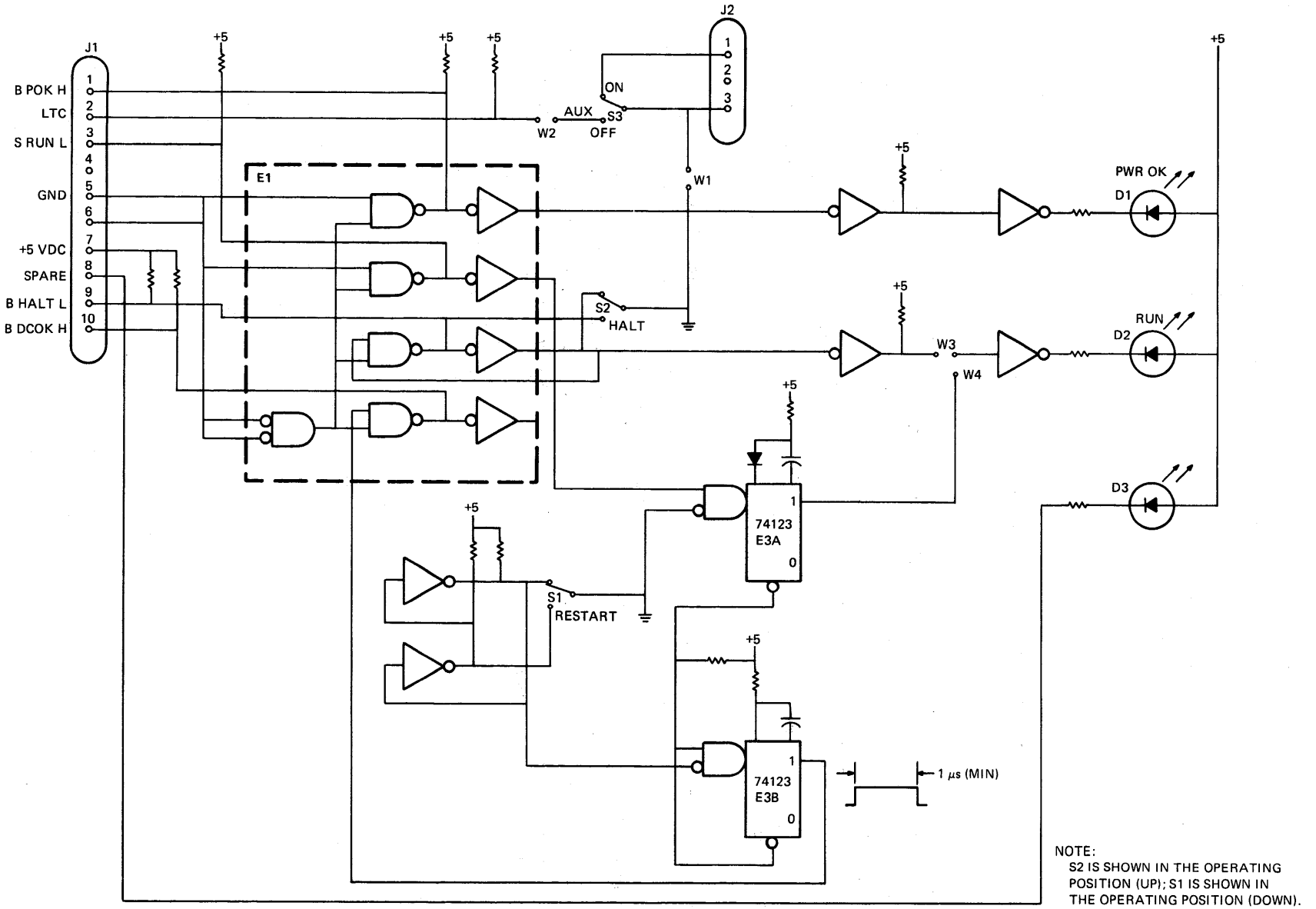


Figure 5-25 Front Panel Logic

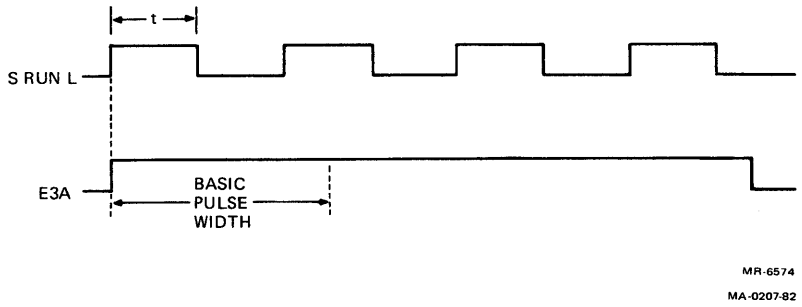


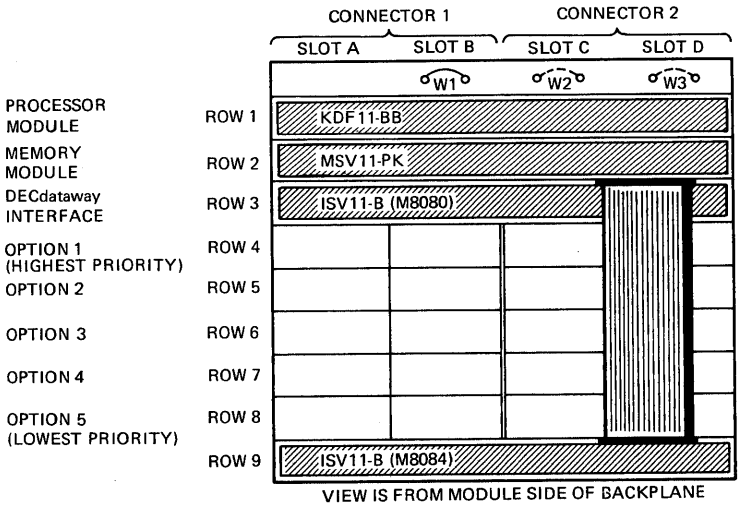
Figure 5-26 RUN Indicator Waveforms

The third switch shown in Figure 5-25 is the AUX switch, S3. The switch contacts can be used for any function; however, the following two mutually exclusive functions are the most common. One function is to operate as a system on/off switch when a power controller is part of the system; jumpers W1 and W2 must be removed if this feature is to be used. The other function is to operate as an on/off switch for the power supply generated LTC signal; jumpers W1 and W2 must be installed if this feature is to be used.

When used as a system on/off switch, S3 is connected to a power controller by a cable that plugs into connector J2. With S3 in the ON position, primary power is applied to the power controller and distributed by it through the system. In the LTC application, S3, when in the ON position, permits the LTC signal to be used as an LTC interrupt in the CPU. In the OFF position, S3 grounds the LTC signal, which is a necessary feature when certain diagnostic programs are being executed.

APPENDIX A
DYS5Ø KERNEL SYSTEM CONFIGURATION

Figures A-1 through A-6 show the factory settings for all DYS5Ø kernel system jumpers and switches.



H9276 OPTION POSITIONS

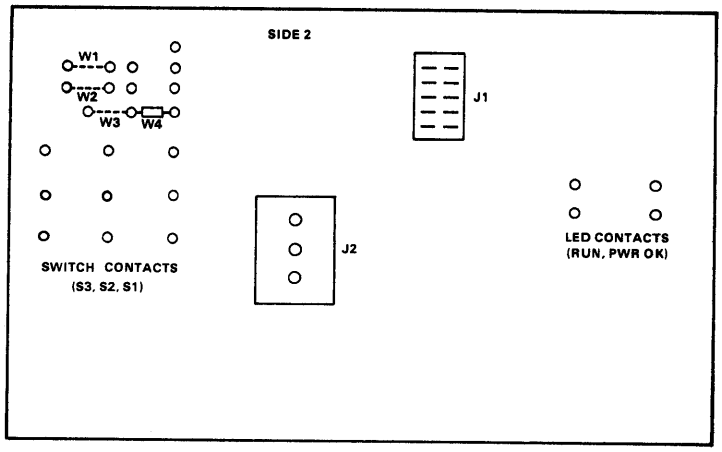
STANDARD FACTORY JUMPER CONFIGURATION

JUMPER	JUMPER STATE	FUNCTION
*W1	IN	THE H7861 POWER SUPPLY GENERATED LTC SIGNAL IS USED TO ASSERT BEVNT L SIGNAL
W2, W3	OUT	THESE JUMPERS HAVE NO EFFECT ON DYS50 OPERATION

*W1 MUST BE REMOVED FROM ALL EXPANDER BOXES IN A MULTIPLE-BOX SYSTEM SINCE ONLY THE BOX CONTAINING THE KDF11-BB (M8189) MODULE MUST BE THE SOURCE OF THE LTC SIGNAL

MA-7101B

Figure A-1 DYS5Ø Kernel System Backplane Configuration



NOTES:

1. VIEW IS FROM THE REAR OF THE BEZEL WHEN THE BOARD IS MOUNTED ON THE BEZEL.
2. JUMPERS ARE MOUNTED ON SIDE 2.

FACTORY JUMPER CONFIGURATION

JUMPER	JUMPER STATE	FUNCTION
W1, W2	OUT	ALLOWS THE AUX ON/OFF SWITCH TO TURN THE SYSTEM POWER ON AND OFF
W3	OUT	CPU IS MOUNTED IN THIS BACKPLANE
W4	IN	ENABLES THE RUN INDICATOR BECAUSE THE CPU IS MOUNTED IN THIS BACKPLANE

MA-07378

Figure A-2 DYS5Ø Bezel Printed Circuit Board Factory Configuration

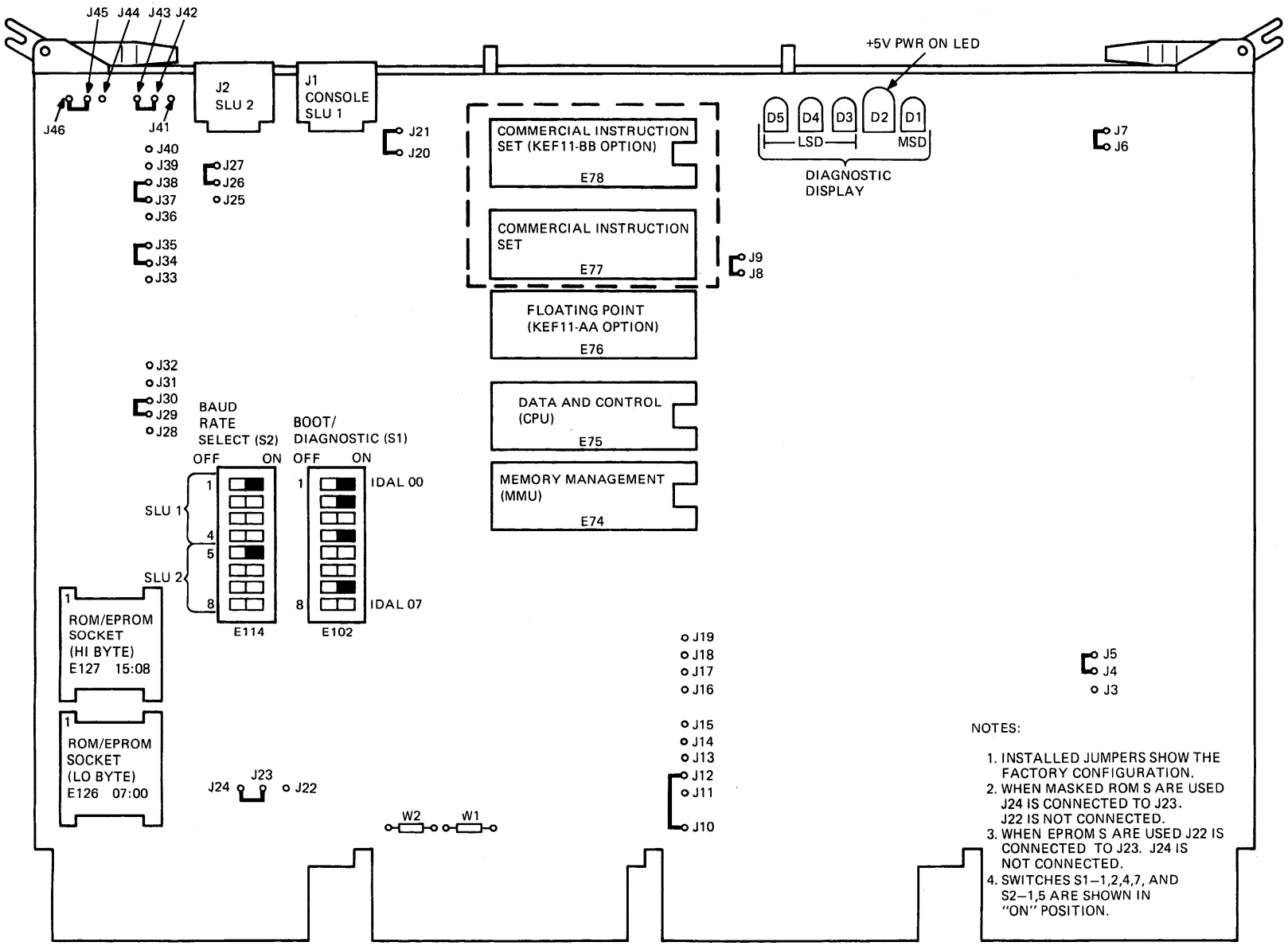
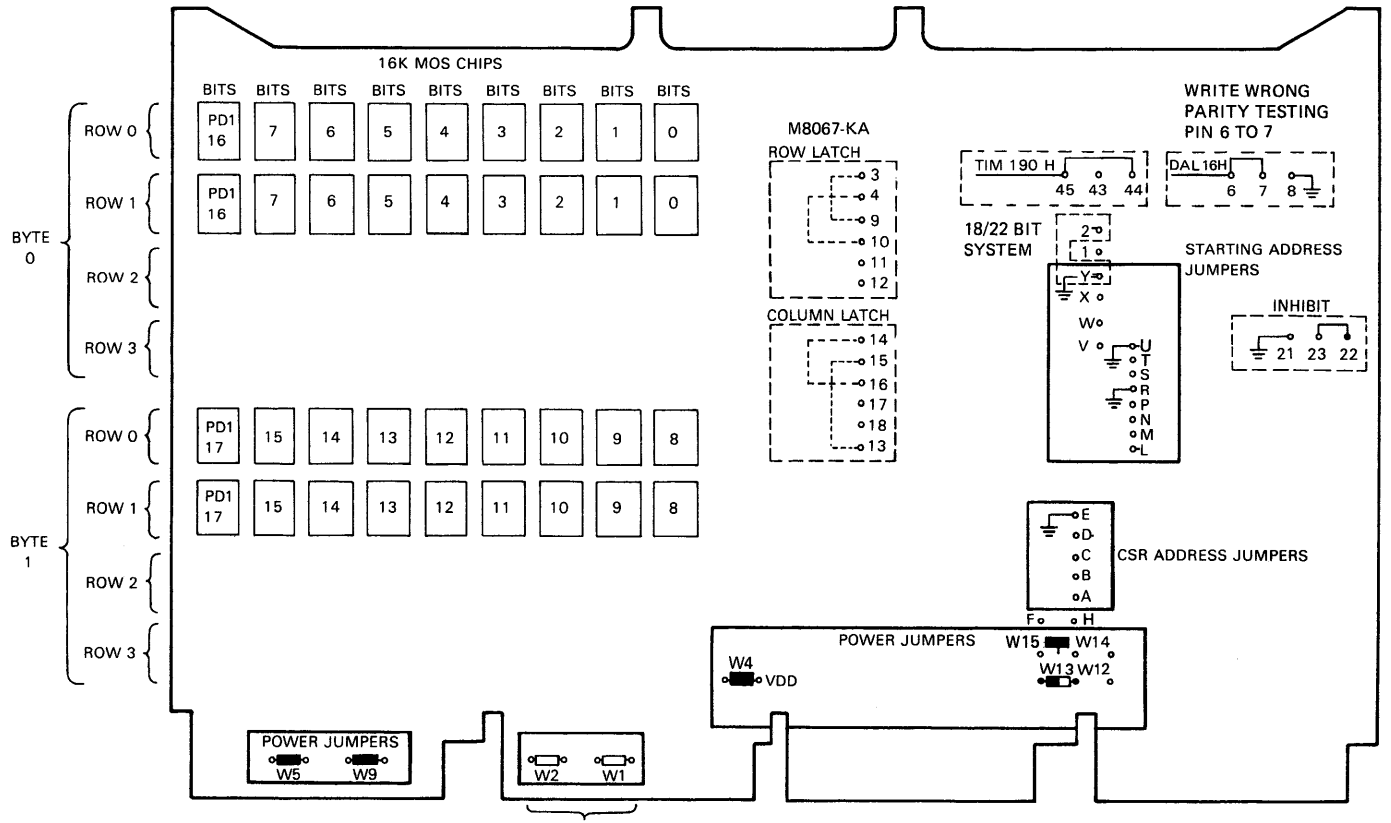


Figure A-3 Factory Configuration of the KDF11-BB (M8189) in the DYS50



16K MULTIPLE VOLTAGE DEVICES

NON-BAT BACK-UP	BAT BACKUP	VOLTAGES
W3	W3	-5
W11	W10	+12 VDD
W13	W12	+5 CR

64K SINGLE VOLTAGE DEVICES

NON-BAT BACK-UP	BAT BACKUP	VOLTAGES
W4	W4	DECOUPLE +5
W5	W5	DECOUPLE +5
W9	W12	+5 CR
W13/W15	W14	+5 VDD

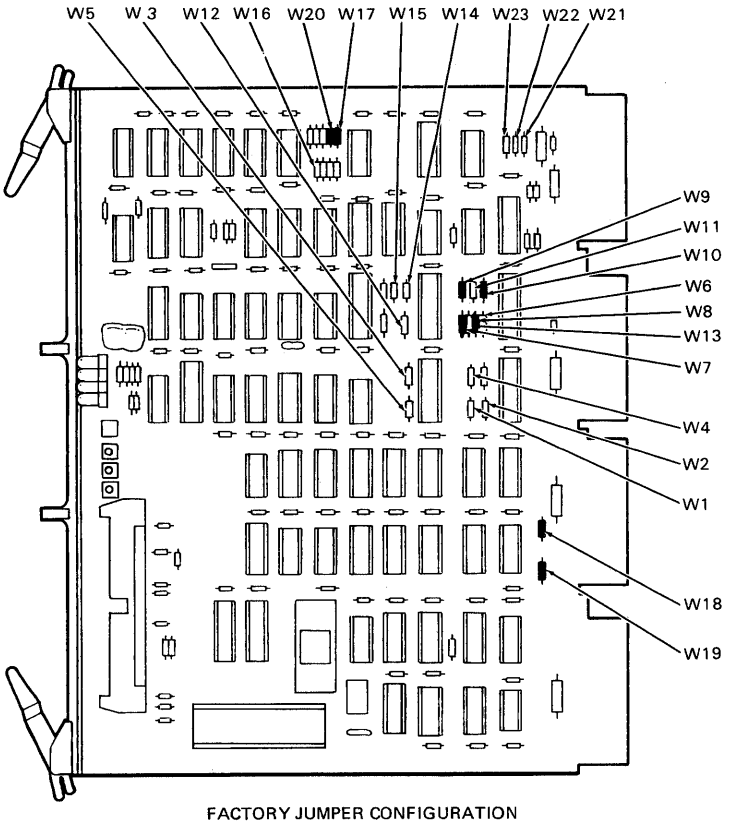
GRANT CONTINUITY
W1 AND W2 IN FOR Q/Q MACHINE, Q22/Q22 MACHINE
W1 AND W2 OUT FOR Q/CD AND Q22/CD MACHINE

POWER JUMPERS FOR 16K MOS CHIPS WITHOUT BATTERY BACKUP

- POWER JUMPER IN FOR 64K CHIPS
- POWER JUMPER IN FOR 16K CHIPS
- POWER JUMPER IN FOR BOTH 64K/16K CHIPS

MA-7148B

Figure A-4 Factory Configuration of the MSV11-P (M8067-KA) in a DYS50



FACTORY JUMPER CONFIGURATION

IN: W7, W8, W9, W10, W17, W18, W19, W20

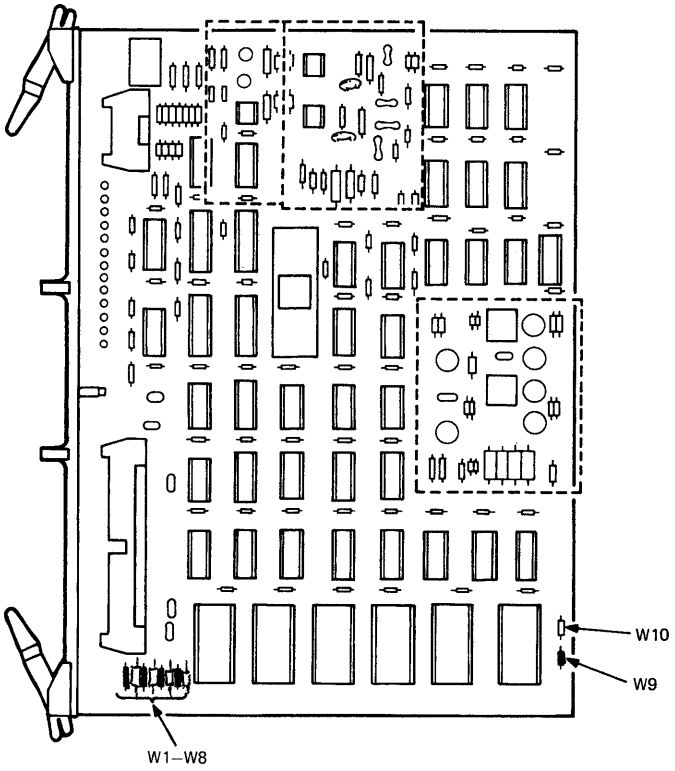
OUT: ALL OTHERS

JUMPER FUNCTIONS

JUMPER	USE
W1-W8, W12, W13	LSI-11 BUS ADDRESS
W9-W11, W14, W15	VECTOR ADDRESS
W16	HOLD ON B SACK L
W17, W20	DMA TIMERS
W18, W19	CONNECT PINS
W21-W23	RESERVED

MA-7104

Figure A-5 ISV11-B M8080 Module Standard Configuration



FACTORY JUMPER CONFIGURATION

IN: W1, W3, W5, W7, W9

OUT: ALL OTHERS

JUMPER FUNCTIONS

JUMPER	USE
W7, W8	PROM SELECTION
W1-W6, W9, W10	PROM POWER

MA-7105

Figure A-6 ISV11-B M8084 Module Standard Configuration

APPENDIX B
SPECIAL CIRCUITS

B.1 DCØØ3 INTERRUPT CONTROL (Figures B-1, B-2, and B-3)

The interrupt control chip is an 18-pin, Ø.762 cm (Ø.3ØØ in) center, DIP device. It provides circuits to perform an interrupt transaction in a computer system that uses a pass-the-pulse arbitration scheme. The device is used in peripheral interfaces and has two interrupt channels labeled A and B. The A section is at a higher priority than the B section. Bus signals use high impedance input circuits or high drive open collector outputs, which allow the device to attach directly to the computer system bus. Maximum current required from the V_{CC} supply is 14Ø mA.

B.2 DCØØ4 I/O ADDRESS DECODER (Figures B-4, B-5, and B-6)

The protocol chip is a 2Ø-pin, Ø.762 cm (Ø.3ØØ in) center, DIP device. It functions as a register selector, providing signals necessary to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are included on the chip. An RC delay circuit slows the peripheral interface response to data transfer requests. The circuit is designed so that if tight tolerance is not required, only an external 1K 2Ø percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{CC} supply is 12Ø mA.

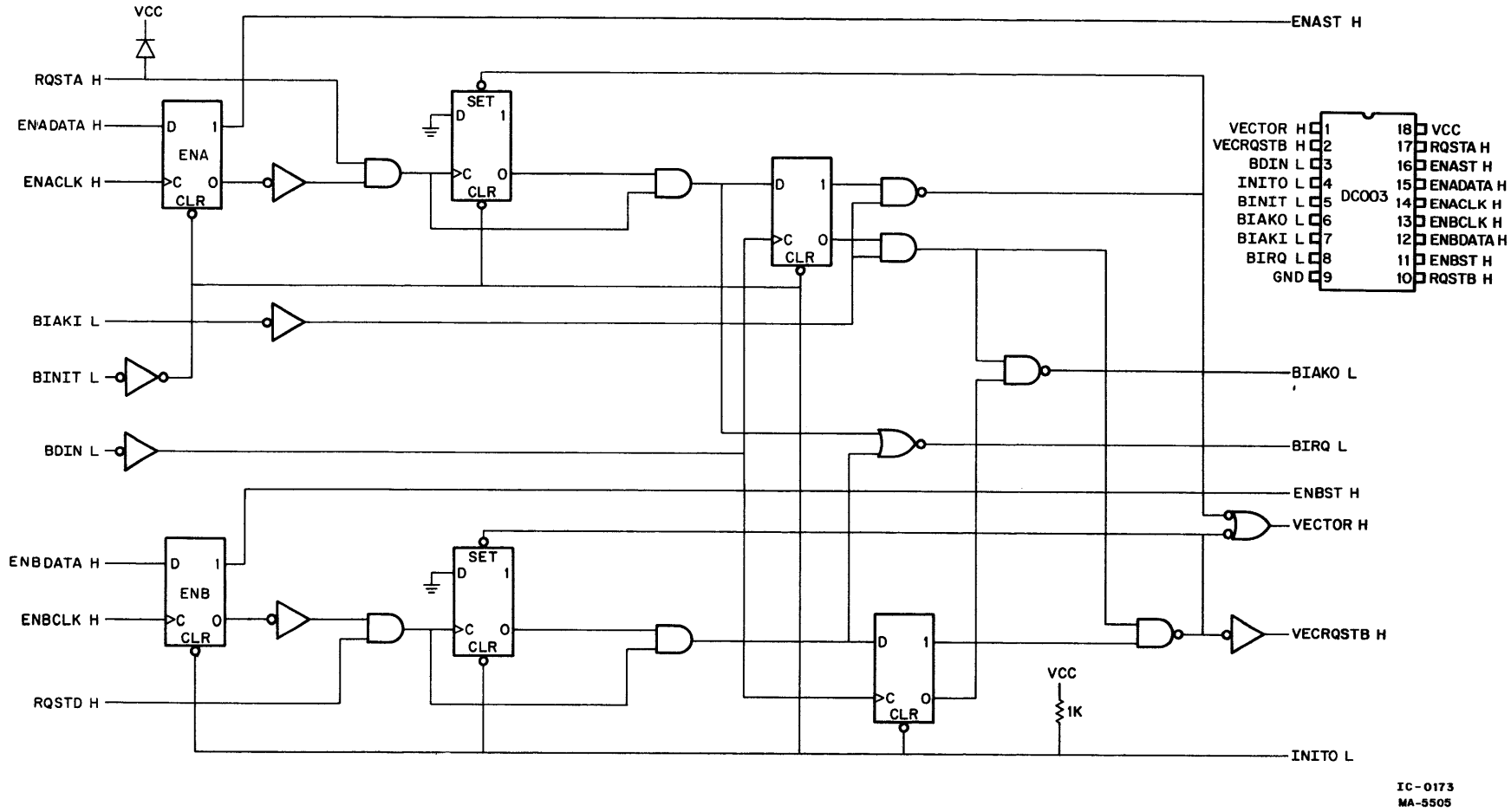


Figure B-1 DCØØ3 Simplified Logic Diagram

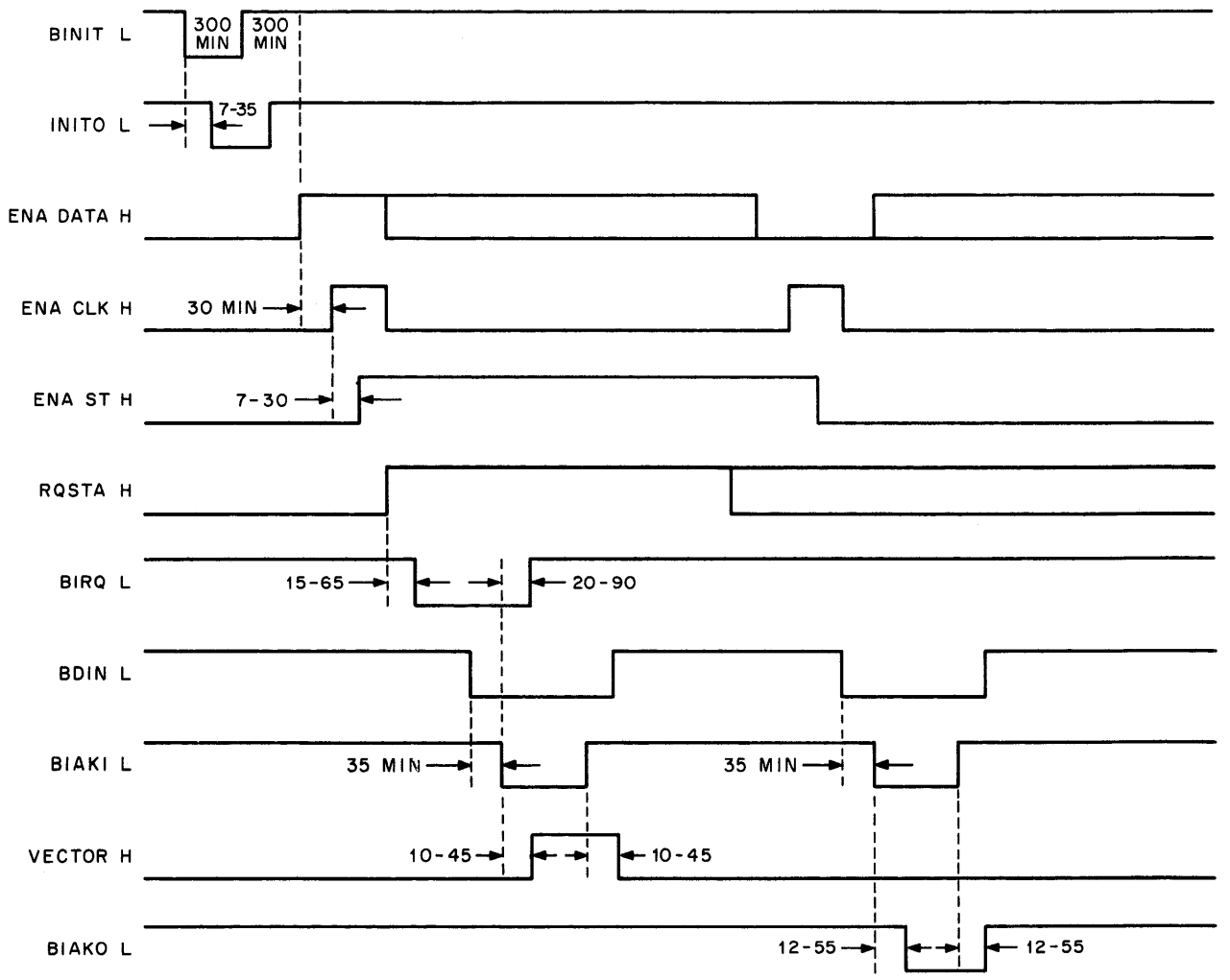
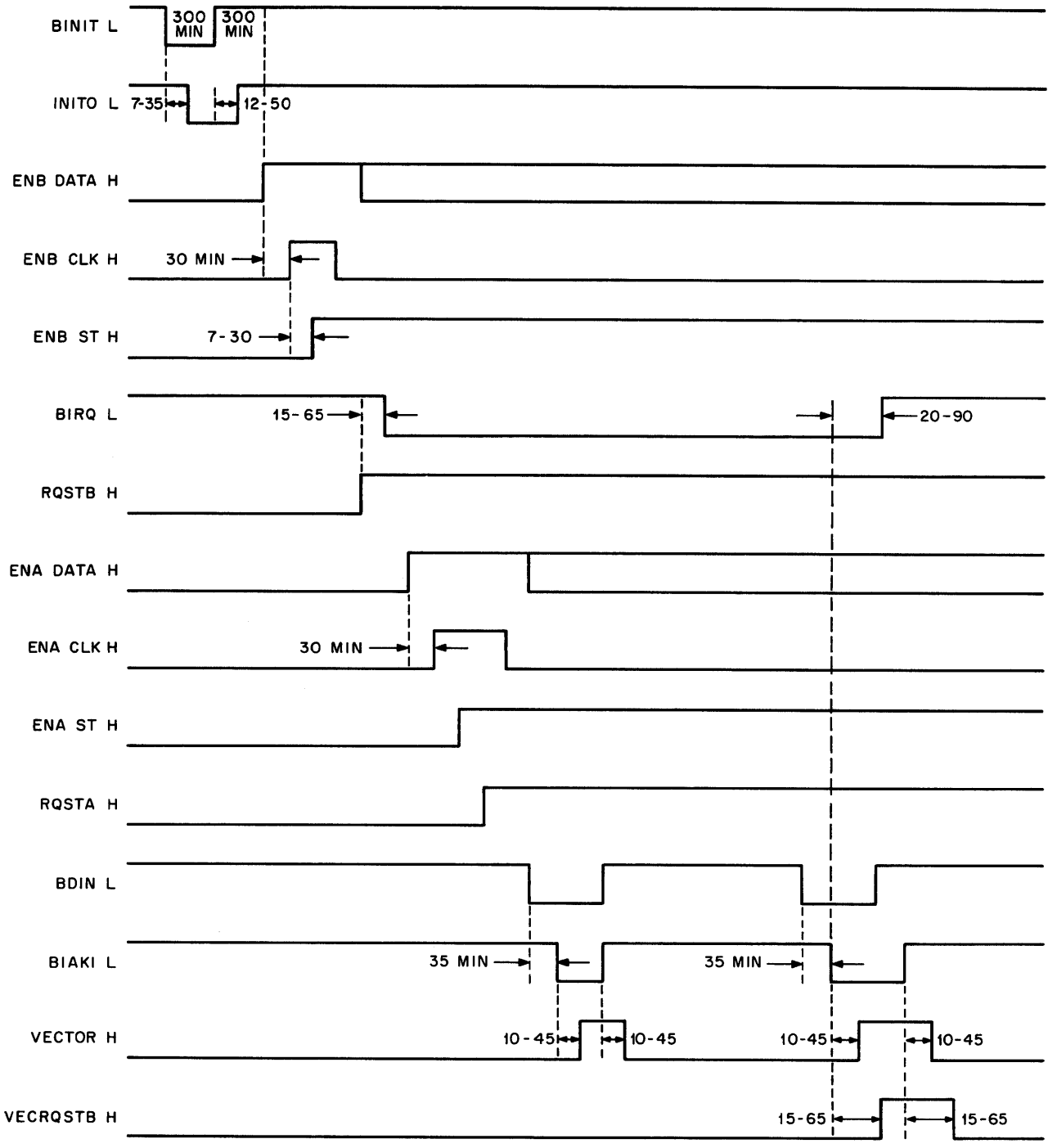


Figure B-2 DCØØ3 Interrupt Section Timing Diagram



NOTE:
Times are in nanoseconds

11-4151
MA-5502

Figure B-3 DCØØ3 Interrupt Section Timing Diagram Sections A and B

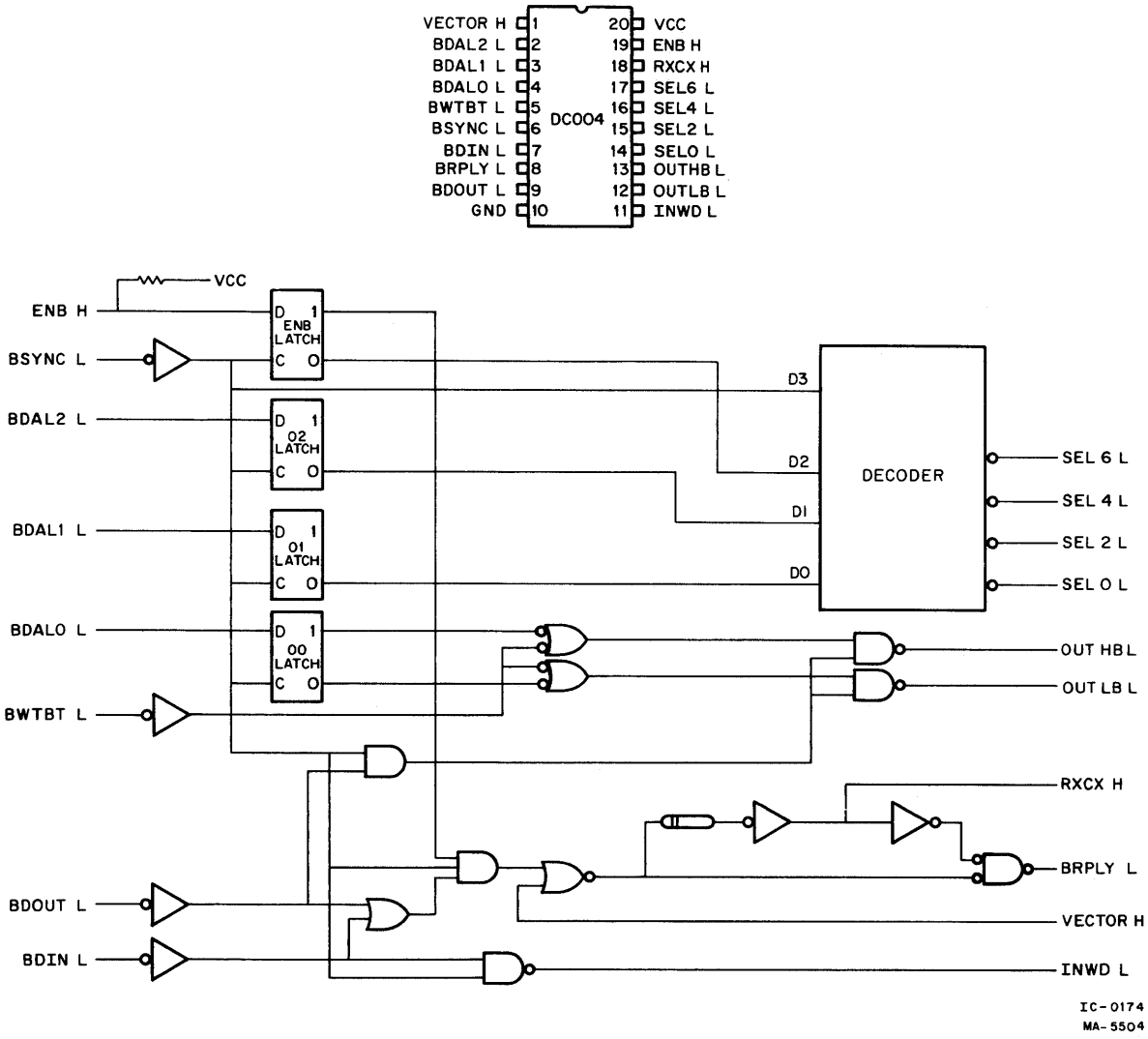
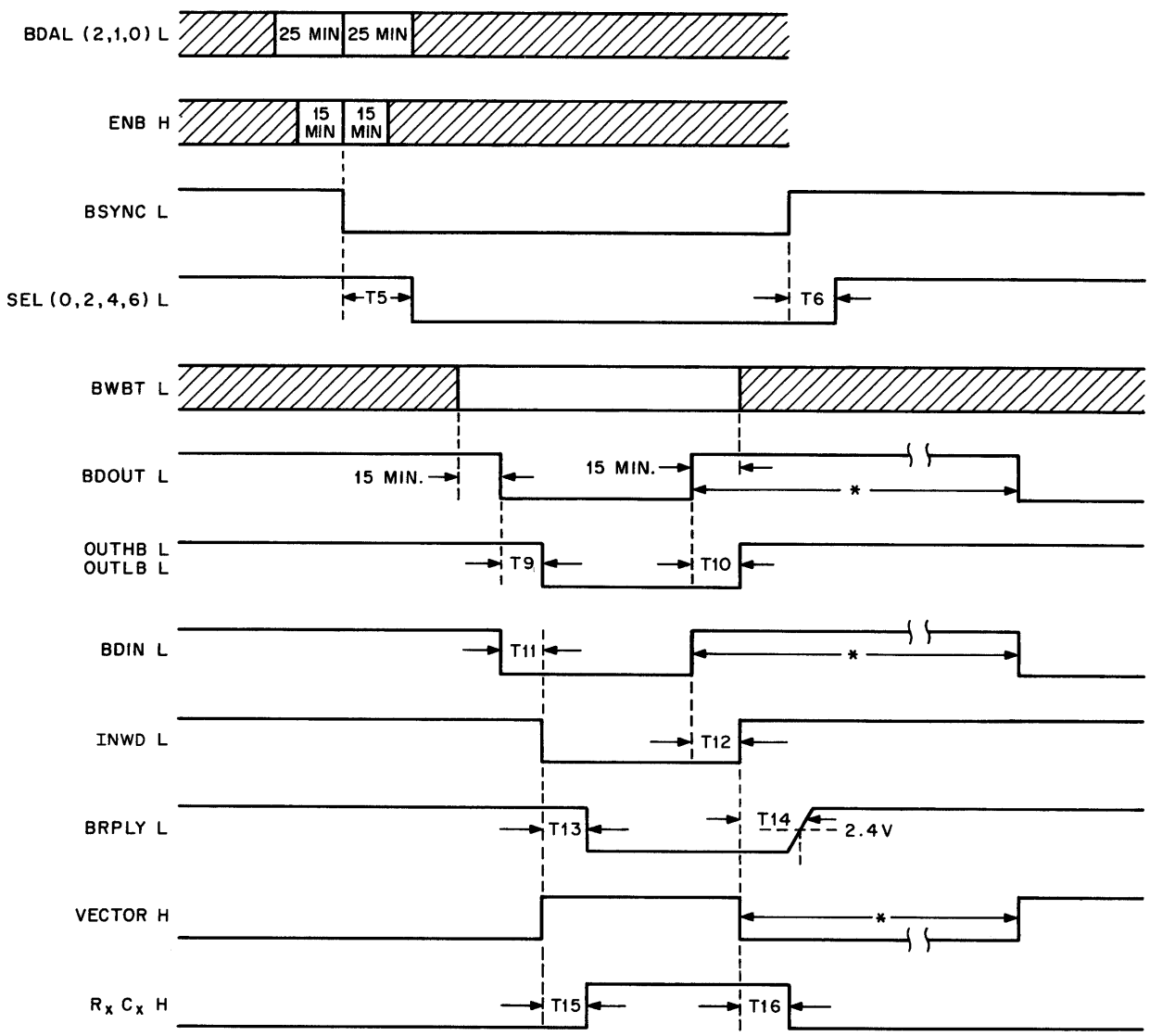


Figure B-4 DCØØ4 Simplified Logic Diagram



* TIME REQUIRED TO DISCHARGE $R_x C_x$ FROM ANY CONDITION ASSERTED = 150 ns

NOTE :
Times are in nanoseconds

11-4348
MA-5501

Figure B-5 DCØØ4 Timing Diagram

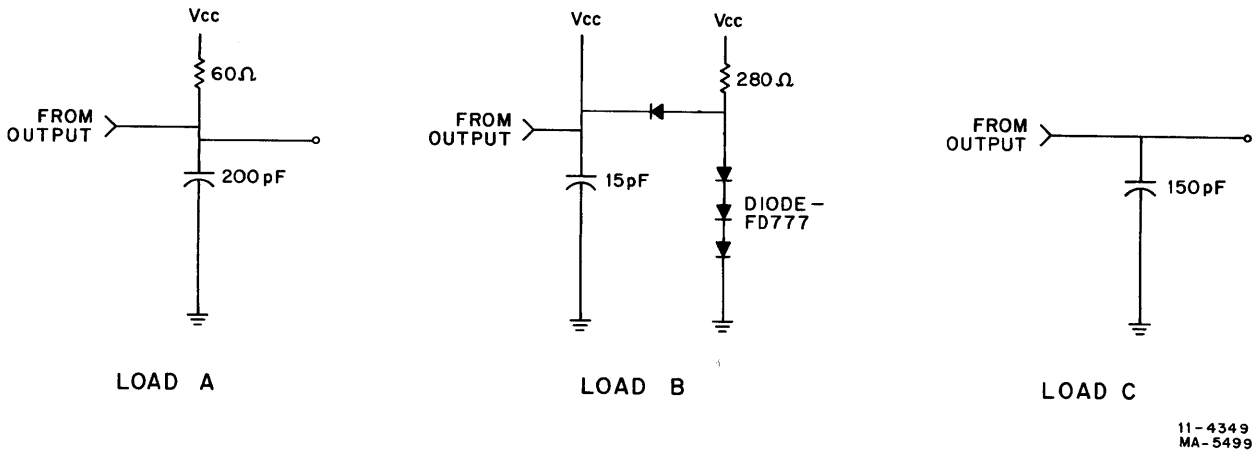


Figure B-6 DCØØ4 Loading Configurations

B.3 DCØØ5 BUS TRANSCEIVER (Figures B-7 and B-8)

The 4-bit transceiver is a 2Ø-pin, Ø.762 cm (Ø.3ØØ in) center, DIP, low-power Schottky device. Its primary use is in peripheral logic. In addition to the isolation function, the device also provides a comparison circuit for address selection and a constant generator, useful for interrupt vector addresses. The bus I/O port has high impedance inputs and high drive (7Ø mA) open collector outputs to allow direct connection to a computer's data bus. The peripheral side includes a bidirectional port, with standard TTL inputs and 2Ø mA three-state drivers. Data on this port is the logical inversion of the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs and to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wired-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disconnects that jumper from the address match, allowing for "don't care" address bits. In addition to the three address jumper inputs, a fourth high impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding control line action. Two control signals are decoded to give three operational states: receive data, transmit data, and disable. Maximum current required from the V_{CC} supply is 1ØØ mA.

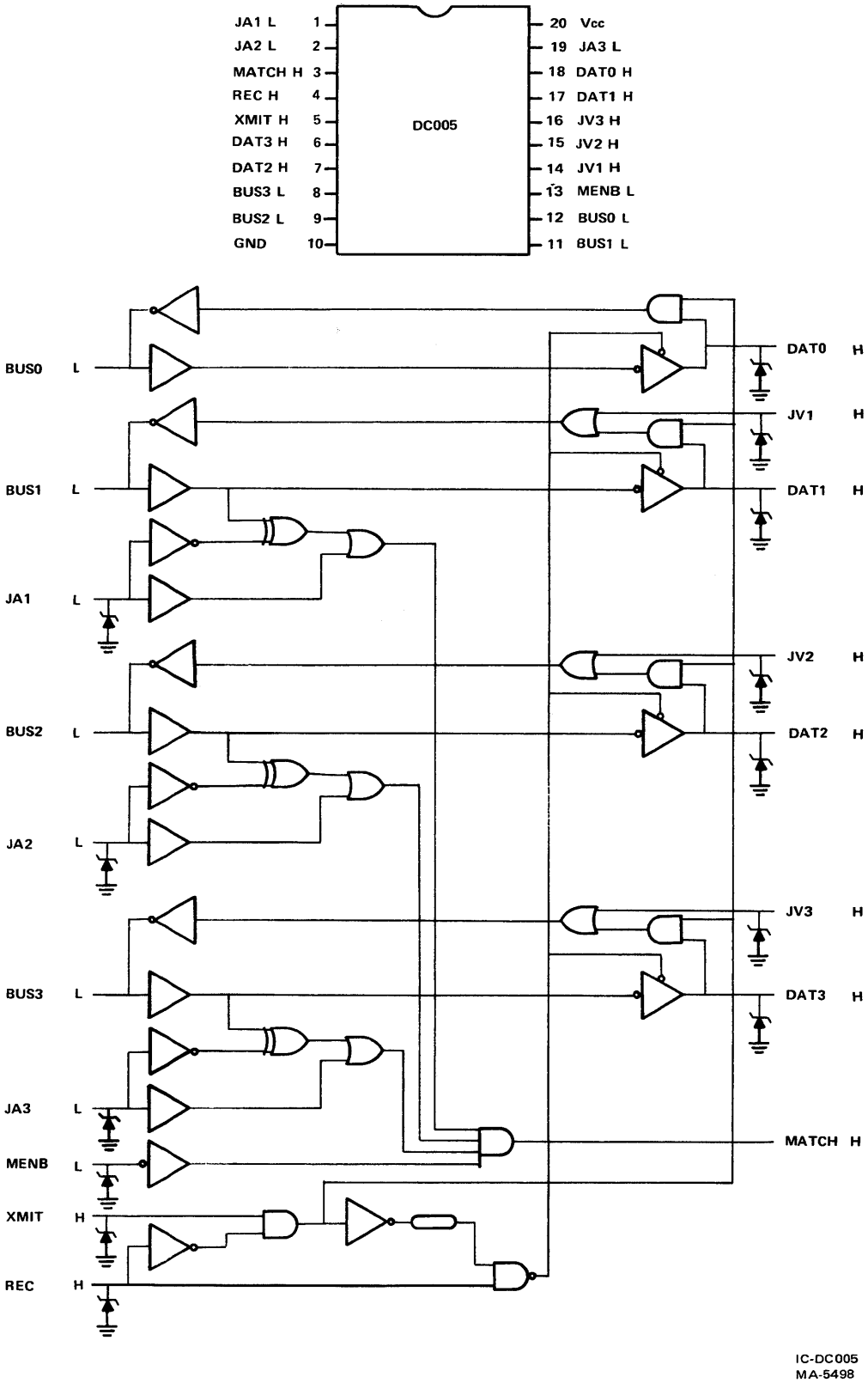


Figure B-7 DCØØ5 Simplified Logic Diagram

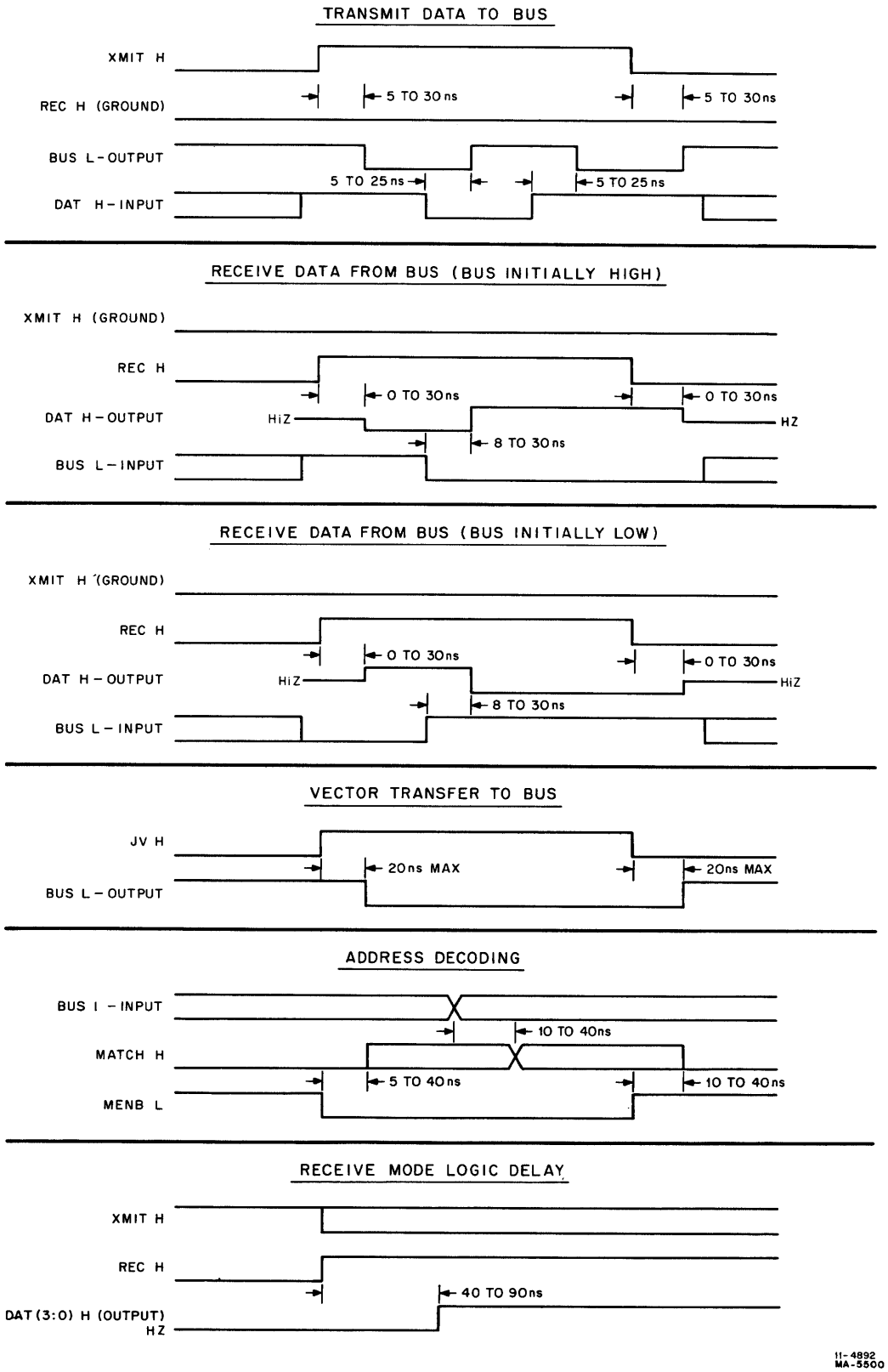


Figure B-8 DC005 Timing Diagram

APPENDIX C
PDP-11/23B BACKPLANE AND MODULE CONFIGURATION

C.1 GENERAL

LSI-11 systems can be either single or multi-backplane systems. If yours is a single backplane system (Figure C-1), observe the following three bus loading rules when configuring it.

C.2 SINGLE-BACKPLANE CONFIGURATION RULES

The following are the rules for single-backplane configuration.

1. The extended LSI-11 bus can support up to 20 ac loads; i.e., the processor has on-board termination for one end of the bus; after 20 ac loads, the other end of the bus must be terminated with 120 ohms.

2. The terminated bus can support up to 35 ac loads.

3. The bus can support up to 20 dc loads.

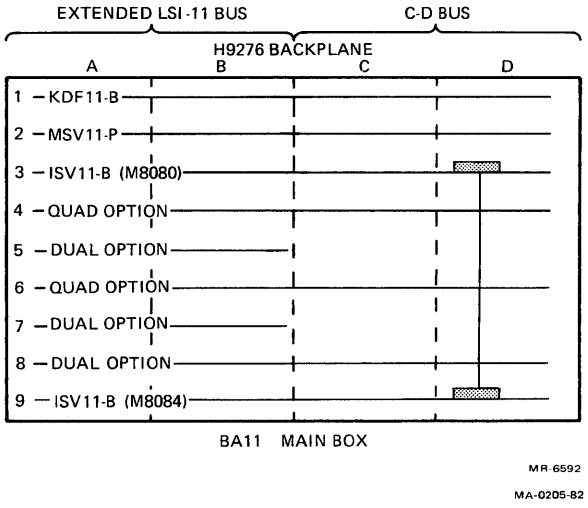


Figure C-1 PDP-11/23B (H9276) Single Backplane Configuration

If your system has more than one backplane (Figures C-2 and C-3), observe the following eight rules.

C.3 MULTIPLE-BACKPLANE CONFIGURATION RULES

The following are the rules for multiple-backplane configuration.

1. No more than three backplanes can be connected together.

2. No backplane can have more than 20 ac loads.

3. The total number of dc loads cannot be more than 20.

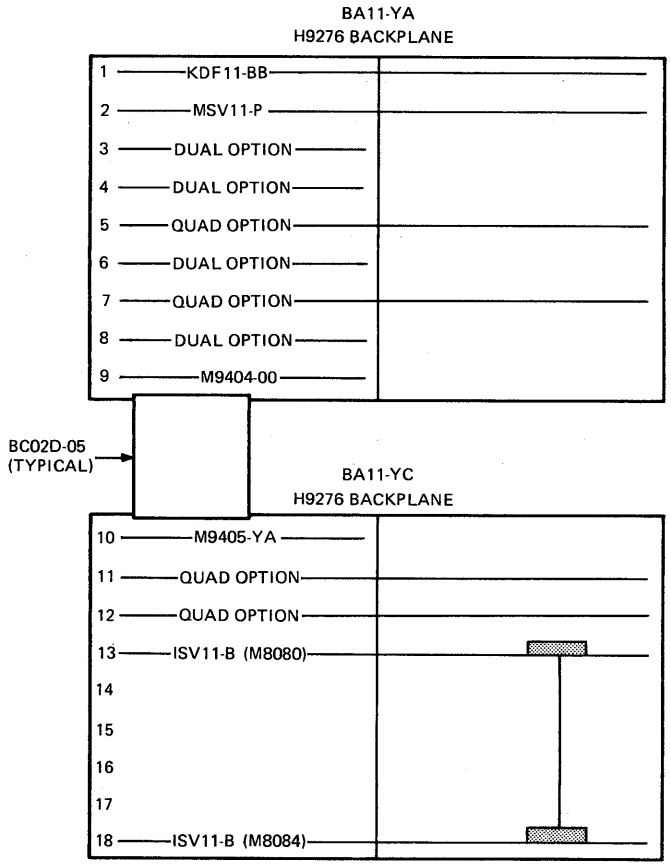
4. Both ends of the termination line (PDP-11/23B) must be terminated with 120 ohms; i.e., the first backplane must have an impedance of 120 ohms and the last backplane must have a termination of 120 ohms.

5. The cable connecting the first two backplanes (i.e., the main box and expander box 1) must be at least 150 cm (5 ft) long.

6. The cable connecting the backplane of expander box 1 to the backplane of expander box 2 must be at least 122 cm (4 ft) longer or shorter than the cable connecting the main box and expander box 1. A 305 cm (10 ft) length of cable is advised for ease of installation.

7. The combined length of both cables in the three-backplane system cannot exceed 488 cm (16 ft).

8. If the cables are customer-supplied, they must have a characteristic impedance of 120 ohms for the PDP-11/23B systems.



NOTES:
1. THE TOTAL DC LOADS OF BOTH BOXES CANNOT EXCEED 20.
2. EACH BC02D CABLE MUST BE AT LEAST 150 CM (5 FT) LONG, IF CONNECTED FROM THE MAIN BOX TO THE FIRST EXPANSION BOX.
3. EACH BC02D CABLE MUST BE AT LEAST 300 CM (10 FT) LONG, WHEN CONNECTED BETWEEN THE SECOND AND THIRD EXPANSION BOX.

MR-6594

MA-0201-82

Figure C-2 PDP-11/23B (H9276) Two Backplane Configurations

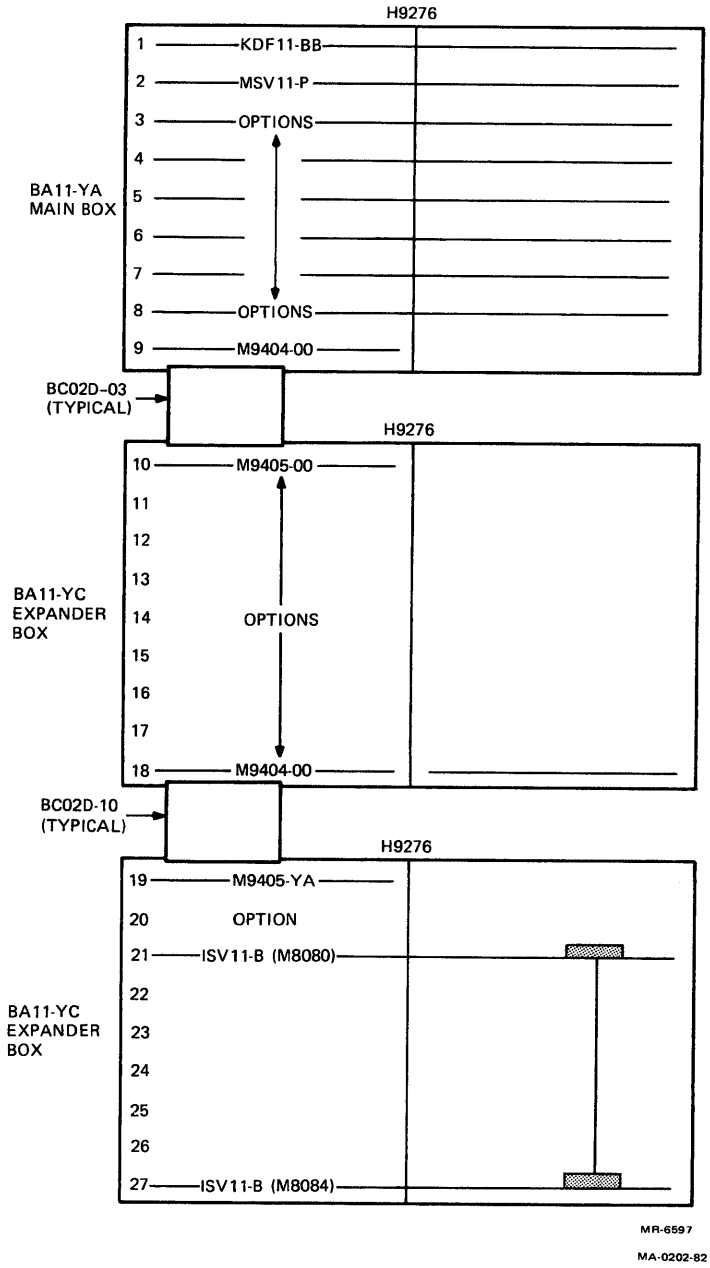


Figure C-3 PDP-11/23B (H9276) Three Backplane Configurations

Backplane configuration figures (Figures C-1 through C-3) are provided to help you follow these configuration rules. First, you must select which backplane configuration is best suited for a specific application. Use the backplane selector figures to determine this configuration.

The column layout of the backplanes makes it easy to establish interrupt and DMA priorities of the modules; i.e., the closer to the top of the column a module is placed, the higher the priority of the module. Furthermore, the column layout easily depicts the correct placement of cable and termination modules.

To configure an extended LSI-11 system, take the following steps.

1. Select the type of memory (MOS, PROM, or combination) needed for the specific application.

2. Select the CPU and memory combination most suited for the application (the PDP-11/23B uses a KDF11-B).

3. Select added memory, interface, and peripheral options needed.

4. Count the total number of module positions.

5. Count the total number of bus positions.

6. Select a backplane configuration that answers the module position requirement, the bus position requirement, and also provides sufficient expansion space.

7. Enter the option names in the backplane positions of the selected configuration.

8. Review the initial backplane configuration to determine if changes must be made.

9. If no changes are necessary, move to the appropriate backplane configuration table (Figures A-1 through A-3). Total the power consumption and the ac and dc loads. If any of these exceed the limits specified, modify the module configuration or use a new backplane configuration.

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