

LEGEND

NUMBER	VARIATION
RX78-PA	115V-60 HZ
RX78-PC	115V-50 HZ
RX78-PD	230V-50HZ
RX78-RA	115V-60 HZ
RX78-RB	115V-50 HZ
RX78-RD	230V-50 HZ
RX78-SA	115V-60 HZ
RX78-SC	115V-50 HZ
RX78-SD	230V-50 HZ
RX78-UA	115V-60 HZ
RX78-UC	115V-50 HZ
RX78-UD	230V-50 HZ
RX78-WA	115V-60 HZ
RX78-WD	230V-50 HZ

NOTE:

- MAKE 1/4 TURN TO THE RIGHT TO SECURE COVER (ITEM 5) TO BASE (ITEM 4)
- WASHERS SUPPLIED WITH SCREW LOCK ASSY (ITEM 1) ARE NOT USED.
- SET S1 ON M7744 (NOT APPLICABLE TO RX78-PA, PC, PD) AS FOLLOWS:

VARIATION	S1-1	S1-2	MOUSE
RX78-RA	OFF	OFF	RX02
RX78-RB	OFF	OFF	RX02
RX78-RD	OFF	OFF	RX02
RX78-SA	OFF	OFF	RX02
RX78-SC	OFF	OFF	RX02
RX78-SD	OFF	OFF	RX02
RX78-UA	ON	OFF	RX01
RX78-UC	ON	OFF	RX01
RX78-UD	ON	OFF	RX01
RX78-WA	OFF	ON	RX02
RX78-WD	OFF	ON	RX02

- INSTALL CABLE (ITEM 27) TO I/O BOARD (M7726 OR M7744). AT BOARD, CABLE MUST BE FOLDED APPROX 4 INCHES OUT FROM THE CONNECTOR AT 45° ANGLE FOR THE M7744 OR M7726 TO CLOSE PROPERLY.
- CONTROLLER BOARD SHOWN IN RAISED POSITION.

QTY	DESCRIPTION	REF
1	COVER	5
1	POWER CORD	1
1	CONTROLLER BOARD	13
1	I/O BOARD	14
1	FAN	15
1	SCREW	16
1	WASHER	17
1	SCREW	18
1	SCREW	19
1	SCREW	20
1	SCREW	21
1	SCREW	22
1	SCREW	23
1	SCREW	24
1	SCREW	25
1	SCREW	26
1	SCREW	27
1	SCREW	28
1	SCREW	29

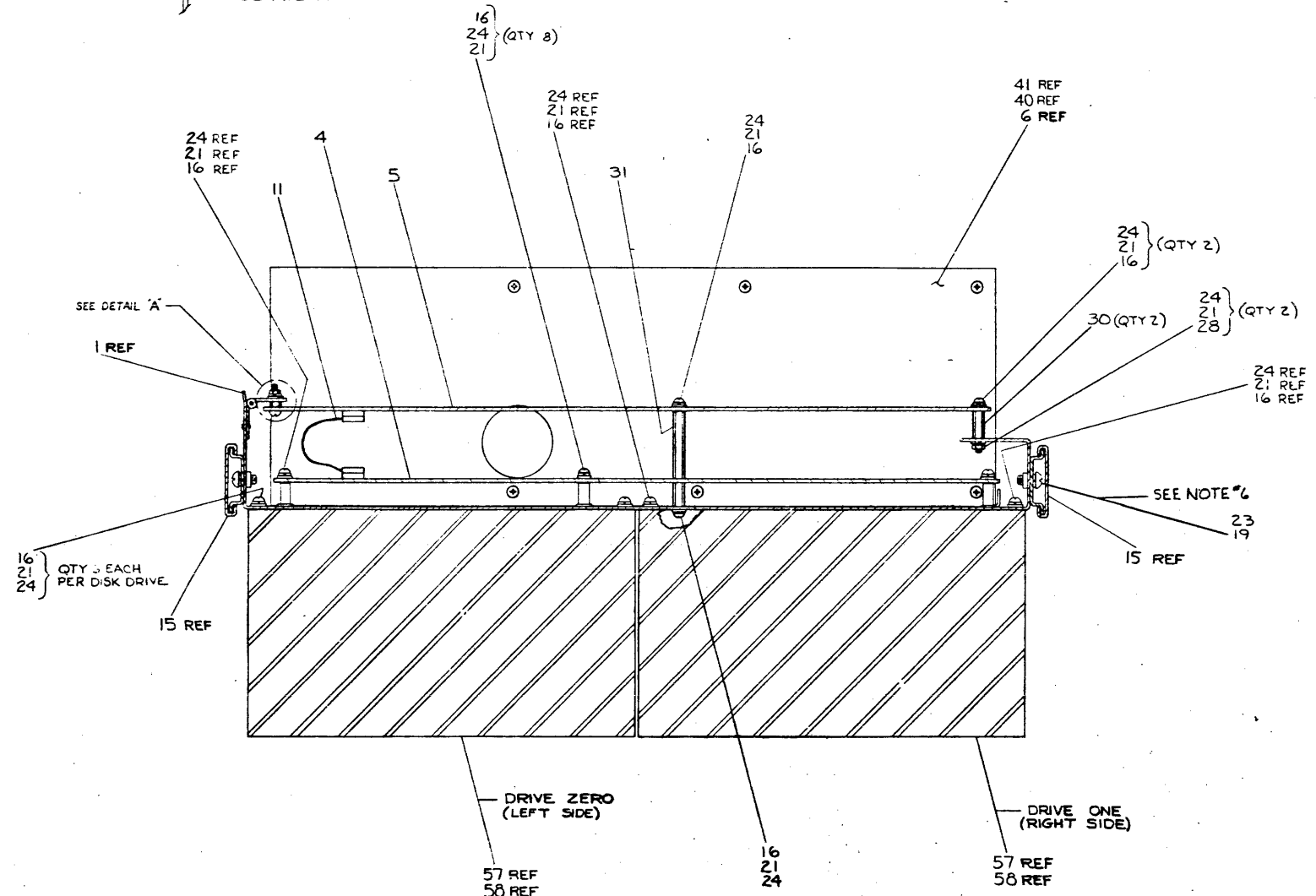
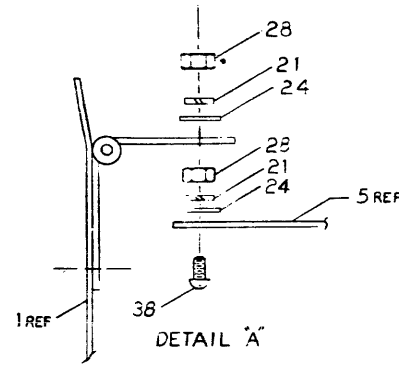
CAUTION: OFF SHEET PARTS LIST EXISTS, SEE K-PL-RX78-0-DBP.

DESCRIPTION	UNIT ASSY (RX78)
REV	1
DATE	11-17-77
BY	W. J. ...
CHECKED	...
APPROVED	...
SCALE	1:1
SEE PARTS LIST	...

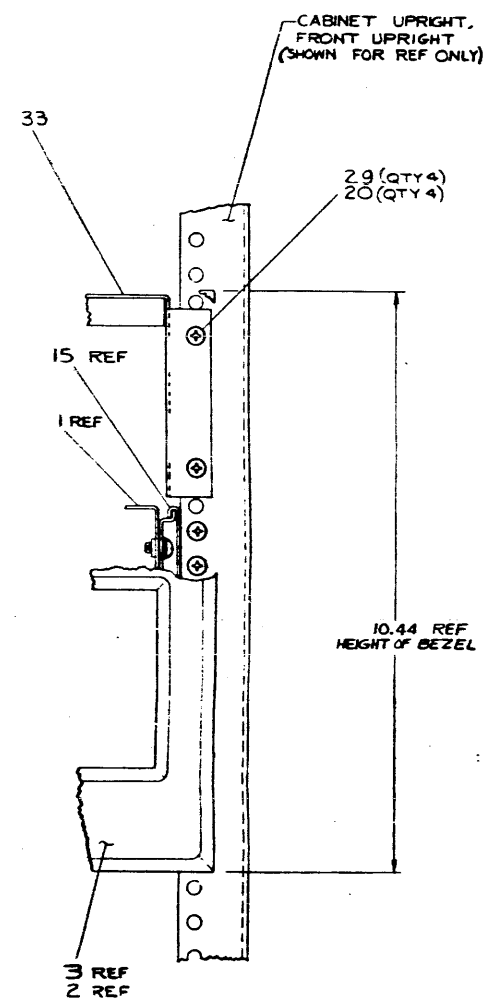
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DO NOT SCALE DRAWING

UNIT VARIATIONS	
RX01-LD	DUAL FLOPPY DISK SYSTEM 2.30V 50HZ (V1 8)
RX01-VA	SINGLE FLOPPY DISK SYSTEM FOR KC780 110V 60HZ
RX01-VC	SINGLE FLOPPY DISK SYSTEM FOR KC780 110V 50HZ
RX01-VD	SINGLE FLOPPY DISK SYSTEM FOR KC780 230V 50HZ



SECTION A-A
SCALE: NONE
SHOWN WITH 'TOP COVER'
(ITEM #33) REMOVED

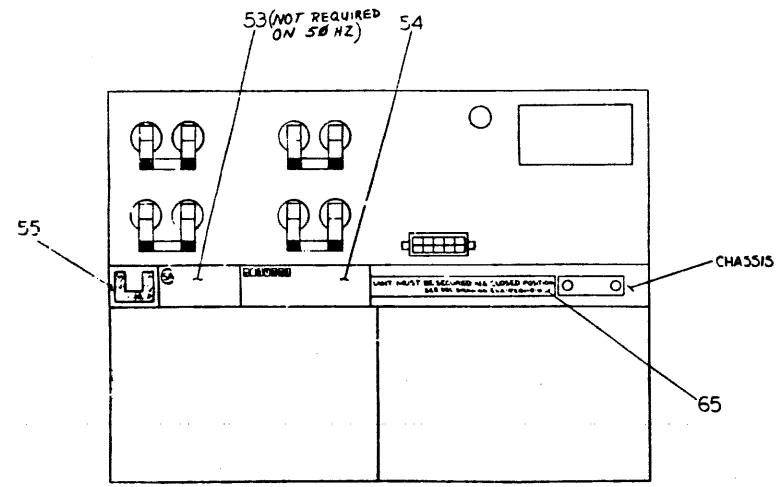
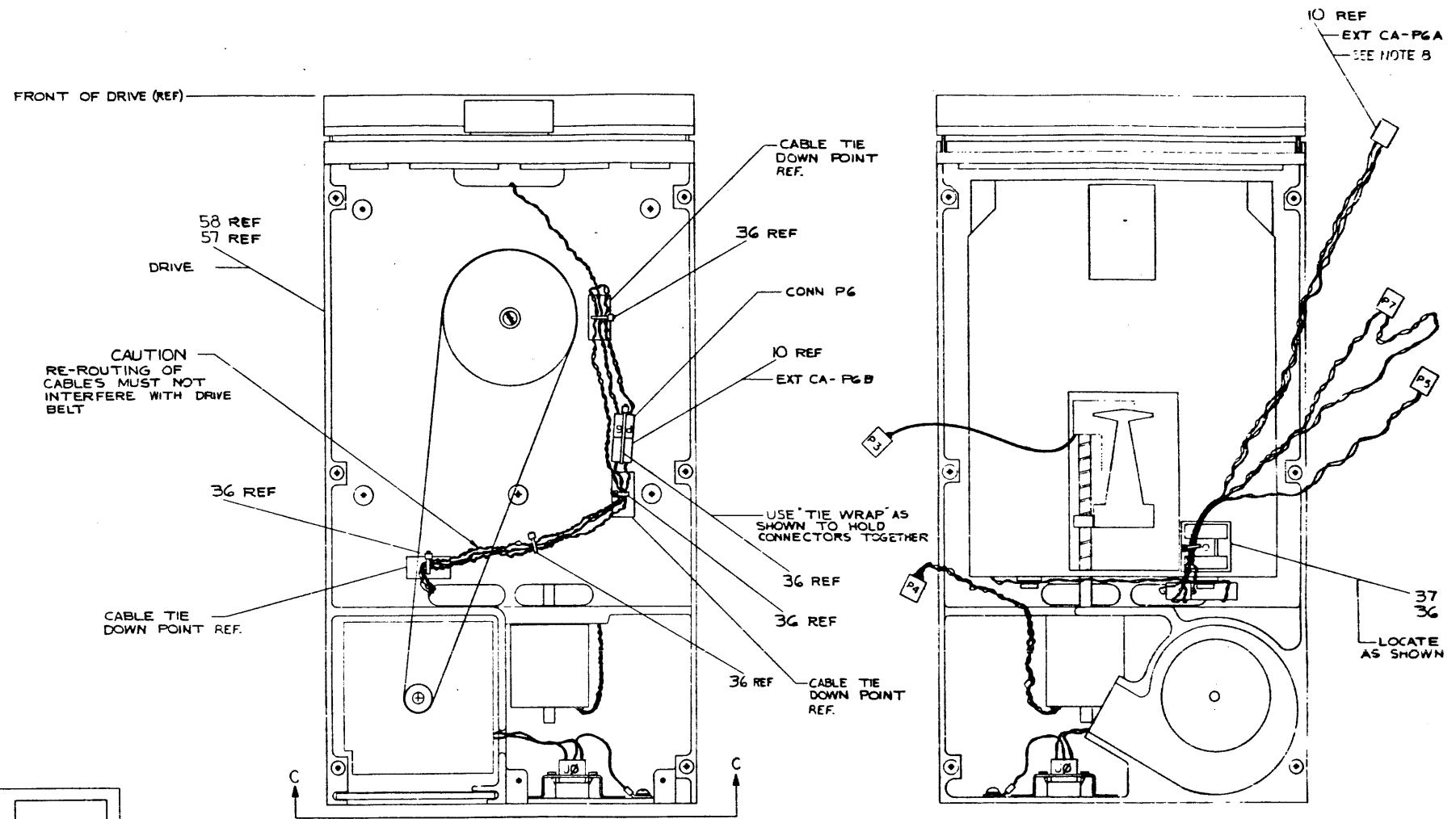


VIEW A-A
SCALE: NONE

REV	DATE	BY	CHK	CHG	NO.	SEC.

MODEL	RX01 FLOPPY DISK DRIVE ASSY	REV	001	NUMBER	EUA RX01-0-0	REV	
SCALE	NONE	SHEET	2 OF 3	DATE			

THIS DRAWING AND SPECIFICATIONS SHALL BE USED IN CONNECTION WITH THE INSTRUCTIONS FOR THE INSTALLATION OF THE RX01 FLOPPY DISK DRIVE ASSY.



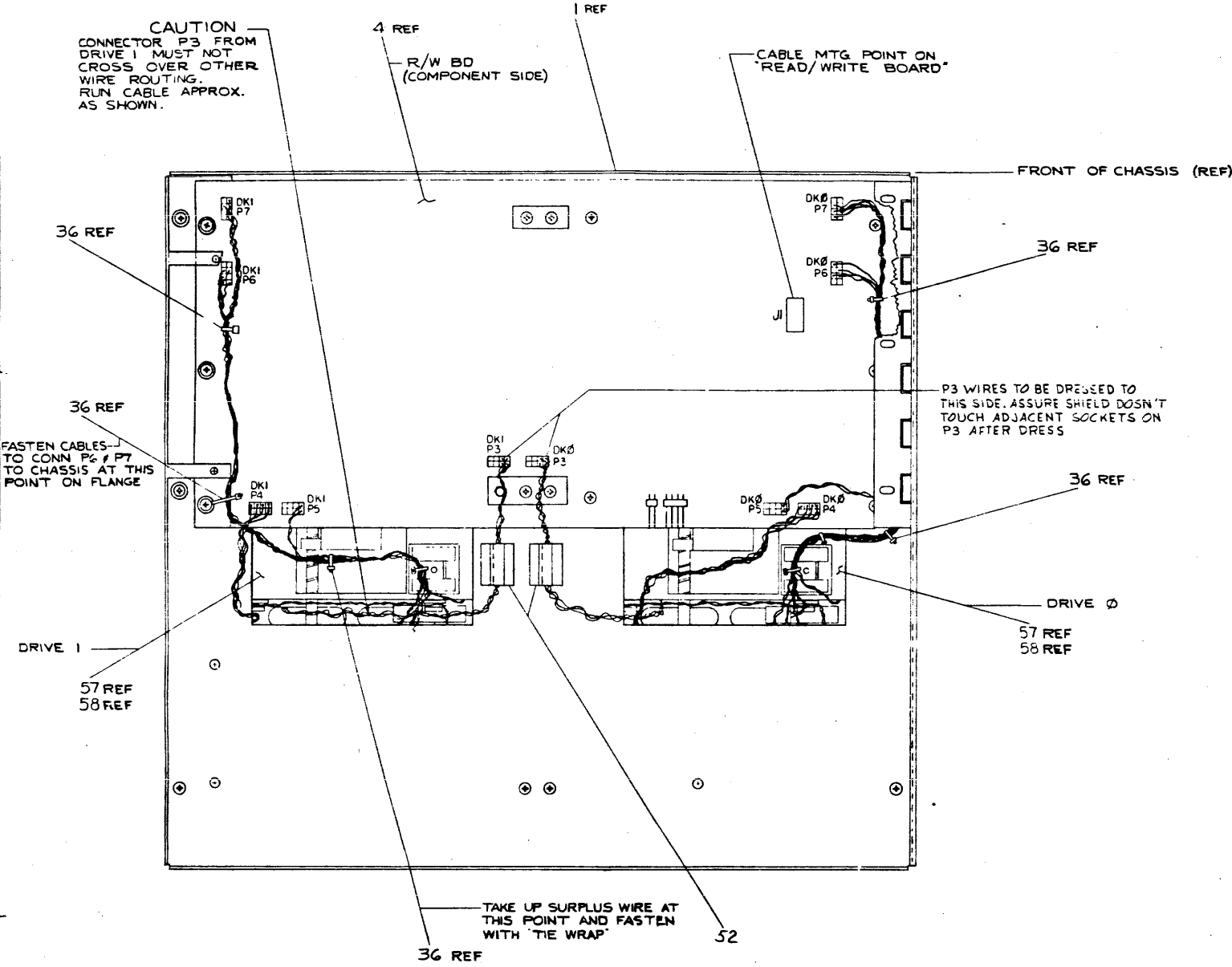
VIEW C-C
SCALE: NONE

BOTTOM VIEW OF "DISK DRIVE" (ITEMS "57+58")
WITH BOTTOM COVER REMOVED.
REPLACE BOTTOM COVER AFTER
RE-ROUTING OF CABLES.

TOP VIEW OF "DISK DRIVE" (ITEMS "57+58")
WITH TOP COVER REMOVED.
DO NOT REPLACE TOP COVER AFTER
RE-ROUTING OF CABLES.

WIRE RE-ROUTING
ALL CABLES MUST BE RE-ROUTED
AS SHOWN BEFORE INSTALLING THE
DRIVE INTO THE RX01 ASSY

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TOP VIEW OF CRITICAL WIRE ROUTING (SCALE: APPROX. 1/1)
 ALL WIRES FROM DRIVE 0
 DRIVE 1 MUST BE ROUTED AS SHOWN.

REVISIONS		DATE		BY		DESCRIPTION		PART NUMBER		REV	
RX01 FLOPPY DISK DRIVE ASSY SCALE: 1 SHEET 4 OF 5								EJA RX01-0-0		S	

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REV. NUMBER SIZE CODE PART NO. 2 | 1
 ↓ K SP RXØ1-Ø-2

B

B

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←

A

A

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1				
PARTS LIST				
DRN. <i>[Signature]</i>	DATE 19 FEB 76	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE FLOPPY CONTROLLER FIRMWARE		
CHK'D. <i>[Signature]</i>	DATE 19 FEB 76			
ENG. <i>[Signature]</i>	DATE 2/19/76			
PROJ. ENG. <i>[Signature]</i>	DATE 2/23/76			
PROD. <i>[Signature]</i>	DATE 2/23/76			
NEXT HIGHER ASSEMBLY				
SCALE		SIZE CODE	NUMBER	REV.
		K SP	RXØ1-Ø-2	
SHEET 1 OF 1		DIST.		

REV.	
CHANGE NO.	
CHK	

DEC FORM NO. DRB 109

4

3

2

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↑

/RX01 FLOPPY CONTROLLER FIRMWARE

/THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
/THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER

/00 INSTRUCTIONS

```

0002 SET#2
0000 CLR#0
0022 ONE#2
0000 ZERO#0
0000 IOB0#0
0004 IOB1#4
0010 IOB2#10
0014 IOB3#14
0020 IOB4#20
0024 IOB5#24
0030 IOB6#30
0000 INTERF=CLR IOB0
0002 DISK#SET IOB0

0004 ERR#IOB1
0010 XREQ#IOB2
0014 IOOUT#IOB3
0020 DONE#IOB4
0024 SHIFT#IOB5
0030 SECDAT#IOB6

0004 WGATE#IOB1
0010 STPHD#IOB2
0014 HDOLT#IOB3
0020 EGATE#IOB4
0024 LQ#CUR#IOB5
0034 UNIT#34
0040 UNHD#40
0042 LQ#D#42
0044 BAR#44
0001 LONG#1
0000 SHORT#0
0002 INCR#2

```

/INTERFACE=DISK BUSS OUTPUT BUFFER

/IOB0 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE

/SET=DISK

/INTERFACE BUFFER DEFINITIONS

/SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED

/SET TO REQUEST AN RX01 WORD TRANSFER

/DIRECTION FOR DATA LINE. SET=TO INTERFACE

/SET TO INDICATE RX01 READYNES TO ACCEPT A COMMAND

/SHIFT FOR DATA LINE

/SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE

/SET=SECTOR BUFFER CLR=SHIFT REGISTER MUST SIG BIT

/DISK BUFFER DEFINITIONS

/WRITE CURRENT ENABLE WHEN SET

/HEAD STEP, TWO PULSES REQUIRED FOR EACH TRACK

/DIRECTION OF HEAD MOTION

/ERASE CURRENT ENABLE

/SPECIFIES WRITE CURRENT LEVEL

/SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)

/DEACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE

/ACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE

/SECTOR BUFFER ADDRESS REGISTER CONTROL

/FORMAT: CLR BAR (SHORT)(LONG)

/SHORT PRESETS FOR COUNT OF 1024

/LONG PRESETS FOR COUNT OF 4096

/FORMAT: INCR BAR INCREMENT THE BUFFER ADDRESS REG.

/RX01 FLOPPY CONTROLLER FIRMWARE

PAL10 V142A 9-FEB-76

9117

PAGE 1 of 1

```

0050 WRTBUF#50
0003 START#3
0000 FIN#0
0054 CRC#54
0057 PRECRC#57
0055 DATCRC#55
0000 FLAG#60
0002 ON#2
0001 OFF#1
0003 TOG#3
0004 LSP#64
0070 LCT#70
0071 ESP#71
0073 ICT#73
0074 ROTATE#74
0075 LSR#75
0077 DATSR#77

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/SECTOR BUFFER WRITE CLOCK

/FORMAT: (START)(FIN) WRTBUF

/A 750NS MINIMUM PULSE IS REQUIRED

/CRC REGISTER CONTROL

/FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO

/BE JAMMED INTO CRC GENERATOR/CHECKER

/PRESETS CRC REG TO ALL ONES

/SHIFTS SEPERATED DATA INTO CRC CIRCUIT

/GENERAL PURPOSE FLAG CONTROL

/FORMAT: FLAG (ON)(OFF)(TOG)

/SET FLAG

/CLR FLAG

/TOGGLE FLAG

/LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG

/LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION

/LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD

/INCREMENT COUNTER

/SHIFT REGISTER CONTROL

/FORMAT: ROTATE(ONE)(ZERO)

/SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT

/WHILE INSERTING A ONE OR ZERO INTO THE LEAST

/SIGNIFICANT BIT

/LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER

/SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED

/DATA INTO LSA


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175 /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
176
177 /FORMAT: JUMP FX (IND)
178 /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
179 /SPECIFIED BY X. THE BRANCH ADDRESS IS TAKEN FROM
180 /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
181 /IF IND IS APPENDED, THE BRANCH ADDRESS
182 /IS TAKEN FROM THE OPEN SCRATCH PAD
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0202 JUMP#202

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0000 F0#0
0004 F1#4
0010 F2#10
0014 F3#14
0020 F4#20
0024 F5#24

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TABLE OF DEFINITIVE ERROR CODES

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0010 KXDV0#10 /DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
0020 KXDV1#20 /DRIVE 1 FAILED TO SEE HOME ON INITIALIZE. DOES NOT CAUSE ERROR
0030 KWRONG#30 /FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT
0040 KERRK#40 /TRIED TO ACCESS A TRACK GREATER THAN 76
0050 KHOMERR#50 /HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
0060 KSELFERR#60 /SELF DIAGNOSTIC ERR
0070 KXADR#70 /DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING
      /AT 52 HEADERS
0100 KAPROT#100 /WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
0110 KTIMER#110 /MORE THAN 40 MICROSECONDS AND NO SEPCLOCK SEEN
0120 KXPRAM#120 /A PREAMBLE COULD NOT BE FOUND
0130 KXIDAM#130 /PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
0140 KRCRCER#140 /CRC ERROR ON WHAT APPEARED TO BE A HEADER. ERROR IS NOT ASSERTED
0150 KTKSKER#150 /THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE
      /WITH THE DESIRED TRACK
0160 KXSTRYS#160 /TOO MANY TRIPS FOR AN IDAM
0170 KCDAM#170 /DATA AM NOT FOUND IN ALLOTTED TIME
0200 KDCRCER#200 /CRC ERROR ON READING THE SECTOR FROM THE DISK
0210 KPARER#210 /PARITY ERROR ON SOME WORD FROM THE INTERFACE

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220 /ROUTINE1 INITIALIZE) IF A HOST PROCESSOR INITIALIZE OR AN
221 /RX01 POWER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
222 /STOPS. UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
223 /INTERNAL DATA PATHS IS MADE. IF AN ERROR OCCURS HERE, ERROR AND
224 /DONE ARE SET, BUT ERREG IS NOT ALTERED. THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
225 /IS MADE TO RECALABRATE DRIVE 1 THEN DRIVE 0. IF DRIVE 0 FAILS TO RECALIBRATE,
226 /THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET. IF DRIVE
227 /0 RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
228 /IS READ INTO THE SECTOR BUFFER, IT IS POSSIBLE FOR A READ ERROR
229 /TO OCCUR WHILE READING THIS SECTOR.

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230
231 *0000          DECIMAL
232
233 0000 0210      OPEN ERREG          /CLEAR ERROR REGISTER
234 0001 0064      LSP
235
236 0002 0222      JUMP F4             /GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
237 0003 2352      TEST
238
239 0004 0070      TSTRN, LCT         /RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
240
241 0005 0004      4
242
243 0006 0075      LSR              /SET THE INIT DONE BIT OF STAT
244 0007 0214      OPEN STAT
245 0010 0064      LSP
246
247 0011 0070      LCT              /SET UP SOME SCRATCHPAD REGISTERS
248 0012 0377      -1
249 0013 0075      LSR              /UNIT 0 TO SOFT UNIT BIT
250 0014 0244      OPEN TEMPD
251 0015 0064      LSP              /NEG ZERO TO BOTH CURRENT TRACK ADDRESSES
252 0016 0200      OPEN CURTK0
253 0017 0064      LSP              /NEG ONE TO TARGET SECTOR
254 0020 0204      OPEN CURTK1
255 0021 0064      LSP              /SELECT DISK RUSS
256
257 0022 0074      ROTATE ZERO
258 0023 0224      OPEN TARSEC
259 0024 0064      LSP              /CALL SUBROUTINE TO LOAD HEAD AND WAIT 25 MS
260 0025 2220      OPEN TARTRK     /TO ALLOW POWER UP DRIVE SETTLE TIME
261 0026 0064      LSP
262
263 0027 0002      DISK
264
265 0030 0070      RECAL1, UNIT ONE /SELECT UNIT ONE FOR RECALIBRATE
266 0031 0034      RECAL0, CLM HDOUT /STEP HEAD IN 17 TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0
267
268 0032 2222      JUMP F4
269 0033 2145      DLY25
270
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275 0036 0070      LCT
276 0037 0365      -10-1
277 0040 0075      LSR
278 0041 0070      LCT
279 0042 0045      IN14
280 0043 0222      JUMP F4
281 0044 2100      STEPHD
282
283 0045 0226      IN14, JUMP F5   /ERROR, HOME WAS SEEN WHILE STEPPING IN,
284 0046 2621      WRONG
285
286 0047 0016      SET HDOUT
287 0050 0070      LCT
288 0051 0257      -80-1
289 0052 0075      LSR
290 0053 0070      LCT
291 0054 0060      RCALOK
292 0055 0040      UNHD
293 0056 0222      JUMP F4
294 0057 2100      STEPHD
295
296 0060 0202      RCALOK, JUMP F0  /HOME WAS FOUND OK
297 0061 0075      WHCHDR
298
299 0062 0174      BR FLAG0 F
300 0063 0070      NXDRV1
301
302 0064 0070      LCT
303 0065 0010      KHXDV0
304 0066 0226      JUMP F5
305 0067 2610      GOERDN
306
307 0070 0070      LCT
308 0071 0020      KHXDV1
309 0072 0075      LSR
310 0073 0210      OPEN ERREG
311 0074 0064      LSP
312
313 0075 0176      WHCHDR, BR FLAG0 T /IF FLAG0 BOTH DRIVES HAVE BEEN RECALIBRATED
314 0076 0372      PUNACL
315
316 0077 0062      FLAG ON
317
318 0100 0034      UNIT ZERO
319
320 0101 0202      JUMP F0
321 0102 0035      RECAL0

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322 /SUBROUTINE1 FINDTRACK)
323 /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR, IT PICKS
324 /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE, CHECKS THAT
325 /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL), MOVES THE
326 /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES THE
327 /TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
328 /THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED
329 /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER
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/SAVE THE RETURN ADDRESS
/CLEAR THE ERROR REGISTER
/SMART UNIT BIT TO SR
/IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
/IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
/DRIVE 2 IS DESIRED AND DRIVE1 WAS SELECTED, SELECT 0
/SET UP SOFT UNIT SELECT AS DRIVE 0
/GO STORE SOFT UNIT BIT
/IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
/DRIVE 1 IS DESIRED BUT DRIVE IS SELECTED, SELECT DRIVE 1
/SET UP SOFT UNIT SELECT BIT AS DRIVE 1
/STORE SOFT UNIT SELECT BIT
/CLR SOFT HD LOAD BIT BECAUSE UNITS CHANGED

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0103 0075 FINDTR, LSR
0104 0274 OPEN RTN
0105 0064 LSP
0106 0070 LCT
0107 0000 0
0110 0075 LSR
0111 0210 OPEN ERREG
0112 0064 LSP
0113 0244 OPEN TEMPD
0114 0071 ESP
0115 0075 LSR
0116 0122 BR SR7 ONE
0117 0127 UZERO
0120 0174 UONE, BR FLAG=0
0121 0141 USAME
0122 0034 UNIT ZERO
0123 0070 LCT
0124 0200 OCTAL
0125 0202 JUMP F0
0126 0134 UDIF
0127 0176 UZERO, BR FLAG=1
0130 0141 USAME
0131 0036 UNIT ONE
0132 0270 LCT
0133 0000 0
0134 0075 LSR
0135 0064 LSP
0136 0074 ROTATE ZERO

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```

/MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
/PUT THE TARGET SECTOR AWAY
/CALL GETWRD SURROUTINE FOR TRACK ADDRESS
/STASH THE TRACK ADDRESS
/START SETUP FOR COMPARING THE
/TARGET TRACK AND TRACK 76
/IF TARGET TRACK
/G= 77
/CALL SUBR "AGCOM TO SEE IF TARGET TRACK
/IS GREATER THAN 114 OCTAL, 76 DECIMAL.
/TARGET TRACK IS 77, ILLEGAL ADDRESS
/GO, REPORT THE ERROR
/TARGET TRACK IS GREATER THAN 77
/60, REPORT THE ERROR

```

```

432 0212 0240 OPEN TEMPO
433 0213 0071 ESP
434 0214 0075 LSR
435 0215 0200 OPEN CURTK0
436 0216 0002 DISK
437 0217 0122 BR SR7 ONE
438 0220 0222 *2
439 0221 0204 OPEN CURTK1
440 0222 0071 ESP
441 0223 0075 LSR
442 0224 0200 OPEN TEMPO
443 0225 0064 LSP
444 0226 0220 OPEN TARTRK
445 0227 0071 ESP
446 0230 0075 LSR
447 0231 0254 OPEN TEMPF
448 0232 0064 LSP
449 0233 0070 LCT
450 0234 0246 TRKEG
451 0235 0075 LSR
452 0236 0270 OPEN RTNA
453 0237 0064 LSP
454 0240 0226 JUMP F5
455 0241 2400 MAGCOM
460 0241 2400
461
462
463 LCT
464 KERTRK
465 JUMP F5
466 GOERDN
467
468
469
470 JUMP F0
471 NOSTEPS
472 OPEN RTNA
473 OPEN RTNA
474 OPEN RTNA
475 LCT
476 STPOUT
477 LSR
478 LSP
479
480 OPEN TEMPO
481 ESP
482 LSR
483
484 OPEN CURTK1
485 BR SR7 ZERO
486 0263 0126

```

```

487 0264 0266 *2
488 0265 0200 OPEN CURTK0
489
490 0266 0071 ESP
491 0267 0075 LSR
492
493 0270 0220 OPEN TARTRK
494 0271 0071 ESP
495
496 0272 0016 SET MOUT
497
498 0273 0226 JUMP F5
499 0274 2462 DIF
500
501
502 STPOUT, JUMP F0
503 0276 0302 *2
504
505 0277 0016 CLR MOUT
506
507 LCT
508 DUMSTP
509
510 UNHD
511 JUMP F4
512 0303 2222 STEPHD
513 0304 2100
514
515 0305 0226 JUMP F5
516 0306 2056 HOMERR
517
518 0307 0204 OPEN TEMPO
519 0310 0071 ESP
520 0311 0075 LSR
521 0312 0220 OPEN TARTRK
522 0313 0071 ESP
523
524 0314 0208 OPEN CURTK0
525 0315 0122 BR SR7 ONE
526 0316 0304 *2
527 0317 0204 OPEN CURTK1
528
529 0320 0075 LSR
530 0321 0064 LSP
531
532
533
534 M0SETL, OPEN TARTRK
535 0323 0071 ESP
536 0324 0075 LSR
537 0325 0254 OPEN TEMPF
538 0326 0064 LSP
539
540 0327 0070 LCT
541 0334 0323 *48-1

```

```

/TARGET TRACK IS OK, GET THE DRIVE
/SELECT FROM TEMPO
/PRESELECT UNIT 0
/SELECT DISK RU99
/WHICH UNIT SELECTED? BIT7#0 MEANS UNIT ONE
/ZERO, SKIP UNIT 1 SETUP
/PASS SELECTED CURRENT TRACK TO MAGCOM SUBR
/PASS TARGET TRACK TO MAGCOM SUBROUTINE
/CALL SUBROUTINE MAGCOM TO SEE IF TARGET
/IS SAME AS CURRENT TRACK, F#TARGET, G#CURRENT
/TRYED TO ACCESS A TRACK GREATER THAN 76 DECIMAL
/TARGET EQUALS THE CURRENT TRACK, NO
/STEPS ARE REQUIRED
/NOOP; TARGET > ACTUAL RETURN
/TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
/CF BOOT SUBROUTINE. SET UP RETURN FROM DIF SUBR
/SOFT UNIT SELECT BIT TO SR7
/PRESELECT UNIT 1
/SR7#0 MEANS UNIT ONE
/PASS SELECTED CURRENT TRACK TO DIFF SUBR VIA SR
/PASS TARGET TRACK TO DIF VIA CNTR
/ASSUME A STEP OUT
/GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED
/TARGET TRACK IS LESS THAN
/THE ACTUAL, MOVE OUT IS NECESSARY
/TARGET IS GREATER THAN ACTUAL. STEPS IN NEEDED
/COMPLEMENT OF STEPS REQUIRED IS IN THE
/SHIFT REG. SET UP RETURN FROM STPHD SUBR
/UNLOAD HEAD BEFORE MOVING
/CALL SUBROUTINE STEPHD
/HOME FOUND BEFORE LAST STEP TAKEN
/SOFT UNIT BIT TO SR7
/GET READY TO PASS TARGET TRK TO PROPER
/CURRENT TRACK
/OPEN PROPER CURRENT TRACK REGISTER
/BIT7#0 MEANS UNIT ONE
/UPDATE THE CURRENT TRACK ADDRESS
/HEAD IS SETTLE, DETERMINE IF ABOVE TRACK #3 DECIMAL
/PASS TARGET TO MAGCOM VIA TEMPF
/PASS #4 TO MAGCOM VIA TEMPF

```

```

542 0331 0075 LSR
543 0332 0260 OPEN TEMPG
544 0333 0064 LSP
545
546 0334 0026 /ASSUME TARGET GREATER THAN 43
547
548 0335 0070 LCT
549 0336 0344 ARV43
550 0337 0075 LSR
551 0340 0270 OPEN RTNA
552 0341 0264 LSP
553 0342 0226 JUMP F5
554 0343 2400 MAGCOM
555
556
557 0344 0202 ARV43, JUMP F0
558 0345 0346 .+1
559
560 0346 0202 JUMP F0
561 0347 0351 .+2
562
563 0350 0024 CLR LOWCUR
564
565 0351 0070 CF1ASE, LCT
566 0352 0355 RFINTR
567 0353 0206 JUMP F1
568 0354 0714 F1NDRE
569
570 0355 0274 RFINTR, OPEN RTN
571 0356 0207 JUMP F1 IND
572
573
574 0357 0250 /NO STEPS REQUIRED
575 0360 0071 /SOFT HEAD LOAD BIT TO SR7
576 0361 0075 LSR
577
578 0362 0122 /IS HEAD LOADFD?
579 0363 0322 /YES, GO UPDATE CURRENT CONTROL
580
581 0364 0070 /NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
582 0365 2322 /RETURN ADDR FROM DLY25 SUBROUTINE
583 0366 0222 JUMP F4
584 0367 2105 DLY25
585
586
587 0370 0212 PFUNCT, JUMP F2
588 0371 1236 /FUNCTION DECODE
589
590 0372 0226 PDNRCL, JUMP F5
591 0373 2625 /CHECK DONE AFTER RECALBRATE
592
593 0374 0000 /SPARE LOCATIONS
594 0375 0000 /OPEN
595 0376 0000 /OPEN
596 0377 0200 /OPEN

```

```

597
598 /ROUTINE: WRITE SECTOR)
599 /THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
600 /WRITES A PREAMBLE OF 6 BYTES OF ZERFS, A DATA OR DELETED DATA MARK,
601 /THEN TURNS ON ERASE GATE. ENTER WITH CNTR=100 IF
602 /DELETED DATA, CNTR=0 IF NORMAL DATA MARK. THE DATA MARK, DATA FIELD, CRC
603 /AND ONE BYTE POSTAMBLE ARE WRITTEN. WRITE CURRENT IS TURNED OFF.
604 /511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF. A HEADER MUST
605 /THEN BE READ TO INSURE DISK IS STILL UP TO SPEED BEFORE THE WRITE
606 /SECTOR FUNCTION IS COMPLETE.
607
608
609
610 0400 0214 WRTSEC, OPEN STAT /DEL DATA BIT TO STAT6
611 0401 0075 LSR
612 0402 0064 LSP
613
614 0403 0070 LCT
615 0404 0407 S*GATE
616 0405 0202 JUMP F0
617 0406 0103 F1NDTR
618
619 0407 0061 S*GATE, FLAG OFF /ALWAYS START WRITING WITH WRITE FLOP CLEARED
620
621 0410 0140 RP WRTEN F /GO REPORT ERROR IF NO WRITE ENABLE
622 0411 0503 PHTERR
623
624 0412 0214 OPEN STAT
625 0413 0071 ESP
626 0414 0006 SET *GATE
627 0415 0075 LSR
628 0416 0074 ROTATE ZERO
629
630 0417 0234 OPEN TEMPB /USE TEMPB FOR SECOND HALF DATA AM PATTERN
631
632 0420 0057 PRECRC /JAM THE CRC GENERATOR WITH FIRST 6 BITS OF DATA AM
633 0421 0056 CRC ONE
634 0422 0056 CRC ONE
635 0423 0056 CRC ONE
636 0424 0056 CRC ONE
637 0425 0056 CRC ONE
638 0426 0054 CPC ZERO
639
640 0427 0120 BR SR7 ZERO
641 0430 0460 DAMSUP /NO, REGULAR DATA MARK
642
643 0431 0070 LCT /YES, SECOND HALF OF DELETED DATA MARK TO CNTR
644 0432 0325 OCTAL /FLUX PATTERN
645
646
647
648 0433 0054 CRC ZERO
649 0434 0054 CRC ZERO
650 0435 0002 DISK
651 0436 0002 DISK

```

```

652 0437 0063 STASH, TOG FLAG
653 /END OF THE FIRST 0 BIT
654 0400 0075 LSR
655 0441 0064 LSP
656
657 0442 0070 LCT
658 0443 0466 HLFDLY
659 0444 0075 LSR
660
661 0405 0070 LCT
662 0406 0374 -2-1
663 0447 0073 ICT
664 0450 0124 BR COFL F
665 0451 0447 -2
666 0452 0002 DISK
667
668 0453 0070 LCT
669 0454 0351 -22-1
670
671
672 0455 0063 TOG FLAG
673 0456 0212 JUMP F2
674 0457 1322 WRT05
675
676
677 0460 0070 DAMSUP, LCT
678 0461 0337 OCTAL
679 337
680 DECIMAL
681
682 0462 0056 CRC ONE
683 0463 0056 CRC ONE
684
685 0464 0206 JUMP F1
686 0465 0437 STASH
687
688 0466 0072 HLFDLY, DISK
689
690 0467 0070 LCT
691 0470 0514 WRTDAM
692 0471 0075 LSR
693
694 0472 0070 LCT
695 0473 0351 -22-1
696 0474 0070 LCT
697 0475 0351 -22-1
698
699 0476 0070 LCT
700 0477 0351 -22-1
701
702 0500 0063 TOG FLAG
703 0501 0212 JUMP F2
704 0502 1322 WRT05
705
706

```

```

707 0503 0070 PRTRERR, LCT
708
709 0504 0010 OCTAL
710 12
711 0505 0075 DECIMAL
712 0506 0214 LSR
713 0507 0064 OPEN STAT
714
715 0510 0070 LCT
716 0511 0100 WRTDAM
717 0512 0226 JUMP F5
718 0513 0010 GSERON
719
720
721
722
723
724
725
726
727
728 0514 0070 WRTDAM, LCT
729 0515 0375 -2-1
730 0516 0075 ICT
731 0517 0075 LSR
732 0520 0124 BR COFL F
733 0521 0516 -3
734
735 0522 0063 TOG FLAG
736
737 0523 0070 LCT
738 0524 0352 OCTAL
739 0525 0075 DECIMAL
740 0526 0070 LCT
741 0527 0376 -7-1
742 0530 0062 DISK
743
744 0531 0120 AGAIN, BR SR7 ZERO
745 0532 0502 A
746
747 0533 0300 CLR BAR
748 0534 0063 TOG FLAG
749 0535 0126 ABACK, BR COFL T
750 0536 0503 SECHLF
751 0537 0070 ROTATE
752 0540 0073 ICT
753
754
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759
760
761

```

THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A DELETED DATA MARK. THE FIRST HALF OF BOTH MARKS ARE IDENTICAL. THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY PUTTING THE SECOND HALF BIT PATTERN IN TEMPB

```

/WASTE 2.0 MICRO SECONDS
/SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
FOR A WRITE PROTECTED DISKETTE
/ERROR CODE FOR WRT PROTECT ERROR
/WRITE A CLOCK BIT AS END OF 48TH ZERO
/FIRST HALF OF DATA MARK PATTERN TO SR
/SET TRANSITION LOOP COUNTER FOR 0 LOOPS
/NOOP
/WHAT'S THE BIT?
/ZERO, NO TRANSITION
/ONE, RESET THE BUFFER ADDR REG TO 0
/WRITE FLUX TRANSITION
/CHECK TRANSITION LOOP COUNT
/GO GET SECOND HALF
/SHIFT NEXT TRANSITION TO SR7
/BUMP TRANSITION LOOP COUNTER

```

```

762 0541 0206 JUMP F1
763 0542 0531 AGAIN
764
765 0543 0234 /SECOND HALF OF DATA MARK TO SR
766 0544 0071 ESP
767 0545 0075 LSR
768
769 0546 0070 LCT
770 0547 0370 -7-1
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814
815
816
0550 0120 /SMALL WE WRITE A TRANSITION?
0551 0564 /NO
0552 0063 /YES
0553 0002 /NOOP
0554 0126 /DONE DATA MARK?
0555 0566 /YES, GO WRITE DATA
0556 0073 /NO, BUMP THE LOOP COUNTER
0557 0074 /BRING UP NEXT HALF BIT TO SR7
/DO ANOTHER LOOP
0560 0206 JUMP F1
0561 0550 AGAINI
0562 0206 A, JUMP F1
0563 0535 ABACK
0564 0206 B, JUMP F1
0565 0554 BBACK

```

/THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.

```

800
801
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815
816
0566 0022 /TURN ON ERASE CURRENT AT START OF DATA FIELD
0567 0073 /NOOP, WASTE 2 CYCLES
0570 0073 /NOOP
0571 0170 /WHAT'S THE DATA BIT?
0572 0615 /ZERO, GO WRITE NOTHING
0573 0056 /ONE, UPDATE THE CRC WITH 1
0574 0063 /WRITE A DATA TRANSITION
0575 0073 /NOOP FOR BIT CELL TIMING
0576 0162 /DONE ENTIRE SECTOR?
0577 0624 /YES, GO WRITE THE CRC
0620 0046 /NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

```

```

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868
869
870
871
0601 0070 LCT
0602 0376 -2
0603 0073 ICT
0604 0124 9R COFL F
0605 0622 SELFER
0606 0063 /WRITE A CLOCK TRANSITION
0607 0074 LCT
0608 0377 -1
0609 0124 9R COFL F
0610 0620 SELFER
0611 0206 JUMP F1
0612 0571 DATA
0615 0054 C, CRC ZERO
0616 0206 JUMP F1
0617 0576 CRACK
0620 0070 SELFER, LCT
0621 0260 /SELFER
0622 0226 JUMP F5
0623 0610 GGERDN
0624 0070 /RTCRC, LCT
0625 0357 -16-1
0626 0075 LSR
0627 0072 /DISK
0628 0120 9R SR7 ZERO
0631 0020 SELFER
0632 0063 /WRITE A CLOCK TRANSITION
0633 0076 /NOOP WASTE 6 CYCLES WITH MORE SELFTEST
0634 0076 /NOOP
0635 0076 /NOOP
0636 0076 /NOOP
0637 0122 9R SR7 ZERO
0640 0620 SELFER
0641 0130 /WHAT IS THE CRC BIT
0642 0653 /ZERO, DO NOT WRITE ANYTHING
0643 0056 /ONE, BRING UP THE NEXT BIT
0644 0063 /WRITE A DATA TRANSITION

```

/THIS ROUTINE WRITES THE 16 BIT CRC GENERATED FOR THE PRECEDING DATA FIELD.

/A SELF DIAGNOSTIC HAS FAILED

```

072 0645 0076 ROTATE ONE /NOOP
073 0646 0073 DBACK, ICT /BUMP THE BIT COUNTER
074 0647 0126 BR COFL T /DONE CRC YET?
075 0650 0656 WRT0ST /YES, GO WRITE A POSTAMBLE
076 0651 0206 JUMP F1 /NO, GO WRITE ANOTHER CRC BIT
077 0652 0627 E
078 0653 0054 0, /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
079 0654 0206 JUMP F1
080 0655 0646 DBACK
081
082
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```

/THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
/WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
/CURRENT, IT UTILIZES THE WRITE ZEROES SUBROUTINE.

```

0656 0070 *RTPST, LCT /SETUP TO CALL *RT0S TO WRITE 8 BITS OF ZEROES
0657 0666 CEGATE
0660 0075 LSR
0661 0070 LCT
0662 0367 -0-1
0663 0063 TOG FLAG /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
0664 0212 JUMP F2 /CALL THE SUBROUTINE WRITE ZEROES
0665 1322 *RT0S
0666 0004 CEGATE, CLR *GATE /DISABLE WRITE CURRENT
0667 0070 LCT /CALL *RT0S FOR 127 BITS (511.2 MICRO SEC)
0672 0676 CEGATE /DELAY TO ERASE TURN OFF
0671 0075 LSR
0672 0070 LCT
0673 0200 -127-1
0674 0212 JUMP F2
0675 1322 *RT0S
0676 0022 CEGATE, CLR EGATE /DISABLE ERASE CURRENT
0677 0070 LCT /CALL *RT0S FOR 25 BIT (101 MICRO SEC) DELAY
0732 0726 READOK /BEFORE TRYING TO READ
0781 0075 LSR
0782 0070 LCT
0783 0346 -25-1
0784 0212 JUMP F2
0785 1322 *RT0S
0786 0070 READOK, LCT /CALL FIND HEADR ROUTINE TO INSURE

```

```

927 0707 0712 GODDLE
928 0710 0216 JUMP F3
929 0711 1400 FINDHD
930
931 0712 0212 GODDNE, JUMP F2 /WRITE SECTOR FUNCTION IS COMPLETE
932 0713 1006
933
934
935
936
937
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981

```

/(SUBROUTINE FINDSECTOR)
/SUBROUTINE TO FIND A SPECIFIC SECTOR, ENTER WITH RETURN ADDRESS
/IN CHPT, DESIRED TRACK ADDRESS IN TRK AND DESIRED SECTOR ADDRESS
/IN TAHRSC, THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
/BEEN REACHED.

```

0714 0270 FINDSE, OPEN RTNA /SAVE RETURN ADDRESS
0715 0075 LSR
0716 0064 LSP
0717 0260 OPEN TEMPG /PRESET SECTOR TRY COUNT TO 52 TRIES
0720 0070 LCT
0721 0313 -52-1
0722 0075 AGAIN2, LSP /STORE SECTOR TRY COUNT
0723 0064 LSP
0724 0070 LCT /CALL SUBROUTINE TO FIND A HEADER
0725 0730 CHKSEC
0726 0216 JUMP F3
0727 1400 FINDHD
0730 0174 CHKSEC, BR FLAGO ZERO /CORRECT SECTOR? FLAG=1 IF NO
0731 0743 WAIT /YES, GO WAIT FOR PREAMBLE
0732 0260 OPEN TEMPG /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
0733 0071 ESP
0734 0073 ICT
0735 0124 BR COFL F /52 TRIES MADE FOR SECTOR YET?
0736 0722 AGAIN2 /NO, TRY ANOTHER SECTOR
0737 0070 LCT /YES, CANN'T FIND THE SECTOR
0740 0070 *XHDR
0741 0226 JUMP F5
0742 0610 GOERDN
0743 0070 LCT /STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
0744 0345 -26-1
0745 0073 ICT
0746 0124 BR COFL F
0747 0745 *-2
0750 0073 ICT
0751 0124 BR COFL F
0752 0750 *-2
0753 0073 ICT

```

```

982 0754 0124 BR COFL F
983 0755 0753 *-2
984
985 0756 0270 /RETURN FROM THIS SUBROUTINE AT WRITE TURN ON TIME
986 0757 0203 /OF THE DESIRED SECTOR
987
988
989
990
991 /([ROUTINE: READ SECTOR])
992
993 RDSEC, ROTATE ZERO /ZERO THE STAT
994 ROTATE ZERO
995 OPEN STAT
996 LSP
997
998 /CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR
999 LCT
1000 GOREAD
1001 JUMP F0
1002 FINDTR
1003
1004 GOREAD, JUMP F4 /GO READ THE DATA FIELD
1005 READ
1006
1007 0 /OPEN FREE LOCATIONS
1008 0 /OPEN
1009 0 /OPEN
1010 0 /OPEN
1011 0 /OPEN
1012 0 /OPEN

```

```

1012 /([ROUTINE: DONE AND ERROR DONE])
1013
1014
1015 EPDONE, CLR DONE
1016 CLR XREG
1017
1018 INTERF /SELECT INTERFACE BUSS
1019
1020 SET ERR /ASSERT ERROR LINE
1021
1022 JUMP F2 /SKIP NEXT INSTRUCTION
1023 *-2
1024
1025 OKDONE, CLR ERR /NEGATE ERROR LINE
1026
1027 OPEN STAT /OPEN STAT TO MOVE TO INTERFACE
1028
1029 ESP /STAT OR ERREG TO SR
1030 LSR
1031
1032 CLR SHIFT /CLEAR INTERFACE OUTPUT BUFFER
1033 CLR DONE
1034 CLR XREG
1035
1036 INTERF /SELECT INTERFACE OUTPUT BUSS
1037
1038 CLR SECDAT /SELECT SR AS DATA LINE SOURCE
1039
1040 SET IOOUT /DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
1041
1042 LCT /MOVE SR TO INTERFACE SERIALY
1043 *-8-1
1044 SET SHIFT
1045 CLR SHIFT
1046 ICT
1047 ROTATE ZERO
1048 BR COFL F *-5
1049
1050 CLR IOOUT /NEXT TRANSFER WILL BE FROM INTERFACE
1051
1052 STDONE, SET DONE /FUNCTION IS DONE
1053 LCT /CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION
1054 PFUNCT
1055 JUMP F4
1056 GETCHD
1057
1058 FUNCT, ROTATE /MOVE UNIT SELECT BIT TO SR7
1059 ROTATE
1060 ROTATE
1061 BR SR7 ONE /FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ONUNIT 0
1062 *-2
1063 FLAG OFF
1064
1065 ROTATE /GET FIRST FUNCTION BIT TO SR7
1066

```

```

1067 1045 0120 BR SR7 ZERO
1068 1046 1006 /FUNCTION 4 OR GREATER
1069 1046 1006 /FUNCTION 4 OR GREATER
1070 1046 1006 /FUNCTION 4 OR GREATER
1071 1047 0074 ROTATE
1072 1047 0074 ROTATE
1073 1050 0120 BR SR7 ZERO
1074 1051 1057 /FUNCTION CODE IS 2 OR 3
1075 1051 1057 /FUNCTION CODE IS 2 OR 3
1076 1051 1057 /FUNCTION CODE IS 2 OR 3
1077 1052 0074 ROTATE
1078 1052 0074 ROTATE
1079 1053 0120 BR SR7 ZERO
1080 1054 1107 EMPTYBUF
1081 1054 1107 EMPTYBUF
1082 1055 0212 JUMP F2
1083 1056 1110 FILLBUF
1084 1056 1110 FILLBUF
1085 1057 0074 /FUNCTION CODE IS 2 OR 3
1086 1057 0074 /FUNCTION CODE IS 2 OR 3
1087 1060 0120 BR SR7 ZERO
1088 1061 1105 PROSEC
1089 1061 1105 PROSEC
1090 1062 0074 LCT
1091 1063 0200 0
1092 1064 2070 JUMP F1
1093 1065 0400 WAITSEC
1094 1065 0400 WAITSEC
1095 1066 0074 /FUNCTION CODE IS 2 OR 3
1096 1066 0074 /FUNCTION CODE IS 2 OR 3
1097 1067 0120 BR SR7 ZERO
1098 1070 1276 /FUNCTION CODE IS 6 OR GREATER
1099 1070 1276 /FUNCTION CODE IS 6 OR GREATER
1100 1071 0074 ROTATE
1101 1071 0074 ROTATE
1102 1072 0120 BR SR7 ZERO
1103 1073 1224 RDSTAT
1104 1073 1224 RDSTAT
1105 1074 0212 JUMP F2
1106 1075 1243 CLRID
1107 1075 1243 CLRID
1108 1076 0074 /FUNCTION CODE IS 2 OR 3
1109 1076 0074 /FUNCTION CODE IS 2 OR 3
1110 1077 0120 BR SR7 ZERO
1111 1100 1275 RDEREG
1112 1100 1275 RDEREG
1113 1101 0270 LCT
1114 1101 0270 OCTAL
1115 1122 212P LOP
1116 1103 2200 DECIMAL
1117 1104 2420 JUMP F1
1118 1104 2420 JUMP F1
1119 1104 2420 WAITSEC
1120 1105 0200 PROSEC, JUMP F1
1121 1106 0700 PROSEC, JUMP F1
1121 1106 0700 PROSEC, JUMP F1

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1122 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1123 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1124 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1125 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1126 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1127 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1128 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1129 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1130 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
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1163 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1164 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1165 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1166 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1167 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1168 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1169 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
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1172 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1173 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1174 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1175 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]
1176 1107 0016 /ROUTINE: FILL AND EMPTY BUFFER]

```

WHICH FUNCTION IS THIS?
/EMPTYBUF

REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRUN CLOSED IT
/SET UP BIT COUNT IN CNTR TO 8 BITS OR 12 BITS

```

1177 1150 0104 BR IOB30T F
1178 1151 1175 FILL1
1179
1180
1181 BYTEOUT, SET SHIFT
1182 INCR BAR
1183 CLR SHIFT
1184 ICT
1185 BR COFL F
1186 BYTEOUT
1187
1188 ESP
1189 BR COFL F
1190 XFRQ
1191
1192 SET XREQ
1193 BR RUN F
1194 *-1
1195
1196 CLR XREQ
1197
1198 JUMP F2
1199 OKDONE
1200
1201 FIN WRITBUF
1202 INCR BAR
1203
1204 SET SHIFT
1205 CLR SHIFT
1206
1207 FILL1, START -RTBUF
1208
1209 /LAST BIT OF BYTE?
1210 BR COFL F
1211 *-7
1212
1213 FIN WRITBUF
1214 INCR BAR
1215
1216 ESP
1217 BR COFL F
1218 XFRQ
1219
1220 JUMP F2
1221 OKDONE
1222
1223 EMPTY, SET SECDAT
1224 ICT
1225 LSR
1226 LSP
1227
1228
1229
1230
1231

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1232 1214 0270 LCT
1233 1215 0367 *-8-1
1234 1216 2150 BK XIIBIT F
1235 1217 1152 BYTEOUT
1236 1220 0070 LCT
1237 1221 0363 *-12-1
1238
1239 JUMP F2
1240 BYTEOUT
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/(ROUTINE: READ STATUS)

```

1224 0244 RDSTAT, OPEN TEMPD
1225 0036 UNIT ONE
1226 0072 LCT
1227 0000 0
1230 0174 BR FLAG0 ZERO
1231 1235 *-4
1232 0034 UNIT ZERO
1233 0070 LCT
1234 0200 OCTAL
1235 0075 LSR
1236 0064 LSP
1237 0070 LCT
1240 1765 PNTROY
1241 0226 JUMP F5
1242 2640 CHKRDY
1243 2214 CLRID, OPEN STAT
1244 0071 ESP
1245 0075 LSR
1246 0061 FLAG OFF
1247 0070 LCT
1250 0372 *-5-1
1251 0122 BR SR7 T
1252 1256 *-4
1253 0074 ROTATE ZERO
1254 0212 JUMP F2
1255 1257 *-2
1256 0076 ROTATE ONE
1257 0073 ICT
1260 0124 SR COFL F

```

/CALL CHECKRDY SUBROUTINE, RETURN TO CLRID

/CLEAR INIT DONE BIT OF STAT
/STATUS TO SHIFT REG

/END AROUND SHIFT OF FIRST 5 BITS

```

1287 1261 1251 *-0
1288 BR FLAG0 T /IF FLAG IS SET THEN ROTATE IS DONE
1289 GODUN
1290 1263 1272
1291 FLAG ON
1292 ROTATE ZERO
1293 LCT
1294 *-2-1
1295 JUMP F2
1296 ROT
1297 1271 1251
1298
1299
1300 GODUN, LSP /RESTORE STAT AND GO DONE
1301 JUMP F2
1302 OKDONE
1303
1304 /ROUTINE1 READ ERROR REGISTER]
1305
1306
1307
1308 RDEREG, OPEN ERREG
1309 JUMP F2
1310 OKDONE+2
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321 DELAY, OPEN RTNB /SAVE THE RETURN ADDRESS
1322 LSP
1323 LSR /MULTIPLIER TO SHIFT REGISTER
1324 LCT
1325 -122-1 /DELAY 490 CYCLES (98 MICRO SECONDS)
1326 ICT
1327 OPEN RTNB
1328 BR COFL F
1329 *-3
1330 ESP /MOVE MULTIPLIER TO CNTR VIA RTNB
1331 LSP
1332 LSR
1333 ESP
1334 LSP /INCREMENT THE MULTIPLIER
1335 ICT
1336 BR COFL F /ANY MORE .1MS LOOPS?
1337 DELAY+1 /YES, GO TO IT
1338
1339 JUMP F4 IND /NO, RETURN FROM SUBROUTINE
1340
1341

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/SUBROUTINE1 WRITE ZEROS)
 /THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
 /WRITE GATE IS ON. IF WRITE GATE IS OFF IT ACTS AS A
 /DELAY OF 1.5 BITS. ENTRANCE IS MADE WITH RETURN ADDRESS
 /IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
 /TRANSITION OCCURRING IMMEDIATELY PRIOR TO THE JUMP INTO
 /THIS SUBROUTINE.

```

1322 2274 *RTOS, OPEN RTN /SAVE RETURN ADDRESS
1323 0064 LSP
1324 0075 LSR /PUT BIT COUNTER IN SR
1325 0230 OPEN TEMP4 /TEMP4 IS THE PATH THROUGH THE SP
1326 0070 LOOP, LCT /STALL 2.6 MICRO SECONDS
1327 0374 -3-1
1328 2073 ICT
1329 0124 BR COFL F
1330 1330 LSP
1331 0064 *-2
1332 0071 ESP /NOOP
1333 0063 TOG FLAG /WRITE A CLOCK TRANSITION IF WR7 GATE IS SET
1334 0064 LSP /PUT BIT COUNT IN THE COUNTER
1335 0071 ESP
1336 0073 ICT /INCREMENT BIT COUNT
1337 0075 LSR /PUT UPDATED BIT COUNT BACK IN SR
1338 0124 BR COFL F /DONE ALL BITS?
1339 1326 LOOP /NO
1340 0274 OPEN RTN /YES, RETURN FROM SUBROUTINE
1341 0207 JUMP IND F1
1342
1343
1344
1345
1346 0222 PGOIT, JUMP F4 /POINTER TO GETWORD FROM WAITRUN
1347 2010 GOTIT
1348
1349
1350 /ROUTINE1 INITIALIZE CONT.)
1351 TEST2, FLAG OFF /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
1352 LCT /LOOP TO TEST THAT SR IS 252 AND THAT
1353 -5-1 /IT CAN BE SHIFTED.
1354 TSTAGN, BR SR7 ZERO /TEST FAILURE
1355 INTER1
1356 ROTATE ONE
1357 BR SR7 ONE

```

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1397 1357 1374 INTER1
1398 1360 0074 ROTATE ZERO
1399 1361 0073 ICT
1400 1362 0124 BR COFL F
1401 1363 1353 TSTAGN
1402
1403 1364 0250 OPEN R10
1404 1365 0071 ESP
1405 1366 0075 LSR
1406
1407 1367 0074 ROTATE ZERO
1408
1409 1370 0176 BR FLAGO ONE
1410 1371 1350 TEST2
1411
1412 1372 0202 TESTDN, JUMP F0
1413 1373 0004 TSTRTN
1414
1415 1374 0006 INTER1, SET ERR
1416 1375 0212 JUMP F2
1417 1376 1031 STDONE
1418
1419 1377 0000 0
    
```

/OPEN

/CONTENTS OF R10 TO SR, SHOULD BE 125

/SHIFT SR ONCE TO CHANGE 125 TO 252

/HAS R10 BEEN TESTED ALREADY?

/NO

/YES, RETURN TO REMAINING INITIALIZE ROUTINE

/SELF TEST ERROR, SET ERROR AND GO SET DONE

```

1420 /SUBROUTINE: FINDHEADER AND FIND DATA ADDRESS MARK1
1421 /SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)
1422 /ENTER WITH THE RETURN ADDRESS IN CNTR. ALSO ROUTINE TO FIND A DATA MARK
1423 /OR DELETED DATA MARK.
    
```

/THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROES.

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1471
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1473
1474
    
```

FINDHND, OPEN RTNB

LSR

LSP

OPEN TEMPB

LCT

-1

LSR

LSP

OPEN TEMPB

LCT

-3-1

TRYAGN, LSR

LSR

CLR BAR LONG

OPEN TEMPB

LCT

-24-1

MOREBS, LSR

LSP

LCT

-200-1

LSR

MOR SEPCLK T

.+3

JUMP F3

TIMERR

BR DECSR7 F

NOZERO

ESP

ICT

BR COFL F

MOREBS

FLAG OFF

GETDAM, CLR BAR LONG

LCT

/3 TO CNTR FOR RAD START OUTER COUNT, 768 BAD STARTS ALLOWED

/RESTORE BAD START COUNT

/RESET FOR A COUNT OF 4096 AS PREAMBLE FAILURE COUNT

/24 TO CNTR AS ZERO BIT COUNT

/RESTORE ZERO BIT COUNT

/PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 40 MICRO SEC WAIT BRANCH

/WAIT 40 MICRO SECONDS FOR SEP CLK

/ERROR, NO SEP CLK

/WHAT IS SEP DATA?

/ONE, GO CHECK PREAMBLE FAILURES

/ZERO FOUND, CHECK ZERO COUNT

/NEED MORE ZEROES FOR PREAMBLE

/FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM

/START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER

/WAIT 40 MICRO SEC FOR SEP CLK

```

1475 1443 0067 -200-1
1476 1440 0346 WBR SEPCLK T
1477 1445 1450 .+3
1478 1446 0216 JUMP F3
1479 1447 1667 TIMERR
1480
1481 1450 0156 BR DEQSR7 T
1482 1451 1755 NOTYET
1483
1484 1452 0160 BR MCEQSR F
1485 1453 1673 BADSRT
1486
1487 1454 0057 PRECRC
1488 1455 0056 CRC ONE
1489 1456 0056 CRC ONE
1490
1491 1457 0070 LCT
1492 1460 0067 -200-1
1493 1461 0346 WBR SEPCLK T
1494 1462 1465 .+3
1495 1463 0216 JUMP F3
1496 1464 1667 TIMERR
1497
1498 1465 0156 BR DEQSR7 T
1499 1466 1673 BADSRT
1500 1467 0166 BR MCEQSR T
1501 1470 1673 BADSRT
1502
1503 1471 0054 CRC ONE
1504 1472 0050 CRC ONE
1505 1473 0056 CRC ONE
1506
1507 1474 0070 LCT
1508 1475 0067 -200-1
1509 1476 0346 WBR SEPCLK T
1510 1477 1502 .+3
1511 1500 0216 JUMP F3
1512 1501 1667 TIMERR
1513
1514 1502 0154 BR DEQSR7 F
1515 1503 1673 BADSRT
1516 1504 0164 BR MCEQSR F
1517 1505 1673 BADSRT
1518
1519 1506 0070 LCT
1520 1507 0000 0
1521 1510 0075 LSR
1522
1523 1511 0070 LCT
1524 1512 0067 -200-1
1525 1513 0346 WBR SEPCLK T
1526 1514 1517 .+3
1527 1515 0216 JUMP F3
1528 1516 1667 TIMERR
1529

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1530 1517 0154 BR DEQSR7 F
1531 1520 1673 BADSRT
1532 1521 0042 LDHD
1533 1522 0042 LDHD
1534 1523 0164 BR MCEQSR F
1535 1524 1673 BADSRT
1536
1537 1525 0070 LCT
1538 1526 0067 -200-1
1539 1527 0346 WBR SEPCLK T
1540 1530 1533 .+3
1541 1531 0216 JUMP F3
1542 1532 1667 TIMERR
1543
1544 1533 0156 BR DEQSR7 T
1545 1534 1673 BADSRT
1546
1547 1535 0176 BR FLAGO T
1548 1536 1675 DAM
1549
1550 1537 0164 BR MCEQSR F
1551 1540 1673 BADSRT
1552
1553 1541 0256 CRC ONE
1554
1555 1542 0070 LCT
1556 1543 0067 -200-1
1557 1544 0346 WBR SEPCLK T
1558 1545 1550 .+3
1559 1546 0216 JUMP F3
1560 1547 1667 TIMERR
1561
1562 1550 0156 BR DEQSR7 T
1563 1551 1673 BADSRT
1564 1552 0164 BR MCEQSR F
1565 1553 1673 BADSRT
1566
1567 1554 0042 LDHD
1568
1569 1555 0056 CRC ONE
1570
1571 1556 0370 LCT
1572 1557 0067 -200-1
1573 1560 0346 WBR SEPCLK T
1574 1561 1564 .+3
1575 1562 0216 JUMP F3
1576 1563 1667 TIMERR
1577
1578 1564 0156 BR DEQSR7 T
1579 1565 1673 BADSRT
1580 1566 0166 BR MCEQSR T
1581 1567 1673 BADSRT
1582
1583 1570 0054 CRC ZERO
1584

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1571 0220      MORCOM, OPEN TARTRK      /TARGET TRACK ADDRESS TO SR
1572 0071      ESP
1573 0075      LSR

1574 0070      LCT
1575 0367      -8-1      /SET BIT COUNTER TO 0

1576 0144      AGAIN3, BR SEPCLK F    /WAIT FOR BIT CELL
1577 1576      .-1

1600 0156      BR DECSRT T          /SEP DATA EQUAL TO SR??
1601 1685      .+4              /NO, TRACK COMPARE ERROR

1602 0074      ROTATE ZERO
1603 0216      JUMP F3
1604 1610      .+4

1605 0210      OPEN ERREG
1606 0276      ROTATE ONE
1607 0064      LSP

1612 0055      DATCRC
1611 0073      ICT
1612 0124      BR COFL F
1613 1576      AGAIN3
1614 0070      LCT
1615 0367      -8-1

1616 0144      AGAIN3, BR SEPCLK F    /WAIT FOR BIT
1617 1616      .-1

1620 0061      FLAG OFF
1621 0261      /CLEAR FLAG FOR NEXT ROUTINE
1622 0061      FLAG OFF
1623 0061      FLAG OFF
1624 0255      DATCRC
1625 0073      ICT
1626 0124      BR COFL F
1627 1616      AGAIN3

1628 0070      LCT
1629 0367      -8-1
1630 0144      AGAIN3, BR SEPCLK F    /WAIT FOR BIT
1631 1616      .-1
1632 0061      FLAG OFF
1633 0261      /CLEAR FLAG FOR NEXT ROUTINE
1634 0061      FLAG OFF
1635 0061      FLAG OFF
1636 0255      DATCRC
1637 0073      ICT
1638 0124      BR COFL F
1639 1616      AGAIN3

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1630 0224      OPEN TARSEC      /TARGET SECTOR ADDRESS TO SR
1631 0271      ESP
1632 0275      LSR

1633 0070      LCT
1634 0367      -8-1      /SET UP BIT COUNTER FOR 8 BITS

1635 0144      AGAIN3, BR SEPCLK F    /WAIT FOR A BIT
1636 1635      .-1

1637 0156      BR DECSRT T          /HOW DO THEY COMPARE?
1640 1643      .+3              /BAD, GO SET THE FLAG

1641 0216      JUMP F3
1642 1644      .+2

1643 0062      FLAG ON
1644 0074      ROTATE ZERO
1645 0055      DATCRC
1646 0073      ICT
1647 0124      BR COFL F
1650 1635      AGAIN3
1651 0070      LCT
1652 0347      -24-1
1653 0144      AGAIN3, BR SEPCLK F    /WAIT FOR BIT
1654 1635      .-1

1655 0074      ROTATE ZERO
1656 0074      ROTATE ZERO
1657 0074      ROTATE ZERO
1660 0074      ROTATE ZERO
1661 0055      DATCRC
1662 0073      ICT
1663 0124      BR COFL F
1664 1653      AGAIN3
1665 0226      JUMP F5
1666 2515      CAHCR3
1667 0070      TIMERR, LCT
1670 0110      ATIMERR
1671 0226      JUMP F5
1672 2610      GOERDN

```

```

/THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
/DESIRED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
/FINDING THE IDAM, ERREG BIT IS SET IF AN ERROR IS DETECTED.

```

```

/THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
/TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
/THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.

```

```

/40 MICROSEC PASSED AND NO SEP CLOCK WAS SEEN

```

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1695
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1697 1673 0226 BADSRT, JUMP F5
1698 1674 2555 /POINTER TO BADSTART ON IDAM OR DATA AM
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708 DAM, BR MCEQSR T /MISSING CLK SHOULD BE T
1709 BADSRT
1710
1711 1677 0054 CRC ZERO /JAM 6TH CRC BIT OF DATA AM
1712
1713 LCT /WAIT FOR SIXTH BIT CELL
1714 -200-1
1715 WBR SEPCLK T
1716 *+3
1717 JUMP F3
1718 TIMERR
1719
1720 BR MCEQSR F /MISSING CLK SHOULD BE F
1721 BADSRT /NOOP FOR LONG SEP CLK
1722 LDHD /IF DATA=0 THEN LOOK FOR DELETED DATA AM
1723
1724 RR DEQSR7 T
1725 DELDAT
1726
1727 CRC ONE /JAM 7TH BIT OF DATA AM
1728
1729 LCT /WAIT FOR SEVENTH BIT OF DATA AM
1730 -200-1
1731 WBR SEPCLK T
1732 *+3
1733 JUMP F3
1734 TIMERR
1735
1736 CRC ONE /JAM LAST BIT OF DATA AM
1737
1738 RR DFQSR7 F /DATA SHOULD BE 1
1739 ENDDAM /FLAG IS SET TO INDICATE NORMAL DATA MARK
1740
1741 JUMP F3 /LAST DATA BIT WAS BAD
1742 BADSRT
1743
1744 DELDAT, CRC ZERO /JAM 7TH CRC BIT OF DEL DATA AM
1745
1746 LCT /WAIT FOR 7TH CELL OF DEL DATA AM
1747 -200-1
1748 WBR SEPCLK T
1749

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1750 1733 1736 *+3
1751 1734 0216 JUMP F3
1752 1735 1667 TIMERR
1753
1754 1736 0061 FLAG OFF /CLR FLAG TO INDICATE DELETED DATA MARK
1755
1756 1737 0054 CRC ZERO /JAM LAST CRC BIT OF DEL DATA AM
1757
1758 1740 0154 BR DEQSR7 F /DATA SHOULD BE 0
1759 1741 1673 BADSRT
1760
1761 1742 0164 ENDDAM, BR MCEQSR F /MISSING CLK SHOULD BE F FOR BOTH DATA AMS
1762 1743 1673 BADSRT
1763
1764 1744 0222 JUMP F4 /GO PICK UP DATA FIELD
1765 1745 2206 DATA
1766
1767
1768 NOZERO, INCR BAR /INCREMENT AND TEST PREAMBLE FAILURE COUNT
1769 1747 0160 BR BARDFL F /OK, TRY AGAIN FOR A PREAMBLE
1770 1750 1416 TRYAGN*3
1771
1772 NXPBRAM, LCT /TOO MANY BITS WITH NO ZEROS
1773 1751 0070
1774 1752 0120 KNXPBRAM
1775 1753 0226 JUMP F5
1776 1754 2610 GOERDN
1777
1778
1779 NOTYET, INCR BAR /INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
1780 1756 0042 LDHD /NOOP FOR LONG SEP CLK
1781 1757 0160 RR BARDFL F /OK, TRY AGAIN
1782 1760 1442 GETDAM+1
1783
1784 NXIDAM, LCT /TOO MANY ZEROS WHILE LOOKING FOR START OF
1785 1762 0130 KNXIDAM /IDAM OR DATA AM
1786 1763 0226 JUMP F5
1787 1764 2610 GOERDN
1788
1789
1790 PATROY, JUMP F2 /POINTERS FROM CHECKRDY SUBROUTINE TO ROSTAT ROUTINE
1791 1766 1243 CLRID
1792 1767 0212 P SRDY, JUMP F2
1793 1770 1243 CLRID
1794
1795 PNRORY, JUMP F2 /POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE
1796 1772 1006 OKDDNE
1797 1773 0226 JUMP F5
1798 1774 2631 INTRDY
1799
1800 1775 0000 0 /OPEN
1801 1776 0000 0 /OPEN
1802 1777 0000 0 /OPEN

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1893 /SUBROUTINE GETWORD AND GETCOMMAND1
1894 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1895 /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1896 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1897 /BIT WORD, ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1898 /IN THE COUNTER, EXIT WITH THE ONES COMPLEMENT OF THE
1899 /DESIRED WORD IN THE SHIFT REGISTER, PARITY IS COMPUTED AND
1900 /CHECKED ON ALL WORDS.
1901
1902 GETWRD, SET XREG /REQUEST A WORD FROM INTERFACE
1903 GETCHD, LSR /SWASH THE RETURN ADDRESS
1904 LSP
1905 LCT
1906 PGOTIT /CALL SUBR WAITRN TO WAIT FOR A WORD
1907 JUMP F4
1908 WAITRN
1909
1910 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
1911 CLR ERR /IN CASE RUN WAS A RESPONSE TO DONE
1912 CLR DONE
1913 LCT /SET UP BIT COUNT IN CNTR, 8 BIT OR 12 BIT
1914 -8-1
1915 BR XIIBIT F
1916 +3
1917 LCT
1918 -12-1
1919
1920 MATDAT, BR DATTAIN ONE /WHAT IS THE DATA BIT?
1921 GOTONE /ITS A ONE, GO SAVE IT
1922
1923 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1924 CHKPAR /YES, GO CHECK PARITY
1925 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN SR
1926 JUMP F4 /GO SHIFT UP ANOTHER BIT.
1927 NUTHER
1928
1929
1930 GOTONE, TOG FLAG /COMPLIMENT THE PARITY GENERATOR
1931 BR COFL T /WAS IT THE PARITY BIT?
1932 CHKPAR /YES, GO CHECK PARITY
1933 ROTATE ZERO /NO, SAVE THE COMPLIMENTED DATA BIT IN SR
1934 NUTHER, SET SHIFT /SHIFT PULSE AND INCREMENT BIT COUNT

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1858 ICT
1859 CLR SHIFT
1860
1861 JUMP F4 /GO TEST THIS BIT.
1862 MATDAT
1863
1864
1865 CHKPAR, BR FLAGO ONE /WHERE THERE AN ODD NO. CF ONES?
1866 GOTWRD /YES, PARITY WAS GOOD
1867
1868 OPEN STAT /NO, STAT TO SR
1869 ESP
1870 LSR
1871
1872 LCT /END AROUND SHIFT OF UPPER 5 BITS OF STAT IN SR
1873 -5-1
1874 BR SR7 T
1875 +4
1876 ROTATE ZERO
1877 JUMP F4
1878 +2
1879 ROTATE ONE
1880 ICT
1881 BR COFL F
1882 +8
1883
1884 ROTATE ZERO /CLEAR INIT DONE
1885 ROTATE ONE /SET PARITY ERROR
1886
1887 BR SR7 T /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN SR
1888 +4
1889 ROTATE ZERO
1890 JUMP F4
1891 +2
1892 ROTATE ONE
1893
1894 LSP /RESTORE STAT TO SCRATCH PAD
1895 LCT /ERRCODE FOR PARITY ERROR
1896 KPARER
1897 JUMP F5
1898 GOERON
1899
1900 GOTWRD, OPEN RTMA /WORD WAS GOOD, EXIT FROM GETWRD, WETCHD
1901 JUMP F0 IND
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2100 0270
2101 0064
2102 0075
2103 0071
2104 0064
2105 0136
2106 2150
2107 0073
2110 0075
2111 0230
2112 0064
2113 0070
2114 2124
2115 0075
2116 0070
2117 0341
2120 0012
2121 0010
2122 0212
2123 1300
2124 0012
2125 0010
2126 0070
2127 2135
2130 0075
2131 0070
2132 0341
2133 0212
2134 1300
2135 0230
2136 0071
2137 2124
2140 2105

/(SUBROUTINE: STEP HEAD)
/THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
/SPECIFIED DIRECTION. DIRECTION IS DETERMINED BY THE HD DIR FLOP
/THE NUMBER OF STEPS IS IN THE SR. RETURN ADDRESS IS IN THE CNTR.
/EXIT IS TO THE RETURN ADDRESS IF HOME IS DETECTED. EXIT IS TO RETURN
/PLUS 2 IF THE LAST STEP HAS BEEN TAKEN. AFTER THE LAST STEP IS TAKEN,
/THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME

STEPHD, OPEN RTNA /STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
LSP
LSP
ESP
LSP
CKHOME, BR HOME T /IS THE HEAD HOME?
OUT /YES, GO EXIT
ICT /NO, INCREMENT STEP COUNT AND STORE IN TEMPA
LSR
OPEN TEMPA
LSP
LCT
SECPLS /PASS 30 TO DELAY SUBR FOR 3MS DELAY
LCT
SECPLS
LCT
-30-1
SET STPHD /ISSUE STEP PULSE
CLR STPHD /CALL DELAY SUBR
JUMP F2
DELAY /ISSUE SECOND STEP PULSE
SECPLS, SET STPHD
CLR STPHD /CALL DELAY FOR 3MS DELAY
LCT
DONSTP
LSR
LCT
-30-1
JUMP F2
DELAY
DONSTP, OPEN TEMPA
ESP
BR COFL F /CHECK STEP COUNT
CKHOME /NOT DONE, GO CHECK IF HOME

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/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-76 9117 PAGE 12-1
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2141 0270
2142 0071
2143 0073
2144 0073
2145 0270
2146 0075
2147 0064
2150 0042
2151 2250
2152 0070
2153 0200
2154 0075
2155 0064
2156 0070
2157 2165
2170 0075
2161 0270
2162 0000
2163 0212
2164 1300
2165 0270
2166 0203
2167 0070
2170 0374
2171 0234
2172 0075
2173 0064
2174 0070
2175 0207
2176 0073
2177 0062
2200 0124
2201 2176
2202 0073
2203 0075
2204 0216
2205 1441

/DORE STEPPING, INCREMENT RETURN ADDRESS BY 2
/STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE
/LOAD HEAD
/SET SOFT HD LOAD BIT
/CALL DELAY SUBR FOR 25MS DELAY
/RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE

/ROUTINE: READ SECTOR CONT.)
READ, LCT /3 TO DATA MARK TRY COUNTER
-3-1
OPEN TEMPB
LSR
LSP
LCT
-120-1
ICT
FLAG ON
BR COFL F
-3
ICT
LSR
JUMP F3
GETDAM

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/STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH
/SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE
/CLR COUNTER AND SR
/GO TRY FIND THE ADDRESS MARK

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2067
2206 0044 DATA CLR BAR /CLEAR THE BUFFER ADDRESS REGISTER
2207 0144 BR SEPCLK F /WAIT FOR CLOCK
2210 2207 *-1
2211 0053 START WRTRBUF /START THE WRITF PULSE FOR THIS BIT
2212 0055 DATCRC /UPDATE THE CRC WITH SEP DATA
2213 0162 BR BAROFL T /IS BUFFER FULL YET?
2214 2221 GETCRC /YES, GO GET THE CRC
2215 0050 FIN WRTRBUF /NO, END THE WRITE PULSE
2216 0046 INCR BAR /ADDRESS NEXT SECTOR BUFFER CELL
2217 0222 JUMP F4 /LOOP BACK FOR NEXT BIT
2220 2207 DATA+1
2221 0050 GETCRC, FIN WRTRBUF /END THE WRITF PULSE FOR THE LAST BIT
2222 0070 LCT /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2223 0357 -16-1
2224 0144 BR SEPCLK F /WAIT FOR NEXT BIT
2225 2224 *-1
2226 0042 LDHD /4 NOOPS FOR LONG SEP CLOCK
2227 0042 LDHD
2230 0042 LDHD
2231 0042 LDHD
2232 0055 DATCRC /PUT CRC BIT IN THE CRC GENERATOR
2233 0073 ICT /INCREMENT AND TEST BIT COUNT
2234 0124 BR COFL F /NOT DONE, GET ANOTHER
2235 2224 *-9
2236 0214 OPEN STAT /STATUS TO SHIFT REG
2237 0071 FSP
2240 0075 LSR
2241 0122 BR SR7 T /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2242 2246 *-4
2243 0074 ROTATE ZERO
2244 0222 JUMP F4
2245 2247 *-2
2246 0076 ROTATE ONE
2247 0176 BR FLAGO T /SET DEL DATA BIT OF STAT IF FLAG=0

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2250 2254 *-4
2251 0076 ROTATE ONE
2252 0222 JUMP F4
2253 2255 *-2
2254 0074 ROTATE ZERO
2255 0070 LCT
2256 0372 -5-1
2257 0122 BR SP7 T
2260 2264 *-4
2261 0074 ROTATE ZERO
2262 0222 JUMP F4
2263 2265 *-2
2264 0076 ROTATE ONE
2265 0073 ICT
2266 0124 BR COFL F
2267 2257 *-8
2270 0070 LCT
2271 0357 -16-1
2272 0132 BR CRC16 ONE
2273 2304 DRCRCR
2274 0054 CRC ZERO
2275 0073 ICT
2276 0124 BR COFL F
2277 2272 *-5
2300 0074 ROTATE ZERO
2301 0064 LSP
2302 0212 JUMP F2
2303 1006 OKDONE
2304 0076 DRCRCR, ROTATE ONE
2305 0064 LSP
2306 0070 LCT
2307 0200 KDCRCR
2310 0226 JUMP F5
2311 2610 GOERDN

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2113 /SUBROUTINE: WAIT FOR RUN]
2114 /THIS SUBROUTINE WILL WAIT FOR RUN. IF 66MS ELAPSES, THE HEAD IS UNLOADED
2115 /AND THE ROUTINE CONTINUES WAITING FOR RUN. RETURN ADDRESS IS PASSED
2116 /VIA THE COUNTER
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2312	0264	WAITRN, OPEN RTNB	/STASH THE RETURN ADDRESS
2313	0075	LSR	
2314	0064	LSP	
2315	0102	BR RUN T	/GOT RUNT
2316	2347	GOTRUN	
2317	0240	OPEN TEMPC	/PRESET LOOP COUNTER TO 0
2320	0070	LCT	
2321	0000	R	
2322	0075	BACK, LSH	/RESTORE LOOP COUNT
2323	0064	LSP	
2324	0302	WBR RUN T	/TIME WHILE WAITING FOR FUN
2325	2347	GOTRUN	
2326	0302	WBR RUN T	
2327	2347	GOTRUN	
2328	0302	WBR RUN T	
2329	2347	GOTRUN	
2330	0302	WBR RUN T	
2331	2347	GOTRUN	
2332	0302	WBR RUN T	
2333	2347	GOTRUN	
2334	0071	ESP	/INCREMENT AND TEST LOOP COUNT
2335	0073	ICT	
2336	0124	BR COFL F	
2337	2322	BACK	/66MS NOT ELAPSED YET
2340	0250	OPEN TEMPC	/TIME IS EXPIRED (45.0 MS). CLEAR THE SOFT HOLD BIT AND UNLOAD THE HEAD
2341	0073	ICT	
2342	0075	LSR	
2343	0064	LSP	
2344	0040	UNHD	
2345	0100	BR RUN F	/WAIT FOR RUN. FOREVER IF NECESSARY
2346	2345	W1	
2347	0010	GOTRUN, CLR YREQ	/IF RUN WAS RESPONSE TO XFREQ
2350	0264	OPEN RTNB	/RETURN FROM WAITRN SUBROUTINE
2351	0213	JUMP IND F2	

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2162 /ROUTINE: INITIALIZE CONT.]
2163 /CONTINUATION OF THE INITIALIZE SELF TEST
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2352	0070	TEST, LCT	/LOAD R5 WITH TEST PATTERN 252
2353	0252	OCTAL 252	
2354	0075	DECIMAL LSR	
2355	0224	OPEN R5	
2356	0064	LSP	
2357	0070	LCT	/LOAD R10 WITH TEST PATTERN 125
2360	0125	OCTAL 125	
2361	0075	DECIMAL LSR	
2362	0254	OPEN R10	
2363	0064	LSP	
2364	0062	FLAG ON	/SET FLAG AND TEST IT
2365	0176	RR FLAGO T	
2366	2371	+3	
2367	0212	JUMP F2	/FLAG FAILURE
2370	1374	INTER1	
2371	0224	OPEN R5	/CONTENTS OF R5 TO R9. SHOULD BE 252
2372	0071	ESP	
2373	0075	LSR	
2374	0212	JUMP F2	/GO CONTINUE UNIT TEST IN FLD 2
2375	1351	TEST1	
2376	0000	0	/OPEN
2377	0000	0	/OPEN

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2197 /SUBROUTINE: MAGNITUDE COMPARISON)
2198 /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
2199 /EXIT IS TO THE RETURN ADDRESS IF F<G. IF F=G, RETURN IS TO RTNA+2.
2200 /IF F>G, RETURN IS TO RTNA+4. CONTENTS OF F AND G ARE UNDEFINED AT
2201 /THE END OF THE SUBROUTINE

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2202 2400 0230 MAGCOM, OPEN TEMPA /FOR BIT COUNT
2203 2401 0070 LCT /BIT COUNT IS 8
2204 2402 0367 -8-1
2205 2403 0075 LSR /RESTORE BIT COUNT
2206 2404 0064 LSP
2207 2405 0254 OPEN TEMPF /F TO SR
2208 2406 0071 ESP
2209 2407 0075 LSR
2210 2410 0120 BR SR7 ZERO
2211 2411 2443 TSTG0
2212 2412 0076 ROTATE ONE /ITS 1, BRING UP NEXT BIT
2213 2413 0064 LSP /RESTORE F
2214 2414 0260 OPEN TEMPG /G TO SR
2215 2415 0071 ESP
2216 2416 0075 LSR
2217 2417 0120 BR SR7 ZERO
2218 2418 2432 GLESSF /ITS 0, G IS LESS THAN F
2219 2420 0074 NEXTG, ROTATE ZERO /ITS 1, BRING UP NEXT G BIT
2220 2422 0064 LSP /RESTORE G
2221 2423 0230 OPEN TEMPA /INCREMENT AND TEST BIT COUNT
2222 2424 0071 ESP
2223 2425 0073 ICT
2224 2426 0124 BR COFL F
2225 2427 2403 MAGCOM+3 /GO COMPARE ANOTHER BIT
2226 2430 0270 OPEN RTNA /ALL BITS COMPARED, NO DIFFERENCE
2227 2431 0203 JUMP F0 IND /G IS LESS THAN F RETURN TO RTNA +4
2228 2432 0270 GLESSF, OPEN RTNA
2229 2433 0071 ESP
2230 2434 0073 ICT
2231 2435 0073 ICT
2232 2436 0273 ICT
2233 2437 0073 ICT
2234 2440 0075 LSR

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2252 2441 0064 LSP
2253 2442 0203 JUMP F0 IND
2254 2443 0074 TSTG0, ROTATE ZERO /F HAS 0, BRING UP NEXT BIT
2255 2444 0064 LSP /RESTORE F
2256 2445 0260 OPEN TEMPG /G TO SR
2257 2446 0071 ESP
2258 2447 0075 LSR
2259 2450 0120 BR SR7 ZERO
2260 2451 2421 NEXTG /MATCHS F, GO BRING UP NEXT G BIT
2261 2452 0270 OPEN RTNA /G IS LESS THAN F. RETURN TO RTNA +2
2262 2453 0071 ESP
2263 2454 0226 JUMP F5
2264 2455 2436 GLESSF+4
2265 /SUBROUTINE: FIND TRACK CONT.)
2266 HUMERR, LCT /HOME FOUND BEFORE LAST STEP TAKEN
2267 KHOMERR
2268 JUMP F5
2269 GOERON

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2270 2462 0230 DIF, OPEN TEMPA /OPEN TEMPORARY PATH THRU THE SP
2271 2463 0126 BR COFL T /HAS A REACHED ALL ONES YET?
2272 2464 2501 DIFB /YES, GO GET A FOR THE DIFFERENCE
2273 2465 0064 LSP /NO, GET B
2274 2466 0075 LSR /A INTO SHIFT RFG
2275 2467 0071 ESP /B INTO COUNTER
2276 2470 0126 BR COFL T /HAS B REACHED ALL ONES YET?
2277 2471 2503 DIFA /YES, GO GET A FOR THE DIFFERENCE
2278 2472 0073 ICT /INCREMENT B
2279 2473 0064 LSP /, BRING BACK A
2280 2474 0075 LSR /B INTO SHIFT REG
2281 2475 0071 ESP /A INTO COUNTER

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2307 2476 0073      ICT
2308 2477 0226      JUMP F5
2309 2502 2463      DIF+1
2310
2311
2312 2501 0270      DIFB, OPEN RTNA
2313 2502 0203      JUMP F0 IND
2314
2315
2316 2503 0270      DIFA, OPEN RTNA
2317 2504 0071      ESP
2318 2505 0073      ICT
2319 2506 0073      ICT
2320
2321 2507 0064      LSP
2322 2510 0075      LSR
2323 2511 0071      ESP
2324 2512 0064      LSP
2325 2513 0075      LSR
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2327 2514 0203      JUMP F0 IND
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/INCREMENT A
 /GO BACK TO TEST A AGAIN
 /R IS THE COMPLIMENT OF THE DIFFERENCE
 /EXIT A>#B
 /A IS THE COMPLIMENT OF THE DIFFERENCE
 /INCREMENT THE RETURN ADDRESS BY 2
 /RESTORE RETURN ADDRESS TO SCRATCHPAD AND A TO SR
 /EXIT A<#B
 /ROUTINE1 FIND HEADER CONT.]
 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
 /AND SECTOR COMPARISONS,
 CKMCRG, LCT /PRESET BIT COUNT TO 16 FOR CRC
 -16-1
 BR CRC16 ONE /IS CRC ZERO
 HRCRER /NO, LOG ERROR AND TRY AGAIN
 ICT /YES, CRC GOOD SO FAR, BUMP BIT CNTR
 CRC ZERO /BRING UP NEXT CRC BIT
 BR COFL F /ALL BITS TESTED?
 -5 /NO, BRANCH BCK
 OPEN ERREG /YES, CRC WAS GOOD, CHECK TRK COMP
 ESP
 LSR
 LCT /ROTATE BIT 0 TO BIT 7
 -7-1
 ROTATE ZERO
 ICT
 BR COFL F /DONE ROTATING?
 -3 /NO

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2362 2536 0122      BR SH7 ONE
2363 2537 2542      TKSKER
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2365 2544 0264      OPEN RTNR
2366 2541 0207      JUMP F1 IND
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/YES, WAS THERE A BAD COMPARE
 /YES, GO REPORT A TRACK SEEK ERROR
 /CORRECT TRACK, EXIT FROM FIND HDR SUBR
 /HEADER CRC WAS GOOD BUT TRACK
 /ADDRESS DID NOT COMPARE, MUST
 /EXIT TO ERROR DONE
 /HEADER CRC WAS NOT CORRECT
 /LOG THE ERROR
 /GO TRY ANOTHER HEADER
 /BAD START ON DATA AM OR IDAM?
 /IDAM, INCREMENT AND TEST BAD START INNER COUNT
 /NO OVERFLOW, GO TRY ANOTHER HEADER
 /INCREMENT AND TEST BAD START OUTER COUNT
 /NO OVERFLOW, GO TRY AGAIN
 /TOO MANY TRIES FOR A HEADER
 /BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT
 /NO OVERFLOW GO TRY FOR DATA AM AGAIN

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/RR01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-76      9117      PAGE 15-8
2417      2606  0070      NODAM,   LCT
2418      2607  0170      KNODAM
2419      2610  0210      GOERDN, OPEN ERREG
2420      2611  0075      LSR
2421      2612  0064      LSP
2422      2613  0212      JUMP F2
2423      2614  1000      ERDONE
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2425      2615  0216      PTRVAG, JUMP F3
2426      2616  1413      TRYAGN
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2429      2617  0216      PGETDA, JUMP F3
2430      2620  1441      GETDAM
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2435      2621  0070      /ROUTINE: INITIALIZE CONT.]
2436      2622  0030      WRONG,   LCT
2437      2623  0226      KARONG
2438      2624  2610      JUMP F5
2439      2625  0070      GOERDN
2440
2441      2625  0070      DNRCAL,   LCT
2442      2626  1771      PNORDY
2443      2627  0226      JUMP F5
2444      2630  2040      CHRDRY
2445
2446      2631  0070      INTRDY,   LCT
2447      2632  0770      GCREAD
2448      2633  0274      OPEN RTN
2449      2634  0075      LSR
2450      2635  0064      JUMP F0
2451      2636  0202      BOOT
2452      2637  0252
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2454
2455

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/RR01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-76      9117      PAGE 16
2456
2457
2458
2459
2460
2461      2640  0274      /CHKRDY, OPEN RTN
2462      2641  0375      LSR
2463      2642  0064      LSP
2464
2465      2643  0070      LCT
2466      2644  0375      -2-1
2467
2468      2645  0230      OPEN TEMPA
2469
2470      2646  0075      NEMPAS,   LSR
2471      2647  0064      LSP
2472
2473      2650  0061      FLAG OFF
2474
2475      2651  0042      LDHD
2476
2477      2652  0070      LCT
2478      2653  0360      -15-1
2479
2480      2654  0234      STDLY,   OPEN TEMPB
2481      2655  0075      LSR
2482      2656  0064      LSP
2483
2484      2657  0070      LCT
2485      2660  0327      -40-1
2486
2487      2661  0240      OPEN TEMPC
2488      2662  0075      SPBACK,   LSR
2489      2663  0064      LSP
2490
2491      2664  0070      LCT
2492      2665  2005      -250-1
2493      2666  0116      BR INDX T
2494      2667  2714      SAKIND
2495      2500  0073      ICT
2496      2501  0124      RR COFL F
2497      2502  2666      *-4
2498
2499      2503  0240      OPEN TEMPC
2500      2504  0071      ESP
2501      2505  0073      ICT
2502      2506  0124      RR COFL F
2503      2507  2662      SPBACK
2504
2505
2506
2507
2508
2509
2510

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/ROUTINE: CHECKREADY]
/SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
/DISK IS INSERTED AND UP TO SPEED. THIS IS DONE BY CHECKING TO SEE IF
/THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 MS AND 180 MS. RETURN
/ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY. NOT READY RETURN IS
/TO THE RETURN ADDRESS. READY RETURN IS TO THE RETURN ADDRESS PLUS 2

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/SAVE RETURN ADDRESS
/2 TO CNTR FOR INDEX PASS COUNT
/FOR INDEX PASS COUNT
/RESTORE INDEX PASS COUNT
/CLOSE INDEX WINDOW
/TO CLEAR INDEX FLOP
/FOR 15 TIMES THROUGH 10MS LOOP
/RESTORE OUTER COUNT
/FOR 40 TIMES THROUGH .25MS LOOP
/RESTORE INNER COUNT
/WAIT .25 MS FOR INDEX
/FOUND INDEX
/INCREMENT AND TEST INNER COUNT

```

```

2511 2700 0234 OPEN TEMPB
2512 2701 0071 ESP
2513 2702 0073 ICT
2514 2703 0124 BR COFL F
2515 2704 2655 STDLY+1
2516
2517 2705 0176 BR FLAGO ONE
2518 2706 2767 UNRDY
2519
2520 2707 0062 FLAG ON
2521
2522 2710 0070 LCT
2523 2711 0374 -3-1
2524
2525 2712 0226 JUMP F5
2526 2713 2654 STDLY
2527
2528
2529
2530 2714 0230 SAWIND, OPEN TEMPB
2531 2715 0071 ESP
2532 2716 0073 ICT
2533 2717 0124 BR COFL F
2534 2720 2646 NEMPAS
2535
2536 2721 0174 BR FLAGO ZERO
2537 2722 2767 UNRDY
2538
2539 2723 0274 OPEN STAT
2540 2724 0071 ESP
2541 2725 0073 ICT
2542 2726 0073 ICT
2543 2727 0075 LSR
2544 2730 0064 LSP
2545
2546 2731 0214 OPEN STAT
2547 2732 0071 ESP
2548 2733 0075 LSR
2549
2550 2734 0076 ROTATE ONE
2551
2552 2735 0061 FLAG OFF
2553
2554 2736 0070 ROT3,
2555 2737 0374 -3-1
2556 2740 0122 BR SR7 T
2557 2741 2745 +0
2558 2742 0074 ROTATE ZERO
2559 2743 0226 JUMP F5
2560 2744 2746 +2
2561 2745 0076 ROTATE ONE
2562 2746 0073 ICT
2563 2747 0124 BR COFL F
2564 2750 2740 +-8
2565 2751 0176 BR FLAGO T

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2566 2752 2764 EXCHRY
2567
2568 2753 0140 BR WRTEN F
2569 2754 2760 +4
2570 2755 0074 ROTATE ZERO
2571 2756 0226 JUMP F5
2572 2757 2761 +2
2573 2760 0076 ROTATE ONE
2574
2575 2761 0062 FLAG ON
2576 2762 0226 JUMP F5
2577 2763 2736 ROT3
2578
2579 2764 0064 EXCHRY, LSP
2580
2581 2765 0274 OPEN RTN
2582 2766 0217 JUMP F3 IND
2583
2584 2767 0214 UNRDY,
2585 2770 0071 ESP
2586 2771 0075 LSR
2587 2772 0074 ROTATE ZERO
2588
2589 2773 0226 JUMP F5
2590 2774 2735 ROT3-1
2591
2592 2775 0000 P
2593 2776 0000 0
2594 2777 0000 0
2595
2596
2597

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0000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
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2200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
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2600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
3000
3100
3200
3300
3400
3500
3600
3700

4000
4100
4200
4300
4400
4500
4600
4700
5000
5100
5200
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5400
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5700
6000
6100
6200
6300
6400
6500
6600
6700
7000
7100
7200
7300
7400
7500
7600
7700

A	0562	EXTRK	0242
ABACK	0535	EXCMRY	2764
ABV43	0344	FILL1	1175
AGAIN	0531	FILLBU	1110
AGAIN1	0550	PINDMD	1400
AGAIN2	0722	FINDSE	0714
AGAIN3	1576	FINDTR	0103
AGAIN4	1616	FUNCT	1036
AGAIN5	1635	FUNCT2	1057
AGAIN6	1653	FUNCT4	1066
B	0564	FUNCT6	1076
BACK	2322	GETCMD	2001
BADDAM	2577	GETCRC	2221
BADHDR	2557	GETDAM	1441
BADSRT	1673	GETTRD	2000
RBACK	0554	GLESSF	2432
BDSRT	2555	GODONE	0712
BOOT	0252	CODUN	1272
BYTEOU	1152	GOERDN	2610
C	0615	GOREAD	0770
CBACK	0576	GOTIT	2010
CEGATE	0674	GOTONE	2032
CFINSE	0351	GOTRUN	2347
CHKPAR	2041	GOTTRD	2076
CHKRDY	2640	HRCRCL	2546
CHKSEC	0730	HORCOM	1571
CKKCR	2515	HOSETL	0322
CKHOME	2105	HLFDLY	0466
CLRID	1243	HOMERR	2456
CKGATE	0666	ILTRK	0206
D	0653	IN10	0845
DAM	1675	INTER1	1374
DAMSUP	0460	INTRDY	2631
DATA	2206	LOOP	1326
DATAA	0571	MAGCOM	2400
DBACK	0646	MOREOS	1421
DCRCER	2304	MEMORD	1141
DELAY	1300	NEWPAS	2646
DELDAT	1727	NEXTG	2421
DIFA	2503	NGDAM	2406
DIFB	2501	NGSTPS	0357
DLY25	2145	NOTYET	1755
DMRCAL	2625	NOZERO	1746
DONDLY	2165	NUTHER	2034
DONSTP	2135	NXDRV0	0064
DUNSTP	0305	NXDRV1	0070
E	0627	NXHDR	0737
EMPTY1	1210	NXIDAM	1761
EMPTYB	1107	NXPRAM	1751
EMDDAM	1742	OKDONE	1006
ERDONE	1400	OUT	2150
		PDURCL	0372

PFUNCT	0370
PGETDA	2617
PGOTIT	1346
PNORDY	1771
PNRDXY	1765
PROSEC	1105
PRTEAR	0503
PTRYAG	2615
PUTSEC	0145
PUTTRV	0166
PYBRDY	1767
RCALOW	0060
RODEF	1275
RDSEC	0760
RDSSTAT	1224
READ	2167
READ00	0706
RECAL7	0035
RECAL1	0034
REFINTR	0355
ROT	1251
ROT3	2736
SAMIND	2714
SECHLF	0543
SECLPS	2124
SELFER	0620
SPBACK	2662
STASH	0437
STDLY	2654
STDONE	1031
STEPHA	2100
STPOUT	0275
SMGATF	0007
TEST	2352
TEST1	1351
TEST2	1350
TESTN	1372
TIMERR	1667
TMSKER	2542
THKEO	0246
TRVAGN	1413
TSTAGN	1353
TSTG00	2443
TSTRTH	0004
UDIF	0134
UNRDY	2767
UONE	0120
USAME	0141
UZERO	0127
WAIT	0743
WAITRN	2312
WATDAY	2021

WMCMDR	0075
WRONG	2621
WRT08	1322
WRTCRC	0624
WRTDAM	0514
WRTDAT	0566
WRTPRT	0400
WRTSEC	0400
XFRD	1131
XSTRY0	2573

ERRORS DETECTED: 0
LINKS GENERATED: 0
RUN-TIME: 18 SECONDS
3K CORE USED

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ITEM NO.	DWG NO./PART NO.	DESCRIPTION	RX01-AA	RX01-AB	RX01-AC	RX01-BA	RX01-BB	RX01-BC	RX01-CA	RX01-CB	RX01-CC	RX01-DA	RX01-DC	RX01-DD	RX01-AD	RX01-BD	RX01-FA	RX01-FC	RX01-FD	RX01-HA	RX01-HC	RX01-HD	RX01-JA	RX01-JC	RX01-JD	RX01-LA	RX01-LC	RX01-LD	RX01-VA	RX01-VC	RX01-VD
44	A-SP-3700229-0-0	PACKAGING INSTRUCTIONS RX01 DRIVES	-	-	-	-	-	1	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	9009813-00	SCR, PHL PAN HD. #10-24 x .38 LG TAPTITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
46	A-PC-3612063-0-0	LABEL, ADHESIVE BACKED, UL PRINTED	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
47	7013503-0-4	PLENUM, ASSY W/O PACKAGING 115VAC	-	-	-	1	1	-	-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	1	1	-	-	-	-	
48	7013503-0-5	PLENUM ASSY W/O PACKAGING 230VAC	-	-	-	-	-	-	-	-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	-	1	1	-	-	
49	7013503-0-6	PLENUM ASSY W/O PACKAGING 115VAC	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
50	7013503-0-7	PLENUM ASSY W/O PACKAGING 230VAC	-	-	-	-	-	-	-	-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
51	A-SP-3700185-1	PACKAGING INSTR. RX01 W/O BEZEL ASSY	-	-	-	-	-	-	-	-	-	1	1	1	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1	
52	9008341	PVC CLIP, DESK LASP, 1"W x .750" LG	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
53	3613211-00	LABEL, CSA	1	-	-	1	-	-	1	-	-	1	-	-	-	1	-	-	1	-	-	1	-	-	1	-	-	1	-	-	
54	3613210-00	DECAL, SERIAL TAG	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
55	3612063-00	U-UL RECOGNIZED LABEL	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
56	9006020-1	SCREW, P.P.H. #6-32 x 1/14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
57	E-UA-7013077-04	FLEXIBLE DISK DRIVE 60HZ (PREFERRED)	1	-	-	2	-	-	1	-	-	2	-	-	-	1	-	-	2	-	-	2	-	-	2	-	-	1	-		
	E-UA-7013077-00	FLEXIBLE DISK DRIVE 60HZ (OPTIONAL)																													
	A-PL-7014300-00	FLEXIBLE DISK DRIVE 60HZ (OPTIONAL)																													
	A-PS-3012304-00	FLEXIBLE DISK DRIVE 60HZ (OPTIONAL)																													
58	E-UA-7013077-05	FLEXIBLE DISK DRIVE 50HZ (PREFERRED)	-	-	1	-	-	2	-	-	1	-	2	2	1	2	-	1	1	-	2	2	-	2	2	-	2	2	-	1	
	E-UA-7013077-01	FLEXIBLE DISK DRIVE 50HZ (OPTIONAL)																													
	A-PL-7014300-01	FLEXIBLE DISK DRIVE 50HZ (OPTIONAL)																													
	A-PS-3012304-01	FLEXIBLE DISK DRIVE 50HZ (OPTIONAL)																													
59	9006074-03	SCR. PHL TRUSS HD #10-32 x 5/8 (TO HOLD CHASSIS TRACK)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
60	9006565-00	NUT KEP (TO HOLD CHASSIS TRACK)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
61	7015622-0-4	PLENUM ASSY W/O PACK. 115VAC NEW STYLE	-	-	-	1	-	1	-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	-	1	1	-	-	-	
62	7015622-0-5	PLENUM ASSY W/O PACK. 230VAC NEW STYLE	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	
63	7015622-0-6	PLENUM ASSY W/O PACK. 115VAC NEW STYLE	1	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
64	7015622-0-7	PLENUM ASSY W/O PACK. 230VAC NEW STYLE	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
65	36-15996	DECAL, UNIT MUST BE SECURED IN CLOSED POSITION	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

REV.	
CHANGE NO.	
CHK	

DRN. W. MCCARTHY	1/22/75	FIRST USED ON	RX01	digital
CHK'D W. MCCARTHY	2/6/75	TITLE	RX01 FLOPPY DISK DRIVE ASSY	
ENG. C. YOUSE				
PROJ. ENG.				
PROD. J. MILLER	3/18/75			
NEXT HIGHER ASSY.				
B-DD-RX01-β		SIZE	C	CODE
SCALE			PL	NUMBER
SHEET 2 OF 2		DIST.		RX01-β-β
				REV. S

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PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
	REF	X-Y COORDINATE HOLE LOCATION	KCO-M7726-0-4	1
	REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M7726-0-5	2
	REF	MODULE ECO HISTORY	B-MH-M7726-0-6	3
1		ETCHED CIRCUIT BOARD	5011390	4
1	J3	RECEP 36 PIN (BEWORK)	B-MD-3509 07-1	5
1	J2	IC SOCKET, 16 PIN GOLD, LOW PROFILE	1211813-02	6
1	R37	RES 10K 1/4W 5% CC	1300479-00	7
3	C 99, C96 - C102	CAP 6.8 μF 35V 10% S.TANT	1005306-00	8
93	C1 - C93	CAP .01 μF 50V AXIAL CER	1001610-00	9
1	C95	CAP 12 PF 100V 5%	1002007-00	10
3	D1 - D3	DIODE 1N4004	1105796-00	11
1	D4	DIODE 1N742A 3.3V 5%	1104860-00	12
1	R 39	RES 100 1/2W 5% CC	1300228-00	13
3	J4	HEADER, 2 PIN (MALE)	1212204-00	14
1	R2, R4, R6, R9, R10, R12, R14, R16	RES 470 1/4W 5% CC	1300316-00	15
6	R27, R29, R31, R47, R52, R43, R41, R45	RES 390 1/4W 5% CC	1300309-00	16
5	R1, R49 - R51, F57	RES 3K 1/4W 5% CC	1300432-00	17
5	R26, R28, R30, R32, R42, R44, R46, R48, R53	RES 180 1/4W 5% CC	1301322-00	18
8	R3, R5, R7, R9, R11, R13, R15, R17	RES 820 1/4W 5% CC	1301775-00	19
1	R35	RES 300 1/4W 5% CC	1301425-00	20
3	R18 - R25	RES 2K 1/4W 5% CC	1302388-00	21
1	R34	RES 261 1/4W 1% MF	1302873-00	22
1	R36	RES 287 1/4W 1% MF	1305124-00	23
1	R40	RES 8.2K 1/4W 5% CC	1303179-00	24
3	R54 - R56	RES 1K 1/4W 5% CC	1300365-00	25
1	Q2	TRANS MXA905	1510705-00	26
1	Q1	TRANS MXA955	1510706-00	27
5	E19, E20, E21, E29, E40	IC 7474	1905547-00	28
3	E9, E57, E59	IC 7400	1905575-00	29
2	E43, E60	IC 7410	1905576-00	30
1	E75	IC 7450	1905580-00	31
1	E55	IC 74H20	1905635-00	32
1	E54	IC 7402	1909004-00	33
2	E68, E72	IC 74H00	1909056-00	34
2	E56, E70	IC 74H11	1909267-00	35
5	E30, E69, E70, E79, E82	IC 74H74	1909667-00	36
2	E44, E76	IC 7404	1909686-00	37
1	E39	IC 74154	1909701-00	38
2	E1, E2	IC 8001	1909705-00	39
1	E61	IC 74H04	1909931-00	40
2	E74, E92	IC 7486	1910011-00	41
4	E88, E89, E90, E91	IC 74193	1910018-00	42
2	E27, E37	IC 8266	1909934-00	43
1	E22	IC 7402	1910046-00	44
1	E65	IC 7437	1910091-00	45
1	E49	IC 74150	1910153-00	46
2	E11, E12	IC 7403	1910155-00	47
2	E47, E48	IC 7489	1910396-00	48
1	E50	IC 74H106	1910408-00	49
3	E80, E81, E87	IC 74H103	1910409-00	50
1	E42	IC 74123	1910436-00	51

CHK	CHANGE NO.	REV

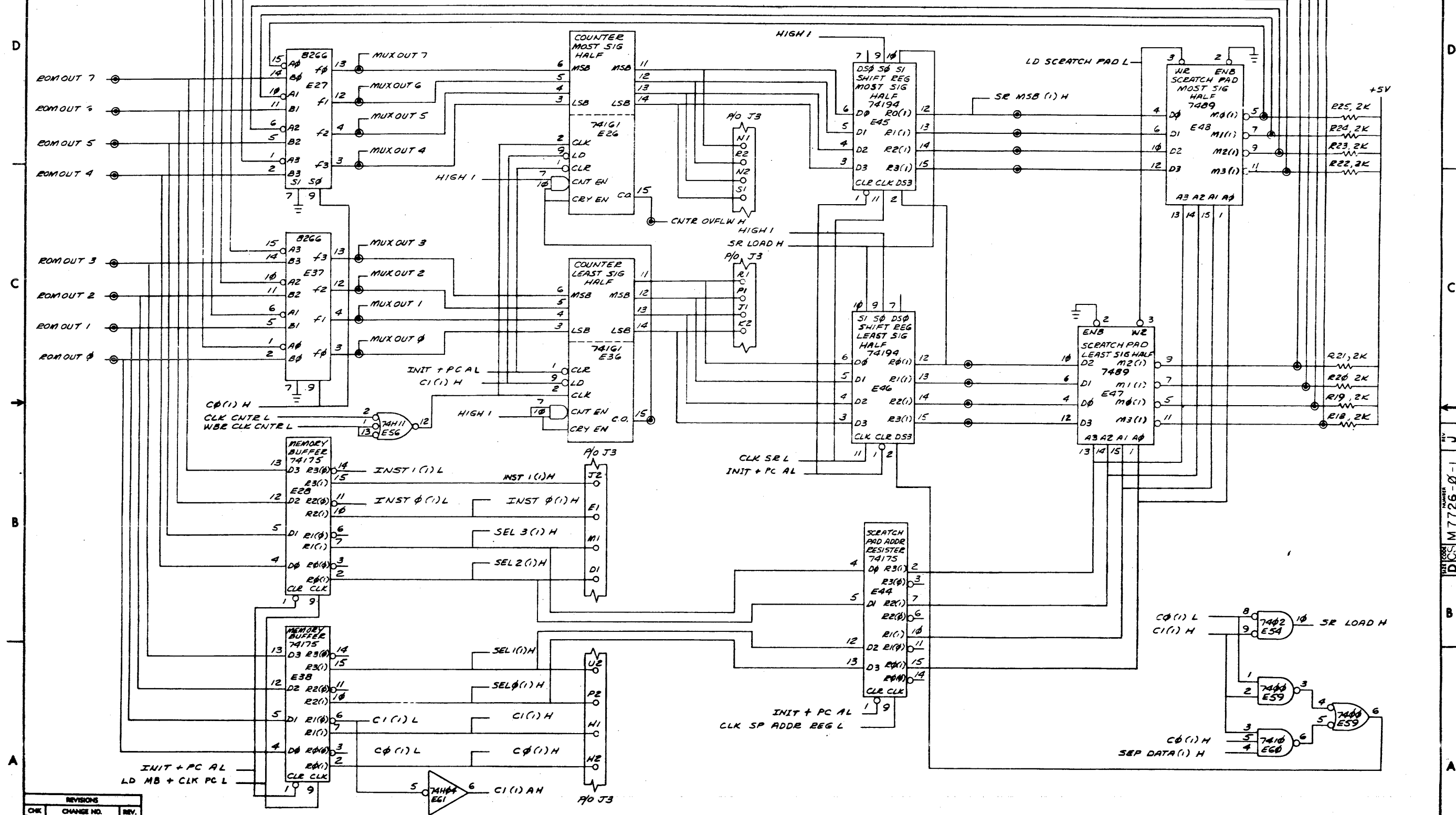
PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
2	E45, E46	IC 74194	1910623-00	52
8	E23, E24, E25, E26, E30, E31, E32, E36	IC 74161	1910650-01	53
3	E84, E85, E86	IC 74174	1910652-00	54
1	E53	IC 7427	1910878-00	55
3	E28, E38, E44	IC 74175	1910651-00	56
2	E10, E66	IC 8640	1911469-00	57
1	E33	IC 2102 680 NS	2111318-02	58
				59
6	E35, E39, E62, E63, E73, E83	SAME IC SPACES		60
1	E67	CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
4	E41, E71, E93, E52	IC 74574	1910544-00	62
1	E51	IC 74H10	1909057-00	63
1	E77	IC 74H40	1905584-00	64
				65
1/2		30 AWG SOLID WIRE (MEL)	9108740-55	66
1	J1	CONN 40 PIN RT ANG HDR	1209941-02	67
1	(J1)	LATCH, LEFT FOR RT ANG HDR	1209941-03	68
1	(J1)	LATCH, RIGHT FOR RT ANG HDR	1209941-04	69
1	E13	IC 256 X 4 ROM FLD0L	23111A2	70
1	E3	IC 256 X 4 ROM FLD0H	23421A2	71
1	E14	IC 256 X 4 ROM FLD1L	23257A2	72
1	E4	IC 256 X 4 ROM FLD1H	23258A2	73
1	E15	IC 256 X 4 ROM FLD2L	23115A2	74
1	E5	IC 256 X 4 ROM FLD2H	23116A2	75
1	E16	IC 256 X 4 ROM FLD3L	23117A2	76
1	E6	IC 256 X 4 ROM FLD3H	23118A2	77
1	E17	IC 256 X 4 ROM FLD4L	23259A2	78
1	E7	IC 256 X 4 ROM FLD4H	23260A2	79
1	E18	IC 256 X 4 ROM FLD5L	23121A2	80
1	E8	IC 256 X 4 ROM FLD5H	23122A2	81
1	R33	RES 150 1/4W 5% CC	1300250-00	82

SAME I.C. GATES			
TYPE	LOCATION	PINS	DESCRIPTION
74H04	E61	1,2	INVERTER
7404	E64	12,13	INVERTER
7404	E76	12,13	INVERTER
7408	E11	6,3,3,8,9,10	2 INPUT AND
74H00	E72	1,2,3,9,6,8,9,10	2 INPUT NAND
7437	E65	8,9,10	2 INPUT NAND BUFFER
8001	E2	8,9,10	2 INPUT NAND G.C.
74H10	E51	3,4,5,6	3 INPUT NAND
74H40	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E84	4,5,6	2 INPUT NOR
8640	E66	2,6,7,11,12,13,8,6	2 INPUT NOR ACVR
7427	E53	1,2,12,13	2 INPUT NOR
7486	E92	4,5,6	2 INPUT XOR
7486	E74	1,2,3,4,5,6	2 INPUT XOR
74574	E52	1,2,3,4,5,6	DTYPE FLIP FLOP
74H106	E80	1,2,3,4,14,15,16	J-K FLIP FLOP
74123	E42	1,2,3,4,13,14,16	ONE SHOT

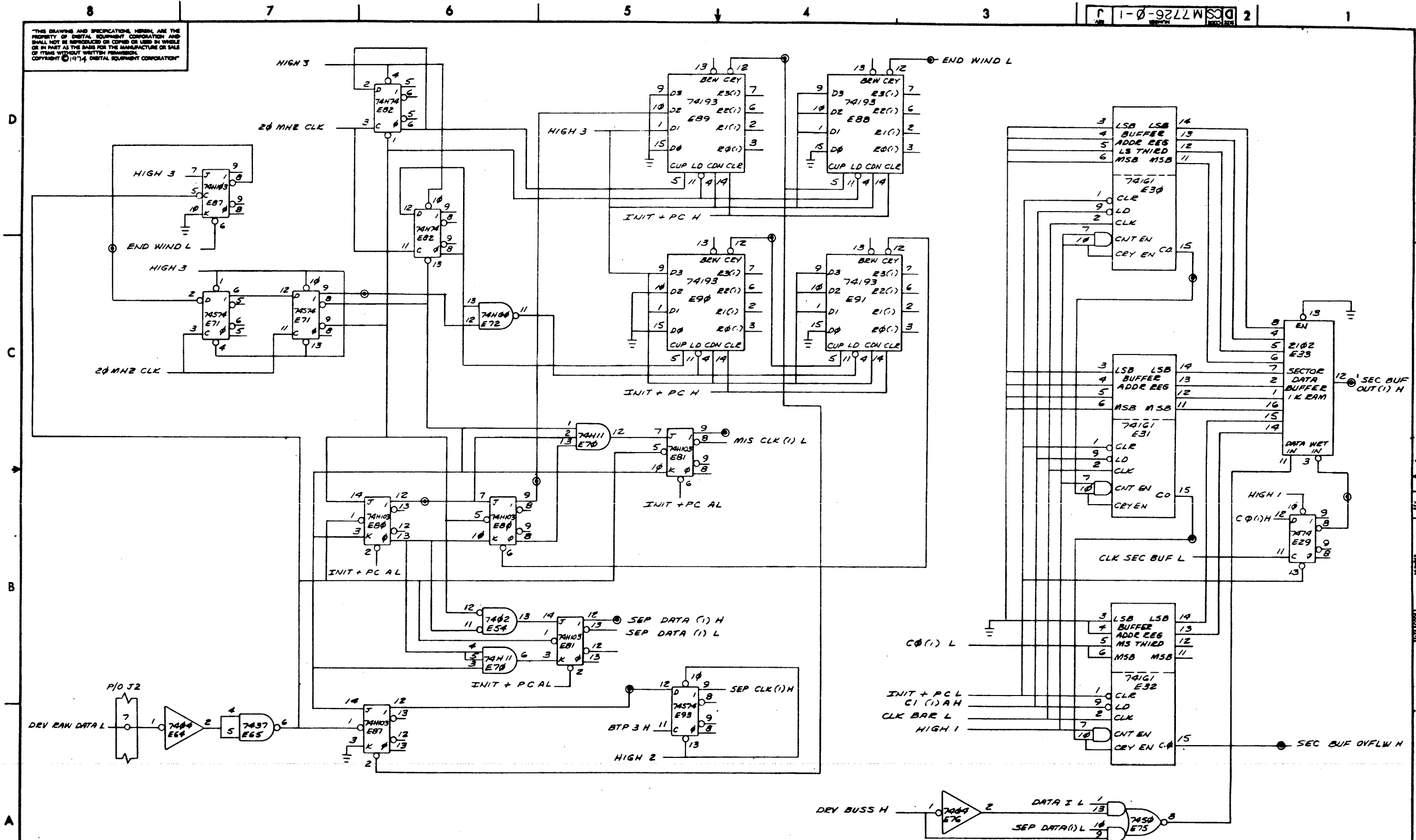
ALLOWABLE SUBSTITUTIONS				
PREFERRED			REPLACEMENT	
TYPE	ITEM #	P.N.	TYPE	P.N.
7489	48	1910396-00	3101A	1910653-00
7489	48	1910396-00	8225	1911162-00

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REVISIONS		
CHK	CHANGE NO.	REV.

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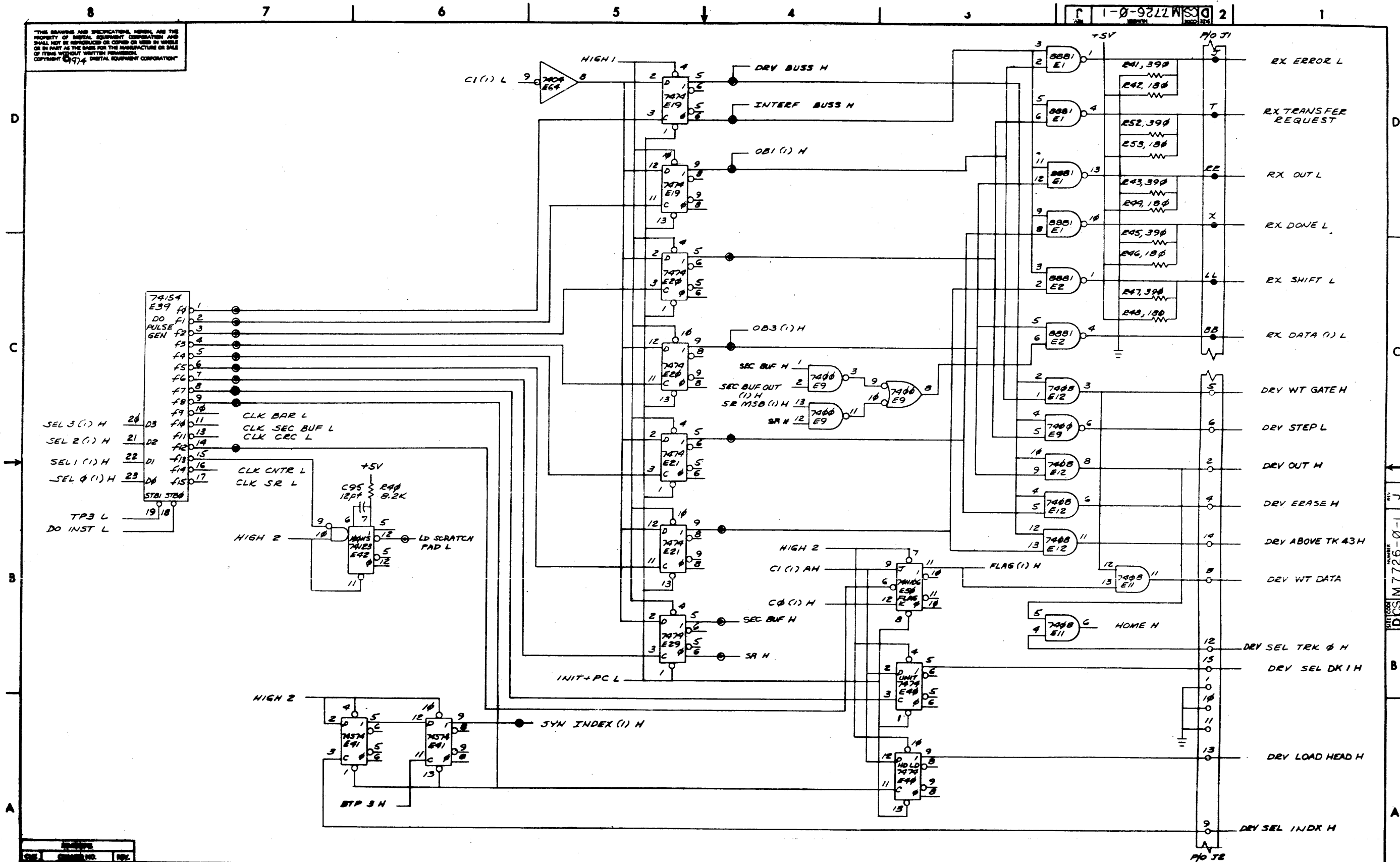


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FLOPPY DISK CONTROLLER (D4)	SIZE CODE	DCS	NUMBER	M7726-0-1	REV.	J
SCALE	1:1	SHEET	4	OF	9	DIST.	

DCS M7726-0-1

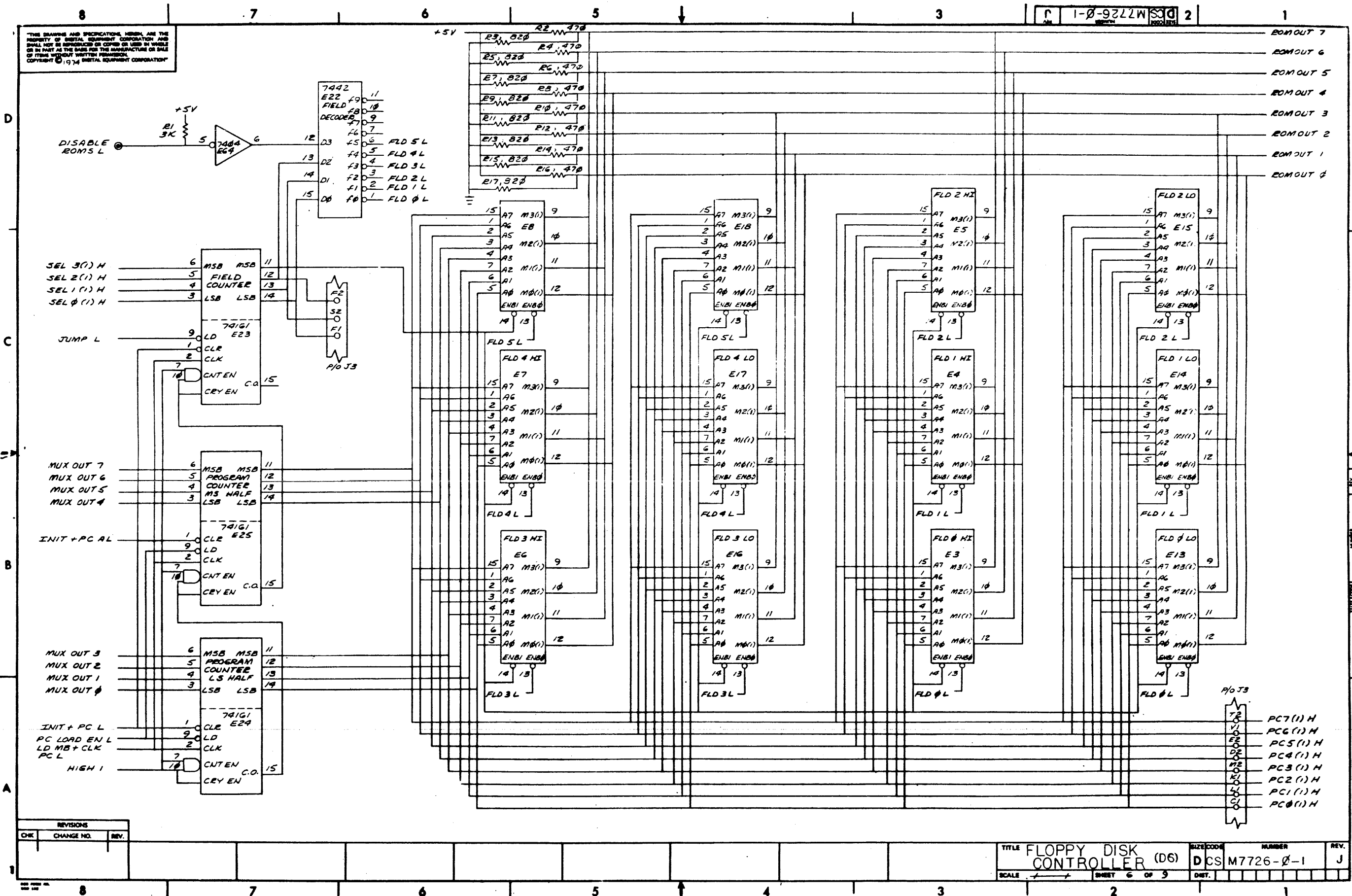
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REV.	DESCRIPTION	DATE

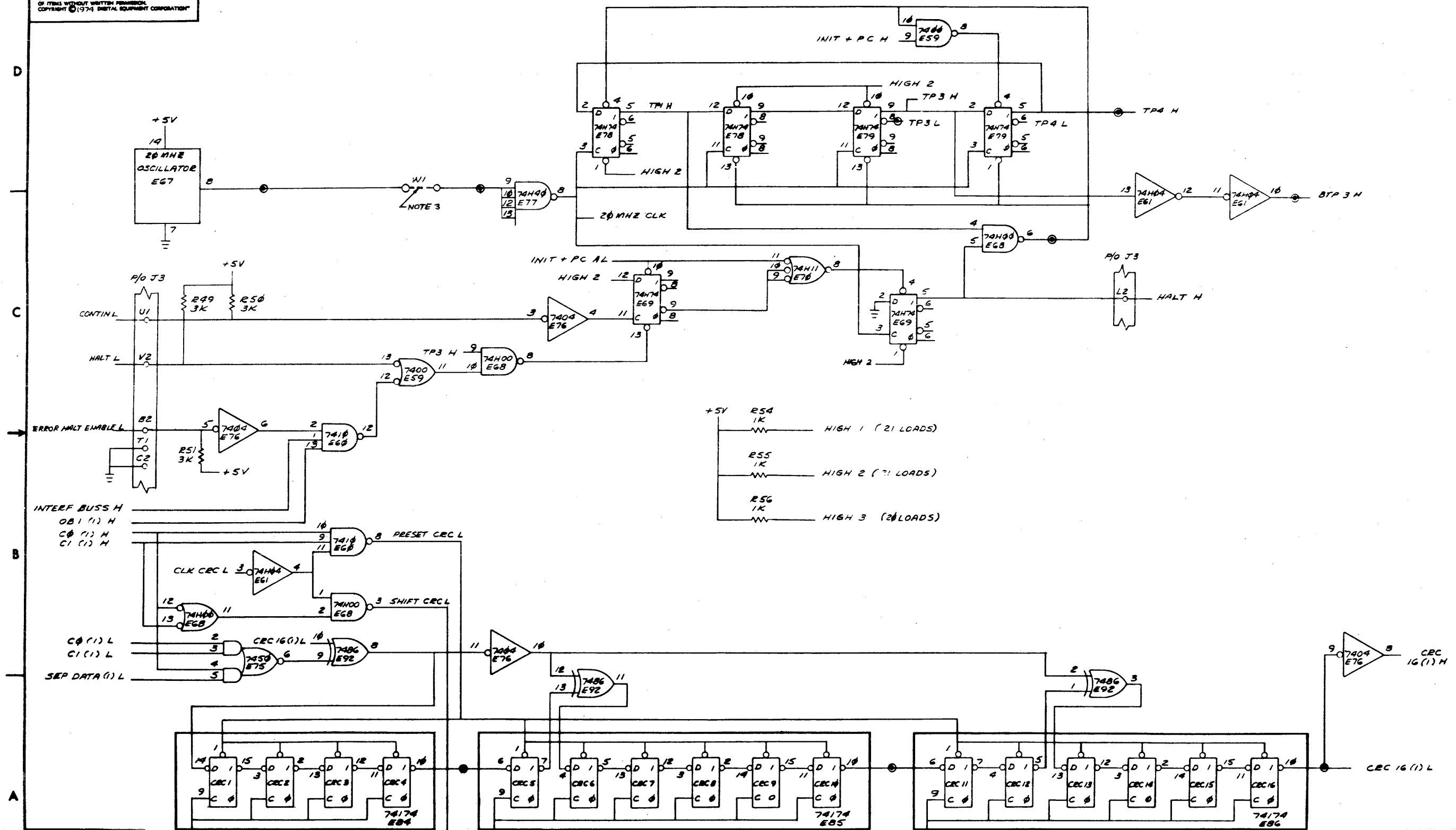
DCSM 7726-0-1 J

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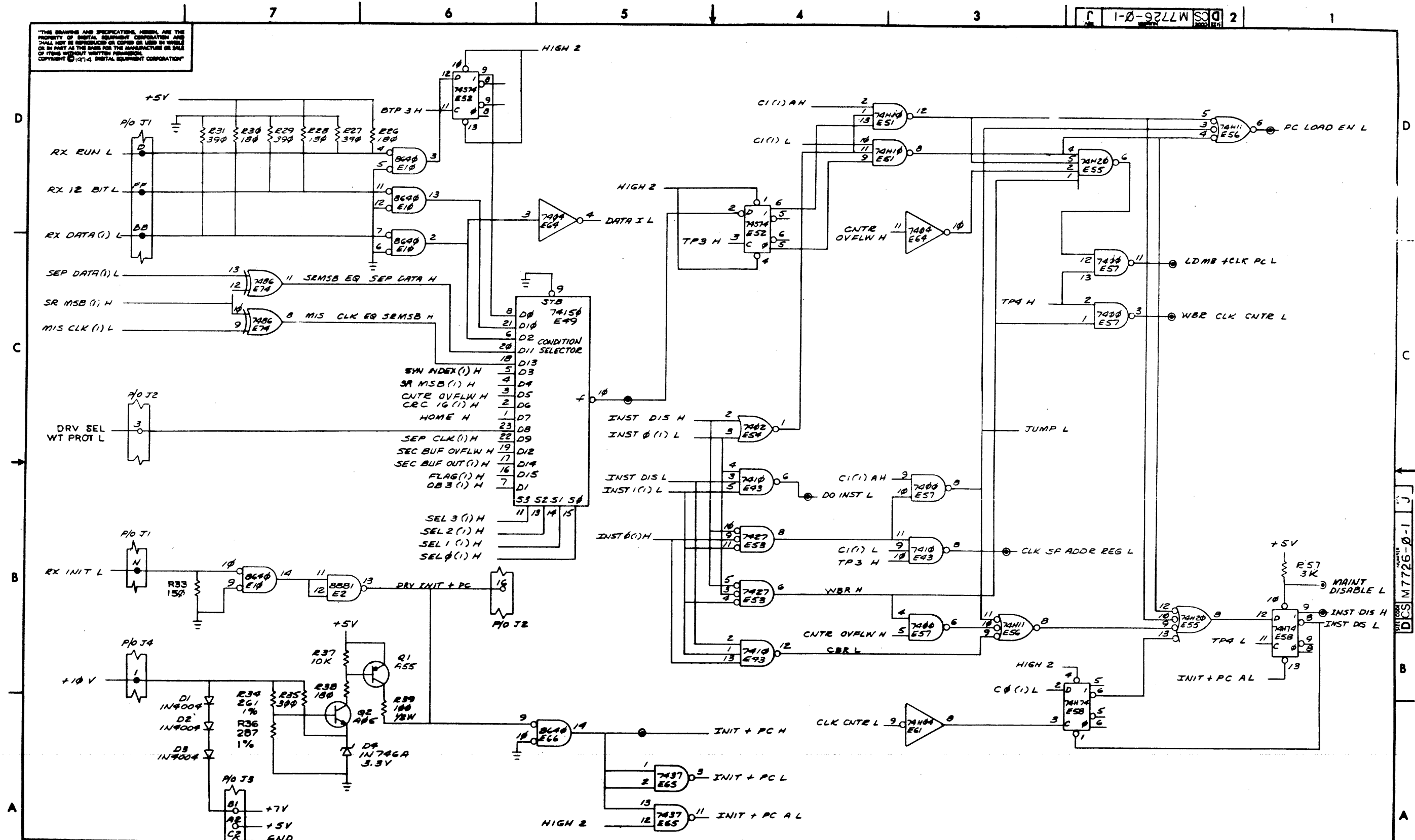
REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
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8	D0	74150	E49
21	D1	74150	E49
6	D2	CONDITION	
20	D11	SELECTOR	
18	D13		
5	D3		
4	D4		
3	D5		
2	D6		
7	D7		
23	D8		
22	D9		
19	D12		
17	D14		
16	D15		
7	D1		
53	S2	S1	S0
11	13	14	15

REV.	CHG.	DATE	BY

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THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE REFERS TO SIGNALS ON THE INTERFACE BUSS
 DRIVE REFERS TO SIGNALS ON THE DRIVE BUSS
 POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
 KM11 REFERS TO SIGNALS ON J3 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
BTP 3 H	D7-C1	D4-A5, D5-A6, D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CNTR L	D5-H7	D3-R7, D8-A4
CLK CRC L	D5-C7	D7-B7
CNTR OVFLW H	D3-C5	D8-D4, D8-C6, D8-B4
CLK SEC BUF L	D5-C7	D4-B2
CLK SP ADDR REG L	D8-B3	D3-A4
CLK SR L	D5-H7	D3-B4
CONTIN L	KM11	D7-C7
CRC16 (1) H	D7-H1	D8-C6
CRC16 (1) L	D7-A1	D7-B7
C1 (1) AH	D3-A6	D4-B3, D5-B4, D8-D4, D8-C4
C1 (1) H	D3-A6	D3-C6, D3-B2, D7-B8
C1 (1) L	D3-A6	D5-D6, D7-R8, D8-D4, D8-B4
C0 (1) H	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-R8
C0 (1) L	D3-A6	D3-B2, D4-B3, D7-R8, D8-B3
DATA I L	D8-D5	D4-A2
DISABLE ROMS L	TEST PAD	D8-D8
DO INST L	D8-H4	D5-H4
DRV BUSS H	D5-D4	D4-A4
DRV ERASE H	D5-D1	DRIVE
DRV OUT H	D5-C1	DRIVE
DRV LOAD HEAD H	D5-A1	DRIVE
DRV STEP L	D5-C1	DRIVE
DRV INIT + PC	D8-H6	DRIVE
DRV ABOVE TK 43 H	D5-B1	DRIVE
DRV RAM DATA L	DRIVE	D4-A8
DRV SEL DK 1 H	D5-B1	DRIVE
DRV SEL INDX H	DRIVE	D5-A1
DRV SEL TRK 0 H	DRIVE	D5-B1
DRV WT DATA	D5-B1	DRIVE
DRV WT GATE H	D5-C1	DRIVE
DRV CEL WT PROT L	DRIVE	D8-C9
RND WIND L	D4-D3	D4-D8
ERRR HLT ENABLE L	KM11	D7-C7

D81 (1) H	D5-D4	D7-R8
D83 (1) H	D5-C4	D8-B6
PC 0 (1) H	D6-A1	KM11
PC 1 (1) H	D6-A1	KM11
PC 2 (1) H	D6-A1	KM11
PC 3 (1) H	D6-A1	KM11
PC 4 (1) H	D6-A1	KM11
PC 5 (1) H	D6-A1	KM11
PC 6 (1) H	D6-A1	KM11
PC 7 (1) H	D6-A1	KM11
PC LOAD EN L	D8-D1	D6-A8
ROM OUT 0	D6-D1	D3-C8
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	D8-B8
RX OUT L	D5-D1	INTERFACE
RX RUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
PX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 MIT L	INTERFACE	D8-D8
SKC BUF OVFLW H	D4-A1	D8-C6
SKC HUF OUT (1) H	D4-C1	D5-C4, D8-R6
SKC HUF H	D5-H4	D5-C4
SFL 0 (1) H	D3-A6	D5-C8, D6-C8, D8-R6, KM11
SEL 1 (1) H	D3-A6	D5-C8, D6-C8, D8-R6, KM11
SEL 2 (1) H	D3-B6	D5-C8, D6-C8, D8-R6, KM11
SEL 3 (1) H	D3-B6	D5-C8, D6-C8, D8-R6, KM11
SEP CLK (1) H	D4-B4	D8-C6
SEP DATA (1) H	D4-H5	D3-A2
SEP DATA (1) L	D4-B5	D4-A2, D7-A8, D8-C8
SR H	D5-B4	D5-C4
SR LOAD H	D3-B1	D3-C4
SR MSB (1) H	D3-D3	D5-C4, D8-C8, D8-C6
SIN INDEX (1) H	D5-A5	D8-C6

FLAG (1) H	D5-B3	D8-B6
FLD 0 L	D6-D6	D6-A3, D6-A2
FLD 1 L	D6-D6	D6-B3, D6-B2
FLD 2 L	D6-D6	D6-C3, D6-C2
FLD 3 L	D6-D6	D6-A6, D6-A4
FLD 4 L	D6-D6	D6-B6, D6-B4
FLD 5 L	D6-D6	D6-C6, D6-C4
HALT H	D7-C3	KM11
HALT L	KM11	D7-C7
HIGH 1	D7-C4	D3-D6, D3-D4, D3-C6, D3-C4, D4-A3
HIGH 2	D7-B4	D4-B1, D5-D5, D6-A8
HIGH 3	D7-B4	D4-A5, D5-B7, D5-A7, D5-B4, D7-D5
HOME H	D5-B2	D7-D4, D7-C4, D7-C5, D8-D5, D8-B3
INIT + PC A L	D8-A4	D8-A5
INIT + PC H	D8-A4	D3-C6, D3-B4, D3-A4, D3-A7, D4-B6
INIT + PC L	D8-A4	D4-B5, D6-B8, D7-C5, D8-B2
INST 0 (1) H	D3-B6	D4-D5, D4-C5, D7-D4
INST 0 (1) L	D3-B6	D4-B3, D5-B5, D6-A8
INST 1 (1) H	D3-B6	KM11, D8-B5
INST 1 (1) L	D3-B6	DR-C5
INST DIS H	D8-B1	KM11
INST DIS L	D8-B1	D8-H5
INTERF BUSS H	D5-D4	D8-C5
JUMP L	D8-C3	D8-H5
LD MR + CLK PC L	D8-C1	D8-H5
LD SCRATCH PAD L	D5-H6	D7-R8
MAINT DIS L	TEST PAD	D6-CN
MIS CLK (1) L	D4-C4	D8-B1
MUX OUT 0	D3-C7	D8-C8
MUX OUT 1	D3-C7	D6-A8
MUX OUT 2	D3-C7	D6-A8
MUX OUT 3	D3-C7	D6-B8
MUX OUT 4	D3-C7	D6-B8
MUX OUT 5	D3-D7	D6-B8
MUX OUT 6	D3-D7	D6-B8
MUX OUT 7	D3-D7	D6-B8

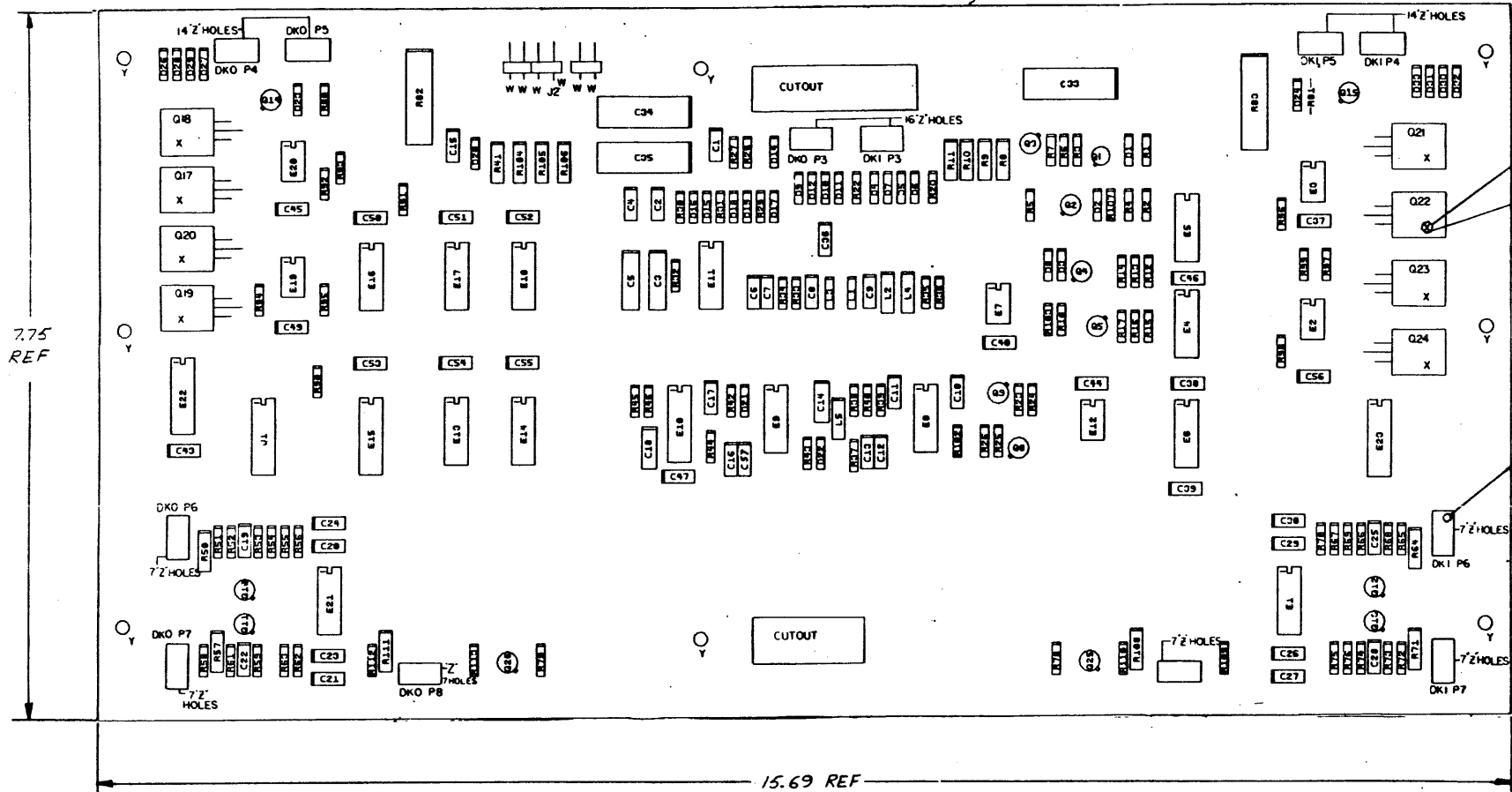
TP3 H	D7-D3	D7-C6, D8-B4, D8-C5
TP3 L	D7-D3	D5-B8
TP4 H	D7-D2	D8-C3
TP4 L	D7-D3	D8-B2
WRR CLK CNTR L	D8-C2	D3-B7
20 MHZ CLK	D7-C5	D4-C8, D4-D7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4, D8-A7
+7V	POWER SUPPLY	KM11
+10V	POWER SUPPLY	D8-B8

REVISIONS		
CHK	CHANGE NO.	REV.

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NOTES:

1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/4W, ±5%.
2. WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE D41CB TRANSISTOR ONLY BY G.E.. THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.
- * 3. FOR TEST SEE NOTE ON PAGE 3 OF D-CS-M7727
4. DEC PART # 13-0166B MAY BE USED FOR INSERTION IF 13-01320 IS NOT AVAILABLE.
5. R32 RES. MAY ALSO BE CHANGED AT SYSTEM TEST.



SEE NOTE 2

IC TYPE	QTY	LOC
7473	11	4
73451	4	8
74157	6	16
75452	4	8
74129	8	16
IC TYPE	QTY	LOC

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REVISIONS

1	H. B. B. (3-1-74)	INITIALS
2	H. B. B. (3-1-74)	INITIALS
3	H. B. B. (3-1-74)	INITIALS
4	D. SWICKER (7 NOV 77)	INITIALS
5	R. C. M7727-0003 D	INITIALS
6	M. SWAN (10-1-77)	INITIALS
7	V. SMITH	INITIALS
8	W. SMITH	INITIALS
9	JM7727-00002 C	INITIALS
10	C. YOUSE	INITIALS
11	W. CLARK (10-8-75)	INITIALS
12	CM7727-00001 B	INITIALS
13	CM7727-00001 REV.	INITIALS

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.																
FIRST USED ON OPTION MODEL M7727																				
ETCH BOARD REV. B																				
PARTS LIST																				
<table border="1"> <tr> <td>DATE</td> <td>12/31/74</td> <td>DESIGNED BY</td> <td>H. B. B.</td> </tr> <tr> <td>DATE</td> <td>11/24/74</td> <td>CHECKED BY</td> <td>P. J. BROWN</td> </tr> <tr> <td>DATE</td> <td>7-24-74</td> <td>DATE</td> <td>7-24-74</td> </tr> <tr> <td>DATE</td> <td>5/1/75</td> <td>DATE</td> <td>5/1/75</td> </tr> </table>					DATE	12/31/74	DESIGNED BY	H. B. B.	DATE	11/24/74	CHECKED BY	P. J. BROWN	DATE	7-24-74	DATE	7-24-74	DATE	5/1/75	DATE	5/1/75
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DATE	7-24-74	DATE	7-24-74																	
DATE	5/1/75	DATE	5/1/75																	
TITLE: digital READ/WRITE CONTROL																				
NEXT HIGHER ASSY: + +																				
SCALE: + + +																				
SHEET 1 OF 6																				
SEMICONDUCTOR CONVERSION CHART																				
DEC NO.	EIA NO.	DEC NO.	EIA NO.	REV.																
				E																

DCS M7727-0-1 E

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PARTS LIST

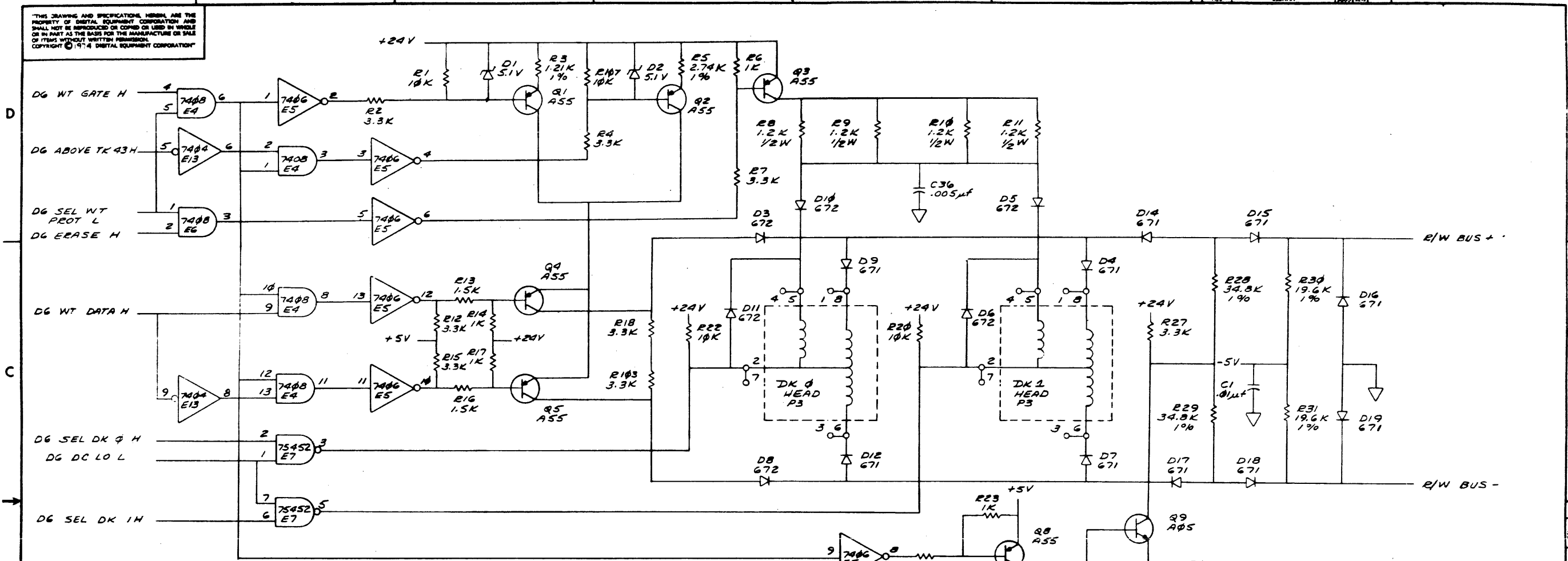
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	TRM
		X-Y COORDINATE HOLE LOCATION	K-CO-M7727-0-4	1
		ASSY/ DRILL HOLE LAYOUT	D-AM-M7727-0-5	2
		MODULE ECO HISTORY	B-MH-M7727-0-6	3
1		ETCHED CIRCUIT BOARD	D-1A-5011370-00	4
2	C17, C18	CAP 100 pf	1000016-00	5
1	C9	CAP 180 pf	1000020-00	6
2	C8, C14	CAP 220 pf	1000021-00	7
32	C1, C2, C4, C10, C11, C15 C16, C20, C21, C23, C24 C26, C27, C29, C30, C37, C38, C39, C40, C43 C44, C45, C46, C47 C49 - C57	CAP .01 μf	1001610-00	8
2	C3, C5	CAP 6.8 μf 35V	1005306-00	9
2	C34, C35	CAP 190 μf	1009433-00	10
1	C33	CAP 50 μf	1000080-00	11
4	C7, C6, C12, C13	CAP .047 μf	1010978-32	12
5	C19, C25, C22, C28, C36	CAP .005 μf	1001765-00	13
10	D4, D7, D9, D12, D14 D15, D16, D17, D18, D19	DIODE D671	1103309-00	14
8	D3, D5, D6, D8, D10 D11, D21, D22	DIODE D672	1105275-00	15
10	D23, D24, D26, D27 D28, D29, D30, D31 D32, D33	DIODE 1N4004	1105796-00	16
1	D20	DIODE 1N4742 12V	1109502-00	17
2	D1, D2	DIODE 5.1V	110713-00	18
9	R90, R92 - R99	RES 150 1/4W 5%	1300250-00	19
4	R7, R104, R105, R106	RES 680 1/2W 5%	1300347-00	20
12	R6, R14, R17, R23, R24, R26, R46 R78, R79, R80, R81 R91,	RES 1K 1/4W 5%	1300365-00	21
4	R8 - R11	RES 1.2K 1/2W 5%	1300385-00	22
6	R50, R57, R64, R71, R88, R111	RES 68 1/2W 5%	1309405-00	23
7	R3, R16, R53, R62 R68, R75, R102	RES 1.5K 1/4W 5%	1300391-00	24
4	R35, R36, R39, R40	RES 511 1/8W 1%	1302411-00	25
1	R5	RES 2.74K 1/8W 1%	1304868-00	26
11	R2, R4, R7, R12, R15 R18, R19, R25, R27 R42, R43	RES 3.3K 1/4W 5%	1300439-00	27
4	R1, R20, R22, R44 R45, R187	RES 10K 1/4W 5%	1300479-00	28
11	R3, R37, R38, R52 R58, R63, R66, R72 R76, R109, R112	RES 1.21K 1/8W 1%	1302871-00	29
1	R52	RES 220 Ω 1/8W 1%	1300271-00	30
2	R33, R34	RES 464 1/8W 1%	1303047-00	31
2	R28, R29	RES 34.8K 1/8W 1%	1303156-00	32
4	R51, R61, R65, R73	RES 10K 1/8W 1%	1303312-00	33
2	R82, R83	RES 100 5W 5%	1309094-00	34
2	R30, R31	RES 19.6K 1/8W 1%	1309419-00	35
6	R55, R59, R67, R74 R110, R113	RES 4.64K 1/4W 1%	1304856-00	36

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	TRM
1	L5	CHOKE 1000 MHY	1602723-00	37
2	L2, L4	CHOKE 33 MHY	1601759-00	38
2	L1, L3	CHOKE 120 MHY	1610663-00	39
1	E17	I.C. 7450	1905580-00	40
2	E16, E18	I.C. 7473	1905587-00	41
1	E14	I.C. 7402	1909004-00	42
1	E13	I.C. 7404	1909686-00	43
2	E4, E6	I.C. 7408	1910155-00	44
3	E1, E9, E21	I.C. 1414	1910337-00	45
5	E2, E3, E12, E19, E20	I.C. 75451	1910406-00	46
1	E10	I.C. 74123	1910436-00	47
2	E8, E11	I.C. 72733	1910644-00	48
1	E15	I.C. 74157	1910655-00	49
1	E5	I.C. 7406	1910741-00	50
1	J1	I.C. SOCKET 16 PIN	1211813-02	51
9	Q9 THRU Q15, Q25, Q26	TRANS MIXA05	1510705-00	52
6	Q1 - Q5, Q8	TRANS MIXA55	1510706-00	53
8	Q17 - Q24	TRANS D44C8	1510421-00	54
86	2 HOLES	WIRE WRAP PIN	1210385-01	55
3	J2	CONN 2 POS	1212204-00	56
8	"X" HOLES	SCREW, PAN HD 4/40 X 5/16	9006010-01	57
8	"X" HOLES	NUT, KEP 4/40 X 1/4 X 3/32	9006557-00	58
1	E7	I.C. 75452	1910645-00	59
4	R54, R56, R69, R70	RES 14.7K 1/4W 1%	1302941-00	60

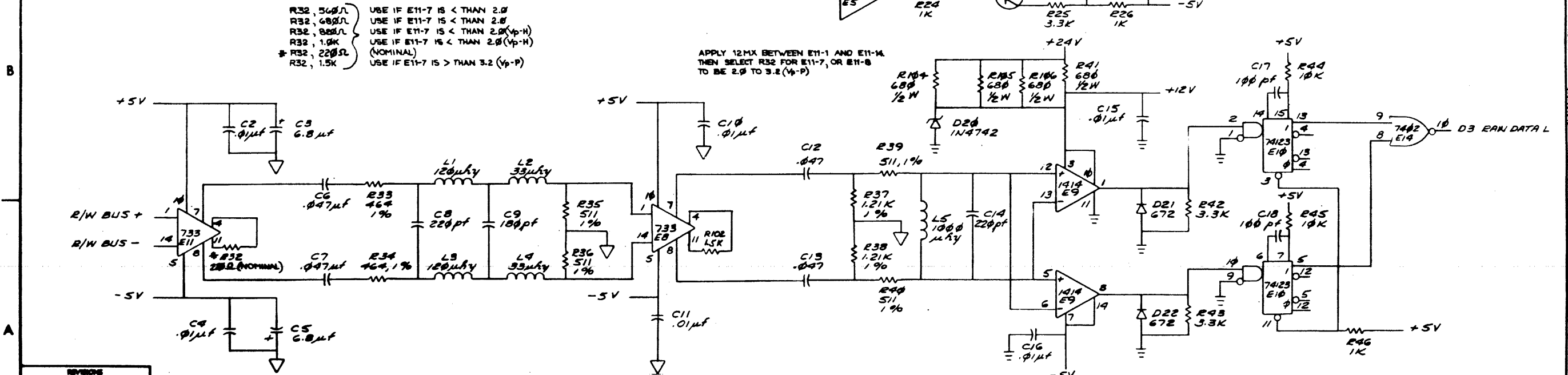
CHK	CHANGE NO.	REV.

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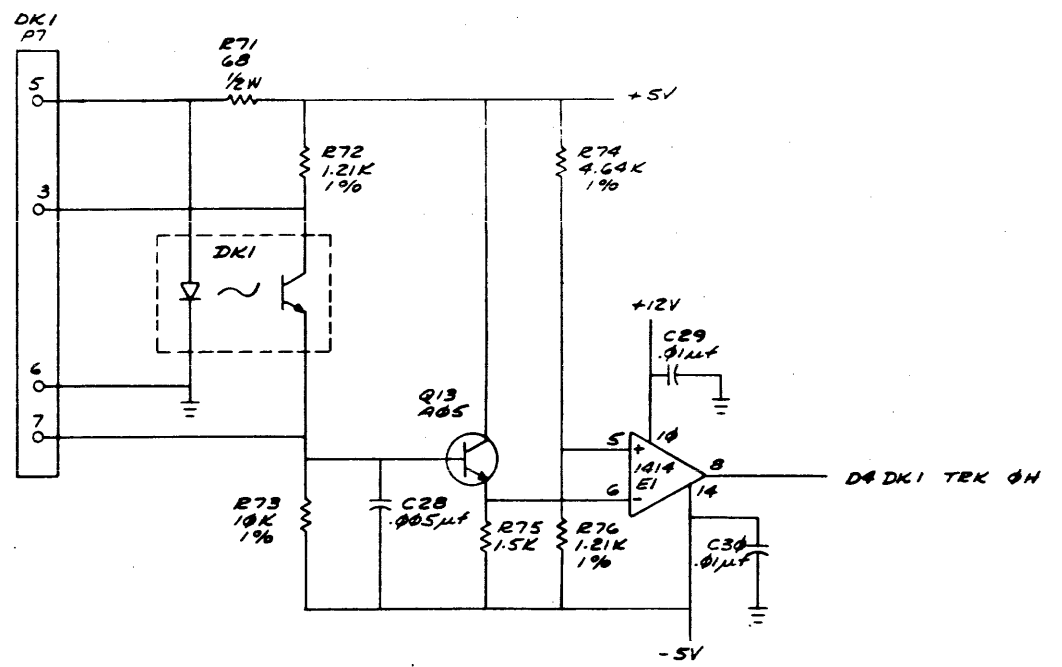
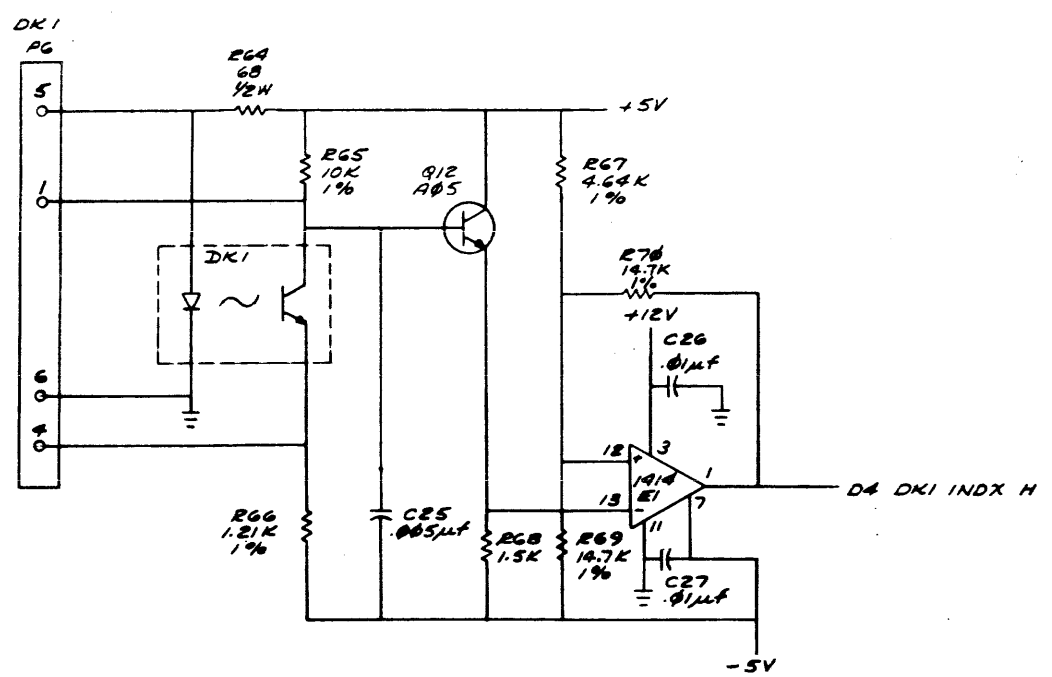
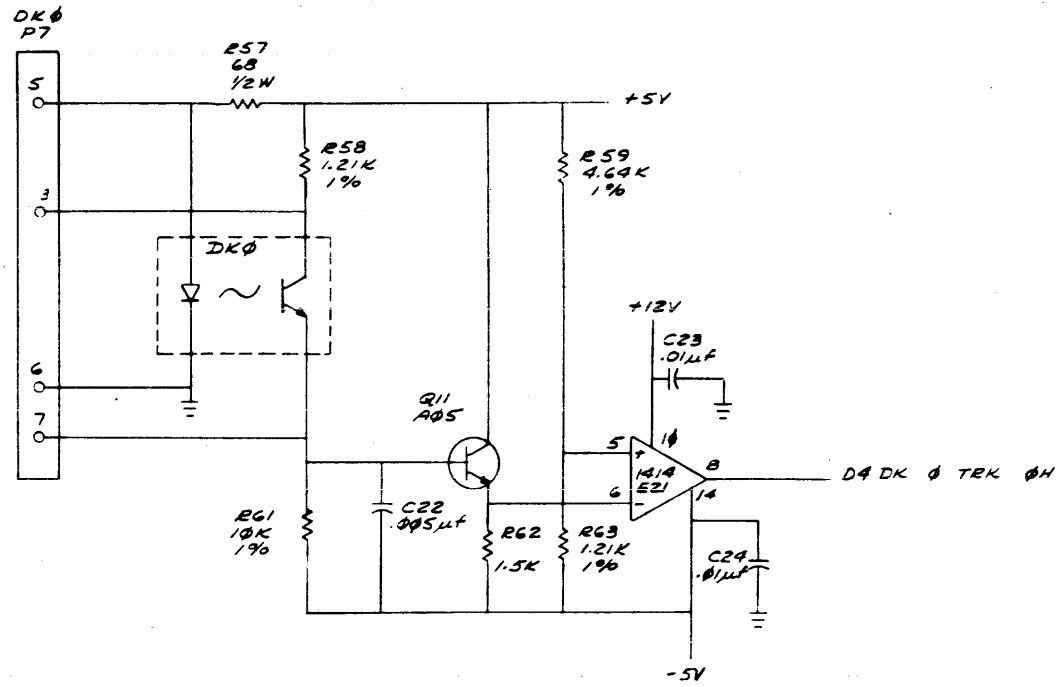
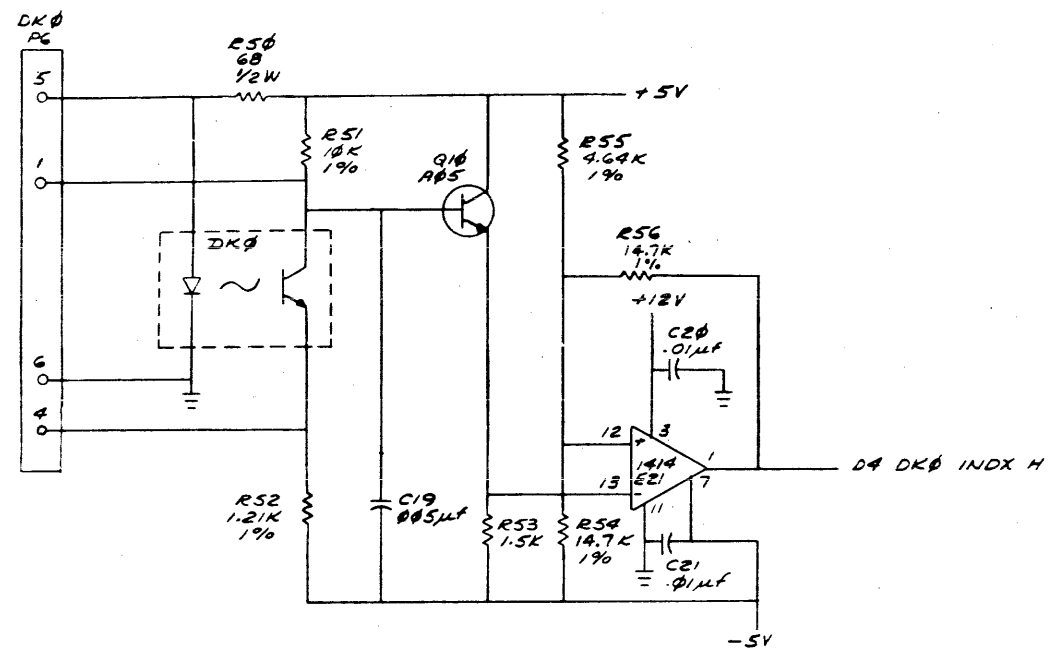
- R32, 560Ω USE IF E11-7 IS < THAN 2.0
- R32, 680Ω USE IF E11-7 IS < THAN 2.0
- R32, 820Ω USE IF E11-7 IS < THAN 2.0 (Vp-H)
- R32, 1.0K USE IF E11-7 IS < THAN 2.0 (Vp-H)
- * R32, 220Ω (NOMINAL)
- R32, 1.5K USE IF E11-7 IS > THAN 3.2 (Vp-P)

APPLY 12MX BETWEEN E11-1 AND E11-14. THEN SELECT R32 FOR E11-7, OR E11-8 TO BE 2.0 TO 3.2 (Vp-P)



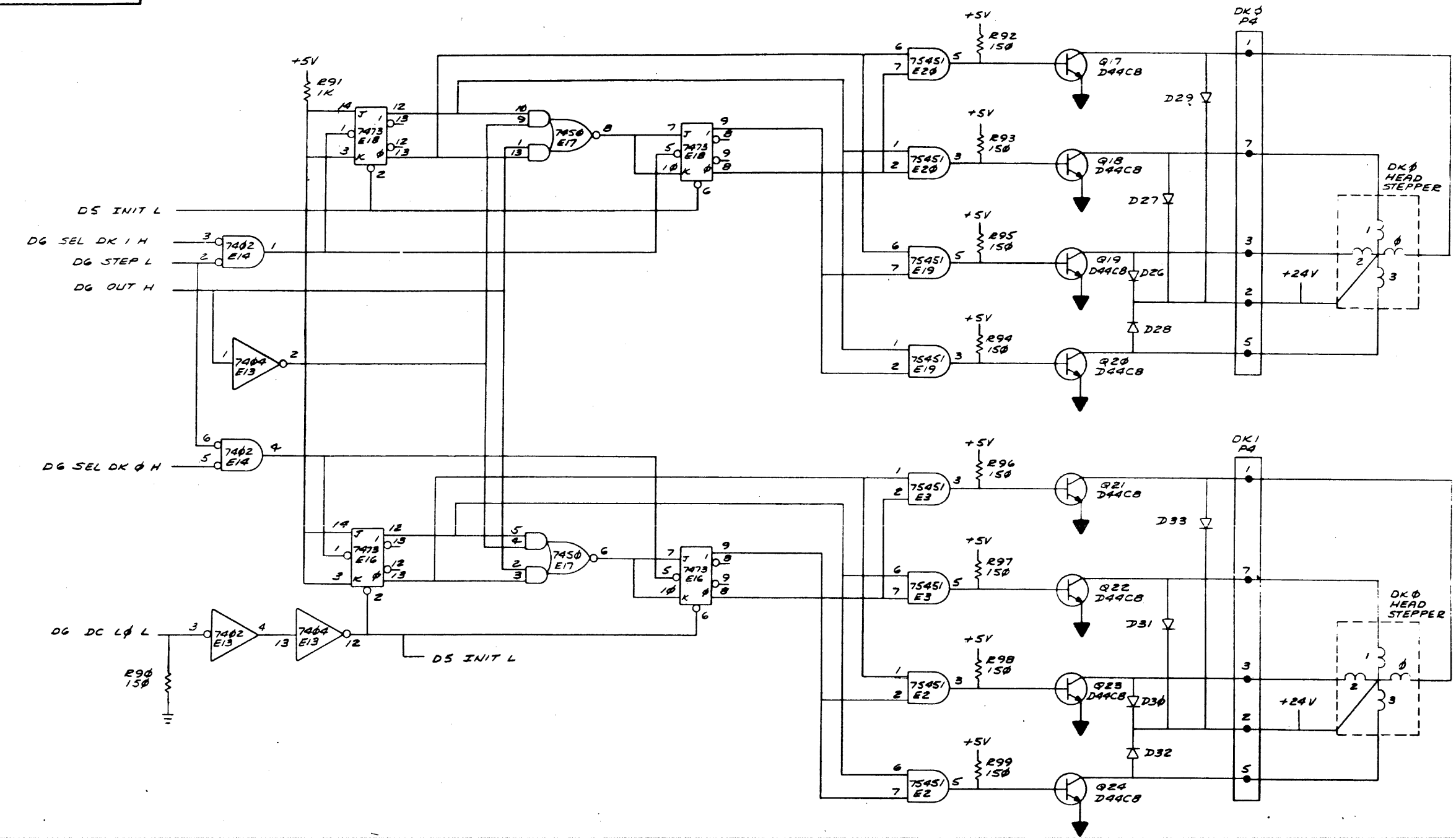
REVISIONS		
CHK	CHANGE NO.	REV.

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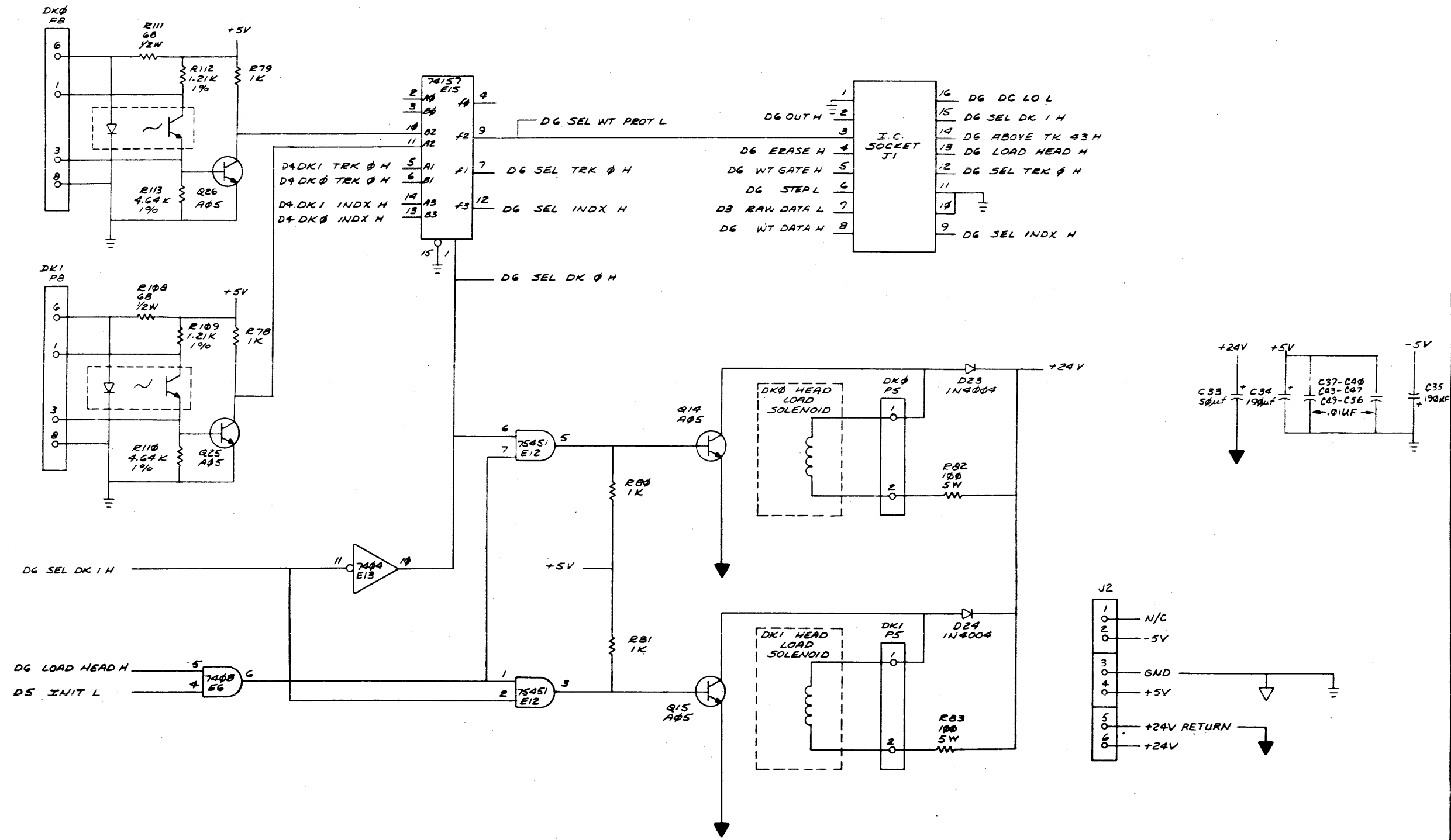
REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
OK	CHANGE NO.	REV.

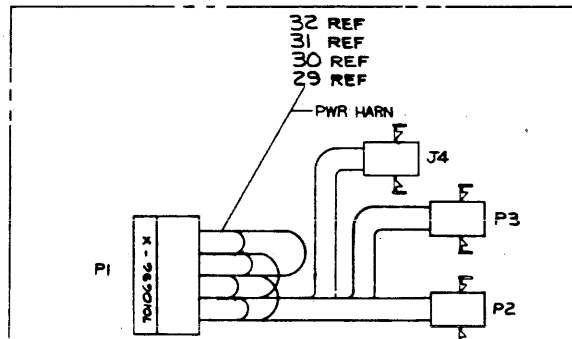
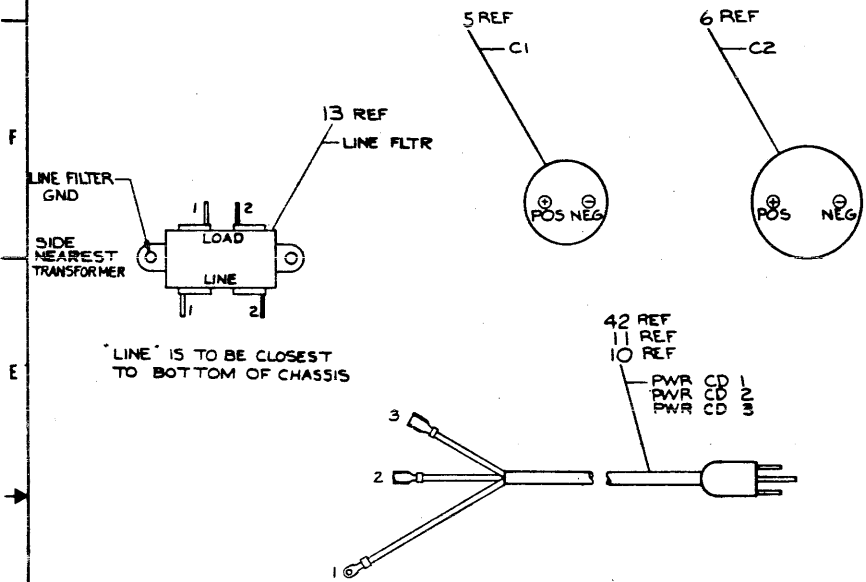
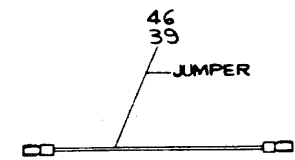
REVISIONS
 DATE CHANGE NO. BY

WIRE TABLE FOR H771-A POWER SUPPLY

ITEM NO	DESCRIPTION	FROM	TO	REMARKS
10	18 GRN	PWR CD 1-1	CHASSIS GND	
	18 WHT	PWR CD 1-2	LINE FLTR-LINE 2	
	18 BLK	PWR CD 1-3	LINE FLTR-LINE 1	
2	14 RED	PWR BD-P3	C1-POS	
	14 BLK	PWR BD-P3	C2-NEG	
	14 ORN	PWR BD-P4	C2-POS	
29-32	14 BLK	PWR BD-P6	C1-NEG	
		PWR HARN-P1	T1-J1	
3		T1-P1	PWR BD-J1	
	20 RED	T1-P2	T1-C	
	20 RED	T1-P3	T1-C	
		T1-P4	LINE FILTER-GND	
	18 BRN/YEL	T1-P5	LINE FILTER-GND	
	18 BRN/YEL	T1-P7	F1-2	33 SEE NOTE 3/4
	18 WHT	T1-P6	LINE FLTR-LOAD 2	
	18 BLK	T1-P8	LINE FLTR-LOAD 1	
	18 BLK	T1-P9	F1-1	33 SEE NOTE 3

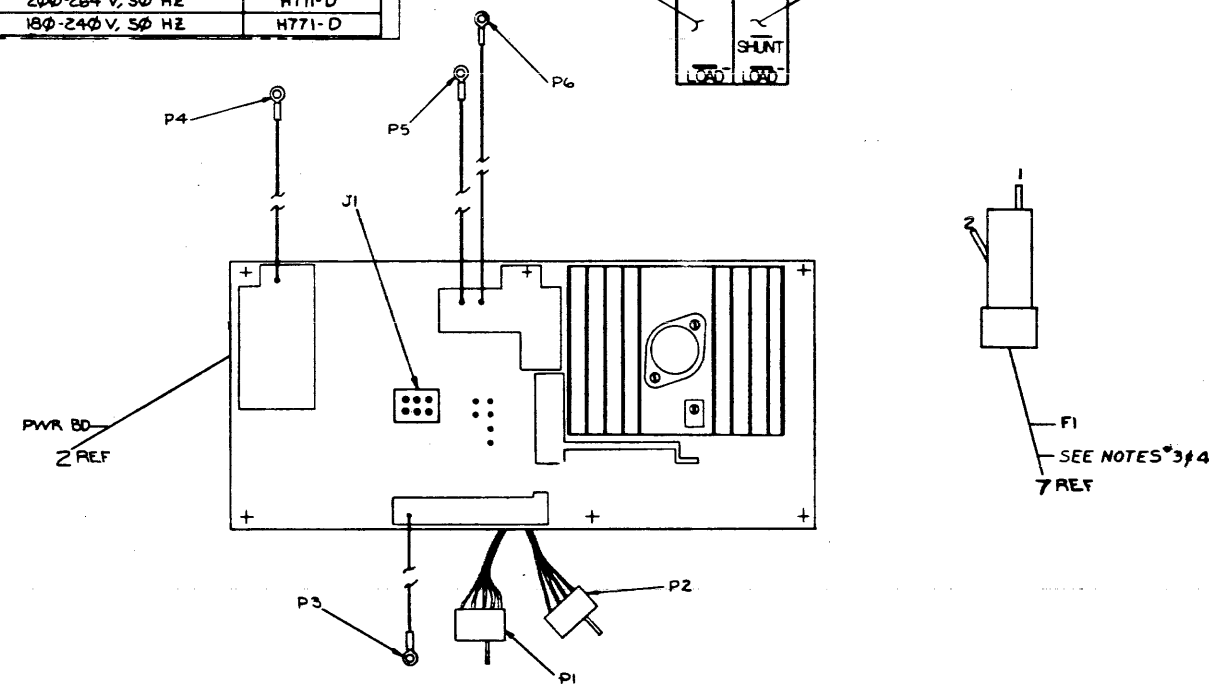
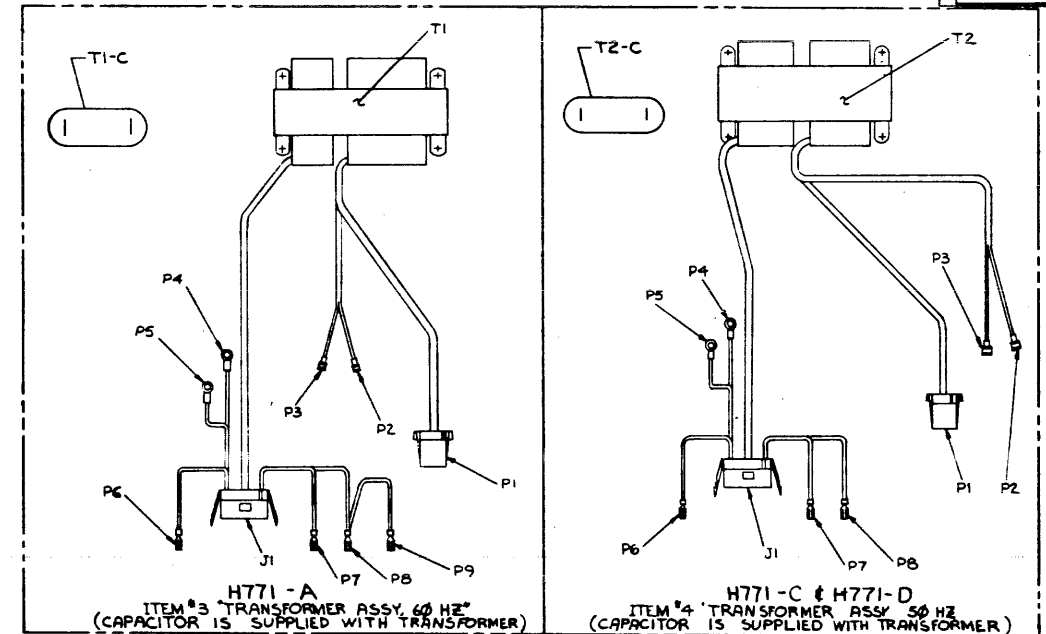
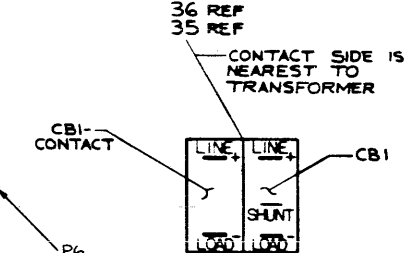
WIRE TABLE FOR H771-C/D POWER SUPPLY

ITEM NO	DESCRIPTION	FROM	TO	REMARKS	
11	18 BRN/YEL	PWR CD 2-1	CHASSIS GND		
	18 BLU	PWR CD 2-2	LINE FLTR-LINE 2		
	18 BRN	PWR CD 2-3	LINE FLTR-LINE 1		
2	14 RED	PWR BD-P3	C1-POS		
	14 BLK	PWR BD-P3	C2-NEG		
	14 ORN	PWR BD-P4	C2-POS		
29-32	14 BLK	PWR BD-P6	C1-NEG		
		PWR HARN-P1	T2-J1		
4		T2-P1	PWR BD-J1		
	20 RED	T2-P2	T2-C		
	20 RED	T2-P3	T2-C		
	18 BRN/YEL	T2-P4	LINE FILTER-GND		
	18 BRN/YEL	T2-P5	LINE FILTER-GND		
	18 BLU	T2-P6	CB1-CONTACT-LOAD		
	18 BRN	T2-P7	CB1-LOAD		
	18 BRN/YEL	T2-P8	CB1-SHUNT		
	33	18 BLU	LINE FLTR-LOAD 2	CB1-CONTACT-LINE	
	46	18 BRN	LINE FLTR-LOAD 1	CB1-CONTACT-LINE	



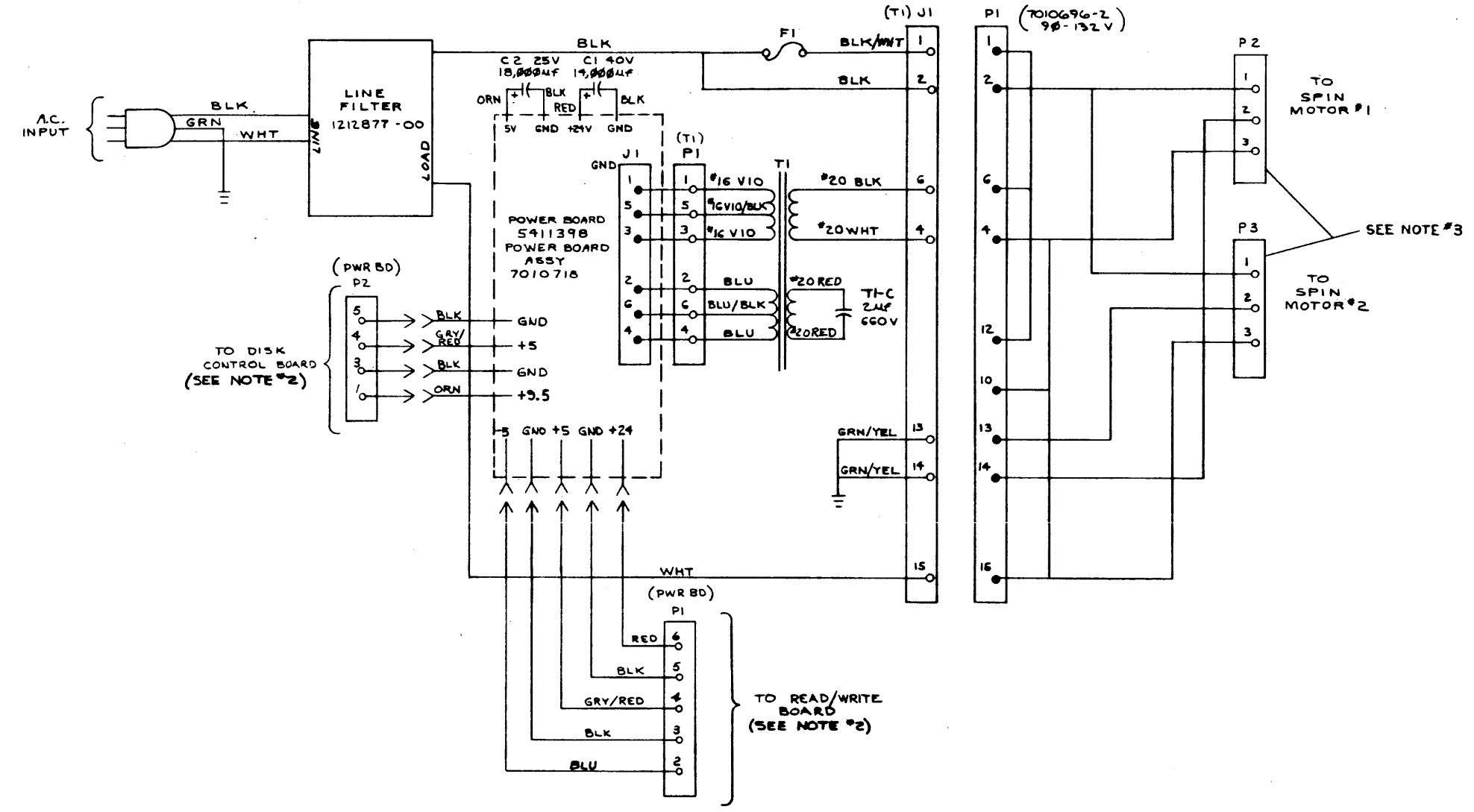
VOLTAGE TABLE (P1)

ITEM NO	VARIATION	USED ON OPTION
29	100-132 V, 50 HZ	H771-C
30	10-132 V, 60 HZ/10-120 V, 50 HZ	H771-A/H771-C
31	200-264 V, 50 HZ	H771-D
32	180-240 V, 50 HZ	H771-D



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- NOTES:
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
 2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
 3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).



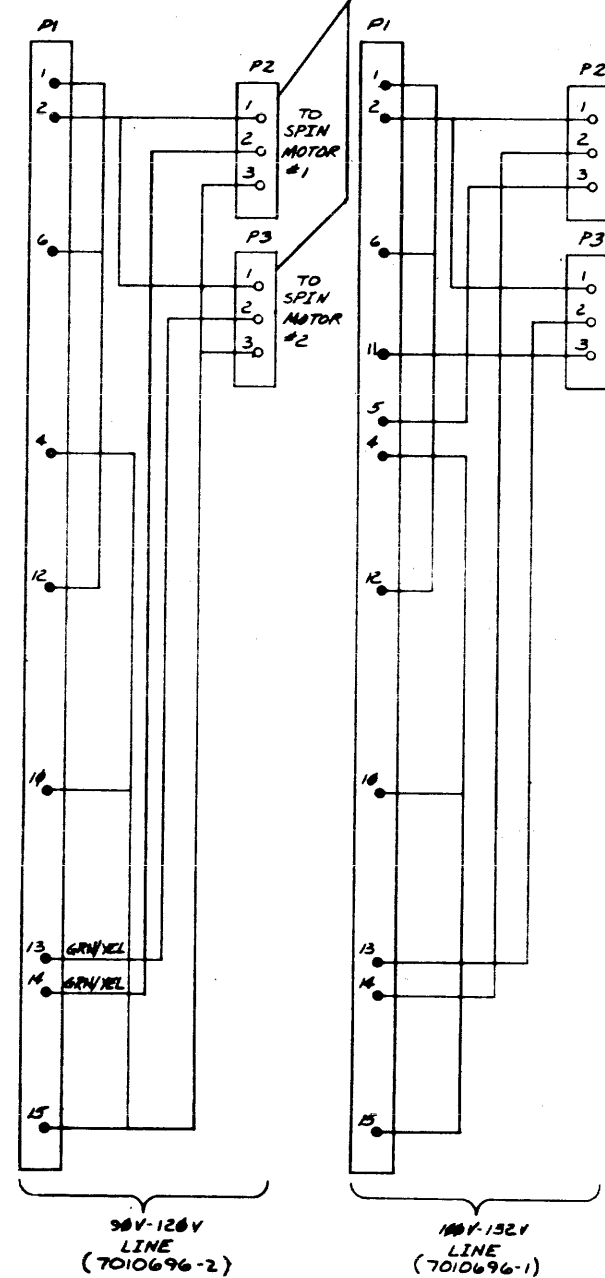
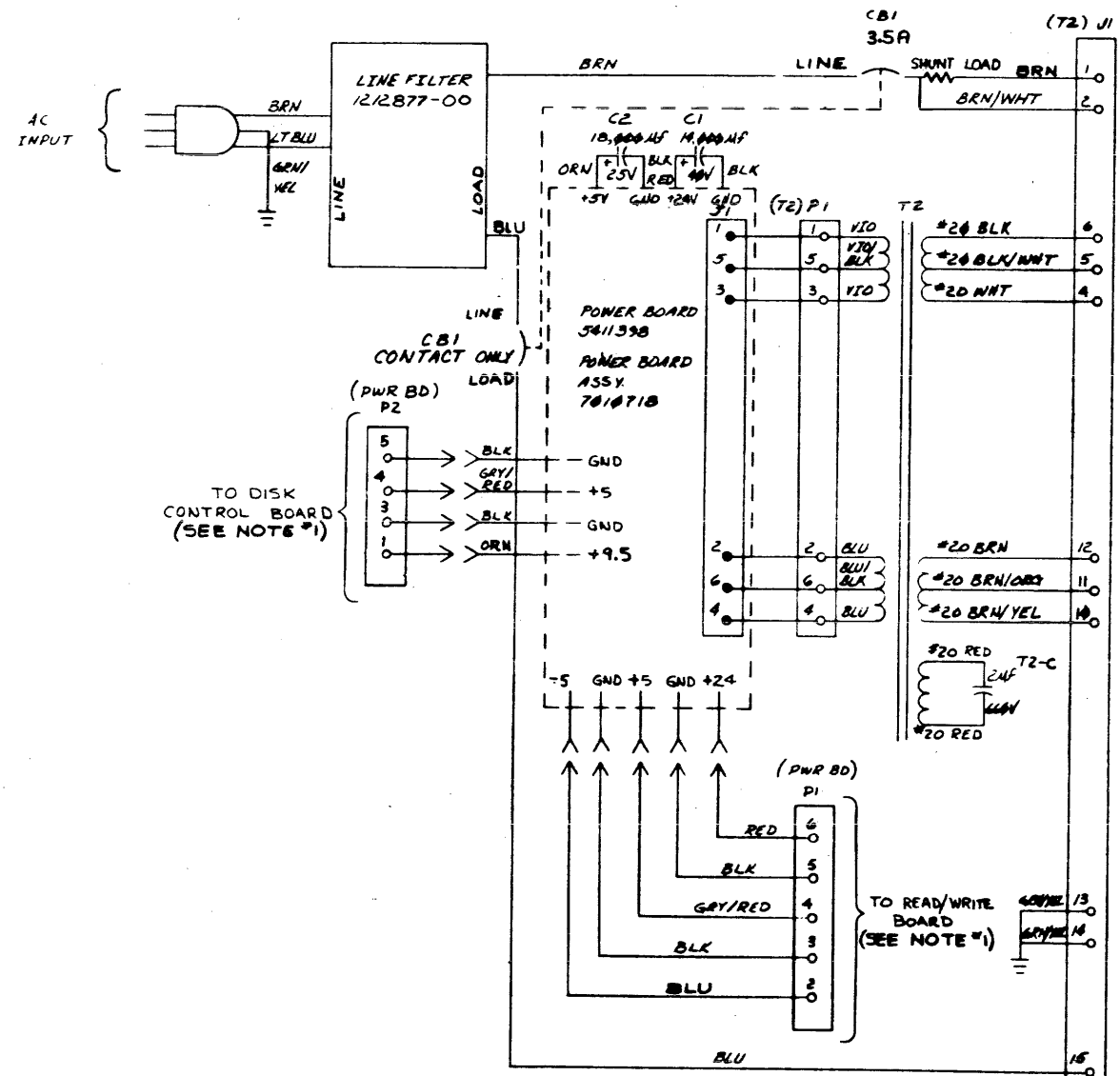
REV.	DATE	BY	CHKD	APP'D	DESCRIPTION
A	1/22/75	B. HAZEN	B. HAZEN		REV. 1
B	2/10/75	B. HAZEN	B. HAZEN		REV. 2

DRN. D.E. O'Brien	1/22/75	FIRST USED ON	Rx01
CHK'D W.F.M.C.	1/22/75	TITLE	H771A POWER CONNECTIONS
ENG. B. HAZEN	2-10-75	SIZE	D CS
PROJ. ENG. W. HAZEN	2-10-75	NUMBER	H771-A-1
PROD. W. HAZEN	2/10/75	REV.	B
NEXT HIGHER ASSY.		SCALE	NONE
B-DD-n771-0		SHEET	1 OF 1

H771-A-1

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- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.

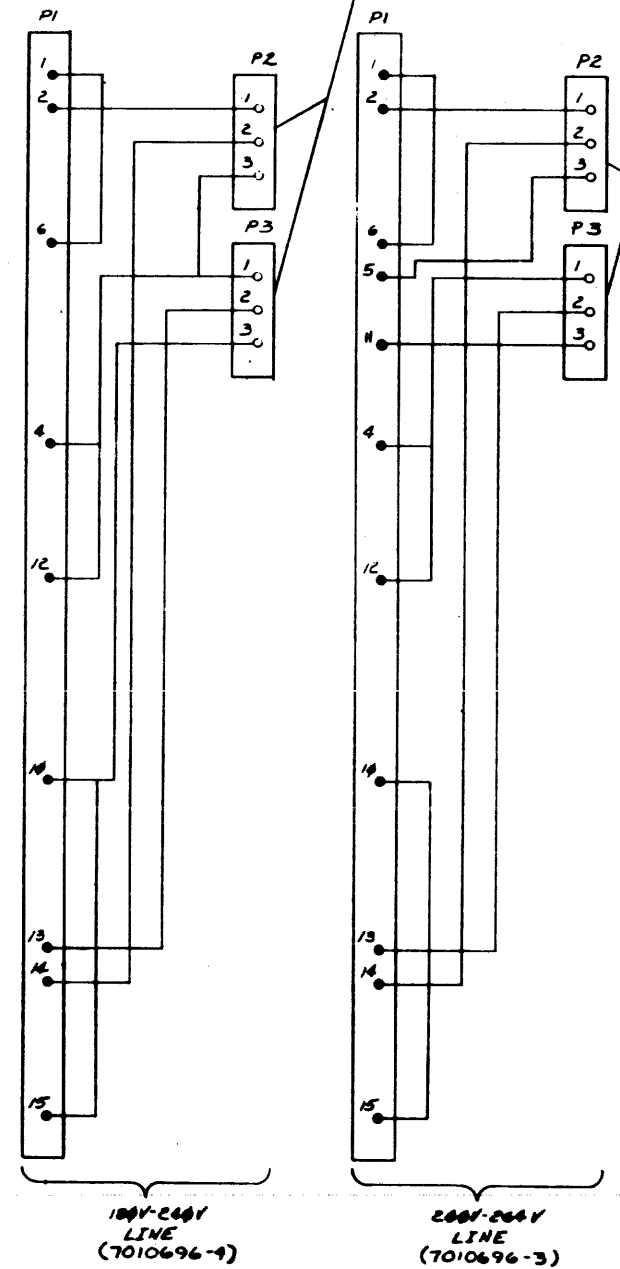
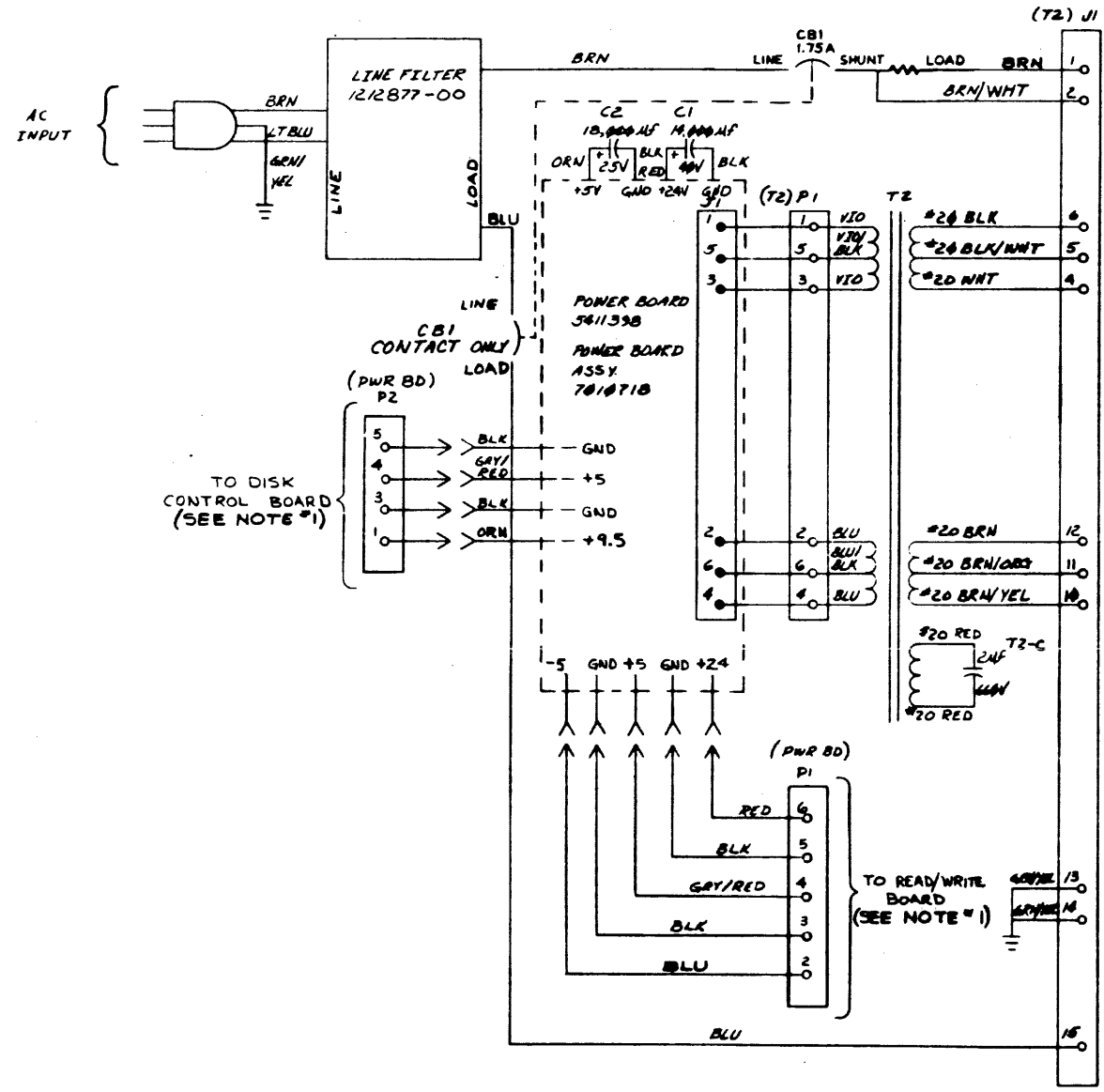


REV.	DATE	BY	CHKD	APP'D	DESCRIPTION
1	11/17/75	B. HAZEN	B. HAZEN		INITIAL RELEASE
2	11/17/75	B. HAZEN	B. HAZEN		REVISION
3	11/17/75	B. HAZEN	B. HAZEN		REVISION
4	11/17/75	B. HAZEN	B. HAZEN		REVISION
5	11/17/75	B. HAZEN	B. HAZEN		REVISION
6	11/17/75	B. HAZEN	B. HAZEN		REVISION
7	11/17/75	B. HAZEN	B. HAZEN		REVISION
8	11/17/75	B. HAZEN	B. HAZEN		REVISION

CHKD	REVISED	DATE	BY	APP'D	DESCRIPTION
E. REMKO	8 5 75				
ENG	8 5 75				
PRG	8 5 75				
PROJ	8 5 75				
EXT	8 5 75				
REV	8 5 75				
DATE	8 5 75				
BY	8 5 75				
APP'D	8 5 75				
DESCRIPTION	H771-C POWER CONNECTIONS				
SCALE	1	SCALE	1	SCALE	1
SHEET	1 OF 1	SHEET	1 OF 1	SHEET	1 OF 1

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- NOTES:
1. SLOT BETWEEN P1-4 AND P1-5 CONTAINS A DUMMY PIN, SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



SEE NOTE #2

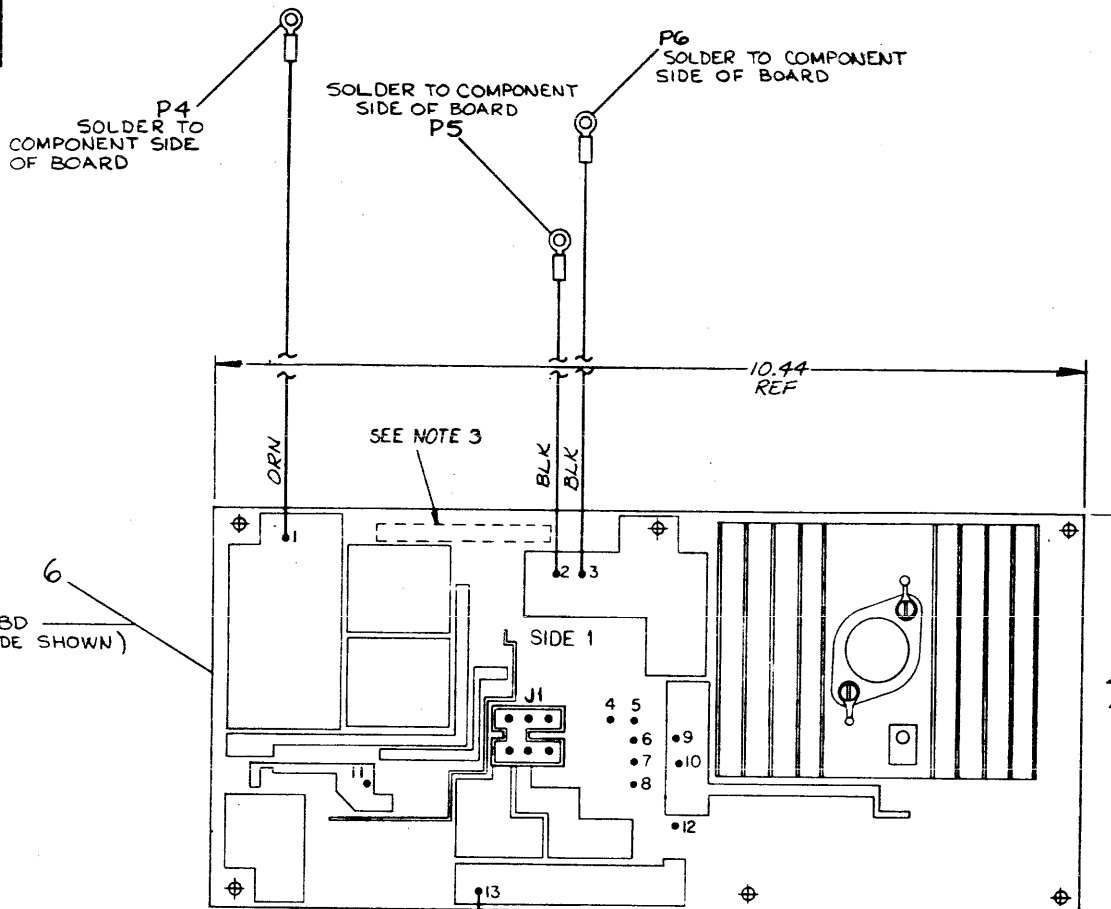
100V-200V LINE (7010696-4)

200V-200V LINE (7010696-3)

REV.	DATE	BY	CHKD.	DESCRIPTION
1	7-30-75	W. HAZEN	E. KEMM	INITIAL DESIGN
2	8-12-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
3	9-17-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
4	10-1-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
5	10-1-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
6	10-1-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
7	10-1-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE
8	10-1-75	W. HAZEN	E. KEMM	REVISED FOR MANUFACTURE

ORIG. BY	DATE	FRONT LABEL ON	REV.
W. HAZEN	7-30-75	RX01	1
CHKD. BY	DATE	TITLE	
E. KEMM	8-5-75	H771-D POWER CONNECTIONS	
PROJ. ENGR.	DATE	SCALE	
W. HAZEN	8-23-75	1:1	
PROJ. MGR.	DATE	SHEET	
W. HAZEN	8-23-75	1 OF 1	
NEXT HIGHER ASSY.	SCALE	SHEET	
B-DD-H771-D	1:1	1 OF 1	
SCALE	SHEET	REV.	
1:1	1 OF 1	C	

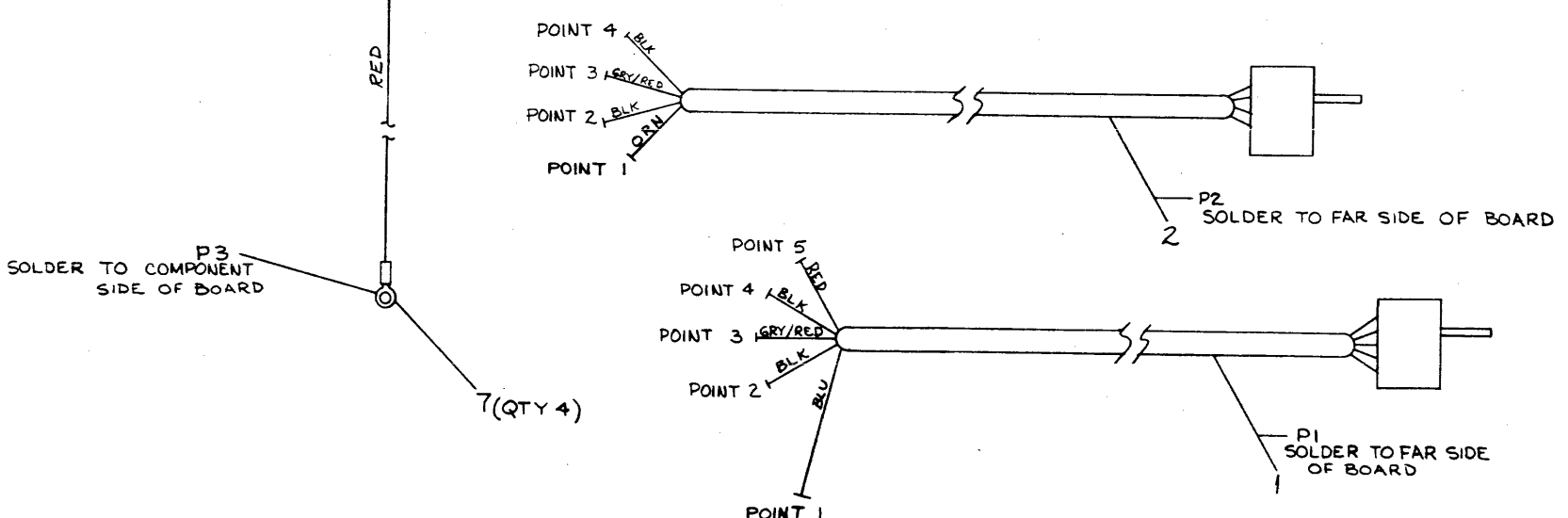
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WIRE TABLE							
ITEM NO.	DESCRIPTION	FROM		TO		LENGTH	
		AWG	COLOR	CONN	TERM		CONN
1	18	BLU	P1	POINT 1	PWR # 11	SOLDER	
		BLK	P1	POINT 2	PWR # 6		
		GRY/RED	P1	POINT 3	PWR # 9		
		BLK	P1	POINT 4	PWR # 5		
		RED	P1	POINT 5	PWR # 12		
2		ORN	P2	POINT 1	PWR # 4		
		BLK	P2	POINT 2	PWR # 7		
		GRY/RED	P2	POINT 3	PWR # 10		
	18	BLK	P2	POINT 4	PWR # 8		
3	14	RED	P3	ITEM 7	PWR # 13		13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR # 2		7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR # 1		11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR # 3	SOLDER	9 IN ±.25

- NOTES:
1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
 2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
 3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.

PWR BD (COMPONENT SIDE SHOWN)



DESCRIPTION	DWG. PART NO.	ITEM NO.
CONN, SOLDERLESS	9007928-00	7
POWER SUPPLY BOARD, RXØ1	D-05-541398-0-1	6
WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
WIRE, #14 AWG, IPVC, RED	9107370-22	3
HARNESS, DISK CONTROL BOARD	D-1A-7010853-0-0	2
HARNESS, READ/WRITE BOARD	D-1F-7010854-0-0	1

REV.	DATE	BY	CHKD
1	7-14-76	C. YOUSSE	
2	7-27-76	B. HAZEN	
3	8-18-76	B. HAZEN	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES	ACCURACY	SURFACE QUALITY	MICROFINISH
90° ± 30'	±.010	MEDIUM	PREFERRED

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

DO NOT SCALE DWG

MATERIAL SEE PARTS LIST

FINISH

DRN: T. Quillen 1-28-75

CHKD: M. C. [Signature]

ENGR: [Signature]

PROL. ENG. [Signature]

PROD. [Signature]

FIRST USED ON: H771

TITLE: RXØ1 POWER BOARD ASSY

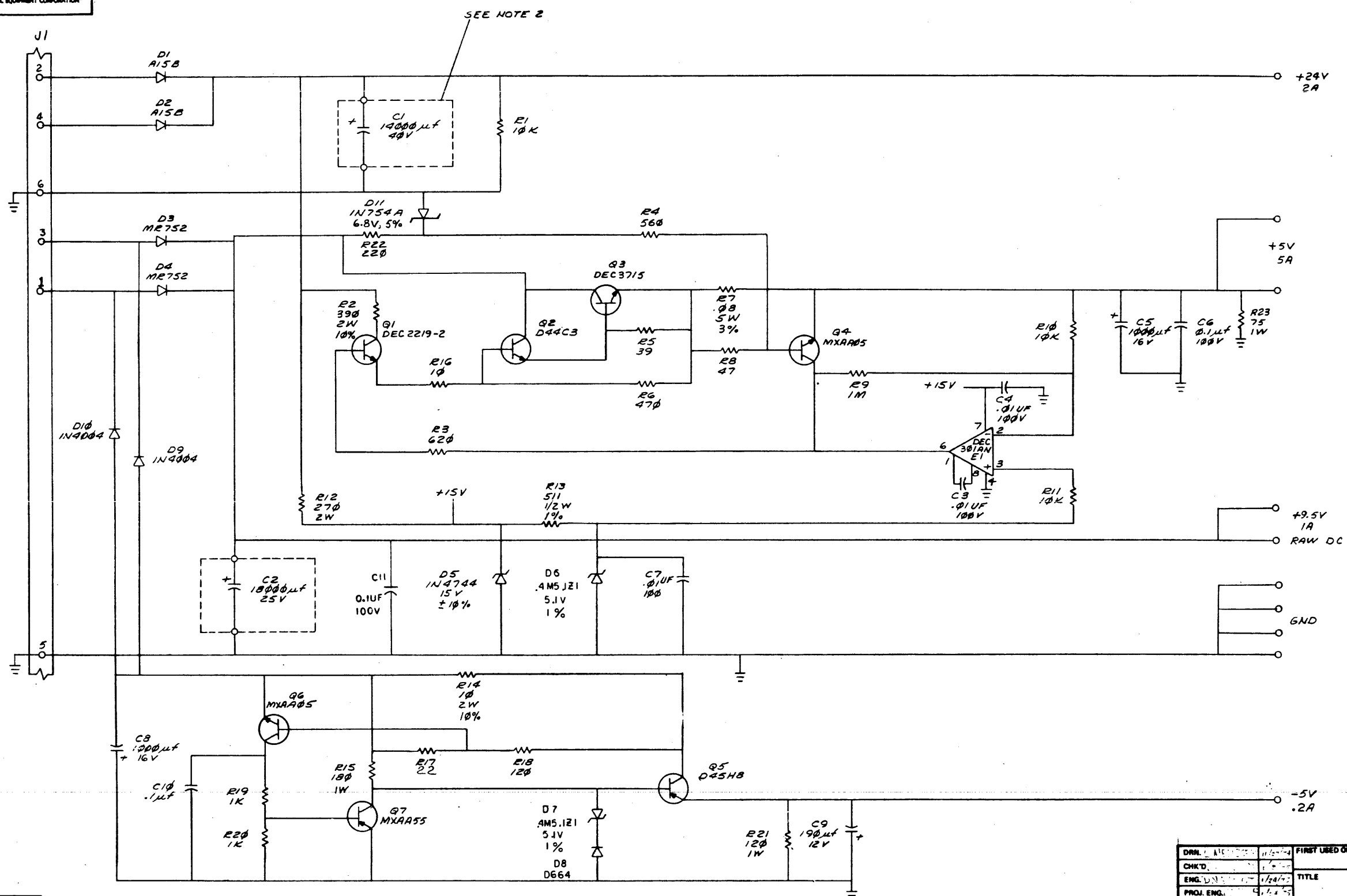
SIZE CODE: D AD 7010718-0-0

NUMBER: 1 OF 1

REV. 5

REV. 5
D AD 7010718-0-0

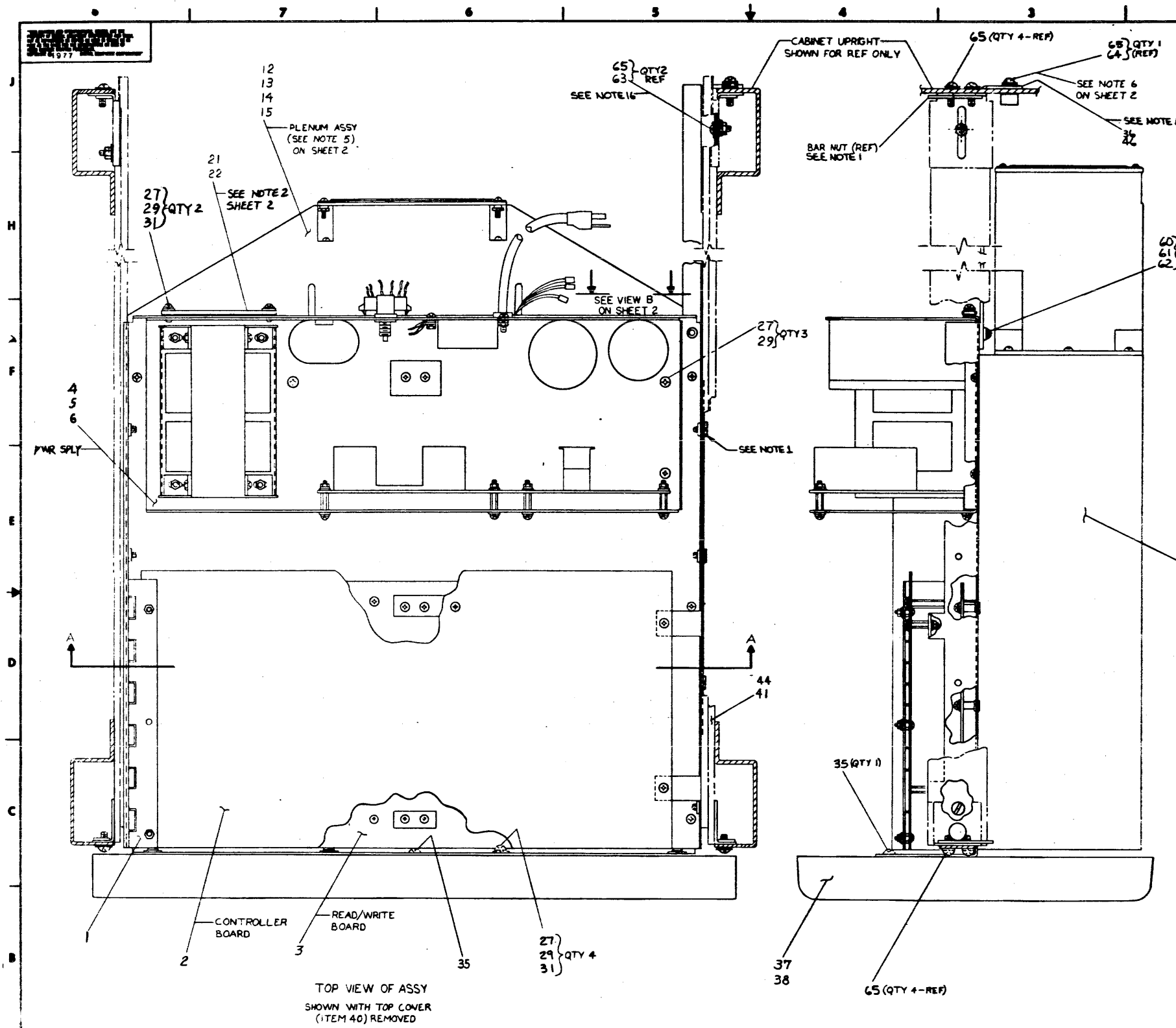
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SEE NOTE 2

REVISIONS		
CHK	CHANGE NO.	REV.
LS	5411398-ML005	F
L. SALAFIA		

DRN. DATE	11/25/74	FIRST USED ON	0101000
CHK'D.		TITLE	RX01 POWER SUPPLY
ENG. DATE	1/24/75	SIZE	D
PROJ. ENG.		CODE	CS
PROD.		NUMBER	5411398-0-1
NEXT HIGHER ASSY.		REV.	F
SCALE	-11	DIST.	
SHEET	OF		



UNIT VARIATIONS	
VARIATION	DESCRIPTION
RX02-AA	SINGLE FLOPPY DISK SYSTEM, 110V, 60 HZ
RX02-AC	SINGLE FLOPPY DISK SYSTEM, 110V, 50 HZ
RX02-AD	SINGLE FLOPPY DISK SYSTEM, 230V, 50 HZ
RX02-BA	DUAL FLOPPY DISK SYSTEM, 110V, 60 HZ
RX02-BC	DUAL FLOPPY DISK SYSTEM, 110V, 50 HZ
RX02-BD	DUAL FLOPPY DISK SYSTEM, 230V, 50 HZ
RX02-CA	SINGLE ADD-ON FLOPPY DISK DRIVE - 50 HZ
RX02-CC	SINGLE ADD-ON FLOPPY DISK DRIVE - 60 HZ
RX02-DA	RX02-BA, BEZEL / COVER
RX02-DC	RX02-BC, BEZEL / COVER
RX02-DD	RX02-BD, BEZEL / COVER
RX02-LA	RX02-BA, SLIDES / COVER
RX02-LC	RX02-BC, SLIDES / COVER
RX02-LD	RX02-BD, SLIDES / COVER
RX02-NA	RX02-AA, SLIDES / COVER
RX02-NC	RX02-AC, SLIDES / COVER
RX02-ND	RX02-AD, SLIDES / COVER
RX02-VA	RX02 SINGLE FOR KC788, 110V, 60 HZ
RX02-VC	RX02 SINGLE FOR KC788, 110V, 50 HZ
RX02-VD	RX02 SINGLE FOR KC788, 230V, 50 HZ

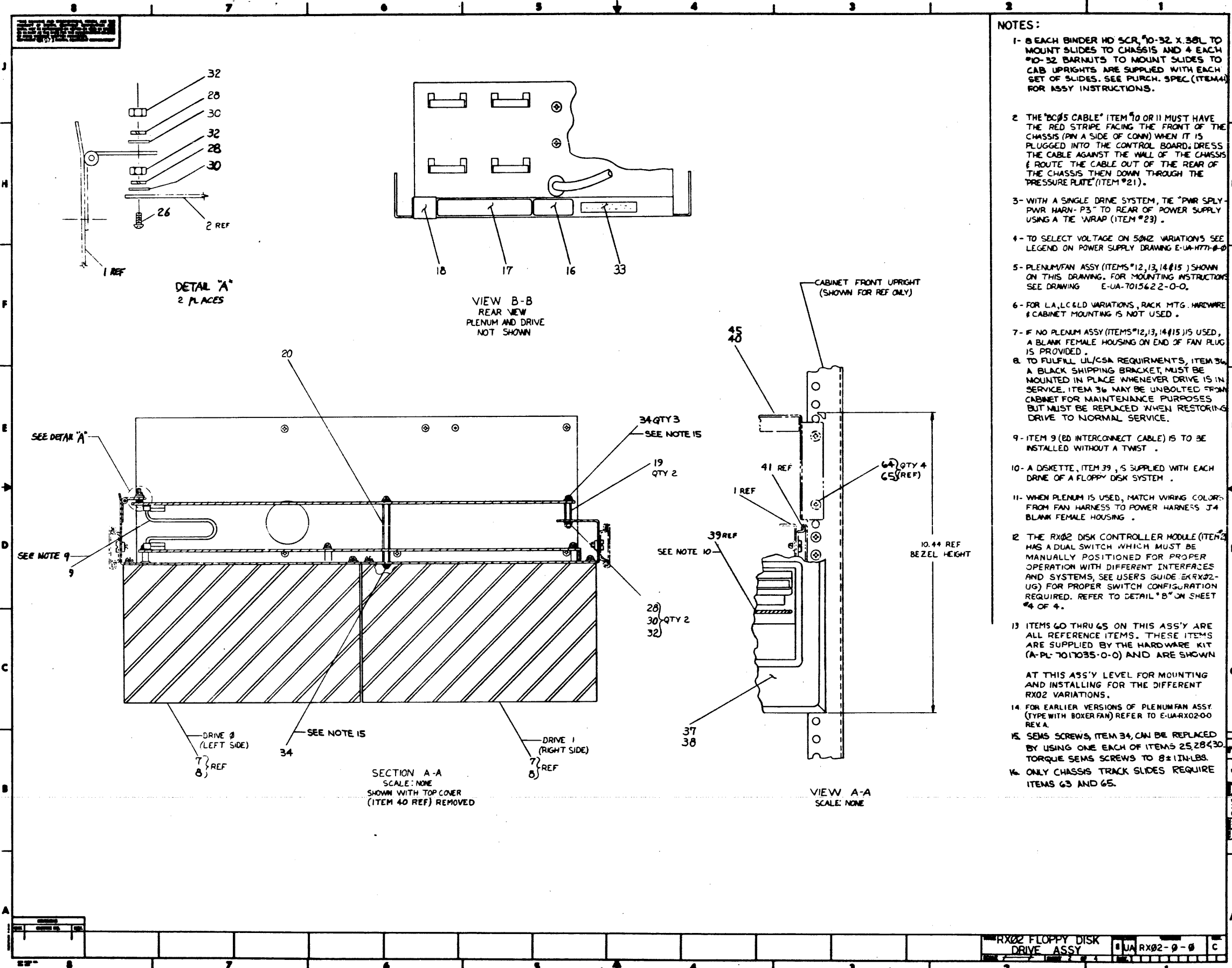
INSTALLATION HARDWARE (SEE NOTE 12)					
RX02 ASSY FIND NO	KIT LIST FIND NO	HARDWARE KIT 101035-0-0			
		CONFL RX02 KIT	SLIDE MTS ITEM 41	COVER MTS ITEM 40	UL BRKT MTS ITEM 36
60	1	1	—	—	1
61	2	1	—	—	1
62	3	1	—	—	1
63	4	2	2	—	—
64	5	5	—	4	1
65	6	15	10	4	1

NOTE: -00 KIT IS ONE EACH -02, -03, -04

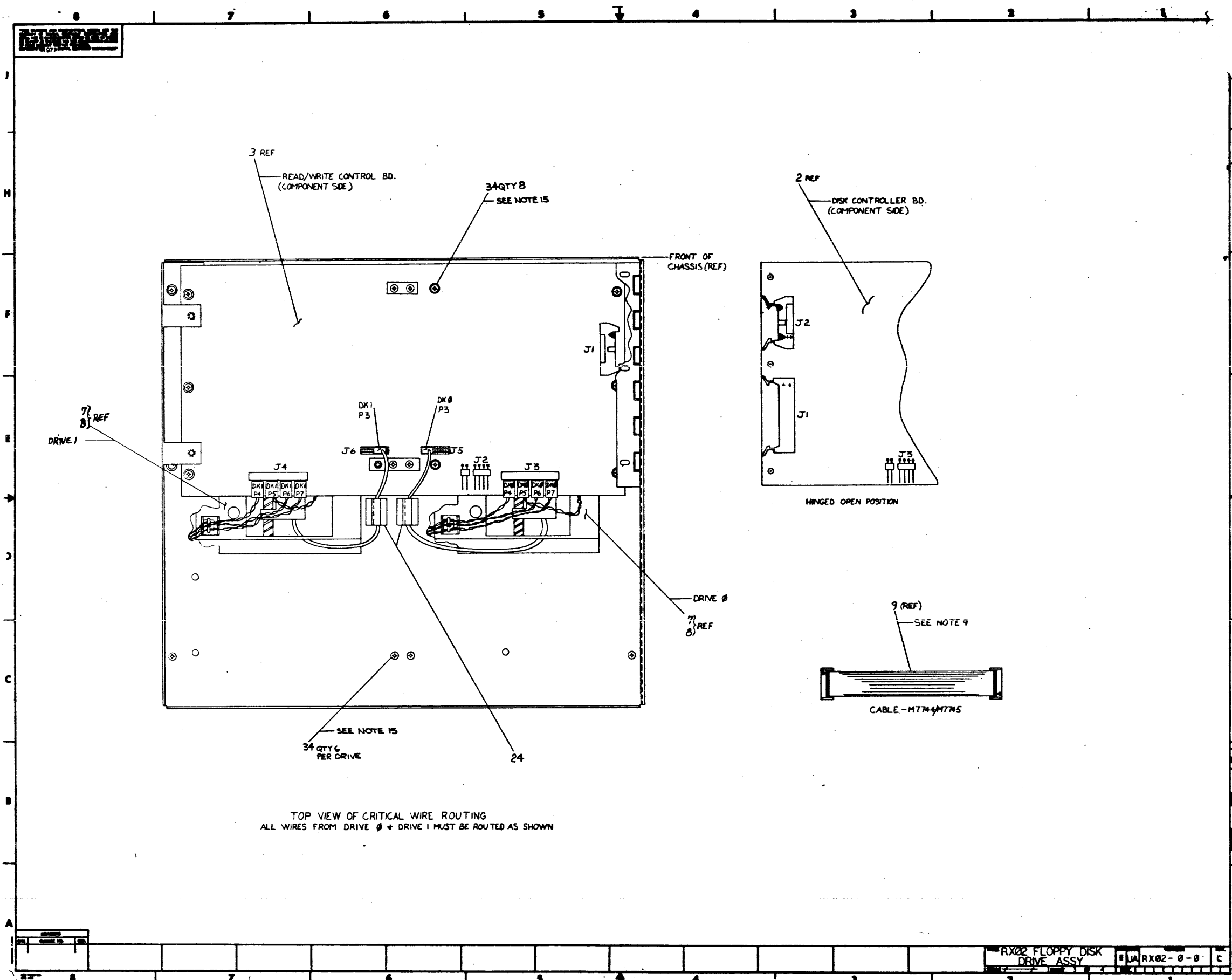
ALL NOTES ARE ON SHEET 2
FOR PARTS LIST, SEE C-PL-RX02-0-0

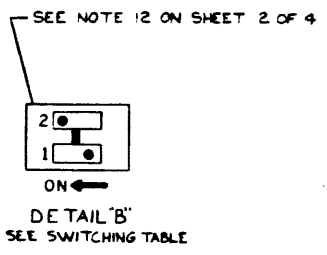
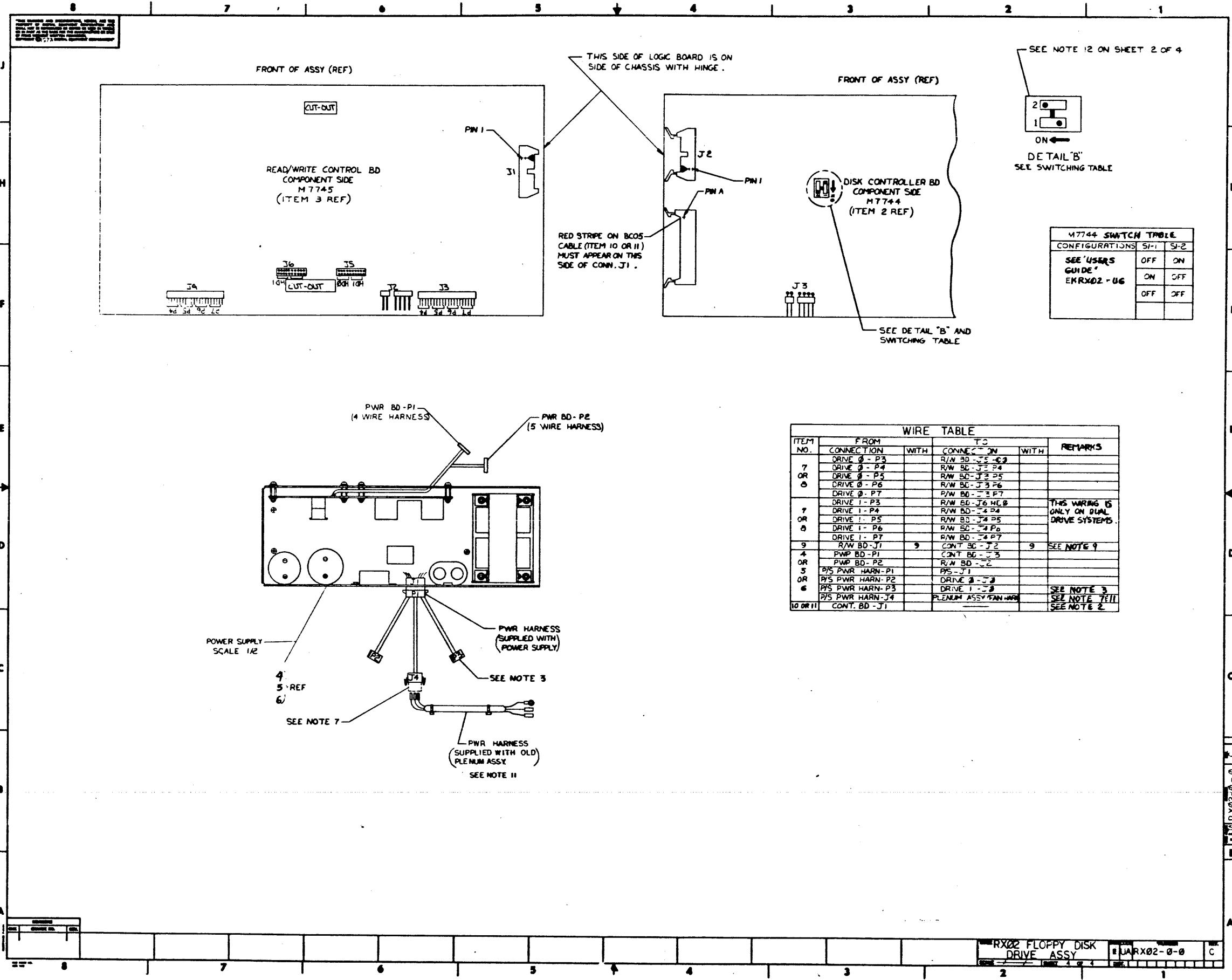
REV	DATE	BY	CHKD	DESCRIPTION
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

DESCRIPTION	RX02	QUANTITY	20-0000
UNIT	RX02 FLOPPY DISK DRIVE ASSY		
SEE C-PL-RX02-0-0			



- NOTES:**
- 1- 8 EACH BINDER HD SCR, #10-32 X .38L TO MOUNT SLIDES TO CHASSIS AND 4 EACH #10-32 BARNUTS TO MOUNT SLIDES TO CAB UPRIGHTS ARE SUPPLIED WITH EACH SET OF SLIDES. SEE PURCH. SPEC. (ITEM 4) FOR ASSY INSTRUCTIONS.
 - 2 THE "BC#5 CABLE" ITEM 10 OR 11 MUST HAVE THE RED STRIPE FACING THE FRONT OF THE CHASSIS (PIN A SIDE OF CONN) WHEN IT IS PLUGGED INTO THE CONTROL BOARD. DRESS THE CABLE AGAINST THE WALL OF THE CHASSIS & ROUTE THE CABLE OUT OF THE REAR OF THE CHASSIS THEN DOWN THROUGH THE "PRESSURE PLATE" (ITEM #21).
 - 3- WITH A SINGLE DRIVE SYSTEM, TIE "PWR SPLY. PWR HARN- P3" TO REAR OF POWER SUPPLY USING A TIE WRAP (ITEM #23).
 - 4- TO SELECT VOLTAGE ON 50HZ VARIATIONS SEE LEGEND ON POWER SUPPLY DRAWING E-UA-177-0-0.
 - 5- PLENUM/FAN ASSY (ITEMS #12, 13, 14#15) SHOWN ON THIS DRAWING. FOR MOUNTING INSTRUCTIONS SEE DRAWING E-UA-7015622-0-0.
 - 6- FOR L.A., L.C. & L.D. VARIATIONS, RACK MTG. HARDWARE & CABINET MOUNTING IS NOT USED.
 - 7- IF NO PLENUM ASSY (ITEMS #12, 13, 14#15) IS USED, A BLANK FEMALE HOUSING ON END OF FAN PLUG IS PROVIDED.
 - 8- TO FULFILL UL/CSA REQUIREMENTS, ITEM 36, A BLACK SHIPPING BRACKET, MUST BE MOUNTED IN PLACE WHENEVER DRIVE IS IN SERVICE. ITEM 36 MAY BE UNBOLTED FROM CABINET FOR MAINTENANCE PURPOSES BUT MUST BE REPLACED WHEN RESTORING DRIVE TO NORMAL SERVICE.
 - 9- ITEM 9 (ED INTERCONNECT CABLE) IS TO BE INSTALLED WITHOUT A TWIST.
 - 10- A DISKETTE, ITEM 39, IS SUPPLIED WITH EACH DRIVE OF A FLOPPY DISK SYSTEM.
 - 11- WHEN PLENUM IS USED, MATCH WIRING COLOR FROM FAN HARNESS TO POWER HARNESS J4 BLANK FEMALE HOUSING.
 - 12 THE RX02 DISK CONTROLLER MODULE (ITEM 2) HAS A DUAL SWITCH WHICH MUST BE MANUALLY POSITIONED FOR PROPER OPERATION WITH DIFFERENT INTERFACES AND SYSTEMS. SEE USER'S GUIDE (E-RX02-UG) FOR PROPER SWITCH CONFIGURATION REQUIRED. REFER TO DETAIL "B" ON SHEET #4 OF 4.
 - 13 ITEMS 60 THRU 65 ON THIS ASSY ARE ALL REFERENCE ITEMS. THESE ITEMS ARE SUPPLIED BY THE HARDWARE KIT (A-PL-7017035-0-0) AND ARE SHOWN AT THIS ASSY LEVEL FOR MOUNTING AND INSTALLING FOR THE DIFFERENT RX02 VARIATIONS.
 - 14 FOR EARLIER VERSIONS OF PLENUM/FAN ASSY (TYPE WITH BOXER FAN) REFER TO E-UA-RX02-00 REV. A.
 - 15 SEMS SCREWS, ITEM 34, CAN BE REPLACED BY USING ONE EACH OF ITEMS 25, 28 & 30. TORQUE SEMS SCREWS TO 8±1 IN-LBS.
 - 16 ONLY CHASSIS TRACK SLIDES REQUIRE ITEMS 63 AND 65.



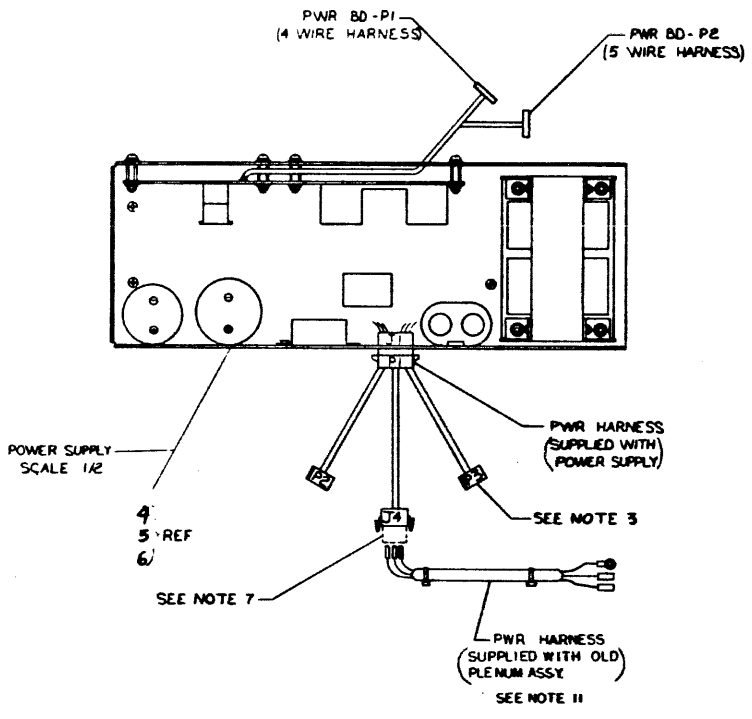


M7744 SWITCH TABLE

CONFIGURATIONS	SP-1	SP-2
SEE 'USERS GUIDE' EKR02-UG	OFF	ON
	ON	OFF
	OFF	OFF

WIRE TABLE

ITEM NO.	FROM		TO		REMARKS
	CONNECTION	WITH	CONNECTION	WITH	
7 OR 8	DRIVE 0 - P3		R/W BD - J5 - C3		
	DRIVE 0 - P4		R/W BD - J5 - P4		
	DRIVE 0 - P5		R/W BD - J5 - P5		
	DRIVE 0 - P6		R/W BD - J5 - P6		
	DRIVE 0 - P7		R/W BD - J5 - P7		
	DRIVE 1 - P3		R/W BD - J6 - HCB		THIS WIRING IS ONLY ON DUAL DRIVE SYSTEMS.
	DRIVE 1 - P4		R/W BD - J6 - P4		
DRIVE 1 - P5		R/W BD - J6 - P5			
DRIVE 1 - P6		R/W BD - J6 - P6			
9	R/W BD - J1	9	CONT. BD - J2	9	SEE NOTE 9
4	PWR BD - P1		CONT. BD - J3		
OR	PWR BD - P2		R/W BD - J2		
5	P/S PWR HARN - P1		P/S - J1		
OR	P/S PWR HARN - P2		DRIVE 0 - J3		
6	P/S PWR HARN - P3		DRIVE 1 - J3		SEE NOTE 3
OR	P/S PWR HARN - J4		PLENUM ASSY PWR HARN		SEE NOTE 7/11
10 OR 11	CONT. BD - J1				SEE NOTE 2



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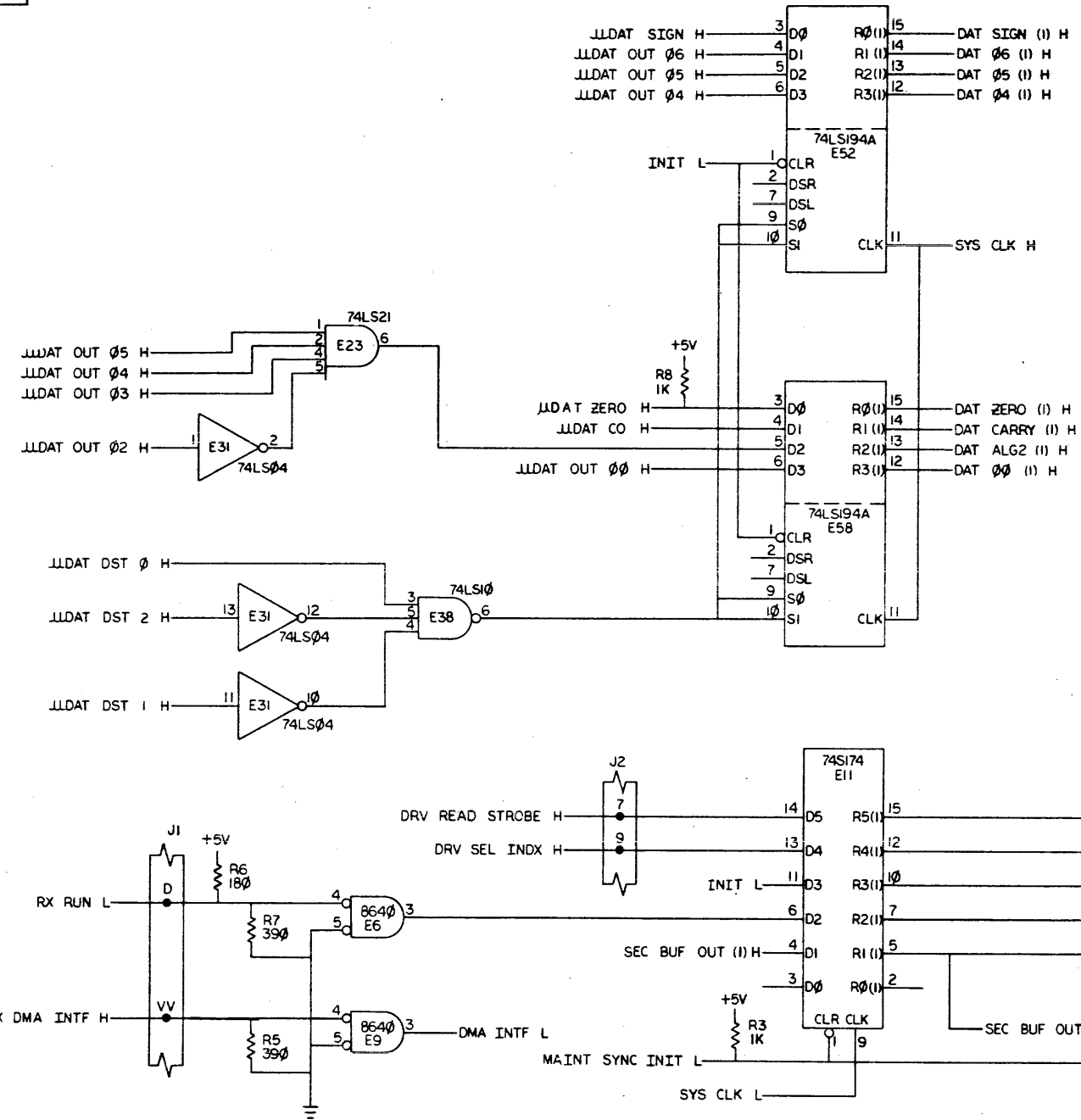
		RX02-AA	RX02-AC	RX02-AD	RX02-BA	RX02-BC	RX02-BD	RX02-CA	RX02-CC	RX02-DA	RX02-DC	RX02-DD	RX02-EA	RX02-LC	RX02-LD	RX02-NA	RX02-NC	RX02-ND	RX02-VA	RX02-VC	RX02-YD	
42																						
43	A-PL-7017035-00	HARDWARE KIT, RX02	1	1	1	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
44	A-PL-7017035-02	HARDWARE KIT, SLIDES	-	-	-	-	-	-	-	1	1	1	-	-	-	-	-	-	-	-	-	
45	A-PL-7017035-03	HARDWARE KIT, TOP COVER	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
46	A-PL-7017035-04	HARDWARE KIT, SHIP, BRKT (U.L.)	-	-	-	-	-	-	-	1	1	1	-	-	-	-	-	-	1	1	1	
47																						
48	A-SP-3700185-00	PACK. INSTR-INTERPLANT W/BEZEL	1	1	1	1	1	-	-	-	-	1	1	1	1	1	1	1	-	-	-	
49	A-SP-3700185-01	PACK. INSTR-INTERPLANT W/O BEZEL	-	-	-	-	-	-	-	1	1	1	-	-	-	-	-	-	-	1	1	1
50	A-SP-3700193-0-0	PACK. INSTR-CUSTOMER (SEE NOTE)	*	*	*	*	*	-	-	*	*	*	*	*	*	*	*	*	*	*	*	*
51	A-SP-3700229-0-0	PACK. INSTR-DRIVE	-	-	-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	-	
52																						
53																						
54																						
55																						
56																						
57																						
ASSEMBLY REFERENCE ONLY																						
60	9006039-01	SCR, PH, P.H., 8-32 X .50L	1	1	1	1	1	-	-	1	1	1	-	-	-	-	-	-	1	1	1	
61	9006690-00	WASHER, LOCK SPLIT, NO 8	1	1	1	1	1	-	-	1	1	1	-	-	-	-	-	-	1	1	1	
62	9006666-00	WASHER, FLAT NO 8	1	1	1	1	1	-	-	1	1	1	-	-	-	-	-	-	1	1	1	
63	9006565-00	NUT, KEP, HEX, 10-32	2	2	2	2	2	-	-	2	2	2	-	-	-	-	-	-	-	-	-	
64	9007786-00	NUT, TINNEMAN, 10-32	5	5	5	5	5	-	-	1	1	1	-	-	-	-	-	-	1	1	1	
65	9009700-00	SCR, SEMS, TRUSS HD, 10-32 X .50L	15	15	15	15	15	-	-	11	11	11	-	-	-	-	-	-	1	1	1	
NOTE: ITEM 50 USED AS REQ'D FOR CUSTOMER SHIP ONLY.																						

REVISIONS	REV.
CHANGE NO.	
CHK	

DRN	R. P. MORIN	1 SEPT	FIRST USED ON	RX02
CHK'D	R. P. MORIN	1 SEPT		
ENG.	R. P. MORIN	1 SEPT	TITLE	RX02 FLOPPY DISK DRIVE ASSY.
PROJ. ENG.	GLAVIN	9-1-79		
PROD.	M. DURHAM	9-1-79		
NEXT HIGHER ASSY.			SIZE	CODE
B-DD-RX02-8			C	PL
SCALE			NUMBER	
SHEET 2 OF 2			RX02-8-8	
			DIST.	REV. C

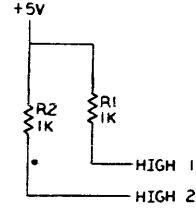
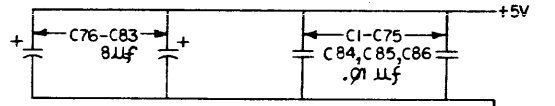
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M7744-0-1



NOTE:
 1. SPARE I.C. LOCATION AT E10, E30, E33, E45.
 2. E42, E55, E61, E69 ARE I.C. LOCATIONS ONLY, NO COMPONENTS ARE TO BE INSERTED. SEE SHEET 10
 3.

M7744 OPTIONS		
	SI-1	SI-2
-B	OFF	ON
-YA	ON	OFF
-YB	OFF	OFF



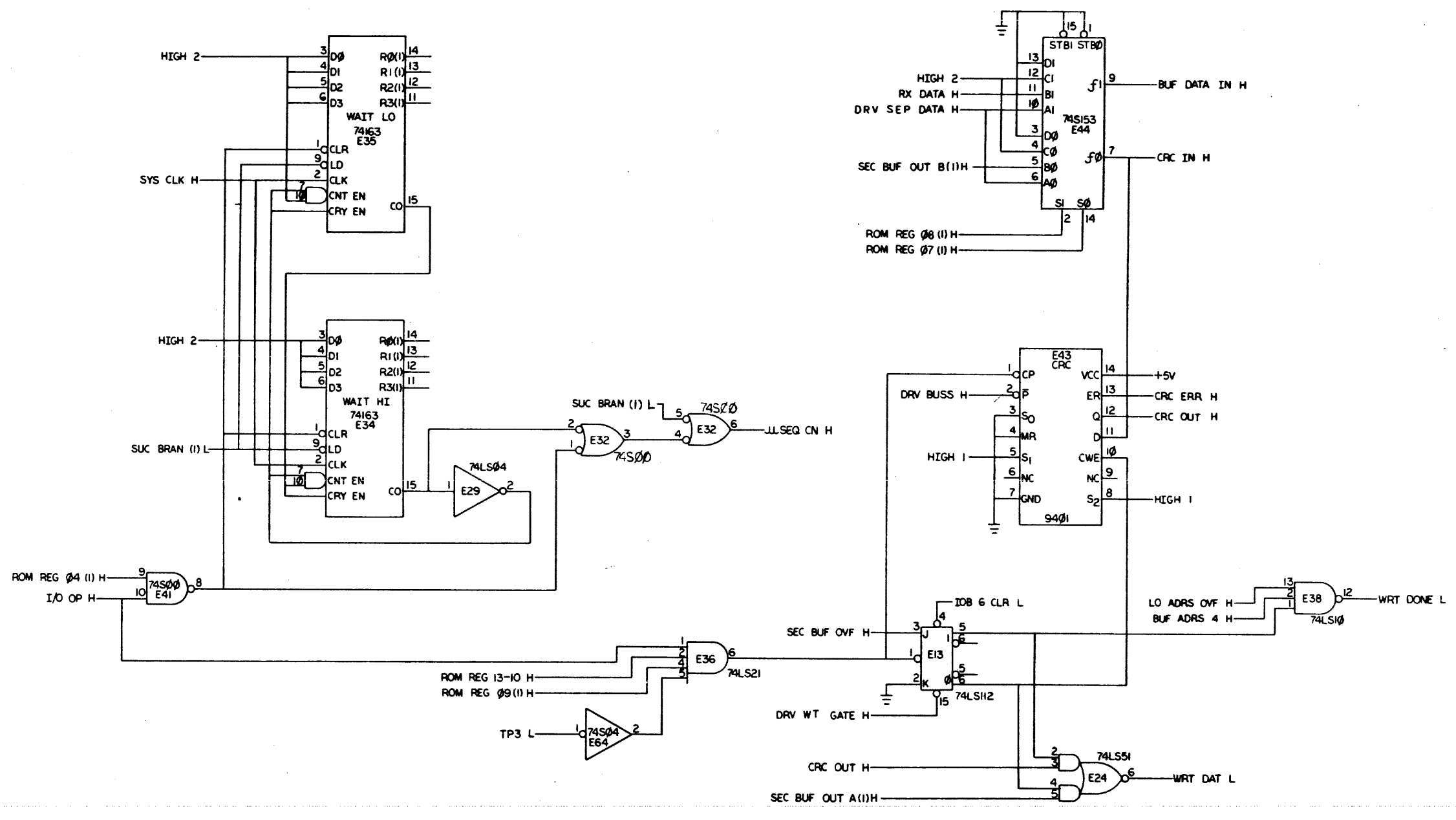
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3	0003	E				
4	0004	F				
5	0005	H				
6	0006	J				
7	0007	L				
8	0008	D				

DRN <i>[Signature]</i>	FIRST USED ON	RX02	digital
CHKD <i>[Signature]</i>	TITLE	RX02 FLOPPY DISK CONTROLLER	
ENG <i>[Signature]</i>	PROJ. ENG.	DATE	2/3/78
PROD. <i>[Signature]</i>	DATE	2/3/78	
NEXT HIGHER ASSY.	SCALE	SIZE CODE	D CS
B-DD-M7744-0	SCALE	NUMBER	M7744-0-1
SHEET 1 OF 10	DIST.		

M7744-0-1

ML 1

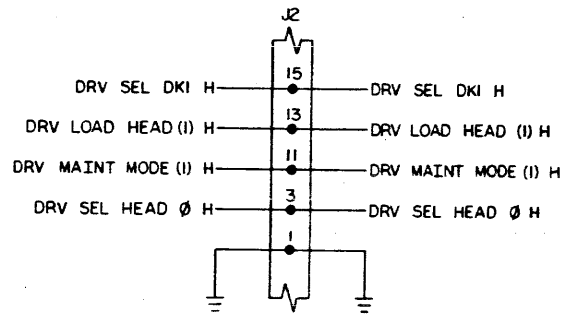
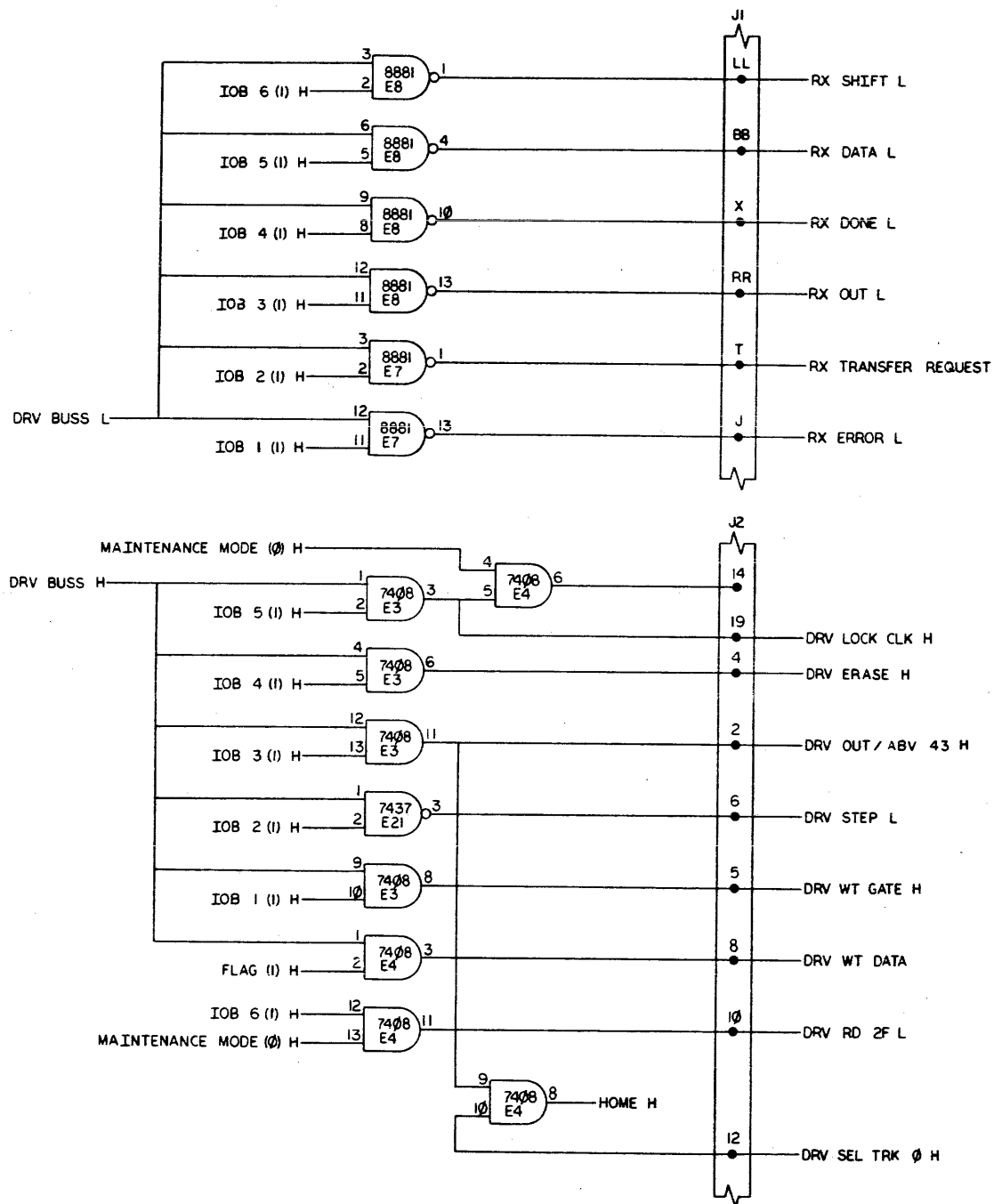
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REV. 1-0-77/1W DCS M7744-01 2



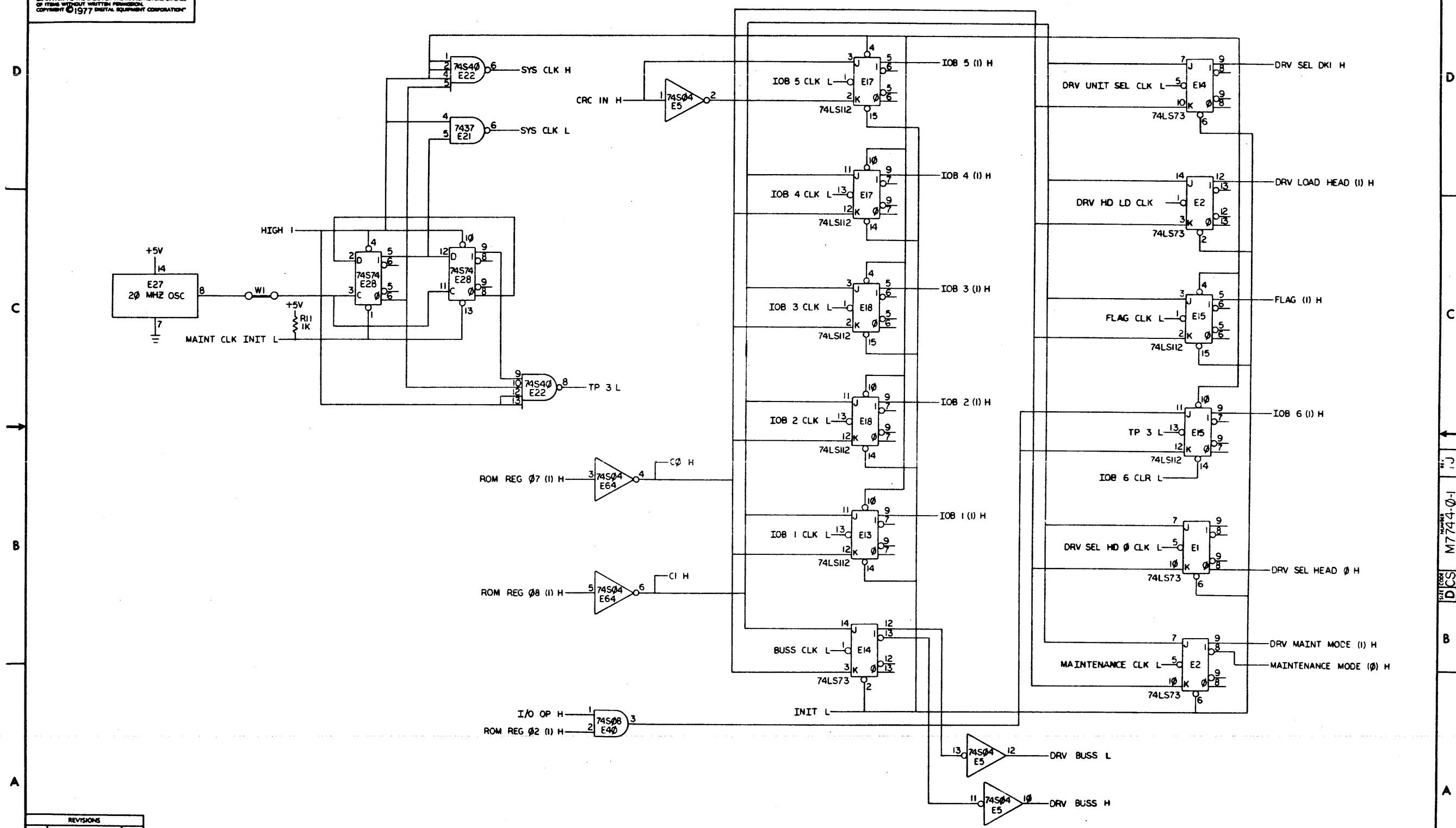
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CHK	CHANGE NO.	REV.

TITLE RX02 FLOPPY DISK CONTROLLER SIZE CODE DCS NUMBER M7744-01 REV. J
SCALE SHEET 3 OF 10 DIST.

REV. 1-0-77/1W DCS M7744-01

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10-0222W 2

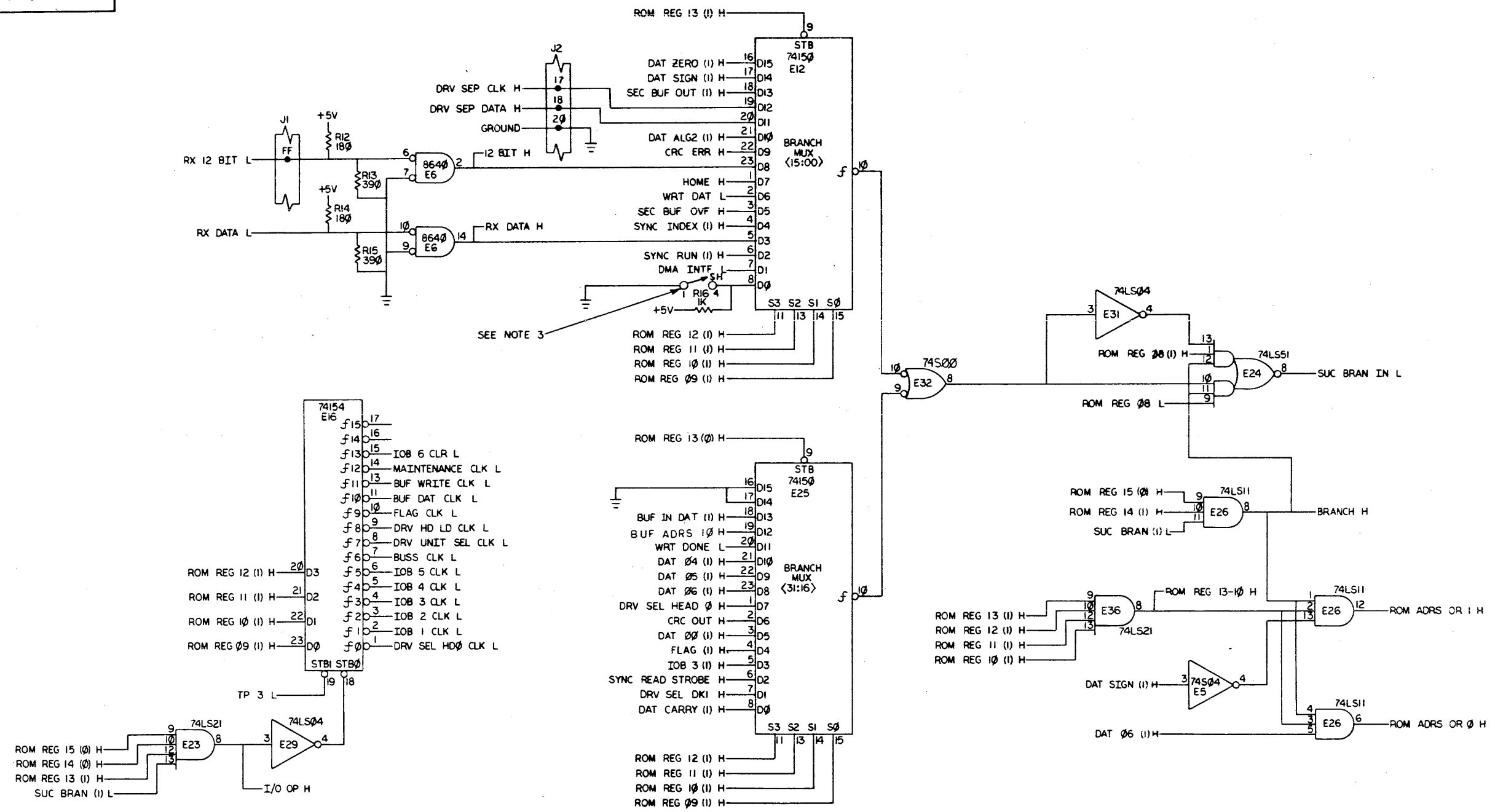


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 SIZE CODE DCS NUMBER M7744-0-1 REV. J
 SCALE SHEET 4 OF 10 DIST.

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10-0222W SQD 2



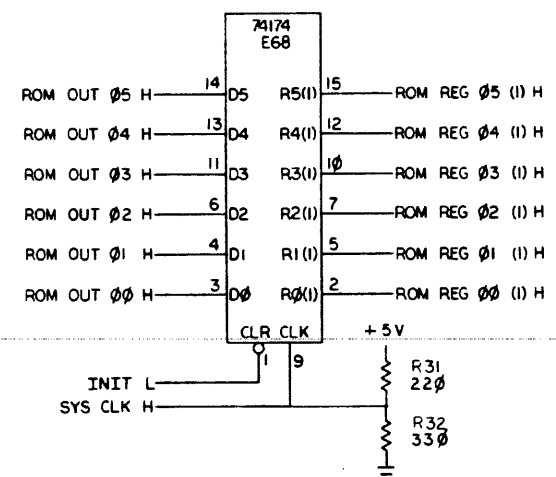
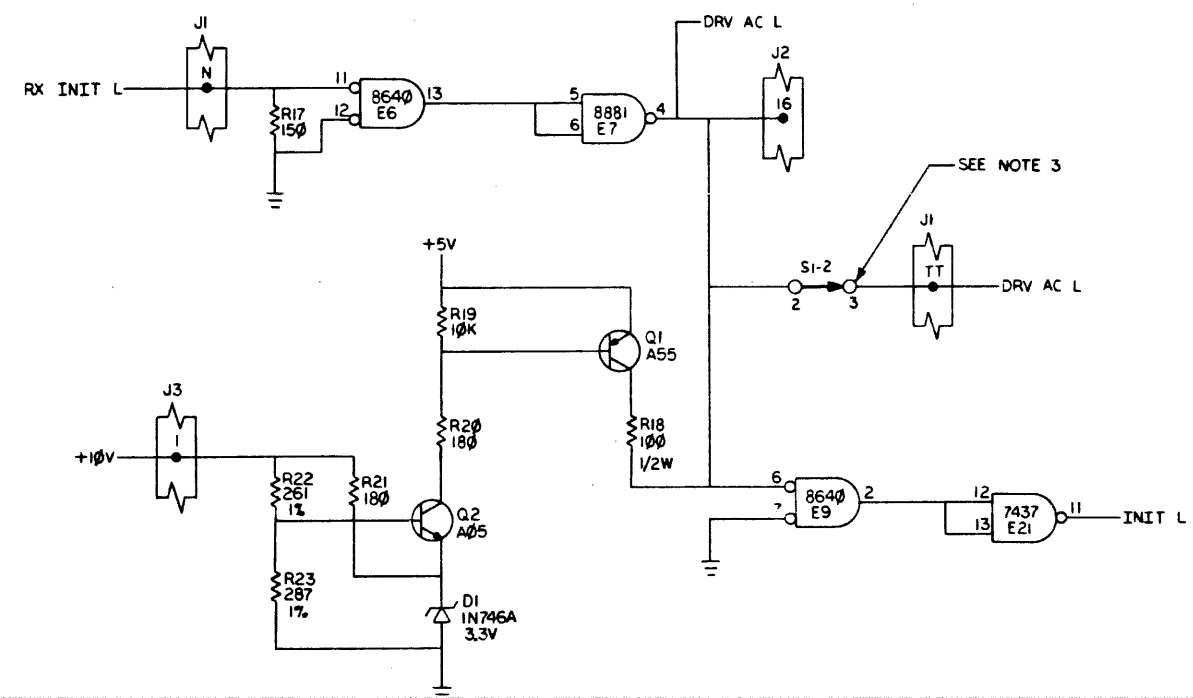
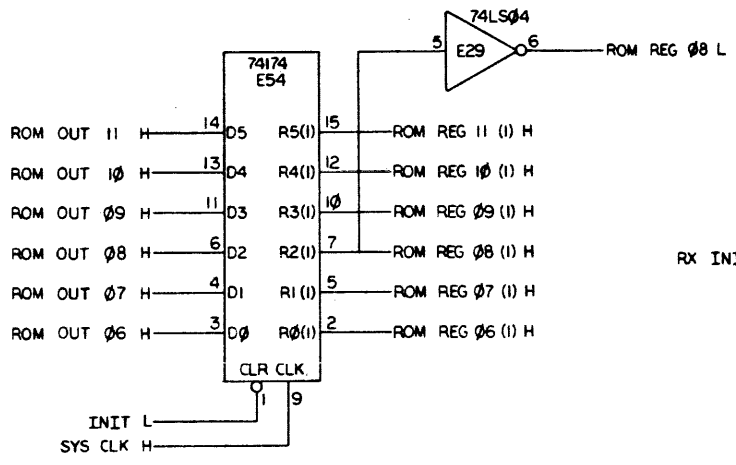
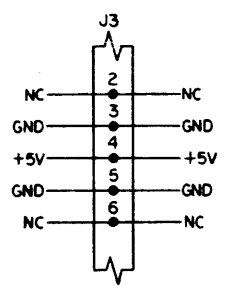
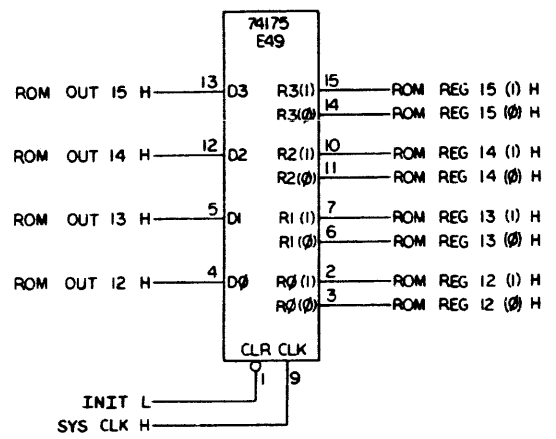
- f15 17
- f14 16
- f13 15 IOB 6 CLR L
- f12 14 MAINTENANCE CLK L
- f11 13 BUF WRITE CLK L
- f10 11 BUF DAT CLK L
- f9 10 FLAG CLK L
- f8 9 DRV HD LD CLK L
- f7 8 DRV UNIT SEL CLK L
- f6 7 BUSS CLK L
- f5 6 IOB 5 CLK L
- f4 5 IOB 4 CLK L
- f3 4 IOB 3 CLK L
- f2 3 IOB 2 CLK L
- f1 2 IOB 1 CLK L
- f0 1 DRV SEL HD0 CLK L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE RX02 FLOPPY DISK CONTROLLER
 SCALE 1:1 SHEET 5 OF 10
 SIZE CODE DCS NUMBER M7744-0-1 REV. J

M7744-0-1

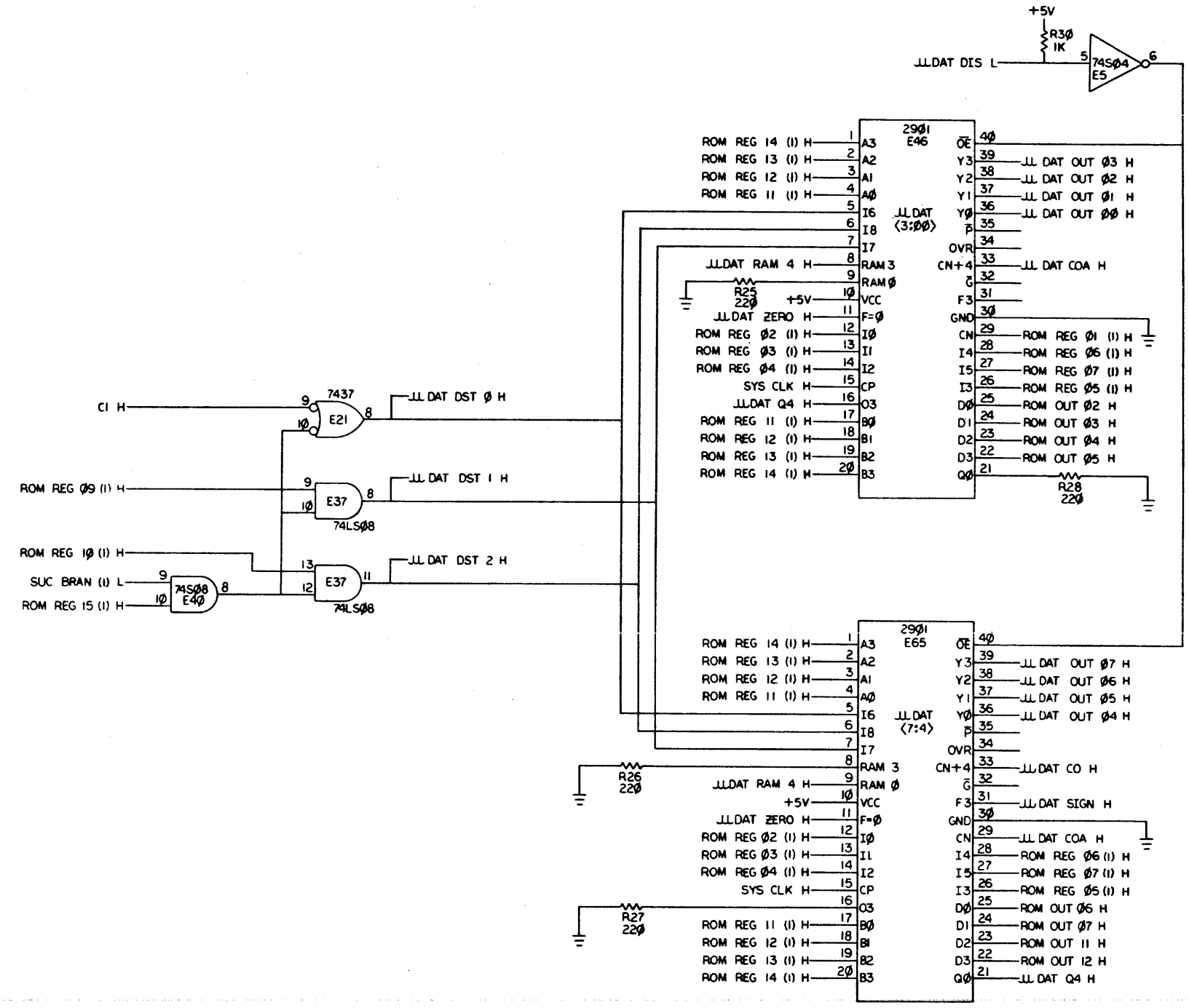
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M7744-01 2



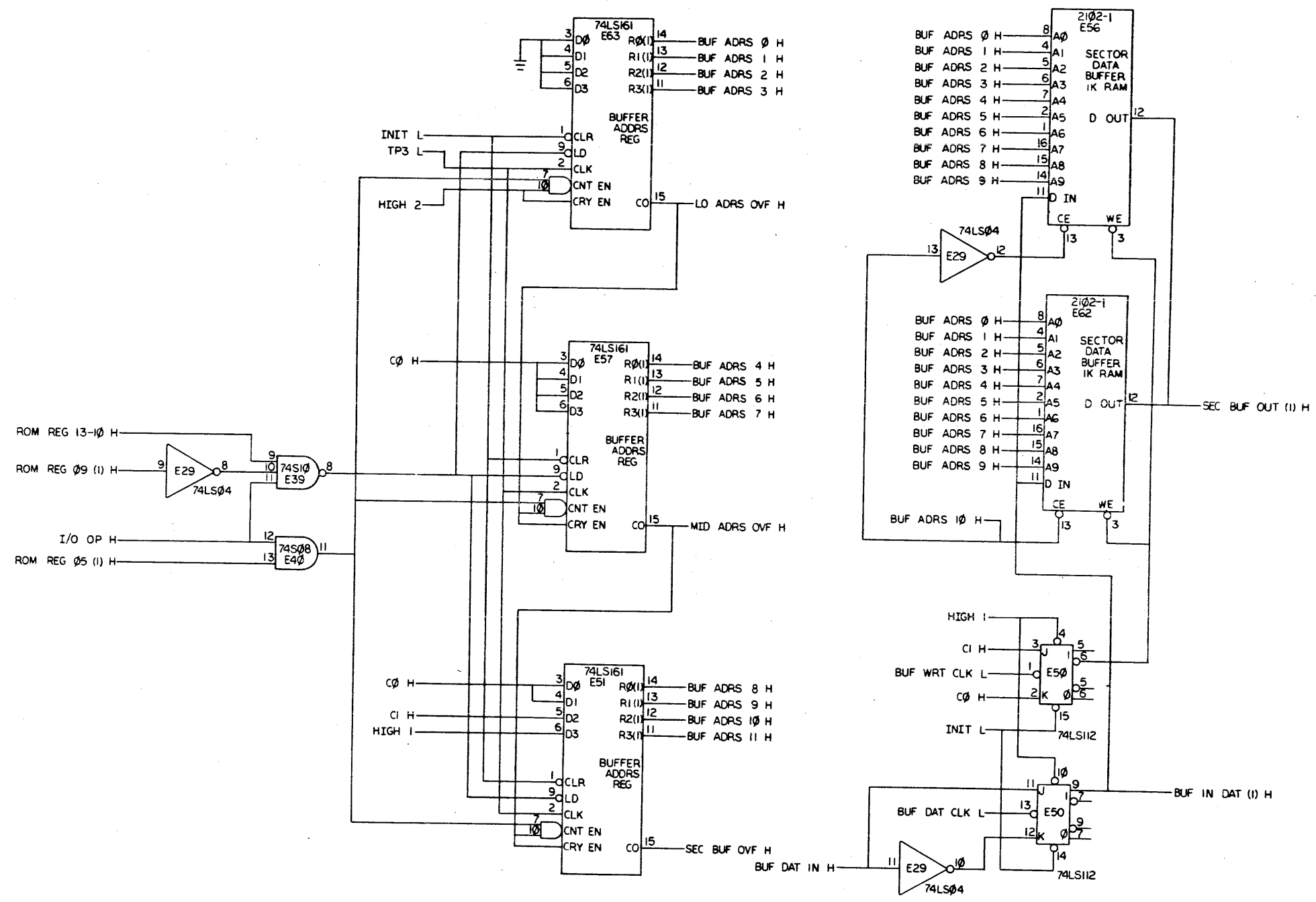
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TITLE RX02 FLOPPY DISK CONTROLLER
 SIZE CODE JCS
 NUMBER M7744-01
 REV. J
 SCALE 1/16" = 1"

M7744-01 J

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REV. 1
M7744-01
DCS
2



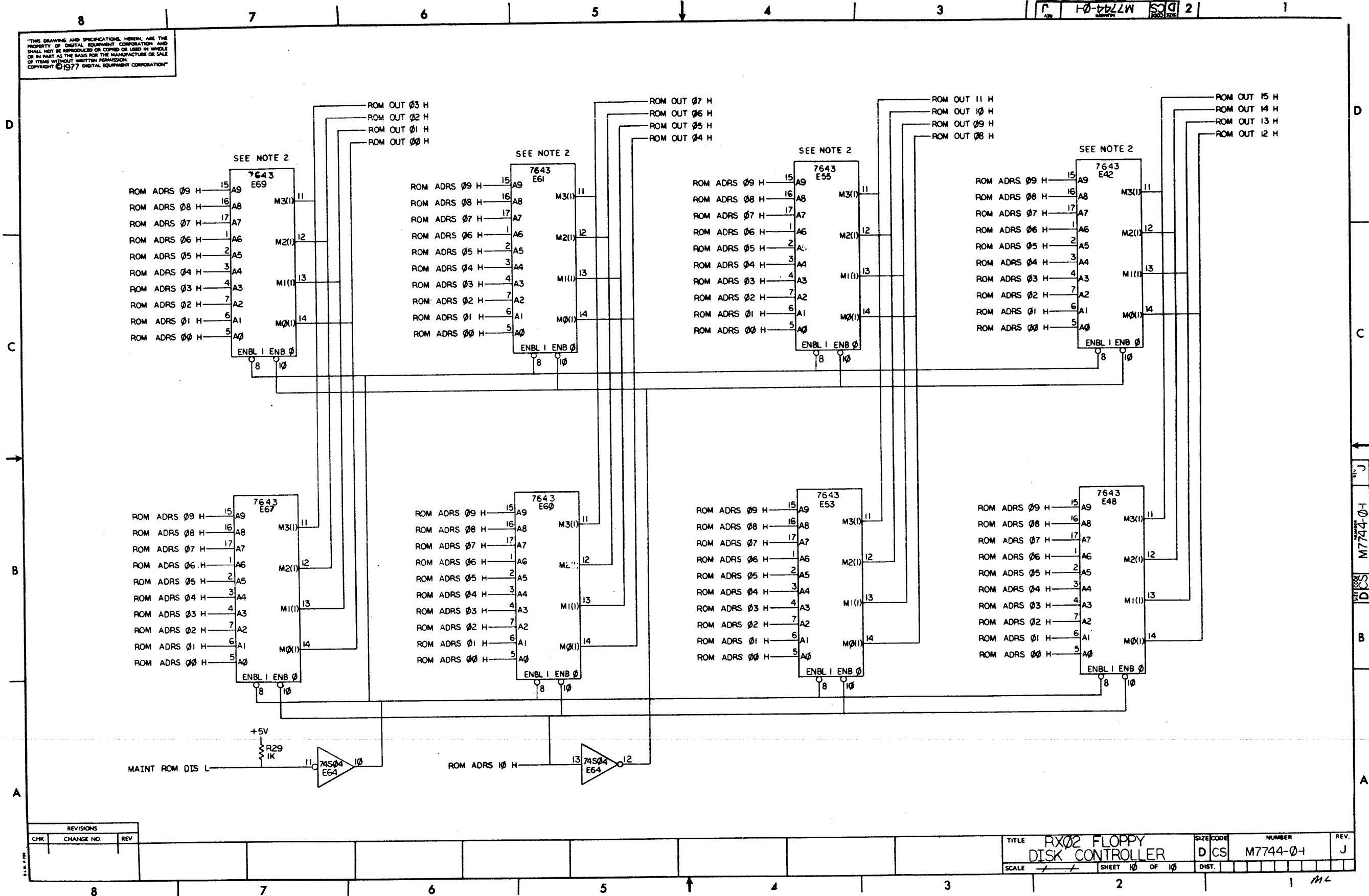
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CHK	CHANGE NO	REV.

DEC FORM NO. 138	8	7	6	5	4	3	TITLE RX02 FLOPPY DISK CONTROLLER	SIZE/CODE DCS	NUMBER M7744-01	REV. J
							SCALE	SHEET 9 OF 10	DIST.	

REV. 1
M7744-01
DCS

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M7744-01



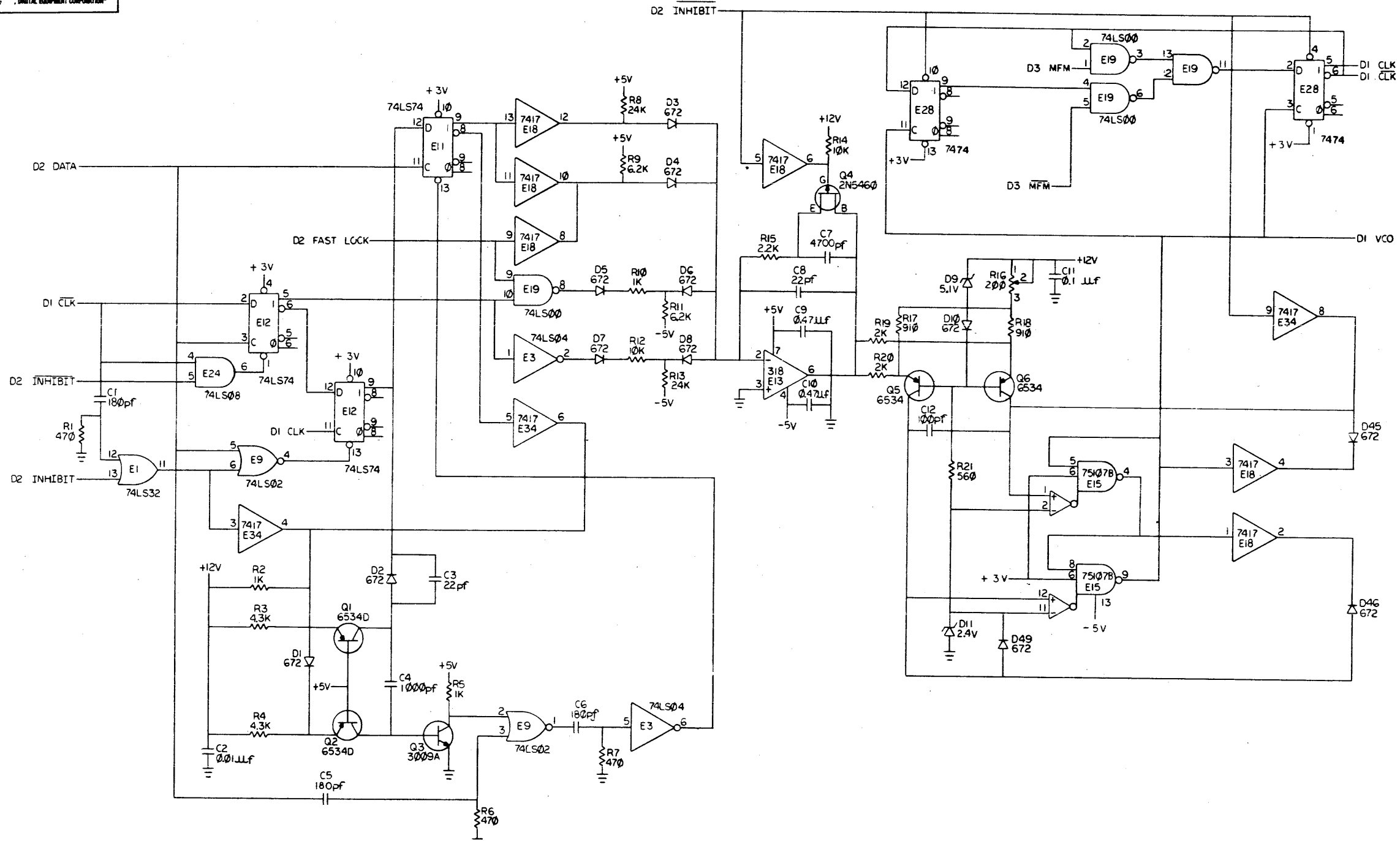
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 SIZE CODE: DCS
 NUMBER: M7744-01
 REV: J
 SCALE: / / SHEET 10 OF 10 DIST. / /

DIGITAL EQUIPMENT CORPORATION
M7744-01

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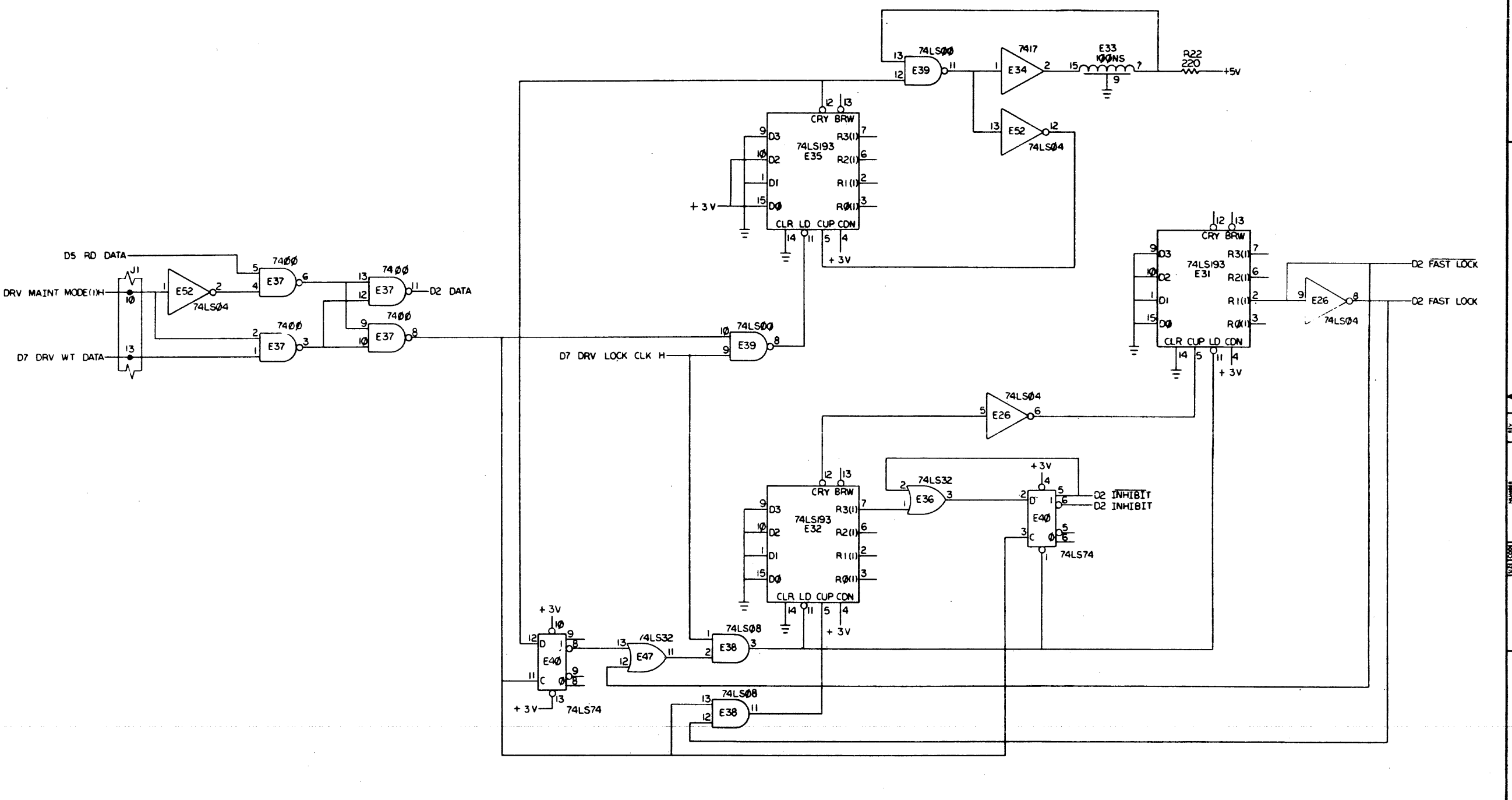
1-0-6222M CS 2



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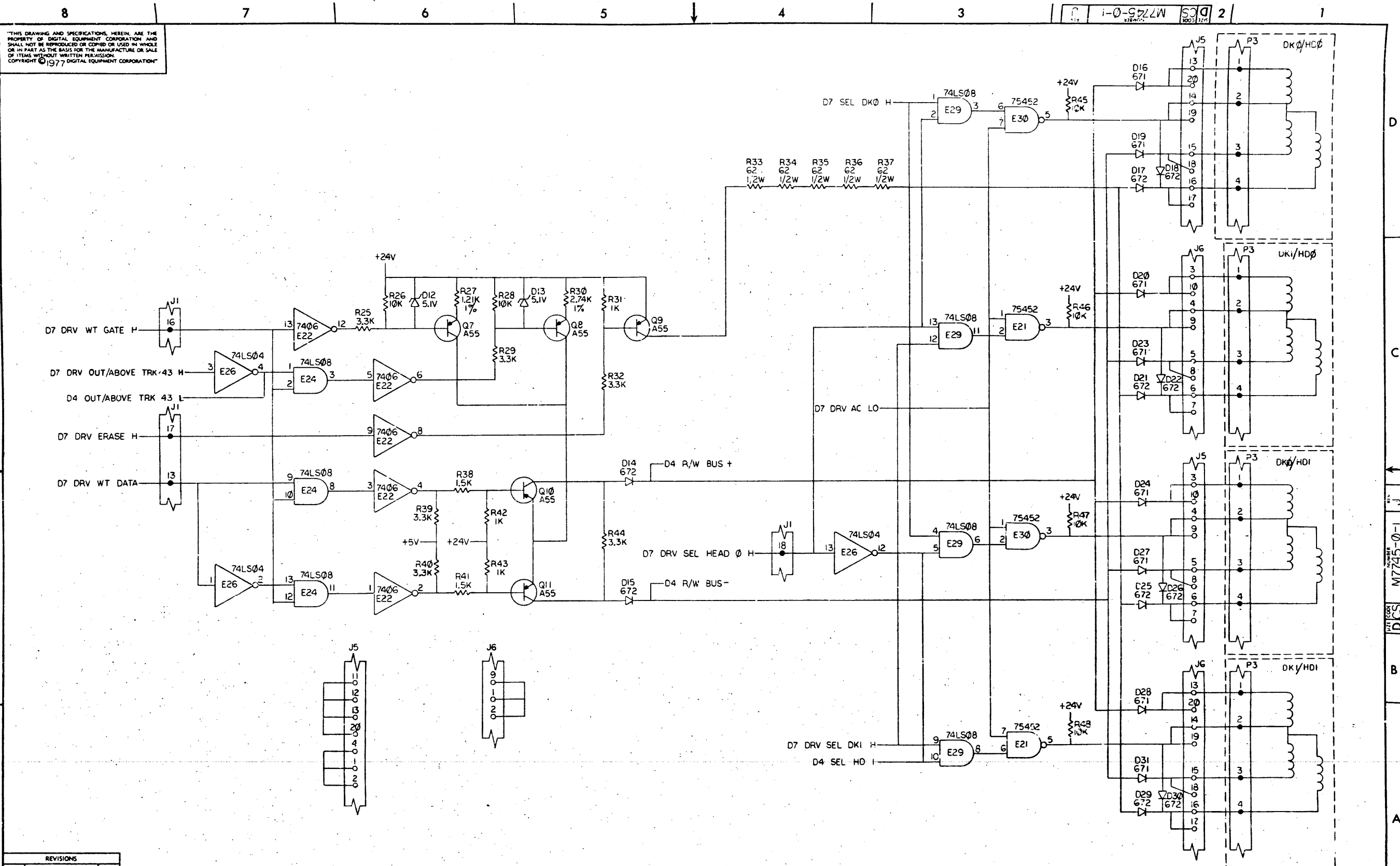
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CHK'D <i>[Signature]</i>	TITLE	READ/WRITE CONTROL
PROJ. ENG. <i>[Signature]</i>	NUMBER	M7745-0-1
PROD. <i>[Signature]</i>	REV.	J
NEXT HIGHER ASSY.		
B-DD-M7745-0		
SCALE 1 OF 7		
SHEET 1 OF 7		

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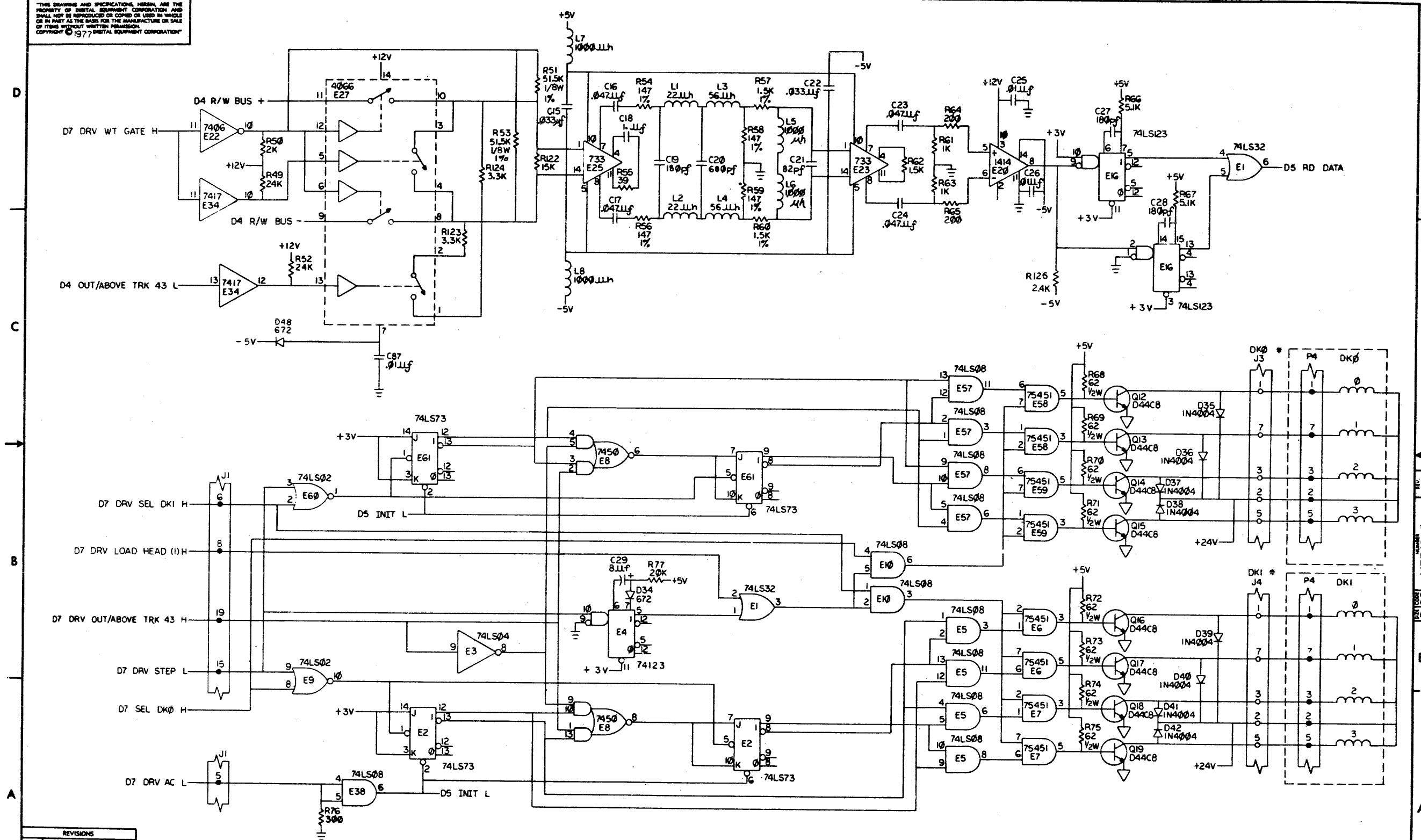
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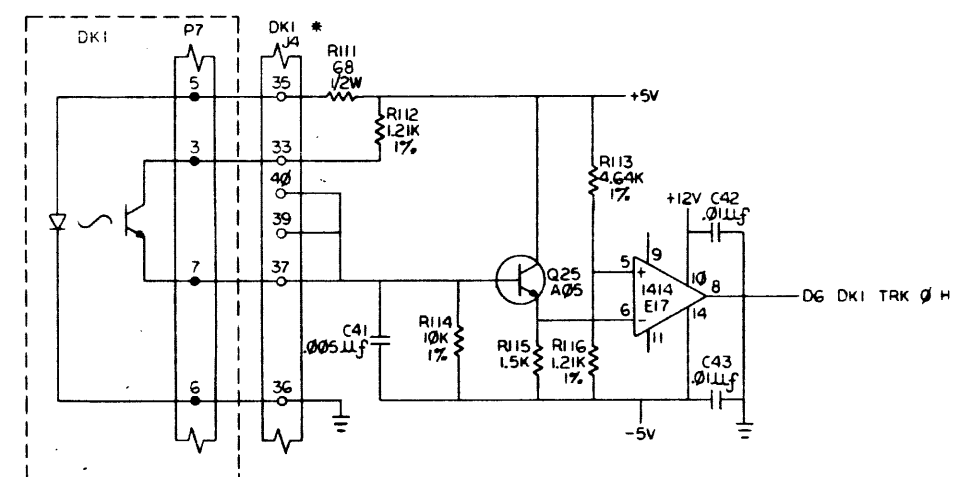
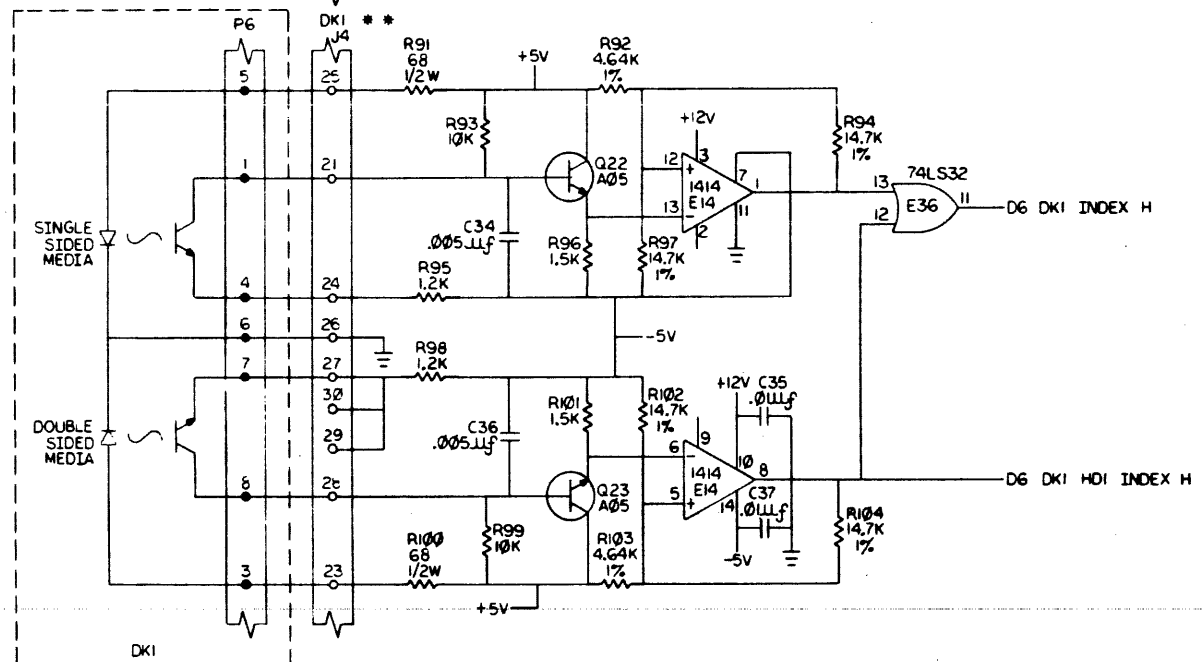
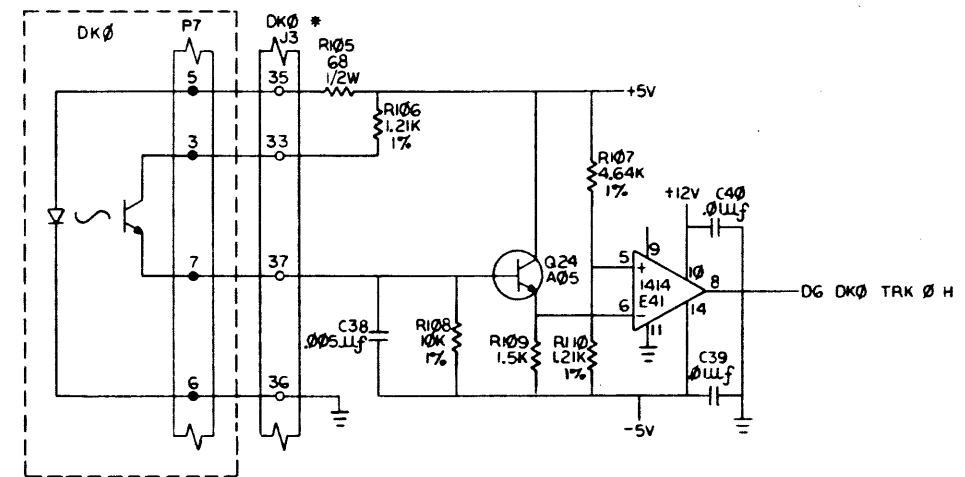
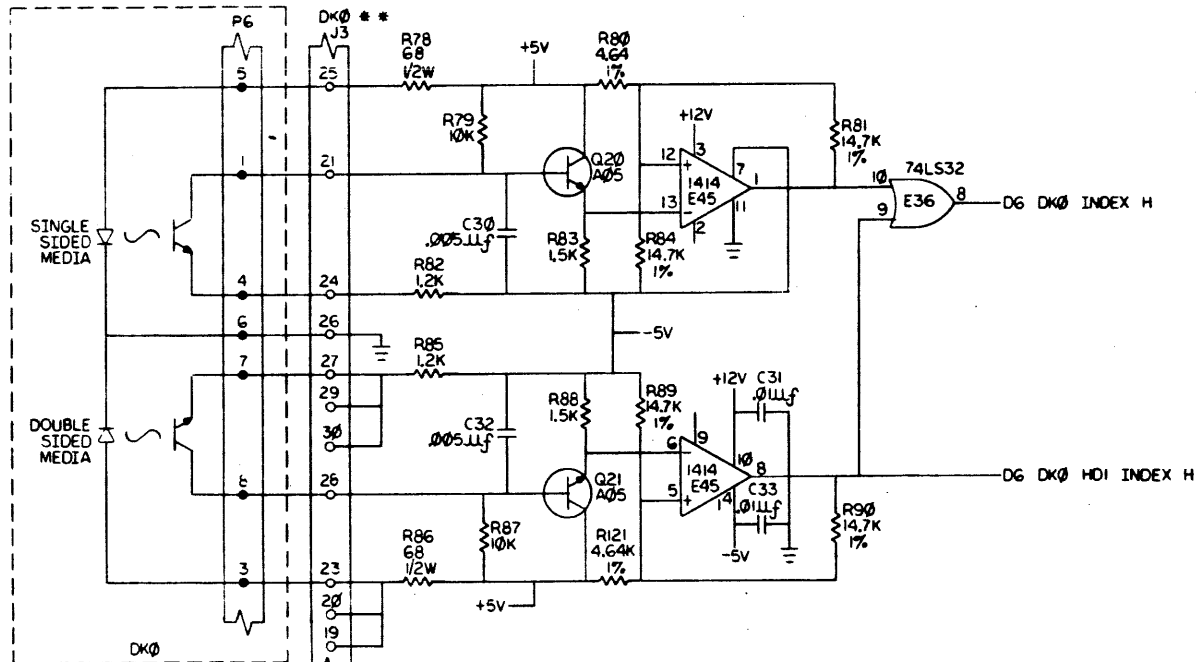
1-0-9D11W SCD 2



REVISIONS		
CHK	CHANGE NO.	REV

TITLE (D5) READ/WRITE CONTROL SIZE CODE DCS NUMBER M7745-0-1 REV. J
 SCALE SHEET 5 OF 7 DIST.

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NOTE:
 * P7-PIN 4 LOCATION IS USED FOR KEY
 * P6-PIN 2 LOCATION IS USED FOR KEY

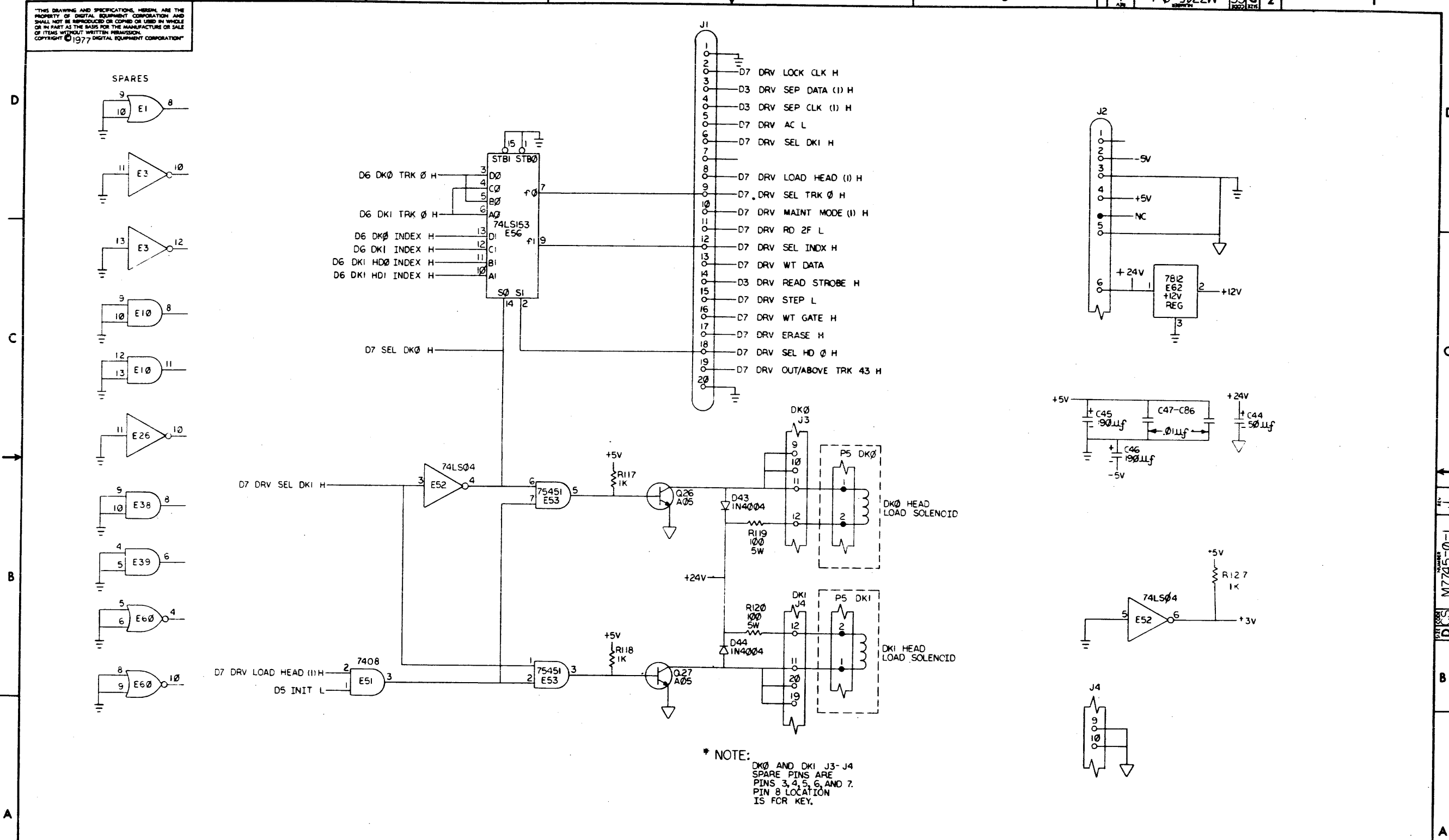
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	(D6)	SIZE CODE	NUMBER	REV.
READY/WRITE CONTROL	D CS	M7745-0-1	J	
SCALE	SHEET 6 OF 7	DIST.		

DCS M7745-0-1
 J

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1-0-06221M DCS 2



REVISIONS		
CHK	CHANGE NO.	REV

TITLE: READ/WRITE CONTROL (D7) SIZE: 0008 NUMBER: M7745-0-1 REV: J
 SCALE: SHEET 7 OF 7 DIST.

REV. 001 DCS M7745-0-1 J

