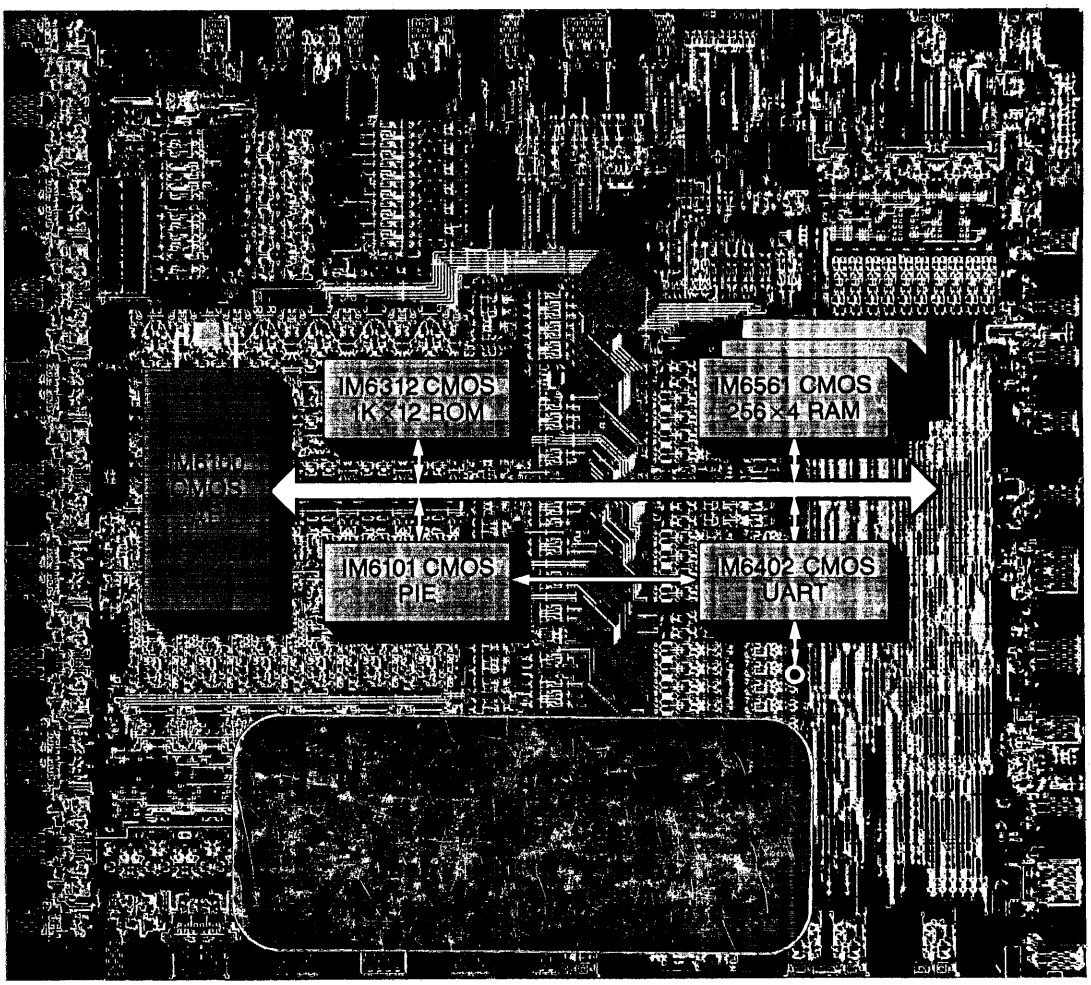
INTERSIL IM6100 CMOS 12 BIT MICROPROCESSOR

INTERSIL



CONTENTS

INTRODUCTION

Since its founding on July 26, 1967, Intersil, Inc. has become a company of many products and processes.

In addition to the digital CMOS devices covered in detail in this publication, Intersil has developed and markets a line of advanced linear products and semiconductor memories. TTL bipolar, MOS, metal-gate CMOS and silicon-gate CMOS processes are all represented in Intersil's line, with the significant design advantage that, because they were developed by a single forward-thinking company, many of the different kinds of devices and technologies produced by Intersil will work together for enhanced performance and greater efficiency and flexibility of the final developed product.

The Silicon Gate CMOS process, which was developed at Intersil over two years ago, offers a semiconductor structure resulting in packing densities which surpass the conventional metal gate process 3:1. Additionally, circuit performance is improved 2:1.

Mass production experience with the Silicon Gate CMOS process, through previously announced 256 and 1024 bit CMOS RAMs, has lead to the practicality of introducing the IM6100 microprocessor.

The IM6100 and IM6100A are single address, fixed word length, parallel transfer microprocessors using 12-bit, two's complement arithmetic. The processors recognize the instruction set of Digital Equipment Corporation's PDP-8/e minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. A 12-bit memory-accumulator ADD instruction is performed in 5μsec by the IM6100 using a +5 volt supply and in 2.5μsec by the IM6100A using a +10 volt supply. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

SECTION I: INTERSIL IM6100 CMOS 12 BIT MICROPROCESSOR

INTRODUCTION

IM6100 MICROPROCESSOR

Since its founding on July 26, 1967, INTERSIL INC. has offered its customers advanced products utilizing the semiconductor industry's most technologically sophisticated processes for the manufacture of practical, economical devices.

The Silicon Gate CMOS process, which was developed at Intersil in 1972, offers a semiconductor structure resulting in packing densities which surpass the conventional metal gate process 3:1. Additionally, circuit performance is improved 2:1.

Mass production experience with the Silicon Gate CMOS process, through previously announced 256 and 1024 bit CMOS RAMs, has lead to the practicality of introducing the IM6100 microprocessor.

The IM6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit, two's complement arithmetic. The processors recognize the instruction set of Digital Equipment Corporation's PDP-8/e minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. A 12-bit memory-accumulator ADD instruction, using a +5 volt supply, is performed in 5μsec by the IM 6100, in 6μsec by the IM6100C and in 2.5μsec by the IM6100A using a +10 volt supply. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

FEATURES

DESIGN

- Silicon Gate Complementary MOS
- Fully Static-0 to 8 MHz
- Single Power Supply
  IM6100/C V_{CC} = 5 volts
  IM6100A V_{CC} = 10 volts
- Crystal Controlled On Chip Timing
- Low Power Dissipation < 10mW @ 4 MHz @ 5 volts
- Single Power Supply 4V ≤ V_{CC} ≤ 11V
- TTL Compatible at 5 volts
- Excellent Noise Immunity
- −55°C to +125°C Operation

INTERFACE

- Memory — Any Speed
- Control Panel
- Switch Register
- Asynchronous CPU — Memory and CPU — Device Communication
- 64 I/O Devices with PDP-8/e Compatible Interface
- Device Controlled Input-Output
- All Control Signals Produced By The CPU
- Power-on Initialize

ARCHITECTURAL

- Executes PDP-8/e, Instruction Set
- Direct, Indirect, and Autoindexed Memory Addressing
- 12-Bit Memory Accumulator ADD Instruction
  IM6100 5μsec @ +5 volts/4.0 MHz
  IM6100A 2.5μsec @ +10 volts/8.0 MHz
  IM6100C 6μsec @ +5 volts/3.3 MHz
- Input-Output Instruction
  IM6100 8.5μsec @ +5 volts/4.0 MHz
  IM6100A 4.25μsec @ +10 volts/8 MHz
  IM6100C 10.2μsec @ +5 volts/3.3 MHz
- Single-Clock, Single-Instruction Capability
- Direct Memory Access (DMA)
- Interrupt
- Dedicated Control Panel Features

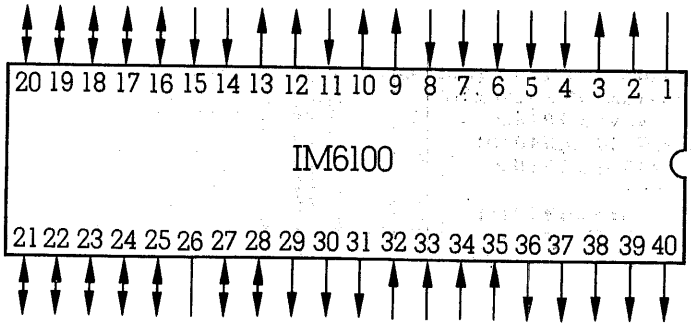
APPLICATIONS

- Intelligent Computer Terminals
- POS Terminals
- Portable Terminals
- Aerospace/Satellite System
- Automotive Systems
- Remote Data Acquisition Systems
- Process Control
- Instrumentation
- Medical Electronics
- Displays
- Traffic Control
- Navigation

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{cc}		Supply voltage.
2	RUN	H	The signal indicates the runstate of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	DMAREQ	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
5	CPREQ	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/HLT	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip flop.
7	RESET	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	INTREQ	L	Peripheral device interrupt request.
9	XT_A	H	External coded minor cycle timing—signifies input transfers to the IM6100.

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	WAIT	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running.
12	XT_B	H	External coded minor cycle timing—signifies output transfers from the IM6100.
13	XT_C	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX_0		DataX—multiplexed data in, data out and address lines.
17	DX_1		See Pin 16—DX_0.
18	DX_2		See Pin 16—DX_0.
19	DX_3		See Pin 16—DX_0.
20	DX_4		See Pin 16—DX_0.



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX_5		See Pin 16—DX_0.
22	DX_6		See Pin 16—DX_0.
23	DX_7		See Pin 16—DX_0.
24	DX_8		See Pin 16—DX_0.
25	DX_9		See Pin 16—DX_0.
26	GND		Ground
27	DX_{10}		See Pin 16—DX_0.
28	DX_{11}		See Pin 16—DX_0.
29	LINK	H	Link flip flop.
30	DEVSEL	L	Device Select for I/O transfers.
31	SWSEL	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	C_0	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	C_1	L	See Pin 32—C_0.
34	C_2	L	See Pin 32—C_0.
35	SKP	L	Skips the next sequential instruction if active during an I/O instruction.
36	IFETCH	H	Instruction Fetch Cycle
37	MEMSEL	L	Memory Select for memory transfers.
38	CPSEL	L	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

SPECIFICATIONS

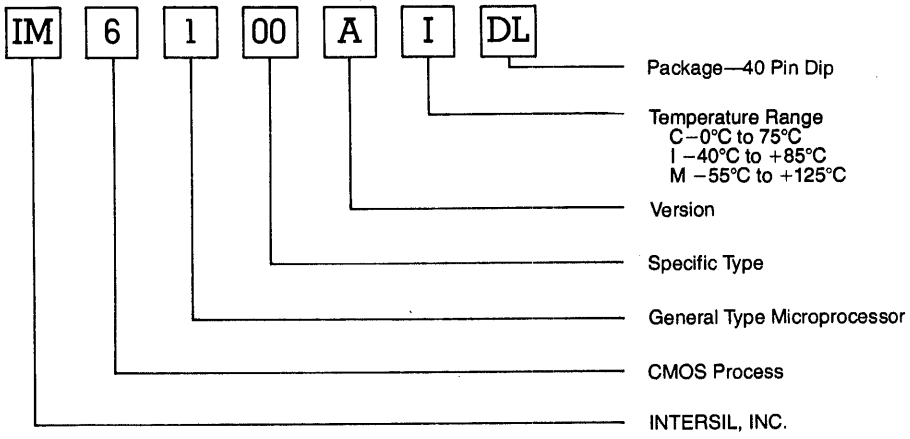
ABSOLUTE MAXIMUM RATINGS

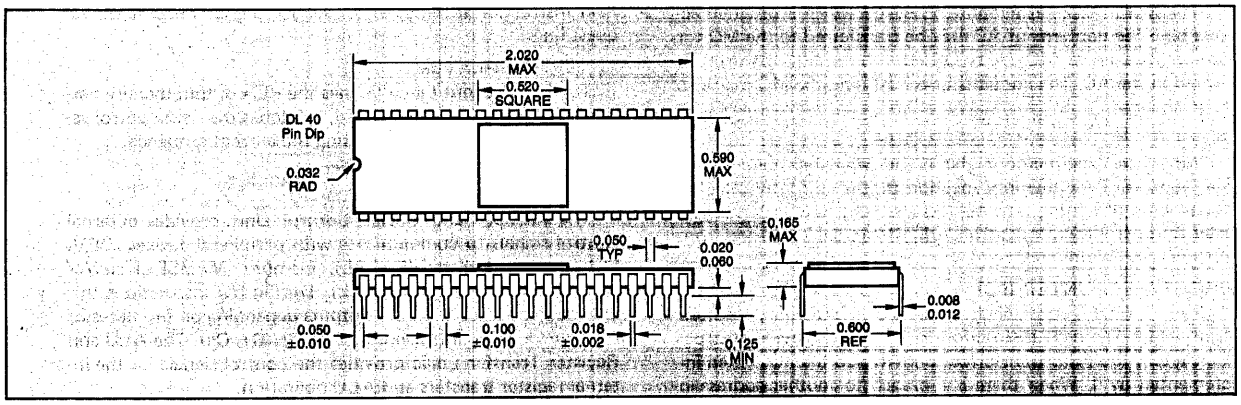
Supply Voltage	IM6100/C +4.0V to +7.0V	Operating Temperature Range	
	IM6100A +4.0V to 11.0V	Commercial	0°C to +70°C
Input or Output Voltage Applied	GND - 0.3V to V_{CC} +0.3V	Industrial	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C	Military	-55°C to +125°C

DC CHARACTERISTICS V_{cc} = 5.0V ± 10% (IM6100), 10.0V ± 10% (IM6100A), T_A = Commercial, Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{cc}			V
Logical "0" Input Voltage	V_{IL}				20%V_{CC}	V
Input Leakage	I_{IL}	$OV \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	I_{OUT}=0	V_{cc}-0.01			V
Logical "1" Output Voltage	V_{OH1}	I_{OH}=-0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	I_{OUT}=0			GND +0.01	V
Logical "0" Output Voltage	V_{OL1}	I_{OL}=1.6 mA			0.45	V
Output Leakage	I_O	$OV \leq V_o \leq V_{cc}$	-1.0		1.0	μA
Supply Current	I_{CC}	V_{CC} = 5.0 volts			2.5	mA
		V_{CC} = 10.0 volts			10.0	mA
		C_L= 50 pF; TA = 25°C				
		F_{CLOCK} = Operating Frequency				
Input Capacitance	C_{IN}			5.0		pF
Output Capacitance	C_O			8.0		pF

ORDERING INFORMATION Circuit marking and product code explanation

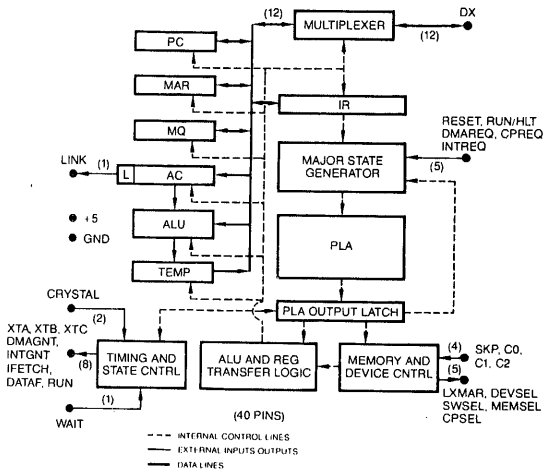




ARCHITECTURE

The IM6100 has 6 twelve bit registers, a programmable logic array, an arithmetic and logic unit and associated gating and timing circuitry. A block diagram of the IM6100 is shown in Figure 1.

FIGURE 1



ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from the memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

LINK (L)

The Link is a 1-bit flip-flop that serves as a high-order extension of the AC. It is used as a carry flip-flop for 2's complement arithmetic. A carry out of the ALU complements the Link. Link can be cleared, set, complemented and tested under program control and rotated as part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

MEMORY ADDRESS REGISTER (MAR)

While accessing memory, the 12-bit MAR register contains the address of the memory location that is currently selected for reading or writing. The MAR is also used as an internal register for microprogram control during data transfers to and from memory and peripherals.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to MAR and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. However, during an input-output operation, a device may specify a branch address. A skip (SKP) instruction increments the PC by 1, thus causing the next instruction to be skipped. The SKP instruction may be unconditional or conditional on the state of the AC and/or the Link. During an input-output operation, a device can also cause the next sequential instruction to be skipped.

ARITHMETIC AND LOGICAL UNIT (ALU)

The ALU performs both arithmetic and logical operations — 2's complement binary addition, AND, OR and complement. The ALU can perform a single position shift either to the left or to the right. A double rotate is implemented in two single bit shifts. The ALU can also shift by 3 positions to implement a byte swap in two steps. The AC is always one of the inputs to the ALU. However, under internal microprogram control, AC may be gated off and all one's or all zero's gated in. The second input may be any one of the other registers under internal microprogram control.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register for microprogram control.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction and is also used as an internal register to store temporary data for microprogram control.

MULTIPLEXER (DX)

The 12-bit Input/Output Multiplexer handles data, address and instruction transfers into and out of the CPU, from or into the main memory and peripheral devices on a time-multiplexed basis.

MAJOR STATE GENERATOR AND THE PROGRAMMED LOGIC ARRAY (PLA)

During an instruction fetch the instruction to be executed is loaded into the IR. The PLA is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state generator scans the internal priority network. The state of the priority network decides whether the machine is going to fetch the next instruction in sequence or service one of the external request lines.

PLA OUTPUT LATCH

The PLA Output Latch latches the PLA output thereby permitting the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

MEMORY AND DEVICE CONTROL, ALU AND REG TRANSFER LOGIC

The Memory and Device Control Unit provides external control signals to communicate with peripheral devices (DEVSEL), switch register (SWSEL), memory (MEMSEL) and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs depending on the states of the four device control lines (SKP, C_0, C_1, C_2). The ALU and Register Transfer Logic provides the control signals for the internal register transfers and ALU operation.

TIMING AND STATE CONTROL

The IM6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500nsec duration. The major timing states are described in Figure 2.

T_1 For memory reference instructions, a 12-bit address is sent on the DataX, DX lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information. LXMAR pulse is active only if a valid address is present on the DX lines.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T_2 Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T_2 state. The wait duration is an integral multiple of the crystal frequency – 250nsec for 4MHz.

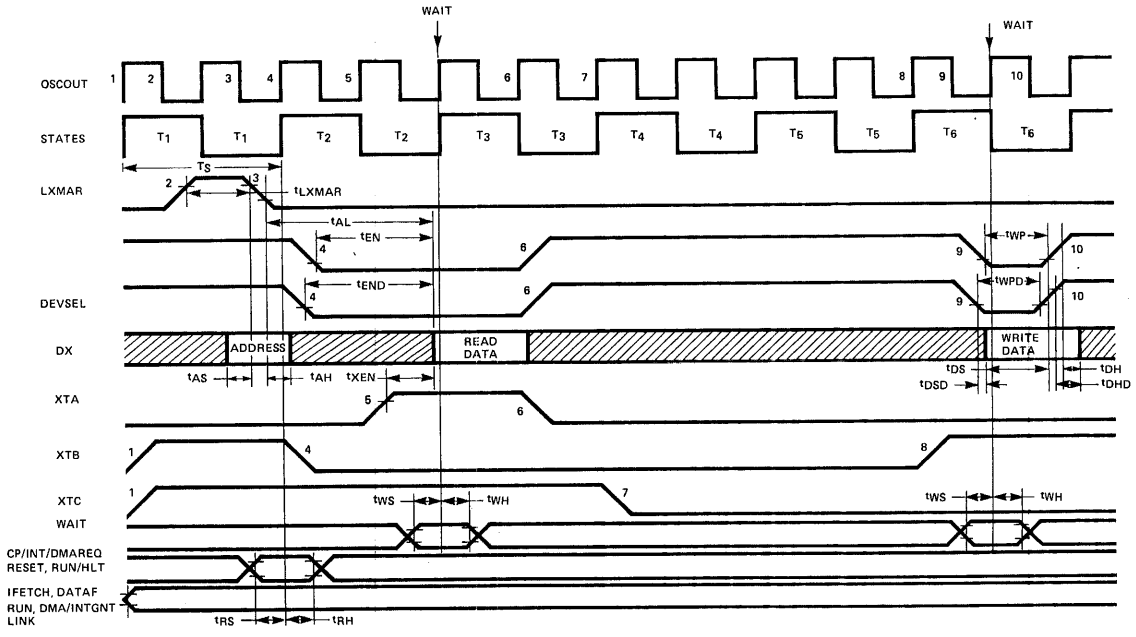
For memory reference instructions, the Memory Select, MEMSEL, line is active. For I/O instructions the Device Select, DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines, C_0, C_1, C_2, and SKP, are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the IM6100 and Control Panel Memory and the Switch Register, respectively.

T_3, T_4, T_5, T_6 ALU operation and internal register transfers. This state is entered for an output transfer (WRITE). The address is defined during T_1. WAIT controls the time for which the Write data must be maintained.

FIGURE 2



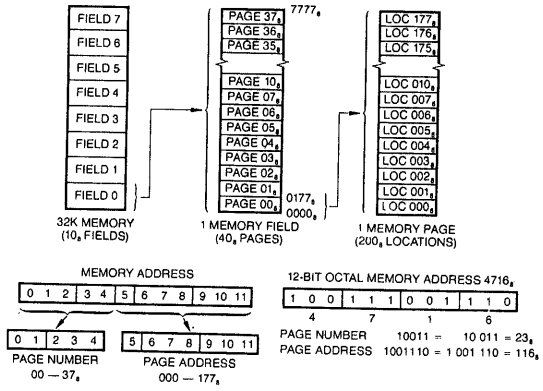
MEMORY AND PROCESSOR INSTRUCTIONS

The IM6100 instructions are 12-bit words stored in memory. The IM6100 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of IM6100 instructions. They are referred to as Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT).

Before proceeding further, we will discuss the Specific Memory Organization with which the IM6100 interfaces.

MEMORY ORGANIZATION

The IM6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended by Extended Memory Control hardware. The memory system is organized in 4096 word blocks, called MEMORY FIELDS. The first 4096 words of memory are in Field 0. If a full 32K of memory is installed, the uppermost Memory Field will be numbered 7. In any given Memory Field every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). Each Memory Field is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.



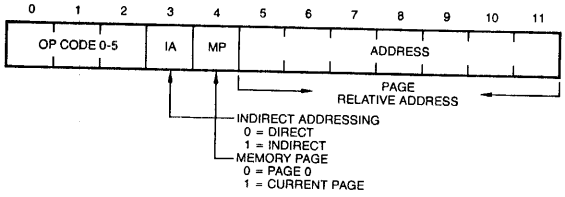
MEMORY ORGANIZATION

During an instruction fetch cycle, the IM6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The MAR contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), by definition, denotes the first 128 words of memory, 0000_8-0177_8.)

MEMORY REFERENCE INSTRUCTION (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 3.

FIGURE 3



MEMORY REFERENCE INSTRUCTION FORMAT

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR PAGE 0 BIT. If bit 4 is a 0, the page address is interpreted as a location on Page 0. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

For example, if bits 5 through 11 represent 123_8 and bit 4 is a 0, the location referenced is the absolute address 0123_8. However, if bit 4 is a 1 and the current instruction is in a memory location whose absolute address is 4610_8 the page address 123_8 designates the absolute address 4723_8, as shown below.

4610_8 = 100 110 001 000 = PAGE 10 011 = PAGE 23_8

Location 4610_8 is in PAGE 23_8. Location 123_8 in PAGE 23_8, CURRENT PAGE, will be:

10 011 1 010 011 = 100 111 010 011 = 4723_8

PAGE NUMBER 23_8 — PAGE ADDRESS 123_8

By this method, 256 locations may be directly addressed, 128 on PAGE 0 and 128 on the CURRENT PAGE. Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in Page 0 or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location.

It should be noted that locations 0010_8-0017_8 in PAGE 0 are AUTOINDEXED. If these locations are addressed indirectly, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications.

Table 1 lists the mnemonics for the five memory reference instruction, their OPCODE, the operations they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600nsec, 500nsec and 250nsec, respectively.

It should be noted that the data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the IM6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777_8 (+2047) and 4000_8 (−2048).

Notations applied in Table 1, are defined as follows:

( ) Denotes the contents of the register or location within the parentheses. (EA) is read as " . . . the contents of the Effective Address."

(( )) Denotes the contents of the location pointed to by the contents of the location within the double parentheses. ((PA)) is read as " . . . the contents of the location pointed to by the contents of the Pointer Address."

<— Denotes " . . . is replaced by . . . "

∧ Denotes, logical AND operation

∨ Denotes, logical OR operation

TABLE 1

MNE-MONIC	OP CODE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs) IM6100 +5.0V 4MHz	IM6100A +10.0V 8MHz	IM6100C +5.0V 3.3MHz
AND	0_8	LOGICAL AND DIRECT (I = 0) Operation: (AC) <—(AC)∧(EA) Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.	10	5.0	2.50	6.0
		LOGICAL AND INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: (AC) <—(AC)∧((PA))	15	7.5	3.75	9.0
		LOGICAL AND AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; (AC) <—(AC)∧((PA))	16	8.0	4.00	9.6
TAD	1_8	BINARY ADD DIRECT (I = 0) Operation: (AC) · —(AC) + (EA) Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC, carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory	10	5.0	2.50	6.0
		BINARY ADD INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: (AC) · —(AC) + ((PA))	15	7.5	3.75	9.0
		BINARY ADD AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; (AC) · —(AC) + ((PA))	16	8.0	4.00	9.6
ISZ	2_8	INCREMENT AND SKIP IF ZERO DIRECT (I = 0) Operation: (EA) <—(EA) + 1; if (EA) = 0000_8, PC <—PC + 1 Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.	16	8.0	4.00	9.6
		INCREMENT AND SKIP IF ZERO INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: ((PA)) <—((PA)) + 1; if ((PA)) = 0000_8, PC <—PC + 1	21	10.5	5.25	12.6
		INCREMENT AND SKIP IF ZERO AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; ((PA)) <—((PA)) + 1; if ((PA)) = 0000_8, PC <—PC + 1	22	11.0	5.50	13.2
DCA	3_8	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT (I = 0) Operation: (EA) <—(AC); (AC) · —0000_8 Description: The contents of the AC are stored in EA and the AC is cleared.	11	5.5	2.75	6.6
		DEPOSIT AND CLEAR THE ACCUMULATOR INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: ((PA)) · —(AC); (AC) · —0000_8	16	8.0	4.00	9.0
		DEPOSIT AND CLEAR THE ACCUMULATOR AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; ((PA)) · —(AC); (AC) · —0000_8	17	8.5	4.25	10.2
JMS	4_8	JUMP TO SUBROUTINE DIRECT (I = 0) Operation: (EA) <—(PC); (PC) <—EA + 1 Description: The contents of the PC are stored in the EA. The PC is incremented by 1 immediately after every instruction fetch. The contents of the EA now point to the next sequential instruction following the JMS (return address). The next instruction is taken from EA + 1.	11	5.5	2.75	6.6
		JUMP TO SUBROUTINE INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: ((PA)) <—PC; (PC) <—(PA) + 1	16	8.0	4.00	9.6
		JUMP TO SUBROUTINE AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; ((PA)) <—PC; (PC) <—(PA) + 1	17	8.5	4.25	10.2
JMP	5_8	JUMP DIRECT (I = 0) Operation: (PC) <—EA Description: The next instruction is taken from the EA.	10	5.0	2.50	6.0
		JUMP INDIRECT (I = 1, PA ≠ 0010-0017$_8$) Operation: (PC) <—(PA)	15	7.5	3.75	9.0
		JUMP AUTOINDEX (I = 1, PA = 0010-0017$_8$) Operation: (PA) <—(PA) + 1; (PC) <—(PA)	16	8.0	4.00	9.6

MEMORY REFERENCE INSTRUCTIONS

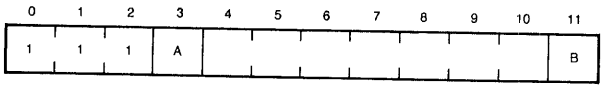
OPERATE INSTRUCTIONS

The Operate Instructions, which have an OPCODE of 7_8 (111), consists of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 microinstructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 4.

Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

FIGURE 4



MICROINSTRUCTION	A	B
GROUP 1	0	0 / 1
GROUP 2	1	0
GROUP 3	1	1

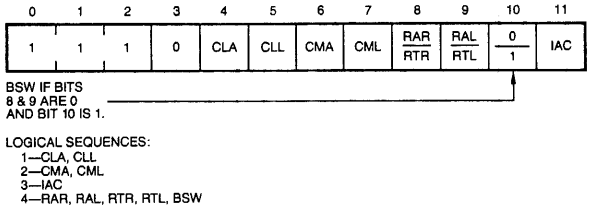
BASIC OPR INSTRUCTION FORMAT

GROUP 1 MICROINSTRUCTIONS

Figure 5 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5.

Table 2 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600nsec, 500nsec and 250nsec, respectively. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

FIGURE 5



GROUP 1 MICROINSTRUCTION FORMAT

TABLE 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs) IM6100 +5.0V 4MHz	IM6100A +10.0V 8MHz	IM6100C +5.0V 3.3MHz
NOP	7000	1	NO OPERATION—This instruction causes a 10 state delay in program execution, without affecting the state of the IM6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.	10	5.0	2.50	6.0
IAC	7001	3	INCREMENT ACCUMULATOR—The content of the AC is incremented by one (1) and carry out complements the Link (L).	10	5.0	2.50	6.0
RAL	7004	4	ROTATE ACCUMULATOR LEFT—The contents of the AC and L are rotated one binary position to the left. AC (0) is shifted to L and L is shifted to AC (11).	15	7.5	3.75	9.0
RTL	7006	4	ROTATE TWO LEFT—The contents of the AC and L are rotated two binary positions to the left. AC (1) is shifted to L and L is shifted to AC (10).	15	7.5	3.75	9.0
RAR	7010	4	ROTATE ACCUMULATOR RIGHT—The content of the AC and L are rotated one binary position to the right. AC (11) is shifted to L and L is shifted to AC (0).	15	7.5	3.75	9.0
RTR	7012	4	ROTATE TWO RIGHT—The contents of the AC and L are rotated two binary positions to the right. AC (10) is shifted to L and L is shifted to AC (1).	15	7.5	3.75	9.0
BSW	7002	4	BYTE SWAP—The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC (0) is swapped with AC (6), AC (1) with AC (7), etc. L is not affected.	15	7.5	3.75	9.0
CML	7020	2	COMPLEMENT LINK—The content of the link is complemented.	10	5.0	2.50	6.0
CMA	7040	2	COMPLEMENT ACCUMULATOR—The content of each bit of the AC is complemented having the effect of replacing the content of the AC with its one's complement.	10	5.0	2.50	6.0
CIA	7041	2,3	COMPLEMENT AND INCREMENT ACCUMULATOR—The content of the AC is replaced with its two's complement. Carry out complements the LINK.	10	5.0	2.50	6.0
CLL	7100	1	CLEAR LINK—The link is loaded with a binary 0.	10	5.0	2.50	6.0
CLL RAL	7104	1,4	CLEAR LINK—ROTATE ACCUMULATOR LEFT.	15	7.5	3.75	9.0
CLL RTL	7106	1,4	CLEAR LINK—ROTATE TWO LEFT.	15	7.5	3.75	9.0
CLL RAR	7110	1,4	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.	15	7.5	3.75	9.0
CLL RTR	7112	1,4	CLEAR LINK—ROTATE TWO RIGHT.	15	7.5	3.75	9.0
STL	7120	1,2	SET THE LINK—The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.	10	5.0	2.50	6.0
CLA	7200	1	CLEAR ACCUMULATOR—The accumulator is loaded with binary 0's.	10	5.0	2.50	6.0
CLA IAC	7201	1,3	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.	10	5.0	2.50	6.0
GLT	7204	1,4	GET THE LINK—The AC is cleared; the content of L is shifted into AC (11), a 0 is shifted into L. This is a microprogrammed combination of CLA and RAL.	15	7.5	3.75	9.0
CLA CLL	7300	1	CLEAR ACCUMULATOR—CLEAR LINK.	10	5.0	2.50	6.0
STA	7240	1,2	SET THE ACCUMULATOR—Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.	10	5.0	2.50	6.0

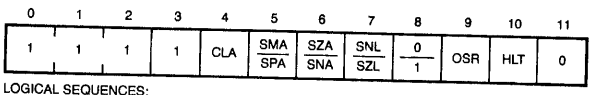
GROUP 1 OPERATION MICROINSTRUCTIONS

GROUP 2 MICROINSTRUCTIONS

Figure 6 shows the instruction format of group 2 microinstructions. Bits 4 – 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 – 7 or 9 – 10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or, when bit 8 is 1, the decision will be based on the logical AND.

FIGURE 6



LOGICAL SEQUENCES:
1 (Bit 8 is Zero) — SMA or SZA or SNL
(Bit 8 is One) — SPA and SNA and SZL
2 — CLA
3 — OSR, HLT

GROUP 2 MICROINSTRUCTION FORMAT

TABLE 3

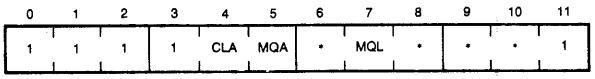
MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs) IM6100 +5.0V 4MHz	IM6100A +10.0V 8MHz	IM6100C +5.0V 3.3MHz
NOP	7400	1	NO OPERATION—See GROUP 1 MICROINSTRUCTIONS	10	5.0	2.50	6.0
HLT	7402	3	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.	10	5.0	2.50	6.0
OSR	7404	3	OR WITH SWITCH REGISTER—The content of the Switch Register if OR'ed with the content of the AC and the result is stored in the AC. The OSR INSTRUCTION TIMING is shown in Figure 8. The IM6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B.	15	7.5	3.75	9.0
SKP	7410	1	SKIP—The content of the PC is incremented by 1, to skip the next sequential instruction.	10	5.0	2.50	6.0
SNL	7420	1	SKIP ON NON-ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.	10	5.0	2.50	6.0
SZL	7430	1	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.	10	5.0	2.50	6.0
SZA	7440	1	SKIP ON ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has all bits which are 0. If any bit in the AC is a 1, the next instruction is executed.	10	5.0	2.50	6.0
SNA	7450	1	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.	10	5.0	2.50	6.0
SZA SNL	7460	1	SKIP ON ZERO ACCUMULATOR, *OR* SKIP ON NON-ZERO LINK, *OR* BOTH	10	5.0	2.50	6.0
SNA SZL	7470	1	SKIP ON NON-ZERO ACCUMULATOR *AND* SKIP ON ZERO LINK	10	5.0	2.50	6.0
SMA	7500	1	SKIP ON MINUS ACCUMULATOR—If the content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.	10	5.0	2.50	6.0
SPA	7510	1	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.	10	5.0	2.50	6.0
SMA SNL	7520	1	SKIP ON MINUS ACCUMULATOR *OR* SKIP ON NON-ZERO LINK *OR* BOTH	10	5.0	2.50	6.0
SPA SZL	7530	1	SKIP ON POSITIVE ACCUMULATOR *AND* SKIP ON ZERO LINK	10	5.0	2.50	6.0
SMA SZA	7540	1	SKIP ON MINUS ACCUMULATOR *OR* SKIP ON ZERO ACCUMULATOR *OR* BOTH	10	5.0	2.50	6.0
SPA SNA	7550	1	SKIP ON POSITIVE ACCUMULATOR *AND* SKIP ON NON-ZERO ACCUMULATOR	10	5.0	2.50	6.0
SMA SZA SNL	7560	1	SKIP ON MINUS ACCUMULATOR *OR* SKIP ON ZERO ACCUMULATOR *OR* SKIP ON NON-ZERO LINK *OR* ALL	10	5.0	2.50	6.0
SPA SNA SZL	7570	1	SKIP ON POSITIVE ACCUMULATOR *AND* SKIP ON NON-ZERO ACCUMULATOR *AND* SKIP ON ZERO LINK	10	5.0	2.50	6.0
CLA	7600	2	CLEAR ACCUMULATOR—The AC is loaded with binary 0's.	10	5.0	2.50	6.0
LAS	7604	1,3	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.	15	7.5	3.75	9.0
SZA CLA	7640	1,2	SKIP ON ZERO ACCUMULATOR *THEN* CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SNA CLA	7650	1,2	SKIP ON NON-ZERO ACCUMULATOR *THEN* CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SMA CLA	7700	1,2	SKIP ON MINUS ACCUMULATOR *THEN* CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SPA CLA	7710	1,2	SKIP ON POSITIVE ACCUMULATOR *THEN* CLEAR ACCUMULATOR	10	5.0	2.50	6.0

GROUP 2 OPERATE MICROINSTRUCTIONS

GROUP 3 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 7.

FIGURE 7



LOGICAL SEQUENCE:
1—CLA
2—MQA, MQL
3—ALL OTHERS

*Don't Care

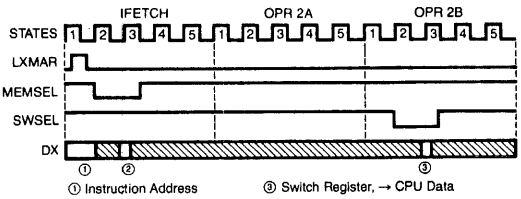
GROUP 3 MICROINSTRUCTION FORMAT

TABLE 4

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs) IM6100 +5.0V 4.0MHz	IM6100A +10.0V 8.0MHz	IM6100C +5.0V 3.3MHz
NOP	7401	3	NO OPERATION—See Group 1 Microinstructions	10	5.0	2.50	6.0
MQL	7421	2	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost.	10	5.0	2.50	6.0
MQA	7501	2	MQ REGISTER INTO ACCUMULATOR—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.	10	5.0	2.50	6.0
SWP	7521	3	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MQA and MQL.	10	5.0	2.50	6.0
CLA	7601	1	CLEAR ACCUMULATOR	10	5.0	2.50	6.0
CAM	7621	3	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogrammed combination of CLA and MQL.	10	5.0	2.50	6.0
ACL	7701	3	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR—This is equivalent to a microprogrammed combination of CLA and MQA.	10	5.0	2.50	6.0
CLA SWP	7721	3	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.	10	5.0	2.50	6.0

GROUP 3 OPERATE MICROINSTRUCTIONS

FIGURE 8



OSR INSTRUCTION TIMING

INPUT/OUTPUT TRANSFER INSTRUCTIONS (IOT)

The input/output transfer instructions, which have an OP-CODE of 6$_8$ are used to initiate the operation of peripheral devices and to transfer data between peripherals and the IM 6100. Three types of data transfer may be used to receive or transmit information between the IM6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12-bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, transfers variable-size blocks of data between high-speed peripherals and the memory with a minimum of program control required by the IM6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer Instruction format, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600nsec, 500nsec and 250nsec, respectively is represented in Figure 9.

The first three bits, 0-2, are always set to 6$_8$ (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

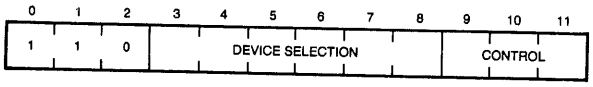
PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the IM6100 fetches an instruction from the memory and recognizes that the curr instruction is an IOT. This is referred to as IFETCH and c sists of five (5) internal states. The IM6100 sequences the I instruction through a 2-cycle execute phase referred to IOT_A and IOT_B. Bits 0-11 of the IOT instructions are availa on DX 0-11 at IOT_A • LXMAR. These bits must be latchec an external address register. DEVSEL is active low to ena data transfers between the IM6100 and the peripheral device Input-Output Instruction Timing is shown in Figure 10. T selected peripheral device communicates with the IM61 through 4 control lines – C_0, C_1, C_2 and SKP. In the IM61 the type of data transfer, during an IOT instruction, is specifi by the peripheral device(s) by asserting the control lines shown in Table 5.

The control line SKP, when low during an IOT, causes t IM6100 to skip the next sequential instruction. This feature used to sense the status of various signals in the device interfa The C_0, C_1, and C_2 lines are treated independently of t SKP line. In the case of a RELATIVE or ABSOLUTE JUM the skip operation is performed after the jump. The input s nals to the IM6100, DX 0-11, C_0, C_1, C_2, and SKP, are sampl at IOT_A during DEVSEL • XT_C. The data from the IM6100 available to the device(s) during DEVSEL • XT_C. IOT_B cyc is internal to the IM6100 to perform the operations request during IOT_A. Both IOT_A and IOT_B consist of six (6) intern states.

In summary, Programmed Data Transfer performs data I/ with a minimum of hardware support. The maximum rate which progammed data transfers may take place is limited b the IM6100 instruction execution rate. However, the data ra of the most commonly used peripheral devices is much low than the maximum rate at which programmed transfers ca take place in the IM6100. The major drawback associated wit Programmed Data Transfer is that the IM6100 must hang up i a waiting loop while the I/O device completes the last transf and prepares for the next transfer. On the other hand, th technique permits easy hardware implementation and simpl economical interface design. For this reason, almost all device except bulk storage units rely heavily on programmed dat transfer for routing data I/O.

FIGURE 9



IOT INSTRUCTION FORMAT

NUMBER OF STATES	EXECUTION TIME (μs)		
	IM6100 +5.0V 4MHz	IM6100A +10.0V 8MHz	IM6100C +5.0V 3.3MHz
17	8.5	4.25	10.2

IOT NUMBER OF STATES/EXECUTION TIME

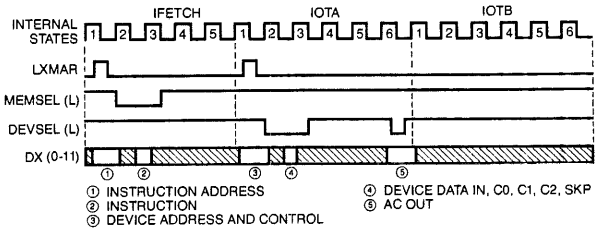
TABLE 5

CONTROL LINES C_0	C_1	C_2	OPERATION	DESCRIPTION
H	H	H	DEV <—AC	The content of the AC is sent to the device.
L	H	H	DEV <—AC;CLA	The content of the AC is sent to a device and then the AC is cleared.
H	L	H	AC <—AC V DEV	Data is received from a device, OR'ed with the data in the AC and the result is stored in the AC.
L	L	H	AC <—DEV	Data is received from a device and loaded into the AC.
*	H	L	PC <—PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
*	L	L	PC <—DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.

*Don't Care

PROGRAMMED I/O CONTROL LINES

FIGURE 10



INPUT-OUTPUT INSTRUCTION TIMING

INTERRUPT TRANSFER

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the IM6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that it requires some sort of intervention from the running program.

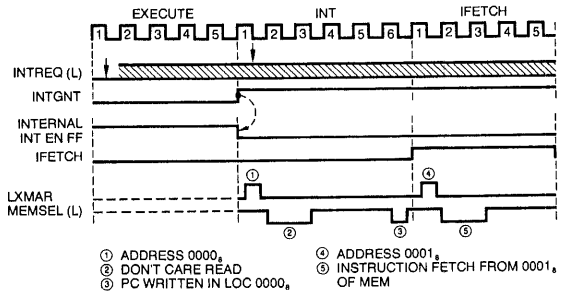
The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input to the IM6100 Low. If no higher priority requests are outstanding and the interrupt system is enabled, the IM6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the IM6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

DEVICE INTERRUPT GRANT TIMING

The current content of the Program Counter, PC, is deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved in a software stack if nested interrupts are permitted. the INTGNT, Figure 11, signal is activated by the IM6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction as shown in Figure 12. The INTGNT signal is necessary to implement the Extended Memory Control hardware when more than 4K of memory is required. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

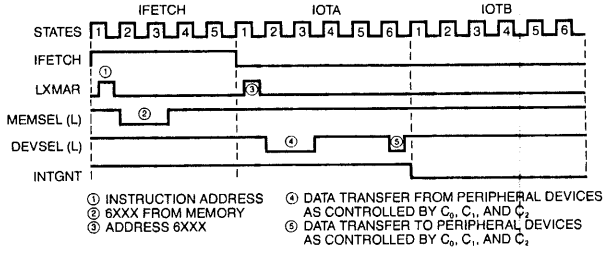
The user program controls the interrupt mechanism of the IM6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

FIGURE 11



DEVICE INTERRUPT GRANT TIMING

FIGURE 12

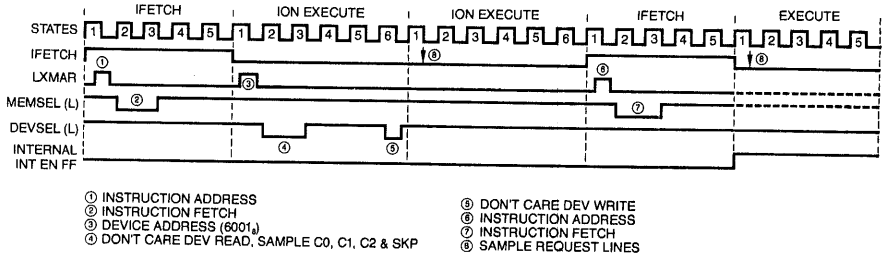


DEVICE INTERRUPT GRANT RESET TIMING

TABLE 6

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON – If interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON – The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13.
IOF	6002	INTERRUPT TURN OFF – The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST – The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS – The following machine states are read into the indicated bits of AC. bit 0 – Link bit 2 – INT request bus bit 4 – Interrupt Enable FF Other bits may be modified by external devices by controlling the C-lines. (ex. Extended memory control).
RTF	6005	RETURN FLAGS – Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control).
SGT	6006	Operation is determined by external devices, if any.
CAF	6007	CLEAR ALL FLAGS – AC and Link are cleared. Interrupt system is disabled.

FIGURE 13



INTERRUPT ENABLE FF ON (ION)

CONTROL PANEL INTERRUPT TRANSFER

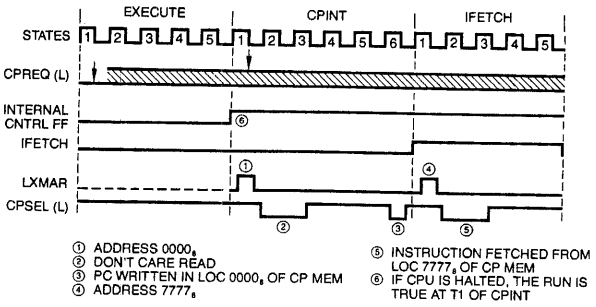
The IM6100 control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

The control panel communicates with the IM6100 with the Control Panel Request, CPREQ, line. The CPREQ is functionally similar to the INTREQ with some important differences. The CPREQ is granted even when the machine is in the HALT state. The IM6100 is temporarily put in the RUN state for the duration of the panel routine. The IM6100 reverts to its original processor state after the panel routine has been executed.

The CPREQ bypasses the interrupt enable system and the processor IOT instructions, ION and IOF, are ignored while the IM6100 is in the Control Panel Mode. Once a CPREQ is granted, the IM6100 will not recognize any DMAREQ or INTREQ until CPREQ has been fully serviced.

When a CPREQ is granted, Figure 14, the PC is stored in location 0000_8 of the Panel Memory and the IM6100 resumes operation at location 7777_8 of the Panel Memory. The Panel Memory would be organized wth RAM's in the lower pages and PROM's in the higher pages. The control panel service routine would be stored in the higher pages in the nonvolatile PROM's, starting at 7777_8.

FIGURE 14

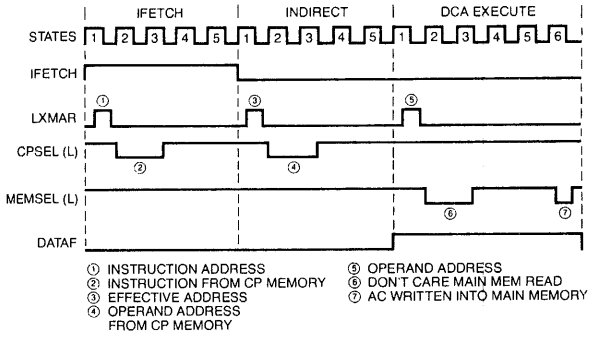


CONTROL PANEL INTERRUPT GRANT TIMING

A Control Panel Flip-Flop, CNTRL FF, which is internal to the IM6100, is set when the CPREQ is granted. The CNTRL FF prevents further CPREQ's from being granted.

As long as the CNTRL FF is set, the Control Panel Memory Select, CPSEL, is active instead of the Memory Select, MEMSEL, for memory references. The CPSEL signal may therefore be used to distinguish the Control Panel Memory from the Main Memory. However, during the Execute phase of indirectly addressed AND, TAD, ISZ or DCA instructions, the MEMSEL is made active. The instructions are always fetched from the control panel memory. The operand address for indirectly addressed AND, TAD, ISZ or DCA refers first to the control panel memory for an effective address, which, in turn, refers to a location in the main memory. A main memory location may therefore be examined and changed by indirectly addressed TAD and DCA instructions, Figure 15, respectively. Every location in the main memory is accessible to the control panel routine.

FIGURE 15



"DCA INDIRECT" IN CONTROL PANEL ROUTINE

Exiting from the control panel routine is achieved by executing the following sequence with reference made to Figure 16.

ION

JMP I 0000_8 (Loc 0000_8 in CPMEM)

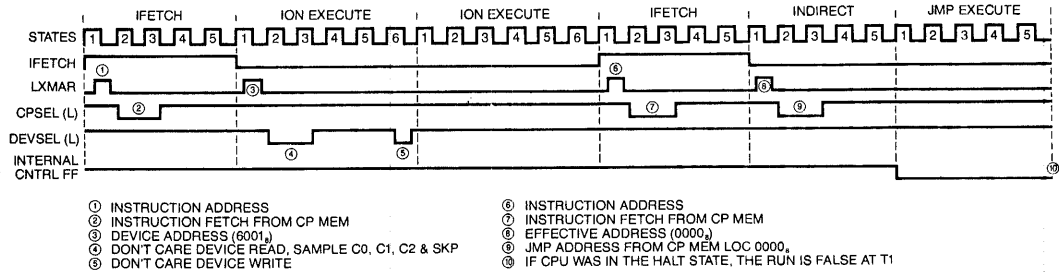
The ION, 6001_8, instruction will reset the CP FF after executing the next sequential instruction. The ION will not affect the interrupt system since the CNTRL FF is still active. Location 0000_8 of the CPMEM contains either the original return address deposited by the IM6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine, for example, by activating the LOAD ADDRESS SWITCH. CPREQ's are normally generated by the manual actuation of the control switches. If the CPU registers must be displayed in real-time, the CPREQ's must be generated by a timer at fixed intervals.

The designer may also make use of the control panel features to implement Bootstrap loaders in the CP Memory so that the loader will be "transparent" to the main memory. Programs will be loaded by DCA I POINTER instruction, the pointer being developed in the CP RAM to point to the main memory location to be loaded.

Approximately 64 P/ROM locations are sufficient to implement all the functions of the PDP8/e Control Panel. The IM6100 provides for a 12-bit switch register which can be read by the IM6100 under program control with the OR THE SWITCH REGISTER, OSR, instruction even without a control panel.

An RTF, 6005_8, instruction also resets the internal CNTRL FF. Exiting from a panel routine can be achieved by activating the RESET line since RESET has a higher priority than CPREQ as shown in Figure 18. If the RUN/HLT line is pulsed while the IM6100 is in the panel mode, it will 'remember' the pulse(s) but defer any action until the IM6100 exits from the panel mode.

FIGURE 16



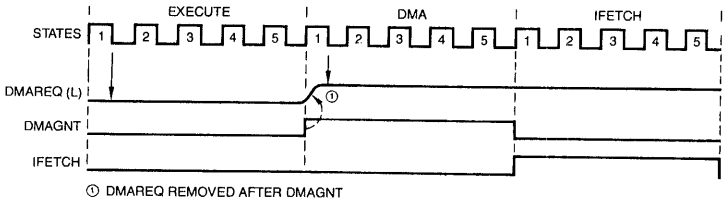
"ION; JMP I 0000_8" IN CONTROL PANEL ROUTINE

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The IM6100 is involved only in setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The IM6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction as shown in Figure 17. The IM6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XT_A, XT_B, and XT_C are active and LXMAR remains low. The device which generated the DMAREQ must provide the address and the necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive "pause" line.

FIGURE 17



DIRECT MEMORY ACCESS (DMA)

INTERNAL PRIORITY STRUCTURE

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 18. The state of the priority network decides the next sequence of the IM6100.

The request lines, RESET, CPREQ, RUN/HLT, DMAREQ and INTREQ, are sampled in the last cycle of an instruction execution, at time T1. The worst case response time of the IM6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the IM6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14μsec at 5 volts.

When the IM6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the IM6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two IM6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition on RUN/HALT should occur at least 10 clock pulses after RESET for it to be recognized.

The internal priority is RESET, CPREQ, RUN/HLT, DMAREQ, INTREQ, and IFETCH.

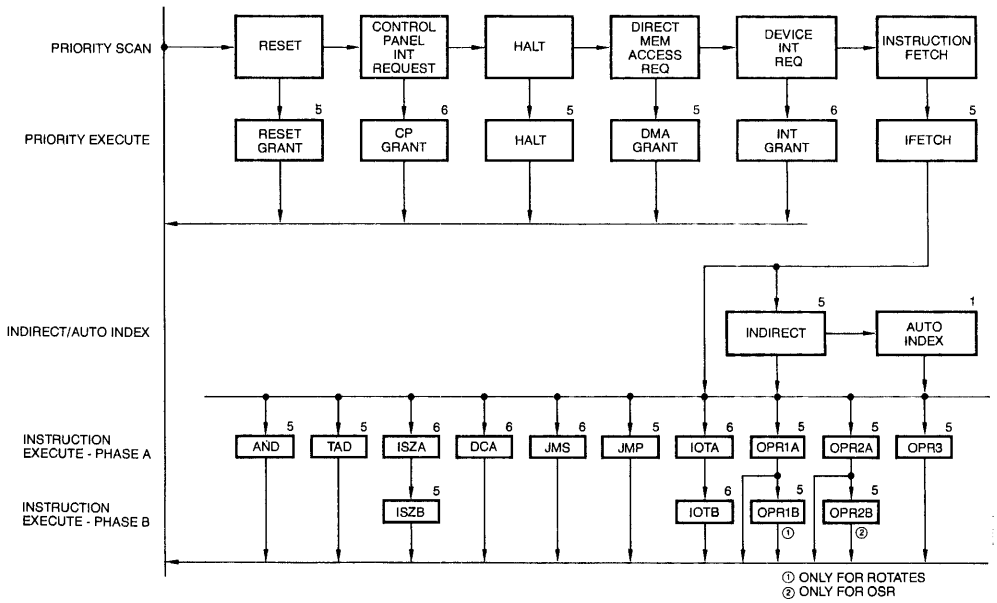
IFETCH

If no external requests are pending, the IM6100 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is active during the cycle in which the instruction is fetched. External devices can monitor DX, 0-2, during IFETCH-XT_A to determine the functional class of the current instruction. For example, the external memory extension hardware must know when JMP or JMS instructions are fetched to implement the Extended Memory Control.

The Programmable Logic Array, PLA, in the IM6100 sequences the IM6100 to execute the fetched instruction. All INDIRECT and AUTOINDEX Memory Reference Instructions go through a common state sequence to generate the Effective Address, EA, of the operand. The subsequent sequence, referred to as the EXECUTE phase, is controlled by the functional class of the instruction. The EXECUTE phase of AND, TAD, DCA, JMS, JMP and OPR Group 3 Microinstruction consists of only one cycle. ISZ and IOT has a 2-cycle EXECUTE phase. OPR Group 1 and Group 2 Microinstructions have an optional second cycle, depending on the microcoding of the OPR instructions. An IM6100 cycle consists of 5 states, T_1, T_2, T_3, T_4 and T_5, with an optional sixth state, T_6, for Output Transfers (WRITE).

The state sequence for internal (processor) and external IOT instructions are identical. The Device Address and Control bits are available in the External Address Register for internal IOT instructions. External hardware, for example Extended Memory Control, can control the C-lines for data transfers to implement Get Flags (GTF), Return Flags (RTF), and Clear All Flags (CAF) instructions. External Control of the C-lines is necessary to implement these internal IOT instructions since the flag bits may be distributed both inside and outside the IM6100.

FIGURE 18



MAJOR PROCESSOR STATES AND NUMBER OF CLOCK CYCLES IN EACH STATE

INTERNAL PRIORITY STRUCTURE CONTINUED

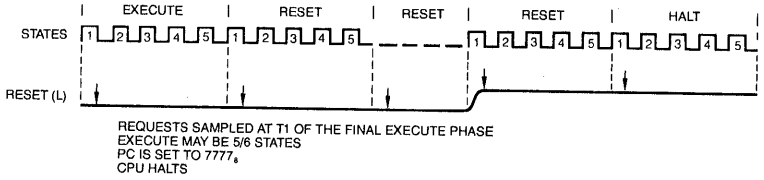
RESET

The Reset initializes all internal IM6100 flags and clears the AC and the LINK. The machine is halted.

The IM6100 remains in the Reset state as long as the Reset line is low as shown in Figure 19. The DX lines are three stated. The IM6100 continues to provide the external timing signals XT_A, XT_B and XT_C. All SEL lines are high.

The PC is set to 7777_8. In most applications, the higher memory locations utilize P/ROM's or ROM's. Therefore, a power-up routine starting at the highest memory location can be used to initialize the system.

FIGURE 19



RESET TIMING

RUN/HALT

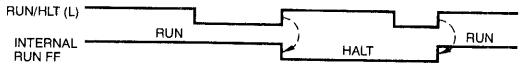
RUN/HLT changes the state of the IM6100's RUN/HLT flip-flop. Pulsing the line low causes the IM6100 to alternately run and halt as shown in Figure 20. The RUN/HLT line is normally high. The IM6100 recognizes the positive transition of the signal.

The RUN/HLT flip-flop can be put in the halt state under program control by executing the HLT, 7402_8, instruction. When the IM6100 is halted, RUN/HLT is functionally identical to the CONTINUE switch of the PDP-8/e control panel.

If the IM6100 is in the halt state, the RUN signal is low. The RUN signal can be used to power down external circuitry for a low power system.

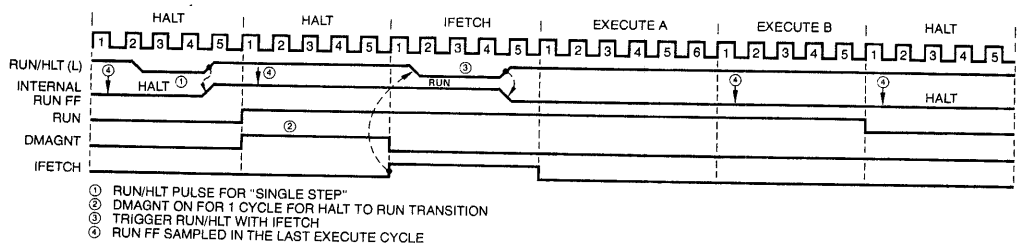
The RUN/HLT can also be used to make the IM6100 execute one instruction at a time as shown in Figure 21. The RUN/HLT combines the functional features of STOP, CONTINUE, and SINGLE INSTRUCTION as defined by the PDP-8/e Control Panel.

FIGURE 20



RUN/HALT TIMING

FIGURE 21



"SINGLE STEP" WITH RUN/HLT

WAIT

The IM6100 samples the WAIT line during input-output data transfers (Figure 22). The WAIT line, if active low, controls the transfer duration. If WAIT is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), WAIT controls the time for which the write data is maintained on the DX lines by extending the T6 state. The wait duration is an integral multiple of the oscillator time period – 250nsec at 4MHz.

The WAIT mechanism is an ideal way of providing for slower memory and peripheral devices in the system without significant degradation in system performance. For example, if one waits for all reads and writes for one delay unit (250nsec at 4MHz), the system throughput is reduced by less than 10%.

FIGURE 22

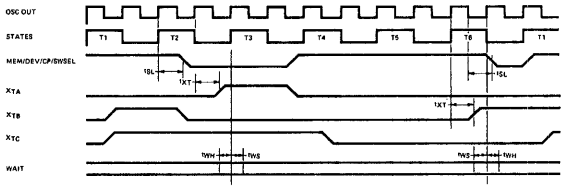
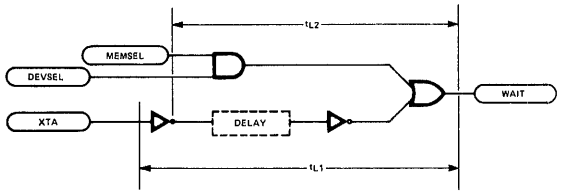


FIGURE 23



The circuit shown in Figure 23 will make the IM6100 wait during main memory and device input (READ) transfers. MEMSEL or DEVSEL, being low, will assert WAIT low. When XTA becomes active high, the WAIT line is asserted high after a delay. The wait duration is controlled by the delay in the XTA-WAIT path (t_{L1}).

The following conditions must be satisfied to obtain x units of delay during READ's:

$$t_{SL(max)} + t_{L2(max)} + t_{WS} < (x+1)\frac{T_S}{2}$$

$$t_{XT(min)} + t_{L1(min)} - t_{WH} \geqslant x\frac{T_S}{2}$$

$$t_{XT(max)} + t_{L1(max)} + t_{WS} < (x+1)\frac{T_S}{2}$$

For example, for an IM6100 I device operating at 4MHz, 5.0V and 25°C, the constraints to be met to obtain 1 unit of delay (250nsec) are as follows:

$$t_{L2(max)} < T_S - t_{SL(max)} - t_{WS}$$
$$< 500 - 300 - 30$$
$$< 170\text{nsec}$$

$$t_{L1(min)} \geqslant \frac{T_S}{2} - t_{XT(min)} + t_{WH}$$
$$\geqslant 250 - 100 + 30$$
$$\geqslant 180\text{nsec}$$

$$t_{L1(max)} < T_S - t_{XT(max)} - t_{WS}$$
$$< 500 - 250 - 30$$
$$< 220\text{nsec}$$

Note that the delay circuit can be as simple as an R-C network in conjunction with CMOS logic. Note also that the WAIT can be made selective on main memory, device, control panel memory or switch register select line.

FIGURE 24

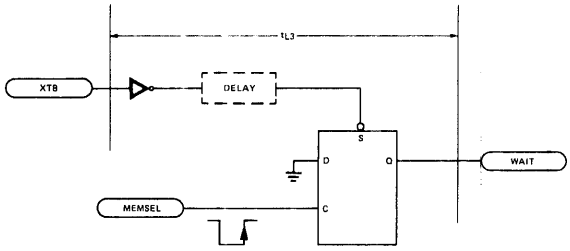


Figure 24 shows a logic implementation to wait during WRITE's only.

The rising edge of MEMSEL (or CPSEL or DEVSEL) during READ clocks in a zero on the WAIT line. XTB, after a delay, releases the WAIT line. Every WRITE pulse is preceded by a READ pulse, and if no write operation is performed in a cycle, the T6 state is not entered and the WAIT line is not sampled.

For x units of delay, the following conditions must be met:

$$t_{xT(min)} + t_{L3(min)} - t_{WH} \geqslant x\frac{T_S}{2} \text{ and}$$

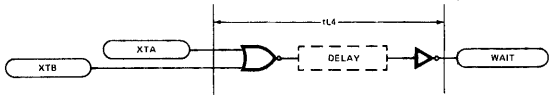
$$t_{xT(max)} + t_{L3(max)} + t_{WS} < (x+1)\frac{T_S}{2}$$

In the circuit shown in Figure 25, the WAIT signal is normally asserted low and it is released by XTA during READ's and XTB during WRITE's. Note that WAIT is active for all data transfers. Since XTA and XTB have identical timing relative to the WAIT sample point, the constraints to be satisfied are as follows:

$$t_{XT(min)} + t_{L4(min)} - t_{WH} \geqslant x\frac{T_S}{2} \text{ and}$$

$$t_{XT(max)} + t_{L4(max)} + t_{WS} < (x+1)\frac{T_S}{2}.$$

FIGURE 25

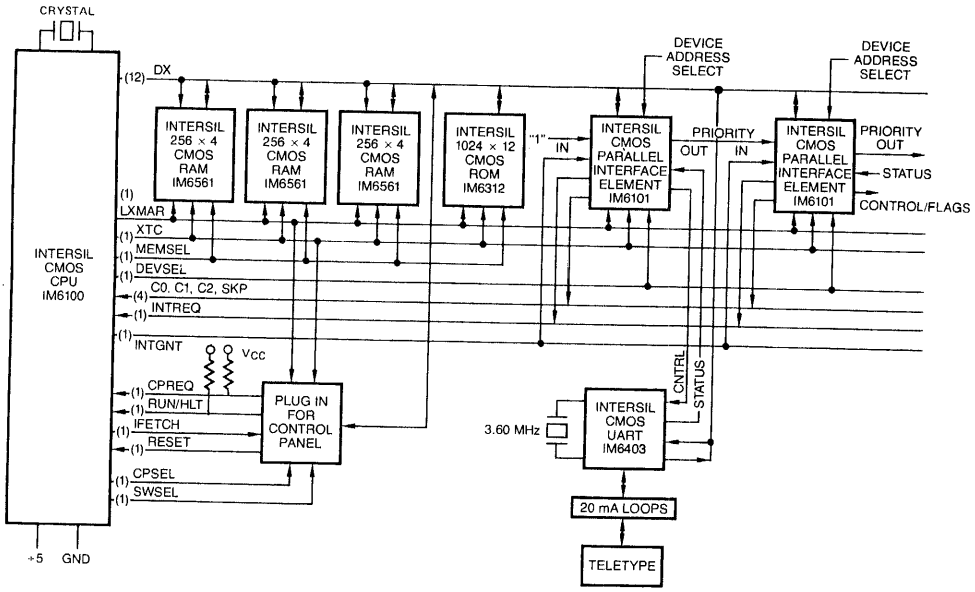


APPLICATIONS

ALL CMOS SYSTEM

The IM6100 microprocessor family provides for the capability of building an all CMOS system with no additional support components. The CMOS RAM devices are organized 256 x 1 (IM6524), 1024 x 1 (IM6508/18) or 256 x 4 (IM6551/6561). They have internal address latches and operate synchronously with an address strobe. A 1024 x 12 bit mask programmable CMOS ROM (IM6312) is also provided. The IM6402/6403 is an industry standard UART with the option of operating directly from a high frequency crystal. The IM6101, Parallel Interface Element (PIE), provides all the signals necessary to communicate with an external device including a vectored priority interrupt chain. For example, a parallel Teletype interface can be designed with only two logic elements — the IM6101 for control and the IM6403 for data handling. The dynamic power dissipation of the CMOS system will be less than 60mW at +5 volts. (Figure 26.)

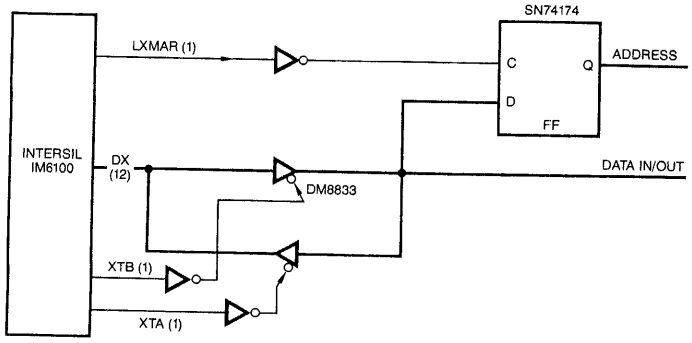
FIGURE 26



GENERAL PURPOSE IM6100 SYSTEM

A few auxiliary circuits are necessary to permit the IM6100 to be operational in a general purpose environment. They include transceivers (DM8833) to buffer the DX lines, address latches (SN74174) and buffers for control lines. The IM6100 requires only 6 additional packages to interface with standard bipolar or MOS RAM's, P/ROM's or FPLA's. (Figure 27.)

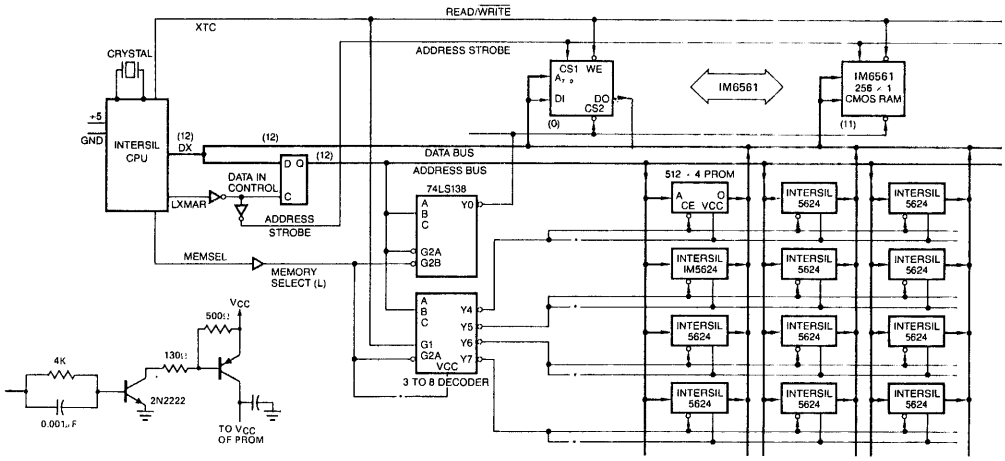
FIGURE 27



256 x 12 RAM, 2K x 12 P/ROM MEMORY SYSTEM

A low power nonvolatile memory with extremely low standby power requirements can be constructed as shown below. A 256 x 12 RAM, 2K x 12 P/ROM organization seems to be sufficient for typical microprocessor applications. Provisions are made, however, to expand the RAM-P/ROM capacity up to 4K words. The P/ROM devices are power strobed with PNP transistors. The CMOS RAM's have extremely low quiescent power requirements, less than 300μW for a 256 x 12 array, and they can be made nonvolatile with an inexpensive battery backup. The system designer can reduce memory power dissipation considerably with CMOS RAM's and power strobed P/ROM's since the memory utilization of microprocessors is typically less than 30%. The power dissipation of the system shown below is less than 0.5 watts at 5 volts. (Figure 28.)

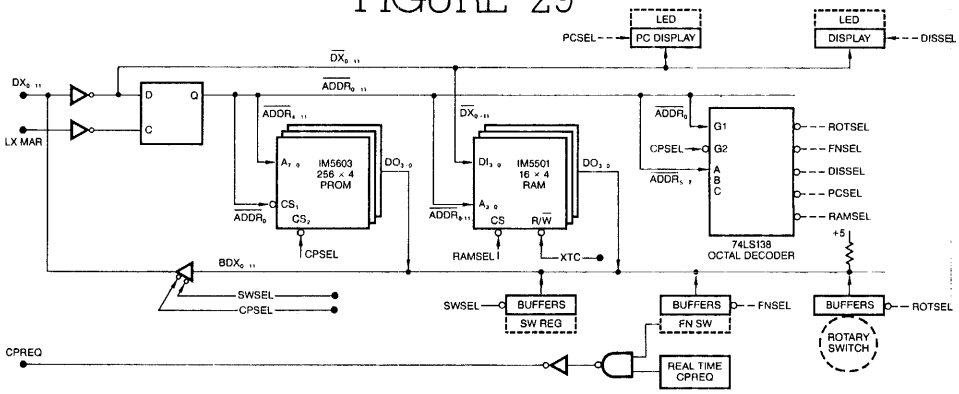
FIGURE 28



TRANSPARENT CONTROL PANEL

A unique feature of the IM6100 is the provision for a dedicated completely independent control panel with its own memory separate from the main memory. The concept of a "transparent" control panel is an important one for microprocessors since microprocessor-based production systems normally do not have a full-fledged panel and the system designer would like to use the entire capacity of the main memory for the specific system applications. A number of panel options which can greatly increase the usefulness, flexibility and reliability of the system, such as test, maintenance and diagnostic routines, bootstrap loaders, etc., can be incorporated just by increasing the size of the panel memory to handle more software. The panel can be considered as a portable device which can be plugged into a socket on the CPU board, whenever the panel functions are needed, and disconnected when not needed without disturbing any part of the user program. (Figure 29).

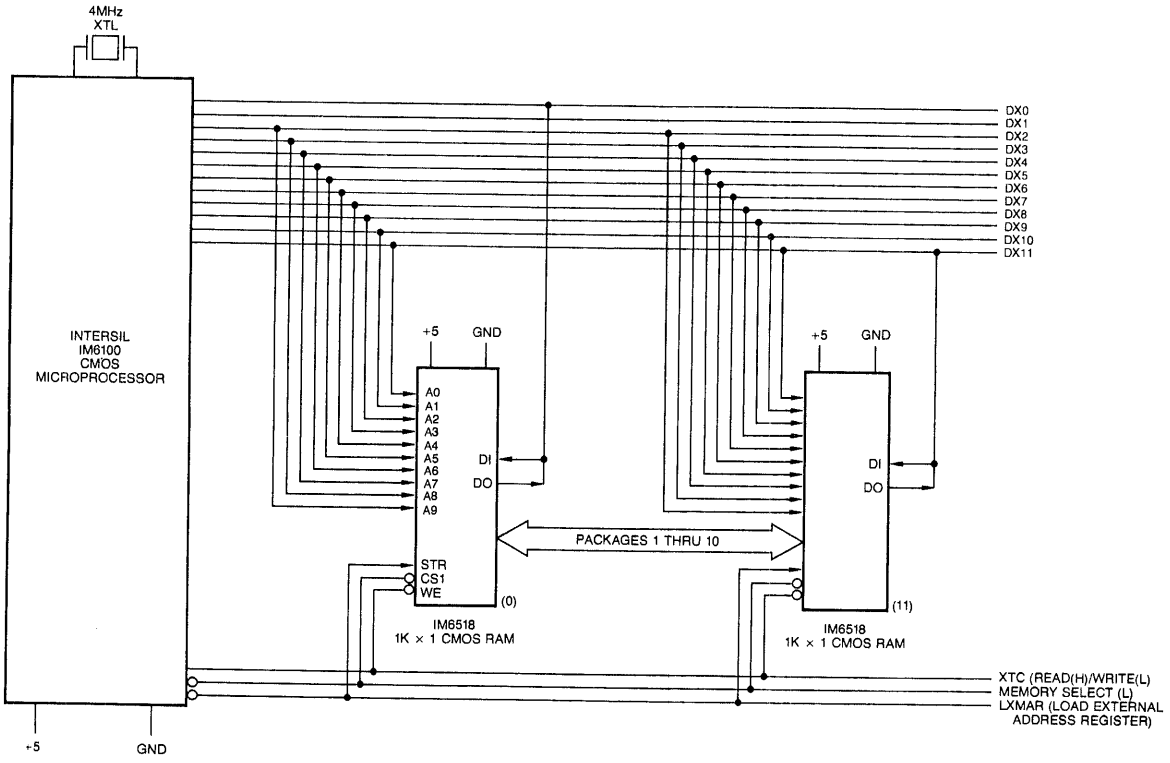
FIGURE 29



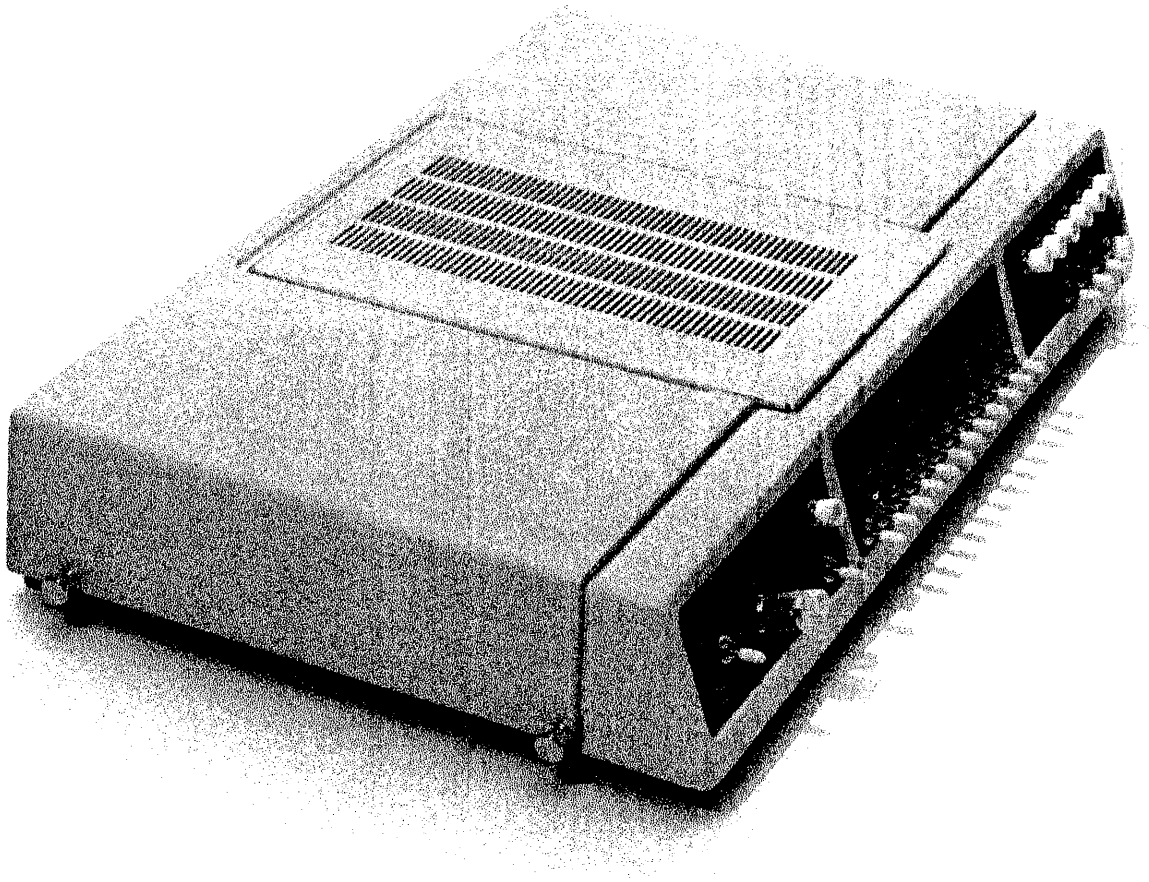
IM6100 TO CMOS RAM INTERFACE

The IM6100 provides all the control signals to interface directly with standard CMOS RAM's. Since the CMOS RAM's have internal address latches, the address information on the DX lines is latched internally with the address strobe. Address, Data-in and Data-out can be multiplexed on the DX lines without any degradation in performance. (Figure 30.)

FIGURE 30



SECTION II:
INTERCEPT
PROTOTYPING SYSTEM



INTRODUCTION

INTERCEPT provides you an easy economical means of prototyping user systems and evaluating the IM6100 family of devices in typical configurations. INTERCEPT, packaged for bench or desk top operation, is dimensioned 10-3/4" X 16-1/2" X 2-7/8" and precisely duplicates the functions and timing of the IM6100 microprocessor. The simplified bus structure, being three-state TTL compatible and fully buffered, eases I/O handling and memory operation. The basic PDP-8/E* papertape software supplied by Digital Equipment Corporation will operate properly with INTERCEPT without any software or hardware modifications. The design features of the prototyping system give the user complete flexibility in developing both software and hardware.

Standard PDP-8 programs require the IM6100 microprocessor to have a Control Panel, 6900-CONTRL, 4K words of RAM, 6901-M4KX12, and a PDP-8/E compatible Teletype interface, 6902-CPUTTY – the basic modules provided in INTERCEPT Four 72 pin-36 position edge connectors are provided on a commo bus (Figure A). The basic modules utilize three connectors and th fourth is provided as a user option. Access to the bus is availabl under the unit (Figure B) for user options or for attaching 690/ INTBUS, the Universal Bus. Two Amplimite High Density 20 ① 25 position pin and socket connectors are provided, uncommittec at the back of the case, as well as a 9 position connector for tele type interface (Figure C). A 5 volt, 3 amp power supply is provide permitting 1.0 amps for user option modules.

With INTERCEPT, the user has a fully interactive facilit to generate and test user programs and peripheral interfaces befor committing to a masked ROM pattern and a final hardware con figuration.

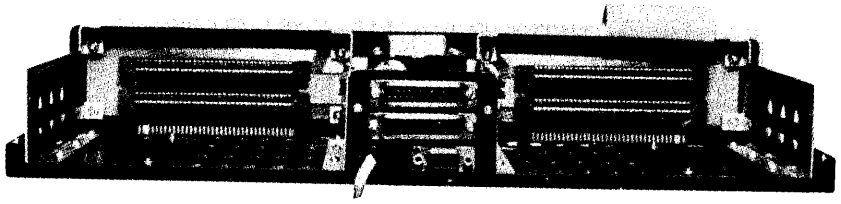


Figure A.

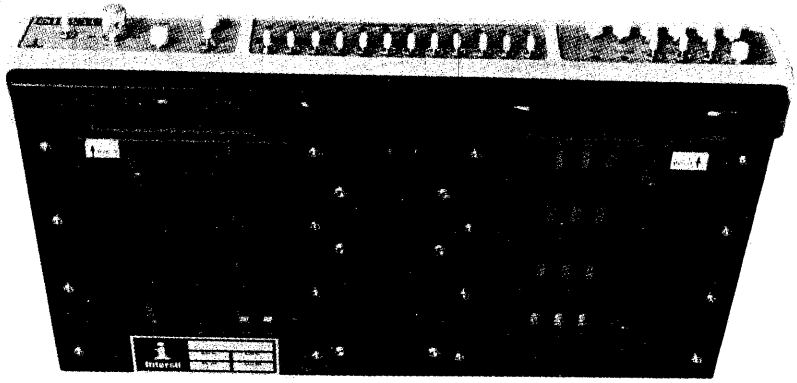


Figure B.

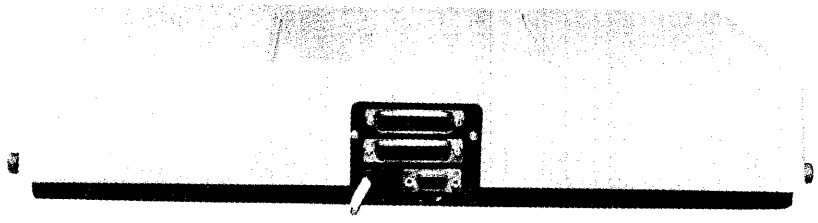


Figure C.

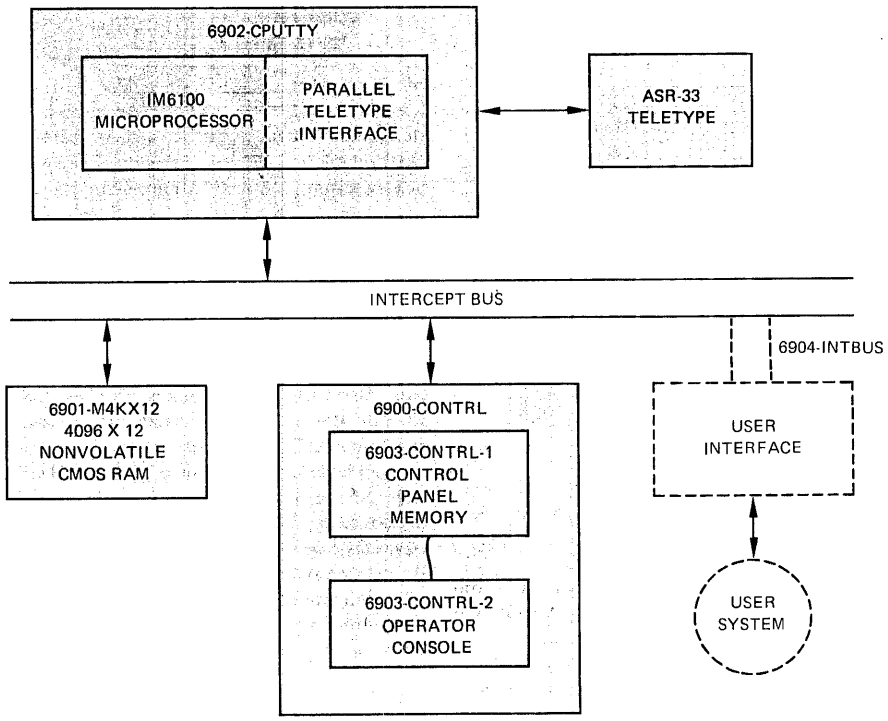
*Trademark Digital Equipment Corp.

① AMP INC., Harrisburg, PA

SPECIFICATIONS

MEMORY	6901-M4KX12	1024 x 1 CMOS Static RAM – IM6508
ORGANIZATION	6901-M4KX12	4096 x 12 – Four 1024 x 12 Arrays
NONVOLATILITY	6901-M4KX12	40 Days @ 25°C
CLOCK RATE	ALL	4 MHz
INPUT SIGNALS	ALL	TTL Compatible
OUTPUT SIGNALS	ALL	TTL Compatible
POWER REQUIRED	6900-CONTRL	900 mA @ 5 V DC
		DC Output of Power Supply
		5 ± 5% Volts
		3 Amps at 40°C
		AC Input
		105-125 or 210-250 Volts at 57-63 Hz
		45 Watts Max. at Full Load Rating
	6901-M4KX12	400 mA @ 5 V DC
	6902-CPUTTY	700 mA @ 5 V DC
DIMENSIONS	6900-CONTRL	10-3/4" x 16-1/2" x 2-7/8"
	6901-M4KX12	6" x 8-1/2" x 3/4"
	6902-CPUTTY	6" x 8-1/2" x 3/4"
CONNECTOR	ALL CARDS	72-Pin – 36 Position, 0.100" Pin-to-Pin Spacing
	6900-CONTRL	Four 72-Pin – 36 Position Sockets, 0.100" Pin-to-Pin Spacing

INTERCEPT PROTOTYPING SYSTEM



6900-CONTRL CONTROL PANEL MODULES

The 6900-CONTRL consists of all the component parts of INTERCEPT except 6901-M4KX12 and 6902-CPUTTY. 6900-CONTRL is organized in two modules: The first, 6903-CONTROL-1, is a PC board which contains logic and memory and is inserted into the 6900 bus. The second, 6903-CONTROL-2, consists of the case and front panel of INTERCEPT, which contains an array of switches and indicators to facilitate processor operation and maintenance. The logic and memory card, 6903-CONTRL-1, is connected to the control panel module, 6903-CONTRL-2, with a flat cable. The control panel module requires 900 mA at 5 V DC.

The operator may start and stop program execution, examine and modify the contents of the main memory, modify and display internal processor operation, manually load and execute machine language programs or **bootstrap** and execute programs via the Teletype or a high speed tape reader. Since th microprocessor register and internal control signals are not availabl externally, the modification and display of internal processc information must be done under program control. The consol program resides in the console memory which is organized a 16 x 12 RAM–256 x 12 P/ROM. The console operations ar completely **transparent** to the user.

Provisions are made for single instruction and single clocl processor operation. The processor state information can also b displayed in **real time.** The user defined routines are implemente with the "USER FN" switch.

Additional information on the 6900-CONTRL modul is provided in Applications Bulletin M006 entitled "IM610(Operator Console".

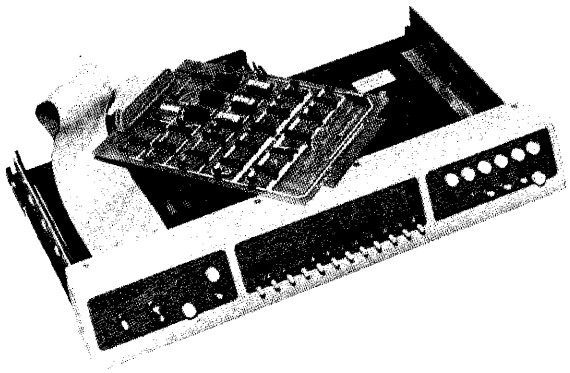


Figure D.

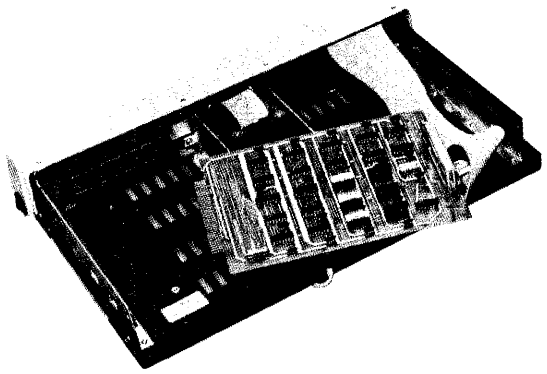


Figure E.

MODULES

6901-M4KX12 4096 X 12 NONVOLATILE CMOS MEMORY MODULE

The 4096 x 12 nonvolatile CMOS memory module consists of 48 CMOS static RAMs (IM6508), providing the user with 49152 bits of random access memory. The module provides for memory expansion by utilizing the Field Select input and is fully decoded and buffered for TTL compatibility. The 3K Write Protect provision enables the user to block the upper 3K words of memory as "read-only" to simulate RAM-ROM configurations. The entire memory may be write protected. The 500mAH Nickel Cadmium battery back-up guarantees data retention up to 40 days and is automatically recharged when the module is powered. If the battery voltage falls below the level required to guarantee data retention, even momentarily, an LED indicator illuminates when the module power is restored. A switch is provided to protect the memory module from stray signals when inserting or removing it from a "live" system. The module requires 400mA at 5 V DC and is dimensioned 6" x 8-1/2" x 3/4".

Additional information on the 6901-M4KX12 module is provided in Applications Bulletin M004 entitled "Static Memory Systems For the IM6100". A blank printed circuit board can be ordered by specifying the number 6901.

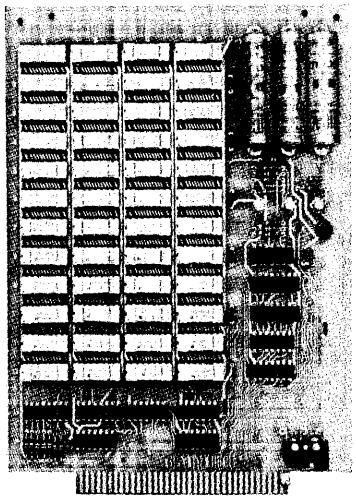


Figure F.

6902-CPUTTY IM6100/TELETYPE[1] MODULE

The 6902-CPUTTY module forms the nucleus of the three-state bus-organized prototyping system. The module contains the IM6100 microprocessor with a DEC[2] PDP-8/E compatible parallel Teletype interface. The microprocessor signals are buffered with standard high current three-state buffers and transceivers to define a TTL compatible bus.

All IM6100 signals are available externally. The input control signals have pull-up resistors to permit open collector wire-ANDing of the request lines. The memory signals are three-stated when the IM6100 grants a Direct Memory Access request permitting the peripheral device, which requested the DMA, to access memory using the same bus lines as the processor.

Since the 6902-CPUTTY module will be principally used for prototyping, provisions are made to stop the free running crystal controlled oscillator and to introduce a TTL compatible clock externally. Gating is provided to ensure integral clocking.

The module contains the required logic to transfer data between the IM6100 and an ASR-3320-3JC Teletype keyboard/reader and printer/punch. A Universal Asynchronous Receiver/Transmitter, UART, is provided for parallel-serial data formatting. In view of the fact that the interface is PDP-8/E compatible, DEC PDP-8 software will operate properly without any modification. The serial data formatting is RS-232 compatible and the interface provides for 20mA current loops. The module requires 700mA at 5 V DC and is dimensioned 6" x 8-1/2" x 3/4".

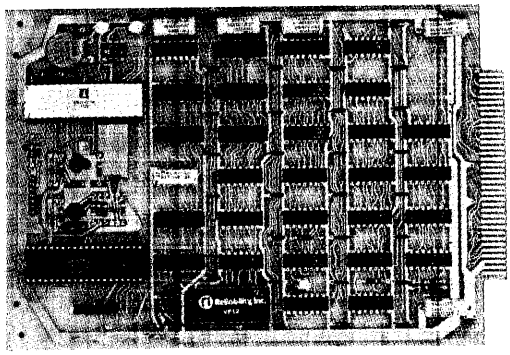


Figure G.

Additional information on the 6902-CPUTTY module is provided in Applications Bulletin M005 entitled "Teletype Interface For the IM6100 CMOS Microprocessor". A blank printed circuit board can be ordered by specifying the number 6902.

[1] Trademark – Teletype Corporation
[2] Trademark – Digital Equipment Corporation, Maynard, MA

SOFTWARE AND HARDWARE OPTIONS

The following additional hardware modules and software packages are also available from Intersil Inc.

6904-INTBUS UNIVERSAL BUS

The 6904-INTBUS shown in Figure H has a bus structure as defined in Appendix 1. The panel provides for eight 72 Pin-36 Position connectors with 1-1/4" connector to connector spacing. A 3' x 2" Flat Flexible Cable is provided to permit attaching the 6904-INTBUS to INTERCEPT for user expansion. The power supply for the 6904-INTBUS is user supplied.

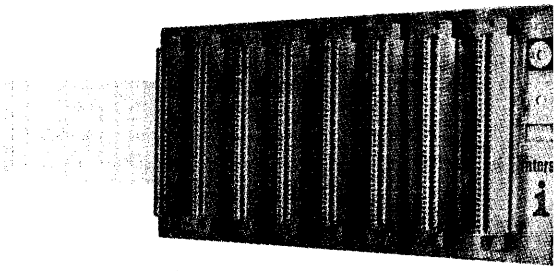


Figure H.

6905-WIREWP UNIVERSAL WIREWRAP MODULE

The Universal Wirewrap module shown in Figure I permits the user to prototype and incorporate user interfaces to the 6900 system. The module provides for all standard dual in line pin spacings.

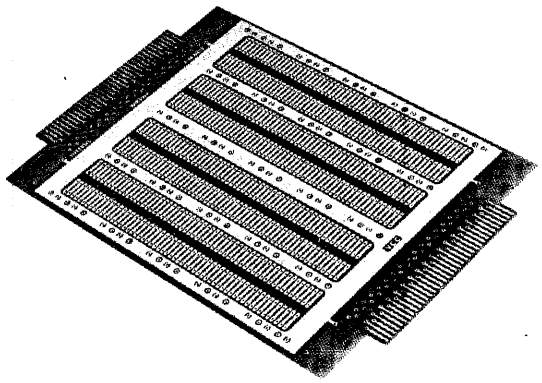


Figure I.

6906-EXTEND EXTENDER MODULE

The Extender module shown in Figure J enables the user to extend any 6900 card for servicing, testing, trouble-shooting and debugging.

6907-EMC EXTENDED MEMORY CONTROLLER MODULE

The 6907-EMC Module together with the 6904-INTBUS permits the user of INTERCEPT to expand the memory up to 32 K words.

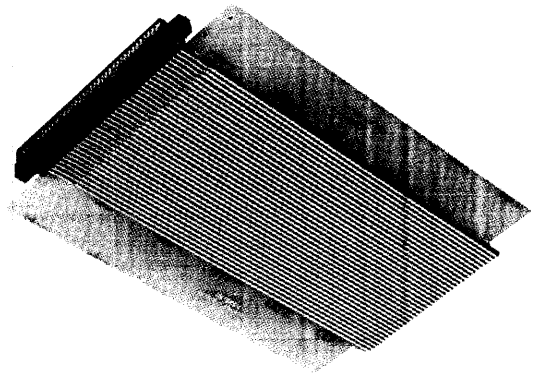


Figure J.

6909-RRELAY READER RELAY

This 2½" x 3¾" PC card provides a means for remote reader control and protection against noise induced by line surges when interfacing ASR33 to the INTERCEPT PROTOTYPING SYSTEM.

EXTENDED SOFTWARE PACKAGE 6982-QF081-AC

The basic PDP-8/E papertape software kit assists the user in creating and editing programs and in debugging and correcting programs after assembly or compilation. Additional information on the software is provided in the Applications Bulletin M003 entitled "IM6100 CMOS Microprocessor Basic Software".

PDP-8/E EXTENDED SOFTWARE KIT

DOCUMENTATION

Small computer handbook (8E, 8F, 8M)
PDP-8 pocket reference card
Introduction to programming
PDP-8 family commonly used utility routines
4K assemblers PAL III/MACRO-8
Self-starting binary loader (PDP-8E, 8M, 8F only)

BINARY PAPERTAPES

Self-starting binary loader
PAL III
DDT*
ODT (LOW)
ODT (HIGH)
Symbolic editor
RIM punch ASR 33 high memory
OCTAL memory dump
Binary punch ASR 33
PDP-8 23 BIT floating point package
RIM papertapes
Binary loader

DIAGNOSTIC SOFTWARE KIT 6985-IDIAG-1

This software package consists of programs to perform extensive tests on the processor, memory and the Teletype.

FOCAL-8* (6982-IS-LFOCA)

FOCAL-8 is an interactive algebraic language. FOCAL's desk calculator mode of operation makes the full computational power of the processor available to the user in response to simple sentence structured keyboard commands. FOCAL is similar to BASIC, ALGOL and FORTRAN in many respects. However, it is more easily learned. The dynamic combination of computational capability and simplicity makes FOCAL-8 an ideal language for on-line problem solving without having to master a complex programming language. FOCAL requires only 4K words of RAM and a Teletype. Yet, it offers a full range of mathematical functions, extendable I/O and versatile self-editing capabilities.

FOCAL-8

Document
Binary Papertape
Listing

FOCAL-8 remove/replace

Binary papertape
Listing

FOCAL-8 8K overlay (8/E)

Binary papertape
Listing

6981-FOPAL-III PAL-III FORTRAN CROSS ASSEMBLER

FOPAL-III is a cross assembler written in standard FORTRAN. The cross assembler is functionally identical to the PDP-8/E PAL-III Assembler, supplied with the Extended Software Package. It will run on any computer installation that supports FORTRAN.

*Trademark Digital Equipment Corp.

6970-IFDOS INTERCEPT FLOPPY DISC OPERATING SYSTEM

DESCRIPTION

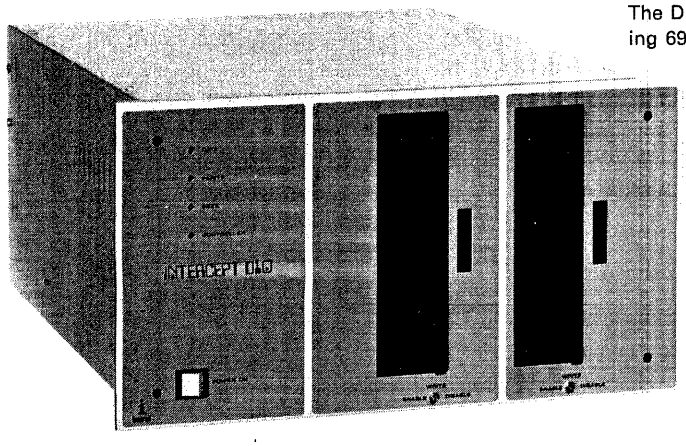
The 6970-IFDOS Floppy Disc Operating System is designed to facilitate development of software for an IM6100 microprocessor-based system. An ASCII terminal such as the ASR33 is required, as well as at least 4K words of memory (included with the INTERCEPT prototyping system).

HARDWARE

The hardware components of 6970-IFDOS consist of two completely interfaced floppy disc drive mechanisms with all electronics, power supplies, and cables necessary to add over four (4) million bits of "on line" mass storage capability to the INTERCEPT prototyping system. All components are contained in a single covered enclosure which is rack mountable or can be placed on any flat surface. The interface module is inserted directly into the INTERCEPT bus and is connected to the disc system via a multi-conductor ribbon cable.

Features:

- IBM 3740 compatible media with multiple sources
- Software compatible with DEC RX8 for the PDP-8 minicomputers
- Intelligent disc drive/controller formatter/interface communications which provide the ability to:
  - Detect, identify, and correct errors resulting from mechanical, electrical, media or human malfunction
  - Completely format a diskette within industry standards
- Automatic transparent self tests on disc related equipment are performed at times when system throughput is least affected
- Flexible Programmed Input/Output for applications that require direct communications between user programs and the storage system



SOFTWARE

Features:

- A file system which maintains a catalog of user files on flo disc and performs file handling and input/output operati as specified by user
- A keyboard monitor which provides communication betw the user and the operating system thereby enabling sim commands to enter and delete files in the user catal transfer files between memory and mass storage, print user file catalog, and call system programs
- An easy to learn text editor which allows the user to cre and modify ASCII text at the console terminal
- An extremely fast and flexible assembler which acce source programs created by the editor and produces bin output for subsequent loading and execution
- A binary loader which loads and executes assembler out files and facilitates loading of existing binary paper tapes
- An octal debugger which allows the user to examine, mo and control execution of programs from the terminal
- Numerous utility programs for absolute block copying dumping of floppy discs, system data handling, contro system parameters, and printing of system program catal

DIAGNOSTIC SOFTWARE

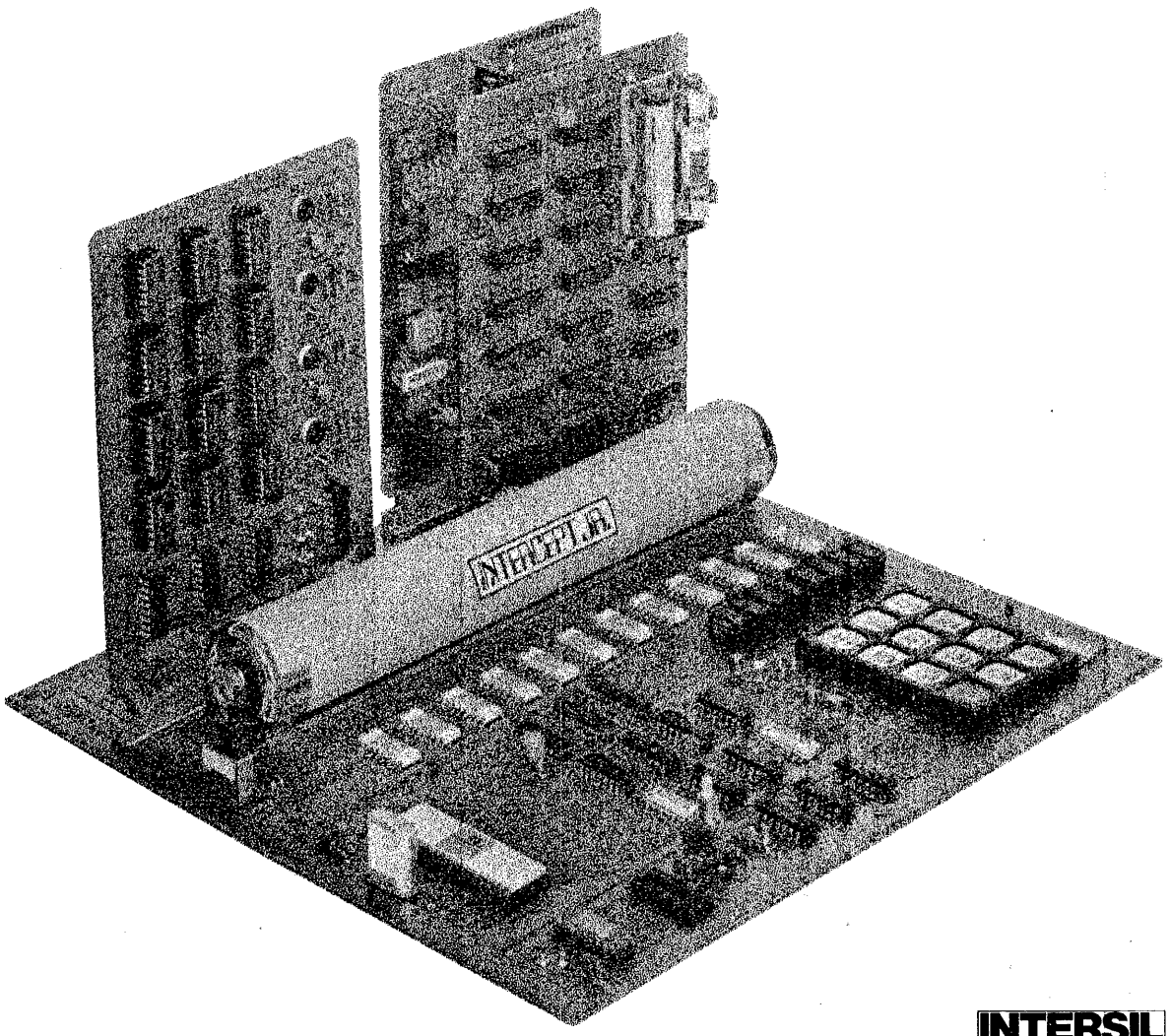
- Binary programs to test the floppy disc system and interf
- A listing of the programs

PHYSICAL SPECIFICATIONS

- DIMENSIONS Height 10.5 inches
  Width 19 inches
  Depth 22.5 inches
- WEIGHT 54 lbs
- POWER REQUIREMENTS
  110 volts @ 60 Hz or 200 volts @ 50 Hz
  2.0 Amps 1.5 Amps

The software component of 6970-IFDOS can be ordered arately by specifying order number 6980-ISOFT. The listing 6980-ISOFT can be ordered separately by specifying 6980-IL The Diagnostic Software can be ordered separately by spe ing 6985-IDIAG-3.

INTERCEPT JR.
IM6100 MICROPROCESSOR TUTORIAL SYSTEM FROM INTERSIL



INTERSIL CMOS/LSI

INTERCEPT JR.

INTRODUCTION

The INTERCEPT JR. TUTORIAL SYSTEM is ideal as a low cost educational tool for the student, hobbyist or designer.

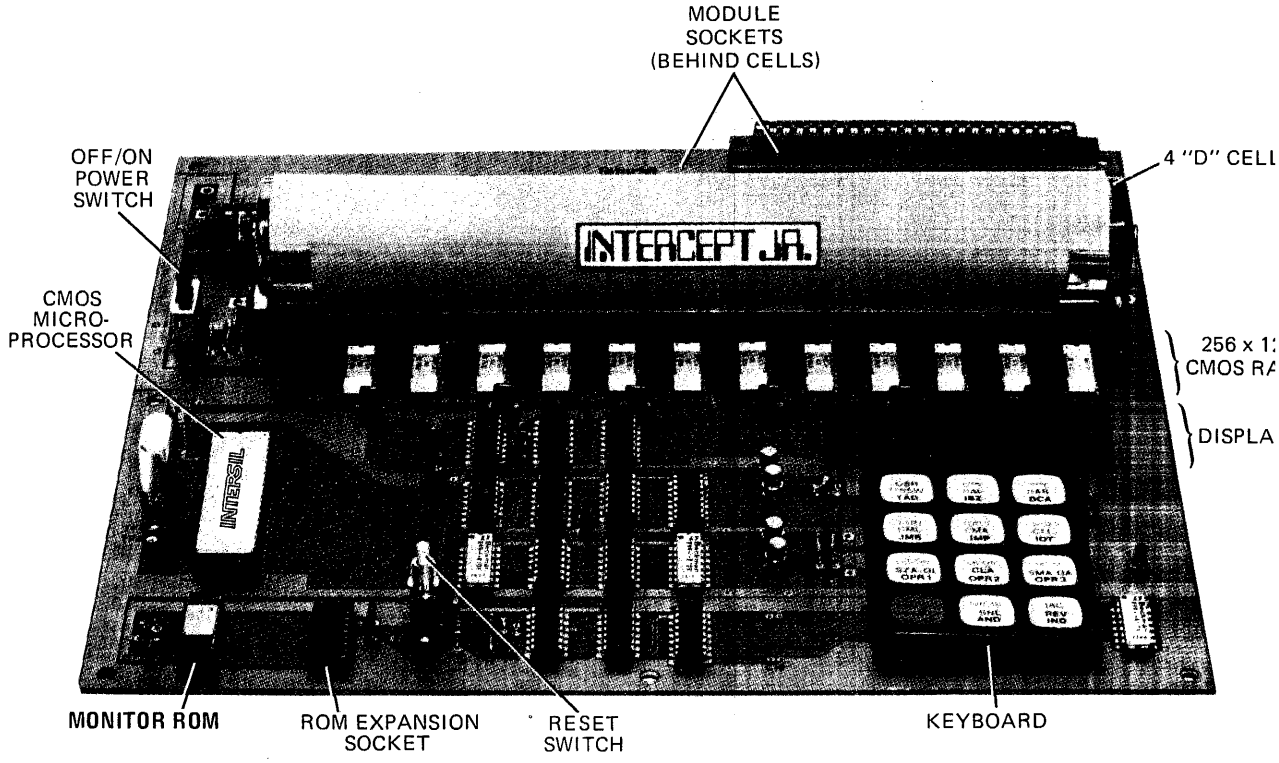
The fully assembled and factory tested system provides battery operation and a user-supplied power supply option for the evaluation of the IM6100 family of devices. The system, which recognizes the instruction set of Digital Equipment Corporation's PDP-8*, is designed with a modular concept to enable the user to purchase only those modules which meet his requirements.

A practical exposure to microprocessors, RAMs, P/ROMs and Input/Output Interfacing can be achieved with the Tutorial System and the Owner's Handbook supplied.

*Trademark-Digital Equipment Corporation, Maynard, MA.

6950-INTERCEPT JR. MODULE

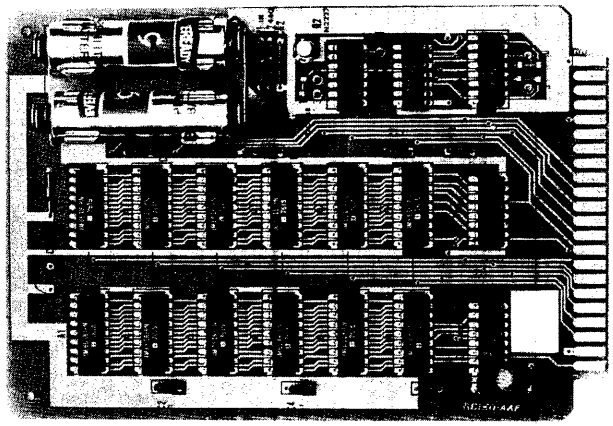
INTERCEPT JR. provides an all CMOS computer on a 10" x 11" double sided PC board. A multiple function calculator type keyboard in concert with a 1024 x 12 CMOS ROM (IM6312) monitor provides control functions, a serial bootstrap loader, a microinterpreter as well as user accessibility as a switch register via an instruction. Memory addresses and data are displayed in octal on two four-digit LED displays. The IM6100 CMOS microprocessor interfaces via a three-state bus with 256 x 12 CMOS RAM. Four D cell batteries allow for non-volatile RAM and battery operation. External terminals permit the user to provide a 5 volt or 10 volt power source. The 10 volt supply, in conjunction with changing the crystal, permits the evaluation of the Intersil high speed, or "A" version, components. A socket is provided for evaluation of a user generated CMOS ROM (IM6312/12A). Three edge connectors with 44 pins on 0.156" pin-to-pin spacing are provided for expansion to the optional boards available.



TUTORIAL SYSTEM

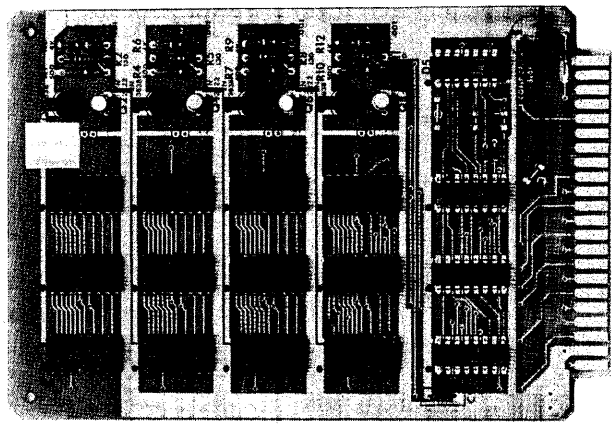
6951-M1KX12 JR. RAM MODULE

The JR. RAM MODULE, utilizing twelve (12) IM-6518 1024 x 1 CMOS RAMS on a 4½" x 6½" PC board, provides a convenient memory extension module. Non-volatility is assured by two (2) pen-light batteries which are provided.



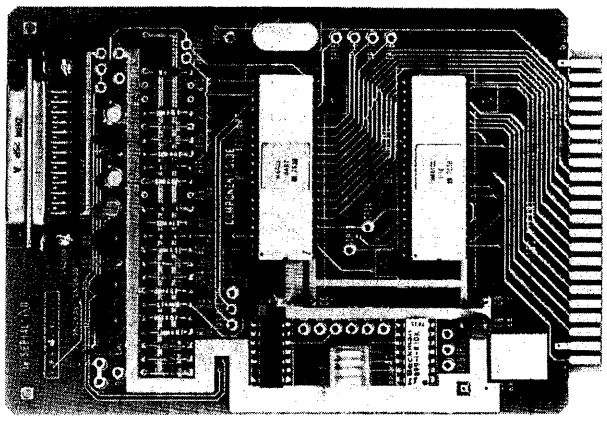
6952-P2KX12 JR. PROGRAMMABLE ROM-P/ROM MODULE

The JR. P/ROM MODULE provides the user with twelve (12) sockets organized on a 4½" x 6½" PC board. The user has the option of utilizing the IM5623, 256 x 4, or IM5624, 512 x 4 three-state-output Avalanche Induced Migration (AIM) programmable bipolar P/ROMs to obtain from 256 to 2048 words of program. Each of the four (4) rows of sockets are power strobed to permit 0.75 watts average when the P/ROMs are accessed.



6953-PIEART JR. SERIAL I/O MODULE

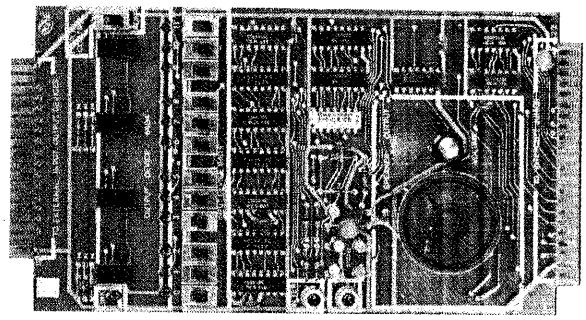
The JR. SERIAL I/O MODULE featuring the IM-6101 CMOS Parallel Interface Element (PIE) and the IM6403 CMOS Universal Asynchronous Receiver Transmitter (UART) provides the user with serial I/O capability with both RS232 and 20 mA current loop interfaces. The IM6100 controls the UART via the PIE. The CMOS ROM monitor contains a bootstrap routine for loading programs from the 6953-PIEART using BIN** formatted media.



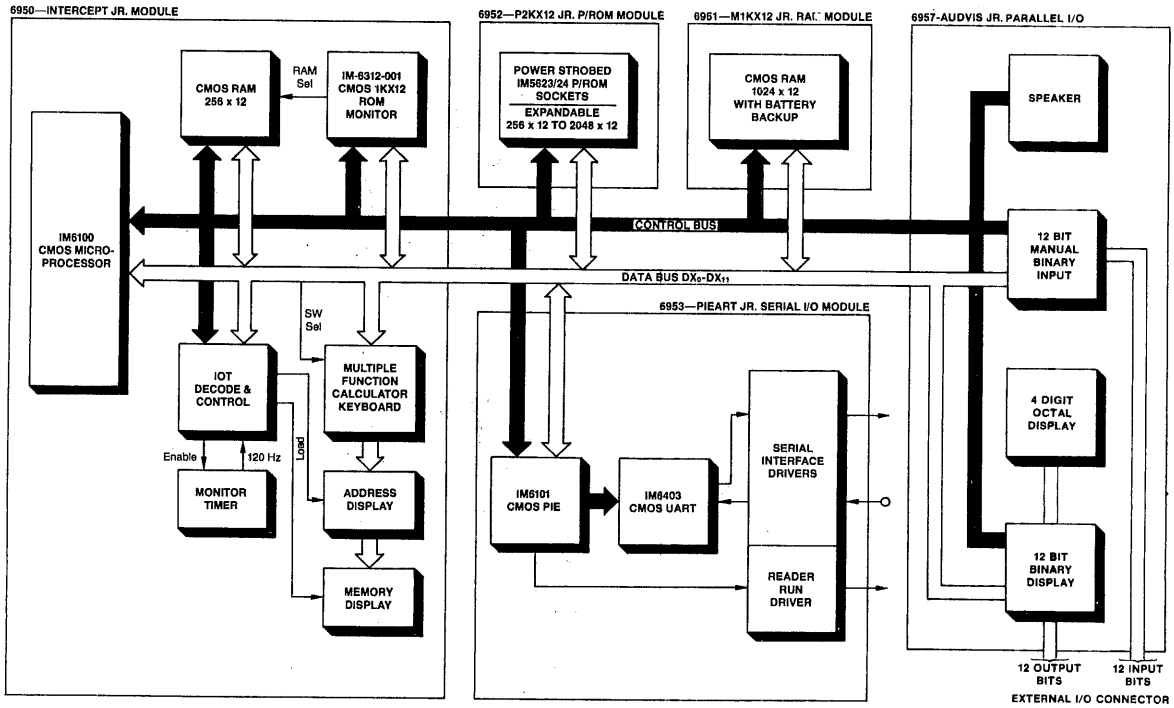
**Digital Equipment Corporation Binary Format

6957-AUDVIS
JR. AUDIO VISUAL MODULE

The JR. AUDIO VISUAL MODULE provides the user with an excellent tutorial device. A switch register, acting as an input, can be loaded into two LED display registers providing both binary and seven segment octal readout. A volume controlled speaker can be "clicked" or used to produce tones by controlling the rate at which the speaker is pulsed. A display control on-off switch is provided for power conservation.



BLOCK DIAGRAM



MICROINTERPRETER SIMPLIFIES PROGRAM ENTRY

EXAMPLE:
Add 7_{10} (0007_8) which is stored in memory location 22_{10} (0026_8), to 15_{10} (0017_8), which is stored in memory location 23_{10} (0027_8), and store the result in 21_{10} (0025_8).

PROGRAM

```
0020    CLA         /Clear Accumulator
0021    TAD 0026    /Read Location 0026
0022    TAD 0027    /Add Location 0027
0023    DCA 0025    /Deposit Result in 0025
0024    HLT         /Halt
```

KEYBOARD OPERATION AND DISPLAY

OPERATION	KEYBOARD ENTRIES (Left to Right)	DISPLAY ADDRESS	DISPLAY MEMORY
PROGRAM	CNTRL SET PC 0 0 2 0	0020	* * * *
	CNTRL MICRO OPR1 CLA	0020	7200
	CNTRL TAD 0 0 2 6	0021	1026
	CNTRL TAD 0 0 2 7	0022	1027
	CNTRL DCA 0 0 2 5	0023	3025
	CNTRL OPR2 HALT	0024	7402
EXIT FROM MICROINTERPRETER	CNTRL CNTRL		
EXECUTE PROGRAM	CNTRL SET PC 0 0 2 0	0020	7600
	CNTRL RUN	0025	0026

Answer is displayed as 0026_8 (22_{10}).

*Don't Care

SECTION III: INTERSIL DATA SHEETS

FEATURES

- IM6100 Compatible
- Low Power – typ $<5.0\mu w$ standby
- 4-11V Supplies
- High Speed
- Static Operation

PRELIMINARY CMOS PARALLEL INTERFACE ELEMENT IM6101/6101A

GENERAL DESCRIPTION

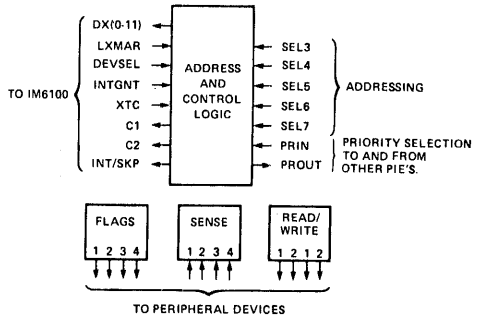
The IM6101 and IM6101A Parallel Interface Elements (PIE) are high speed low power silicon gate CMOS general purpose devices which provide addressing, interrupt and control for a variety of peripheral functions such as UARTs, FIFOs, Keyboards, etc. The PIE is designed to eliminate external logic. Data transfers between the Intersil IM6100 CMOS Microprocessor and the IM6101 are via IOT instructions, control lines and DX bus. Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. The A and B registers program write polarities, sense polarities, sense levels or edges, flag values and interrupt enables. The vector register has 10 bits writeable from the IM6100 and 2 bits indicating the highest priority SENSE input that generated the interrupt.

INSTRUCTIONS (DX 8, 9, 10, 11)

1000 - READ2	0000 - READ1
1001 - WRITE 2	0001 - WRITE1
1010 - SKIP3	0010 - SKIP1
1011 - SKIP4	0011 - SKIP2
1100 - WVR	0100 - RCRA
1101 - WCRB	0101 - WCRA
1110 - SFLAG3	0110 - SFLAG1
1111 - CFLAG3	0111 - CFLAG1

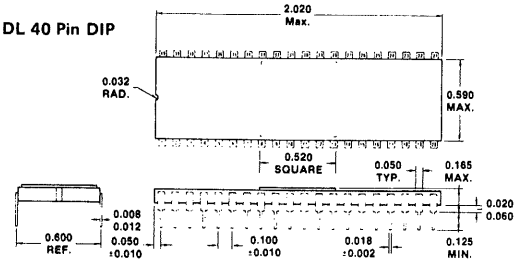
6007 - CAF (Internal IOT)
clears interrupt requests

FUNCTIONAL DIAGRAM

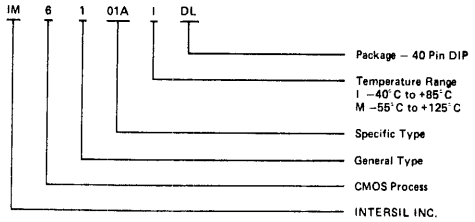


PACKAGE DIMENSIONS

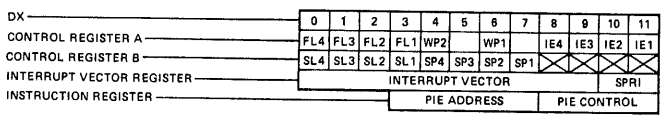
DL 40 Pin DIP



ORDERING INFORMATION



REGISTER BIT ASSIGNMENTS



FL - Flag
WP - Write Polarity
IE - Interrupt Enable
SL - Sense Level
SP - Sense Polarity
SPRI - Sense Priority

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- IM6101 +8.0V
- IM6101A +12.0V

Applied Input or Output Voltage: GND −0.3V to V_{CC} +0.3V

Storage Temperature Range: −65°C to 150°C

Operating Temperature Range
- Industrial −40°C to 85°C
- Military −55°C to 125°C

Operating Voltage Range
- IM6101 4V to 7V
- IM6101A 4V to 11V

DC CHARACTERISTICS

V_{CC} = Operating Voltage Range T_A = Temperature Range

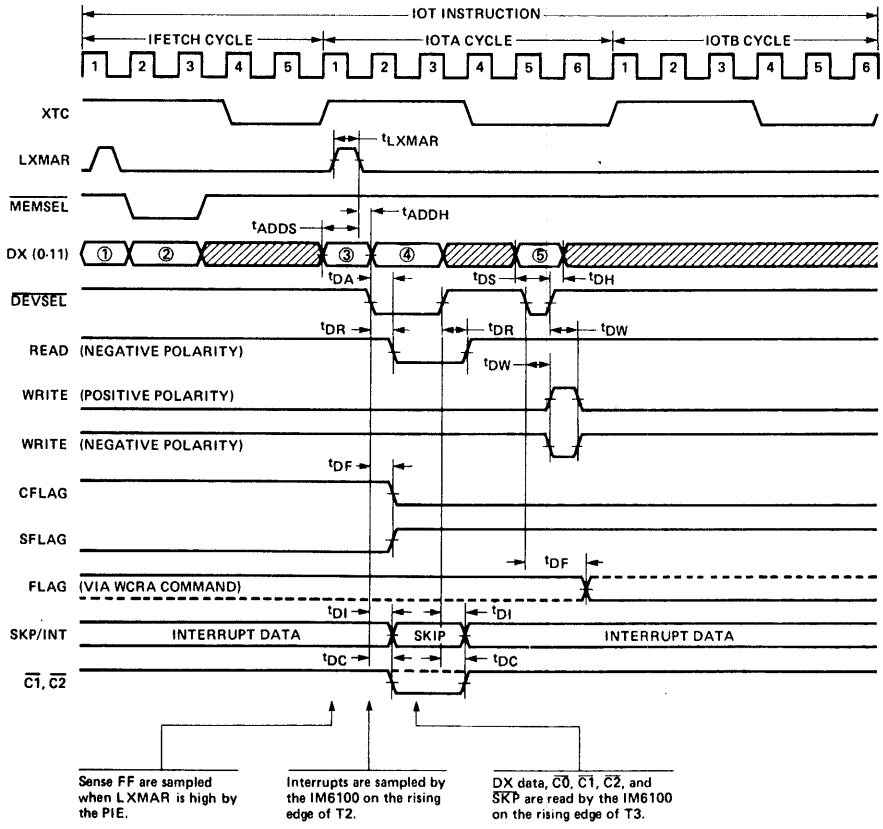
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	V_{CC} - 0.01			V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2$ mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$			GND + 0.01	V
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 2.0$ mA			0.45	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC1}	$V_{IN} = V_{CC}$		1.0		μA
	I_{CC2}	$V_{CC} = 5V$ $f_{IM6100} = 4$ MHz		1.0		mA
Input Capacitance	C_I			5	7	pf
Output Capacitance	C_O			8	10	pf
Input/Output Capacitance	C_{ID}			8	10	pf

AC CHARACTERISTICS $T_A = 25°C$ $C_L = 50$pf Derate 0.3%/°C plus 2 times V_{CC} tolerance.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Delay from DEVSEL to READ	t_{DR}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$		180 90	ns ns
Delay from DEVSEL to WRITE	t_{DW}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	100 50	180 90	ns ns
Delay from DEVSEL to FLAG	t_{DF}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$		200 100	ns ns
Delay from DEVSEL to C1, C2	t_{DC}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$		160 80	ns ns
Delay from DEVSEL to SKP/INT	t_{DI}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$		190 95	ns ns
Delay from DEVSEL to DX	t_{DA}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$		280 140	ns ns
LXMAR pulse width	t_{LXMAR}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	200 100		ns ns
Address setup time	t_{ADDS}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	50 25		ns ns
Address hold time	t_{ADDH}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	150 75		ns ns
Data setup time	t_{DS}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	100 50		ns ns
Data hold time	t_{DH}	IM6101 $V_{CC} = 5V$ IM6101A $V_{CC} = 10V$	100 50		ns ns

TIMING DIAGRAM

Timing for a typical IOT transfer is shown below. During IFETCH the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on DEVSEL while XTC is high ④ is used by the addressed PIE along with decoded control information to generate C1, C2, SKP and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on DEVSEL while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator instruction data into peripheral devices.



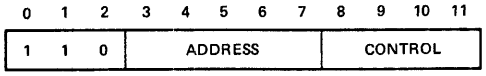
All PIE timing is generated from IM6100 signals LXMAR, DEVSEL, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the IM6100.

PIE ADDRESS AND INSTRUCTIONS

The IM6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's. Address zero is reserved for IOT's internal to the IM6100. The four control bits are decoded to select one of 16 instructions.

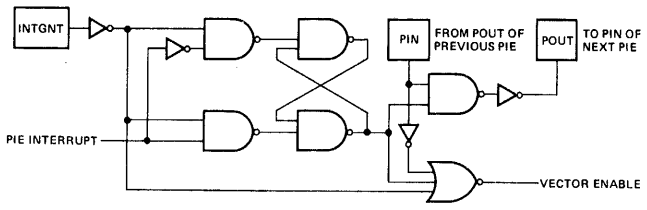
PIE INSTRUCTION FORMAT

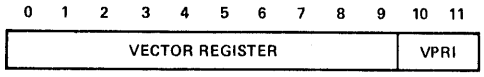


CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate data onto the DX bus to be "OR'ed" with the IM6100 accumulator data. The IM6100 accumulator is cleared prior to reading peripheral data when CO is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the IM6100 accumulator data on the DX lines into peripheral data registers. The IM6100 AC is cleared after the write operation when the CO input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the IM6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the IM6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time (4) to be "OR" transferred to the IM6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer IM6100 AC data on the DX lines during time (5) of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	IM6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

PRIORITY FOR VECTORED INTERRUPT

A hardware priority network uniquely selects a PIE to provide a vectored address. *The first IOT command of any type,* after the IM6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.





VPRI	Conditions
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

I/O CONTROL LINES (C1 and C2)

The type of input-output transfer is controlled by the selected PIE by activating the C1, C2 lines as shown below. These outputs are open drain.

C1	C2	
H	H	DEV/PIE ← AC Write
L	H	AC ← AC V DEV/PIE "OR" Read
L	L	PC ← VECTOR ADDRESS Vectored Interrupt

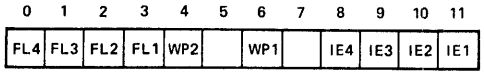
INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the IM6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of XTC. Interrupt requests are asserted by driving the INT/SKP line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data.

If the SENSE flip flop is set, the INT/SKP line is driven low to cause the IM6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the IM6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.



FL(1-4) Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1,2) A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1-4) A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B

The CRB can be written by the IM6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown below.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

SL(1-4) A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level on the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is recognized only if a sense line is set up to be edge sensitive.

SP(1-4) A high level on the SENSE POLARITY bits causes the sense flip flop to be set by a high level or positive going edge. A low level causes the sense flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE (1-4) The sense inputs are used to set the flip flops SENSE FF. Conditions for setting SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB. The SENSE FF's are sampled on the rising edge of XTC. Interrupt requests are generated when the sense flip flops are set and interrupts are enabled (SENSE FF and IE). Sense flip flops are reset on two conditions.

1. Vectored interrupt resets highest priority SENSE FF on selected PIE.
2. SKIP instruction resets corresponding SENSE FF if set.

READ (1,2) The READ outputs are activated by the read instructions and are used by peripheral devices to gate data onto the DX lines for transfer to the IM6100 (see Figure 1). READ lines are active low.

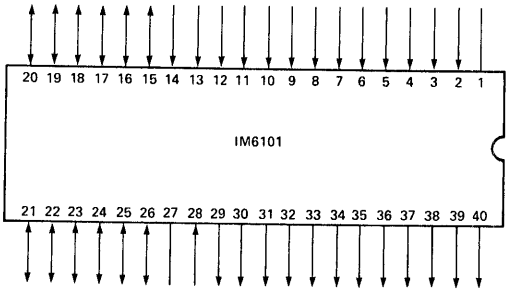
WRITE (1,2) The WRITE outputs are activated by the write instructions and are used by peripheral devices to load IM6100 AC data from the DX lines into peripheral data registers (see Figure 1). Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

FLAG (1-4) The FLAG's are general purpose outputs that can be set and cleared under program control. FLAG1 follows bit FL1 in CRA and etc. FLAG's can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		+5 volts
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 -- SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a write operation.
14	SEL 7	TRUE	See Pin 8 -- SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 -- DX 0
20	DX 5	TRUE	See Pin 15 -- DX 0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 -- DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	DEVSEL	L	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	C1	L	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cyc'e to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	C2	L	See Pin 33 – C1
35	READ1	PROG	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the IM6100. Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the IM6100 DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	PROG	See Pin 35 -- READ1
38	WRITE2	PROG	See Pin 36 -- WRITE1
39	SKP/INT	L	The PIE asserts this line low to generate interrupt requests and to signal the IM6100 when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

APPLICATION

INTRODUCTION

The IM6101, Parallel Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the IM6100 Microprocessor.

The IM6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables.

The data transfer between the IM6100 and the peripheral devices does not take place through the PIE. The Parallel Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips, UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the IM6100 until the peripheral device is ready to accept it and to latch data from the peripheral devices until the IM6100 asks for it.

INTERRUPT HANDLING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 30.5μs at 4 MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the IM6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the IM6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000_8 of the memory and the program fetches the next instruction from location 0001_8. The return address is hence available in location 0000_8. This address must be saved in a software stack if nested interrupts are allowed.

The IM6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the IM6100 when the processor executes the first IOT instruction after the INTGNT. It is recommended that the internal processor instruction, Interrupt Off (IOF - 6002_8) be used for vectoring. IOF, in this context, is a NOP since the interrupt system is automatically disabled after an interrupt grant.

The 12-bit vector address generated by the PIE consists of 10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001_8 is IOF - 6002_8, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 30.5μs interrupt acknowledge time at 4 MHz consists of 14μs (max) to recognize an interrupt request, 3μs to grant an interrupt request, 8.5μs to execute the IOF for vectoring and 5.0μs to execute a Jump instruction to a specific service routine.

PIN INSTRUCTION FORMAT

The IM6100 communicates with the PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6_8 (110) to sepcify an IOT instruction. The standard DEC* convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the DEC interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, a write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by DEC interfaces. The first three bits are, as usual, set to 6_8 to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specific pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READ1 line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address. The 6900 Prototyping System assigns bit patterns 00001 and 00010 for the PDP-8/E^T compatible Teletype interface and these two addresses also must not be used for PIEs if the 6900 System is used for prototyping.

* Digital Equipment Corporation, Maynard, MA

^{T} Registered Trademark, Digital Equipment Corporation

ASYNCHRONOUS SERIAL INTERFACE WITH PIE AND UART

The IM6402/03 Universal Asynchronous Receiver/ Transmitter is a general, purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with start, data, parity and stop bits. The data word length may be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1½ when transmitting a 5 bit code.

The IM6204/03 can be used in a wide variety of applications including interfacing modems, Teletypes[T] and remote data acquisition systems to the IM6100 microprocessor. The IM6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the IM6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/IM6100 interface is shown below. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits – a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz. The configuration shown is compatible with the DEC BIN and RIM paper tape formatting.

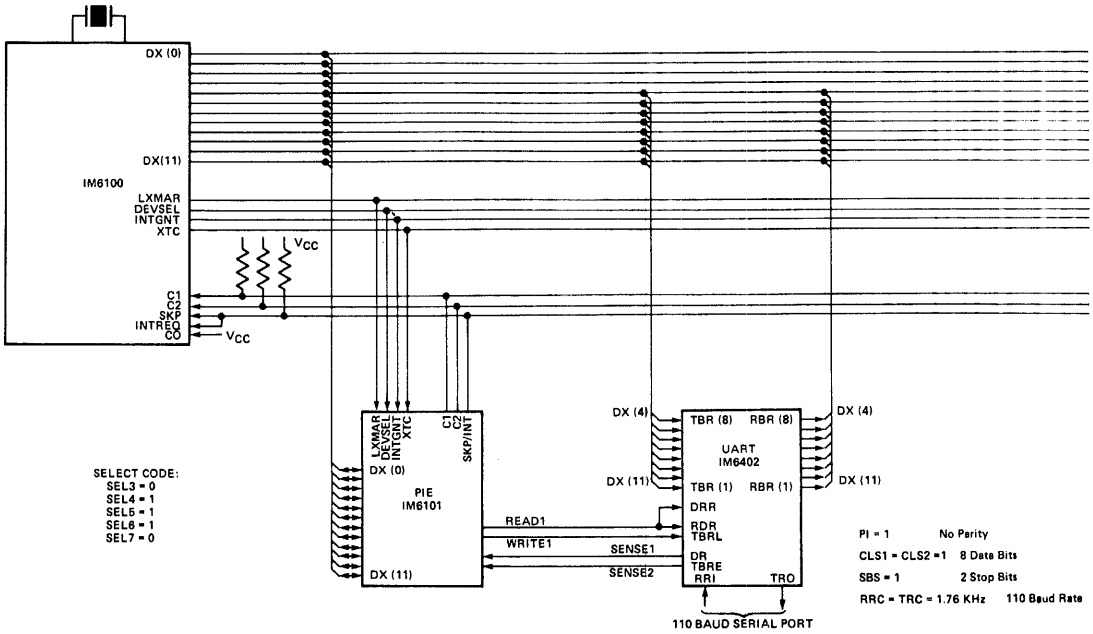
An 8-bit data word from the IM6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to one transistion. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked into the Receive Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

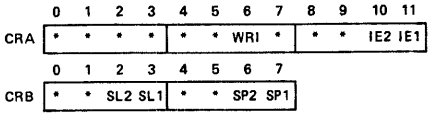
The UART interface uses only the low order 8 bits of the IM6100 data bus (DX) to receive and transmit characters.

[T] Registered trademark for Teletype Corporation

PIE/UART/IM6100 INTERFACE



PIE CONTROL REGISTER ASSIGNMENTS FOR IM6402 UART INTERFACE:



WP1 = 0 — Active low WRITE1 (TBRL)

Active low READ1

IE2 = 1 — Interrupt enable for SENSE2 (TBRE)

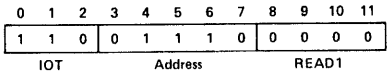
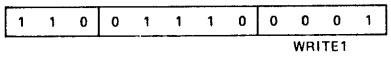
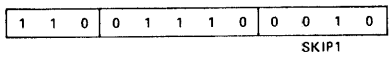
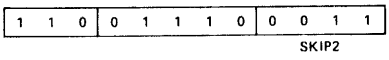
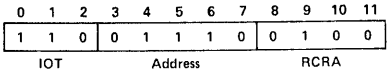
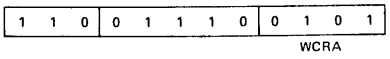
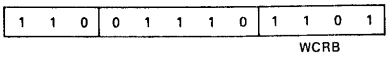
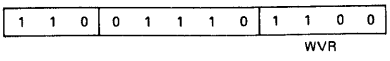
IE1 = 1 — Interrupt enable for SENSE1 (DR)

If vectored interrupts are used (PIN = 1 or is part of a priority chain) the Interrupt Vector Register must be loaded with the desired vector address.

SL2 = 0; SP2 = 1 — SENSE2 (TBRE) active on 0 to 1 transition

SL1 = 0; SP1 = 1 — SENSE1 (DR) active on 0 to 1 transition

PIE ADDRESS AND CONTROL ASSIGNMENTS:

EXTERNAL COMMANDS	OCTAL CODE	ACTION
	6340	Activate RRD low to transfer Receiver Register contents onto the DX lines and clear the Data Received Flag.
	6341	Activate TBRL low to transfer data from the DX lines to the Transmit Buffer Register.
	6342	Skip the next instruction if the internal SENSE FF1 was set by a positive transition on Data Received (DR) and then clear SENSE FF1.
	6343	Skip the next instruction if the internal SENSE FF2 was set by a positive transition on Transmit Buffer Register Empty (TBRE) and then clear Sense FF2.
INTERNAL COMMANDS		
	6344	'OR' transfer Control Register A to the AC.
	6345	Transfer AC to Control Register A
	6355	Transfer AC to Control Register B
	6354	Transfer AC (0-9) to Vector Register (0-9)

Subroutines for programmed IOT transfers:

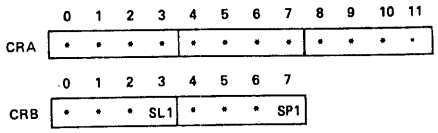
Program Listing:

```
                        /REFER TO THE APPLICATION BULLETIN M008
                         /"ROM BASED SUBROUTINE CALLS WITH THE
                         /IM6100" FOR THE IMPLEMENTATION OF A
                         /SOFTWARE STACK. THE ROUTINES IN THIS
                         /NOTE ASSUMES THAT THE SUBROUTINES ARE
                         /ARE RESIDENT IN RAM AND ARE CALLED BY
                         /THE CONVENTIONAL JMS INSTRUCTION.


                        *3200

                        /INPUT-OUTPUT ROUTINES FOR UART
                         /INPUT ROUTINE READS AN 8-BIT CHAR
                         /FROM THE UART INTO THE AC RIGHT
                         /JUSIFIED. THE OUTPUT ROUTINE XMTS
                         /A CHAR FROM THE AC TO THE UART AND
                         /THEN CLEARS THE AC.
                                /USER DEFINED MNEMONICS
                                RUART=6340      /READ UART DATA
                                WUART=6341      /WRITE UART

                                SKPDR=6342      /SKP IF DATA RECD
                               SKPTBR=6343      /SKP IF XMT RDY

3200  0000  INPUT,  0                          /ENTRY FOR SUBROUTINE
3201  6342           SKPDR
3202  5201           JMP .-1                   /WAIT FOR DATA READY

3203  7200           CLA
3204  6340           RUART                     /AC<= UART
3205  0207           AND K0377                 /STRIP 0-3
3206  5600           JMP I INPUT               /RETURN

3207  0377  K0377,  0377



3210  0000  OUTPUT, 0
3211  6343           SKPTBR
3212  5211           JMP .-1                   /WAIT FOR XMT RDY

3213  6341           WUART
3214  7200           CLA                       /WRITE UART & CLA
3215  5610           JMP I OUTPUT              /RETURN
```

TELETYPE INTERFACE WITH PIE

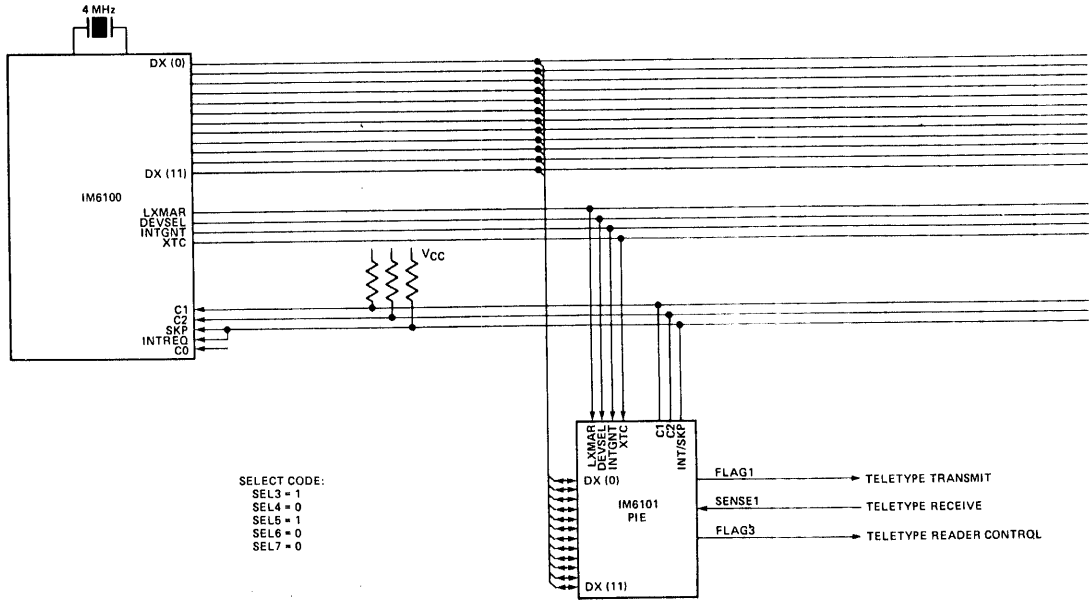
A simple economical program controlled serial interface for a Teletype can be built using only the Parallel Interface Element. The interface uses one Sense line to receive serial data, one Flag line to transmit serial data and one Flag line to control the Teletype paper tape reader, as shown below. Timing for proper transmit pulse widths, setting and clearing FLAG1, and proper receiver sampling times, testing SENSE1, is created via software timing loops.

PIE Control Register Assignments



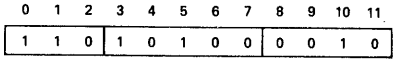
SL1 = 1; SP1 = 0 SENSE1 is level sensitive and active low.

IM6100/PIE/TELETYPE INTERFACE

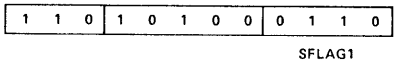


PIE Address and Control Assignments:

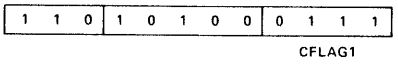
EXTERNAL COMMANDS



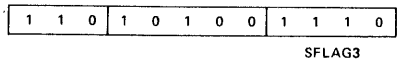
OCTAL CODE	ACTION
6502	Skip and clear if SENSE1 is low – used to detect the status of the receive line.



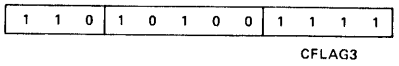
6506	Set FLAG1 to put the transmit line high ("MARK")



6507	Clear FLAG1 to put the transmit line low ("SPACE")

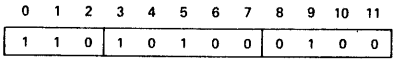


6516	Set FLAG3 to enable the paper tape reader

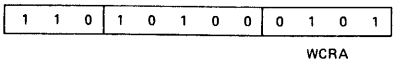


6517	Clear FLAG3 to disable the paper tape reader

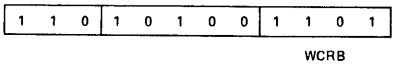
INTERNAL COMMANDS



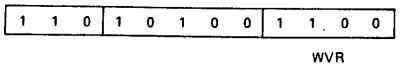
6504	'OR' transfer Control Register A to AC



6505	Transfer AC to Control Register A



6515	Transfer AC to Control Register B



6514	Transfer AC (0-9) to Vector Register (0-9)

Subroutines for programmed IOT transfers:

Transmit character routine:

The transmit routine takes an 8-bit character from the Accumulator and transmits it to the Teletype via FLAG1. FLAG1 is initially set high or "mark". For each character, the program sends out a start bit ("space" - zero), 8 data bits with the least significant bit first and 2 stop bits ("mark" - one).

Program listing:

```
                        /TELETYPE XMT ROUTINE
                         /FLAG1 IS INITIALISED TO 1(MARK)
                         /CHAR TO BE XMTED IN AC4-11
                         /NOMINAL BIT TIME 9.09 MS
                         /4MHZ OPERATION FOR IM6100
                         /AC AND L CLEARED AFTER XMT

                                /USER DEFINED MNEMONICS

                                TMARK=6506      /XMT MARK (1)
                                TSPACE=6507     /XMT SPACE(0)

                        *3000

3000  0000  XMT,       0
3001  3160              DCA TEMP1           /SAVE AC
3002  1235              TAD M8
3003  3161              DCA TEMP2           /-8 IN TEMP2
3004  1160              TAD TEMP1           /RESTORE AC

3005  6507              TSPACE              /START BIT
3006  4225              JMS DELAY           /TIME OUT BIT

                                /XMT 8 DATA BITS LSB FIRST
3007  7010  LOOP,       RAR                 /XMT BIT IN L
3010  7430              SZL
3011  5214              JMP .+3             /JMP IF 1

3012  6507              TSPACE              /XMT 0
3013  7410              SKP

3014  6506              TMARK               /XMT 1

3015  4225              JMS DELAY           /TIME OUT BIT
                                            /9.082 MS NOMINAL <.1% ERROR

3016  2161              ISZ TEMP2
3017  5207              JMP LOOP            /XMT 8 BITS

3020  6506              TMARK               /STOP BIT
3021  4225              JMS DELAY
3022  4225              JMS DELAY           /2 STOP BITS

3023  7300              CLA CLL
3024  5600              JMP I XMT           /RETURN

3025  0000  DELAY,      0000                /9.043 MS
3026  3160              DCA TEMP1           /SAVE AC
3027  1236              TAD M693
3030  3162              DCA TEMP3           /-693 IN TEMP3
3031  1160              TAD TEMP1           /RESTORE AC

3032  2162              ISZ TEMP3
3033  5232              JMP .-1             /TIME OUT LOOP
                                            /9.009 MS

3034  5625              JMP I DELAY         /RETURN

3035  7770  M8,         7770
3036  6513  M693,       6513

                        *160
0160  0000  TEMP1,      0000
0161  0000  TEMP2,      0000
0162  0000  TEMP3,      0000
```

Receiver character routine:

The receive routine accepts a serial data string from the Teletype which consists of a start bit, 8 data bits with the least significant bit first and 2 stop bits and assembles them, right justified, into an 8-bit word in the Accumulator. Each bit is sampled in the middle of the bit interval. The user can read character by character from the Teletype reader by turning the reader off after receiving each character and then reenabling it under program control to fetch the next character in sequence. The routine assumes that the program is waiting for a character from the Teletype.

Program listing:

```
                        *3100
                        /TELETYPE RECEIVE ROUTINE
                         /SENSE1 IS INITIALISED TO BE LEVEL
                              /SENSITIVE AND ACTIVE LOW
                         /AC AND L ARE CLEARED. CHAR IN AC 4-11

                              /USER DEFINED MNEMONICS

                              SKPLOW=6502      /SKP IF TTY IN IS 0
                              RDRON=6516       /ENABLE RDR
                              RDROFF=6517      /RDR OFF

3100  0000  RCVE,  0000
3101  7300        CLA CLL
3102  1235        TAD M8
3103  3161        DCA TEMP2        /-8 IN TEMP2

3104  6516        RDRON            /ENABLE RDR

3105  6502  START, SKPLOW
3106  5305        JMP .-1          /WAIT FOR START BIT

3107  1330        TAD M349
3110  3162        DCA TEMP3        /-349 IN TEMP3

3111  2162        ISZ TEMP3
3112  5311        JMP .-1          /1/2 BIT DELAY
                                   /4.532 MS

3113  6502        SKPLOW
3114  5305        JMP START        /FALSE START BIT

3115  6517        RDROFF           /GOOD START BIT
                                   /TURN OFF RDR
3116  4225  DATA,  JMS DELAY       /FULL BIT DELAY TO THE
                                   /MIDDLE OF NEXT BIT
                                   /<.15% ERROR

3117  7100        CLL
3120  6502        SKPLOW
3121  7020        CML              /L=1 IF MARK
3122  7010        RAR

3123  2161        ISZ TEMP2
3124  5316        JMP DATA         /RCVE 8 BITS

3125  7012        RTR
3126  7012        RTR              /RIGHT JUSIFY

3127  5700        JMP I RCVE       /RETURN

3130  7243  M349, 7243
```

MEMORY EXTENSION/DMA/ INTERVAL TIMER/CONTROLLER (MEDIC)

IM6102

FEATURES

DESIGN:

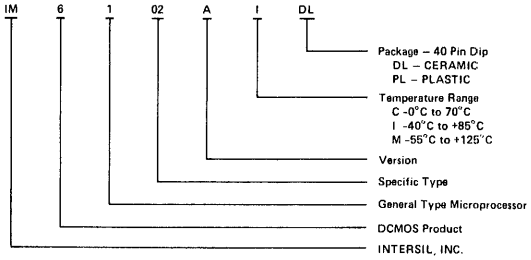
1. Silicon gate CMOS
2. Fully static 0-8 MHZ
3. Single power supply 4-11v.
4. Low power dissipation
5. TTL compatible at 5v.
6. Excellent noise immunity
7. -55°C to +125°C operation

FUNCTIONAL:

1. Interfaces directly with the IM6100 microprocessor through bidirectional DX bus and handshake lines.
2. Provides simultaneous DMA channel that uses DX bus during second half of a cycle to access memory.
3. Provides extended address capability to 32K
4. Designed to use DMA channel for refreshing dynamic memory arrays.
5. Provides real time clock programmable by the user.
6. Hardware reset.
7. Interrupt priority and vectoring.
8. Recognizes 28 different types of I/O instructions.

ORDERING INFORMATION

Circuit Marking and Product code explanation



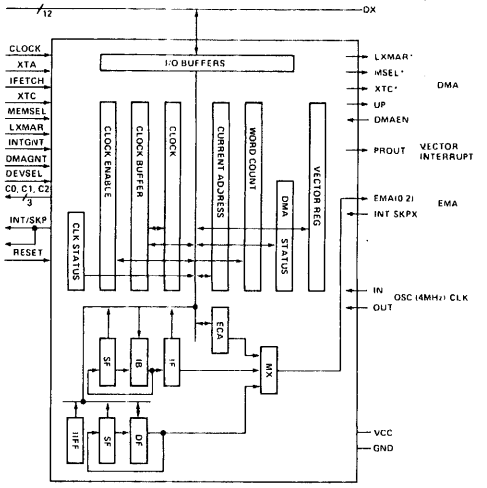
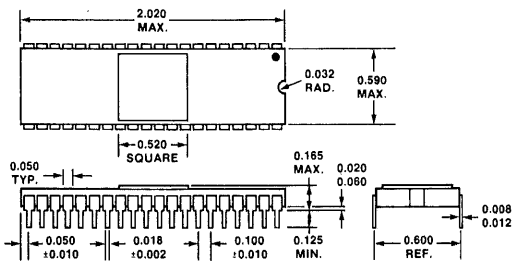


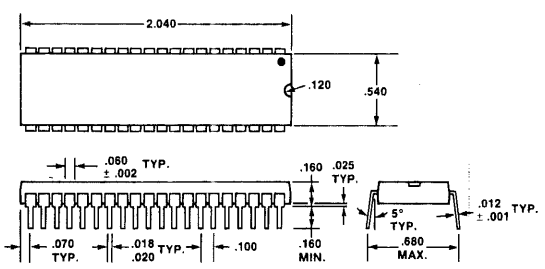
FIGURE 1: IM6102 MEMORY EXTENSION/DMA/INTERVAL TIMER CONTROLLER (MEDIC)

PACKAGE DIMENSIONS

40 Pin Ceramic Dual-In-Line Package (DL)



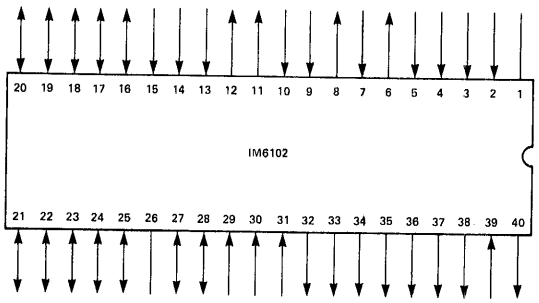
40 Pin Plastic Dual-In-Line Package (PL)



PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		Supply voltage
2	DMAEN	L	Enable the IM6102 DMA channel to transfer data
3	DMAGNT	H	CPU direct memory access grant
4	MEMSEL	L	Memory select for read or write from CPU
5	IFETCH	H	CPU flag indicating instruction fetch cycle
6	MEMSEL*	L	Memory select generated by the IM6102
7	RESET	L	Asynchronous reset will clear Instruction Field to 0_8 disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to "stop," "divide by 2^{12} mode" and "enable divide counters"
8	UP	L	User pulse (read or write)
9	XTA	H	CPU external minor cycle timing signal

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	↓	CPU signal to load external memory address register
11	LXMAR*	↓	LXMAR generated by the IM6102
12	XTC*	H	XTC generated by the IM6102
13	XTC	H	CPU external minor cycle timing signal
14	CLOCK		Oscillator OUT pulses from CPU for timing the IM6102 DMA transfers
15	SKP/INTX	L	Multiplexed SKP/INT line from lower priority devices
16	DX0	True	Most significant bit of the 12-bit multiplexed address and data I/O bus
17	DX1	True	See pin 16-DX0
18	DX2	True	See pin 16-DX0
19	DX3	True	See pin 16-DX0
20	DX4	True	See pin 16-DX0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX5	True	See pin 16-DX0
22	DX6	True	See pin 16-DX0
23	DX7	True	See pin 16-DX0
24	DX8	True	See pin 16-DX0
25	DX9	True	See pin 16-DX0
26	GND		Power supply
27	DX10	True	See pin 16-DX0
28	DX11	True	See pin 16-DX0
29	OSCIN		Crystal input for timer oscillator
30	DEVSEL	L	Device select for read or write from CPU
31	OSC OUT		See pin 29

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
32	C_0		Control lines to CPU determining type of peripheral data transfer
33	C_1		See pin 32-C_0
34	C_2		See pin 32-C_0
35	SKP/INT	L	Multiplexed SKP/INT input to the CPU
36	EMAO	H	Extended memory address field (most significant bit)
37	EMA1	H	Extended memory address field
38	EMA2	H	Extended memory address field
39	INTGNT	H	CPU interrupt grant
40	PROUT	L	Priority out for vectored interrupt

NOTE:
All DX lines are bidirectional with three-state outputs: Pins 4, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs and outputs protected with resistors and clamp diodes.

ABSOLUTE MAXIMUM RATINGS

IM6102AI
IM6102AM

Supply Voltage	12V
Input or Output Voltage applied	GND–0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	IM6102AI -40°C to +85°C
	IM6102AM -55°C to +125°C
Operating Voltage Range	4-11V

DC CHARACTERISTICS V_{CC} = 4-11V T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$ except pins 15, 29, 31	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0 except pins 32, 33, 34	V_{CC}-0.01			V
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND+0.01	V
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	-1.0		1.0	μA
Supply Current	I_{CC}	V_{CC} = 10V C_L = 50 pF; TA = 25°C F_{CLOCK} = Operating Frequency			10.0	mA
Input Capacitance	C_{IN}			7.0	8.0	pF
Output Capacitance	C_O			8.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 10.0V T_A = 25°C C_L = 50pF fc = 8MHz : T_S = 2/fc = 250 ns All times in ns

PARAMETER	SYMBOL	MIN	TYP	MAX	PARAMETER	SYMBOL	MIN	TYP	MAX
LXMAR pulse width IN	t_{LIN}	125			LXMAR* pulse width	t_{LD}		125	
XTA pulse width IN	t_{XAI}	250	75						
					DMA READ access time:				
Address setup time IN: DX-LXMAR (↓)	t_{AIS}		50		LXMAR* (↓)-UP (↑)	t_{DRAT}		250	
Address hold time IN: LXMAR (↓)-DX	t_{AIH}		50						
					DX & EMA address setup time	t_{DXAS}		200	
Data output enable time:					wrt LXMAR* (↓)	t_{EMAS}		200	
DEVSEL (↓)-DX	t_{DEN}		100						
Controls output enable time:					DX & EMA address hold time	t_{DXAH}		60	
DEVSEL (↓)-lines C0, C1, C2, S/I	t_{CEN}		50		wrt LXMAR* (↓)	t_{EMAH}		60	
Write pulse width IN	t_{DVW}		40		DMA READ enable time:				
					MEMSEL* (↓)-UP (↑)	t_{DREN}		200	
Data input setup time: DX-DEVSEL (↑)	t_{DIS}		0						
Data input hold time: DEVSEL (↑)-DX	t_{DIH}		25		UP pulse width DMA READ	t_{RUP}		125	
RESET input pulse width	t_{RST}		50		DMA WRITE access time:				
					LXMAR* (↓)-MEMSEL* (↑)	t_{DWAT}		250	
SKP/INTX to SKP/INT									
propagation delay	t_{SID}		50		DMA WRITE enable time:				
					UP (↓)-MEMSEL* (↑)	t_{DWEN}		200	
DMA control signals delay: XTC-XTC*;									
MEMSEL-MEMSEL*, LXMAR-LXMAR*	t_{DMLX}		50		MEMSEL* setup time DMA WRITE				
					MEMSEL*(↓)-LXMAR* (↓)	t_{MWS}		60	
Enable/Disable time from					DMAEN setup time w.r.t. XTA (↑)	t_{DMS}		25	
DMAGNT to EMA lines	t_{DEM}		50		DMAEN hold time w.r.t. XTA (↑)	t_{DMH}		25	
MEMSEL* pulse width - DMA READ	t_{MDR}		250		UP pulse width DMA WRITE	t_{WUP}		250	
MEMSEL* pulse width - DMA WRITE	t_{MDW}		300						
MEMSEL* pulse width -									
DMA READ/REFSH	t_{MDRR}		250						
MEMSEL* pulse width -									
DMA WRITE/REFSH	t_{MDWR}		200						

ABSOLUTE MAXIMUM RATINGS

IM6102I
IM6102M

Supply Voltage	8V
Input or Output Voltage applied	GND -0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	IM6102I -40°C to +85°C IM6102M -55°C to +125°C
Operating Voltage Range	4–7V

DC CHARACTERISTICS V_{CC} = 5.0V ± 10% T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} -2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$ except pins 15, 29, 31	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = -0.2 mA except pins 32, 33, 34	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	-1.0		1.0	μA
Supply Current	I_{CC}	V_{CC} = 5.0V			2.5	mA
		C_L = 50 pF; TA = 25°C F_{CLOCK} = Operating Frequency				
Input Capacitance	C_{IN}			7.0	8.0	pF
Output Capacitance	C_O			8.0	10.0	pF

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10% T_A = Industrial or Military C_L = 50pF fc = 4MHZ : T_S = 2/fc = 500ns All times in ns

PARAMETER	SYMBOL	MIN	TYP	MAX	PARAMETER	SYMBOL	MIN	TYP	MAX
LXMAR pulse width IN	t_{LIN}	250			LXMAR* pulse width	t_{LD}		250	
XTA pulse width IN	t_{XAI}	500	150						
					DMA READ access time:				
Address setup time IN: DX-LXMAR (↓)	t_{AIS}		100		LXMAR* (↓)-UP (↑)	t_{DRAT}		500	
Address hold time IN: LXMAR (↓)-DX	t_{AIH}		100						
					DX & EMA address setup time	t_{DXAS}		375	
Data output enable time:					wrt LXMAR* (↓)	t_{EMAS}		375	
DEVSEL (↓)-DX	t_{DEN}		200						
Controls output enable time:					DX & EMA address hold time	t_{DXAH}		125	
DEVSEL (↓)-lines C0, C1, C2, S/I	t_{CEN}		100		wrt LXMAR* (↓)	t_{EMAH}		125	
Write pulse width IN	t_{DVW}		75		DMA READ enable time:				
					MEMSEL* (↓)-UP (↑)	t_{DREN}		375	
Data input setup time: DX-DEVSEL (↑)	t_{DIS}		0						
Data input hold time: DEVSEL (↑)-DX	t_{DIH}		50		UP pulse width DMA READ	t_{RUP}		250	
RESET input pulse width	t_{RST}		100		DMA WRITE access time:				
					LXMAR* (↓)-MEMSEL* (↑)	t_{DWAT}		500	
SKP/INTX to SKP/INT									
propagation delay	t_{SID}		100		DMA WRITE enable time:				
					UP (↓)-MEMSEL* (↑)	t_{DWEN}		375	
DMA control signals delay: XTC-XTC*;									
MEMSEL-MEMSEL*, LXMAR-LXMAR*	t_{DMLX}		100		MEMSEL* setup time DMA WRITE				
					MEMSEL* (↓)-LXMAR* (↓)	t_{MWS}		125	
Enable/Disable time from									
DMAGNT to EMA lines	t_{DEM}		100		DMAEN setup time w.r.t. XTA (↑)	t_{DMS}		50	
					DMAEN hold time w.r.t. XTA (↑)	t_{DMH}		50	
MEMSEL* pulse width - DMA READ	t_{MDR}		500						
MEMSEL* pulse width - DMA WRITE	t_{MDW}		625		UP pulse width DMA WRITE	t_{WUP}		500	
MEMSEL* pulse width -									
DMA READ/REFSH	t_{MDRR}		500						
MEMSEL* pulse width -									
DMA WRITE/REFSH	t_{MDWR}		375						

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Input or Output Voltage applied	GND - 0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range Commercial	0°C to 70°C

DC CHARACTERISTICS V_{CC} = 5.0V ± 5% T_A = Commercial

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} -1.5			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$ except pins 15, 29, 31	-5.0		+5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = -0.2 mA except pins 32, 33, 34	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	-5.0		5.0	μA
Supply Current	I_{CC}	V_{CC} = 5.0V			2.5	mA
					10.0	mA
		C_L = 50 pF; TA = 25°C				
		F_{CLOCK} = Operating Frequency				
Input Capacitance	C_{IN}			7.0	8.0	pF
Output Capacitance	C_O			8.0	10.0	pF

AC CHARACTERISTICS

V_{CC} = 5.0V ± 5% T_A = Commercial C_L = 50 pF fc = 3.3MHZ; T_S = 600ns All times in ns

PARAMETER	SYMBOL	MIN	TYP	MAX	PARAMETER	SYMBOL	MIN	TYP	MAX
LXMAR pulse width IN	t_{LIN}	300			LXMAR* pulse width	t_{LD}		300	
XTA pulse width IN	t_{XAI}	600	150						
					DMA READ access time:				
Address setup time IN: DX-LXMAR (↓)	t_{AIS}		100		LXMAR* (↓)-UP (↑)	t_{DRAT}		600	
Address hold time IN: LXMAR (↓)-DX	t_{AIH}		100						
					DX & EMA address setup time	t_{DXAS}		450	
Data output enable time:					wrt LXMAR* (↓)	t_{EMAS}		450	
DEVSEL (↓)-DX	t_{DEN}		200						
Controls output enable time:					DX & EMA address hold time	t_{DXAH}		150	
DEVSEL (↓)-lines C0, C1, C2, S/I	t_{CEN}		100		wrt LXMAR* (↓)	t_{EMAH}		150	
Write pulse width IN	t_{DVW}		75		DMA READ enable time:				
					MEMSEL* (↓)-UP (↑)	t_{DREN}		450	
Data input setup time: DX-DEVSEL (↑)	t_{DIS}		0						
Data input hold time: DEVSEL (↑)-DX	t_{DIH}		50		UP pulse width DMA READ	t_{RUP}		300	
RESET input pulse width	t_{RST}		100		DMA WRITE access time:				
					LXMAR* (↓)-MEMSEL* (↑)	t_{DWAT}		600	
SKP/INTX to SKP/INT									
propagation delay	t_{SID}		100		DMA WRITE enable time:				
					UP (↓)-MEMSEL* (↑)	t_{DWEN}		450	
DMA control signals delay: XTC-XTC*;									
MEMSEL-MEMSEL*, LXMAR-					MEMSEL* setup time DMA WRITE				
LXMAR*	t_{DMLX}		100		MEMSEL*(↓)-LXMAR* (↓)	t_{MWS}		150	
					DMAEN setup time w.r.t. XTA (↑)	t_{DMS}		50	
Enable/Disable time from					DMAEN hold time w.r.t. XTA (↑)	t_{DMH}		50	
DMAGNT to EMA lines	t_{DEM}		100						
					UP pulse width DMA WRITE	t_{WUP}		600	
MEMSEL* pulse width - DMA READ	t_{MDR}		600						
MEMSEL* pulse width - DMA WRITE	t_{MDW}		750						
MEMSEL* pulse width -									
DMA READ/REFSH	t_{MDRR}		600						
MEMSEL* pulse width -									
DMA WRITE/REFSH	t_{MDWR}		450						

SDMA OPERATIONS TIMING

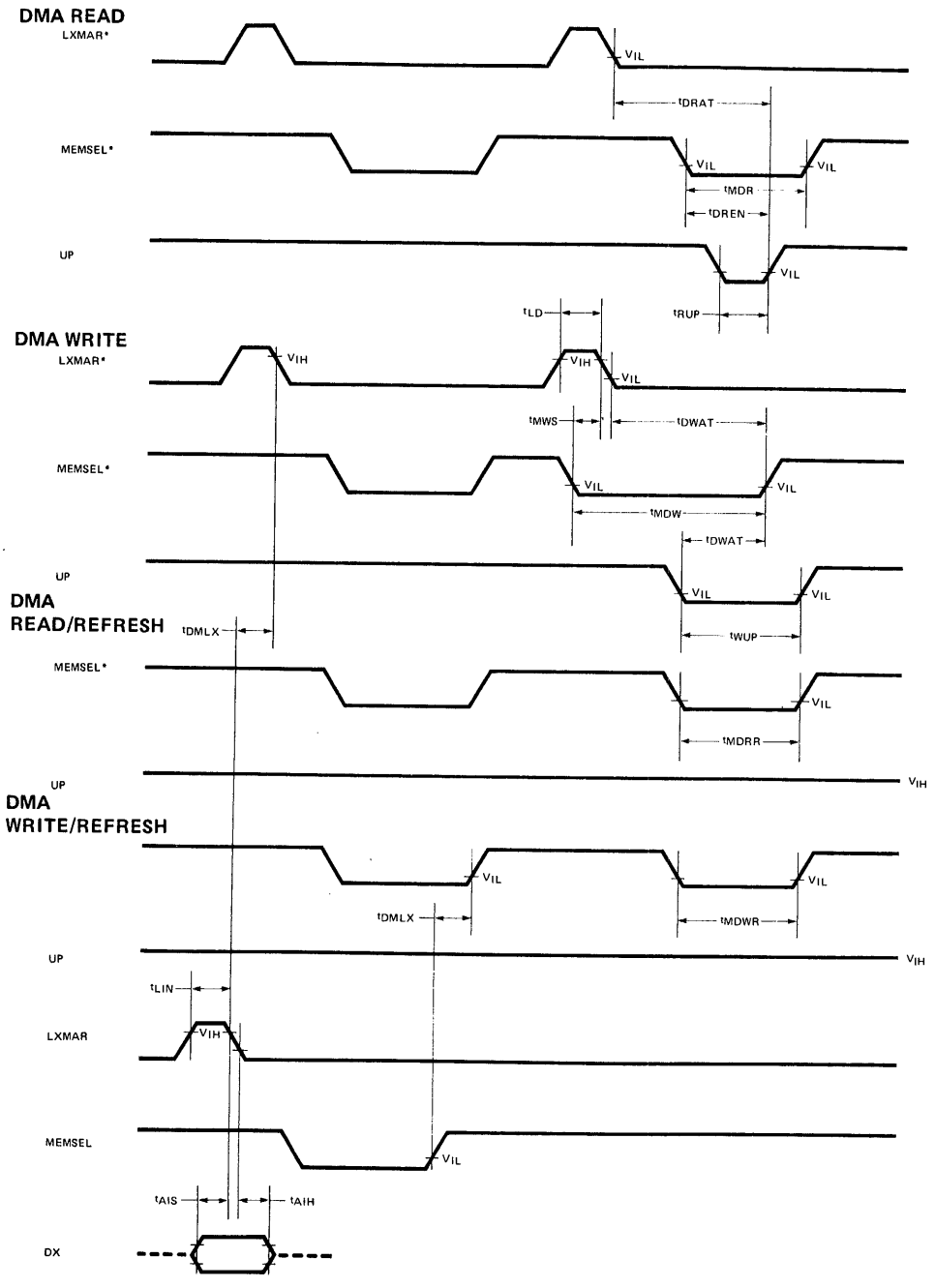


TABLE 1 SUMMARY OF IM6102 INSTRUCTIONS

MNEMONIC	OCTAL CODE	I/O CONTROL LINES			OPERATION
		C0	C1	C2	
GTF	6004	0	0	1	① Get flags, INT INH FF → AC(3), SF (0-5) → AC(6-11)
RTF	6005	1	1	1	② Return flags, AC(6-8) → IB, AC(9-11) → DF
CDF	62N1	1	1	1	Change Data Field, N → DF
CIF	62N2	1	1	1	Change IF, N → IB
CDF, CIF	62N3	1	1	1	Combination of CDF, CIF
RDF	6214	1	0	1	Read DF, DF ∨ AC(6-8) → AC(6-8)
RIF	6224	1	0	1	Read IF, IF ∨ AC(6-8) →AC(6-8)
RIB	6234	1	0	1	Read Save Field, SF ∨ AC(6-11) → AC(6-11)
RMF	6244	1	1	1	Restore Mem. Field, SF(0-2) → IB, SF(3-5) → DF
LIF	6254	1	1	1	Load IF, IB → IF
CLZE	6130	1	1	1	Clear Clock Enable Register if corresponding AC bit is set AC not changed
CLSK	6131	1	1	1	Skip on Clock Overflow Interrupt condition
CLDE	6132	1	1	1	Set Clock Enable Register if corresponding AC bit is set AC not changed
CLAB	6133	1	1	1	AC → Clock Buffer; Clock Buffer → Clock Counter; AC not changed
CLEN	6134	0	0	1	Clock Enable Register → AC
CLSA	6135	0	0	1	COF → AC(0), Clear COF Status bit
CLBA	6136	0	0	1	Clock Buffer → AC
CLCA	6137	0	0	1	Clock Counter → Clock Buffer; Clock Buffer → AC
LCAR	6205	0	1	1	AC → Current Address Register, 0 → AC
RCAR	6215	0	0	1	Current Address Register → AC
LWCR	6225	0	1	1	AC → Word Count Register, Start DMA, 0 → AC; clears word count overflow (WOF)
LEAR	62N6	1	1	1	N → Extended Current Address Register (ECA)
REAR	6235	1	0	1	Read ECA, ECA ∨ AC(6-8) → AC(6-8)
LFSR	6245	0	1	1	AC(7-11) → Status Register, 0 → AC
RFSR	6255	1	0	1	DMA Status Register ∨ AC(5-11) → AC(5-11); clears Field 7 Wraparound error (F7E)
SKOF	6265	1	1	1	Skip on Word Count Overflow
WRVR	6275	0	1	1	AC(0-10) → Vector Register, 0 → AC
CAF	6007	1	1	1	③ Clear all flags (F7E, W0F, COF) Clear clock Enable register, clock buffer

NOTES:

1. The internal flags of the IM6100 are defined as follows: LINK → AC (0), INTREQ → AC (2) and INTERRUPT ENABLE FF → AC(4).
2. When RTF is executed, the LINK is restored from AC(0) and the Interrupt System is enabled after the next sequential instruction is executed.
3. A hardware RESET clears F7E, W0F, IIFF and COF. The IF is cleared to 0_8. The DMA status register is cleared. (Read; refresh; disable F7E and W0F interrupts; no carry from CA0 to ECA2). The clock Enable register is cleared (Disable COF interrupt; disable clock buffer to clock counter transfer on COF; disable counter). Counter/buffer is cleared.

TABLE 2 SUMMARY OF IM6102 REGISTER BIT ASSIGNMENTS

	DX0	DX1	DX2	DX3	DX4	DX5	DX6	DX7	DX8	DX9	DX10	DX11
Current Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
Extended Current Address							ECA0	ECA1	ECA2			
Word Count	WC0	WC1	WC2	WC3	WC4	WC5	WC6	WC7	WC8	WC9	WC10	WC11
DMA Status (1)						SR5	SR6	SR7	SR8	SR9	SR10	SR11
Interrupt Vector (2)	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11
RIF Instruction (3)							IF0	IF1	IF2			
RTF, CIF Instruction							IB0	IB1	IB2			
GTF, RIB Instruction				IIFF(4)			SF0	SF1	SF2	SF3	SF4	SF5
CDF, RDF Instruction							DF0	DF1	DF2			
RTF Instruction										DF0	DF1	DF2
Clock Enable (5)	EN0		EN2	EN3	EN4	EN5		EN7				
Clock Buffer	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11
Clock Overflow (6)	COF											

(1) DMA STATUS

SR5 Set if Field 7 wraparound carry error — F7E; cleared by CAF, RFSR (at IOTA · $\overline{XTC}$ time), RESET } READ ONLY BITS

SR6 Set if DMA Word Counter Overflow — W0F; cleared by CAF, LWCR, RESET } READ ONLY BITS

SR7 Mode Bit 7 } ; Cleared by RESET (REFRESH MODE)

SR8 Mode Bit 8 } See below

SR9 Carry enable from CA0-11 to ECA2 if set — CE

SR10 DMA Write if set

SR11 Enable F7E or W0F interrupt if set — IE

(2) VR0-VR10 loaded from AC. VR11 is equivalent to $\overline{COF}$ (reset to '0' if interrupt caused by clock overflow)

(3) IF — Instruction Field; cleared to 0_8 by RESET AND INTGNT

(4) IIFF — Interrupt Inhibit Flip-Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by RESET and IB → IF transfer

(5) EN0 — Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by RESET, CAF

EN2 — When set causes clock buffer to be transferred to clock counter on COF. Counter runs at selected rate; COF remains set until cleared with CLSA. When cleared to 0, counter runs at selected rate, overflow occurs every 2^{12} counts and COF remains set. EN2 is cleared by RESET, CAF

EN3, EN4, EN5 — Select interval between pulses. Cleared to 000 by RESET (counter disabled), CAF See below.

EN7 — Inhibits clock counter when set. Cleared by **RESET, CAF**

(6) COF — Clock Overflow status bit; cleared by CAF, RESET and **CLSA; complement provides LSB of interrupt vector.**

SR 7, 8		EN 3, 4,5	with	4MHZ clock
00	Refresh mode; WC is frozen, no UP, DMAEN don't care	000		STOP
01	Normal mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; stop if WC overflows	001		STOP
10	Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; reverts to refresh mode if WC overflows.	010		10 ms interval
11	Stops SDMA	011		1 ms interval
		100		100 μs interval
		101		10 μs interval
		110		1 μs interval
		111		STOP

ARCHITECTURE

The IM6102 is composed of three distinct functions:

a) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

b) An extended memory address controller that augments the 12-bit addresses generated by the IM6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

c) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.

A block diagram of the IM6102 is shown in Figure 1.

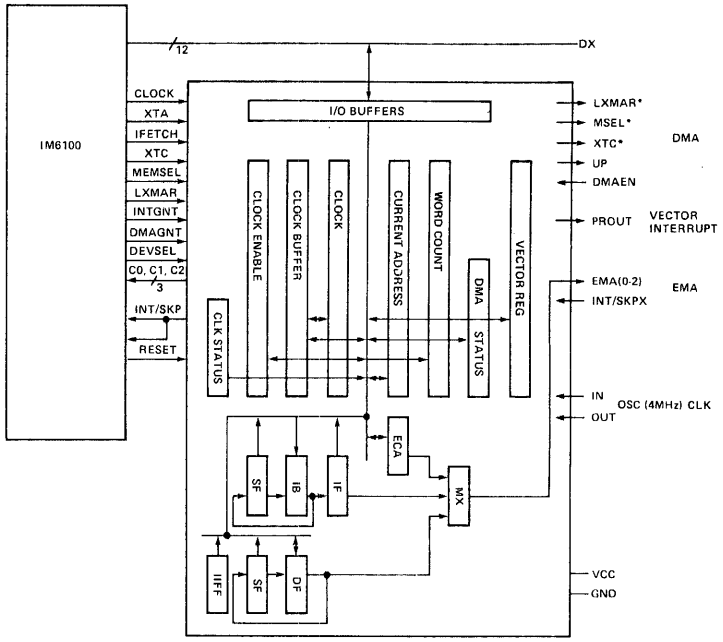


FIGURE 1: IM6102 MEMORY EXTENSION/DMA/INTERVAL TIMER CONTROLLER (MEDIC)

The IM6102 registers are summarized as follows:

A. Simultaneous DMA Channel Figure 3.

CURRENT ADDRESS (CA) REGISTER

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

EXTENDED CURRENT ADDRESS (ECA) REGISTER

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around in field 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777_8 to 0000_8.

WORD COUNT (WC) REGISTER

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers.

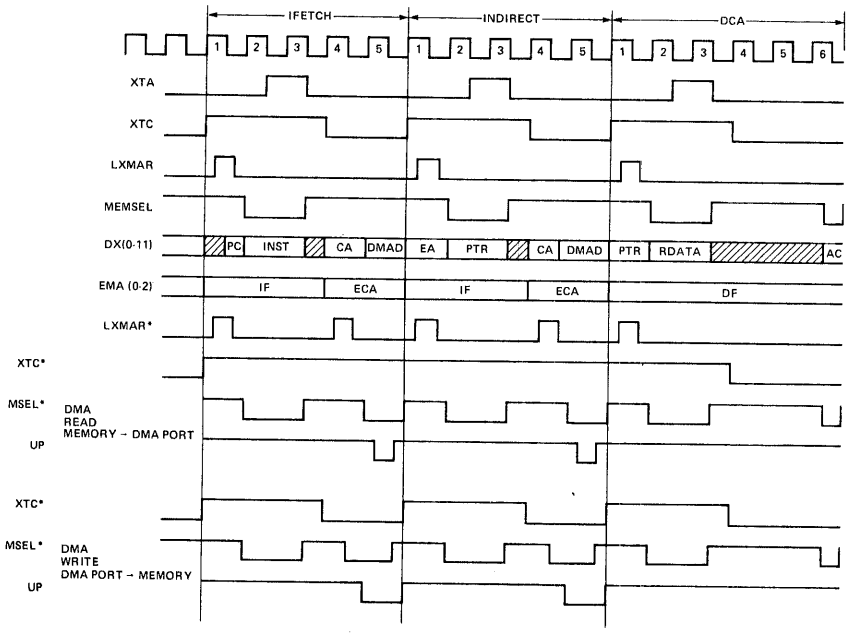


FIGURE 2: MEDIC TIMING FOR DCA I

DMA STATUS REGISTER

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description refer to the register bit assignments.

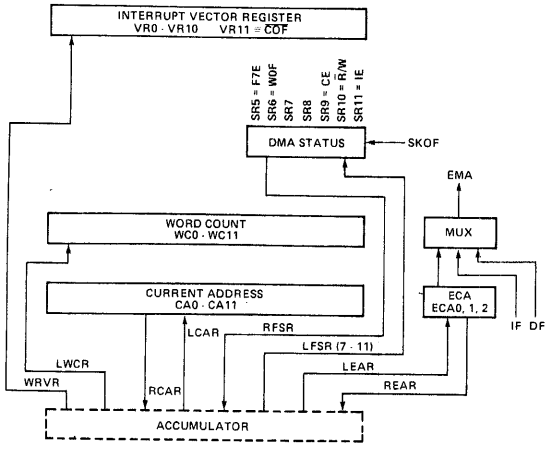


FIGURE 3: SDMA REGISTERS

OPERATION

The IM6102 SDMA channel augments the throughput of the IM6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are "stolen" from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

TABLE 3 SDMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
LCAR	6205_8	LOAD CURRENT ADDRESS REGISTER (CA) The contents of the AC replace the contents of the CA and the AC is cleared.
RCAR	6215_8	READ CURRENT ADDRESS REGISTER Description: Contents of CA transferred to AC.
LWCR	6225_8	LOAD WORD COUNT REGISTER (WC) Description: Contents of AC are transferred to the WORD COUNT REGISTER, the AC is cleared WORD COUNT OVERFLOW (WOF) is cleared and DMA operation started.
LEAR	$62N6_8$	LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA) Description: Field N of the IOT instruction is transferred to the Extended current address register.
REAR	6235_8	READ EXTENDED CA Description: Extended current address register contents OR'd into bits 6, 7, 8, of AC.
LFSR	6245_8	LOAD DMA FLAGS and STATUS REGISTER Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.
RFSR	6255_8	READ DMA FLAGS and STATUS REGISTER Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.
SKOF	6265_8	SKIP ON OVERFLOW Description: The PC is incremented by 1 if a word count register overflow condition is present causing next instruction to be skipped.
WRVR	6275_8	WRITE VECTOR REGISTER Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.
CAF	6007_8	CLEAR ALL FLAGS—clears F7E and WOF(and also COF),Clock enable and clock buffer

TABLE 4 DMA FLAGS AND STATUS REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
*	*	*	*	*	F7E	WOF	SR7	SR8	CE	$\overline{R}$/W	IE

where* – don't care for write and zero for read.

F7E Field 7 wrap around carry error; cleared by CAF, RFSR and RESET

WOF Logic one indicates word counter overflow; clear by CAF, LWCR and RESET

CE Carry enable from CA(0-11) to ECA; cleared by RESET

$\overline{R}$/W Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET

IE Enable interrupt when WC overflows or Field 7 error occurs; cleared by RESET

SR7, 8
- 00 Refresh mode; WC is frozen, no UP, DMAEN is don't care
- 01 Normal mode; DMAEN(H) freezes WC CA and no UP if WC has not overflowed; stop if WC overflows
- 10 Burst mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows
- 11 Stops DMA

DMA MODES

$SR_7 = SR_8 = 0$ REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accesses will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

$SR_7 = 0; SR_8 = 1$ NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

```
CLA      /Clear AC
TAD CA   /Get starting address
LCAR     /Load into current address register and
          clear AC
```

```
TAD SR   /Get DMA status Register Constant
LFSR     /Change status (from refresh to normal
          for example)
TAD WC   /Get two's complement of block length
LWCR     /Load word count register and start
          DMA TRANSFERS
```

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↑) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location $X0000_8$),

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS.

$SR_7 = 1; SR_8 = 0$ BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

$SR_7 = 1; SR_8 = 1$ STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.

B. EXTENDED MEMORY ADDRESS CONTROL

Figure 4 shows the EMA registers in more detail along with the register transfers caused by various instructions. The EMA function of the IM6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions for which a summary is included in Table 1.

Figure 4 shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the IM6100. A discussion of the various registers follows.

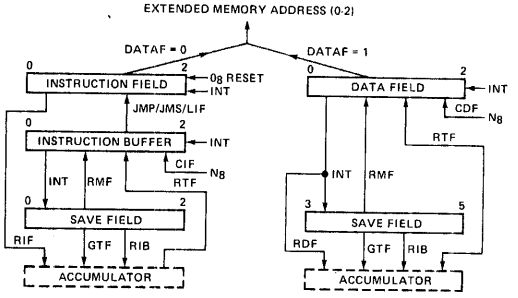


FIGURE 4: EMA REGISTERS

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension of the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777_8 to 0000_8. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0_8 and the IM6100 Program Counter is set to 7777_8 by RESET.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB

register. The transfer from IB to IF takes place at the beginning of the execute phase of the "next" JMP or JMS instruction or immediately upon execution of an LIF instruction. Using this feature, a program segment can execute an instruction to modify the IF and then "exit" the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the "next" sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IB and IF differ and also yields a method for the panel to extract or alter the status of the primary EMA registers.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the "current" Program Counter (PC) in location 0000_8 of Memory Field 0_8 and the CPU resumes operation in location 0001_8 of Memory Field 0_8. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The INTREQ (Interrupt Request) line to the IM6100 must be "gated" by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP or JMS instruction is executed. Since the actual modification of the Instruction Field takes place only after the "next" JMP/JMS, this inhibition of the INTREQ's ensures that the program sequence resumes operation in the "new" memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an INTREQ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment.

TABLE 5 EMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004_8	GET FLAGS Operation: AC (0) ← LINK AC (2) ← INTREQ Line AC (3) ← INT INHIBIT FF AC (4) ← INT ENABLE FF AC (6-11) ← SF (0-5) Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC.
RTF	6005_8	RETURN FLAGS Operation: LINK ← AC (0) IB ← AC (6-8) DF ← AC (9-11) Description: LINK is restored. All AC bits are available externally during IOTA T6 to restore other flag bits. The internal Interrupt System is enabled. However, the Interrupt Inhibit FF is made active until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF.
CDF	$62N1_8$	CHANGE DATA FIELD Operation: DF ← N_8 Description: Change DF register to N (0_8-7_8).

TABLE 5, Continued

MNEMONIC	OCTAL CODE	OPERATION
CIF	$62N2_8$	CHANGE INSTRUCTION FIELD Operation: IB ← N_8 Description: Change IB to N (0_8-7_8). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is active until the "next" JMP/JMS/LIF.
CDF, CIF	$62N3_8$	CHANGE DF, IF Operation: DF ← N_8 IB ← N_8 Description: Combination of CDF and CIF.
RDF	6214_8	READ DATA FIELD Operation: AC (6-8) ← AC (6-8) V DF Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected.
RIF	6224_8	READ INSTRUCTION FIELD Operation: AC (6-8) ← AC (6-8) V IF Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected.
RIB	6234_8	READ INTERRUPT BUFFER READ SAVE FIELD Operation: AC (6-11) ← AC (6-11) V SF Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected.
RMF	6244_8	RESTORE MEMORY FIELD Operation: IB ← SF (0-2) DF ← SF (3-5) Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routine in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is active until the next JMP/JMS/LIF.
LIF	6254_8	LOAD INSTRUCTION FIELD Operation: IF ← IB Description: Transfer IB to IF and clear the Interrupt Inhibit FF

OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF.

Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

ADDRESS MODE	IF	DF	AND, TAD, ISZ or DCA
Direct	m	n	Operand in field m
Indirect	m	n	Absolute address of operand in field m; operand in field n

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The indirect autoindex cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777_8 to 0000_8. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE
/CONTENTS OF THE DATA FIELD
        CIF 10          /CHANGE TO INSTRUCTION
                        /FIELD 1 = 6212
        JMS I SUBRP     /SUBRP = ENTRY ADDRESS
        CDF 20          /RESTORE DATA FIELD
          .
          .
          .
SUBRP,  SUBR            /POINTER
                                        FIELD 2
                                        FIELD 1
                        /CALLED SUBROUTINE,
                        /LOCATION IN FIELD 1
SUBR,   0               /RETURN ADDRESS
                        /STORED HERE
        CLA
        RDF             /READ DATA FIELD INTO AC
        TAD RETURN      /CONTENTS OF THE AC =
                        /6202 + DATA FIELD BITS
        DCA EXIT        /STORE CIF N INSTRUCTION
          .             /NOW CHANGE DATA FIELD
          .             /IF DESIRED
          .
EXIT,   0               /A CIF INSTRUCTION
        JMP I SUBR      /RETURN TO CALLING
                        /PROGRAM
RETURN, CIF             /USED TO FORM CIF N
                        /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program counter is stored in location 0000_8 of field 0_8 and program control advances to location 0001_8 of field 0_8. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed:

```
          .
          .
          .
          .
        CLA
        TAD AC          /RESTORE AC
        RMF             /LOAD IB AND DF FROM SF
        ION             /TURN ON INTERRUPT
                        /SYSTEM
        JMP I 0         /RESTORE PC WITH
                        /CONTENTS OF LOCATION
                        /0000₈ AND LOAD
                        /IF FROM IB
```

IM6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrupts from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instruction.

Users should also note that the GTF and RIB instructions read the IB register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt, which is why interrupts must be inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instruction and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

C. Programmable Real Time Clock

The IM6102 RTC function is program compatible with the DEC PDP-8/E DK8-EP Programmable Real Time Clock option.

It offers the 6100 user a number of ways to accurately measure and count intervals or events in order to implement real time data acquisition and data processing systems.

The crystal used should have the following characteristics:

$R_S \leqslant 150$ ohms

C_M = 3-30 mpF (10^{-15}F)

C_O = 10-50 pF

Static capacitance should be around 5pF; for the greatest stability, C_O should be around 12pF and the oscillator should be parallel resonant.

TABLE 6 CLOCK ENABLE REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
EN0	*	EN2	EN3	EN4	EN5	*	EN7	*	*	*	*

* Don't care for write and zero for read.

Where EN0 – When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by RESET, CAF.

EN2 – When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^{12}) counts.COF flag remains set until cleared by IOT 6135 (CLSA), CAF, RESET.

When set to a 1-counter runs at selected rate. Overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by RESET, CAF.

EN3, 4, 5 – Assuming 4 MHz crystal oscillator cleared by RESET, CAF.

Bits 3,4,5	Octal	Interval Between Pulses	Frequency
000	0	Stop	0
001	1	Stop	0
010	2	10 msec	100 Hz
011	3	1 msec	1 kHz
100	4	100 μsec	10 kHz
101	5	10 μsec	100 kHz
110	6	1 μsec	1 MHz
111	7	Stop	0

EN7 – Inhibits clock counter when set to 1 cleared by RESET, CAF

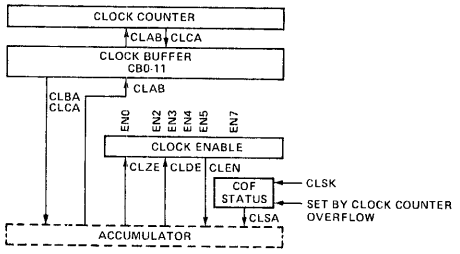


FIGURE 5 RTC REGISTERS

A discussion of the Real Time Clock registers as shown in Fig. 5 follows:

CLOCK ENABLE REGISTER

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description refer to the register bit assignments.

CLOCK BUFFER REGISTER (CB)

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

CLOCK COUNTER REGISTER (CC)

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 4 MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

TIME BASE MULTIPLEXER

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 4 MHz crystal for the clock will result in proportionately different time bases.

CLOCK OVERFLOW FLAG

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and RESET. Its complement provides LSB (VRII) of interrupt vector. If ENO of clock enable counter is set, COF can cause an interrupt request.

TABLE 7 RTC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130_8	CLEAR ENABLE REGISTER PER AC Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLSK	6131_8	SKIP ON CLOCK INTERRUPT Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped.
CLDE	6132_8	SET ENABLE REGISTER PER AC Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLAB	6133_8	TRANSFER AC TO CLOCK BUFFER Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed.
CLEN	6134_8	READ CLOCK ENABLE REGISTER Description: Causes contents of the Clock Enable Register to be transferred into the AC.
CLSA	6135_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0.
CLBA	6136_8	READ CLOCK BUFFER Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC.
CLCA	6137_8	READ CLOCK COUNTER Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC.
CAF	6007_8	CLEAR ALL FLAGS Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers.

An example illustrates how the RTC function of the IM6102 can be used as a double-precision free-running clock, using the clock counter as the low order 12 bits and a memory location as the high order 12 bits.

```
        CLA
        DCA HIGH        /Zero high order word
        TAD ENABLE      /Read enable word COF
                        /interrupt + ÷212 + rate)
        CLDE            /Set clock enable register
        ION             /Turn interrupt system on
        JMP MAIN        /Go to main program
```

The interrupt service routine with vectoring disabled, is

```
        DCA AC          /Save AC
        CLSK            /COF interrupt?
        JMP OTHERS      /No
        CLSA            /Yes, clear flag
        ISZ HIGH        /Increment high order word
        NOP             /In case HIGH overflows
        CLA             /Clear AC
        TAD AC          /Restore AC
        ION             /Turn interrupt system on
        JMP I 0000      /Return to main program
```

This can be used to keep time during program execution. Thus, even with the rate selected to be 1 μsec between pulses, an interrupt will be generated every 4095 μsec, or about every 800 instructions and the overhead required to update the clock is some 60 μsec every 4 msec (at the fastest rate, or every 40 seconds at the slowest rate).

The location HIGH is available for examination by programs that have to be stopped, started or interrupted on a real time basis.

The following example shows how the IM6102 may be programmed to function as an alarm clock, counting off a period of time, giving an alarm (that is, generating an interrupt, or executing an I/O instruction, or manipulating status bits), automatically resetting itself, and continuing. In this example, the "alarm" will go off every second.

```
START,  CLA
        TAD KM1000      /Read constant -1000₁₀
        CLAB            /Transfer AC to clock
                        /buffer, clock buffer to
                        /clock counter
        CLA             /Clear AC (note that CLAB
                        /won't clear AC)
        TAD ENABLE      /Read enable word
        CLDE            /Set clock enable register
                        /per AC
LOOP,   CLSK            /Clock overflow?
        JMP. -1
        CLSA            /Yes, clear flag
        JMS ALARM       /Alarm subroutine
        JMP LOOP
KM1000, 6030
ENABLE, 1300
```

The alarm subroutine could ring a bell, start a data converter, initiate an I/O operation, etc. By setting EN_0, this program could be modified to work in the interrupt mode, thus avoiding the waiting loop for the clock overflow.

SYSTEM CONSIDERATIONS

The IM6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its "priority-in", PRIN, input.

The IM6102 when requesting an interrupt activates the SKP/INT line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the IM6102 preclude the use of certain device addresses when the system uses IM6101 PIEs. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the IM6102. These addresses are 00101, 01000, 01001, 01010, 01011 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The IM6102 does not generate DMAREQ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMA 0, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the IM6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the IM6102 will detect the referencing of location 0000_8 by the IM6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000_8 is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the IM6102. This will not affect the generation of INTREQ so the IM6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not desirable in extended memory applications (unless device interrupts are disallowed) as the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001_8 of Memory Field 0_8).

If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the IM6102 interrupt request flip-flop is clear and POUT the priority out signal is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR11 is set and/or clock enable bit ENO is set) and an interrupting condition occurs (F7E, WOF, COF), the interrupt request flip-flop latches this condition asynchronously and the POUT signal goes low disabling interrupt requests downstream.

If the Interrupt Inhibit Flip-Flop is not set, the SKP/INT line is driven low by the interrupt request flip-flop. If the IIFF is set, the SKP/INT line stays high until the IIFF is cleared (by RESET or an IB to IF transfer) at which time SKP/INT may be driven low. Skip requests will always propagate independently of IIFF during IOTA •$\overline{\text{DEVSEL}}$• XTC.

Interrupt requests from devices downstream of the IM6102 must also be channeled via the IM6102 in order that the IIFF may condition the request timing. The IM6102 provides a built in pull-up on the SKP/INTX line coming in from devices downstream in the priority chain. At 5v, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving AC, MQ and L. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the IM6102 to place a vector address on the bus if it requested an interrupt and pull the C1 and C2 lines low, thus placing the vector in PC and forcing a branch to the service routine. If the C2 line is left unconnected, the vector address will not be forced into the PC, but will be loaded into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overflow or a field 7 wraparound error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the SKP/INT line to go low during IOTA • XTC time if the flag being tested is set. At all other times, the SKP/INT line carries interrupt requests as modified by the IM6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an autoindexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a JMP• loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the MEMSEL* signal narrows when the mode changes from write to refresh (burst mode). In such systems, RESET signals may need to be limited in duration to prevent loss of memory data.

The accuracy of the clock counter in the programmable real time clock section of the IM6102 is as follows:

CASE 1: Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is +½ count ±½ count that is, from +0 to -1 count.

CASE 2: CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator. However, the loading operation takes 1 μsec, so when 1 μsec count intervals are selected, the counter should be loaded with the two's complement of the actual count desired less one.

IM6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the IM6102 functions. All unlisted pins must be used when implementing any of the three basic features.

PIN NUMBER	PIN NAME	RTC ONLY	SDMA ONLY	EMC ONLY	EMC & DYNAMIC REFRESH
2	DMAEN	GND	USED	GND	GND
3	DMAGNT	USED	USED	USED	USED
6	MEMSEL*	N/C	USED	N/C	USED
8	UP	N/C	USED	N/C	N/C
11	LXMAR*	N/C	USED	N/C	USED
12	XTC*	N/C	USED	N/C	USED
15	SKP/INTX	VCC	VCC	USED	USED
29	OSCIN	USED	GND	GND	GND
31	OSC OUT	USED	N/C	N/C	N/C
34	C2	USED	USED	N/C	N/C
36	EMAO	N/C	N/C	USED	USED
37	EMA 1	N/C	N/C	USED	USED
38	EMA 2	N/C	N/C	USED	USED
40	PROUT	USED	USED	N/C	N/C

FEATURES

- IM6100 Compatible
- Low Power - typ. 5.0μW Standby
- 4-11V V_{CC} Operation
- High Speed
- Static Operation

CMOS ROM
1024 WORD × 12 BIT
IM6312/IM6312A

GENERAL DESCRIPTION

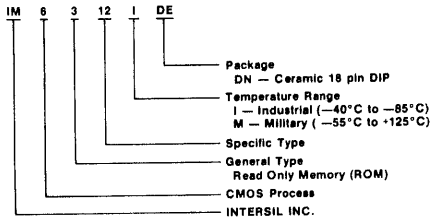
The IM6312 and IM6312A are high speed lower power silicon gate CMOS static ROMs organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4-7 volts with a typical 5 volt 25 °C access time of 250 ns. Higher operating voltages, 4-11 volts, are available with the A version. Signal polarities and functions are specified for interfacing with the IM6100 microprocessor.

OPERATION

Addresses and data out are multiplexed on 12 lines, DXO-DX11. Addresses are loaded into an on chip register by the falling edge of STR. Data out, corresponding to the latched address, is enabled when STR and OEL are low and OEH is high and the decoded state of DX0 and DX1 are true. The RSEL output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2, and DX3. This output eiminates a four bit register and decoder for the high order address bits to select RAM.

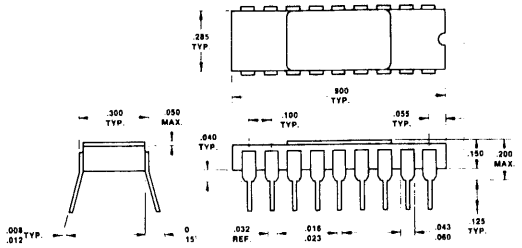
ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION



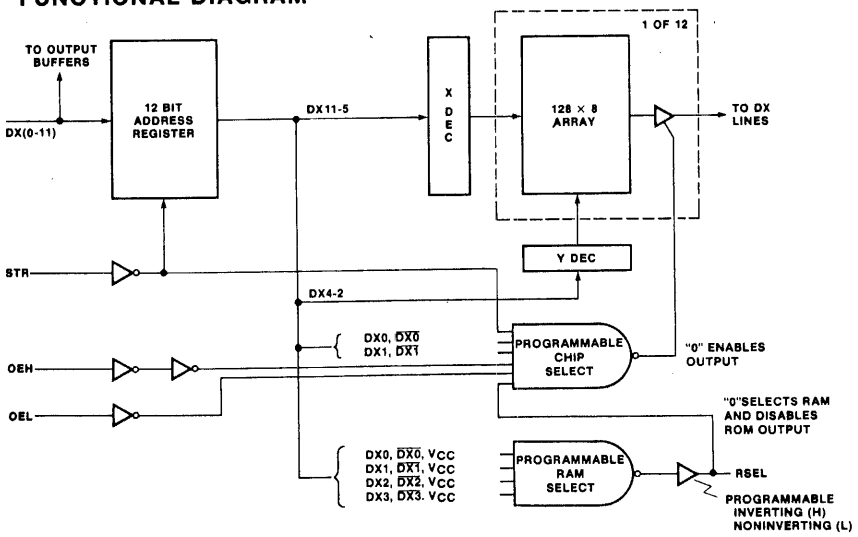
PACKAGE DIMENSIONS

18 LEAD CERAMIC DIP

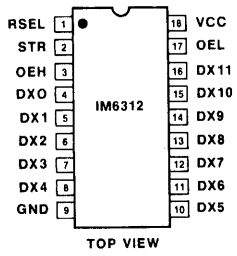


NOTE: Board drilling dimensions will equal standard practice for .020 diameter lead.

FUNCTIONAL DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

Pin 1 is designated either by a dot or a notch.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage IM6312	+8.0V
Supply Voltage IM6312A	+12.0V
Applied Input or Output Voltage	GND −0.3V to V_{CC} to .3V
Operating Temperature Range	
Industrial IM6312/12AI	−40° to 85°C
Military IM6312/12AM	−55° to 125°C

DC CHARACTERISTICS

IM6312 V_{CC} =4-7 volts, IM6312A V_{CC} =4-11 volts T_A = Temperature Range

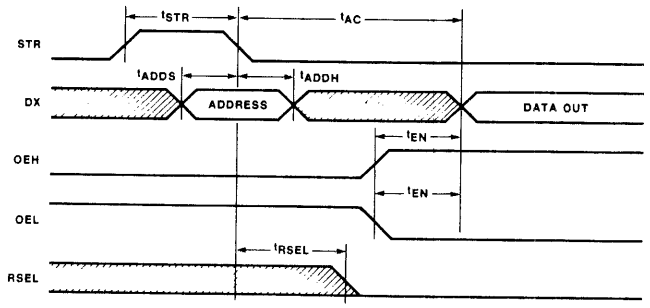
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$	−1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC} - .01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND + .01	V
Output Leakage	I_O	$0V \le V_{OUT} \le V_{CC}$	−1.0		1.0	µA
Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		1.0		µA
Input Capacitance	C_{IN}			5.0	7.0	pf
Output Capacitance	C_{OUT}			6.0	10.0	pf

AC CHARACTERISTICS

T_A = 25° C_L = 50pf

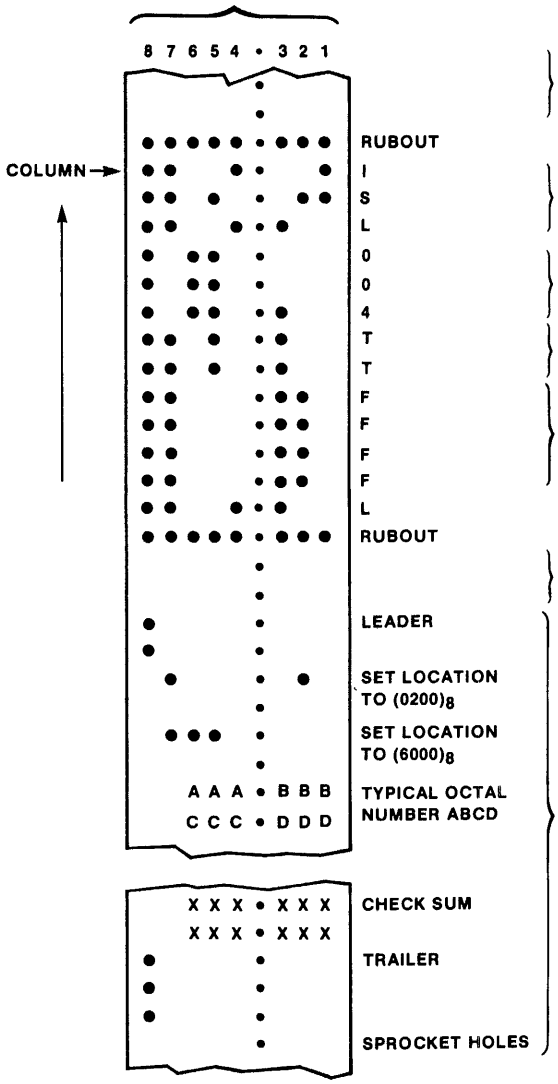
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Access time from STR	t_{AC}	IM6312	V_{CC} = 5.0V		200	400	ns
		IM6312A	V_{CC} = 10.0V		90	200	ns
Output enable time	t_{EN}	IM6312	V_{CC} = 5.0V		100	200	ns
		IM6312A	V_{CC} = 10.0V		60	120	ns
Strobe positive pulse width	t_{STR}	IM6312	V_{CC} = 5.0V	200	70		ns
		IM6312A	V_{CC} = 10.0V	120	80		ns
Address setup time	t_{ADDS}	IM6312	V_{CC} = 5.0V	25	-10		ns
		IM6312A	V_{CC} = 10.0V	20	0		ns
Address hold time	t_{ADDH}	IM6312	V_{CC} = 5.0V	100	40		ns
		IM6312A	V_{CC} = 10.0V	60	30		ns
Propagation to RAM Select	t_{RS}	IM6312	V_{CC} = 5.0V		80	180	ns
		IM6312A	V_{CC} = 10.0V		70	120	ns

SWITCHING WAVEFORMS



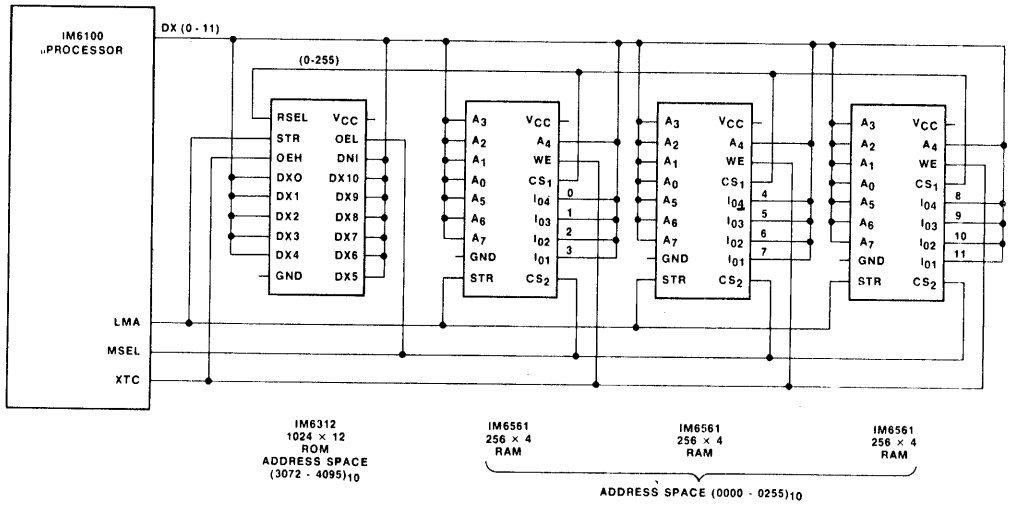
CUSTOM ROM PROGRAMMING

IM6312/IM6312A programming information is generated from the PAL III Symbolic Assembler as a "second pass" binary paper tape. A separate tape is required for each 1024 word ROM pattern, i.e. a separate symbolic should be generated for each 1024 word block of memory used, $(0000\text{-}1777)_8$, $(2000\text{-}3777)_8$, $(4000\text{-}5777)_8$ and $(6000\text{-}7777)_8$. A header is added to the front of each tape giving customer ID, chip select and RAM select programming information. The header consists of 15 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 letters designating true, false or don't care for inputs DX0 and DX1 to chips select gate A (see functional diagram), and 4 letters designating true, false, don't care for inputs DX0, DX1, DX2 and DX3 to the RAM select gate B (see functional diagram). Next is one letter (H or L) designating RSEL as active high or active low. RSEL function is inhibited when all RSEL inputs are VCC and RSE is active high. The leader ends with a rubout.



The example shown above has a customer ID and pattern ISL 004. chip selects are programmed to recognize addresses $(6000\text{-}7777)_8$ or $(3072\text{-}4095)_{10}$. RAM select is active low for addresses $(0000\text{-}0400)_8$ or $(0000\text{-}0255)_{10}$. For programs using less than 1024 words, the unused locations are automatically programed to a logic one.

A MINIMAL MICROPROCESSOR SYSTEM



FEATURES

- Operation from DC to 4.0 MHz
- Low Power - typ.<10mW @ 3.0 MHz
- 4V-11V Operation
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UART's
- Crystal Operation—IM6403

CMOS/LSI UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) IM6402/6403 IM6402A/6403A

GENERAL DESCRIPTION

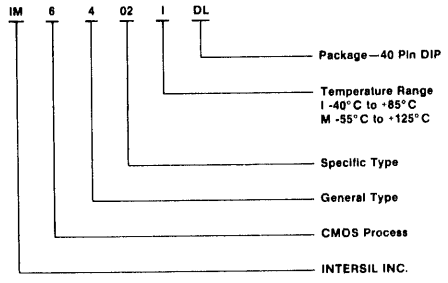
The IM6402 and IM6403 are CMOS/LSI subsystems for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operating clock frequencies up to 4.0 MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mw to 10mw. Status logic increases flexibility and simplifies the user interface.

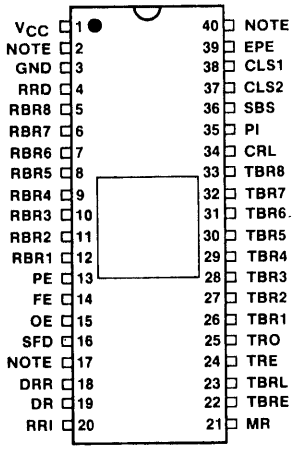
The IM6402 differs from the IM6403 on pins 2, 17, 19, 22, and 40 as shown in the connection diagram. The IM6403 utilizes pin 2 as a control and pins 17 and 40 for an inexpensive crystal oscillator as shown on page 5. TBREmpty and DReady are always active. All other input and output functions of the IM6402 and IM6403 are as described.

ORDERING INFORMATION

CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

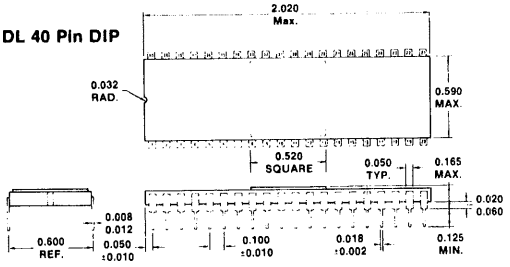


CONNECTION DIAGRAM



PACKAGE DIMENSIONS

DL 40 Pin DIP



NOTE:

PIN	IM6402	IM6403
2	N/C	CONTROL
17	RRC	OSC IN
40	TRC	OSC OUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND − 0.3V to VCC+ 0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial IM6402A/03AI	-40°C to +85°C
Military IM6402A/03AM	-55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% VCC			V
Logical "0" Input Voltage	V_{IL}				20% VCC	V
Input Leakage	I_{IL}	OV VIN VCC	-1.0		1.0	µA
Logical "1" Output Voltage	V_{OH}	IOUT = 0	VCC - 0.01			V
Logical "0" Output Voltage	V_{OL}	IOUT = 0			GND + 0.01	V
Output Leakage	I_O	OV Vo VCC	-I.0		I.0	µA
Supply Current IM6402A/03A	I_{CC}	VIN = VCC		5.0	500	µA
Input Capacitance	C_{IN}			7.0	8.0	pF
Output Clearance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 10.0V, C_L = 50pF, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency IM6402	f_{clock}		D.C.	6.0	4.0	MHz
Crystal Frequency IM6403	$f_{crystal}$		D.C.	8.0	6.0	MHz
Pulse Widths CRL, DRR, TBRL	t_{pw}		100	40		ns
Pulse Width MR	t_{pw}	See switching time	400	200		ns
Input Data Setup Time	t_{SET}	waveforms 1, 2, 3	30	0		ns
Input Data Hold Time	t_{HOLD}		50	30		ns
Output Propagation Delays	t_{pd}			40	70	ns

SWITCHING WAVEFORMS

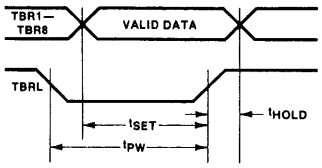


FIGURE 1.

DATA INPUT CYCLE

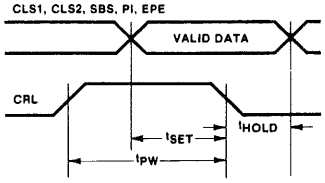


FIGURE 2.

CONTROL REGISTER LOAD CYCLE

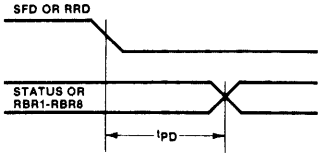


FIGURE 3.

STATUS FLAG OUTPUT DELAYS OR DATA OUTPUT DELAYS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+7.0V
Input or Output Voltage Applied		GND -0.3V to V_{CC}+0.3V
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range	Industrial IM6402/03I	-40°C to +85°C
	Military IM6402/03M	-55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0 +− 10%. T_A = Operating Temperature Range

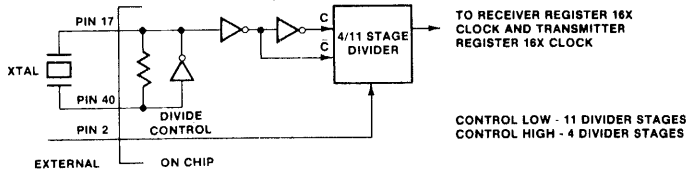
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		$V_{CC}-2.0$			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$OV \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.2 mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output Leakage	I_O	$OV \leq V_O \leq V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC}	V_{IN} = GND or V_{CC}; Output Open		1.0	100	μA
Input Capacitance	C_{IN}			7.0	8.0	
Output Capacitance	C_O			8.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency IM6402	f_{clock}		D.C.	3.0	2.0	MHz
Crystal Frequency IM6403	$f_{crystal}$		D.C.	4.0	3.58	MHz
Pulse Widths CRL, DRR, TBRL	t_{pw}		150	50		ns
Pulse Width MR	t_{pw}	See switching time	400	200		ns
Input Data Setup Time	t_{SET}	waveforms 1, 2, 3	50	20		ns
Input Data Hold Time	t_{HOLD}		60	40		ns
Output Propagation Delays	t_{pd}			80	120	ns

IM6403 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER WITH ON CHIP 4/11 STAGE DIVIDER

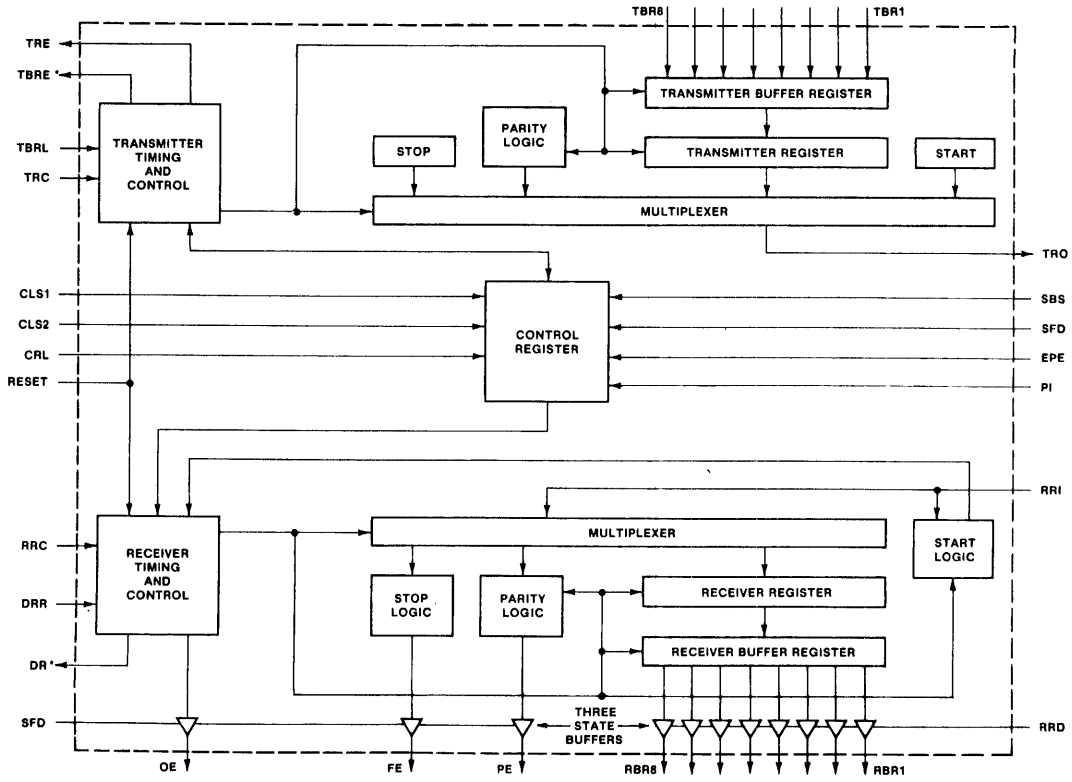
The IM6403 differs from the IM6402 on three inputs, TRC, RRC, and pin 2, and two outputs TBRE and DR. Outputs DR and TBRE are not three-state, but are always active.



The divider chain output acts as a 16X clock to both the receiver register and transmitter register. Consequently both receiver and transmitter operate at the same frequency. The TRClock and RRClock inputs are used for a crystal oscillator while pin 2 controls the number of divider stages.

The on chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2 Hz for an easy teletype interface.

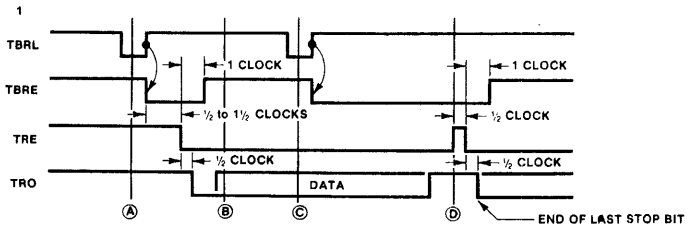
FUNCTIONAL BLOCK DIAGRAM



*These outputs are three state (IM6402) or always active (IM6403).

TRANSMITTER OPERATION

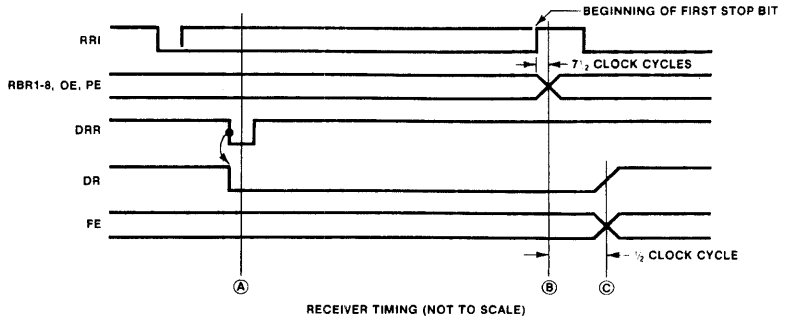
The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. (A) Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. (B) The rising edge of TBRL clears TBREmpty. ½ to 1½ clock cycles later data is transferred to the transmitter register and TREmpty is cleared. ½ cycle later transmission starts. Output data is clocked by TRClock. The clock rate is 16 times the data rate. ½ clock cycle later TBREmpty is reset to a logic high. (C) A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

RECEIVER OPERATION

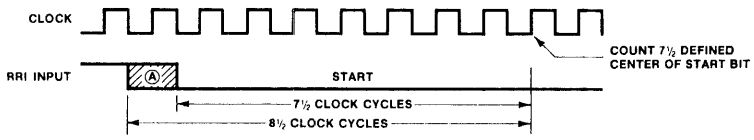
Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. (A) A low level on DRReset clears the DReady line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. © ½ clock cycle later DReady is reset to a logic high, FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error.



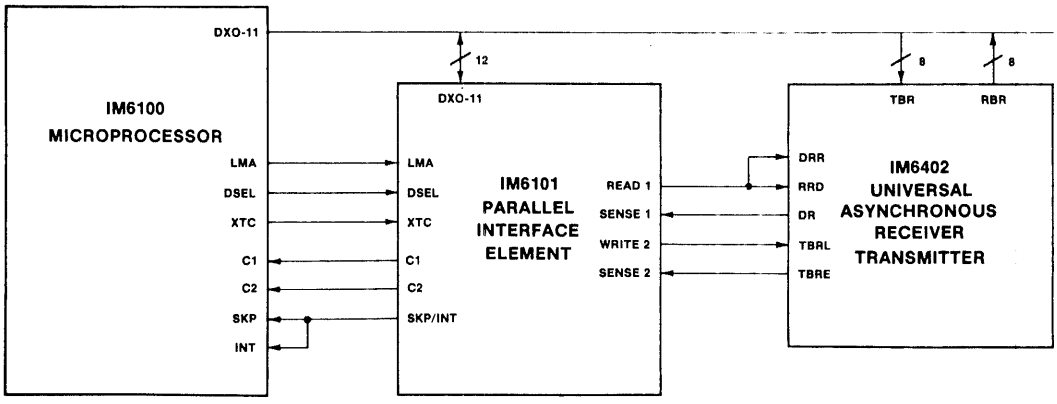
RECEIVER TIMING (NOT TO SCALE)

START BIT DETECTION

The receiver uses a 16X clock for timing. (A) the start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, ±1/32 bit or ±3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



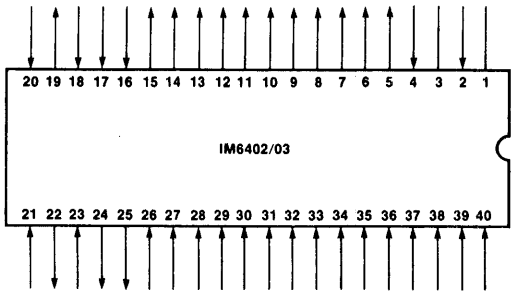
INTERFACING WITH THE IM6100 MICROPROCESSOR



PIN ASSIGNMENT AND FUNCTIONS

PIN	SYMBOL	DESCRIPTION
1	VCC	+5 Volts Supply
2	IM6402-N/C IM6403-Control	No Connection 4/11 Stage Divider High: 4 Stage Low: 11 Stage
3	GND	Ground
4	RRD	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8

PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	IM6402-RRC IM6403-OSCIN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received outputDR, to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE 6	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1-TBR8	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-OSCOUT	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

FEATURES

- Low Power - typ $<5.0\mu W$ standby
- Excellent Speed Operation
- TTL or CMOS Compatible On Inputs and Outputs
- 4V–11V V_{CC} Operation
- Static Operation
- On-Chip Address Register

CMOS RAM
1024 BIT
IM6508/IM6518
IM6508A/IM6518A

GENERAL DESCRIPTION

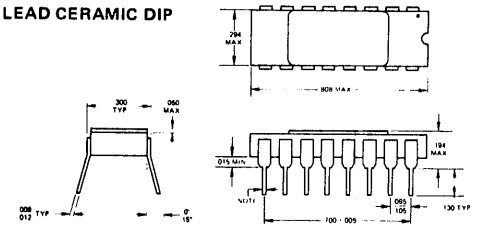
The IM6508/18 are high speed, low power, silicon gate CMOS 1024 bit static RAM's organized 1024 words by 1 bit. In all static states these RAM's exhibit the microwatt power requirements typical of CMOS. Inputs and three state output are TTL compatible. The basic part operates at 4 to 7 volts with a 5V, 25°C access time of 350 ns and supply current of $100\mu A$. Faster access times and lower supply currents are offered in a DASH-1 version. Higher operating voltages are offered in an "A" version. Data retention is guaranteed to 2.2 volts on all parts.

Write Enable and Chip Select functions are active in the low state. These functions are specified for easy interface to common I/O data busses. On chip address registers (clocked by the falling edge of STR) can often improve system performance and reduce package count. The two additional chip selects available on the IM6518 allow faster system design and reduced interconnect by multiplexing addresses, data in and data out on the same lines.

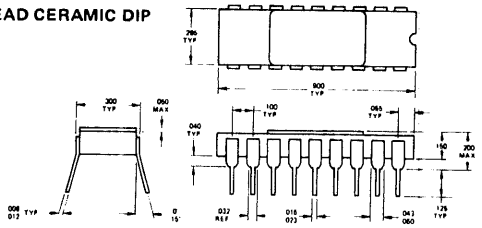
These devices are ideally suited for memory systems requiring low operating power, high performance or non-volatility (battery backup).

PACKAGE DIMENSIONS

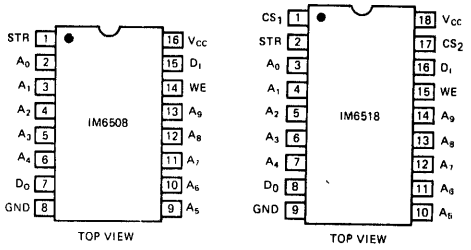
16 LEAD CERAMIC DIP



18 LEAD CERAMIC DIP



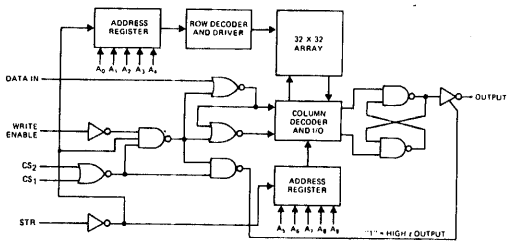
CONNECTION DIAGRAMS



Pin 1 is designated either by a dot or a notch.

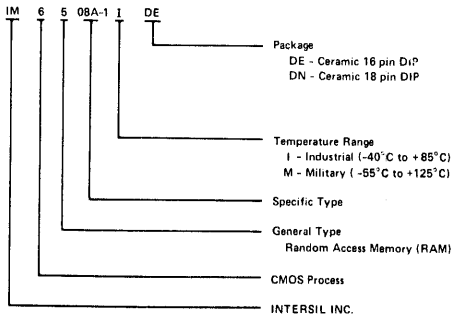
FUNCTIONAL DIAGRAM IM6518

The IM6508 functions as if CS_1, CS_2, and STR were tied together.

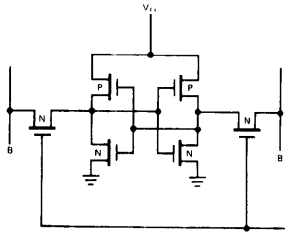


ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION:



CELL



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND −0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial	−40°C to +85°C
Military	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC} − 0.01			V
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND + 0.01	V
Output Leakage	I_O	$0V \leq V_o \leq V_{CC}$	−1.0		1.0	μA
Supply Current IM6508A/18A	I_{CC}	$V_{IN} = V_{CC}$		5.0	500	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.1	10	μA
IM6508A-1/18A-1	I_{CC}	$V_{IN} = V_{CC}$		1.0	100	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.01	1.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V, 10V C_L = 50 pF, T_A = 25°C

PARAMETER	SYMBOL	V_{CC}	IM6508A-1/18A-1		IM6508A/18A		UNITS
			MIN	MAX	MIN	MAX	
Access Time From STR	t_{AC}	5		200		350	ns
		10		95		150	ns
Output Enable Time	t_{EN}	5		120		210	ns
		10		55		90	ns
Output Disable Time	t_{DIS}	5		120		210	ns
		10		55		90	ns
STR Pulse Width (Positive)	t_{STR}	5	135		235		ns
		10	65		95		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	5	200		350		ns
		10	95		150		ns
Write Pulse Width (Negative)	t_{WP}	5	135		235		ns
		10	65		95		ns
Address Setup Time	t_{ADDS}	5	5		10		ns
		10	5		10		ns
Address Hold Time	t_{ADDH}	5	60		105		ns
		10	30		45		ns
Date Setup Time	t_{DS}	5	135		235		ns
		10	65		95		ns
Data Hold Time	t_{DH}	5	0		0		ns
		10	0		0		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND -0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial	-40°C to +85°C
Military	-55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} - 2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	I_{OUT} = 0	V_{CC} - 0.01			V
Logical "1" Output Voltage	V_{OH1}	I_{OH} = -0.2 mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	I_{OUT} = 0			GND + 0.01	V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output Leakage	I_O	$0 V \leqslant V_o \leqslant V_{CC}$	-1.0		1.0	μA
Supply Current IM6508/18	I_{CC}	$V_{IN} = V_{CC}$		1.0	100	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.1	10	μA
IM6508-1/18-1	I_{CC}	$V_{IN} = V_{CC}$		0.1	10	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.01	1.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50 pF (One TTL Load), T_A = Industrial or Military

PARAMETER	SYMBOL	IM6508-1/18-1		IM6508/18		UNITS
		MIN	MAX	MIN	MAX	
Access Time From STR	t_{AC}		300		460	ns
Output Enable Time	t_{EN}		180		285	ns
Output Disable Time	t_{DIS}		180		285	ns
STR Pulse Width (Positive)	t_{STR}	200		300		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	300		460		ns
Write Pulse Width (Negative)	t_{WP}	200		300		ns
Address Setup Time	t_{ADDS}	7		15		ns
Address Hold Time	t_{ADDH}	90		130		ns
Data Setup Time	t_{DS}	200		300		ns
Data Hold Time	t_{DH}	0		0		ns

SWITCHING WAVEFORMS AND SWITCHING TIME LOAD

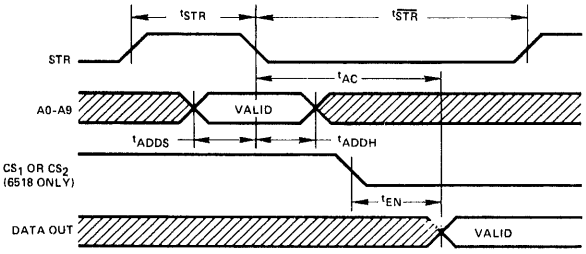


FIGURE 1. READ CYCLE

The IM6508 output is active when STR is low. The IM6518 output data latch retains the data when STR returns high.

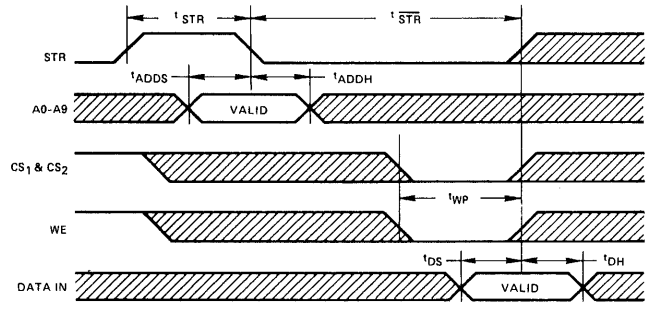


FIGURE 2. WRITE CYCLE

The IM6508 performs a write operation when STR = WE = 0. The IM6518 performs a write operation when STR = CS_1 = CS_2 = WE = 0. The write operation is terminated on any positive edge from STR or CS_1 or CS_2 or WE.

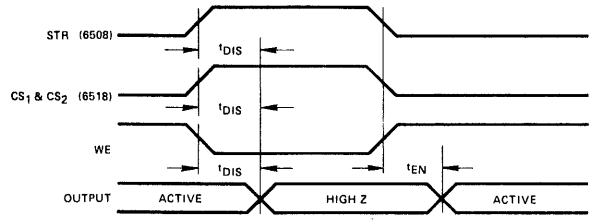


FIGURE 3. OUTPUT ENABLE

The IM6508 output is high impedance when STR = 1 or WE = 0. The IM6518 output is high impedance when CS_1 or CS_2 = 1 or WE = 0.

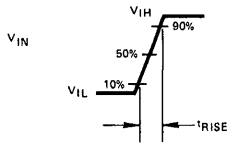
IM6508

STR	WE	OPERATION	OUTPUT
0	0	Write	High Resistance
0*	1	Read	Memory Data
1	X	Hold	High Resistance

* Addresses are loaded on chip by the falling edge of STROBE.

IM6518

STR	CS1	CS2	WE	OPERATION	OUTPUT
0	0	0	0	Write	High Resistance
0*	0	0	1	Read	Memory Data
1	0	0	1	Read	Memory Data
X	0	1	X	Hold	High Resistance
X	1	0	X	Hold	High Resistance



$t_{rise} = t_{fall} = 20$ ns

DELAY TIMES ARE MEASURED FROM 50% TO 50%

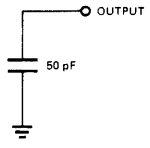
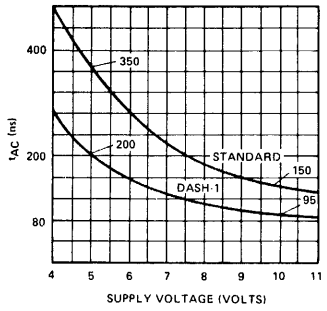


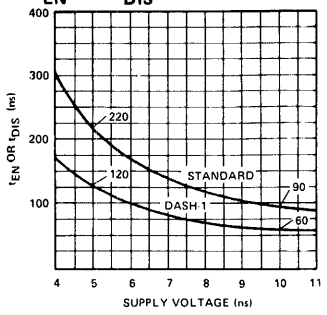
FIGURE 4. SWITCHING TIME WAVEFORMS AND LOAD

GUARANTEED AC CHARACTERISTICS

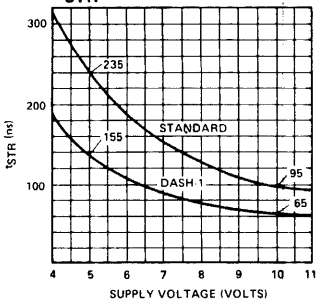
ACCESS TIME FROM STR
t_{AC} INCREASES 0.3%/°C



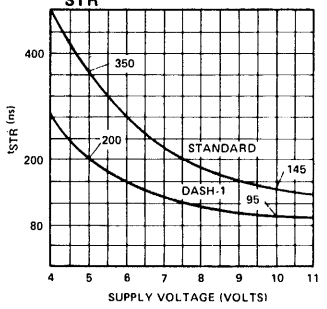
OUTPUT ENABLE TIME
OUTPUT DISABLE TIME
t_{EN} AND t_{DIS} INCREASE 0.3%/°C



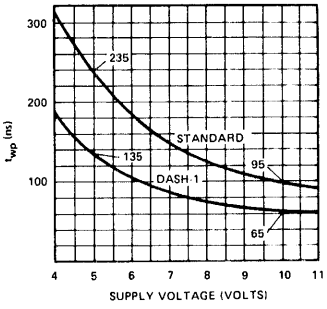
MINIMUM STR PULSE WIDTH (POSITIVE)
t_{STR} INCREASES 0.3%/°C



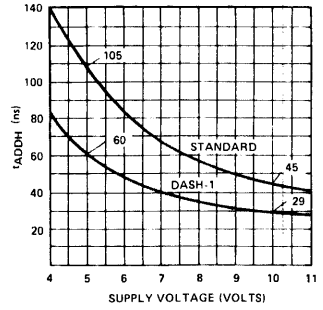
MINIMUM STR PULSE WIDTH (NEGATIVE)
$t_{\overline{STR}}$ INCREASES 0.3%/°C



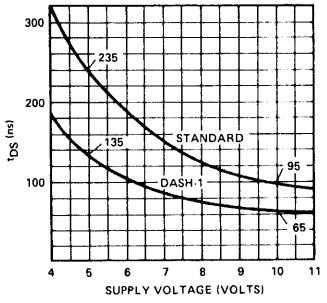
WRITE PULSE WIDTH
twp INCREASES 0.3%/°C



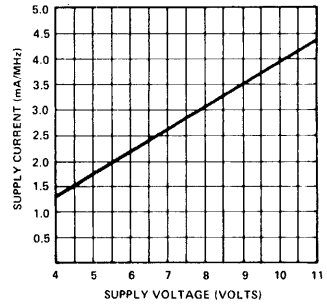
ADDRESS HOLD TIME
t_{ADDH} INCREASES 0.3%/°C



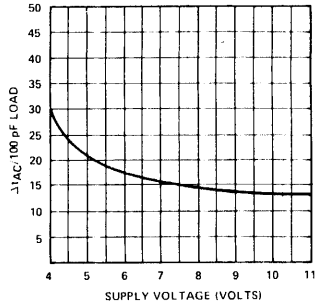
INPUT DATA SETUP TIME
t_{DS} INCREASES 0.3%/°C



DYNAMIC POWER REQUIREMENTS
AT 1 MHz I_{DYN} = (CURVE VALUE)
(OPERATING FREQUENCY)/ (1 MHz)

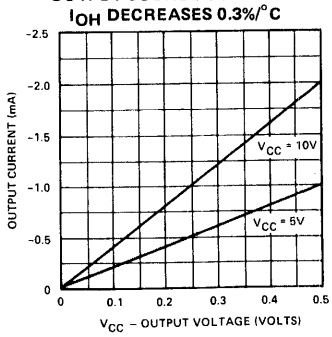


DELTA ACCESS TIME
PER 100 pF LOAD CAPACITANCE
Δt_{AC} INCREASES 0.3%/°C

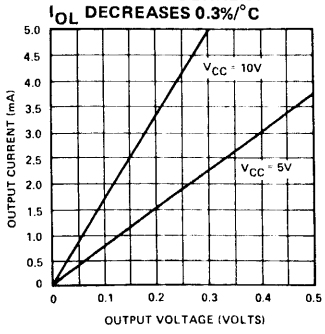


GUARANTEED DC CHARACTERISTICS

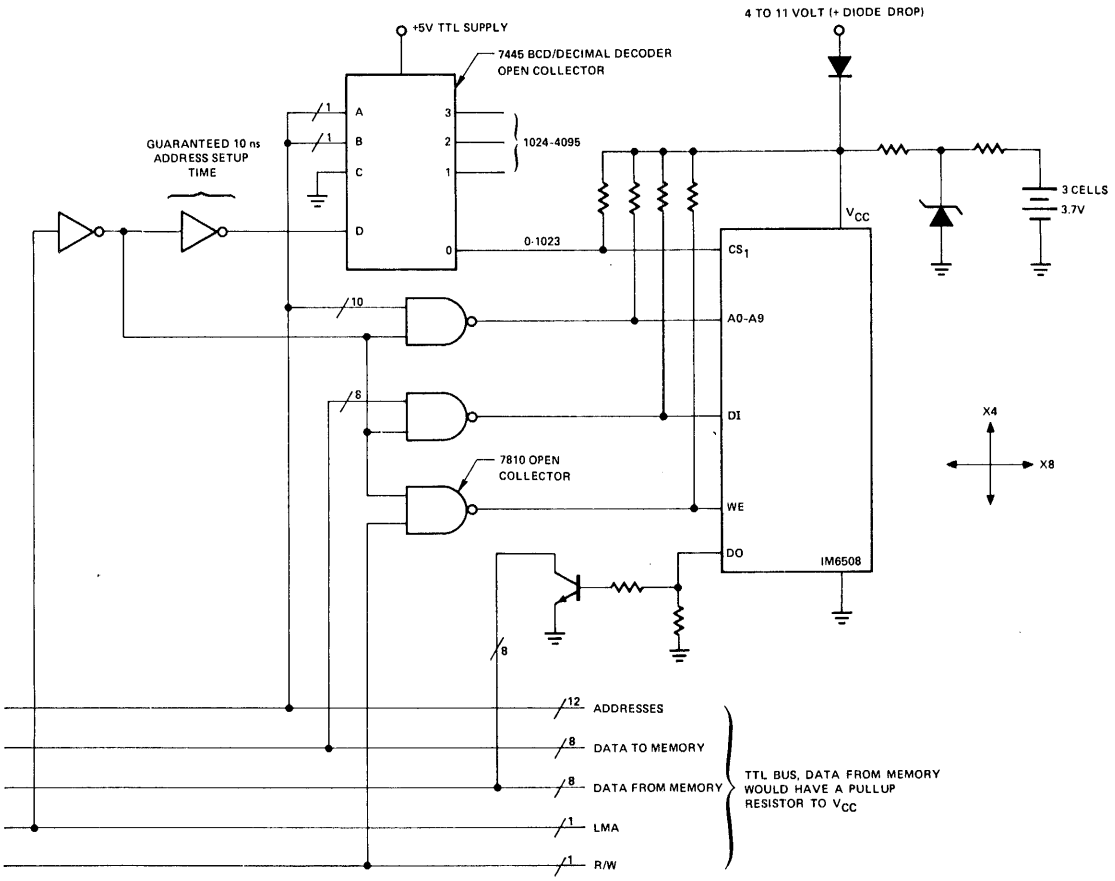
OUTPUT SOURCE CURRENT
I_{OH} DECREASES 0.3%/°C

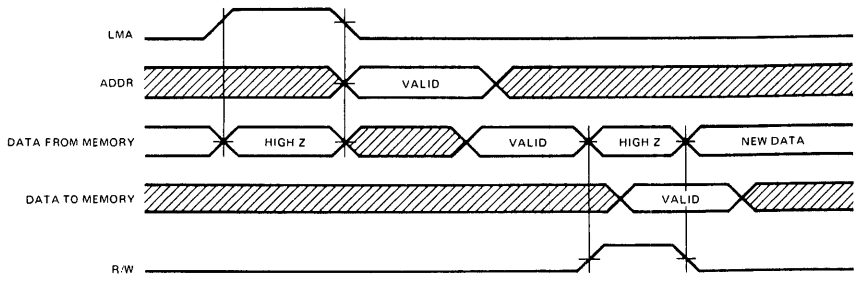


OUTPUT SINK CURRENT
I_{OL} DECREASES 0.3%/°C



TYPICAL 4K x 8 NONVOLATILE MEMORY PLANE WITH INTERFACE TO A TTL BUS





READ MODIFY WRITE WAVE FORMS

FEATURES

- Low Power – typ < 5.0 μW standby
- Excellent Speed Operation
- TTL Compatible On Inputs and Outputs
- 5 V V_{CC} Operation
- Static Operation
- On-Chip Address Register

CMOS RAM
1024-BIT
IM6508C/IM6518C

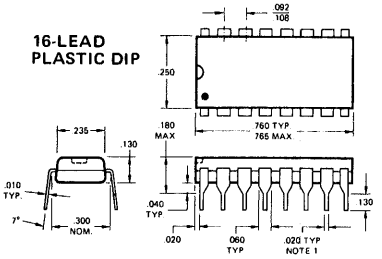
GENERAL DESCRIPTION

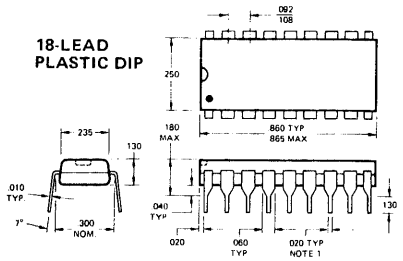
The IM6508/18 are high speed, low power, silicon gate CMOS 1024 bit static RAM's organized 1024 words by 1 bit. In all static states these RAM's exhibit the microwatt power requirements typical of CMOS. Inputs and three state output are TTL compatible. The basic part operates at 5 V, 0°C to 75°C, with an access time of 600 ns and a supply current of 1.6 mA.

Write Enable and Chip Select functions are active in the low state. These functions are specified for easy interface to common I/O data busses. On chip address registers (clocked by the falling edge of STR) can often improve system performance and reduce package count. The two additional chip selects available on the IM6518 allow faster system design and reduced interconnect by multiplexing addresses, data in and data out on the same lines.

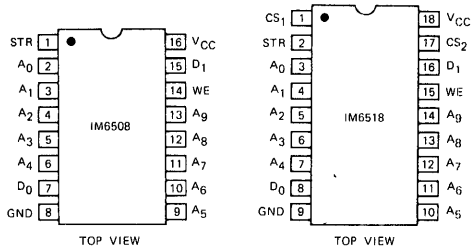
These devices are ideally suited for memory systems requiring low operating power, high performance or non-volatility (battery backup).

PACKAGE DIMENSIONS





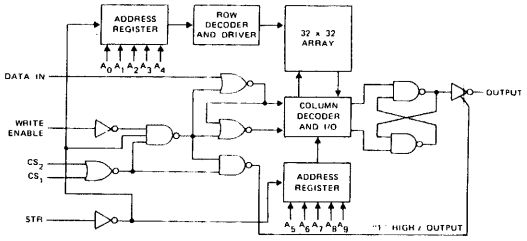
CONNECTION DIAGRAMS



Pin 1 is designated either by a dot or a notch.

FUNCTIONAL DIAGRAM IM6518

The IM6508 functions as if CS_1, CS_2, and STR were tied together.



ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION:

IM 6 5 08 I PE

- PE – Plastic 16 pin DIP
  PN – Plastic 18 pin DIP — Package
- C – Commercial (0°C to +75°C) — Temperature Range
- Specific Type
- Random Access Memory (RAM) — General Type
- CMOS Process
- INTERSIL INC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0 V
Input or Output Voltage Supplied	GND –0.5 V to V_{CC} +0.5 V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range Commercial	0°C to +75°C

DC CHARACTERISTICS V_{CC} = 5.0 V ± 5%, T_A = Commercial

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} –2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0 V \leqslant V_{IN} \leqslant V_{CC}$	–5.0		5.0	μA
Logical "1" Output Voltage	V_{OH2}	I_{OUT} = 0	V_{CC} –0.01			V
Logical "1" Output Voltage	V_{OH1}	I_{OH} = –0.2 mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	I_{OUT} = 0			GND +0.01	V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 1.6 mA			0.45	V
Output Leakage	I_O	$0 V \leqslant V_o \leqslant V_{CC}$	–5.0		5.0	μA
Supply Current IM6508/18	I_{CC}	$V_{IN} = V_{CC}$		1.0	1.6	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0 V ± 5%, C_L = 50 pF (One TTL Load), T_A = Industrial or Military

PARAMETER	SYMBOL	IM6508/18		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		600	ns
Output Enable Time	t_{EN}		375	ns
Output Disable Time	t_{DIS}		375	ns
STR Pulse Width (Positive)	t_{STR}	395		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	600		ns
Write Pulse Width (Negative)	t_{WP}	395		ns
Address Setup Time	t_{ADDS}	20		ns
Address Hold Time	t_{ADDH}	170		ns
Data Setup Time	t_{DS}	395		ns
Data Hold Time	t_{DH}	0		ns

TRUTH TABLES

IM6508

STR	WE	OPERATION	OUTPUT
0	0	Write	High Resistance
0*	1	Read	Memory Data
1	X	Hold	High Resistance

* Addresses are loaded on chip by the falling edge of STROBE.

IM6518

STR	CS1	CS2	WE	OPERATION	OUTPUT
0	0	0	0	Write	High Resistance
0*	0	0	1	Read	Memory Data
1	0	0	1	Read	Memory Data
X	0	1	X	Hold	High Resistance
X	1	0	X	Hold	High Resistance

FEATURES

- Low Power Operation
- TTL or CMOS Compatible on Inputs and Outputs
- 4V - 11V V_{CC} Operation
- Static Operation
- On-Chip Address Register
- Two IM6512's can be used with IM6100 and IM6312 without additional components

PRELIMINARY CMOS RAM 768 BIT (64 × 12) IM6512/IM6512A

GENERAL DESCRIPTION

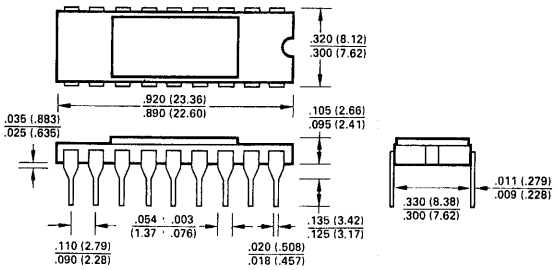
The IM6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 350ns. A wider operating voltage range, 4-11 volts, is available with the A version. Signal polarities and functions are specified for direct interfacing with the IM6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

FUNCTIONAL DESCRIPTION

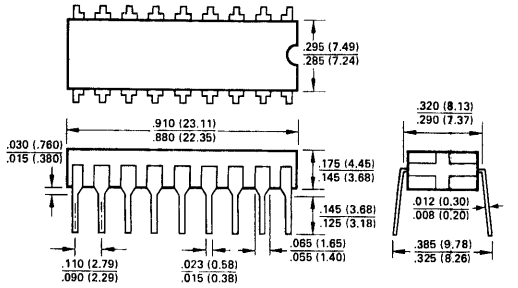
The MSEL pin performs both chip enable and write-enable functions. The IM6512 has three modes of operation: read-modify-write, read only, and write. The ADR input allows two IM6512's to be used without additional decoding circuitry.

PACKAGE DIMENSIONS

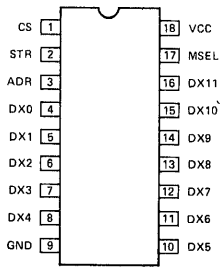
18 LEAD CERAMIC DIP



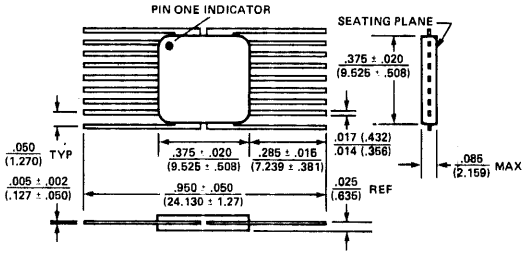
18 LEAD CERDIP



CONNECTION DIAGRAM



18 LEAD FLAT PACK



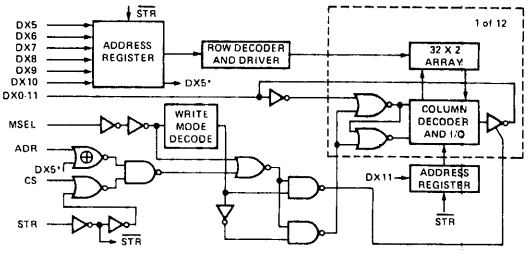
ORDERING INFORMATION

MEMORY CIRCUIT AND PRODUCT CODE EXPLANATION:

IM 6 5 12A I DN

- DN - Ceramic 18 pin DIP
  JN - Cerdip 18 pin
  FN - Flatpack 18 pin
- Temperature
  C - Commercial (0°C to +70°C)
  I - Industrial (−40°C to +85°C)
  M - Military (−55°C to +125°C)
- Specific Type
- General Type
  Random Access Memory (RAM)
- DCMOS Product
- INTERSIL INC.

FUNCTIONAL DIAGRAM IM6512/12A



INTERSIL CMOS/LSI

ABSOLUTE MAXIMUM RATINGS

IM6512A

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND – 0.3V to V_{CC} +0.3V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
Industrial IM6512AI	–40°C to +85°C
Military IM6512AM	–55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	–1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC}–0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND+0.01	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	–1.0		1.0	μA
Supply Current	I_{CC}	*		5.0	500	μA
	I_{CC}	*V_{CC} = 3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 10V, C_L = 50pF, T_A = 25°C

PARAMETER	SYMBOL	IM6512A		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		150	ns
Output Enable Time	t_{EN}		90	ns
Output Disable Time	t_{DIS}		90	ns
STR Pulse Width (Positive)	t_{STR}	95		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	150		ns
Cycle Time	t_C	245		ns
Write Pulse Width (Negative)	t_{WP}	95		ns
Address Setup Time	t_{AS}	20		ns
Address Hold Time	t_{AH}	45		ns
Data Setup Time	t_{DS}	95		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	60		ns
MSEL Setup Time	t_{MS}	20		ns
MSEL Hold Time	t_{MH}	20		ns

ABSOLUTE MAXIMUM RATINGS

IM6512

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND –0.3V to V_{CC} +0.3V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
Industrial IM6512I	–40°C to +85°C
Military IM6512M	–55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}–2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	–1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = –0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	–1.0		1.0	μA
Supply Current	I_{CC}	*		1.0	100	μA
	I_{CC}	*V_{CC} = 3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capactiance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50 pF , T_A = Industrial or Military

PARAMETER	SYMBOL	IM6512		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		460	ns
Output Enable Time	t_{EN}		285	ns
Output Disable Time	t_{DIS}		285	ns
STR Pulse Width (Positive)	t_{STR}	300		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	460		ns
Cycle Time	t_C	760		ns
Write Pulse Width (Negative)	t_{WP}	300		ns
Address Setup Time	t_{AS}	40		ns
Address Hold Time	t_{AH}	130		ns
Data Setup Time	t_{DS}	300		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	150		ns
MSEL Setup Time	t_{MS}	50		ns
MSEL Hold Time	t_{MH}	50		ns

ABSOLUTE MAXIMUM RATINGS

IM6512C

Supply Voltage	+7.0V
Input or Output Voltage Supplied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Commercial IM6512C	0°C to +70°C

DC CHARACTERISTICS V_{CC} = 5.0V ±5%, T_A = Commercial

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−1.5			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	−5.0		5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.45	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	−5.0		5.0	μA
Supply Current	I_{CC}	*			800	μA
Input Capactiance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

*STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 5.0V ±5%, C_L = 50 pF , T_A = Commercial

PARAMETER	SYMBOL	IM6512C		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		600	ns
Output Enable Time	t_{EN}		375	ns
Output Disable Time	t_{DIS}		375	ns
STR Pulse Width (Positive)	t_{STR}	395		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	600		ns
Cycle Time	t_C	995		ns
Write Pulse Width (Negative)	t_{WP}	395		ns
Address Setup Time	t_{AS}	40		ns
Address Hold Time	t_{AH}	130		ns
Data Setup Time	t_{DS}	395		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	150		ns
MSEL Setup Time	t_{MS}	50		ns
MSEL Hold Time	t_{MH}	50		ns

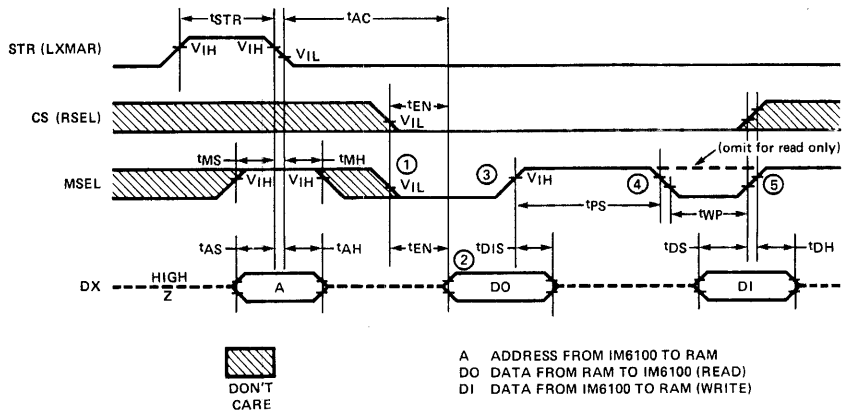


FIGURE 1. Read-Modify-Write or Read Cycle

Read-Modify-Write (MSEL high when STR goes low)

DX pins are high impedance until the first negative-going edge on MSEL ① which enables the outputs to read data from memory ②. When MSEL returns high ③ the DX pins return to high impedance for the remainder of the cycle.

The (optional) second negative-going MSEL pulse ④ causes a write to memory. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑤. MSEL must remain high until STR returns high ending the cycle.

Read Only

Same as Read-Modify-Write except the second negative-going MSEL pulse is omitted.

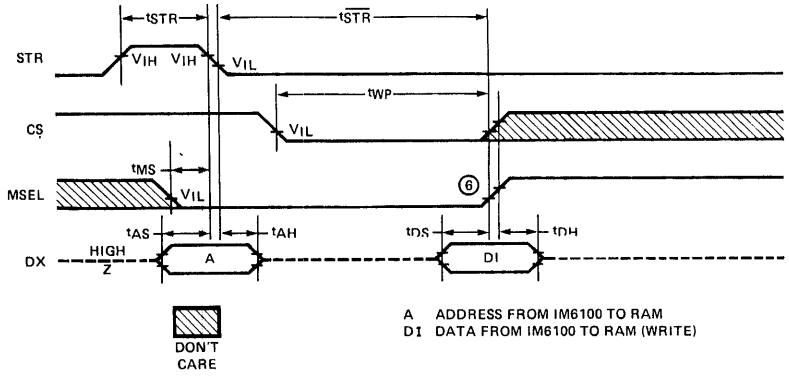


FIGURE 2. Write Cycle

Write (MSEL low when STR goes low)

DX pins are always high impedance. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑥.

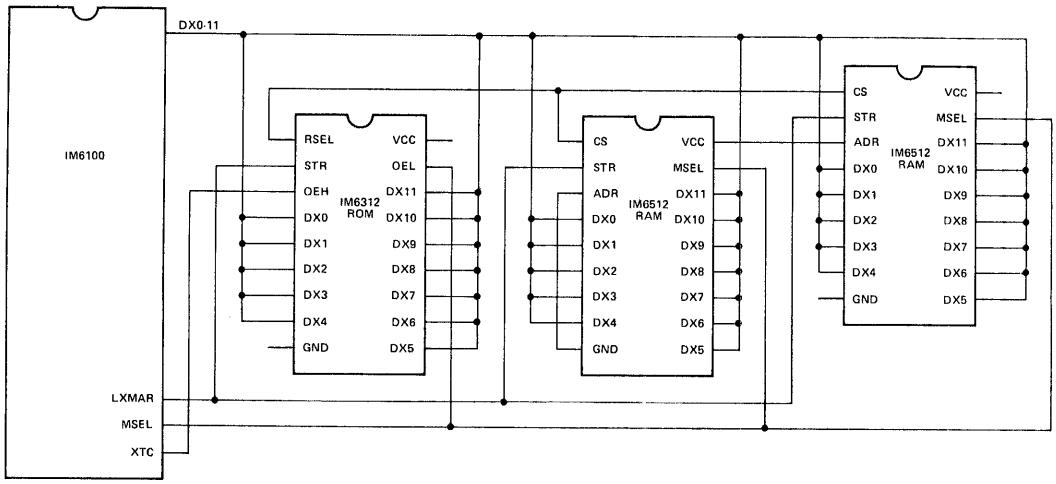


FIGURE 3. A Typical Microprocessor System

Typical Microprocessor System (Figure 3)

In the example shown, the IM6312 RSEL (RAM Select) output is programmed to go low for addresses 0-255. IM6512 with ADR = "0" will respond to addresses 0-63 (and 128-191); IM6512 with ADR = "1" will respond to addresses 64-127 (and 192-255).

ADR

ADR should be either tied to logic "0" (GND) or logic "1" (V_{CC}). The data on this pin is compared internally with address data on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the IM6512 DX lines remain high impedance and data is unchanged. As a result, two IM6512 memories can be used with the IM6100 and IM6312 without additional components.

ADR	DX5*	MSEL @ $\overline{STR}$[1]	FUNCTION
L	L	L	WRITE
L	L	H	READ-MODIFY-WRITE, READ ONLY
L	H	X	NO OP. (HI-Z)
H	L	X	NO OP. (HI-Z)
H	H	L	WRITE
H	H	H	READ-MODIFY-WRITE, READ ONLY

X = DON'T CARE

Note 1: Addresses are latched on chip by the falling edge of STR

FIGURE 4. IM6512 Truth Table

256-BIT CMOS SILICON GATE RAM

IM6523

FEATURES

- Low power < 1μW/bit
- +5V V_{CC} operation
- T^2L compatible on inputs and outputs
- Medium speed operation, < 500 ns access
- Static operation — totally asynchronous
- Fully decoded and buffered

GENERAL DESCRIPTION

The IM6523 is a fully decoded and buffered CMOS Silicon Gate 256-bit Random Access Memory. Pinouts, polarities and functional operation are similiar to IM5523 (74200), CS_1, CS_2, CS_3 and $\overline{WE}$ are active in the low state. D_{OUT} complements D_{IN}. Operation is specified at V_{CC} = +5V ±10%. Operating range is for $4V \leqslant V_{CC} \leqslant 7V$.

OPERATION

Chip Enables: Three chip enables are provided. CS_2 and CS_3 are convential logical chip enables; they disable the internal write circuitry and output buffer; and chip enable access time is relatively fast. CS_1 disables the X-decoder in addition to the internal write circuitry and output buffer. CS_1 has a slower access time, and puts the chip in a low power mode.

Power: The IM6523 has three sources of power consumption:

1. **Ratio Power (I_{CC1})**
   Eight ratio stages on chip consume power when CS_1 = 0 and not when CS1 = 1.

2. **Junction Leakage (I_{CC2})**
   P-N junction leakage from V_{CC} to ground.

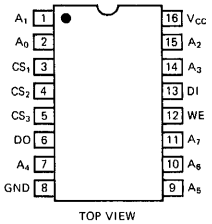
3. **f_oCV^2 Power (I_{CC3})**
   Power consumed switching capacitance from ground to V_{CC} and back at a rate f_o.

Total power requirements for a package can be calculated $P_T = V_{CC} \times [(I_{CC2}) + (I_{CC1}) \times (\text{duty cycle}) + I_{CC3}]$. In a system additional f_oCV^2 power should be allowed for switching capacitance associated with device inputs, device outputs and PC board layout.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+7.0V
Input Voltage Applied		GND–.3V to V_{CC} +.3V
Output Voltage Applied		–0.5V to $+V_{CC}$
Operating Temperature Range	(INDUSTRIAL)	–40°C to +85°C
	(MILITARY)	–55°C to +125°C
Storage Temperature Range		–65°C to +150°C

CONNECTION DIAGRAM



TOP VIEW

Pin 1 is designated by a dot or a notch.

DC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = Industrial or Military)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Logical "1" Input Voltage	V_{IN}		V_{CC}–2.0	1.9		V
Logical "0" Input Voltage	V_{IL}			1.3	0.8	
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	–1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	I_{OUT} = 0μA	V_{CC}–.01			V
Logical "1" Output Voltage	V_{OH1}	I_{OUT} = –0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	I_{OUT} = 0μA			GND + .01	V
Logical "0" Output Voltage	V_{OL1}	I_{OUT} = 2.0mA			0.45	V
Output Leakage	I_O	$0V \leq V_{OUT} \leq V_{CC}$	–1.0		1.0	μA
Supply Current (Active)	I_{CC1}	CS_1 = 0V, WE = V_{CC}			6.0	mA
(Standby)	I_{CC2}	CS_1 = V_{CC}		0.1	50	μA
(Dynamic)	I_{CC3}	$\overline{WE}$ = GND, Cycle Time = 1μs, other Inputs Switching From GND to V_{CC}			800	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_o			6.0	10.0	pF

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = Industrial or Military, C_L = 15pF)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
READ CYCLE					
Access Time From CS_1	t_{AS}		400	800	ns
Access Time From CS_2 or CS_3	t_{AC}		80	200	ns
Access Time From Address	t_{AA}		400	800	ns
Output Disable Time From Any CS	t_{DIS}		80	200	ns
Output Hold Time From Address	t_{OH}	50	300		ns
Read Cycle Time	t_{RC}		400	800	ns
WRITE CYCLE					
Delay Time From CS_1 to WE	t_{SW}	550	350		ns
Delay Time From CS_2 or CS_3 to WE	t_{CW}	250	125		ns
Delay Time From Address to WE	t_{AW}	550	350		ns
Write Pulse Width	t_{WP}	250	125		ns
Delay Time From WE to Any CS	t_{WC}	0	–100		ns
Delay Time From WE to Address	t_{WA}	0	–100		ns
Input Data Set-Up Time	t_{DS}	300	150		ns
Input Data Hold Time	t_{DH}	50	0		ns
Output Disable Time From WE	t_{DIS}		80	200	ns
Output Recovery Time From WE	t_{WR}		80	200	ns
Write Cycle Time	t_{WC}		475	800	ns
Maximum Rise and Fall Time			100	20	μs

NOTE: 1. All typicals are shown for V_{CC} = 5V and T_A = 25°C.

MEMORY FUNCTION TABLE

CS_1	CS_2	CS_3	$\overline{WE}$	OPERATION	POWER	OUTPUT
0	0	0	0	Write	I_{CC1}	High Z
0	0	0	1	Read	I_{CC1}	Active
0	1	X	X	Hold	I_{CC1}	High Z
0	X	1	X	Hold	I_{CC1}	High Z
1	X	X	X	Hold	I_{CC2}	High Z

SWITCHING TIME WAVEFORMS

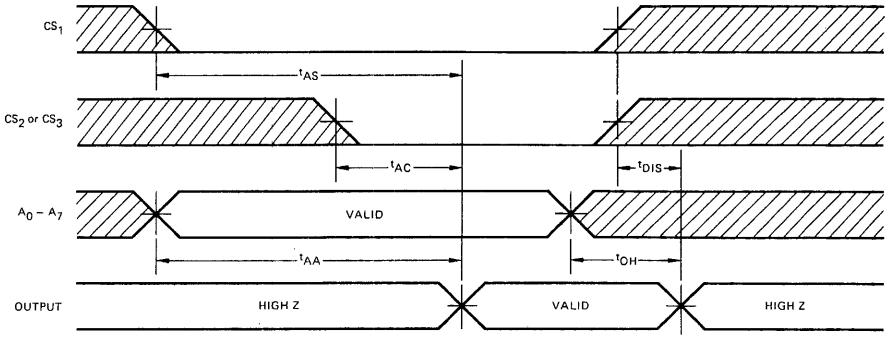


FIGURE 1. READ CYCLE

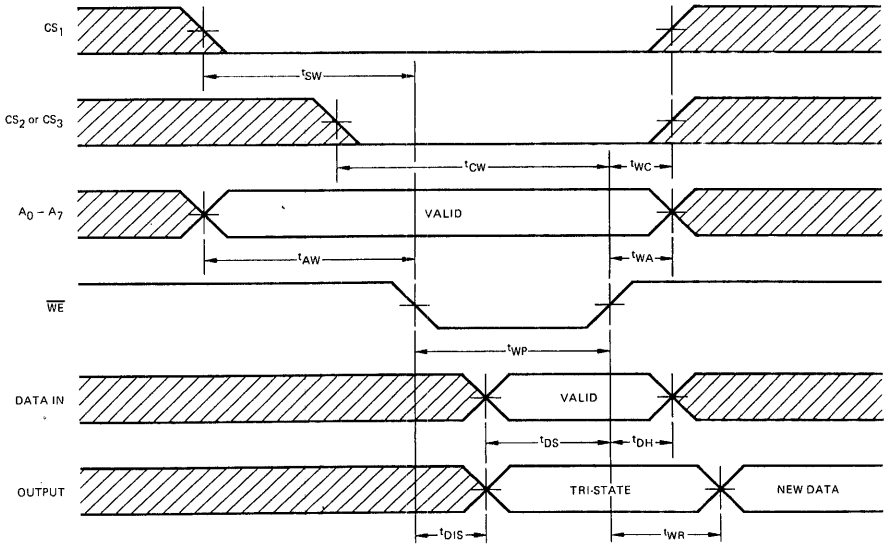


FIGURE 2. WRITE CYCLE

NOTES: 1. All times referenced to 1.5V.
2. Inputs are switched from .8V to 3.0V.
3. Output load is 50 pF.

TYPICAL DC CHARACTERISTICS

FIGURE 3. LOGIC "0" OUTPUT CHARACTERISTICS

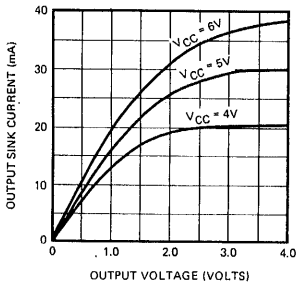
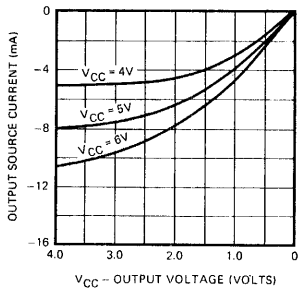


FIGURE 4. LOGIC "1" OUTPUT CHARACTERISTICS



GUARANTEED AC CHARACTERISTICS

FIGURE 5. CHANGE IN ACCESS TIME VERSUS LOAD CAPACITANCE

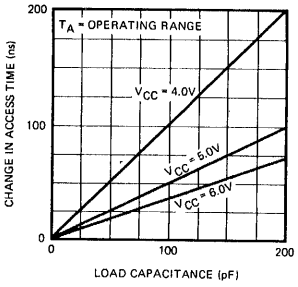


FIGURE 6. ACCESS TIME VERSUS V_{CC}

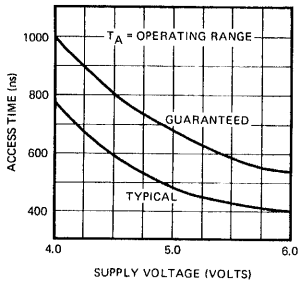
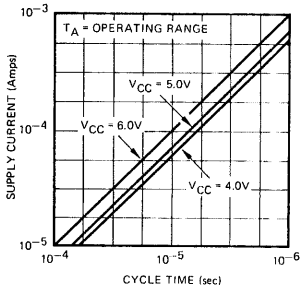
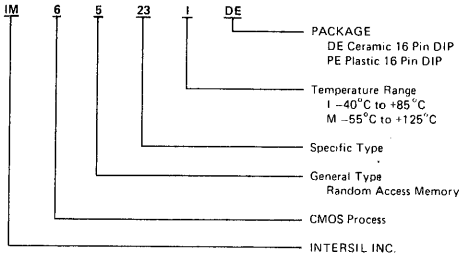


FIGURE 7. DYNAMIC SUPPLY CURRENT (I_{CC3}) VERSUS CYCLE TIME



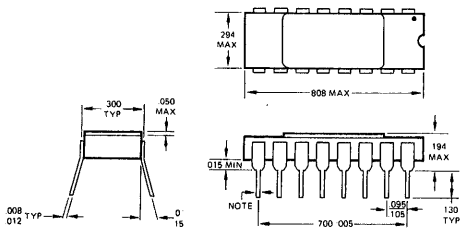
ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

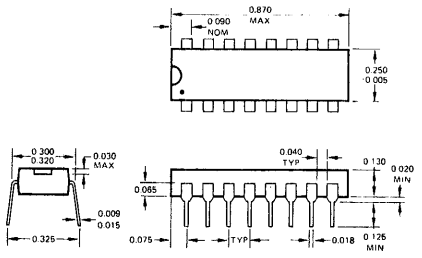


PACKAGE DIMENSIONS

16 LEAD CERAMIC DIP



16 LEAD PLASTIC DIP



NOTE: Board drilling dimensions will equal standard practice for .020 diameter lead.

FEATURES

- Low Power Operation
- Excellent Speed Operation
- TTL or CMOS Compatible On Inputs and Outputs
- 4V—11V V_{CC} Operation
- Static Operation
- On-Chip Address Register

CMOS RAM
1024 (256 X 4) BIT
IM6551/IM6561
IM6551A/IM6561A

GENERAL DESCRIPTION

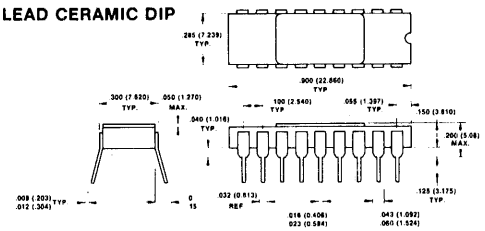
The IM6551/61 are high speed, low power silicon gate CMOS 1024 bit static RAM's organized 256 words by 4 bits. In all static states these RAMs exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4 to 7 volts with a 5V, 25°C access time of 200nS and supply current of 100μA. Faster access times and lower supply currents are offered in a DASH-1 version. Higher operating voltages are offered in an "A" version. Data retention is guaranteed to 2.0 volts.

Write Enable and Chip Select functions are active in the low state. Chip Selects (IM6551 CS, IM6561 CS1 and CS2) are level sensitive and may occur after the falling edge of the STR without affecting access time. On chip address registers and chip enable register (IM6551 CE) are clocked by the falling edge of STR. These signals must be valid for a setup time (tADDS) prior to and a hold time (tADDH) following the falling edge of STR. On chip registers can improve system performance and reduce package count. Chip selects allow faster system design and reduced interconnect by multiplexing addresses, data in and data out on the same lines.

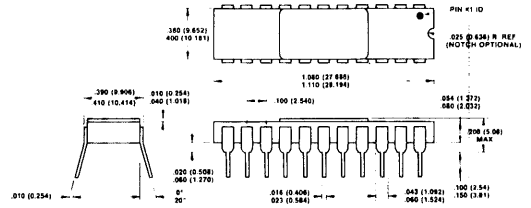
These devices are ideally suited for memory systems requiring low operating power, high performance or nonvolatility (battery backup).

PACKAGE DIMENSIONS

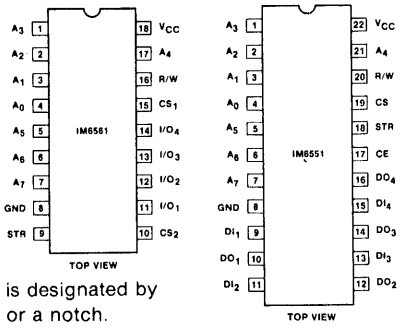
18 LEAD CERAMIC DIP



22 LEAD CERAMIC DIP

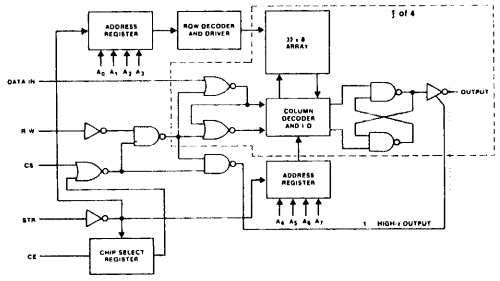


CONNECTION DIAGRAMS

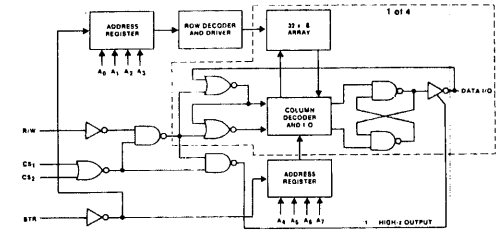


Pin 1 is designated by a dot or a notch.

FUNCTIONAL DIAGRAM IM6551/51A

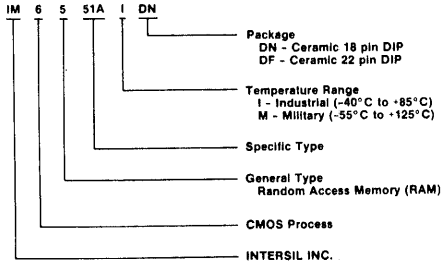


FUNCTIONAL DIAGRAM IM6561/61A



ORDERING INFORMATION

MEMORY CIRCUIT AND PRODUCT CODE EXPLANATION:



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND − 0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial IM6551A/61AI	-40°C to +85°C
Military IM6551A/61AM	-55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT}=0$	V_{CC}-0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT}=0$			GND+0.01	V
Output Leakage	I_O	$0V \leq V_o \leq V_{CC}$	-1.0		1.0	μA
Supply Current	I_{CC}	$V_{IN}=V_{CC}$		5.0	500	μA
	I_{CC}	$V_{CC}=3.0V$		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS VCC = 5.0V, 10V CL = 50pF, TA = 25°C

PARAMETER	SYMBOL	IM6551A/61A			UNITS
		MIN	TYP	MAX	
Access Time From STR	t_{AC}		120	180	ns
Output Enable Time	t_{EN}		60	90	ns
Output Disable Time	t_{DIS}		60	90	ns
STR Pulse Width (Positive)	t_{STR}	60	30		ns
STR Pulse Width (Negative)	t_{STR}	110	72		ns
Write Pulse Width (Negative)	t_{WP}	120	80		ns
Address Setup Time	t_{ADDS}	25	12		ns
Address Hold Time	t_{ADDH}	60	0		ns
Data Setup Time	t_{DS}	60	30		ns
Data Hold Time	t_{DH}	30	0		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND − 0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial IM6551/61I	-40°C to +85°C
Military IM6551/61M	-55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}-2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH1}	I_{OH}=-0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL1}	I_{OL}= 2.0mA			0.45	V
Output Leakage	I_O	$0V \leq V_o \leq V_{CC}$	-1.0		1.0	μA
Supply Current	I_{CC}	$V_{IN}=V_{CC}$		1.0	100	μA
	I_{CC}	V_{CC}=3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V ± 10%, C_L = 50 pF, T_A = Industrial or Military

PARAMETER	SYMBOL	IM6551/61			UNITS
		MIN	TYP	MAX	
Access Time From STR	t_{AC}		240	360	ns
Output Enable Time	t_{EN}		120	180	ns
Output Disable Time	t_{DIS}		120	180	ns
STR Pulse Width (Positive)	t_{STR}	120	60		ns
STR Pulse Width (Negative)	t_{STR}	220	150		ns
Write Pulse Width (Negative)	t_{WP}	240	160		ns
Address Setup Time	t_{ADDS}	50	25		ns
Address Hold Time	t_{ADDH}	120	0		ns
Data Setup Time	t_{DS}	120	60		ns
Data Hold Time	t_{DH}	60	0		ns

SWITCHING WAVEFORMS AND SWITCHING TIME LOAD

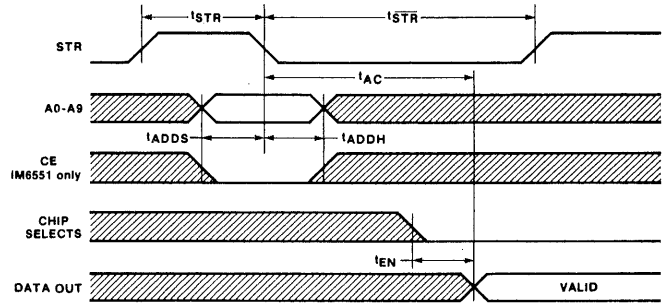


FIGURE 1. READ CYCLE

The IM6551/61 output data latch maintains data when STR returns high.

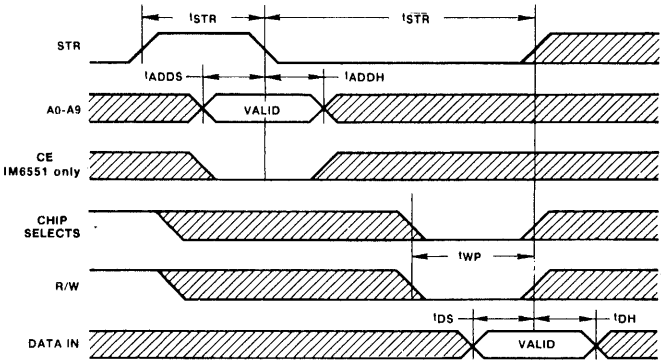


FIGURE 2. WRITE CYCLE

The IM6551/61 perform a write operation when CS1 = CS2 = STR = WE = 0. The write operation is terminated on any positive edge from CHIP SELECTS or STR or WE.

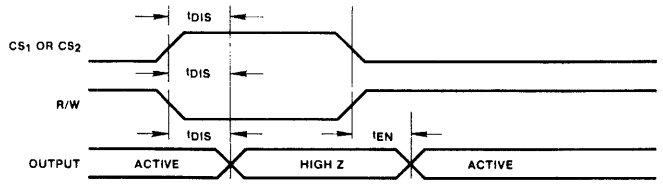


FIGURE 3. OUTPUT ENABLE

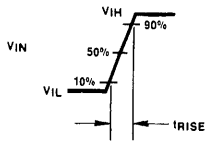
The IM6561 output is high impedance when CS1 or CS2 = 1 or WE = 0. The IM6551 output is high impedance whenever latched CE is high or CS = 1 or WE = 0.

MEMORY FUNCTION TABLE IM6551/61

STR	CS1	CS2**	WE	OPERATION	OUTPUT
0	0	0	0	Write	High Resistance
0*	0	0	1	Read	Memory Data
X	0	1	X	Hold	High Resistance
X	1	0	X	Hold	High Resistance

*Addresses are loaded on chip by the falling edge of STR.

**IM6551 latches CE on the falling edge of STR. Changes in CE while STR is low will not affect the IM6551 operation. The IM6561 does not latch CS2. Changes in CS2 are recognized by the IM6561 at any time.



$t_{rise} = t_{fall} = 20$ ns
DELAY TIMES ARE MEASURED
FROM 50% TO 50%

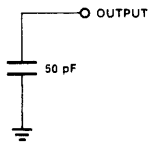


FIGURE 4. SWITCHING TIME WAVEFORMS AND LOAD

2048 BIT BIPOLAR PROGRAMMABLE READ ONLY MEMORY IM5604/IM5624

FEATURES

- Proven Reliable Programming Element
- Programming Element is TTL Processing Compatible—No Extra Steps Required
- Best Available Programming Speed < 1 second for 2048 Bits
- Low Power/Bit < 275μW/Bit
- Good Operating Speed—50 ns Typical Address to Output Access Delay
- DTL/TTL Compatible Inputs and Outputs
- Large Output Drive Capability—16 mA at .45 V
- Resistor Pullup (IM5604) or Active Pullup (IM5624)
- Logical High on Chip Enable Gives High Impedance Output Condition to Allow Wire AND-ing Outputs for Memory Expansion
- Pinout Facilitates Wiring for Expansion From IM5603A/IM5623 1024 Bit to IM5604/IM5624 2048 Bit. Only Pin 14 Differs Between the Two Different Memory Sizes.

GENERAL DESCRIPTION

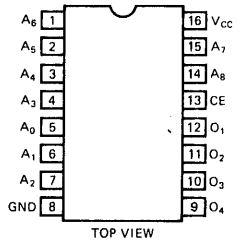
The IM5604/IM5624 is a high speed, electrically programmable, fully decoded 2048 bit read only memory. The organization is 512 words by 4 bits. A high speed chip enable is provided for implementing larger organizations.

Before programming, the memory contains all logic level ZEROS (low voltage state). A logic level ONE (high voltage state) may be electrically programmed into any bit location by following the programming specifications. Programming specifications shown in the IM5603A/IM5623 data sheet are applicable.

APPLICATIONS

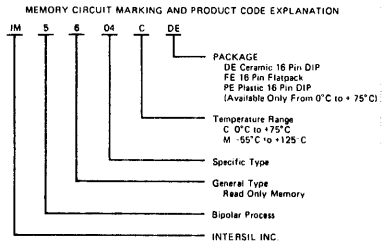
- Random Combinatorial Logic
- Code Conversion
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits, Counter, Registers, RAMs, etc.
- Character Generators
- Decoders or Encoders

CONNECTION DIAGRAM



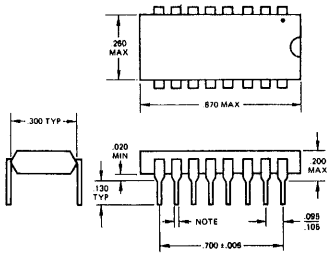
TOP VIEW

ORDERING INFORMATION

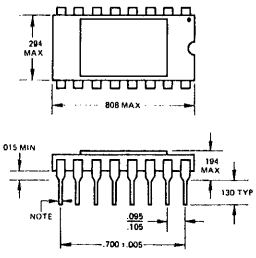


PACKAGE DIMENSIONS

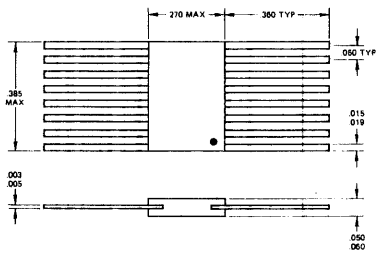
16 LEAD PLASTIC DIP



16 LEAD CERAMIC DIP



16 LEAD FLAT-PACK



NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Storage Temperature	−65°C to +150°C
Input Voltage Applied	−1.5V to +5.5V	Operating Temperature Range*	
Output Voltage Applied	−0.5V to $+V_{CC}$	(IM5604C and IM5624C)	0°C to +75°C
Output Voltage Applied (Programming Only)	28V	(IM5604M and IM5624M)	−55°C to +125°C
Current Into Output (Programming Only)	210 mA		

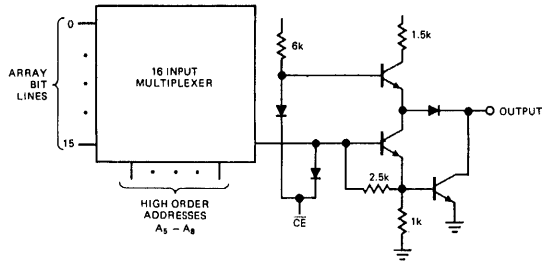
*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

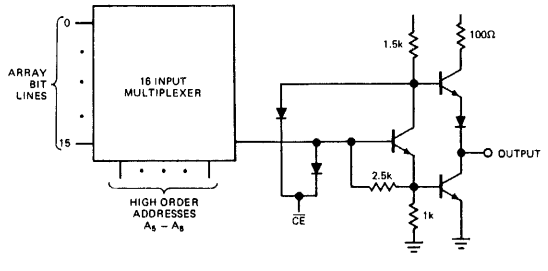
SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C			LIMITS V_{CC} = 5.0V ±10% T = -55°C to +125°C			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
I_{FA}	Address Input Load Current		-0.63	-1.0		-0.63	-1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		-0.63	-1.0		-0.63	-1.0	mA	V_{CE} = 0.4V
I_{RA}	Address Input Leakage Current		5.0	60		5.0	100	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5.0	60		5.0	100	μA	V_{CE} = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA V_{CE} = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8	V	
V_{IH}	Input High Voltage	2.0			2.0			V	
V_C	Input Clamp Voltage		-0.9	-1.5		-0.9	-1.5	V	I_{IN} = -10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5		V	I_{IN} = 1.0 mA
I_{CC}	Power Supply Current			140			140	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1.0	40		<1.0	40	μA	V_O = 5.5V, V_{CE} = 2.4V
I_O (High R State)	Output Leakage Current		<-1.0	-40		<-1.0	-40	μA	V_O = 0.4V, V_{CE} = 2.4V
C_{IN}	Input Capacitance		5.0			5.0		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7.0			7.0		pF	V_O = 2.0V, V_{CC} = 0V
The following are guaranteed characteristics of the output high level state when the chip is enabled (CE = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.									
I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	μA	V_O = 5.5V, V_{CE} = 0.4V
V_{OH} (IM5604)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_O = -0.4 mA
V_{OH} (IM5624)	Output High Voltage	2.4	3.2		2.4	3.2		V	I_O = -1.0 mA (IM5624M) I_O = -2.4 mA (IM5624C)
I_{SC} (IM5604)	Output Short Circuit Current	-1.0	-3.0	-6.0	-1.0	-3.0	-6.0	mA	V_O = 0V
I_{SC} (IM5624)	Output Short Circuit Current	-15	-30	-60	-15	-30	-60	mA	V_O = 0V

NOTE 1: Typical characteristics are for V_{CC} = 5.0V, T_A = 25°C.

OUTPUT STAGE SCHEMATICS



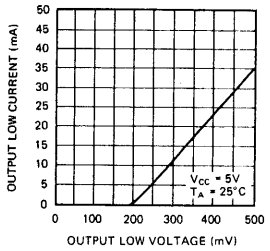
IM5604



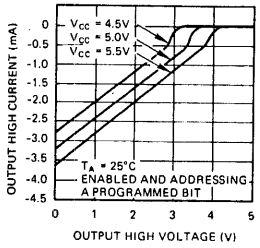
IM5624

TYPICAL DC CHARACTERISTICS

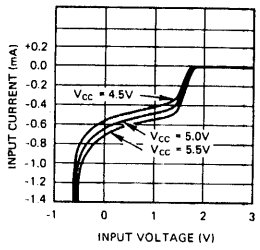
IM5604 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



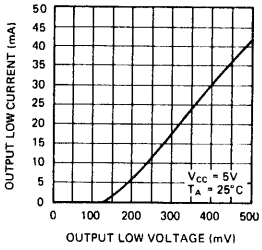
IM5604 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



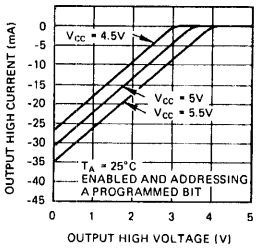
IM5604 OR IM5624 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE



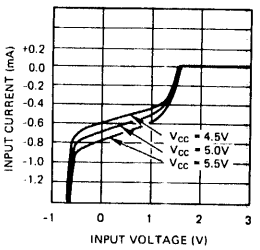
IM5624 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



IM5624 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



IM5604 OR IM5624 ADDRESS INPUT CURRENT VS INPUT VOLTAGE



TRUTH TABLE

ADDRESS INPUTS $A_0 - A_8$	CE	ANY OUTPUT $O_1 - O_4$
Any one of 512 possible addresses	L	H – if the bit uniquely associated with this output and address has been electrically programmed. L – if it has not been programmed.
Any one of 512 possible addresses	H	All outputs are forced to a high impedance state regardless of the address.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

SYMBOL	CHARACTERISTICS	LIMITS		UNITS	CONDITIONS
		TYP	MAX		
t_{AA}	Access Time (Via Address Inputs) (See Figure 9)	50	70	ns	
t_{DIS}	Output Disable Time* (See Figure 10)	20	30	ns	
t_{EN}	Output Enable Time* (See Figure 10)	25	30	ns	For $t_{EN'1'}$ on IM5604 Pull-Up Resistor = 1kΩ

***NOTE:** Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

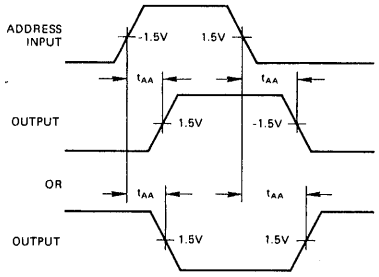


FIGURE 1. ACCESS TIME VIA ADDRESS INPUTS

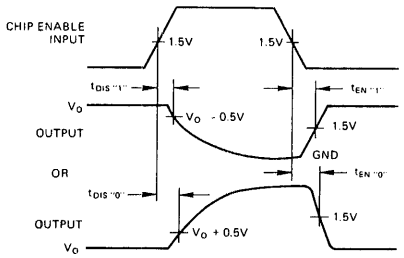


FIGURE 2. OUTPUT ENABLE AND DISABLE TIMES

SWITCHING TIME TEST CONDITIONS

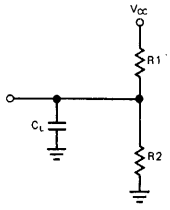


FIGURE 3. OUTPUT LOAD CIRCUIT

SWITCHING PARAMETER	IM5604			IM5624		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{DIS} "1"	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{DIS} "0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{EN} "1"	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{EN} "0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude – 0V to 3V
Rise and Fall Time – 5 ns From 1V to 2V
Frequency – 1 MHz

3½ DIGIT A/D PAIR

8052/7101

FEATURES

- Guaranteed zero reading for 0 volts input
- Auto-zero; auto polarity
- 5pA input current typical
- Single reference voltage
- Latched parallel (full-time) BCD output for LCDs or data busing
- True polarity at zero count for precise null detection
- On-board clock and reference

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7101	0°C to 70°C	40 pin plastic DIP	ICL7101CPL
7101	0°C to 70°C	40 pin ceramic DIP	ICL7101CDL

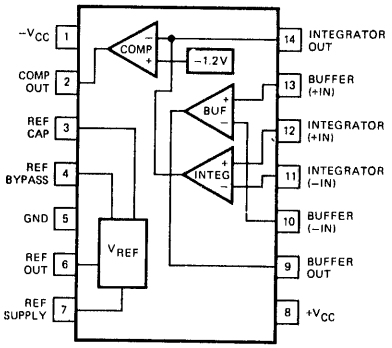
GENERAL DESCRIPTION

The 8052/7101 A/D Pair, with its parallel BCD outputs, is ideally suited for data processing applications or interfacing with 3½-digit Liquid Crystal Displays. No external circuitry is required to demultiplex the information. In addition, it has a "start/reset" input and "busy" output that allows easy synchronization to system requirements. The 8052/7101 provides 4½-digit accuracy in a 3½-digit format with typical system performance like 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift and Linearity to 0.002%.

The 8052/7101 A/D pair also features conversion rates from 10 seconds to 30 per second, making them ideally suited for a wide variety of applications.

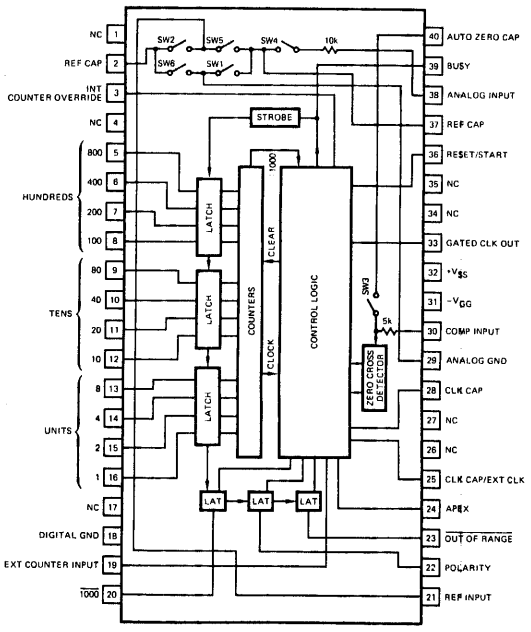
CONNECTION DIAGRAM

8052 Analog Signal Conditioner



CONNECTION DIAGRAM

7101 Digital Processor



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C
8052 ONLY	
Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C
7101 ONLY	
Source Current (I_S)	100mA
Drain Current (I_D)	100mA
Digital Inputs	5mA
V^+ to V^-	25V
Digital Input	V^- to V^+

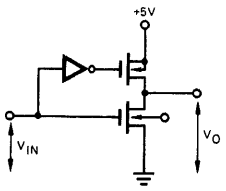
Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

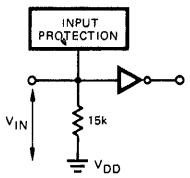
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

7101 ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V$, $V^- = -15V$, $T_A = +25°C$ unless otherwise specified)

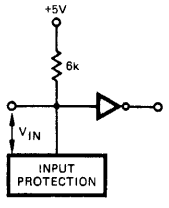
PARAMETER	SYMBOL	CONDITIONS	7101			UNITS
			MIN	TYP	MAX	
Clock Frequency	f_{IN}	C = 1500 pF		20		kHz
External Clock In	I_{INL}	V_{IN} = 0 V		0.35	1.0	mA
External Clock In	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
Reset/Start	I_{INL}	V_{IN} = 0 V		0.8	2.0	mA
Internal Counter Override External Counter Input	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
BCD	V_{OL}	I_{OL} = 1.6 mA		0.25	0.4	V
BCD	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Out-of-Range	V_{OL}	I_{OL} = 3.2 mA		0.25	0.4	V
Out-of-Range	V_{OH}	I_{OH} = 400 μA	2.4	4.5		V
Polarity, Apex, Busy, $\overline{1000}$	V_{OL}	I_{OL} = 0.8 mA		0.25	0.4	
Polarity, Apex, Busy, $\overline{1000}$	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Gated Clockout	V_{OL}	I_{OL} = 0.3 mA		0.25	0.4	V
Gated Clockout	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Switches 1, 3, 4, 5, 6	$R_{DS(ON)}$			400		Ω
Switch 2	$R_{DS(ON)}$			2500		Ω
+5.0 V Supply Current	I_{CC}^+			15	25	mA
−15 V Supply Current	I_{CC}^-			3.0	5.0	mA



Output



External Counter Input
Internal Counter Override



Start/Reset

TYPICAL INPUT/OUTPUT SCHEMATICS

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			UNITS
		MIN	TYP	MAX	
OPERATIONAL AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110		dB
Large Signal Voltage Gain	R_L = 10kΩ V_{OUT} = ±10V	20,000			V/V
Slew Rate			6		V/μs
Unity Gain Bandwidth			1		MHz
Output Short-Circuit Current			20	50	mA
COMPARATOR AMPLIFIER					
Small-Signal Voltage Gain	R_L = 30kΩ		4000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-2.0	-2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.5	1.75	2.0	V
Output Resistance			5		ohms
Temperature Coefficient			40		ppm
Supply Current Total			6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5.0V, V_- = −15V, T_A = +25°C, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7101(1)			UNITS
		MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V	-0.000	±0.000	+0.000	Digital Reading
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.998	+1.000	+1.001	Digital Reading
Linearity over ± Full Scale (error off reading from best straight line)	$-2V \leq V_{in} \leq +2V$		0.1	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.1	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		0.2		Digital
	Full scale = 2.000V		0.05		Count
Leakage Current into Input	V_{in} = 0V		5	30	pA
Zero Reading Drift	V_{in} = 0V $0° \leq T_A \leq 70°C$		1	5	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0° \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		3	15	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 1 clock frequency 20kHz.

CIRCUIT DESCRIPTION

Figure 1 shows a typical circuit for a DVM. A minimum of external components is required since the chips have an on-board clock and a medium-quality (40ppm/°C) internal reference. The circuit also shows the switching required for two scale factors: 2.000V and 200.0mV full scale.

The system uses the time-proven dual-slope integration with all of its advantages, i.e., non-critical components, high rejection of noise and AC signals, non-critical clock frequency and true ratiometric readings. At the same time, it eliminates one of the basic disadvantages of dual-slope conversion: separate positive and negative reference sources. In this system, the negative reference is generated by charging the reference capacitor to the positive reference potential and then switching it into the circuit inverted when a negative reference is required. Due to the very low leakage and charge injection of the FET switches, the positive and negative references track each other to 10μV over a wide temperature range. This assures a very small error between positive and negative scale factor and, thus, excellent linearity from (+) full-scale to (−) full-scale (.002% typical).

The measurement cycle for the 8052/7101 has three phases. These are auto-zero, integrate input, and integrate reference. At the end of a measurement the system automatically reverts to the auto-zero mode until a new measurement is initiated. If an over-load has not occurred in the previous measurement, 10 milliseconds of auto-zero is sufficient to null any offsets to 10μV. At power on, or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value.

Start Conversion

Prior to conversion, the reset-start input must be held low to inhibit conversion (during auto-zero). Conversion is initiated by a positive transition on the start-reset line. (It must therefore return to the low state prior to completion of conversion in order to allow proper auto-zero function.) The positive transition generates a clear pulse which resets all internal logic (counters, etc.) and sets the clock enable, thus initiating the conversion sequence.

Integrate Input

During the first period, switch #4 is closed (all others open), applying the input potential to the buffer input. Since the amplifier offsets are stored on the auto-zero capacitor, the integrator's slope is determined solely by the input voltage. The input voltage is integrated for exactly 1000 counts, thus reaching an integrator output proportional to the integral of the input for a fixed time.

Integrate Reference

At the end of 1000 counts, switch #4 is opened, the polarity flip-flop is set, and the integrate reference period begins. Depending on the polarity, switch #5 or #6 is closed, connecting the buffer input to ground or $2V_{ref}$. This causes the integrator to ramp towards its quiescent (auto-zero) point with a slope proportional to $+V_{ref}$ or $-V_{ref}$. When the integrator crosses its quiescent auto-zero point, the comparator changes state, causing the zero crossing detector to generate a conversion complete signal which inhibits the clock and loads the logic information into the output latches. Switch #5 (or #6) is opened, switches #1, #2, and #3 are closed, and the system returns to a quiescent auto-zero mode, awaiting the next initiate conversion signal. If 2000 counts are received prior to zero crossing, an out-of-range signal is generated which sets the "out-of-range" output and resets the system.

Note 1: Internal reference out ≃ 1.8V, reference input = 1,000 volts for 1.999 volt scale and 100mV for 199.9mV scale.
Note 2: External components shown are suggested for 3 readings/sec.
Note 3: Parallel BCD outputs and other latched outputs are strobed at end of conversion and retain data until completion of next conversion.
Note 4: Start/Reset should remain Low during Auto-Zero. Conversion is initiated by a positive pulse on start pin. (minimum width 100nsec).
Note 5: Component values ±20% typ.

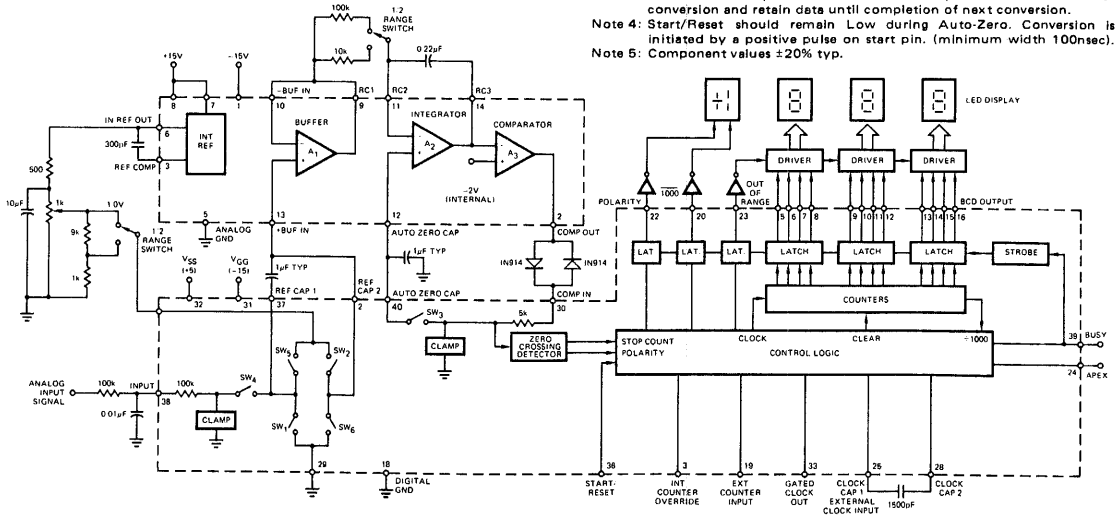


FIGURE 1. 3½ DIGIT A/D CONVERTER FUNCTIONAL DIAGRAM

7101 Digital Processor Controls

Two pins are included on the 7101 that allow the user to externally control the gain of the converter. The first pin, "Internal Counter Override", if held high, will inhibit the carry pulse from the internal counter that switches the converter from signal integrate to reference integrate. As long as this input is high, the converter will remain in the signal integrate mode. At the same time, it enables the other pin, External Counter Input, to supply this transition pulse from external sources. One technique for changing the gain of the system would be to hold "Internal Counter Override" high through the first N carry pulses. This would increase the signal integrate time by a factor of N+1 and, thus, the sensitivity of the system by N+1. Since the number of suppressed pulses could be controlled digitally, the system could accomodate signals from ±2.000V to ±200.0mV (or lower, if time permits) without changing the external analog scale factor components. By using more complex external logic and both inputs, the user could digitally set offset (tare) and scale factor to convert voltages to physical units such as "degrees centigrade", "pounds", or "feet".

A "BUSY" pin is provided which permits interrogating the 8052/7101 to determine the status of the conversion. During the signal integrate and reference integrate periods, the "busy" line is high until the conversion is complete, at which time "busy" line goes low. This transition can be used to signal "new data available".

The "Apex" pin provides a digital signal which goes high during the reference integrate period.

"OUT-OF-RANGE" is indicated by a latched "low" on pin 23 for counts over 2000. The BCD digital values are "high" (true), except $\overline{1000}$ which is "low".

A positive polarity of the analog input signal is indicated by a "high" state at the output of the "polarity" latch on pin 22.

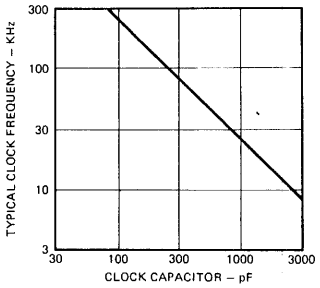


FIGURE 2.

The 7101 has an internal clock which requires a single capacitor between Pins 25 and 28 to operate. Figure 2 shows the typical capacitor value required to give the desired frequency.

During auto-zero, the clock is internally gated-off with Pin 28 high and Pin 25 low. When "start-reset" goes high, starting a measurement cycle, the clock starts counting with Pins 25 and 28 immediately changing phase. The counting continues until the end of the measurement cycle, at which time the clock is returned to its auto-zero condition.

In a typical application where visual readings are required, three readings per second is near the optimum speed. Faster readings make it difficult to resolve individual readings, while at slower rates the reader has to wait too long between measurements. In this application, 40% of the time (133mS) could be allocated to auto-zero and 60% (200mS) to signal and reference integrate. Since a measurement cycle consists of 3,000 clock pulses maximum, this dictates a clock frequency of 15kHz. Also, since the dual-slope technique of A/D conversion is not first-order dependent on clock frequency, the ±20% variation of clock frequency from unit-to-unit would result in no measurable error. However, in some applications, a more precise clock frequency would be desired. For instance, if precise rejection of 60Hz is required, the signal integrate phase (1,000 counts) would have to contain an integral number of 60Hz periods. For these applications, an external clock can be used by deleting the capacitor and connecting the external clock to Pin 25. However, if the clock is run asynchronously with start/reset, there will be one clock pulse of uncertainty in the integrate signal time, depending on where in the clock pulse period the start/reset went high. This will show up as one count of noise for signal near full-scale. This noise or jitter can be avoided by synchronizing the start/reset pulse to the negative-going edge of the external clock. Pin 33, Gated Clock Out, is a buffered output of the clock (internal or external) that is off (low) during auto-zero and in phase with Pin 25 during measurement.

Component Selection

Except for the reference voltage, none of the component values are first order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance, the reference capacitor and auto-zero capacitor are each shown as 1.0μfd. These relatively large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7101.

The ratio of integrating resistor and capacitor is selected to give 9-volt swing for full-scale inputs. This is a compromise between possibly saturating the integrator (at ±14V) due to tolerance build-up between the resistor, capacitor, and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again, the .22μfd value for the integrating capacitor is selected for PC board considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating capacitor is low dielectric absorption. A polypropylene capacitor gave excellent results. In fact, a good test for dielectric absorption is to use the capacitor in this circuit with the input tied to reference. This ratiometric condition should read 1.000 and any deviation . probably due to dielectric absorption. In this ratiometric condition, a polycarbonate capacitor contributed an error of approximately 0.8 digit, polystyrene about 0.3 digit, and polypropylene less than 0.05 digit. The increased T.C. of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

The back-to-back diodes on the comparator output are recommended in the 200.0mV range to reduce the noise effects. In the normal operating mode, they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero capacitor. At start-up or recovery from an overload, their impedance is low to large signals so the capacitor can be charged in one auto-zero cycle. If only the 2.000V range is used, a 100k resistor in place of the back-to-back diodes is adequate for noise effects.

Maximum Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period), half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash 1 on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate **anticipation** errors that greatly exceed the 3μS **delay** error. Also, it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitor. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

APPLICATIONS

8052/7101 3½ Digit LCD DPM/DVM

Figure 3 illustrates an application where the 8052/7101 interfaces with a Liquid Crystal Display. The CD4054 and CD4055s are Liquid Crystal Display Drivers (4-segment and 7-segment, respectively) which provide the level shifting (up to $30V_{p-p}$ at $V_{DD}-V_{EE}$ = 15V) necessary to drive the LCD. Overrange is indicated by a special character. If blanking of any part of the display is required on overload, Pin 23 (7101) can be used to drive Pin 7 on those display drivers via an inverter and level shift such as CD4009 or 74C903 or another CD4054. Display applications requiring a plus sign rather than a blank indication for positive analog input levels (i.e., +1.999 versus 1.999) need to invert the "polarity" logic output level which is normally high for positive analog input signals.

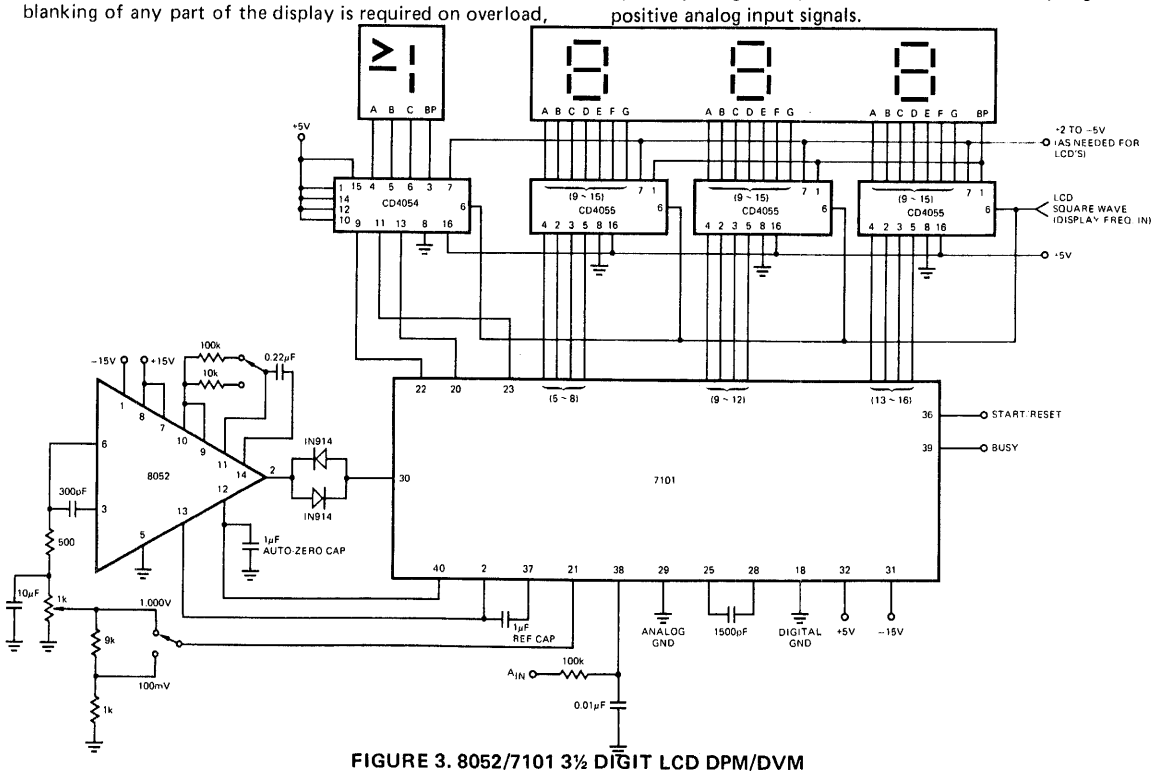


FIGURE 3. 8052/7101 3½ DIGIT LCD DPM/DVM

8052/7101/6100/6101 Set

The circuit in Figure 4 interfaces the 8052/7101 A-to-D converter chip set to an IM6100* microprocessor, using the 6101* Parallel Interface Element. Hex Tri-state Buffers (e.g., MM80C95*) are used to control bus access from the 7101 during read operations.

Conversion is initiated by activating the WRITE 1 line (positive going). The converter pair will then convert the analog input to digital form, and latch the data in the 7101. The busy line will go low as the the conversion ends, and this transition is sensed by the SENSE 1 line, triggering an interrupt. The interrupt routine should read the 12-line data word, and then the polarity, $\overline{1000}$ and out-of-range lines.

Sufficient time must be allowed for the auto-zero loop to settle before retriggering a conversion. Ten milliseconds of auto-zero is sufficient to null any offsets to 10 microvolts. At power-on or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value. This time delay may be implemented conveniently using the IM6102 (Memory Extender/Time Delay Device).

Some skeletal service routines for this connection are given on page 7 and 8.

*References:
Intersil IM6100 CMOS 12-bit Microprocessor
Intersil IM6101 Parallel Interface Element
National MM80C95 Hex CMOS Tri-State Buffers

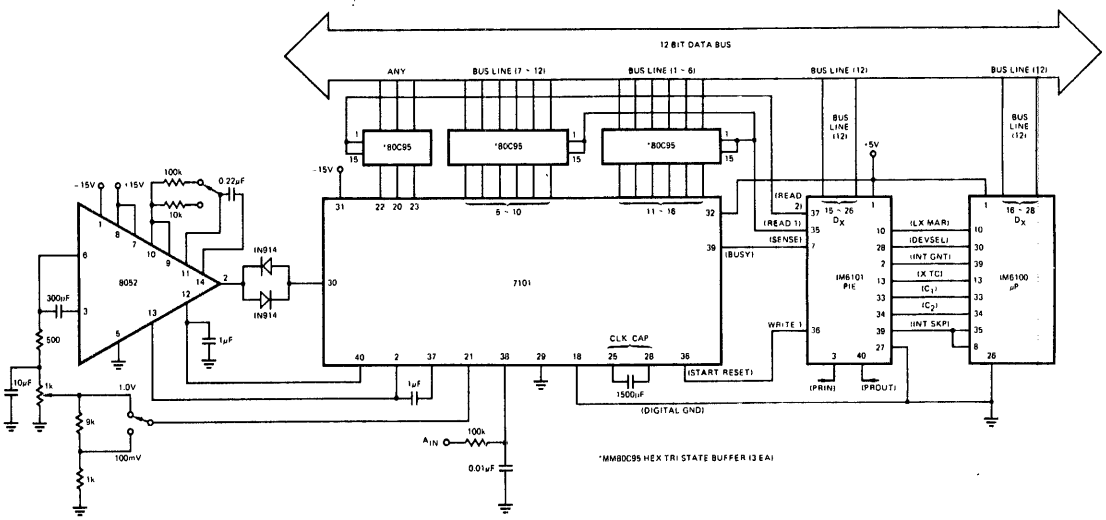


FIGURE 4. 3½ DIGIT PARALLEL BCD DATA ACQUISITION SYSTEM

8052/7101/6100/6101 APPLICATION PROGRAM

A possible set-up and service routine for the connection is given below.

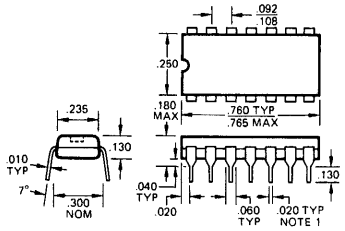
```
/ASSUME PIE SELECT IS SET TO 54, INTERRUPT VECTOR TO 2000
        (OCTAL)
/INITIALIZE ROUTINE: SET-UP FOR NO INTERRUPT

1200    7200            CLA
1201    1240            TAD SSCRA
1202    6545            WCRA 54         /SET-UP CONTROL REGISTER A
1203    7200            CLA
1204    1241            TAD SSCRB
1205    6555            WCRB 54         /SET-UP CONTROL REGISTER B
1206    7200            CLA
1207    1242            TAD SSVV
1210    6556            WVR 54          /SET-UP VECTOR REGISTER

1220    0000  CONVERT,  Ø               /INITIATE CONVERSION SUBROUTINE
1221    1243            TAD SSCRAI
```

8052/7101/6100/6101 APPLICATION PROGRAM (CON'T)

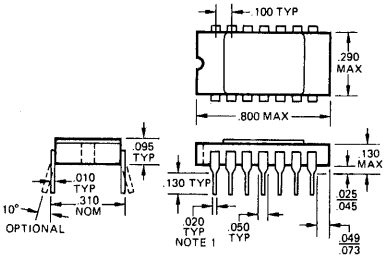
```
1222    6545            WCRA 54             /SET-UP CONTROL REGISTER A
1223    6541            WRITE1 54           /THE WRITE PULSE STARTS CONVERSION

1224    5620            JMP I CONVERT       /RETURN

1240    0040    SSCRA,  0040                /WP 1 SET HI, IE1 SET LO
1241    0000    SCRRB,  0000                /SL1, SP1 SET LP, NEGATIVE EDGE SENSE
1242    2000    SSVV,   2000                /VECTOR ADDRESS
1243    0041    SSCRAI, 0041                /WPI SET HI, IE1 SET HI

0000    0000    INTRPT, Ø                   /ENTRY POINT FOR INTERRUPT
0001    6002            IOF                 /DISABLE INTERRUPT, JUMP TO VECTOR ADDRESS

0140    0000    AD1,    Ø                   /FIRST WORD OF DATA
0141    0000    AD2,    Ø                   /SECOND WORD OF DATA
0160    0000    TEMP1,  Ø                   /TEMPORARY STORAGE

2000    5210    VV,     JMP ATOD            /JUMP TO SERVICE POINT

2010    3160    ATOD,   DCA TEMP1           /SAVE AC
2011    6540            READ1 54            /READ BCD LINES
2012    3140            DCA AD1             /AND STORE
2013    6550            READ2 54            /READ POLARITY, 1000, AND OVERRANGE
2014    7040            CMA                 /COMPLEMENT TO THE TRUE
2015    3141            DCA AD2             /AND STORE
/       – –     – – –   – – – –             /ANY OTHER WORK
2020    1160            TAD TEMP1           /RESTORE AC
2021    6001            ION                 /RESTORE INTERRUPT
2022    5400            JMP I INTRPT        /RETURN
```

PACKAGE DIMENSIONS

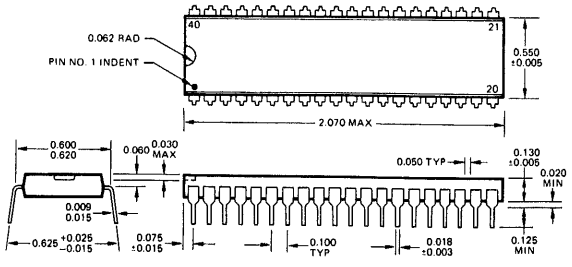
14 Pin Plastic Dual-In-Line Package



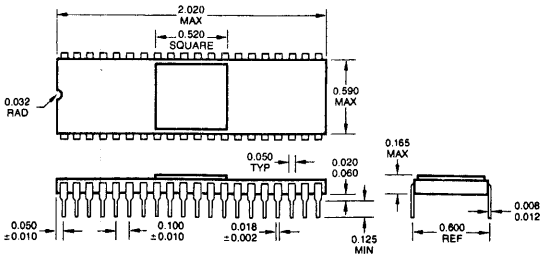
14 Pin Ceramic Dual-In-Line Package



40 Pin Plastic Dual-In-Line Package



40 Pin Ceramic Dual-In-Line Package



PRECISION PAIR FOR A-D CONVERTERS

4½ DIGIT PAIR 8052A/7103A 3½ DIGIT PAIR 8052/7103

FEATURES

- Accuracy guaranteed to ±1 count over entire ±20,000 counts (8052A/7103A)
- Guaranteed zero reading for 0 volts input
- 5pA input current typical
- True polarity at zero count for precise null detection
- Single reference voltage required
- Over-range and under-range signals available for auto-ranging capability
- All outputs TTL compatible
- Medium quality reference (40ppm typical) on board
- Blinking display gives visual indication of over-range
- Six auxillary inputs/outputs are available for interfacing to UARTS, Microprocessors or other complex circuitry

GENERAL DESCRIPTION

The 8052A/7103A with its multiplexed BCD outputs and digit drivers is ideally suited for the visual display DVM/DPM market. Accuracy is outstanding with performance like: 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift; linearity of 0.002%; scale factor temperature coefficients of 3ppm/°C (with external reference). The system uses the time-proven dual-slope integration with all its advantages, i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency, almost perfect differential linearity and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the 8052A/7103A pairs, critical board layout is no longer required to give low charge injection by the switches and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuit.

The 8052/7103 (3½ digit pair) features conversion rates from 1 measurement every 10 seconds to 30/second, making them ideally suited for a wide variety of applications.

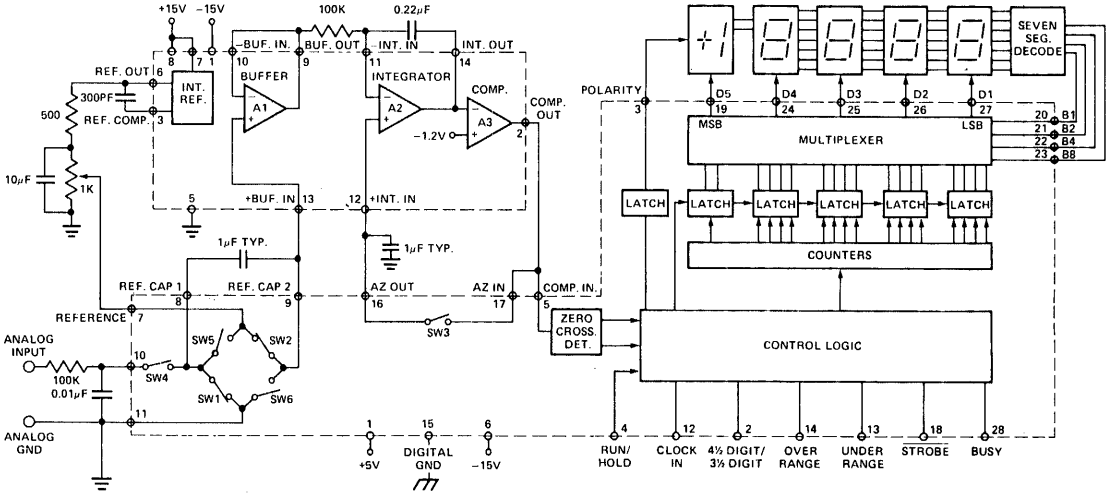


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

3½ Digit Pair

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7103	0°C to 70°C	28 pin plastic DIP	ICL7103CPI
7103	0°C to 70°C	28 pin ceramic DIP	ICL7103CDI

4½ Digit Pair

Part	Temp. Range	Package	Order Number
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
7103A	0°C to 70°C	28 pin plastic DIP	ICL7103ACPI
7103A	0°C to 70°C	28 pin ceramic DIP	ICL7103ACDI

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C

8052, 8052A

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

7103, 7103A

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Digital Inputs	5 mA
V^+ to V^-	25V
Digital Input to V^+	V^- to V^+
Digital Input to V^-	V^+ to V^-

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7103(1)			8052A/7103A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 2.000V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading (3)	$V_{in} \equiv V_{Ref.}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-2V \leqslant V_{in} \leqslant +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \cong +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV Full scale = 2.000V		20 50			30		μV
Leakage Current at Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \leqslant T_A \leqslant 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 3 clock frequency 12 kHz. Pin 2 7103 connected to Gnd.

(2) Tested in 4½ digit (20,000 count) circuit shown in Fig. 3 clock frequency 120 kHz. Pin 2 7103A open.

(3) Tested with a low dielectric absorbtion integrating capacitor. See Component Selection Section.

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
Supply Current Total			6	12		6	12	mA

*This is the only component that causes error in dual-slope converter.

7103 AND 7103A ELECTRICAL CHARACTERISTICS (V^+ = +5.0, V^- = −15V, Ta = 25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS	Clock In, Run/Hold, 4½/3½	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.2 .1	.6 10	mA μA
	Comp. In	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.1 .1	10 10	μA μA
OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5 Busy, Strobe, Over-range, Under-range Polarity	V_{OL} V_{OH} V_{OH}	I_{OL} = 1.6ma I_{OH} = −1mA I_{OH} = −10μA	 2.4 4.9	.25 4.2 4.99	.40	V V V
SWITCH	Switches 1, 3, 4, 5, 6 Switch 2 Switch Leakage (All)	$R_{DS\ ON}$ $R_{DS\ ON}$ $I_{D\ OFF}$		 1200	400 2		Ω Ω pA
SUPPLY	+5V Supply Current −15V Supply Current	I_{CC+} I_{CC-}			20 4	30 6	mA mA

THEORY OF OPERATION

Figure 1 shows a function diagram for an A/D converter using the 8052/7103 pair. In this circuit, each measurement cycle is divided into four equal parts. The first part, phase 1, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second part, Phase 2, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final part, reference integrate, includes phases 3 & 4. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is porportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

1. Low Charge Injection.

During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8052/7103 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. Junction FET Op Amps.

Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakage contributes less than 2μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would more than swamp out any improvement.

3. Zero-Crossing Flip Flop.

The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

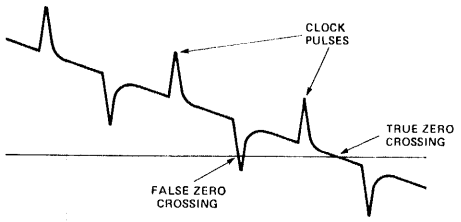


FIGURE 2. INTEGRATOR OUTPUT NEAR ZERO-CROSSING

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to disable the counter for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2 so that true ratiometric readings are possible.

APPLICATIONS

Specific Circuits Using the 8052A/7103A

Figure 3 shows the complete circuit for a 4½ digit (±2.000V) full scale) A/D with LED readout using the internal reference of the 8052A. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower or the filter deleted completely. The ½ digit LED is driven off of the 7 segment decoder with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

A voltage translation network is connected between the comparator output of the 8052A and the auto-zero input of the 7103A. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 7103A logic (+2.5V) while the auto-cap is being charged to V_{REF} (+1.0 volts for a 2.000V instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature of the network is that it holds the source of switch 3 to ≈ +4V during the integrate and deintegrate cycles of positive input voltages. During this time, the comparator output is clamped by an internal diode on the 7103A to ≈ +5.7 volts. Since the gate of switch 3 is at +5 volts for this off condition, the +1 volt Vgs of the FET assures the switch is off to the 1 or 2 pA leakage level. Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle.

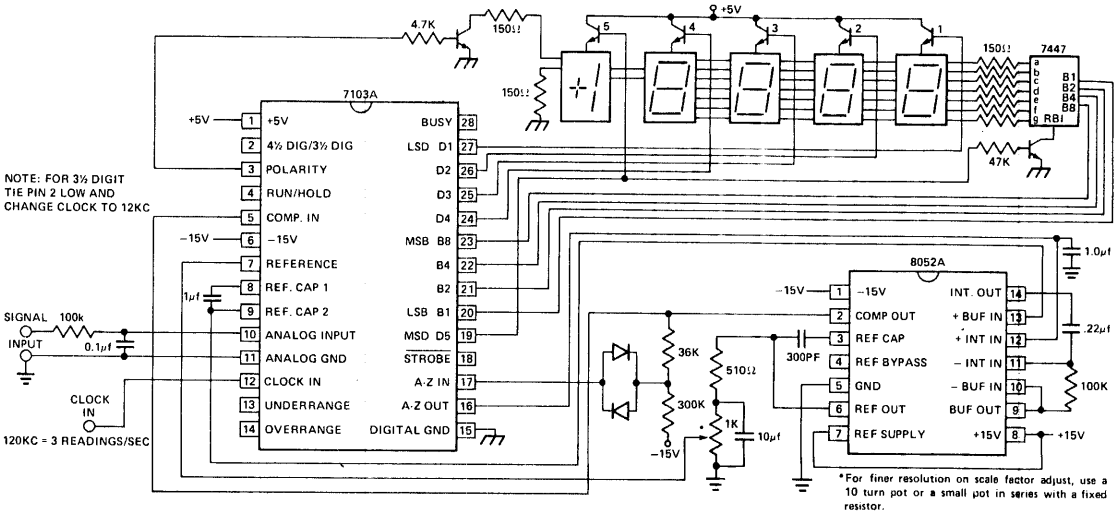


FIGURE 3. 8052A/7103A 4½ DIGIT A-D CONVERTER

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7103. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22μF value for the integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, up to 500kHz clock rate may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

AUXILIARY INPUTS/OUTPUTS

The 7103 and 7103A include several pins that allow them to operate conveniently in more sophisticated systems. These include:

1. 4½/3½ (Pin 2). When high (or open) the internal counter operates as a full 4½ decade counter with a complete measurement cycle requiring 40,000 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4000 clock pulses. All 5 digit drivers are active in either case with each digit lasting 200 counts with pin 2 high (4½ digit) and 20 counts for pin 2 low (3½ digit). The only difference between 7103A and 7103 is that they were tested with this pin high and low respectively. Actually, most 7103 will operate satisfactorily in a 4½ digit application. They simply have not received the more complex testing required to prove it.

2. Run/Hold (Pin 4). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,000/4,000 clock pulses. If taken low, the converter will continue the full measurement cycle that it is in and then hold this reading as long as pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with 10,000/1,000 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,000/4,000 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is in. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 100/10 counts after the end of this cycle. Thus, if Run/Hold is low and has been low for at least 100/10 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. $\overline{\text{Strobe}}$ (Pin 18). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{Strobe}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 100/10 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 200/20 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{Strobe}}$ pulse goes negative for ½ clock pulse width. Similarly, after 200/20 clock pulses, digit 4 goes high and 100/10 pulses later the $\overline{\text{Strobe}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{Strobe}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{Strobe}}$ pulses will be sent until a new measurement is available.

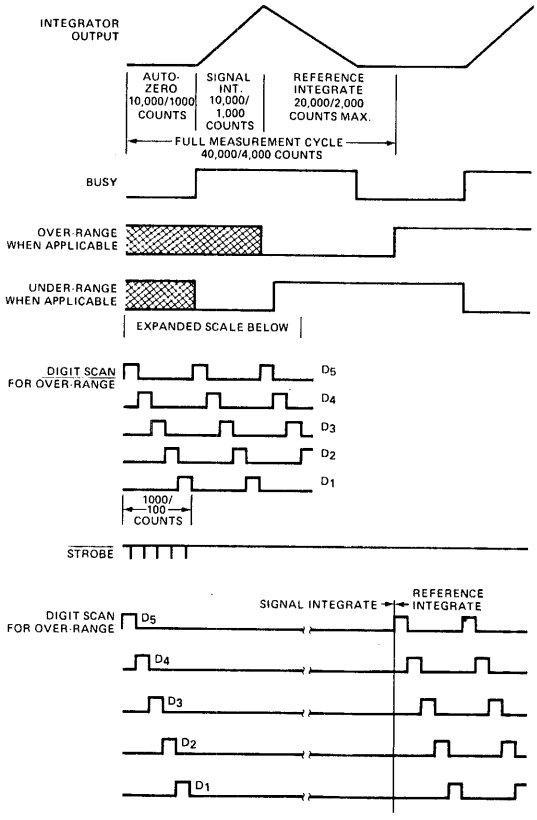


FIGURE 4. TIMING DIAGRAM

4. Busy (Pin 28). Busy goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., transferred during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered a $\overline{A\text{-}Z}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received (as mentioned previously there is one NO count pulse in each reference integrate (cycle).

5. Over-range (Pin 14). This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of Busy and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

6. Under-range (Pin 13). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of busy (if the new reading is 1800/180 or less) and is reset at the beginning of signal integrate of the next reading.

7. Polarity (Pin 3). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

8. Digit Drives (Pins 19, 24, 25, 26 and 27). The digit drives are a positive going signal that each last for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3½ digit mode. The scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This gives a blinking display as a visual indication of over-range.

9. BCD (pins 20, 21, 22 and 23). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver.

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 5 shows a very simple interface between a free-running 8052A/7103A and a UART. The five $\overline{\text{Strobe}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative.

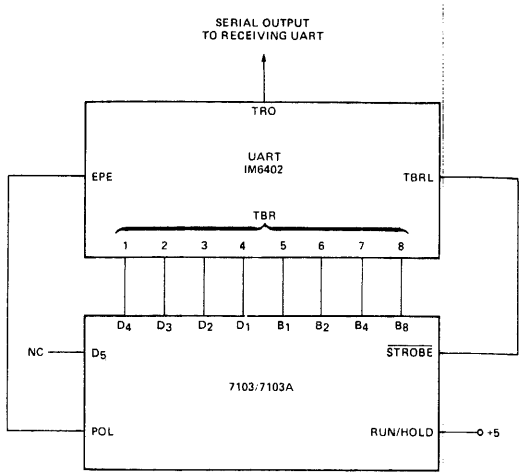


FIGURE 5. SIMPLE 7103/7103A TO UART INTERFACE

A more complex arrangement is shown in Fig. 6. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again $\overline{\text{Strobe}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

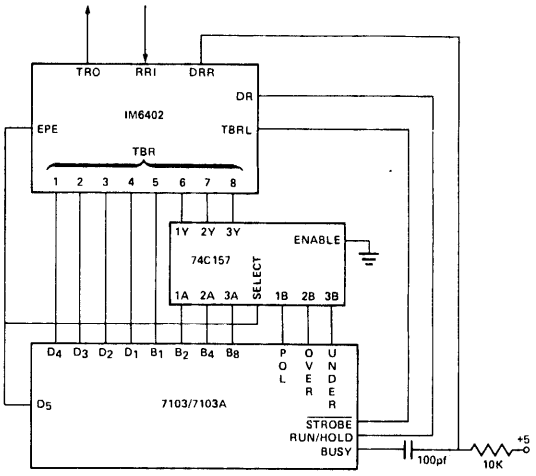


FIGURE 6. COMPLEX 7103/7103A TO UART INTERFACE

Circuits for the 7103/7103A to interface directly with three popular microprocessors are shown in Figures 7, 8 and 9. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080 and the MC6800 with 8 bits words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

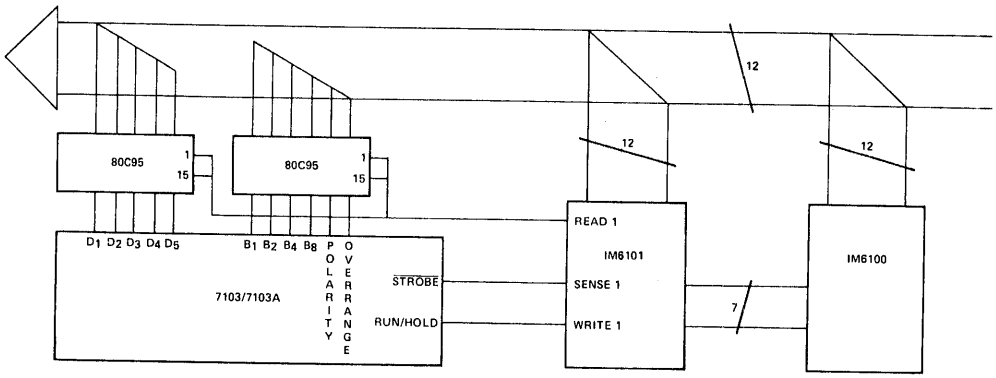


FIGURE 7. IM6100 TO 7103/7103A INTERFACE

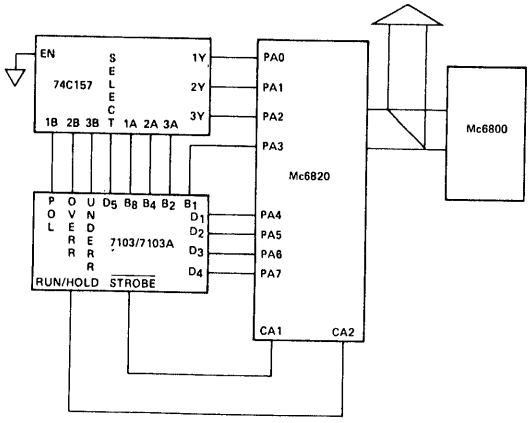


FIGURE 8. Mc6800 TO 7103/7103A INTERFACE

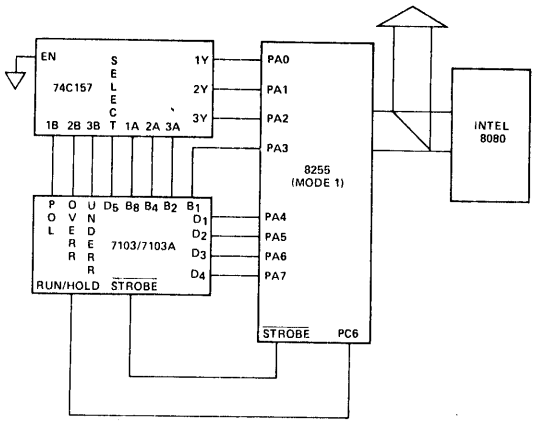
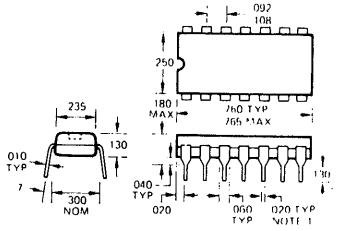


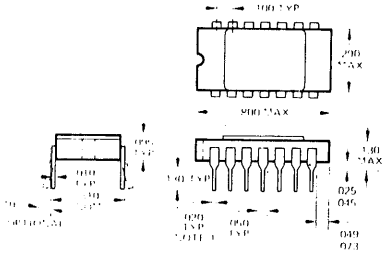
FIGURE 9. INTEL 8080 TO 7103/7103A INTERFACE

PACKAGE DIMENSIONS

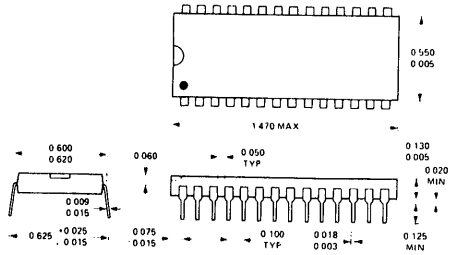
14 Pin Plastic Dual-In-Line Package



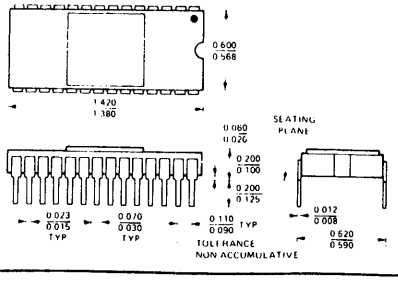
14 Pin Ceramic Dual-In-Line Package



28 Pin Plastic Dual-In-Line Package



28 Pin Ceramic Dual-In-Line Package



LOW BATTERY VOLTAGE INDICATOR

ICM7201

FEATURES

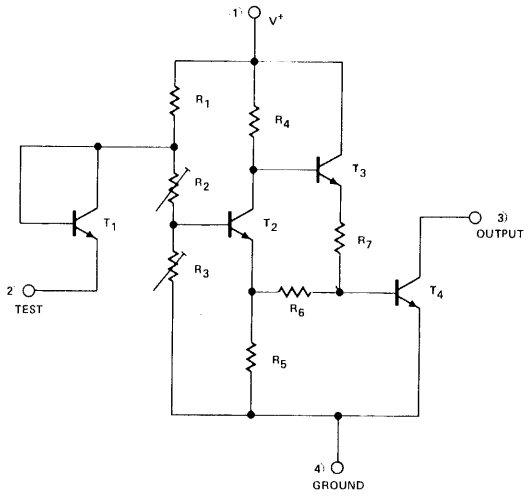
- Accurate voltage indication: $2.9V \leqslant V_{TH} \leqslant 3.3V$
- Simple to use: requires only an additional LED lamp for complete system
- Low power consumption: 4.5 mW at $V_{SUPPLY} = 3.6V$
- Good noise rejection – 0.2V of hysteresis for device threshold voltage

DESCRIPTION

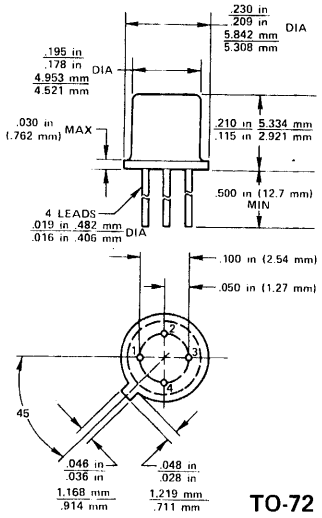
The ICM7201 is intended to be used in battery operated systems which require an indication of when the battery stack has depleted to a fixed voltage. When used with an LED lamp the lamp will light at voltages below 2.9 volts. At voltages above 2.9 volts the lamp may be lit by connecting the "TEST" terminal to the "GROUND" terminal.

The ICM7201 has hysteresis designed into its threshold voltage trigger point so that the lamp will not flicker with supply voltage noise and also will not gradually be turned on at the trigger voltage. Under all normal circumstances the lamp will either be fully on or fully off.

SCHEMATIC ICM7201

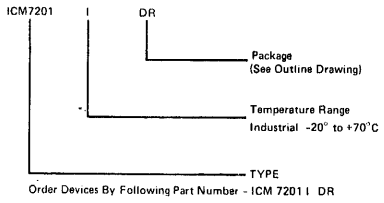


PACKAGE DIMENSIONS



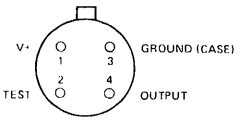
TO-72

ORDERING INFORMATION



Order Devices By Following Part Number - ICM 7201 I DR

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS:

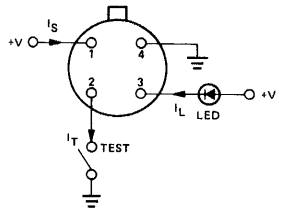
Power Dissipation		100 mW
Maximum Supply Voltage		5.5V
Maximum Output Current	Note 1	100 mA
Operating Temperature		−20°C to +70°C
Storage Temperature		−55°C to +125°C

TYPICAL OPERATING CHARACTERISTICS: T_A = 25°C , Test Circuit unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_S	Bulb off, V_S = +3.6V		1.2	2	mA
Trigger Voltage	V_T		2.9	3.1	3.3	V
Temperature Coefficient of Trigger Voltage	T_C			−12		mV/°C
Hysteresis Voltage	V_H			0.2		V
Lamp Current at Trigger Voltage	I_L	V_F of LED approx 1.7V V_S = 3.1V		15		mA
Test Current	I_T	V_{SUPPLY} = 3.6V		0.5	1.5	mA

NOTE 1: At high supply voltages (approaching 5 volts) it is necessary to include a current limiting resistor in series with the LED light bulb to limit the output current to 100 mA maximum.

TEST CIRCUIT

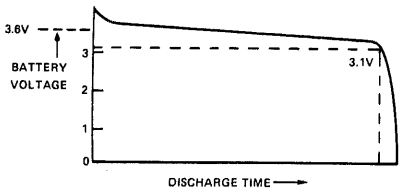


APPLICATION NOTES

The ICM7201 is designed to provide adequate warning that a 3 cell nickel-cadmium battery stack is depleted.

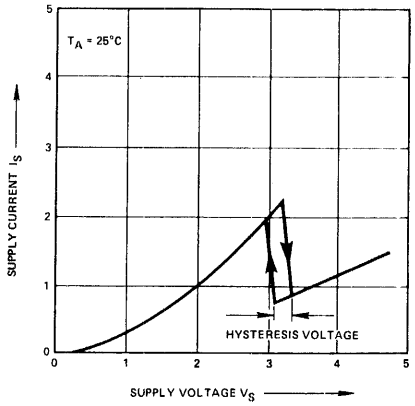
The nickel-cadmium battery maintains an almost constant voltage (3.6V) during approximately 95% of its discharge and then the voltage collapses rapidly. If a higher nominal threshold voltage had been selected for the ICM7201 this would restrict the useful temperature range with a 3 cell Nickel-Cadmium stack because of the −12 mV/°C temperature coefficient. On the other hand if a very low threshold voltage were chosen the extremely rapid battery discharge at low voltages would result in an insufficient warning signal time.

Ni-Cad 3-CELL DISCHARGE



TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OPTIONS

The ICM7201 can be supplied with maximum supply voltage options up to 15 volts and threshold voltage ranges starting from 1.8 volts. For further information contact the factory.

DCMOS RELIABILITY REPORT

DCMOS RAM RELIABILITY REPORT—IM6523, IM6508, IM6100

The purpose of this report is to present the reliability program to control and evaluate Intersil's Silicon Gate Complementary MOS Technology. Extensive reliability characterization has been performed on the following CMOS devices:

1. IM-6523, 256x1 Asynchronous RAM
2. IM-6508, 1024x1 Synchronous RAM
3. IM-6100, Microprocessor

RELIABILITY PROGRAM

Intersil has an established program to qualify, monitor, and perform failure analysis on products, as required, to ensure a high standard of reliability for various applications.

During the design phase of a new product, Reliability determines and isolates failure modes by submitting samples from each processed run to accelerated evaluation tests. Once the failure mechanisms are identified, corrective action is initiated at processing, manufacturing, or final test to ensure reliability of product.

To monitor the effectiveness of instituted corrective action, Reliability receives samples from processed runs and submits those to extended life testing at elevated temperatures. All runs have lot traceability, and records maintained, which are kept on file providing complete historical data from processing to eventual extended life testing. Traceability to wafer run number is maintained throughout manufacturing.

All failures which occur during reliability evaluation are processed through Intersil's Failure Analysis Laboratory, which is equipped to perform electrical testing, bench test analysis, SEM, micromanipulator probing, optical inspection up to 1000X, microsectioning, and chemical analysis.

TABLE I
INTERSIL 100% PROCESSING

PROCESSING STEP	CONDITIONS	INTERSIL SPEC NO.	MIL-STD-883A
Pre-Cap Visual	Class B	QAP-213	Method 2010.2
Stabilization Bake	150°C 24 hr. Min.	FPS-107	Method 1008.1 Cond. C
Temperature Cycle	−65°C to +150°C 10 Cycles	FPS-101	Method 1010.1 Cond. C
Centrifuge	30,000G Y1* Axis	FPS-110	Method 2001.1 Cond. E
Hermeticity			
Fine Leak	Helium 5 x 10^{-7} cc/sec	FPS-109	Method 1014.1 Cond. A or B
Gross Leak	Fluorocarbon	FPS-104	Method 1014.1 Cond. C1
Final Electrical			Per Applicable Spec.

*Packages to 24 leads (>24 leads, 10,000G).

i38510 RELIABILITY PROGRAM

Intersil's in-house reliability program, i38510, offers as standard processing SEM, positive traceability, MIL-STD-883 Level B processing and MIL-M-38510 controls (reference data sheet "i38510 Reliability Program," dated July, 1974).

MEAN-LIFE EVALUATION

Mean-life evaluation is achieved by selecting random samples from finished goods on a periodic basis. These represent standard production parts, which passed all 100% inspections (table I) and Group A quality conformance. High temperature operating life tests are performed under accelerated conditions to reduce testing time and to speed up potential failure mechanisms. Failure analysis is routinely performed on all rejects to assure that results are pertinent and provide timely corrective action. Details of life test results are shown in Table II.

These tables consider the following two categories of failures:

Category 1: **Operable Failure**
These devices have characteristics which have changed according to our data sheet specifications, but still function normally.

Category 2: **Catastrophic Failure**
Devices with catastrophic failures, which would fail to perform the expected logical functions.

TABLE II
SUMMARY LIFE TEST/STORAGE DATA

DEVICE TYPE	year of mfg.	TEST	SAMPLE SIZE	REJECTS		DEVICE HRS. x 10^3
				CATASTROPHIC	OPERABLE	
6523	1973	Op. Life + 125°C + 5V	201	0	0	236.0
6523	1974	Op. Life + 125°C + 5V	332	1	3	1,352.0
6523	1975	Op. Life + 125°C + 5V	94	0	0	93.0
6523		TOTAL	627	1	3	1,681.0
6508	1974	Op. Life + 125°C + 5V	36	0	0	69.0
6508	1975	Op. Life + 125°C + 5V	485	0	2	637.0
6508	1975	Op. Life + 125°C + 10V	37	0	0	67.0
6508	1975	Storage + 150°C	65	0	0	65.0
6508	1975	Dynamic Life + 125°C + 5V	25	0	0	25.0
6508		TOTAL	668	0	2	863.0
6100	1975	Op. Life + 125°C + 5V	30	0	1	57.0

TABLE III
FAILURE RATE CALCULATIONS

DEVICE	REJECTS		EQUIV. DEVICE HRS. @ + 55°C x 10^6	F/R %/1K HRS. @ 60% CONFIDENCE
	A*	B**		
6523	1		16.81	.012
6508	0		8.38	.011
6100	0		.57	.160
	1		25.76	.008
6523		4	16.81	.031
6508		2	8.38	.038
6100		1	.57	.350
		7	25.76	.033

*A = Catastrophic

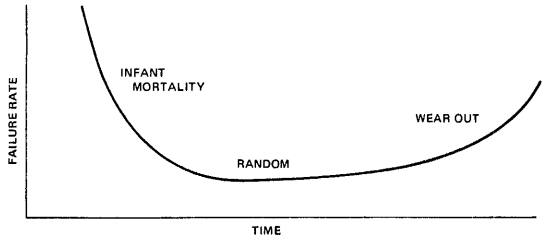
**B = Catastrophic + Operable

The above calculations are based on the following:

1. 10:1 acceleration factor for + 125°C Op. Life and Storage Life @ + 150°C to + 55°C.
2. No weight given to infant mortalities (i.e. failures at or below 168 hours of test time).
3. Reference MIL-STD-690A. Graph for F/R at 60% confidence level.

It should be noted that of the 7 rejects shown, only one was catastrophic. Therefore, our failure rate of 0.008% at 60% confidence level should be used to represent actual field use at + 55°C.

FAILURE MECHANISMS
FIGURE 1



The above curve represents the typical failure rate pattern which can be expected from any group of devices under test. It shows three major regions which concern the reliability engineer; infant mortality, random failures and wear out.

Each of the three areas of the curve have their own specific failure mechanisms and can be described as follows:

a. **Ionic Contamination** (sodium ions, etc.)
This has been one of the more serious problems in MOS manufacturing. Generally, contamination is mobile positive charges trapped within the gate oxide causing a threshold voltage drift. N-Channel is more susceptible than P-Channel as the mobile ions are pushed into the gate region due to the direction of the electrostatic field (see Figure 2).

FIGURE 2

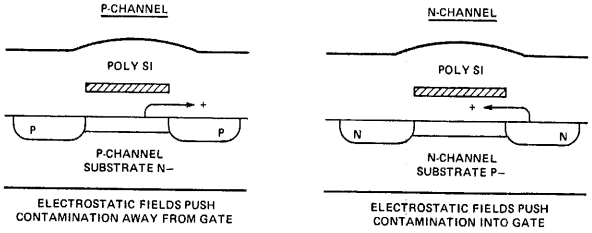
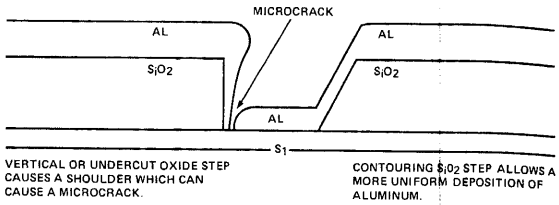


FIGURE 3



The ionic contamination phenomenon is detected during the infant mortality region by high temperature bias testing. Also, the silicon gate process allows the device to be subjected to high temperature gettering, which cleans the oxide and prevents further precaution, each wafer run is monitored for C-V drift by Quality Control.

b. **Polarization**
Polarization is another drift phenomenon which can occur if the gate oxide contains polarizable molecules. This problem is usually present if phosphorus glass is left in the gate region. Polarization is a wear out phenomenon with a strong dependence on temperature (i.e. the higher the temperature the sooner it will occur).

c. **Microcracks**
A random type failure mode is microcracks. This, as the name implies, is the formation of minute cracks in the aluminum metallization which usually occurs over a step. Microcracks can be prevented by contouring the steps before metal deposition (See Figure 3). This failure mode can be detected by thermal cycling or running the circuit under accelerated life conditions.

Quality Control performs in-line inspection of the metal system for microcracks using its scanning electron microscope (SEM).

d. Oxide defects can cause dielectric breakdown in the MOS structures, which generally result in an electrical short. This failure mode is seen in both **infant mortality** and **random** areas of the reliability curve. Operating life test or high voltage stress test can be used to screen for this mechanism, which is mainly voltage sensitive.

e. Packaging assembly problems such as bond wire breaking or failing to adhere to bonding pad, floating die, and improper sealing are all screenable using Intersil's 100% processing listed in Table I.

The curve shown in Figure 4 indicates our reliability status versus manufacturing time. It can be seen that we have significantly improved our overall reliability each year. This has been achieved by constant surveillance of our ultra-clean processing. Written procedures have been set-up, which are rigorously followed at each specific processing step.

Production and Quality Control carefully control and monitor phosphorus doping concentrations at intermediate and top side levels by C-V plotting taken daily. For each metallization run, our evaporators are checked for contamination by C-V plotting to ensure stability of threshold voltages.

LIFE TEST RESULTS
FAILURES AS A FUNCTION OF TIME

CIRCUIT	TEST	VOLTAGE	°C TEMPERATURE	SAMPLE	FAILURE TIME POINT HOURS						
					168	500	1K	2K	3K	5K	10K
6523	Op. Life	5.0	125	43	0	0	1	0	0	0	0
6523	Op. Life	5.0	125	143	4	1	1	1	0	0	
6523	Op. Life	5.0	125	441	7	0	0	0	0		
6508	Op. Life	5.0	125	12	0	0	1	0	0	0	
6508	Op. Life	5.0	125	29	0	0	0	0	0		
6508	Op. Life	5.0	125	74	0	1	0	0			
6508	Op. Life	10.0	125	37	0	0	0	0			
6508	Op. Life	5.0	125	426	0	0	0				
6508	Storage	—	150	65	0	0	0				
6100	Op. Life	5.0	125	30	1	0	0	1			
				1,300	12	2	3	2	0	0	0