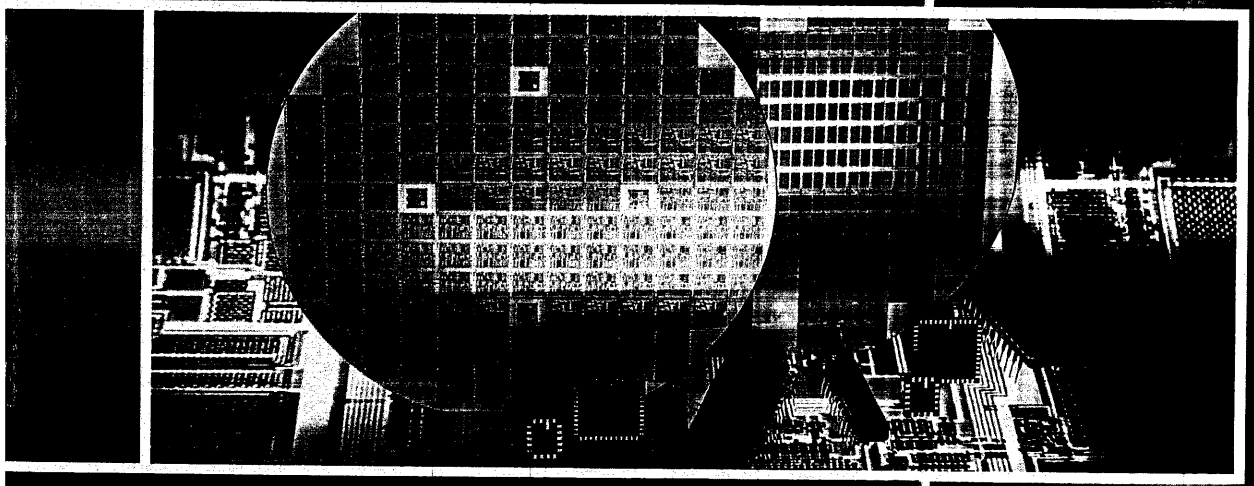
CMOS
DIGITAL DATA BOOK



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CMOS Microprocessor and Peripherals Product Index

HARRIS

HD-6120

CMOS HIGH SPEED 12 BIT MICROPROCESSOR

Features

- LOW POWER, 50 MW OPERATING, 2 MW STATIC
- SINGLE SUPPLY – 5V
- OPERATION FROM DC TO 5.1 MHZ
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- ON-CHIP CRYSTAL OSCILLATOR CIRCUITRY
- ON-CHIP EXTENDED MEMORY ADDRESSING–32K MAIN MEMORY, 32K CONTROL PANEL
- OPTIMIZED MICRO-CODE MINIMIZES THE NUMBER OF CLOCK CYCLES REQUIRED FOR ALL INSTRUCTIONS
- TWO ON-CHIP STACK POINTERS
- SIMPLIFIED MEMORY AND I/O CONTROL SIGNALS FOR EASY HARDWARE INTERFACING
- VECTORED INTERRUPT CAPABILITY
- SOFTWARE IS PAGE RELOCATABLE

Description

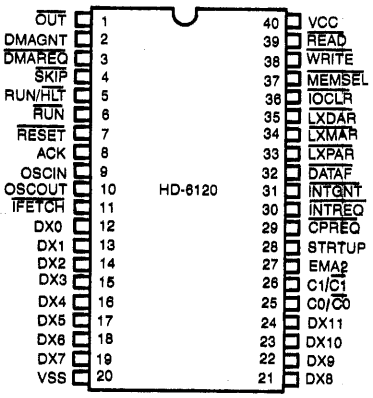
The HD-6120 is a general purpose high speed, CMOS 12 bit microprocessor. It is designed to recognize the instruction set of Digital Equipment Corporation's PDP-8/E* minicomputer.

Many architectural, functional and processing enhancements have been designed into the 6120 such that it can provide much higher system performance than its predecessor, the 6100.

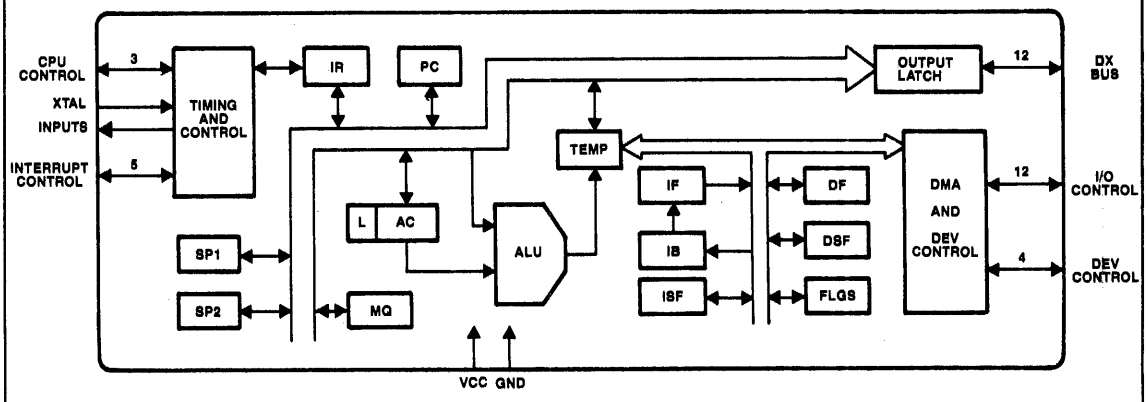
The 6120 is targeted toward the experienced PDP-8* or 6100 user. Twelve bit accuracy, rapid interrupt response, battery backup and low power (sealed enclosure) capability all equate to a processor ideally suited to real time control applications such as data acquisition, industrial control and harsh environment military systems.

* *TRADEMARK OF DIGITAL EQUIPMENT CORP.*

Pinout



Functional Diagrams



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS
Operating Voltage Range	+4V to +7V
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial (−9, −9+)	−40°C to +85°C
Military (−2, −8)	−55°C to +125°C
Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VIH(CLK)	LOGICAL ONE CLOCK VOLTAGE	VCC−0.5		V	50% duty cycle tr, tf ≤ 20 ns
VIL(CLK)	LOGICAL ZERO CLOCK VOLTAGE		VSS+0.5	V	50% duty cycle tr, tf ≤ 20 ns
VTH+	SCHMITT TRIGGER POSITIVE THRESHOLD	50% VCC	VCC−0.5	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VTH−	SCHMITT TRIGGER NEGATIVE THRESHOLD	0.5	30% VCC	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	OUTPUT LEAKAGE CURRENT	−10.0	10.0	μA	OV≤VO≤VCC
ICC	POWER SUPPLY STANDBY CURRENT		500	μA	VIN=VCC or GND VCC = 5.25 V RESET STATE OUTPUTS OPEN
ICC*	POWER SUPPLY OPERATING		10	ma	VIN=VCC or GND VCC = 5.25 V F = 5.1 Mhz OUTPUTS OPEN
IOSH	HOLD CURRENT DURING DMAGNT	−0.2	−0.6 −10.0	ma μa	Vout = VCC−1.0V Vout = OV $\overline{\text{LXMAR}}$, $\overline{\text{LXPAR}}$, $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, $\overline{\text{OUT}}$ AND MEMSEL
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−1.6	−10.0	ma	Vout = OV C0, C1, AND $\overline{\text{SKIP}}$ OUTPUTS
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−50	−250	μa	Vout = OV $\overline{\text{INTREQ}}$ OUTPUT
CIN*	INPUT CAPACITANCE		5	pf	FREQ = 1 MHZ TA=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pf	FREQ = 1 MHZ TA=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A=Industrial or Military; C_L=50 pf, FREQ=5.1 MHZ

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
F	OPERATING FREQUENCY	0	5.1	Mhz	
T	MINOR CYCLE PERIOD	392		ns	T = 2/F
TL	LXMAR, LXPAR, LXDAR PULSE WIDTH	125		ns	F=5.1 Mhz
TAS	ADDRESS SET UP TIME	60		ns	
TAH	ADDRESS HOLD TIME	180		ns	
TREAD	READ ACCESS TIME	720		ns	
TRS	READ SET UP TIME	135		ns	
TRH	READ HOLD TIME	20		ns	MEMORY OPERATIONS
TRP	READ PULSE WIDTH	425		ns	
TRD	READ PULSE DELAY	40		ns	
TWPD	WRITE PULSE DELAY	200		ns	
TWS	WRITE SET UP TIME (ALL NON IOT)	375		ns	
TWP	WRITE PULSE WIDTH (ALL NON IOT)	425		ns	
TWH	WRITE HOLD TIME (ALL NON IOT)	200		ns	
TWSIO	WRITE SET UP TIME (IOT)	200		ns	
TWIO	WRITE PULSE WIDTH (IOT)	375		ns	
TWHIO	WRITE HOLD TIME (IOT)	125		ns	
TDA	READ ACK DELAY FOR NO WAIT		150	ns	
TXA	WRITE ACK DELAY FOR NO WAIT		150	ns	F=5.1 Mhz

NOTE: All measurements are taken with input rise and fall times ≤ 20 nsec.

)ECOUPLING CAPACITORS

ıe transient current required to charge and discharge the 50 pF ad capacitance specified in the 6120 data sheet is determined by

$$i = C_L\,(dv/dt)$$

ssuming that all DX outputs change state at the same time and at dv/dt is constant;

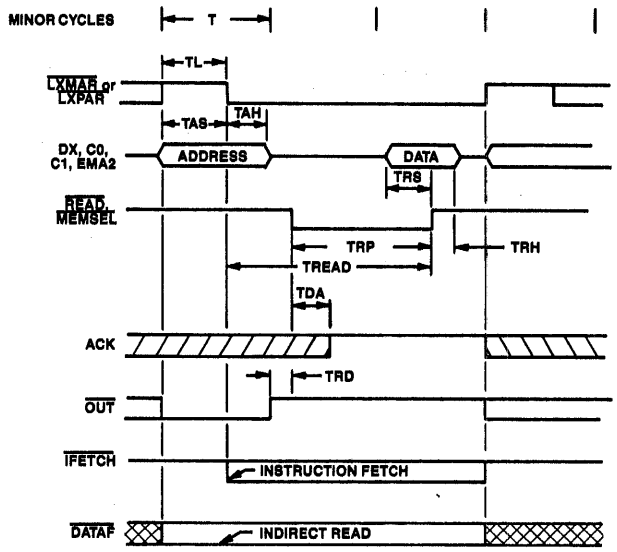
$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

ıere t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve ıtputs.

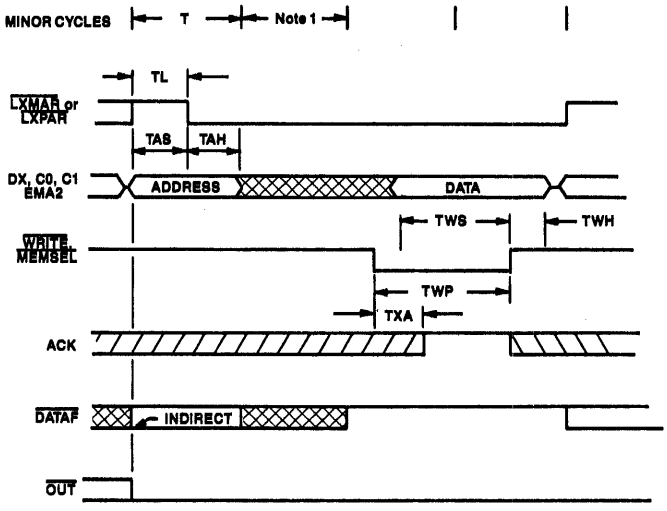
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120\ mA$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

It is recommended that for systems with greater than 50 pF loading on the DX outputs that Harris HD-6432 CMOS Hex Bi-directional bus drivers be used to buffer the 6120 from the rest of the system. The HD-6432 bus driver has guaranteed performance specifications up to a 300 pF load.

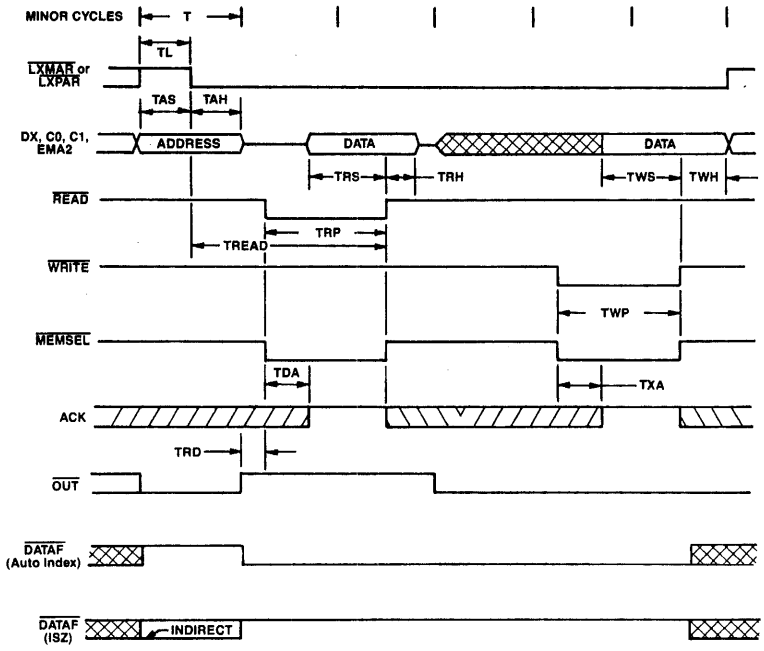


MEMORY READ OPERATION

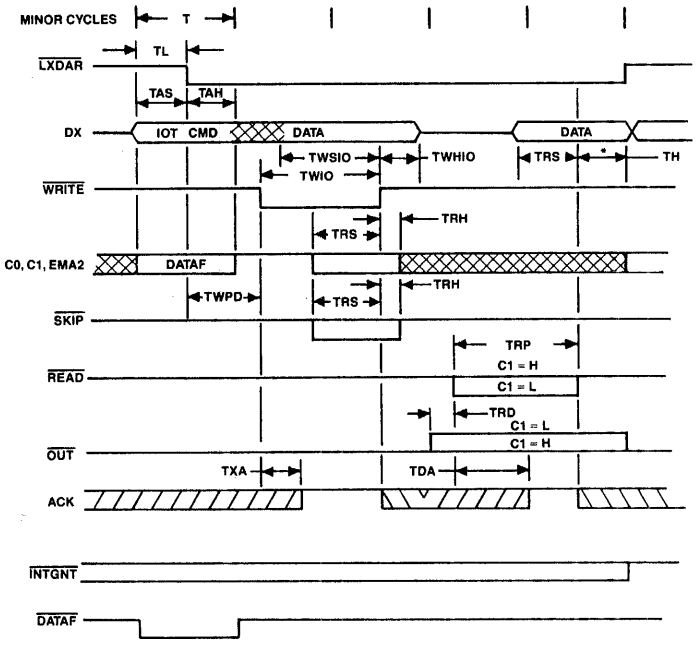


NOTE 1: This cycle is deleted on PAC1, PAC2, PPC1, PPC2 and control panel interrupt writes.

MEMORY WRITE OPERATION

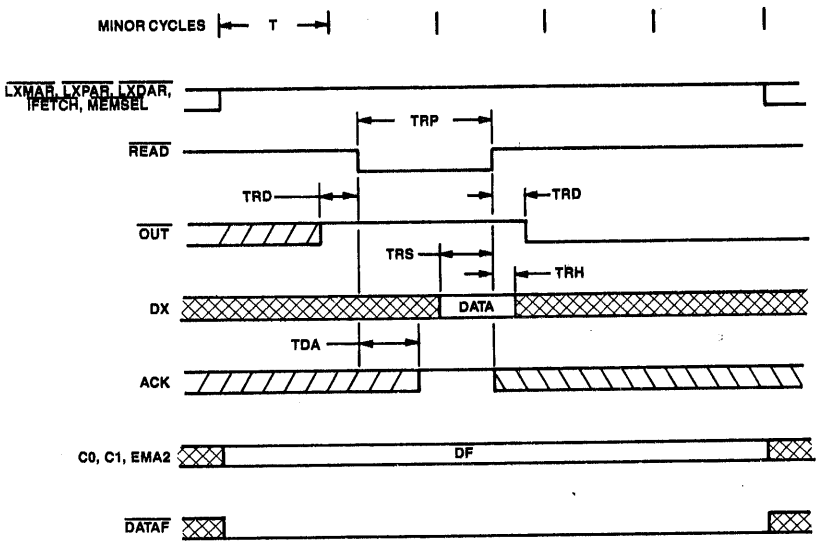


MEMORY READ-MODIFY-WRITE OPERATION

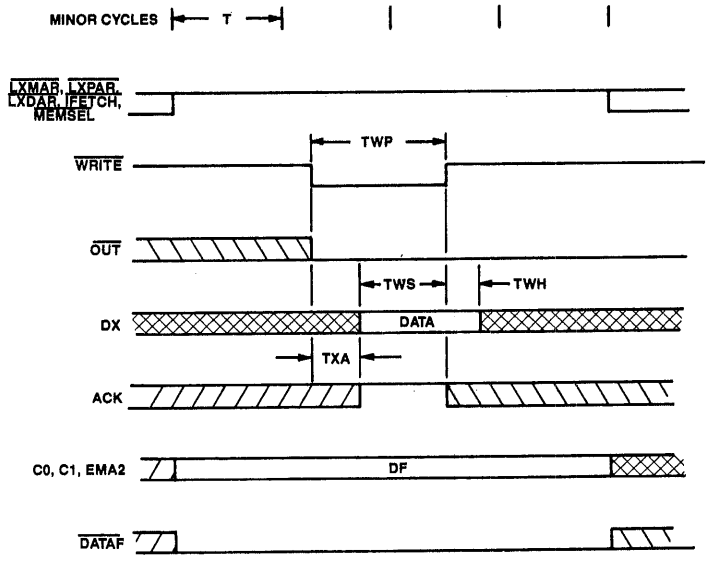


NOTES: Operation is shortened one Minor Cycle if READ is not executed.
* Read Data must be held until the rising edge of LXDAR for Read IOTs.

EXTERNAL IOT OPERATION



OR SWITCH REGISTER (OSR)



WRITE TO SWITCH REGISTER

Pin Assignments

I/O	Pin	Symbol	Active Level	Description
O	1	$\overline{OUT}$	Low	Bus timing control output which is low during all bus write or addressing operations. This signal is used to enable outbound bus drivers.
O	2	DMAGNT	High	Direct memory access grant output – DX, C0, C1, and EMA2 lines are high impedance.
I	3	$\overline{DMAREQ}$	Low	Schmitt trigger input. Direct memory access request – DMA is granted at the end of the current bus operation. Upon DMA grant, the 6120 suspends program execution until the $\overline{DMAREQ}$ line is pulled high.
I	4	$\overline{SKIP}$	Low	Input which causes the 6120 to skip the next instruction if low during an I/O instruction.
I	5	RUN/$\overline{HLT}$		Pulsing the RUN/$\overline{HLT}$ input causes the 6120 to alternately run and halt by changing the state of the internal RUNHLT flip flop on the positive transition of the RUN/$\overline{HLT}$ line.
O	6	$\overline{RUN}$	Low	This output indicates the operating state of the 6120. It is low at all times except during the reset and halt states.
I	7	$\overline{RESET}$	Low	Schmitt trigger input. Clears the AC and the memory extension registers and loads 7777 (octal) into the PC. RUNHLT is set. The STRTUP line controls whether execution starts in control panel or main memory. $\overline{RESET}$ must be held low at least 42 clock cycles after the clock starts running in order to initialize the timing generator. $\overline{LXDAR}$ is held low while $\overline{RESET}$ is low, and remains low until after the positive transition of $\overline{RESET}$ and $\overline{IOCLR}$.
I	8	ACK	High	This input indicates that peripheral or external memory is ready to transfer data. The 6120 read or write state gets extended as long as ACK is low. During this time the 6120 is in the lowest power state with clocks running.
I	9	OSCIN		Input to crystal oscillator amplifier. (Also external clock input.)
O	10	OSCOUT		Output of crystal oscillator amplifier.
O	11	$\overline{IFETCH}$	Low	Instruction fetch cycle output.
I/O	12-19, 21-24	DX0-DX11	High	Multiplexed bidirectional data in, data out and address lines. (DX0=MSB, DX11=LSB.)
	20	VSS		Most negative supply voltage.
I/O	25	C0/$\overline{C0}$		Multiplexed extended memory address (EMA) active high output MSB and peripheral device control line active low input from the peripheral device during an I/O transfer.
I/O	26	C1/$\overline{C1}$		Multiplexed EMA bit 1 and peripheral control line. See C0.
O	27	EMA2	High	Low order extended memory address output.
I	28	STRTUP		This input is tied to either VCC or VSS. If tied to VSS, the 6120 makes a panel request (caused by the PWRON flag) as soon as $\overline{RESET}$ goes to VCC. 7777 is stored in location 0000 of field 0 of panel memory. If STRTUP is tied to VCC, PWRON does not cause a panel request. Instead, the CPU starts running in location 7777 of field 0 of main memory. Location 0000 of main memory is not altered.
I	29	$\overline{CPREQ}$	Low	Schmitt trigger input. External control panel request – a dedicated interrupt which bypasses the normal device interrupt request structure. $\overline{CPREQ}$ causes a control panel interrupt request by setting the bootstrap flag with the negative going transition of $\overline{CPREQ}$. Therefore, this input is transition rather than level sensitive.
I	30	$\overline{INTREQ}$	Low	Peripheral device interrupt request input.
O	31	$\overline{INTGNT}$	Low	Peripheral device interrupt grant output.
O	32	$\overline{DATAF}$	Low	Output which is low whenever the Data Field is placed on the C0, C1 and EMA2 lines.
O	33	$\overline{LXPAR}$	Low	Output which causes control panel memory address register to be loaded. Same as $\overline{LXMAR}$, but for control panel memory operations.
O	34	$\overline{LXMAR}$	Low	Output which causes main memory address register to be loaded. Address is strobed into the main memory at the falling edge of $\overline{LXMAR}$.
O	35	$\overline{LXDAR}$	Low	Output which causes device address register to be loaded. Same as $\overline{LXMAR}$ or $\overline{LXPAR}$, except for IOT operations. Also used to distinguish between $\overline{IOCLR}$ signals. See $\overline{IOCLR}$ below.
O	36	$\overline{IOCLR}$	Low	Output which is low when $\overline{RESET}$ is low, or when CAF instruction is given. Used to clear I/O flags. If caused by $\overline{RESET}$, $\overline{LXDAR}$ is low during and after the trailing edge of $\overline{IOCLR}$.
O	37	$\overline{MEMSEL}$	Low	Memory select. During memory operations, this output pulses to VSS at bus read and write times.
O	38	$\overline{WRITE}$	Low	Write pulse. This output is low during all bus data write operations; memory, I/O, and write to switch register.
O	39	$\overline{READ}$	Low	Read pulse. This output is low during all bus read operations; memory, I/O and switch register. It also serves the function of enabling inbound bus drivers.
	40	VCC		Positive supply voltage.

Major Registers

ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

Link (L)

L is a 1-bit flip flop that serves as a high-order extension of the AC. It is used as a carry flip flop for 2's complement arithmetic. A carry out of the ALU complements L. L can be cleared, set, complemented and tested under program control and rotated as a part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

OUTPUT LATCH (OL)

While accessing memory or I/O, all data or addresses generated by the 6120 on the DX bus are held in the OL for the time required on the bus. This frees the 6120 internal bus for other uses during these operations. The output latch can also be read to the 6120 internal bus so that it can function as a temporary holding register for internal operations.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to OL and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. A skip (SKP, SMA, SZA, SNL, etc.) instruction increments the PC by 1 (again), thus causing the next instruction to be skipped. The skip instruction may be unconditional or conditional on the state of the AC and/or LINK. During an input-output operation, a device can also cause the next instruction to be skipped.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register during instruction execution.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the 6120.

STACK POINTERS (SP1 and SP2)

The stack pointers are two twelve-bit registers which hold the address of the next stack storage location. PPCX or PACX instructions cause post-decrement of the contents of stack pointer SPX. RTNX or POPX cause a pre-increment of the contents of the stack pointer. Stack pointers are loaded from, and read into, the AC. They may also be used as program-controlled temporary registers.

Memory Extension Control Registers

INSTRUCTION FIELD (IF)

The 3-bit Instruction Field holds the memory field from which all instructions, all indirect address pointers and all directly addressed operands are obtained. It may be read into the AC, and loaded from the IB. It is cleared by $\overline{\text{RESET}}$.

INSTRUCTION BUFFER (IB)

The 3-bit Instruction Buffer serves as a holding register for instructions which change the IF. Instead of changing the IF directly, field bits are loaded into the IB, and transferred to the IF at the next JMP, JMS, RTN1 or RTN2. The IB may be loaded from instruction bits, from the AC or from the ISF. The IB is cleared by $\overline{\text{RESET}}$.

INSTRUCTION SAVE FIELD (ISF)

The 3-bit ISF is loaded with the contents of the IF upon granting of an interrupt. The ISF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA FIELD (DF)

The 3-bit Data Field holds the memory field from which all indirectly addressed operands are obtained. The DF may be loaded from instruction bits, from the AC or from the DSF. It may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA SAVE FIELD (DSF)

The 3-bit DSF is loaded with the contents of the DF upon granting of an interrupt. The DSF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

Basic Timing and State Control

A 15-bit address is sent on the C0, C1, EMA2 and DX lines for memory reference instructions. The $\overline{\text{LXMAR}}$ or $\overline{\text{LXPAR}}$ signals cause an external register to store the address information if required. When executing an input-output instruction, $\overline{\text{LXDAR}}$ causes an external register to be loaded with device address and control information.

Memory data is read for an input transfer (READ). ACK controls the transfer duration. If ACK is low during input transfers, the 6120 waits with the $\overline{\text{READ}}$ line low. The high state of the ACK signal causes the 6120 to continue.

Output transfers are similar to input transfers. The address is defined as given above. ACK controls the length of time for which the $\overline{\text{WRITE}}$ signal is low, similar to the $\overline{\text{READ}}$ line control.

During an instruction fetch the instruction to be executed is retained internally and then executed. During the sequencing of the instruction the external request lines are sampled by the priority network. The state of this network decides whether the machine is going to fetch the next instruction in sequence or service one of the internal or external request lines.

Internal Priority Structure

GENERAL DESCRIPTION

The external request lines and the internal request flags are sampled in an internal priority network. The internal priority is RESET, DMAREQ, RUN/HLT, CPREQ, INTREQ, and IFETCH. The state of the priority network determines the next operation.

IFETCH

If no external or internal requests are pending, the 6120 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is low during the cycle in which the instruction is fetched.

RESET

RESET initializes all internal flags and clears the AC, LINK and MQ. All memory extension bits (IF, IB, DF, ISF and DSF) are cleared. The interrupt enable and interrupt inhibit flip flops are cleared. RUNHLT is set to the run state. The RUN line is held high by RESET. The states of SP1 and SP2 are undefined at power up, and are unaffected by RESET.

Upon application of power, the internal timing generator is completely initialized within 42 clock pulses after power is within limits with RESET held low.

The 6120 remains in the reset state as long as the RESET line is low. LXMAR, LXPAR, READ, WRITE, MEMSEL, INTGNT and IFETCH are held high. IOCLR is held low. After RESET is changed from low to high, IOCLR is made high. LXDAR is held low for one minor cycle after IOCLR is high. DMAGNT and OUT are low. The first LXMAR or LXPAR occurs 5-1/2 minor cycles after IOCLR goes high. The PC is set to 7777 (octal) and execution commences in control panel or main memory, depending on whether the STRTUP input is low or high respectively. If execution commences in control panel memory, the FZ flag is set, the Panel Data flag is cleared, and 7777 is deposited in location 0000 of control panel memory before beginning instruction execution at location 7777. If execution commences in main memory, location 0000 of main memory is not modified.

RUN/HLT

The RUN/HLT line changes the state of the RUNHLT flip flop. This flip flop is initially placed in the run state by RESET. Pulsing RUN/HLT low causes the 6120 to alternately run and halt. This is true whether executing in main memory or control memory. The RUN/HLT line is normally high. The 6120 recognizes the positive transition of the RUN/HLT signal. The HLT instruction (7402 octal) does not cause the RUNHLT flip flop to be cleared, but causes entry into panel mode with the HLTFLG set.

Memory Organization

The 6120 has a basic addressing capacity of 4096 12-bit words. The addressing capacity is extended by the internal extended memory control hardware. The memory system is organized in 4096 word groups, called memory fields. The first 4096 words of memory are in field 0. If a full 32K block of memory is installed, the uppermost memory field will be numbered 7. Two 32K word blocks of memory may be connected to the 6120. One of these blocks is known as main memory and the other is known as panel memory.

In any given memory field, every location has a unique 4 digit octal (12 bit binary) address, 0000 to 7777 (0000 to 4095 decimal). Each memory field is subdivided into 32 pages of 128 words each. Memory pages are numbered sequentially from page 00, containing octal addresses 0000-0177, to page 37 (octal), containing octal addresses 7600-7777. The most significant 5 bits of a 12-bit memory address denote the page number and the 7 low order bits specify the address of the memory location within the given page.

During an instruction fetch cycle, the 6120 fetches the instruction pointed to by the IF, PC, and address strobes LXMAR or LXPAR. The contents of the PC are transferred to the OL. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The OL now contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the OL identify the current page, that is, the page from which instructions are currently being fetched. Bits 5-11 of the OL identify the location within the current page. (Page zero, by definition, denotes the first 128 words of memory within a field, octal addresses 0000-0177.)

Memory Reference Instructions (MRI)

The memory reference instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. Bits 0-2 of a memory reference instruction specify the operation code, or opcode, and the 9 low-order bits specify the operand address. Bits 5-11, the page address, identify the location of the operand on a given page, but they do not identify the page itself. The page is specified by bit 4, called the page bit. If bit 4 is a 0, the page address is interpreted as a location on page 0. If bit 4 is a 1, the page address is interpreted to be on the current page. The entire 12-bit address, consisting of the 7 low-order bits from the instruction and either 0 or the contents of the OL in the 5 high-order bits is known as the instruction address, or IA. The IF provides the 3 high-order bits of the complete 15-bit address, IA.

Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand is directly addressed, and IA is the location of the operand. When bit 3 is a 1, the operand is indirectly addressed, and the contents of IA specify the location of the operand. To address a location that is not on page 0 or the current page, the absolute address of the desired location is stored in one of the 256 directly-addressable locations as a pointer address. The instruction addresses the operand indirectly through this pointer. Upon execution, the MRI operates on the contents of the location identified by the address contained in the pointer location. The pointer is obtained from the current Instruction Field; the data is in the current Data Field.

It should be noted that locations 0010-0017 (octal) in page 0 of any field are autoindexed. If these locations are addressed as indirect pointers, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications. During the memory write operation, the DF appears on CO, C2, and EMA2. Indirect reference to auto index registers from page 0 work as defined whether the page bit is "1" or "0".

Data is represented in two's complement integer notation. In this system of notation, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most-significant bit. In the 12-bit word used in the 6120, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The number range for this system is +3777 to −4000 octal (+2047 to −2048 decimal).

Microprogramming

Group 1, 2 and 3 instructions are all microprogrammable. This means that as many as five discrete instructions can be combined into one instruction which can execute in the same amount of time required for a single discrete instruction. Instructions listed under Groups 1, 2 and 3 represent the most commonly used microcoded instructions for these groups and are not a complete listing of all possible instructions. The general rule of thumb is that if an instruction can be represented in machine code (using the "Microinstruction Format" templet), then it is a legal instruction. The logical sequence table which accompanies each "Microinstruction Format" templet shows the order in which the microcoded operations are performed. "Introduction to Programming" by Digital Equipment Corporation further explains the PDP-8* instruction set and the use of microprogramming. This handbook is also available from Harris Semiconductor.

* Trademark of Digital Equipment Corporation

HD-6120 Oscillator Requirements

The HD-6120 has been designed to work with either a parallel resonant, fundamental mode crystal or an external frequency source.

EXTERNAL CRYSTAL

When using an external crystal, two capacitors and a resistor are required to complete the oscillator circuit. Table 1 lists the required crystal characteristics and Figure 1 shows the correct circuit connections.

TABLE 1

Parameter	Typical Characteristic
Frequency	2.4 – 5.1 Mhz
Type of Operation	Parallel resonant, AT cut, Fundamental mode
Load Capacitance	C_L = 20pf or 32pf
R_{series} (Max.)	200 Ω at 5.1 Mhz

The load capacitors C1, C2 are chosen such that the total (including stray) capacitance seen by the crystal matches the specified load capacitance (C_L). For C_L = 20pf, a value of C1 = C2 = 20pf. is normally used. For C_L = 32pf. C1 and C2 would be approximately 47pf. The actual values are normally not critical unless an ultra precise frequency is desired.

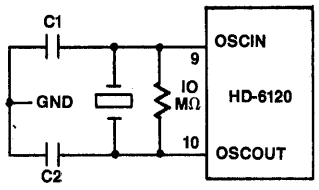


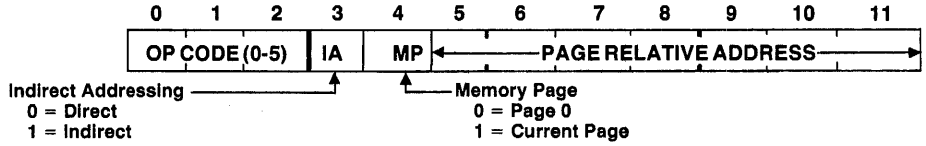
FIGURE 1

EXTERNAL FREQUENCY SOURCE

When using an external frequency source, the duty cycle should be 50/50 with rise and fall times less than 20ns. Input voltage levels should be $V_{IH} \geq VCC-0.5V$ and $V_{IL} \leq 0.5V$. The OSCIN pin of the HD-6120 is used in this case with the OSCOUT pin left open. The Harris 82C84A CMOS Clock Generator is an excellent external frequency source which provides three outputs at different divide ratios (÷1, ÷3, ÷6).

Memory Reference Instructions

MICROINSTRUCTION FORMAT



Mnemonic	Opcode	Minor Cycles Dir	Ind	Auto	Operation
AND	0xxx	7	10	12	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (xxx) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1xxx	7	10	12	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a load from memory.
ISZ	2xxx	9*	12*	14*	INCREMENT AND SKIP IF ZERO: The contents of the effective address is incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3xxx	7	10	12	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4xxx	7	10	12	JUMP TO SUBROUTINE: The contents of the PC is stored in the effective address and the effective address + 1 is stored in the PC. The Link, AC and MQ are unchanged.
JMP	5xxx	4	7	9	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.

* Add two Minor Cycles if a skip is taken.

Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	R1	R2	R3	IAC

Logical Sequence:
1 – CLA, CLL
2 – CMA, CML
3 – IAC
4 – RAR, RAL, RTR, RTL, BSW, R3L

Bit	R1	R2	R3	
	0	0	0	No Rotate
	0	0	1	BSW
	0	1	0	RAL
	0	1	1	RTL
	1	0	0	RAR
	1	0	1	RTR
	1	1	0	R3L
	1	1	1	Do Not Use

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7000	1	No operation.
IAC	7001	3	Increment accumulator – the contents of the AC is incremented by 1. Carry out complements the LINK.
BSW	7002	4	Byte swap – AC0–5 are exchanged with AC6–11 respectively. The LINK is not changed.
RAL	7004	4	Rotate accumulator left – the contents of the AC and LINK are rotated one binary position to the left. AC0 is shifted to LINK and LINK is shifted to AC11.
RTL	7006	4	Rotate two left – equivalent to two RAL's.
RAR	7010	4	Rotate accumulator right – the contents of the AC and LINK are rotated one binary position to the right. AC11 is shifted into the LINK, and LINK is shifted to AC0.
RTR	7012	4	Rotate two right – equivalent to two RAR's.
R3L	7014	4	Rotate AC (but not LINK) left 3 places. AC0 is rotated into AC9, AC1 into AC10, etc.
CML	7020	2	Complement LINK – the contents of the LINK is complemented.
CMA	7040	2	Complement accumulator – the contents of the AC is replaced by its 1's complement.
CIA	7041	2, 3	Complement and increment accumulator – the contents of the AC is replaced by its 2's complement.
CLL	7100	1	Clear LINK – the LINK is made 0.
CLL RAL	7104	1, 4	Clear LINK, rotate left.
CLL RTL	7106	1, 4	Clear LINK, rotate two left.
CLL RAR	7110	1, 4	Clear LINK, rotate right.
CLL RTR	7112	1, 4	Clear LINK, rotate two right.
STL	7120	1, 2	Set the LINK – load binary 1 into LINK.
CLA	7200	1	Clear accumulator – load AC with 0000.
CLA IAC	7201	1, 3	Clear and increment accumulator – load AC with 0001.
GLK	7204	1, 4	Get LINK – place LINK in AC11; clear AC0-10 and LINK.
STA	7240	1, 2	Set accumulator – make AC=7777.
CLA CLL	7300	1	Clear AC and LINK.

Group 2 Operate Instructions

All group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
					SMA	SZA	SNL	0			
1	1	1	1	CLA	SPA	SNA	SZL	1	OSR	HLT	0

Logical Sequence:
1 – (BIT 8=0) – SMA or SZA or SNL
– (BIT 8=1) – SPA and SNA and SZL
2 – CLA
3 – OSR, HLT

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7400	1	No operation
HLT	7402	3	Set the HLTFLG. Causes entry into panel mode instead of executing the next instruction provided IIFF is not set. If IIFF is set, panel mode is entered after the JMP, JMS, RTN1 or RTN2 which clears IIFF. This instruction in panel mode does not cause a re-entry into panel mode, but does set HLTFLG.
OSR	7404	3	OR with switch register – the contents of an external device are "OR"ed with the contents of the AC, and the result stored in the AC. The contents of the DF are available for device selection.
SKP	7410	1	Skip – the content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	Skip on non-zero LINK – skip if LINK one
SZL	7430	1	Skip if LINK zero
SZA	7440	1	Skip on zero accumulator – skip if AC=0000
SNA	7450	1	Skip on non-zero accumulator
SZA SNL	7460	1	Skip if AC=0000 or if LINK=1
SNA SZL	7470	1	Skip if AC not 0000 and if LINK is zero
SMA	7500	1	Skip on minus accumulator (ACO=1)
SPA	7510	1	Skip on positive accumulator (ACO=0)
SMA SNL	7520	1	Skip if AC is minus or if LINK is 1
SPA SZL	7530	1	Skip if AC is plus and if LINK is 0
SMA SZA	7540	1	Skip if AC is minus or zero
SPA SNA	7550	1	Skip if AC is positive and non-zero
SMA SZA SNL	7560	1	Skip if AC is minus or if AC is =0000 or if LINK is 1
SPA SNA SZL	7570	1	Skip if AC is positive, nonzero and if LINK is zero
CLA	7600	2	Clear accumulator
LAS	7604	2, 3	Load accumulator from switch register
SZA CLA	7640	1, 2	Skip if AC=0000, then clear AC
SNA CLA	7650	1, 2	Skip on non-zero accumulator, then clear AC
SMA CLA	7700	1, 2	Skip on minus AC, then clear AC
SPA CLA	7710	1, 2	Skip on positive AC, then clear AC

Group 3 Operate Instructions

If bits 6, 8, 9 or 10 are set to a one, instruction execution is not altered but the instruction becomes uninterruptable by either panel or normal interrupts. That is, the next instruction is guaranteed to be fetched barring a reset, DMAREQ or RUN/HLT flip flop in the HLT state.

Group 3 Operate Instructions

All group 3 instructions require 6 minor cycles.

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

Logical Sequence:
1 – CLA
2 – MQA, MQL
3 – ALL OTHERS
* – CAUSES INSTRUCTION TO IGNORE INTERRUPTS IF A "1"

BIT 4 5 7	
0 0 0	NOP
0 0 1	AC→MQ, O→AC
0 1 0	(MQ + AC)→AC
0 1 1	MQ→AC
1 0 0	0→AC
1 0 1	0→AC: 0→MQ
1 1 0	MQ→AC
1 1 1	MQ→AC, 0→MQ

+ denotes logical OR

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7401	3	No operation
MQL	7421	2	MQ register load – the MQ is loaded with the contents of the AC and the AC is cleared. The original contents of the MQ is lost.
MQA	7501	2	MQ "OR" with accumulator – the contents of the MQ is "OR"ed with the contents of the AC, and the result left in the AC. The MQ is not modified.
SWP	7521	3	Swap contents of AC and MQ – the contents of the AC and MQ are exchanged
CLA	7601	1	Clear accumulator
CAM	7621	3	Clear AC and MQ (actually a CLA MQL)
ACL	7701	3	Load AC with contents of MQ
CLA SWP	7721	3	Clear AC, then swap – the MQ is loaded into the AC; 0000 is loaded into the MQ

Stack Operation Instructions

The following IOT instructions are internally decoded to perform stack operations using internal stack pointers SP1 and SP2. These are internal IOT instructions; the $\overline{\text{LXDAR}}$ signal is not generated. If instructions are being fetched from main memory, the stacks are located in field 0 of main memory. If instructions are being fetched from panel memory, the stacks are located in field 0 of panel memory, except for the case of a ReTurN from control panel memory via a RTN1 or RTN2 instruction. In this case, the main memory stack is accessed by the instruction fetched from panel memory. Two separate stacks may be maintained – one for the PC, the second for the AC. An increment of the stack pointer is defined as a pop off the stack.

Mnemonic	Opcode	Operation
PPC1	6205	PUSH PC ON STACK. The contents of the PC are incremented by one and the result is loaded into the memory location pointed to by the contents of SP1. SP1 is then decremented by 1.
PPC2	6245	PUSH PC ON STACK. The same as PPC1 except that SP2 is used as the memory pointer.
PAC1	6215	PUSH AC ON STACK. The contents of the AC is loaded into the memory location pointed to by the contents of SP1. The contents of SP1 is then decremented by 1.
PAC2	6255	PUSH AC ON STACK. The same as PAC1 except that SP2 is used as the memory pointer.
RTN1	6225	RETURN. The contents of the stack pointer (SP1) is incremented by one. The contents of the Instruction Buffer (IB) is loaded into the Instruction Field (IF) register. If a prior PEX instruction was executed, the Control Panel Flip Flop (CTRLFF) is cleared. If the Interrupt Inhibit Flip Flop (IIFF) is set, then the Force Zero (FZ) flag is cleared. The contents of the memory location pointed to by SP1 is loaded into the PC. Prior PEX is cleared.
RTN2	6265	Same as RTN1 except that SP2 is used as the stack pointer.
POP1	6235	The contents of SP1 is incremented by 1. The contents of the memory location pointed to by SP1 is then loaded into the AC.
POP2	6275	Same as POP1 except that SP2 is used as the stack pointer.
RSP1	6207	The contents of SP1 is loaded into the AC.
RSP2	6227	The contents of SP2 is loaded into the AC.
LSP1	6217	The contents of the AC is loaded into SP1. The AC is cleared.
LSP2	6237	The contents of the AC is loaded into SP2. The AC is cleared.
CAUTION: When switching between main and control panel memory, the stack pointers must be saved and restored.		

Internal Control Instructions

Note that these instructions apply if the 6120 is executing instructions from main memory or control panel.

Mnemonic	Opcode	Operation
ION	6001	Turn on interrupt system. The Interrupt Enable Flip Flop is set. Neither $\overline{\text{INTREQ}}$ or any control panel request will be granted until after execution of the next instruction. (6 minor cycles.)
IOF	6002	Turn off interrupt. The interrupt enable flip flop is cleared immediately. If $\overline{\text{INTREQ}}$ is low while this instruction is being processed, the interrupt will not be recognized. (6 minor cycles.)
RTF	6005	Load the following from the AC: AC bit → To 0 → LINK 1 → GT 4 → IEFF 6-8 → IB 9-11 → DF The IIFF is set. The AC is cleared following the load operation. (8 minor cycles.)
SGT	6006	Skip if the GT flag is set. (7 minor cycles.)
CAF	6007	The AC, LINK and GT flag are cleared. Interrupt enable flip flop is cleared. $\overline{\text{IOCLR}}$ is generated with $\overline{\text{LXDAR}}$ high, causing peripheral devices to clear their flags. (7 minor cycles.)
WSR	6246	Write to switch register. The contents of the AC are written to an external device using a special I/O transfer. The AC is then cleared. The contents of the DF are available for device selection. DATAF is asserted. (7 minor cycles.)
GCF	6256	Get current fields. The following bits are loaded into the AC: AC bit → Function 0 → LINK 1 → GT flag 2 → 1 if $\overline{\text{INTREQ}}$ is low; 0 if $\overline{\text{INTREQ}}$ is high 3 → PWRON flag 4 → IEFF 5 → 0 6-8 → IF 0-2 9-11 → DF 0-2 (9 minor cycles.)

Main Memory Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from main memory.

Mnemonic	Opcode	Operation
SKON	6000	Skip if interrupt on, and turn off interrupt system. (7 minor cycles.)
SRQ	6003	Skip if the device interrupt line is low. Note that this skip does not depend on the state of the memory extension control's interrupt inhibit flip flop. The SRQ merely tests the state of the $\overline{\text{INTREQ}}$ pin. (7 minor cycles.)
GTF	6004	Get flags. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if $\overline{\text{INTREQ}}$ is low 0 if $\overline{\text{INTREQ}}$ is high
3	PWRON flag
4	1
5	0
6-8	ISF 0-2
9-11	DSF 0-2

(9 minor cycles.)

PR0 PR1 PR2 PR3	6206 6216 6226 6236	These four opcodes have the same effect. The PNLTRP is set, causing the 6120 to enter panel mode instead of executing the next instruction, provided the interrupt inhibit flip flop is not set. If the interrupt inhibit flip flop is set, the panel mode will be entered following the JMP, JMS, RTN1 or RTN2 which clears the interrupt inhibit flip flop. These instructions are a NOP in panel mode. (6 minor cycles.)

Panel Memory Control Instructions

The 6120's control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

Panel mode is entered because of the occurrence of any of four events. Each of these events sets a status flag, as well as causing the entry into panel mode. It should be noted that more than one event might happen simultaneously.

Flag	Set by	Cleared by
PWRON	$\overline{\text{RESET}}$ low and STRTUP low	PRS and PEX
PNLTRP	PRQ (main memory)	PRS and PEX
HLTFLG	HLT instruction (or any OPR2 instruction with bit 10 a 1)	PGO
BTSTRP	High-to-low transition of $\overline{\text{CPREQ}}$	PRS if BTSTRP was set when status read

Panel mode entry is functionally similar to the granting of an interrupt with some important differences. Entry into panel mode for any reason is inhibited by the interrupt inhibit flip flop. Note that this means that a PRQ or HLT instruction executed when the interrupt inhibit flip flop is set will not be recognized until after the interrupt inhibit flip flop is cleared on the next JMP, JMS, RTN1 or RTN2. Entry into panel mode is also inhibited immediately following the ION instruction but will be recognized after the instruction following the ION is executed.

When a panel request is granted, the PC is stored in location 0000 of the control panel memory and the 6120 resumes operation at location 7777 (octal) of the panel memory. During PC write, 0 appears on C0, C1 and EMA2. The states of the IB, IF, DF, ISF and DSF registers are not disturbed by entry into the control panel mode but execution is forced to commence in field zero. The panel memory would be organized with RAM in the lower pages and ROM or PROM in the higher pages of field zero. The control panel service routine would be stored in the nonvolatile ROMs, starting at 7777 (octal).

A ConTRoL panel Flip Flop, CTRLFF, which is internal to the 6120, is set when the $\overline{\text{CPREQ}}$ is granted. The CTRLFF prevents further $\overline{\text{CPREQ}}$s from being granted, bypasses the interrupt enable system and redefines several of the internal control instructions.

As long as the CTRLFF is set, $\overline{\text{LXPAR}}$ is used for all instruction, direct data and indirect pointer references. Also, while CTRLFF is set, the $\overline{\text{INTGNT}}$ line is held high but the interrupt grant flip flop is not cleared. IOTs executed while CTRLFF is set do not clear the interrupt grant flip flop.

Indirectly addressed data references by control panel AND, TAD, ISZ or DCA instructions reference panel memory or main memory as controlled by a Panel Data Flag (PDF) internal to the 6120. If set, this flag causes indirect references from control panel memory to address control panel memory using $\overline{\text{LXPAR}}$. If cleared, this flag causes indirect references from control panel memory to address main memory using $\overline{\text{LXMAR}}$.

The PDF is cleared unconditionally whenever the panel mode is entered for any reason. It is also cleared by an instruction called CPD (Clear Panel Data). The PDF is set by an instruction called SPD (Set Panel Data). The state of the Panel Data flag is ignored when not operating in panel mode.

Extended memory operations are implemented for panel mode instructions by a 1-bit flag in the EMA logic (the Force Zero – FZ – flag). This flag is always set when panel mode is entered and before the first panel mode memory operation (the store of the PC at control panel memory location 0000). As long as the FZ flag is set, zero appears on C0, C1 and EMA2 in place of the IF except for special C0, C1, EMA2 contents defined during write intervals, which remain undisturbed by FZ being set. The IF remains unchanged, however, and may be read by the RIF instruction. The data field is unaffected by the FZ flag and functions as defined above, using the panel data flag to determine whether operands are in main or control panel memory. In particular if FZ=0:

Control panel instruction fetch is to control panel field 0.

Control panel indirect address fetch is to control panel field 0.

Control panel current page or page zero direct data operations are to control panel field 0.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

The FZ flag is cleared in panel mode simultaneously with the (IF)←(IB) transfer following the first panel mode instruction which may change the IF. These instructions are CIF (62X2), CDF CIF (62X3), RTF (6005), and RMF (6244). The (IF)←(IB) transfer (and hence the FZ clear) takes place during the first JMP, JMS, RTN1, or RTN2 following the instruction. Once the FZ flag is cleared, the EMA logic operates in control panel memory as it does in main memory with the exception that the panel data flag controls whether indirect data operations are to control panel or main memory. In particular:

Control panel instruction fetch is specified by IF.

Control panel indirect address fetch is specified by IF.

Control panel current page or page zero data operations are specified by IF.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

Once the FZ flag is cleared in panel mode, it is not set until panel mode is entered again. The state of the FZ flag when not in panel mode is a "don't care".

Exiting from the control panel routine is normally achieved by executing the following sequence:

```
PEX
JMP I 0000    /location 0000 in control panel memory
```

The second instruction in this sequence may be any JMP, JMS, RTN1 or RTN2 instruction. The use of JMS is not recommended, since the programmer has no means of preserving the FZ and panel data flags.

The PEX instruction will cause the next JMP, JMS, RTN1 or RTN2 instruction to reset the CTRLFF. Location 0000 in the control panel memory contains either the original return address deposited by the 6120 when the control panel routine was entered or it may be a new starting address defined by the control panel routine. The IF and DF registers may also contain their original field designations or may have been altered by the control panel routine. If an exit is made from the control panel routine with the HLTFLG set, one instruction is executed in main memory before control panel mode is reentered due to the HLTFLG being set. Note that this allows a software-controlled single step operation of programs in main memory. Caution: Single step operation will not occur for any uninterruptable instructions or any instructions which set the IIFF. Exiting from a control panel routine can also be achieved by activating the $\overline{\text{RESET}}$ line, since reset has a higher priority than control panel request. If the RUN/$\overline{\text{HLT}}$ line is pulsed while the 6120 is in the panel mode, the 6120 will halt at the completion of the current instruction.

Panel Mode Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from Control Panel Memory

<table>
<tr><th>Mnemonic</th><th>Opcode</th><th>Description</th></tr>
<tr><td>PRS</td><td>6000</td><td>Read panel status bits into AC0-4, 0 into remainder of AC.
The bits are read as follows:
<table>
<tr><th>AC bit</th><th>Function</th></tr>
<tr><td>0</td><td>BTSTRP</td></tr>
<tr><td>1</td><td>PNLTRP</td></tr>
<tr><td>2</td><td>1 if $\overline{\text{INTREQ}}$ is low
0 if $\overline{\text{INTREQ}}$ is high</td></tr>
<tr><td>3</td><td>PWRON</td></tr>
<tr><td>4</td><td>HLTFLG</td></tr>
<tr><td>5-11</td><td>0</td></tr>
</table>
Following the reading of the flags into the AC, the flags are cleared, with the exception of HLTFLG. BTSTRP is cleared only if a 1 was read into AC0. (8 minor cycles).</td></tr>
<tr><td>PG0</td><td>6003</td><td>Reset the HLTFLG flip flop. (6 minor cycles).</td></tr>
<tr><td>PEX</td><td>6004</td><td>Exit from panel mode into main memory at the end of the next JMP, JMS, RTN1 or RTN2 instruction. Clear PWRON and PNLTRP. (6 minor cycles).</td></tr>
<tr><td>CPD</td><td>6266</td><td>Clear Panel Data Flag (PDF). Clears the panel data flag so that indirect data operands of panel mode instructions are obtained from main memory. The panel data flag is also cleared upon entry into panel memory. (5 minor cycles).</td></tr>
<tr><td>SPD</td><td>6276</td><td>Set panel data flag. Sets the panel data flag so that indirect data operands of panel mode instructions are obtained from panel memory. (5 minor cycles).</td></tr>
</table>

Memory Extension Instructions

Most memory extension instructions require 6 minor cycles, except for RIB which requires 9 minor cycles.

The internal memory extension control extends the basic 4K addressing structure of the 6120 to 32K. It does so by appending three high-order bits to the memory address. These bits, which appear on C0, C1 and EMA2 lines, apply to addresses within main memory or control panel memory. The changing of memory fields is accomplished via internal control instructions.

The Instruction Field (IF) serves as an extension to the PC, providing three high-order bits during instruction fetches. Note that there is no carry from the most-significant PC bit into the IF. The IF is also used for directly-addressed operands, and for indirect address pointers.

The Data Field (DF) serves to extend the address of indirectly addressed operands, external IOTs, OSR and WSR functions.

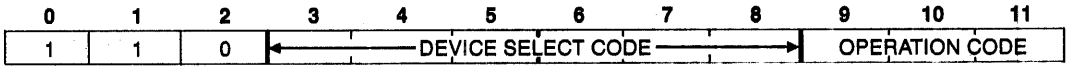
The Instruction Save Field and Data Save Field are used to retain the contents of the IF and the DF which existed prior to an interrupt.

Mnemonic	Opcode	Operation
CDF	62X1	Change Data Field to X. X is loaded into DF.
CIF	62X2	Change Instruction Field to X. X is loaded into IB, and the IIFF is set. (The set state IIFF causes the priority network to ignore interrupt requests). The contents of IB are loaded into the IF at the end of the next JMP, JMS, RTN1 or RTN2 instruction. At the same time the interrupt inhibit flip flop is cleared.
CDF CIF	62X3	A microprogrammed combination of CDF and CIF. Both fields are set to X.
RDF	6214	Load the contents of the Data Field register into bits 6-8 of the AC. DF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIF	6224	Load the contents of the Instruction Field register into bits 6-8 of the AC. IF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIB	6234	Load the contents of the ISF and DSF into bits 6-11 of the AC. ISF0-2 goes to AC6-8 and DSF0-2 goes to AC9-11 respectively. AC0-5 are unchanged.
RMF	6244	Load the contents of ISF into IB, DSF into DF, and set the interrupt inhibit flip flop. This instruction is used to restore the contents of the memory field registers to their values before an interrupt occurred.

Input/Output Instructions

Input/output transfer instructions, which have an opcode of 6, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the 6120. Three types of data transfer may be used to receive or transmit information between the 6120 and one or more peripheral I/O devices. Programmed data transfer provides a straight-forward means of communicating with relatively slow I/O devices, such as teletypes, cassettes, card readers and CRT displays. Interrupt transfers use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with I/O operations. Both programmed data transfers and program interrupt transfers use the accumulator as a buffer, or storage area, for all data transfers.

IOT INSTRUCTION FORMAT



Bits 0-2 are always set to 6 (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended. Device selection codes 00 and 2X specify internal operations, and may not be used by external devices. Up to 55 I/O devices can be specified. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface (see the 6121 specification).

Programmed data transfer begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are placed on DX0-11; the data field is placed on C0, C1 and EMA2; and $\overline{\text{DATAF}}$ is asserted. $\overline{\text{LXDAR}}$ then falls, signalling the beginning of the IOT execute phase. These bits must be latched in an external register, since they are then removed to free the DX bus for I/O data exchanges. Following the fall of $\overline{\text{LXDAR}}$, the 6120 generates a write signal. During the $\overline{\text{WRITE}}$, the 6120 reads the $\overline{\text{SKIP}}$, C0 and C1 lines. $\overline{\text{SKIP}}$, C0, and C1 define the type of I/O operation. If C1 is pulled low during the write signal, then the 6120 adds one minor cycle and performs a read operation after the write.

The control line $\overline{\text{SKIP}}$, when low during the write portion of an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The C0 and C1 lines are treated independently of the $\overline{\text{SKIP}}$ line.

Programmed I/O Control Lines

External programmed data transfers require 10 minor cycles if there is a read, 9 if not.

Control Lines C0	C1	Operation	Description
High	High	(Device)←(AC)	The contents of the AC is sent to the device.
Low	High	(Device)←(AC), CLA	The contents of the AC is sent to the device; then the AC is cleared.
High	Low	(AC)←(AC)V(Device)	Data is received from a device, "OR"ed with the data in the AC, and the result is stored in the AC.
Low	Low	(AC)←(Device)	Data is received from a device and loaded into the AC.

Interrupt Transfer

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced. It also provides a means of performing programmed data transfers between the 6120 and peripheral devices while executing another program. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device is set, indicating that the device is actually ready to perform the next data transfer.

The interrupt system allows external conditions to interrupt the computer program (which must be in main memory) by driving $\overline{\text{INTREQ}}$ low. If no internal higher priority requests are outstanding and the interrupt system is enabled, the 6120 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the interrupt enable flip flop in the 6120 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The interrupt inhibit flip flop prevents interrupts (both device and control panel) from occurring when there is a possibility that the IF is not equal to the IB. More specifically, the interrupt inhibit flip flop is set whenever the IB is loaded (i.e., by the instructions CIF, CDF CIF, RMF or RTF), and cleared whenever the IF is loaded from the IB (i.e., at the proper phase of JMP, JMS, RTN1 or RTN2 instructions). Device interrupts are recognized only if the interrupt system is enabled, the interrupt inhibit flip flop is cleared and $\overline{\text{INTREQ}}$ is low.

Upon recognition of an interrupt, the 6120 stores the PC in location 0000 of field 0 and clears the interrupt enable flip flop. Zero appears on C0, C1 and EMA2 when the PC is stored. At the same time, $\overline{\text{INTGNT}}$ goes low. During the interrupt grant sequence, IF is loaded into ISF and DF is loaded into DSF. IF, IB and DF are then cleared. The next instruction is fetched from location 0001 of main memory field 0. $\overline{\text{INTGNT}}$ remains low until the trailing edge of the first $\overline{\text{LXDAR}}$ generated by a main memory IOT following the recognition of the interrupt. The granting of an interrupt requires 4 minor cycles. If a control panel interrupt is granted while $\overline{\text{INTGNT}}$ is low, $\overline{\text{INTGNT}}$ will be forced high as long as CTRLFF is set but will return to the low state when CTRLFF is cleared.

Direct Memory Access

Direct memory access, sometimes called data break, is the preferred form of data transfer to use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The 6120 is involved only in setting up the transfer; the transfers take place with no 6120 intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The external device generates a DMA request when it is ready to transfer data. The 6120 grants the $\overline{\text{DMAREQ}}$ by pulling the DMAGNT signal high at any point in any of the instructions, or between instructions, when the 6120 is not using the DX bus in performing a bus read, write or read-modify-write operation. The 6120 suspends its internal timing until the $\overline{\text{DMAREQ}}$ line is high. The DX lines, EMA2, C0 and C1 lines are tristated. $\overline{\text{LXPAR}}$, $\overline{\text{LXMAR}}$, $\overline{\text{MEMSEL}}$, $\overline{\text{OUT}}$, $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are all held high by a device on each of these lines which only has a very small pull-up drive. These lines can then be pulled down by an external device. In this way, these control lines are stable until the external device can gain control of them. $\overline{\text{IFETCH}}$ and $\overline{\text{LXDAR}}$ are both held high. $\overline{\text{RUN}}$ is held low. The states of $\overline{\text{DATAF}}$ and $\overline{\text{INTGNT}}$ are undisturbed.

The external DMA device must not drive the bus until DMAGNT is high. The DMA device must:

a. Drive all signals with three-state devices.
b. Provide all address, data, $\overline{\text{LXPAR}}$, $\overline{\text{LXMAR}}$, and other control signals with the proper timing.
c. Return all control lines to the high state before relinquishing the bus.
d. Three-state all drivers at or before $\overline{\text{DMAREQ}}$ is pulled high by the device.

After the $\overline{\text{DMAREQ}}$ line is pulled high, the 6120 negates DMAGNT and re-establishes proper timing before proceeding.

Internal Flags

Name	Set Conditions	Clear Conditions	Load Conditions	Comments
IEFF	ION inst.	1. $\overline{\text{RESET}}$=low 2. IOF inst. 3. During $\overline{\text{INTGNT}}$ sequence 4. SKON inst.	RTF inst.	INTERRUPT ENABLE FLIP FLOP: Tested by the SKON instruction. GCF inst. loads state of IEFF into AC4. $\overline{\text{INTREQ}}$ is honored only if IEFF is set (1).
IIFF	1. CIF inst. 2. CIF CDF 3. RMF 4. RTF	1. $\overline{\text{RESET}}$=low 2. JMP, JMS, RTN inst.	none	INTERRUPT INHIBIT FLIP FLOP: Suppresses any $\overline{\text{INTREQ}}$ or Control Panel mode request.
CTRLFF	Upon entry into panel mode	1. $\overline{\text{RESET}}$=low 2. Next JMP, JMS or RTN after PEX inst.	none	CONTROL PANEL FLIP FLOP: Indicates control panel operation. Interrupts are not honored when set.
FZ	Upon entry into panel mode	First JMP, JMS or RTN inst. executed with IIFF set.	none	FORCE ZERO FLAG: Forces control panel instruction field access to field zero. Indirect data accesses are not affected.
PDF	SPD inst.	1. Panel mode entry 2. CPD inst.	none	PANEL DATA FLAG: When set causes indirect data operations executed in control panel to access CP memory. Otherwise they are to main memory. PDF is ignored when executing in main memory.
RUNHLT	$\overline{\text{RESET}}$=low	none	On the low to high transition of the RUN/HLT line	RUN HALT FLIP FLOP: When cleared the 6120 will halt after the first instruction in which this state is detected. The 6120 will respond to $\overline{\text{DMAREQ}}$ in this state.
HLTFLG	HLT inst.	1. $\overline{\text{RESET}}$=low 2. PG0 inst.	none	HALT FLAG: When set, panel mode will be entered unless the IIFF is set or $\overline{\text{RESET}}$ is low. IIFF can be cleared on the next JMP, JMS or RTN instruction at which point panel mode will be entered.
PNLTRP	PR0, PR1, PR2, PR3 inst. (main only)	1. $\overline{\text{RESET}}$=low 2. PRS inst. 3. PEX inst.	none	PANEL TRAP FLAG: Same result as defined for HLTFLG.
BTSTRP	High to low transition of $\overline{\text{CPREQ}}$	1. $\overline{\text{RESET}}$=low 2. PRS inst.	none	BOOTSTRAP FLAG: Same result as defined for HLTFLG.
PWRON	$\overline{\text{RESET}}$ and STRTUP=low	1. $\overline{\text{RESET}}$ and STRTUP=high 2. PRS inst. 3. PEX inst.	none	POWER-ON FLAG: Causes entry into panel mode when $\overline{\text{RESET}}$ is released and this flag is set.
GT	none	$\overline{\text{RESET}}$=low	RTF inst.	GREATER THAN FLAG: General purpose flag which has no arithmetic significance.

HARRIS

HD-6121

CMOS I/O CONTROLLER

Features

- LOW POWER, TYP. < 2 mW
- SINGLE SUPPLY – 5V
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 6120 COMPATIBLE INTERFACE
- CONTROLS ANY COMBINATION OF FIVE INPUT OR OUTPUT PORTS WITH HANDSHAKING
- ELIMINATES GATED READ AND WRITE SIGNALS THROUGH THE CONTROLLER
- CONFORMS TO DEC* CONVENTIONS REGARDING DEVICE ADDRESSING AND COMMANDS
- INDEPENDENT PROGRAMMING OF EACH DEVICE'S ADDRESS AND DATA DIRECTION
- COMPLETE INTERRUPT AND SKIP LOGIC FOR EACH DEVICE INCLUDING PRIORITY INTERRUPT VECTORING
- STROBE OUTPUTS ARE PROGRAMMABLE HIGH OR LOW TRUE
- SENSE INPUTS ARE PROGRAMMABLE FOR LEVEL OR EDGE SENSITIVITY
- ENABLE OUTPUTS FUNCTION AS USER PROGRAMMABLE CHIP SELECTS

Description

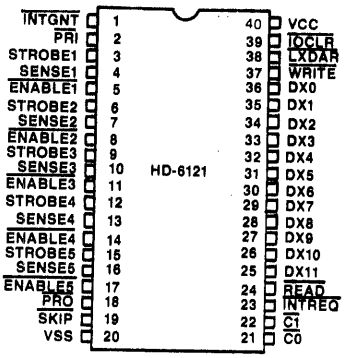
The HD-6121 Input/Output Controller (IOC) is a high performance, CMOS support circuit for the 6120 microprocessor. Fully programmable, this device offers independent control of any combination of five, 12 bit input or output ports.

Used in conjunction with the 6120 microprocessor, the 6121 provides user programmable chip select decoding, priority vectored interrupt control, software readable status and I/O port handshaking signals.

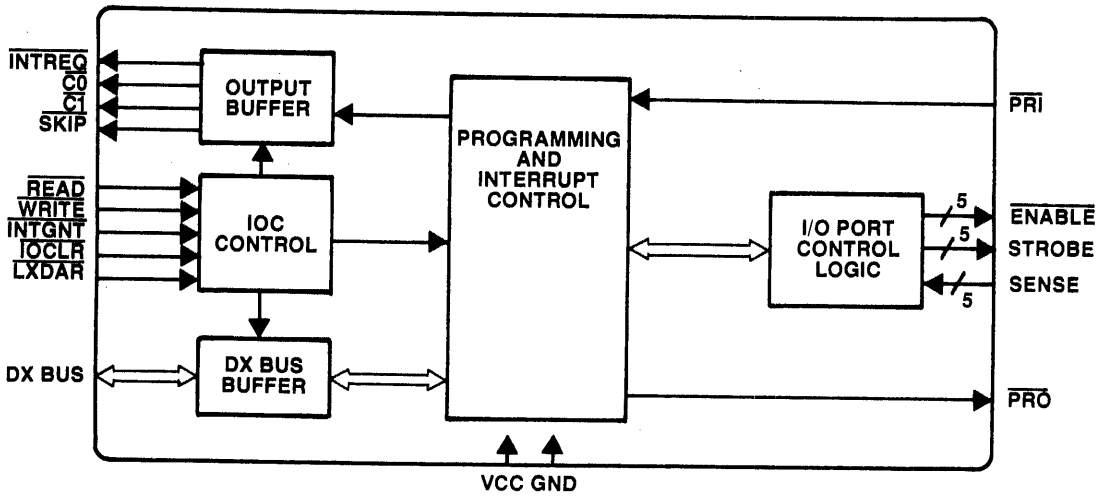
The Priority In ($\overline{PRI}$) and Priority Out ($\overline{PRO}$) control signals permit up to eleven 6121s to be used without any additional hardware. Industrial control and other I/O intensive systems can profit greatly from the highly hardware/software efficient capability provided by the 6120/6121 chip set.

* *TRADEMARK of Digital Equipment Corp.*

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Industrial (−9, −9+)	−40°C to +85°C
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V	Military (−2, −8)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA Except for SKIP, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$ and $\overline{\text{C1}}$ which are open drain.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA Except for $\overline{\text{SKIP}}$, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$ and $\overline{\text{C1}}$.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 15 mA $\overline{\text{SKIP}}$, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$, $\overline{\text{C1}}$ OUTPUTS
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	I/O, OUTPUT LEAKAGE CURRENT	−10	10	μA	OV≤VO≤VCC NOTE 1
ICC	POWER SUPPLY CURRENT		100	μA	VIN=VCC or GND VCC = 5.25 V OUTPUTS OPEN
CIN*	INPUT CAPACITANCE		5	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

NOTE 1: APPLIES ONLY TO DX0 THROUGH DX11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{SKIP}}$, AND $\overline{\text{INTREQ}}$ WITH THE OUTPUT DRIVERS DISABLED OR OPEN DRAIN OUTPUTS OFF.

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A=Industrial or Military; C_L=50 pf,

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAS	ADDRESS SET UP TIME	30		ns	
TAH	ADDRESS HOLD TIME	70		ns	
TRWE	WRITE ENABLE DELAY		100	ns	
TRWD	WRITE DISABLE DELAY		100	ns	
TWS	WRITE SET UP TIME	50		ns	
TWH	WRITE HOLD TIME	50		ns	
TPDE	ENABLE OUTPUT DELAY		125	ns	
TPDD	ENABLE OUTPUT DISABLE DELAY		200	ns	
TRE	READ VECTOR ENABLE		100	ns	
TRD	READ VECTOR DISABLE		100	ns	
TWPD	WRITE PULSE DELAY	100		ns	
TLXH	RESET DELAY, IOCLR TO LXDAR	100		ns	

NOTE: ALL MEASUREMENTS ARE TAKEN WITH INPUT RISE AND FALL TIMES ≤ 20 NSEC

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 50 pf load capacitance specified in the 6121 data sheet is determined by

$$i = C_L\,(dv/dt)$$

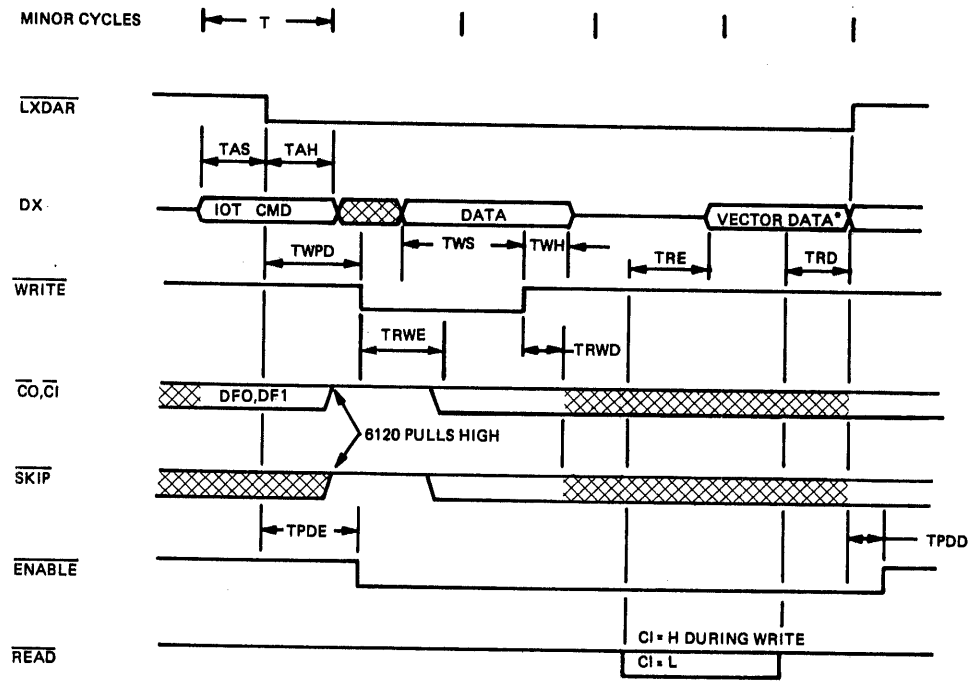
Assuming that all DX outputs change state at the same time and that dv/dt is constant;

$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve outputs.

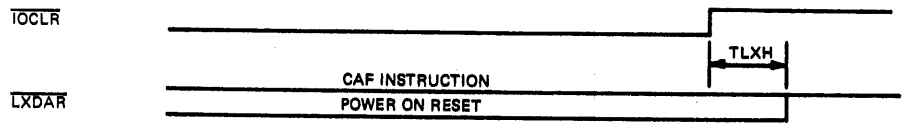
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120\ mA$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.



* *Vector Operation Only*

EXTERNAL IOT and VECTORED INTERRUPT OPERATION



RESET TIMING

I/O	PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
I	1	$\overline{\text{INTGNT}}$	Low	Interrupt grant signal from the 6120.
I	2	$\overline{\text{PRI}}$	Low	Input for priority string. Low implies no higher priority up the string. Device #1 internally is the highest priority device.
O	3, 6, 9, 12, 15	STROBE 1-5	High or Low	Output strobes set true by a transfer command. Cleared by a Set Flag command or by the corresponding sense input going true. Programmable polarity.
I	4, 7, 10, 13, 16	SENSE 1-5	High or Low	Status inputs from an external device. Can cause IOT skips or interrupts. Programmable edge or level sense and polarity.
O	5, 8, 11, 14, 17	$\overline{\text{ENABLE}}$ 1-5	Low	Bus transfer enable pulses for external devices. True during $\overline{\text{LXDAR}}$.
O	18	$\overline{\text{PRO}}$	Low	Output for priority string. Low implies enable for next device down the string. Device #5 internally is the lowest priority device and drives this output.
O	19	$\overline{\text{SKIP}}$	Low	True during $\overline{\text{LXDAR}}$ and $\overline{\text{WRITE}}$ to indicate to the 6120 that a skip is to occur on the current IOT. N-Channel open drain.
	20	VSS		Power supply ground.
O	21, 22	$\overline{\text{C0}}$, $\overline{\text{C1}}$	Low	Control signals to the 6120 which specify the type of transfer required for an I/O instruction. See Table 1. N-Channel open drain.
O	23	$\overline{\text{INTREQ}}$	Low	Interrupt request to the 6120. N-Channel open drain output.
I	24	$\overline{\text{READ}}$	Low	6120 bus read pulse.
I/O	25-36	DX11-0	High	6120 data/address bus. (DXO=MSB, DX11=LSB)
I	37	$\overline{\text{WRITE}}$	Low	6120 bus write pulse.
I	38	$\overline{\text{LXDAR}}$	Low	6120 I/O transfer enable signal. True during the execute phase of external IOT instruction. Also true during power on reset.
I	39	$\overline{\text{IOCLR}}$	Low	Reset from the 6120 generated by power on reset or CAF instruction.
	40	VCC		Positive supply voltage.

CONCEPT:

The concept of the IOC is to provide basic control and enable signals for the devices which it controls but not be involved in the critical speed timing of the DX bus transfers to and from these devices. Each input or output port still has its own output latch or input driver interface which results in maximum flexibility with regard to I/O device characteristics. Because these latches and input drivers are not included in the 6121, this 40 pin device is able to provide complete handshaking for five I/O ports.

Software programmable chip select decoding ($\overline{\text{ENABLE}}$ outputs) provides a means whereby I/O device addressing is readily changed with no change to the users PC board. This on-chip feature replaces the 2-5 IC's normally associated with chip select decoding.

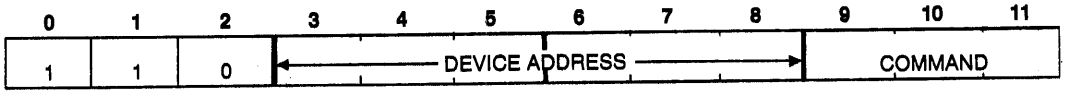
Another feature of the 6121 IOC is an on-chip priority interrupt controller. The interrupt logic includes software programmable vectors and complete interrupt request/grant handshaking for the 6120 microprocessor. This on-chip feature of the 6121 eliminates a separate interrupt controller IC. Up to eleven 6121 IOCs can be daisy chained without the need for any interfacing logic. This results in vectored interrupt control of up to 55 I/O ports. The Priority In ($\overline{\text{PRI}}$) and Priority Out ($\overline{\text{PRO}}$) control signals are used for this I/O expansion capability.

Another major on-chip feature of the 6121 IOC is the inclusion of I/O port handshaking signals. These signals provide the capability of polling the status of an input port (SENSE inputs) and that of signaling an Output port that it has received data (STROBE outputs). These signals can be thought of as "Input Buffer Full" and "Output Buffer Full" status lines. The characteristics of these signals are software programmable which greatly increases their flexibility.

6120 IOT INSTRUCTION SEQUENCING:

The 6121 is designed to interface with the 6120 external IOT sequence. This sequence begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (Bits 0−2=6) whose device code (Bits 3-8) is not 00 or 2X.

EXTERNAL IOT COMMAND FORMAT



The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are available on DX0-11 as $\overline{LXDAR}$ falls near the start of the execute phase. The 6121 IOC accepts the IOT command on the falling edge of $\overline{LXDAR}$ and latches this information into an internal command latch. $\overline{WRITE}$ or $\overline{READ}$ is active low to enable data transfers between the 6120 and the peripheral device(s). The 6121 communicates with the 6120 through 3 control lines... $\overline{C0}$, $\overline{C1}$ and $\overline{SKIP}$. The type of data transfer during an IOT instruction is specified by the peripheral device by asserting the control lines as shown in Table 1.

The control line $\overline{SKIP}$, when low during an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The $\overline{C0}$ and $\overline{C1}$ lines are treated independently of the $\overline{SKIP}$ line. The input command signals, $\overline{C0}$, $\overline{C1}$ and $\overline{SKIP}$, are sampled during $\overline{LXDAR}$ low • $\overline{WRITE}$ low. The data from the 6120 is available to the device(s) during $\overline{LXDAR}$ low • $\overline{WRITE}$ low. If $\overline{C1}$ is low at $\overline{LXDAR}$ low • $\overline{WRITE}$ low, a read is also performed and data is read from the peripheral into the 6120 during $\overline{LXDAR}$ low • $\overline{READ}$ low.

TABLE 1 – PROGRAMMED I/O CONTROL LINES

CONTROL LINES $\overline{C0}$	$\overline{C1}$	OPERATION	DESCRIPTION
High	High	(Device)◄—(AC)	The contents of the AC is sent to the device.
Low	High	(Device)◄—(AC), Clear (AC)	The contents of the AC is sent to the device, then the AC is cleared.
High	Low	(AC)◄—(AC)V(Device)	Data is received from a device,"OR'ed" with the data in the AC and the result stored in the AC.
Low	Low	(AC)◄—(Device)	Data is received from a device and loaded into the AC.

INTERNAL DEVICE CONTROLLER FLIP FLOP DEFINITIONS:

There are five device controllers within the 6121 IOC. Each controller has a set of control and status flip flops which are defined below:

FLAG FLIP FLOP – Internal device control status flip flop which only has meaning if the IS programming bit is a 1. It is set by a SET FLAG IOT or by true going edge of sense input. It is cleared by the SKIP ON FLAG instruction only if it was sampled by that instruction as being set; by the interrupt vector operation; or by $\overline{IOCLR}$. If the flag is set, interrupts can be generated if otherwise enabled. If the IS programming bit is 0, the flag flip flop is held in the cleared state.

FLAG SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the flag flip flop at the falling edge of $\overline{LXDAR}$. The set state of this flip flop causes the skip line to be pulled and the flag flip flop to be cleared during $\overline{WRITE}$ pulses of a skip IOT.

STROBE FLIP FLOP – Internal device control flip flop which controls strobe output line. It is set by a transfer IOT at the trailing edge of the $\overline{LXDAR}$ pulse. It is cleared by $\overline{IOCLR}$, the true going edge of the sense input (if the IS programming bit set) or the SET FLAG IOT command. The STROBE output reflects the state of this flip flop any time the strobe flip flop is cleared or at the end of $\overline{LXDAR}$ if the strobe flip flop is set.

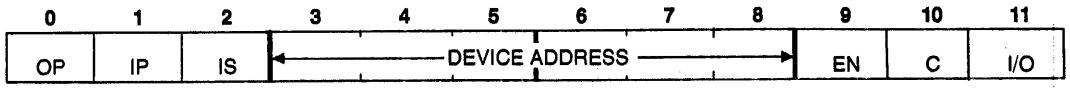
INTERRUPT ENABLE FLIP FLOP – Internal device control flip flop which allows program enable of interrupts. This bit is set by $\overline{IOCLR}$. This bit is loaded by DX11 during $\overline{WRITE}$ of LOAD INTERRUPT ENABLE IOT. If this flip flop and the flag flip flop are both set, then the $\overline{INTREQ}$ pin is pulled low.

INTERRUPT SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the interrupt condition at the falling edge of $\overline{INTGNT}$. The falling edge of $\overline{INTGNT}$ sets the interrupt sample flip flop if the flag flip flop and interrupt enable flip flop are set and the priority input is true. If the flag flip flop is clear or the priority input is false at the fall of $\overline{INTGNT}$, the state of the interrupt sample flip flop is not changed. The interrupt sample flip flop is cleared by the SKIP ON FLAG IOT, by the reset state of the interrupt enable flip flop or by $\overline{IOCLR}$. If this flip flop is set, the device's priority output is false (high).

PROGRAMMING:

Immediately after power on reset, the five device controllers within the IOC are set to a state such that the first IOT command received with $\overline{PRI}$ low will be interpreted as a programming command to set up various IOC parameters. This is true only for power on reset and is *not* true for the reset generated by the 6120 CAF instruction. Power on reset from the 6120 is distinguished by $\overline{LXDAR}$ being low at the end of the $\overline{IOCLR}$ pulse. During the reset caused by the CAF instruction, $\overline{LXDAR}$ is high throughout the $\overline{IOCLR}$ pulse. Each of the five device controllers within the IOC are programmed independently by separate IOT commands. If PRI is low, the first IOT programs the highest priority device (Device #1). The second IOT programs the second highest priority device (Device #2). This continues until all the devices in the IOC are programmed, at which time $\overline{PRO}$ is made low so that programming can commence on the next IOC (if any) down the priority chain. The IOC will not accept any operational IOT commands to any of the five devices until all five devices have been programmed. The programming IOT writes data from the 6120 accumulator. The lower 9 bits of the IOT instruction itself perform no programming function. The IOT instruction must be an external IOT, not device #00 or 2X. The programming format from the accumulator is shown below:

PROGRAMMING COMMAND FORMAT



OP Output polarity
1=High true strobe output
0=Low true strobe output

IP Input polarity
1=High true sense polarity
0=Low true sense polarity

IS Input edge sensitivity
1=Set flag flip flop and interrupt (if interrupts enabled) on true-going edge of sense input. Skip on flag flip flop set.
0=Skip on sense line input level true. (No interrupt on sense true.)

DEVICE ADDRESS The 6 bit device address assigned to the device controller.

EN Enable output control select.
1=Enable output is true (low) whenever the device is addressed. (Except for programming and vector operations.)
0=Enable is true only when a transfer command (4_8 or 6_8) is given.

C C line control.
0=Transfer commands do not cause C lines to be controlled.
1=Transfer commands cause C lines to be controlled.

I/O Input or output port select. This programming bit has no meaning if the "C" programming bit is set to a "0".
1=Transfer commands cause outputs to the device. ($\overline{C1}$ is not pulled low.)
0=Transfer commands cause inputs from the device. ($\overline{C1}$ is pulled low.)

After all five devices of the IOC are programmed, they are ready to respond to IOT commands with their programmed addresses. Because of this, no operational IOT commands can be used until all system IOC's have been programmed. An additional constraint is that each device must have its own unique address.

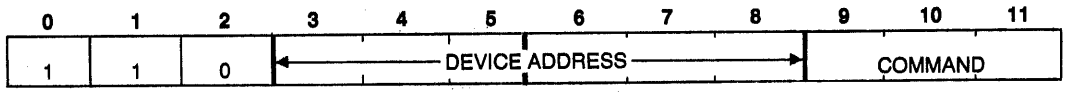
Note that unused devices must be turned off during programming simply by programming them with an internal IOT address (00 or 2X), and with the IS programming bit set to "0" to prevent interrupts. Also, sense inputs must be tied to ground. Internal 6120 IOT's do not generate $\overline{LXDAR}$. The IOT controller is therefore made insensitive to all external IOT commands when programmed with an internal IOT address. Whenever a device controller within the IOC responds to its programming IOT, it pulls the $\overline{C0}$ line low so that the 6120 will perform an output operation from the AC followed by clearing the AC.

IOC COMMANDS:

Power on reset– This is indicated by the $\overline{IOCLR}$ input low and $\overline{LXDAR}$ low at the end of the $\overline{IOCLR}$ pulse. This operation sets up the IOC to be programmed as discussed above. Also, all five flag flip flops are cleared as are the flag sample and interrupt sample flip flops. The interrupt enable flip flops are all set. The strobe flip flops are cleared, the STROBE outputs are set low and the $\overline{ENABLE}$ outputs are set high. Note that if a controller is programmed for a low true STROBE output, then there will be a low to high transition on the strobe output when this device is programmed. Also, care must be taken to assure that the state of the flag, flag sample, interrupt sample, interrupt inhibit and strobe flip flops are *not* disturbed by the programming function.

The 6120 Clear All Flags (CAF) Instruction – This instruction is indicated to the IOC by $\overline{IOCLR}$ going low and $\overline{LXDAR}$ staying high during the $\overline{IOCLR}$ pulse. This operation performs exactly the same operation as power on reset on the device flag, flag sample, interrupt sample, interrupt enable and strobe flip flops. It does not set up the IOC for programming, nor does it disturb the state of any of the programming information stored within the IOC.

EXTERNAL IOT COMMAND FORMAT



	Bit 9	10	11
SET FLAG, CLEAR STROBE	0	0	0
SKIP ON FLAG, CLEAR FLAG	0	0	1
CLEAR ACCUMULATOR (If programmed for input)	0	1	0
NOP	0	1	1
DATA TRANSFER ($\overline{C0}$ not pulled low)	1	0	0
LOAD INTERRUPT ENABLE (From DX11)	1	0	1
DATA TRANSFER ($\overline{C0}$ pulled low)	1	1	0
NOP	1	1	1

Each IOT is discussed below:

SET FLAG, CLEAR STROBE – If the device is programmed for edge sensitive SENSE input, this IOT command causes the internal flag flip flop to be set and also clears the STROBE output to the programmed false state. If the device is programmed for level sensitive SENSE input, then the flag flip flop is not set by this instruction, but the STROBE output is cleared.

SKIP ON FLAG, CLEAR FLAG – The skip on flag operation depends on whether the device is programmed for edge or level sensitivity. If programmed for level sensitivity and the SENSE input is logic true, then the $\overline{SKIP}$ line is pulled low during the IOT $\overline{WRITE}$ pulse; the clear flag operation has no meaning. If programmed for edge sensitivity, then the state of the flag flip flop is sampled to the flag sample flip flop at the falling edge of $\overline{LXDAR}$. During the IOT $\overline{WRITE}$ pulse, the $\overline{SKIP}$ line will be pulled low if the flag sample flip flop is true. If the flag sample flip flop is set, then the flag flip flop will be cleared some time before or at the trailing edge of $\overline{LXDAR}$.

CLEAR ACCUMULATOR – This command only functions if the C line control programming bit (bit 10=1) has been programmed for the device to control the C lines and the device has been programmed as an input device (bit 11=0). When enabled by the above two programming conditions, this command will cause $\overline{C0}$ to be pulled low during the IOT $\overline{WRITE}$ pulse. This will cause the 6120 accumulator to be cleared.

DATA TRANSFER (4_8 or 6_8) – Either transfer command will unconditionally set the STROBE output to its true state. If the "C" programming bit is set, the transfer commands will also cause the "C" lines to be controlled to specify the type of I/O transfer to be performed. If not, then the IOC device does not control the "C" lines. If the device "I/O" programming bit is 1, then $\overline{C1}$ is not pulled low and an output transfer is specified by either 4_8 or 6_8. If the I/O programming bit is 0, then an input transfer is specified by pulling $\overline{C1}$ low during the $\overline{WRITE}$ pulse. Command 4_8 does not pull $\overline{C0}$ low. For an output, this corresponds to not clearing the AC after the output. For an input, this corresponds to "OR'ing" the input data with the AC. Command 6_8 always pulls $\overline{C0}$ low. For an output, this causes the AC to be cleared following the output. For an input, this corresponds to the input data being loaded into the AC. The STROBE output is cleared when the flag flip flop is set by the SENSE transition or by a SET FLAG command.

LOAD INTERRUPT ENABLE – This command causes a write of 6120 AC bit 11 to the addressed device's interrupt enable flip flop. This write holds neither $\overline{C0}$ nor $\overline{C1}$ low so that a write without a clear of the AC is performed. The device is incapable of generating interrupts if the interrupt enable flip flop is cleared.

INTERRUPT LOGIC:

A device controller within the IOC is capable of generating an interrupt by pulling the $\overline{INTREQ}$ line low if all of the following conditions are true:

1. The device is programmed for edge sensitive SENSE input, and
2. The device flag flip flop has been set, and
3. The device interrupt enable flip flop is set, and
4. The priority string input for that device is true.

Normally, with no system interrupts outstanding, all device priority inputs and outputs are low. At the highest priority IOC, the $\overline{PRI}$ input must be tied to V_{SS}.

Whenever the interrupt conditions are met at any device on the IOC, the $\overline{INTREQ}$ line is pulled low and the following sequence of events occurs:

1. The 6120 $\overline{INTREQ}$ being low causes $\overline{INTGNT}$ low. All IOC driving device controllers which have the interrupt condition met set their interrupt sample flip flops. Note that this is an edge triggered *set* and is *not* a "load". All device controllers which have their interrupt sample flip flops set will hold their respective priority outputs high. All device controllers with a high priority input hold their priority outputs high and also are inhibited from driving the $\overline{INTREQ}$ bus low.
2. When the first IOT is executed with $\overline{INTGNT}$ low, one of two events occurs, depending on the IOT command:

a. If the command issued is a SKIP ON FLAG (1_8) command, then the normal operation of the IOT command occurs in the addressed device. A SKIP ON FLAG (1_8) instruction will clear the interrupt sample flip flop of the addressed device and will clear the flag flip flop if it is set.

b. If the command is not a SKIP ON FLAG (1_8) command, then the fact that $\overline{INTGNT}$ is low causes special action. During the $\overline{WRITE}$ pulse $\overline{C0}$ and $\overline{C1}$ are both pulled low by the highest priority device with its interrupt sample flip flop set. No other device (not even the addressed device) will respond on this IOT. This IOT specifies a JAM read cycle. The 6120 then generates a $\overline{READ}$ pulse which causes the device address of the highest priority device with its interrupt sample flip flop set to put its device address on DX6-11 and all zeros on DX0-5. Also, the flag flip flop of that device is cleared, causing it to remove the $\overline{INTREQ}$ drive. The interrupt sample flip flop is not cleared at this time so that the priority output of that device continues to be held false (high).

c. Near the end of the interrupt service routine of that particular device, the software should (with the 6120 interrupts disabled) execute a SKIP ON FLAG IOT to the device. This will clear the interrupt sample flip flop of the device, which in turn will set the priority output of that device true, enabling interrupts from devices lower in the chain.

SOFTWARE NOTES:

1. When performing the interrupt vector operation from the 6120, the accumulator must be loaded with a "no interrupt" vector address (such as zero) before the vector IOT is issued. This vector is left in the accumulator if no internal vector is returned by a device controller.
2. Before a device's interrupts are turned off by resetting its interrupt enable flip flop with a 6XX5 command the 6120's interrupts must be turned off. Failure to do so can result in an unidentifiable interrupt from the device.
3. When turning on a device's interrupt with a 6XX5 command, an immediate interrupt will result if the device's flag is set and the 6120 interrupts are turned on.
4. Because the IOC programming sequence relies on an exact sequence of IOT instructions to be executed and $\overline{IOCLR}$ enables interrupts, the programming instructions must be executed with the 6120's interrupts off.
5. Use of the level sensitive "Skip on Flag, Clear Flag" operation (6xx1), requires that a redundant skip instruction followed by a NOP be used to guarantee that the "Flag Sample Flip Flop" is reset.

TESTING NOTE:

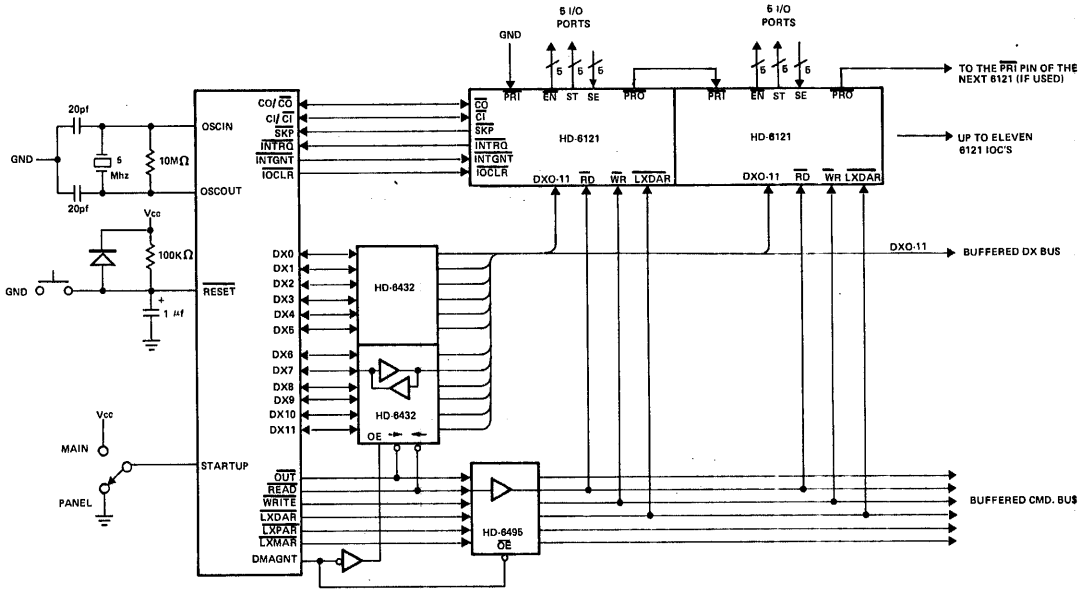
The $\overline{PRO}$ line cannot go true after any $\overline{IOCLR}$ true pulse (either in programming or in a CAF) until there is at least one $\overline{READ}$ pulse. In addition, no external IOT commands can be executed during an $\overline{IOCLR}$ true pulse.

SUMMARY OF 6120, 6121 CONDITIONS:

The following table provides a brief summary of all the 6120 and 6121 Operations.

IOT COMMANDS BIT 9	BIT 10	BIT 11	PROGRAMMING BITS C	I/O	OUTPUTS $\overline{C0}$	$\overline{C1}$	6120 OPERATION	6121 OPERATION
0	1	0	1	1	HiZ	HiZ	Output (AC)	NOP
1	0	0	1	1	HiZ	HiZ	Output (AC)	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
1	1	0	1	1	Low	HiZ	Output (AC) then (AC)◄— 0	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
0	1	0	1	0	Low	HiZ	Output (AC) then (AC)◄—0	NOP except for low $\overline{C0}$ output. Result is only to clear 6120 AC.
1	0	0	1	0	HiZ	Low	(AC)◄— Input V(AC)	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	1	0	1	0	Low	Low	(AC)◄—Input	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	0	1	X	X	HiZ	HiZ	Output (AC)	Load interrupt enable flip flop from DX11.
0	0	0	X	X	HiZ	HiZ	Output (AC)	Set flag flip flop if its prog. bit is set. Clear STROBE output.
0	0	1	X	X	HiZ	HiZ	Output (AC)	Pull $\overline{\text{SKIP}}$ low and clear Flag F.F. if flag sample flip flop is a 1 during the write pulse.
X	1	1	X	X	HiZ	HiZ	Output (AC)	No operation.
Vector Read			X	X	Low	Low	(AC)◄— Input	Place interrupt vector on DX bus, clear Flag F.F.
Programming IOT			X	X	Low	HiZ	Output (AC) then (AC)◄—0	Load programming information to device programming register from the DX bus during write.

BUFFERED BUS 6120/6121 INTERFACING EXAMPLE



NOTE: This simplified example does not show the extended Memory Addressing and other features of the 6120.

HARRIS

HM-6100

CMOS 12 BIT MICROPROCESSOR (CPU)

Features

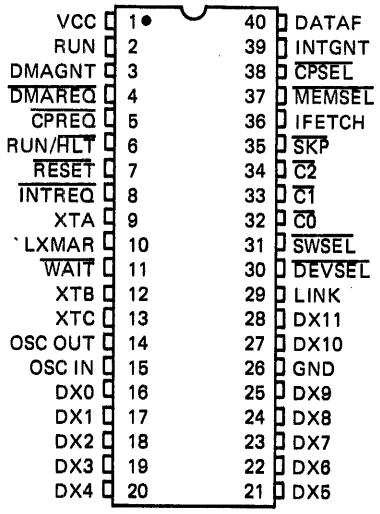
- LOW POWER - TYP.$<$ 5.0μW
- SINGLE +5V POWER SUPPLY
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- 12-BIT DATA WORD
- OVER 90 SINGLE WORD INSTRUCTIONS
- RELOCATABLE MEMORY ORGANIZATION
- BASIC ADDRESSING TO 4K 12 BIT WORDS
- PROVISION FOR DEDICATED CONTROL PANEL
- 128 GENERAL PURPOSE REGISTERS
- 8 AUTOINDEXING REGISTERS
- FLEXIBLE PROGRAMMED I/O TRANSFERS
- VECTORED INTERRUPT CAPABILITY

Description

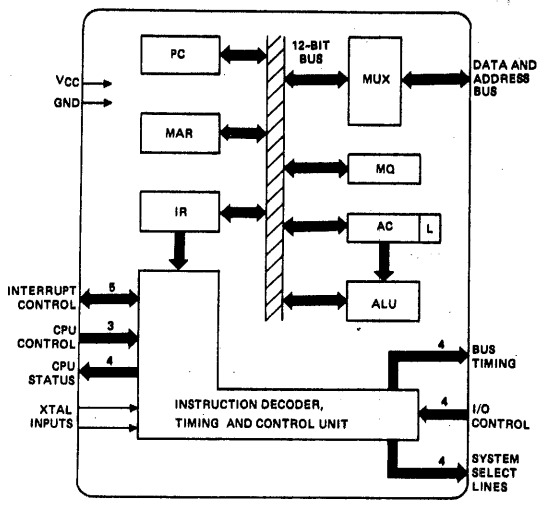
The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit two's complement arithmetic. It is a general purpose processor which recognizes the instruction set of Digital Equipment Corporation's PDP-8/E Minicomputer.

Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart. Five 12-bit registers are used to control microprocessor operations, address memory, perform arithmetic or logical operations, and store data. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

Pinout



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100-9	-40°C to +85°C
Military HM-6100-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-1.0		+1.0	μA	0V≤VIN≤VCC
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		+1.0	μA	0V≤VO≤VCC
ICC1	Supply Current (Static)			400	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			2.5	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V (1)		TA = Indust. VCC = 5.0 ± 10%V		TA = Military VCC = 5.0 ± 10%V			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
fMAX	Max Operating Frequency		4.0		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	500		600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	220		230		355		ns	
TAS	Address Setup Time	80		85		200		ns	
TAH	Address Hold Time	150		125		175		ns	
TAL	Access Time from LXMAR		450		520		745	ns	
TEN	Output Enable (Memory)		250		300		470	ns	
TEND	Output Enable (I/O)		300		470		655	ns	
TWP	Write Pulse Width	200		235		330		ns	
TDS	Data Setup (Memory)	160		135		250		ns	
TDSD	Data Setup (I/O)	185		225		350		ns	
TDH	Data Hold Time	125		125		170		ns	
TST	Status Signals Valid		250		300		325	ns	
TRS	Request Inputs Setup	0		0		0		ns	
TRH	Request Inputs Hold	200		250		300		ns	
TWS	Wait Setup Time	0		50		50		ns	
TWH	Wait Hold Time	100		100		150		ns	
TRHS	Run Halt Setup Time	0		50		50		ns	
TRHP	Run Halt Pulse Width	100		100		150		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

Specifications HM-6100C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0 ± 5% Volts, T_A = Industrial

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			.8	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-10		+10	μA	0V≤VIN≤VCC
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	0V≤VO≤VCC
ICC1	Supply Current (Static)			600	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			5.0	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC=5.0V(1)		TA = Indust. VCC = 5.0 ± 5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT	TEST CONDITION
fMAX	Max operating Freq.		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	270		335		ns	
TAS	Address Setup Time	100		120		ns	
TAH	Address Hold Time	150		175		ns	
TAL	Access Time from LXMAR		500		650	ns	
TEN	Output Enable (Memory)		300		400	ns	
TEND	Output Enable (I/O)		350		575	ns	
TWP	Write Pulse Width	250		320		ns	
TDS	Data Setup (Memory)	180		240		ns	
TDSD	Data Setup (I/O)	200		275		ns	
TDH	Data Hold Time	130		175		ns	
TST	Status Signals Valid		300		350	ns	
TRS	Request Inputs Setup	0		0		ns	
TRH	Request Inputs Hold	100		130		ns	
TWS	Wait Setup Time	0		0		ns	
TWH	Wait Hold Time	100		130		ns	
TRHS	Run Halt Setup Time	0		70		ns	
TRHP	Run Halt Pulse Width	100		130		ns	

Note 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

Timing and State Control

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 1.

T1 For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T2 Memory/Peripheral data is read for an input transfer (READ). $\overline{\text{WAIT}}$ controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers, the CPU waits in the T2 state. The wait duration is an integral multiple of the crystal frequency - 250ns for 4MHz.

For Memory reference instructions, the Memory Select, $\overline{\text{MEMSEL}}$, lines are active. For I/O instruction the $\overline{\text{DEVSEL}}$, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$, and SKP are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, $\overline{\text{CPSEL}}$, and Switch Register Select, $\overline{\text{SWSEL}}$, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T3, T4, T5
ALU operation and internal register transfers.

T6 This state is entered for an output transfer (WRITE). The address is defined during T1. $\overline{\text{WAIT}}$ controls the time for which the WRITE data must be maintained.

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single clocked.

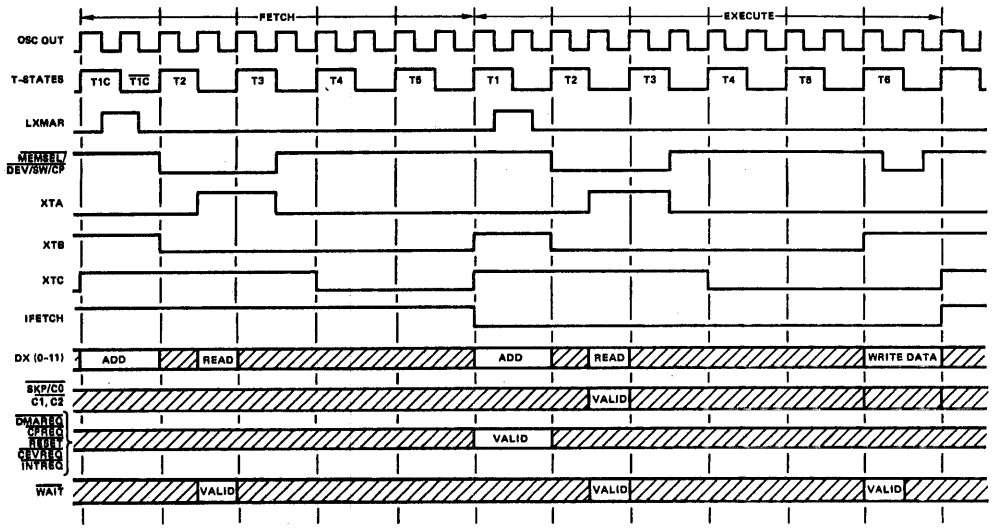


FIGURE 1 – Static Timing

The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications) It defines the interface requirements for memory and I/O devices on the bus.

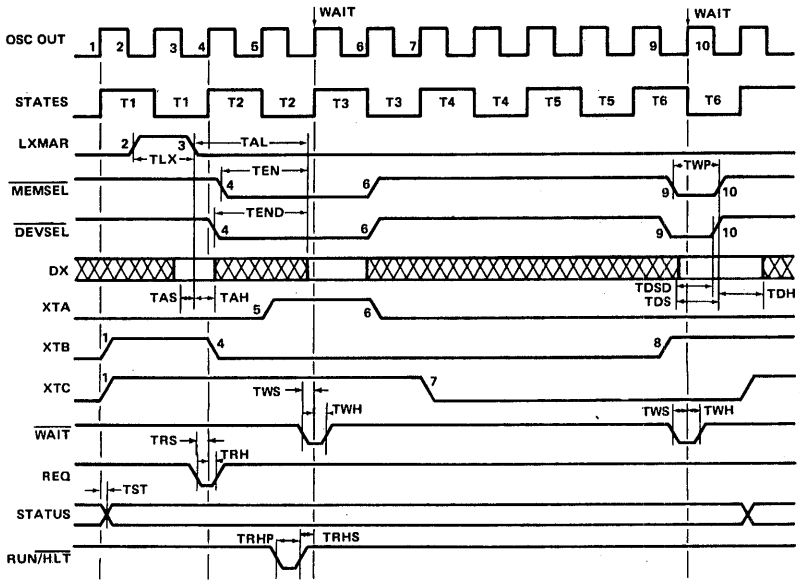


FIGURE 2 – Dynamic Timing

Microprocessor Architecture

The block diagram of the CPU architecture, shown on the front page, consists of the following major functional segments:

- CPU Registers
- Arithmetic and Logic Unit
- Dx-Bus Multiplexer
- Timing and Control Unit

Each one is briefly described below.

CPU REGISTERS

The CPU consists of five, 12-bit registers, of which three are user programmable; 1) Accumulator (AC), 2) Program Counter (PC), and 3) Multiply Quotient (MQ). The remaining two registers are the Instruction Register (IR) and the Memory Address Register (MAR) which are used exclusively for internal operations. The CPU registers are defined as follows.

ACCUMULATOR AND LINK (AC/L)

All arithmetic and logical operations are performed in the AC. For any arithmetic operation, the AC data and memory data are combined in the ALU and the result is temporarily stored in the AC. Under software control, the AC can be cleared, set, complemented, incremented, tested or rotated. Using the Operate Microinstructions, a variety of register operate instructions can be derived.

The link is a one-bit extension of the AC. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the AC. It also serves as the carry output for two's complement arithmetic.

MULTIPLY QUOTIENT (MQ)

The MQ register can be used as a temporary storage for the AC. The MQ may be OR'ed with the AC and the result stored in the AC or the contents of the AC and MQ may be swapped. The MQ is used in conjunction with the AC to perform multiplication, division, and double-precision operations.

PROGRAM COUNTER (PC)

The PC supports both memory and input-output device operations. For memory operations, the PC is controlled exclusively by internal logic and instructions fetched from memory. During an instruction fetch cycle the contents of the PC are transferred to the memory address register (MAR) while the current instruction is being decoded. The PC is then loaded with a new address or simply incremented for the next instruction depending upon the type of instruction. The next instruction obtained from memory is then loaded into the Instruction Register. For example, if the instruction is a JMP X, then the branch address X is loaded into the PC for program controlled branching.

Branching can also be controlled by an external device during input-output operations. This feature allows I/O controlled vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)

The MAR contains the address of the memory location that is currently selected for memory or I/O read-write operations. It is also used for microprogram control during data transfers to and from memory and peripherals.

INSTRUCTION REGISTER (IR)

The instruction fetched from memory is held in the IR while being interpreted by the Instruction Decoder. The IR specifies the initial step of the microprogram sequence for each instruction and is also used to store temporary data for microprogram control.

ARITHMETIC AND LOGIC UNIT (ALU)

The ALU performs 12-bit arithmetic, logical and rotate operations. Its input is derived from the AC and any one of the other CPU registers. The type of operations performed by the ALU include:

ADD	Left-right shifts and rotates
Logical AND	Increment
Logical OR	Complement
Test AC	Set/Clear

DX-BUS MULTIPLEXER

To keep the CPU pin count to a reasonable 40 and still maintain a 12-bit word structure, the address and data paths are multiplexed by the DX-Bus Multiplexer. It handles data, address and instruction transfers between the CPU and memory or peripheral devices on a time-multiplexed basis.

TIMING AND CONTROL UNIT

The Timing and Control Unit generates the state and cycle timing signals from a single-phase clock and maintains the proper sequences of events required for any processing task. It also decodes the instruction obtained from the IR and combines the result with various timing signals and external control inputs to provide control and gating signals required by other functional units (both internal and external to the CPU).

Memory Organization

The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended to 32K words by Extended Memory Control hardware. Every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). The Memory is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

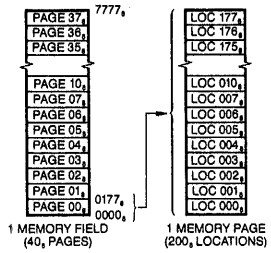


FIGURE 3 – Memory Organization

Memory and Processor Instructions

The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instruction and data; it can manipulate instructions as stored variables or execute data as instructions. There are three general classes of HM-6100 instructions. They are Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOT).

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the "current" instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), 0000_8-0177_8, by definition, denotes the first 128 words of memory and is called the Register Page.)

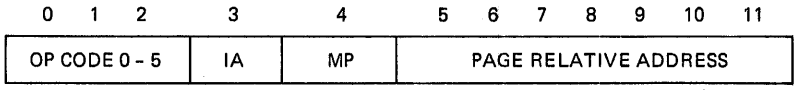
Since the HM-6100 is a static design it can operate at any crystal frequency from 0 to 8MHz. State times required for execution are given for each instruction. Execution time can be calculated from the equation:

$$T = N*(2*(1/F))$$

where N is the number of state times and F is the crystal or input clock frequency.

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 4.



IA: Indirect Addressing 0 = Direct; 1 = Indirect
MP: Memory Page 0 = Register Page; 1 = Current Page

FIGURE 4 – Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR REGISTER PAGE BIT. If bit 4 is a 0, the page address is interpreted as a location on the Register Page. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

By this Method, 256 locations may be directly addressed, 128 on the REGISTER PAGE and 128 on the CURRENT PAGE. Other locations are addressed by using bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in the REGISTER PAGE or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location. Note that locations 0010_8-0017_8 in the Register Page are AUTOINDEXED. When these locations are used for index registers their contents are incremented by 1 and restored before they are used as the operand address. These locations are therefore convenient for indexing applications.

Combinations of mode and page bits yield four (4) addressing modes:

- Current Page, Direct
- Current Page, Indirect
- Register Page, Direct
- Register Page, Indirect

A fifth addressing mode results from use of the AUTOINDEX registers:

- Register Page, Autoindexed

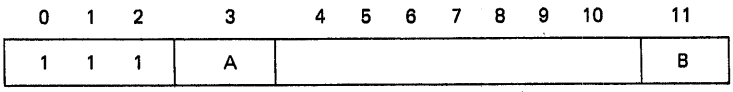
TABLE 1

MNE-MONIC	OP CODE	NUMBER OF STATES			OPERATION
		DIRECT	INDIRECT	AUTO-INDEXED	
AND	0XXX	10	15	16	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (XXX) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1XXX	10	15	16	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a LOAD from memory.
ISZ	2XXX	16	21	22	INCREMENT AND SKIP IF ZERO: The contents of the effective address are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3XXX	11	16	17	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4XXX	11	16	17	JUMP TO SUBROUTINE: The contents of the PC are stored in the effective address and the effective address + 1 is stored in the PC. The link, AC, and MQ are unchanged.
JMP	5XXX	10	15	16	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.
IOT	6XXX	17			INPUT/OUTPUT TRANSFER: Used to initiate the operation of peripheral devices and to transfer data between the peripherals and the CPU.
OPI	7XXX				OPERATE Instructions: Used to perform logical operations on the contents of the major registers.
		10			2 - Cycle OPERATE
		15			3 - Cycle OPERATE

Operate Instructions

The Operate Instructions, which have an OPCODE of 7g(111), consist of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 5. Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third, and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

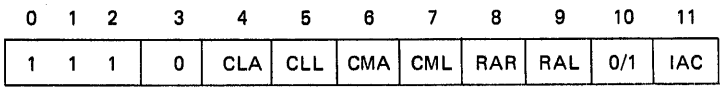


MICROINSTRUCTION	A	B
Group 1	0	0/1
Group 2	1	0
Group 3	1	1

FIGURE 5 – Basic OPR Instruction Format

GROUP 1 MICROINSTRUCTIONS

Figure 6 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 6.



Logical Sequences:
1- CLA CLL
2 - CMA CML
3 - IAC
4 - RAR RAL RTR RTL BSW

BIT 8	BIT 9	BIT 10	FUNCTION
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR

FIGURE 6 – Group 1 Microinstruction Format

Table 2-1 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, and the number of states. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

There are several commonly used microprogrammed combinations of group 1 microinstructions. These are listed in Table 2-2. When writing programs it is necessary to load various constants into the AC for such purposes as initiallizing counters and to provide comparisons. Table 2-3 lists those constants which can be loaded directly via microprogrammed combinations of group 1 instructions.

TABLE 2 - 1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION - This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
CLA	7200	1	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary 0's.

FIGURE 2 - 1 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLL	7100	1	10	CLEAR LINK - The link is loaded with a binary 0.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR - The content of each bit of the AC is complemented. This has the effect of replacing the contents of the AC with its one's complement.
CML	7020	2	10	COMPLEMENT LINK - The content of the link is complemented.
IAC	7001	3	10	INCREMENT ACCUMULATOR - The content of the AC is incremented by one (1) and the carry out componments the Link (L).
BSW	7002	4	15	BYTE SWAP - The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC(0) is swapped with AC(6), AC(1) with AC(7), etc. The link is not affected.
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT - The content of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(11). The ROTATE instructions use what is commonly called a circular shift, meaning that any bit rotated off one end of the accumulator will reappear at the other end.
RTL	7006	4	15	ROTATE TWO LEFT - The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT - The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).
RTR	7012	4	15	ROTATE TWO RIGHT - The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).

TABLE 2 - 2

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLA CLL	7300	1	10	CLEAR ACCUMULATOR - CLEAR LINK
CIA	7041	2, 3	10	COMPLEMENT AND INCREMENT ACCUMULATOR - The content of the AC is replaced with its two's complement. The carry out complements the link. This is a microprogrammed combination of CMA and IAC.
STL	7120	1, 2	10	SET THE LINK - The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
STA	7240	1, 2	10	SET THE ACCUMULATOR - Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.
CLA IAC	7201	1, 3	10	Sets the accumulator to a 1.

TABLE 2 - 2 Continued

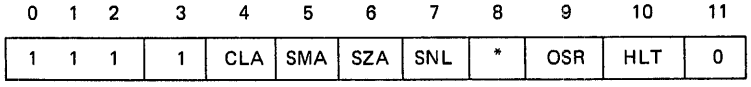
MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
GLK	7204	1, 4	15	GET LINK - The AC is cleared and the content of the link is shifted into AC(11) while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.
CLL RAL	7104	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR LEFT
CLL RTL	7106	1, 4	15	CLEAR LINK - ROTATE TWO LEFT
CLL RAR	7110	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR RIGHT
CLL RTR	7112	1, 4	15	CLEAR LINK - ROTATE TWO RIGHT

TABLE 2 - 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	DECIMAL CONSTANT	INSTRUCTIONS COMBINED
NL0000	7300	1	10	0	CLA CLL
NL0001	7301	1, 3	10	1	CLA CLL IAC
NL0002	7305	1, 3, 4	15	2	CLA CLL IAC RAL
NL0003	7325	1, 2, 3, 4	15	3	CLA CLL CML IAC RAL
NL0004	7307	1, 3, 4	15	4	CLA CLL IAC RTL
NL0006	7327	1, 2, 3, 4	15	6	CLA CLL CML IAC RTL
NL0100	7303	1, 3, 4	15	64	CLA IAC BSW
NL2000	7332	1, 2, 4	15	1024	CLA CLL CML RTR
NL3777	7350	1, 2, 4	15	2047	CLA CLL CMA RAR
NL4000	7330	1, 2, 4	15	-0	CLA CLL CML RAR
NL5777	7352	1, 2, 4	15	-1025	CLA CLL CMA RTL
NL6000	7333	1, 2, 3, 4	15	-1024	CLA CLL CML IAC RTR
NL7775	7346	1, 2, 4	15	-3	CLA CLL CMA RTL
NL7776	7344	1, 2, 4	15	-2	CLA CLL CMA RAL
NL7777	7340	1, 2	10	-1	CLA CLL CMA

GROUP 2 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 2 microinstructions, Bits 4 - 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 - 7 or 9 - 10 is set, the instruction is a microprogrammed combination group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 7.



Logical Sequences:
1 (BIT 8 = 0) -SMA or SZA or SNL
(BIT 8 = 1) -SPA or SNA or SZL
2 -CLA
3 -OSR, HLT

* Reverse sensing BIT:
Unconditional SKIP when
BITS 5, 6, & 7 are 0's

FIGURE 7 — Group 2 Microinstruction Format

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or when bit 8 is 1, the decision will be based on the logical AND.

TABLE 3-1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION - See Group 1 microinstructions.
CLA	7600	2	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary O's.
HLT	7402	3	10	HALT - Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
SKP	7410	1	10	SKIP - The content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK - The content of L is sampled; the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK - The instruction is skipped if the link contains a 0.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR - The content of the AC is sampled; the next sequential instruction is skipped if all AC bits are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR - The next instruction is skipped if any one bit of the AC contains a 1. If every bit in the AC is 0, the next instruction is executed.
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR - If the content of AC(0) contains a negative two's complement number, the next sequential instruction is skipped. If AC(0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR - If the content of AC(0) contains a 0, indicating a positive two's complement number, the next sequential instruction is skipped.
OSR	7404	3	15	OR WITH SWITCH REGISTER - The content of the Switch Register is inclusively OR'ed with the content of the AC and the result stored in the AC. The HM-6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B. This instruction provides the simplest way to input data to the HM-6100 from peripherals.
LAS	7604	1, 3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER - The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.

Table 3 - 2 lists every legal combination of skip microinstructions, along with the resulting condition upon which the decision to skip or execute the next sequential instruction is based. When these combinations include a CLA, the accumulator is cleared after the decision is made. This is a useful trick to save code when a new value will be TAD'ed into the AC.

TABLE 3 - 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
SZA SNL	7460	1	10	Skip if AC = 0 or L = 1 or both.
SNA SZL	7470	1	10	Skip if AC $\neq$ 0 and L = 0.
SMA SNL	7520	1	10	Skip if AC $<$ 0 or L = 1 or both.
SPA SZL	7530	1	10	Skip if AC $\geq$ 0 and L = 0.
SMA SZA	7540	1	10	Skip if AC $\leq$ 0.
SPA SNA	7550	1	10	Skip if AC $>$ 0.
SMA SZA SNL	7560	1	10	Skip if AC $\leq$ 0 or L = 1 or both.
SPA SNA SZL	7570	1	10	Skip if AC $>$ 0 and L = 0.

When writing an actual program, it is useful to think in terms of the FORTRAN relational operators - .LT., .EQ., etc.- when trying to compare numbers. The following method along with Table 3 - 3 will provide this.

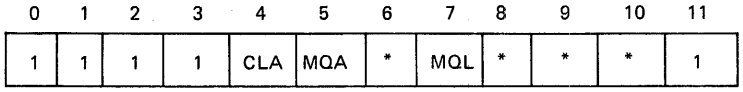
```
CLA CLL              / Initialize AC and Link
TAD B                /Fetch 2nd number
CML CMA IAC          /Create "-B" (AC & L act like a 13 bit accumulator)
TAD A                /Fetch 1st number
Test  CLA            /Use instructions from Table 3 - 3 to provide test
                     /The CLA is optional to provide a clear AC after test
JMP FAIL             /Branch to FAIL routine if test failed
...                  /Test passed, continue with program
...
```

TABLE 3 - 3

SKIP IF	UNSIGNED COMPARE	SIGNED COMPARE
A. NE. B	SNA	SNA
A. LT. B	SNL	SMA
A. LE. B	SNL SZA	SMA SZA
A. EQ. B	SZA	SZA
A. GE. B	SZL	SPA
A. GT. B	SZL SNA	SPA SAN

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8.



Logical Sequences: *Don't care
1 - CLA
2 - MQA, MQL
3 - NOP

FIGURE 8 - Group 3 Microinstruction Format

TABLE 4

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION - See group 1 microinstructions.
CLA	7600	1	10	CLEAR ACCUMULATOR
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR - The content of the MQ is logical OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
MQL	7421	2	10	MQ REGISTER LOAD - The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost. This is similar to a DCA instruction.
ACL	7701	1, 2	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR - This is equivalent to a microprogrammed combination of CLA and MQA. It is similar to the two instruction combination of CLA and TAD.
CAM	7621	1, 2	10	CLEAR ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogram combination of CLA and MQL.
SWP	7521	2	10	SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are interchanged by accomplishing a microprogrammed combination of MQA and MQL.
CLA SWP	7721	1, 2	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

Input Output Transfer Instructions (IOT)

The input/output transfer instructions, which have an OPCODE of 6_8 are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, Transfers variable-size blocks of data between high-speed peripherals and the memory with minimum of program control required by the HM-6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer instruction format is represented in Figure 9.

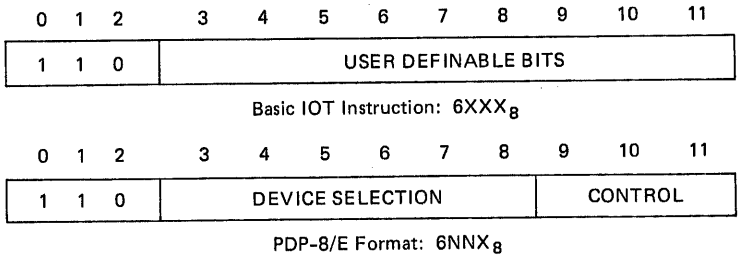


FIGURE 9 — IOT Instruction Format

The first three bits, 0 - 2, are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3 - 11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3 - 8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9 - 11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT (2). This is referred to an IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOTA and IOTB. Bits 0 - 11 of the IOT instruction are available on DX0 - 11 at IOTA ^ LXMAR (3). These bits must be latched in an external address register. $\overline{\text{DEVSEL}}$ is active low to enalbe data transfers between the HM-6100 and the peripheral device (4) & (5). Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines - $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Tables 5-1 and 5-2.

The control line $\overline{\text{SKP}}$, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C0, C1, and C2 lines are treated independently of the $\overline{\text{SKP}}$ line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX0 - 11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$, are sampled during IOTA on the rising edge of time state 3 (4). The data from the HM-6100 is available to the device during $\overline{\text{DEVSEL}}$ ^ $\overline{\text{XTC}}$ (5). The IOTB cycle is internal to the HM-6100 to perform the operations requested during IOTA. Both IOTA and IOTB consists of six (6) internal states.

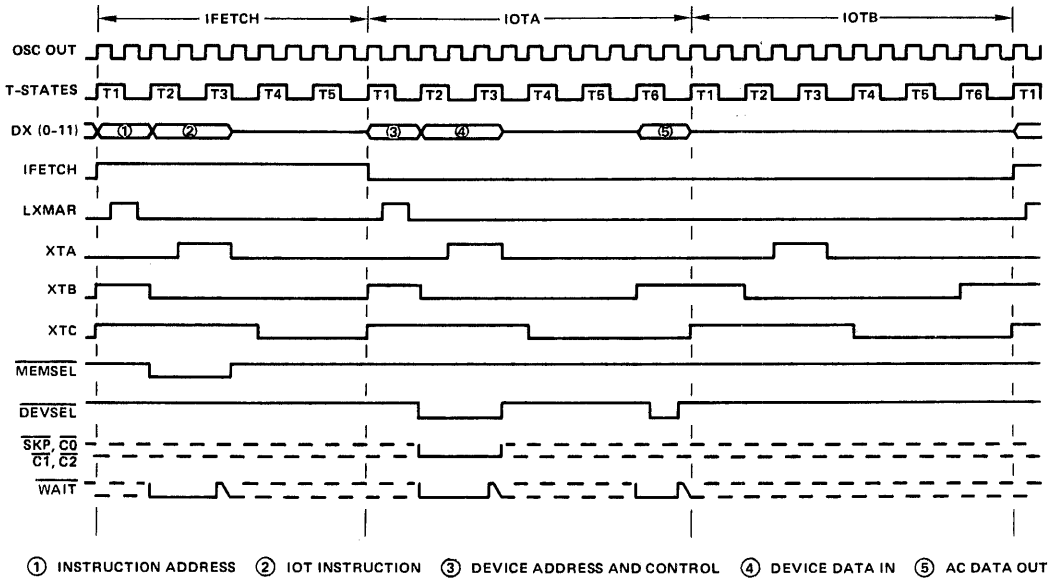


FIGURE 10 – Input-output instruction timing

TABLE 5 - 1
AC DATA TRANSFERS

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	DEV ← AC	The content of the AC is sent to the device.
H	L	H	H	DEV ← AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	H	L	H	AC ← AC V DEV; DEV ← AC	Data is received from a device OR'ed with the data in the AC and the result is stored in the AC. The new AC content is sent to the device.
H	L	L	H	AC ← DEV; DEV ← AC	Data is received from a device and loaded into the AC. The new AC content is sent to the device.
L	H	H	H	DEV ← AC; PC ← PC + 1	The content of the AC is sent to the device and the microprocessor skips the next sequential instruction.
L	L	H	H	DEV ← AC; CLA; PC ← PC + 1	The content of the AC is sent to a device, the AC is cleared, and the microprocessor skips the next sequential instruction.
L	H	L	H	AC ← AC V DEV; DEV ← AC; PC ← PC + 1	Data is OR'ed into the AC, the new AC sent to the device, and the microprocessor skips the next sequential instruction.
L	L	L	H	AC ← DEV; DEV ← AC PC ← PC + 1	Data is loaded into the AC, the new AC contents sent to the device, and the next sequential instruction skipped.

TABLE 5 - 2
PC VECTOR TRANSFERS

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$		
H	*	H	L	PC ← PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
H	*	L	L	PC ← DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.
L	*	H	L	PC ← PC + DEV; PC ← PC + 1	The RELATIVE JUMP is performed and then the microprocessor skips the next sequential instruction.
L	*	L	L	PC ← DEV; PC ← PC + 1	The ABSOLUTE JUMP is executed and then the next sequential instruction is skipped.

* Don't Care

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that is requires some sort of intervention from the running program.

TABLE 6
PROCESSOR IOT INSTRUCTIONS

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON - If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON - The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction.
IOF	6002	INTERRUPT TURN OFF - The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST - The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS - The following machines states are read into the indicated bits of AC. bit 0 - Link bit 1 - Greater than flag* bit 4 - Interrupt Enable FF* bit 2 - INT request bus bit 5 - User flag* bit 3 - Interrupt Inhibit FF* bit 6 - 11 - Save Field Register* * These bits are modified by external devices driving the DX bus and the $\overline{C}$-lines ($\overline{C0}$ = L, $\overline{C1}$ = L). For example, bits 1 and 6 - 11 are part of the Extended Memory Control.
RTF	6005	RETURN FLAGS - Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control). ($\overline{C0}$ = H, $\overline{C1}$ = H)
SGT	6006	SKIP ON GREATER THAN FLAG - Operation is determined by external devices, if any. This flag is external and must control the skip line.
CAF	6007	CLEAR ALL FLAGS - AC and link are cleared. Interrupt system is disabled.

The interrupt system allows certain external conditions to interrupt the computer program by driving the $\overline{\text{INTREQ}}$ input to the HM-6100 low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The current content of the Program Counter, PC, is deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved, possibly in a software stack, if nested interrupts are permitted. The INTGNT signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the perferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only is setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the $\overline{\text{DMAREQ}}$ by activating the DMAGNT signal at the end of the current instruction. The HM-6100 suspends any further instruction fetches until the $\overline{\text{DMAREQ}}$ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XTA, XTB, and XTC are active. The device which generated the $\overline{\text{DMAREQ}}$ must provide the address and necessary control signals to the memory for data transfers. The $\overline{\text{DMAREQ}}$ line can also be used as a level sensitive "pause" line.

Control Panel Interrupt Transfer

The HM-6100 CPU provides a unique Control Panel (CP) feature through its $\overline{\text{CPREQ}}$ input and $\overline{\text{CPSEL}}$ output lines. After acknowledging the control panel request, the CPU generates the necessary timing to execute program code in CP memory while also providing the capability to transfer data between CP memory and the user memory using the AC as a buffer. This allows the user memory to be examined and/or modified by the CP software. The CPU will output the $\overline{\text{MEMSEL}}$ signal for all user memory references while the $\overline{\text{CPSEL}}$ signal is generated for CP memory references as shown in Figure 11.

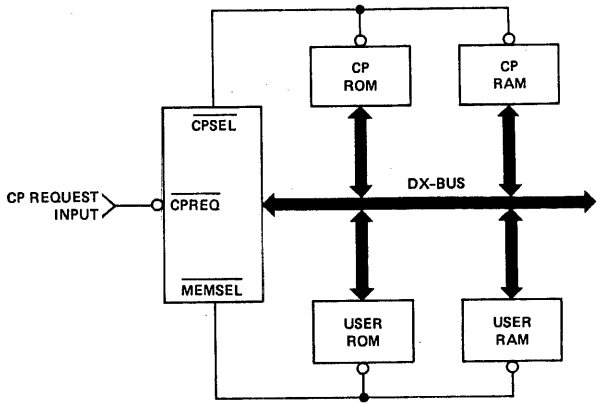


FIGURE 11 – Control Panel Block Diagram

The designer can make use of the control panel features to implement various functions that will be "transparent" to the user's (main) memory. Some of the more common functions include:

- Binary Loader and Punch
- Register Examination and Modification
- Single Cycle
- Octal Debug with Breakpoints
- Octal listing
- Auto Bootstrap

When a $\overline{\text{CPREQ}}$ is granted the PC is stored in location 0000 of Panel Memory and the HM-6100 resumes operation at location 7777 of the Panel Memory. The $\overline{\text{CPREQ}}$ bypasses the interrupt enable system and the processor IOT instruction, ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a $\overline{\text{CPREQ}}$ is granted, the HM-6100 will not recognize any $\overline{\text{DMAREQ}}$ or $\overline{\text{INTREQ}}$ until the CPREQ has been fully serviced.

During Control Panel program execution access to the user memory is gained through use of indirect TAD, AND, DCA and ISZ instructions. The CPU will transfer control from $\overline{\text{CPSEL}}$ to $\overline{\text{MEMSEL}}$ during the execute phase of these instructions. The instructions are always fetched from control panel memory.

Exiting from the control panel routine is achieved by executing the following sequence:

- ION
- JMP I 0000 /Exit via location 0000 in Panel Memory

Location 0000 contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine.

Internal Priority Structure

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in in Figure 12. The state of the priority network decides the next sequence of the HM-6100.

The CPU samples the $\overline{\text{RESET}}$ line, the request lines $\overline{\text{CPREQ}}$, $\overline{\text{DMAREQ}}$, and $\overline{\text{INTREQ}}$, and the state of its internal RUN flip-flop during the last execute cycle of each instruction. The worst case response time of the HM-6100 to an external request is, therefore the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μs at 4MHz clock frequency.

When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition of RUN/$\overline{\text{HLT}}$ should occur at least 10 clock pulses after $\overline{\text{RESET}}$ to be recognized.

The priority hierarchy is:

- $\overline{\text{RESET}}$ - If the $\overline{\text{RESET}}$ line is asserted at the sample time, the processor immediately sets its program counter to 7777, clears the Accumulator and Link, and puts the processor in the $\overline{\text{HALT}}$ state. While halted, the processor continues to cycle and generate the timing signals XTA, XTB, and XTC. During reset the DX line is tri-stated and the SEL lines are high.
- $\overline{\text{CPREQ}}$ - If the $\overline{\text{RESET}}$ line is not found to be asserted, but the $\overline{\text{CPREQ}}$ line is, the processor grants the control panel interrupt request at the end of the current cycle.
- RUN/$\overline{\text{HLT}}$ - If neither of the foregoing lines are asserted, but the processor finds its internal RUN FF in the halt state, it enters the HALT cycle at the end of the last execute cycle. Pulsing the RUN/$\overline{\text{HLT}}$ line low causes the HM-6100 to alternately run and halt. The internal RUN FF changes state on the rising edge of the RUN/$\overline{\text{HLT}}$ line. While halted the processor continues to generate the timing signals XTA, XTB, and XTC.
- $\overline{\text{DMAREQ}}$ - DMA requests are granted at the end of the current cycle only if none of the above actions are pending.
- $\overline{\text{INTREQ}}$ - An interrupt request is granted at the end of the current cycle only if none of the higher priority lines preempts it.
- IFETCH - If none of the above actions are indicated, the processor will fetch the next sequential instruction in the next cycle.

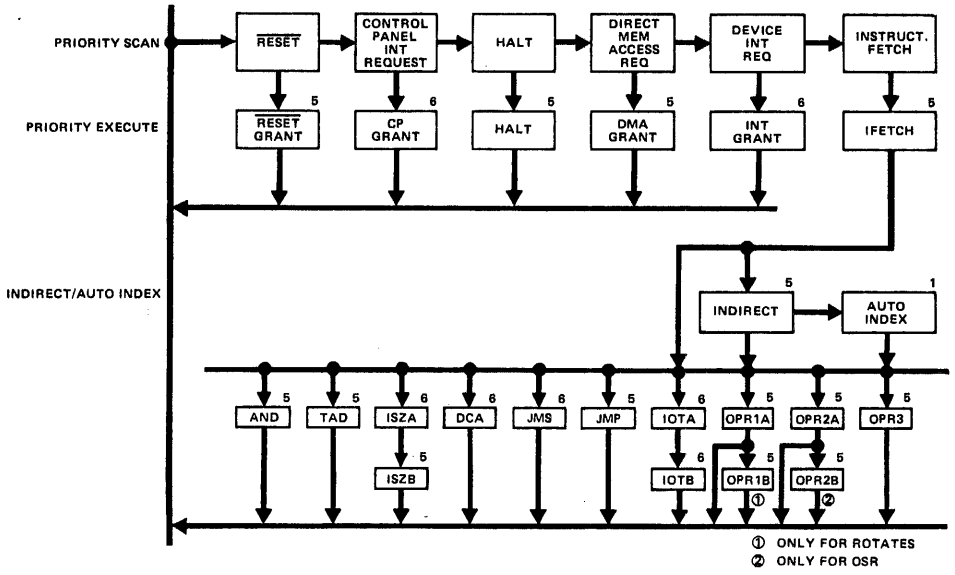


FIGURE 12 – Major processor states and number of clock cycles in each state.

Use of Wait Input

The HM-6100 samples the $\overline{\text{WAIT}}$ line during input-output data transfers. The $\overline{\text{WAIT}}$ line, if active low, controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), $\overline{\text{WAIT}}$ controls the time for which the write data is maintained on the DX lines by extending the T6 state. When operating at the max frequency, the internal delay of the HM-6100 causes the falling edge select lines to be past the $\overline{\text{WAIT}}$ setup time for WRITE. The rising edge of the select line for READ can be used to activate $\overline{\text{WAIT}}$ for a WRITE. The wait duration is an integral multiple of the oscillator time period (Figure 13).

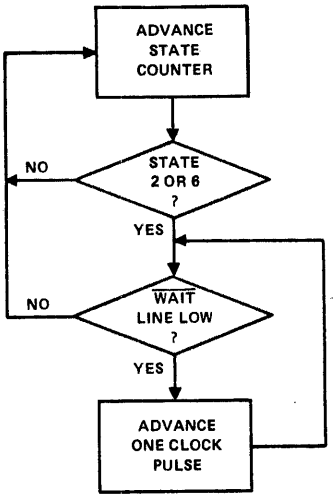


FIGURE 13 – WAIT sequencing steps.

HM-6100 Oscillator Requirements

USING AN EXTERNAL CRYSTAL

An inexpensive crystal can be used thereby eliminating the need for a clock generator. The crystal operates at parallel resonance, and thus is looks inductive in the circuit. An "AT" cut crystal should be used because it has a low temperature coefficient and can be used over a wide temperature range. The Feedback resistor and shunt capacitance are included internally. The crystal parameters needed are:

- Frequency
- Mod of Resonance - Parallel (anti-resonant)
- Maximum Power level - 1 milliwatt
- Load Capacitance - 32pF
- Series Resistance (max) - 250Ω

For precise frequency determination the effect of the stray circuit capacitance and internal 30pF capacitance must be taken into account.

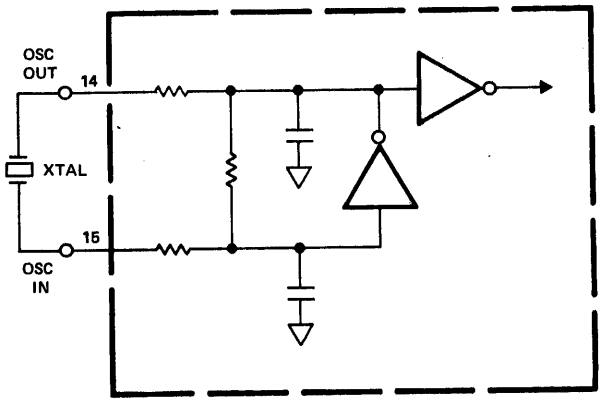


FIGURE 14 – Oscillator input schematic

USING AN EXTERNAL CLOCK GENERATOR

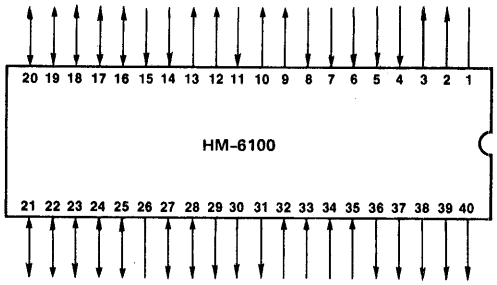
When a system clock is needed, eg. for a baud rate generator for UARTs, the HM-6100 can be externally clocked, thus eliminating the need for separate crystals. The external clock can be connected to the oscillator output pin while grounding oscillator input. This has the effect of over driving the small internal oscillator inverter causing an increase in supply current.

Duty cycle - 50/50
T_{rise}, T_{fall} - 20ns

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		Supply voltage.
2	RUN	H	The signal indicates the run state of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the $\overline{\text{DMAREQ}}$ line is released.
5	$\overline{\text{CPREQ}}$	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/$\overline{\text{HLT}}$	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/$\overline{\text{HLT}}$ flip flop.
7	$\overline{\text{RESET}}$	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	L	Peripheral device interrupt request.
9	XTA	H	External coded minor cycle timing—signifies input transfers to the HM-6100.

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	$\overline{\text{WAIT}}$	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as $\overline{\text{WAIT}}$ is active. The CPU is in the lowest power state with clocks running.
12	XTB	H	External coded minor cycle timing—signifies output transfers from the HM-6100.
13	XTC	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX0		DataX—multiplexed data in, data out and address lines.
17	DX1		See Pin 16—DX0.
18	DX2		See Pin 16—DX0.
19	DX3		See Pin 16—DX0.
20	DX4		See Pin 16—DX0.



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX5		See Pin 16—DX0.
22	DX6		See Pin 16—DX0.
23	DX7		See Pin 16—DX0.
24	DX8		See Pin 16—DX0.
25	DX9		See Pin 16—DX0.
26	GND		Ground
27	DX10		See Pin 16—DX0.
28	DX11		See Pin 16—DX0.
29	LINK	H	Link flip flop.
30	$\overline{\text{DEVSEL}}$	L	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{\text{C0}}$	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	$\overline{\text{C1}}$	L	See Pin 32—C0.
34	$\overline{\text{C2}}$	L	See Pin 32—C0.
35	$\overline{\text{SKP}}$	L	Skips the next sequential instruction if active during an I/O instruction. (Table 5)
36	IFETCH	H	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	L	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	L	The Control Panel Memory Select becomes active, instead of the $\overline{\text{MEMSEL}}$, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

HARRIS

HD-6101
CMOS PARALLEL INTERFACE ELEMENT (PIE)

Features

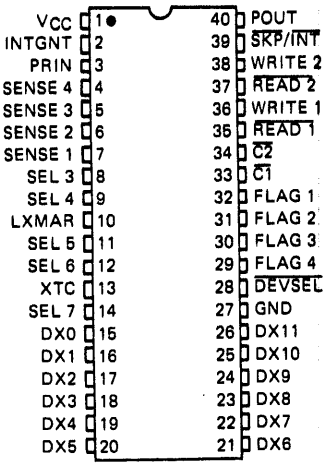
- HM-6100 COMPATIBLE
- LOW POWER STANDBY -500μW MAX
- SINGLE SUPPLY 4–11 VOLTS
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12 BIT INPUT PORTS
- CONTROL FOR TWO 12 BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

Description

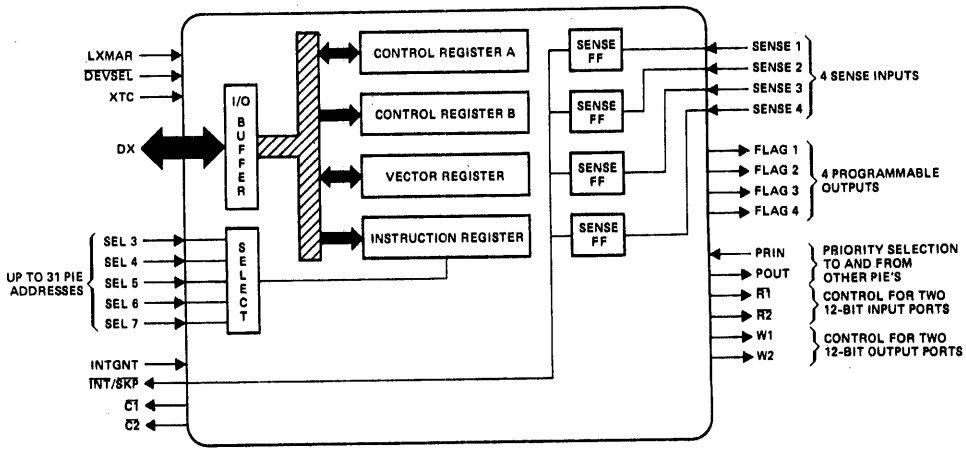
The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Pinout



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC + 0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101-9	-40°C to +85°C
Military HD-6101-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		+1.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	100	μA	$V_{IN} = V_{CC}$, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±10%		T_A = MILITARY V_{CC} = 5V ±10%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		200		300		330	ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	220	140	300	150	330	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		200		375		415	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		160		460		510	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		210		460		510	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		350		460		510	ns	
tLX	LXMAR Pulse Width	200		240		265		ns	
tAS	Address Set-Up Time	60		80		90		ns	
tAH	Address Hold Time	100		125		140		ns	
tDS	Data Set-Up Time	50		80		80		ns	
tDH	Data Hold Time	100		100		110		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Specifications HD-6101C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%; T_A = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% VCC			V	
V_{IL}	Logical "0" Input Voltage			.8	V	
I_{IL}	Input Leakage	-10		+10	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
VOH	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
VOL	Logical "0" Output Voltage			0.45	V	I_{OL} = 1.6mA
IO	Output Leakage	-10		+10	µA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	800	µA	$V_{IN} = V_{CC}$, Freq. = 0
CI	Input Capacitance(2)		5	7	pF	
CO	Output Capacitance(2)		8	10	pF	
CIO	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		230		375	ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	240	125	375	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		230		475	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		190		560	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		250		560	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		400		560	ns	
tLX	LXMAR Pulse Width	230		300		ns	
tAS	Address Set-Up Time	80		100		ns	
tAH	Address Hold Time	120		150		ns	
tDS	Data Set-Up Time	60		90		ns	
tDH	Data Hold Time	120		150		ns	

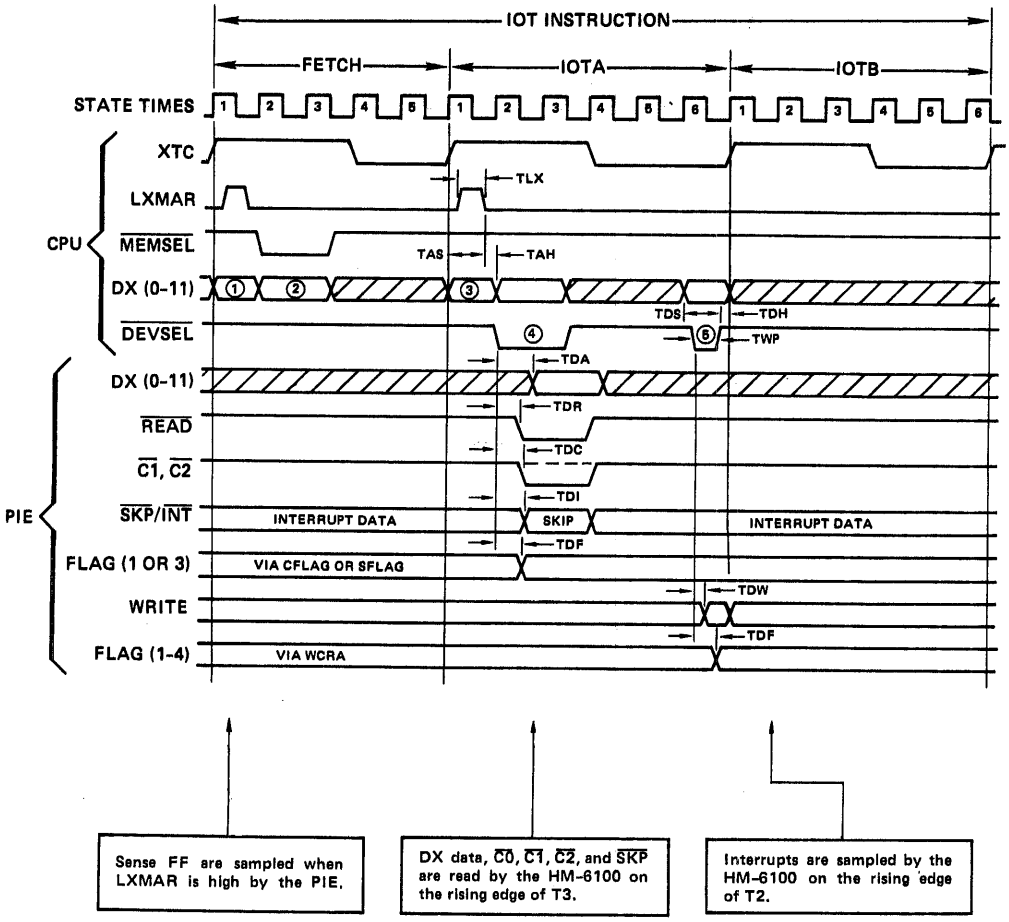
NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Timing Diagram

Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus (1) and obtains from memory an IOT instruction of the form 6XXX (2) . During IOTA of the execute phase the processor places that instruction back on the DX lines (3) and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high (4) is used by the addressed PIE along with the decoded control information to generate CPU control signals $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$. Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are generated to gate peripheral data to the DX lines. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low (5) is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.

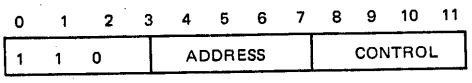


Pie Address and Instructions

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT



CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{CO}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{CO}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{SKP}/\overline{INT}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE not assert the $\overline{SKP}/\overline{INT}$ output and the HM-6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 4 to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

Programmable Outputs

FLAGs (1-4) - The FLAGs are general purpose outputs that can be set and cleared under program control. GLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF's are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

CONDITION	SENSE FLIP FLOPS	
	SKIP FF	INTERRUPT FF
CAF Instruction (6007ß)	Clears All	Clears All
SKIP Instruction	Clears Corresponding FF	Clears Corresponding FF
Vectored Interrupt	Not Cleared	Clears Highest Priority FF on Selected PIE After Vectoring
Interrupt Disabled (IE = "0")	Not Cleared	Disables Interrupt by Holding Corresponding FF in Reset State

Controls for Input and Output Ports

READ (1-2) – The $\overline{\text{READ}}$ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) – The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES – There are three I/O control lines from the PIE to the microprocessor – $\overline{C1}$, $\overline{C2}$, and $\overline{INT}/\overline{SKP}$. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the $\overline{C1}$ and $\overline{C2}$ control lines as shown below.

Interrupt and skip information are time multiplexed on the same line ($\overline{SKP}/\overline{INT}$). Since the HM-6100 samples skip and interrupt data at separate times there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the $\overline{INT}/\overline{SKP}$ line low. During IOTA of SKIP instructions the $\overline{INT}/\overline{SKP}$ reflects the SENSE FF data when $\overline{DEVSEL}$ is low and XTC is high. If the SENSE flip flop is set, the $\overline{INT}/\overline{SKP}$ line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$*	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	PIE ← AC	The contents of the AC is sent to the PIE.
H	H	L	H	AC ← AC V PIE	Data is received from the PIE, OR'ed with the data in the AC and the result stored in the AC.
H	H	L	L	PC ← Vector Address	Vector address received from PIE and loaded into PC. This is referred to as an absolute jump.
L	H	H	H	PC ← PC + 1	Forces Microprocessor to skip next sequential instruction.

NOTE: *The $\overline{C0}$ line must be connected to V_{CC} using a pull-up resistor.

Programmable Registers

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) – Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) – A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) – A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) – A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) – A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

0	1	2	3	4	5	6	7	8	9	10	11
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1	*	*	*	*

* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

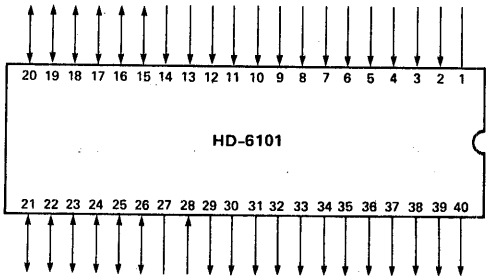
0	1	2	3	4	5	6	7	8	9	10	11
VECTOR REGISTER										VPRI	

VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

Pin Definitions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		Positive voltage
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 – SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on $\overline{DEVSEL}$ initiates a "read" operation. When XTC is low, a low going pulse on $\overline{DEVSEL}$ initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	$\overline{DEVSEL}$	L	The $\overline{DEVSEL}$ input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	$\overline{C1}$	L	The PIE decodes address, control and priority information and asserts outputs $\overline{C1}$ and $\overline{C2}$ during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. $\overline{C1}$(L), $\overline{C2}$(L) - vectored interrupt $\overline{C1}$(L), $\overline{C2}$(H) - $\overline{READ1}$, $\overline{READ2}$ or RRA commands $\overline{C1}$(H), $\overline{C2}$(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	$\overline{C2}$	L	See Pin 33 – $\overline{C1}$
35	$\overline{READ1}$	PROG	Outputs $\overline{READ1}$ and $\overline{READ2}$ are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100** Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	$\overline{READ2}$	PROG	See Pin 35 – $\overline{READ1}$
38	WRITE2	PROG	See Pin 36 – WRITE1
39	$\overline{SKP/INT}$	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

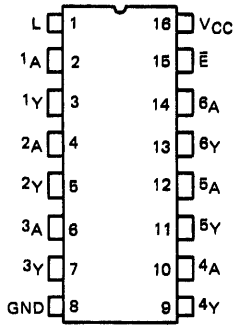
HD-6431
CMOS HEX LATCHING BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 75nsec MAX.

Pinout

TOP VIEW



Truth Table

CONTROL INPUTS		DATA PORT STATUS	
Ē	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

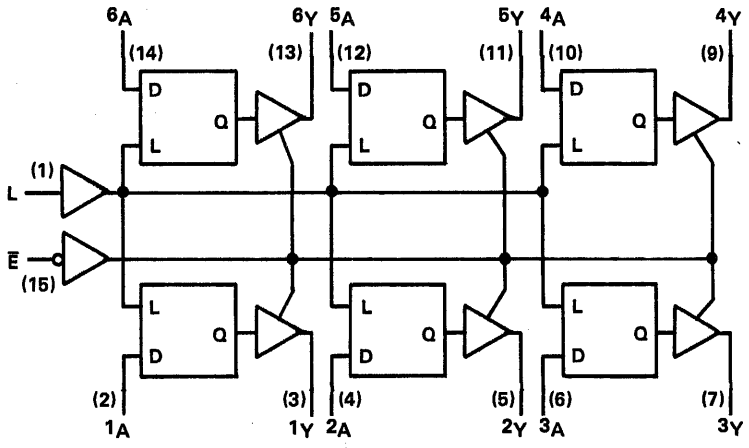
* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Description

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control Ē forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

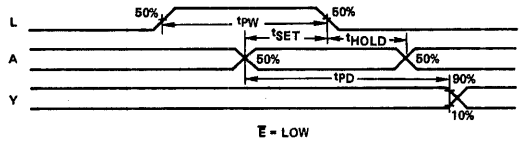
C_L = 300pF

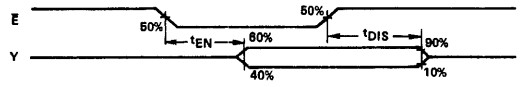
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		65		75	ns
t_{EN}	Enable Time		80		90	ns
t_{DIS}	Disable Time		80		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	25		30		ns
t_R	Output Rise Time		80		90	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

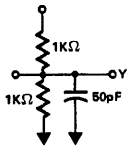
Switching Waveforms





All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

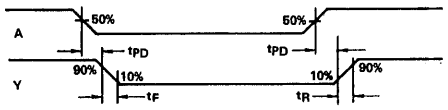


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 80ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



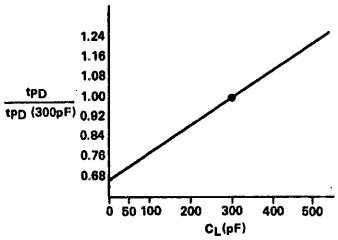


FIGURE 1

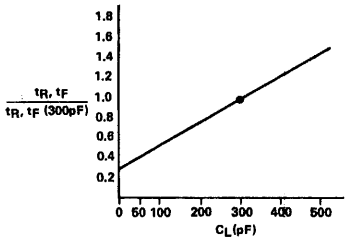


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

HARRIS

HD-6432

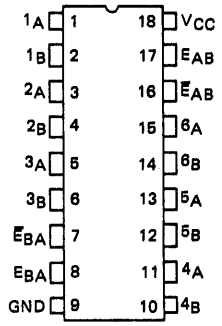
CMOS HEX BI-DIRECTIONAL BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 55nsec MAX.

Pinout

TOP VIEW



Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

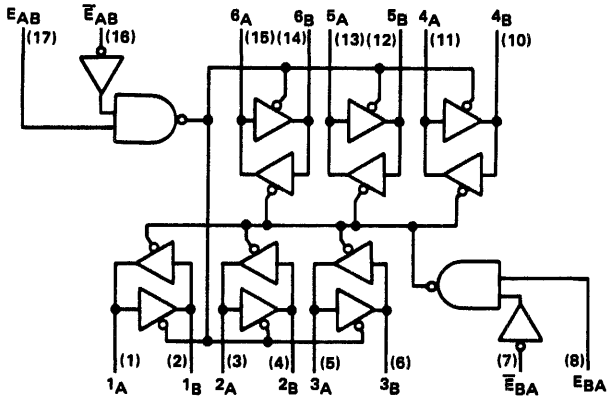
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

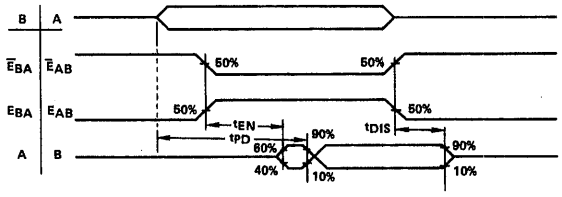
C_L = 300pF

A.C.

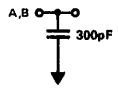
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45		55	ns
t_{EN}	Enable Time		65		75	ns
t_{DIS}	Disable Time		100		110	ns
t_R	Output Rise Time		100		110	ns
t_F	Output Fall Time		70		80	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

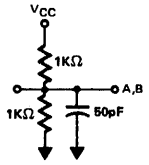
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

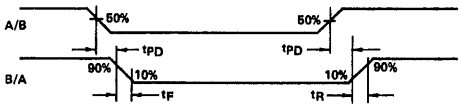


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 100\text{ns} \quad V_{CC} = 5.0\text{V} \quad \text{each } C_L = 300\text{pF} \quad I_T = (6)\,(300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



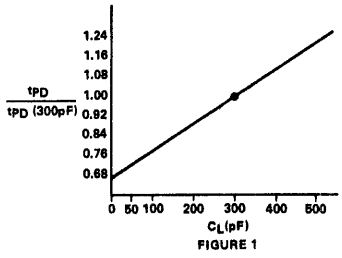


FIGURE 1

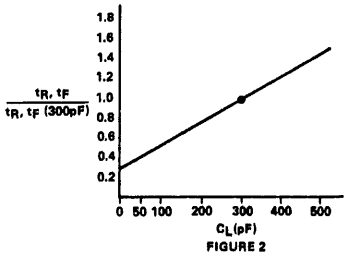


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

HARRIS

HD-6433

CMOS QUAD BUS SEPARATOR/DRIVER

Features

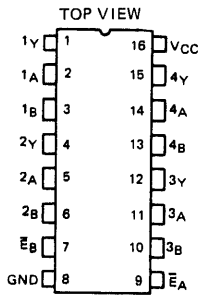
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 50nsec MAX.

Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

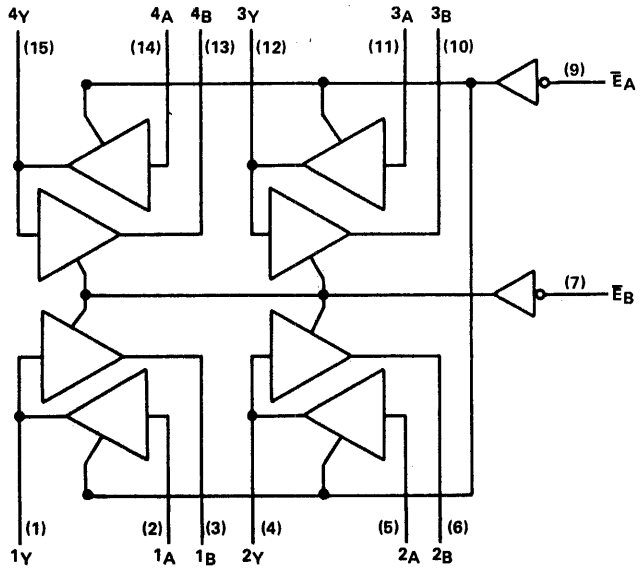


Truth Table

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

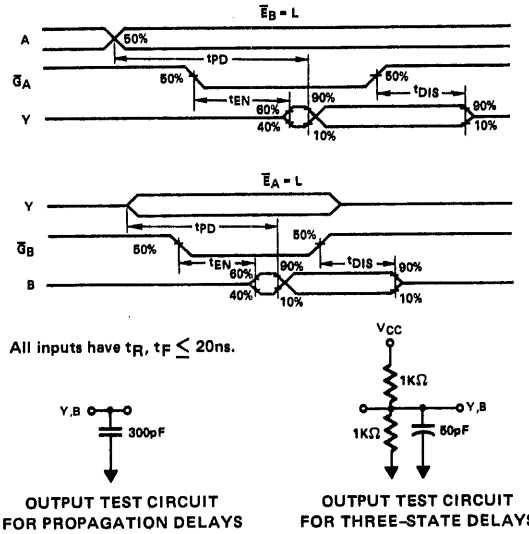
C_L = 300pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% TA = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		40		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

Switching Waveforms

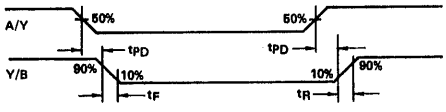


DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 85ns, V_{CC} = 5.0V, each C_L = 300pF, $I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}}$ = 56.5mA.] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

4 µP & PERIPHERALS

PROPAGATION DELAYS



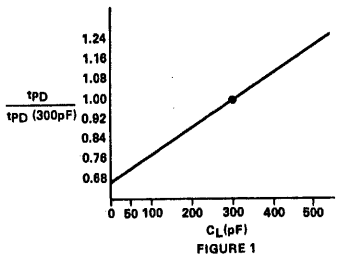


FIGURE 1

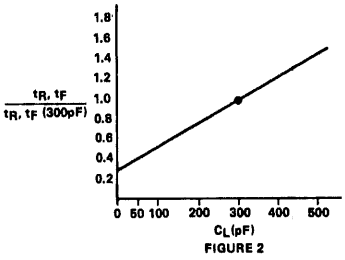


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

HARRIS

HD-6434

CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 6mA
- SINK CURRENT — 9mA
- PROPAGATION DELAY — 50nsec MAX.

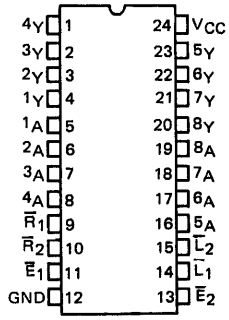
Description

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

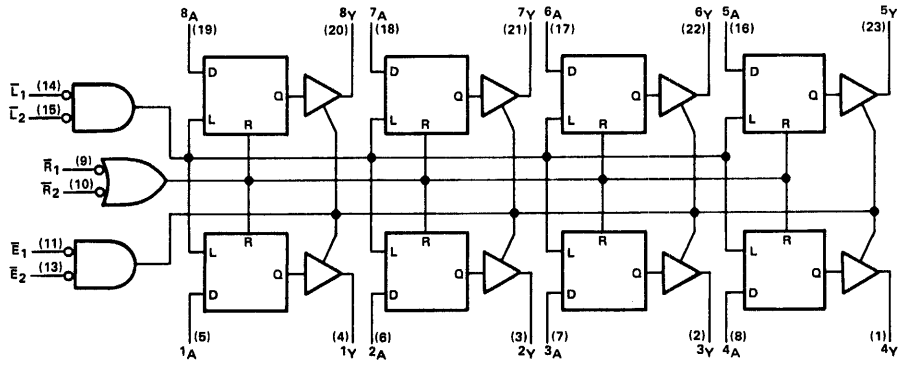


Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the value of the last input
↑ = Transition from a Low to High level

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6434-9	-40°C to +85°C
Military HD-6434-2/8	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

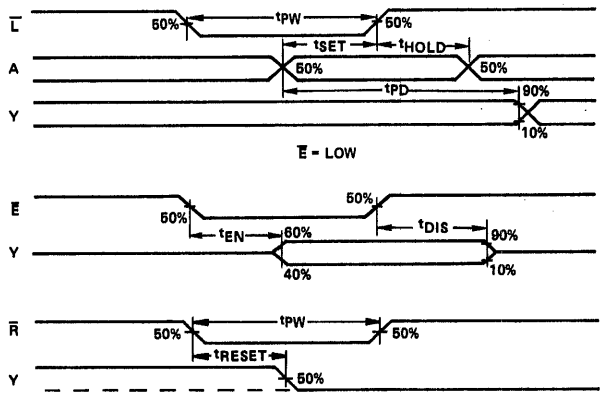
* Guaranteed and sampled, but not 100% tested.

A.C.

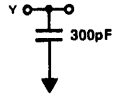
		VCC = 5.0V TEMP = 25°C C_L = 50pF ①	VCC ±5.0V ±10% TEMP = IND OR MIL C_L = 300pF		
SYMBOL	PARAMETER	TYP	MIN	MAX	UNITS
tPD	Propagation Delay	40		50	ns
tEN	Enable Time	45		50	ns
tDIS	Disable Time	45		50	ns
tSET	Input Setup Time	25	35		ns
tHOLD	Input Hold Time	40	45		ns
tPW	Pulse Width	45	65		ns
tR	Output Rise Time	45		50	ns
tF	Output Fall Time	30		50	ns
tRESET	Reset Delay Time	75		125	ns

① All devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

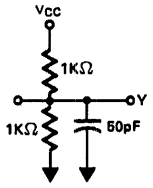
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

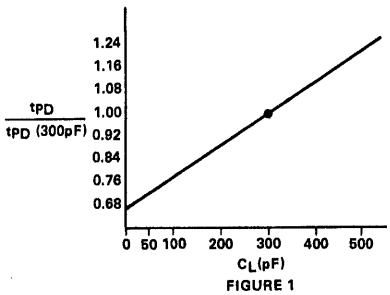


FIGURE 1

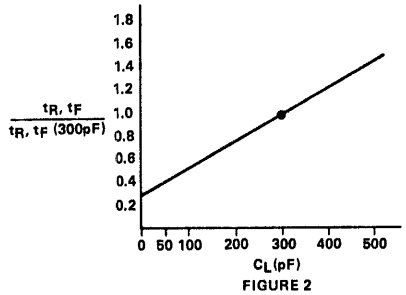


FIGURE 2

TYPICAL CURVES

HARRIS

HD-6436

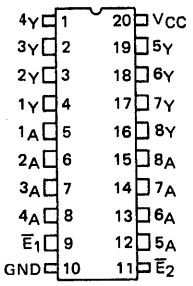
CMOS OCTAL BUS BUFFER/DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 6mA
- SINK CURRENT — 9mA
- PROPAGATION DELAY — 55nsec MAX.

Pinout

TOP VIEW



Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 noninverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

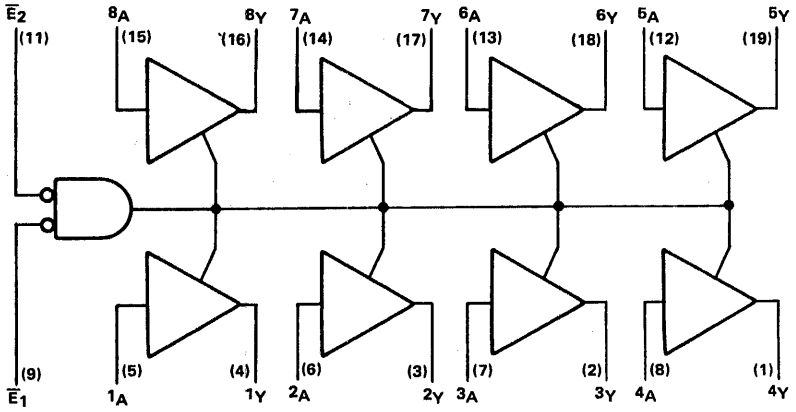
Outputs guaranteed valid at V_{CC} = 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	Hi-Z
H	L	X	Hi-Z
H	H	X	Hi-Z

L = Low, H = High
X = Don't Care
Hi-Z = High Impedance

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6436-9	-40°C to +85°C
Military HD-6436-2/8	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

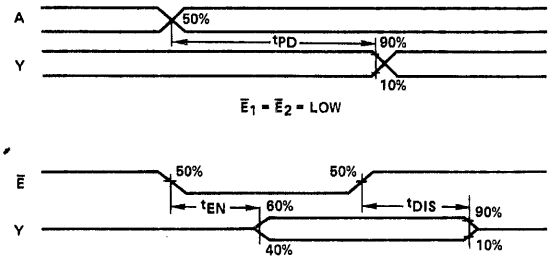
* Guaranteed and sampled, but not 100% tested.

A.C.

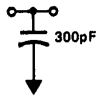
		V_{CC} = 5.0V TEMP = 25°C C_L = 50pF ①	V_{CC} = 5.0V ±10% TEMP = IND OR MIL C_L = 300pF	
SYMBOL	PARAMETER	TYP	MAX	UNITS
tPD	Propagation Delay	35	55	ns
tEN	Enable Time	50	65	ns
tDIS	Disable Time	50	55	ns
tR	Output Rise Time	30	55	ns
tF	Output Fall Time	25	55	ns

① All Devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

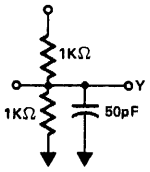
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

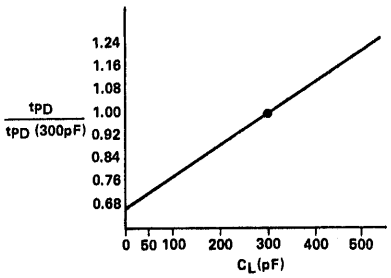


FIGURE 1

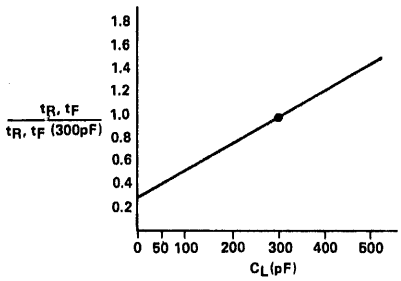


FIGURE 2

TYPICAL CURVES

HD-6440

CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . . TYPICALLY<50μW @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

Description

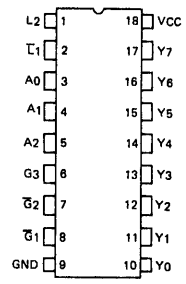
The HD-6440 is a self aligned silicon CMOS gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



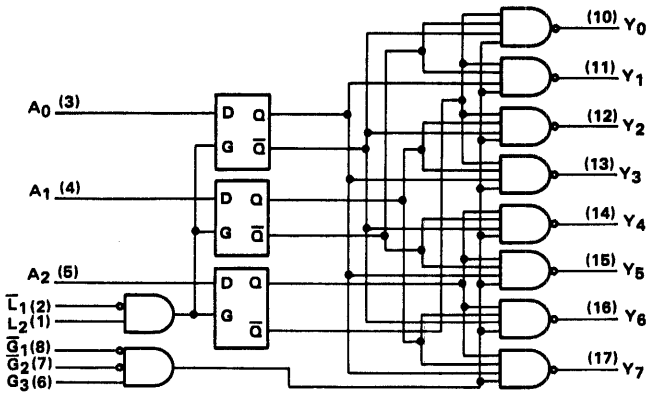
Truth Table

INPUTS																OUTPUTS								
ENABLE						ADDRESS																		
$\overline{G_1}$	$\overline{G_2}$	G_3		$\overline{L_1}$	L_2		A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L		X	X		X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X		X	X		X	X	X	H	H	H	H	H	H	H	H	
H	X	X		X	X		X	X	X	H	H	H	H	H	H	H	H	
L	L	H		L	H		L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H		L	H		L	L	H	H	L	H	H	H	H	H	H	
L	L	H		L	H		L	H	L	H	H	L	H	H	H	H	H	
L	L	H		L	H		L	H	H	H	H	H	L	H	H	H	H	
L	L	H		L	H		H	L	L	H	H	H	H	L	H	H	H	
L	L	H		L	H		H	L	H	H	H	H	H	H	L	H	H	
L	L	H		L	H		H	H	L	H	H	H	H	H	H	L	H	
L	L	H		L	H		H	H	H	H	H	H	H	H	H	H	L	
L	L	H		X	L		X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H		H	X		X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

L = Low, H = High, X = Don't Care

Y_n = Data is latched to the value of the last input

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440-9	-40°C to +85°C
Military HD-6440-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	µA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

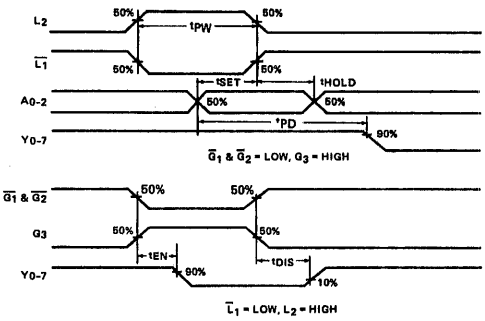
CL = 200pF

A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		90	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

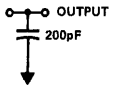
NOTE:
① All devices guaranteed at worse case limits. Room temperature, 5V data provided for information - not guaranteed.

Switching Waveforms



All Inputs have t_R, $t_F \leq 20ns$

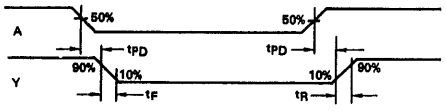
OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 60ns, V_{CC} = 5.0V, \text{each } C_L = 200pF, I_T = (2)\ (200 \times 10^{-12})\ \frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAY



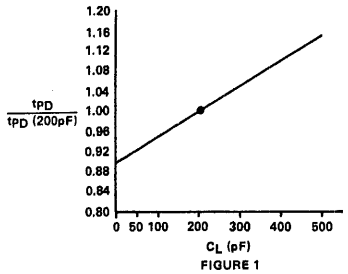


FIGURE 1

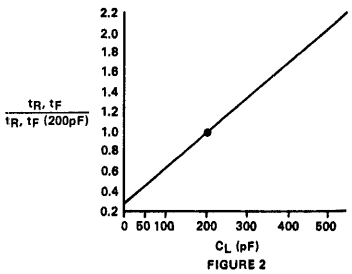


FIGURE 2

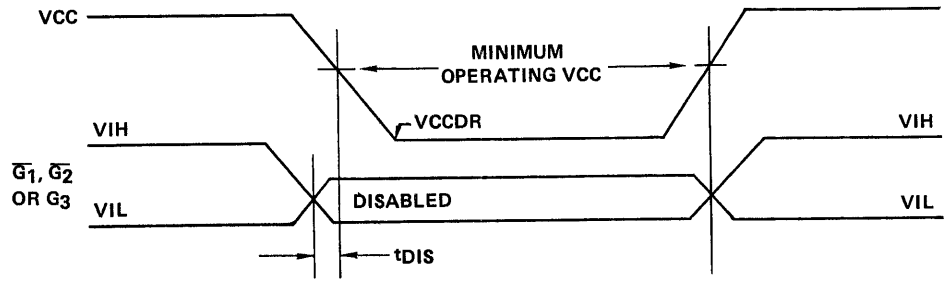
The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is, therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

Battery Backup Applications

The HD-6440 is especially well suited for use in battery backup systems in conjunction with low power CMOS RAM arrays. When designing a RAM array in conjunction with the HD-6440, the following criteria should be met:

1. As RAM VCC drops, the inputs logical one voltages should follow so as not to exceed VCC +0.3V and logical zero voltages do not go below GND -0.3V.
2. $\overline{G}_1$ or $\overline{G}_2$ must be held high at CMOS VCC, or G_3 held low. L_1, L_2 and address inputs should be held at either GND or CMOS VCC.
3. Y_0 - Y_7 will maintain a VOH of VCC -0.3 or greater at IOH of 100 μA provided the HD-6440 VCC is $\geq$2.0V.
4. When exiting from the battery backup mode, VCC should ramp without ring on discontinuities.
5. The HD-6440 can begin operation when VCC reaches the minimum operating voltage.
6. The HD-6440 should be disabled one t_{DIS} before VCC reaches the minimum operating voltage.

TIMING DIAGRAM



HARRIS

HD-6495

CMOS HEX BUS DRIVER

Features

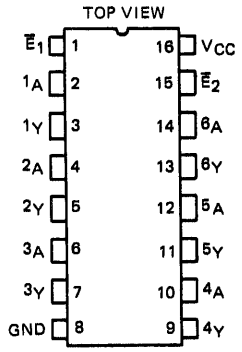
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 45nsec MAX.

Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

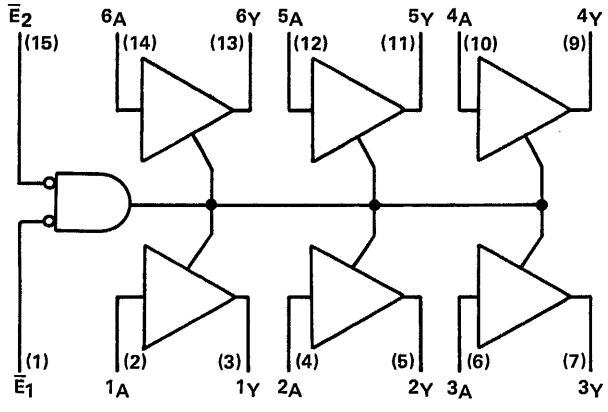


Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

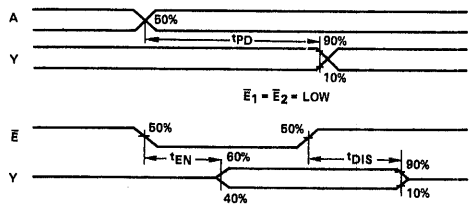
C_L = 300pF

A.C.

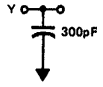
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		90		100	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		65		75	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

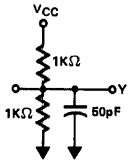
Switching Waveforms



All inputs have $t_R, t_F \leq 20ns.$



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

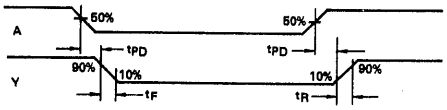


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



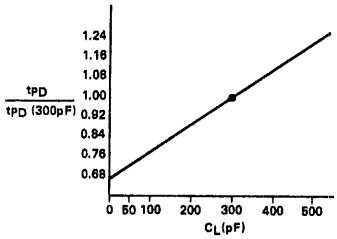


FIGURE 1

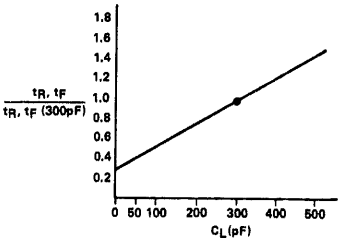


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

HARRIS

REFERENCE PAGE 3-77 FOR COMPLETE SPECIFICATIONS

82C82

CMOS OCTAL LATCHING BUS DRIVER

Advance Information

Features

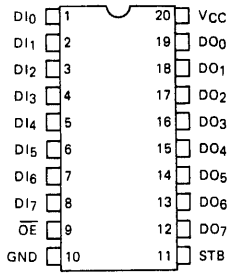
- FULL EIGHT BIT PARALLEL LATCHING BUFFER
- BIPOLAR 8282 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ► FULL TEMPERATURE RANGE
  - ► 10% POWER SUPPLY TOLERANCE
  - ► C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

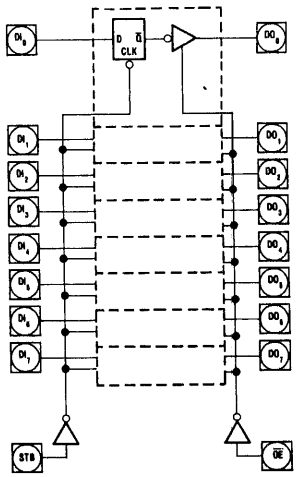
The Harris 82C82 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Pinout

TOP VIEW



Functional Diagram



PIN NAMES

DI_0 - DI_7	Data Input Pins
DO_0 - DO_7	Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Truth Table

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

H = Logic One Hi-Z = High Impedance
L = Logic Zero ↓ = Negative Transition
X = Don't Care * = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C83

CMOS OCTAL LATCHING INVERTING BUS DRIVER

Preview

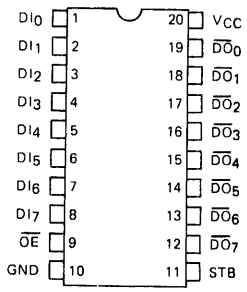
Features

- FULL EIGHT BIT PARALLEL LATCHING INVERTING BUFFER
- BIPOLAR 8283 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ▶ FULL TEMPERATURE RANGE
  - ▶ 10% POWER SUPPLY TOLERANCE
  - ▶ C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

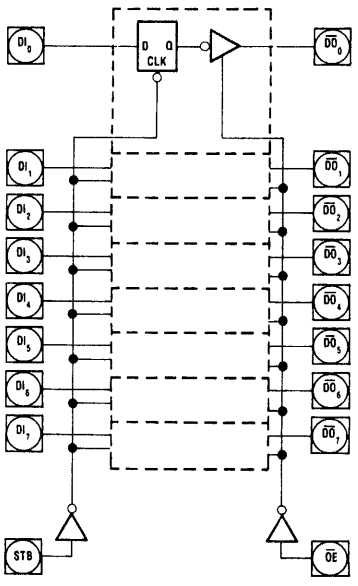
The Harris 82C83 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems. The 82C83 provides inverted data at the outputs.

Pinout



PIN NAMES	
DI_0 - DI_7	Data Input Pins
$\overline{DO}_0$ - $\overline{DO}_7$	Inverted Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Truth Table

STB	$\overline{OE}$	DI	$\overline{DO}$
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

H = Logic One Hi-Z = High Impedance
L = Logic Zero ↓ = Negative Transition
X = Don't Care * = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C86

CMOS OCTAL BUS TRANSCIEVER

Preview

Features

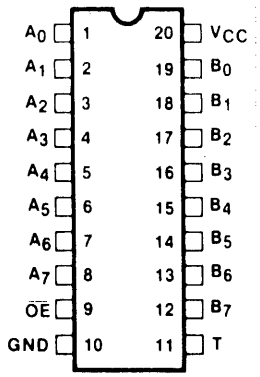
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8286 COMPATIBLE PINOUT
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY — 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - C_L = 100pF
  - B SIDE - C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT — 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C86 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) allows simple interface to the 80C86 and other microprocessors. The outputs of the 82C86 are non-inverting.

Pinout

TOP VIEW

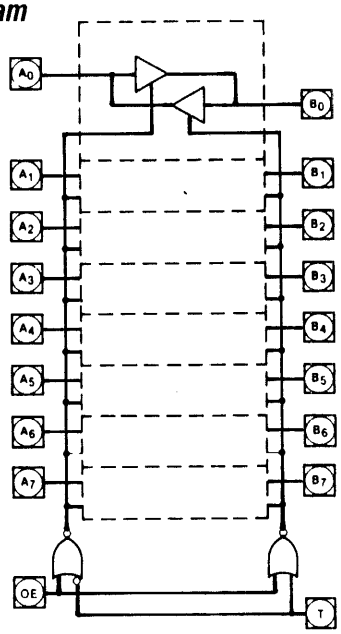


PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
B_0-B_7	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

4 µP & PERIPHERALS

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = logical one
L = logical zero
I = input mode
O = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C87

CMOS OCTAL INVERTING BUS TRANSCEIVER

Preview

Features

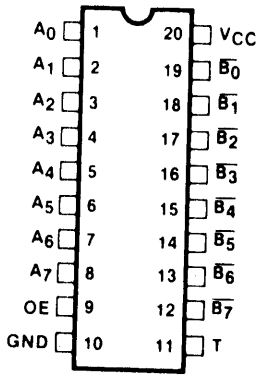
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8287 COMPATIBLE PINOUT
- THREE STATE INVERTING OUTPUTS
- PROPAGATION DELAY — 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - C_L = 100pF
  - B SIDE - C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT — 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C87 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) allows simple interface to state of the art microprocessors. Data at the outputs of the 82C87 are inverted.

Pinout

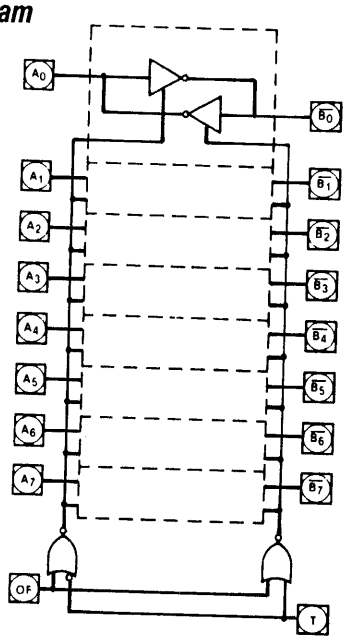
TOP VIEW



PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
$\overline{B_0}$-$\overline{B_7}$	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	$\overline{B}$
X	H	Hi-Z	Hi-Z
H	L	I	0
L	L	0	I

H = logical one
L = logical zero
I = input mode
0 = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.