EK-DUP11-OP-002

DUP11
Bit Synchronous Interface
User's Manual

digital

EK-DUP11-OP-002

DUP11
Bit Synchronous Interface
User's Manual

Prepared by Educational Services
of
Digital Equipment Corporation

1st Edition, November, 1976
2nd Edition (Rev), August, 1982

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

CONTENTS (Cont)

FIGURES

TABLES

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides the user with the information necessary to install and operate the DUP11 Synchronous Line Interface. The manual is organized into three chapters and one appendix.

Chapter 1 – Introduction
Chapter 2 – Installation
Chapter 3 – Register Description
Appendix A – PDP-11 Memory Organization and Addressing Conventions

This chapter provides a general description of the DUP11 and a general discussion of the Synchronous Data Link Control (SDLC) protocol and Digital Data Communications Message Protocol (DDCMP).

1.2 DUP11 GENERAL DESCRIPTION

The DUP11 provides a data path between a synchronous modem and the Unibus. It operates under the discipline of SDLC, ADCCP, DDCMP, and other similar protocols. Protocols of the BISYNC family can be used with some loss of efficiency due to the additional software decisions required.

The DUP11 provides parallel-to-serial conversion of data to be transmitted and serial-to-parallel conversion of received data. Logic is provided to create a transparent data stream and to compute a CRC check character during transmission. All information is handled in 8-bit bytes and VRC parity is not provided. CRC error detection is provided during reception. Modem control and level conversion logic is provided also.

Interrupt control logic is used to generate requests for the transfer of data between the DUP11 and the PDP-11 system memory via the Unibus. No direct memory access (DMA) logic is contained in the DUP11.

The DUP11 contains logic to perform the following functions:

1. Program control of secondary station address recognition. Primary station operation is used as the default condition (SDLC protocol family only).

2. Programmable SYN character recognition (DDCMP and BISYNC protocol families).

3. CRC characters computation and error detection (SDLC and DDCMP protocol families).

4. Automatic transmission of flag characters initiated by the program (SDLC protocol family only).

5. Program control of transmission of abort sequence and 16 zero sequence (SDLC protocol family only).

6. Hardware detection of received flags and abort sequences (SDLC protocol family only).

The DUP11, including level conversion, is contained on a hex module. The DUP11 is connected to the modem via a BC05C cable and BC02 cable that support RS232-C specifications only. Current mode operation is not supported by the DUP11 and it is not compatible with the DF11 series options.

The modem control logic is compatible with Bell 201, 208, and 209 series modems. There is no interlock between the transfer of data and modem control. The program controls handshaking with the modem, if it is required. Once the handshaking has been completed, the program can initiate the transfer of data. The modem control logic includes secondary receive and transmit leads. These leads can be redefined by the Field Service engineer at the user's request.

1.3 SDLC AND DDCMP PROTOCOLS

1.3.1 Introduction

This discussion provides a general description of the SDLC and DDCMP protocols. It is the prerequisite to a thorough understanding of the operation of the DUP11. Details of the SDLC, DDCMP, ADCCP and BISYNC protocols are found in the following documents:

Digital Data Communications Message Protocol (Digital Equipment 130-959-007-02)
IBM Binary Synchronous Communications General Information (GA27-3004-2)
ADCCP ANSI X3S34/475 DR7
ADCCP ANSI X3S34/584 DR1

1.3.2 General Information

Although the mentioned protocols are not identical, they are similar enough to operate with the DUP11. The program directly controls the DUP11 operation through the use of control and status registers. The program must provide a continuous flow of data to be transmitted. No intra-message fill characters are allowed. The program must also service the receiver data buffer within the prescribed time.

When transmitting in the SDLC or DDCMP family of protocols, the program must form the address and command fields plus any other header information that is required. The program must maintain the transmitter data buffer and set marker bits to delimit the transmitted message. When receiving in the SDLC or DDCMP family of protocols, the program must interpret the header information, service the receiver data buffer, and monitor the status bits associated with the received data.

Protocols such as BISYNC that achieve transparency by using special control characters are less efficient than SDLC and DDCMP when used with the DUP11. This occurs because of the increased program involvement required to maintain transparency and compute the CRC character. The CRC control logic in the DUP11 is not suited to protocols in which special control characters appear within the body of the message. For these protocols, the CRC logic should be disabled by setting the NO CRC bit (PARCSR bit 9).

1.3.3 SDLC Protocol Description

1.3.3.1 Message Format – The SDLC message format is shown in Figure 1-1. This format is called a frame and is the standard structure for all transmissions.

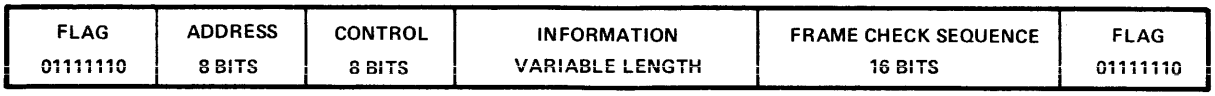

Figure 1-1 SDLC Message Format

The frame starts with the 8-bit Flag sequence, 01111110, followed in order by the Address sequence, Control sequence, Information sequence (if present), Frame Check sequence, and ends with another Flag sequence. In some applications, the Flag is preceded by a sequence of 16 zeros.

Each sequence in the frame is discussed below with emphasis on related operational features of the DUP11, if applicable.

Flag Character
The flag character is a unique 8-bit character of the form 01111110. Flag characters are used to delimit the message. They can be used to fill in between messages but cannot be used as fillers within messages. When the transmitter initiates the start of a message by asserting the TSOM (transmitter start of message) bit, the initial flag character is automatically transmitted. If the TSOM bit is still asserted at the end of the first flag character, another flag character is transmitted. When the TXDONE (transmitter done bit) is asserted by the DUP11 subsequent to the program's asserting of the TSOM bit, the program may respond by loading data into the TXDBUF (transmitter data buffer) low byte, or leave the TSOM bit asserted and send another flag.

In some applications, the TSOM and TEOM bits are used to initiate a sequence of 16 zeros. This sequence can be initiated only from the idle state. To transmit this sequence, SEND must be asserted and TXACT must be cleared. With these requirements met, the program simultaneously sets TSOM and TEOM and the 16 zeros are transmitted. When the first zero bit is presented to the serial output, TXDONE is set. Now, the program should clear TEOM and on the next transition of TXDONE the program should clear TSOM. The first data character can be loaded now. This point marks the start of the initial flag character. the first data character is transmitted subsequent to the current flag character.

When the last character of a message has been loaded into the TXDBUF, that character is then transmitted. Subsequent to loading the last character, the TXDONE bit is asserted again by the DUP11. This marks the start of the transmission of the last character. At this time, the TEOM (transmitter end of message) may be asserted in the upper byte of the TXDBUF. The character currently being serialized (i.e., the last character of the message) is transmitted and followed by a CRC check character and the terminating flag character. This concludes the message.

When the receiver logic is enabled by the software, it searches for flag characters. If the basic SDLC or ADCCP message format is followed and the receiver is programmed to operate in the secondary mode, the following actions occur.

The eight bits after the last received flag are compared to the secondary station address. If a match is not found, the receiver continues to hunt for a flag. When the next flag character is located, this comparison of addresses is reiterated.

If the character subsequent to the flag character matches the secondary station address, characters received subsequent to the address character cause the RXDONE (receiver done) bit to be asserted. The RSOM (receiver start of message) bit is presented to the program along with the first data character.

When the secondary station receiver is actively transferring data, the following events occur when a terminating flag character is detected. The receiver logic automatically resumes the address search as cited earlier. Also, a status entry is made into the receiver data buffer, the REOM bit is asserted and the CRC error bit is set if an error was detected. The lower byte of data in this entry is invalid.

When the receiver logic is programmed to operate as a primary station, all characters subsequent to the last received flag character cause the RXDONE bit to be asserted. The first character of the frame is accompanied by the RSOM bit.

When the terminating flag character of a message is received, primary station operation is the same as cited above for secondary station operation. When the next data character is received, the receiver logic again sets the RSOM and RXDONE bits. The last two bytes preceding the flag were the receiver CRC bytes.

Address Character
The address character appears subsequent to the flag character and is eight bits long. This format supports a maximum of 256 addresses. The protocol has provisions for the recursive expansion of the number of addresses. This feature is not supported by the DUP11 hardware. It must be maintained by the program. In the secondary station mode, the program must load the address of the receiving station into the low byte of the PARCSR.

Control Field
The 8-bit control field follows the address character. This field is controlled by the program and is encoded to indicate the commands and responses to control the data link. This field has three formats as described below.

1. Nonsequenced Format – used by the primary station primarily for data link management. Such duties include activating and initializing secondary stations, controlling the response mode of secondary stations, and reporting procedural errors.
2. Supervisory Format – does not contain an information field but it is an adjunct to the information format. It is used by the primary station to poll the secondary stations. The secondary stations use this format to provide acknowledgment to the primary station.
3. Information Format – used by primary and secondary stations for the transfer of information fields.

Information Field
This field is used for the transmission of data or status information. This field contains an arbitrary number of characters as specified by the documents covering the protocols. **The DUP11 handles the data in this field as eight bit characters.**

When one character is transmitted from the transmitter shift register, another character is taken from the data buffer. If the data buffer is empty, the transmitted data lead goes to a mark hold state. Also, a status bit is asserted to indicate the data underrun condition in SDLC or ADCCP and an Abort character is automatically transmitted.

There are no restrictions on bit patterns that appear between flags in an SDLC frame. Therefore, the transmitted data may contain six or more contiguous 1s and this pattern could be interpreted as a flag which would inadvertently terminate an incomplete frame. To prevent this action and to maintain data

transparency, the DUP11 contains 0 insertion and 0 removal logic that is active on all characters between the flags. During transmission, when five contiguous 1s occur, the transmitter automatically inserts a 0 after the fifth 1. During reception, the 0 after five contiguous 1s is automatically removed. This applies to all fields except the Flag.

Frame Check Sequence (FCS) Field
This 16-bit field follows the information field and is also referred to as the Block Check Character (BCC) or CRC check character. It is used in all SDLC frames to detect errors.

Logic to compute CRC check characters is included in the transmitter logic. Similarly, logic is included in the receiver logic to check the results when the check character is received. This operation of computing and verifying the CRC check is transparent to the program. Any error in the computation of the received check character in SDLC type protocol operation is indicated by a status bit in the receiver data buffer. If DDCMP operation is selected, the program must monitor a status bit to detect the desired accumulated results.

Two CRC polynomials are supported by the DUP11: CRC 16 and CCITT. When the SDLC or ADCCP mode of operation is selected, the CCITT polynomial is used and the internal CRC registers are effectively initialized to all 1s. During transmission, the complement of the accumulated CRC character is sent. If the SDLC or ADCCP mode is not selected, the CRC 16 polynomial is used providing CRC checking is not inhibited.

1.3.3.2 Abort Sequence - An abort is the premature termination of a data line by the transmitting station. An abort is detected by the reception of more than seven contiguous 1s. When the abort sequence is received, the message in progress is terminated. A flag (RXERROR) is set and RXDONE is set also. If the program has set RXITEN, an a interrupt request is generated when RXDONE is set. A transmitting station can send abort sequences under program control by setting the TXABORT bit. If the program response time to the TXDONE bit is excessive, the TXDATLAT bit is set and the transmitter idles abort characters.

1.3.4 DDCMP Protocol
DDCMP (Digital Data Communications Message Protocol) was developed to provide full-duplex message transfer over standard existing hardware.

1.3.4.1 Controlling Data Transfers - The DDCMP message format is shown in Figure 1-2. A single control character is used in a DDCMP message, and is the first character in the message. Three control characters are provided in DDCMP to differentiate between the three possible types of messages:

SOH - data message follows
ENQ - control message follows
DLE - bootstrap message follows.

Note that the use of a fixed-length header and message-size declaration obviates the BSC requirement for extensive message and header delimiter codes.

Figure 1-3 shows a simple example of data exchange between the DUP11/PDP-11 and a data terminal. More efficient procedures can be derived after a study of DDCMP.

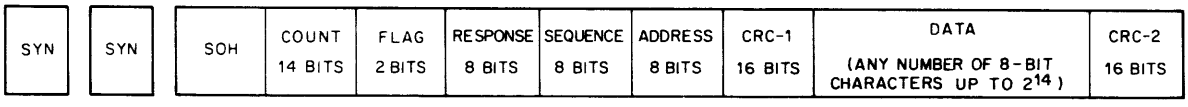

Figure 1-2 DDCMP Data Message Format

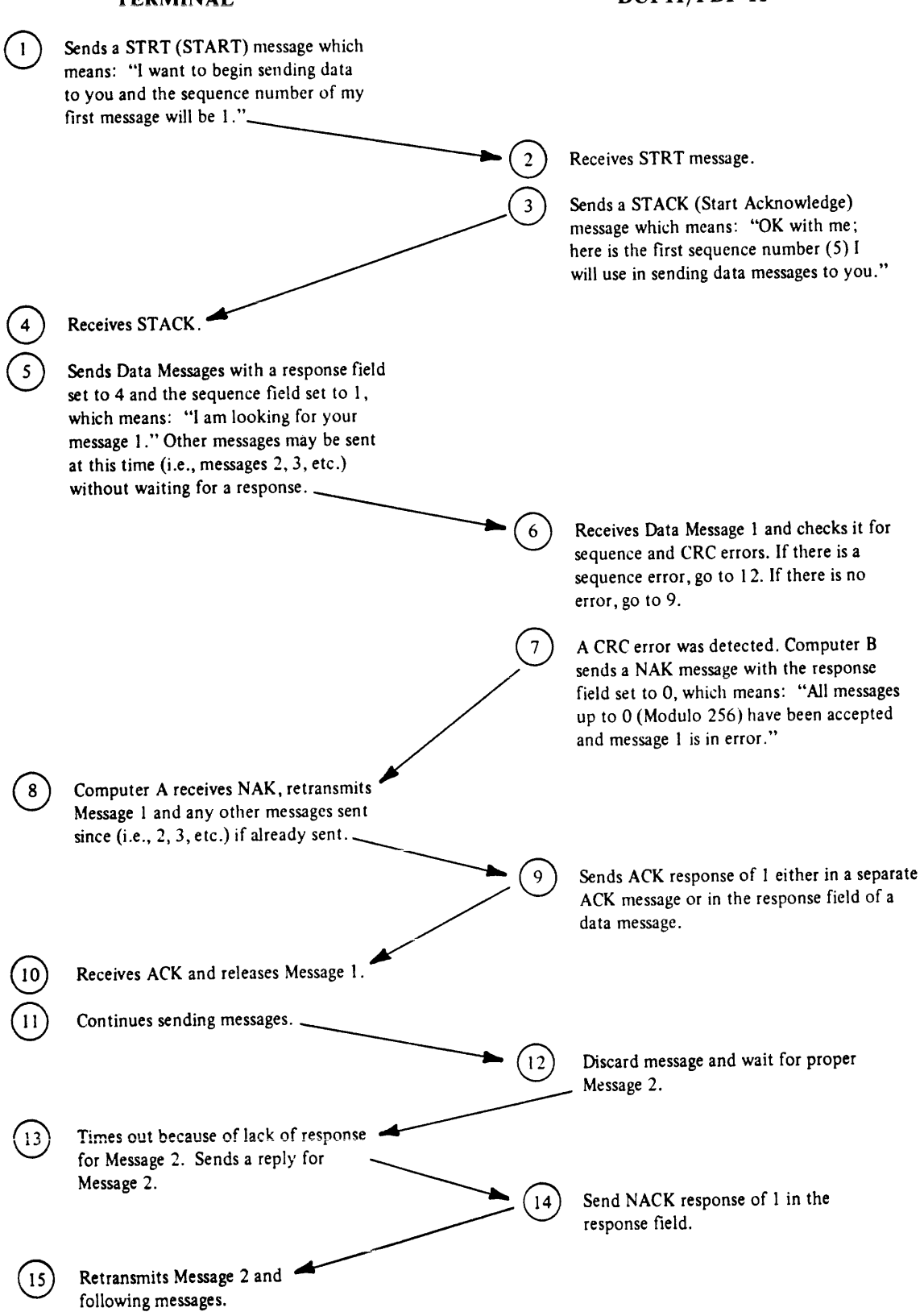

Figure 1-3 DDCMP Sample Handshaking Procedure

1.3.4.2 Error Checking and Recovery - DDCMP uses CRC-16 for detecting transmission errors. When an error occurs, DDCMP sends a separate NAK message. DDCMP does not require an acknowledgment message for all data messages. The number in the response field of a normal header, or in either the special NAK or ACK message, specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgment was sent and message 6 is bad, the NAK message specifies number 5 which says "messages 4 and 5 are good and 6 is bad." When DDCMP operates in full-duplex mode, the line does not have to be turned around - the NAK is simply added to the sequence of messages for the transmitter.

When a sequence error occurs in DDCMP, the receiving station does not respond to the message. The transmitting station detects from the response field of the messages it receives (or via time-out) that the receiving station is still looking for a certain message and sends it again. For example, if the next message the receiver expects to receive is 5, but 6 is received, the receiver will not change the response field of its data messages, which contains 4. This says: "I accept all messages up through message 4 and I'm still looking for message 5."

1.3.4.3 Character Coding - DDCMP uses ASCII control characters for SYN, SOH, ENQ and DLE. The remainder of the message, including the header, is transparent.

1.3.4.4 Data Transparency - DDCMP defines transparency by use of a count field in the header. The header is of fixed length. The count in the header determines the length of the transparent information field, which can be 0 to 16,383 bytes long. To validate the header and count field, it is followed by a 16-bit CRC-16 field; all header characters are included in the CRC calculation. Once validated, the count is used to receive the data and to locate the second CRC-16 which is calculated on the datafield. Thus, character stuffing is avoided.

1.3.4.5 Data Channel Utilization - DDCMP uses either full- or half-duplex circuits at optimum efficiency. In the full-duplex mode, DDCMP operates as two dependent one-way channels, each containing its own data stream. The acknowledgments are the only dependency which must be sent in the data stream in the opposite direction.

Separate ACK messages are unnecessary and reduce control overhead. Acknowledgments are simply placed in the response field of the next message for the opposite direction. If several messages are received correctly before the terminal is able to send a message, all of them can be acknowledged by one response. Only when a transmission error occurs, or when traffic in the opposite direction is light (no data message to send) is it necessary to send a special NAK or ACK message, respectively.

In summary, DDCMP data channel utilization features include:

1. Low control character overhead
2. No "character stuffing"
3. No separate ACKs when traffic is heavy - saving on extra SYN characters and inter-message gaps
4. Multiple acknowledgments (up to 255) with one ACK
5. The ability to support point-to-point and multipoint lines.

1.3.4.6 Synchronization - DDCMP achieves synchronization through the use of two ASCII SYN characters preceding the SOH, ENQ, or DLE. It is not necessary to synchronize between messages as long as no gap exists. Gaps are filled with SYN characters. Two sync characters are required but more are usually transmitted. If synchronization between messages is deliberately lost by sending PAD (all 1s) characters, the inter-message interval must be at least 14 character times in length.

1.3.4.7 Bootstrapping - DDCMP has a bootstrap message as part of the protocol. It begins with the ASCII control character DLE. The information field contains the system reload programs and is totally transparent.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides information for installing and checking out a DUP11 Synchronous Line Interface.

2.2 UNPACKING AND INSPECTION

There is only one version of the DUP11 – the DUP11-DA; it consists of six items (refer to Figure 2-1).

M7867 Bit Synchronous Interface
BC22F-25 Cable
BC08S-10 Cable
H325 Test Connector
H3001 Distribution Panel
74-27292 Bracket*

Inspect these parts for visible damage. Report any damage or shortage immediately to the shipper and the DIGITAL representative.

2.3 TOOLS REQUIRED FOR INSTALLATION

The standard field service tool kit contains all the required tools for the installation of the DUP11.

2.4 PREINSTALLATION SET-UP PROCEDURES

Before installing the DUP11 option, the following five steps must be performed.

1. Examine the eight jumpers (W1 – W8) on the M7867 module. Refer to Figure 2-2 to locate and identify the jumpers. All M7867 modules are shipped with the standard jumper configuration described in Table 2-1. All DUP11 diagnostics must be run on each M7867 utilizing the standard jumper configuration. After successfully completing the diagnostic testing in the shipped configuration, the M7867 may be reconfigured to meet the customer's requirements. MAINDEC CZDPE (DUP11 Quick Verify Test) should then be run to verify operation of the new configuration.

2. The DUP11 device address must be selected in accordance with Paragraph 2.9. For diagnostics, device address default = 760050.

3. The DUP11 vector address must be selected in accordance with Paragraph 2.10. For diagnostics, vector address default = 770.

*Used in configurations not incorporating I/O bulkhead.

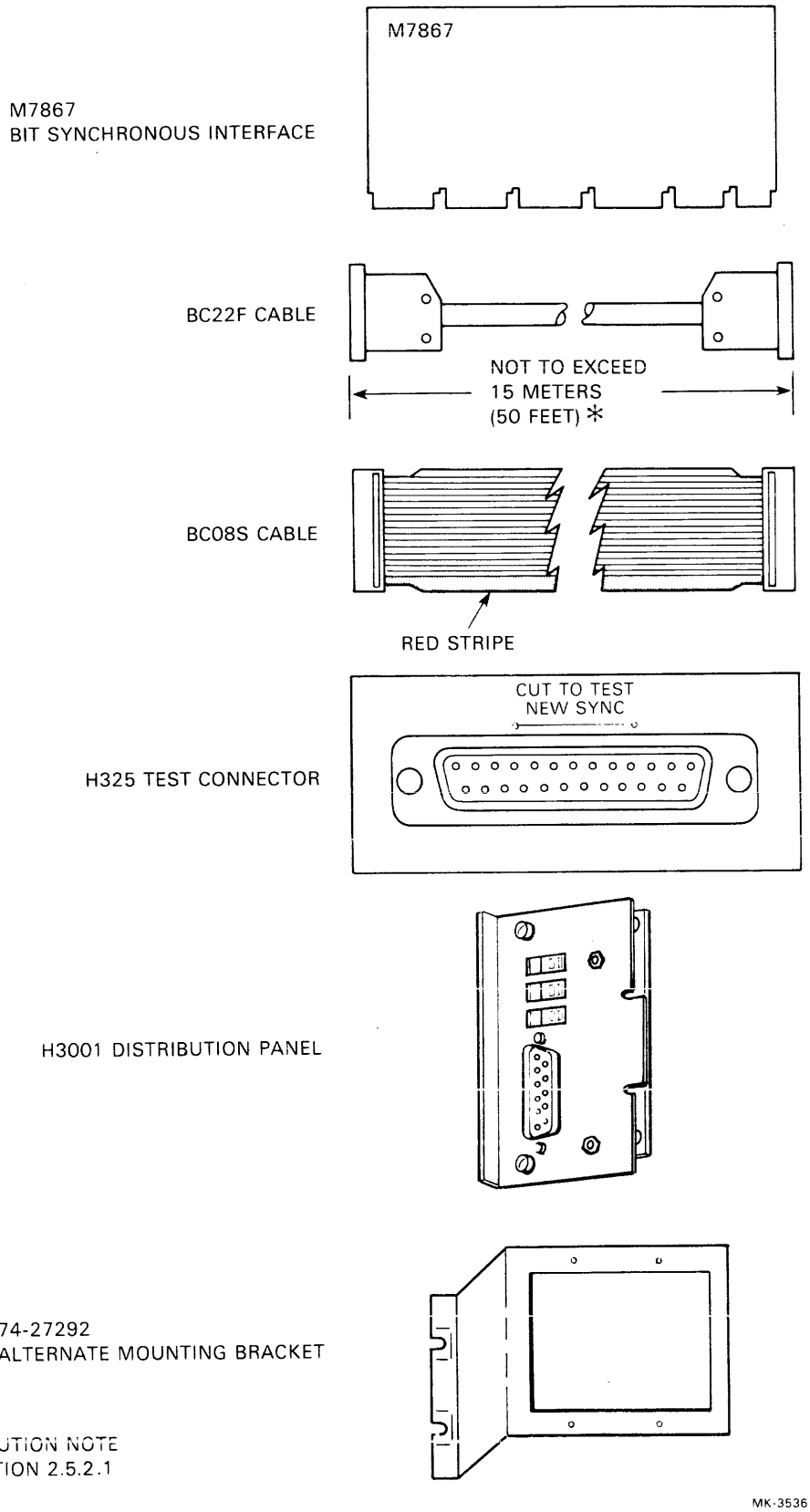

Figure 2-1 DUP11 Parts Diagram

Table 2-1 M7867 Jumper Configuration

Jumper Number	Standard Configuration	Function
W1	Installed	Secondary Receive Enable – With this jumper installed, the state of the data set Secondary Received Data line is received by the DUP11. This jumper is used in conjunction with jumper W2. With this jumper removed, pin JJ of the Berg header is available for some other function.
W2	Removed	Secondary Receive Disable – This jumper must be removed when W1 is installed. Conversely, it must be installed when W1 is removed. When installed, the EIA SEC REC receiver input is grounded; however, this has no effect on the Berg header, cable, or data set.
W3	Installed	Clear option – With this jumper removed, the following bits cannot be directly cleared by DEVICE RESET or BUS INIT. Secondary Transmit Data (RXCSR bit 3) Request to Send (RXCSR bit 2) Data Terminal Ready (RXCSR bit 1) Some data sets may require that these connections be excluded from a device reset function.
W4	Installed	Secondary Transmit Enable – With this jumper installed, the state of the Secondary Transmit Data line is sent to the data set. With this jumper removed, this signal is disconnected at the output of the EIA driver. Some data sets do not use this signal.
W5	Removed	A Data Set Control – With this jumper removed, positive transitions on the Ring line and any transitions on the Clear to Send line set ADAT SET CH. This flag requests a receiver interrupt if the DSITEN bit has been set by the program. With this jumper installed, any transition on three additional lines set ADAT SET CH: Carrier Data Set Ready Secondary Received Data
W6	Installed	A and B Data Set Control – With this jumper installed, transitions on the Carrier, Data Set Ready, and Secondary Received Data lines set BDAT SET CH. This signal is a flag only and does not request interrupts. With this jumper removed, the BDAT SET CH flag (RXCSR bit 0) is inhibited.
W7	Installed	NPR Latency Improvement – With this jumper installed, the NPR latency improvement circuit in the interrupt control logic is enabled. This jumper should be removed only if the DUP11 is installed in a system using a KA11 processor with no KH11 latency reduction option.
W8	Installed	External Clock Enable – Remove for Bell 201A modem.

4. Confirm that a BR5 priority plug is installed in the module. The diagnostics assume a BR5 priority level (see Figure 2-2 to locate and identify the BR5 plug).

5. Set up the H3001 module in accordance with Paragraph 2.7.

2.5 INSTALLATION

Installation of the DUP11 is treated in two paragraphs. Paragraph 2.5.1 contains instructions for installing the M7867 module. Paragraph 2.5.2 contains instructions for installing the H3001 distribution panel.

Examine Figure 2-3. This drawing shows the cabling configuration for the DUP11 installation.

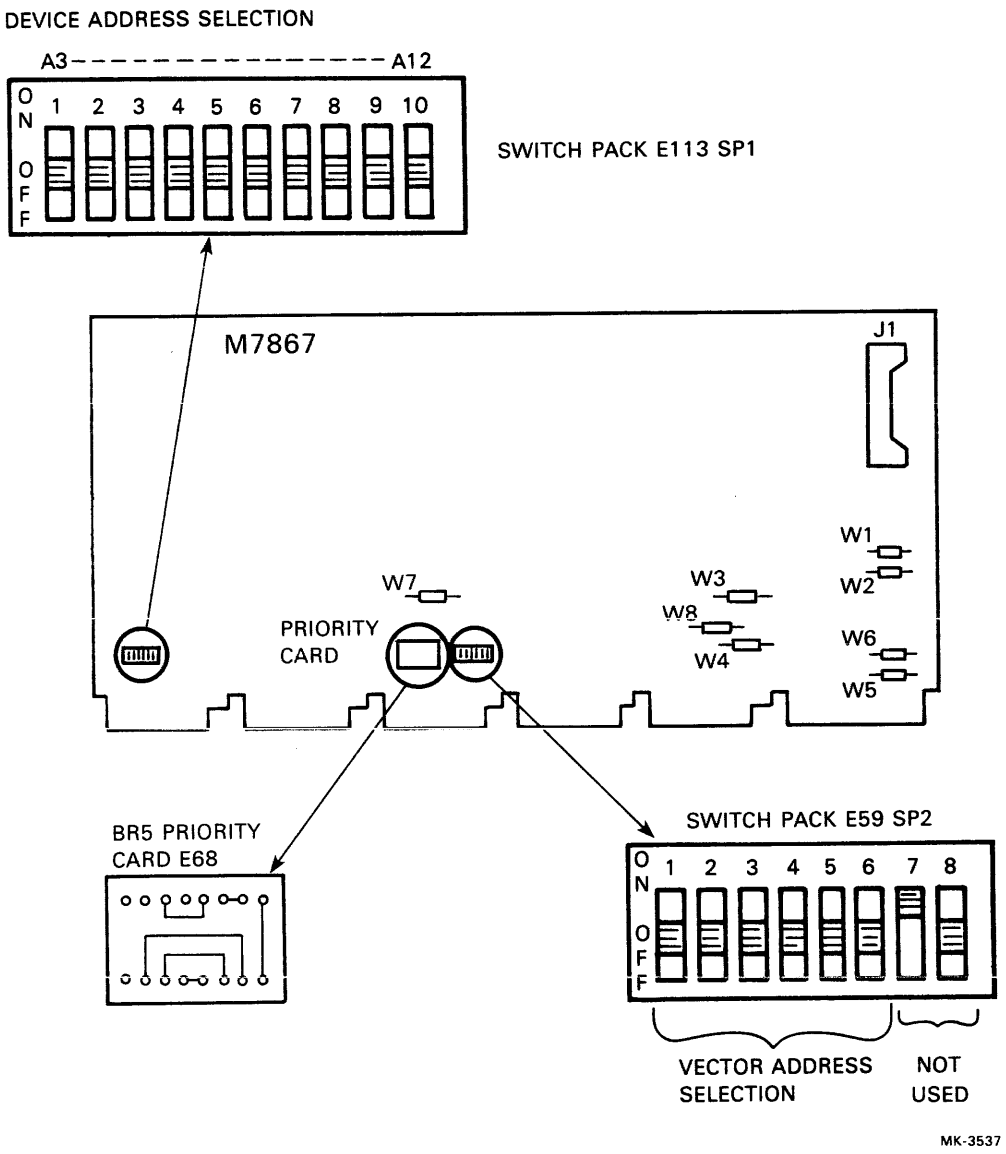

Figure 2-2 Component Location

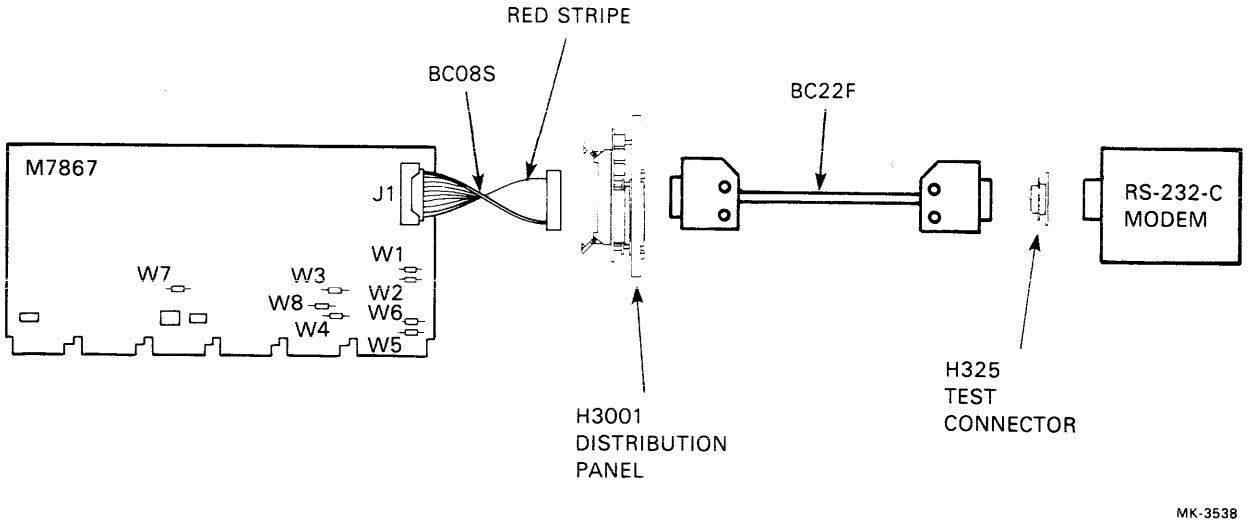

Figure 2-3 DUP11 Cabling

2.5.1 M7867 Module Installation

The DUP11 can be installed in any small peripheral controller (SPC) hex slot in the PDP-11 UNIBUS. Figure 2-4 shows the DD11-B system unit. This unit contains four slots but the DUP11 can only be installed in slots 2 and 3 because of the configuration of the prewired backplane.

WARNING

Turn all power OFF.

CONNECTOR

SLOT	A	B	C	D	E	F
1	UNIBUS IN (NOTE 2)			G727*		
2	M7867 HEX MODULE (NOTE 1)					
3				G727*		
4	UNIBUS OUT (NOTE 3)			G727*		

MODULE SIDE VIEW

*G727 GRANT CONTINUITY MODULE MUST BE INSTALLED IN EACH SLOT IN WHICH AN INTERFACE MODULE IS NOT INSTALLED.

NOTES
1. M7867 CAN BE MOUNTED ONLY IN SLOT 2 OR 3.
2. CAN BE M920 UNIBUS CONNECTOR OR BC11S UNIBUS CABLE.
3. CAN BE M920, BC11A, OR M930 UNIBUS TERMINATOR.

MK-3539

Figure 2-4 DUP11 (M7867 Module) Mounted in DD11-B

The M7867 installation procedure is as follows:

1. Connect the female Berg connector on the BC08S cable (ribbed side up) to the header on the M7867 module.

2. Plug the module into an SPC slot or into slot 2 or 3 of the DD11-B system unit.

2.5.2 H3001 Distribution Panel Installation

Two different approaches to installing the H3001 distribution panel assembly are included in this manual.

FCC regulations necessitate the incorporation of I/O bulkheads in most new installations to limit electromagnetic interference (EMI) leakage. For installations utilizing an I/O bulkhead, follow the steps outlined in Paragraph 2.5.2.1.

Alternate instructions are included for non-FCC compliant cabinets that require a slightly modified installation procedure. If the system does not incorporate an I/O bulkhead, follow the procedures in Paragraph 2.5.2.2.

2.5.2.1 H3001 Installation In an I/O Bulkhead – The following instructions are for cabinets utilizing an I/O bulkhead. If a particular cabinet does not include an I/O bulkhead, omit these steps and follow the instructions in Paragraph 2.5.2.2.

Though there are differences in the orientation and positioning of I/O bulkheads of different levels of the PDP-11, the installation concept is the same. Once the H3001 distribution panel is installed, there should be no openings (panels omitted) left in the I/O frame on the rear of the cabinet which could permit EMI leakage. For this reason, it is important to tighten both mounting screws on the distribution panel. Figures 2-5 and 2-6 depict the various I/O bulkhead types and illustrate the correct approach to each.

1. Gain access to the I/O bulkhead through the door on the rear of the system cabinet and remove one of the 4.5 cm (2 in) wide panels on the bulkhead.

2. Route the remaining BC08S cable through the cabinet and through the opening in the I/O bulkhead at the rear of the cabinet. Keep in mind that the cable must be routed and dressed in a manner compatible with the existing cabinet cabling.

3. Plug the connector on the free end of the BC08S cable into the Berg connector on the rear of the H3001 distribution panel. Make sure that the ribbed side of the cable faces the pins lettered A to UU (not B to VV) of the Berg connector (see Figure 2-9). This assures pin to pin correspondence between the connectors of the M7867 and H3001 modules.

4. Install the panel into the opening of the I/O bulkhead in place of the 4.5 cm (2 in) panel that was removed in Step 1.

NOTE

It is imperative to maintain an interference-free environment outside the cabinet enclosure. Any additional panels that may have been removed to facilitate easier installation of the H3001 must be replaced in order to maintain the integrity of the I/O bulkhead.

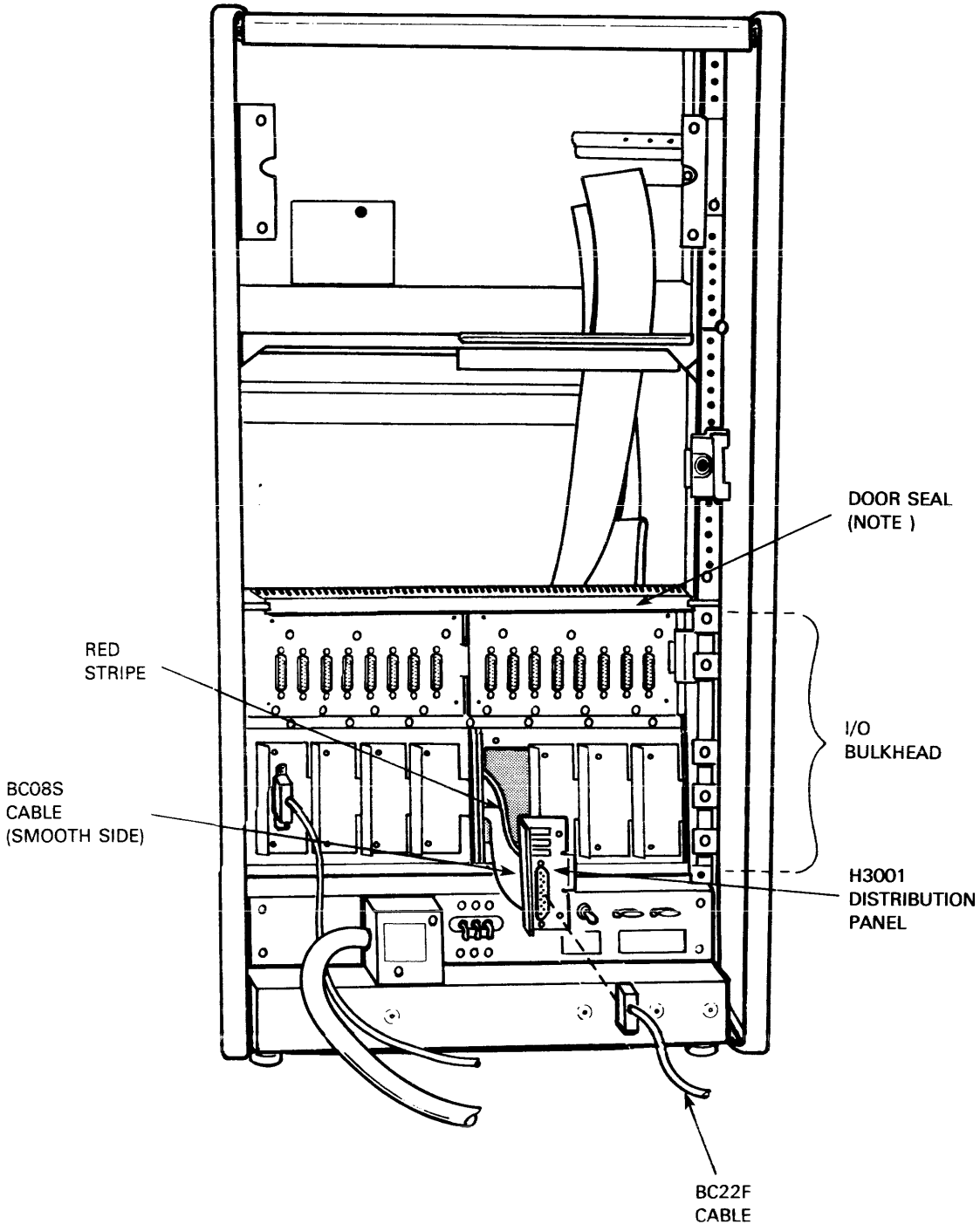

Figure 2-5 H3001 Installation in a Horizontally Oriented I/O Bulkhead

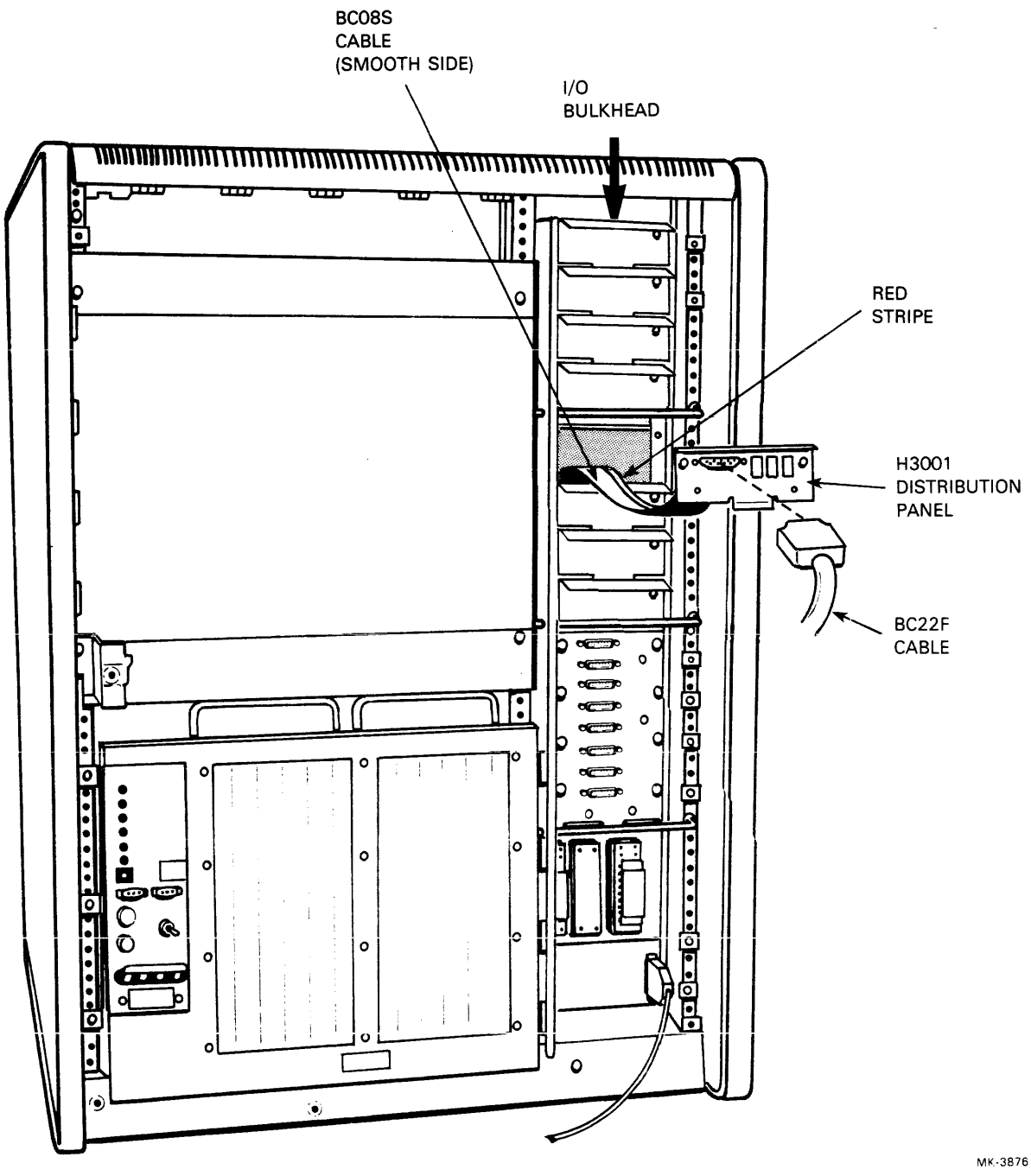

Figure 2-6 H3001 Installation in a Vertically Oriented I/O Bulkhead

5. Connect the female Cinch connector of the BC22F cable to the 25-pin Cinch connector on the rear of the H3001 module. The cable should exit the cabinet with the other signal cables.

CAUTION

BC22F cable lengths in excess of 7.62 meters (25 feet) may exceed the maximum load capacitance defined by the RS-232-C specification. Note, however, that up to 15 meters (50 feet) provides satisfactory DUP11 performance levels.

6. Connect the other end of the BC22F cable to the modem or to the H325 test connector which is the configuration assumed by the diagnostics.

7. Turn power ON.

2.5.2.2 H3001 Installation in Cabinets Without an I/O Bulkhead –

1. Gain access to the rear of the system cabinet and mount the bracket (Part No. 74-27292) to one of the rear side rails as shown in Figure 2-7. Mount the H3001 distribution panel into the bracket.

2. Route the remaining BC08S cable through the cabinet and to the bracket at the rear of the cabinet. Keep in mind that the cable must be routed and dressed in a manner compatible with the existing cabinet cabling.

3. Plug the connector on the free end of the BCO8S cable into the Berg connector on the rear of the H3001 distribution panel. Make sure that the ribbed side of the cable faces the pins lettered A to UU (not B to VV) of the Berg connector (see Figure 2-9). This assures pin to pin correspondence between the connectors of the M7867 and H3001 modules.

4. Connect the female Cinch connector of the BC22F cable to the 25-pin Cinch connector on the rear of the H3001 module. The cable should exit the cabinet with the other signal cables.

CAUTION

BC22F cable lengths in excess of 7.62 meters (25 feet) may exceed the maximum load capacitance defined by the RS-232-C specification. Note, however, that up to 15 meters (50 feet) provides satisfactory DUP11 performance levels.

5. Connect the other end of the BC22F cable to the modem or to the H325 test connector which is the configuration assumed by the diagnostics.

6. Configure the H3001 panel switches according to the chart in Table 2-2.

7. Turn power ON.

Figure 2-8 is included for convenience. Use this figure for quick reference when installing the DUP11 option.

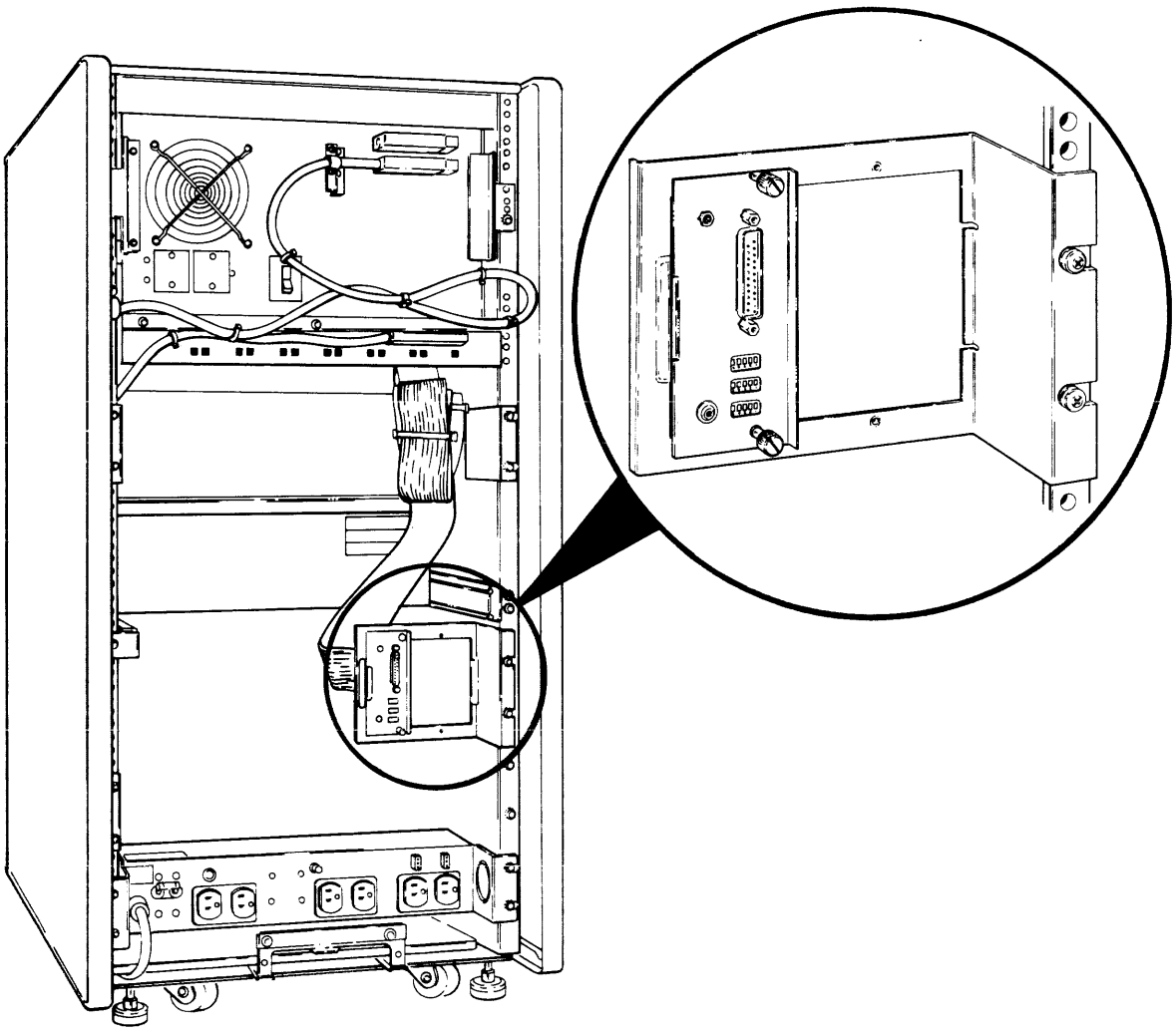

Figure 2-7 Side Rail Installation of H3001 Distribution Panel

Table 2-2 H3001 Switch Settings

	DF03	BELL 201C	BELL 208B	BELL 209A	DIAGNOSTICS & H325
S1					ON
S2					
S3					
S4					
S5					ON
S6					
S7					
S8					
S9					
S10		*			
S11					
S12					
S13					
S14					
S15					

SWITCHES ARE OFF UNLESS OTHERWISE INDICATED

*ON IF NEW SYNC CONFIGURED ON M7867

MK-3838

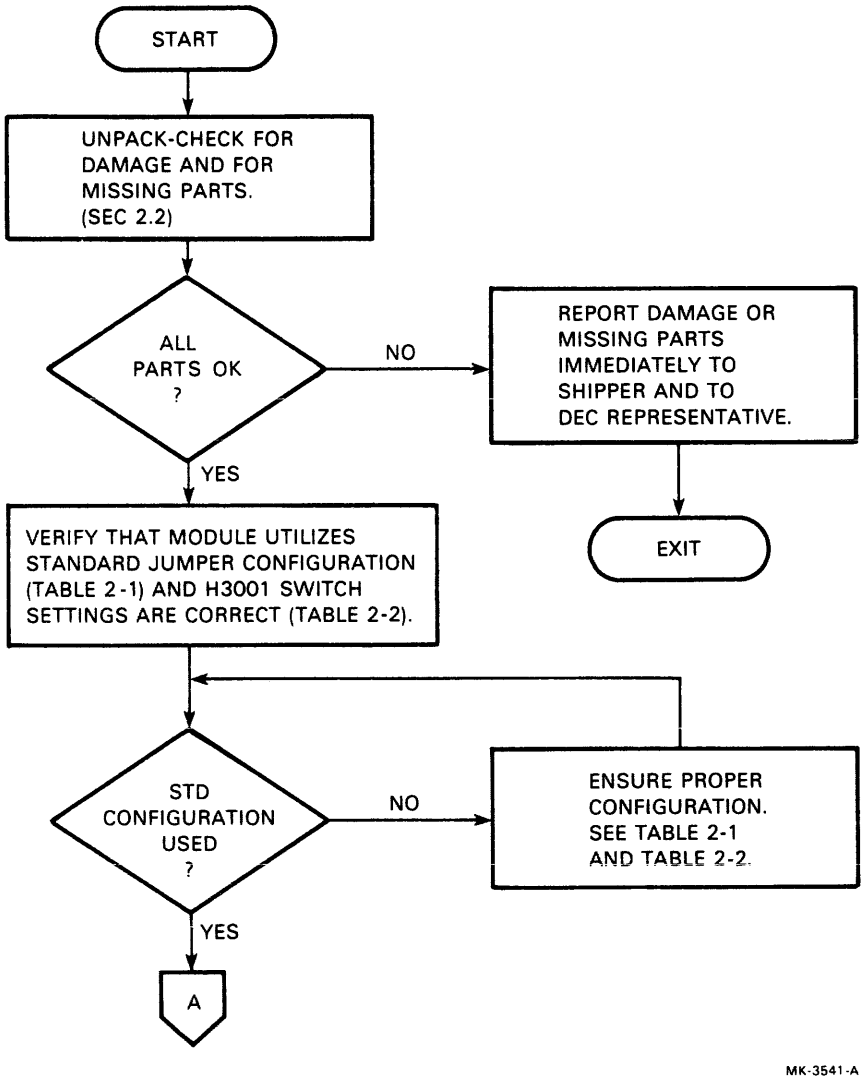

Figure 2-8 Installation Procedure Flowchart (Sheet 1 of 6)

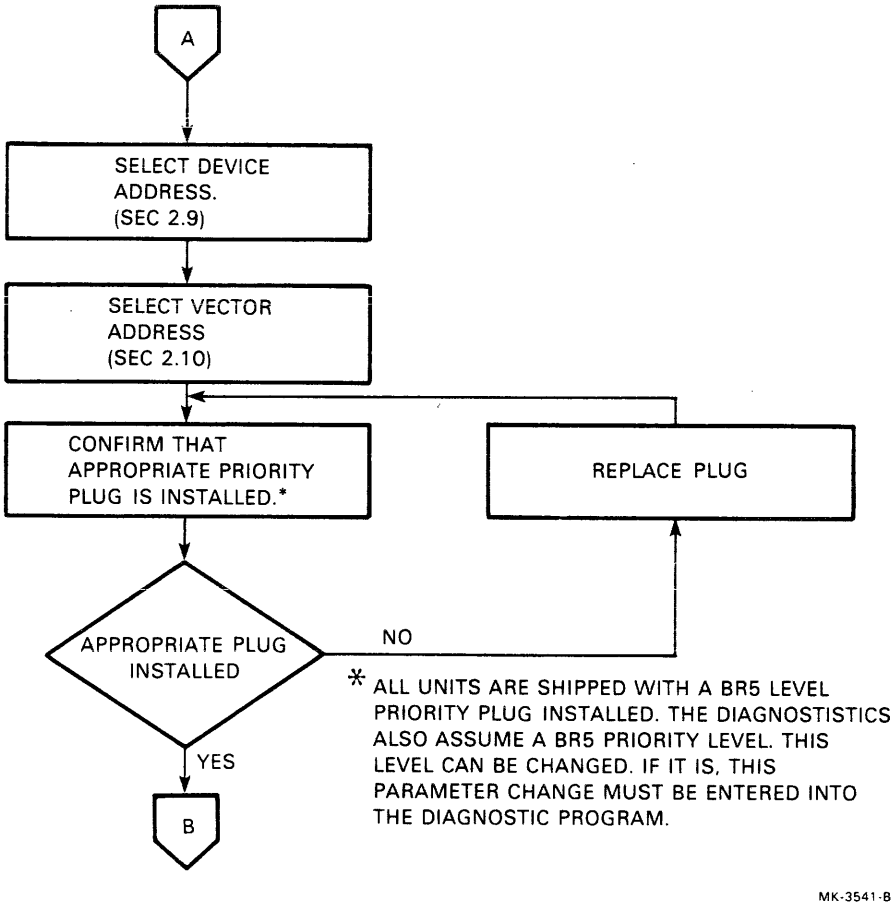

Figure 2-8 Installation Procedure Flowchart (Sheet 2 of 6)

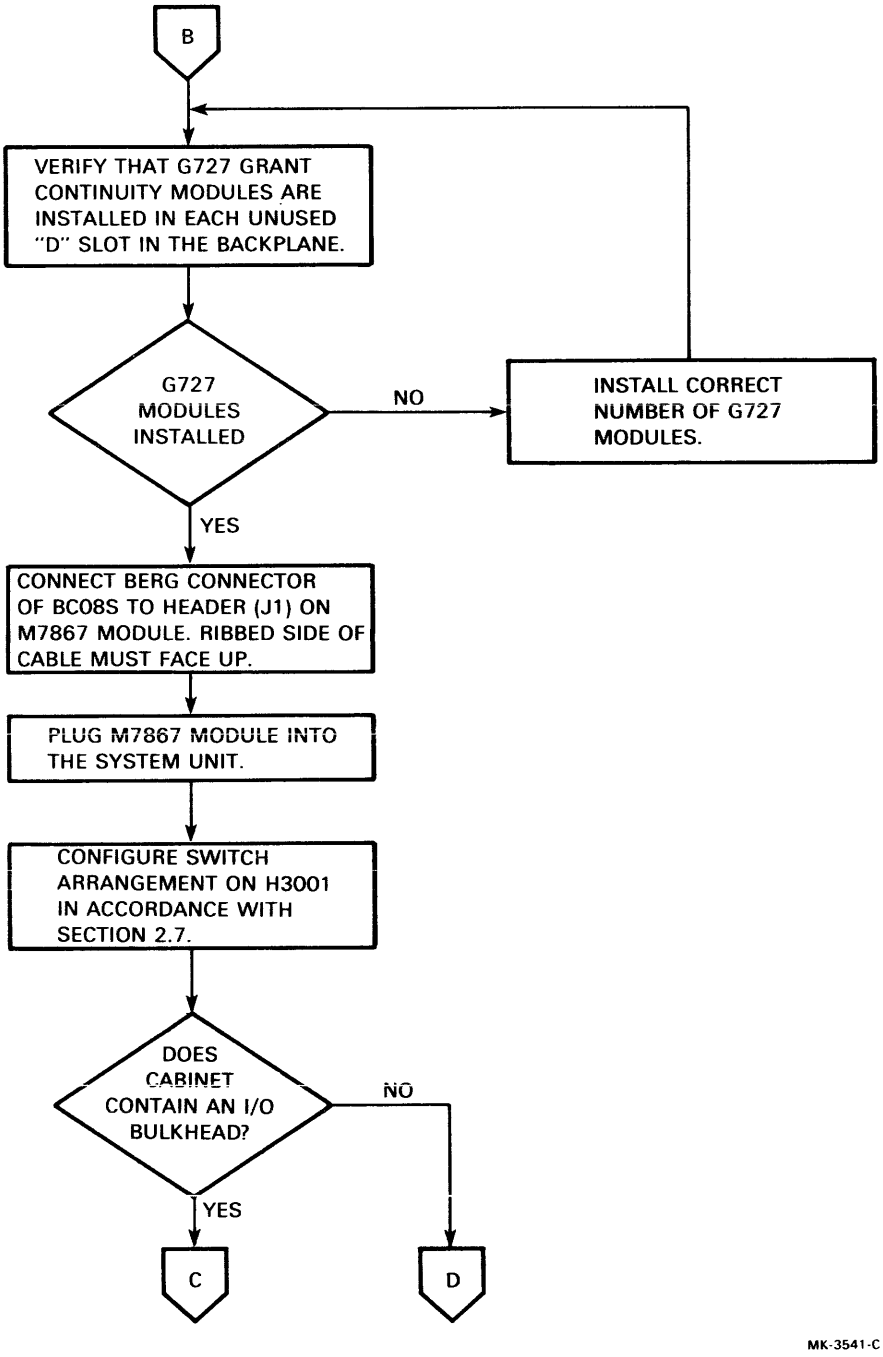

Figure 2-8 Installation Procedure Flowchart (Sheet 3 of 6)

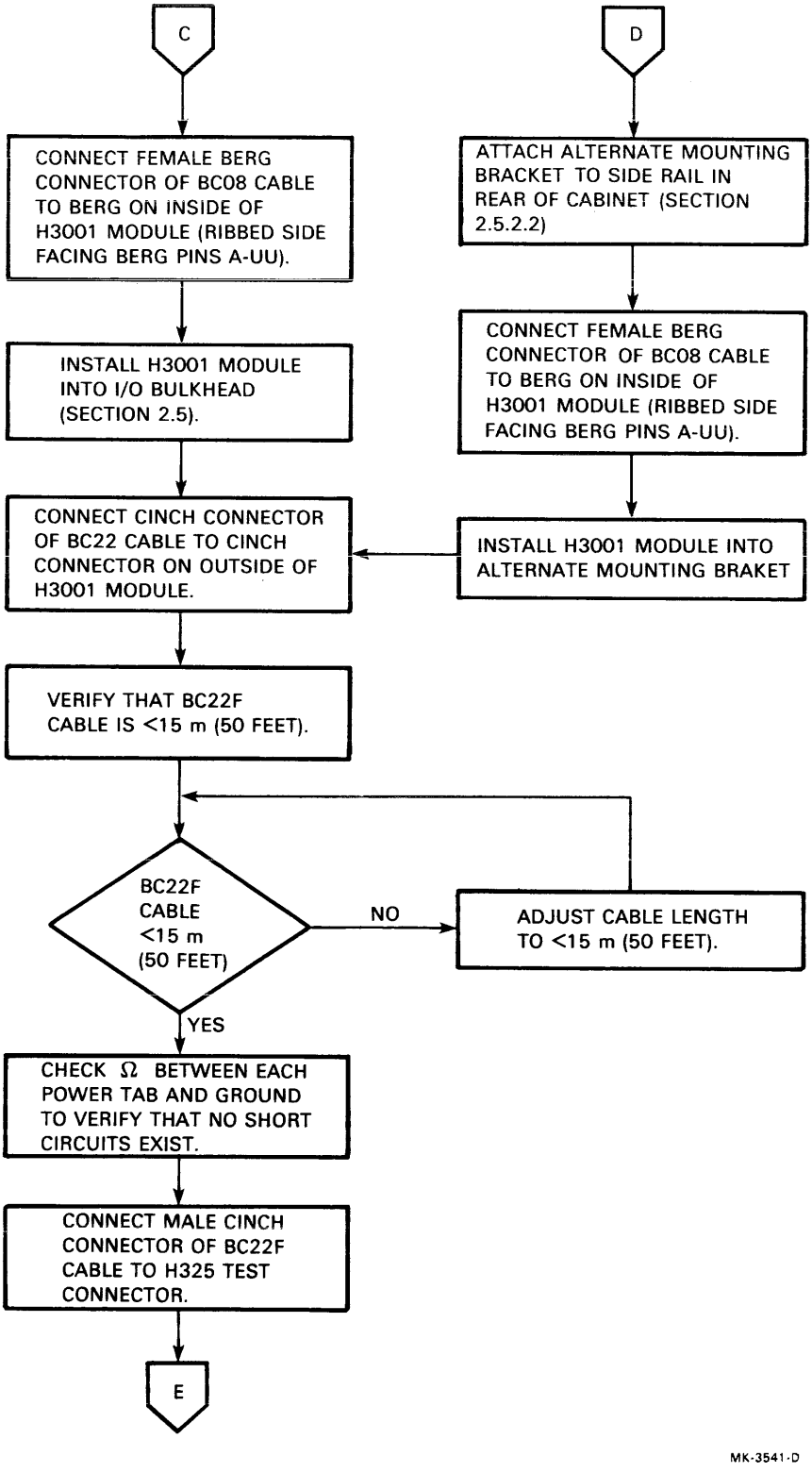

Figure 2-8 Installation Procedure Flowchart (Sheet 4 of 6)

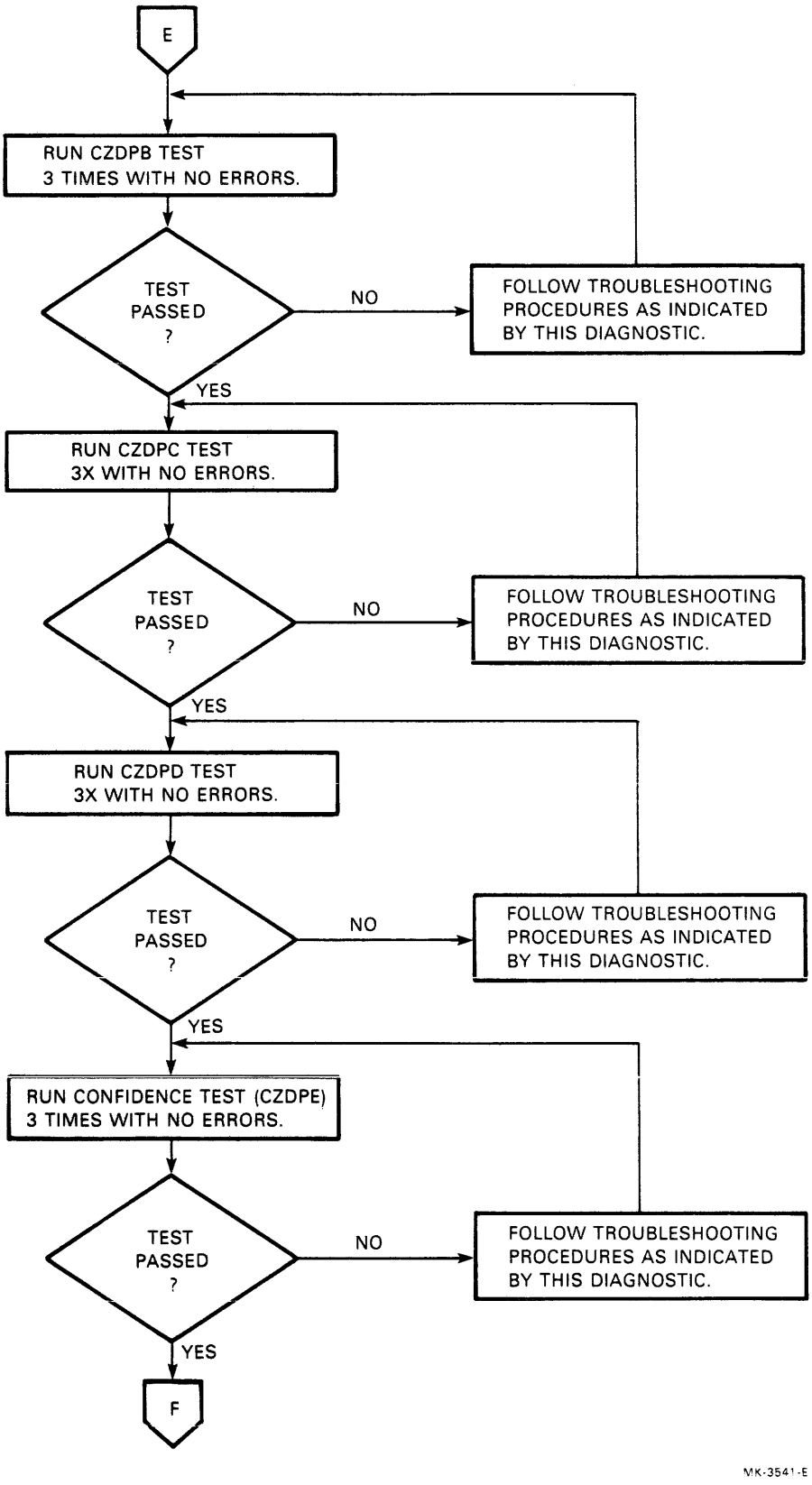

Figure 2-8 Installation Procedure Flowchart (Sheet 5 of 6)

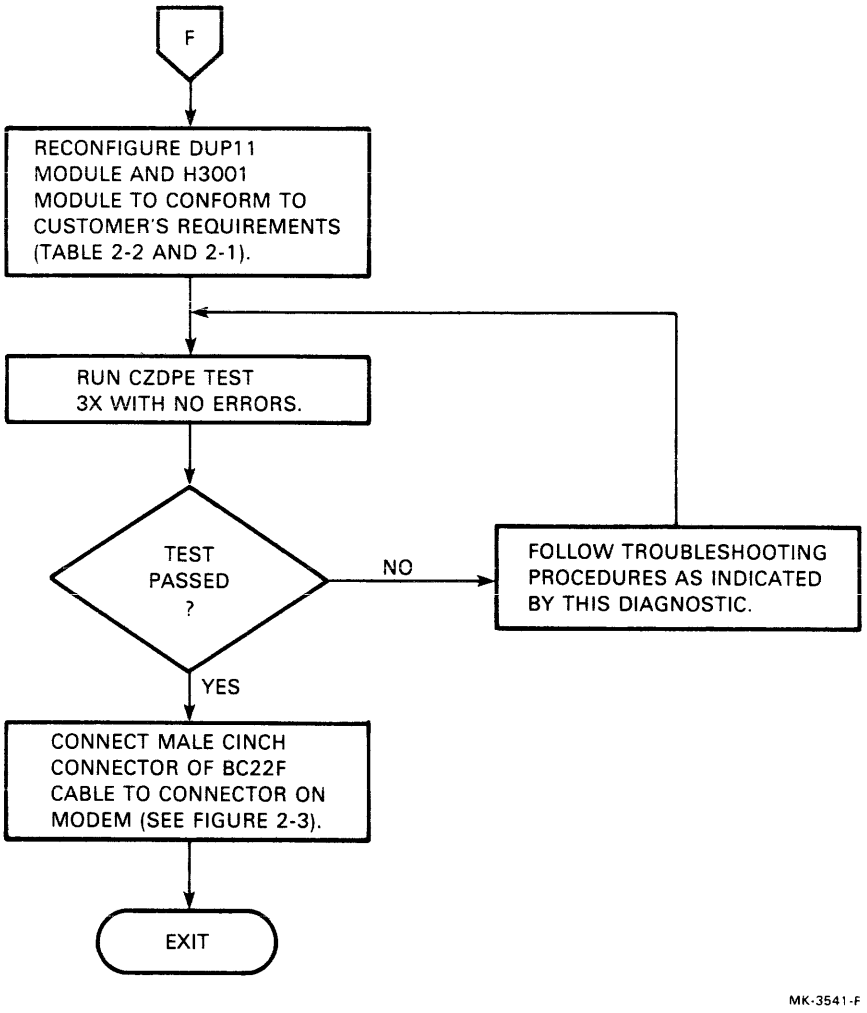

Figure 2-8 Installation Procedure Flowchart (Sheet 6 of 6)

2.6 VERIFICATION OF HARDWARE OPERATION

Verification of proper DUP11 operation is performed by a series of diagnostic programs. A general description of the diagnostics is included in Chapter 5 of the technical manual. Details on the content and use of the diagnostics is contained in the diagnostic documentation package supplied with the DUP11.

Proceed as follows:

1. Run the following diagnostics in the following order:

   CZDPB – Basic and Off-line Transmitter Tests

   CZDPC – Off-line and SDLC Receiver Tests and Off-line Modem Control and Interrupt Tests

   CZDPD – Off-line SDLC and DEC MODE Data and Function Tests

2. Run diagnostic CZDPE. This is a confidence test that requires a dialog with the user to ensure proper setting of the DUP11 and system parameters. It offers a quick test to verify that the DUP11 is operational.

Each diagnostic must make three passes without an error.

Reconfigure the H3001 and the DUP11 in accordance with the customer's requirements (Tables 2-1 and 2-2). Then run diagnostic CZDPE (DUP11 quick verify test) to check the final configuration.

System testing consists of running DECX11 module CXDPB to exercise all DUP11s in a system. Run DECX11 until three error-free passes of module CXDPB are obtained. Note that only four DUP11s can be tested with one DECX11 module.

2.7 COMPATIBILITY

The DUP11 is compatible with the DF03 and Bell type 201™, 208™, and 209™ modems or equivalent. In addition, compatibility with these and other modems is enhanced through the incorporation of the H3001 distribution panel.

Adjust the switches on the H3001 to correspond to the settings indicated in Table 2-2 for the particular modem used in your configuration. The H3001 switches are contained in three DIP switch packages grouped together on the H3001 modules. Refer to Figure 2-9 for the location of these switches. The switches are rocker or slide type and are pushed to the desired position.

A schematic of the H3001 distribution panel is included in Chapter 5 (Figure 5-1) of the technical manual. Use this figure as an aid in determining the proper switch settings and jumper configuration if the modem used is not listed in Table 2-2.

Jumper W1 (see Figure 2-9) is normally not installed. Install this jumper when RS-232 protective ground (pin 1 of Cinch connector) must be connected to enclosure ground. Note that this may introduce an undesirable ground loop.

Bell 201, 208, and 209 are trademarks of Western Electric.

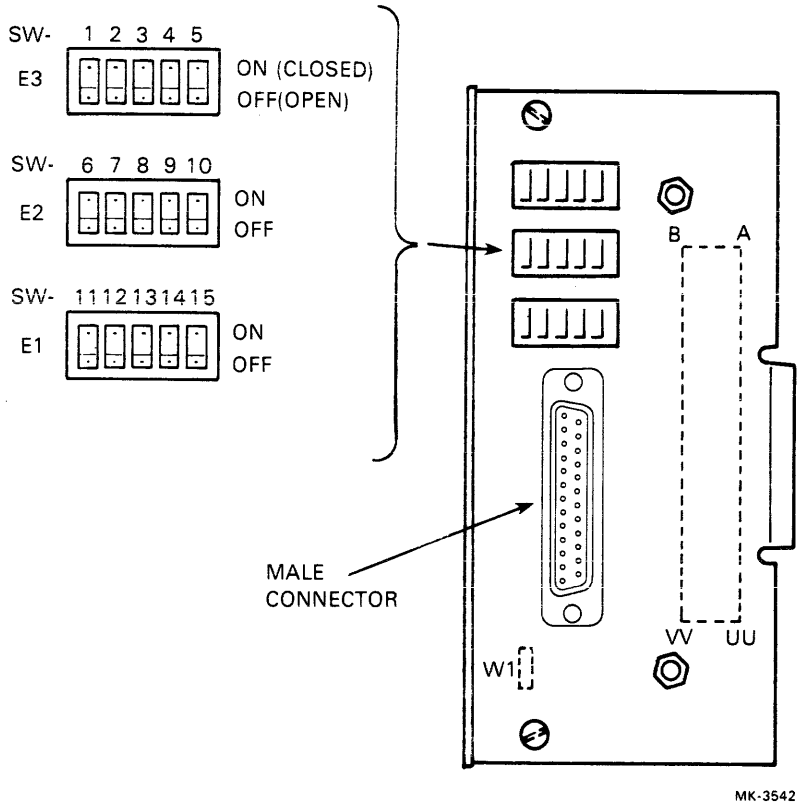

Figure 2-9 H3001 Distribution Panel

NOTE

Due to the extensive variety of modems currently available, DIGITAL cannot guarantee that the DUP11 interface will fully support all features of every modem.

2.8 POWER REQUIREMENTS

The DUP11 requires the following power:

+5 V at 3.6 A
+15 V at 75 mA
−15 V at 75 mA

2.9 DEVICE ADDRESSES

2.9.1 Introduction

Starting with the DJ11, new communications devices are to be assigned floating addresses. The addresses for current production devices are to be retained. The word *floating* means that addresses are not assigned absolutely for the maximum number of each communications device that can be used in a system.

2.9.2 Floating Device Address Assignment

Floating device addresses are assigned as follows:

1. The floating address space starts at location 760010 and extends to location 764000 (octal designations).

2. The devices are assigned in order by type: DJ11, DH11, DQ11, DU11, and DUP11; then the next device is introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

3. The first address of a new type device must start on a modulo 10_8 boundary, if it contains one to four bus-addressable registers. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 has eight registers.

4. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used if the device following it is used. The equivalent of a gap should be left after the last assigned device to indicate that nothing follows.

5. A new type device cannot be inserted ahead of a device on the list.

6. If additional devices on the list are to be added to a system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required to make room for the additions.

The following examples show typical floating device assignments for communications devices in a system:

EXAMPLE 1: No DJ11s, 2 DH11s, 2 DQ11s, and 1 DUP11

760010	DJ11 gap
760020	DH11 #0 first address
760040	DH11 #1 first address
760060	DH11 gap
760070	DQ11 #0 first address
760110	DQ11 gap
760120	DU11 gap
760130	DUP11 #0 first address
760140	Indicates no more DUP11s and no other devices follow.

EXAMPLE 2: 1 DJ11, 1 DH11, 2 DQ11s, and DUP11s

760010	DJ11 #0 first address
760020	DJ11 gap
760040	DH11 #0 first address
760060	DH11 gap
760070	DQ11 #0 first address
760100	DQ11 #1 first address
760110	DQ11 gap
760120	DUP11 gap
760130	DUP11 #0 first address
760140	DUP11 #1 first address
760150	Indicates no more DUP11s and no other devices follow.

EXAMPLE 3: 1 DUP11

760010 DJ11 gap
760020 DH11 gap
760030 DQ11 gap
760040 DU11 gap
760050 DUP11 #0 first address
760060 Indicates no more DUP11s and no other devices follow.

2.9.3 Device Address Selection

In the floating address space (760010-764000), bits 13-17 are always 1s (function of PDP-11 processor). Appendix B of the technical manual shows the PDP-11 memory organization and addressing conventions. Bits 3-12 are selected by switches in the address decoding logic (Table 2-3). With the switch ON (closed), the decoder looks for a 0 on the associated UNIBUS address line; conversely, with the switch OFF (open), the decoder looks for a 1 on the associated UNIBUS address line. Bits 1 and 2 are decoded to select one of four registers. They determine the least significant digit (octal) of the device address because bit 0 is not used for address decoding. It is used to select the proper byte during byte transactions.

Table 2-3 Guide for Setting Switches to Select Device Address

Switch No.	10	9	8	7	6	5	4	3	2	1	Device
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										X	760010
									X		760020
									X	X	760030
								X			760040
								X		X	760050
								X	X		760060
								X	X	X	760070
							X				760100
						X					760200
						X	X				760300
					X						760400
					X		X				760500
					X	X					760600
					X	X	X				760700
				X							761000
			X								762000
			X	X							763000
		X									764000

Notes:
1. X means switch off (open) to respond to logical 1 on the Unibus.
2. Switch numbers are physical positions in switch package 1.

Switch Identification
The device address selection switches are contained in one DIP switch package (E113). Refer to Figure 2-2 for the location of the package. All ten switches in the package are used. The correlation between switch numbers and bit numbers is shown in Table 2-3. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker or slide type and are pushed to the desired position.

The DUP11 requires four addresses:

76XXX0 Receiver Control and Status Register

76XXX2 Receiver Data Buffer Register (Read Only) and Parameter Control and Status Register (Write Only)

76XXX4 Transmitter Control and Status Register

76XXX6 Transmitter Data Buffer Register

2.10 VECTOR ADDRESSES

2.10.1 Introduction
Communications devices are assigned floating vector addresses. This eliminates the necessity of assigning addresses absolutely for the maximum number of each device that can be used in the system.

2.10.2 Floating Vector Address Assignment
Floating vector addresses are assigned as follows:

1. The floating address space starts at location 300 and proceeds upward to 777. Addresses 500-534 are reserved.

2. The devices are assigned in order by type: DC11; KL11/DL11-A, -B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, -D -E; DJ11; DH11; GT40; LPS11; VT20; DQ11; KW11-W; DU11; DUP11; and DV11.

3. If any type device is not used in a system, address assignments move up to fill the vacancies.

4. If additional devices are to be added to the system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required.

2.10.3 Vector Address Selection
Each device interrupt vector requires four address locations (two words) which implies only even-numbered addresses. A further constraint is that all vector addresses must end in 0 or 4. The vector address is specified as a three-digit, binary-coded, octal number using UNIBUS data bits 0-8. Because the vector must end in 0 or 4, bits 1 or 0 are not specified (they are always 0) and bit 2 determines the least significant octal digit of the vector address (0 or 4). The interrupt control logic sends only seven bits (2-8) to the PDP-11 processor to represent the vector address.

The DUP11 is shipped with a BR5 priority selection plug installed in the interrupt control logic. This logic generates two vector addresses: receiver interrupts generate vector addresses of the form XX0, and transmitter interrupts generate vector addresses of the form XX4. For this method of operation, the state of bit 2 is selected by the logic, not by a switch. The two most significant octal digits of the vector address are determined by switches in lines 3-8 (Table 2-4). With the switch OFF (open), a 0 is generated on the associated UNIBUS data line; with the switch ON (closed), a 1 is generated on the associated UNIBUS data line. Also, the NPR jumper (W7) in this logic is left in to improve NPR latency time.

Table 2-4 Guide for Setting Switches to Select Vector Address

Switch No.	1	2	3	4	5	6	Vector
Bit No.	8	7	6	5	4	3	Address
	X			X	X	X	300
	X			X	X		310
	X			X		X	320
	X			X			330
	X				X	X	340
	X				X		350
	X					X	360
	X						370
		X	X	X	X	X	400
		X		X	X	X	500
			X	X	X	X	600
				X	X	X	700

Notes:
1. X means switch off (open) to produce a logical 0 on the Unibus.
2. Switch numbers are physical positions in switch package 2.

Switch Identification

The vector address selection switches are contained in one DIP switch package (E59). Refer to Figure 2-2 for the location of the package. Only six of the eight switches in the package are used. The correlation between switch numbers and bit numbers is shown in Table 2-4. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker or slide type and are pushed to the desired position.

CHAPTER 3
REGISTER DESCRIPTIONS AND OPERATING FEATURES

3.1 INTRODUCTION
This chapter describes the bit assignments for the five DUP11 Registers.

3.2 DUP11 REGISTERS AND DEVICE ADDRESS SELECTION
The five registers used in the DUP11 are shown in Table 3-1. There is no conflict in assigning the same address (76XXX2) to two registers because the RXDBUF is read-only and the PARCSR is write-only.

Communications devices are assigned floating device addresses in the range 760010 to 764000. Rules for assigning floating device addresses are contained in Chapter 2.

3.3 INTERRUPT VECTORS
The DUP11 generates two vector addresses: receiver interrupts (REQ A) generate vector addresses of the form XX0, and transmitter interrupts (REQ B) generate vector addresses of the form XX4.

Communications devices are assigned floating vector addresses in the range 300–777 (500–534 are reserved). Rules for assigning floating vector addresses are contained in Chapter 2.

3.4 PRIORITY SELECTION
The priority selection (BR level) for receiver and transmitter interrupts is selectable on the module via a plug-in priority selection card. The DUP11 is shipped with a priority 5 card installed that establishes BR5 as the bus request level for interrupts.

3.5 REGISTER BIT ASSIGNMENTS
Bit assignments for the five DUP11 registers are shown in Figure 3-1. Each register is described by showing a bit assignment illustration and an accompanying table that discusses each bit in detail.

Table 3-1 DUP11 Registers

Register Name	Mnemonic	Address	Comments
Receiver Control and Status	RXCSR	76XXX0	Word- and byte-addressable. Read/write.
Receiver Data Buffer	RXDBUF	76XXX2	Word-addressable. Read-only.
Parameter Control and Status	PARCSR	76XXX2	Word-addressable. Write-only.
Transmitter Control and Status	TXCSR	76XXX4	Word- and byte-addressable. Read/write.
Transmitter Data Buffer	TXDBUF	76XXX6	Word- and byte-addressable. Read/write.

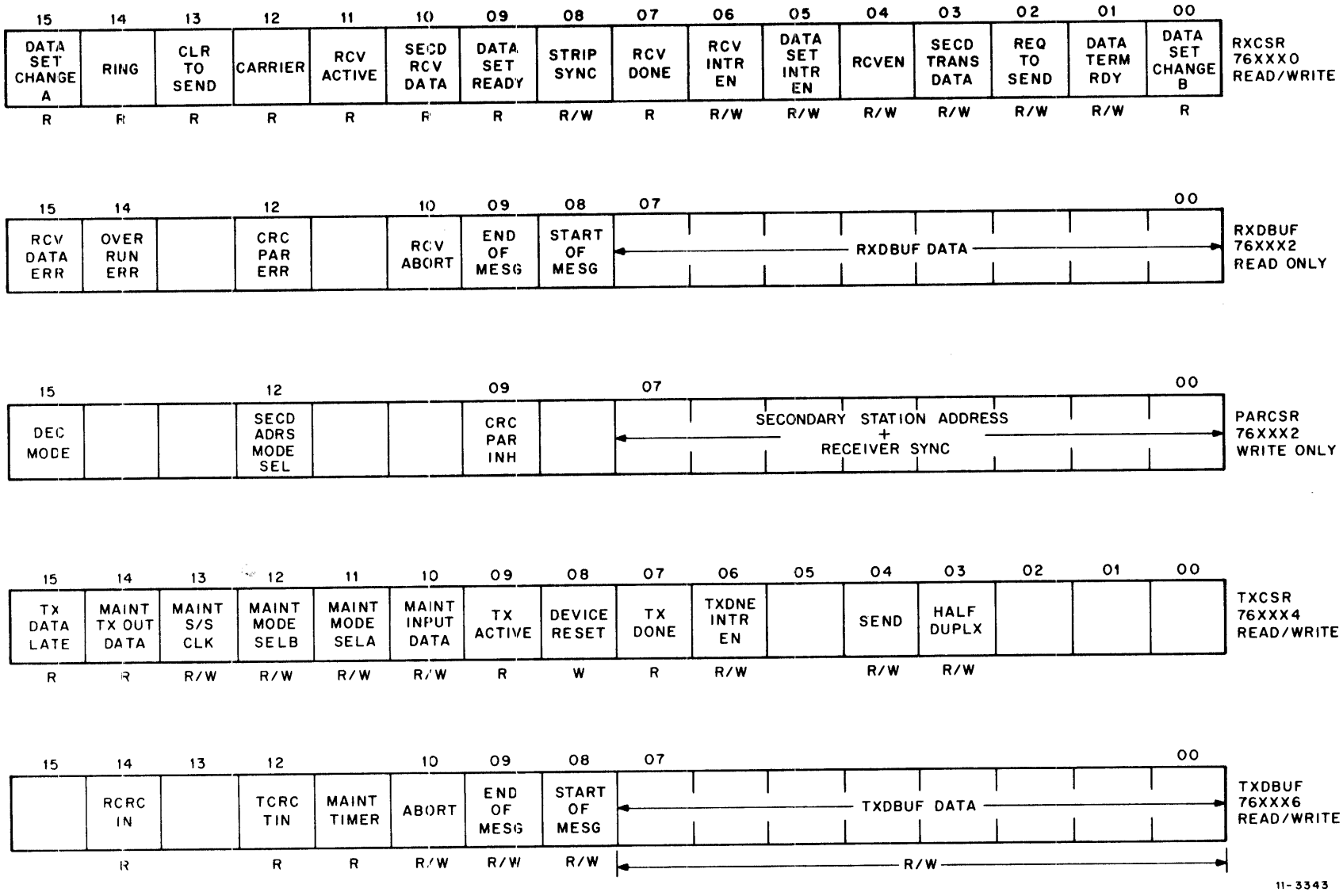

Figure 3-1 DUP11 Register Configurations and Bit Assignments

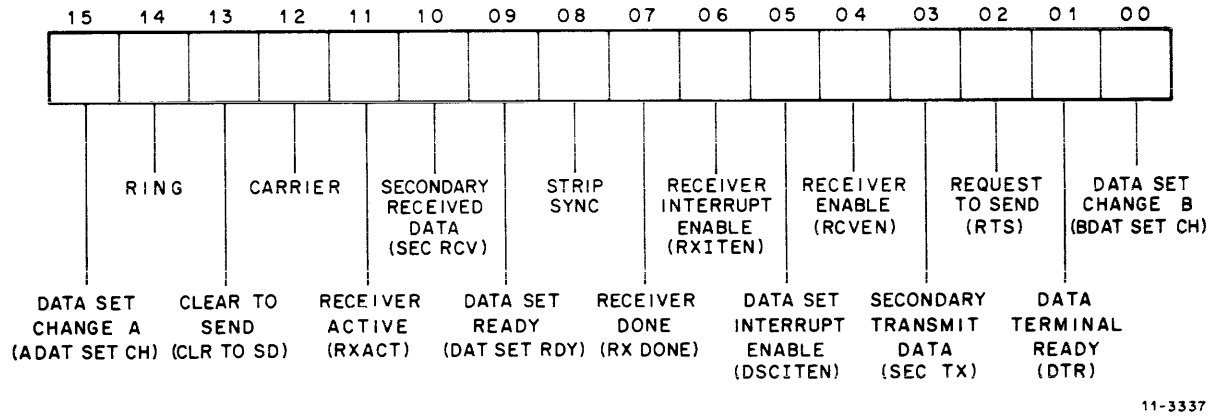

Figure 3-2 Receiver Control and Status Register Format

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Refer to Figure 3-2)

Bit	Name	Description
15	ADAT SET CH (Data Set Change A)	This bit is set when any of the following transitions occur on the data set control lines. A positive transition on the Ring line greater than 10 ms. Any transition on the Clear to Send line. An optional jumper modification allows this bit to be set by any of the following transitions. This modification is a field installation change supported by diagnostics. Any transitions of the Carrier line Any transitions of the Data Set Ready line Any transitions of the Secondary Received Data line Normally these three transitions cause the Data Set Change B bit to be set in this register. If the jumper modification is made, this bit is disabled. If bit 05 (Data Set Interrupt Enable) of this register is set, the assertion of this bit causes an interrupt to the receiver vector. This bit is program read only and is cleared by INIT, device reset or when the RXCSR is read.
14	RING	This bit reflects the state of the modem Ring line. Any positive transition of this line greater than 10 ms causes the Data Set Change A bit to be set. This bit is program read-only.

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Cont)
(Refer to Figure 3-2)

Bit	Name	Description
13	CLR TO SD (Clear to Send)	This bit reflects the state of the Clear to Send line of the modem. Any transition of this line causes the Data Set Change A bit to be set. This bit is program read only.
12	CARRIER	This bit is a direct reflection of the modem carrier. Any change in the state of this line causes Data Set Change B to be set unless the data set change jumper modification has been made. (Refer to bit 15 of this register.) This bit is program read only.
11	RXACT (Receiver Active)	The function of this bit is to reflect the current state of the receiver logic in accordance with the selected mode of operation as defined by the contents of the PARCSR. **SDLC or ADCCP Protocol:** In the SDLC or ADCCP mode of operation, (i.e., DEC MODE cleared) this bit is set by the DUP11 logic when the first character of a message frame is being received. CRC computation is performed for all data received, if not inhibited. If the SECD ADRS MS (Secondary Mode Address Select) bit in the PARCSR is cleared, the receiver's operating mode is that of a primary station. In this mode of operation, the RXACT bit stays asserted until the terminating flag character is received. At this time the RXACT bit is cleared and the REOM bit is asserted. The internal receiver CRC register is tested for an error condition and re-initialized at this time in preparation for the next message, if CRC is not inhibited. If an Abort sequence is not received prior to the terminating flag, the RXACT bit is re-asserted when the first data character of the next message is received. The RSOM bit will appear with this character. Any inter-message flag characters are ignored by the receiver. With the Secondary Address Mode Select bit asserted in the PARCSR, the receiving station operates as a secondary station. The major difference between the primary and secondary modes, as far as the DUP11 hardware is concerned, is the character subsequent to the last initial flag character. In secondary mode, this character must match the contents of the low byte of the PARCSR; if not, the RXACT will not be set and the receiver logic searches for the next flag sequence.

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Cont)
(Refer to Figure 3-2)

Bit	Name	Description
		If extended secondary addressing is implemented in a system, (i.e., 16-bit addresses), the second byte of the address must be recognized by the software. **DDCMP or BISYNC Protocol:** Setting the DEC MODE bit in the PARCSR causes the DUP11 to operate in a manner compatible to the DDCMP or BISYNC family protocols. The low byte of the PARCSR must be loaded with the SYNC character being utilized by the system. This regiter is used only by the receiver logic for comparison purposes. It is not utilized by the transmitter logic. When the RCVEN bit is asserted, the receiver logic searches the received data stream for two consecutive SYNC characters. When two consecutive SYNC characters have been recognized, the receiver is to be considered synchronized to the transmitting station. At this time, all characters subsequent to the two SYNC characters that caused the synchronization are presented to the program (i.e., RXDONE is set) conditional on the character and the state of the STRIP SYNC bit asserted by the program. The RXACT bit is normally asserted when the first character is received subsequent to the synchronization process, unless the STRIP SYNC bit is set. If STRIP SYNC is set, the assertion of RXACT by the DUP11 logic is delayed until the first non-sync character is received. Once RXACT is asserted, the CRC detection logic is activated, provided it is not inhibited in the PARCSR (bit 9) and the STRIP SYNC function is disabled internally. When the completion of the message has been detected, the program must clear the RCVEN bit to re-initialize the receiver. Clearing the RCVEN bit causes the RXACT bit to be cleared also. This bit is program read only and is cleared by INIT, device reset, an off transition of RCVEN, and an ABORT sequence is received in the SDLC or ADCCP mode.
10	SEC RCV (Secondary Received Data)	This bit reflects the state of the Secondary Received Data line from the modem. Any transition on this line causes the Data Set Change B bit to be set unless the data set change jumper modification has been installed. Refer to bit 15 of this register. Used with certain modems only. This bit is program read only.

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Cont)
(Refer to Figure 3-2)

Bit	Name	Description
9	DAT SET RDY (Data Set Ready)	This bit reflects the state of the Data Set Ready (or interlock) lead from the modem. When asserted, this line indicates that the modem is powered up, is not in test, talk, or dial mode. Any transition of this bit causes the Data Set Change B bit to be asserted unless the data set change jumper modification has been installed. Refer to bit 15 of this register. Program read only.
8	STRIP SYNC	This bit is used only with the DDCMP or BISYNC family protocols. Once the receiver has achieved synchronization, any characters received that match the contents of the low byte of the PARCSR and are contiguous to the initial SYNC characters are not presented to the program (i.e., RXDONE will not be set) if this bit is set. This is useful in stripping off any SYNC characters that are subsequent to the SYNC characters that caused the actual syn chronization of the receiver logic. **NOTE** **This bit must be cleared when the SDLC or ADCCP mode is invoked. Failure to clear this bit disables the receiver logic.** This bit is program read/write and is cleared by INIT or device reset.
7	RXDONE (Receiver Done)	This bit is set by the device when the RXACT bit is set and a character is transferred from the internal receiver shift register into the RXDBUF (receiver data buffer) for the program's acceptance. This bit is also set whenever SYNC characters are received immediately subsequent to the actual synchronization SYNC character, unless the STRIP SYNC bit is set. This applies only to DDCMP or BISYNC modes. In SDLC mode, this bit also is set when an ABORT sequence is received or when the REOM bit is set in the RXDBUF. The RABORT bit in the RXDBUF is asserted when an ABORT sequence is received while the RXACT bit is asserted, or when seven consecutive 1s are detected following a final flag character. In the latter case, RXACT is clear when RXDONE is set and occurs only for the first received ABORT sequence.

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Cont)
(Refer to Figure 3-2)

Bit	Name	Description
		This bit is program read and is cleared by reading the RXDBUF, INIT, or Device Reset. An interrupt request is generated if the Receiver Done Interrupt Enable bit is set when this bit is asserted.
6	RXITEN (Receiver Interrupt Enable)	When set, this bit allows interrupt requests to be made to the receiver vector if the RXDONE bit is set. All interrupts should be serviced at a processor level equal to or higher than the device Bus Request level which is shipped at level 5. This bit is program read/write and is cleared by INIT or device reset.
5	DSCITEN (Data Set Interrupt Enable)	When set, this bit allows interrupt requests to be made to the receiver vector if the Data Set Change A bit is set. All interrupt requests should be serviced at a processor level equal to or higher than the device interrupt request level which is shipped at level 5. This bit is program read/write and is cleared by INIT or Device Reset.
4	RCVEN (Receiver Enable)	This bit controls the operation of the receiver logic. When initially set, the receiver is enabled to search for synchronization, irrespective of the DUP11's operating mode. Once synchronization has been achieved, the reception of received data and timing is controlled by this bit. Clearing this bit at any time causes all receiver timing and control functions to be reset asynchronously to the modem clock or the data stream currently being received. The RXDONE bit is cleared by the off transition of this bit. This bit is program read/write and is cleared by INIT and device reset.
3	SEC TX (Secondary Transmit Data)	This bit is connected to the Secondary Transmit line of the modem. Supervisory data can be transmitted over this line at a reduced rate. This applies to certain modems only. This bit is program read/write and is optionally cleared by INIT or Device Reset.

Table 3-2 Bit Descriptions for Receiver Control and Status Register (RXCSR) (Cont)
(Refer to Figure 3-2)

Bit	Name	Description
2	RTS (Request to Send)	When set, this bit causes the Request to Send lead to be asserted at the modem interface. This bit is program read/write and is optionally cleared by INIT and Device Reset.
1	DTR (Data Terminal Ready)	When set, this bit causes the Data Terminal Ready lead to be set. For auto dial and manual call origination, it maintains the established call. For auto answer, it allows handshaking in response to a Ring signal. This bit is program read/write and is optionally cleared by INIT or device reset.
0	BDAT SET CH (Data Set Change B)	This bit is asserted when any of the following transitions occur on the respective data set control lines. Any transition of the Carrier line Any transition of the Data Set Ready line Any transition of the Secondary Received Data line Two optional jumper modifications can be made in the field with respect to this bit, the normal jumper configuration is as cited above. Removing the data set change jumper inhibits the setting of the Data Set Change B bit. The Data Set Change B bit is inhibited and the signal transitions cited above are combined with the signal transitions that set Data Set Change A. In this case Data Set Change A is also set by the transitions cited above. These variations are supported by diagnostics. This bit is program read and is cleared by INIT, device reset or by reading the RXCSR.

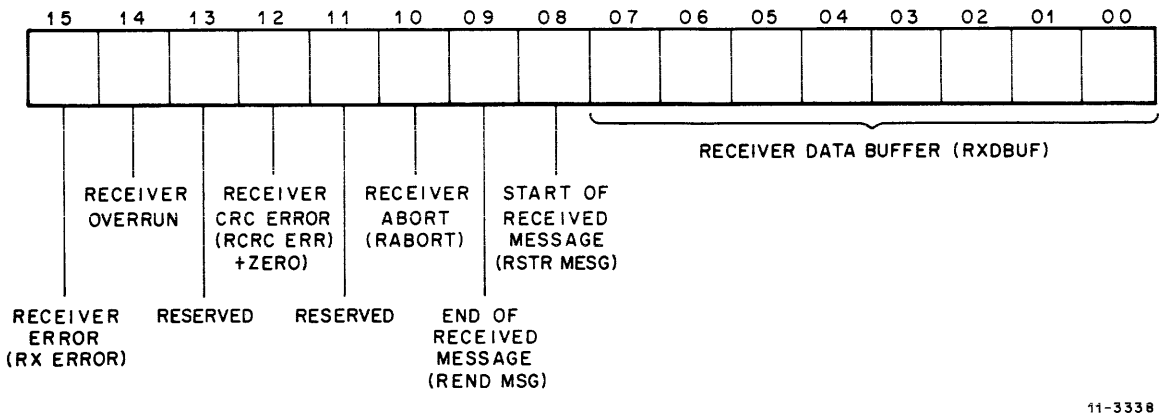

Figure 3-3 Receiver Data Buffer Register Format

Table 3-3 Bit Descriptions for Receiver Data Buffer Register (RXDBUF) (Refer to Figure 3-3)

Bit	Name	Description
15	RX ERROR (Receiver Error)	This bit is set if one of the three error bits in the RXDBUF is set. (Logical OR of bits 14, 12, and 10.) **NOTE** **If the DEC mode bit is set, the setting of bit 12 does not cause this bit to be set.** This bit is program read only and is cleared only when bits 14, 12, or 10 are cleared.
14	REC OVERRUN (Receiver Overrun)	When the receiver logic detects an overrun condition, this bit is set. An overrun is caused primarily by poor program response time. Once the RXDONE bit is set, the program must respond within (1/bps) (8+n) (bit time) sec: if not, overrun occurs. This condition indicates the loss of at least one character. This bit causes the error bit to be set. This bit is set for a minimum of one character time. This bit is cleared within one character time after the overrun condition has been relieved by reading the RXDBUF (i.e., When the next transfer from the internal receiver shift register into the RXDBUF occurs). The Receiver Error bit is set when this bit is set. n = number of inserted zero bits (SDLC or ADCCP only) ($n \leqslant 2$) This bit is program read only and is cleared by INIT, device reset, or by clearing RCVEN.

Table 3-3 Bit Descriptions for Receiver Data Buffer Register (RXDBUF) (Cont)
(Refer to Figure 3-3)

Bit	Name	Description
13		Reserved.
12	RCRC ERR + ZERO (Receiver CRC Error)	When the SDLC or ADCCP mode is selected, this bit is set when the receiver logic detects a CRC error upon termination of a message. The error check is made only when the REOM bit is set in the RXDBUF. When the DDCMP protocol is being used, this bit is set when the internal receiver CRC register is equal to zero. When this bit is set, it stays set for one character time, or until the next transfer is made into the RXDBUF from the internal receiver shift register. The Receiver Error bit is set when this bit is set if the DEC MODE bit is cleared in the PARCSR. This bit is program read and is cleared by INIT, device reset, or by clearing RCVEN.
11		Reserved.
10	RABORT (Receiver Abort)	When an SDLC or ADCCP abort sequence has been received, this bit is set. All receiver timing, internal control and registers are reset. The receiver logic detects ABORT sequences, providing an initial or final flag character has been received. The ABORT sequence is defined as seven or more contiguous 1s. If multiple ABORT sequences are being transmitted the receiver indicates reception of only the first ABORT of the sequence. If the RCVEN bit is left asserted, the receiver resumes searching for a flag synchronization sequence. The RXDONE bit is set when the abort sequence is received and the Receiver Error bit is set also. This bit is cleared by INIT, device reset, clearing RCVEN, or reading the RXDBUF.
9	REND MESG (End of Received Message)	This bit is functional only in SDLC or ADCCP mode. It is set when a terminating flag character is received. This occurs when a flag character is received with the RXACT bit set. When this bit is set, bits 07–00 of this register are invalid. This bit is set for a minimum of one character time. The next transfer from the receiver shift register into the RXDBUF clears this bit. This bit is program read and is cleared by INIT, device reset, or by clearing RCVEN.

Table 3-3 Bit Descriptions for Receiver Data Buffer Register (RXDBUF) (Cont)
(Refer to Figure 3-3)

Bit	Name	Description
8	RSTR MESG (Start of Received Message)	This bit is functional only in SDLC or ADCCP mode. When operating in the primary mode, this bit is set when the first data character is received. When operating in the secondary mode, this bit is set if the character following the last received flag matches the contents of the secondary station address register. This bit is set for a minimum of one character time. The next transfer from the receiver shift register into the RXDBUF clears this bit. This bit is program read and is cleared by INIT, device reset, or by clearing RCVEN.
7-0	RXDBUF (Receiver Data Buffer)	This register contains the data received from the modem. All characters that are presented to the program through this register are eight bits. All characters in this register are right-adjusted with bit 00 being the least significant bit, and bit 07 being the most significant bit. When the End of Received Message bit is set, the data in this register is not valid. If CRC checking is being used, the last two characters that precede the setting of the End of Received Message bit are the CRC check characters that were transmitted. These bits are program read and are cleared by INIT, device reset, RABORT, or by clearing RCVEN.

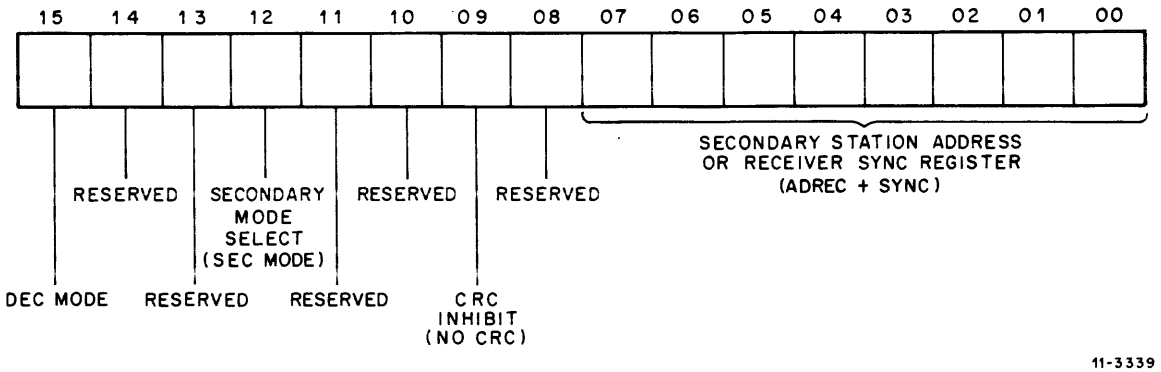

Figure 3-4 Parameter Control and Status Register Format

Table 3-4 Bit Descriptions for Parameter Control and Status Register (PARCSR) (Refer to Figure 3-4)

Bit	Name	Description
		NOTE **The contents of the PARCSR register should be modified only when the transmitter and receiver are in the idle state.**
15	DEC MODE	When this bit is set, the DUP11 logic operates in the manner compatible with the DDCMP or BISYNC protocols. If this bit is clear, the device operates as an SDLC or ADCCP station. As a DDCMP or BISYNC type interface, the receiver logic is synchronized to the transmitting station when two or more consecutive SYNC characters have been recognized. The SYNC character used in the system must be loaded into the low byte of the PARCSR before the RCVEN bit is set. The transmitter logic has no ability to idle SYNC characters from the low byte of the PARCSR. When it is required to transmit SYNC character, the program must load the SYNC character into the TXDBUF. The program should also set the TSOM bit in the TXDBUF when the SYNC character is loaded. This is done to inhibit the inclusion of the SYNC character in the computation of the transmit CRC check character, if CRC is not inhibited. Setting the TSOM also suppresses the setting of the TXDAT LATE (transmit data late) bit. This is useful if the need to idle SYNCs existed. In this case, the program would load the SYNC character into the TXDBUF along with the TSOM bit, and the SYNC character would be transmitted until the program initiated a new operation. During this period, the servicing of the TXDONE could be disregarded without causing the TXDAT LATE error. The bit is program write and is cleared by INIT or device reset.
14, 13		Reserved.
12	SEC MODE (Secondary Mode Select)	Used with SDLC family protocols only. Cleared for DDCMP and BISYNC operation. When this bit is cleared, the device operates as a primary station. All data subsequent to the last received flag character is presented to the program until the termination flag is received. Secondary station operation is in effect when this bit is set. In this mode, only messages that are prefixed with the correct secondary address are presented to the program. The secondary station address must have been loaded into the low byte of the PARCSR before the RCVEN bit was set. The actual address character is not presented to the program in the secondary mode.

Table 3-4 Bit Descriptions for Parameter Control and Status Register (PARCSR) (Cont)
(Refer to Figure 3-4)

Bit	Name	Description
		If extended secondary addresses are used, (i.e., 16-bit address), the first 8 bits of the address can be detected by the hardware. The software must confirm the next 8 bits of address. This bit is program write and is cleared by INIT or device reset.
11, 10		Reserved.
9	NO CRC (CRC Inhibit)	When set, this bit inhibits the transmission of the CRC check character and testing of the CRC error detection logic during reception. This bit is program write and is cleared by INIT or device reset.
8		Reserved.
7-0	ADREC + SYNC (Secondary Station Address Register or Receiver SYNC Register)	This register contains the desired secondary station address when operating in the SDLC or ADCCP secondary mode. The contents of this register is compared to the character received in the shift register (excluding zeros inserted for transparency) subsequent to the last received flag character. If the DEC MODE bit is set, this register must be loaded with the expected SYNC character. This register is used by the receiver logic only. Bit 00 is the least significant and bit 07 is the most significant. These bits are program write and are cleared by INIT or device reset.

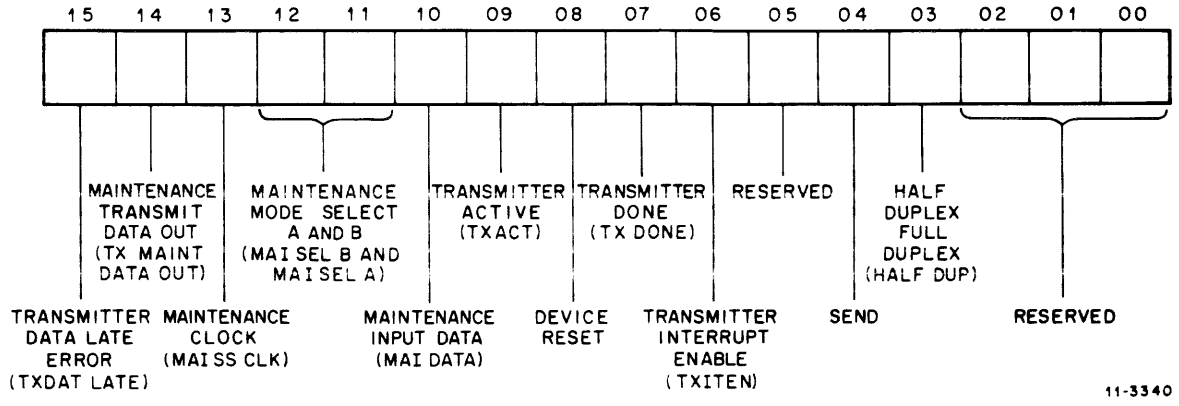

Figure 3-5 Transmitter Control and Status Register Format

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Refer to Figure 3-5)

Bit	Name	Description
15	TXDAT LATE (Transmitter Data Late Error)	This bit is set by the transmitter logic when the program response time to the transmitter Done bit is longer than the specified time frame. When this bit is set and the SDLC or ADCCP mode is selected, the transmitter idles abort characters until either a new message is started or the Send bit is cleared. In DDCMP mode, the line is held in the mark state until a new message is initiated. The program must respond to the TXDONE bit by loading the TXDBUF within the following time frame: (1/bps) 8 + N (bit time) N = number of zeros inserted to maintain transparency, SDLC or ADCCP mode only. This bit is program read and is cleared by INIT, device reset, or by setting the TSOM bit.
14	TX MAINT DATA OUT (Maintenance Transmit Data Out)	The function of this bit is to provide a monitoring point of serial output data of the transmitter for the diagnostic program when using the internal maintenance mode. This bit is program read during internal maintenance mode only and is cleared by INIT or device reset.
13	MAI SS CLK (Maintenance Clock)	This bit is used to simulate the transmitter and receiver clock for diagnostic purposes only. Using it in the internal maintenance mode, the diagnostic has the ability to single-step the interface with respect to the handling of data. A 0-to-1 transition of this bit causes the transmitter to transfer one bit of information to the serial line. A 1-to-0 transition of this bit causes the receiver to shift the contents of the receiver shift register and sample the serial input line. This bit must be cleared during the user mode. This bit is program read/write and is cleared by INIT or device reset.

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Cont)
(Refer to Figure 3-5)

Bit	Name	Description
12, 11	MAI SELB and MAI SELA (Maintenance Mode Select B and A)	These two bits are used together to select the maintenance mode of the interface. **Bit 12 (Select B)** **Bit 11 (Select A)** 0 0 User mode 0 1 External maintenance mode 1 0 Internal maintenance mode 1 1 System test mode 1 = bit set 0 = bit cleared The user mode is the normal operating mode with all level conversion enabled. The modem is expected to provide all necessary clock signals with a 50/50 duty cycle in accordance with the RS334 standard. The maximum rate is 10 kHz. External maintenance mode provides complete checking of all interface components including level converts and cables. The clocking for this mode is provided by a free-running clock contained within the interface at a 10 kHz ± 20% rate asynchronous to the program. This mode can be used in some circumstances to verify the operation of system's software. When this mode is utilized, the device is disconnected at the modem and a maintenance turn-around connector (H325) is used in place of the modem at the end of the cable. The internal maintenance mode provides a means of analyzing 90 percent of the interface without disconnecting the modem. The interface to the modem cannot be diagnosed when this mode is used (i.e., level converts and cables). Fault isolation is greatly enhanced by this mode since the diagnostic program supplies the data set clocking via the maintenance clock bit. Data being transmitted can be monitored on a bit-by-bit basis at the Maintenance Transmit Data Out bit. The The receiver input can be simulated by either the output of the transmitter or by the Maintenance Input Data bit.

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Cont)
(Refer to Figure 3-5)

Bit	Name	Description
		The system's test mode provides asynchronous bus interaction between this device and other devices on the UNIBUS. Data set clocking is simulated by a free-running clock contained on the module at 5 kHz ± 20%. This clocking is asynchronous to the operation of the program. When this mode is used, the device may remain connected to the modem. Receiver and transmitter clocking and data level conversion are inhibited. Modem control signals are not inhibited from being received or transmitted. Transmitted data is internally looped from the transmitter output to the input of the receiver. It is assumed that system test programs will utilize this mode. This bit is program read/write and is cleared by INIT or device reset.
10	MAI DATA (Maintenance Input Data)	When the internal maintenance mode is used, this bit can be used as the receiver serial input. When this bit is set and the maintenance clock bit makes a 1-to-0 transition, a logical 1 is transferred into the receiver shift register. This bit is program read/write and is cleared by INIT or device reset.
9	TXACT (Transmitter Active)	The function of this bit is to indicate the current state of the DUP11 transmitter logic. When the transmitter has been previously in the idle state, (i.e., SEND cleared) and a new message is initiated, this bit is set after a one-half bit time delay, subsequent to the presentation of the first bit to the serial line. When this bit is clear, the transmitter logic is in the idle state and the serial line is held in the mark state. The idle state can be entered by clearing the SEND bit in this same register. The idle state is entered synchronously with the data stream and is also dependent on the DEC MODE, CRC INHIBIT, and TEOM bits. Once the idle state is entered, all transmitter timing and internal control logic is reset.

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Cont)
(Refer to Figure 3-5)

Bit	Name	Description
		If the SEND bit is cleared and the TEOM bit is not asserted, the character currently being transmitted from the transmitter shift register is completed and the line goes to the mark state. The TXDONE bit is not asserted by the completion of this character. After a one-half bit time delay, the TXACT bit is cleared by the DUP11 hardware. This off transition of TXACT causes the TXDONE bit to be set. The following description assumes that the SEND bit is being cleared within the same character frame as the assertion of TEOM. In the SDLC mode, the transmitter sequence consists of the CRC character (if enabled) and a terminating flag. In the DDCMP mode, the CRC character (if enabled) is transmitted. If these conditions are met, the TXACT bit is cleared 1-1/2 bit times after the last character of the sequence. This transition of the TXACT bit causes TXDONE bit to be set, not the completion of individual characters during the sequence. If DEC MODE is selected and CRC is not inhibited, the character currently being serialized is completed and followed by the automatic transmission of the CRC check character. In this case, the CRC check character is considered the last character of the sequence. If CRC is inhibited, the character currently being serialized is the last character of the sequence. When the DEC MODE bit is cleared and CRC is not inhibited, the character currently being serialized is completed. The CRC check character follows this character. Subsequent to the check character, one terminating flag character is transmitted. This flag character is considered the last character of this sequence. If the CRC INHIBIT bit is asserted, the CRC check character is omitted and the flag character is transmitted subsequent to the character being serialized. The flag character is the last character of this sequence. The one-half bit time delay involved with the assertion of TXDONE in this case is useful in the manipulation of the Clear to Send line. At this time, the Request to Send line can be cleared on most modems without losing the last characer. If the transmitter is left enable (SEND is asserted) and TEOM is also left asserted following the transmission of a sequence, continuous flag characters are transmitted until SEND or TEOM is cleared. The current character being transmitted is completed. This bit is program read and is cleared by INIT or device reset.

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Cont)
(Refer to Figure 3-5)

Bit	Name	Description
8	DEVICE RESET	Device reset and the Unibus Initialize signal perform identical functions with respect to the DUP11. When this bit is set, all components of the interface are initialized unless the optional clear jumper is removed. When this jumper is removed, the modem control signals emanating from the device (SEC XMIT, ATS, and DTR) are not affected. This bit is a 1 μs one-shot and self clears. With the optional clear jumper W3 installed, all bits in the interface are cleared with the exception of the transmitter Done bit. Program access should not be made while this bit is set. Both configurations of this jumper are supported by diagnostics. This bit is program write and is cleared by INIT or device reset.
7	TXDONE (Transmitter Done)	This bit is set when the transmitter data buffer is available for a new character. This occurs either as a result of an INIT, device reset, or when a character is transferred from the TXDBUF into the transmit shift register. If the transmitter is entering the idle state, (i.e., SEND is cleared during the current message), the off transition of the TXACT bit causes TXDONE to assert, not the completion of the current character. The TXDONE bit also is set whenever a SYNC, FLAG, or ABORT character has completed transmission, providing the SEND bit is asserted. The TX DATA LATE bit will not assert if a FLAG or ABORT sequence is being transmitted. The transitions of TXDONE can be used to count the number of fill characters transmitted. If this is done, the TXDONE bit can be cleared by reloading the TXDBUF with either TSOM if FLAGS or SYNCS are being used as fill, or TXABORT, if ABORT characters are used. For timing information related to the TXDONE bit and its relationship to the data stream and control bits, refer to the print set. The program must respond to the assertion of this bit within the previously cited time span in order to avoid data under run errors. If the Transmitter Interrupt Enable bit is set, the setting of this bit creates an interrupt request. This bit is program read. It is cleared by writing into the TXDBUF and is set by INIT, device reset, or clearing TXACT.

Table 3-5 Bit Descriptions for Transmitter Control and Status Register (TXCSR) (Cont)
(Refer to Figure 3-5)

Bit	Name	Description
6	TXITEN (Transmitter Interrupt Enable)	When set, this bit allows a program interrupt request to be generated by the TXDONE bit. All interrupt requests should be serviced at a processor level equal to or greater than the device's Bus Request level which is shipped at level 5. This bit is program read/write and is cleared by INIT or device reset.
5		Reserved.
4	SEND	This bit is used to enable the transmitter logic. Once enabled, the transmitter starts transmission of a message when the TSOM bit is detected in the TXDBUF. This bit should remain set until the TEOM bit is loaded into the TXDBUF. IF this bit is cleared at any other time, the current character is finished and the transmitter output goes to a mark hold state. If SEND is cleared while TEOM is still asserted, the current character being transmitted is completed. Following this character, and depending on the protocol being used, any necessary CRC and/or control characters are transmitted. For further information, refer to the TXACT bit in this same register. This bit is program read/write and is cleared by INIT or device reset.
3	HALF DUP (Half Duplex/Full Duplex)	When this bit is set, operation is in half-duplex mode. In half-duplex mode, the receiver is disabled if the SEND bit in the TXCSR is asserted. This bit is read/write and is cleared by INIT or device reset.
2, 1, 0		Reserved.

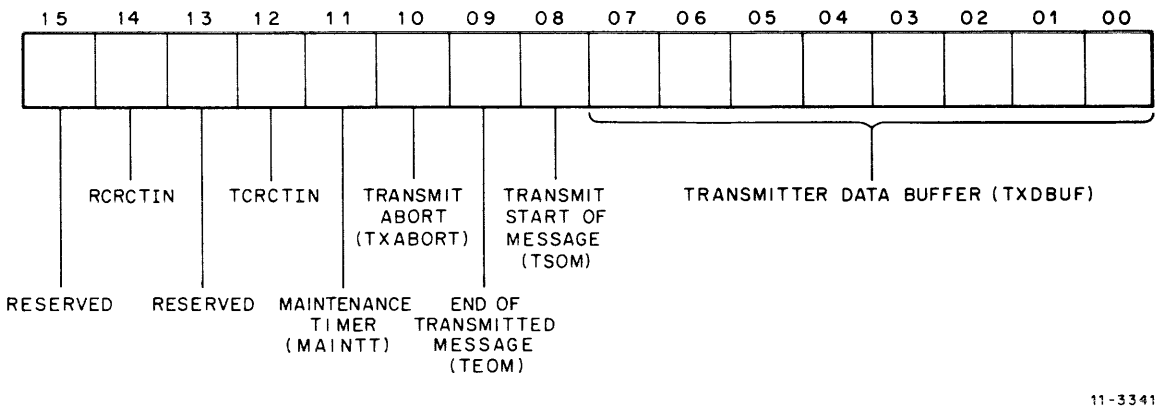

Figure 3-6 Transmitter Data Buffer Register Format

Table 3-6 Bit Descriptions for Transmitter Data Buffer Register (TXDBUF) (Refer to Figure 3-6)

Bit	Name	Description
15		Reserved.
14	RCRCTIN	This bit is provided for maintenance purposes only and is enabled only in internal maintenance mode. The function of this bit is to provide a higher degree of error isolation when diagnosing the receiver CRC register. RCRCTIN is the input to the least significant bit of the receiver CRC register. Refer to Note 1, below, for further information. This bit is program read during the internal maintenance mode only.
13		Reserved.
12	TCRCTIN	This bit is provided for maintenance purposes only and is enabled only in internal maintenance mode. The function of this bit is to provide a higher degree of error isolation when diagnosing the transmitter CRC register. TCRCTIN is the input to the least significant bit of the transmitter CRC register. Refer to Note 1, below, for further information.

Table 3-6 Bit Descriptions for Transmitter Data Buffer Register (TXDBUF)
(Refer to Figure 3-6)

Bit	Name	Description
		These bits are program read during the internal maintenance mode only. **NOTE 1** **The true state of these bits is dependent on the protocol being tested.** The RCRCTIN and TCRCTIN bits are XORed inputs to the respective CRC shift register. Data from either the transmitter or receiver data shift registers is presented as a logical 1 being the high state to the XOR gate. The state of data presented to the XOR gate from the most significant bit of either CRC shift register depends on the state of the DEC MODE bit. When DEC MODE is set, a logical 1 output from bit 15 of the respective CRC register is defined as being high. A logical 0 is defined as being low. When DEC MODE is cleared, a logical 1 output from bit 15 of the respective CRC register is defined as being low. A logical 0 is defined as being high.
11	MAINTT (Maintenance Timer)	The function of this bit is to provide a known timing reference for diagnostic programming purposes only. This bit is enabled only in the external or system's test modes. A transition of this bit occurs every 100 μs. The frequency of this clock is 5 kc ± 20%. This bit is program read in external or system's test mode. It is cleared by INIT or device reset.
10	TXABORT (Transmit Abort)	When this bit is asserted, an Abort sequence is transmitted subsequent to the serialization of the current character, if a character is in process. The SEND bit should be asserted when the Abort sequence is to be transmitted. The TXDONE bit is set at the end of end of each abort character. An abort character is defined as being more than seven contiguous 1 bits. This bit is program read/write and is cleared by INIT and device reset.

Table 3-6 Bit Descriptions for Transmitter Data Buffer Register (TXDBUF) (Cont)
(Refer to Figure 3-6)

Bit	Name	Description
9	TEOM (End of Transmitted Message)	The function of this bit is to terminate the message in progress. How the message is terminated is dependent on the transmitter's mode of operation, as controlled by the information contained in the PARCSR and the state of the SEND bit. If the transmitter is to enter the idle state after the completion of the current sequence, the TEOM bit is set and SEND is cleared by the Program. Refer to the description of the TXACT bit. Termination of a message in DDCMP or BISYNC mode (DEC MODE set) should always cause the transmitter to enter the idle state. Termination of a message in SDLC or ADCCP mode can be achieved in one of two ways. Upon completion, the idle state is entered, or flag characters are idled at completion of the message until the next message is initiated. If upon completion of a message sequence, flags are to be idled, the SEND and TEOM bits should remain set. Flag characters are transmitted until a new message is initiated by clearing the TEOM bit and loading the data. The recommended procedure is to load the new data and clear TEOM in the same operation that accesses the TXDBUF. The contents of the TCRC register always contains all 0s or all 1s after transfer of the CRC character. This bit is program read/write and is cleared by INIT or device reset.
8	TSOM (Transmit Start of Message)	The function of this bit is to initiate the start of a new message if the transmitter is in the Idle state (TXACT = 0). The assertion of this bit causes the internal transmitter CRC register to be re-initialized. The re-initialization of the CRC register and the transfer of the first bit of information occurs within two bit times of the assertion of this bit. If the DEC MODE bit is asserted, the procedure for initiating the start of the message requires that the SYNC character be loaded into the TXDBUF along with the TSOM bit. The character loaded into the buffer is transmitted as the SYNC character until the TSOM bit is cleared. This character is not included as part of the CRC computation. When the TSOM bit is cleared, the SYNC character currently being serialized is finished and is followed by data. All data characters are included in the character computation.

Table 3-6 Bit Descriptions for Transmitter Data Buffer Register (TXDBUF) (Cont)
(Refer to Figure 3-6)

Bit	Name	Description
		If the DEC MODE bit is cleared, the setting of this bit causes the initiation of a message using the SDLC or ADCCP protocols. A flag character is automatically transmitted as long as this bit remains asserted. When data is to be transferred, this bit is cleared by the program and the data is loaded into the TXDBUF. At the completion of the current flag character, the actual transmission of data begins. This bit should not be set when another message is actively being transmitted. Setting this bit also causes the TXDAT LATE bit to be cleared. The TXDONE bit is asserted at the completion of each flag or SYNC character when this bit is asserted. This bit is program read/write and is cleared by INIT or device reset.
7–0	TXDBUF (Transmitter Data Buffer)	This register is loaded with the information to be transmitted. All data is treated as eight bit characters. If the DEC MODE bit is set, the SYNC character to be transmitted must be loaded into this register prior to initiating the synchronization process. The least significant bit of this register is bit 00. Bit 07 is the most significant. These bits are program read/write and are cleared by INIT or device reset.

3.6 MAJOR OPERATING FEATURES

3.6.1 Introduction

This paragraph discusses the major operating features of the DUP11 at the functional level. The discussion is divided into three sections as shown below.

Title	Par. No.
Modem Control	3.6.2
Transmitter Section	3.6.3
Receiver Section	3.6.4

This discussion assumes that the DUP11 is operating in the user mode. The maintenance modes, which are used to service the DUP11, are described in Chapter 5 of the Technical Manual.

3.6.2 Modem Control

The modem control and status lines are monitored along with a flag to indicate a change in any line's state since the last time it was monitored by the program. Using these indicators, the program must determine when it can transmit data. Once this has been established, the transmitter is enabled and transmission begins when the first character is loaded into the data buffer.

In some systems, this handshaking is not necessary. The transmitter is simply enabled and transmission starts when the program sets the TSOM bit in the transmit data buffer register (TXDBUF). The receiver may start searching for synchronization without first having been rung.

The flow of data is not interlocked with signals received from the modem. When modem control is being used in a system, the program must monitor the received modem control signals contained in the RXCSR register.

The secondary receive and transmit leads are also included in the modem control section. While these leads have no function in the Bell 201, 208, and 209 modems, they can be redefined for other user purposes at installation time.

All clock signals used in conjunction with data received from or transmitted to the modem must emanate from the modem and be in accordance with EIA RS 334 at a rate $\leqslant$ 10 kHz. No external clock to the modem is supplied by this interface. Maintenance mode clocking used to facilitate checkout and diagnostic engineering is provided. This clocking is under program control and is intended to be used only when the DUP11 is being serviced.

3.6.3 Transmitter Section

The transmitter section provides the following functions.

1. Buffers and serializes parallel data.
2. Generates CRC check characters.
3. Creates transparent data stream for SDLC and ADCCP protocols.
4. Transmits flag and abort sequences and leading zero sequences.

The transmitter section is enabled when the program asserts the SEND bit in the TXCSR transmitter control and status register (TXCSR). The actual state of the transmitter logic is indicated by the TXACT bit in this register.

A character or control bit may be loaded into the TXDBUF whenever the TXDONE bit is asserted. This occurs after an initialize pulse, device reset by the program, or when the logic completes transmission of a character. This bit is cleared when a character is loaded into the TXDBUF.

TRANSMIT OPERATION UNDER SDLC FAMILY PROTOCOL DISCIPLINE

Assuming that the transmitter section is in the idle state (TXACT = 0) and is enabled by the SEND bit, transmission of a message sequence begins when the TSOM bit in the TXDBUF is detected. Upon detecting this bit, the transmitter automatically transmits the initial flag character.

When starting from the idle state, the first bit of the flag character is delayed for a period equal to two bit times. The TXDONE and TXACT bits are asserted when this first bit is transferred to the serial line. At this point, the first data character may be loaded into the TXDBUF. If the TSOM bit is still asserted at the completion of the flag character currently in progress, then another flag character is transmitted. Flags are sent until TSOM is cleared.

The transmitter goes into the transparent state immediately following the transmission of the last initial flag characters and also begins the accumulation of the CRC check character, providing that the CRC inhibit bit is cleared in the PARCSR. When the transmitter is in the transparent state, the logic automatically inserts a 0 following five consecutive ones, to preserve the properties of the flag and abort characters.

Termination of a message is accomplished by asserting the TEOM bit in the TXDBUF. The character currently being serialized in the transmitter shift register is completed. If CRC is not inhibited, the computed CRC check character is automatically transmitted and followed by a terminating flag character. If CRC is inhibited, the terminating flag character follows the character currently being serialized. The TEOM bit must remain asserted until transmission of the terminating flag character starts. If the SEND bit is asserted when TEOM is asserted, the start of the transmission of the flag is identified by the next transition of TXDONE. These events occur simultaneously.

At this point, the program has three options.

1. Clear SEND which allows the flag character currently being transmitted to be finished. At the end of the flag, there is a delay of one and one half bit times after which the transmitter enters the idle state.

2. Leave TEOM asserted, which allows continuous flag characters to be transmitted until option 1 or 3 is executed. In this option, Data Late errors do not occur. The number of flag characters sent can be determined by counting the transitions (set state) of TXDONE. This bit is set when the TXDBUF register is loaded. In this case, the program should keep TEOM set.

3. Initiate another data transfer by clearing TEOM and loading the data byte into the TXDBUF register. If TEOM is cleared during transmission of the first terminating flag, then only one flag separates the SDLC frames. If TXACT is asserted, it is not necessary to set TSOM to start a subsequent message. The recommended procedure is to load the new data and clear TEOM in the same operation that accesses the TXDBUF. The TSOM bit should be used to initiate a message only when TXACT is cleared.

If the SEND bit is cleared between the time that the TEOM bit is asserted and the transmission of the terminating flag has started, then the transition of TXDONE is deferred until the transmitter returns to the idle state.

This delay of half a bit time in most cases ensures the integrity of the last character before attempting to turn the line around in half-duplex situations; however, this is modem dependent and each modem manual should be referenced for applicability.

If SEND is cleared and no transmitter control bits are set, the current character is transmitted and the transmitter is shut down after a 1 1/2 bit delay.

In some instances it may be necessary, because of system or timing restriction, to transmit a given number of ABORT characters subsequent to the last flag characters. This can be accomplished by asserting the TXABORT bit at the appropriate time. The SEND bit must remain asserted for this operation.

The TXABORT bit can be asserted when the last required flag character has begun transmission. The earliest possible time that the TXABORT bit can be asserted (for this purpose) is immediately after the second assertion of the TXDONE bit subsequent to the setting of the TEOM bit.

The first assertion of the TXDONE bit subsequent to the setting of the TEOM bit occurs when the serialization of CRC check information begins. It is necessary to clear the TXDONE bit before the end of the transmission of the CRC character so that the second transition of the TXDONE bit can occur. This transition marks the start of the transmission of the terminating flag character. This second transition can be created by again setting the TEOM bit. The TXABORT bit can be set when the TXDONE bit asserts marking the beginning of the terminating flag character.

TRANSMIT OPERATION UNDER DDCMP OR BISYNC PROTOCOL DISCIPLINE

Assuming that the transmitter is enabled by the SEND bit in the TXCSR, transmission starts when the TSOM bit is set in the TXDBUF by the program. When the TSOM bit is asserted, the SYNC character being used must be present in the lower byte of the TXDBUF. All transmitted SYNC characters must be loaded into the TXDBUF. The TSOM bit must remain asserted until the start of the last SYNC character. The TXDONE bit is asserted at the completion of each SYNC character. When it is necessary to count the number of transmitted SYNC characters, the TXDONE bit can be cleared by again setting the TSOM bit. This allows the next transition of TXDONE at the end of the character.

When the last SYNC character is transmitted, the TSOM bit is cleared and the first character of data is entered into the TXDBUF. This character and all subsequent data characters are included in the transmitter's CRC computation.

For protocols such as BISYNC, the CRC feature of this device must usually be inhibited. Protocols such as DDCMP can make efficient use of the CRC logic. These protocols are characterized by the fact that no special control characters are embedded within the message that are not included as part of the CRC computation.

The accumulated CRC check character is transmitted subsequent to the assertion of the TEOM bit. When the character currently being transmitted is complete, the CRC check character is sent next, if the TEOM bit is asserted. The TXDONE bit is asserted at the start of the CRC character transmission. This can be ignored or cleared by again setting the TEOM bit.

The DUP11 does not provide the feature of automatically idling SYNC characters without program intervention.

Data must be presented to the TXDBUF as 8-bit characters. The message length is not restricted.

TRANSMITTER CRC CHARACTER GENERATION

To enable the CRC logic, the program must clear NO CRC (PARCSR bit 9). Two cyclic redundancy checking (CRC) codes are used. The SDLC family protocols use code CCITT which is represented by polynomial $X^{16} + X^{12} + X^5 + 1$. The DDCMP family protocols use code CRC-16 which is represented by polynomial $X^{16} + X^{15} + X^2 + 1$. With CRC enabled, the accumulated CRC check character is a result of all data loaded by the program into the TXDBUF. With the SDLC and ADCCP protocols, 0s that are inserted into the message to maintain transparency are not included as part of the calculation.

The transmitter CRC register is initialized (cleared) when TSOM is asserted, which is internally synchronized. When initialized, the register reads all 0s in the DDCMP mode and all 1s in the SDLC mode. Initializing the register to all 1s provides protection against obliterating leading zeros which may not be detected if the register is zero. In the DDCMP mode, the CRC check character is transmitted as is. In the SDLC mode, it is complemented before it is transmitted.

TRANSMITTER LATENCY

The specifications of the SDLC, ADCCP, and DDCMP protocols require that the flow of data be contiguous; that is, no intramessage fill characters are allowed.

Since the DUP11 is double buffered, one character time (and in some cases more) is allowed before data late errors are encountered. The data late condition is indicated whenever the TXDBUF is not serviced within the appropriate response time before assertion of the TXDONE bit.

This time can be expressed as follows:

(1/baud rate) 8 + n (secs)

n = number of inserted zeros.
(Applicable only for SDLC family protocols)

$n \leqslant 2$

When the current character has been transmitted, the absence of valid data in the TXDBUF causes the TXDAT LATE bit to be asserted in the TXCSR, unless the TEOM bit was asserted in the TXDBUF. This indication suggests retransmission of the message. When this occurs, the transmitter automatically transmits abort characters in the SDLC or ADCCP modes until a new message is presented to the transmitter, providing the SEND bit is asserted. In the DDCMP or BISYNC modes the line is held in the mark hold state. Assertion of the TSOM bit clears the TXDAT LATE bit.

3.6.4 Receiver Section

The receiver section provides the following functions.

1. Buffers and converts received serial data to parallel data.
2. Interprets transparent data stream in SDLC or ADCCP protocols.
3. Recognizes flag and abort sequences.
4. Recognizes secondary station addresses (SDLC mode) and SYNC characters (DDCMP mode).
5. Detects CRC errors.

The receiver section is capable of operating as either a secondary or primary station when the SDLC and ADCCP protocols are selected. This is controlled by the state of SEC MODE bit in the PARCSR. When operating as a primary station, all received messages are presented to the program. In the secondary mode, only messages that are prefixed with a secondary station address that matches the contents of the low byte of the PARCSR are presented to the program.

If the DDCMP or BISYNC mode of operation is selected, the low byte of the PARCSR must be loaded with the SYNC character being used by the system. All data received is handled as eight bit characters.

The receiver logic is controlled by the RCVEN bit in RXCSR. The state of the receiver is indicated by the RXACT bit in the same register.

RECEIVE OPERATION UNDER SDLC FAMILY PROTOCOL DISCIPLINE

Once the initialization and any necessary modem handshaking have been completed, the RCVEN bit can be set. When the RCVEN bit is asserted, the receive logic searches for initial flag character. When operating in the primary mode, all data received subsequent to the last initial flag character is presented to the program. The first character is accompanied by the RSOM in the RXDBUF. When operating in the secondary mode, the character subsequent to the last flag character is compared to the contents of the low byte of the PARCSR (any bits inserted for transparency are stripped prior to performing the

compare). If the comparison is not true, then the search for a flag is reiterated. When this comparison is true, the RXACT bit is asserted in the RXCSR. The RSOM bit in the RXDBUF is set to indicate the beginning of a new message. The received address character is not presented to the program. The character subsequent to it is the first character to be presented to the program along with the RSOM bit. When this character is transferred to the receiver data buffer, the RSDONE bit is also asserted. Any character subsequent to this causes the RXDONE bit to be asserted with the receiver interrupt enable bit asserted; the assertion of the RXDONE bit creates an interrupt request. When the program accesses the RXDBUF, the RXDONE bit is cleared.

When the terminating flag character is received, the REOM bit is asserted in the RXDBUF and the RXDONE bit is asserted in the RXCSR. The low order byte of the RXDBUF is invalid when the REOM bit is set.

If CRC checking is not inhibited, an error would be indicated only when the REOM bit is asserted. The check is performed on all data received beginning with the secondary station address up until the first check character is received. When CRC checking is implemented, the last two bytes of information received by the program are the CRC check characters.

Messages in progress can be aborted if the sending station transmits an ABORT sequence. When the receiver detects the ABORT sequence, the RABORT bit in the RXDBUF is set along with the RXDONE bit in the RXCSR. The receiver logic detects one ABORT sequence after receiving an initial or final flag character.

All data received is handled and presented to the program in eight bit characters.

Transparency is maintained at the receiver by searching the data stream for zeros inserted by the transmitter and removing them.

RECEIVE OPERATION UNDER DDCMP OR BISYNC PROTOCOL DISCIPLINE

The DDCMP and BISYNC family of protocols are also handled by this device. In most BISYNC applications, the software overhead is increased. This occurs because of the extra amount of character recognition or processing of message header information required. Also, in some cases, the CRC feature of the DUP11 may have to be inhibited because of control characters embedded within the data stream.

The low byte of the PARCSR must be loaded with the SYNC character being utilized by the system before the receiver is enabled. This character is loaded into the PARCSR and is used only by the receiver logic for comparison with data being received. This register is not used by the transmitter logic.

Once the initialization and any necessary modem handshaking have taken place, the program may assert the RCVEN bit. With the RCVEN bit asserted, the first operation of the receiver logic is to search the data stream for two consecutive SYNC characters. When two consecutive SYNCs have been recognized, the receiver logic is considered synchronized and any subsequent information is assembled as eight bit characters. When an eight bit character is assembled, it is transferred into the RXDBUF and RXDONE bit is asserted conditional on the character being received, and the state of the STRIP SYNC bit and RXACT bit. If the program has asserted the STRIP SYNC bit, the character received matches the contents of the PARCSR low byte, and the RXACT bit has not been set by the logic, the RXDONE bit is not asserted.

When the logic has located the first non-SYNC characters, the RXACT bit is asserted by the logic. This character and all subsequent characters are included in the receiver's CRC computation. At this point, the function of the STRIP SYNC bit is internally disabled.

The RCVEN bit in the RXCSR should be left asserted for the entire message, and cleared at the end of the message. Clearing this bit reinitializes the receiver logic.

RECEIVER CRC CHARACTER CHECKING

CRC error detection is performed by the receiver logic if the NO CRC bit is cleared. The method of detecting errors and the polynomial used vary according to the mode of operation as controlled by the DEC MODE bit in the PARCSR.

If the DEC MODE bit is cleared, then the CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) is used and the logic operates in a manner compatible with the SDLC and ADCCP protocols. The receiver CRC error detection logic is effectively set to all ones when the RXACT bit is cleared.

The contents of the receiver CRC register are tested when a terminating flag is received in SDCL or ADCCP mode. The register is tested for the following bit pattern: LSB 1 111 000 010 111 000 MSB. The absence of this bit pattern causes assertion of the RCRC ERR + ZERO bit in the RXDBUF. The REOM bit is also asserted at this time. This bit pattern is the result of all data received between the last initial flag character and the terminating flag, excluding intermessage flags and zeros inserted for transparency.

The last tow bytes (16 bits) of data presented to the program through the RXDBUF comprise the received CRC check character. The data received in the RXDBUF when the REOM bit is asserted is meaningless and should be disregarded.

DDCMP compatible operation is enabled by asserting the DEC MODE bit. In this mode the CRC 16 ($X^{16} + X^{15} + X^2 + 1$) polynomial is used to generate the receiver check character. The receiver CRC register is initialized to all zeros when the RXACT bit is cleared.

Once the receiver has been synchronized, the data received and presented to the program is included in the computation of the check character. This occurs when the RXACT bit is asserted. Characters received during the reception of a message (after RXACT is asserted) are including in the CRC computation even if they match the contents of the PARCSR. The function of STRIP SYNC is internally disabled when RXACT is asserted.

The RCRC ERR + ZERO bit is asserted in this mode when, during the reception of a message, the CRC register is equal to zero coincidental with the end of the current character.

The program should only test the RCRC ERR + ZERO bit when the expected number of bytes including CRC information have been received. It is entirely possible that during the reception of a message, this bit may be asserted without having received the actual CRC check character. Normally the RCRC ERR + ZERO bit is presented to the program along with the second CRC check character.

RECEIVER LATENCY

The program must respond to the RXDONE bit within a specified time frame in order to avoid overrun errors.

If the program has not read the contents of the RXDBUF within this time frame, the OVRUN FRR bit in the RXDBUF is set. The contents of the data buffer contain the last received character. This error suggests retransmission of the message.

Because this device is double buffered, the time lag in which the program must respond is as long as a full character time and can be expressed as the following.

(1/baud rate) 8 + n (secs.)

n = number of inserted zeros. $n \leq 2$

(SDLC family protocols only)

INTERRUPT REQUESTS

In the RXCSR, there are two interrupt request enable bits; in the TXCSR, there is one. These bits can be used to selectively allow interrupt requests that occur asynchronous to the operation of the program.

The Data Set Interrupt Enable bit (DSCITEN) allows interrupt requests to be generated on the receiver interrupt vector if the DATA SET CHANGE A bit is asserted. The Receiver Interrupt Enable bit (RXITEN) also allows interrupts to be generated on this same vector if the RXDONE bit is asserted. If both interrupt conditions exist simultaneously on the receiver vector, then the interrupt requests occur back to back and there is no fixed scheme in which the requests should be serviced.

There is only one interrupt request made on the transmitter interrupt vector. This request is made if the Transmitter Interrupt Enable bit (TXITEN) is set and the logic asserts the TXDONE bit.

All interrupt requests should be serviced at a processor status level equal to or above that of the device interrupt priority level. If simultaneous interrupt requests are generated on both the receiver and transmitter vectors, the receiver request is honored first.

HALF-DUPLEX OPERATION

The program can select half-duplex operation. This can be done by asserting the HALF DUPLEX bit in the TXCSR.

In this mode of operation, the receiver logic does not transfer data. It is completely disabled, if the SEND bit is asserted in the TXCSR. All other characteristics of the interface are maintained.

APPENDIX A
PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized in 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location: low bytes are even-numbered and high bytes are odd-numbered. Words are addressed at even-numbered locations only and the high (odd) byte of the word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even-numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00). Eighteen bits provide the capability of addressing 256K memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multipler K equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. The maximum memory size can be used only by a PDP-11 processor with a memory management unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 2^{18} or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the processor uses as shown below.

The highest 8K address locations (760000–77777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248 bytes or 124K words to program.

A PDP-11 processor without the memory management unit provides 16 address bits that specify 2^{16} or 65,536 (64K) locations (Figure A-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s when the processor is master to allow generation of addresses in the reserved area with only 16-bit control.

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Address Bit
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	Binary
1			1			7			6			0			1			Octal

Address Word Format

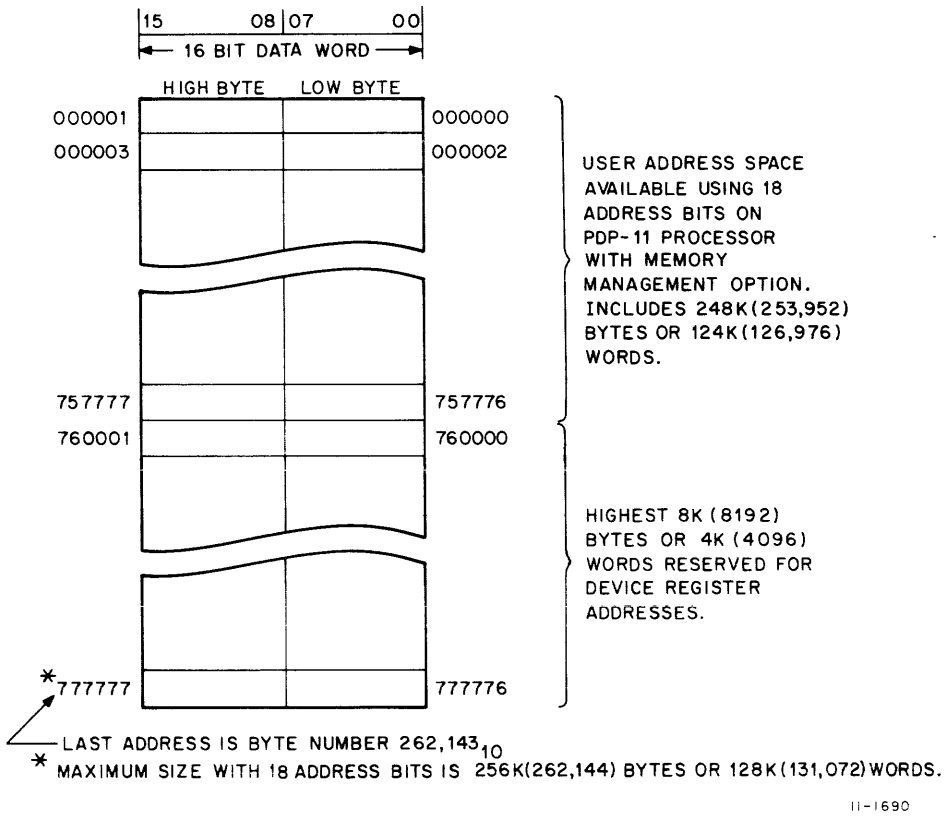

Figure A-1 Memory Organization for Maximum Size Using 18 Address Bits

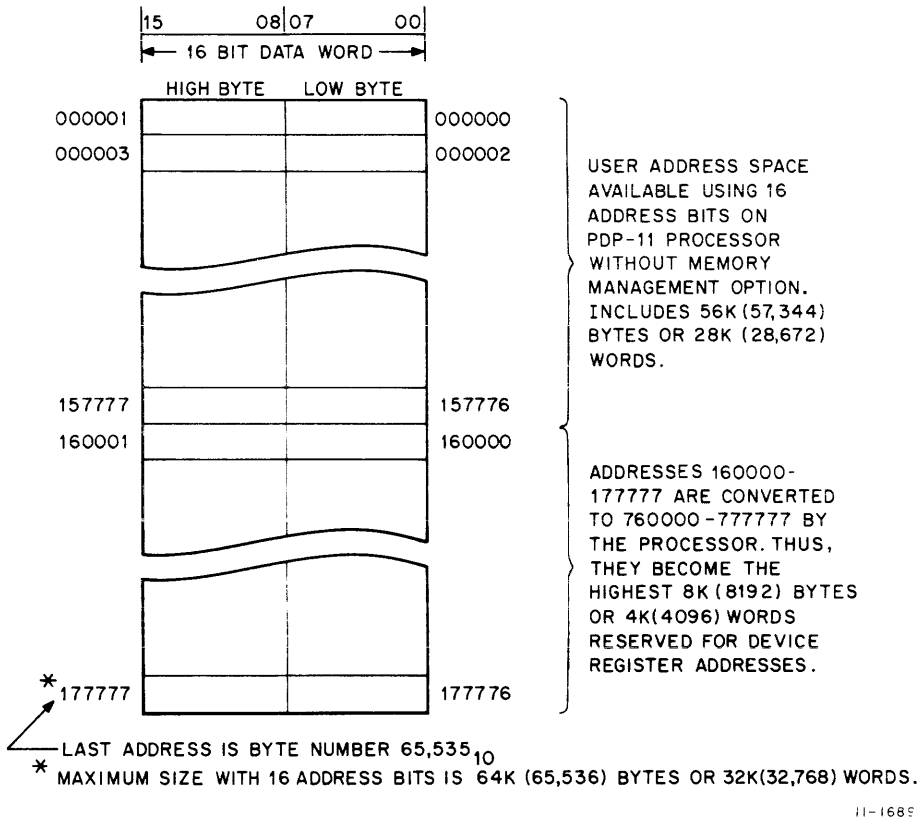

Figure A-2 Memory Organization for Maximum Size Using 16 Address Bits

Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777, which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interfering with the reserved space.

PDP-11 memories are available in a variety of increments. The highest location of various size memories are shown below.

Memory Size		Highest Location
K-Words	**K-Bytes**	**(Octal)**
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

DUP11 Bit Synchronous Interface
User's Manual
EK-DUP11-OP-002
(MK)

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgement is it complete, accurate, well organized, well written, etc? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults or errors have you found in the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____
Title _____ City _____
Company _____ State/Country _____
Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
146 Main St.
Maynard, MA 01754

Attention: Printing and Circulation Services (NR2/M15)
Customer Services Section

Order No. **EK-DUP11-OP-002** _____

Fold Here

Do Not Tear – Fold Here and Staple

digital

No Postage Necessary if Mailed in the United States

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 33 MERRIMACK, NH

POSTAGE WILL BE PAID BY ADDRESSEE

Digital Equipment Corporation
Educational Services/Quality Assurance
12 Crosby Drive, BU/E08
Bedford, MA 01730

Digital Equipment Corporation • Bedford, MA 01730