IDENTIFICATION

Product Code:	MAINDEC-14-D7LA-D-(D)
Product Name:	TEST - 14L
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1. ABSTRACT

TEST-14L is a program written to be run on a PDP-8 I/L computer to thoroughly test a PDP-14L Computer System consisting of a PDP-14L processor, and I-, O-, and S-Boxes. It is loaded into and run on an 8 I/L connected to the PDP-14L under test. The program provides error type outs, error halts and oscilloscope looping. The program can be run for a short period of time (minutes) to initially test a PDP-14L, or it may be run for a long time (approximately 2 hours) to provide a comprehensive test to all the logic circuitry.

2. REQUIREMENTS

2.1 Equipment

PDP-8 I/L Computer
PDP-14L to PDP-8 I/L Interface Module (M745)
PDP-14L Computer
PDP-14L, I-, O-, and S-Boxes with the output of the O Boxes tied back (electrically) to the respective inputs of the I- Boxes.

2.2 Storage

The program occupies most of PDP-8 I/L memory

2.3 Preliminary Programs

None

3. LOADING PROCEDURE

3.1 Method

The program is loaded using the "standard" PDP-8 Binary Loader technique.

4. STARTING PROCEDURE

4.1 Control Switch Settings

The following is a program of switch register settings and their operation upon the program:

SR	Set As	Action
0	1	Loop on Current Test
	0	Don't Loop
1	1	Don't Halt on Error
	0	Halt on Error
2	1	Don't Print Errors
	0	Print Errors
3	1	Long Test
	0	Short Test
4	1	Repeat All Tests
	0	Stop at End of Tests
5	1	Test Memory Logic
	0	Don't Test Memory Logic

4.2 Starting Addresses

Start the program at location 0200 if it is desired to interrogate operator about PDP-14L configuration.

Start the program at location 0201 if the PDP-14L configuration has been previously defined to the program.

4.3 Program and/or Operator Action

4.3.1 Connect the PDP-14L to be tested to the PDP-8I/L using the appropriate cables and revision of the M745 interface module.

4.3.2 Connect to the PDP-14L the I-, O-, and S-Boxes to be used in the test. The I-Box cables must occupy consecutive address slots in the I-Box section of the PDP-14L. The O-Box cables must also occupy consecutive address slots, but in the O-Box section of the PDP-14L. The S-Box cables must occupy consecutive address slots in the O-Box section immediately following the last O-Box cable. Electrically connect the output of the O-Boxes to the respective inputs of the I-Boxes (i.e. 0 to 0, 1 to 1, 2 to 2, etc.) If there are extra

In-Box inputs left over, connect these respectively to outputs 0, 1, 2 etc.(i.e. input 40 to output 0, input 41 to output 1, etc) until all input terminals are connected to a respective output. Return to output Ø as much as necessary to accomplish this. Connect the appropriate supply voltage (normally 110 Volts, 60 Hz) to the O-Boxes.

4.3.3 If the memory logic is to be tested, plug the special test module into the PDP-14L.
(see the Engineering Checkout Procedure)

4.3.4 Power up the PDP-8I/L and the PDP-14L computers.

4.3.5 Load the binary program "TEST-14L" into the 8I/L using the PDP-8 Binary Loader.

4.3.6 Start the program at location 0200. Set Switch register per 4.1 above.

4.3.7 Answer the questions asked by the program, concerning how many I-,O-, and Half - S Boxes are connected to the PDP-14L (1 S-Box = 2 Half S-Boxes) and the presence of a ROM via the PDP-8I/L Teletype Keyboard (See below)

```
HOW MANY I-BOXES?
2
HOW MANY O-BOXES?
4
HOW MANY HALF  S-BOXES?
Ø

IS A ROM INSTALLED (Y-YES N-NO) ?  Y
```

4.3.8 Program will now run to completion (assuming no errors) and will type out "PASS 'N' "COMPLETE" upon completing each pass of the program (See Below).

```
PASS ØØØ1 COMPLETE

PASS ØØØ2 COMPLETE

PASS ØØØ3 COMPLETE
```

5. OPERATING PROCEDURE

5.1 Operational Switch Settings
See 4.1 above.

5.2 Subroutine Abstracts
None

5.3 Program and/or Operator Action

There is normally no communication between the operator and the computer after the initial interrogation except via the Switch Register. The computer will not communicate with the operator except when an error occurs or the computer completes a pass through the program.

6. ERRORS

6.1 Error Halts and Description

Most of the error halts in the program are preceded by error typeouts. However, if in doubt about the cause of the error halt, consult the program listing.

6.2 Error Recovery

To scope an error condition after an error halt, set the switch register per 4.1 (above) and depress "CONTINUE".

After replacing suspected bad modules, always restart the program at location 0201 (it is not necessary to repeat interrogation if the PDP-14L configuration has not changed or the program has not been reloaded).

6.3 Error Messages

The error messages output by the program (with very few exceptions) will contain as error designator (a 2 letter error number) followed by a description of the test being performed and/or description of the failing error condition. If desired, the operator can use the 2 letter error designator to go directly to the module call list to see which modules should be replaced. Or, if he desires, he may set up a program 'scope loop and probe the PDP-14L to determine the failing condition, then replace the failing module.

Examples of the various types of error messages are shown below:

6.3.1 Register Errors

6.3.1.1 Single Register Errors

```
**A!** JMP (4224) TEST
       OLD  GOOD BAD
PC1    0000 0001 0000
```

In the example shown of the previous page, the error designator is "AI". The operator can go to the module call table and look up "AI" or he can analyze the rest of the message. The test being performed involves some of the basic gating of the PDP-14L and the "JMP" instruction. The failing register was PC1 (or possibly the "output register" as it is impossible to tell at this point in the testing scheme).

6.3.1.2 Multiple Register Errors

```
**AL** TRM (4226) TEST
       OLD  GOOD BAD
OUTPUT 0000 0642 0000

PC1    0000 0003 0000
```

It is possible that more than one register can be affected in a test. In the example shown above both the "Output Register" and "PC1" were in error

6.3.2 Non Register Errors

6.3.2.1 I/O Instruction Errors

```
**BZ** TEST FLOP  NOT SET BY TXN 0060
```

The above example indicate a problem in the I/O section of the PDP-14L. The operator can refer to the module call for error "BZ" after reading this message, or he can further analyze the message if he desires to 'scope the error. In this test he would 'scope the "TXN" class of instruction to check pulse generation, addressing, gating, decoding, etc. in the PDP-14L processor and in the I-Box affected.

6.3.2.2 PDP-8 to PDP-14L Interface Errors

```
**DA** EXTERNAL FLAG NOT CLEARED BY POWER CLEAR OR 6161 ALWAYS SKIPS
```

The above example indicates a problem in the PDP-8 to PDP-14L Interface module (M745). 'Scope loops are provided, however it is generally easier to simply replace the M745 module and try again.

6.3.3 Non-Diagnostic Errors

PDP-14 HUNG

PDP-14 STOPPED

Unfortunatly, these are a few errors which the PDP-14L can perform which are not analyzible by the program, although they are detectible. These are shown above. If the PDP-14L stops or hangs, one of the above printouts will occur. Depressing PDP-8 "continue" may provide more information about the error.

6.4 Error Identifier - Module Call

Note: In addition to the modules listed for each error identifier, the following modules are common to all errors

M774 - IR Decoder
M235 - Major Registers
M745 - PDP-8 to PDP-14L Interface

Identifier	Module Type(s) and Function(
AI	M741 Major states and timing
AL	See Note
AO	See Note
AR	See AI
BH	M743 I/O interface K2Ø7 O-Box K135 O-Box K161 O-Box
BI	See BH
BJ	M743 I/O interface K161 I-Box K378 I-Box K135 I-Box

Identifier	Module Type(s) and Function(s)
BK	See BJ
BL	See BH
BM	See BJ
BN	See BH
BO	See AI
BP	See AI
BQ	See BH
BR	See AI
BS	See BH
BT	See AI
BU	See AI
BV	See BJ
BW	See AI
BX	See BH
BY	See BH
BB	X614 O-Box, See BJ
CA	See BB
CB	See BH
CC	See BH
CD	See AI
CE	See Note
DA	See AI

Identifier	Moudle Type (s) and Function(S
DB	See AI
DC	See AI
DE	See AI
DF	See AI
DG	See AI
DH	See AI
DI	See AI
DJ	See AI
DK	See AI

7. RESTRICTIONS

7.1 Starting Restrictions

PDP-14L Power Clear is expected at program start time, don't stop TEST-14L in the middle of the I/O test and restart at Ø2ØØ or Ø2Ø1 without powering down and powering back up the PDP-14L

7.2 Operating Restrictions

All I-, O-, and S-Box cables must occupy consecutive address slots starting with address slot Ø in the respective area of the PDP-14L processor

The special test module must be plugged in to test the memory logic.

8. MISCELLANEOUS

8.1 Execution Time

The execution time of the program is dependent upon the I/O configuration of the PDP-14 under test.

The short test should take no more than five (5) minutes.

The long test should take approximately two (2) hours.

9. PROGRAM DESCRIPTION

9.1 Test 1 (SA=1ØØØ)-

The first test performed checks the operation of the external flag to set and clear and operate on the PDP-8 interrupt bus properly.

9.2 Test 2 (SA=12ØØ) -

Checks the operation of the output register flag to set and clear and operate on the PDP-8 interrupt bus properly.

9.3 Test 9 (SA=32ØØ)

Checks JMP instruction (4224). If SR3=1 (long test) jump from and to all locations. If SR3=0 (short test) jump from 0 to all locations.

9.4 Test 12 (SA=34ØØ)

Checks the instruction TRM (4226)

9.5 Test 15 (SA=36ØØ)

Check the instruction NOP (0000) at all locations

9.6 Test 18 (SA=3666)

Checks the instruction JFF (5000) to jump properly. If SR3=1 (long test) JFF is executed to and from all locations. If SR3=0 (short test) JFF is executed to all locations from all page location 0's.

9.7 Test 34 (SA=5606)

The first test to be performed on the I/O checks that after an "SYF 377" (3377) no outputs are on.

9.8 Test 35 (SA=5644)

Checks that after an "SYF 377" (3377) all outputs are off.

9.9 Test 36 (SA=5677)

Checks that no inputs are on after an "SYF 377"

9.10 Test 37 (SA=5733)

Checks that all inputs are off after an "SYF 377"

9.11 Test 39 (SA=6ØØ2)

Checks a TXD "N" status word with the "TEST" flop set and input off

9.12 Test 40 (SA=6ØØ4)

Checks a TYD "N" status word with the "TEST" flop set and output off

9.13 Test 41 (SA=6ØØ6)

Checks the JFN Y instruction with the "TEST" flop set

9.14 Test 43 (SA=6Ø54)

Checks the JFF Y instructions with the "TEST" flop cleared

9.15 Test 44 (SA=6112)

Check a TXD "N" status word with the "TEST" flop cleared and input off.

9.16 Test 45 (SA=6115)

Checks a TYD "N" status word with the "TEST" flop cleared and output off

9.17 Test 47 (SA=6122)

Checks the JFF Y instruction with the "TEST" flop set

9.18 Test 49 (SA=62ØØ)

Checks the JFN Y instruction with the "TEST" flop cleared

9.19 Test 54 (SA=6237)

Checks that with output "N" on, only TYN "N" sets the "TEST" flop.

9.20 *Test 55 (SA=6314)

Checks a TXD "N" status word with the "TEST" flop set and input on.

9.21 Test 56 (SA=6317)

Checks a TYD "N" status word with the "TEST" flop set and output on.

9.22 Test 57 (SA=6322)

Checks that with output "N" on, all TYF's set the "TEST" flop except TYF "N"

9.23 Test 58 (SA=64ØØ)

Checks a TYD "N" status word with the 'TEST" flop cleared and output on.

9.24 *Test 59 (SA=641Ø)

Checks a TXD "N" status word with the "TEST" flop cleared and input on.

9.25 *Test 60 (SA=6413)

Checks that with output "N" on, only TXN "N" and "offsets" (other inputs connected to output "N") set the "TEST" flop.

9.26 *Test 61 (SA=6476)

Checks that with output "N" on, only TXF "N" and "offsets" do not set the "TEST" flop.

9.27 Test 66 (SA=66ØØ)

Checks that only SYF "N" and SYF 377 clears output "N"

9.28 Test 68 (SA=7000)

Checks that only SYN "N" turns on output "N"

9.29 Test 69 (SA=5517)

Checks the operation of memory circuitry by issuing TRM (4426) using 6165 IOT. The number in the OUTPUT Register should be the same number as was in PC1.

*These tests are not performed when an S-Box is being tested.