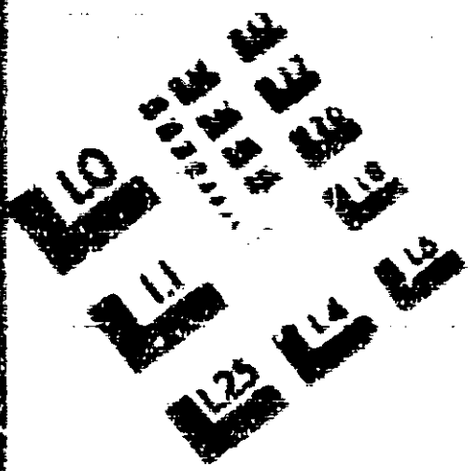


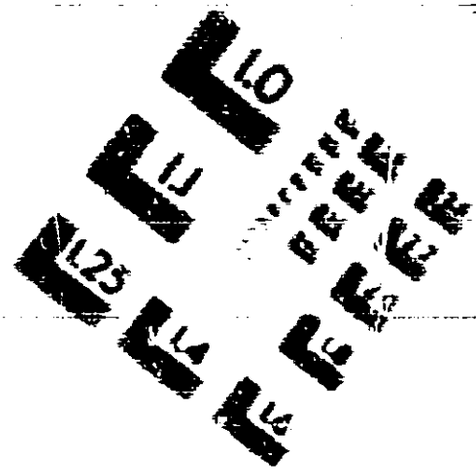
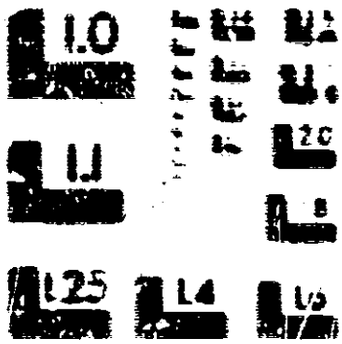
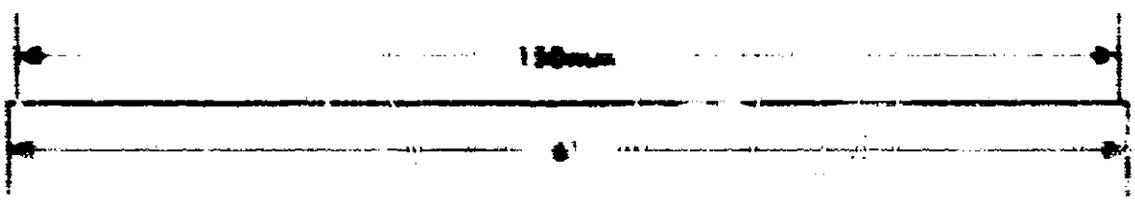
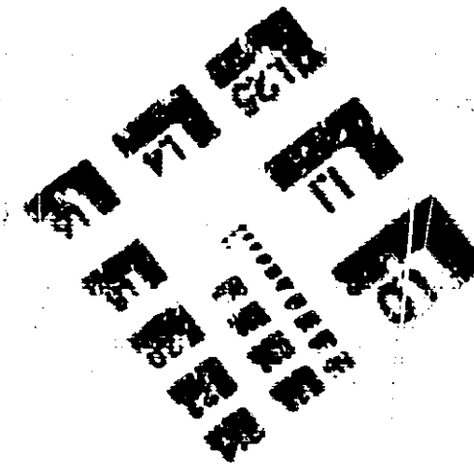


IMAGE EVALUATION
TEST TARGET (MT-2)







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DWBUA

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DWBUA
UNIBUS Adapter
Technical Manual

Prepared by Educational Services
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1st Edition, January 1986

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DECUS	RSTS	VT
		Work Processor

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FIGURES (Cont)

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PREFACE

MANUAL STRUCTURE AND ALIGNMENT

The manual is divided into two parts:

Part I - Installation

Part I includes an introduction to the DWBI A, product specifications, and instructions for installing and testing a DWBI A system. It is intended for DIGITAL personnel or customers who install this adapter. A knowledge of VAX hardware is assumed.

Part II - Technical Description

This part of the manual provides the technical information needed by the system programmer and the support group, as well as by customer engineers and programmers who incorporate this adapter into their own product or system. A knowledge of VAX architecture, the VAX Bus Interconnect (VAXBI), and the UNIBUS is assumed.

RELATED DOCUMENTATION

The DWBI A is one of a family of processors, memories, and adapters that use the 32-bit VAXBI bus. For a functional summary of the VAXBI bus and a description of VAXBI options, see the *VAXBI Options Handbook*, EB-[illegible]-46.

NOTE: *For ease of use and for a fuller comprehension, the DWBI A adapter (VAXBI to UNIBUS adapter) will be referred to as DWBI A throughout this document. The VAXBI bus will be referred to as VAXBI, and UNIBUS bus will be referred to as UNIBUS.*

PART 1
INSTALLATION

CHAPTER 1

CHAPTER 1
INTRODUCTION

1.1 PRODUCT DESCRIPTION

The VAXBI to UNIBUS Adapter (DWBUA) enables transfers between the high-speed synchronous VAXBI and the asynchronous UNIBUS. Through the DWBUA, the VAXBI has access to any UNIBUS address space, and the UNIBUS has access to any VAXBI address space.

The DWBUA transfers data between the buses in two ways:

1. Through the Direct Data Path (DDP) the data is transferred immediately.

2. Through a Buffered Data Path (BDP), the DWBUA [illegible] buffers [illegible] (16 bytes) of data per transfer to maximize the VAXBI bandwidth.

All VAXBI-initiated transactions transfer data through the Direct Data Path. UNIBUS-initiated transactions can transfer data through either the Direct Data Path or a Buffered Data Path.

Other features of the DWBUA are:

- UNIBUS arbitration
- UNIBUS devices can interrupt on the VAXBI
- Data transfer rate up to [illegible]
- Self-test to verify data paths and control logic, and to report failures to the VAXBI

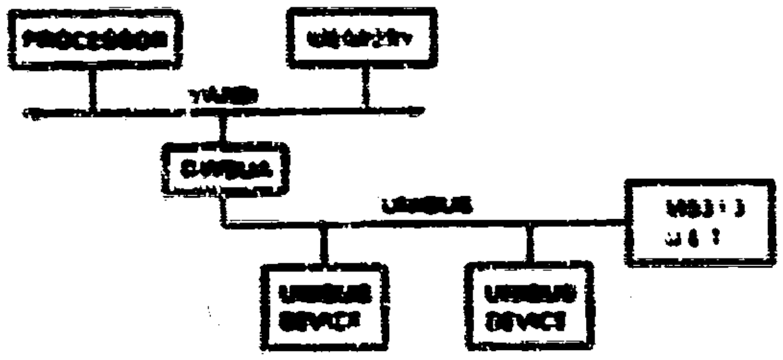


Figure 1-1 Typical DWBUA Configuration

1.2 SPECIFICATIONS

1.2.1 Bus Loading

The DWBL-A is 0.5 dc unit load on the UNIBUS

The DWBR-A is 1.5 ac unit load on the UNIBUS

1.2.2 Power Requirements

Table 1-1 DWBL-A Power Requirements

	POWER (Watts)			
VOLTAGE	Minimum	Typical	Standard	Maximum
+5V	3.75	4.50	4.75	5.25
-12V	-0.01	0.036	0.54	0.6

1.2.3 Current Requirements

Table 1-2 DWBL-A Current Requirements

	CURRENT (Amps)			
VOLTAGE	Minimum	Typical	Standard	Maximum
+5V	0.75	0.9	1.1	1.3
-12V	-0.001	0.003	0.045	0.05

1.3 SUPPORTED UNIBUS DEVICES

A subset of the available UNIBUS devices is supported on a configuration with a DWBL-A. See Appendix A for details.

CHAPTER 2

CHAPTER 2
INSTALLATION AND TEST

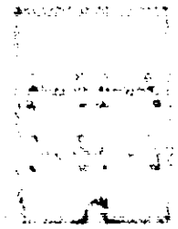


Figure 2-1

Table 2-1 DWBLA Components – UNIBUS Installed in BA23/BA123 Box

Component	Qty	Part Number	Location
DWBLA module	1	Y1010	VAXBI cardcage
UET module	1	M9313	UNIBUS cardcage
UNIBUS pathboard	1	M7168	UNIBUS cardcage
Transition header	1	12-22240-01	VAXBI cardcage
UNIBUS cable	1	17-00837-01	M7168 to transition header

Table 2-2 DWBLA Components – UNIBUS Installed in BA11 Box

Component	Qty	Part Number	Location
DWBLA module	1	Y1010	VAXBI cardcage
UET module	1	M9313	UNIBUS cardcage
UNIBUS pathboard	1	M7168	UNIBUS cardcage
Transition header	1	12-22240-01	VAXBI cardcage
UNIBUS cable	2	17-00837-01	M7168 to transition header
DEC STD 120 power bus cable	1	17-00931-01	Processor cabinet to UNIBUS cabinet

The DWBLA components are put together in the configuration shown in Figure 2-2.

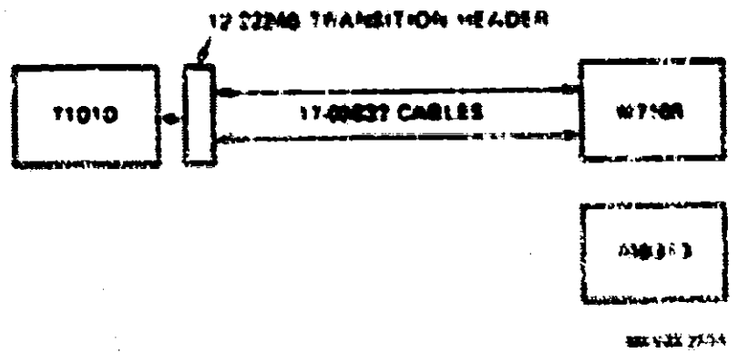


Figure 2-2 DWBLA Configuration

2.2 INSTALLATION

CAUTION
An antistatic wrist strap connected to an active ground must be worn when installing the DWBLA.

WARNING
Shut off system power before proceeding.

1. Attach the two UNIBUS cables to the M7168 pathboard (Figure 2-4). The connectors are keyed

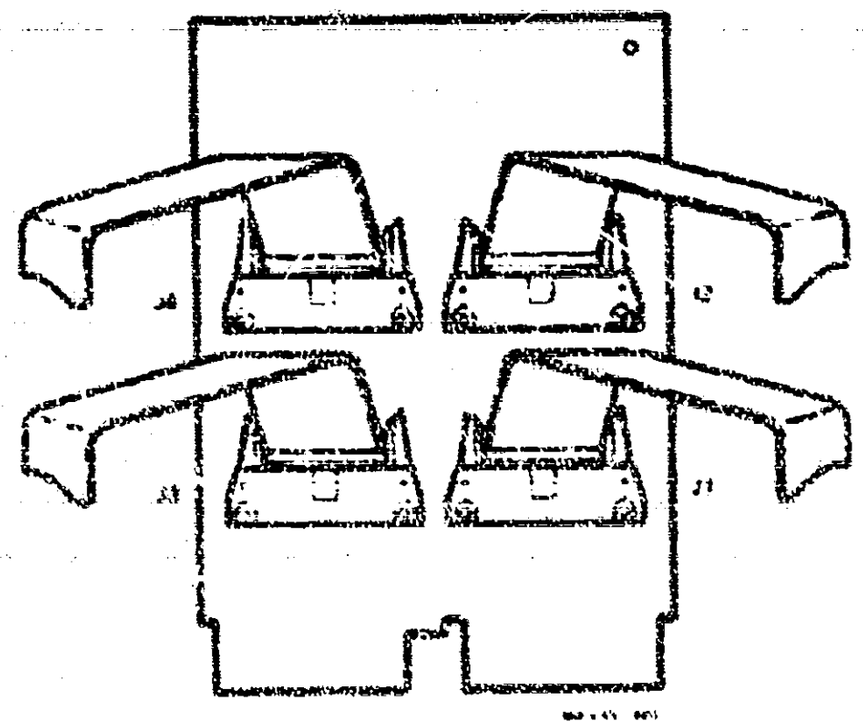


Figure 2-4 M7168 Pathboard with UNIBUS Cables

2. Insert the M7166 port board into slot 1, segments A and B, of the UNIBUS backplane (Figure 2-4).

3. Insert the M9313 UET module into the last slot, segments A and B, of the UNIBUS backplane (Figure 2-4).

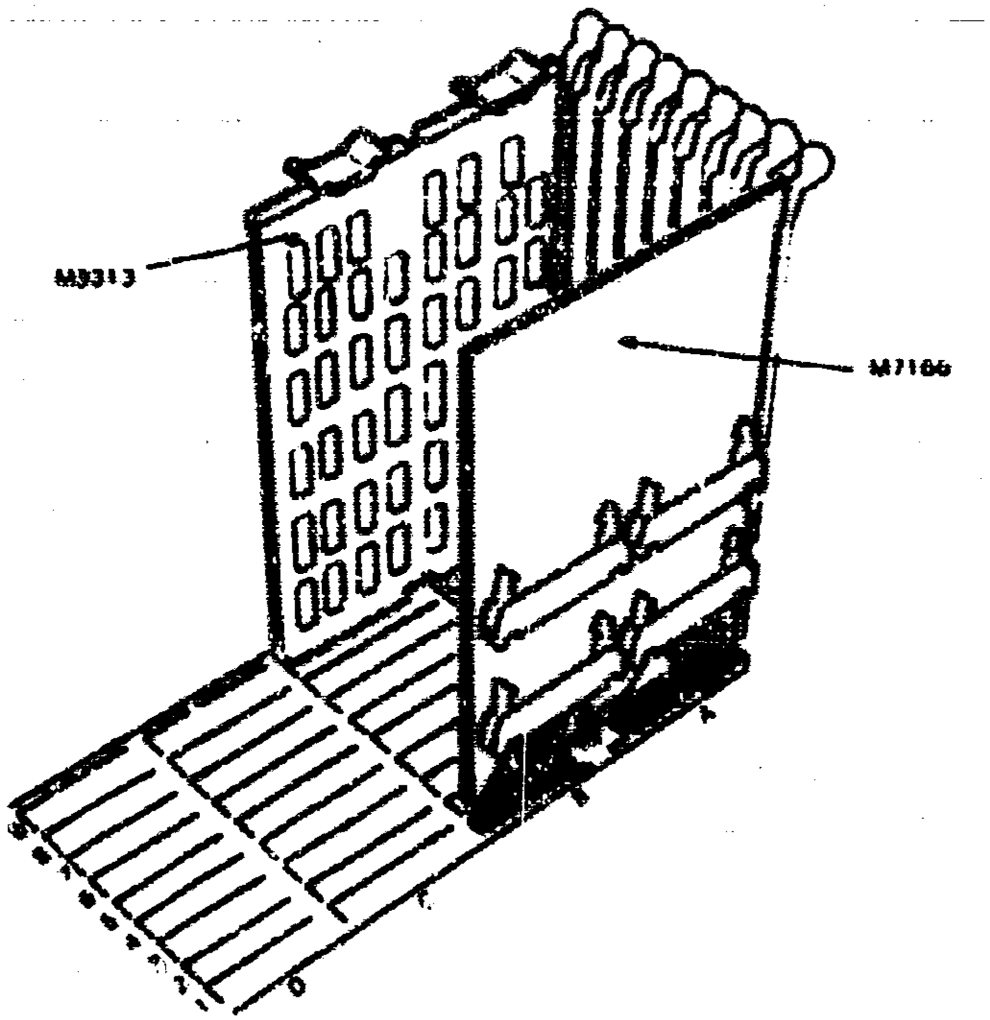


Figure 2-4 UNIBUS Backplane

4. Insert grant continuity cards in all unused UNIBUS slots.

NOTE

For field installations only, the T1010 module may be installed in any empty VAXBI slot except slot 1. Installation in the next empty slot after slot 1 is suggested.

5. Install the transition header on the backplane of the slot that contains the T1010 module (Figure 2-5).

NOTE

When installing the transition header, use only the torque screwdriver (P/N [illegible]) provided in the Field Service kit.

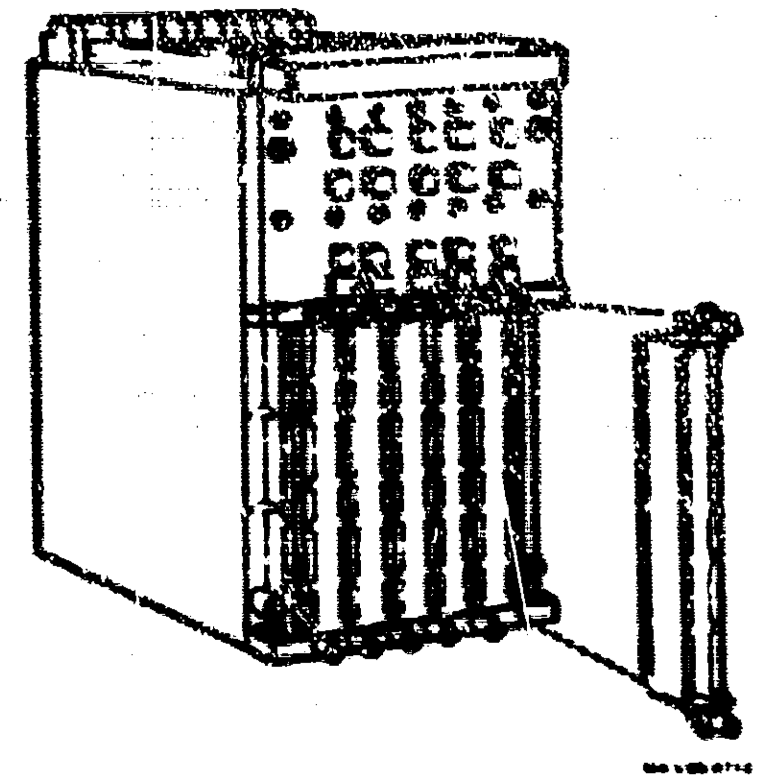


Figure 2-5 VAXBI Transition Header Installation

6. Refer to Figure 2-6 and connect the four I/NIBUS cables to the Ethernet header assembly.

J1 segment 1 (left)
J2 segment 1 (right)
J3 segment 0 (left)
J4 segment 0 (right)

The connectors are keyed.

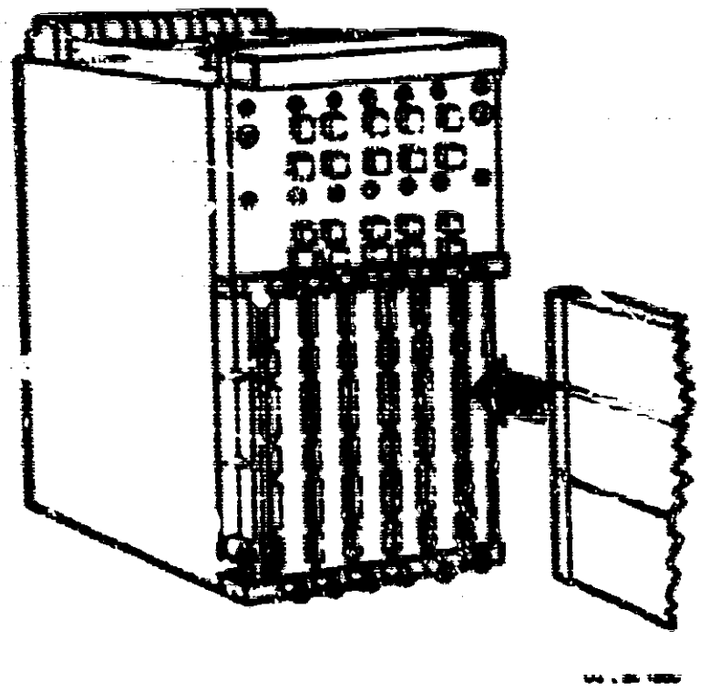


Figure 2-6 I/NIBUS Cable Connections

7. Insert the T1010 module into the appropriate slot of the VAXBI backplane.

8. If the I/NIBUS backplane is in an expansion cabinet, the power bus cable (P/N 17-01961-01) may be installed from the processor cabinet to the expansion cabinet.

9. Power up the system. The DWBI's self-test runs upon power-up. Check that the yellow LED on the T1010 module lights. See Figure 2-7.

If the yellow LED does not light, see Section 2.4.

10. Run one full pass of EVRTB, the DWBI's maintenance program. See Section 2.4.2.

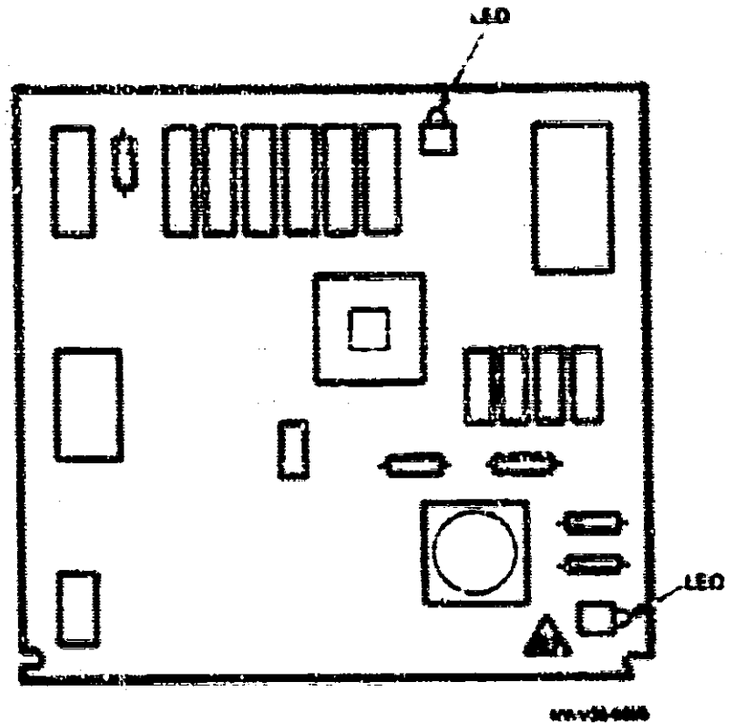


Figure 2-7 T1010 Module

2.3 TEST

2.3.1 Self-Test Microdiagnostic Program

NOTE
A UNIBUS Exerciser Terminator (UET) module (29-23130) must be installed in the last slot, segments A and B, of the UNIBUS backplane. The DWBUA self-test runs only if the UET module is installed.

The DWBUA self-test microdiagnostic program runs at powerup or when the VAXBI Control and Status Register RESTART bit (BICSR<15>) is set. Successful completion of the self-test is indicated by the lighting of the yellow LED on the T1010 module. The location of the LED is shown in Figure 2-7.

The DWBUA self-test microdiagnostic consists of 10 separate tests, which are described in Appendix C.

2.3.2 Microdiagnostic Program

The microdiagnostic program for the DWBUA is EVCBB.B. It is a level 3 diagnostic that runs standalone under the VAX diagnostic supervisor, and it isolates failures to the ratio of functions.

Descriptions of the microdiagnostic tests can be found in Appendix D.

To run EVCBB, do the following:

NOTE
Operator input is underlined.

1. Run the diagnostic supervisor.

2. Attach the DWBUA:

   DS> ATTACH DWBUA HLB DWn node br RET

   DWn is the number of the DWBUA. "n" is a number between 0 and 7.

   "node" is the VAXBI node ID, expressed as a decimal number (0 to 15).

   NOTE
   Refer to the appropriate system user guide to determine the node ID number.

   "br" is the UNIBUS BR interrupt level, a number between 4 and 7. The recommended value is 7.

3. Run the microdiagnostic:

   DS> RUN EVCBB/SECTION=xxx RET

   Inclusion of the SECTION name ("xxx" in the above command) is optional. If no SECTION name is included, the DEFAULT section is run. The SECTION names and the tests they include are listed in Table 2-3.

Tests 31 and 32 can be run only if a UNIBUS Extender (UBE) is attached.

Table 2-3 Microdiagnostic Program Sections

Section	Tests
DEFAULT	1 - 30
ALL	1 - 32
UBE	31, 32

2.4 ERROR RECOVERY

This procedure provides the information needed to isolate a DWBUA failure to one of its assemblies (T1010 module, BC19 cable, M7504 pushbutton, UNIBUS or VAXBI backplane). Corrective maintenance of the DWBUA consists of faulty subassembly replacement.

This procedure does not attempt to isolate problems caused by devices attached to the UNIBUS. It does, however, identify the UNIBUS node that is causing a DWBUA malfunction.

The assumption is made in this procedure that system troubleshooting procedures have indicated a problem in the DWBUA. No system-specific troubleshooting procedures are included here.

2.4.1 Tools and Test Equipment

The tools and test equipment listed in Table 2-4 are needed to perform the maintenance procedure described in this section.

Table 2-4 Tools and Test Equipment for Maintenance Procedures

Equipment	Manufacturer	Designation	DIGITAL Part Number
Cable Wraps	Tyco	TX309	29-01691-01
Torque Screwdriver	Utica		29-17181-00
Bus Grant Card			54-17273

2.4.2 Procedure

This section is a step-by-step procedure for isolating faults to the field replaceable units (FRUs). It uses the tools and test equipment listed in Table 2-4 and the DWBUA adapter self-test. By using this procedure, faults in the DWBUA can be isolated when the system is not capable of running diagnostics. (Such a situation can occur if the DWBUA is on the boot path for the operating system and diagnostics.)

See Section 2.3.1 and Appendix C for information on the DWBUA adapter self-test.

NOTE
Follow the steps in the order listed.

1. **START** – Is the DWBUA malfunctioning?

   The DWBUA may be suspect if

   a. The system cannot be booted from a UNIBUS device.

   b. No UNIBUS devices can be used.

   c. The system console indicates that the node number corresponding to DWBUA adapter's node ID is malfunctioning.

   d. Excessive errors occur when using any UNIBUS device.

   e. The system crashes.

2. **POWER DOWN THE SYSTEM** – Wait 30 seconds for the stored power to drain off.

3. **OPEN THE CABINET** – Open the system cabinet so that the yellow lights on the modules can be seen.

4. **POWER UP THE SYSTEM** – This starts the DWBUA self-test.

5. **CHECK THE LIGHT ON THE T1010 MODULE** – If the yellow light on the T1010 module is lit, the DWBUA has passed self-test. The problem is most likely not in the T1010 module, the UNIBUS cabling, or the terminator card (UFT). If the light is OFF, go to Step 7.

6. **RUN EVCBB** – If the system is operational, run the system level diagnostic, EVCBB, to further verify that the problem is not in the DWBUA. Refer to the microdiagnostic printout and documentation to isolate the failing FRU if this diagnostic should fail.

   If one of the symptoms listed in Step 1 exists, but the DWBUA self-test passes, the problem is probably somewhere other than in the DWBUA. Refer to Table 2-5 for suggested areas to troubleshoot.

Table 2-5 Symptoms and Possible Causes

Symptom	Possible Cause
Cannot boot from a UNIBUS device	Boot device
Unable to use devices on the UNIBUS	Bad device or software
Excessive errors when using any devices on the UNIBUS	Devices on the bus or system-wide problems
System crashes	System software

7. **THE YELLOW LIGHT IS OFF** – If the yellow light on the T1010 module is OFF, the self-test has failed. Look for a fault in one of the items in Figure 2-1. If no fault exists in these items, look for a UNIBUS device that is causing the UNIBUS to malfunction.

8. **DETERMINE NODE NUMBER AND STARTING ADDRESS**

   a. Halt the system from the console by typing CTRL P.

   b. Type E address to examine the contents of the Device Type Register (bb+00) for each node space in succession until one with a value of [illegible] is found. This is the DWBUA device type. Make a note of the address. (See Figure [illegible] and Appendix [illegible].)

   If working on a system that has more than one VAXBI, bus 0 addresses are as described. See Table 2-6 for the base addresses for bus 1 through bus 3.

Table 2-6 Multiple VAXBI Base Addresses

VAXBI Bus #	Base Address
0	2000 0000
1	2200 0000
2	2400 0000
3	2600 0000

NOTE
If nothing is returned from any of the examines, a system problem exists. See the troubleshooting procedures for the system being used. THE PROBLEM IS NOT IN THE DWBUA.

Example 2-1: Determining Node Number and Starting Address

>>> E	20000000 <CR>		This is the base address of the first node in I/O space: node 0
P	20000000	00010001	Address and contents returned. Node 0 is not a DWBUA.
>>> E	20002000		This is the base address of node 1
P	20002000	00010101	Node 1 is not a DWBUA.
>>> E	2000C000		This is the base address of node 6
P	2000C000	00010102	Node 6 is a DWBUA.

9 **FIND GPR0 ADDRESS** – Subtract 10 (GPR0 address). Add 10 (hex) to the address found in the previous step.

Example 2-2 Finding the Address of GPR0

Node 1 GPR0 = 30002000 + 10 = 30002010
Node 2 GPR0 = 30004000 + 10 = 30004010
Node 3 GPR0 = 30006000 + 10 = 30006010
Node 4 GPR0 = 30008000 + 10 = 30008010
Node 5 GPR0 = 3000A000 + 10 = 3000A010
Node 6 GPR0 = 3000C000 + 10 = 3000C010

10 **EXAMINE GPR0** – Use the console to examine GPR0 at the address calculated in the last step. GPR0 bits <31:16> contain the test number that failed in the self-test. Refer to Appendix C for a description of the self-test execution tests.

NOTE

Failure of the DWBUA self-test can prevent accessing of the DWBUA internal registers. To access these registers to explore the cause of the self-test failure, set the BCICSR (bb+28) bit <08> (LCSREN).

11 **ISOLATE FRU** – Use the flowchart in Figure 2-8 to isolate the FRU at fault.

NOTES

1. **The T1010 module is suspect throughout this troubleshooting procedure since it is the engine running the test.**

2. **Power-down the system to replace a component. When the system is powered back up, the self-test will run. Return to Step 1 of this procedure to verify the fix.**

3. **When replacing a component, follow the removal and replacement procedures in the installation manual for the system being used.**

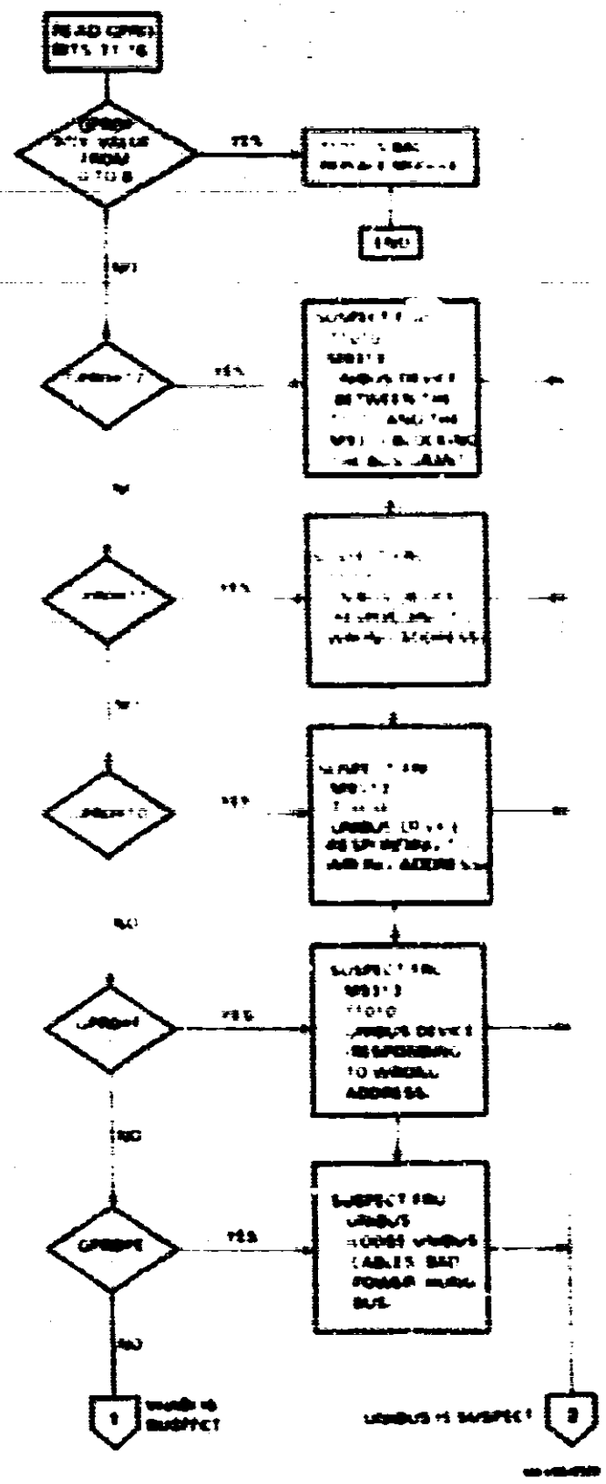


Figure 2-8 Troubleshooting Flow (Sheet 1 of 3)

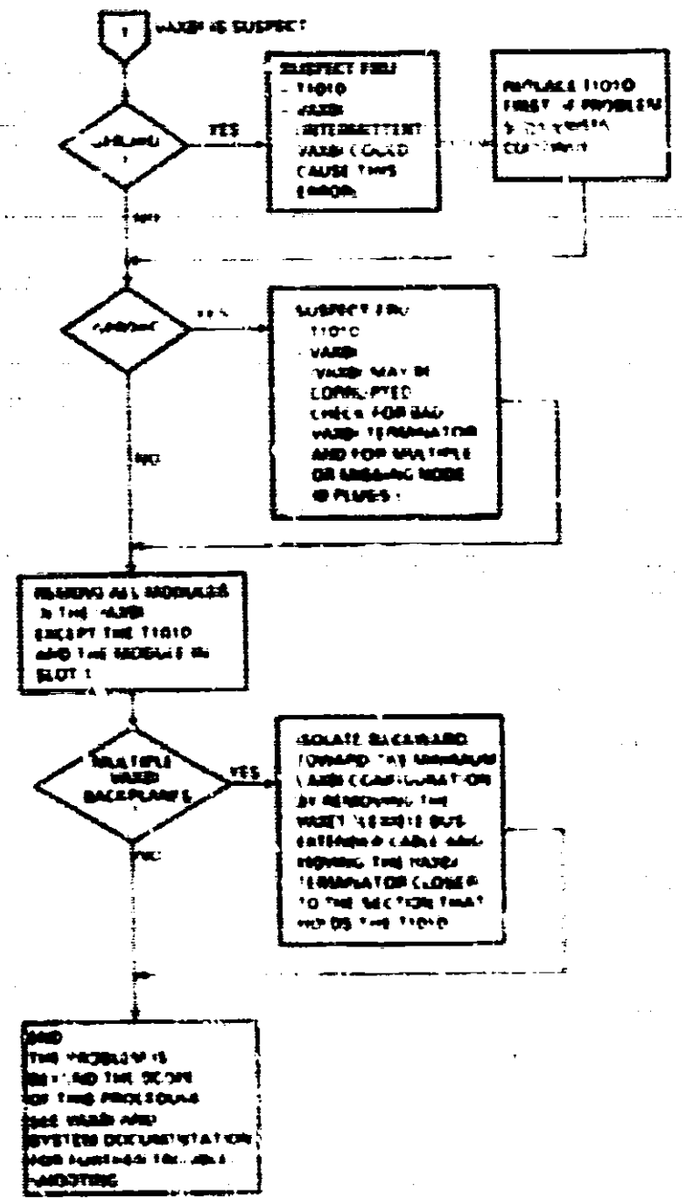


Figure 2-8 Troubleshooting Flow (Sheet 2 of 3)

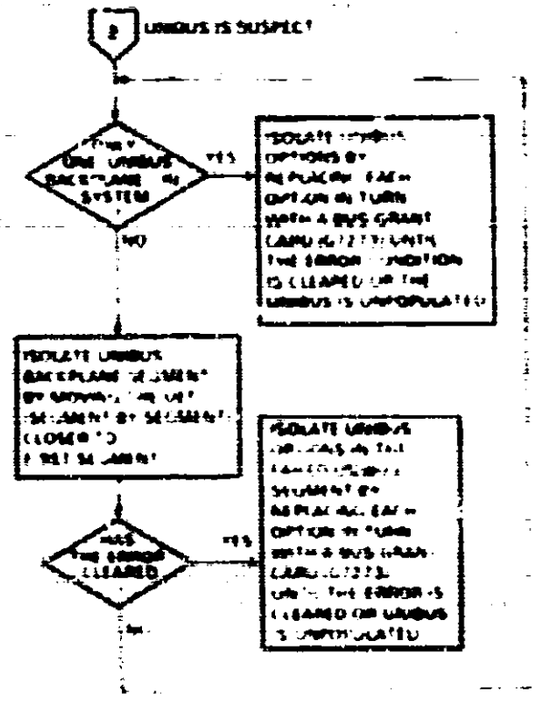


Figure 2-8 Troubleshooting Flow (Sheet 3 of 3)

2.4.3 Helpful Hints

The DWBI A self-test may not run to successful completion if the system includes VAXBI nodes that use burst mode or that excessively stall the VAXBI bus. The DWBI A self-test may fail if the configuration is large and has extensive VAXBI bus activity.

If these hints if the self-test has passed but the DWBI A still does not work correctly. Most of the items listed relate to the VAXBI S

1 PROBLEM: SYS\ unusual errors on VAXBI S devices

SUGGESTED ACTION: Verify VAXBI DWBI A node ID and arbitration mode

The DWBI A must be node 0 (receive systems based on BA42-SC AD boxes) and the software must set the DWBI A to fixed-high priority. Verify this by reading the device Type Register (bb+00) for node 0 to ensure that the device is DWBI A (see Appendix H). Also read the VAXBI Control and Status Register (bb+[illegible]) and the contents of [illegible] should be 8 (hex), fixed-high arbitration

2\. **PROBLEM:** Intermittent operation of UNIBUS devices, involving several or all options on the UNIBUS.

SUGGESTED ACTION: Verify the UNIBUS power and quiescent levels (Tables 2-7 and 2-8).

Table 2-7 UNIBUS Power

Voltage (Volts)	UNIBUS DC Voltage Level (Volts)	P.S. Ripple p-p Maximum (mV)
+5	[illegible]	[illegible]
+12	[illegible]	[illegible]

Table 2-8 UNIBUS Quiescent Levels

Line	Quiescent Level (Volts)
BRs NPRs	[illegible]
AC LO DC LO	[illegible]
[illegible]	[illegible]
All others	[illegible]

SUGGESTED ACTION: Check if the configuration is correct.

a. Verify that the DW[illegible]-A is [illegible] on the [illegible] (except systems based on BA11-AC/AD boxes).

b. Verify that all NPR grant jumper wires (CA1 to CB1) have been removed from the UNIBUS backplane on every slot that has an NPR option.

c. Check that every empty UNIBUS slot contains a grant continuity card.

Two different grant continuity cards can be used. The first (G727A) goes into the UNIBUS backplane slot D and provides grant continuity for the four interrupts (BR4–BR7) but not for the NPR. When the G727A grant card is used in the empty slots, a jumper (CA1 to CB1) is needed for NPR grants. The second grant card (G7273) provides grant continuity for both BR and NPR grants, and is much easier to install.

d. Verify that the vector and address jumpers are correct for each option and that no two options are selected for the same address or vector.

e. Use the PAL-11 program to verify the configuration.

SUGGESTED ACTION: Verify that the configuration is supported.

Check that no nonstandard devices or unsupported devices are on the bus.

SUGGESTED ACTION: Look for bus loading problems on large UNIBUS configurations.

Calculate the ac and dc loading of the configuration. [illegible] A UNIBUS without a repeater can support 20 ac loads and 20 dc loads. (Refer to the *PDP-11 Bus Handbook* for details.)

3\. **PROBLEM:** One option does not work or the entire UNIBUS fails when the option is installed.

SUGGESTED ACTION: Verify that the option is supported on the UNIBUS.

a. Check the [illegible] documentation to ensure that the revisions are correct for the hardware and software.

b. If the option works but does not work correctly with the [illegible], [illegible] the option on a shortened UNIBUS.

c. Check that the jumper wire (from CA1 to CB1) has been removed from the UNIBUS slot in which the option is being installed.

PART 2
TECHNICAL
DESCRIPTION

CHAPTER 3

CHAPTER 3
PROGRAMMING

3.1 SYSTEM ADDRESS SPACE

3.1.1 Address Space Divisions

The 1024 megabyte system address space on the VAX 8600 is divided into memory space (from address 0000 0000 through 1111 1111 hexadecimal) and I/O space (from address 2000 0000 through 3111 1111 hexadecimal). Physical memory is assigned addresses starting at 0000 0000. Most I/O space is reserved for special uses.

Figure 3-1 shows the system address space divisions.

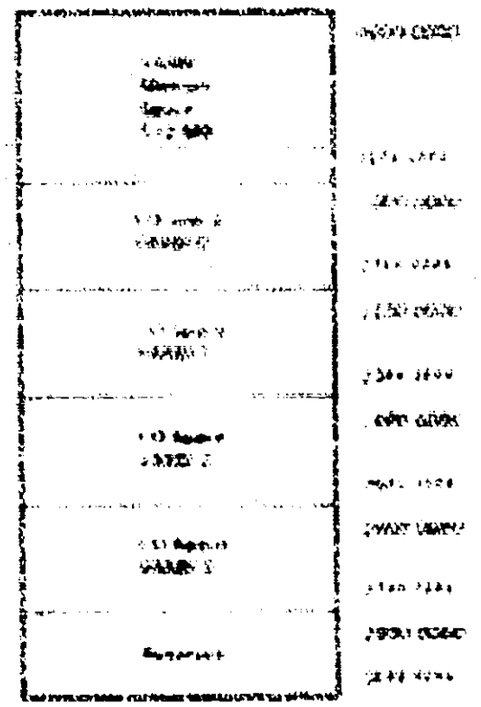


Figure 3-1 System Address Space
(Illustration)

3.2.2 System I/O Space

The 512 megabyte system I/O space is divided into several dedicated sections, as shown in Figure 3-2.

The locations of the DWBUA adapter's node space and window space depend on the DWBUA adapter's assigned node ID. If, for example, the DWBUA is assigned node 3, its node space and window space are located as shown in Figure 3-3. Appendix C lists the starting and ending addresses of the node space and window space for each node ID.

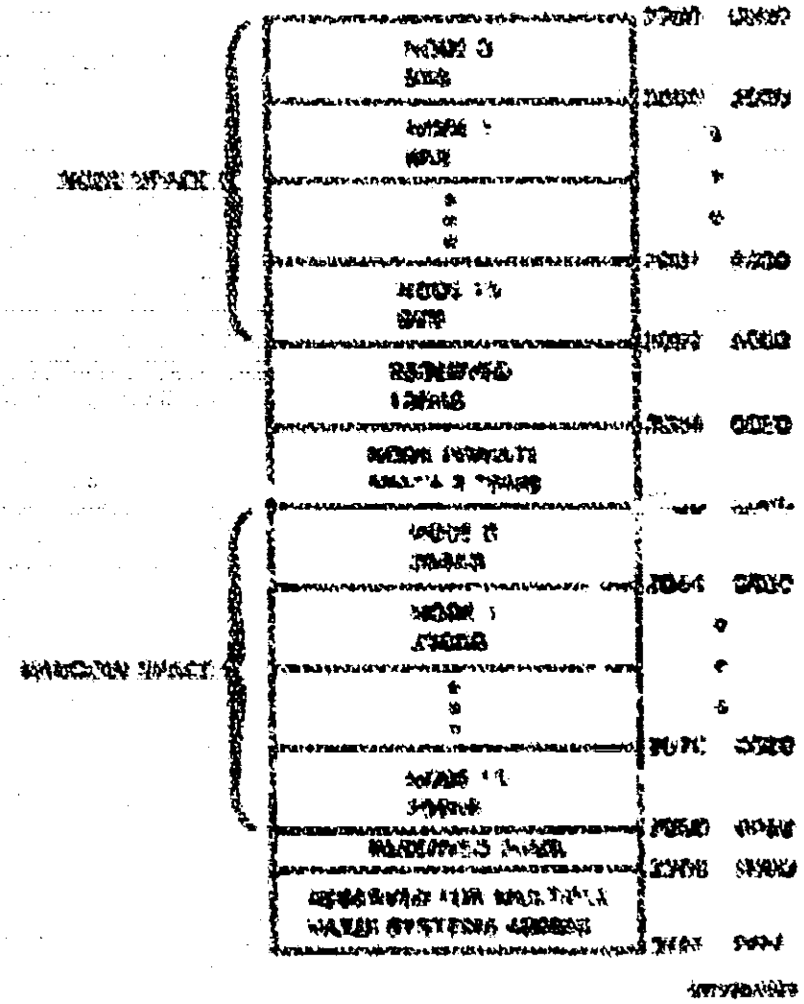


Figure 3-2 System I/O Space

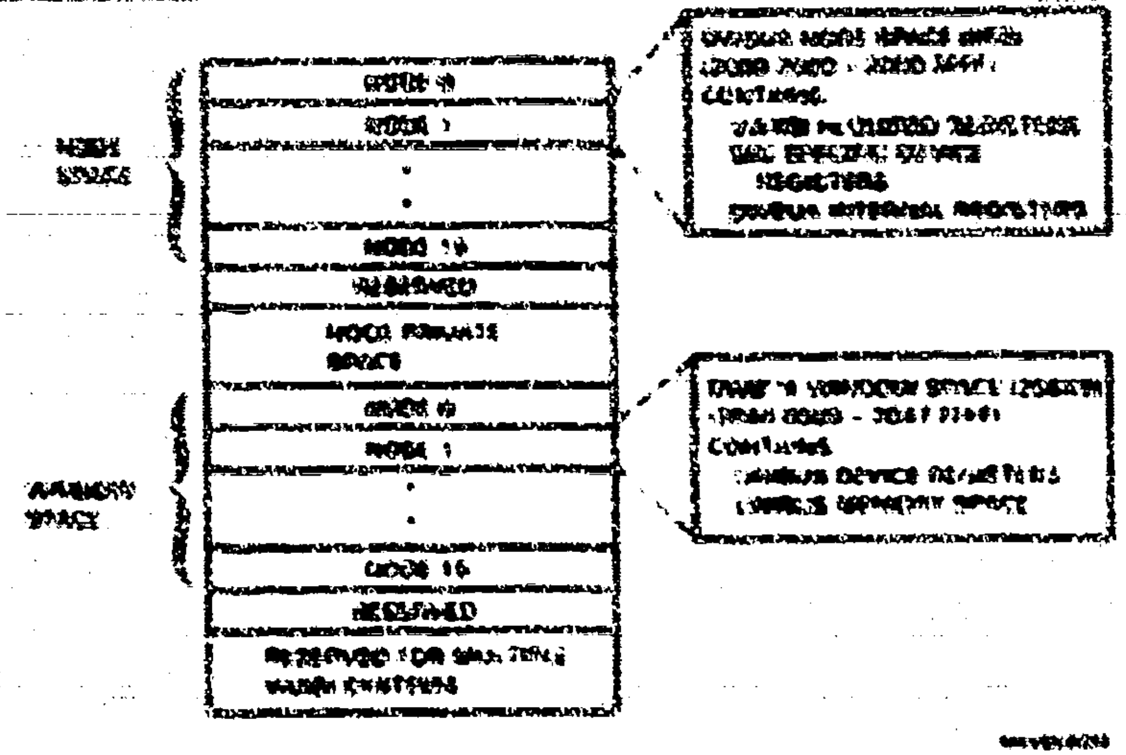


Figure 3-3 DWBUA Node Space and Window Space

3.3 DWBUA ADDRESS SPACE

The DWBUA adapter's node space is divided into three sets of registers: VAXBI required registers, BIIC specific device registers, and DWBUA registers. Figure 3-4 is a map of the DWBUA address space.

NOTE

The address of each register is stated as "bb + xxx." Use the following procedure to calculate the base address, "bb."

1. **Determine the DWBUA adapter's node ID. This is a hexadecimal number between 0 and F.**

2. **Solve for "bb" in the following equation:**

   bb = (2000 0000$_{hex}$) + (2000$_{hex}$ × (node ID$_{hex}$))

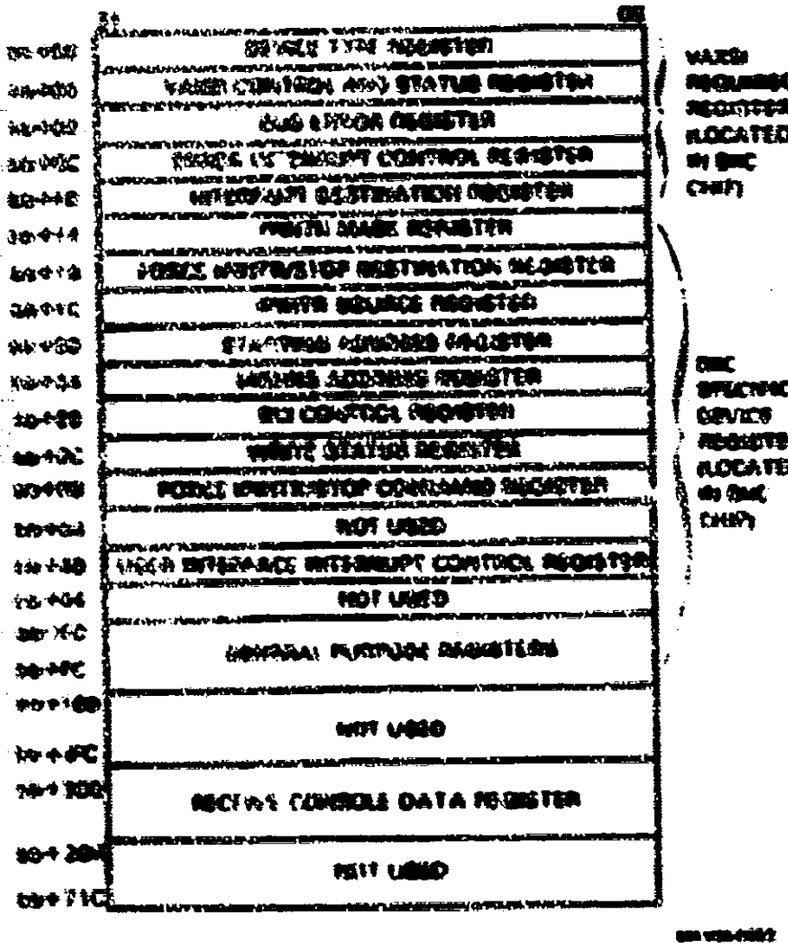


Figure 3-4 DWBR A Address Space (Sheet 1 of 2)

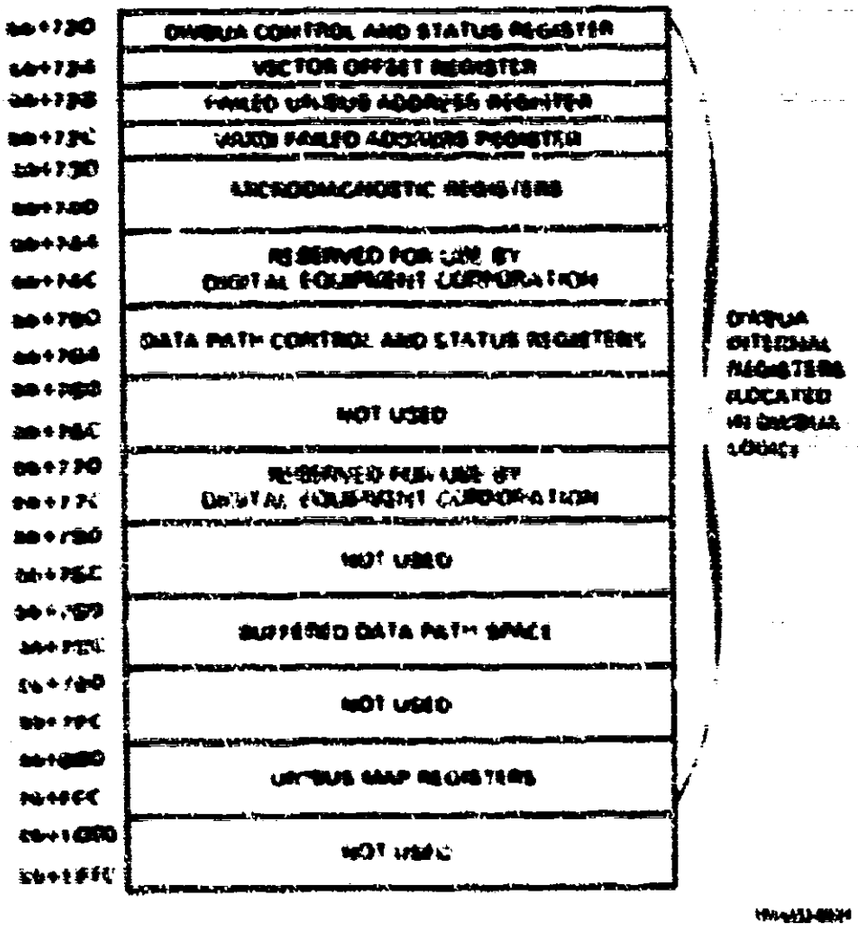


Figure 3-4 DWBR A Address Space (Sheet 2 of 2)

3.2.2 Register Bit Characteristics

The characteristics listed in Table 3-1 can apply to individual bits, to fields, or to entire registers. In the register descriptions in the following sections, the bit characteristics are identified after the name of each bit or field.

Bits indicated as "0" on the register diagrams are not implemented. These bits are READ/ZERO locations that always return "0".

Table 3-1 Register Bit Characteristics

Register Bit Characteristic	Description
DEVICE	Cleared following successful completion of the DWBUA self-test executed by the execution of BOOT 10H
RO	READ/ONLY
R/W	READ/WRITE
SC	Special Case; operation defined in the detailed description
SETUP	Cleared by a SETUP command directed to the DWBUA
W1C	Write 1 to Clear
WO	WRITE/ONLY; always reads 0

3.2.3 VAXBI Required Registers

The VAXBI required registers are implemented in the BIIC on the DWBUA. The discussion that follows focuses on the specific uses of these registers by the DWBUA. The state of each register following successful completion of the DWBUA self-test is included in the discussion of that register. VAXBI required registers that are not described here, or bits that are not included in the register descriptions, are initialized to the state defined in Appendix H.

The DWBUA, as a VAXBI node, is required to implement a number of registers. These registers are:

- Device Type Register
- VAXBI Control and Status Register
- Bus Error Register
- Error Interrupt Control Register*
- Interrupt Destination Register*

NOTE

Registers marked with * are described here in detail.

3.2.3.1 Error Interrupt Control Register – The Error Interrupt Control Register (BIIC+0C) controls the operation of interrupts initiated by a BIIC detected bus error. The LEVEL and VECTOR fields of this register must be initialized by the operating system. These fields are zero after successful completion of the DWBUA self-test. Figure 3-4 is an illustration of the Error Interrupt Control Register.

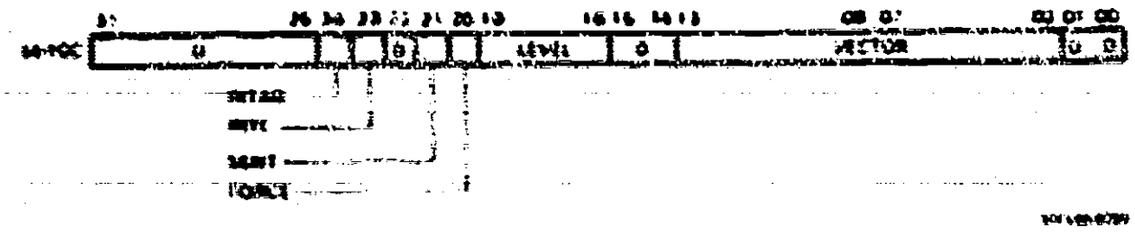


Figure 3-4 Error Interrupt Control Register

INTAH 31	Interrupt abort (W1C, DCLEAR, SC)	This bit is set if a VAXBI INTR command sent by the DWBUA is aborted.
INTC 23	Interrupt complete (W1C, DCLEAR, SC)	This bit is set when the vector for an error interrupt has been successfully transmitted or if a VAXBI INTR command sent by the DWBUA has aborted.
SFAIL 21	Send (W1C, DCLEAR, SETUP, SC)	The DWBUA has sent the VAXBI INTR command, and is awaiting the RSP XT from the VAXBI.
FORCE 20	Force (R/W, DCLEAR)	When this bit is set, the DWBUA forces an interrupt to occur regardless of the state of the Bus Error Register (BIIC+04). The DWBUA sets the FORCE bit when a DWBUA error has occurred and the DWBUA error interrupt enable (EIE) bit is set. The FORCE bit is cleared upon initialization. The operating system must clear this bit after servicing the error interrupt.
LEVEL 19:16	Level (R/W, DCLEAR)	The LEVEL field determines the level at which INTR commands are transmitted under the control of this register. The 0 corresponds to interrupt level A, the 1 to level B, the 2 to level C, and the 3 to level D. The operating system must initialize the LEVEL field.
VECTOR 15:02	(R/W, DCLEAR)	The VECTOR field contains the vector used during error interrupt sequences. It is transmitted when the DWBUA sends a VAXBI INTR cycle on an IDENT transaction that matches the conditions in the Error Interrupt Control Register. The operating system must initialize the VECTOR field.

3.2.2.2 **Interrupt Destination Register** - The format of the Interrupt Destination Register (bb+10) is shown in Figure 3-6.

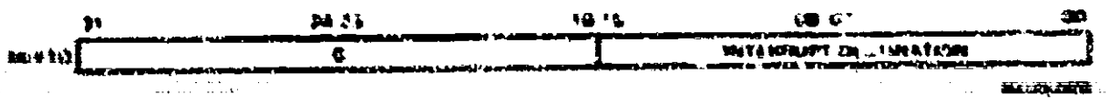


Figure 3-6. Interrupt Destination Register

INTERRUPT DESTINATION (BB+10) (WRITE)

The field determines which VAXBI nodes receive INTR commands sent by the IDA68 A. Each bit in the INTERRUPT DESTINATION field corresponds to one VAXBI node. Bit 0 corresponds to node 0, bit 1 to node 1, and so on. During an IDENT command, the destination node ID (VAXBI node number) is compared to the corresponding bit in the INTERRUPT DESTINATION field. The IDA68 A adapter's BIIC responds to the IDENT if that corresponding bit is set and if the level transmitted in the IDENT command matches the level of an interrupt pending in the BIIC.

The IDA68 A will not write bit in the INTERRUPT DESTINATION field which corresponds to the IDA68 A adapter's VAXBI node ID. The operating system must change this field to reflect the node ID of the interrupt-handler node. If an interrupt occurs before the INTERRUPT DESTINATION field is set by the operating system, the INTAD bit in one of the registers is set. The register in which the INTAD bit is set depends on the type of interrupt occurring. Four Interface Interrupt Control Registers (BB+40) store interrupt Error Interrupt Control Register (BB+48)

3.2.3 **BIIC Specific Device Registers**

The BIIC specific device registers are implemented in the BIIC on the IDA68 A. The discussion that follows focuses on the specific uses of these registers by the IDA68 A. The state of each register following successful completion of the IDA68 A self-test is included in the discussion of that register. BIIC specific device registers that are not described here, or bits that are not indicated in the register descriptions, are untouched by the tests defined in Appendix H.

The BIIC specific device registers control IDA68 A-specific functions of the BIIC. The BIIC specific device registers are:

- IPINTR Write Register
- Local IPINTR WRITE Destination Register
- IPINTR Source Register
- Interrupt Address Register*
- Failing Address Register*
- BIIC Control Register*
- Write Status Register
- Local IPINTR WRITE Command Register
- Error Interface Interrupt Control Register*
- General Purpose Register*

NOTE

Registers marked with * are examined here in detail.

3.2.3.1 Starting Address Register

3.2.3.1 Starting Address Register - The Starting Address Register (bb + 20) defines the lower limit of the DWBUA adapter's window space. Figure 3-7 is the Starting Address Register format.

31	24 23	16 15	08 07	00
bb+20	STARTING ADDRESS			

Figure 3-7 Starting Address Register

STARTING ADDRESS <31:18>	This field determines bits <29:18> of the lowest UNIBUS address. The DWBUA self-test leaves in this register the lower limit of the DWBUA adapter's window space, based on the node ID of the DWBUA. The range is 2040 0000 to 207C 0000 (bits <17:0> must be zero).

3.2.3.2 Ending Address Register

3.2.3.2 Ending Address Register - The Ending Address Register (bb + 24) defines the first location after the upper limit of the DWBUA adapter's window space. Figure 3-8 is the Ending Address Register format.

31	24 23	16 15	08 07	00
bb+24	ENDING ADDRESS			

Figure 3-8 Ending Address Register

ENDING ADDRESS <31:18>	This field defines bits <29:18> of the highest UNIBUS address. The DWBUA self-test leaves in this register the upper limit + 1 of the DWBUA adapter's window space, based on the node ID of the DWBUA. The range is 2044 0000 to 2080 0000 (bits <17:0> must be zero).

3.3.3.3 BCI Control Register – The BCI Control Register (bb+20) format is shown in Figure 3-9.

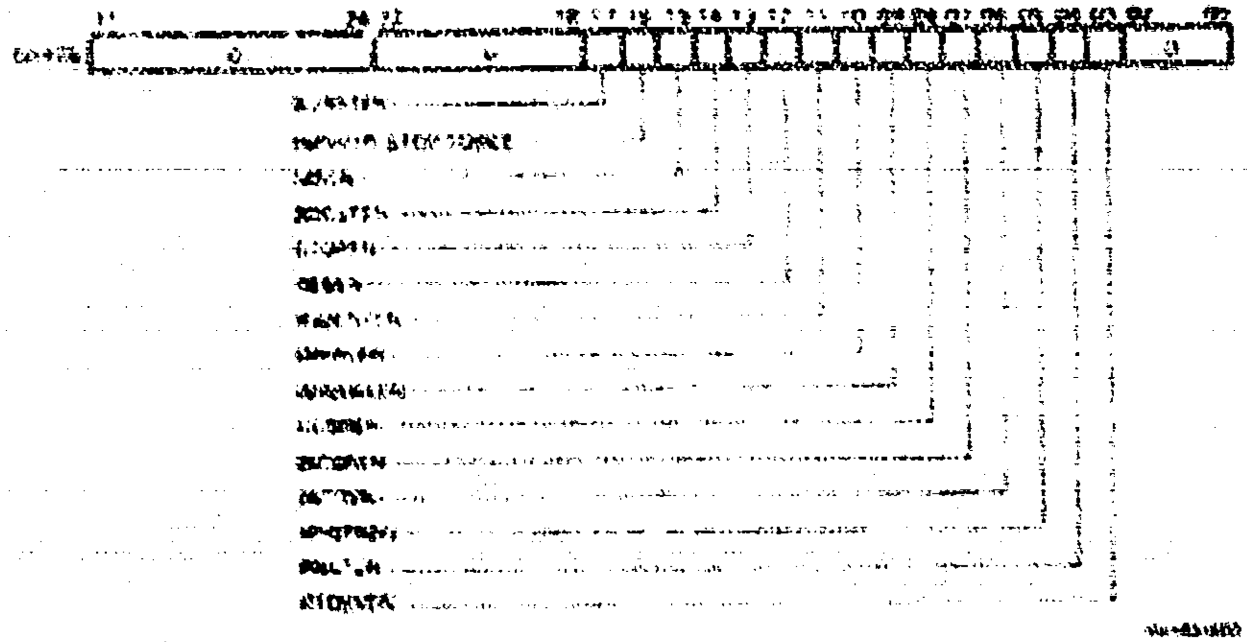


Figure 3-9 BCI Control Register

STOPEN <13>	STOP Enable (R/W, DCLO)	When set, this bit enables the DWBUA to respond to a VAXBI STOP command directed to it. The DWBUA adapter's BIIC asserts BCI SEL L and the appropriate BCI SC<2:0> code.
IDENTEN <11>	IDENT Enable (R/W, DCLO)	When set, this bit enables the DWBUA to forward interrupt vectors from UNIBUS devices when a transaction occurs on IDENT. The DWBUA adapter's BIIC asserts BCI SEL L and the appropriate BCI SC<2:0> code. This bit affects only the output of SEL L and the IDENT SC code.
UCSREN <08>	User CSR Space Enable (R/W, DCLO)	When this bit is set, the DWBUA can respond to a VAXBI READ or WRITE command with an address in DWBUA's user CSR space. The DWBUA adapter's BIIC asserts BCI SEL L and the appropriate BCI SC<2:0> code.

NOTE

The DWBUA sets the above three bits upon successful completion of its self-test. All other bits in this register should be clear.

3.3.3.4 User Interface Interrupt Control Register – Figure 3-10 is the User Interface Interrupt Control Register (bb+40) format.

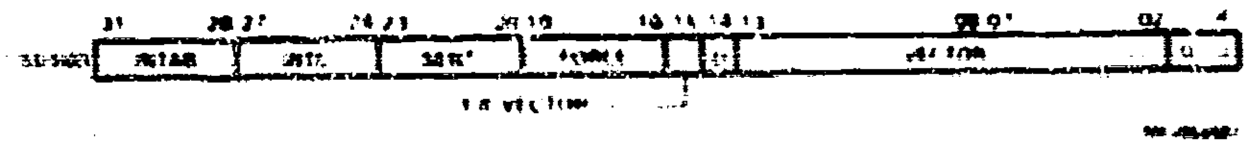


Figure 3-10 User Interface Interrupt Control Register

FORCE <19:16>	Force	This field must be zero.
EX VEC ENB <15>	External vector	This bit is set by the DWBUA self-test and it must remain set. It enables the DWBUA to use the external vector for transfer of UNIBUS interrupt vectors which have the controlled vector offset applied.

3.2.3.5 General Purpose Registers

3.2.3.5 General Purpose Registers - The only General Purpose Register (GPR) used by the DWBUA is GPR0 (bb+F0). Figure 3-11 shows the format of GPR0.

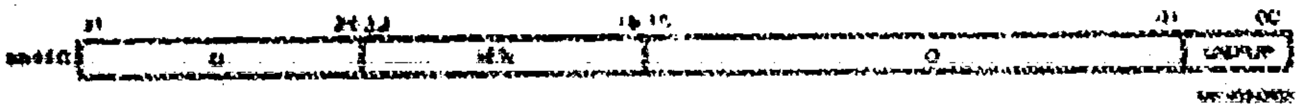


Figure 3-11 General Purpose Register 0

IEN <23:16>	Internal Error Number (R/W)	This field is a copy of the IEN field of the BIUCSR ([illegible]). This field contains the self-test error number if the DWBUA self-test fails and if the DWBUA functions sufficiently to write to this register. (See Appendix C.) This field is clear if the DWBUA self-test passes.
UNPUP <00>	UNIBUS Power Up (R/W)	This bit is set when the UNIBUS power is ON. It is cleared by the DWBUA when UNIBUS power goes down. This bit is set upon successful completion of the DWBUA self-test. (The DWBUA fails self-test if the UNIBUS is not powered up.)

General Purpose Registers 1-3 are not used by the DWBUA. They are cleared by the BIIC self-test.

3.2.4 DWBUA Internal Registers

With the exception of the Data Path Control and Status Registers and the upper 16 UNIBUS Map Registers, all DWBUA internal registers are cleared by the DWBUA self-test.

3.2.4.1 Receive Console Data Register - The Receive Console Data Register (RXCD) is considered an unimplemented register by the DWBUA. The DWBUA responds with NO ACK to any access to this register. Any VAXBI node that might access this register should have a way to detect this response. Figure 3-12 shows the format of the Receive Console Data Register.

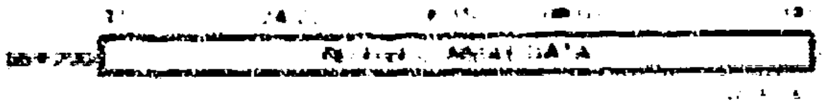


Figure 3-12 Receive Console Data Register

3.2.4.2 DWBI A Control and Status Register - The DWBI A Control and Status Register (BI_CSR, bb+7A0) contains error and other operating information about the DWBI A. Figure 3-11 shows the format of the DWBI A Control and Status Register.

When an error occurs during DWBI A operation, the VAXBI is interrupted if interrupts are enabled. Error interrupts are sent to the VAXBI in two ways:

- The BIIC sends an error interrupt to the VAXBI if an error occurs during a VAXBI transaction.
- The FORCE bit in the Error Interrupt Control Register (bb+0C) is set by the DWBI A if an error occurs either on the DWBI A or during a CNBI S operation, and if error interrupts are enabled.

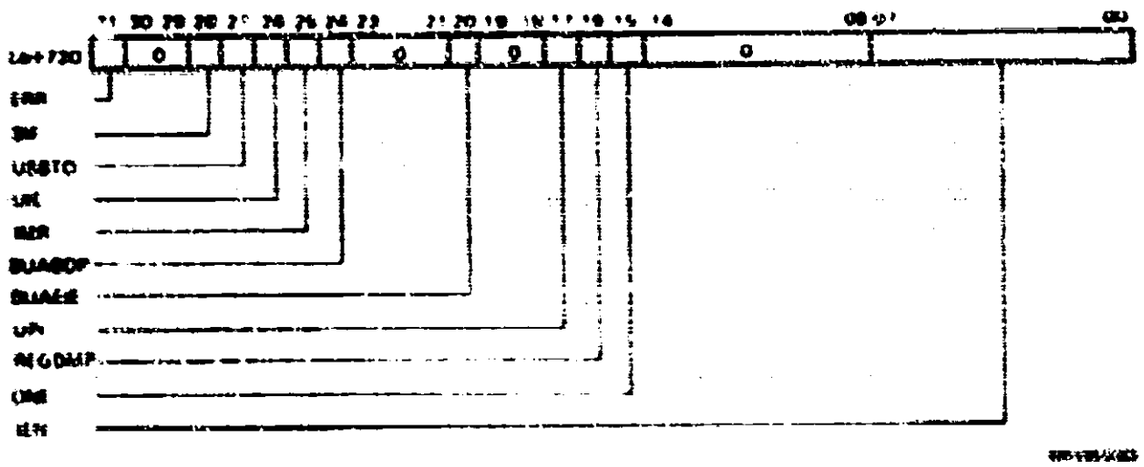


Figure 3-11 DWBI A Control and Status Register

LRR (31)	Error (RO, INIT)	This bit is a logical "OR" of all error bits in the BI_CSR.
BII (28)	VAXBI Failure (WIC, INIT)	This bit is set if a DWBI A initiated VAXBI transaction fails. A VAXBI failure has occurred if the DWBI A receives any of the following in response to one of its VAXBI commands: NO ACK – Illegal confirmation code Read data substitute status code See Table 3-1 for a list of BIIC EVENT codes that cause the BII bit to set.
LOSTO (27)	CNBI S SSYN Timeout (WIC, INIT)	This bit is set when a VAXBI-to-CNBI S command attempts access to a CNBI S address and does not receive SSYN within 19.2 µs after assertion of MSYN.
LII (26)	CNBI S Interlock Error (WIC, INIT)	This bit is set if a CNBI S DATIP command is not immediately followed by a DATOB(I) command. This happens when MSYN is dropped by a device after the DATIP command.
INR (25)	Invalid Map Register (WIC, INIT)	This bit is set if a CNBI S Map Register (bb+800 – bb+FFC) which has its VALID bit clear is accessed during a CNBI S-to-VAXBI transaction.
BUAEBDP (24)	Bad Buffered Data Path Selected (WIC, INIT)	This bit is set if (inadvertently) Buffered Data Path 0 or 1 is selected.
BUAERR (23)	DWBI A Error Interrupt Enable (R/W, INIT)	If an error occurs, the DWBI A initiates an error interrupt on the VAXBI if this bit is set.
UPI (19)	CNBI S Power Initialization (WO)	Writing a one to this bit causes a power-up initialization of the CNBI S.
REGDMP (18)	Microdiagnostic Register Dump (WO)	Writing a one to this bit causes the microcode contained in dump the internal registers to the Microdiagnostic Registers (bb+700 – bb+7B0). A RESET of the Microdiagnostic Registers area can then be performed to read the values.
ONI (15)	(RO)	The ONI bit is a READ ONLY bit that should always read one. This bit is used for error handling by the operating system, if it reads zero, an error has occurred.
INT (07:00)	Internal Error Number (RO)	This field contains the self-test error number of the DWBI A self-test fails and if the DWBI A functions sufficiently to write to this register. This field is clear if the DWBI A self-test passes.

3.2.4.3 **Vector Offset Register** - The Vector Offset Register (VOR, bb+1224) contains a 5-bit field which is concatenated with the incoming I NIBUS vector to form the new VAXBI vector.

The Vector Offset Register format is shown in Figure 3-14.

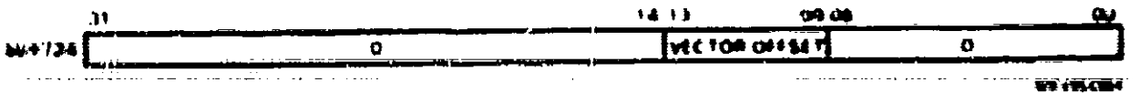


Figure 3-14 Vector Offset Register

VECTOR OFFSET <13:09> (R/W)

The five bits in this field are concatenated with the incoming I NIBUS vector (I NIBUS bits <08:02>) in the range of 00H to 7FH to form the new 14-bit VAXBI vector (1140). The VECTOR OFFSET field bits are READ/WRITE; they must be set by the operating system.

NOTE

Bits <31:14> and <08:00> must be zero.

3.2.4.4 **Failed I NIBUS Address Register** - When a VAXBI-to-I NIBUS transaction results in a SSYNC timeout, the failed I NIBUS Address Register (FUBAR, bb+1228) holds the failed I NIBUS address sent by the VAXBI master. I NIBUS address bits <17:02> are stored in FUBAR <15:00>.

The FUBAR is written only on the first occurrence of an address failure. Subsequent failures do not modify the contents of the FUBAR until the LOSTTO bit of the BI ACSR is cleared.

Figure 3-15 shows the format of the Failed I NIBUS Address Register.

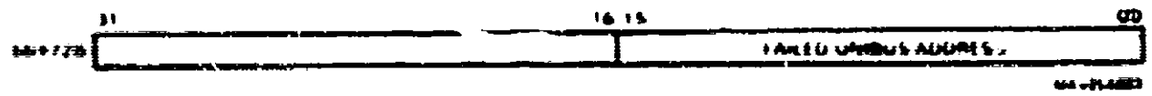


Figure 3-15 Failed I NIBUS Address Register

FAILED I NIBUS ADDRESS <15:00> (RO)

This field contains bits <17:02> of the first failed I NIBUS address. Subsequent failures are not recorded until the LOSTTO bit of the BI ACSR is cleared.

3.2.4.5 VAXBI Failed Address Register - The VAXBI Failed Address Register (BIFAR, bb+720) holds the address of a failed DWBUA-initiated VAXBI transaction. The BIFAR is written on the first occurrence of a VAXBI address failure only. The BIF bit of the BICSR is set when the BIFAR is written; subsequent failures do not modify the contents of the BIFAR until the BIF bit has been cleared.

Figure 3-16 shows the format of the VAXBI Failed Address Register.

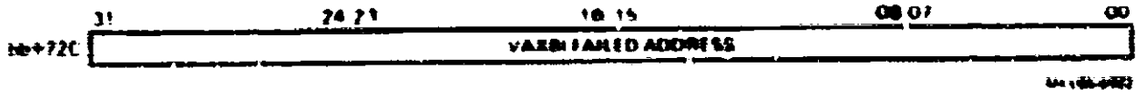


Figure 3-16 VAXBI Failed Address Register

VAXBI FAILED ADDRESS <31:00>	(RO)	This register contains the VAXBI address of the first DWBUA-initiated failure on the VAXBI. Subsequent failures are not recorded until the operating system clears the BIF bit in the BICSR.

3.2.4.6 Microdiagnostic Registers - The five Microdiagnostic Registers (bb+730 - bb+740) receive the address and status information for the five Buffered Data Paths. This information is received from the microcode control when a one is written to the REGDMP bit in the BICSR.

The Microdiagnostic Registers are READ-ONLY. A VAXBI WRITE transaction to any of these registers results in a NO ACK response from the DWBUA.

The Microdiagnostic Registers are listed in Table 3-2.

Table 3-2 Microdiagnostic Register Addresses

Microdiagnostic Register for BDP	Address
1	bb+730
2	bb+734
3	bb+738
4	bb+73C
5	bb+740

The five Microdiagnostic Registers have an identical format which is shown in Figure 3-17.

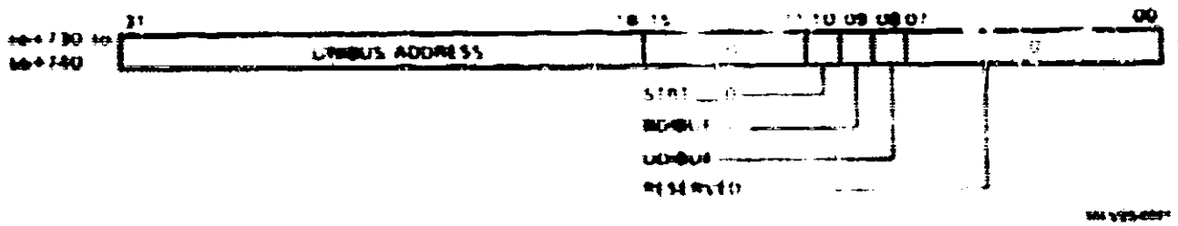


Figure 3-17 Microdiagnostic Register

VAXBI ADDRESS <31:16>	(RO)	This field holds VAXBI address bits <31:16> of the current outbound transfer through the specific Buffered Data Path.
STRT_0 <10>	(RO)	When set, this bit indicates that the first transaction through the Buffered Data Path began at an aligned or lowword address.
MAMP 1 <09>	(RO)	This bit is set to indicate that the BDP buffer contains VAXBI data.
UDMBUF <08>	(RO)	This bit is set to indicate that the BDP buffer contains UNIBUS data.

3.2.4.7 **Data Path Control and Status Registers** - The DWBI A has six Data Path Control and Status Registers (DPCSR, bb+'740 - bb+'768). DPCSR0 is for the Direct Data Path, and the remaining five correspond to the five Buffered Data Paths. The addresses of the Data Path Control and Status Registers are shown in Table 3-3.

Table 3-3 Data Path Control and Status Register Addresses

DPCSRn	Address
DPCSR0	bb+'740
DPCSR1	bb+'748
DPCSR2	bb+'750
DPCSR3	bb+'758
DPCSR4	bb+'760
DPCSR5	bb+'768

The six Data Path Control and Status Registers have an identical format, which is shown in Figure 3-18.

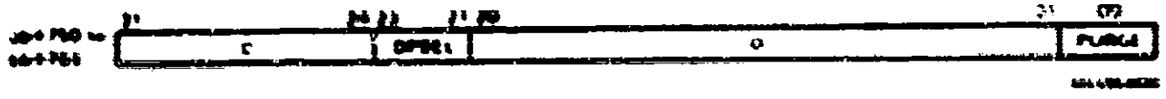


Figure 3-18 Data Path Control and Status Register

DPSEL <21:16>	Data Path Select (RO)	These three bits define the data Path (0 - Direct Data Path, 1 - 5 corresponds to the five Buffered Data Paths. This field is written by the DWBI A microcode.
PURGE <00>	Purge (WO)	When set by the operating system, the PURGE bit causes the specific BDP buffer to be purged. This is a WRITE ONLY bit.

Purging a BDP buffer has different effects depending on the buffer's status. For DPCSR0 (the Direct Data Path Control and Status Register), the BDP buffer is not purged and no further action occurs. For the other five Data Path Control and Status Registers, writing a one to the PURGE bit has the following results:

I/NIBUS data in buffer	The data is written to the VAXBI and the flags are cleared, indicating that the buffer is empty.
VAXBI data in buffer	The flags are cleared to indicate that the buffer is empty.
Empty buffer	No action occurs.

3.2.4.8 **Buffered Data Path Space** - The quadword buffers associated with each Buffered Data Path are addressable in DWBI A I/O space (bb+'780 - bb+'7D8). Although the BDP buffers are not usually accessed directly through software, they are READABLE and are supposed accessible for diagnostic purposes.

3.2.4.9 **I/NIBUS Map Registers** - The 512 I/NIBUS Map Registers (bb+'800 - bb+'FFC) are READ/WRITE accessible to the operating system. These registers are initialized by writing zeros to them. VAXBI bus errors do not affect them.

An I/NIBUS Map Register translates an 18-bit I/NIBUS address to a 30-bit VAXBI address. The translation is illustrated in Figure 3-19.

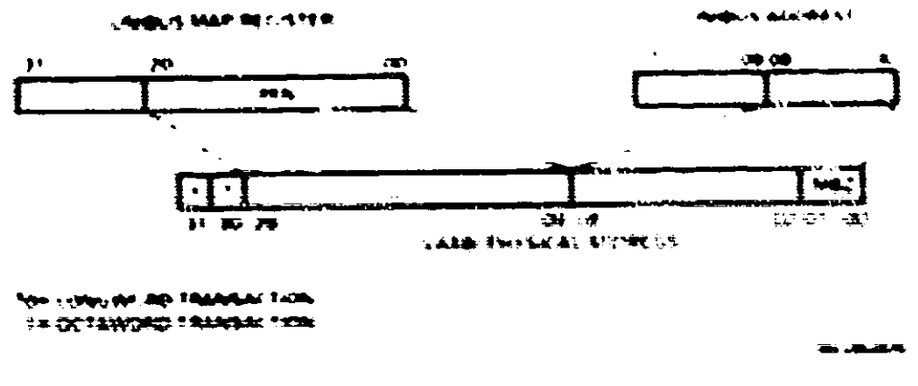


Figure 3-19 I/NIBUS to VAXBI Address Translation

The I/NIBUS Map Register format is shown in Figure 3-20.

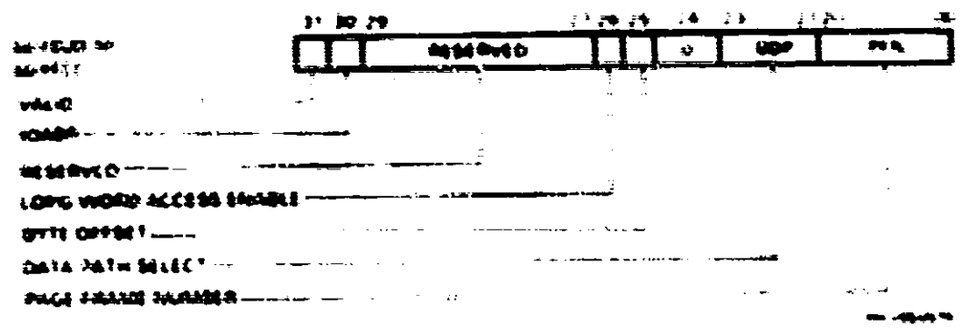


Figure 3-20 I/NIBUS Map Register

VALID <31>	(R/W, DCLOC)	Clearing this bit prevents a UNIBUS transfer from mapping to the VAXBI. A transaction that uses a UNIBUS Map Register with a clear VALID bit does not receive SSYN. When this happens, the IVMR bit in the BUACSR is set and an error interrupt is sent to the VAXBI (if interrupts are enabled).
IOADR <30>	(R/W, DCLOC)	This bit designates I/O address space. When a UNIBUS device initiates a transfer to a UNIBUS Map Register with contents FFFFFFFF (hex), the DWBUA ignores the transfer. That is, the DWBUA does not assert SSYN, does not set the IVMR bit in the BUACSR, and does not cause an interrupt. (The transfer is ignored if the IOADR, VALID, LWAEN, and BYTE OFFSET bits are set and if DPSEL <24:21> is set to 7. If IOADR and VALID are set, but some of the other bits are not set, the DWBUA sets IVMR, causing an interrupt.)
LWAEN <26>	Longword Access Enable (R/W, DCLOC)	When set, this bit specifies that the maximum length of a buffered transaction is one longword. The buffer is purged by an octaword WRITE operation when an aligned longword of data has been collected. When this bit is clear, the buffered transaction depth may be as long as one octaword before the contents are sent to the VAXBI. This bit is ignored when set in a UNIBUS Map Register with the Direct Data Path selected.
BYTE OFFSET <25>	(R/W, DCLOC)	When this bit is set, the UNIBUS address is transferred as if it is incremented by one.
DATA PATH SELECT <24:21>	(R/W, DCLOC)	This 4-bit field determines which of the data paths is used. A 0 in this field selects the Direct Data Path; 1 through 5 correspond to the five Buffered Data Paths. A 6 or a 7 in this field causes the DWBUA to assert the BADMDP bit in the BUACSR. The DWBUA then sends an error interrupt to the VAXBI if interrupts are enabled.
PAGE FRAME NUMBER <20:0>	(R/W, DCLOC)	This 21-bit address field is concatenated with UNIBUS address bits <8:0> to form a 30-bit physical address on the VAXBI.

3.3 INITIALIZATION

3.3.1 DWBUA Hardware Initialization

Upon successful completion of the self-test, all DWBUA internal registers and Buffered Data Path flags are cleared, with the exception of the Data Path Control and Status Registers and the upper 16 UNIBUS Map Registers.

3.3.2 UNIBUS Initialization

The UNIBUS can be initialized in several ways.

1. The DWBUA monitors the UNIBUS AC LO signal. When this signal is asserted, the DWBUA initializes the UNIBUS (that is, the DWBUA clears the UBPUP bit in GPR0, and, if interrupts are enabled, issues an error interrupt). When UNIBUS AC LO is deasserted and UNIBUS initialization is complete, another interrupt is sent if interrupts are enabled.

2. The DWBUA initializes the UNIBUS (that is, the DWBUA INIT) if a processor sets the UPI bit in the BUACSR. Two interrupts are issued if interrupts are enabled.

3. The DWBUA asserts UNIBUS AC LO whenever BI AC LO L is asserted; therefore, a brownout or blackout that affects the VAXBI causes the UNIBUS to be initialized.

4. The DWBUA asserts UNIBUS AC LO when a processor sets the SST bit in the BICSR. This mechanism for initializing the DWBUA also initializes the UNIBUS.

The state diagram for UNIBUS initialization (Figure 3-21) applies to all of the cases above.

During UNIBUS initialization, which takes at least 50 ms, the UBPUP bit in GPR0 (BIIC GPR0 <0>) is cleared by the DWBUA, indicating that UNIBUS power is down. The DWBUA sends an error interrupt to the VAXBI if interrupts are enabled.

During UNIBUS initialization, the DWBUA internal registers are not accessible. The DWBUA sends an ACK in response to all WRITE commands from the VAXBI and ignores the data. All READ commands are acknowledged with zero data. The BIIC registers may be accessed, and they respond normally to all VAXBI transactions. Once power is restored on the UNIBUS, UBPUP is set in GPR0 and the VAXBI is interrupted if interrupts are enabled.

3.4 PROGRAMMING CONSIDERATIONS

3.4.1 UNIBUS Map Registers

The DWBUA register set includes 512 UNIBUS Map Registers. When its VALID bit is set, a UNIBUS Map Register maps one 512-byte page of UNIBUS address space to a page of VAXBI space.

The user must ensure that VALID pages do not correspond to UNIBUS addresses of devices on the UNIBUS. To do this, leave the contents of the upper 16 UNIBUS Map Registers unchanged after DWBUA initialization.

The upper 16 UNIBUS Map Registers are initialized to FFFFFFFF. (If memory is placed on the UNIBUS for special applications, the UNIBUS Map Registers which correspond to that memory should be initialized to FFFFFFFF. This is the responsibility of the applications software.) The DWBUA ignores any transactions involving a UNIBUS Map Register that contains FFFFFFFF.

The lower 496 UNIBUS Map Registers are initialized to zero (also known as invalidated — that is, their VALID bits are cleared) by the DWBUA on receipt of BI DC LO.

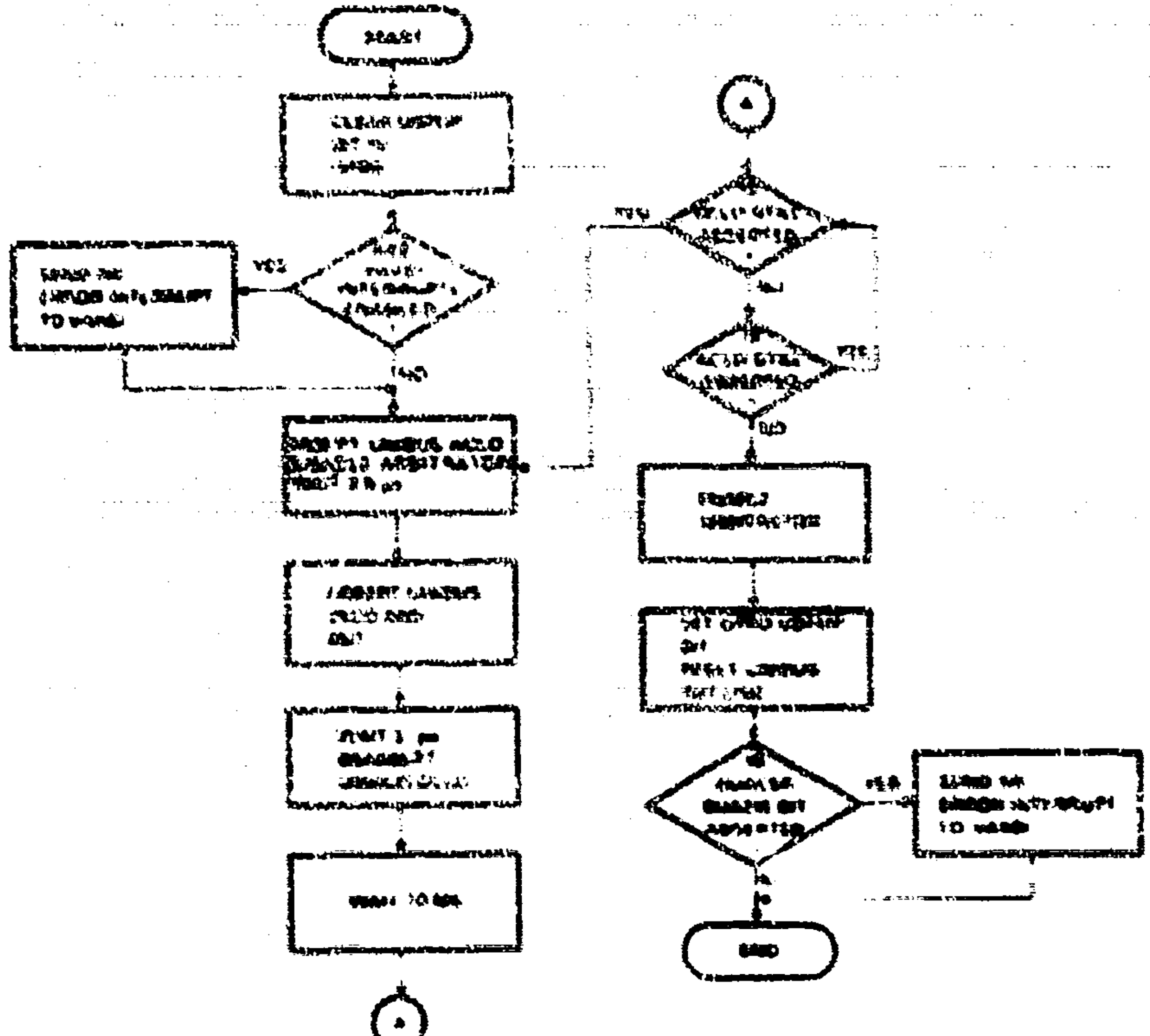


Figure 3-21 UNIBUS Initialization State Diagram

When a UNIBUS device initiates a transfer that corresponds to one of the upper 16 UNIBUS Map Registers, the DWBUA ignores the transfer and expects the UNIBUS device to respond. If a UNIBUS-initiated transfer accesses a UNIBUS Map Register with the VALID, [illegible], and BYTE OFFSET bits asserted and DPN<[illegible]> equal to [illegible], the DWBUA ignores the corresponding UNIBUS transfer.

3.4.1.1 Contiguous Allocation - One or more UNIBUS Map Registers must be allocated for each transfer. When more than one is allocated, the UNIBUS Map Registers must be contiguous in UNIBUS space, since sequential transfers are contiguous in UNIBUS space. This means that the set of UNIBUS Map Registers is contiguous in VAXBI node space. The contents of the UNIBUS Map Registers do not normally point to a contiguous area of VAXBI memory space.

3.4.1.2 Mapping to VAXBI I/O Space - UNIBUS Map Registers can be used to map to VAXBI I/O space, although no reason for doing so is known and many restrictions exist.

A UNIBUS device cannot modify the UNIBUS Map Registers of the DWBUA to which it is connected. An attempt to modify a UNIBUS Map Register results in the UNIBUS device never receiving SSYN. In addition, the DWBUA may hang.

3.4.1.3 BYTE OFFSET Bit - If the BYTE OFFSET bit in the UNIBUS Map Register is set and if the transfer uses n UNIBUS Map Registers, then the BYTE OFFSET bit should be set for all n registers and the n+1th register should be allocated and invalidated. If the n+1th register is VALID when a UNIBUS device issues a DATO with a UNIBUS address corresponding to the last word of the nth page, then two VAXBI WRITEs can occur: one includes the last byte of the nth page, and the other includes the first byte of the n+1th page.

If the BYTE OFFSET bit is not set, it is not necessary to allocate the n+1th UNIBUS Map Register since the DWBUA does not prefetch data from VAXBI memory space.

3.4.2 UNIBUS Power Down

When UNIBUS power goes down, the UNIBUS requires a minimum of 20 ms to complete its power-down/power-up sequence. During this sequence, the DWBUA cannot respond normally to VAXBI transactions. Any attempted access to window space or to node space (except the first 256 bytes, which are in BIIC space) receives ACK. For WRITE commands, the DWBUA ignores the data; for READ commands, the DWBUA returns zero data. Further, the IRCI command does not set the DWBUA adapter [illegible].

3.4.3 Use of Buffered Data Paths

VAXBI memory may be corrupted if a UNIBUS device issues nonsequential DATO(B) transactions through a BDP. In particular, a DATO with UNIBUS address 8*n followed by a DATO with UNIBUS address 8*n-14 causes the entire octaword in the BDP to be written to VAXBI memory space. A DATOB with UNIBUS address 8*n followed by a DATOB with UNIBUS address 8*n-1 has the same effect. This conforms to the standard restriction on UNIBUS devices which use BDPs (sequential transfers only) and causes the programming restrictions described in the next two paragraphs.

UNIBUS Map Registers associated with BDPs must not be double-allocated. A set of UNIBUS Map Registers may be allocated to only one transfer. Concurrently allocating a set of UNIBUS Map Registers to two transfers may cause VAXBI memory space to be corrupted.

A BDP must be purged (by writing one to the PURGE bit in the corresponding DPR/SR) before the UNIBUS Map Registers allocated to a transfer may be allocated to another transfer, and before the contents of the UNIBUS Map Registers may be changed.

After a UNIBUS power outage occurs and power is restored, all of the BDPs must be purged using the PURGE bit in the DPCSRs.

During a UNIBUS (sequential) DATO using a Buffered Data Path transaction, the DWBUA issues SSYN before determining if the corresponding VAXBI transaction is required. (That is, the DWBUA issues SSYN before determining if the buffer is full.) This means that if an error occurs during the VAXBI transfer, the DWBUA cannot report that error to the UNIBUS device. If the transaction is a DATI, the DWBUA completes the corresponding VAXBI transfer before it issues SSYN to the UNIBUS device.

3.4.4 VAXBI Access to the DWBUA Internal Registers

All IRCI transactions to the DWBUA internal registers are treated as READ commands and do not set the interlock on the DWBUA. All UWMCI and WMCI transactions to DWBUA registers are treated as WRITE transactions, and the mask bits are ignored by the DWBUA.

The DWBUA responds with NO ACK to all accesses to the unused register locations in the DWBUA internal register space. A WRITE (or UWMCI or WMCI) transaction to the READ-ONLY registers of the DWBUA also results in a NO ACK response.

3.4.5 Data Length

The DWBUA responds only to VAXBI transactions with a data length of longword. Quadword, octaword, and RESERVED data length transactions result in a NO ACK response.

3.4.6 IRCI/UWMCI Commands

When an IRCI transaction is issued to a DWBUA adapter's window space, the DWBUA first performs a DATIP transaction on the UNIBUS using the address supplied with the IRCI command. The DWBUA then sets its interlock. Once interlocked, the DWBUA responds with RETRY to all transactions issued to DWBUA's window space or node space (except BIIC space) until a UWMCI transaction is received. The DWBUA ignores the address supplied with the UWMCI command. The DWBUA assumes that the UWMCI is addressed to the same word as the IRCI command and performs the DATO(B) to that word address (taking into account the mask bits supplied with the UWMCI data).

3.4.7 UNIBUS DATIP

When a UNIBUS device issues a DATIP, the DWBUA responds with RETRY to any VAXBI transaction issued to DWBUA window space or node space (except BIIC space) until a DATO(B) is sent by the UNIBUS master device.

3.4.8 Hung UNIBUS

If a UNIBUS device hangs the UNIBUS (for example, by not deasserting MSYN), the DWBUA will RETRY any VAXBI transaction issued to DWBUA window space or node space (except BIIC space).

3.4.9 VAXBI Bus Error

If the DWBUA encounters an error on the VAXBI during a DWBUA-initiated transaction, it sets the BI [illegible] bit in the BUACSR. The DWBUA also clears the mask bits and the internal BDP flags, thereby indicating that the buffer is empty for the current BDP. If this error occurs during a WMCI transaction, the [illegible] of the data path for which the VAXBI transaction failed. The DWBUA may withhold SSYN, resulting in SSYN timeout to the UNIBUS device that initiated the transfer.

3.4.10 UNIBUS Devices

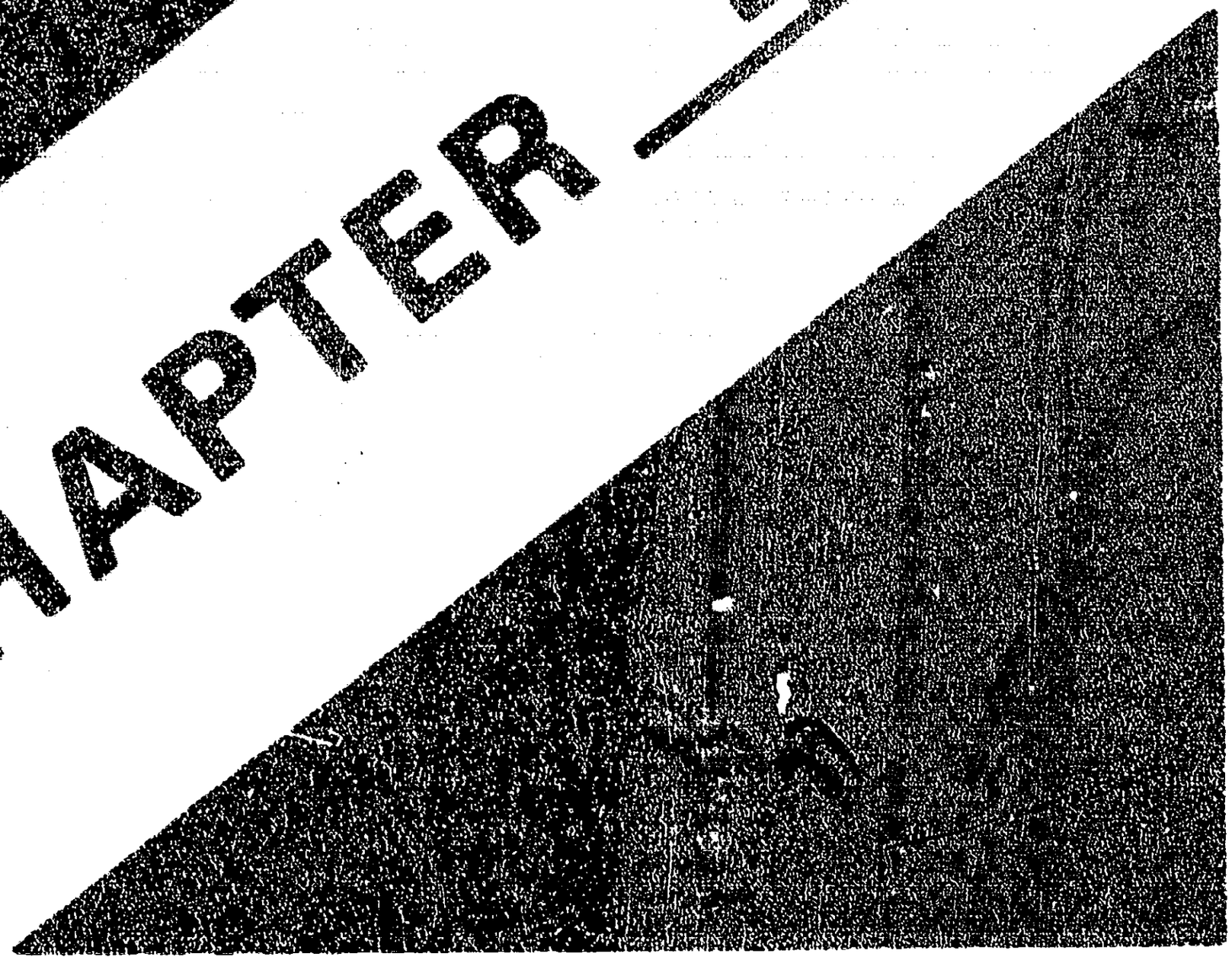
The DWBUA allows those UNIBUS devices that perform data transfers (instead of sending vectors) during the INTR cycle to be attached to the UNIBUS. These devices, however, cause a passive release every time they assert the BR lines to perform a DMA transfer.

3.4.11 Access to Nonexistent Registers

The DWBUA responds with NO ACK to any VAXBI command with an address in unused DWBUA register space. It also responds with NO ACK to WRITE (WCI, WMCI, UWMCI) commands to READ-ONLY registers.

READ transactions to unimplemented BIIC registers read zero data. WRITE (WCI, WMCI, UWMCI) commands to these registers receive an ACK response, but the data is dropped.

CHAPTER 4



CHAPTER 4
FUNCTIONAL DESCRIPTION

4.1 [illegible]

The functional description of the DMA is presented in two parts. In the first part, the components on the block diagram are described. The second part explains the way in which the DMA interfaces between the two buses.

4.2 [illegible]

Figure 4-1 is the DMA's block diagram. Table 4-1 provides functional descriptions of the blocks in Figure 4-1.

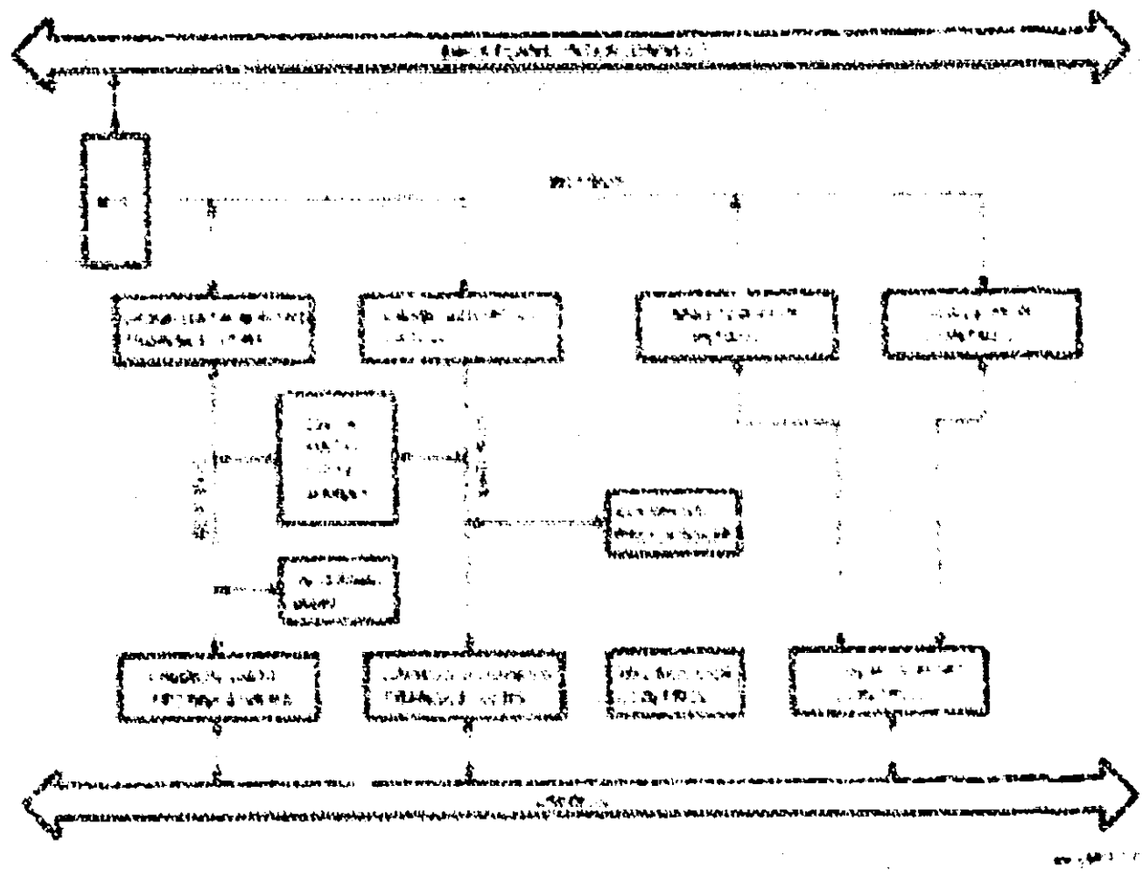


Figure 4-1 [illegible]

Table 4-1 [illegible]

Block	Description
[illegible]	[illegible]
Master Port Control	[illegible]
Slave Port Control	[illegible]
VAX/VME Data and Address Transceivers	[illegible]
VAX/VME Address Latch	[illegible]
[illegible] Data Transceivers	[illegible]
[illegible] Address Transceivers	[illegible]
[illegible] Port Control	[illegible]
Data Path Gate Array	[illegible]

Table 4-1 [illegible] (Continued)

Block	Description
[illegible]	[illegible]
Address Decoder	[illegible]
Miscellaneous Control	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]

4.3 TRANSACTION TYPES

The DWBUA acts as a translator between the VAXBI and the UNIBUS. It interprets commands received from one bus into a format that the other bus can understand, and it provides controls and responses that enable the completion of these commands. These sequences of commands, controls, and responses are called DWBUA transactions. In this section, some typical transactions handled by the DWBUA are examined in detail.

DWBUA transactions are divided into three categories:

- VAXBI-to-DWBUA
- VAXBI-to-UNIBUS
- UNIBUS-to-VAXBI

4.3.1 VAXBI-to-DWBUA Transactions

4.3.1.1 DWBUA Response to VAXBI-to-DWBUA Transactions - The VAXBI sends READ and WRITE commands to the DWBUA. The purpose of these commands is to read data from or to write data to the DWBUA adapter's internal registers. The VAXBI node that initiates the transaction is the VAXBI master, and the DWBUA is the VAXBI slave in all VAXBI-to-DWBUA transactions.

Table 4-2 DWBUA Response to VAXBI-to-DWBUA Transactions

VAXBI-to-DWBUA Transaction	DWBUA Response
READ of DWBUA internal register	1. STALL 2. Register data with read data status code 3. ACK
READ of unused DWBUA register space	NO ACK
WRITE to DWBUA internal register	1. STALL 2. ACK (if no parity error on the VAXBI*) 3. Register updated
WRITE to unused DWBUA register space or READ-ONLY register	NO ACK

* If a parity error occurs, the register is not updated.

4.3.1.2 VAXBI-to-DWBUA Commands -

Table 4-3 VAXBI-to-DWBUA Commands

VAXBI Command	DWBUA Response	Possible Errors	See Note
READ	ACK/RETRY	None	1
IRCI	ACK/RETRY	None	1,2
RCI	ACK/RETRY	None	1
WRITE	ACK/RETRY	Parity Error	1,5
WCI	ACK/RETRY	Parity Error	1,5
WMCI	ACK/RETRY	Parity Error	1,4,5
UWMCI	ACK/RETRY	Parity Error	1,3,5

NOTES FOR TABLE 4-3:

(1) Longword length only.

(2) IRCI commands are accepted, but they are treated as READ commands. The DWBUA does not interlock.

(3) UWMCI commands are accepted, but they are treated as WRITE commands. The DWBUA does not interlock. The mask bits are ignored.

(4) WMCI commands are accepted, but they are treated as WRITE commands. The mask bits are ignored, and the full longword of data is assumed to be valid.

(5) If a parity error occurs on the VAXBI, the DWBUA ignores the transaction.

4.3.1.3 Example: VAXBI WRITE to a UNIBUS Map Register - The VAXBI-to-DWBI A transaction used as an example in this section is a VAXBI WRITE to a UNIBUS Map Register. The purpose of this transaction is for the operating system to set up a UNIBUS Map Register for a future UNIBUS-to-VAXBI transaction. A UNIBUS Map Register corresponds to a block of addresses on the UNIBUS in a future direct memory access (DMA) transaction (not necessarily the one following this transaction). Data will be transferred between this block of UNIBUS addresses and a VAXBI address.

Figure 4-2 is a flow diagram of the VAXBI WRITE to a UNIBUS Map Register transaction. The numbered paragraphs that follow refer to the corresponding numbers on Figure 4-2.

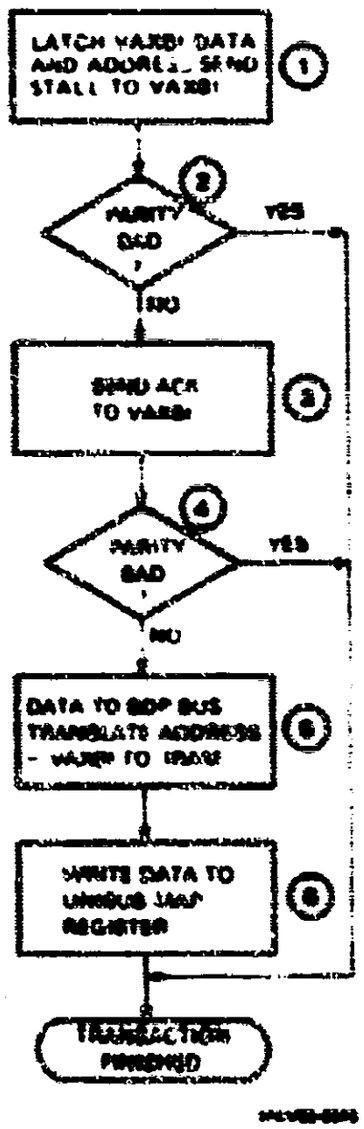


Figure 4-2 VAXBI WRITE to a UNIBUS Map Register Flow Diagram

1. The VAXBI command, address, and data are received by the DWBI A. The slave bus control determines that the transaction is for the DWBI A. The VAXBI address is latched in the VAXBI address latch, and the VAXBI data is latched in the VAXBI data and address transceivers. The VAXBI address is the address of the UNIBUS Map Register that will be written. The VAXBI data will be written into the UNIBUS Map Register.

   The initial DWBI A response to the VAXBI is STALL.

2. The DWBI A checks for a parity error on the VAXBI. If either the data or the command/address has a parity error, the transaction is immediately terminated.

3. The DWBI A responds to the VAXBI with ACK. The VAXBI interprets the transaction as complete.

4. The DWBI A checks for a parity error on the VAXBI. The DWBI A terminates the transaction immediately if the data received in the VAXBI cycle in which ACK was sent has a parity error. The DWBI A issues an error or corrupt to the VAXBI if errors are enabled.

5. The data in the VAXBI data and address transceivers is put onto the BDP bus.

   The VAXBI address is translated into an internal RAM address specifically for the address of the UNIBUS Map Register to be written.

6. The data on the BDP bus is written to the UNIBUS Map Register in the internal RAM. The transaction is complete.

4.3.2 VAXBI-to-UNIBUS Transactions

4.3.2.1 DWBI A Response to VAXBI-to-UNIBUS Transactions - In a VAXBI-to-UNIBUS transaction, the VAXBI master sends to the DWBI A a command that requires the DWBI A to read from or write to a UNIBUS device.

Table 4-4 Bus Masters and Slaves for VAXBI-to-UNIBUS Transactions

Bus	Master	Slave
VAXBI	Node initiating transaction	DWBI A
UNIBUS	DWBI A	UNIBUS device

The DWBI A monitors the UNIBUS BBSY signal before it attempts to perform the DATO(B) transaction on the UNIBUS. If BBSY is deasserted, the DWBI A asserts BBSY and gains UNIBUS mastership. If the DWBI A does not gain UNIBUS mastership within 51 µs, a UNIBUS timeout occurs.

Table 4-5 details the DWBUA responses to three types of VAXBI commands that require DWBUA interaction with devices on the UNIBUS: READ, WRITE (WMCI, WCI), and IRCI/UWMCI.

Table 4-5 DWBUA Responses to VAXBI-to-UNIBUS Transactions

VAXBI-to-UNIBUS Transaction	DWBUA Response
READ	Initial response — STALL Initiates UNIBUS DATI command Continues STALL responses to VAXBI until • SSYN received from UNIBUS slave, or • SSYN timeout occurs (1) Sends to VAXBI • Data from UNIBUS • Read data status code (2) • ACK
WRITE (WMCI, WCI)	Initial response — STALL Checks for parity error on the VAXBI (3) Sends ACK to VAXBI Initiates UNIBUS DATO(B) command (4) Waits for SSYN from UNIBUS device or for SSYN timeout (5)
IRCI/UWMCI	
IRCI	Initial response — STALL Initiates UNIBUS DATIP command Continues STALL responses to VAXBI until • SSYN received from UNIBUS slave, or • SSYN timeout occurs (1) Sends to VAXBI • Data from UNIBUS • Read data status code (2) • ACK Sets interlock (6)
UWMCI (7)	Initial response — STALL Checks for parity error on the VAXBI (8) Sends ACK to VAXBI Releases interlock Initiates UNIBUS DATO(B) command (4,9)

NOTE

When the DWBUA is busy, it sends RETRY to the VAXBI. It does this when:

- **VAXBI attempts access of UNIBUS address space while the DWBUA is processing a UNIBUS transaction, or**
- **Current transaction requires DWBUA mastership of the VAXBI.**

NOTES FOR TABLE 4-5:

(1) The DWBUA does the following in response to a SSYN timeout during a READ transaction:

a. Sends zero data with read data substitute status code to the VAXBI.

b. Sends an ACK response to the VAXBI.

c. Sets the LSSTO bit in the BIACSR.

d. Issues an error interrupt to the VAXBI if interrupts are enabled.

(2) If the UNIBUS PB (parity bad) line is asserted, the DWBUA sends zero data with a read data substitute status code to the VAXBI.

(3) If a parity error has occurred on the VAXBI, the DWBUA terminates the transaction.

(4) The DWBUA issues a DATO or a DATOB depending on the mask bits.

(5) The DWBUA does the following in response to a SSYN timeout during the UNIBUS portion of a WRITE transaction:

a. Sets the LSSTO bit in the BIACSR.

b. Issues an error interrupt to the VAXBI if interrupts are enabled.

(6) After the DWBUA sets its interlock, it sends a RETRY response to all VAXBI commands except LWMCI.

(7) The DWBUA may receive a LWMCI command without having received a preceding IRCI command. When this happens, the DWBUA processes the LWMCI command as a WMCI command.

(8) If the VAXBI command, address or data has a parity error, the corresponding UNIBUS DATO(B) command is not issued, and the DWBUA adapter's interlock is not released, hanging the DWBUA.

(9) The DWBUA assumes that the LWMCI is targeted for the same address as the IRCI and ignores the incoming address.

4.3.2.2 VAXBI-to-UNIBUS Commands -

Table 4-6 VAXBI-to-UNIBUS Commands

VAXBI COMMAND Code	Name	UNIBUS Command Translation	DWBUA Response to VAXBI	Possible Errors	See Note
0000	Reserved	None	NO ACK	None	1
0001	READ	DATI	ACK/RETRY	USSTO	2,12
0010	IRCI	DATIP	ACK/RETRY	USSTO	3,12
0011	RCI	DATI	ACK/RETRY	USSTO	4,12
0100	WRITE	DATO	ACK/RETRY	USSTO	5
				VAXBI PE	12,13
0101	WCI	DATO	ACK/RETRY	USSTO	6
				VAXBI PE	12,13
0110	UWMCI	DATO(B)	ACK/RETRY	USSTO	3,7
				VAXBI PE	12,13
0111	WMCI	DATO(B)	ACK/RETRY	USSTO	7
				VAXBI PE	12,13
1000	INTR	None	NO ACK	None	8
1001	IDENT	BG	ACK/RETRY	NACK	9,14
1010	Reserved	None	NO ACK	None	1
1011	Reserved	None	NO ACK	None	1
1100	STOP	SEE NOTES	ACK	None	10
1101	INVAL	None	NO ACK	None	11
1110	BDCST	None	NO ACK	None	11
1111	IPINTR	None	NO ACK	None	11

NOTES FOR TABLE 4-6:

(1) These codes are reserved by Digital Equipment Corporation for future expansion. The DWBUA responds to these codes with NO ACK.

(2) All VAXBI READs of UNIBUS space are limited to longword length only. VAXBI address bit A<01> determines which word is read from the UNIBUS.

(3) IRCI/UWMCI commands operate as UNIBUS DATIP/DATO(B) sequences. The DWBUA is interlocked by the IRCI command; the UWMCI command releases the interlock. All other READ and WRITE commands directed to the DWBUA receive RETRY responses while the DWBUA is interlocked. Due to UNIBUS constraints, the address supplied with a UWMCI command must be the same as for the IRCI command. Hence, the DWBUA uses the address of the IRCI command while servicing the UWMCI command, ignoring the address supplied with the latter command.

(4) A VAXBI RCI command is treated as a READ command.

(5) VAXBI-to-UNIBUS WRITEs are limited to longword length only. VAXBI address bit A<01> determines which word is written.

(6) A VAXBI WCI command is treated as a WRITE command.

(7) Data length is longword only. VAXBI address bit A<01> determines which word of a longword is written. If either of the two mask bits is not set on the selected word, the DWBUA will respond to the command with ACK. This may corrupt the UNIBUS data or may cause a SSYN timeout. Mask information for the word not selected by VAXBI bit A<01> is ignored by the DWBUA.

(8) Since interrupts are only permitted in the UNIBUS-to-VAXBI direction, the DWBUA responds to all INTR commands with NO ACK.

(9) The DWBUA responds to IDENT commands with a preloaded interrupt vector if present at an appropriate level. If there is no loaded vector, the DWBUA will fetch an interrupt vector from the UNIBUS device by issuing a BG at the corresponding level of the IDENT command.

(10) The STOP command resets all pending interrupts and DMA requests from the UNIBUS. The DWBUA does not reset the contents of any register implemented in the user CSR space. The DWBUA responds to all subsequent VAXBI commands but does not attempt to gain mastership of the VAXBI. The effect of the STOP command is reset only by BI DC LO.

(11) INVAL, BDCST, and IPINTR are ignored by the DWBUA. The DWBUA responds to these codes with NO ACK.

(12) USSTO — The corresponding UNIBUS transaction has resulted in a SSYN timeout. (The DWBUA did not receive SSYN within 19.2 µs after asserting MSYN.) The USSTO bit in the BUACSR is set, and an error interrupt is sent to the VAXBI (if interrupts are enabled).

(13) VAXBI PE — Parity error on the VAXBI. The DWBUA ignores the transaction.

(14) NACK — SACK is not asserted by the interrupting UNIBUS device. The DWBUA sends zero data for the vector.

4.3.2.3 Example: VAXBI READ of UNIBUS Data - The VAXBI-to-UNIBUS transaction used as an example in this section is a VAXBI READ of UNIBUS data. In this transaction, the VAXBI master reads data from a device on the UNIBUS.

Figure 4-3 is a flow diagram of the VAXBI READ of a UNIBUS data transaction. The numbered paragraphs that follow refer to the corresponding numbers in Figure 4-3.

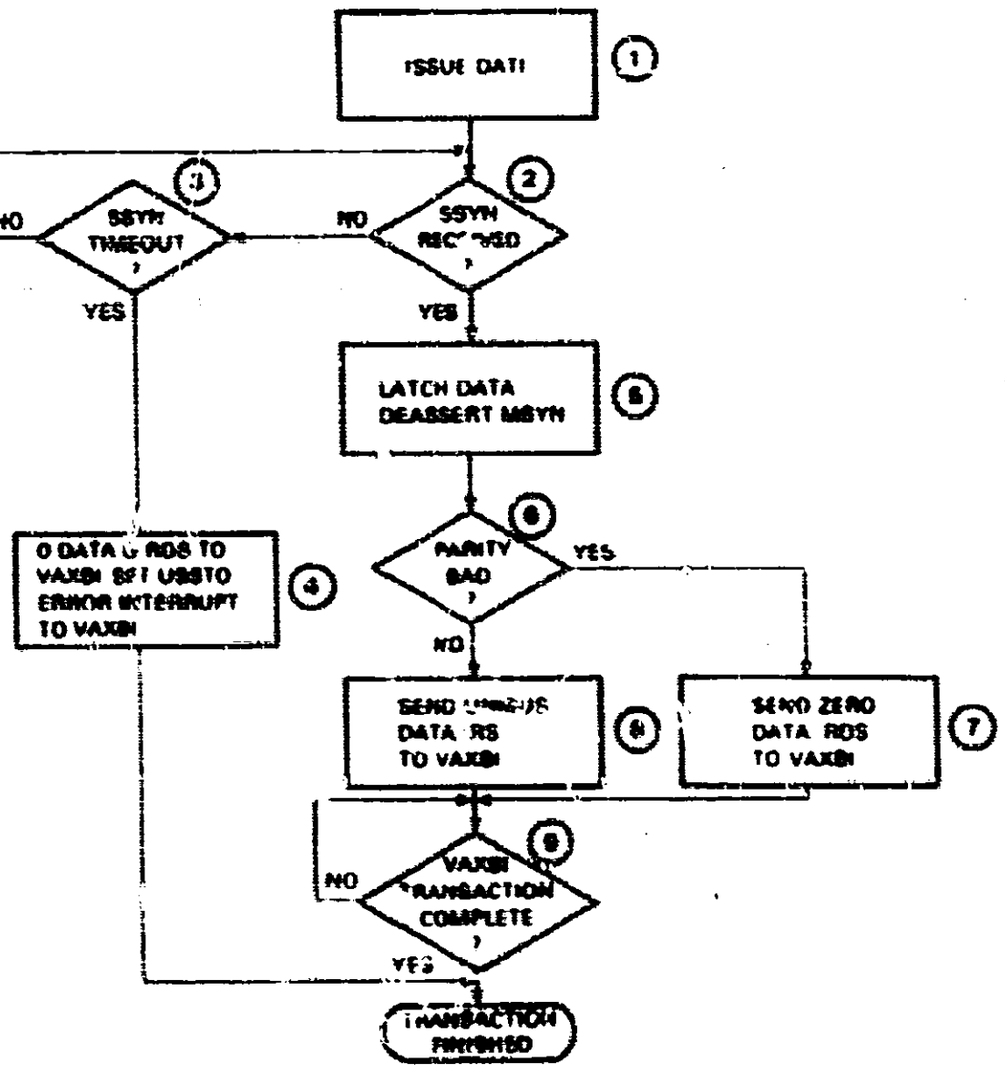


Figure 4-3 VAXBI READ of UNIBUS Data Flow Diagram

(1) The VAXBI command and address are received by the DWBUA. The slave port control determines that the transaction is for the DWBUA. The DWBUA responds to the VAXBI as SLAVE.

The VAXBI address is latched in the VAXBI address latch.

The DWBUA monitors the BBSY signal on the UNIBUS. If it is asserted, the DWBUA waits until it is deasserted. Since the DWBUA is the UNIBUS arbitrator, it has the highest priority on the UNIBUS. When BBSY is deasserted by the present UNIBUS master, the DWBUA asserts BBSY and gains bus mastership.

The DWBUA issues a DATI command. The address in the VAXBI address latch is sent over the BAD bus to the UNIBUS address transceivers. Address and control bits are sent out on the UNIBUS.

The DWBUA asserts MSYN. The data drivers put the data onto the UNIBUS D lines.

(2) The DWBUA monitors SSYN and waits for it to be asserted.

(3) If SSYN is not asserted within [illegible] µs from assertion of MSYN, a SSYN timeout occurs.

(4) SSYN timeout causes the DWBUA to send zero data and RDS to the VAXBI, set the USSTO bit of the BICSR, and issue an error interrupt to the VAXBI if interrupts are enabled. The transaction is terminated.

(5) The UNIBUS slave sends the data and SSYN to the DWBUA. Data is received at the UNIBUS data transceivers.

(6) Parity for the data is checked.

(7) If the data has a parity error, zero data and a read data substitute (RDS) status code are sent to the VAXBI. The RDS status code warns the VAXBI that the data contains an uncorrectable error. The transaction is terminated.

(8) If parity is good, the UNIBUS data is sent over the BDP bus to the VAXBI data transceivers. From there it is sent over the BI bus to the BIIC and out to the VAXBI. A read data status code is sent to the VAXBI, indicating that the data is error free.

(9) When all of the data has been sent to the VAXBI, the DWBUA sends three AC lows to the VAXBI, indicating that the transaction is complete.

4.3.3 UNIBUS-to-VAXBI Transactions

4.3.3.1 DWBUA Response to UNIBUS-to-VAXBI Transactions - In a UNIBUS-to-VAXBI transaction, the UNIBUS master sends a command to the DWBUA that requires the DWBUA to read from or to write to a VAXBI node.

Table 4-7 Bus Masters and Slaves for UNIBUS-to-VAXBI Transactions

Bus	Master	Slave
UNIBUS	Device initiating transaction	DWBUA
VAXBI	DWBUA	VAXBI node

The DWBUA responds to three UNIBUS commands that require DWBUA interaction with other VAXBI nodes: DATI, DATO(B), and DATIP-DATO(B). These responses are listed in Table 4-8. The DWBUA responses to UNIBUS commands are independent of the data path used.

Table 4-8 DWBUA Responses to UNIBUS-to-VAXBI Transactions

UNIBUS-to-VAXBI Transaction	DWBUA Response
DATI (1)	Data (2) SSYN (3)
DATO(B) (4)	SSYN (5) Data to VAXBI (6)
DATIP-DATO(B) (7)	
DATIP (8)	Data (2) SSYN (3)
DATO(B) (9)	SSYN (5) Data to VAXBI (6)

NOTE

If the DWBUA is processing a VAXBI transaction when the UNIBUS request is received, the DWBUA withholds the bus grant until the VAXBI transaction has completed.

NOTES FOR TABLE 4-8

(1) A DATI command from a UNIBUS device reads data from the DWBUA.

(2) If a VAXBI error occurs while the DWBUA is fetching the data from the VAXBI, SSYN is [illegible] withheld. If it is withheld, a SSYN timeout results. The DWBUA sets the [illegible] bit of the BUA CSR and the BIIC issues an error interrupt on the VAXBI if interrupts are enabled.

(3) The DWBUA issues SSYN in response to a DATI command only when the VAXBI slave responds to the VAXBI portion of the transaction with ACK. Any other response from the VAXBI slave results in the DWBUA withholding SSYN.

(4) When the DWBUA processes a DATO(B) command, it accepts data from a UNIBUS device.

(5) The DWBUA issues SSYN before it completes the corresponding VAXBI transaction.

(6) If an error occurs while the DWBUA is writing the data to the VAXBI node, the DWBUA sets the [illegible] bit of the BUA CSR, and the BIIC issues an error interrupt on the VAXBI if errors are enabled. SSYN may be withheld from the UNIBUS device; withholding SSYN results in an SSYN timeout.

(7) The DATIP-DATO(B) command sequence may be performed only through the DWBUA adapter's Direct Data Path. An attempt to perform this command sequence through a Buffered Data Path results in an SSYN timeout. The BYTE OFFSET bit in the UNIBUS Map Register corresponding to the Direct Data Path is ignored and treated as if it is clear. If the bit is set, the command is executed as if the bit is clear.

(8) A SSYN timeout occurs if a DATIP through the Direct Data Path results in [illegible] the VAXBI.

(9) UNIBUS protocol requires that a DATIP be followed immediately by a DATO(B) command. BBSY and the address lines must not be deasserted between the two commands. Any deviation from this causes the DWBUA to set the [illegible] bit of the BUA CSR. If a DATO(B) is received but a VAXBI failure occurs during the [illegible] that is generated, then the [illegible] bit of the BUA CSR is set. Each of these errors causes an error interrupt on the VAXBI if interrupts are enabled.

4.3.3.2 UNIBUS-to-VAXBI Commands Through the Direct Data Path

NOTE.
A complete description of data path operation can be found in Appendix I.

Table 4-9 UNIBUS-to-VAXBI Commands Through the Direct Data Path

UNIBUS Command	UNIBUS Address <1>	Command to VAXBI	Transfer Length	Possible Errors	See Note
BYTE OFFSET BIT = 0					
DATI	ANY	READ	LONGWORD	A, B	4
DATIP	ANY	IRCI	LONGWORD	A, B, C	1,4
DATO	ANY	WMCI or UWMCI	LONGWORD	A, B	2,4
DATOB	ANY	WMCI or UWMCI	LONGWORD	A, B	4
BYTE OFFSET BIT = 1					
DATI	ANY	READ	LONGWORD	A, B	3,4
DATIP	ANY	N/A	N/A	N/A	1
DATO	ANY	WMCI	LONGWORD	A, B	3,4
DATOB	ANY	WMCI	LONGWORD	A, B	4

NOTES FOR TABLE 4-9:

(1) A DATIP command is valid only through the Direct Data Path. If a DATIP is attempted through a Buffered Data Path or through the Direct Data Path with the BYTE OFFSET bit set, the UNIBUS command is ignored and the DWBUA does not send SSYN. This causes an SSYN timeout. During this time, all VAXBI transactions to the DWBUA receive a RETRY response until the UNIBUS device negates BBSY.

If a DATIP command is not followed by a DATO(B), the DWBUA sets the UIE bit of the BUACSR and forces an error interrupt (if interrupts are enabled).

(2) All UNIBUS DATO(B)s through the Direct Data Path translate to a longword WMCI transaction with the mask bits set for each valid data byte.

(3) The DWBUA performs two longword transactions on the VAXBI for a [illegible] length transfer through the Direct Data Path if both the BYTE OFFSET bit and UNIBUS address bit A<1> are set.

(4) Possible Errors

(A) BIE — The VAXBI transaction has returned an error code that the DWBUA recognizes as an error code (RTO, RDSR, [illegible]). The BIE bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled. The DWBUA then withholds SSYN, resulting in an SSYN timeout to the UNIBUS device that initiated the transfer.

(B) IMR — The VALID bit is not set in the UNIBUS Map Register for the incoming UNIBUS address. The IMR bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled.

(C) UIE — The UNIBUS master deasserted BBSY after the DATIP without issuing the accompanying DATO(B). The UIE bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled.

4.3.3.3 A sample DATOB Using the Direct Data Path - In this transaction the I-NIBS master writes data to a VAXBI node. The data is not temporarily stored in a BDP buffer, as it is during a Buffered Data Path transaction, instead, it goes directly to the VAXBI.

Figure 4-4 is a flow diagram of the DATOB using the Direct Data Path transaction. The numbered paragraphs that follow refer to the corresponding numbers on Figure 4-4.

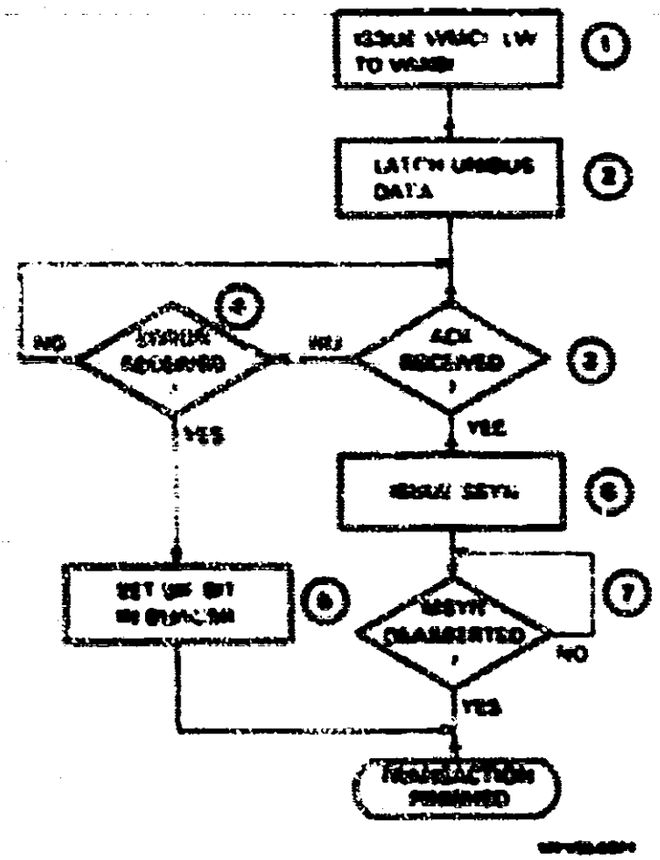


Figure 4-4 DATOB Using the Direct Data Path Flow Diagram

(1) The I-NIBS master sends the address, control lines, and data to the DWBI-A and it then asserts MSYN. The DWBI-A decodes the control lines and determines that the command is a DATOB.

The DWBI-A requests the VAXBI and starts a WRITE LW (write mask with cache invalidate longword) transaction. This is the VAXBI transaction that corresponds to a I-NIBS DATO. The mask bits are determined by the command (DATO or DATOB). The I-NIBS address is longword aligned.

(2) The I-NIBS data is latched on the I-NIBS data transceivers.

The data goes from the I-NIBS data transceivers to the BDP bus through the VAXBI data transceivers and to the VAXBI.

(3) The VAXBI slave sends ACK to the DWBI-A indicating that it has received the data. After ACK is received, the BDP sends the DWBI-A a master transaction complete signal.

(4) If ACK is not received, the DWBI-A looks for an error.

(5) If an error is received, the BIT bit in the BI_MCSR is set and the transaction is terminated. SSYN may not be issued, resulting in an MSYN timeout.

(6) The DWBI-A issues SSYN completing the I-NIBS transaction.

(7) The DWBI-A monitors MSYN. When it is deasserted, the VAXBI transaction is complete.

4.3.3.4 UNIBUS-to-VAXBI Commands Through a Buffered Data Path -

Table 4-10 UNIBUS-to-VAXBI Commands Through a Buffered Data Path

UNIBUS Command	UNIBUS Address <3:0>	Buffer Status	Command to VAXBI	Transfer Length	Possible Errors	See Notes
BYTE OFFSET BIT = 0						
DATI	ANY	EMPTY	READ	OCTAWORD	B, C, D	[illegible]
DATI	ANY	IN/M	NONE	N/A		[illegible]
DATI	ANY	IN/D	READ	OCTAWORD	B, C, D	[illegible]
DATI	ANY	OUT	WMCI or READ	OCTAWORD	B, C, D	[illegible]
DATIP	ANY	N/A	N/A	N/A		[illegible]
DATO	ANY	IN or EMPTY	WMCI	OCTAWORD	B, C, D	[illegible]
DATO	ANY	OUT/M	WMCI	OCTAWORD	B, C, D	[illegible]
DATO	ANY	OUT/D	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	IN or EMPTY	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	OUT/M	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	OUT/D	WMCI	OCTAWORD	B, C, D	[illegible]
BYTE OFFSET BIT = 1						
DATI	0 to C	EMPTY	READ	OCTAWORD	A, B, [illegible]	[illegible]
DATI	0 to C	IN/M	NONE	N/A		[illegible]
DATI	0 to C	IN/D	READ	OCTAWORD	A, B, D	[illegible]
DATI	0 to C	OUT	READ	[illegible]	A, B	[illegible]
DATI	E	EMPTY	READ	OCTAWORD	A, B, D	[illegible]
DATI	E	IN/M	READ	OCTAWORD	A, B, D	[illegible]
DATI	E	IN/D	READ	OCTAWORD	A, B, D	[illegible]
DATI	E	OUT	READ	[illegible]	A, B	[illegible]
DATIP	ANY	N/A	NONE	N/A		[illegible]
DATO	0 to C	IN or EMPTY	NONE	N/A		[illegible]
DATO	0 to C	OUT/M	NONE	N/A		[illegible]
DATO	0 to C	OUT/D	WMCI	OCTAWORD	B, C, D	[illegible]
DATO	E	IN or EMPTY	WMCI	OCTAWORD	B, C, D	[illegible]
DATO	E	OUT/M	WMCI	OCTAWORD	B, C, D	[illegible]
DATO	E	OUT/D	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	IN or EMPTY	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	OUT/M	WMCI	OCTAWORD	B, C, D	[illegible]
DATOB	ANY	OUT/D	WMCI	OCTAWORD	B, C, D	[illegible]

NOTES FOR TABLE 4-10

(1) This special case is [illegible] from other Buffered Data Path transfers [illegible] SSYN. [illegible] DATI word is fetched by performing a [illegible] through the Direct Data Path. [illegible] buffer [illegible] READ through the BDP. [illegible] during this transaction.

(2) A DATIP transaction is valid only through the DDP.

(3) A UNIBUS DATI command through a Buffered Data Path results in an octaword READ of VAXBI space, if the requested data is not in the BDP buffer. If the UNIBUS data is stored in the BDP buffer, however, the buffer must be purged by performing an octaword WMCI on the VAXBI before reading the data from the VAXBI. The entire octaword is loaded into the buffer; subsequent accesses within the octaword through the same Buffered Data Path cause the DWBUA to fetch the data from the buffer, with no VAXBI transaction required.

(4) Data for a DATO(B) command through a BDP is stored until the buffer is full. The DWBUA then performs a VAXBI octaword WRITE [illegible] if the buffer contains an entire octaword of valid data from the UNIBUS device. A VAXBI octaword WMCI is performed if the buffer contains less than a complete octaword of valid data.

(5) Possible Errors

(A) BE — The VAXBI transaction has returned an error code that the DWBUA recognizes as an error code: [illegible]. The BE bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled. The DWBUA [illegible] SSYN, resulting in an SSYN timeout for the UNIBUS device that initiated the transfer.

(B) IMR — The VALID bit is not set in the UNIBUS Map Register for the incoming UNIBUS address. The IMR bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled.

(C) UIE — The UNIBUS master deasserted [illegible] after the DATIP before executing the [illegible] DATO(B). The UIE bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled.

(D) [illegible] — The UNIBUS Map Register that corresponds to the incoming UNIBUS address [illegible] in the BDP SEL field [illegible] attempting to select Buffered Data Path [illegible]. The [illegible] bit is set in the BUACSR and an error interrupt is sent to the VAXBI if interrupts are enabled.

(6) Buffer states

IN/M — The BDP buffer contains the UNIBUS DATI data received from the VAXBI, and the addresses match.

IN/D — The BDP buffer contains the UNIBUS DATI data received from the VAXBI, and the addresses do not match.

OUT — The BDP buffer contains the UNIBUS DATO data to be sent to the VAXBI.

EMPTY — The BDP buffer is empty.

(7) The command to the VAXBI is sent after SSYN is issued.

(8) The command to the VAXBI may be sent after SSYN is issued.

[illegible] Example [illegible] Using a Buffered Data Path – In this transaction the [illegible] master writes data to a [illegible] node. Each [illegible] writes two bytes of data into a [illegible] buffer. The [illegible] buffer can hold [illegible] bytes [illegible] buffer. The buffer [illegible] node.

Figure 4-[illegible] is a flow diagram of the [illegible] using a Buffered Data Path transaction. The numbered paragraphs that follow refer to the corresponding numbers in Figure 4-[illegible].

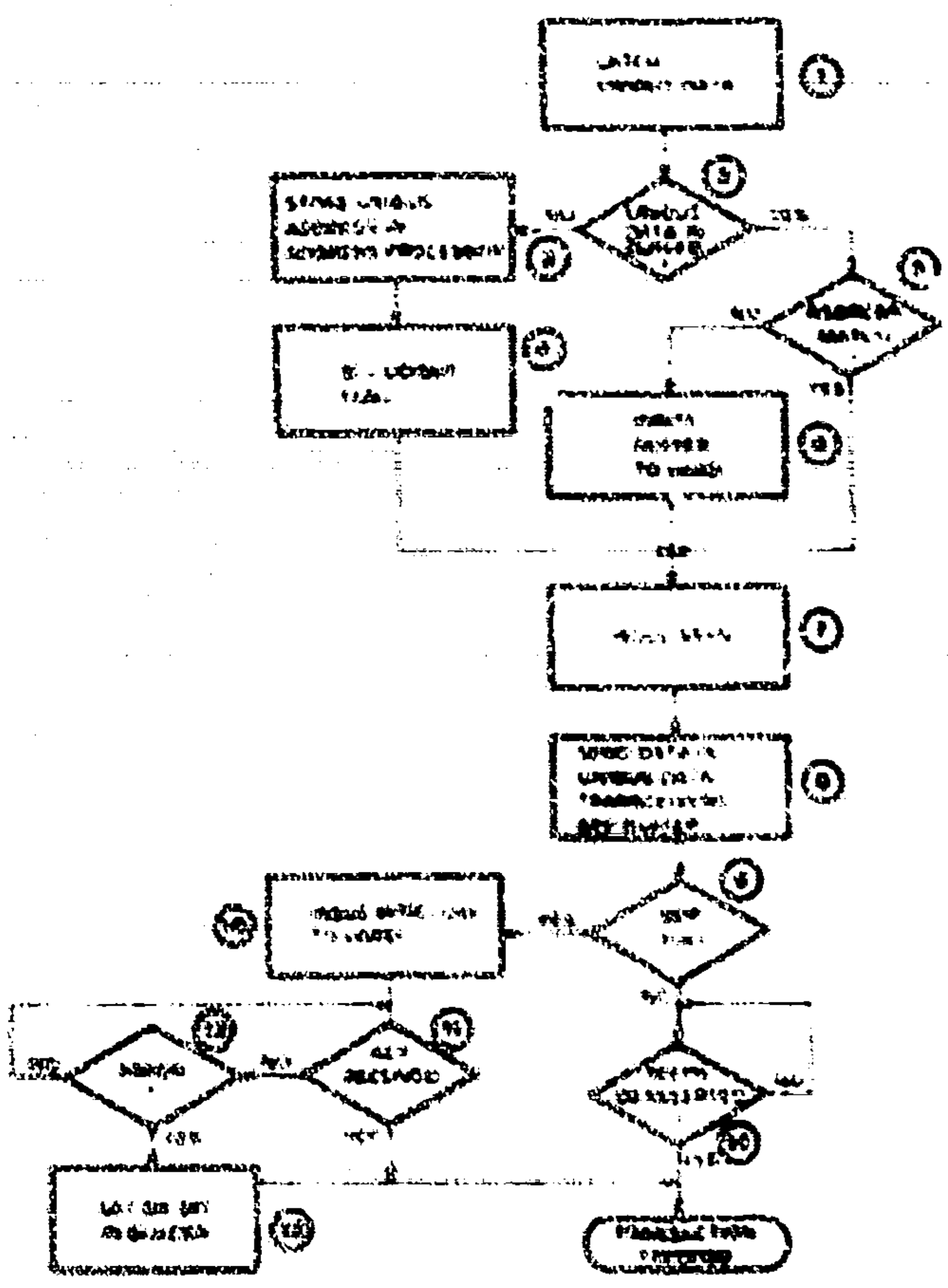


Figure 4-[illegible] [illegible] Using a Buffered Data Path Flow Diagram

1. The [illegible] master sends address, control bits, and data to the [illegible] and then asserts MSYN. The two bytes of [illegible] data are latched in the [illegible] data transceivers.
2. The [illegible] bit in the Data Path Control and Status Register is checked.
3. If the [illegible] bit is clear, the [illegible] address goes over the DAD bus to the address processor where it is stored.
4. The [illegible] sets the [illegible] bit, indicating that [illegible] data is stored in the [illegible] buffer.
5. If the [illegible] bit is set, the [illegible] determines if the present data is part of the same [illegible] as the data already in the [illegible] buffer. To determine if the present data is part of the same [illegible] bits [illegible] of the address stored in the address processor are compared with the incoming [illegible] address.
6. If the compared addresses do not match, the selected [illegible] buffer is [illegible]. That is, the data in the [illegible] buffer is [illegible] to the [illegible] with an [illegible] command. In this way, the [illegible] ensures that the existing data is not overwritten or lost.
7. The [illegible] asserts SSYN, completing the [illegible] portion of the transaction.
8. The two bytes of data [illegible] over the [illegible] bus to the [illegible] buffer [illegible] within the [illegible].
9. The [illegible] checks the [illegible] buffer [illegible].
10. If the [illegible] buffer is full, the [illegible] becomes the [illegible] master and sends the contents of the [illegible] buffer to the [illegible]. The [illegible] used [illegible] whether all the data in the [illegible] buffer is valid:

a. [illegible]
b. [illegible]

The [illegible] buffer. After the transaction is complete, the [illegible] the [illegible] for the [illegible] buffer.

11. The [illegible] waits for the [illegible] slave node to assert [illegible], ending the transaction.
12. If [illegible] is not received, the [illegible] for an error [illegible].
13. If an error has occurred on the [illegible], the [illegible] sets the [illegible] bit in the [illegible] and the transaction is terminated.
14. The [illegible] waits until MSYN is deasserted by the [illegible] master and then it ends the transaction.

4.3.2.6 Example: DATI Using a Buffered Data Path – In this transaction the UNIBUS master reads data from a VAXBI node. The VAXBI node writes [illegible] of data to a BDP buffer. This buffer is read by the UNIBUS device two bytes at a time, so eight DATI transactions are carried out to read the entire buffer.

Figure 4-6 is a flow diagram of the DATI using a Buffered Data Path transaction. The numbered paragraphs that follow refer to the corresponding numbers in Figure 4-6.

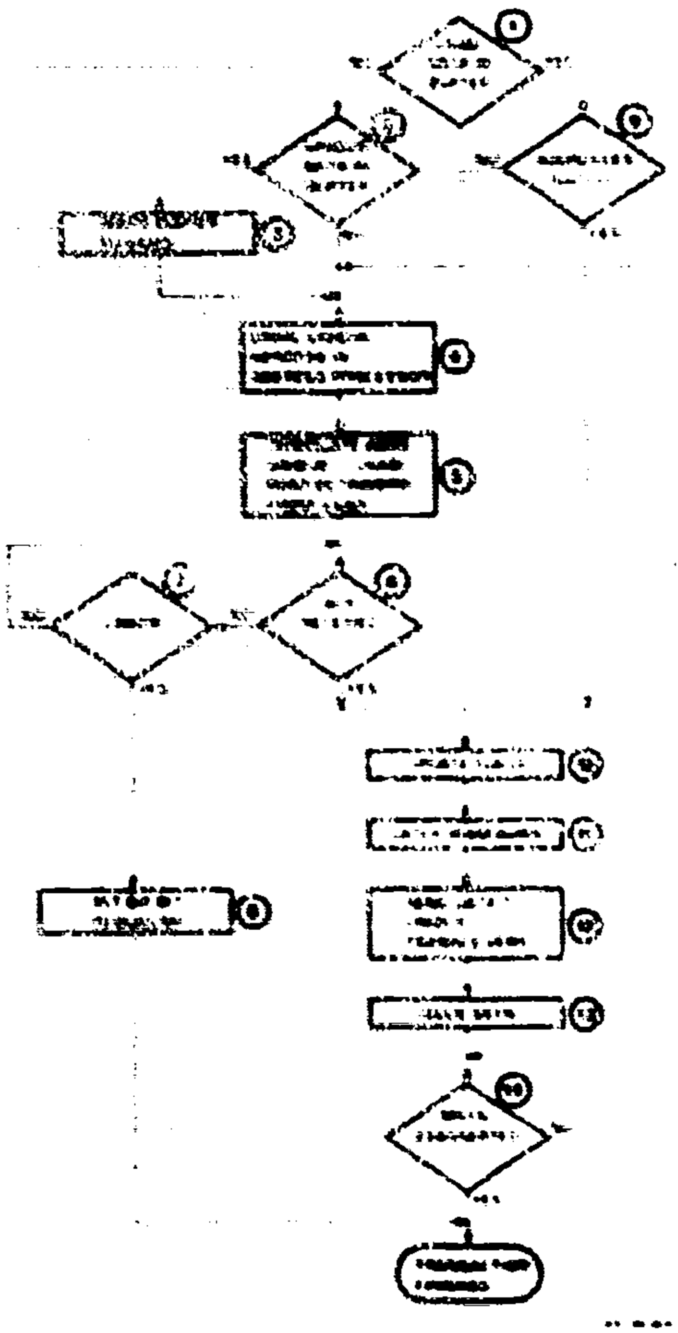


Figure 4-6 DATI Using a Buffered Data Path Flow Diagram

1. The DWBUA checks the BDPBF bit in the Data Path Control and Status Register.
2. If the BDPBF bit is clear, the BDP buffer does not contain VAXBI data. The UDBPF bit is tested.
3. If the UDBPF bit is set, the BDP buffer contains UNIBUS data. The buffer contents are [illegible].
4. The UNIBUS address is stored in the address processor.
5. The UNIBUS address is translated into a VAXBI address. A VAXBI READ is initiated and an octaword of data is returned by the VAXBI slave. The data goes into the BDP buffer.
6. The DWBUA waits for the VAXBI slave node to return ACK.
7. If ACK is not received, the DWBUA looks for an error code.
8. If an error occurred on the VAXBI, the BIE bit in the BUACSR is set and the transaction is terminated.
9. If the BDPBF bit in the DPCSR is set, bits <17:4> of the address stored in the address processor are compared with the UNIBUS address latched in the UNIBUS address transceivers.
10. BDPBF and UDBPF bits are updated.
11. The UNIBUS address (from the address processor) is latched.
12. The requested data word goes from the BDP buffer and is latched in the UNIBUS data transceivers.
13. The DWBUA asserts SSYN.
14. The DWBUA waits for MSYN to be deasserted by the UNIBUS master. When MSYN is deasserted, the transaction is finished.

4.4 REPRESENTATIVE TIMING DIAGRAMS

The timing diagrams in this section represent typical DWBUA transactions. The following assumptions apply:

1. No errors occur during the transaction.
2. The transaction follows a straight-line path through the flows.
3. No time scale is employed. The diagrams indicate relative timing only.

In the following diagrams, the device name that appears in parentheses under the assertion is the device that asserts that signal.

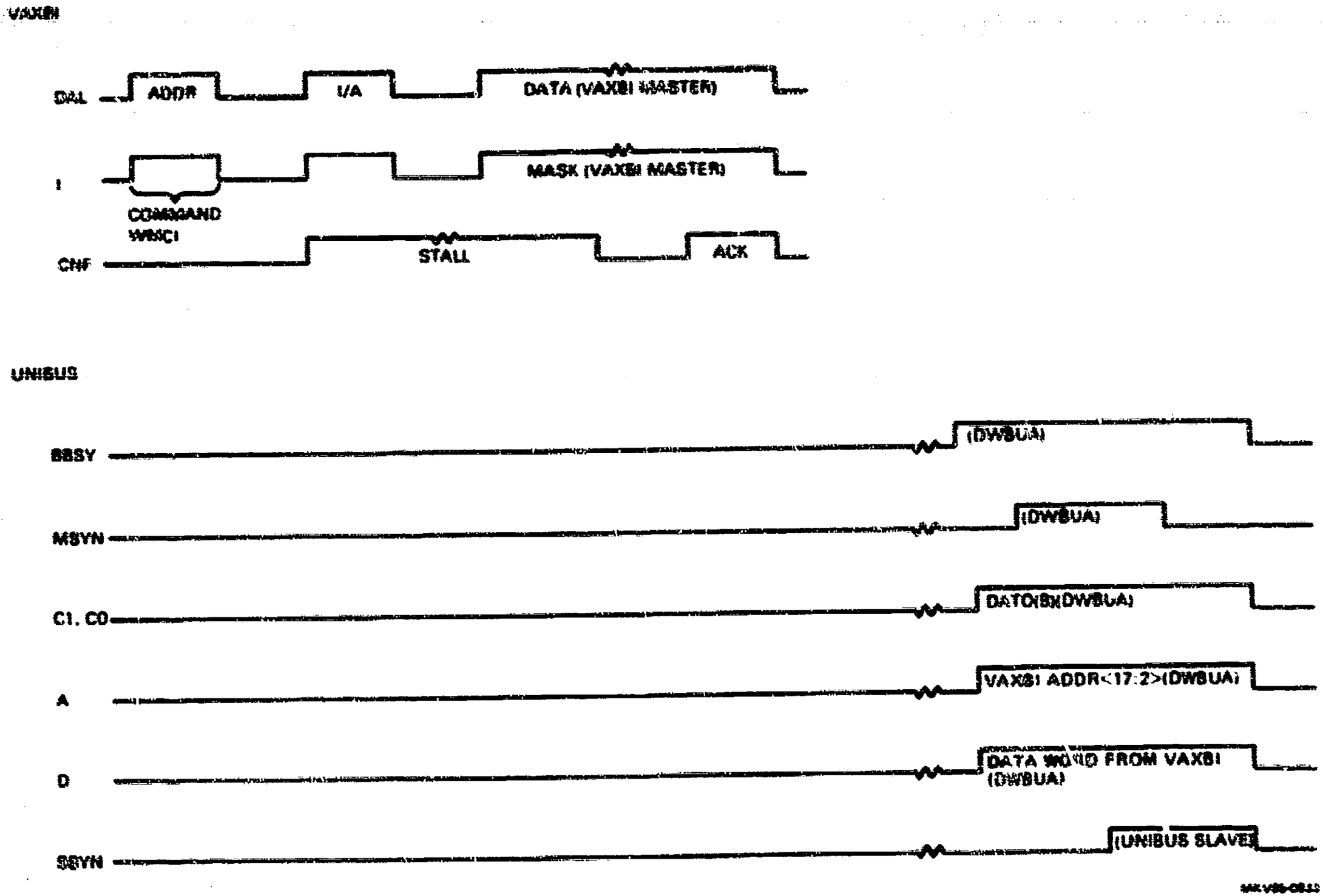


Figure 4-7 VAXBI-to-UNIBUS WRITE Timing Diagram

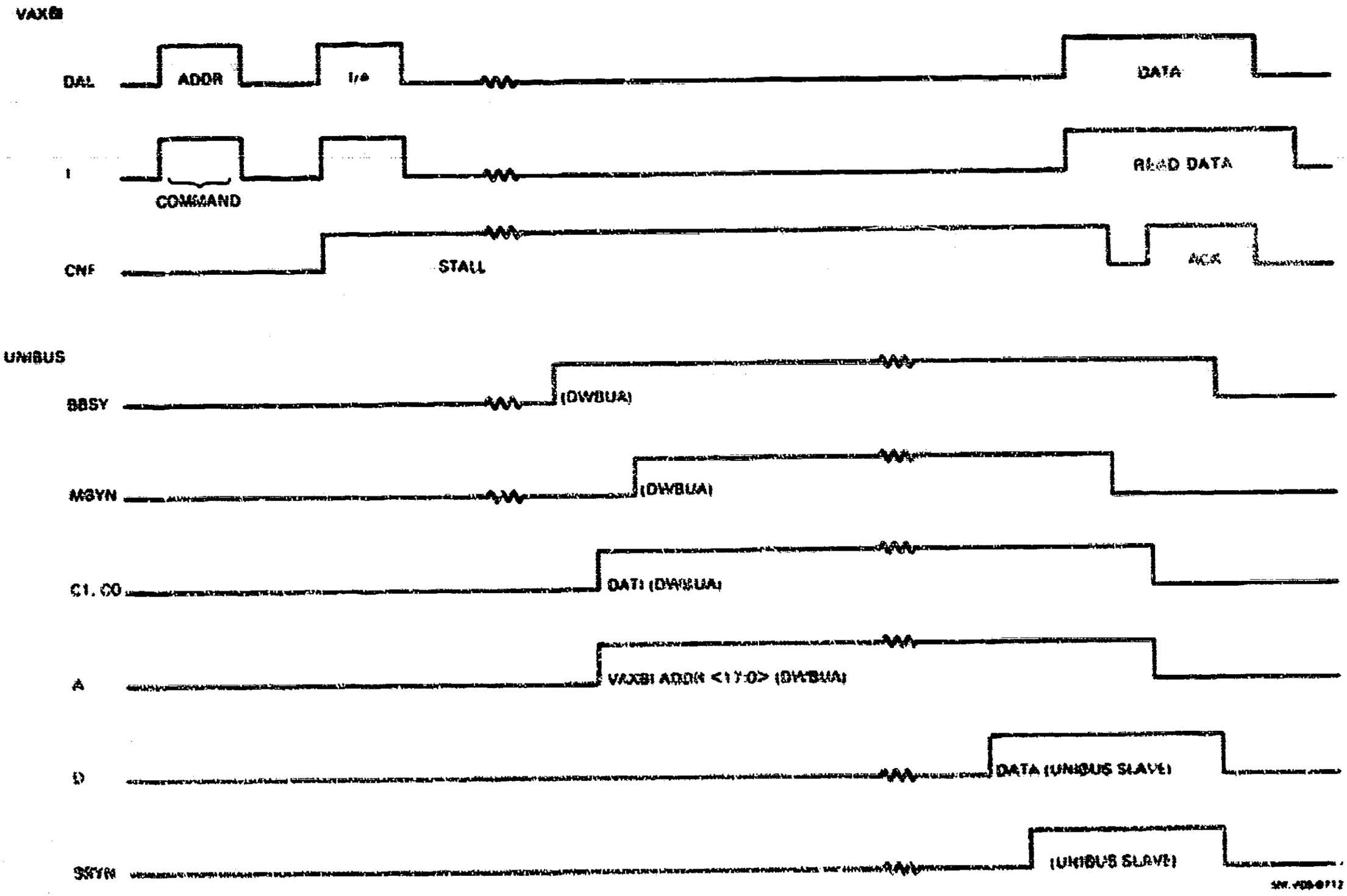


Figure 4-8 VAXBI-to-UNIBUS READ Timing Diagram

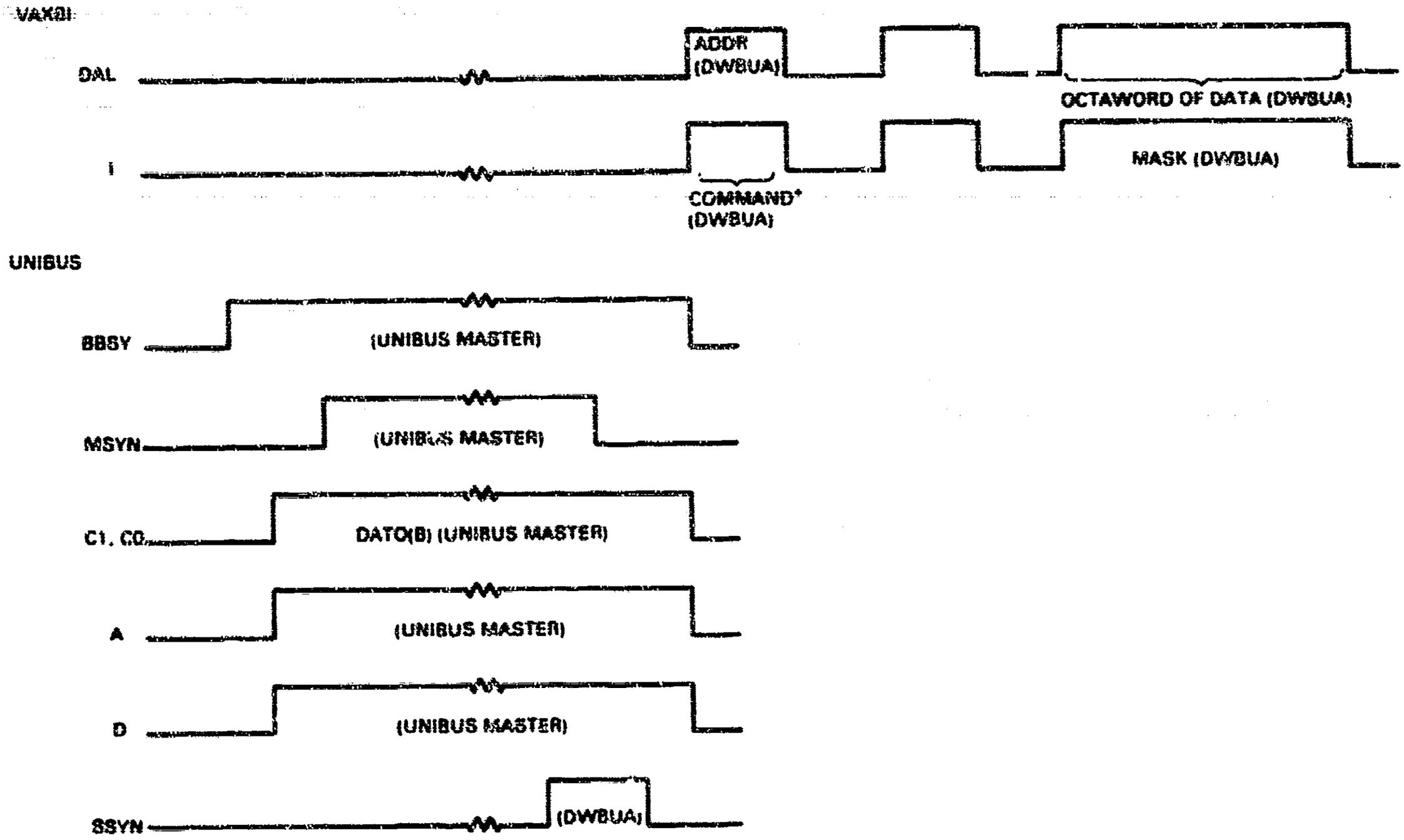


Figure 4-9 DATO(B) Through a Buffered Data Path Timing Diagram

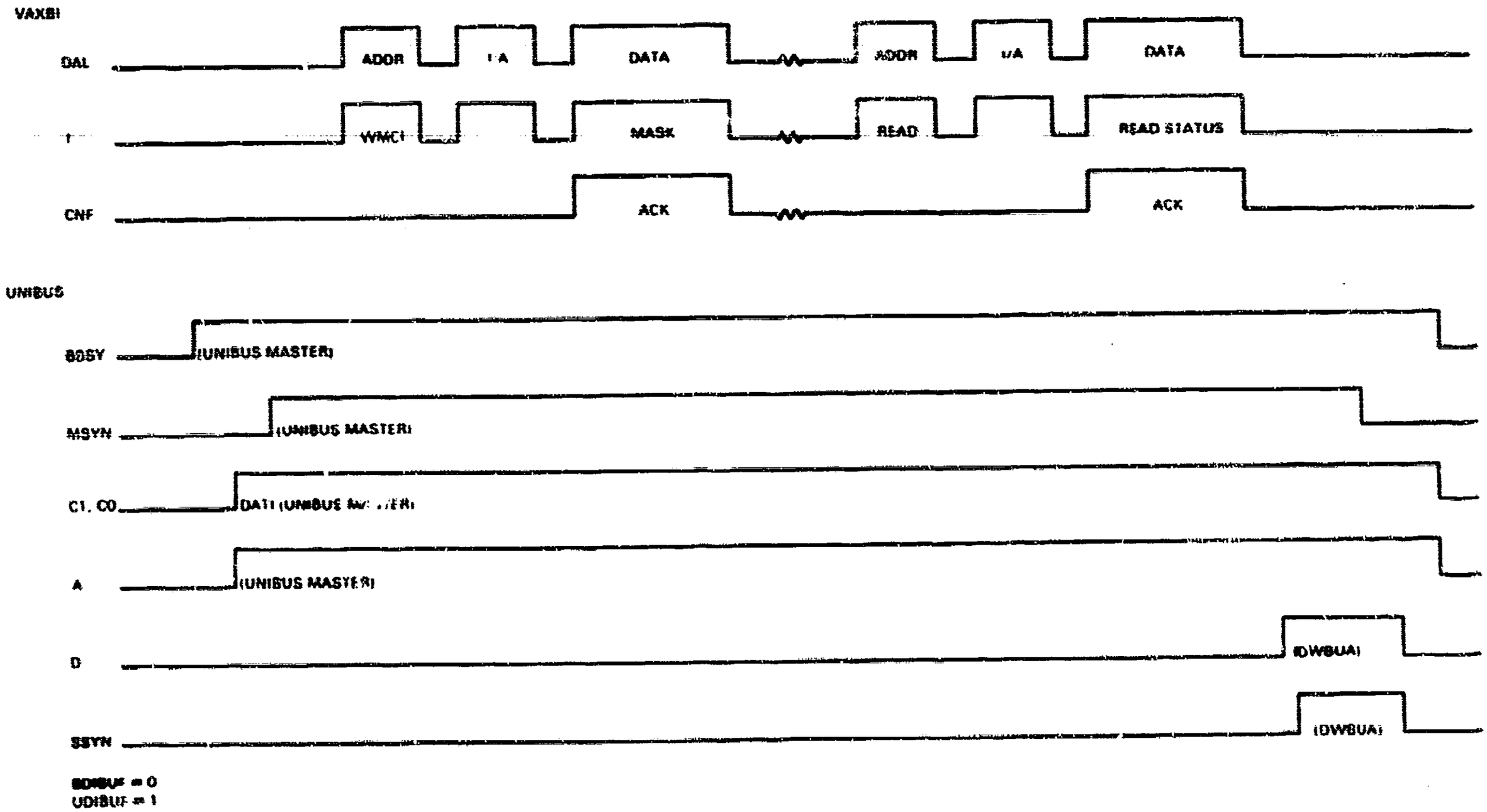


Figure 4-10 DATI Through BDP with Autopurge Timing Diagram

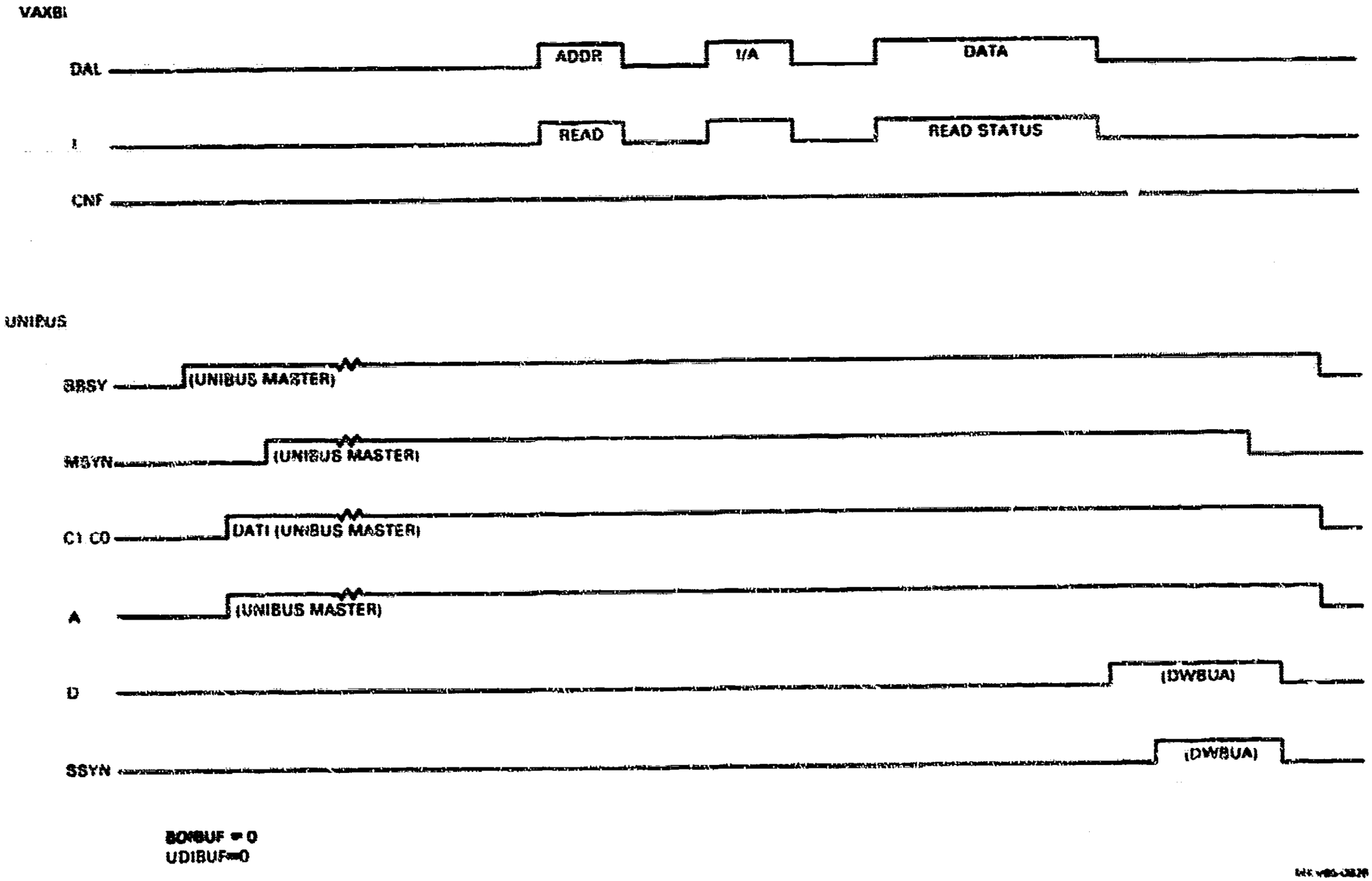


Figure 4-11 DATI Through BDP Timing Diagram

APPENDIX A

APPENDIX A
DWBUA-SUPPORTED UNIBUS DEVICES

A DWBUA UNIBUS configuration supports a subset of the available UNIBUS devices. The following devices cannot be put on a DWBUA-controlled UNIBUS:

- Any PDP-11 processor
- Any device that attempts to perform UNIBUS arbitration
- Any device that has an SSYN timeout period of less than 20 µs

Any device that issues MSYN after using a BR to arbitrate for the UNIBUS may not work satisfactorily.

Contact the local DIGITAL software office for a list of currently supported devices.

APPENDIX B

APPENDIX B
GLOSSARY

ACK Acknowledge. As a VAXBI command response, ACK indicates that the VAXBI slave acknowledges that it is capable of executing the command at this time. As a VAXBI data response, ACK indicates that no error has been detected and that the cycle is not to be STALLed.

AUTOPURGE The act of writing the contents of a partially filled DWBUA BDP buffer to the VAXBI. A buffer is autopurged when it is partially filled with UNIBUS data and one of the following occurs: a DATI is requested through the same BDP or a DATO(B) is requested and its address is not within the same octaword as the data currently stored in the buffer. Data is written from the buffer using a VAXBI octaword WMCI command with the predicted mask bits set for each valid data byte.

BAD DWBUA Buffered Address.

BASE ADDRESS The starting address of a VAXBI node's node space.

BB Base address.

BBSY Bus Busy, a UNIBUS signal. This signal is sent by the bus master to all other bus devices to indicate that the bus is in use.

BCI VAXBI Chip Interface. This is a synchronous interface bus that provides for all communication between the BIIC and the DWBUA.

BDCST Broadcast, a VAXBI command. This command announces a significant event without incurring the overhead of an interrupt. The use of this command is reserved to Digital Equipment Corporation.

BDP DWBUA Buffered Data Path.

BIIC Backplane Interconnect Interface Chip. This chip is a general purpose interface to the VAXBI.

BUACSR DWBUA Control and Status Register, a DWBUA internal register.

DATI Data In, a UNIBUS command. This command requests a transfer of data from the UNIBUS slave to the UNIBUS master. The transfer is always word length.

DATIP Data In Pause, a UNIBUS command. DATIP is identical to DATI except DATIP informs the UNIBUS slave that the present transfer is the first part of a read-modify-write cycle. DATIP must be followed by DATO(B) to the same word address.

DATO(B) Data Out (Byte), a UNIBUS command. This command transfers a word (DATO) or byte (DATOB) of data from the UNIBUS master to the UNIBUS slave.

DDP DWBUA Direct Data Path.

DMA - Direct Memory Access

DPCSR - Data Path Control and Status Register; a DWBUA internal register

DWBUA - VAXBI to UNIBUS Adapter

FUBAR - Failed UNIBUS Address Register; a DWBUA internal register

IDENT - Identify; a VAXBI command. This command is used by processors and other intelligent interrupt fielding nodes to obtain vector information.

INTERLOCK - A mechanism in the DWBUA that locks out transactions while waiting for a specific command. It is used when the DWBUA receives an IRCI from the VAXBI or a DATIP from the UNIBUS. It locks out all other transactions (except STOP from the VAXBI) until it receives the UWMCI or the DATO(B) that completes the current transaction.

INTR - Interrupt; a VAXBI command. This command signals interrupts to other nodes on the VAXBI.

INVAL - Invalidate; a VAXBI command. This command from a processor or another intelligent node signals to other nodes that they may have in their caches data that is no longer valid.

IPINTR - Interprocessor interrupt; a VAXBI command. This command is used by a processor to interrupt another processor or an intelligent adapter.

IRAM - DWBUA Internal RAM

IRCI - Interlock READ with Cache Intent; a VAXBI command. The data READ from the slave is placed in the master's cache. This is the first part of a read-modify-write cycle. IRCI must be followed by UWMCI.

LWAEN - Longword Access Enable; a UNIBUS Map Register bit

MBZ - Must Be Zero

MSYN - Master Sync; a UNIBUS signal issued by the bus master and received by the bus slave. Assertion of MSYN requests the slave, defined by the UNIBUS address lines, to perform the function required by the UNIBUS control lines. Negation of MSYN indicates to the slave that the master considers the data transfer concluded.

NO ACK - No Acknowledge. As a VAXBI command response, NO ACK indicates that no slave has been selected or that an error occurred during transmission of the command/address cycle. As a VAXBI data response, NO ACK indicates that an error has been detected in the transaction.

NODE - See VAXBI Node

NODE ID - A hexadecimal number between 0 and F (or a decimal number between 0 and 15) that indicates which of the sixteen logical locations a particular VAXBI node occupies.

NODE SPACE - An 8K byte block of I/O addresses. Each node, based on its node ID, is allocated a unique node space. The DWBUA adapter's node space holds the DWBUA registers.

OCTAWORD - Sixteen contiguous bytes starting on an arbitrary byte boundary.

PORT LOCK - This mechanism locks the VAXBI and UNIBUS ports while the DWBUA is servicing a transaction.

PURGE - The act of emptying a BDP buffer by setting the corresponding DPCSR PURGE bit.

RCI - READ with Cache Intent; a VAXBI command. The data read from the slave is placed in the master's cache.

READ - A VAXBI command. The master node reads data from the slave.

RETRY - A VAXBI command response. This response indicates that the slave cannot immediately execute the command sent to it.

SACK - Selection Acknowledged; a UNIBUS signal. A device that has requested the bus acknowledges that it has been granted the bus, and that it accepts.

SSYN - Slave Sync; a UNIBUS signal issued by the bus slave and received by the bus master. Assertion of SSYN informs the bus master that the slave has concluded its part of the current data transfer. Negation of SSYN informs all bus devices that the slave has concluded the current data transfer.

STALL - As a VAXBI command response, STALL indicates that the slave needs additional time to acknowledge the command, is not ready to return the first data word on a READ command or vector data on an IDENT command, or is not ready to accept a data word on a WRITE command. As a VAXBI data response, STALL is used by the slave to delay the transmission of data.

STOP - A VAXBI command. This command selectively forces nodes to a state in which they do not start VAXBI transactions, yet they retain as much error information as possible.

UA - UNIBUS address

UNIBUS - An asynchronous bus consisting of 56 lines.

UNIBUS ARBITRATOR - Logic circuit that compares priorities from devices requesting the use of the data section of the UNIBUS. The arbitrator determines which device will next be granted control of the UNIBUS. A UNIBUS must have one and only one arbitrator. For the configuration described in this manual, the DWBUA is always the UNIBUS arbitrator.

UWMCI - Unlock WRITE Mask with Cache Intent; a VAXBI command. This command completes a read-modify-write cycle that began with an IRCI command.

VAXBI - VAX Bus Interconnect. It joins a processor to a combination of devices that can include I/O controllers, I/O bus adapters, memories, and other processors. This is a double-clock, synchronously operated interconnect with bus events occurring at fixed intervals. Bus arbitration and address and data transmissions are time-multiplexed over 32 data lines. Data transmission is at fixed lengths of 4, 8, or 16 bytes on naturally aligned addressing boundaries.

VAXBI NODE - An interface that occupies one of sixteen logical locations on a VAXBI. A VAXBI node consists of one or more VAXBI modules.

VOR - Vector Offset Register; a DWBUA internal register

WCI - WRITE with Cache Intent; a VAXBI command. The master node writes data to the slave and alerts other nodes to issue a VAXBI INVAL, if necessary, for the address written.

WINDOW SPACE — A 256K-byte block of I/O addresses. Each node, based on its node ID, is allocated a unique window space. The DWBUA adapter's window space holds the UNIBUS device registers and the UNIBUS memory space. The Starting Address Register and Ending Address Register must be set to enable this space.

WMCI — WRITE Mask with Cache Intent, a VAXBI command. This command is similar to WCI except the master selects the bytes of the addressed location that it wants to modify.

WRITE — A VAXBI command. The master node writes data to the slave.

APPENDIX - ع

APPENDIX C
SELF-TEST
MICRODIAGNOSTIC TESTS

The self-test microdiagnostic tests run in the order shown in Table C-1. Tests 1 through 3 check the DWBI A logic, tests 4 through 6 check the A WBI port logic, and tests 7 through 9 check the A WBI port logic and the I WBI S and its port logic.

Table C-1 Self-Test Microdiagnostic Tests

Test Number	Test Name	Description
1	29116 RAM Test	Verifies addressability and data integrity of last 16 locations of address processor RAM space. (Locations are used for storage of constants and DWBI A register addresses.) Other locations are verified in a later test.
2	DWBI A BAD Bit and BAD Register Test	Verifies Buffered Address (BAD) Bit, BAD Register, and BAD Output Mux of Data Path Gate Array.
3	BDP MAP IRAM March Test	Standard march test (10 data patterns) of Internal RAM (IRAM). Verifies that each IRAM location is uniquely addressable, checks each location for data integrity. This test cannot differentiate between data and address failures.
4	BDP Bus Latch Test	Verifies high words of both the receiving and multiplexing BDP bus latches.
5	IRAM Mask Chip Select Test	Verifies the chip select logic used when accessing the IRAM in mask mode.
6	BDP Stored Address Test	Checks that the DWBI A can properly execute Buffered Data Path instructions in verifying correct storage of buffers' addresses.
7	IRAM Address Increment Test	Verifies that the Data Path Gate Array can properly increment an IRAM address.
8	Translation Buffer Test	Verifies the integrity of the Translation Buffer.
9	29116 Condition Code Test	Performs a branch test on all condition codes that are not tested in other parts of this self-test.
A	29116 Instruction Test	Verifies that address processor can execute all functional microcode instructions that are not otherwise executed during this self-test.

Table C-1 Self-Test Microdiagnostic Tests (Cont)

Test Number	Test Name	Description
8	Starting/Ending Address Registers Test	Performs VAXBI transactions. Writes to the DIR Starting Address and Ending Address Registers with the range of UNIBUS window space, reads the node ID from the DIR CSR, compares the corresponding values for the two registers, and then writes to each of these registers.
C	BDP Write Mask Test	Verifies the write mask flip-flops on the Data Path Gate Array. These flip-flops store the mask for a VAXBI extended WRITE mask transaction. (This transaction is executed whenever a Buffered Data Path is purged.)
D	VAXBI WMCI/RIAD Test	Verifies that the DWBUA can perform VAXBI RIAD and WRITE transactions to the DIR by performing word-length transactions on the VAXBI. (These operations are used by UNIBUS-to-VAXBI Direct Data Path transactions.) This test uses the DIR General Purpose Registers, and it verifies that both word and byte length transactions are possible from the UNIBUS to the VAXBI.
E	UNIBUS DATO/DATI Test	Uses the LFT module to verify that the DWBUA can write to and read from the UNIBUS. Performs a VAXBI WMCI instruction to set up the VAXBI Address Transceiver with the LFT module's Address Register address and to set a data pattern on the BDP bus. The test then operates similarly to the DWBUA functional microcode. Failure of this test indicates a problem in the UNIBUS cabling, power, or LFT module.
F	VAXBI-to-UNIBUS IRCI/UWMCI Test	This test ensures that VAXBI IRCI/UWMCI commands can be processed by the DWBUA. The DWBUA verifies that the corresponding DATIP/DATOB sequence functions properly on the UNIBUS. The test initially writes a known data pattern (AAAA hex) to the LFT Data Register. A DATIP is then issued to read this register. The DATIP is immediately followed by a DATOB. The address is driven on the UNIBUS through the duration of the DATIP/DATOB sequence. The data for the DATOB (5555 hex) is loaded into the Data Path Gate Array prior to initiation of the DATIP. After completion of the DATOB, the data from the DATIP is read from the Data Path Gate Array and verified in the address processor. A DATI is then issued to the LFT Address Register to verify that the DATOB completed properly.

Table C-1 Self-Test Microdiagnostic Tests (Cont)

Test Number	Test Name	Description
10	UNIBUS DATO/DATI Test	Verifies that a UNIBUS DATI command can execute through the the Direct Data Path. UNIBUS Map Registers are set up and the corresponding UNIBUS address is written into the LFT Address Register. A DATI is issued, and the test then waits for the UNA part request to come into the DWBUA. If it does, the incoming address is resolved through the UNIBUS Map Register. The test verifies that the correct UNIBUS Map Register was referenced by a macrocode jump with values from that register.
11	DWBUA Error Test	Attempts special-case transactions between the VAXBI and UNIBUS and verifies proper execution of these transactions. These special cases are: VAXBI READ of an unmated UNIBUS address, and a DWBUA RETRY response to the VAXBI due to the servicing of a concurrent UNIBUS request.
12	VAXBI INTR/IDENT Test	Verifies that a UNIBUS device can successfully interrupt the VAXBI and pass along its vector information. Writes the LFT CSR to generate a UNIBUS request. The LFT module is written and a UNIBUS BR is asserted. This causes the DIR to initiate a VAXBI interrupt to the DWBUA. The DWBUA processes a VAXBI IDENT command at the level corresponding to the INTR that was issued. The test generates the IDENT command.

APPENDIX D

APPENDIX D
MACRODIAGNOSTIC TESTS

\MDT>

The macrodiagnostic error messages indicate the failing test number, the expected data, and the received data.

Table D-1 Macrodiagnostic Tests

Test Number	Subtest Number	Name
1		IBM A Common and Device Type Registers Test
	1	IBM A Self Test and Register Subtest
	2	IBM A Reserved and Device Type Subtest
2		IBM A Registers Test
	1	VAXBI IBER Read/Write Subtest
	2	VAXBI FKER Read Subtest
	3	VAXBI Interrupt Destination Register Read/Write Subtest
	4	IBM A VAMP Read/Write Subtest
	5	VAXBI GPR Read/Write Subtest
3		Map RAM Match Test
4		I/O Read/Write Test
	1	Word Read Subtest
	2	Word Read/Write Subtest
	3	Word Read/Byte Write Subtest
5		I/O SCSI A READ/I/O A WRITE Test
6		I/O SCSI VAXBI Addressing Test
7		Data Path Select Test
8		Direct Data Path DATI Test
9		Direct Data Path DATO Test
10		Buffered Address Register Test

Table D-1 Macrodiagnostic Tests (Cont)

Test Number	Subtest Number	Name
11		Buffered Data Path DATI Test
12		Buffered Data Path DATO Test
13		Buffered Data Path DATOB Test
14		Buffered Data Path Autosize Test
15		Byte Mask DATI Test
16		Byte Offset Bus DATO Test
17		Byte Offset BDP DATO Test
18		Byte Offset BDP DATOB Test
19		Byte Offset BDP DATOB Test
20		Page Boundary Transfer Test
	1	UET DATI Subtest
	2	UET DATO Subtest
	3	UET DATI/DATO Subtest
	4	UET DATO/DATI Subtest
21		BDP Byte to Octaword Transfer Test
	1	Address Match Octaword DATOB Subtest
	2	Address Match Octaword DATI Subtest
22		BDP Longword Access Enable Test
23		Bus Transceiver Test
	1	VAXBI to UNIBUS Bus Transceiver Subtest
	2	UNIBUS to VAXBI Bus Transceiver Subtest
24		Map Invalid Test
25		Map Entry Functional Test
26		CSR Status Bit Test
	1	BII and NEX Error Subtest
	2	REGDUMB Subtest
	3	USSTO Error subtest
	4	BADBDP Error Subtest
	5	IMR Error Subtest

Table D-1 Macrodiagnostic Tests (Cont)

Test Number	Subtest Number	Name
27		Interrupt Test
	1	UET BR7 Interrupt Subtest
	2	UET BR6 Interrupt Subtest
	3	UET BR5 Interrupt Subtest
	4	UET BR4 Interrupt Subtest
28		VAXBI Error Test
	1	UNIBUS Parity Bit Subtest
	2	UET Invalid BDP DATIP Subtest
29		Bus Int Test
	1	UNIBUS Int Subtest
	2	VAXBI STOP Command Subtest
30		IVBAR Register Test
31		UBI Multi Transfer Test
32		UBI Block Transfer Test

APPENDIX E

APPENDIX E
ERROR CONDITIONS

E.1 VAXBI-TO-UNIBUS TRANSACTIONS

E.1.1 Quadword and Octaword Transfers
The DWBUA accepts only valid longword transfers. The DWBUA responds to all quadword and octaword transfers with NO ACK.

E.1.2 BIIC Error EVENT Codes
Table E-1 lists the DWBUA responses to BIIC error EVENT codes. In the responses listed, the DWBUA sends error interrupts to the VAXBI only if interrupts are enabled.

Table E-1 DWBUA Response to BIIC EVENT Codes

EVENT CODE					Mnemonic	DWBUA Response
H	L	H	L	L	IAI	The current BIIC command is ignored. No bus grant is withheld from the UNIBUS.
L	H	H	H	L	BPE	The current slave WRITE-type transaction is ignored, and the data is not updated.
L	H	H	H	H	STO	If the transaction is a RMW-type, it is ignored. The BIIC sends an error interrupt.
L	H	H	L	H	XRSD	
L	H	H	L	L	RBE	
H	H	H	L	L	BSO	The BUACSR BSE bit is asserted. The BIIC sends an error interrupt. SSYN may be withheld from the UNIBUS device which would result in an SSYN timeout.
L	L	H	H	H	RDMR	
L	L	H	H	L	XCRAR	
L	L	H	L	H	WCRAR	
L	L	L	H	H	IURMD	
L	L	L	H	L	RTO*	
L	L	L	L	H	BPM	
L	L	L	L	L	MTLT	

* The DWBUA receives this error EVENT code only if the RTOEN bit in the DWBUA adapter's BICSR is asserted.

E.1.3 Mask Values
The mask value in a WRITE-mask command is legal only if at least one mask bit is set in the word pointed to by address bit A1, and no mask bits are set in the other word of the longword. (The DWBUA responds with ACK regardless of the mask value.) The following are the only legal mask values:

A1=0 0000yyyy yy≠00
A1=1 yyyy0000

Any mask values that do not conform to this format are illegal. These illegal values either corrupt UNIBUS data or cause an SSYN timeout to the DWBUA.

E.1.4 Nonexistent UNIBUS Address

A valid WRITE or READ command is sent to a nonexistent UNIBUS address.

- The DWBUA responds to the WRITE command as ACK. It then sets the UNIBUS bit in the BUACSR, issues an error interrupt if interrupts are enabled, and writes the UNIBUS address to the Failed UNIBUS Address Register (bb+??6).

- The DWBUA sends zero data and an RIX status code in response to the READ command. It also sets the UNIBUS bit in the BUACSR, issues an error interrupt if interrupts are enabled, and writes the UNIBUS address to the Failed UNIBUS Address Register (bb+??6).

E.1.5 Invalid VAXBI Command

A VAXBI command that the DWBUA considers an invalid results in a NO ACK response from the DWBUA. The VAXBI commands that the DWBUA considers invalid are:

- RESERVED (BCI[3:0] = 0000)
- INTR
- RESERVED (BCI[3:0] = 1010 - 1011)
- RESERVED (BCI[3:0] = 1101 - 1111)
- INVALIDATE
- BROADCAST
- IPINTR

E.1.6 Improper Use of a DWBUA Register

An attempt to improperly use a DWBUA register results in a RETRY response from the DWBUA. Improper use of a DWBUA register is:

- Attempted WRITE to a READ-ONLY bit in a DWBUA control register
- Attempted access of an unused address in the DWBUA register space

E.2 UNIBUS-TO-VAXBI TRANSACTIONS

E.2.1 VAXBI Error in UNIBUS-Initiated Transfer

- Direct Data Path and DATI through a Buffered Data Path

  The DWBUA does not assert SSYNC to the UNIBUS device when a VAXBI error is encountered during a DDP transaction or during a DATI through a BDP. The DWBUA asserts the BUACSR BEI bit and writes the VAXBI address to the VAXBI Failed Address Register (bb+??4).

- DATO(B) through a Buffered Data Path

  The DWBUA asserts SSYNC to the UNIBUS device before it checks for VAXBI errors during a DATO(B) through a BDP. The DWBUA causes an NPR/NAK timeout during the next transfer within the present UNIBUS arbitration cycle. If the current transfer, however, is the last transfer within the present UNIBUS arbitration cycle, the UNIBUS device cannot be notified of the VAXBI error. The DWBUA asserts the BUACSR BEI bit and writes the VAXBI address to the VAXBI Failed Address Register (bb+??4).

E.2.2 Illegal Map Entries

- DMA access through an invalid map page

  A UNIBUS device might attempt a DMA access through an invalid map page (that is, the UNIBUS Map Register is NOT VALID) but is unaware. If this happens, the DWBUA asserts the BUACSR IMR bit, issues an error interrupt if interrupts are enabled, and withholds SSYNC, causing an NXM timeout for the UNIBUS device.

- DMA access through an illegal BDP

  If a UNIBUS device attempts a DMA access through BDP 4 or 5, the DWBUA asserts the BUACSR BADBDP bit, issues an error interrupt if interrupts are enabled, and withholds SSYNC, causing an NXM timeout for the UNIBUS device.

- DATIP through a BDP

  If a UNIBUS device attempts a DATIP through any Buffered Data Path, the DWBUA withholds SSYNC, causing an NXM timeout for the UNIBUS device.

E.2.3 Illegal UNIBUS Transaction

DATI(B) must follow a DATIP but if BBSY is unasserted during the DATI(B), the DWBUA asserts the BUACSR UBI bit and issues an error interrupt if interrupts are enabled.

APPENDIX E

APPENDIX F
UNIBUS
EXERCISER TERMINATOR

F.1 UNIBUS EXERCISER TERMINATOR DESCRIPTION

The UNIBUS Exerciser Terminator (UET) [illegible] module is located in sections A and B of the last UNIBUS slot. The UET enables diagnostic testing of the DWBUA adapter's capabilities to handle UNIBUS addressing, data transfers, and interrupts.

F.2 UNIBUS EXERCISER TERMINATOR REGISTERS

Table F-1 UNIBUS Exerciser Terminator Registers

Register Address (octal)	Register Name/Bits	Notes
777140	Address Register (AR<15:00>)	Word load only. Byte loading causes timeout
777142	Data Register (DR<15:00>)	Both byte and word loading allowed
777144	Control Register (CR<15:00>)	Word load only. Byte loading causes timeout

F.2.1 Control Register Format

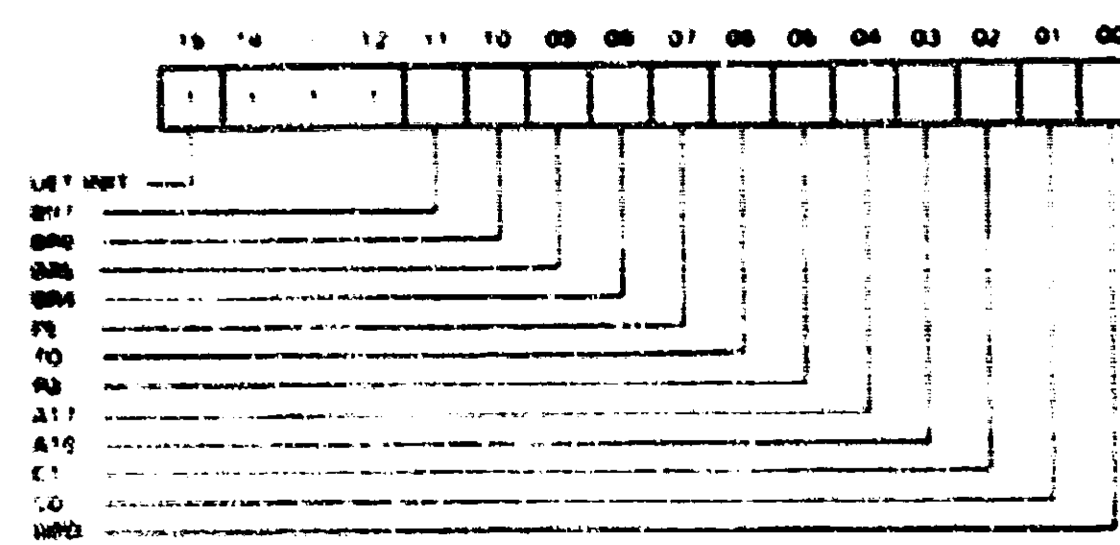


Figure F-1 UET Control Register Format

F.2.2 Control Register Bit Descriptions

UET Init CR<15>	Initialize UET to simulate reset or power-up. This WRITE-ONLY bit always reads 1. It does not clear CR<4,3>.
Unused CR<14:12>	Always read as 0
BR7, BR4 CR<11:08>	Write 1 to initiate interrupt
PI CR<7>	Parity Error detected during UET DATI. Checked on each UET DATI and cleared by UET Init.
TO CR<6>	Timeout (SSYN not returned). Checked on each transfer; cleared by UET Init.
PB CR<5>	Parity Bit. When set, the PB line will be asserted when the UET Data Register is read. This bit is cleared by UET Init.
A17, A16 CR<4,3>	High-order UNIBUS addressing bits
C1, C0 CR<2,1>	Transfer command bits (see Table F-2)
NPR CR<0>	Write 1 to initiate transfer

Table F-2 Transfer Command Bits

C1	C0	Command
0	0	UET DATI
0	1	UET DATIP
1	0	UET DATO
1	1	UET DATOB

NOTE

CR<11:08> and CR<0> (BR7 - BR4 and NPR respectively) remain set until the grant is returned at which time they are cleared. These bits are also cleared by writing a 0 to the bit or by writing a 1 to UET Init (CR<15>). Multiple interrupts may occur if more than one bit is set.

F.3 NPR DATA TRANSFERS

F.3.1 UET WRITE

A UET WRITE consists of the following sequence of events.

1. Load Address Register (A<15:00>)
2. Load Data Register (D<15:00>)
3. Load Control Register to initiate the transfer:
   a. CR<4,3> (A<17,16> of UNIBUS Address)
   b. CR<2,1> (10 for DATO, 11 for DATOB)
   c. CR<0> (Generate NPR)

F.3.2 UET READ

A UET READ consists of the following sequence of events.

1. Load Address Register (A<15:00>)
2. Load Data Register (D<15:00>)
3. Load Control Register to initiate the transfer:
   a. CR<4,3> (A<17,16> of UNIBUS Address)
   b. CR<2,1> (00 for DATI, 01 for DATIP)
   c. CR<0> (Generate NPR)

NOTE

The UET does not send a DATO/DATOB following a DATIP. After it has completed the DATIP, the UET drops SACK and releases the UNIBUS.

F.4 BR INTERRUPTS

The following sequence of events implements a BR interrupt.

1. Load the Data Register (D<15:00>) with the vector address.

2. Load Control Register bits CR<11:08> with the BR (BR7 - BR4) level

APPENDIX G

APPENDIX G
NODE SPACE AND WINDOW SPACE ADDRESSES

Table G-1 Node Space and Window Space Addresses

NODE NUMBER	NODE SPACE ADDRESSES		WINDOW SPACE ADDRESSES	
	Starting	Ending	Starting	Ending
0	[illegible]	[illegible]	[illegible]	[illegible]
1	[illegible]	[illegible]	[illegible]	[illegible]
2	[illegible]	[illegible]	[illegible]	[illegible]
3	[illegible]	[illegible]	[illegible]	[illegible]
4	[illegible]	[illegible]	[illegible]	[illegible]
5	[illegible]	[illegible]	[illegible]	[illegible]
6	[illegible]	[illegible]	[illegible]	[illegible]
7	[illegible]	[illegible]	[illegible]	[illegible]
8	[illegible]	[illegible]	[illegible]	[illegible]
9	[illegible]	[illegible]	[illegible]	[illegible]
A	[illegible]	[illegible]	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]
C	[illegible]	[illegible]	[illegible]	[illegible]
D	[illegible]	[illegible]	[illegible]	[illegible]
E	[illegible]	[illegible]	[illegible]	[illegible]
F	[illegible]	[illegible]	[illegible]	[illegible]

APPENDIX H

APPENDIX H
REGISTER INITIAL STATES

The initial state of each register is its state after successful completion of the BIIC and DWBUA self-tests.

Table H-1 Register Initial States

Address (bb+)	Register	Initial State	Notes
00	Device Type	xxxx0102	xxxx = DWBUA revision
04	VAXBI Control and Status	[illegible]	xx = VAXBI interface revision x = DWBUA node ID (hex)
08	Bus Error	00000000	
0C	Error Interrupt Control	00000000	
10	Interrupt Destination	0000xxxx	xxxx = decoded DWBUA node ID (one bit set)
14	IPINTR Mask	xxxx0000	xxxx = IPINTR mask
18	Force IPINTR/STOP Destination	0000xxxx	xxxx = force IPINTR/STOP destination
1C	IPINTR Source	xxxx0000	xxxx = IPINTR source
20	Starting Address	xxxx0000	xxxx = starting address of DWBUA adapter's window space (between 2000 and 203C, last digit 0, 4, 8, or C)
24	Ending Address	xxxx0000	xxxx = starting address of window space after DWBUA (between 2004 and 2040, last digit 0, 4, 8, or C)
28	BCI Control	0000[illegible]	STOPEN, IDENTEN, and UCSREN bits set
2C	Write Status	10000000	
30	Force IPINTR/STOP Command	00001800	
40	User Interface Interrupt Control	00000000	
F0	GPR 0	00000001	UBPUP = 1, self-test passed

Table H-1 Register Initial States (Cont)

Address (hex)	Register	Initial State	Notes
14-1C	GPR 3-7	[illegible]	
720	DWDR A Control and Status	[illegible]	
724	Vector Offset	[illegible]	
728	Failed UNIBUS Address	[illegible]	
72C	VAX BI Failed Address	[illegible]	
730-740	Microdiagnostic	[illegible]	
740	DPCSR 0	[illegible]	DPCSR = Data Path Control and Status Register
744	DPCSR 1	[illegible]	
748	DPCSR 2	[illegible]	
74C	DPCSR 3	[illegible]	
7xx	DPCSR 4	[illegible]	
7xx	DPCSR 5	[illegible]	
8000-1FFC	UNIBUS Map	[illegible]	Location invalid
E000-FFFC	UNIBUS Map	[illegible]	I/O space addresses

APPENDIX

APPENDIX I
DATA PATH
OPERATION

I.1 DIRECT DATA PATH

The DWBA starts the VAXBI section of a LNIBUS-initiated transaction immediately after it receives the LNIBUS command. The DWBA issues SSYN to the LNIBUS transaction only if the VAXBI transfer completes successfully. If an error occurs during the VAXBI transfer, the BI_ACNF_ERR bit is set and an error interrupt is issued by the BIIC if interrupts are enabled. The DWBA may not issue SSYN to the LNIBUS device, causing an SSYN timeout.

The following two special cases must be noted for LNIBUS-initiated transactions through the Direct Data Path. In both cases, the BYTE_OFFSET bit in the corresponding LNIBUS Map Register is set, causing the LNIBUS address to be incremented by one before the corresponding VAXBI transaction is completed.

CASE 1 - DATO WITH LNIBUS ADDRESS BIT <01> SET

Two VAXBI longword WRITE transactions, with the data and mask bits shown in Figure I-1, are performed.

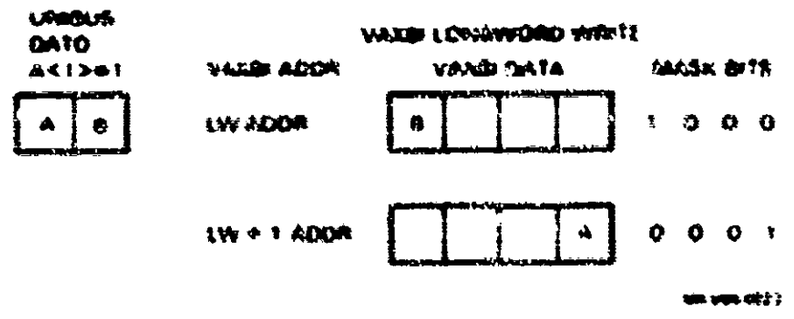


Figure I-1 DATO with LNIBUS Address Bit <01> Set

CASE 2 - DATI WITH UNIBUS ADDRESS BIT <01> SET

Two VAXBI longword READ transactions are performed. They obtain data for the UNIBUS transaction as shown in Figure 1-2.

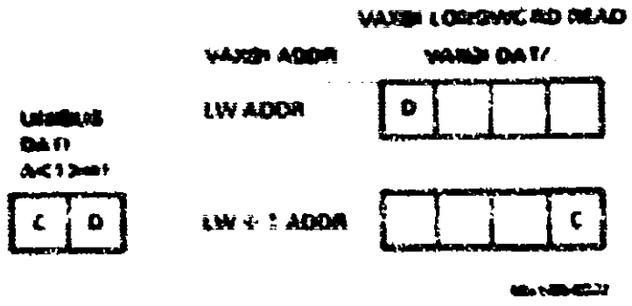


Figure 1-2 DATI with UNIBUS Address Bit <01> Set

For improved UNIBUS bandwidth, the DWBUA completes the corresponding UNIBUS DATO or DATOB transaction (by issuing SSYNC) prior to performing the VAXBI WRITE transfer. The DWBUA does not issue SSYNC as early for Direct Data Path DATI and DATIP transactions as it does for Buffered Data Path transactions, since the VAXBI transfer must first be completed in order to obtain the requested data.

1.3 BUFFERED DATA PATH

The DWBUA has five Buffered Data Paths (BDPs). Each BDP consists of three sections: a 16-byte buffer, a 16-bit address register, and a 16-bit status register.

1. Buffer - Each Buffered Data Path has a 16-byte buffer available for storage of as much as one octaword of data. The buffered data is naturally aligned at an octaword address. When the IWAEN bit is set in the UNIBUS Map Register for the current UNIBUS-to-VAXBI transaction, the buffer is virtually reduced to longword in length.

2. Address Register - The address register is a 16-bit register that contains UNIBUS address bits <17:04> in its most significant 14 bits. These 14 bits correspond to the data currently stored in the buffer. The least significant two bits of the address register are zero.

3. Status Register - Internal flags monitor the status of the data in the buffer. These flags are:

   BDBUF - VAXBI Data in Buffer
   UDBUF - UNIBUS Data in Buffer
   STRT_0 - Start Zero

   UDBUF and BDBUF are updated only during the first transaction through a Buffered Data Path. They indicate that either UNIBUS Data (UDBUF) or VAXBI Data (BDBUF) is being held in the buffer, as shown in Figure 1-3.

   UNIBUS-to-VAXBI buffered transactions do not necessarily cause the DWBUA to generate a VAXBI transfer. Rather, the DWBUA stores as much as one octaword of data locally.

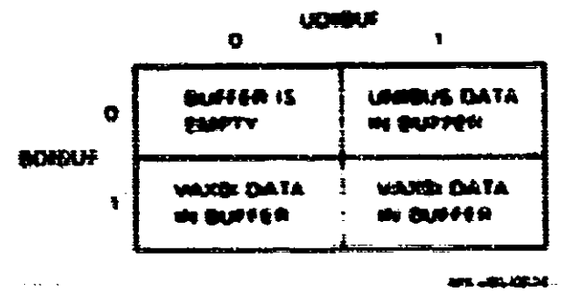


Figure 1-3 BDBUF and UDBUF Flags

When UDBUF is set, the DWBUA also updates the STRT_0 flag. The STRT_0 flag indicates that the first transaction through the Buffered Data Path began at an aligned octaword address (i.e., 10 - 04 = 0000). When the last byte in the buffer is written, the DWBUA sets the STRT_0 flag. If STRT_0 is set, the DWBUA assumes that the buffer contains a full octaword of valid data. The DWBUA then purges the data by performing an octaword WRITE (unmasked) transaction. If STRT_0 is not set, the DWBUA performs an octaword WMCI operation when writing the buffer to the VAXBI.

Each Buffered Data Path has its own status register and address register. These registers can be read by using the REGDMP feature, as explained in Section 3.2.4.1.

1.3.1 Definitions

Three common terms used in discussing Buffered Data Path behavior are Address Match, Autopurge, and Write-to-VAXBI. These terms are defined as follows:

1. Address Match - The BDP address register holds the UNIBUS address of the current octaword of data stored in the buffer. When another UNIBUS-to-VAXBI transaction is received, bits <17:04> of the incoming UNIBUS address are compared to the stored address. If the addresses match, the DWBUA manipulates the data in the buffer. If the addresses do not match, however, and the buffer contains UNIBUS data, then the DWBUA performs an autopurge.

2. Write-to-VAXBI - This term describes the process of writing UNIBUS data in a buffer to the VAXBI when the buffer is full. When IWAEN is not set and the buffer is full, the DWBUA checks the buffer's STRT_0 flag. If the flag is set, the DWBUA assumes that a full octaword of data is being held in the buffer. The Write-to-VAXBI will be performed using a VAXBI octaword WRITE. If the STRT_0 flag is not set or if the IWAEN bit is set, then the DWBUA assumes that the buffered transaction began with a nonaligned octaword address. Only part of the buffer contains valid data and the Write-to-VAXBI is performed using a VAXBI octaword WMCI.

3. Autopurge - If the buffer is not full and UNIBUS data is in the buffer, two occurrences will cause the data in the buffer to be written to the VAXBI. They are:

   a. A DATI is requested through the Buffered Data Path.

   b. A DATUBx is requested, but the addresses of the transaction and the data in the buffer do not match.

   Data is written from the buffer using a VAXBI octaword WMCI command with the presented mask bits set for each valid data byte. This act of writing the partially filled buffer to the VAXBI due to an address mismatch or mixed transaction types is known as autopurge.

1.2.2 BYTE OFFSET Bit Clear

The following three cases describe the behavior of the DWBUA depending on the contents of the BDP buffer. For each case, assume that a UNIBUS-to-VAXBI transaction is requested, and the BYTE OFFSET bit in the UNIBUS Map Register is not set.

CASE 1 - THE BUFFER IS EMPTY

The UNIBUS master is attempting a DATI through a valid UNIBUS Map Register. The DWBUA performs an octaword READ of VAXBI data and fills the BDP buffer. The DWBUA then places the requested data on the UNIBUS, asserts SSYN, updates the BDP flags by setting BDIBUF and clearing UDBUF, and stores the address value for the Buffered Data Path.

The UNIBUS master is attempting a DATO(B) through a valid UNIBUS Map Register. The DWBUA updates the BDP flags by setting UDBUF and clearing BDIBUF, stores the incoming UNIBUS address, asserts SSYN, and stores the data in the appropriate bytes of the BDP buffer with the correct mask bits set.

CASE 2 - THE BUFFER CONTAINS UNIBUS DATA

1. The UNIBUS master requests a DATI.

   The BDP buffer contains UNIBUS data, the current data in the buffer is autopurged. Once the autopurge is complete, the DWBUA treats the DATI request as it did in CASE 1 (since the buffer is empty).

2. The UNIBUS master requests a DATO(B).

   The BDP buffer contains UNIBUS data. The DWBUA checks for an address match. If the addresses do not match, the incoming UNIBUS address and data are temporarily stored within the DWBUA and the data currently in the BDP buffer is autopurged. Once the autopurge is complete, the DWBUA asserts SSYN. The DWBUA then loads the BDP address register with the address of the temporarily stored data. The DWBUA stores the data in the appropriate bytes of the BDP buffer, with the correct mask bits set.

   If the addresses do match, the DWBUA first asserts SSYN, then stores the data in the BDP buffer. If the DATO(B) writes the last byte in the buffer, the DWBUA performs a Write-to-VAXBI and marks the buffer as empty.

CASE 3 - THE BUFFER CONTAINS VAXBI DATA

The UNIBUS master requests a DATI, the buffer contains VAXBI data. The DWBUA checks for an address match. If the addresses do not match, the buffer is treated as if it were empty. The buffer is overwritten with the new octaword of VAXBI data (see CASE 1). If the addresses do match, the requested data is taken from the buffer, placed on the UNIBUS, and SSYN is asserted.

The UNIBUS master requests a DATO(B), the buffer contains VAXBI data. The DWBUA treats the buffer as if it were empty (see CASE 1).

1.2.3 BYTE OFFSET Bit Set

When the UNIBUS Map Register BYTE OFFSET bit is set, the DWBUA services requests in much the same way as when that bit is clear. The only exception is that the incoming UNIBUS address is incremented prior to address matching and storage. The following special cases, however, can occur when the BYTE OFFSET bit is set.

CASE 1 - UNIBUS ADDRESS <3:0> = 1110 (BYTE OFFSET BIT IS SET)

The address is incremented so that A<3:0> = 1111. A word length transaction to this address crosses an octaword boundary.

1. The UNIBUS master requests a DATI.

   If the BDP buffer contains VAXBI data, the DWBUA checks for an address match. If the addresses match, the DWBUA temporarily stores the last byte of the octaword. If the addresses do not match, the DWBUA requests a VAXBI octaword READ. When the READ transaction is complete, the DWBUA temporarily stores the last byte of the octaword.

   Once the low byte of data is stored within the DWBUA, the high byte of data is fetched by incrementing the incoming UNIBUS address to an octaword level, remapping, and reinitiating a VAXBI octaword READ for the next higher octaword address. Because the next octaword address must be remapped, the next UNIBUS Map Register must have the same value in the DATA PATH SELECT field as the current UNIBUS Map Register. If it does not, data integrity for all Buffered Data Paths cannot be ensured. When the READ transaction is complete, the first byte of the second octaword is fetched and concatenated with the temporarily stored low byte to form a word of UNIBUS data. This word is placed on the UNIBUS and SSYN is asserted.

   If the BDP buffer contains UNIBUS data, the DWBUA treats the transaction in a special way. The DWBUA does not autopurge the buffer as it does in a non-byte-offset transaction. Instead, the DWBUA READs a longword of VAXBI data through the Direct Data Path. This longword of data contains the low byte of the requested word, which is stored internally. Next, the DWBUA reads the next longword of data, which falls in the next octaword boundary in VAXBI memory. The corresponding map register must have the same value in the Data Path Select field as the current map register in order to ensure data integrity. The DWBUA then READs the longword and fetches the high byte of data, which it concatenates to the previously stored lower byte, forming a word of UNIBUS data. The DWBUA places this word on the UNIBUS and asserts SSYN. Thus, in this special case, the data stored in the buffer remains unchanged and the transaction is carried out through the Direct Data Path.

2. The UNIBUS master requests a DATO.

   If the buffer is empty or if it contains VAXBI data, the low byte of the incoming data is written into the last byte of the buffer, and a Write-to-VAXBI is performed. This generates an octaword WMCI transaction with only one byte of valid data. If the buffer contains UNIBUS data, the DWBUA checks for an address match. If the addresses match, the low byte of the incoming UNIBUS data is written to the last byte of the octaword, and a Write-to-VAXBI is performed. If the addresses do not match, the buffer is autopurged. When the autopurge is complete, the low byte of the incoming UNIBUS data is written to the last byte of the octaword buffer. A Write-to-VAXBI is performed, where only the last byte of the octaword contains valid data.

   Once the low byte has been written to the VAXBI, the high byte is written into the buffer with the appropriate mask. The flags are updated by setting UDBUF and clearing BDIBUF, the incoming address is incremented to the next octaword and stored, and SSYN is asserted. The BDP is left in the state it would be if a DATOB had been performed to an octaword-aligned address with no byte offset.

([illegible] – [illegible] = [illegible])

[illegible] standard set ([illegible] the model [illegible]). The only difference is that the multiple transactions that are generated (as explained above) occur each time a longword boundary is crossed rather than at a quadword boundary.

1.3.4 Examples

Figures 1-4 through 1-6 show the contents of a BDP buffer for various multiple DATOB(I) transactions. Each valid byte of data in the buffer has its corresponding mask bit set. All other mask bits for the BDP buffer are clear.

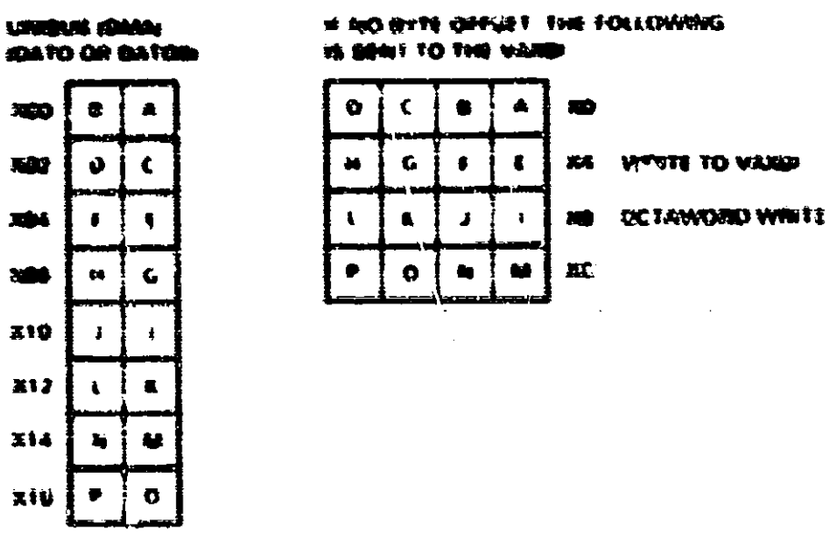


Figure 1-4 DATOB(I) Through BDP, BYTE (N)XM-1 (Low) Starting at Octaword Boundary

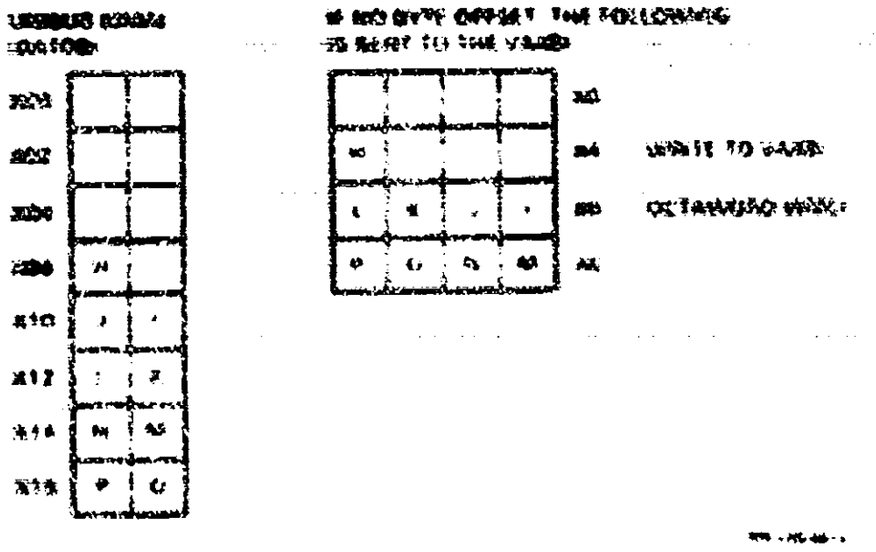


Figure 1-5 DATOB(I) Through BDP, BYTE (N)XM-1 (Low), Starting at Byte N

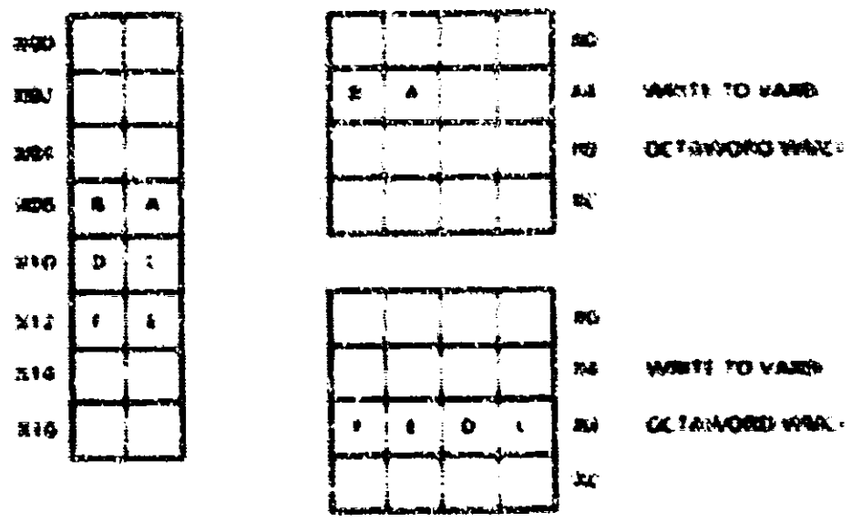


Figure 1-6 DATOB(I) Through BDP, BYTE (N)XM-1 (Low), LW Alone Set

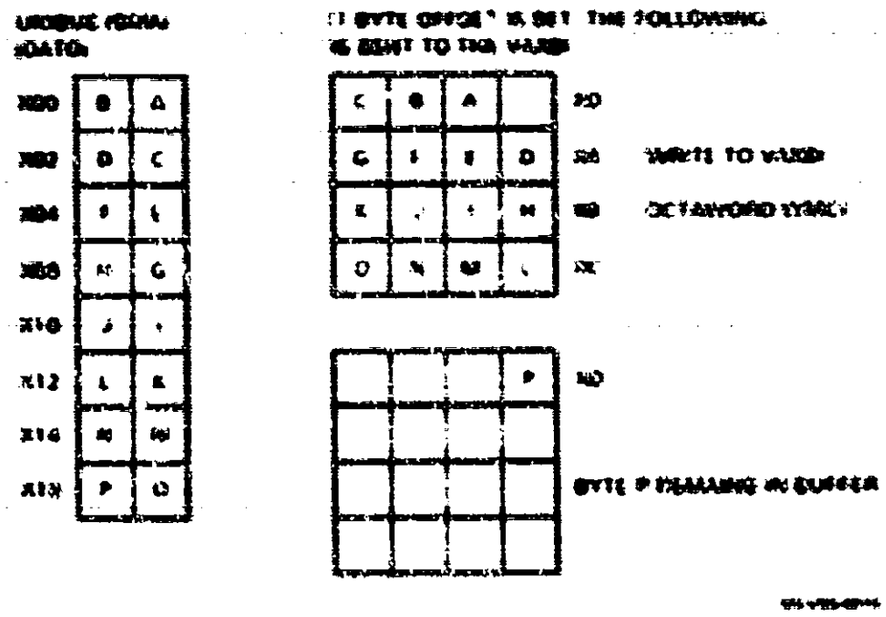


Figure 1-7 DATO Through RDP, BYTE OFFSET Set

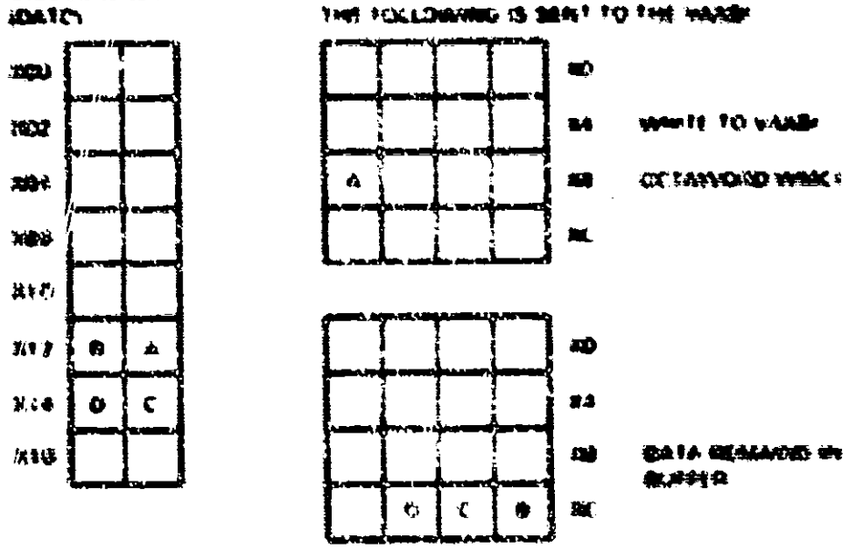


Figure 1-8 DATO Through RDP, BYTE OFFSET and [illegible] Set

APPENDIX J

APPENDIX J
PORT LOCK, RETRY, AND INTERRUPT MECHANISMS

J.1 PORT LOCK MECHANISM

The DWBUA has a port lock mechanism to ensure that a processor completes a transaction at a time. The mechanism locks the VAXBI and UNIBUS ports from accepting new transactions until the DWBUA is able to service that another request. While the DWBUA is locked it sends RETRY to all valid incoming VAXBI transactions except the STOP command. The DWBUA unconditionally sends an ACK response to the STOP command. The DWBUA also disables the UNIBUS arbitrator from issuing grants to UNIBUS devices while it is locked.

The DWBUA is locked during the following four circumstances and sends a RETRY response to all VAXBI transactions until it is:

1. The DWBUA has accepted a VAXBI transaction. The lock is released when the DWBUA has completed servicing the transaction. However, if the VAXBI transaction is an IDENT, the DWBUA sends a RETRY response to all transactions until a CLEAR command is sent to the DWBUA.

2. A UNIBUS DWBUA request is granted. The lock is released when a UNIBUS BBSY is negated by the UNIBUS master.

3. The DWBUA issues a VAXBI transaction such as autoprogram or the forcing of an error interrupt on the VAXBI. The port lock is released when the transaction is completed.

4. The DWBUA as the VAXBI master, the slave VAXBI node responds to its transaction with a RETRY. The DWBUA then sends a RETRY response to all subsequent incoming VAXBI transactions until its RETRYed master transaction has successfully completed.

J.2 RETRY MECHANISM

The RETRY mechanism reduces the number of RETRY responses sent by the DWBUA as VAXBI master nodes. It works by disabling and enabling the UNIBUS arbitrator.

When the DWBUA sends a RETRY response to a valid VAXBI command that it would otherwise accept, the DWBUA also disables the UNIBUS arbitrator. The UNIBUS arbitrator is enabled again when the DWBUA, as a slave node on the VAXBI, sends an ACK response to any VAXBI command.

A VAXBI node that receives a RETRY response from the DWBUA should keep requesting the DWBUA until it receives an ACK response. In this way, the VAXBI node ensures that its transaction will be the next one serviced by the DWBUA.

3.3 UNIBUS INTERRUPTS

Interrupts are permitted only from the UNIBUS to the VAXBI

3.3.1 Interrupt/IDENT Sequence

A BR of any level generates a VAXBI INTR transaction at the same level. The DWBUA does this by asserting the corresponding BCI INT line. The BIIC then performs the VAXBI INTR transaction.

The DWBUA responds to any VAXBI IDENT that meets two conditions:

1. The DWBUA must have a pending interrupt at the same level, and
2. The VAXBI master's decoded ID must match the ID in the Interrupt Destination Register (bits<10>).

Figure 3-1 is a flow diagram of the IDENT transaction. In the explanation that follows the figure, the numbered paragraphs refer to the numbers in the figure.

Figure 3-2 is a timing diagram of the interrupt/IDENT sequence. The following assumptions apply:

1. No errors occur during the transaction.
2. The transaction follows a straightforward path through the flows.
3. No time scale is employed. The diagram indicates relative timing only.

In the diagram, the device name that appears in parentheses under any waveform is the device that asserts that signal.

3.3.2 Passive Release

When some UNIBUS devices become bus master under BR-BG transactions, they drop BUSY and SACK and never issue an interrupt vector or assert INTR. This is known as a passive release. Passive release causes the DWBUA to send a zero vector back to the VAXBI, but the DWBUA does not flag an error interrupt.

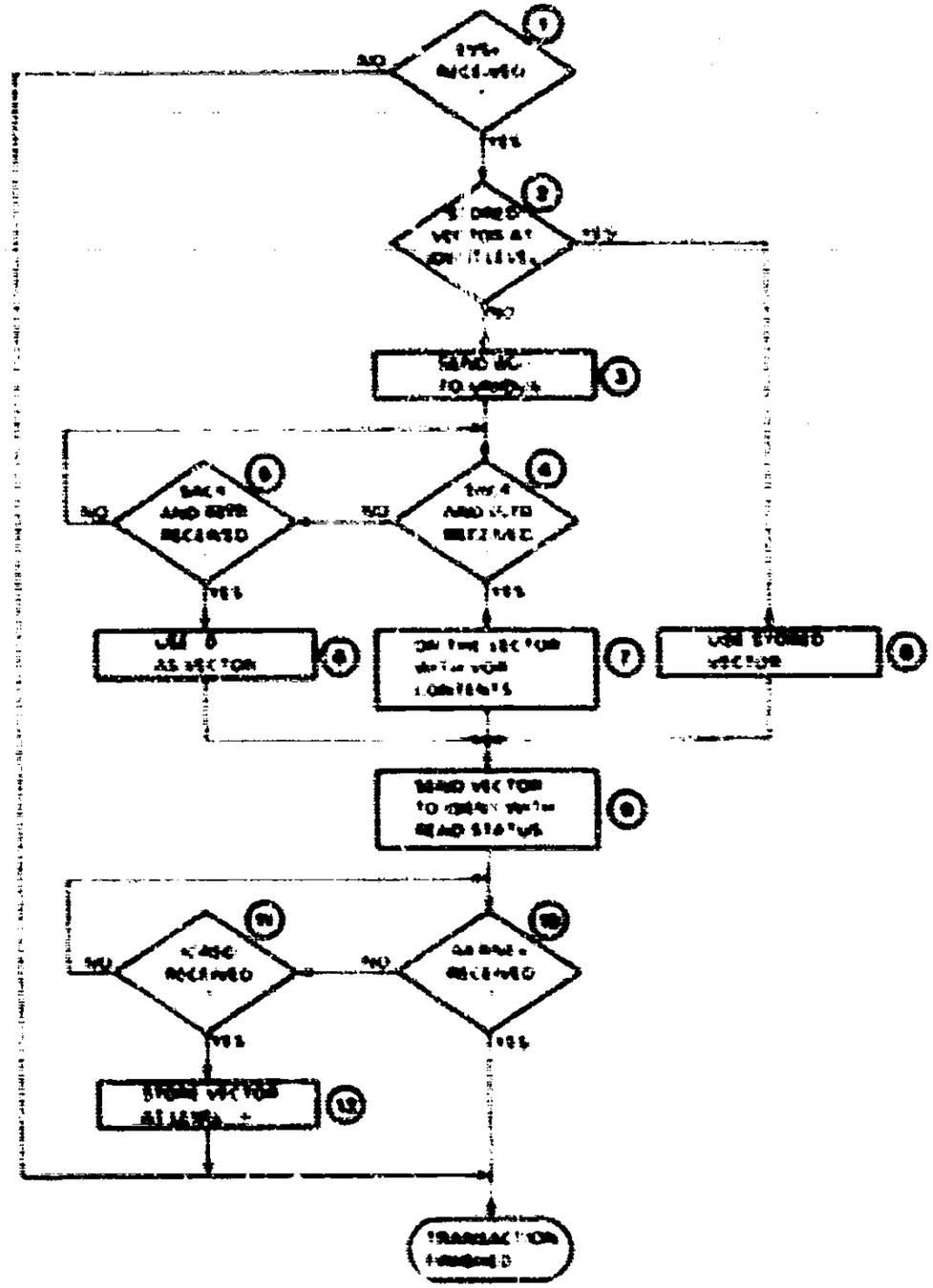


Figure 3-1 IDENT Flow Diagram

(1) The DWBI A checks that it has been selected by verifying that it has received an "External Vector Selected" EV code (EVSx). Receiving this EV code means that the DWBI A had an interrupt pending at the IDENT level and that the DWBI A adapter's Internal Destination Register (bits 7-0) contains the same decoded ID as the IDENT. The DWBI A then checks for the "IDENT Arbitrated" EV code to ensure that it has won the IDENT arbitration.

The DWBI A begins to service an incoming IDENT command only after it verifies that it has been selected for the IDENT and that it has won the IDENT arbitration. If these conditions are not met, the Interrupt/IDENT transaction is aborted.

(2) The DWBI A determines if it had a previous failed IDENT command at the present IDENT level.

(3) If it did not have a previous failed IDENT command at the present IDENT level, the DWBI A issues a BG to the interrupting UNIBUS device at the level indicated by the IDENT command.

(4) The DWBI A checks that SACK and INTR have both been received. This indicates that the interrupting UNIBUS device has given an expected response, placed the interrupt vector on the UNIBUS data lines, asserted INTR, and then deasserted SACK. The DWBI A issues SSYN and completes the UNIBUS transaction.

(5) If the interrupting UNIBUS device fails to respond to the BG, the UNIBUS arbitration resets and then deasserts SACK. When SACK is deasserted without the prior assertion of INTR, the DWBI A detects a SACK timeout.

(6) The DWBI A continues servicing the IDENT transaction normally, but it uses "0" as the interrupt vector.

(7) The DWBI A ORs the received vector with the contents of its Vector Offset Register (bits 7-2). This becomes the interrupt vector.

(8) The DWBI A uses the internally stored vector as the interrupt vector.

(9) The interrupt vector is placed on the BUS D lines along with a Read Data Status code.

(10) When the DWBI A receives the "Data Received for Same Error Vector" EV code (SAMEV), the IDENT has completed properly, and the DWBI A returns to its idle state.

(11) If the DWBI A receives an "Illegal CNF Received for Slave Data" EV code (ILRSD), the VMEbus master has not successfully received the IDENT vector.

(12) The DWBI A stores the failed IDENT command vector. This vector will be provided for any subsequent IDENT command at that particular level.

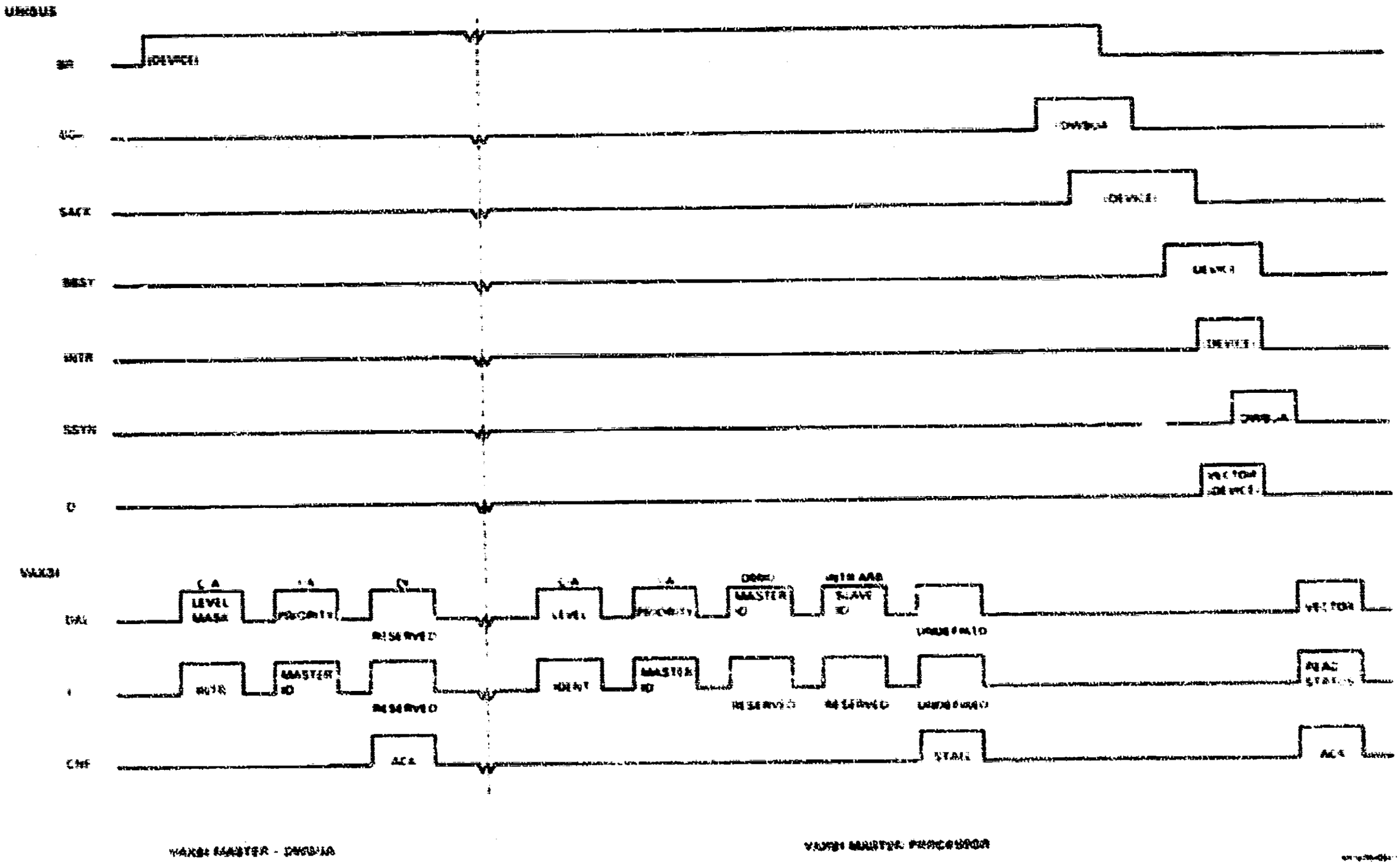


Figure J-2 Interrupt/IDENT Timing Diagram

APPENDIX K

APPENDIX K
MSYN-6SYN
TIME INTERVALS

NOTE

The MSYN - 6SYN time intervals listed in Table K-1 may change with enhancements to the DSMS system. The times listed were valid at the time of publication of this manual.

The following conventions are used in Table K-1:

- All transactions listed in brackets (()) are performed after MSYN is issued to the UNIBUS driver.
- The (data) means that the BDP buffer contains the UNIBUS DATO data to be sent to the VAXBI.
- The (data) means that the BDP buffer contains the UNIBUS DATI data received from the VAXBI.

Table K-1 MSYN - SSYN Time Intervals

Path	Byte Offset Bit	UNIBUS Command	UNIBUS Address <3:0>	Data Path Status	VAXBI Transaction	Max Time MSYN - SSYN (µs)	See Note
DDP	0	DATI	ANY	N/A	LW READ	[illegible]	
DDP	0	DATIP	ANY	N/A	LW IRCI	[illegible]	1
DDP	0	DATO	ANY	N/A	LW WMCI or LW UWMCI	[illegible]	2
DDP	0	DATOB	ANY	N/A	LW WMCI or LW UWMCI	[illegible]	
DDP	1	DATI	ANY	N/A	LW READ LW READ (ADDR <1> = 1)	[illegible]	3
DDP	1	DATIP	ANY	N/A	N/A	SSYN timeout	
DDP	1	DATO	ANY	N/A	LW WMCI LW WMCI (ADDR <1> = 1)	[illegible]	3
DDP	1	DATOB	ANY	N/A	LW WMCI	[illegible]	
BDP	0	DATI	ANY	Empty	OW READ	[illegible]	4
BDP	0	DATI	ANY	In-data & match	No BI transaction	[illegible]	
BDP	0	DATI	ANY	In-data, no match	OW READ	[illegible]	
BDP	0	DATI	ANY	Out-data	OW WMCI OW READ	[illegible]	
BDP	1	DATI	0 to [illegible]	Empty	OW READ	[illegible]	
BDP	1	DATI	0 to [illegible]	In-data & match	No BI transaction	[illegible]	
BDP	1	DATI	0 to [illegible]	In-data, no match	OW READ	[illegible]	
BDP	1	DATI	0 to [illegible]	Out-data	OW WMCI OW READ	[illegible]	
BDP	1	DATI	[illegible]	Empty	OW READ OW READ	[illegible]	
BDP	1	DATI	[illegible]	In-data & match	OW READ	[illegible]	
BDP	1	DATI	[illegible]	In-data, no match	OW READ OW READ	[illegible]	
BDP	1	DATI	[illegible]	Out-data	LW READ LW READ	[illegible]	5
BDP	X	DATIP	ANY	N/A	N/A	SSYN timeout	
BDP	0	DATO	ANY	Empty or in-data	[illegible]	[illegible]	6
BDP	0	DATO	ANY	Out-data & match	[illegible]	[illegible]	
BDP	0	DATO	ANY	Out-data, no match	OW WMCI [illegible]	[illegible]	
BDP	1	DATO	0 to [illegible]	Empty or in-data	No BI transaction	[illegible]	
BDP	1	DATO	0 to [illegible]	Out-data & match	No BI transaction	[illegible]	
BDP	1	DATO	0 to [illegible]	Out-data, no match	OW WMCI	[illegible]	
BDP	1	DATO	[illegible]	Empty or in-data	OW WMCI	[illegible]	
BDP	1	DATO	[illegible]	Out-data & match	OW WMCI	[illegible]	
BDP	1	DATO	[illegible]	Out-data, no match	OW WMCI OW WMCI	[illegible]	
BDP	0	DATOB	ANY	Empty or in-data	[illegible]	[illegible]	
BDP	0	DATOB	ANY	Out-data & match	[illegible]	[illegible]	
BDP	0	DATOB	ANY	Out-data, no match	OW WMCI [illegible]	[illegible]	
BDP	1	DATOB	ANY	Empty or in-data	[illegible]	[illegible]	
BDP	1	DATOB	ANY	In-data & match	[illegible]	[illegible]	
BDP	1	DATOB	ANY	Out-data, no match	OW WMCI [illegible]	[illegible]	

NOTES FOR TABLE K-1:

(1) A DATIP command is valid only through the Direct Data Path. If a DATIP is attempted through a Buffered Data Path or through the Direct Data Path with the BYTE OFFSET bit set, the UNIBUS command is ignored and the DWBUA does not issue SSYN, causing an SSYN timeout. During this time, all VAXBI transactions to the DWBUA receive a RETRY response until the UNIBUS device negates BBSY.

If a DATIP command is not followed by a DATO(B), the DWBUA sets the LIE bit in the BUACSR and forces an error interrupt if interrupts are enabled.

(2) A UNIBUS DATO(B) through the Direct Data Path translates to a longword WMCI transaction with the mask bits set for each valid data byte.

(3) The DWBUA performs two longword transactions on the VAXBI for a word-length transfer through the Direct Data Path if both the BYTE OFFSET bit and UNIBUS address bit <1> are set.

(4) A UNIBUS DATI command through a Buffered Data Path results in an octaword READ of VAXBI space if the requested data is not in the BDP buffer. If the UNIBUS data is stored in the BDP buffer, however, the buffer must be purged by performing an octaword WMCI to the VAXBI before reading the data from the VAXBI. The entire octaword is loaded into the buffer; subsequent accesses within the octaword through the same Buffered Data Path cause the DWBUA to fetch the data from the buffer, with no VAXBI transaction required.

(5) This special case is treated differently from other Buffered Data Path transfers to avoid delay in issuing SSYN. In this case, the low byte of the requested DATI word is fetched by performing a longword READ through the Direct Data Path. The high byte is fetched from either the current BDP buffer or the VAXBI with a longword READ through the DDP. The current BDP status remains unchanged during this transaction.

(6) A DATIP transaction is valid only through the DDP.

(7) Data for a DATO(B) command through a BDP is stored until the buffer is full. The DWBUA then performs a VAXBI octaword WRITE (unmasked) if the buffer contains an entire octaword of valid data from the UNIBUS device. A VAXBI octaword WMCI is performed if the buffer contains less than a complete octaword of valid data.

APPENDIX

APPENDIX L
DWBUA PARITY CHECKING

L.1 PARITY CHECKING

The DWBUA uses its 32-bit internal RAM as an internal storage source. When the RAM is updated, the [illegible] section of the DWBUA stores odd parity for the updated data in a separate RAM. The DWBUA checks for a parity error every time the internal RAM is read, thus verifying data integrity. This appendix describes the DWBUA adapter's parity checking and parity error reporting scheme.

L.2 INTERNAL RAM

The DWBUA adapter's internal RAM contains the UNIBUS Map Registers, BDP buffers, vector registers, and other DWBUA internal registers. The internal RAM is read during such operations as a VAXBI-requested READ of a DWBUA internal register or UNIBUS Map Register, [illegible] reading of a UNIBUS Map Register, a data transfer involving a BDP buffer, and any other operation that requires the DWBUA to read the contents of its internal RAM. A parity error can occur during any of these operations. The DWBUA handles a parity error slightly differently in each case.

L.3 PARITY ERRORS

In the newer versions of the DWBUA, which is capable of detecting parity errors, the DWBUA Control and Status Register contains these two additional bits:

PARITY ERROR <29>	(W1C, [illegible])	This bit is set if the DWBUA has found a parity error while reading its internal RAM.
PARITY DISABLE <28>	(R/W, [illegible])	While this bit is set, the DWBUA does not generate odd parity while writing to its internal RAM. This causes a parity error when the same RAM location is read later. This bit is for use of Digital Equipment Corporation diagnostics only and should not be used for any other purpose.

Whenever the DWBUA detects a parity error while reading its internal RAM, it sets the PARITY ERROR bit in the BCSR and sends an error interrupt to the VAXBI (if interrupts are enabled). The remaining sections describe the other effects of a parity error detected during various operations.

L.3.1 Parity Errors on UNIBUS Map Registers

A DWBUA UNIBUS Map Register enables mapping of an 18-bit UNIBUS address to a [illegible] VAXBI address. If a parity error occurs during a UNIBUS Map Register READ, it can cause the DWBUA to transfer the data to a different location from the correct target address. Hence, the DWBUA does not initiate the corresponding VAXBI transfer if it detects a parity error when reading a UNIBUS Map Register.

When a UNIBUS device initiates a transfer, the DWBUA reads the corresponding UNIBUS Map Register before servicing the UNIBUS data transfer. If a parity error occurs during this time, the DWBUA withholds an SSYN, causing the UNIBUS device that initiated the transfer to detect an SSYN timeout. The DWBUA then proceeds to report a parity error to the VAXBI. The data transfer associated with the error is not completed.

The UNIBUS Map Register may also be read when the DWBUA WRITEs or READs data during a DATO(B) or DATI transfer through a Buffered Data Path. If a parity error occurs when the UNIBUS Map Register is being read, the DWBUA does not send the VAXBI a [illegible]. The DWBUA withholds SSYN so the UNIBUS [illegible] SSYN has not been previously issued, causing an SSYN timeout to the UNIBUS device. The DWBUA then reports a parity error to the VAXBI. The DWBUA also clears the LOADED, [illegible] and [illegible] flags for the current Buffered Data Path, indicating that the BDP buffer is empty.

I.3.2 Parity Errors on BDP Buffers

The DWBUA BDP buffers are in the internal RAM. These buffers are read under the following conditions:

1. The BDP buffer contains the VAXBI data that is requested by the UNIBUS device initiated DATI transfer. If a parity error occurs while this data is being read from the BDP buffer, the DWBUA does not send the data to the UNIBUS device. The DWBUA withholds SSYN, causing an SSYN timeout. The DWBUA then reports a parity error to the VAXBI.

2. When a BDP buffer is full or has been [illegible], the DWBUA initiates an octaword WRITE (WMCI) transfer on the VAXBI. The DWBUA reads its internal RAM for each longword of data to be shipped. If a parity error occurs during the read of any one of the four longwords of data, the DWBUA completes the VAXBI transfer with the data that has the parity error. The DWBUA then reports the error to the VAXBI. The DWBUA clears its BDP flags, indicating that the Buffered Data Path is clear. The DWBUA may withhold SSYN if it has not been previously issued, causing an SSYN timeout. Hence, it may not be possible for the VAXBI processor to detect which data in the VAXBI memory has a parity error.

I.3.3 Parity Errors on Vector Registers

The DWBUA may receive an IDENT [illegible] from a UNIBUS device during an INTA command. When this happens, the DWBUA stores the vector [illegible] in its internal RAM. Subsequently, the next time the DWBUA receives an INTA command at the same level, the DWBUA uses the stored data as the vector. If the DWBUA detects a parity error during the reading of the stored vector, it sends zero data, a READ DATA status code, and an ACK response to the VAXBI master which initiated the INTA command. This should be treated as a passive release by the INTA-ing master. The DWBUA then reports a parity error as specified in Section I.5.

I.3.4 Parity Errors on DWBUA Internal Registers

When the VAXBI master device READs a DWBUA internal register, the DWBUA reads the data from the internal RAM and sends the data to the VAXBI master device with a READ DATA status code and an ACK response. If the DWBUA detects a parity error when reading the data from the internal RAM, it sends zero data, a READ DATA [illegible] status code, and an ACK response. The DWBUA then reports a parity error as specified in Section I.5.

I.4 PARITY ERROR TESTING

The DWBUA [illegible] of the logic associated with parity [illegible] parity for each location of the internal RAM and [illegible] the DWBUA [illegible]. The DWBUA [illegible] WRITE (WMCI) [illegible] VAXBI [illegible]. This means that the logic that detects a parity error during [illegible] verified.

The PARITY DISABLE [illegible] [illegible] parity generation logic. [illegible] PARITY DISABLE [illegible] the DWBUA [illegible] force a parity error [illegible] the DWBUA [illegible] of the functions listed under Section I.3 and verifies that the DWBUA [illegible] during the octaword WRITE (WMCI) [illegible] and verifies that the DWBUA has detected the parity error and reported [illegible].

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