

DRV11-WA General Purpose DMA Interface

User's Guide

**Prepared by
Computer Special Systems**

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1.1 GENERAL DESCRIPTION

The DRV11-WA is a general-purpose Direct Memory Access (DMA) interface for transferring 16-bit data words directly between the Q-bus memory and a user's I/O device. Data Transfer Out (DATO) or Data Transfer In (DATI) takes place over the Q-bus after a DMA request, once the DRV11-WA becomes bus master. Burst modes (four-word or continuous), byte addressing, and read-modify-write operation (DATIO) are possible with the DRV11-WA. The DRV11-WA features switch-selectable device and vector addresses, two 40-pin connectors, and one 2-pin connector that provide simple interfacing to the user's I/O device. (The DRV11-WA is compatible with both standard and extended Q-buses.)

There are six registers in the DRV11-WA. They are as follows:

- Word Count Register (WCR),
- Bus Address Register (BAR),
- Extended Bus Address Register (BAE),
- Control/Status Register (CSR), and
- Input and Output Data Buffer Registers (DBRs).

The CSR and DBRs are word- and byte-addressable, whereas the WCR, BAR, and BAE are only word-addressable.

DRV11-WA operation is initialized under program control by:

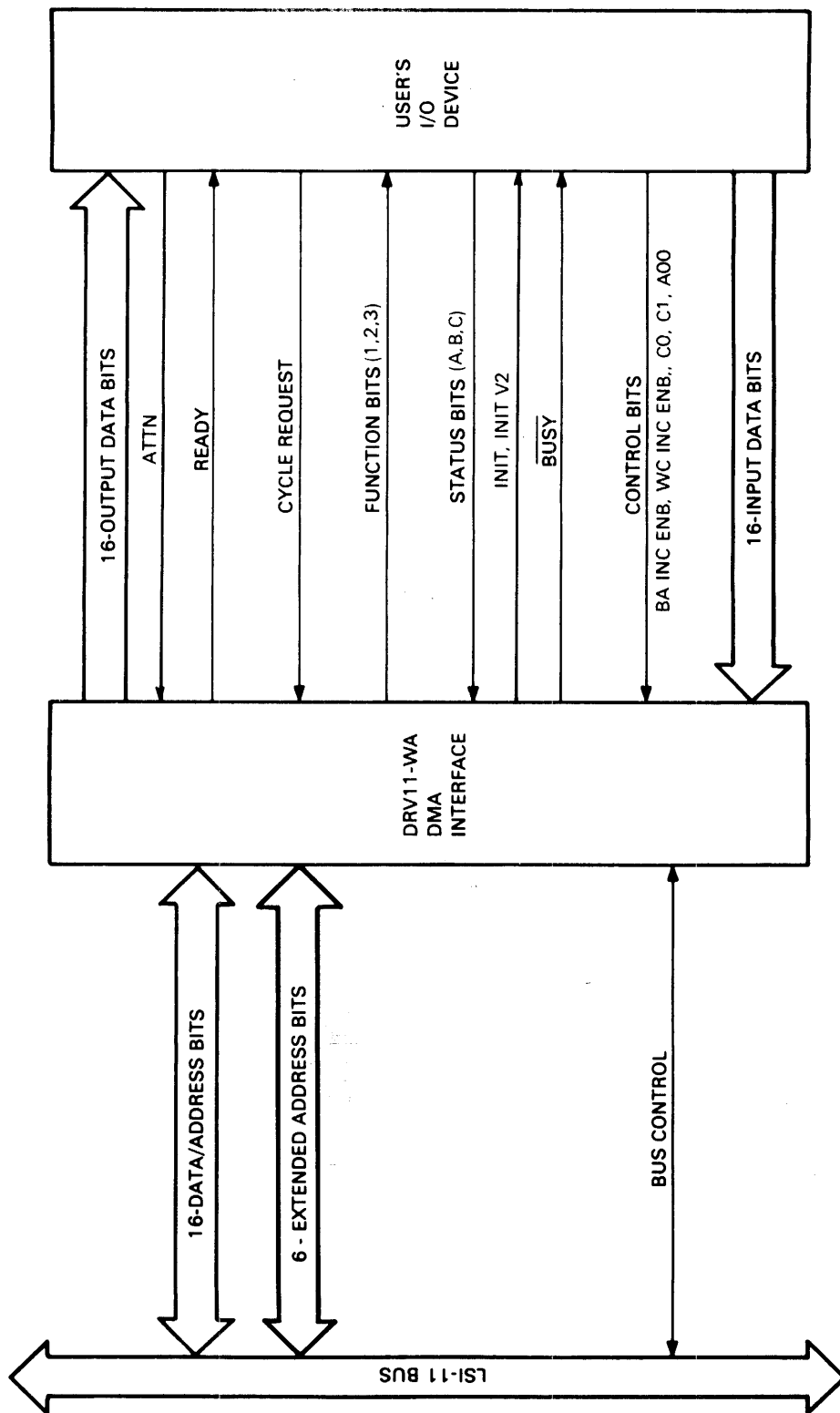
1. Loading the WCR with the 2's complement of the number of transfers,
2. Loading the BAR and BAE with the first address to or from which data is to be transferred, and
3. Loading the CSR with the desired function bits.

Data transfers may now proceed under the control of the DRV11-WA DMA logic.

Figure 1-1 shows the primary interface signals between the DRV11-WA and the user's I/O device. DMA input (DATI) or output (DATO) data transfers take place when the processor clears READY. For a DATO cycle (DRV11-WA to memory transfer), the user's I/O device first presets the CONTROL BITS (word count increment enable, bus address increment enable, C1, C0, A00, and ATTN), and then asserts CYCLE REQUEST to gain use of the Q-bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the CONTROL BITS are latched into the DRV11-WA DMA control, and BUSY goes low. (A DATI cycle memory to DRV11-WA transfer is handled in a similar manner, except that the output data is latched into the output DBR during the bus cycle.)

When the DRV11-WA becomes bus master, a DATO or DATI cycle is performed directly to or from the Q-bus memory location specified by the BAR and BAE. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue asynchronously until the WCR increments to zero, at which time READY goes high and the DRV11-WA generates an interrupt (if interrupt enable is set) to the Q-bus processor.

If continuous burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete synchronous transfer of the specified number of data words.



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Figure 1-1 DRV11-WA Simplified Interface Diagram

1.2 SPECIFICATIONS

The following specifications and particulars are for informational purposes and are subject to change without notice.

Physical

Dual height, single width, extended length module.

Dimensions:

Circuit Card

Length: 21.6 cm (8.5 in)
Height: 12.7 cm (5.0 in)
Width: 1.3 cm (.5 in)

Circuit Card Plus Handle

Length: 22.8 cm (8.9 in)
Height: 13.2 cm (5.2 in)
Width: 1.3 cm (.5 in)

Weight: 215 grams

User I/O Connections: Two 40-pin connectors, one 2-pin connector

Mounting Requirements: Plugs directly into Q-bus backplane or Q-bus expansion backplane.

Electrical

Logic Power Requirements: 1.8 A @ +5V \pm 5% (nominal)

LSI-11 Bus Loading: Presents one bus load

User Loading:

Input Data Lines

1 TTL unit load each
HIGH = Logic one
LOW = Logic zero

Input Control Lines

1 TTL unit load each
HIGH = Logic one
LOW = Logic zero

Output Data Lines

10 TTL unit loads (drive) each
HIGH = Logic one
LOW = Logic zero

Output Control Lines

10 TTL unit loads (drive) each
HIGH = Logic one
LOW = Logic zero

Module Type: M7651

Operational:

Transfer Mode: DMA or program-controlled with interrupts

Data Transfer Rate:

Up to 250,000 16-bit words per second in single cycle mode
Up to 400,000 16-bit words per second in burst mode*

Environmental

Temperature: Storage: -40°C to 66°C (-40° to 150°F)
Operating: 5°C to 50°C (41° to 122°F)

Relative Humidity: 10% to 95% noncondensing

1.3 RELATED LITERATURE

In addition to the M7651 print set (MP01582), the Microcomputer Processor Handbook and the Microcomputer Interface Handbook contain useful information for installing and operating the DRV11-WA general-purpose DMA interface. Handbooks may be ordered from the nearest Digital Equipment Corporation Sales Office.

-
- * While doing continuous burst mode transfers, the DRV11-WA becomes bus master and holds the bus until the entire transfer is complete. This action may potentially lock out other devices from accessing the bus while the transfers are ongoing. This mode of operation is consistent with the operation of the 18-bit predecessor product, DRV11-B.

CHAPTER 2 INSTALLATION

2.1 GENERAL

Installation of the DRV11-WA general-purpose DMA interface consists of selecting the device and interrupt vector addresses, selecting mode of operation (18- or 22-bit addressing), selecting functional operating modes as necessary (independent interrupts, four-word or continuous burst mode, interprocessor link mode), and then inserting the interface into an LSI-11/MicroVAX processor system.

2.2 SYSTEM CONSIDERATIONS

Before installing the DRV11-WA into a Q-bus system, consideration must be given to bus loading, power, priority, and space requirements.

2.2.1 LSI-11 Bus Loading

The DRV11-WA presents one bus load to the Q-bus. Fifteen bus loads can be handled by the Q-bus; therefore, the user must determine the existing Q-bus load when installing additional Q-bus modules.

2.2.2 Power Requirements

The DRV11-WA requires 1.8 A @ +5V \pm 5% (nominal). Power for the DRV11-WA is obtained from the Q-bus system power supply.

2.2.3 Priority Requirements

Each device on the Q-bus has an interrupt and DMA priority based on its relative position from the processor. The DRV11-WA is a priority 4 device. Since the user may install the DRV11-WA on the bus along with other devices that use the same interrupt or DMA priority, the user must bear in mind that when more than one device is requesting service, the device electrically nearest the Q-bus processor has the highest priority and will be serviced first.

In addition, if the REV11 DMA refresh option is used (for LSI-II systems), the REV11 must be at a priority level higher than that of the DRV11-WA. Refer to the Microcomputer Processor Handbook for detailed information on the REV11 options.

2.2.4 Space Requirements

The DRV11-WA requires one double height module slot.

2.3 USER I/O CABLES

The DRV11-WA has two 40-pin connectors which provide the interface to the user's device. Two cable assemblies are required. It is recommended that cable assemblies from Table 2-1 be used to connect the DRV11-WA to the user's device. The listed cables are terminated (one or both ends) with H856 40-pin connectors that mate with the connectors on the DRV11-WA. Cable selection is determined by the type of connections used on the user's device. The desired cable length (XX) must be specified when ordering. (Lengths longer than 25 feet are not recommended for use with the DRV11-WA.) Cables may be ordered from the nearest Digital Equipment Corporation Sales Office. Non-standard length cables may be ordered at additional cost.

2.3.1 User Termination Connector

The DRV11-WA has one 2-pin connector which optionally allows the user to provide additional signal termination when cables other than the one listed in Table 2-1 is used.

Table 2-1 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft/m)
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25 ft (0.305, 1.830, 3.050, 3.660, 6.100, 7.625 m)

2.4 JUMPER AND SWITCH CONFIGURATION

The DRV11-WA contains two DIP (dual in-line package) switch units (E40 and E50) and a number of jumpers that allow the user to select the module features desired. The location of the switch units and jumpers is shown in Figure 2-1. The address selection switch (E50) consists of ten switches that let the user select the device address. The second switch unit (E40) consists of ten switches that let the user select the interrupt vector address and 18-bit or 22-bit addressing mode.

2.4.1 Device Address Selection

The DRV11-WA contains six registers:

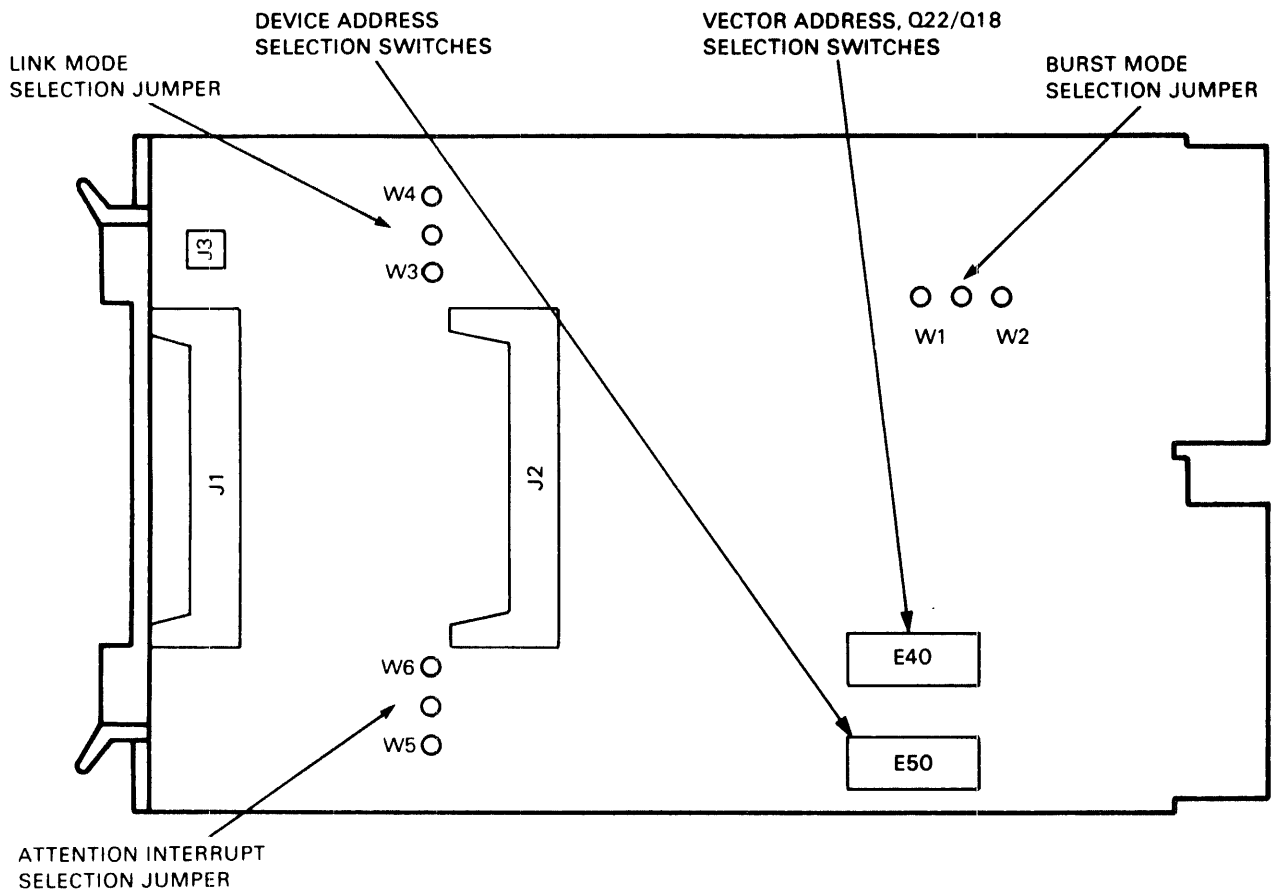
- WCR
- BAR
- BAE
- CSR
- Input DBR
- Output DBR

These registers must be addressed for data and status transfers between the DRV11-WA and the LSI-11/MicroVAX processor. The BAR and BAE use the same address. The two DBRs use the same address. The register addresses are sequential by even numbers and are as follows.

Register	BBS7	Octal Address	Hex Address
WCR	1	XXXXXX0	3FF508
BAR	1	XXXXXX2	XXXXXA
BAE	1	XXXXXX2	XXXXXA
CSR	1	XXXXXX4	XXXXXC
DBRs	1	XXXXXX6	XXXXXE

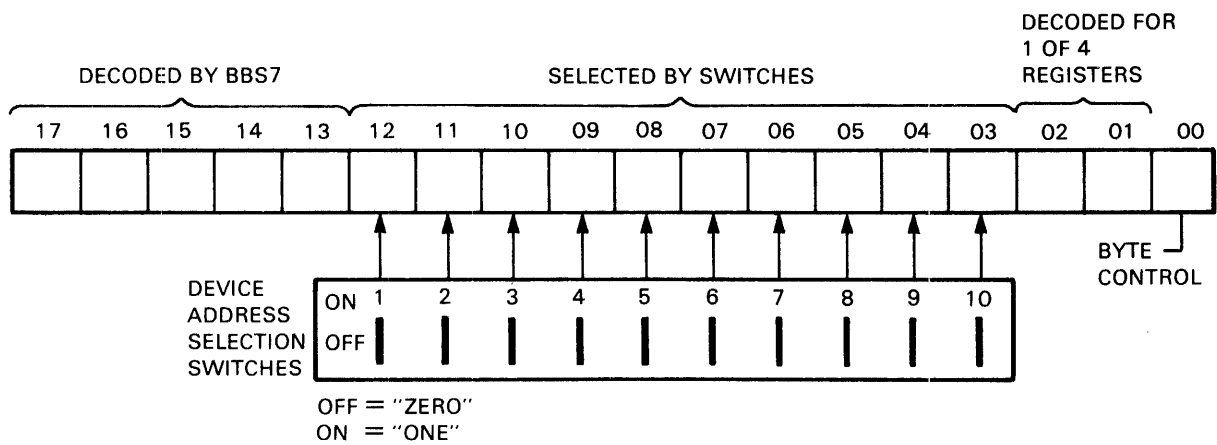
The assigned DMA interface base address is 772410_8 , $3FF508_{16}$. The user selects a base address for assignment to the WCR and sets the device address selection switches on the DRV11-WA module to decode this address. The remaining BAR, BAE, CSR and DBR addresses are then properly decoded by the module as they are received from the LSI-11 processor.

Figure 2-1 shows the location of the device address selection switches on the DRV11-WA module. Switches are set to the ON (closed) position for bits to be decoded as "ONE" bits in the base address. Bits decoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-2 shows the address select format and presents the switch-to-bit relationship for the device address selection switches.



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Figure 2-1 DRV11-WA Connector and Switch Locations



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Figure 2-2 DRV11-WA Device Address Select Format

2.4.2 Interrupt Vector Address Selection

Vector addresses 0-1774₈ are reserved for Q-bus system users. The DRV11-WA is assigned vector address 124₈. The user selects the interrupt vector address by means of switches on the DRV11-WA module. Figure 2-1 shows the location of the vector address selection switches. Vector address selection switches are set to the ON (closed) position for bits to be encoded as "ONE" bits in the vector address. Bits encoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-3 shows the address select format and presents the switch-to-bit relationship for the vector address selection switches.

NOTE

The DRV11-WA is designed to be compatible with the DRV11-B; therefore, its assigned base address is 772410(8). However, under MicroVMS, the DRV11-WA is treated, as much as possible, like a DRV11-W. Therefore, in order for the device to autoconfigure correctly, you must set the device address and interrupt vector address to those reserved for the DRV11-W; namely, set the device address to rank 19 and the interrupt vector address to rank 40, both in floating address space.

2.4.3 Addressing Mode Selection

The user selects 18- or 22-bit addressing by setting E40 switch 10 OFF (OFF=0) for 18-bit addressing, or ON (ON=1) for 22-bit addressing (see Figure 2-3).

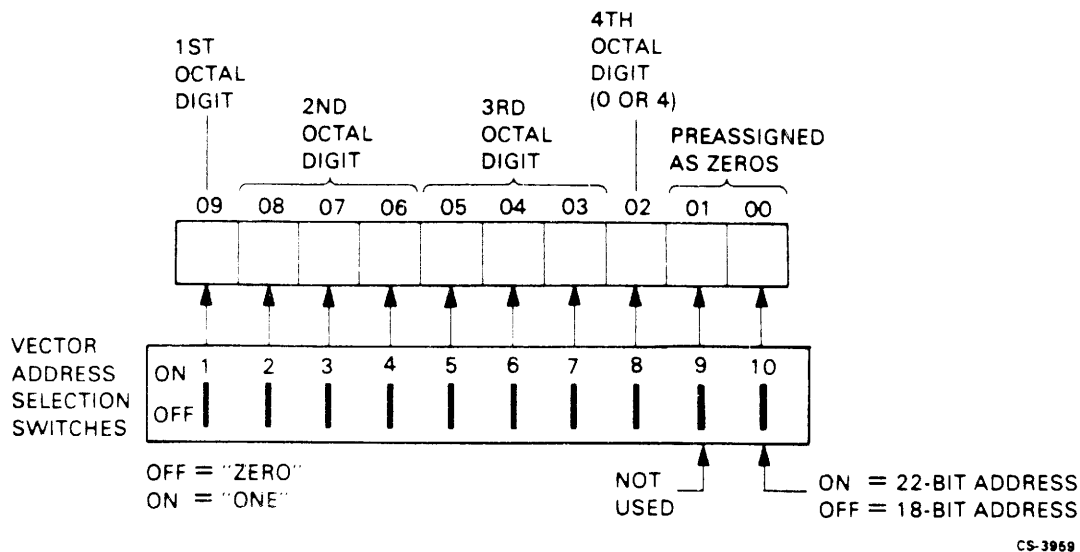


Figure 2-3 DRV11-WA Interrupt Vector Address Select Format

2.4.4 Burst Mode Jumper

The DRV11-WA will, by default (W2 jumper installed), relinquish and re-request bus mastership after every four DMA transfers. The user may select continuous burst mode transfers by removing the push-on jumper from W2 and installing it at W1. (Refer to Table 2-2 and Figure 2-1.)

NOTE

If continuous burst mode is selected, the DRV11-WA will not relinquish the bus until the entire transfer is complete. This action is not recommended as it may potentially lock out other devices from gaining access to the bus while the transfers are ongoing.

Table 2-2 Burst Mode Jumper

Jumper	Function	Factory Setting
W1	Module is backward compatible with the DRV11-B and will perform continuous burst mode transfers and will not release the bus until all transfers are completed.	R
W2	Module will relinquish and re-request the bus after every four DMA cycles.	I

R = Removed
I = Installed

2.4.5 Interprocessor Link Mode Jumper

The user may operate the DRV11-WA as an interprocessor link with another DRV11-WA by removing the push-on jumper from W3 and installing it at W4. (Refer to Table 2-3 and Figure 2-1). This is the recommended setting to use the DRV11-WA as an interprocessor link.

In the default setting (W3 jumper installed), the DRV11-WA is backward compatible with the DRV11-B and will not function as an interprocessor link unless one of the processors acts as the slave, and the other acts as the master. Use of the DRV11-WA within this configuration (W3 jumper installed) for interprocessor link is not recommended.

Table 2-3 Interprocessor Link Mode Jumper

Jumper	Function	Factory Setting
W3	Module is backward compatible with DRV11-B and should not be used as an interprocessor link.	I
W4	Module may be used as an interprocessor link between two DRV11-WA modules.	R

R = Removed
I = Installed

2.4.6 Independent Interrupts Jumper

While in the default interrupt mode (W5 jumper installed), it is not necessary for the READY bit (CSR Bit 7) to be CLEAR for the DRV11-WA to interrupt. With the IE bit (CSR Bit 6) set, the DRV11-WA will interrupt when the ATTN bit (CSR Bit 13) or the NEX bit (CSR Bit 14) is set.

For backward compatibility with the DRV11-B, the user may remove the push-on jumper from W5 and install it at W6. (Refer to Table 2-4 and Figure 2-1). In this setting, the DRV11-WA will only interrupt when the READY bit (Bit 7) of the CSR is set, and the IE bit (Bit 6) in the CSR is set.

Table 2-4 Independent Interrupts

Jumper	Function	Factory Setting
W5	With the CSR IE bit set, module will interrupt when CSR ATTN or NEX bits are set, independent of the READY bit being set.	I
W6	Module is backward compatible with DRV11-B. With the CSR IE bit set, module will interrupt only when the READY bit is set.	R

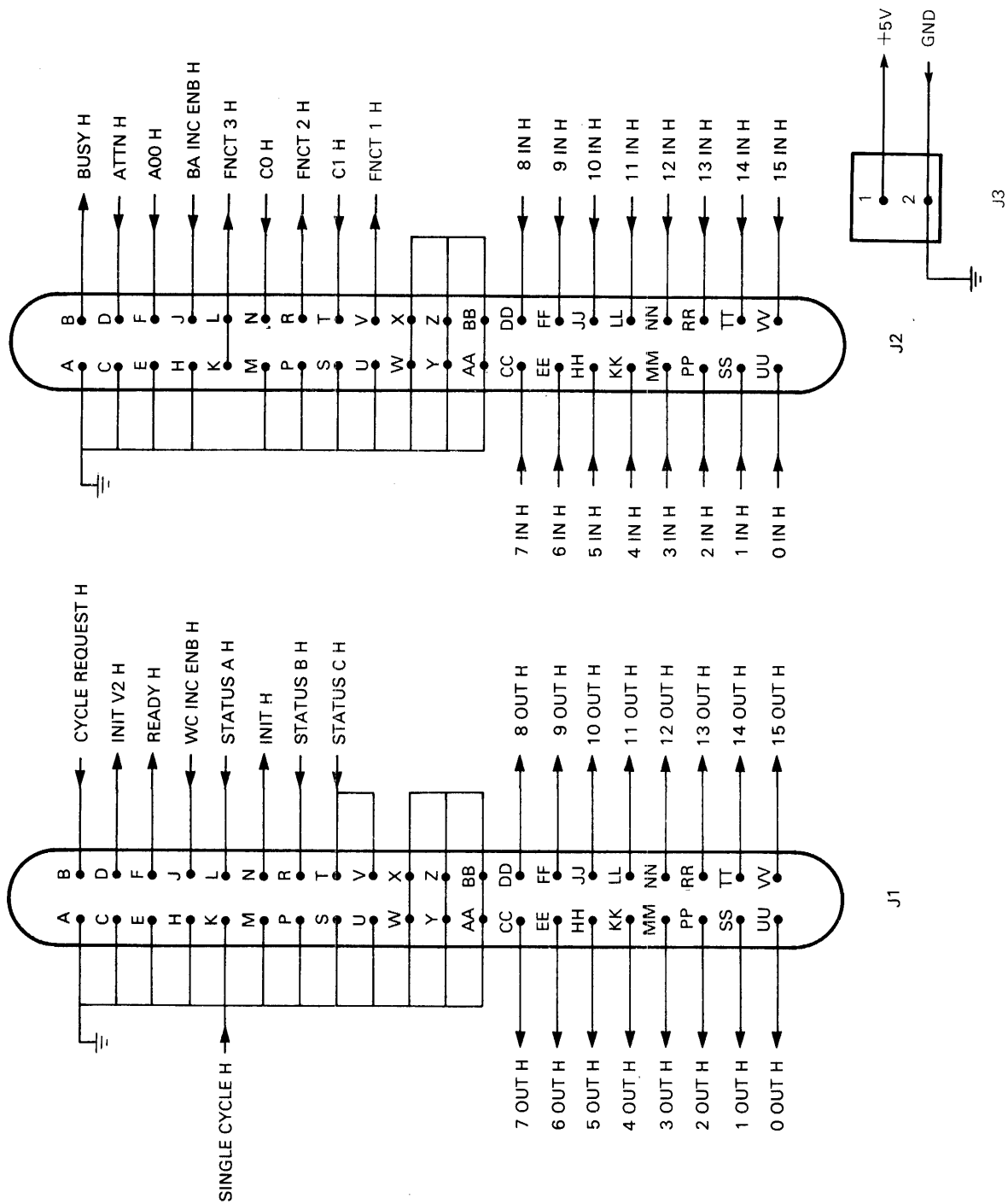
R = Removed
I = Installed

2.5 MODULE INSTALLATION

The type of CPU and its current configuration determines which of the following procedures must be performed.

2.5.1 Installing the DRV11-WA in an LSI-11 CPU

With the exception of the first two/four slots (the LSI-11 processor always occupies the first two/four slots depending on CPU type), the DRV11-WA can be installed into any Q22 slot (see Section 2.2.4) of the LSI-11 backplane. However, if REV11 DMA refresh option is used, the DRV11-WA must be at a lower priority than the REV11. When inserting the module into the backplane, make sure that the deep notch on the module seats against the connector block rib. Do not insert or remove the module with power applied. After performing the initial turn-on (see Section 2.8), connect the user's I/O cables to J1 and J2 on the DRV11-WA I/O connectors. Connector locations for the DRV11-WA are shown in Figure 2-1. Pin assignments for J1 and J2 are shown in Figure 2-4 and are specified in Chapter 1, Section 1.2.



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Figure 2-4 DRV11-WA Connector Pin Assignments

2.5.2 Installing the DRV11-WA in the BA23 Enclosure (MICRO-11/MicroVAX)

1. Remove the ac power cable from the wall outlet.
2. Remove the rear cover and all external cables. Label all cables for reinstallation later.
3. Loosen the two screws retaining the rear I/O panel assembly. Swing the assembly open and remove both retaining straps.
4. Disconnect any internal cables attached to the back of the I/O panel assembly. Note their specific location and the orientation of the connector on each cable. Remove the rear I/O panel assembly.
5. Set the device and vector address switches and desired jumper options (refer to Section 2.4).
6. Connect the BC08R-XX ribbon cables from J1 and J2 on the module to the insert connector assemblies on the I/O panel. Label the insert connectors for connection to the user's I/O cables later.
7. When installing the DRV11-WA in the BA23 enclosure, observe the configuration rules and guidelines outline in the CPU technical manual(s).

Slide the module into the appropriate backplane slot.

8. Reconnect any internal cables removed from the I/O panel.
9. Replace the retaining straps and swing the I/O panel closed. Tighten the two panel retaining screws.
10. Do not replace the rear cover at this time. Replace all external cables.
11. Connect the ac power cord.
12. Perform the initial turn-on procedures (Section 2.6).
13. Connect the user I/O cables to the insert connector assemblies on the I/O panel.
14. Replace the rear cover.

2.5.3 Installing the DRV11-WA in the BA123 Enclosure (MICRO-11/ MicroVAX)

1. Remove the ac power cable from the wall outlet.
2. Open the rear door.
3. Loosen the captive screw that fastens the right-side panel to the rear of the enclosure frame.
4. Pull out on the bottom of the right-side panel until it releases from the two snap fasteners holding it to the bottom of the frame.
5. Lift the panel far enough to release it from the slot in the lip at the top of the frame.
6. Release the clasps at the front of the card-cage door, swing the door open, and remove it.
7. Set the device and vector address switches and desired jumper options (refer to Section 2.4).
8. Connect the BC08R-XX ribbon cables from J1 and J2 on the module to the insert connector assemblies on the I/O panel. Label the insert connectors for connection to the user's I/O cables later.
9. When installing the DRV11-WA in the B123 enclosure, observe the configuration rules and guidelines outlined in the CPU technical manual(s).

Slide the module into the appropriate backplane slot.

10. Do not replace the card-cage door or right-side panel at this time.
11. Connect the ac power cord.
12. Perform the initial turn-on procedures (Section 2.6).
13. Connect the user I/O cables to the insert connector assemblies on the I/O panel.
14. Replace the card-cage door and the right-side panel, reversing steps 2 through 6 of this section.

2.6 INITIAL TURN-ON

After completing the module installation, turn-on the LSI-11/MicroVAX and initialize the system. With no I/O cables connected and using the console terminal and operating procedures, perform the following quick operational verification.

LSI-11

1. Load the addresses of the WCR, BAR, CSR, AND DBRs through the system terminal and examine the locations. The terminal will indicate the following:

22-Bit	18-Bit
WCR contents will be 000000	WCR contents will be 000000
BAR contents will be 000001	BAR contents will be 000001
BAE contents will be 100000	
CSR contents will be 127200	CSR contents will be 127200
DBR contents will be 177777	DBR contents will be 177777

2. The WCR, BAR, and BAE (if 22 bit addressing is selected) can be loaded with data from the system terminal and the corresponding data read back on the terminal. BAR bit 0 will read as a one (1) with no I/O cables connected.

NOTE

BAE (ADDRESS xxxxx2) is read by first examining the BAR (ADDRESS xxxxx2) and then examining ADDRESS xxxxx2 again to access the BAE.

MicroVAX

1. Enter MicroVAX console mode (see MicroVAX Owner's Manual). The console mode prompt is ">>>".
2. Examine the addresses of the WCR, BAR, CSR, and DBRs (refer to Section 2.4.1) through the system console using the console-mode commands shown in Example 2-1. This example shows the expected contents of the registers, assuming the assigned base device address for the module is used. The hex addresses used in the example were determined as follows:

22-bit register address:		3FF5nn
22-bit I/O space base address:	-	3FE000
I/O address offset:		15nn
32-bit I/O space select (bit 29):	+	20000000
32-bit physical register address:		200015nn

>>> E/W/P 20001508<Return>	!WCR
P 20001508 0000	! " contents
>>> E/W/P 2000150A<Return>	!BAR
P 2000150A 0001	! " contents
>>> E/W/P 2000150A<Return>	!BAE
P 2000150A 8000	! " contents
>>> E/W/P 2000150C<Return>	!CSR
P 2000150C AE80	! " contents
>>> E/W/P 2000150E<Return>	!DBRs
P 2000150E FFFF	! " contents

Example 2-1 Module Register Check on MicroVAX

NOTE

For an explanation of the MicroVAX console commands, refer to the MicroVAX Technical Manual(s).

The user's I/O device cables can now be connected to the DRV11-WA (Figure 2-1).

2.7 DIAGNOSTIC PROGRAM - LSI-11

The check procedure performed in Section 2.6 does not completely verify the operation of the DRV11-WA. Complete module operation can be verified through the use of the diagnostic software program AC-T974C-MC. The program can be loaded into the LSI-11 system by means of any standard loadable device. A BC05L or BC06R maintenance cable (not longer than 25 ft) is required to loop the DBR output to the DBR input for checking the I/O data path. A complete description of the diagnostic software program and its implementation is provided in AC-T974C-MC.

When you execute the AC-T974C-MC diagnostic, you must select software Switch 12 (SW12) of the SWR to correspond with your selection of hardware Switch 10-E40. SW12 must be ON (ON=1) to enable 22-bit address testing, or OFF (OFF=0) to enable 18-bit address testing. The default setting is OFF.

S10-E40

SW12 of Diagnostic

ON = 22-bit addressing
OFF = 18-bit addressing

ON = Enable 22-bit address testing
OFF = Disable 22-bit address testing

The diagnostic will continue to run until it is terminated with a control character.

2.8 DIAGNOSTIC PROGRAM - MicroVAX

The DRV11-WA MicroVAX diagnostic is called NADRAE and runs under MDM (MicroVAX Diagnostic Monitor). The diagnostic comprises the tests listed in Table 2-5.

Table 2-5 DRV11-WA Diagnostic Tests

Test	Function/Component Tested
1	WCR (Word Count Register)
2	BAR (Bus Address Register)
3	BAE (Extended Bus Address Register)
4	CSR (Control and Status Register)
5	CSR Byte/Word addressing and interrupts
6	CSR GO, READY, FUNCTION 1:3, and STATUS A:C bits
7	Read/Write to the DBR (Data Buffer Registers)
8	READY controls BAR BIT 0
9	DBR is clocked by the cycle bit
10	Memory to device single-word transfers (DATI) Device to memory single-word transfers (DATO)
11	Memory to device multiple-word transfers Device to memory multiple-word transfers
12	Memory to device multiple-word burst mode transfers Device to memory multiple-word burst mode transfers
13	Maintenance bit control of C1 and single cycle
14	NXM (Non-existent memory) bit functionality
15	NPR transfers in maintenance mode

The MDM VERIFY mode (see Example 2-2) runs tests 1 through 4, and requires no loopback. SERVICE mode runs all 15 tests, and requires the digital loopback to be installed. The loopback should be installed at the bulkhead panel, connecting output (J1) to input (J2).

2.8.1 Running MDM

The DRV11-WA MicroVAX diagnostic is supplied as one of the diagnostics on the MDM diskette or tape. Each media requires a different boot procedure, described in detail in Chapter 1 of the appropriate MicroVAX II Technical Manual(s) (Table H-3, page H-2). Briefly, the boot procedures are as follows.

2.8.1.1 MDM Diskette Boot --

1. Insert the MDM diskette in diskette drive 1.
2. Set the MicroVAX II power switch to 1 (turn power on), or press RESTART. The diagnostic will boot as follows:
 - a. If Halts are disabled, the diagnostic will boot automatically.

- b. If Halts are enabled, the MicroVAX II will enter console mode and display the console prompt. Manually boot the diagnostic from DUAL:

>>> B DUAL

3. Several information screens will be displayed followed by prompts to enter date and time, to insert the remaining diskettes, and to continue. Respond to the prompts.
4. The MAIN MENU will then be displayed:
 - Select item #4 to display the Service Menu.
 - Select item #4 to enter system commands.
5. The MDM prompt will then be displayed:

MDM>>

Examples 2-2 through 2-5 show the MDM commands and how they are used.

2.8.1.2 MDM Tape Boot --

1. Push the Fixed-disk 0 Ready pushbutton(s) to place the fixed-disk unit(s) off-line.
2. Set the MicroVAX II power switch to 1 (turn power on).
3. Insert the MDM tape cartridge into tape drive 1.
4. Push the Load/Unload pushbutton. The diagnostic will boot as follows:
 - a. If Halts are disabled, the diagnostic will boot automatically.
 - b. If Halts are enabled, the MicroVAX II will enter console mode and display the console prompt. Manually boot the diagnostic from MUA0:

>>> B MUA0

5. Several information screens will be displayed followed by prompts to enter date and time, and to continue. Respond to the prompts.
6. The MAIN MENU will then be displayed:
 - Select item #4 to display the Service Menu.
 - Select item #4 to enter system commands.

7. The MDM prompt will then be displayed:

MDM>>>

Examples 2-2 through 2-5 show the MDM commands and how they are used.

2.8.1.3 MDM Examples -- Example 2-2 shows how the HELP command is entered to display a list of current MDM commands.

MDM>> HELP<Return>

Current Commands are:

CONFIGURE	- Configure system
SELECT Diag_name	- Select a diagnostic (all units) to run
DISABLE Diag_name	- Prevent a diagnostic from running
ENABLE Diag_name	- Allow a diagnostic to run
SET DETAILED ON	- Display detailed messages
DETAILED OFF	- DO NOT display detailed messages
MODE VERIFY	- Set verify mode tests
SERVICE	- Set service mode tests
PROGRESS OFF	- Display no progress messages
PROGRESS BRIEF	- Controller progress messages
PROGRESS FULL	- Controller and test progress messages
SECTION FUNCTIONAL	- Set functional test section
UTILITY	- Set utility test section
EXERCISER	- Set exerciser test section
TEST ALL	- Run all enabled tests
xx	- Run only test number xx
PASSES xx	- Run tests for xx passes
START	- Start selected tests running
START ALL	- Start all enabled tests running
SHOW CONFIGURATION	- Show system configuration information
SHOW DEFAULT	- Show default settings
SHOW DEVICE UTILITIES	- Show utility titles
SHOW ERRORS	- Show reported errors

MDM>>

Example 2-2 MDM HELP Command

Example 2-3 shows the defaults for the DRV11-WA diagnostic. Note that commands can be abbreviated by typing only enough of the command to uniquely identify it. For example, typing SH DEF is the same as typing SHOW DEFAULT.

```
MDM>> CONFIG<Return>
```

```
MDM>> SHOW CONFIG<Return>
```

```
MDM>> SEL DRV11WA<Return>
```

```
MDM>> SH DEF<Return>
```

```
Selected device:
 1  DRV11WA Enabled
Mode is SERVICE
Selection is FUNCTIONAL
Number of passes is: 1
No time limit
Tests to be run: ALL
Continue on error
Detailed message is Off
Progress message is Off
MDM>>
```

Example 2-3 MDM SHOW DEFAULT Command

The SHOW DEFAULT command shows the current setting of default parameters. The "real" defaults (shown in Example 2-3) are listed only when the diagnostic is first booted and no parameters are changed with MDM commands. The parameter of a specific command can only be changed by entering the command with a new parameter. For example, the default test SECTION is FUNCTIONAL and can only be changed by typing either:

```
MDM>> SET SEC UT
```

or

```
MDM>> SET SEC EX
```

Example 2-4 shows the commands to run the full set of functional tests.

MDM>> CONFIG<Return>

MDM>> SEL DRV11WA<Return>

MDM>> SET PROG FULL<Return>

MDM>> SET DET ON <Return>

MDM>> SET MODE SERVICE<Return>

MDM>> SET SECT FUNCTIONAL<Return>

MDM>> ST<Return>

DRV11WA started.

 Please follow instructions carefully!

 All testing will be done from the bulkhead

 Please attach loopback cable from output (J1)
 to input (J2) CKDRV1-KA connector

 Press RETURN when completed...

 Thank you, you may continue your testing

DRV11WA pass 1 test number 1 started.

DRV11WA pass 1 test number 2 started.

DRV11WA pass 1 test number 3 started.

DRV11WA pass 1 test number 4 started.

DRV11WA pass 1 test number 5 started.

DRV11WA pass 1 test number 6 started.

DRV11WA pass 1 test number 7 started.

DRV11WA pass 1 test number 8 started.

DRV11WA pass 1 test number 9 started.

DRV11WA pass 1 test number 10 started.

 Start of DATI section of test

 Start of DATO section of test

DRV11WA pass 1 test number 11 started.

 Start of DATI section of test

 Start of DATO section of test

DRV11WA pass 1 test number 12 started.

 Start of DATI section of test

 Start of DATO section of test

DRV11WA pass 1 test number 13 started.

DRV11WA pass 1 test number 14 started.

 Start of DATI section of test

 Start of DATO section of test

DRV11WA pass 1 test number 15 started.

 Start of DATI section of test

DRV11WA passed.

MDM>>

Example 2-5 shows how the UTILITY section is run.

```
MDM>> CONFIG<Return>
MDM>> SEL DRV11WA<Return>
MDM>> SET DET ON<Return>
MDM>> SET PROG BRIEF<Return>
MDM>> SET MODE SERVICE<Return>
MDM>> SET SECT UTILITY<Return>
MDM>> ST<Return>
DRV11WA started.

DRV11WA pass 1 - test number 1 started.

DRV11WA passed.

MDM>>
```

Example 2-5 MDM Commands to Run the UTILITY Section

NOTE

To run the UTILITY Section, SERVICE Mode must be set and the digital loopback must be installed.

3.1 GENERAL

This chapter contains a functional description of the DRV11-WA. The DRV11-WA registers are described as well as user device and bus operations necessary to perform DMA transfers. Figure 3-1 is a block diagram of the DRV11-WA. All descriptions are written to this diagram. The chapter ends with a brief description of the timing associated with DMA transfers.

3.2 FUNCTIONAL DESCRIPTION

3.2.1 DRV11-WA Registers

The DRV11-WA contains six registers:

- Word Count Register (WCR),
- Bus Address Register (BAR),
- Extended Bus Address Register (BAE),
- Control Status Register (CSR), and
- Input and Output Data Buffer Registers (DBRs).

3.2.1.1 Word Count Register (WCR) -- The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement (negative number) of the number of words to be transferred. At the end of each transfer, the word count register is incremented (if WC INC ENB is high). When the contents of the WCR is incremented to zero, transfers are terminated, READY is set, and if the interrupt enable bit is set, an interrupt is requested. The WCR is word-addressable only.

3.2.1.2 Bus Address Register (BAR) -- The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including address bit 0) that specifies the location to or from which data is to be transferred. The BAR is incremented after each transfer (if BA INC ENB is high), and can be incremented across 32K memory boundaries by means of the extended address feature of the DRV11-WA. Systems with only 16 address bits will "wrap-around" to location zero when the extended address bits are incremented. On systems with extended addressing, an overflow in the BAR will increment the XA16, XA17 bits in the CSR when in Q18 mode or the BAE register when in Q22 mode. The BAR is word-addressable only.

3.2.1.3 Extended Bus Address Register (BAE) -- The BAE is a 6-bit read/write register accessible when extended addressing mode (Q22) is selected. This register is loaded (under program control) with bits 16-21 of a bus address that specifies the location to or from which data is to be transferred. If the BAR overflows, it will increment the extended address bits in Q22 mode. The BAE is word-addressable only.

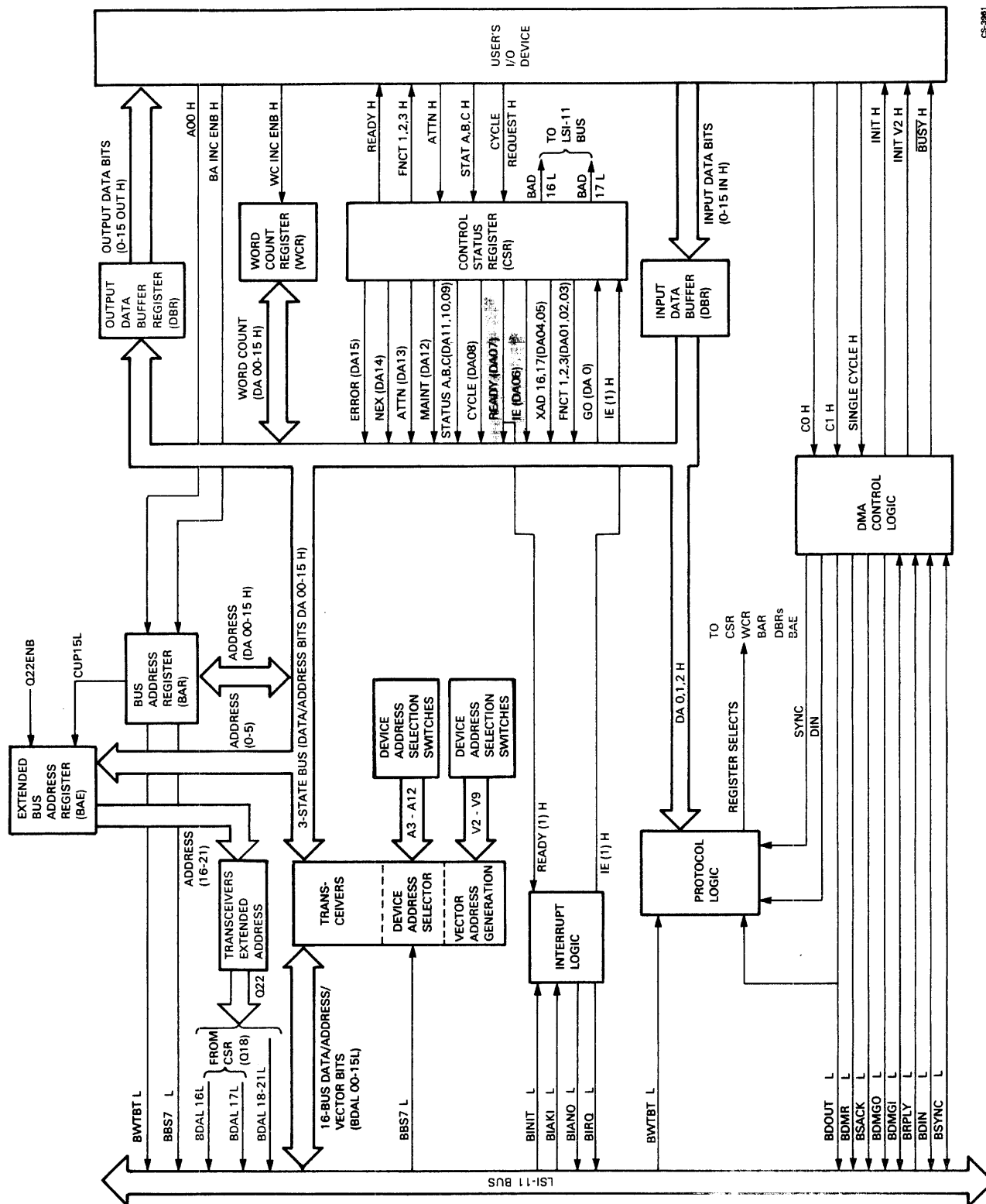


Figure 3-1 DRV11-WA Block Diagram

3.2.1.4 Control/Status Register (CSR) -- The CSR is a 16-bit register used to control the functions and monitor the status of the interface. Bit 00 is a write-only bit and always reads as a zero. Bits 01-06, 08, and 12 are read/write bits, while bits 07, 09-11, and 13-15 are read-only bits. Bit 14 can be written to a zero. Bits 04 and 05 are the extended addressing bits. If extended address mode (Q22) is selected, bits 04 and 05 are read-only bits. CSR functions are fully described in Chapter 4. The CSR is both byte- and word-addressable.

3.2.1.5 Input and Output Data Buffer Registers (DBRs) -- The two DBRs are 16-bit registers. The input DBR is a read-only register; the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred to memory under DMA control by the DRV11-WA, or under program control by the Q-bus processor. Conversely, data is written into the output DBR from memory under DMA control by the DRV11-WA, or under program control by the Q-bus processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

3.2.2 User Interface Lines

There are 50 interface lines (25 per connector) between the DRV11-WA and the user's I/O device. Of these lines, 32 are I/O data lines, three are for status, and 15 are for control. A brief description of these interface lines follows.

Mnemonic	Description
00 OUT - 15 OUT	16 TTL data output lines from the DRV11-WA. One = high. Correspond to ODBR <00:15>.
00 IN - 15 IN	16 TTL data input lines from the user's device. One = high. Correspond to IDBR <00:15>.
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user. Correspond to CSR <09:11> (Table 4-1).
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user. Correspond to CSR <01:03> (Table 4-1).
INIT	One TTL output line; used to initialize the user's device.

Mnemonic	Description
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.
A00	One TTL input line from the user's device. This line is normally low for word transfers. During byte transfers this line controls address bit 00.
<u>BUSY</u>	One TTL output line to the user's device. BUSY is low when the DRV11-WA DMA control logic is requesting control of the Q-bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low, DMA transfers may be initiated by the user's device.
C0, C1	Two TTL input lines from the user's device. These lines control the Q-bus cycle for DMA transfers. C0 and C1 codes for the four possible bus cycles are listed as follows.

C0 and C1 Codes

Bus Cycle	C0	C1
DATI	0	0
DATI0	1	0
DATO	0	1
DATOB	1	1

SINGLE CYCLE	One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation, SINGLE CYCLE is driven low by the user's device.
--------------	---

CAUTION

When SINGLE CYCLE is driven low, total system operation is affected because the Q-bus becomes dedicated to the DMA device; other devices, including the MOS memory refresh function, cannot use the bus.

WC INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-WA word counter. Low inhibits incrementing.
------------	--

Mnemonic	Description
BA INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.
CYCLE REQUEST	One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.
ATTN	One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY, and request an interrupt if the interrupt enable bit is set. This line must be low to execute DMA transfers. Corresponds to CSR <13> (Table 4-1).

3.2.3 LSI-11 Bus Lines

There are 38 LSI-11 bus signal lines used by the DRV11-WA; 16 of these are multiplexed and bidirectional lines that carry data and address bits. Six lines are used for extended address bits, while 16 lines are used for control signals. A brief description of the 38 bus lines follows.

Mnemonic	Description
BDAL 0 - BDAL 15	16 bus data/address lines. An address is first placed on these lines followed by the data. These lines are asserted when driven low.
BDAL 16, 17	Two bus lines used to address beyond 32K of memory by the DRV11-WA. These lines are asserted when low.
BDAL 18-21	Four bus lines used to address beyond 128K of memory. These lines are asserted when low.
BDOUT	One bus line; when asserted (low), indicates that data is available on the BDAL lines and an output transfer (with respect to the bus master) is taking place.
BRPLY	One bus line; asserted (low) in response to BDIN or BDOUT and in response to BIAK transactions. It is generated by the slave device for address recognition.

Mnemonic	Description
BDIN	One bus line; when asserted (low) during BSYNC time, indicates an input transfer (with respect to the bus master). Requires a BRPLY response. BDIN is asserted when the bus master is ready to accept data from the slave. When asserted without BSYNC, indicates that an interrupt operation is occurring.
BSYNC	One bus line; asserted (low) by the bus master to indicate that it has placed an address on the BDAL lines. The transfer is in progress until BSYNC is negated (high).
BWTBT	One bus line; asserted (low) during address time to indicate that an output sequence (DATO or DATOB) is to follow. BWTBT is also asserted during data time for byte addressing during a DATOB.
BIRQ	One bus line; device asserts (low) this line when its interrupt enable, interrupt request, and ready flip-flops are set. BIRQ informs the LSI-11 processor that service is requested.
BIAKI, BIAKO	Two bus lines; one is interrupt acknowledge in, the other is interrupt acknowledge out. BIAKI is generated by the LSI-11 processor in response to BIRQ. The processor asserts (low) BIAKO which is routed to the BIAKI pin of the first device on the bus. If the device is not requesting an interrupt, BIAKO is passed (as BIAKI) to the next device.
BBS7	One bus line; asserted (low) by the LSI-11 processor when addressing a device for program-controlled transfers. The DRV11-WA can assert BBS7 and address other devices on the LSI-11 bus without processor intervention.
BDMGI, BDMGO	Two bus lines; one is DMA grant in, the other is DMA grant out. The LSI-11 processor generates BDMGO which is routed to the BDMGI pin of the first bus device. If the device is requesting the bus, it will inhibit passing BDMGO to the next bus device. If the device is not requesting the bus, it will pass BDMGO as (BDMGI) to the next device.

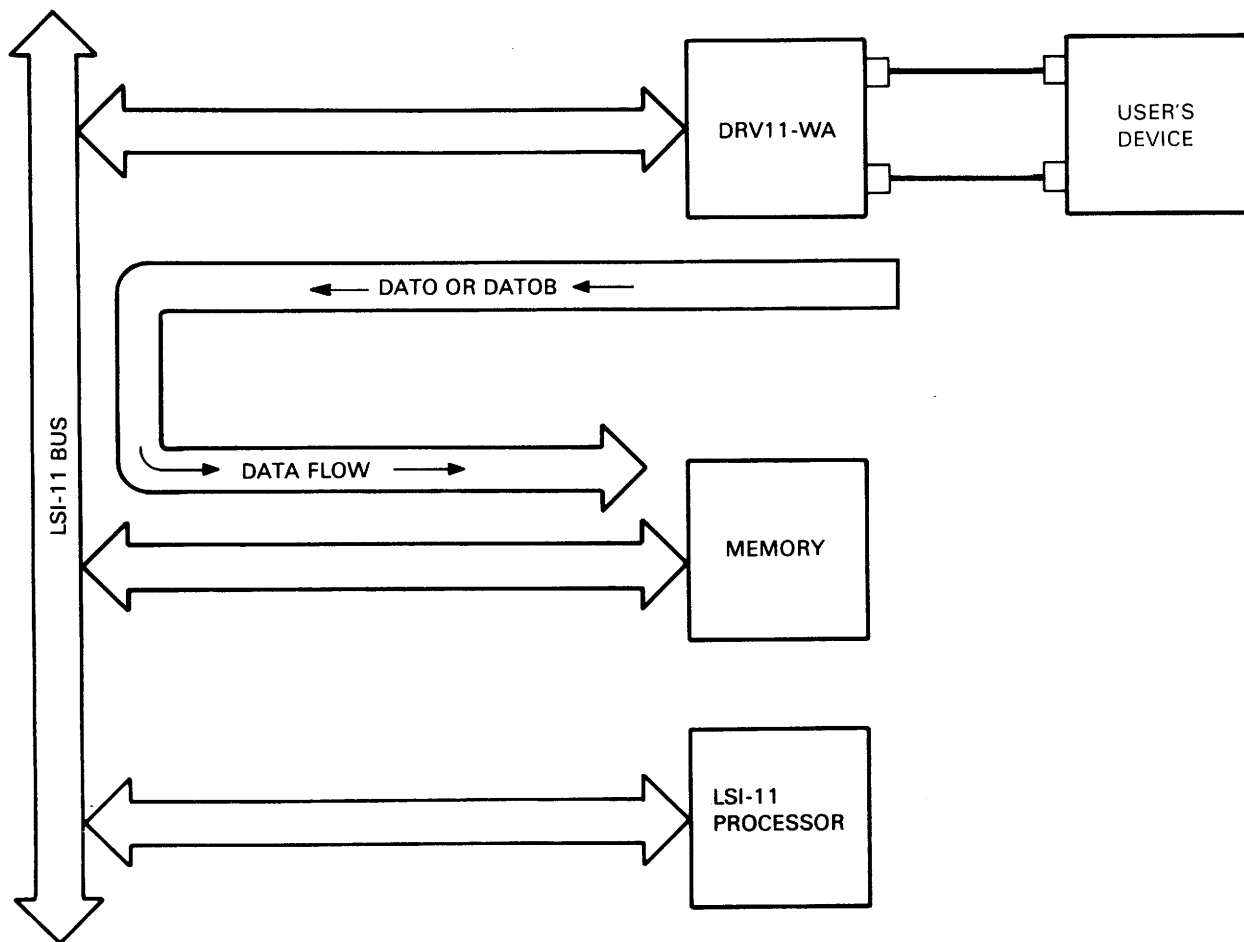
Mnemonic	Description
BINIT	One bus line; asserted (low) by the LSI-11 processor to initialize or clear devices connected to the LSI-11 bus.
BSACK	One bus line; BSACK is asserted (low) by a DMA device in response to the LSI-11 processor's BDMGO signal, indicating that the DMA device is bus master.
BDMR	One bus line; a device asserts this signal for DMA requests and to become bus master.

3.2.4 User's I/O Device to Q-Bus Memory Transfer (DATO or DATOB)
Data transfers from the user's I/O device to the Q-bus memory are DMA transfers. Figure 3-2 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 3-1, DMA transfers are initialized under program control by loading the DRV11-WA WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR (and BAE if Q22 is selected) with the starting memory address for word storage; and setting the CSR for transfers.

The user's I/O device must set ATTN low (ZERO), then the GO bit of the CSR is written to a "one", READY goes low and the user's I/O device conditions the A00, BA INC ENB, WC INC ENB, SINGLE CYCLE (high for normal DMA transfers), and the C0, C1 lines (refer to Section 3.2.2), and then asserts CYCLE REQUEST. The INPUT DATA BITS and control bits (C0, C1 and SINGLE CYCLE, BA INC ENABLE, WC INC ENABLE) are latched into the respective DRV11-WA registers (at the high-to-low transition of BUSY). CYCLE REQUEST sets CYCLE and causes the DRV11-WA to assert BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-WA becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

As bus master, the DRV11-WA performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The LSI-11 memory decodes the address; then, the DRV11-WA removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB) and then places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-WA negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus is released when the DRV11-WA negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-WA WCR and BAR are incremented (for normal DMA transfers), BUSY goes high, while READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST. DMA transfers can continue until the WCR increments to zero and generates an interrupt request, if the interrupt enable bit is set.



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Figure 3-2 DMA DATO/DATOB Data Flow Diagram

3.2.4.1 Interrupts -- When the WCR increments to zero, READY goes high and the DRV11-WA generates an interrupt request (if the interrupt circuits are enabled). The Q-bus processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-WA and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The Q-bus processor receives the vector address and negates BDIN and BIAKI. The DRV11-WA now negates BRPLY, while the processor exits from the main program and enters a service program for the DRV11-WA as indicated by the vector address.

Interrupt requests from the DRV11-WA occur for the following conditions:

1. When the WCR increments to zero. This is a normal interrupt at the end of a designated number of transfers.
2. When the user's I/O device asserts ATTN. This is a special condition interrupt which overrides the WCR or, if the independent interrupt jumper is installed, may independently cause interrupts.
3. When a non-existent memory location is addressed by the DRV11-WA. This condition interrupt is produced when no BRPLY is received from the Q-Bus memory.

Interrupts are explained in greater detail in Chapter 4 of this manual.

NOTE

As of module CS Revision C, the DRV11-WA module will no longer generate an interrupt if the IE bit of the CSR is written to a one without simultaneously setting the GO bit. In earlier module revisions, setting the IE bit without setting the GO bit simultaneously would generate a spurious interrupt. Software written to ignore this first interrupt should be modified to process the interrupt.

3.2.5 Q-Bus Memory to User's Device Transfers (DATIO or DATI)

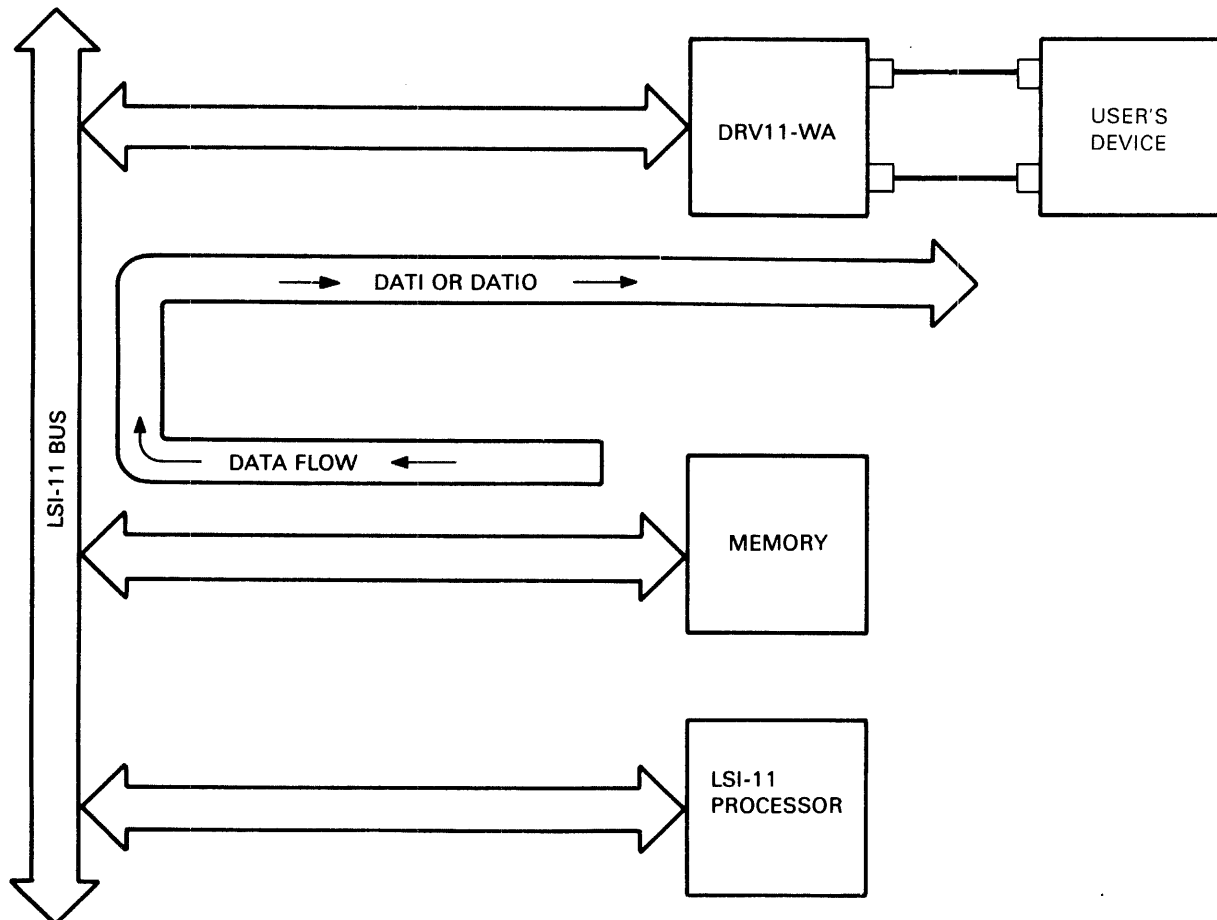
DMA transfers from the Q-Bus memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 3-3 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-WA WCR (Figure 3-1) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come. The CSR is set for transfers.

The user's I/O device must set ATTN low (zero). Then, with the CSR set, READY goes low and the user's I/O device conditions the C0, C1 lines (refer to Section 3.2.2) for a DATI or a DATIO, and conditions the WC INC ENB, BA INC END, SINGLE CYCLE (high for normal DMA transfers), and asserts CYCLE REQUEST. BUSY from the DRV11-WA goes low and the user's control bits are latched into the DRV11-WA. The DRV11-WA then asserts BDMR, which makes a bus request. When the request is arbitrated as described in Section 3.2.4, the DRV11-WA becomes bus master.

When the DRV11-WA becomes bus master, a DATI or DATIO bus cycle is performed (the following describes a DATI). The DRV11-WA places the address of the memory location from which the first word is taken on the BDAL lines and asserts BSYNC. Memory decodes and

latches the address. The DRV11-WA then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-WA and BDIN is negated. Memory negates BRPLY and the DRV11-WA negates BSACK and BSYNC to terminate the bus cycle and release the bus. The OUTPUT DATA BITS for the user's I/O device are stored in the DRV11-WA output data buffer register. These bits can be read by the user's device at the low-to-high transition of BUSY.

At the end of the first transfer, the DRV11-WA WCR and BAR (or BAE, if extended addressing is selected) are incremented, BUSY goes high, while READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated (see Section 3.2.4.1).

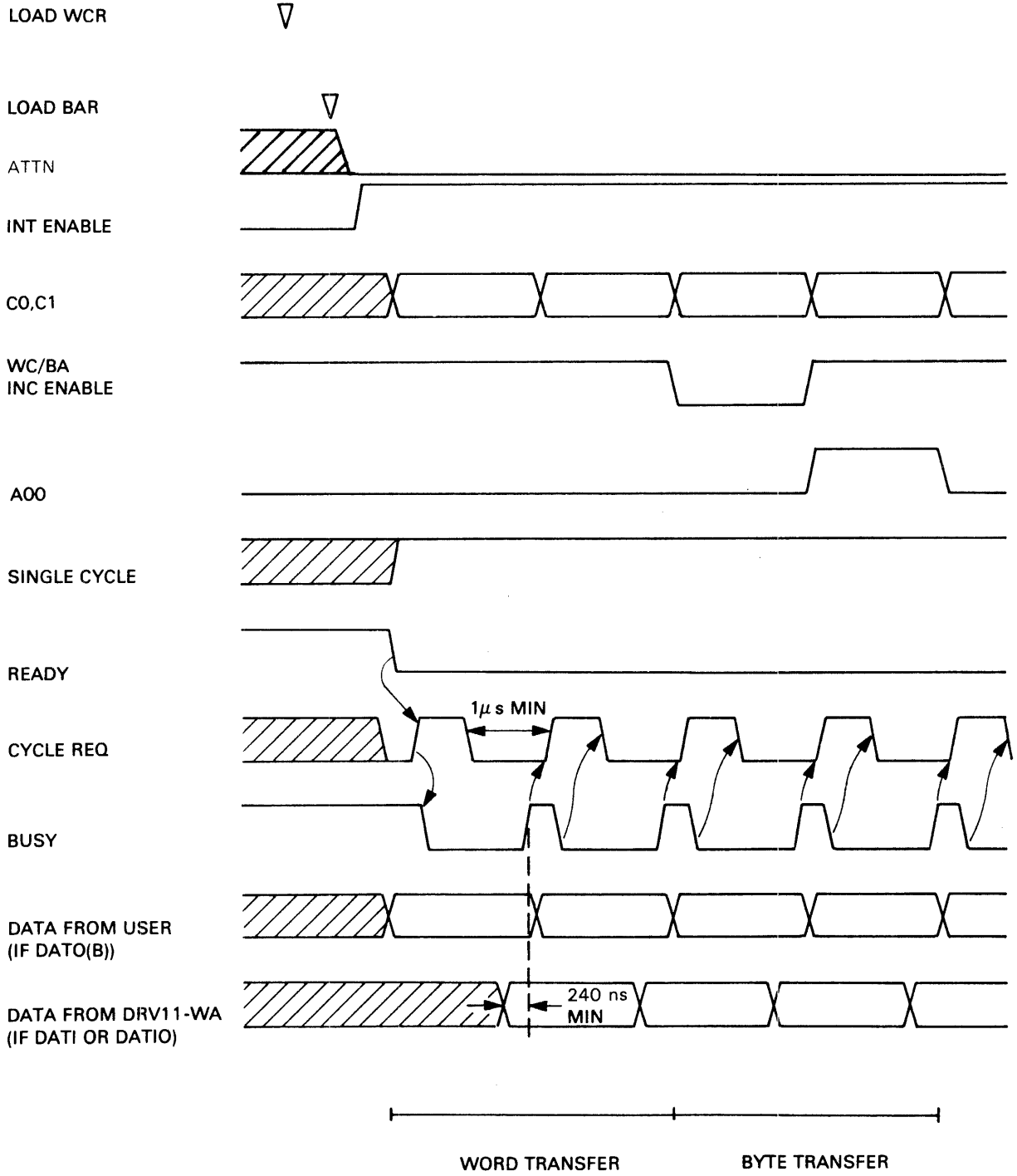


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Figure 3-3 DMA DATIO/DATI Data Flow Diagram

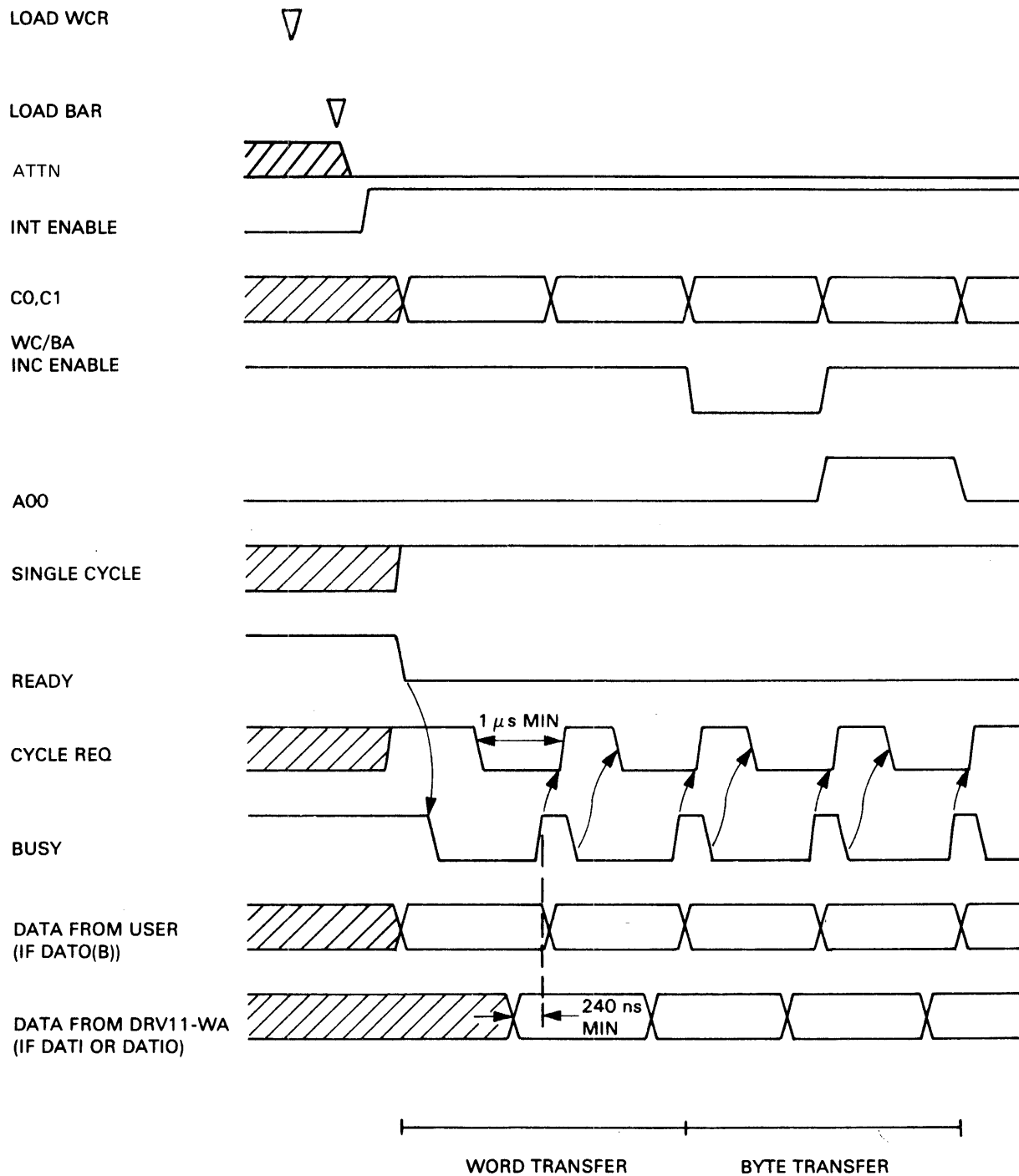
3.3 TIMING

Input and output timing for the DRV11-WA is shown in Figures 3-4 through 3-8. The timing diagrams show user signal timing for single cycle and burst mode operations which can be either program- or user-initiated.



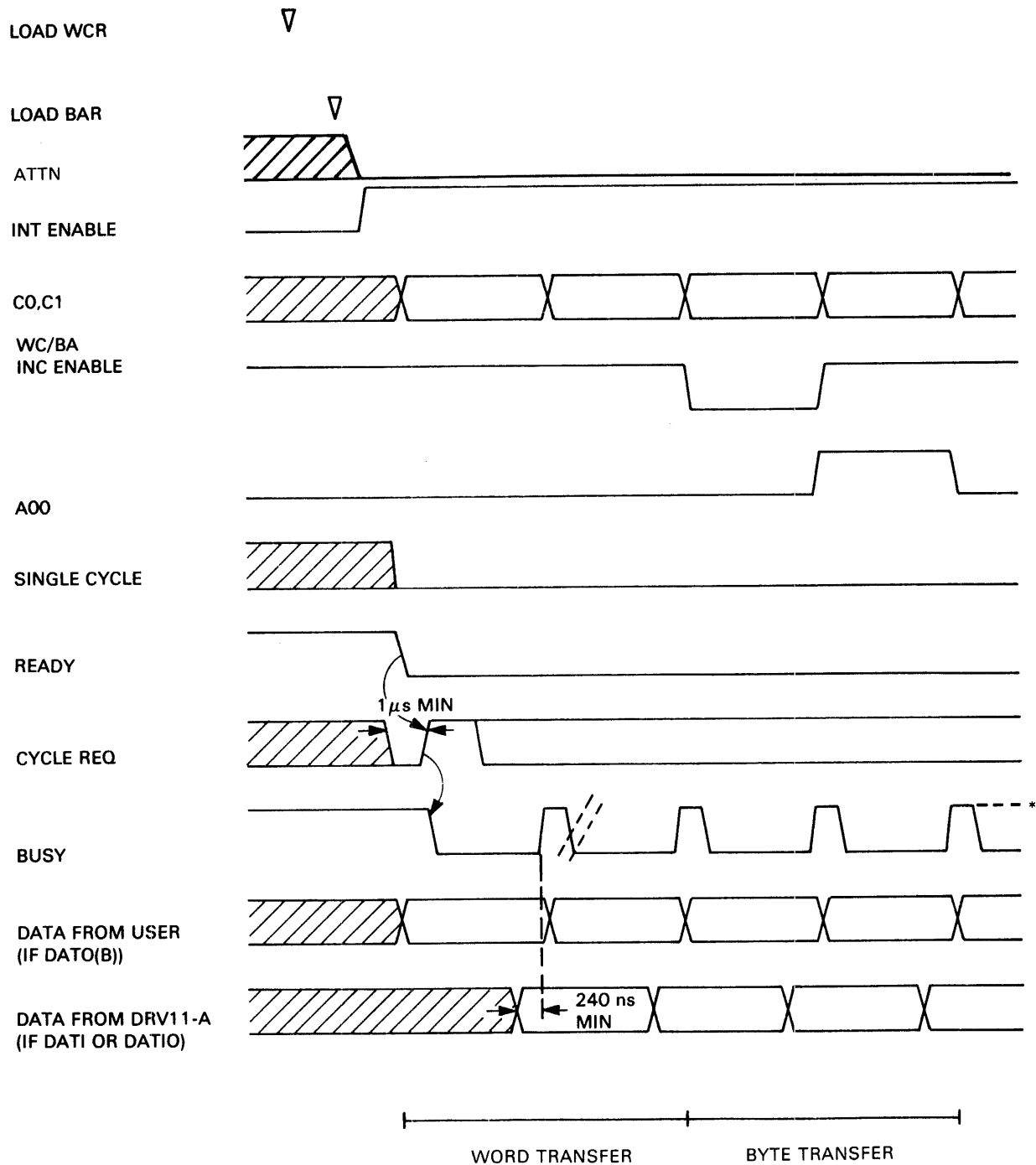
CS-4722

Figure 3-4 DRV11-WA Single Cycle, User-Initiated, Timing Diagram



CS-4723

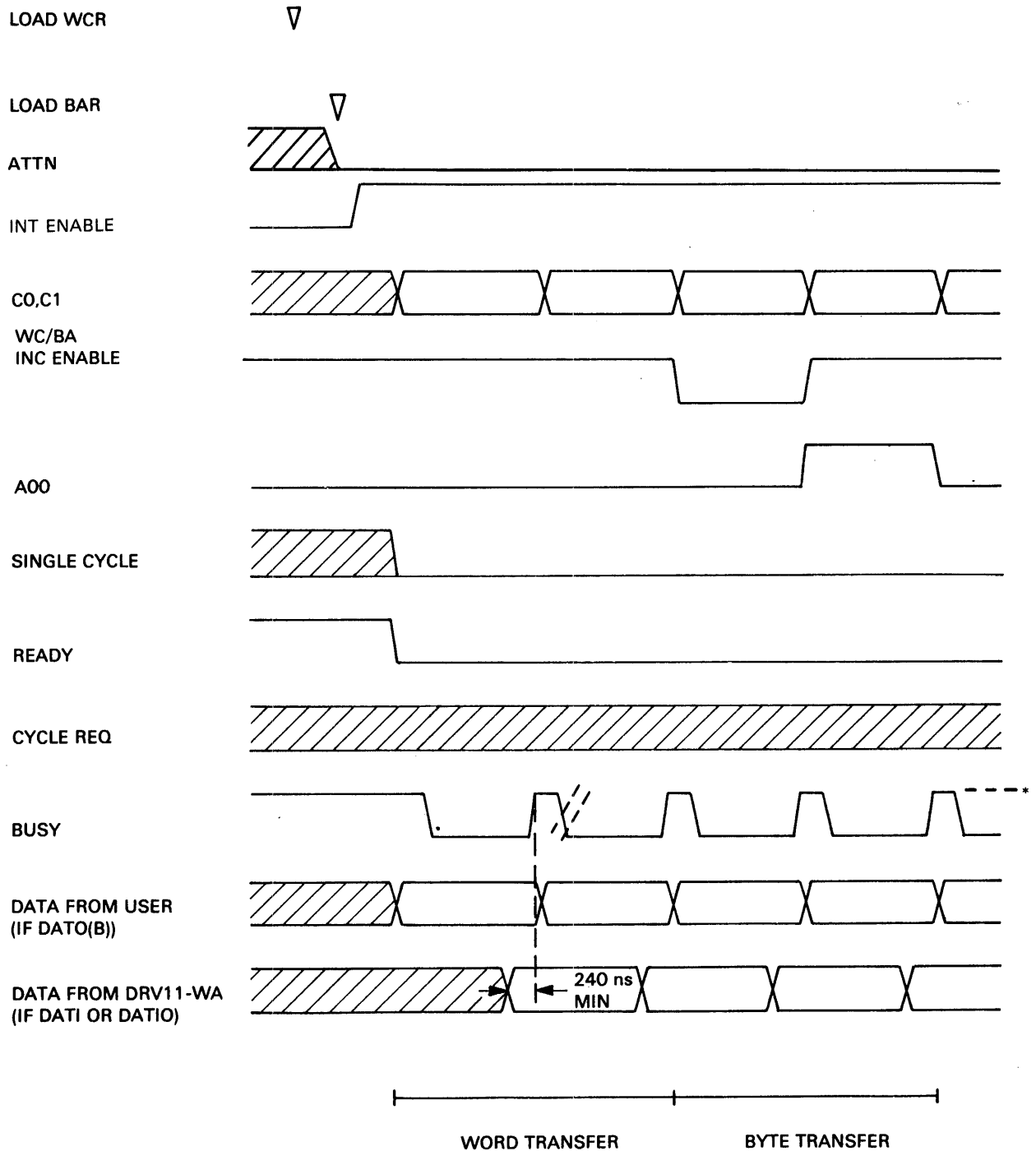
Figure 3-5 DRV11-WA Single Cycle, Program-Initiated, Timing Diagram



* NOTE: If W2 jumper is installed, the DRV11-WA will relinquish bus mastership and re-request mastership after every four words transferred.

CS-4724

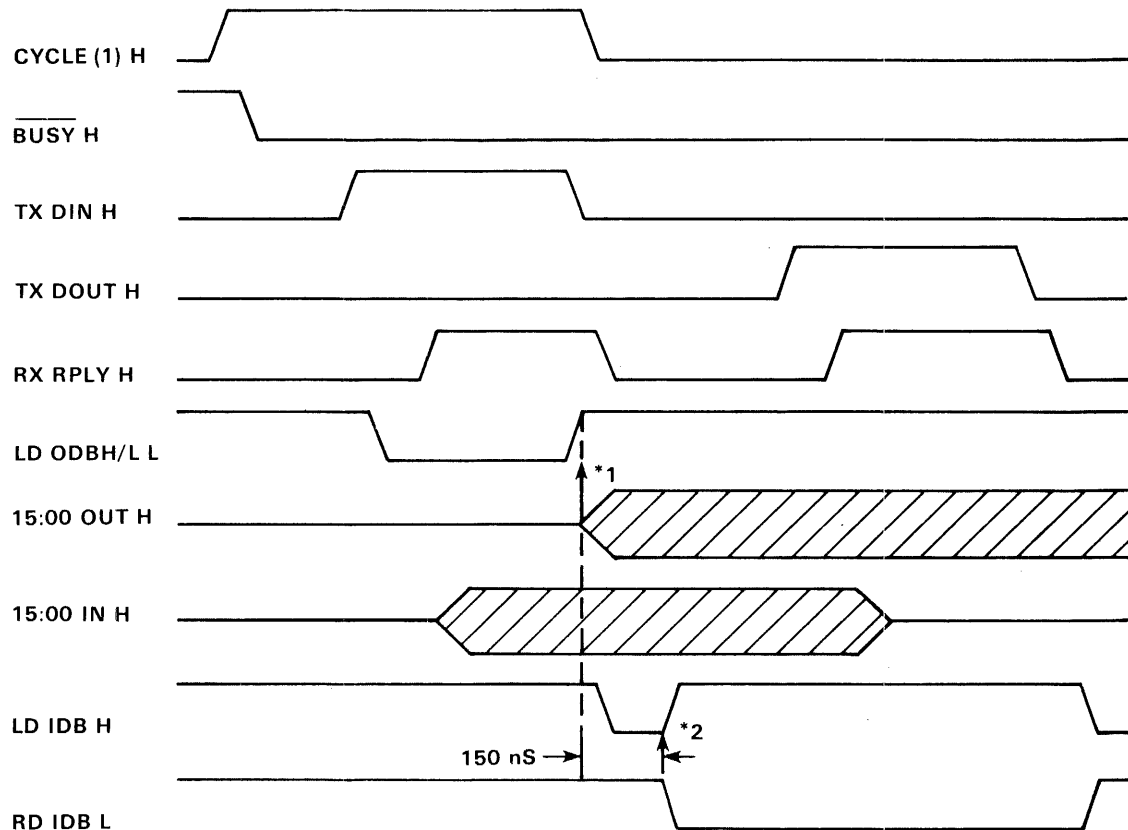
Figure 3-6 DRV11-WA Burst Mode, User-Initiated, Timing Diagram



* NOTE: IF W2 jumper is installed, the DRV11-WA will relinquish bus mastership and re-request mastership after every four words transferred.

CS-4725

Figure 3-7 DRV11-WA Burst Mode, Program-Initiated, Timing Diagram



*1 : OUTPUT DATA (READ DATA FROM MEMORY) LATCH TIMING TO THE USER'S DEVICE (ODBR). DATA OUTPUT STARTS HERE.

*2 : READ DATA (WRITE TO MEMORY) INTERNAL LATCH TIMING (IDBR).

NOTE: *1 AND *2 CANNOT BE ACKNOWLEDGED FROM USER SIDE. TIMING FROM *1 TO *2 IS APPROXIMATELY 150 nS.

CS-4904

Figure 3-8 DRV11-WA DATIO Timing Diagram

4.1 GENERAL

This chapter presents basic programming information for the DRV11-WA. The types of programming instructions, the use of the registers, program interrupts, and special program considerations are presented.

4.2 PROGRAMMING INSTRUCTIONS

All programming instructions used for the Q-Bus processor may be used for programming the DRV11-WA.

4.3 DRV11-WA REGISTERS

Six registers are used by the DRV11-WA:

- Word Count (WCR),
- Bus Address (BAR),
- Extended Bus Address Register (BAE),
- Control/Status (CSR), and
- Input and Output Data Buffers (DBRs).

The input and output data buffer registers share the same bus address while WCR, BAR, and CSR have unique addresses. If extended addressing mode (Q22) is selected, the BAR and BAE share the same address. To access the BAE for reading/writing, you must first access the BAR. The BAR and BAE are read/written to alternately.

4.3.1 WCR

Load the 16-bit WCR with the 2's complement (negative number) of DMA data transfers. At the end of each DMA cycle, the WCR is incremented by one (if WC INC ENB is high). When the last transfer is made, the WCR is incremented to zero and an interrupt is requested. The WCR is not byte-addressable.

4.3.2 BAR

Load the 15-bit BAR with the address that specifies the memory location into which the first word is written, or from which the first word is read. Following the transfer of each word, the BAR is incremented by two, (if BA INC ENB is high) to point to the next higher sequential memory word location. In 18-bit mode, if the BAR overflows, it will increment the extended address bits in the CSR and "wrap-around" to location zero. In extended addressing (Q22) mode, if the BAR overflows, it will increment the BAE and "wrap-around" to location zero. Address bit A00 used for byte transfers, is driven by the user's device. The BAR is not byte-addressable.

4.3.3 BAE

If extended addressing mode (Q22) is selected, load the 6-bit BAE with the address that specifies the memory location into/from which the first word is written/read. If the BAR overflows, it will increment the BAE extended address bits and "wrap-around" to location zero. The BAE is not byte-addressable. As of module CS Revision C, BAE bit 15 will always read as a "one".

4.3.4 CSR

The 16-bit CSR is monitored for interface status and loaded with control bits. The CSR is byte-addressable. Figure 4-1 shows the CSR bit assignments. The function of each bit is described in Table 4-1.

4.3.5 DBRs

The DBRs hold the 16-bit data words for transfer to memory from the user's I/O device (input DBR), or from memory to the user's I/O drive (output DBR). Both DBRs share the same bus address and are word- and byte-addressable.

4.4 PROGRAM INTERRUPTS

DRV11-WA interrupts are enabled by setting bit 06 (IE) of the CSR (Figure 4-1 and Table 4-1). Interrupts can occur when the READY bit is set, or if independent interrupts are enabled when ATTN is set.

The READY bit is set when:

- Word count overflow (normal interrupt).
- CSR ERROR bit (bit 15) is set (special condition).

4.4.1 Word Count Overflow

An interrupt request is generated when the DRV11-WA WCR increments to zero and produces WC OFLO (word count overflow). WC OFLO sets READY in the CSR at the end of the DMA cycle.

4.4.2 CSR ERROR Bit (Bit 15)

The CSR ERROR bit can set for two possible reasons:

1. When bit 14 (NEX) of the CSR is set, or
2. When CSR bit 13 (ATTN) is set.

CSR bit 14 is set when a non-existent (NEX) memory location is addressed and a reply from the addressed location is not received within 20 μ s.

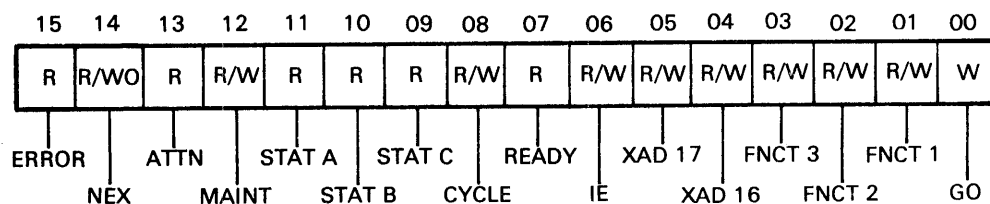
Bit 14 will set if a DAT0 bus cycle does not occur 20 μ s after performing a DAT10 bus cycle.

ATTN bit 13 sets the CSR ERROR bit when the user's I/O device drives ATTN high.

ATTN is a user-defined function that can be utilized to generate an independent interrupt request. When independent interrupts are enabled, an interrupt can be generated regardless of the state of READY.

4.5 FUNCTION AND STATUS BITS

There are three function bits (FNCT 1, 2, 3) and three status bits (STAT A, B, C), which the user can employ (at his option) to control and indicate the status of the DMA transfers and/or the user interface. The function bits (CSR bits 01, 02, and 03) can be used to transfer control data to the user's interface by means of the OUTPUT DATA BIT lines of the DRV11-WA. The status bits (CSR bits 09, 10, and 11) can be used to indicate the status information is on the DRV11-WA INPUT DATA BIT lines.



LEGEND:

R = READ ONLY
R/W = READ/WRITE
R/WO = READ/WRITE TO 0
W = WRITE ONLY. ALWAYS READS AS A 0.

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Figure 4-1 CSR Format

Table 4-1 CSR Bit Functions

Bit	Function
00	GO: Write-only bit; always reads as a zero. <ol style="list-style-type: none"> 1. Causes READY to be sent to the user's device, indicating that a command has been issued. 2. Allows DMA operation.
01, 02, 03	FNCT 1, 2, 3: Read/write bits. <ol style="list-style-type: none"> 1. Three output bits available for user-defined functions. 2. Cleared by INIT.

Table 4-1 CSR Bit Functions (Cont)

Bit	Function
04, 05	XAD16, 17: For standard Q-Buses (non-Q22). Read/write bits. Two bits used for extended addressing. Bits 04 and 05 increment with the address count when the BAR "wraps-around" to zero. For extended addressing Q-Buses, if extended addressing mode is selected, these bits are read-only.
06	IE: Read/write bit. <ol style="list-style-type: none"> 1. Enables interrupts to occur when READY is set. 2. Enables interrupts to occur when ERROR is set.* 3. Cleared by INIT.
07	READY: Read-only bit. Indicates that the DRV11-WA is able to accept a new command: <ol style="list-style-type: none"> 1. Set by INIT. 2. Set by WCOFLO. 3. Set by ERROR. 4. Cleared by GO (bit 00).
08	CYCLE: Read/write bit. CYCLE is used to prime a DMA bus cycle: <ol style="list-style-type: none"> 1. Set by CYCLE REQUEST. 2. Cleared during DMA cycle by INIT.
09, 10, 11	STAT A,B,C: Read-only bits. Three device status input bits that indicate the state of the DSTAT A, B, and C user signals. These bits are set and cleared by the user.
12	MAINT: Read/write bit. Maintenance bit for use with the MAINDEC diagnostic.
13	ATTN: Read-only bit. Indicates the state of the ATTN user signal; sets READY, ERROR. *

* See Section 4.4.2.

Table 4-1 CSR Bit Functions (Cont)

Bit	Function
14	<p>NEX: Read/write to zero bit.</p> <ol style="list-style-type: none"> 1. Non-existent memory; indicates that as bus master, the DRV11-WA did not receive BRPLY or that a DATIO cycle was not completed. 2. Sets ERROR. 3. Cleared by INIT or by writing it to a zero.
15	<p>ERROR: Read-only bit.</p> <ol style="list-style-type: none"> 1. Indicates one of the following special conditions: <ol style="list-style-type: none"> a. NEX (bit 14) b. ATTN (bit 13) 2. Sets READY (bit 7) and causes an interrupt if IE (bit 6) is set. * 3. Cleared by removing the special condition as follows: <ol style="list-style-type: none"> a. NEX is cleared by writing bit 14 to zero. b. ATTN is cleared by the user device.

* See Section 4.4.2.

4.6 LSI-11 PROGRAMMING EXAMPLE

The following programs are sample programs for the DRV11-WA.

```

;* SAMPLE PROGRAM FOR Q18 BIT MODE
;* DO A 200 NPR DATA TRANSFER
DRVWCR=      172410
DRVBAR=      172412
DRVCSR=      172414
DRVDBR=      172416
PRO=         0

START:  MOV    #-200.,@#DRVWCR    ;WILL DO 200 XFER'S
        MOV    #DBUF,@#DRVBAR    ;SET UP BUFFER ADDRESS
        MTPS   #PRO              ;ENABLE INTR
        MOV    #101,@#DRVCSR     ;SET IE & GO
        BIS    #400,@#DRVCSR     ;SET CYCLE
WAIT:   BR     WAIT              ;WAIT HERE

```

```

;* SAMPLE PROGRAM FOR Q22 BIT MODE
;* DO A 200 NPR DATA TRANSFER
DRVWCR=      172410
DRVBAR=      172412
DRVBAE=      172412
DRVCSR=      172414
DRVDBR=      172416
PRO=         0

START:  MOV    #-200.,@#DRVWCR    ;WILL DO 200 XFER'S
        TST    @DRVWCR           ;CLEAR BAE FLAG *
        MOV    #DBUF,@#DRVBAR    ;SET UP BUFFER ADDRESS
        MOV    #DBUF1,@#DRVBAE   ;SET UP EXTENDED BUFFER ADDRESS
        MTPS   #PRO              ;ENABLE INTR
        MOV    #101,@#DRVCSR     ;SET IE & GO
        BIS    #400,@#DRVCSR     ;SET CYCLE
WAIT:   BR     WAIT              ;WAIT HERE

```

* By accessing the BAR, a flag gets set to a one (1) (BAEFLAG=1). This flag automatically gets cleared by accessing the BAE register. To ensure that you will be accessing the BAR on your next attempt, it is advisable to clear the BAE flag in your program. This can be done by accessing any of the other registers (that is, TST @DRVWCR).

5.1 GENERAL

The DRV11-WA can be configured for operation as a DMA parallel-data transfer link between two computer systems (Figure 5-1) by installing jumper W4 and removing jumper W3. The link operates in a half-duplex communications mode; that is, it has the capability of transmitting data bidirectionally between the two computer systems, but in only one direction at a time.

5.2 OPERATING MODES

From a hardware standpoint, the link can operate in one of three modes: word mode, single cycle mode, and burst mode.

In word mode, information can be passed between two computers in a word-by-word sequence controlled by an interrupt-driven program. In the single cycle and burst modes (which to the software are essentially identical), the link transmits a contiguous block of memory data from one computer to the other. DMA transfer is used in both machines. The principal difference between the two modes of operation is that in the single cycle mode, the DRV11-WA must obtain and release the bus for each data transfer made. In the burst mode, the DRV11-WA holds onto the bus once the bus grant is received, until the requested 4-cycle or N-cycle transfer is completed.

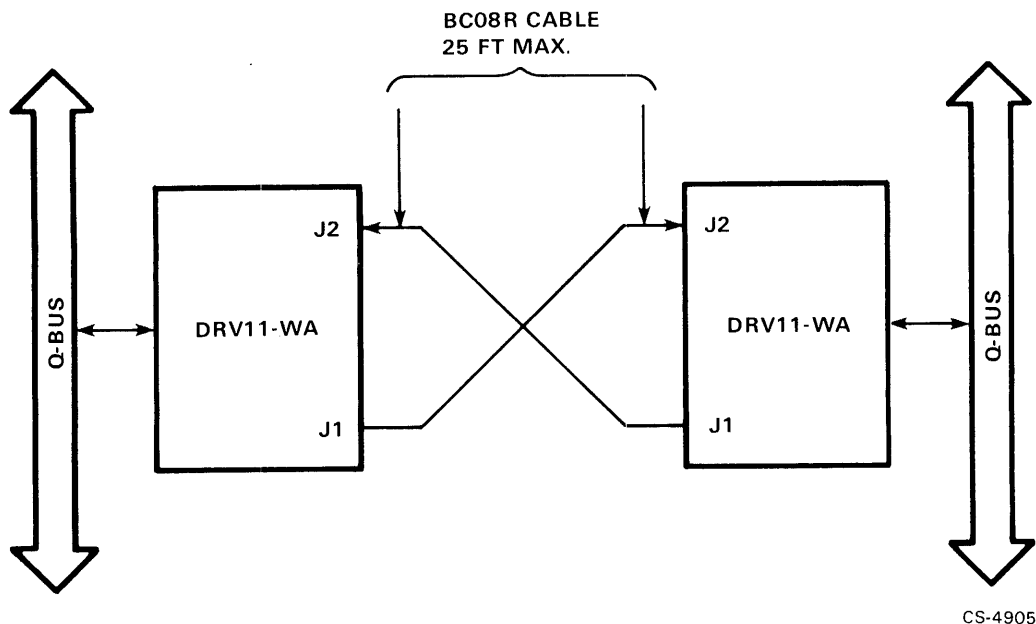


Figure 5-1 Interprocessor Link Block Program

Each of the computers in the link configuration maintains independent control of its own interface. The programs for the two computers must be written so as to ensure compatibility in terms of information flow direction, setting bus address registers, and control of word count at the respective computer interfaces with the DRV11-WA.

In the environment provided by the VAX-system software (and recommended for the PDP-11 systems) the communication between the linked computers is established by means of CSR bits (03:01) and (11:09), respectively (see Chapter 4, Figure 4-1 and Table 4-1 for this register). When CSR bits (03:01) are loaded into the CSR of one DRV11-WA, the information appears in the other DRV11-WA of the link configuration. Table 5-1 shows the functional correlation of these bit relationships for the DRV11-WA interprocessor links.

Table 5-1 Correlation of CSR Function and Status Bits in Interprocessor Link Operation

CSR Bits		DRV11-W/DRV11-B Function	Meaning of CSR Bit Status at Transfer-Initiating Computer	
Transfer-Initiating Computer	Transfer-Responding Computer			
Bit 3 (FNCT 3)	Bit 11 (STAT A)	Single Cycle/ Burst NPR Transfer	Set -	Single cycle NPR transfer
			Clear -	Burst NPR transfer
Bit 2 (FNCT 2)	Bit 10 (STAT B)	INTR (Interrupt) Request	Set -	Interrupt of re- sponding computer
Bit 1 (FNCT 1)	Bit 9 (STAT C)	DATI/DATO	Set -	DATO
			Clear -	DATI

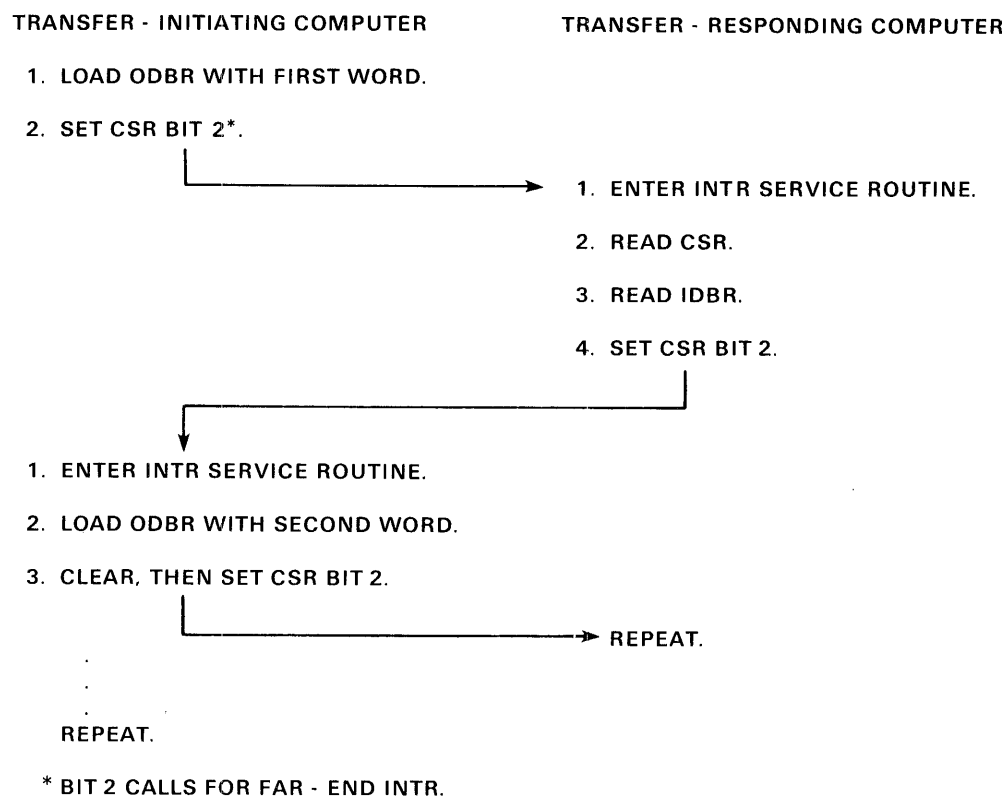
5.2.1 Word Mode

Setting CSR bit 2 (FUNC 2) in the transmitting DRV11-WA sets both CSR bit 10 (STATUS B) and CSR bit 13 (ATTN) in the receiving DRV11-WA. ATTN generates ERROR, which in turn generates an interrupt if IE is set.

In all three transfer modes, when power failure occurs in one computer, an ACLO is transmitted to the other computer, where it sets ATTN and (as described above) causes an interrupt.

During word-mode transfers, the data must be maintained in the ODBR until read by the other computer. In general, this operation requires that the receiving computer send back a "handshaking" signal to indicate that it has read the data, and that the transmitting computer cannot modify the data in its ODBR.

The interrupt capability incorporated in the CSR can be used in conjunction with the ODBR to pass information between computers in a word-transfer interrupt sequence (Figure 5-2).



CS-4906

Figure 5-2 Interrupt Sequence for Word Mode Interprocessor Link

5.2.2 Single Cycle

NPR transfers by the link may be requested by either computer, and may flow in either direction. The NPR cycles always occur in pairs: the first cycle is a DATI (read from memory) by the transmitter; the second cycle is a DATO (write into memory) by the receiver. These alternating pairs of cycles repeat until the entire buffer has been transmitted.

The computer designated as a link transmitter sets GO and CYCLE to generate the first NPR cycle. Subsequent NPR cycles are generated by hardware handshaking between the DRV11-WAs.

The programming sequence used to initiate a block transfer is given in Figure 5-3.

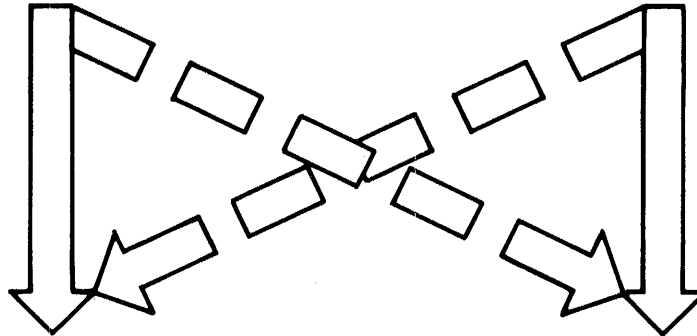
When the transmitter has read the data word from its memory and loaded the word onto its ODBR, BUSY is deasserted. BUSY is connected to CYCLE RQ at the receiving DRV11-WA. The trailing edge of BUSY triggers an NPR cycle that writes the data word into the receiver's memory. Completion of the write cycle deasserts BUSY in the receiving DRV11-WA. BUSY returns to the transmitting DRV11-WA as CYCLE RQ A. This alternating sequence continues until the word count register overflows and halts the block transfer.

TRANSFER - INITIATING COMPUTER

**TRANSMITS MESSAGE DESCRIBING DATA
TO BE EXCHANGED (LENGTH, DIRECTION, ETC.)**

TRANSFER - RESPONDING COMPUTER

**ACKNOWLEDGES DATA TO BE
EXCHANGED.**



DATA TRANSMITTER

1. SETS UP ITS OWN WC AND BA.

2. LOADS CSR:

- SETS GO TO 1 TO CLEAR READY.
- CLEARS FNCT 1 TO 0 TO INDICATE DATI.
- SETS FNCT 3 TO 1 TO INDICATE SINGLE CYCLE TRANSFER.
- SETS CYCLE TO 1 TO INITIATE FIRST NPR CYCLE.

DATA RECEIVER

1. SETS UP ITS OWN WC AND BA.

2. LOADS CSR:

- SETS GO TO 1 TO CLEAR READY.
- SETS FNCT 1 TO 1 TO INDICATE DATO
- SETS FNCT 3 TO 1 TO INDICATE SINGLE CYCLE TRANSFER.

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Figure 5-3 Single Cycle Transfer Sequence for Interprocessor Link

5.2.3 Burst Mode

The NPR burst mode requires that FNCT 3 be cleared on both DRV11-WAs. The programming procedure is similar to the single cycle.

Clearing FNCT 3 drives SINGLE CYCLE H low on the other DRV11-WA. During the first NPR cycle, the SINGLE CYCLE flip-flop clears and stays clear until the last NPR cycle, during which WCOF occurs. When the single cycle flop is cleared, it effectively holds the bus from releasing.

NOTE

N-cycle burst mode is not supported in a VAX/DRV11-WA link.

5.3 PROGRAMMING

The programming characteristics of the interprocessor link are basically the same as those of a single DRV11-WA configuration. However, when two DRV11-WAs are interconnected, the programming of the registers is slightly modified, as explained in the following sections.

5.3.1 Word Count Register (WCR)

The function of the WCR is the same as in the non-link mode. However, the WC INC ENB signal is asserted continually in link mode.

5.3.2 Bus Address Register (BAR)

The basic function of the BAR is unchanged when the DRV11-WA is operated in link mode. However, since the hardware configuration of the link permanently sets bit 00 to 0, interprocessor transfers are for full words only.

5.3.3 Output Data Buffer Register/Input Data Buffer Register (ODBR/IDBR)

The basic function of the ODBR/IDBR remains unchanged when the DRV11-WA is operated in link mode.

5.3.4 Control and Status Register (CSR)

In interprocessor link operation, the CSR bits are defined somewhat differently than in link operation. The differences are:

BIT 00 (GO)

When set by itself, GO conditions the DRV11-WA for either a transmit or a receive transfer.

BITS 1,2,3 (FNCT 1,2,3)

FNCT 1 Is 1 to a receiving DRV11-WA, and 0 to a transmitting DRV11-WA. If set in one DRV11-WA, it is cleared in the other DRV11-WA. It is initialized by the software.

FNCT 2 Sends an interrupt request to the companion computer; sets STATUS B, ATTN, and READY in the companion computer, thereby causing an interrupt request if the computer's IE bit is set, and ATTN interrupts are enabled.

FNCT 3 If FNCT 3 is a 0, the companion computer performs DMA transfers in the burst mode; if FNCT 3 is a 1, the companion computer performs DMA transfers in single-cycle mode.

BITS 4,5 (XBA 16, 17)

The functions of these bits are the same in both link and non-link modes. Refer to Chapter 4, Table 4-1 for definitions.

BIT 6

The function of this bit is the same in both link and non-link modes. Refer to Table 4-1 for bit definition. When set, this bit permits the DRV11-WA to generate an interrupt request if STATUS B sets as a result of FNCT 2 being set in the companion computer.

BIT 7 (READY)

The function of this bit is the same in both link and non-link modes. Refer to Chapter 4, Table 4-1 for bit definition.

BIT 8 (CYCLE)

This bit is used to initiate single cycle and burst transfers when the associated DRV11-WA is the transmitter. When this bit is set in conjunction with bit 00 (GO), an immediate NPR cycle occurs.

BITS 9, 10, 11 (STATUS C, B A)

STATUS C This bit is read by the computer initiating the transfer. If Status C is set, the responding computer initiates a DATO; if the bit is cleared, the responding computer initiates a DATI.

STATUS B Reads FNCT 2 of the companion computer. When set, this bit indicates that an interprocessor interrupt has been requested by the companion computer. This bit also sets ATTN and READY, and causes an interrupt request if the IE bit is set.

STATUS A Bit 11 (STATUS A) at 0 indicates a burst mode NPR transfer; if bit 11 is a 1, a single cycle NPR transfer is indicated.

BIT 13 (ATTN)

The function of this bit is the same in the link and non-link modes. ATTN is also set by either FNCT 2 or ACLO of the companion computer. ATTN generates ERROR.

BIT 14

The function of this bit is the same in both link and non-link modes. Refer to Chapter 4, Table 4-1 for bit definition.

BIT 15 (ERROR)

The function of this bit is the same in both link and non-link modes. Refer to Chapter 4, Table 4-1 for bit definition.

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