EK-DRVWA-UG-001

DRV11-WA General Purpose DMA Interface

User's Guide

Prepared by Computer Special Systems
of
Digital Equipment Corporation

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	Rainbow	

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CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The DRV11-WA is a general-purpose Direct Memory Access (DMA) interface for transferring 16-bit data words directly between the LSI-11/23, LSI-11/23-PLUS (includes Micro PDP-11), and LSI-11/73 memory, and a user's I/O device. Data Transfer Out (DATO) or Data Transfer In (DATI) takes place over the LSI-11 bus after a DMA request, once the DRV11-WA becomes bus master. Burst modes, byte addressing, and read-modify-write operation (DATIO) are possible with the DRV11-WA. The DRV11-WA features switch-selectable device and vector addresses, and two 40-pin connectors that provide simple interfacing to the user's I/O device. (The DRV11-WA is compatible with both standard and extended LSI buses.)

There are six registers in the DRV11-WA. They are as follows:

- Word Count Register (WCR),
- Bus Address Register (BAR),
- Extended Bus Address Register (BAE),
- Control/Status Register (CSR), and
- Input and Output Data Buffer Registers (DBRs).

The CSR and DBRs are word- and byte-addressable, whereas the WCR, BAR, and BAE are only word-addressable.

DRV11-WA operation is initialized under program control by:

1. Loading the WCR with the 2's complement of the number of transfers,
2. Loading the BAR and BAE with the first address to or from which data is to be transferred, and
3. Loading the CSR with the desired function bits.

Data transfers may now proceed under the control of the DRV11-WA DMA logic.

Figure 1-1 shows the primary interface signals between the DRV11-WA and the user's I/O device. DMA input (DATI) or output (DATO) data transfers take place when the processor clears READY. For a DATO cycle (DRV11-WA to memory transfer), the user's I/O device presets the CONTROL BITS (word count increment enable, bus address increment enable, C1, C0, A00, and ATTN), and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the CONTROL BITS are latched into the DRV11-WA DMA control, and BUSY goes low. (A DATI cycle memory to DRV11-WA transfer is handled in a similar manner, except that the output data is latched into the output DBR during the bus cycle.)

When the DRV11-WA becomes bus master, a DATO or DATI cycle is performed directly to or from the LSI-11 memory location specified by the BAR and BAE. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue asynchronously until the WCR increments to zero, at which time READY goes high and the DRV11-WA generates an interrupt (if interrupt enable is set) to the LSI-11 processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete synchronous transfer of the specified number of data words.

1.2 SPECIFICATIONS

The following specifications and particulars are for informational purposes and are subject to change without notice.

Physical

Dual height, single width, extended length module.

Dimensions:

Circuit Card	Circuit Card Plus Handle
Length: 21.6 cm (8.5 in)	Length: 22.8 cm (8.9 in)
Height: 12.7 cm (5.0 in)	Height: 13.2 cm (5.2 in)
Width: 1.3 cm (.5 in)	Width: 1.3 cm (.5 in)

Weight: 215 grams

User I/O Connections: Two 40-pin connectors

Mounting Requirements: Plugs directly into LSI-11 backplane or LSI-11 expansion backplane.

Electrical

Logic Power Requirements: 1.8 A @ +5V $\pm$ 5% (nominal)

LSI-11 Bus Loading: Presents one bus load

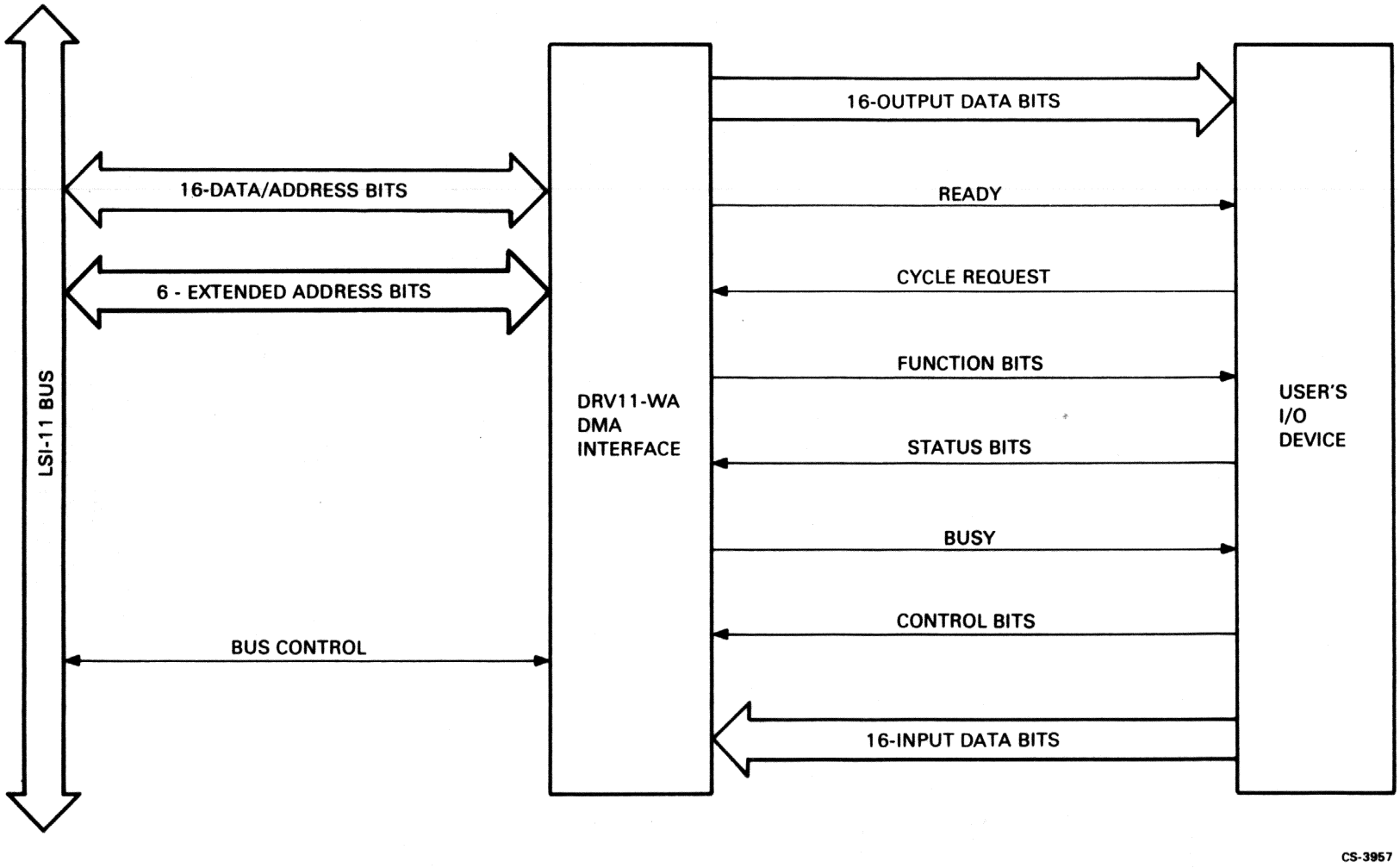


Figure 1-1 DRV11-WA Simplified Interface Diagram

User Loading:

Input Data Lines

1 TTL unit load each
HIGH = Logic one
LOW = Logic zero

Input Control Lines

1 TTL unit load each
HIGH = Logic one
LOW = Logic zero

Output Data Lines

10 TTL unit loads (drive) each
HIGH = Logic one
LOW = Logic zero

Output Control Lines

10 TTL unit loads (drive) each
HIGH = Logic one
LOW = Logic zero

Module Type: M7651

Operational:

Transfer Mode: DMA or program-controlled with interrupts

Data Transfer Rate:

Up to 250,000 16-bit words per second in single cycle mode
Up to 500,000 16-bit words per second in burst mode*

Environmental

Temperature: Storage: -40° to 66°C (-40° to 150°F)
Operating: 5° to 50°C (41° to 122°F)

Relative Humidity: 10% to 95% noncondensing

* While doing burst mode transfers, the DRV11-WA becomes bus master and holds the bus until the entire transfer is complete. This action may potentially lock out other devices from accessing the bus while the transfers are ongoing. This mode of operation is consistent with the operation of the 18-bit predecessor product, DRV11-B.

1.3 RELATED LITERATURE

In addition to the M7651 print set (MP01582-01), the Microcomputer Processor Handbook and the Microcomputer Interface Handbook contain useful information for installing and operating the DRV11-WA general-purpose DMA interface. Handbooks may be ordered from the nearest Digital Equipment Corporation Sales Office.

CHAPTER 2
INSTALLATION

2.1 GENERAL

Installation of the DRV11-WA general-purpose DMA interface consists of selecting the device and interrupt vector addresses, selecting mode of operation (18- or 22-bit addressing), and then inserting the interface into an LSI-11 processor system.

2.2 SYSTEM CONSIDERATIONS

Before installing the DRV11-WA into an LSI-11 system, consideration must be given to bus loading, power, priority, and space requirements.

2.2.1 LSI-11 Bus Loading

The DRV11-WA presents one bus load to the LSI-11 bus. Fifteen bus loads can be handled by the LSI-11 bus; therefore, the user must determine the existing LSI-11 bus load when installing additional LSI-11 modules.

2.2.2 Power Requirements

The DRV11-WA requires 1.8 A @ +5V ± 5% (nominal). Power for the DRV11-WA is obtained from the LSI-11 system power supply.

2.2.3 Priority Requirements

Each device on the LSI-11 bus has an interrupt and DMA priority based on its relative position from the processor. Since the user may install the DRV11-WA on the bus along with other devices that use the same interrupt or DMA priority, the user must bear in mind that when more than one device is requesting service, the device electrically nearest the LSI-11 microprocessor has the highest priority and will be serviced first. In addition, if the REV11 DMA refresh option is used, the REV11 must be at a priority level higher than that of the DRV11-WA. Refer to the Microcomputer Processor Handbook for detailed information on the REV11 options.

2.2.4 Space Requirements

The DRV11-WA requires one double height module slot.

2.3 USER I/O CABLES

The DRV11-WA has two 40-pin connectors which provide the interface to the user's device. Two cable assemblies are required. It is recommended that cable assemblies from Table 2-1 be used to connect the DRV11-WA to the user's device. The listed cables are terminated (one or both ends) with H856 40-pin connectors that mate with the connectors on the DRV11-WA. Cable selection is determined by the type of connections used on the user's device. The desired cable length (XX) must be specified when ordering. (Lengths longer than 25 feet are not recommended for use with the DRV11-WA.) Cables may be ordered from the nearest Digital Equipment Corporation Sales Office. Non-standard length cables may be ordered at additional cost.

Table 2-1 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft/m)
BCØ8R-XX	H856 to H856	Shielded flat	1, 6, 1Ø, 12, 2Ø, 25 ft (Ø.3Ø5, 1.83Ø, 3.Ø5Ø, 3.66Ø, 6.1ØØ, 7.625 m)
BCØ4Z-XX	H856 to open end	Shielded flat	6, 1Ø, 15, 25 ft (1.83Ø, 3.Ø5Ø, 4.575, 7.625 m)

2.4 DEVICE ADDRESS SELECTION

The DRV11-WA contains six registers:

1. The WCR,
2. The BAR,
3. The BAE,
4. The CSR,
5. The input DBR, and
6. The output DBR.

These registers must be addressed for data and status transfers between the DRV11-WA and the LSI-11 processor. The BAR and BAE use the same address. The two DBRs use the same address. The register addresses are sequential by even numbers and are as follows.

Register	BBS7	Octal Address
WCR	1	XXXXXØ
BAR	1	XXXXX2
BAE	1	XXXXX2
CSR	1	XXXXX4
DBRs	1	XXXXX6

The assigned DMA interface base address is 772410_8. The user selects a base address for assignment to the WCR and sets the device address selection switches on the DRV11-WA module to decode this address. The remaining BAR, BAE, CSR and DBR addresses are then properly decoded by the module as they are received from the LSI-11 processor.

Figure 2-1 shows the location of the device address selection switches on the DRV11-WA module. Switches are set to the ON (closed) position for bits to be decoded as "ONE" bits in the base address. Bits decoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-2 shows the address select format and presents the switch-to-bit relationship for the device address selection switches.

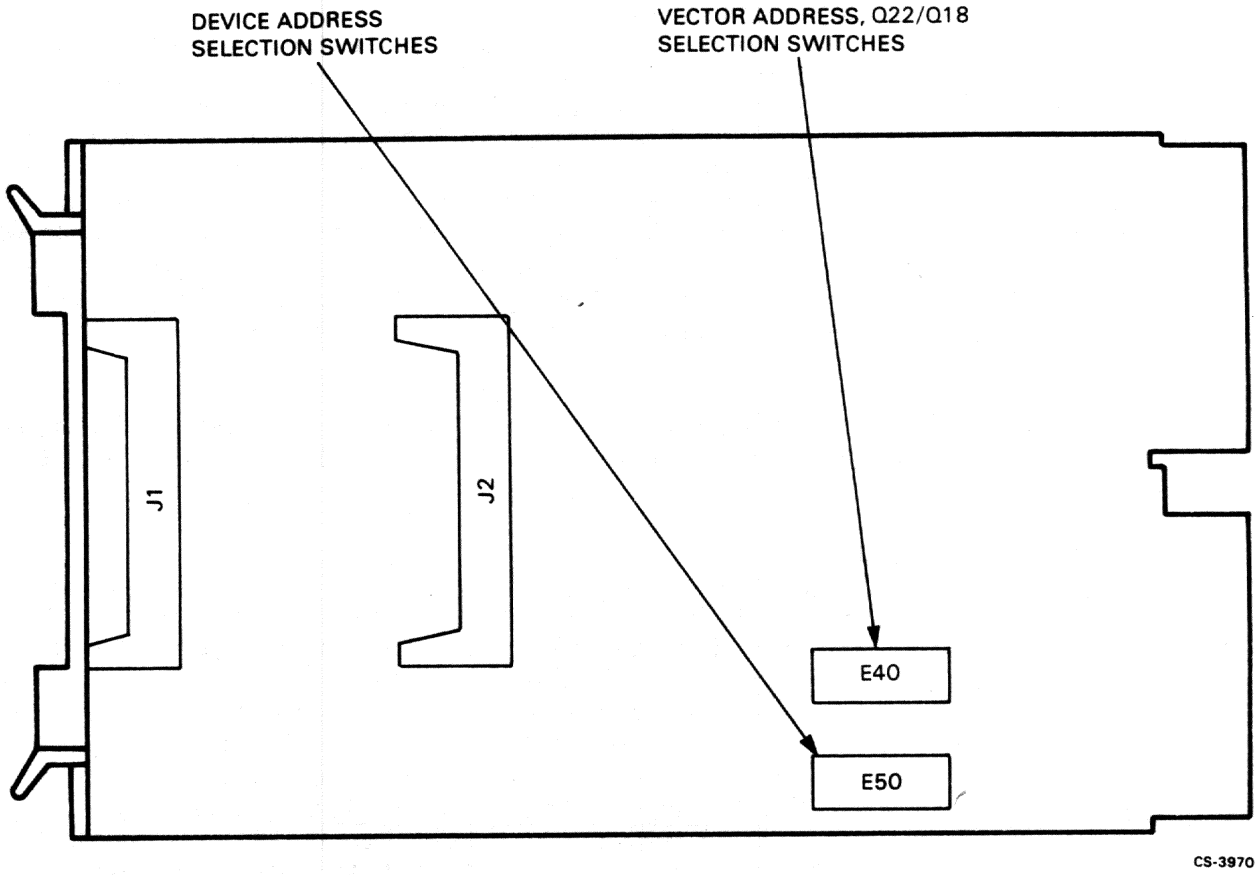


Figure 2-1 DRV11-WA Connector and Switch Locations

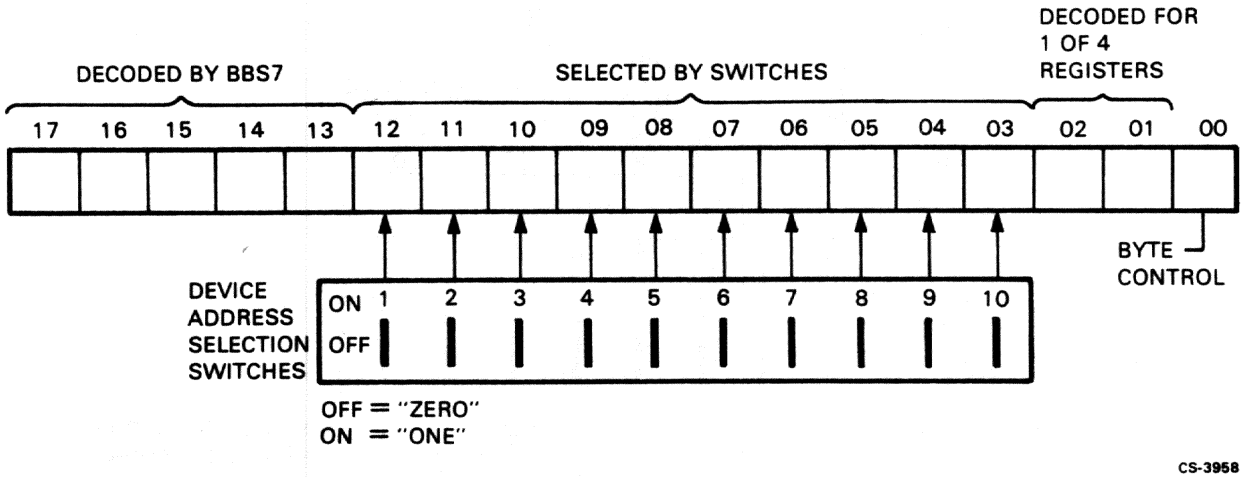


Figure 2-2 DRV11-WA Device Address Select Format

2.5 INTERRUPT VECTOR ADDRESS SELECTION

Vector addresses $\emptyset$-1774_8 are reserved for LSI-11 system users. The DRV11-WA is assigned vector address 124_8. The user selects the interrupt vector address by means of switches on the DRV11-WA module. Figure 2-1 shows the location of the vector address selection switches. Vector address selection switches are set to the ON (closed) position for bits to be encoded as "ONE" bits in the vector address. Bits encoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-3 shows the address select format and presents the switch-to-bit relationship for the vector address selection switches.

2.6 ADDRESSING MODE SELECTION

The user selects 18- or 22-bit addressing by setting E40 switch 10 OFF (OFF=$\emptyset$) for 18-bit addressing, or ON (ON=1) for 22-bit addressing (see Figure 2-3).

2.7 MODULE INSTALLATION

With the exception of the first two/four slots (the LSI-11 processor always occupies the first two/four slots depending on CPU TYPE), the DRV11-WA can be installed into any slot (see Section 2.2.4) of the LSI-11 backplane. However, if REV11 DMA refresh option is used, the DRV11-WA must be at a lower priority than the REV11. When inserting the module into the backplane, make sure that the deep notch on the module seats against the connector block rib. Do not insert or remove the module with power applied. After performing the initial turnon (see Section 2.8), connect the user's I/O cables to J1 and J2 on the DRV11-WA I/O connectors. Connector locations for the DRV11-WA are shown in Figure 2-1. Pin assignments for J1 and J2 are shown in Figure 2-4 and are specified in Chapter 1, Section 1.2.

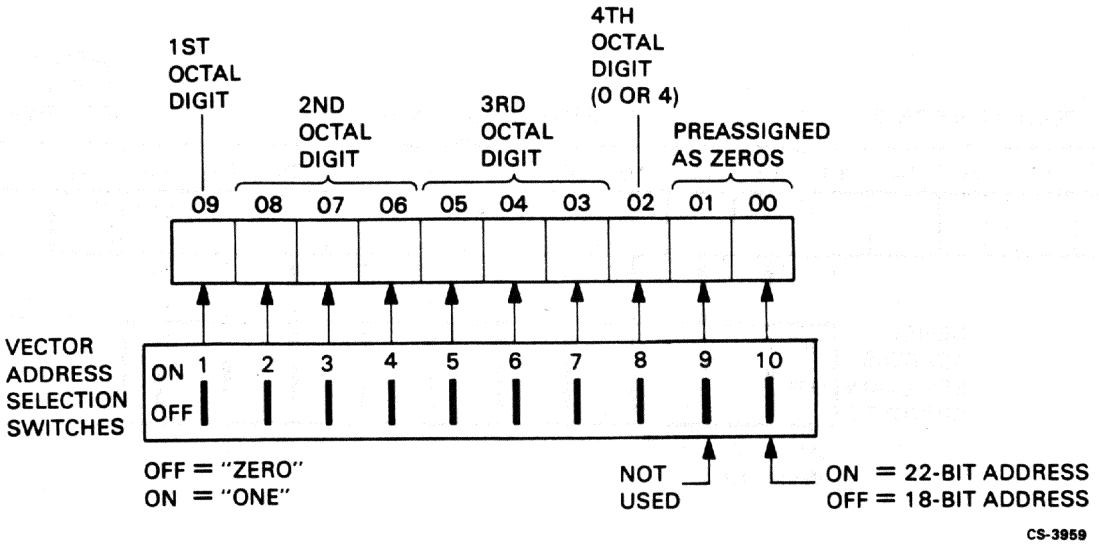


Figure 2-3 DRV11-WA Interrupt Vector Address Select Format

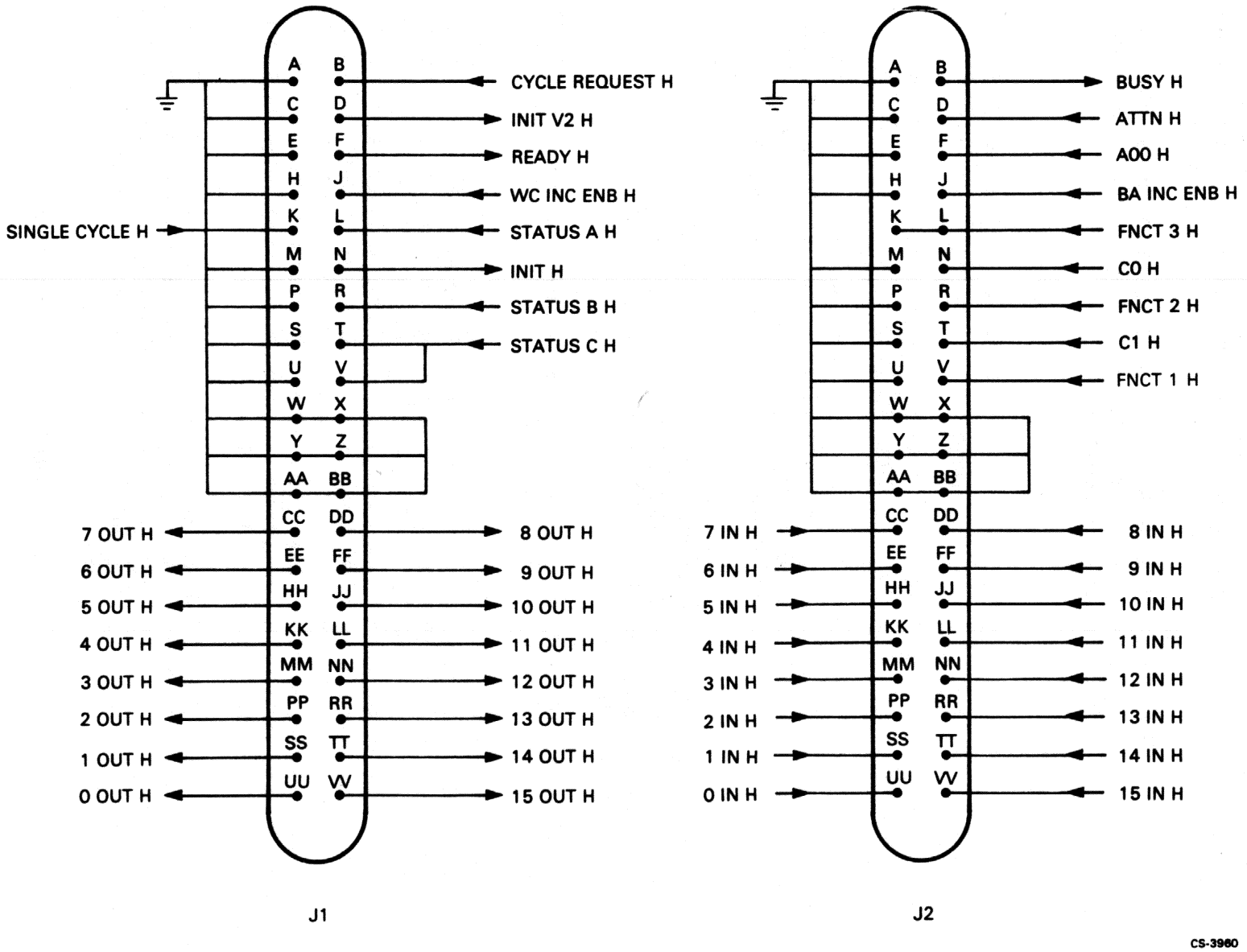


Figure 2-4 DRV11-WA Connector Pin Assignments

2.8 INITIAL TURN-ON

After completing the module installation, turn on the LSI-11 and initialize the system. With no I/O cables connected and using the LSI-11 terminal and operating procedures, perform the following quick operational verification.

1. Load the addresses of the WCR, BAR, CSR, AND DBRs through the system terminal and examine the locations. The terminal will indicate the following:

22-Bit	18-Bit
WCR contents will be 000000	WCR contents will be 000000
BAR contents will be 000001	BAR contents will be 000001
BAE contents will be 000000	
CSR contents will be 172000	CSR contents will be 172000
DBR contents will be 177777	DBR contents will be 177777

2. The WCR, BAR, and BAE (if 22 bit addressing is selected) can be loaded with data from the system terminal and the corresponding data read back on the terminal. BAR bit 0 will read as a one (1) with no I/O cables connected.

NOTE

BAE (ADDRESS xxxxx2) is read by first examining the BAR (ADDRESS xxxxx2) and then examining ADDRESS xxxxx2 again to access the BAE.

The user's I/O device cables can now be connected to the DRV11-WA (Figure 2-1).

2.9 DIAGNOSTIC PROGRAM

The check procedure performed in Section 2.8 does not completely verify the operation of the DRV11-WA. Complete module operation can be verified through the use of the diagnostic software program AC-T974B-MC. The program can be loaded into the LSI-11 system by means of any standard loadable device. A BC05L or BC06R maintenance cable (not longer than 25 ft) is required to loop the DBR output to the DBR input for checking the I/O data path. A complete description of the diagnostic software program and its implementation is provided in AC-T974B-MC.

When you execute the AC-T974B-MC diagnostic, you must select software Switch 12 (SW12) of the SWR to correspond with your selection of hardware Switch 10-E40. SW12 must be ON (ON=1) to enable 22-bit address testing, or OFF (OFF=0) to enable 18-bit address testing. The default setting is OFF.

S10-E40	SW12 of Diagnostic
ON = 22-bit addressing	ON = Enable 22-bit address testing
OFF = 18-bit addressing	OFF = Disable 22-bit address testing

The diagnostic will continue to run until it is terminated with a control character.

CHAPTER 3
BASIC OPERATION

3.1 GENERAL

This chapter contains a functional description of the DRV11-WA. The DRV11-WA registers are described as well as user device and bus operations necessary to perform DMA transfers. Figure 3-1 is a block diagram of the DRV11-WA. All descriptions are written to this diagram. The chapter ends with a brief description of the timing associated with DMA transfers.

3.2 FUNCTIONAL DESCRIPTION

3.2.1 DRV11-WA Registers

The DRV11-WA contains six registers:

- Word Count Register (WCR),
- Bus Address Register (BAR),
- Extended Bus Address Register (BAE),
- Control Status Register (CSR), and
- Input and Output Data Buffer Registers (DBRs).

3.2.1.1 Word Count Register (WCR) -- The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement (negative number) of the number of words to be transferred. At the end of each transfer, the word count register is incremented. When the contents of the WCR is incremented to zero, transfers are terminated, READY is set, and if the interrupt enable bit is set, an interrupt is requested. The WCR is word-addressable only.

3.2.1.2 Bus Address Register (BAR) - The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including address bit Ø) that specifies the location to or from which data is to be transferred. The BAR is incremented after each transfer and can be incremented across 32K memory boundaries by means of the extended address feature of the DRV11-WA. Systems with only 16 address bits will "wrap-around" to location zero when the extended address bits are incremented. On systems with extended addressing, an overflow in the BAR will increment the BAE. The BAR is word-addressable only.

3.2.1.3 Extended Bus Address Register (BAE) -- The BAE is a 6-bit read/write register accessible when extended addressing mode (Q22) is selected. This register is loaded (under program control) with a bus address that specifies the location to or from which data is to be transferred. If the BAR overflows, it will increment the extended address bits. The BAE is word-addressable only.

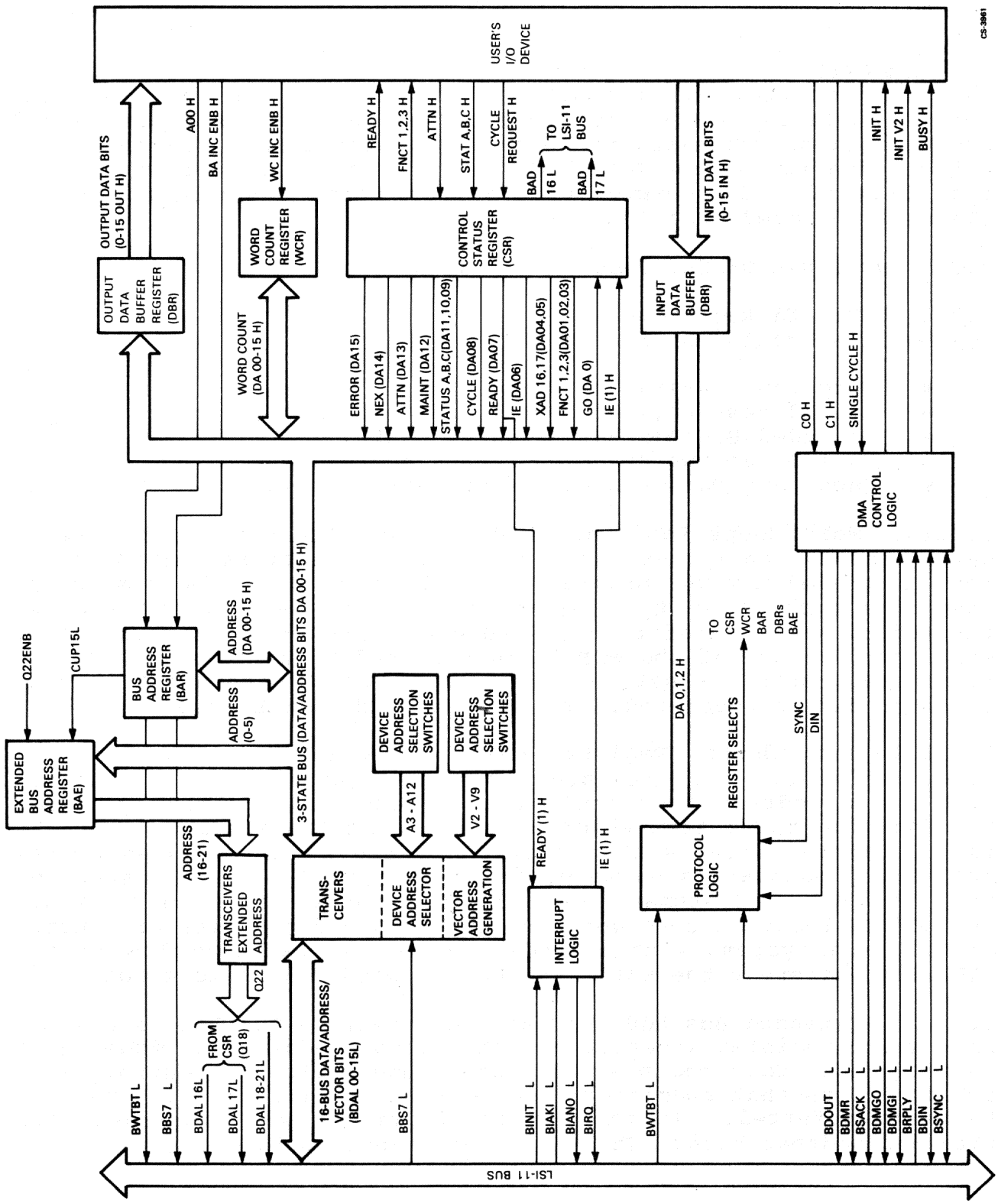


Figure 3-1 DRV11-WA Block Diagram

3.2.1.4 Control/Status Register (CSR) -- The CSR is a 16-bit register used to control the functions and monitor the status of the interface. Bit ØØ is a write-only bit and always reads as a zero. Bits Ø1-Ø6, Ø8, and 12 are read/write bits, while bits Ø7, Ø9-11, and 13-15 are read-only bits. Bit 14 can be written to a zero. Bits Ø4 and Ø5 are the extended addressing bits. If extended address mode (Q22) is selected, bits Ø4 and Ø5 are read-only bits. CSR functions are fully described in Chapter 4. The CSR is both byte- and word-addressable.

3.2.1.5 Input and Output Data Buffer Registers (DBRs) -- The two DBRs are 16-bit registers. The input DBR is a read-only register; the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred to memory under DMA control by the DRV11-WA, or under program control by the LSI-11 processor. Conversely, data is written into the output DBR from memory under DMA control by the DRV11-WA, or under program control by the LSI-11 processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

3.2.2 User Interface Lines

There are 50 interface lines (25 per connector) between the DRV11-WA and the user's I/O device. Of these lines, 32 are I/O data lines, 3 are for status, and 15 are for control. A brief description of these interface lines follows.

Mnemonic	Description
ØØ OUT - 15 OUT	16 TTL data output lines from the DRV11-WA. One = high.
ØØ IN - 15 IN	16 TTL data input lines from the user's device. One = high.
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user.
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user.
INIT	One TTL output line; used to initialize the user's device.
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.

Mnemonic	Description
A00	One TTL input line from the user's device. This line is normally low for word transfers. During byte transfers this line controls address bit 00.
BUSY	One TTL output line to the user's device. BUSY is low when the DRV11-WA DMA control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low, DMA transfers may be initiated by the user's device.
C0, C1	Two TTL input lines from the user's device. These lines control the LSI-11 bus cycle for DMA transfers. C0 and C1 codes for the four possible bus cycles are listed as follows.

C0 and C1 Codes

Bus Cycle	C0	C1
DATI	0	0
DATI0	1	0
DATO	0	1
DATOB	1	1

SINGLE CYCLE	One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation, SINGLE CYCLE is driven low by the user's device.

CAUTION

When SINGLE CYCLE is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device; other devices, including the MOS memory refresh function, cannot use the bus.

WC INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-WA word counter. Low inhibits incrementing.

Mnemonic	Description
BA INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.
CYCLE REQUEST	One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.
ATTN	One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY, and request an interrupt if the interrupt enable bit is set.

3.2.3 LSI-11 Bus Lines

There are 38 LSI-11 bus signal lines used by the DRV11-WA; 16 of these are multiplexed and bidirectional lines that carry data and address bits. Six lines are used for extended address bits, while 16 lines are used for control signals. A brief description of the 38 bus lines follows.

Mnemonic	Description
BDAL Ø - BDAL 15	16 bus data/address lines. An address is first placed on these lines followed by the data. These lines are asserted when driven low.
BDAL 16, 17	Two bus lines used to address beyond 32K of memory by the DRV11-WA. These lines are asserted when low.
BDAL 18-21	Four bus lines used to address beyond 128K of memory. These lines are asserted when low.
BDOUT	One bus line; when asserted (low), indicates that data is available on the BDAL lines and an output transfer (with respect to the bus master) is taking place.
BRPLY	One bus line; asserted (low) in response to BDIN or BDOUT and in response to BIAK transactions. It is generated by the slave device for address recognition.

Mnemonic	Description
BDIN	One bus line; when asserted (low) during BSYNC time, indicates an input transfer (with respect to the bus master). Requires a BRPLY response. BDIN is asserted when the bus master is ready to accept data from the slave. When asserted without BSYNC, indicates that an interrupt operation is occurring.
BSYNC	One bus line; asserted (low) by the bus master to indicate that it has placed an address on the BDAL lines. The transfer is in progress until BSYNC is negated (high).
BWTBT	One bus line; asserted (low) during address time to indicate that an output sequence (DATO or DATOB) is to follow. BWTBT is also asserted during data time for byte addresing during a DATOB.
BIRQ	One bus line; device asserts (low) this line when its interrupt enable, interrupt request, and ready flip-flops are set. BIRQ informs the LSI-11 processor that service is requested.
BIAKI, BIAKO	Two bus lines; one is interrupt acknowledge in, the other is interrupt acknowledge out. BIAKI is generated by the LSI-11 processor in response to BIRQ. The processor asserts (low) BIAKO which is routed to the BIAKI pin of the first device on the bus. If the device is not requesting an interrupt, BIAKO is passed (as BIAKI) to the next device.
BBS7	One bus line; asserted (low) by the LSI-11 processor when addressing a device for program-controlled transfers. The DRV11-WA can assert BBS7 and address other devices on the LSI-11 bus without processor intervention.
BDMGI, BDMGO	Two bus lines; one is DMA grant in, the other is DMA grant out. The LSI-11 processor generates BDMGO which is routed to the BDMGI pin of the first bus device. If the device is requesting the bus, it will inhibit passing BDMGO to the next bus device. If the device is not requesting the bus, it will pass BDMGO as (BDMGI) to the next device.

Mnemonic	Description
BINIT	One bus line; asserted (low) by the LSI-11 processor to initialize or clear devices connected to the LSI-11 bus.
BSACK	One bus line; BSACK is asserted (low) by a DMA device in response to the LSI-11 processor's BDMGO signal, indicating that the DMA device is bus master.
BDMR	One bus line; a device asserts this signal for DMA requests and to become bus master.

3.2.4 User's I/O Device to LSI-11 Memory Transfer (DATO or DATOB)
Data transfers from the user's I/O device to the LSI-11 memory are DMA transfers. Figure 3-2 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 3-1, DMA transfers are initialized under program control by loading the DRV11-WA WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR (and BAE if Q22 is selected) with the starting memory address for word storage; and setting the CSR for transfers.

When the GO bit of the CSR is written to a "one", READY goes low and the user's I/O device conditions the AØØ, BA INC ENB, WC INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and the CØ, C1 lines (refer to Section 3.2.2), and then asserts CYCLE REQUEST. The INPUT DATA BITS and control bits (CØ, C1 and SINGLE CYCLE, BA INC ENABLE, WC INC ENABLE) are latched into the respective DRV11-WA registers (at the high-to-low transition of BUSY). CYCLE REQUEST sets CYCLE and causes the DRV11-WA to assert BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-WA becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

As bus master, the DRV11-WA performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The LSI-11 memory decodes the address; then, the DRV11-WA removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB) and then places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-WA negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus is released when the DRV11-WA negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-WA WCR and BAR are incremented (for normal DMA transfers), BUSY goes high, while READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST. DMA transfers can continue until the WCR increments to

zero and generates an interrupt request, if the interrupt enable bit is set.

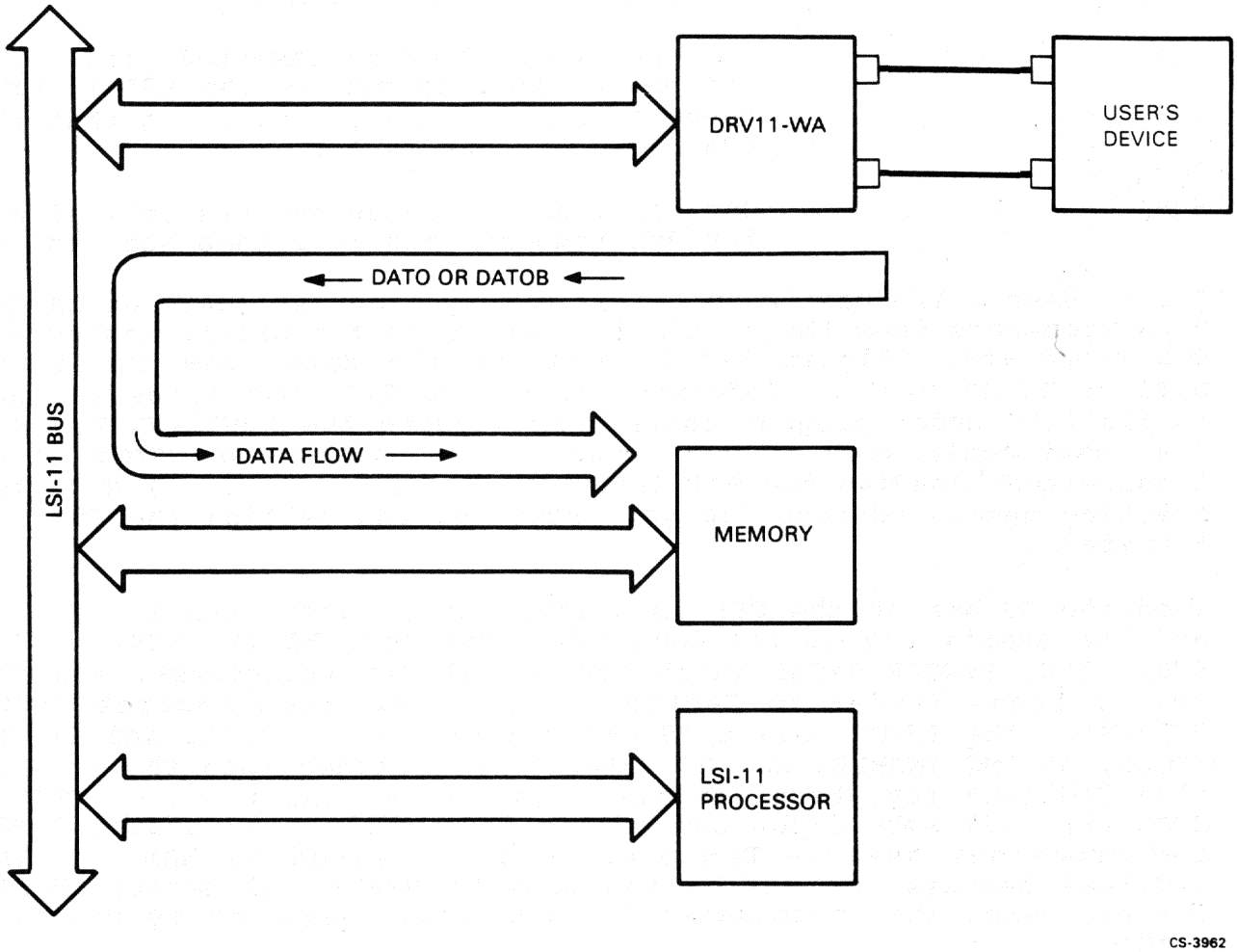


Figure 3-2 DMA DATO/DATOB Data Flow Diagram

3.2.4.1 Interrupts -- When the WCR increments to zero, READY goes high and the DRV11-WA generates an interrupt request (if the interrupt circuits are enabled). The LSI-11 processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-WA and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The LSI-11 processor receives the vector address and negates BDIN and BIAKI. The DRV11-WA now negates BRPLY, while the procesor exits from the main program and enters a service program for the DRV11-WA as indicated by the vector address.

Interrupt requests from the DRV11-WA occur for the following conditions:

1. When the WCR increments to zero. This is a normal interrupt at the end of a designated number of transfers.

2. When the user's I/O device asserts ATTN. This is a special condition interrupt which may be defined by the user to override the WCR.

3. When a nonexistent memory location is addressed by the DRV11-WA. This condition interrupt is produced when no BRPLY is received from the LSI-11 memory.

Interrupts are explained in greater detail in Chapter 4 of this manual.

3.2.5 LSI-11 Memory to User's Device Transfers (DATIO or DATI)

DMA transfers from the LSI-11 memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 3-3 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-WA WCR (Figure 3-1) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come. The CSR is set for transfers.

With the CSR set, READY goes low and the user's I/O device conditions the CØ, C1 lines (refer to Section 3.2.2) for a DATI or a DATIO, and conditions the WC INC ENB, BA INC END, ATTN, SINGLE CYCLE (high for normal DMA transfers), and asserts CYCLE REQUEST. BUSY from the DRV11-WA goes low and the user's control bits are latched into the DRV11-WA. The DRV11-WA then asserts BDMR, which makes a bus request. When the request is arbitrated as described in Section 3.2.4, the DRV11-WA becomes bus master.

When the DRV11-WA becomes bus master, a DATI or DATIO bus cycle is performed (the following describes a DATI). The DRV11-WA places the address of the memory location from which the first word is taken on the BDAL lines and asserts BSYNC. Memory decodes and latches the address. The DRV11-WA then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-WA and BDIN is negated. Memory negates BRPLY and the DRV11-WA negates BSACK and BSYNC to terminate the bus cycle and release the bus. The OUTPUT DATA BITS for the user's I/O device are stored in the DRV11-WA output data buffer register. These bits can be read by the user's device at the low-to-high transition of BUSY.

At the end of the first transfer, the DRV11-WA WCR and BAR (or BAE, if extended addressing is selected) are incremented, BUSY goes high, while READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated (see Section 3.2.4.1).

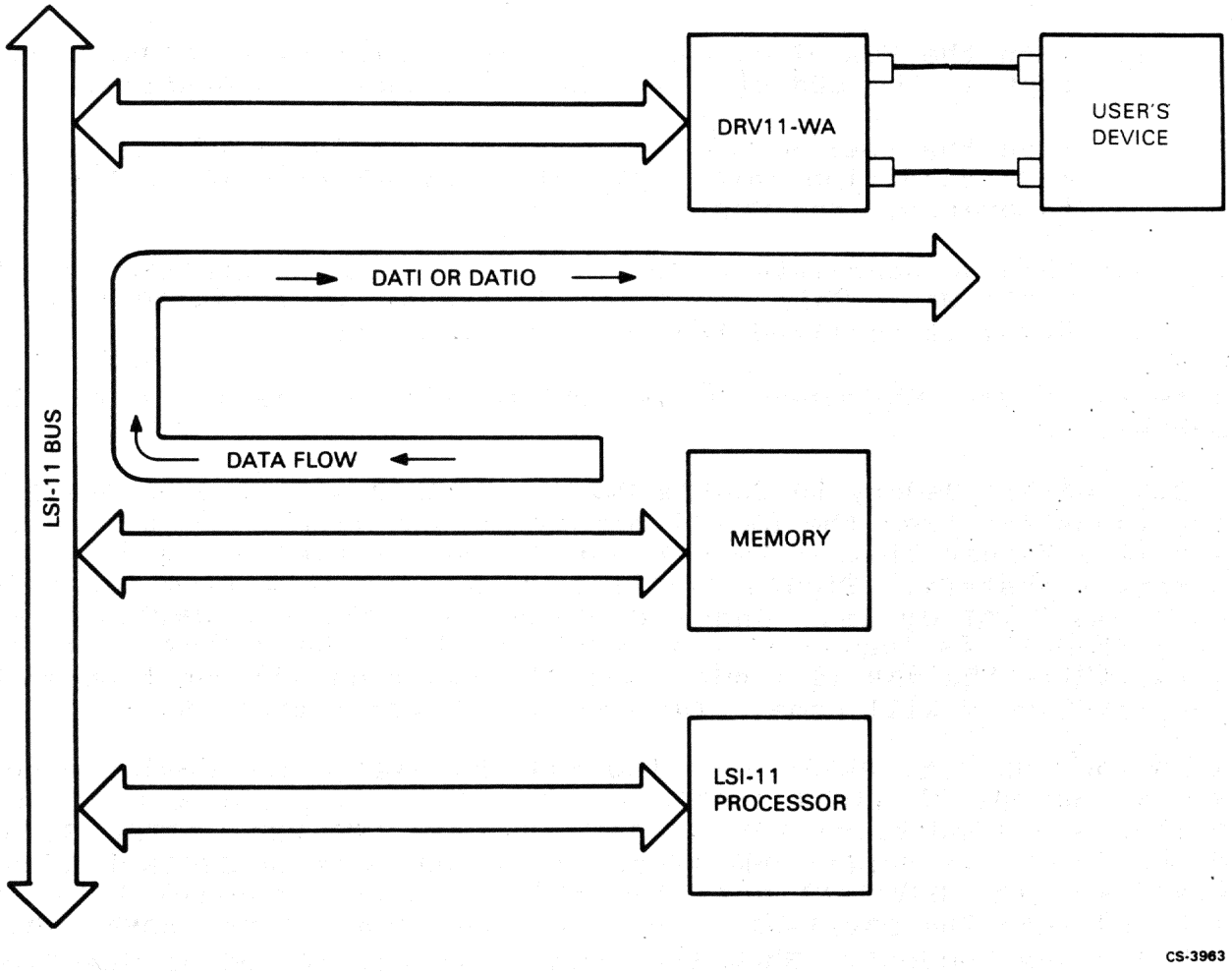


Figure 3-3 DMA DATIO/DATI Data Flow Diagram

3.2.6 Using DRV11-WAs as Interprocessor Links

When you connect two LSI-11 processors together using DRV11-WAs, you have to initiate the DMA from transmit side, while the receive side waits for CYCLE to be set. When BUSY goes high on the transmit side, CYCLE is set on the receive side (see Figure 3-4).

At the transmit side, when you set the GO bit, READY goes low, and CYCLE REQUEST is asserted. CYCLE REQUEST sets CYCLE and causes the DRV11-WA to assert BDMR, which makes an LSI-11 bus request and causes BUSY to go low. The transmit DRV11-WA then takes the data from memory, puts it into the ODBR, and negates BUSY H.

At the end of the first transfer, the transmit DRV11-WA WCR and BAR (or BAE if extended addressing is selected) are incremented, transmit BUSY goes high, while transmit READY remains low. BUSY high at the transmit side sets CYCLE at the receive side and causes receive BUSY to go low. With receive BUSY low, the receive DRV11-WA starts DMA and receives the data into the input DBR for subsequent transfer to memory under DMA control by the receive DRV11-WA, or under program control by the LSI-11 processor. At

the end of the first receive, the receive BUSY goes high, which sets CYCLE on the transmit side. This causes the transmit DRV11-WA to initiate another transfer. DMA transfers can continue until the transmit WCR increments to zero and generates an interrupt request, if the interrupt enable bit is set.

If you initiate the DMA from receive side, you will receive the data that is stored in the transmit DRV11-WA ODBR before the transmit DRV11-WA takes the data from memory and puts it into the ODBR.

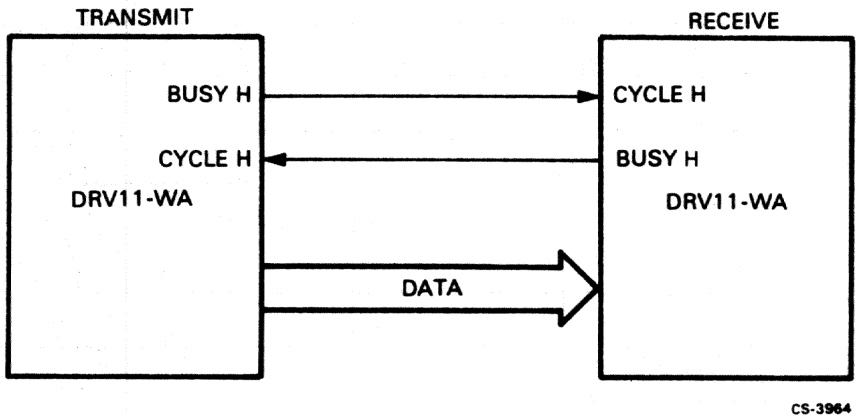


Figure 3-4 DRV11-WA as Interprocessor Link

3.3 TIMING

Input and output timing for the DRV11-WA is shown in Figures 3-5 through 3-8. The timing diagrams show user signal timing for single cycle and burst mode operations which can be either programmer user-initiated.

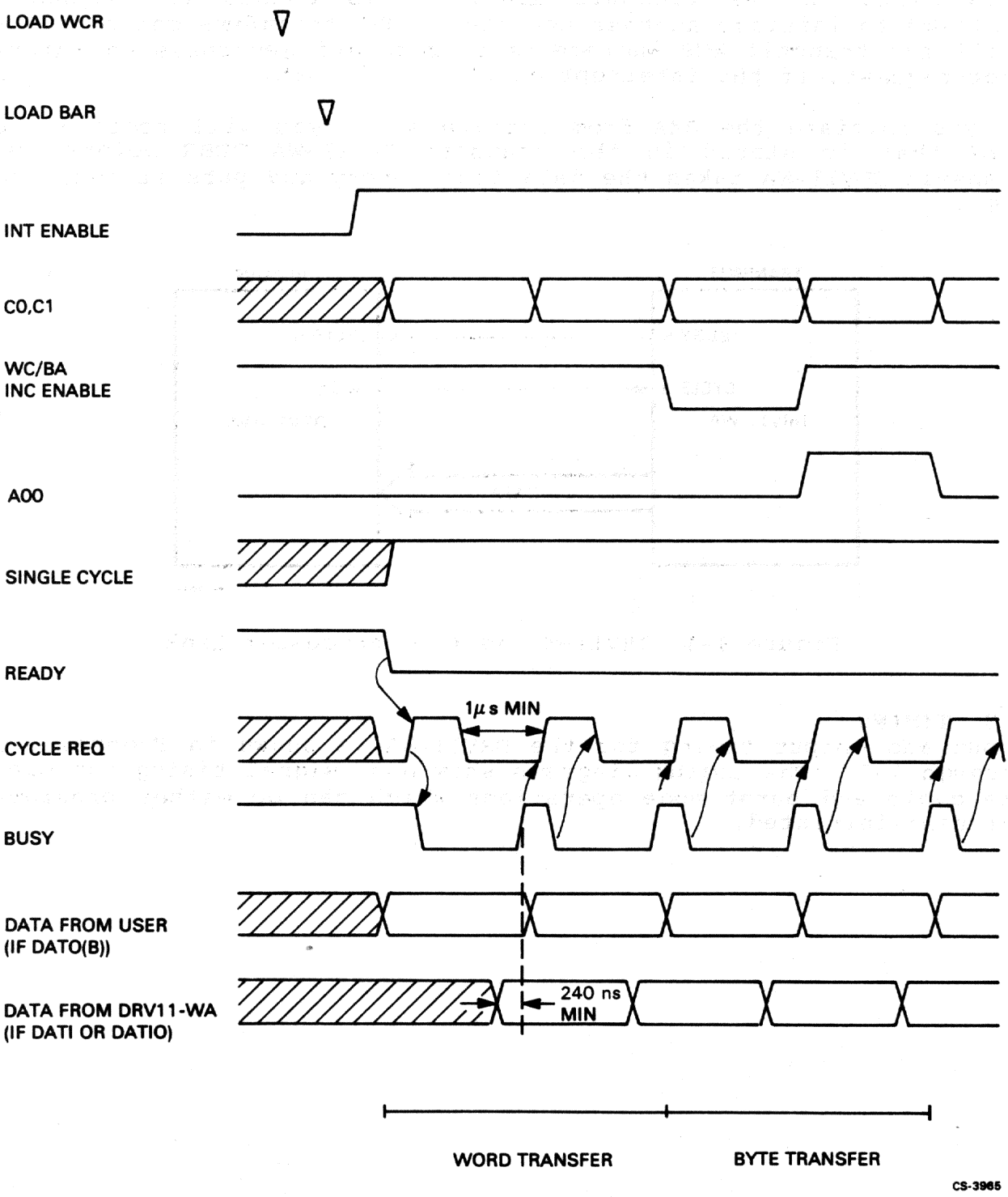


Figure 3-5 DRV11-WA Single Cycle, User-Initiated, Timing Diagram

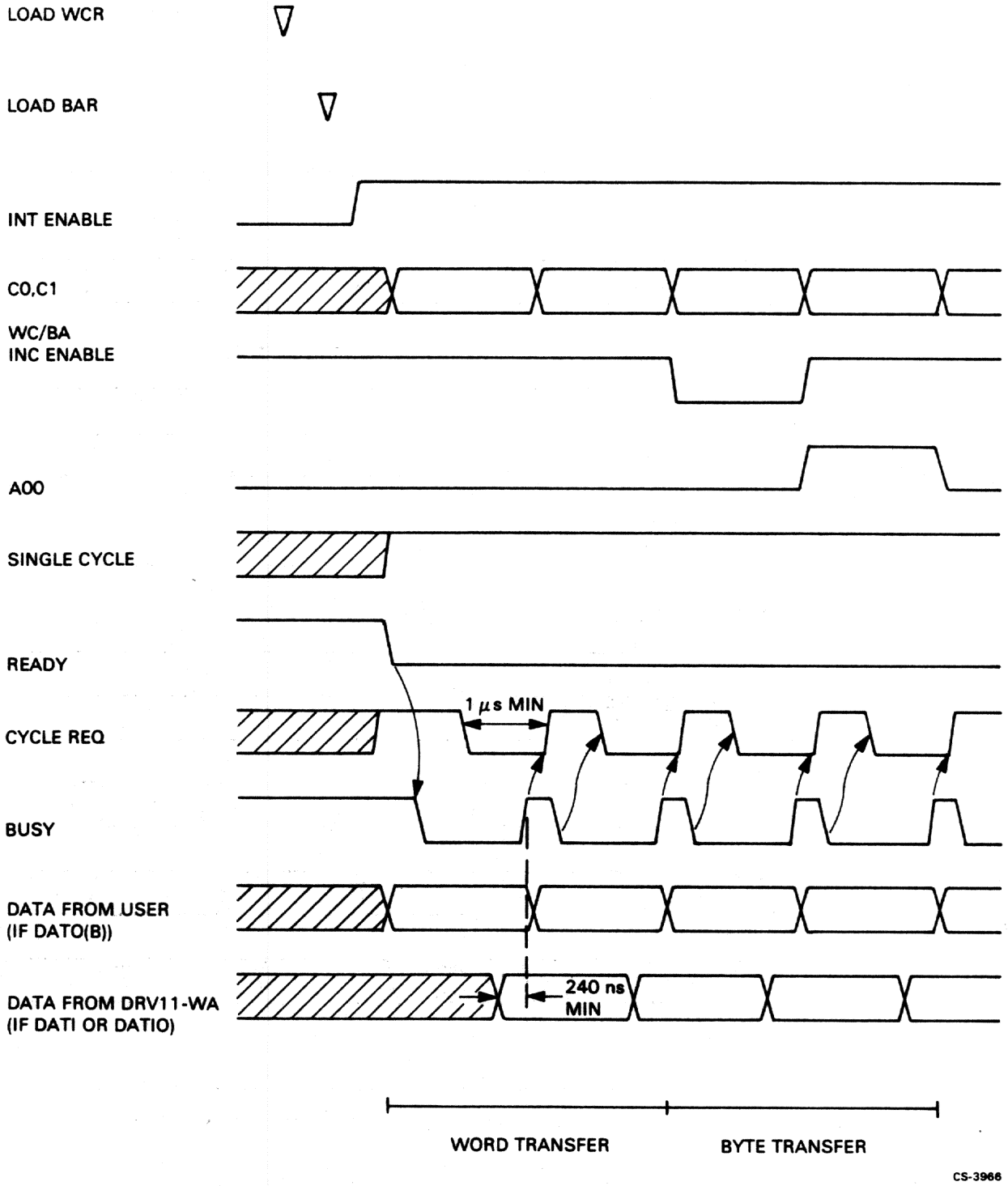


Figure 3-6 DRV11-WA Single Cycle, Program-Initiated, Timing Diagram

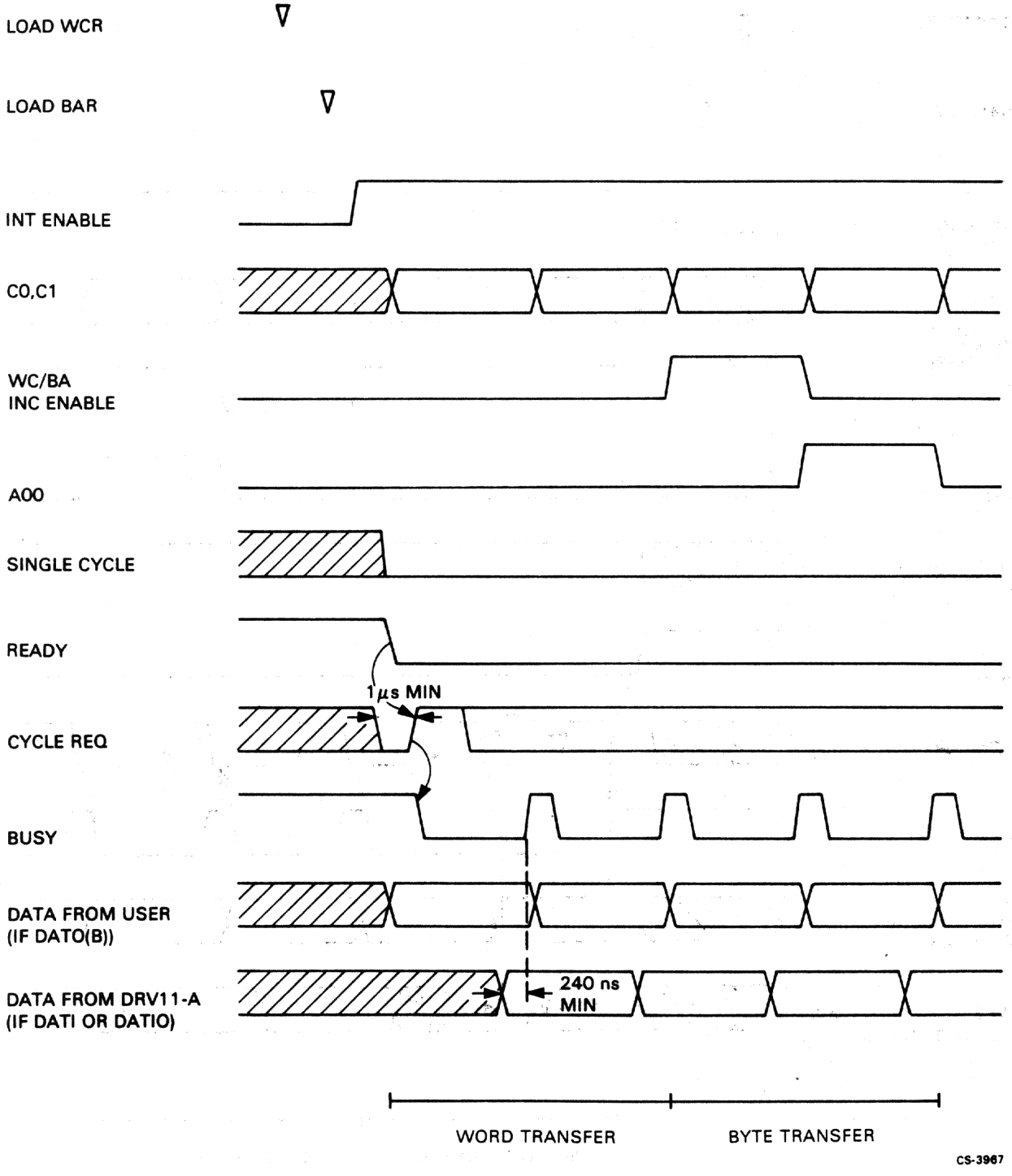


Figure 3-7 DRV11-WA Burst Mode, User-Initiated, Timing Diagram

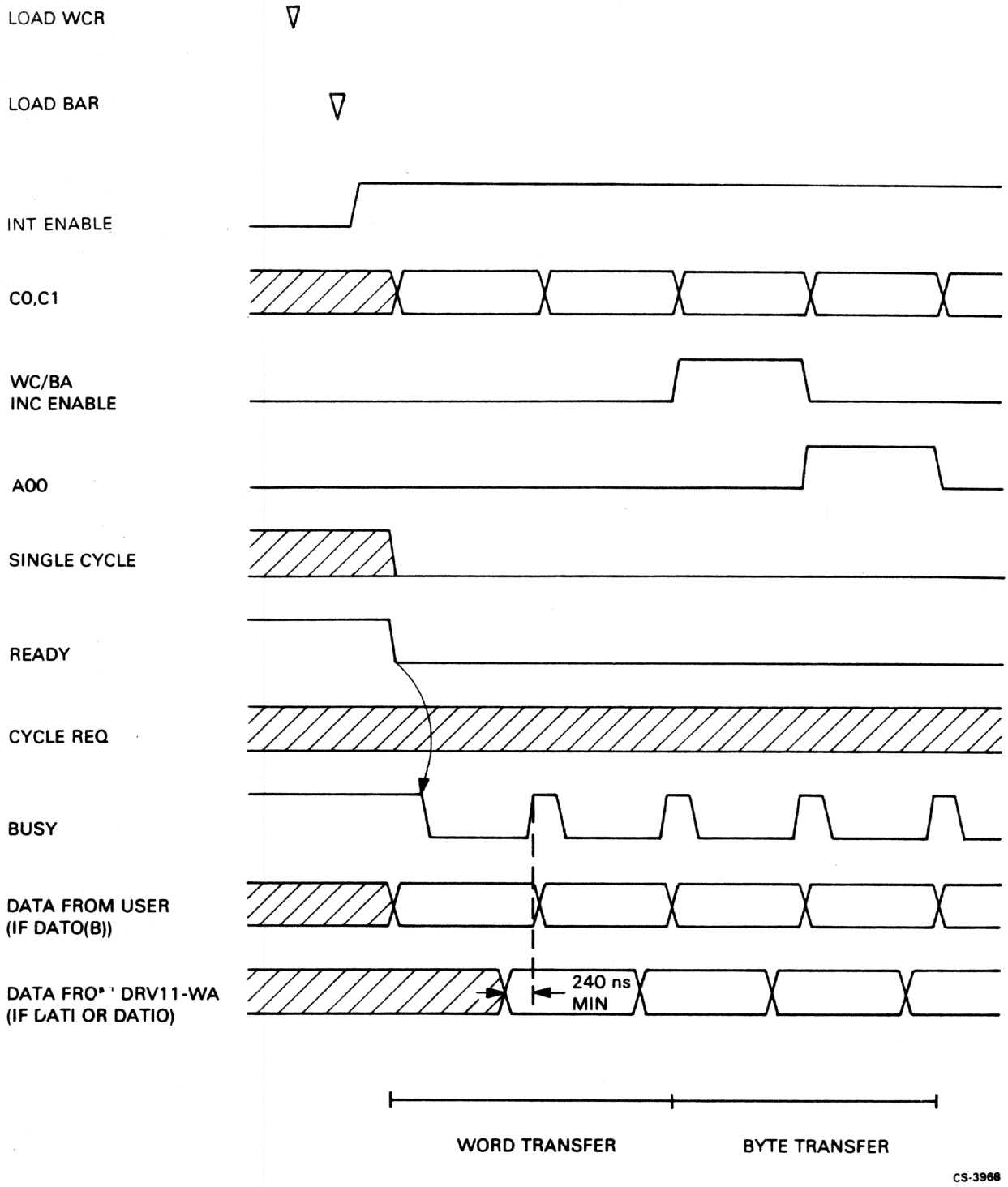


Figure 3-8 DRV11-WA Burst Mode, Program-Initiated, Timing Diagram

CHAPTER 4
PROGRAMMING

4.1 GENERAL

This chapter presents basic programming information for the DRV11-WA. The types of programming instructions, the use of the registers, program interrupts, and special program considerations are presented.

4.2 PROGRAMMING INSTRUCTIONS

All programming instructions used for the LSI-11 processor may be used for programming the DRV11-WA.

4.3 DRV11-WA REGISTERS

Six registers are used by the DRV11-WA:

- Word Count (WCR),
- Bus Address (BAR),
- Extended Bus Address Register (BAE),
- Control/Status (CSR), and
- Input and Output Data Buffers (DBRs).

The input and output data buffer registers share the same bus address while WCR, BAR, and CSR have unique addresses. If extended addressing mode (Q22) is selected, the BAR and BAE share the same address. To access the BAE for reading/writing, you must first access the BAR. The BAR and BAE are read/written to alternately.

4.3.1 WCR

Load the 16-bit WCR with the 2's complement (negative number) of DMA data transfers. At the end of each DMA cycle, the WCR is incremented by one. When the last transfer is made, the WCR is incremented to zero and an interrupt is requested. The WCR is not byte-addressable.

4.3.2 BAR

Load the 15-bit BAR with the address that specifies the memory location into which the first word is written, or from which the first word is read. Following the transfer of each word, the BAR is incremented by two, to point to the next higher sequential memory word location. In 18-bit mode, if the BAR overflows, it will increment the extended address bits and "wrap-around" to location zero. In extended addressing mode, if the BAR overflows, it will increment the BAE and "wrap-around" to location zero. Address bit A00 used for byte transfers, is driven by the user's device. The BAR is not byte-addressable.

4.3.3 BAE

If extended addressing mode (Q22) is selected, load the 6-bit BAE with the address that specifies the memory location into/from which the first word is written/read. If the BAR overflows, it

will increment the BAE extended address bits and "wrap-around" to location zero. The BAE is not byte-addressable.

4.3.4 CSR

The 16-bit CSR is monitored for interface status and loaded with control bits. The CSR is byte-addressable. Figure 4-1 shows the CSR bit assignments. The function of each bit is described in Table 4-1.

4.3.5 DBRs

The DBRs hold the 16-bit data words for transfer to memory from the user's I/O device (input DBR), or from memory to the user's I/O drive (output DBR). Both DBRs share the same bus address and are word- and byte-addressable.

4.4 PROGRAM INTERRUPTS

DRV11-WA interrupts are enabled by setting bit 06 (IE) of the CSR when the GO bit (bit 00) is issued (Figure 4-1 and Table 4-1). Interrupts can occur for the following reasons:

1. Word count overflow (normal interrupt), and
2. CSR ERROR bit (bit 15) set (special condition).

4.4.1 Word Count Overflow

An interrupt request is generated when the DRV11-WA WCR increments to zero and produces WC OFLO (word count overflow). WC OFLO sets READY in the CSR at the end of the DMA cycle.

4.4.2 CSR ERROR Bit (Bit 15)

The CSR ERROR bit can set for two possible reasons:

1. When bit 14 (NEX) of the CSR is set, or
2. When CSR bit 13 (ATTN) is set.

CSR bit 14 is set when a nonexistent (NEX) memory location is addressed and a reply from the addressed location is not received within 20 μs.

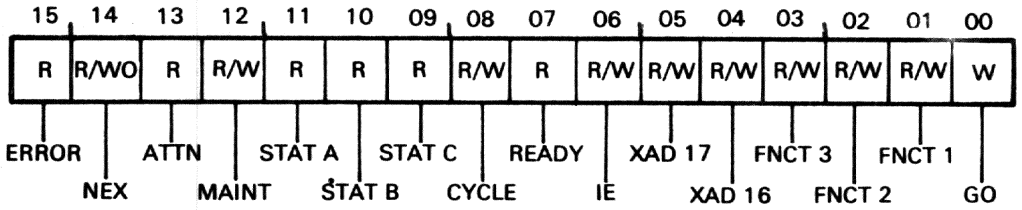
Bit 14 will set if a DATO bus cycle does not occur 20 μs after performing a DATIO bus cycle.

ATTN bit 13 sets the CSR ERROR bit when the user's I/O device drives ATTN high. ATTN is a user-defined function that can be utilized to generate an interrupt request.

4.5 FUNCTION AND STATUS BITS

There are three function bits (FNCT 1, 2, 3) and three status bits (STAT A, B, C), which the user can employ (at his option) to control and indicate the status of the DMA transfers and/or the user interface. The function bits (CSR bits 01, 02, and 03) can be used to transfer control data to the user's interface by means of the OUTPUT DATA BIT lines of the DRV11-WA. The status bits (CSR

bits Ø9, 1Ø, and 11) can be used to indicate the status information is on the DRV11-WA INPUT DATA BIT lines.



LEGEND:

R = READ ONLY
R/W = READ/WRITE
R/WO = READ/WRITE TO 0
W = WRITE ONLY. ALWAYS READS AS A 0.

CS-3969

Figure 4-1 CSR Format

Table 4-1 CSR Bit Functions

Bit	Function
ØØ	GO: Write-only bit; always reads as a zero. 1. Causes READY to be sent to the user's device, indicating that a command has been issued. 2. Allows DMA operation.
Ø1, Ø2, Ø3	FNCT 1, 2, 3: Read/write bits. 1. Three output bits available for user-defined functions. 2. Cleared by INIT.
Ø4, Ø5	XAD16, 17: For standard LSI buses (non-Q22). Read/write bits. Two bits used for extended addressing. Bits Ø4 and Ø5 increment with the address count when the BAR "wraps-around" to zero. For extended addressing LSI buses, if extended addressing mode is selected, these bits are read-only.
Ø6	IE: Read/write bit. 1. Enables interrupts to occur when READY is set. 2. Cleared by INIT.

Table 4-1 CSR Bit Functions (Cont)

Bit	Function
Ø7	READY: Read-only bit. Indicates that the DRV11-WA is able to accept a new command. Set by INIT, WCOFLO, ERROR; cleared by GO (bit ØØ).
Ø8	CYCLE: Read/write bit. CYCLE is used to prime a DMA bus cycle; set by CYCLE REQUEST, cleared during DMA cycle by INIT.
Ø9, 1Ø, 11	STAT A,B,C: Read-only bits. Three device status input bits that indicate the state of the DSTAT A, B, and C user signals. These bits are set and cleared by the user.
12	MAINT: Read/write bit. Maintenance bit for use with the MAINDEC diagnostic.
13	ATTN: Read-only bit. Indicates the state of the ATTN user signal; sets READY, ERROR.
14	NEX: Read/write to zero bit. 1. Nonexistent memory; indicates that as bus master, the DRV11-WA did not receive BRPLY or that a DATIO cycle was not completed. 2. Sets ERROR. 3. Cleared by INIT or by writing it to a zero.
15	ERROR: Read-only bit. 1. Indicates one of the following special conditions: a. NEX (bit 14) b. ATTN (bit 13) 2. Sets READY (bit 7) and causes an interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition as follows: a. NEX is cleared by writing bit 14 to zero. b. ATTN is cleared by the user device.

4.6 PROGRAMMING EXAMPLE

The following programs are sample programs for the DRV11-WA.

```
;*  SAMPLE PROGRAM FOR Q18 BIT MODE
;*   DO A 200 NPR DATA TRANSFER
DRVWCR=          172410
DRVBAR=          172412
DRVCSR=          172414
DRVDBR=          172416
PRO=             0

START:   MOV     #-200.,@#DRVWCR     ;WILL DO 200 XFER'S
         MOV     #DBUF,@#DRVBAR      ;SET UP BUFFER ADDRESS
         MTPS    #PRO                ;ENABLE INTR
         MOV     #101,@#DRVCSR       ;SET IE & GO
         BIS     #400,@#DRVCSR       ;SET CYCLE
WAIT:    BR      WAIT                ;WAIT HERE
```

```
;* SAMPLE PROGRAM FOR Q22 BIT MODE
;*  DO A 200 NPR DATA TRANSFER
DRVWCR=          172410
DRVBAR=          172412
DRVBAE=          172412
DRVCSR=          172414
DRVDBR=          172416
PRO=             0

START:   MOV    #-200.,@#DRVWCR    ;WILL DO 200 XFER'S
         TST    @DRVBAR            ;CLEAR BAE FLAG *
         MOV    #DBUF,@#DRVBAR     ;SET UP BUFFER ADDRESS
         MOV    #DBUF1,@#DRVBAE    ;SET UP EXTENDED BUFFER ADDRESS
         MTPS   #PRO               ;ENABLE INTR
         MOV    #101,@#DRVCSR      ;SET IE & GO
         BIS    #400,@#DRVCSR      ;SET CYCLE
WAIT:    BR     WAIT               ;WAIT HERE
```

* By accessing the BAR, a flag gets set to a one (1) (BAEFLAG=1). This flag automatically gets cleared by accessing the BAE register. To ensure that you will be accessing the BAR on your next attempt, it is advisable to clear the BAE flag in your program. This can be done by accessing any of the other registers (that is, TST @DRVWCR).

DRV11-WA GENERAL PURPOSE
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