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DR11-C
general device interface
user's manual

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general device interface
user's manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The DR11-C is a general-purpose interface between the PDP-11 Unibus and a user's peripheral (Figure 1-1). The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions. The DR11-C is software compatible with the DR11-A.

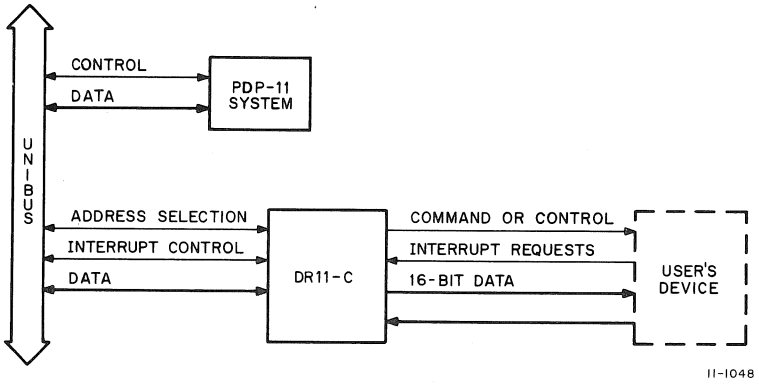

Figure 1-1 System Block Diagram

1.2 GENERAL DESCRIPTION

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

If an output operation is specified, information from the Unibus is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, NEW DATA READY control signals are supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to Unibus transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the maintenance mode, they are also used to check operation of the interface.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, thereby permitting the two processors to communicate. A description of the DR11-C used as an interprocessor buffer is provided in Chapter 4. DEC does not supply software for this configuration.

1.3 PHYSICAL DESCRIPTION

The DR11-C interface is packaged on a single M7860 quad module that can easily be plugged into either a small peripheral slot in the processor or into one of the four slots in a DD11-A Peripheral Mounting Panel (Figure 1-2). Appendix A shows the method of installing the DR11-C in a BB11 Blank Mounting Panel. Power is applied to the logic through the power harness already provided in the BA11 mounting box. The required current is approximately 1.5A at +5V. No −15V power source is needed.

The M7860 module has two Berg connectors for all user input/output signals. Two M971 connector boards, which are *not* supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two BC08R cables. Note that this cable is a "mirror image" rather than a straight one-to-one cable (Figure 3-1).

Specifications for the basic DR11-C are given in Table 1-1. The DR11-C interface is available in the following standard configuration:

a. one M7860 interface module
b. one BC08R-1 maintenance cable
c. applicable documentation

The following accessories are available for interfacing and may be ordered separately:

a. BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8. 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.

b. M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.

c. H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

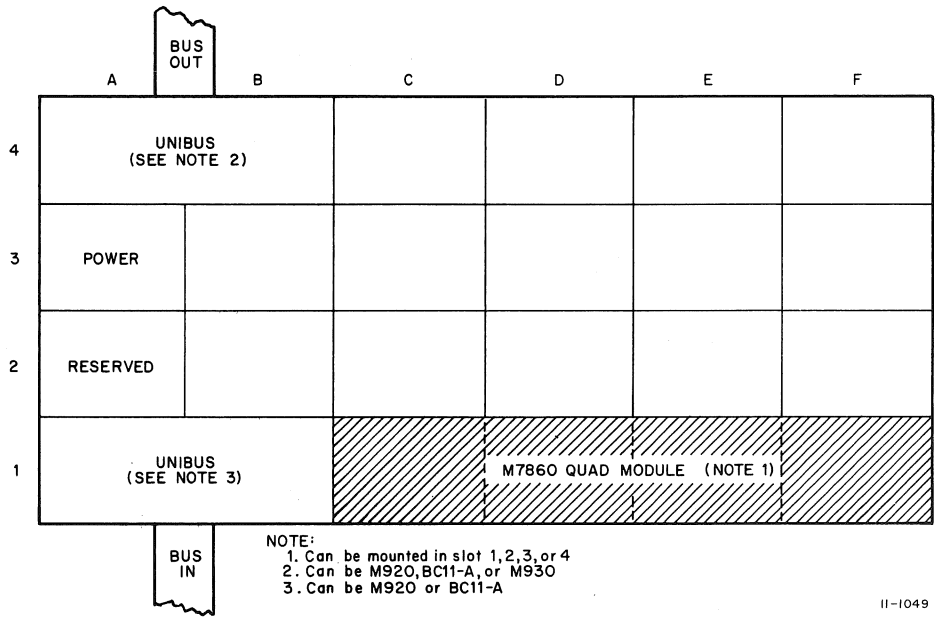

Figure 1-2 Typical M7860 Quad Module Mounting In a DD11-A

Table 1-1
DR11-C Specifications

Registers	Status and Control Register (DRCSR) Output Buffer Register (DROUTBUF) Input Buffer Register (DRINBUF)
Register Addresses	DRCSR – 767770 DROUTBUF – 767772 DRINBUF – 767774 } may be changed by user
Interrupts	Priority = BR5 (may be changed by jumper plug) Vector = 300, 304 (user selectable) Types = REQUEST A, B (function defined by user)
Control and Status Bits	Controlled by program = INT ENB A, B; CSR0, CSR1 Controlled by device = REQUEST A,B
Inputs	One standard TTL unit load; diode protection clamps to ground and +5V
Outputs	TTL levels capable of driving 8 unit loads except for the following: NEW DATA READY = 30 unit loads DATA TRANSMITTED = 30 unit loads INIT (initialize) = common signal on both connectors driven by one 30-unit load driver
Signals	NEW DATA READY – drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor DATA TRANSMITTED – drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor INIT (initialize) – common signal on both connectors driven by one 30-unit load driver NEW DATA READY LO H – drives 30 unit loads, positive pulse, 400-ns wide unless width is changed by an external capacitor (only on etch revision E or later) NEW DATA READY HI H – drives 30 unit loads, positive pulse, 400-ns wide unless width is changed by an external capacitor (only on etch revision E or later)
Data Inputs	16-bit word from the external device
Data Outputs	16-bit word from the Unibus. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.
Maintenance Mode	A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 07 to read as CSR1 and CSR0, respectively.
Size	Consists of a single quad module (M7860)
Mounting	M7860 module occupies 1/4 of a DD11-A (or equivalent) or one of two controller slots in a KA11, KC11, or other PDP-11 processor system unit.
Power	≃1.5A @ +5V (derived from power supply in mounting box where DR11-C is installed)

CHAPTER 2
SOFTWARE INTERFACE

2.1 SCOPE

This chapter presents a detailed description of the three DR11-C registers (Figure 2-1). These registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their addresses. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or the occurrence of a power-up or power-down condition of a system power supply.

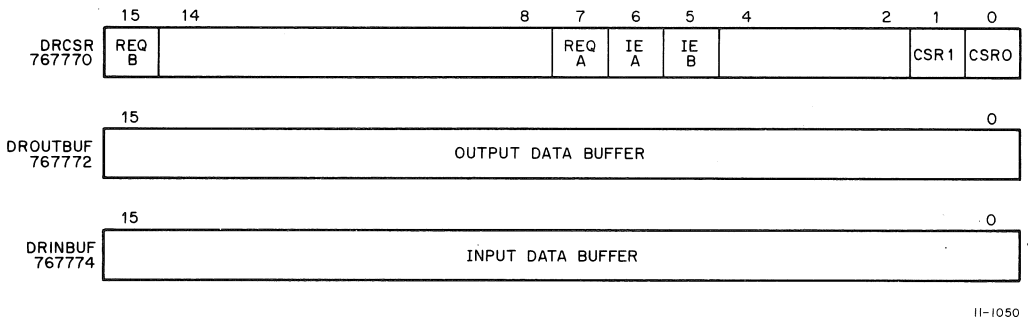

Figure 2-1 DR11-C Register Assignments

The device registers and associated addresses are listed in Table 2-1. Note that these addresses can be changed by altering the jumpers on the address selection logic. However, any programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed. Paragraph 2.5 discusses priority levels and the addressing scheme when more than one DR11-C is used.

Table 2-1
Standard DR11-C Register Assignments

Register	Mnemonic*	Address
Control and Status Register	DRCSR	767770
Output Buffer	DROUTBUF	767772
Input Buffer	DRINBUF	767774

* First two letters of mnemonic (DR) refer to DR11-C interface; the remaining letters represent the mnemonic of a specific register.

Paragraphs 2.2 through 2.4 describe operation of the DR11-C registers. Note that unused bits are always read as 0s. Loading unused or read-only bits has no effect on the bit position.

2.2 INPUT BUFFER REGISTER (DRINBUF)

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the Unibus. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the Unibus for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

2.3 OUTPUT BUFFER REGISTER (DROUTBUF)

The output buffer is a 16-bit read/write register that may be read or loaded from the Unibus. Information from the bus is loaded into this register under program control. At the time of loading, pulsed signals (NEW DATA READY) are generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic.

The DROUTBUF is cleared by INIT.

2.4 CONTROL AND STATUS REGISTER (DRCSR)

The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT ENB (interrupt enable) bits which are under program control. Two other bits (CSR0 and CSR1) are controlled from the Unibus and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 07 for ready indications and both of these bits can generate interrupt requests. In addition, bit 00 is normally used for start or go commands.

Table 2-2 gives the bit assignments and provides a brief description of each bit in the control and status register.

2.5 ADDRESS AND VECTOR ASSIGNMENTS

The register address and vector address assignments are listed in Table 2-3. Note that four addresses are allotted for each DR11-C even though only three addresses are used.

Table 2-2
DRCSR Bit Assignments

Bit	Name	Meaning and Operation
15	REQUEST B	This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT.
14–08	Unused	Not Applicable
07	REQUEST A	Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Read-only bit. Cleared by INIT.
06	INT ENB A	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
05	INT ENB B	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
04–02	Unused	Not Applicable
01	CSR1	This bit can be loaded or read (under program control) from the Unibus and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Read/write bit (can be loaded or read by the program). Cleared by INIT.
00	CSR0	Performs the same function as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.

Table 2-3
Address Assignments

No. of DR11-Cs	Register Addresses	Vector Addresses
DR11-C No. 0	767776 – 767770	300, 304
DR11-C No. 1	767766 – 767760	310, 314
DR11-C No. 2	767756 – 767750	320, 324
.	.	.
.	.	.
.	.	.
DR11-C No. 7	767706 – 767700	370, 374
.	.	.
.	.	.
.	.	.
DR11-C No. 15	767606 – 767600	470, 474

The addresses in the above table were assigned assuming that the system contains only DR11-Cs and no DR11-As. If DR11-A interfaces are present in the system, addresses must be assigned for them before assigning DR11-C addresses.

The DR11-C has floating vectors which are assigned in the following sequence:

a. Starting at 300 and proceeding upward, assign all DC11s.
b. Then any extra KL11s called for (VT05, VT06, LC11).
c. Then any DP11s
d. Then any DM11s
e. Then any DN11s
f. Then any DM11-BBs
g. Then any DR11-As
h. Then any DR11-Cs

NOTE
Some devices use only one vector address.

The register address and vector address assignments are implemented by changing jumpers on the M7860 module. The register address lines are jumpered for a 0; the vector address lines are jumpered for a 1.

The priority level of both interrupts must be the same, with interrupt A (REQUEST A) on a higher sublevel than interrupt B (REQUEST B). REQUEST A uses the vector block with the least significant octal digit equal to 0 and REQUEST B uses the vector block with the least significant octal digit equal to 4 (i.e., REQUEST A using 430 and REQUEST B using 434). The M7860 module contains a priority jumper plug which is normally set at the BR5 level. This priority level may be changed by changing the jumper plug. (Levels of BR4 through BR7 are available.)

Direct memory access (NPR request) is not possible with a DR11-C interface.

CHAPTER 3
USER INPUT/OUTPUT SIGNALS

3.1 SIGNAL LIST

Tables 3-1 and 3-2 list the signals available to the user's device. Input loading refers to the number of TTL unit loads the input signal must drive. A unit load is defined as:

2.4V $\leqslant$ Input high voltage $\leqslant$ 5.0V @ 40 μA
0.0V $\leqslant$ Input low voltage $\leqslant$ 0.4V @ – 1.6 mA

where current flow is defined as positive into the driven gate. All inputs are one standard TTL unit load and have diode protection clamps to ground and +5V.

Table 3-1
User Input Signals

Name	No. of Signals	Loading	Description
IN00 through IN15	16	1 each	Data input from user device. The levels presented on these lines can be examined by reading the input buffer register (DRINBUF) with an instruction such as MOV DRINBUF, R0. This data is transferred to the Unibus when the DR11-C responds to a DATI bus cycle. Because the input buffer register consists of gating logic, the device must hold the IN lines asserted until read onto the Unibus. This is indicated by the trailing edge of the DATA TRANSMITTED pulse. Logic levels are: +3V = 1; 0V = 0.
REQUEST A, B	2	1 each	Two request lines that can be asserted (+3V) by the external device to initiate an interrupt sequence or to generate a flag that can be tested by the program. These request lines must be levels that are held asserted for the entire interrupt sequence and would normally be cleared by NEW DATA READY or DATA TRANSMITTED. Although the external device controls these request lines, an interrupt sequence can only be started by the program because of the associated interrupt enable (IE) bits under program control. Methods of generating these request levels in the user's device are described in Chapter 4. Logic levels are: +3V = 1; 0V = 0.

Table 3-2
User Output Signals

Name	No. of Signals	Driving Capability	Description
OUT00 through OUT15	16	7 each	Data output to user's device. These signals represent the contents of the output buffer register (DROUTBUF), which is loaded under program control (e.g., MOV R0, DROUTBUF). Logic levels are: +3V = 1; 0V = 0. All lines are cleared to 0 by INIT.
NEW DATA READY	1	30	This pulsed signal is generated when either byte of the DROUTBUF is loaded to indicate to the user's device that the buffer is loaded with data from the Unibus. The signal is true (+3V) as soon as the DROUTBUF has been addressed for loading and remains true for approximately 400 ns; therefore, the trailing edge of this pulse should be used for sampling the lines at the user's end of the cable. This duration can be changed as described in Paragraph 3.2.
NEW DATA READY LO	1	30	This pulsed signal is only generated when the low byte of the DROUTBUF is loaded. The signal is only available on M7860 modules of etch revision E or later. Otherwise, the description for NEW DATA READY applies.
NEW DATA READY HI	1	30	This pulsed signal is only generated when the high byte of the DROUTBUF is loaded. The signal is only available on M7860 modules of etch revision E or later. Otherwise, the description for NEW DATA READY applies.
DATA TRANSMITTED	1	30	This pulsed signal is generated when the DRINBUF register is read by a DATI sequence to inform the user's device that the transfer has been completed. The signal is true (+3V) as soon as the DRINBUF has been addressed for reading and remains true for approximately 400 ns; therefore, the lines should be held until the trailing edge of this signal. This duration can be changed by the user as described in Paragraph 3.2.
CSR0, 1	2	7 each	Device status bits 0 and 1. The levels applied to these lines appear as bits 00 and 01 in the control and status register (DRCSR). These two lines can be loaded or read from the Unibus (under program control). When the DR11-C is used as an interprocessor buffer, these bits are used for communication between the two processors. Logic levels are: +3V = 1; 0V = 0. Cleared by INIT.
INIT	1	30 (one driver for the signal on both of the cables)	This line is true (+3V) whenever the Unibus is initialized, which occurs during any one of the following conditions: a programmed RESET instruction is issued, the console START switch is depressed, or a power-up or power-down condition occurs.

All outputs are TTL levels capable of driving seven unit loads with the following exceptions:

NEW DATA READY – 30 unit loads
NEW DATA READY LO – 30 unit loads
NEW DATA READY HI – 30 unit loads
DATA TRANSMITTED – 30 unit loads
INIT – a common signal on both connectors which is driven by one 30-unit load driver

The NEW DATA READY and DATA TRANSMITTED signals are described more fully in Paragraph 3.2.

3.2 VARIABLE SIGNALS

The NEW DATA READY signals are positive pulses which load the output buffer register on the leading edge of the pulse. The DATA TRANSMITTED signal is also a positive pulse and is generated when the input buffer register is read by a DATI sequence.

Both of these signals are approximately 400 ns in duration. However, this duration can be changed by adding an external capacitor between back panel pin EB1 and ground. Some typical capacitor values and resultant pulse widths are listed in Table 3-3. The effect of the additional capacitance results in lengthening the bus cycle. This is, therefore, a factor in NPR latency considerations.

Table 3-3
External Capacitor Values

External Capacitor	NEW DATA READY	DATA TRANSMITTED
none	350 ns	450 ns
470 pF	500 ns	600 ns
820 pF	600 ns	750 ns

3.3 CONNECTORS

Figure 3-1 illustrates the layout for the M7860 module, the Berg connectors, and the M971 connector modules referenced in Tables 3-4 and 3-5.

The input and output signals are listed in Table 3-4 and indicate the Berg pin on the M7860 module. Table 3-5 lists all pin connections (in pin number order) for the Berg header on the M7860 module, the Berg header on the M971, and the M971 board pins. Figure 3-2 illustrates the physical location of the pins on the Berg connector.

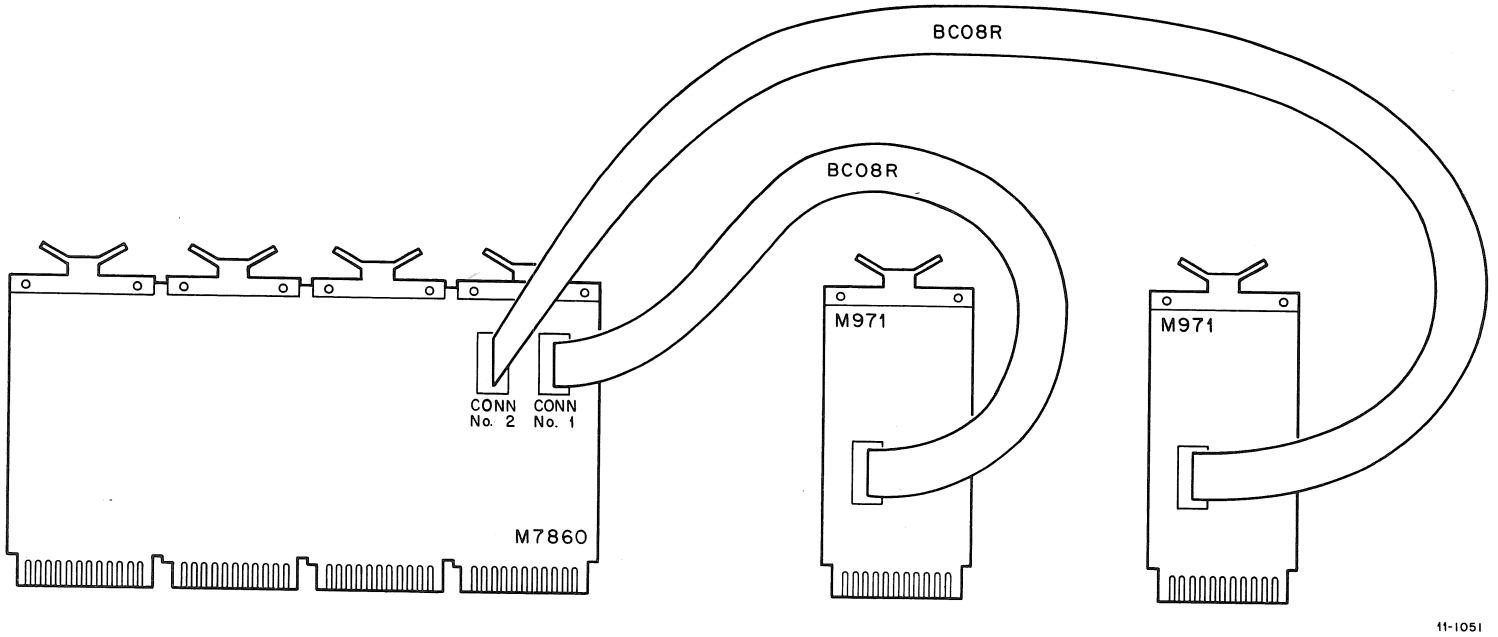

Figure 3-1 M7860 Module Interconnect Diagram
When The Optional M971 Connectors Are Used.

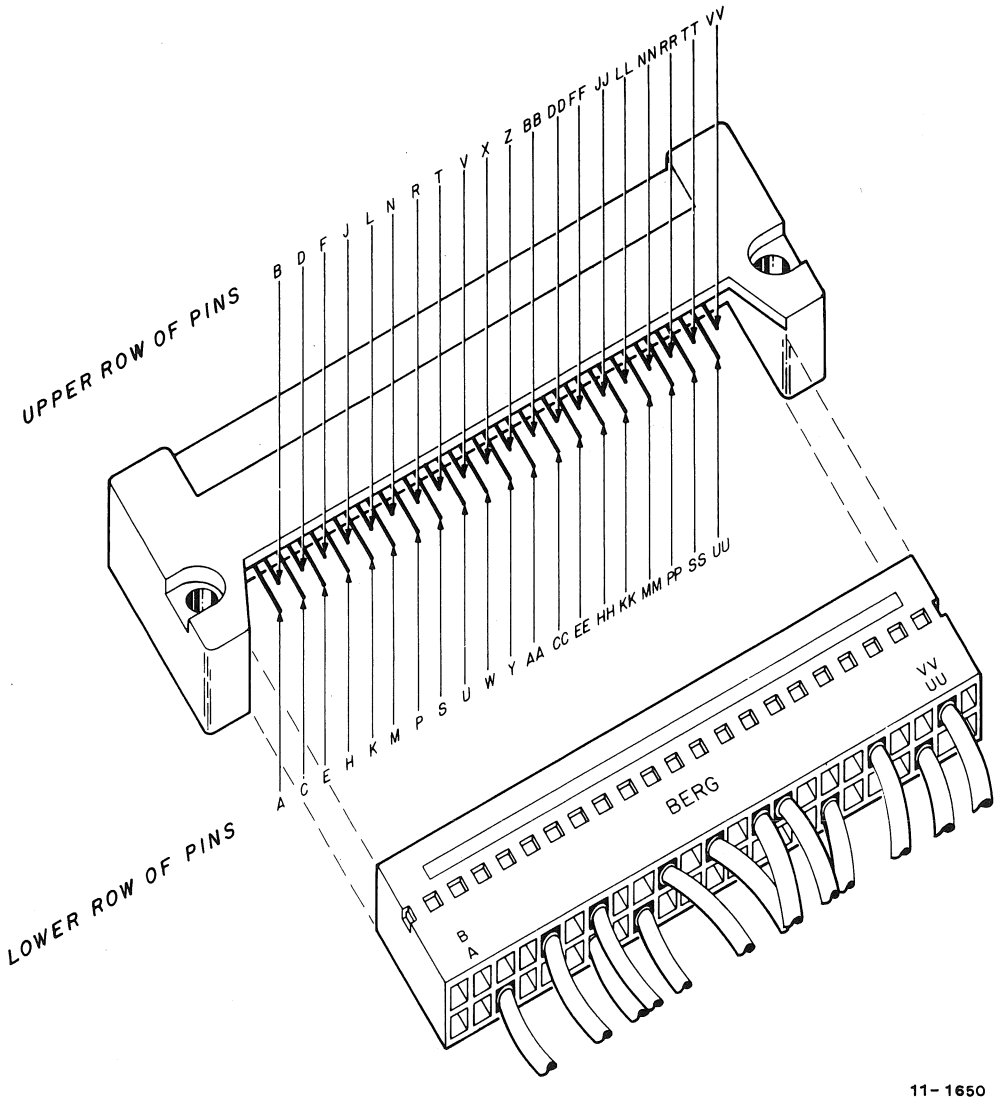

Figure 3-2 Berg Connector

Table 3-4
Input and Output Signals

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	CC	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS.*	2	C
			CSR0	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

* Pulse signals, approximately 400-ns wide. Width can be changed by user.

Table 3-5
Pin Connections

M971		M7860				M971	
Board	Berg Header	Connector No. 2 Pin	Name	Connector No. 1 Name	Pin	Berg Header	Board
V2	A	VV	OPEN	OPEN	A	VV	A1
U1	B	UU	GND	OPEN	B	UU	A2
U2	C	TT	IN00	OUT00	C	TT	A1
V1	D	SS	GND	OPEN	D	SS	A2
T2	E	RR	INIT H	NEW DATA RDY HI	E	RR	B1
T1	F	PP	GND	OPEN	F	PP	B2
T2	H	NN	INIT H	NEW DATA RDY LO	H	NN	C1
T1	J	MM	GND	GND	J	MM	C2
S2	K	LL	IN01	OUT01	K	LL	D1
S1	L	KK	IN04	OUT04	L	KK	D2
R2	M	JJ	GND	GND	M	JJ	E1
R1	N	HH	IN05	OUT05	N	HH	E2
P2	P	FF	OPEN	INIT H	P	FF	F1

(continued on next page)

Table 3-5 (Cont)
Pin Connections

M971		M7860				M971	
Board	Berg Header	Connector No. 2 Pin	Name	Name	Connector No. 1 Pin	Berg Header	Board
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	CC	IN07	OUT07	T	CC	H2
M2	U	BB	IN03	OUT03	U	BB	J1
M1	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M1
J1	BB	U	IN12	OUT12	BB	U	M2
H2	CC	T	GND	GND	CC	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
E1	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSR0	REQ A	LL	K	S2
C2	MM	J	GND	GND	MM	J	T1
C1	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	OPEN	OPEN	RR	E	T2
A2	SS	D	OPEN	GND	SS	D	V1
A1	TT	C	DATA TRANS.	OPEN	TT	C	U2
A2	UU	B	OPEN	GND	UU	B	U1
A1	VV	A	OPEN	NEW DATA RDY	VV	A	V2

CHAPTER 4
DR11-C APPLICATIONS

4.1 BASIC INTERFACE

Figure 4-1 illustrates a typical user's device interface, consisting of a basic control section and a data assembly register.

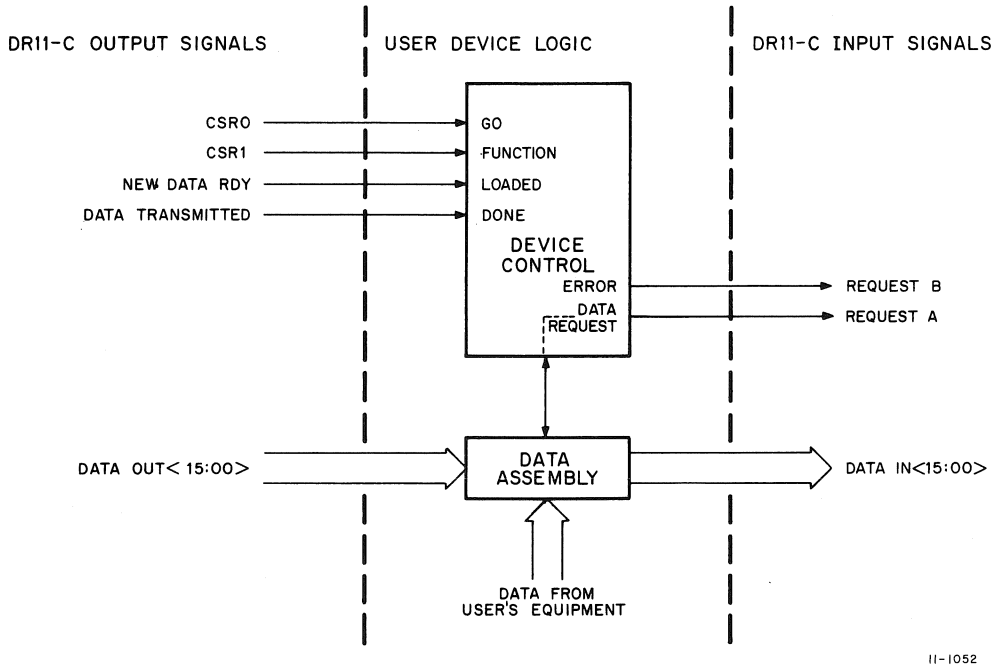

Figure 4-1 Basic Interface

Operation of the interface is initiated by the GO level. The FUNCTION bit informs the device whether it is to perform a read or write operation. When data is ready for transfer to the Unibus or data is required from the Unibus, a low-to-high transition on DATA REQUEST activates the REQUEST A line. The REQUEST A line initiates an interrupt sequence provided the INT ENB A bit in the DR11-C status register has been set. If the desired function is to load data into the user device, a LOADED (NEW DATA READY) pulse informs the device control when the data is ready for transfer. If a write function has been selected, a DONE (DATA TRANSMITTED) pulse informs the device control when the DR11-C has completed strobing of the data. The ERROR

line becomes true if some type of error condition occurs in the device. This ERROR line (REQUEST B) can either be monitored by the program or can be used to initiate an interrupt sequence (provided INT ENB B is set) to cause the program to branch to an error handling routine.

With the signals available to the user, there are many possible variations to this basic interface. For example, the two CSR bits (CSR0 and CSR1) could provide a 2-bit code to select one of four operations to be performed by the external device.

Another possibility would be to use one REQUEST line for interrupts and the other REQUEST line for a flag (associated INT ENB not used) in order to inform the program of the desired operation to be performed on the data.

A third possibility might be to use the two CSR bits as a selection code and have DONE (NEW DATA READY) serve as a start command so that device operation begins as soon as the DR11-C output buffer has been loaded from the bus.

4.2 INTERRUPT SERVICED INTERFACE

Figure 4-2 is an example of an interrupt serviced interface that employs a DR11-C to interface an analog-to-digital converter (ADC) to the Unibus. This interface allows the processor to concurrently execute instructions of another program while the ADC performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the data after it has been collected. This interface eliminates the necessity of having the processor spend time testing for a ready signal.

Note that this example uses only the REQUEST A line. The available REQUEST B line can be used as an ERROR indicator, if desired, and the two CSR lines could be used to initiate other actions within the external device.

A similar, and more detailed, example of this type of interface is given in the *PDP-11 Peripherals Handbook.* However, the example presented in this handbook uses a DR11-A which does not have all of the capabilities of the DR11-C interface.

4.3 GENERATING REQUEST LINE LEVELS

Two request lines (REQUEST A, B) are furnished and may be asserted (+3V) by the user's device to initiate an interrupt sequence or to produce a flag that can be tested by the program. The request lines must be levels and must remain asserted for the entire interrupt sequence. Typically, they are generated in the user's device by a REQUEST flip-flop which is set by the device when an interrupt is requested and cleared by the interrupt service routine by means of the NEW DATA READY or DATA TRANSMITTED signals.

Figure 4-3 represents the control circuit necessary to generate the REQUEST A H and REQUEST B H signals. Similar logic could be used if it is desired to have CSR0 H and CSR1 H control the clearing of the REQUEST lines.

4.4 INTERPROCESSOR BUFFER

Two DR11-C interfaces can be interconnected to allow data transfers and intercommunication between two PDP-11 Systems. Figure 4-4 is a simplified diagram of this interconnection.

The two interconnecting cables are the same as the MAINT cable and may be procured in either 1-ft or 25-ft lengths. Maximum allowable cable length is 25 ft.

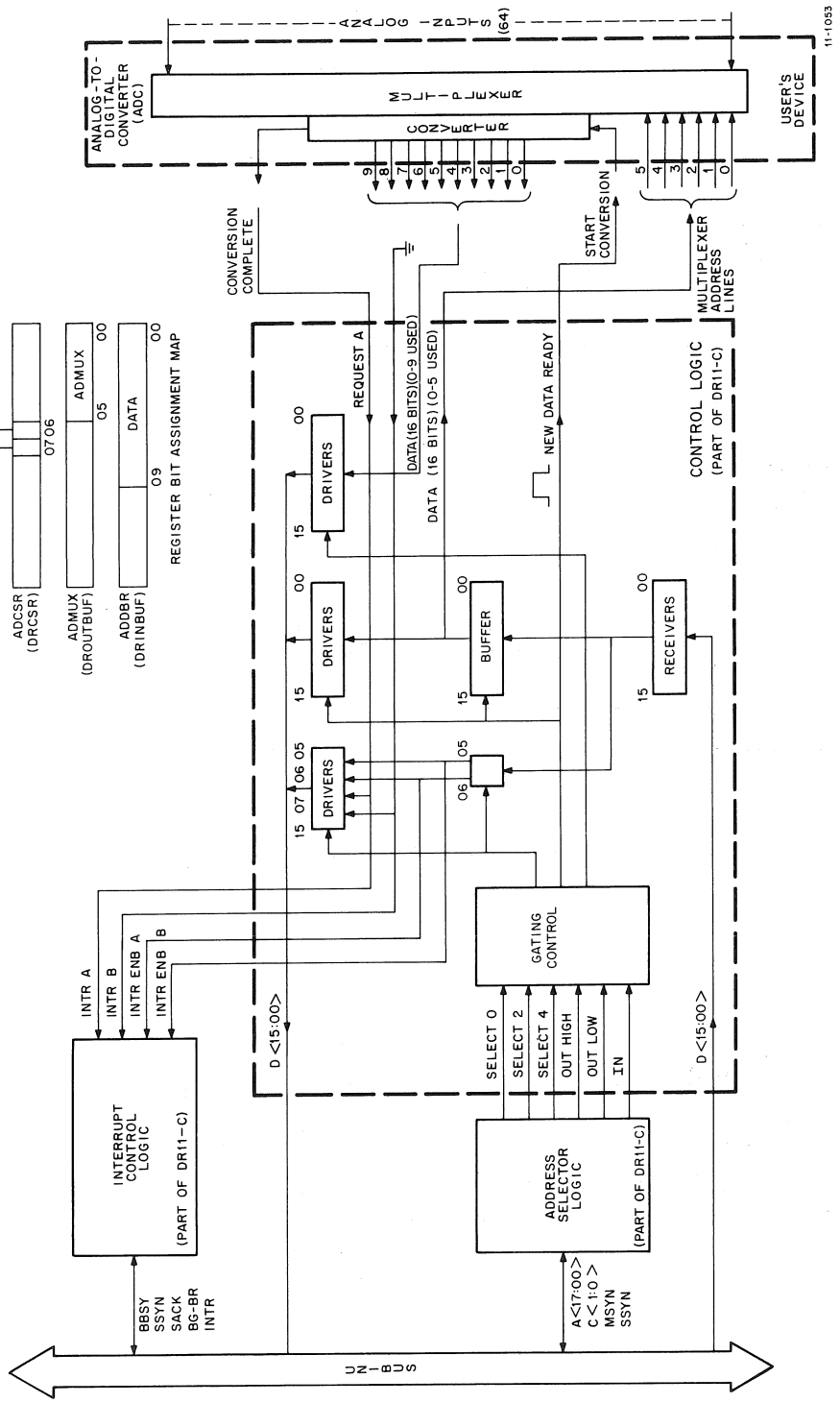

Figure 4-2 Interrupt Serviced Interface

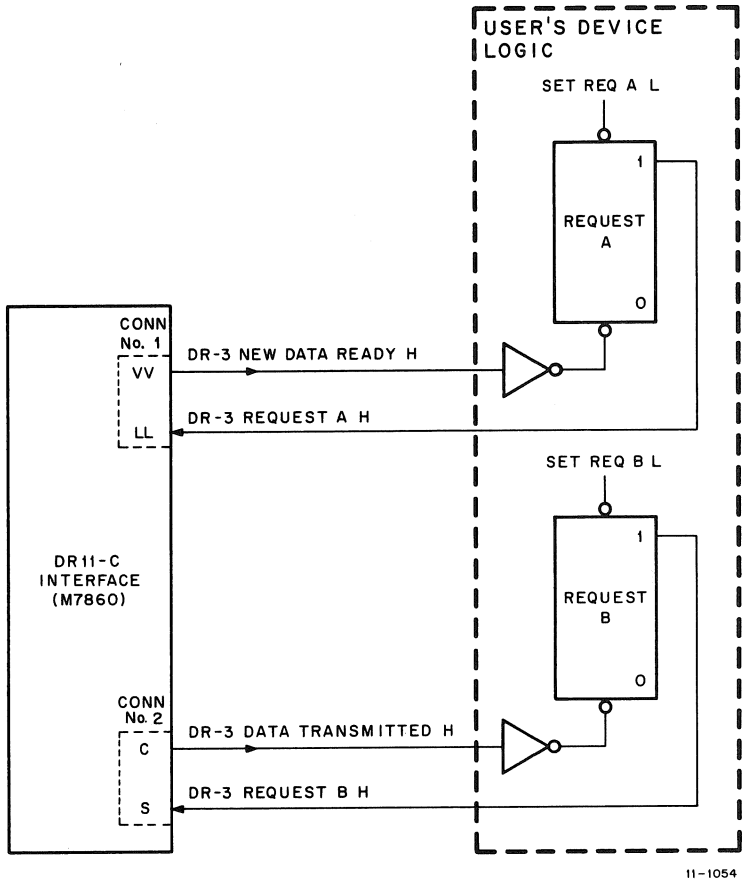

Figure 4-3 Request Line Control Logic

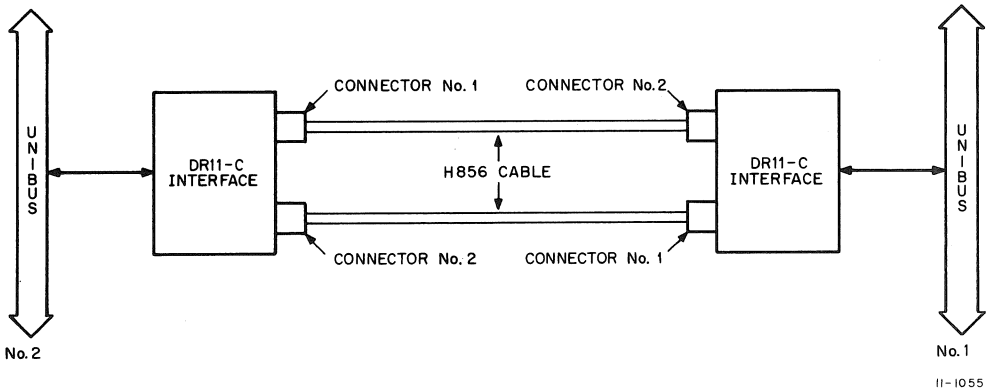

Figure 4-4 Interprocessor Buffer, Simplified Diagram

The Connector No. 1 of the first DR11-C is connected to Connector No. 2 of the second DR11-C This causes all of the output lines (OUT00 – OUT15) of the first interface to be connected to the corresponding input lines (IN00 – IN15) of the second interface (refer to pin connections given in Table 3-5). The CSR0 and CSR1 lines of the first unit are connected to the REQ A and B lines, respectively, of the second unit.

Connector No. 2 of the first unit is connected to Connector No. 1 of the second unit. This connects the IN lines and REQ lines of the first unit to the OUT lines and CSR lines of the second unit.

With the two PDP-11 buses interfaced in this manner, setting a CSR bit in one interface activates the REQ line in the other interface to initiate an interrupt sequence. Data can then be loaded from the bus into the DROUTBUF of the first unit for transfer to the DRINBUF of the second unit.

When DR11-Cs are used as interprocessor buffers, a power fail situation on either Unibus must be handled by the software. The software routine would be entered from the power fail trap vector and, by use of the REQUEST lines, would inform the other DR11-C that power is failing.

APPENDIX A
USE OF BB11

The BB11 Blank Mounting Panel is a prewired system unit designed for general interfacing. Figure B-1 illustrates the method of mounting a DR11-C interface into a BB11 system unit, assuming that the BB11 has slot 1 wired as a DD11-A or equivalent.

The first step is to mount the DR11-C in one of the four slots. Two of the remaining slots are used for the two M971 Cable Connector modules. This leaves 12 double-height slots available for mounting user interface logic.

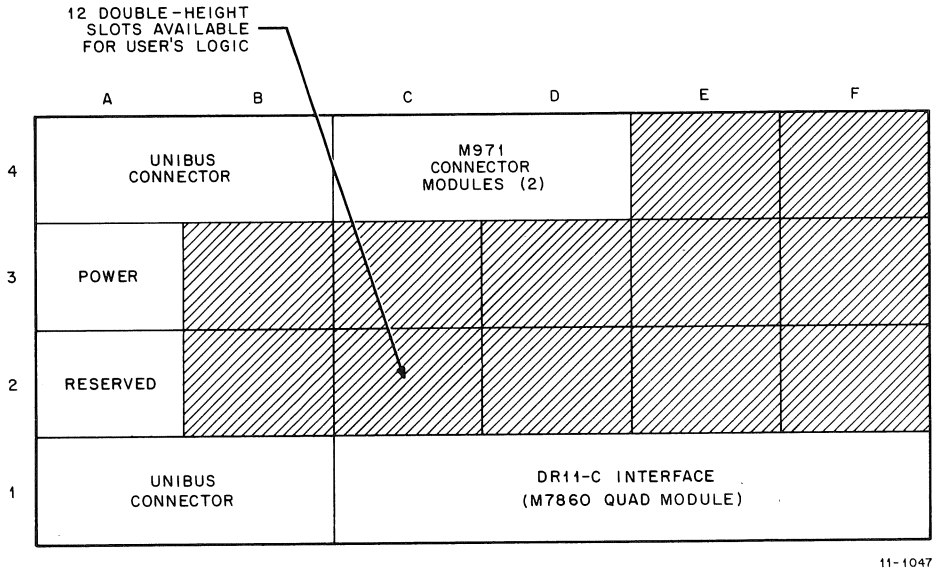

Figure A-1 DR11-C Mounted in BB11 System Unit

Reader's Comments

DR11-C GENERAL DEVICE
INTERFACE USER'S MANUAL
EK-DR11C-OP-001

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_____

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What features are most useful? _____

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