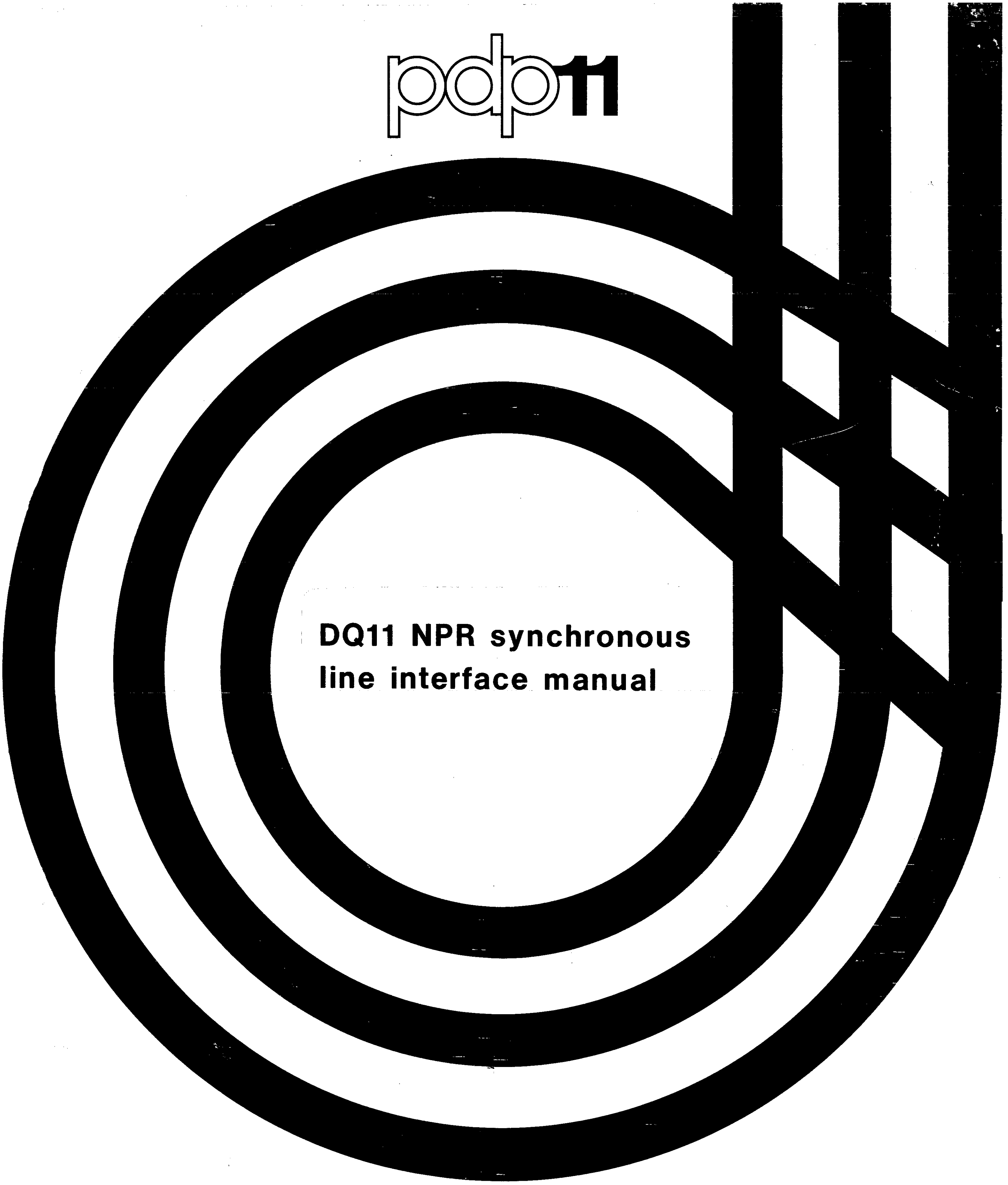
pdp11



DQ11 NPR synchronous line interface manual

digital

EK-DQ11-MM-002

DQ11 NPR synchronous line interface manual

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ERRATA SHEET

DQ11 NPR SYNCHRONOUS LINE INTERFACE MANUAL
(EK-DQ11-MM-02A)

Refer to Paragraph 3.6.6 which contains five sample programs. All programs have an identical error in line 25.

Line 25 now reads:

```
25   01032    062737        ADD #200, @ # WENP
              000200
              002002
```

Change Line 25 to read:

```
25   01032    062737        ADD #400, @ # WENP
              000400
              002002
```

Printed in U.S.A.

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides the user with the information necessary to install, operate and maintain the *DQ11 NPR Synchronous Line Interface*. The manual is organized into four chapters.

Chapter 1 – Introduction
Chapter 2 – Installation
Chapter 3 – Programming
Chapter 4 – Detailed Description

This chapter contains general specifications, configurations and an overall functional description.

1.2 GENERAL FEATURES AND SPECIFICATIONS

1.2.1 Features

The DQ11 is a high-speed, double-buffered communications device designed to interface the PDP-11 processor to a serial-synchronous communications channel. This interface allows the PDP-11 to be used for remote batch and remote concentrator applications. With the DQ11, the PDP-11 can also be used as a front-end, synchronous-line controller to handle remote and local synchronous terminals.

Transmit and receive data transfers between the PDP-11 Unibus and the DQ11 are handled as Non-Processor Requests (NPR). These are direct memory or device access data transfers without processor supervision. As an NPR device, the DQ11 provides extremely fast access to the PDP-11 Unibus and can transfer data at exceptionally high rates once it gains control. The PDP-11 processor state is not affected by NPR transfers, since they occur on a cycle-steal basis.

Standard features:

Non-Processor Request (NPR) data transfers for transmit and receive

Transmission speeds up to 1 megabaud (Wideband communications network interface capability)

Full- or half-duplex operation

Vertical Redundancy Check (VRC) – Parity (odd or even) is switch-selectable

Data set control

Switch-selectable (one or two) sync characters to character frame

Programmable sync character

Programmable character size; up to 16 bits per single character and 8 bits or less for double characters

Double-buffered transmit and receive data registers

Double-buffered character count and bus address register

Auto idle, strip sync, and half-duplex program selectable

Diagnostic-controlled, self-testing capabilities

Three switch-selectable control characters for program interrupts

Interfaces to Bell 201 and 303 or equivalent modems

Additional features available through expanded hardware:

Programmable error detection using a polynomial of up to 24 bits to implement Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC)

Programmable character recognition and hardware sequence control for protocol handling

Internal crystal clock – set to accommodate user baud rate.

1.2.2 General Specifications

Operational Modes
Full- or half-duplex

Interfaces
EIA or current mode

Character Transfer Rate
Up to 62,500 characters per second (1 megabaud, half-duplex with only basic unit)

Code Format (Protocol)
IBM Binary SYNCHronous

Capability
ASCII

Character Size
Programmable up to 16 bits with double-character transfers for characters of 8 bits or less

Error Detection
Basic Unit – Vertical redundancy check

Expander Unit – Programmable polynomial for longitudinal redundancy check or cyclic redundancy check

Character Recognition
Basic Unit – Up to 3 switch-selectable control characters for program interrupts

Expander Unit – Up to 16 programmable single- and/or double-characters for character recognition

Bus Addressing
Up to 128K (max)

Character Count
Block transfer size
Up to 64K characters

Clocking
Internal crystal clock option specified at baud rate or external clock (modem)

Sync Character
Program selected

Sync Detection
Activates on first non-sync character following one or two successive sync characters, or immediately upon detecting one or two successive sync characters.

Environmental
Temperature
+50° to +110° F
Humidity
0 – 90%, non-condensing

Power Requirements
Basic Unit
+5 V at 6.0 A
+15 V at .04 A
-15 V at .07 A
Expander Unit
Error detection: +5 V at 1.2 A
Character recognition: +5 V at 1.6 A

1.3 PHYSICAL DESCRIPTION AND CONFIGURATIONS

1.3.1 Physical Description

The DQ11 consists of a basic system unit and an optional expander system unit. Each unit consists of a wired backplane assembly, modules and cables and has the same basic physical appearance and dimensions; each measures 10.5 in. X 16.5 in. X 5 in. and weighs approximately 15 pounds.

Each DQ11 system unit can be mounted in a PDP-11/05NC, PDP-11/35, PDP-11/40, PDP-11/45 processor box, or in an H960-type expansion box.

The DQ11 basic unit and the expander unit must be located next to each other; the basic unit must be the first of the two on the Unibus. Cables connect the two system units together.

Each of the two system units presents one load to the PDP-11 Unibus.

1.3.2 Configurations

A brief description of the DQ11 options follows:

DEC No.	Description	Prerequisite
DQ11-DA	Full/half-duplex synchronous line module set. EIA/CCITT termination suitable for direct use with Bell System 201 or equivalent modems. Transmission speeds up to 10,000 baud. Data set control included. Supplied with 7.6 m (25 ft) modem cable.	PDP-11
DQ11-EA	Full/half-duplex synchronous line module set. TTL to Bell System 303 or equivalent modems. Transmission speeds up to 1.0 megabaud. Data set control included. Supplied with 7.6 m (25 ft) modem cable.	PDP-11
DQ11-AB	Cable-connected second system unit (Error Detection Expander), with provisions for error detection of up to 24-bit polynomials for LRC and CRC checking.	DQ11-DA or DQ11-EA
DQ11-BB	Cable-connected second system unit (Character Recognition Expander), with provisions for character recognition and hardware sequence control for protocol handling.	DQ11-AB
DQ11-KA	Internal Crystal Clock specified at baud rate. Standard frequencies are 2.0K, 2.4K, 4.8K, 9.6K and 19.2K.	

1.4 FUNCTIONAL DESCRIPTION

1.4.1 Introduction

The DQ11 functional description is keyed to the simplified block diagram (Figure 1-1) which shows the complete DQ11 at the module level. The major functional areas of each module are discussed along with some operational concepts.

1.4.2 Basic Unit

Exclusive of the Unibus connectors and backplane, the basic unit contains the following modules.

Size	Number	Name
Single	M105	Address Selector
Single	M7821	Interrupt Control
Single	M7815	Data Set Control
Double	M7818	Hard-Wired Character Detection and NPR Control
Hex	M7812	Bus Selectors, Control/Status Registers and Shift Registers
Hex	M7813	Character Count Registers, Bus Address Registers and Shift Register Control

If the basic unit is to be EIA/CCITT compatible (DQ11-DA), it uses a DF11-A Level Converter; if the basic unit is to be current mode compatible (DQ11-EA), it uses a DF11-G Level Converter.

The major functional areas of each module are discussed below.

M105 Address Selector

This standard module contains jumpers that are configured to respond to the device address assigned to the DQ11. It decodes Unibus address lines A(17:00) and control lines C(01:00) to pick a specific DQ register and to indicate the bus transaction (DATI, DATO, DATOB) to be performed. The four DQ11 addresses are:

Address	Register
76XXX0	RX Control and Status
76XXX2	TX Control and Status
76XXX4	REG/ERR Control and Status
76XXX6	Used with bits 8–11 of the REG/ERR register to select 16 secondary registers

M7821 Interrupt Control

This module contains two control sections: section A controls nonprocessor requests (NPRs) and section B controls bus requests (BRs).

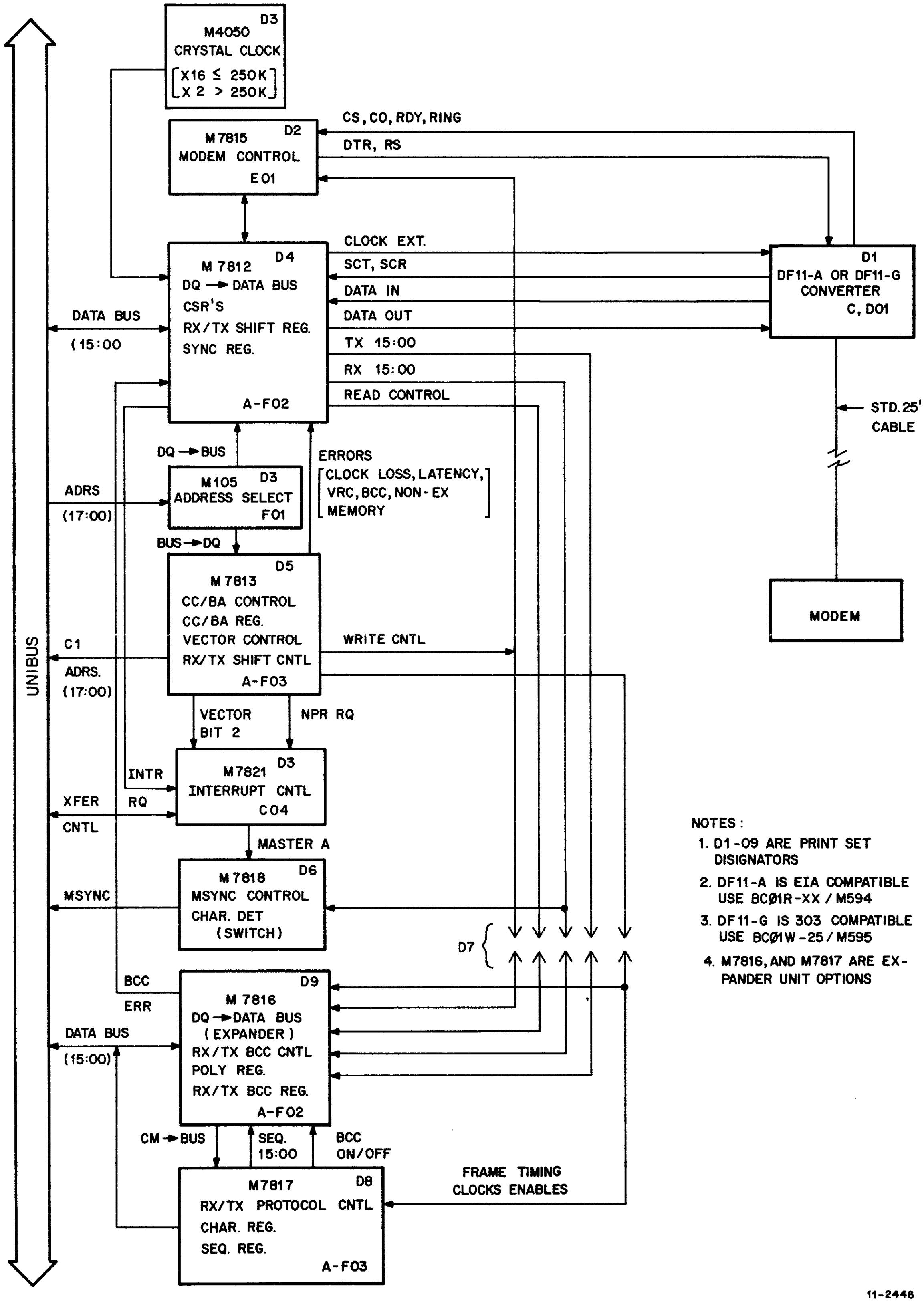


Figure 1-1 DQ11 Simplified Block Diagram

NPRs are requested when a receive or transmit data transfer is required, that is, when a received character is sent to the PDP-11 memory or a character to be transmitted is obtained from the PDP-11 memory.

BRs are requested when certain conditions are indicated by flags in the DQ11. Two vector addresses are generated by the M7821; however, both are level BR5. Receive interrupts generate a vector address of the form XX0 and transmit interrupts generate a vector address of the form XX4.

M7815 Data Set Control
This module generates two control signals to the data set: Data Terminal Ready (DTR) and Request to Send (RS). DTR is bit 9 of the TX Control and Status Register; RS is bit 8 of the same register. In addition, four data set leads are monitored: Carrier Detect (CO), Clear to Send (CS), Ring Indicator (RING) and Data Set Ready (DSR).

Circuits are provided to allow changes in the status of CO, CS, RING and three-user assigned signals to request a data set interrupt if the appropriate interrupt enable bit is set. Data set interrupts generate a vector address of the form XX4.

CS, CO and RING are TX CSR bits 13, 12 and 11, respectively. The data set interrupt enable signal is TX CSR bit 4. The data set interrupt flag is TX CSR bit 15. User option signals UO14 and UO13 are RX CSR bits 14 and 13, respectively.

M7818 Wired Character Detection and NPR Control Logic
This module contains two functionally separate logic circuits: the hard-wired character detection logic and the NPR control logic.

The character detection logic provides three switch-selectable control characters. Maximum character length is 16 bits. Switches are provided to enable the characters, by bytes, to accommodate single- or double-character operation. The character to be detected is set into the detector bit switches and the associated enabling switch is closed. When the received character matches the switch-selectable character, a flag is asserted which is sent to the bus selector logic on the M7812 module where it can be read. Another switch is provided that allows the detected character to request an interrupt.

The NPR control logic allows the DQ11 to become bus master and perform a DATI or DATO bus transaction to the PDP-11 memory. The DQ11 takes a character from memory (DATI) for transmission or it sends a received character to memory (DATO) for storage. This logic also generates the load signal for the transmitter buffer register if a transmit operation requested the NPR.

M7812 Bus Selectors, Control/Status Registers and Shift Registers
This module contains 8 functional circuits:

Bus Selectors and Control Logic
The outputs of 8 registers in the basic DQ11 are multiplexed to the Unibus data lines through one set of 16 bus drivers. The registers are:

Receiver Control and Status (RX CSR)
Transmitter Control and Status (TX CSR)
Register Pointer/Error (REG/ERR)
Received Data Register (RX RD)
Transmitter Buffer (TX BUF)
Miscellaneous (MISC)
Synchronous (SYNC)
Character Count/Bus Address (CC/BA)

Refer to Chapter 3 for a discussion of the bit assignments for these registers. Decoding logic enables the multiplexers and selects the desired registers.

Miscellaneous (MISC) Register and Internal Clock
The internal clock and MISC register are discussed together because several bits of the register are related to operation of the clock or its output logic during servicing.

Five bits (4, 5, 12, 13 and 14) of the MISC register are located on the M7813 module. The 11 bits on this module are program-controlled.

The internal RC clock supplies a 14 Kbaud signal to the external clock line. This clock could be used as the transmit clock. Usually, the transmit clock is supplied by the modem or by the optional crystal controlled clock (M4050) which can be installed in the DQ11. The receive clock is always supplied by the modem with the incoming characters.

If the external receive or transmit clock is lost, the RC clock takes over and completes shifting the character into the RX or TX shift register before the receiver or transmitter is shut down by the clock loss circuit on the M7813 module. The last character is not valid.

Transmit Control and Status Register (TX CSR)
Six bits of the TX CSR are located on this module: 0, 1, 3, and 5–7. Bit 14 is not assigned (user option) and is available on the backplane as a TTL connection. Bit 2 is located on the M7813 module. Bits 4, 8, 9, and 15 are located on the M7815 module. Bits 10–13 are signals to or from the data set and are picked off the DF11 level converter.

Receiver Control and Status Register (RX CSR)
Eight bits of the RX CSR are located on this module: 0, 1, 3, 4–7 and 15. Bits 2 and 12 are located on the M7813 module. Bits 8–11 are located on the M7818 module and bits 13 and 14 are located on the M7815 module.

Register Pointer and Error Register (REG/ERR)
All bits except one (bit 12) are located on this module. Bit 12 is located on the M7813 module.

Sync Register (SYNC) and Transmitter Data Output Logic
The desired sync character is loaded into the SYNC register (16 bits maximum). The output of the SYNC register is compared with the output of the receiver buffer register which contains the received sync word. If they match, a signal is sent to the hard-wired character detection logic (M7818) to set a flag and to initiate an interrupt request if RX ACTIVE and CHAR INTR ENABLE bits are set.

The serialized output of the SYNC register, transmitter data register, transmitter BCC generator and VRC circuit are ORed to become the serial data out to the data set.

Transmitter Shift Register
The transmitter shift register consists of an input buffer, shift holding register and an output data selector. Data to be transmitted is brought from the PDP-11 memory and loaded, in parallel, into the buffer. It goes from the buffer to the shift holding register to the output data selector where it is serialized starting with the LSB.

Receiver Shift Register
The receiver shift register consists of a shift register and two buffer registers. In addition, the receiver data decoder enters the serial received data into the correct bit position of the shift register. This is required because the character length is selectable. The output (second) buffer places the data, in parallel, on the Unibus data lines.

M7813 Character Count Registers, Bus Address Registers and Shift Register Control
This module contains 7 functional circuits:

Character Count/Bus Address Register
The Character Count/Bus Address Register (CC/BA) actually consists of eight registers:

Receiver	**Transmitter**
Primary BA	Primary BA
Secondary BA	Secondary BA
Primary CC	Primary CC
Secondary CC	Secondary CC

These registers are 16 bits long and are contained in a read/write memory on the module. The BA registers are expandable to 18 bits to allow addressing PDP-11 memories that contain more than 32K words.

The BA register is loaded with the address of the first character to be transmitted (from memory to DQ11) or the address of the first received character (sent to memory from DQ11). The BA register is automatically incremented during each data transfer which selects consecutive memory addresses.

One or both CC registers are loaded with the 2's complement of the number of characters to be transferred. The first one is incremented toward overflow, which it reaches when the desired number of characters have been transferred. If more characters are to be processed, the associated CC register is activated and the sequence continues; if the associated CC register shows a zero count, the transfers stop. The output of the CC/BA register is sent to the bus selector circuit on the M7812 module where it can be read.

Character Count/Bus Address Control Logic
This logic controls the updating of the CC/BA register during an NPR cycle. Normally, it loads and increments the CC register, loads and increments the BA register, then shuts down until it is started again during the next NPR cycle.

When the logic detects the last character to be processed, it looks at the associated CC register (primary or secondary) to see if it contains a character count. If it does not, there are no more characters to be processed. If it contains a character count, these additional characters are processed starting with the next NPR cycle.

A section of this logic responds to the NPR request signals from the transmit control logic and the receive control logic. It generates signals that are used in the NPR control logic on the M7818 module.

Clock Loss, Register Select, and Done Control Logic
The clock loss circuit generates a flag if either the receive or transmit flag is lost during operation. This logic also turns on the internal RC clock which continues the shifting operation until the sequence is ended normally at the end of the NPR cycle. Under these conditions, the last character is not valid.

The register select logic decodes signal from the M105 Address Module and generates control signals for the CC/BA internal memories, MISC register, SYNC register, and the REG/ERR register.

The DONE control logic generates signals that clear the RX GO and TX GO bits and set the RX and TX primary/secondary register DONE bits. It also provides addressing signals for the CC/BA registers.

Interrupt and Vector Control Logic
This logic is the controlling link between the interrupt requesting logic in the DQ11 and the M7821 Interrupt Module that actually requests the interrupt.

As part of its controlling function, it sends a signal to the M7821 that determines which vector address is asserted: vector A (XX0) or vector B (XX4).

Transmitter Control Logic
This logic is divided into several functional areas which are described as follows:

Transmit Bit Counter – The counter is loaded with the 2's complement of the number of bits per character selected by the program. Its outputs are select signals that control the parallel-to-serial conversion of data in the TX shift register.

Send Enable Circuit – Controls the priority of information to be transmitted. The priority, in descending order, is: DLE, BCC, SYNC, Data, and PAD.

SYNC/Data Enable Circuit – Provides enabling signals for the SYNC and TX data registers.

Character Count Logic – Provides byte control of the TX data register to accommodate single- and double-character operation.

Save Sync Logic – Allows the SYNC register to be enabled and disabled so that idle characters can be transmitted.

Vertical Redundancy Checking (VRC) – When selected, the VRC logic examines the data to be transmitted and puts a MARK (logical 1) in the MSB position of each character if required to make the total number of MARKs, including the VRC bit, even or odd as selected.

Fake End Logic – In the double-character mode (≤ 8 bits per character) with an odd count, only one byte of the last word contains a character to be transmitted. This logic allows the other byte to be ignored and fakes the end of the current transmission. This permits the next NPR to start sooner.

Data Sync/NPR Logic – At the start of transmission, this logic generates a data enable and synchronizes the loading of the TX shift register. It also generates an NPR request after data is moved from the TX buffer to the TX shift register.

Receiver Start Up and VRC Logic
In the receive mode, the start-up logic searches for sync characters and, when the correct pattern is detected, it asserts RX ACTIVE which indicates that the receiver is in the data transfer mode. Framing (synchronization) can be selected to occur on one or two sync characters. RX ACTIVE can be selected for assertion when framing occurs or on the first non-sync character after framing.

The VRC logic, when enabled, checks the received character for correct parity. Odd or even parity can be selected. If incorrect parity is detected, the RX VRC error flag is asserted.

Receiver Control Logic
This logic counts a character as being received or not. It responds to single- and double-character operation. Further discrimination is made between odd and even character counts. When this logic determines that the received character is what was expected (single or double, odd or even count) an NPR request is generated, the character is sent to the receiver buffer, and the receive character control logic is prepared for the next count.

1.4.3 Expander Unit

Exclusive of the backplane, Unibus connectors and interconnecting cables, the expander unit can contain two options. Each one is contained on a hex module as shown below:

Module No.	Option Designation	Name
M7816	DQ11-AB	AB Selectors and BCC Control
M7817	DQ11-BB	Character Detection and Sequence Control

The major functional areas of these modules are discussed below.

M7816 AB Selectors and BCC Control Logic

This module contains 6 functional circuits:

Bus Selectors and Decoding Logic

The outputs of three registers on this module and one on the M7817 module are multiplexed to the Unibus data lines through one set of 16 bus drivers. The registers are:

Sequence Register (M7817)
Polynomial Register (M7816)
Receive BCC Register (M7816)
Transmit BCC Register (M7816)

The decoding logic generates signals to enable the bus selectors and to select the desired register.

Polynomial Register

This register is a 24-bit read/write register that stores the polynomial used in generating the BCC character during transmission or checking the BCC character during reception.

Receive Block Check Generator

If a message is processed with error detection, the transmitting and receiving stations must use the same error detecting code. The RX BCC generator examines the data and computes a BCC character. It examines the received BCC character and goes to all 0s if the received BCC character agrees with the computed one. This means that the message has been received without error.

If the BCC characters do not agree, one or more errors are present in the message. The RX BCC generator asserts a flag that denotes that an incorrect message has been received. The receiving station should request that the message be retransmitted.

Transmit Block Check Generator

The architecture of the TX BCC generator is very similar to the RX BCC generator. The generator examines the data being transmitted and accumulates a BCC character. This character is appended to the transmitted data.

Transmit BCC Control

This logic is divided into three functional areas:

TX Transparency Control – This circuit allows the transmitter to enter and exit the transparent mode under control of REG/ERR bits 14 (ENTER T) and 13 (EXIT T). This is a function of the M7816 module only and is called *total transparency* to differentiate it from transparent text which is what the transparent mode is called when it is controlled by the M7817 module.

TX BCC Counter and BCC Request – Jumpers on this module qualify the TX BCC counter to allow appending of 1, 2, or 3 BCC characters. If the M7817 module is installed, it provides control signals to qualify the counter.

TX BCC Shift and Clear – This logic generates the pulses that shift the TX BCC generator. It also provides a signal to clear the generator.

Receive BCC Control

This logic is divided into four functional areas:

RX P and RX S Save – This logic looks ahead to see if the receiver is going to enter the total transparency mode. If it is, the logic allows total transparency to be turned on one transfer time sooner.

RX Transparency Control and BCC Counter – This logic allows the receiver to enter and exit total transparency under control of REG/ERR bits 14 (ENTER T) and 13 (EXIT T). When the receiver enters total transparency, this logic sends a signal to the RX BCC turn-on circuit that starts the RX BCC generator. When the receiver exits total transparency, this logic enables the RX BCC counter and allows reception of the selected number of BCC characters before turning off the RX BCC generator.

RX BCC Turn-On – This logic generates pulses that shift the RX BCC generator.

Test RX BCC – This logic responds to a signal from the RX BCC generator after the data and BCC characters have been received. If an erroneous message has been received, the logic asserts a BCC error flag.

M7817 Character Detection and Sequence Control

This module contains six functional circuits:

Character Detect and Sequence Registers

The character detect and seqeunce registers are 16-word-by-16-bit random access semiconductor (TTL) memories that provide non-destructive readout.

With character recognition enabled, characters to be detected are written into the character detect memory by the program. The desired functions to be performed by the hardware are selected by setting the appropriate bits in the corresponding word of the sequence register.

The output of the receiver buffer register and the output of the transmitter shift hold register are compared with each word of the character detect memory in succession.

When a received character (in RX buffer register) or a character to be transmitted (in TX shift hold register) matches any character in the character detect memory, a hardware control sequence is initiated in accordance with the bits set in the sequence register for the associated word.

Transmit and Receive Compare Logic

Each received character, and character to be transmitted, is compared with each word in the character detect memory. When character detection is enabled, only characters of 8 bits or less can be processed. In the receive mode, two comparisons are made; high byte and word. In the transmit mode, four comparisons are made; high byte, low byte, word and saved word.

Character Detect Control Logic

In response to each received character, and each character to be transmitted, this logic causes the character detect register to step through all 16 words, starting at word 0 and ending at word 15. At each step, the character detect memory word is compared with the character being processed and a match signal is generated if they agree. This match signal, along with other qualifying signals, generates an RX or TX strobe signal that is used in other logic to initiate a hardware control function determined by the status of the bits in the sequence register for the corresponding word.

Setting bit 12 or 13 of the sequence register allows the received character that caused the match to set the character flag bit (RX CSR bit 15). The address of the detected character is also stored in the character detect store register and can be read by the program.

Sequence Decoding Logic

This logic examines the outputs of the sequence register to generate control signals that are used to implement hardware operations. The basic enabling signals for this logic are the RX and TX strobe signals.

Transmitter Protocol Control Logic

This logic is divided into five functional areas:

DLE Logic – Stores the representation of a DLE character that is placed in the character detect memory. It allows fast access to a DLE when adding a DLE in the transmit mode or stripping the DLE in the receive mode.

BCC Exclude Logic – Allows exclusion of a received character or character to be transmitted from the BCC accumulation when not in the transparent text mode. Sequence register bit 11 (RX/TX BCC EXCLUDE) controls this function.

PAD Logic – Allows insertion of a PAD character following the last character to be transmitted. A jumper allows selection of one or two PAD characters.

TX Transparency Control Logic – Allows entry into transparent text on the next character to be transmitted or on the one following.

TX BCC Control Logic – Excludes the first TX BCC start-up control character from the BCC accumulation. The next TX BCC start-up control character within this message is included in the BCC accumulation.

Receiver Protocol Control Logic

This logic is divided into four functional areas as described below.

RX BCC Control Logic – Excludes the first RX BCC start-up control character from the BCC accumulation. The next RX BCC start-up control character within this message is included in the BCC accumulation.

Character Strip Logic – Prevents the detected character from being transferred to the PDP-11 memory but allows it to be included in the RX BCC accumulation. It also allows stripping the DLE, SYNC sequence in the receive transparent text mode.

RX BCC Disabling Logic – Stops the RX BCC generator to exclude a detected character from the BCC accumulation. The categories of characters to be excluded are listed below:

1. All DLE characters
2. A SYNC character following a DLE character
3. SYNC characters following framing in non-transparent operation
4. Any detected character if sequence register bit 11 (RX BCC EXCLUDED) is set

Clear GO/Set DONE Logic – Allows RX GO to be cleared and RX DONE to be set at the end of a transfer only. The circuit is independent of the clearing of RX ACTIVE.

1.4.4 Types of Data Transfers Performed by the DQ11

1.4.4.1 Introduction – The DQ11 performs several types of data transfers, depending on the options selected. The DQ11-DA/EA basic units are expanded by adding the DQ11-AB and DQ11-BB options to provide increased versatility. With the maximum DQ11 configuration (basic plus AB and BB options), the programmer can drop back to the AB option or to the basic unit without hardware changes.

1.4.4.2 Data Transfers – The DQ11 handles typical messages using the representative message control characters; however, its full capabilities are evident during block transfers. Such transfers consist of blocks of pure binary data. Using maximum character counts and high baud rates, a large amount of data is handled in a short time.

The method of handling block transfers for the basic unit and AB/BB options is discussed in the following paragraphs.

Basic Unit (DQ11-DA/EA)
The basic unit handles typical data transfers with or without character recognition and idle control. Transparent block transfers are handled without character recognition and idle control.

DQ11-AB Option
This option allows transparent block transfers with error detection (LRC/CRC). Character recognition is disabled when a transparent block is started and is enabled when the block ends. In this case, character control consists of the three switch-selectable characters in the basic unit. Disabling and enabling character control during transparent operation allows the use of idle control without destroying the integrity of the transparent blocks.

The transparent block starts with the first used character count field provided REG/ERR bit 14 (ENTER T) is set. It ends in any other character count field provided REG/ERR bit 13 (EXIT T) is set. These bits are reset by the hardware.

DQ11-BB Option
This option provides programmable character detection that activates hardware functions that are also programmable. Character detection is for single- or double-characters with a length of 8 bits or less. Block size, character sets and error polynomial configuration are unrestricted.

With this option installed, the programmer can drop back to the AB option or the basic unit without hardware changes. However, character recognition is always software programmable, regardless of the level of hardware under program control because when this option is installed the hard-wired character detection feature is disabled.

The BB option provides the following programmable hardware functions:

Text transparency
BCC control
Protocol start-up and shut-down
Special character interrupts
DLE insertion and deletion

DLE characters are inserted under the following conditions:

a. When a binary character representing a DLE is transmitted during transparent text, the hardware automatically inserts another DLE (called DLE stuffing).

b. When going to an idle condition during transparent text, the hardware inserts the sequence DLE-SYNC, DLE-SYNC, etc.

c. Insertion of DLE characters during transmission requires a program function that allows the hardware to exit the transparent text mode. This is performed through any new character count provided the EXIT T bit is set. When the exit transparent text function is detected, the hardware sends a DLE character preceding the new character count field. The first character from the new character count field must be the control character that ends the block or text (ETX, ETB, ITB, etc.).

1.5 BASIC OPERATING PRINCIPLES

1.5.1 Introduction

The following paragraphs cover some basic operating principles of the DQ11 and its options.

1.5.2 Transmit Operation

After initializing the system, the program must select the desired character length using MISC register bits 11–8. The Transmit Bus Address Register (TX BA) and the Transmit Character Count Register (TX CC) must be selected using REG/ERR register secondary pointer bits 11–8. The TX BA is loaded with the starting address in the PDP-11 memory of the first character to be transmitted. This register is incremented as each character is transferred, which selects consecutive PDP-11 memory addresses.

The TX CC register is loaded with the 2's complement of the number of characters to be transmitted. It is incremented by the CC/BA counter, which at overflow indicates that the character count has been completed.

The SYNC register must be loaded with the sync character to be used during the transmission. The same sync character must be the first character transmitted and the most convenient way to obtain it is by storing it in the PDP-11 memory.

Any required handshaking to establish connection with the data set should be done now. The program can now assert the Transmit GO (TX GO) bit in the TX CSR to start transmission. Data transfers from the PDP-11 memory to the DQ11 are accomplished during NPR cycles (one per NPR).

Characters are transmitted until a TX CC overflow is detected. Control is switched to the associated TX CC if additional characters remain to be transmitted. If no more characters remain to be transmitted, the associated TX CC reads zero. The appropriate TX CC DONE bit in the TX CSR is set and the hardware clears TX GO which shuts off the transmitter.

If the IDLE MODE bit in the TX CSR is set, idle characters are transmitted whenever TX GO is cleared. In the non-transparent mode, the idle character is the contents of the SYNC register. In the transparent text mode (requires BB option), the idle character is the DLE character followed by the contents of the SYNC register in a repetitive sequence (DLE SYNC, DLE SYNC, etc.).

1.5.3 Receive Operation

As in the case of transmit operation, the Receive Bus Address Register (RX BA) and Receive Character Count Register (RX CC) must be loaded. The RX BA register is loaded with the starting address in the PDP-11 memory where the first received character is to be deposited.

The SYNC register is loaded and, after any required handshaking with the data set, the RX GO bit in the RX CSR is set to start the receive operation. The receiver starts accepting data and is prepared by circuit board jumpers to be synchronized (framed) after receiving one or two sync characters. After framing, the RX ACTIVE bit in the RX CSR is set and data transfers are started.

Received characters are transferred to the PDP-11 memory until at RX CC overflow the associated RX CC register indicates a zero count. The appropriate RX CC DONE bit in the RX CSR is set and the hardware clears RX GO which shuts off the receiver.

Clearing RX ACTIVE while RX GO is set forces resynchronization of the receiver.

1.5.4 Error Detection

The DQ11-AB option (M7816 module) provides error detection using Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC). LRC and CRC error detection processes use a polynomial to represent the code that both the sending and receiving stations must use to generate and check the block check character (BCC).

A 24-bit programmable polynomial register (POLY) stores the code that qualifies both the receive and transmit BCC generators.

As one DQ11 transmits data, its TX BCC generator is accumulating a BCC character that is appended to the data. The receiving DQ11 accepts the data and accumulates a BCC character in its RX BCC generator. When it receives the transmitted BCC character, the register in the RX BCC generator should go to all 0s. This indicates that the BCC characters on both ends are identical and that the message has been received without error. An error in the message means that the BCC characters cannot be the same. This results in a remainder (not all 0s) in the RX BCC register. This condition asserts the RX BCC error flag in the REG/ERR register. The proper response to this error flag is to request that the message be retransmitted. As a result of the error flag, the RX BCC register is cleared.

1.5.5 Protocol Handling

The DQ11-BB option (M7817 module) provides effective protocol handling by using programmable character detection to initiate hardware sequences which are also programmable. The features of the DQ11-BB option are discussed in Paragraph 1.4.3.

This option is well suited for handling line protocols, such as IBM's Binary Synchronous (BISYNC) protocol.

The BB option can be used without error detection to provide interrupts upon detecting any of the 16 programmable control characters. In this situation (no error detection), it still provides the hardware control; however, the error detection module (M7816) must be installed.

CHAPTER 2
INSTALLATION

2.1 GENERAL

This chapter provides information for installing and testing a DQ11.

2.2 EQUIPMENT CHECKLIST

After unpacking, check that all parts are present for the DQ11 configuration given in the subsequent paragraphs.

2.2.1 DQ11-DA Configuration

Check that the following modules and assemblies are supplied for the DQ11-DA configuration.

7009467 – Wired Backplane Assembly

M920 – Internal Bus Connector

M105 – Address Selector Module

M7821 – Interrupt Control Module

M7815 – Data Set Control Module

M7818 – Wired Character Detection and NPR Control Logic Module

M7812 – Bus Selectors, Control/Status Registers and Shift Registers Module

M7813 – Character Count Registers, Bus Address Registers and Shift Register Control Module

DF11-A – EIA/CCITT Converter/Cable (M594 and BC01R-XX)

2.2.2 DQ11-EA Configuration

The DQ11-EA configuration has the same parts as the DQ11-DA except that a 301/303 level converter and cable (DF11-G) is substituted for the EIA/CCITT level converter and cable. The DF11-G consists of an M595 Converter Module and a BC01W cable.

2.2.3 DQ11-AB Configuration

Check that the following parts are supplied with the DQ11-AB configuration.

7009468 – Wired Backplane Assembly

M920 – Internal Bus Connector

M7816 – AB Selectors and BCC Control Logic Module

M971 – Cable Connector (6)

BC08S – I/O Cable Assembly (3)

2.2.4 DQ11-BB Configuration

Check that one M7817 Programmable Character Detection and Sequence Control Module is supplied for the DQ11-BB option.

2.2.5 DQ11-KA Configuration

Check that one M4050 Crystal Clock Module is supplied for the DQ11-KA option. The crystal frequency must be 16 times the required baud rate for rates of 250 Kbaud or less. Over 250 Kbaud, the frequency must be two times the baud rate.

2.2.6 Accessories

Check that the following accessories are supplied with each DQ11 configuration.

LIB KIT 11-KQ11A-A-K Software Kit
B-DD-DQ11-0 Customer Print Set
DEC-11-HDQAA-A-D Maintenance Manual

2.3 BASIC UNIT AND EXPANDER UNIT INSTALLATION PROCEDURE

2.3.1 Unit Assembly

A unit assembly drawing (D-UA-DQ11-0-0) is supplied as part of the DQ11 customer print set as an aid to the installation process. To install the DQ11, proceed as follows:

1. Before installing the system unit, install the 7009563 harnesses, being very careful to install the Faston connectors on their respective tabs without catching against or cutting any of the nearby backplane wiring. Proper connections are listed on the backplane etch and their relative positions are shown in drawing C-IA-70094647-0-0 for the Basic Unit and drawing C-IA-70094648-0-0 for the Expander Unit.

2. With all power off, install the DQ11 single- or double-system unit, containing the wired logic, in a convenient spot in the expander box or processor box.

3. Make interconnections between the Basic Unit and Expander Unit (if supplied) as shown in drawing D-UA-DQ11-0-0.

4. Without modules installed, apply power and check supply voltages at the following backplane pins. Adjust if required.

   +5 V on pin C1A2
   -15 V on pin C1B2
   +15 V on pin C1N2

2.3.2 Module Installation

Before installing modules, jumpers on the M105 and M7821 modules must be cut to provide the correct device address and vector address assignments. Refer to Paragraph 2.5 for selecting the device address (M105) and to Paragraph 2.6 for selecting the vector addresses (M7821).

Refer to Paragraph 2.7 for switch/jumper selections for the DQ11 basic and expander units (M7812, M7813, M7815, M7816, M7817 and M7818). The jumper configuration for the DF11 Converter Module and M4050 Crystal Clock Module are also included in this paragraph.

The diagnostics must be run with the switch/jumper selections shown in Paragraph 2.7.1 due to a few configurations that are not supported by diagnostics. The exceptions are shown in Paragraph 2.7.2 along with a description of all switches and jumpers.

Install the modules in their respective slots as shown in drawing D-MU-DQ11-0-1 for the Basic Unit (DQ11-AA) and drawing D-MU-DQ11-0-2 for the Expander Unit (DQ11-AB).

2.4 POWER REQUIREMENTS

Basic Unit
+5 V at 6.0 A
+15 V at 0.04 A
-15 V at 0.07 A

Expander Unit
Error Detection (M7816): +5 V at 1.2 A
Character Recognition (M7817): +5 V at 1.6 A

2.5 DEVICE ADDRESSES

2.5.1 Introduction

Starting with the DJ11, new communications devices are to be assigned floating addresses. The addresses for current production devices are to be retained.

The word *floating* means that addresses are not assigned absolutely for the maximum number of each communications device that can be used in a system.

2.5.2 Floating Device Address Assignment

Floating device addresses are assigned as follows:

1. The floating address space starts at location 760010 and extends to location 764000 (octal designations).

2. The devices are assigned in order by type: DJ11, DH11, DQ11, DU11, and then the next device introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

3. The first address of a new type device must start on a modulo 10_8 boundary, if it contains one to four bus-addressable registers. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 has eight registers.

4. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used, if the device following it is used. The equivalent of a gap should be left after the last device assigned to indicate that nothing follows.

5. No new type devices can be inserted ahead of a device on the list.

6. If additional devices on the list are to be added to a system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required to make room for the additions.

The following examples show typical floating device assignments for communication devices in a system.

Example 1: No DJ11s, 2 DH11s and 2 DQ11s

760010	Cannot be used for DH11 starting address
760020	DH11 #0 first address
760040	DH11 #1 first address
760060	DH11 gap
760070	DQ11 #0 first address
760100	DQ11 #1 first address
760110	Indicates no more DQ11s

Example 2: 1 DJ11, 1 DH11 and 2 DQ11s

760010	DJ11 #0 first address
760020	DJ11 gap
760040	DH11 #0 first address
760060	DH11 gap
760070	DQ11 #0 first address
760100	DQ11 #1 first address
760110	Indicates no more DQ11s

2.5.3 Device Address Selection (M105 Module)

A typical DQ11 address (760070) is represented graphically in Figure 2-1. In the floating address space (760010–764000), bits 13–17 are always 1s (function of PDP-11 processor). Appendix B shows the PDP-11 memory organization and addressing conventions. Bits 3–12 are selected by jumpers on the M105 module. With the jumper in, the decoder looks for a 0 on the associated Unibus address line; conversely, with the jumper out, the decoder looks for a 1 on the associated Unibus address line. Bits 1 and 2 are decoded to select 1 of 4 registers. They determine the least significant digit (octal) of the device address because bit 0 is not used for address decoding and is assumed to be 0.

The DQ11 requires four addresses:

76XXX0	RX Control and Status Register
76XXX2	TX Control and Status Register
76XXX4	REG/ERR Control and Status Register
76XXX6	Used with bits 8–11 of REG/ERR CSR to select 16 secondary registers.

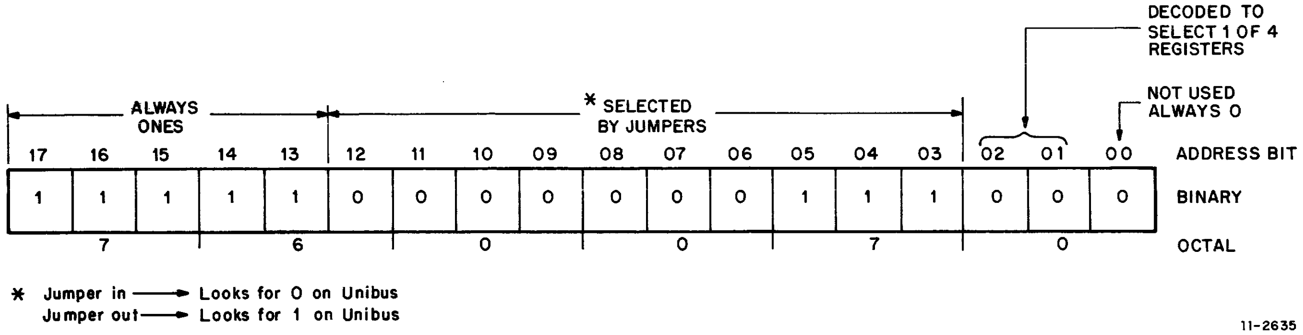


Figure 2-1 Device Address Format

Table 2-1 shows which M105 jumpers to cut for specific device addresses.

Table 2-1
Guide for Cutting M105 Jumpers to Select Device Address

Jumper										Device Address
12	11	10	9	8	7	6	5	4	3	
									X	760010
								X		760020
								X	X	760030
							X			760040
							X		X	760050
								X		760060
							X	X	X	760070
						X				760100
					X					760200
					X	X				760300
				X						760400
				X		X				760500
				X	X					760600
				X	X	X				760700
			X							761000
		X								762000
		X	X							763000
	X									764000

Note: X means remove (cut) jumper (logical 1 on the Unibus)

2.6 VECTOR ADDRESSES

2.6.1 Introduction

Communications devices are assigned floating vector addresses. This eliminates the necessity of assigning addresses absolutely for the maximum number of each device that can be used in the system.

2.6.2 Floating Vector Address Assignment

Floating vector addresses are assigned as follows:

1. The floating address space starts at location 300 and proceeds upward to 777. Addresses 500–534 are reserved.
2. The devices are assigned in order by type: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, D, E; DJ11; DH11; DQ11; DU11.
3. If any type device is not used in a system, address assignments move up to fill the vacancies.
4. If additional devices are to be added to the system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required.

2.6.3 Vector Address Selection (M7821 Module)

Each device interrupt vector requires four address locations (two words) which implies only even-numbered addresses. A further constraint is that all vector addresses must end in 0 or 4. The vector address is specified as a three-digit, binary-coded, octal number using Unibus data bits 0–8. Because the vector must end in 0 or 4, bits 1 and 0 are not specified (they are always 0) and bit 2 determines the least significant octal digit of the vector address (0 or 4). The logic on the M7821 module sends only seven bits (2–8) to the PDP-11 processor to represent the vector address.

The DQ11 is shipped with a BR5 priority selection card installed in the M7813 module. The BR section of the M7821 Interrupt Control Module generates two vector addresses: receiver interrupts generate vector addresses of the form XX0, and transmitter interrupts generate vector addresses of the form XX4. For this method of operation, the bit 2 jumper on the M7821 module must be left installed. The two most significant octal digits of the vector address are determined by jumpers in lines 3–8. With the jumper in, a 1 is generated on the associated Unibus data line; with the jumper out, a 0 is generated on the associated Unibus data line. Also, the NPR jumper on the M7821 module should be left in to improve NPR latency time.

Table 2-2 shows which M7821 jumpers to cut for specific vector addresses.

Table 2-2
Guide for Cutting M7821 Jumpers
to Select Vector Address

Jumper						Vector Address
8	7	6	5	4	3	
X			X	X	X	300
X			X	X		310
X			X		X	320
X			X			330
X				X	X	340
X				X		350
X					X	360
X						370
	X	X	X	X	X	400

	X		X	X	X	500

		X	X	X	X	600

			X	X	X	700

Note: X means remove (cut) jumper (logical 0 on the Unibus)

2.7 BASIC UNIT AND EXPANDER UNIT SWITCH/JUMPER SELECTIONS

2.7.1 Introduction

The DQ11 is shipped with the switches and jumpers in the following configuration:

M7812 Module

S1 SW1 – ON
SW2 – OFF
SW3 – ON only if clock option (KA) is installed and baud rate is ⩽ 250K.
SW4 – ON only if clock option (KA) is installed and baud rate is > 250K.
SW5 – ON only if clock option (KA) is not installed.
SW6 – OFF
SW7 – OFF
SW8 – OFF

M7813 Module

S1 SW1 – ON
SW2 – ON
SW3–SW8 – OFF

M7818 Module

S5 SW33–SW40 – ON, all others OFF

M7816 Module

Jumper W1 – OUT
Jumper W2 – IN
Jumper W3 – OUT

M7817 Module

Jumper W1 – OUT
Jumper W2 – OUT

M4050 Module

Jumper W10 – OUT
Jumpers W1–W9 – Depends on crystal frequency. Refer to M4050 listing in Paragraph 2.7.2

2.7.2 Module Switch/Jumper Selections

After all diagnostics have been run successfully, configure the modules per the customers requirements using the descriptions listed below.

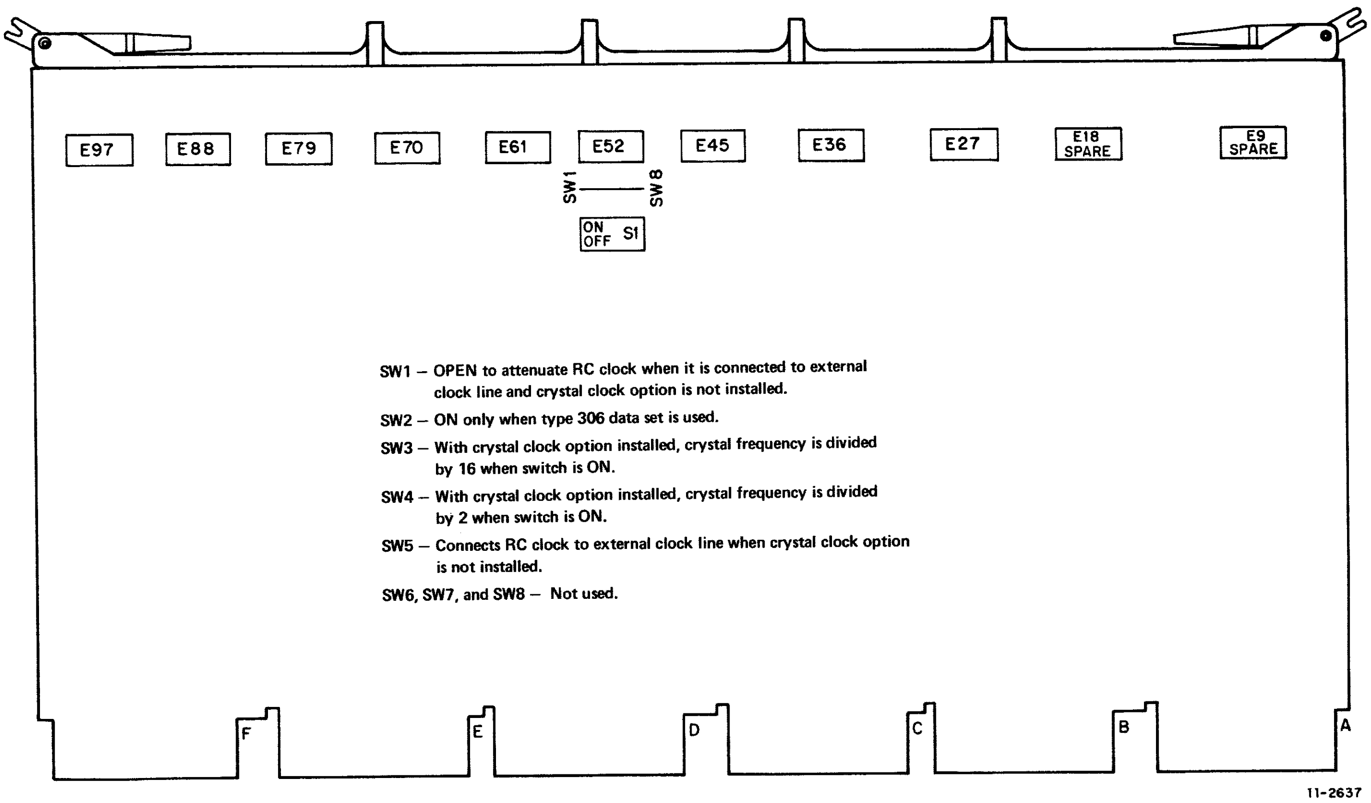
M7812 Module (Figure 2-2)

The operational capabilities of this module are switch-selectable and are described below. All the switches are contained in one dual-in-line package (S1) located between components E51 and E52.

Switch	Description
SW1	Set to ON to run diagnostics DZDQE and DZDQF. Following completion of these diagnostics, SW1 should be set to OFF unless the DQ11-KA option is installed.
SW2	Set to ON only if the DQ is interfaced to a Bell 308 modem (T1 Carrier).
SW3	Set to ON if DQ11-KA is equal to or less than 250 Kbaud (÷16).
SW4	Set to ON if DQ11-KA is greater than 250 Kbaud (÷2).
SW5	Set to ON if DQ11-KA clock is NOT installed. This switch provides a 14 Kbaud RC clock for cable test.

NOTE

If the DQ11-KA crystal clock is installed, it is used for the cable test.



SW1 – OPEN to attenuate RC clock when it is connected to external clock line and crystal clock option is not installed.

SW2 – ON only when type 306 data set is used.

SW3 – With crystal clock option installed, crystal frequency is divided by 16 when switch is ON.

SW4 – With crystal clock option installed, crystal frequency is divided by 2 when switch is ON.

SW5 – Connects RC clock to external clock line when crystal clock option is not installed.

SW6, SW7, and SW8 – Not used.

Figure 2-2 Switch Locations on M7812 Module

M7813 Module (Figure 2-3)

The operational capabilities of this module are switch-selectable and are described below. All the switches are contained in one dual-in-line package (S1) located between components E96 and E97.

Switch	Description
SW1	Set to ON for two sync characters to frame. Set to OFF for one sync character to frame.
SW2	Set to ON for Receive Active on first non-sync character after frame has occurred. Set to OFF for Receive Active when frame occurs.
SW4	Set to ON for even VRC and OFF for odd VRC.

NOTE

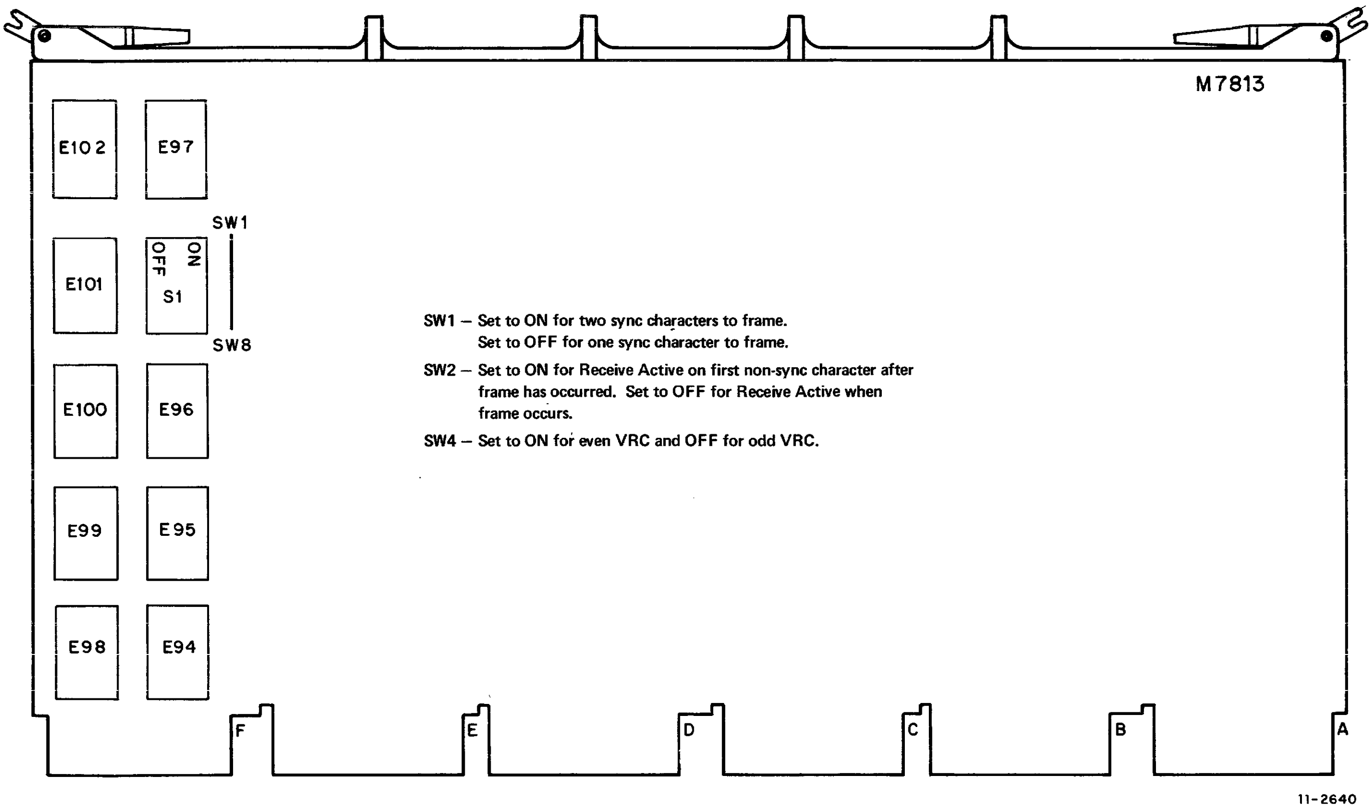
If no customer preference is expressed, set SW1 and SW2 to ON and all other switches to OFF.

M7818 Module (Figure 2-4)

The operational capabilities of this module are switch-selectable. All the switches are contained in seven dual-in-line packages (S1–S7). Refer to print D-CS-M7818-0-1, sheets 1 and 2 for switch locations. Sheet 2 of this print also contains basic rules for using the switches. Refer to Paragraph 4.2 of this manual for a detailed discussion on the use of the switches.

M7815 Module (DQ11-BA)

The operational capabilities of this module are jumper-selectable and are described below. Refer to print D-CS-M7815-0-1, sheet 1 and Figure 2-4 for jumper locations.

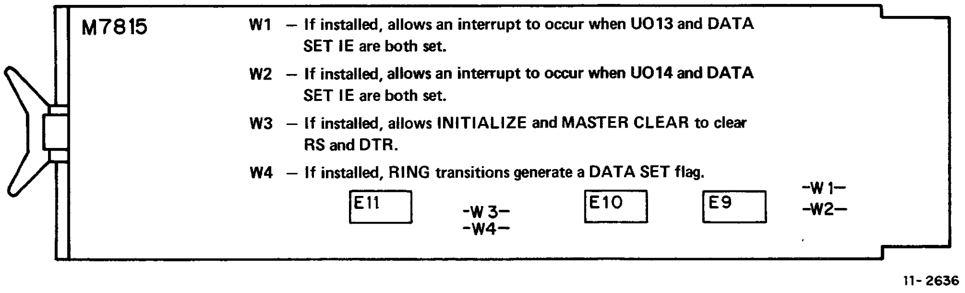


SW1 – Set to ON for two sync characters to frame.
Set to OFF for one sync character to frame.

SW2 – Set to ON for Receive Active on first non-sync character after frame has occurred. Set to OFF for Receive Active when frame occurs.

SW4 – Set to ON for even VRC and OFF for odd VRC.

Figure 2-3 Switch Locations on M7813 Module



W1 – If installed, allows an interrupt to occur when UO13 and DATA SET IE are both set.

W2 – If installed, allows an interrupt to occur when UO14 and DATA SET IE are both set.

W3 – If installed, allows INITIALIZE and MASTER CLEAR to clear RS and DTR.

W4 – If installed, RING transitions generate a DATA SET flag.

Figure 2-4 Jumper Locations on M7815 Module

Jumper	Description
W1	If installed, allows an interrupt to occur when UO13 and DATA SET IE are both set.
W2	If installed, allows an interrupt to occur when UO14 and DATA SET IE are both set.
W3	If installed, allows INITIALIZE and MASTER CLEAR to clear RS and DTR.
W4	If installed, RING transitions generate a DATA SET flag.

NOTE

DQ11 is shipped with all jumpers in, which is the normal configuration. Removal of jumpers W3 and W4 is not supported by diagnostics.

M7816 Module (DQ11-AB)

This module uses jumpers (W1, W2) to select the number of BCCs to be tested (receive) or appended (transmit) when used for block transfers with the error detection feature. (See Figure 2-5 for jumper locations.) The jumper configuration for the number of BCCs selected is as follows:

W1	W2	BCCs ≤8 bits/char.	BCCs >8 bits/char.
IN	OUT	3	2
OUT	IN	2	1
OUT	OUT	1	–

When the third jumper (W3) is installed, the start BCC (RX) control character is included in the BCC. Installation of jumper W3 is not supported by diagnostics. This jumper is used with the DQ11-BB option only.

M7817 Module (DQ11-BB)

The M7817 module has two jumpers that can be used for the following purposes. (See Figure 2-6 for jumper locations.)

Jumper	Description
W1	If installed, selects two pad characters (all 1s) when SEQ 10 is used.
W2	If installed, the start BCC (TX) control character is included in the BCC.

NOTE

Jumpers W1 and W2 installed is not supported by diagnostics.

M4050 Module (DQ11-KA)

The frequency value of the crystal installed in this module determines the configuration of the jumpers. Note that jumper W10 must always be removed.

Crystal Frequency	Jumpers Removed*
5–38 kHz	W9
38–500 kHz	W7, W8
500 kHz–1 MHz	W1, W2, W7, W8
1–5 MHz	W1, W2, W3, W4, W7, W8

*W10 always removed.

DF11 Cable Module

Remove all jumpers except the two labeled 202 and the two labeled 301 when using a Bell 201, Bell 208, Bell 303 or equivalent modem. Remove all jumpers except the two labeled 202 when using a Bell 301 modem or equivalent.

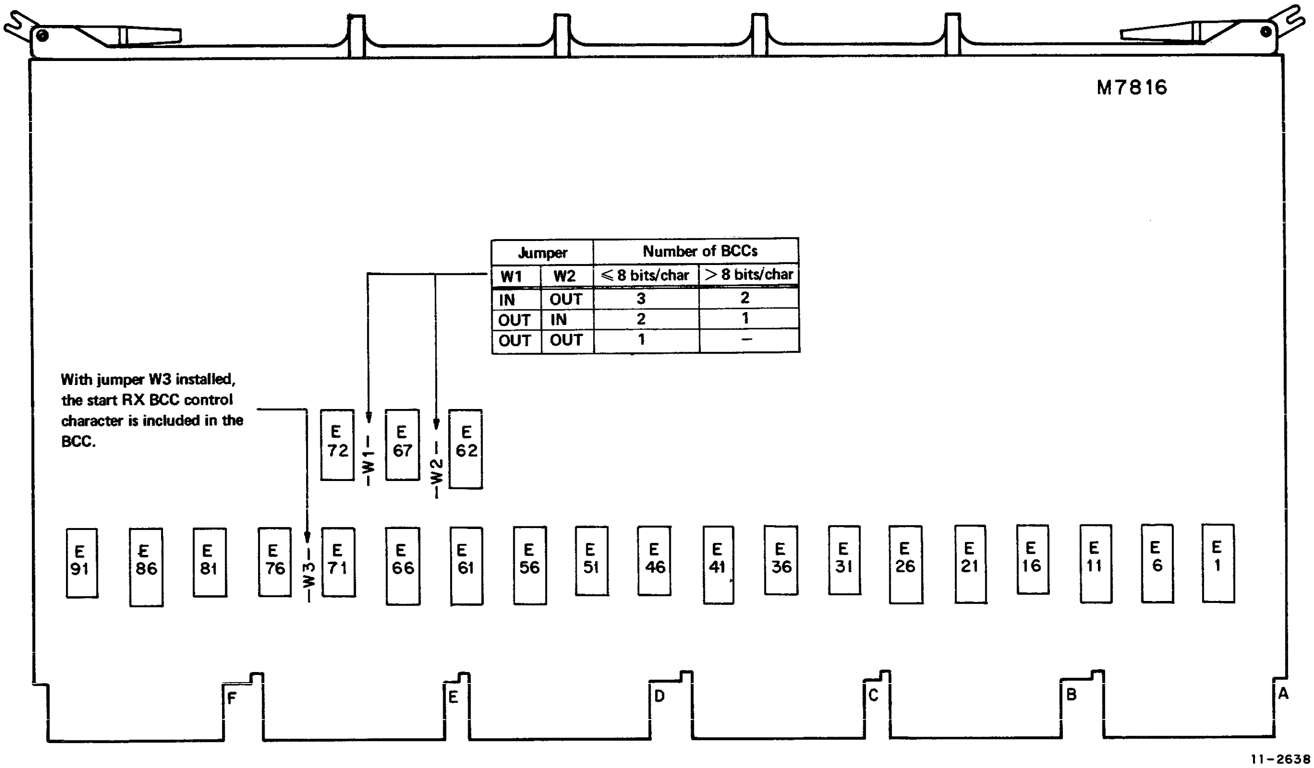
2.8 HARDWARE VERIFICATION

2.8.1 Diagnostics

Diagnostics DZDQ-A through -F should all be run with iterations for a minimum of one pass without errors. Switch/jumper configuration should be as described in Paragraph 2.7.1.

2.8.2 System Exerciser

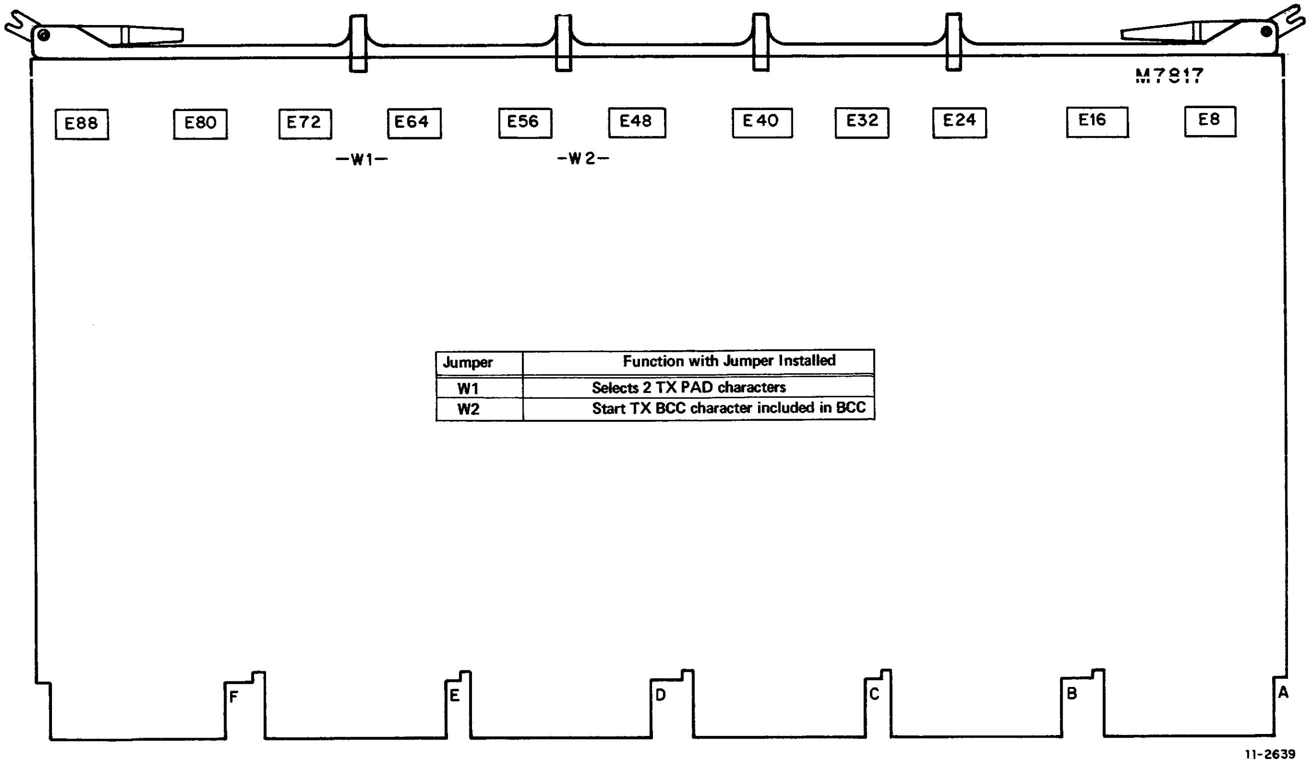
System exerciser DEC/X11 should be run without error to verify that the system and the DQ11 are ready for operation.



Jumper		Number of BCCs	
W1	W2	≤ 8 bits/char	> 8 bits/char
IN	OUT	3	2
OUT	IN	2	1
OUT	OUT	1	–

With jumper W3 installed, the start RX BCC control character is included in the BCC.

Figure 2-5 Jumper Locations on M7816 Module



Jumper	Function with Jumper Installed
W1	Selects 2 TX PAD characters
W2	Start TX BCC character included in BCC

Figure 2-6 Jumper Locations on M7817 Module

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter contains general DQ11 programming information. It is divided into two sections: one lists the register bit functions and the other discusses programming procedures.

3.2 DQ11 REGISTERS AND DEVICE ADDRESS SELECTION

The DQ11 employs address selection logic to detect one of four addresses. The first three addresses are used to select primary registers as shown below:

Address	Primary Register
76XXX0	Receive Status Register (RX CSR)
76XXX2	Transmit Status Register (TX CSR)
76XXX4	REG/ERR Register

The fourth address (76XXX6) is used in conjunction with the secondary register pointer bits (8–11) of the REG/ERR register. Selection of a secondary register requires two DATO transactions. The first one, using 76XXX4, addresses the REG/ERR register and sets bits 8–11 to point to the desired secondary register. The second one, using 76XXX6, enables decoding logic in the hardware that uses bits 8–11 to address the selected secondary register. A list of the 16 secondary registers is shown below:

Octal No.	Register
0	Receive Bus Address (Rx BA) – Primary
1	Receive Character Count (Rx CC) – Primary
2	Transmit Bus Address (Tx BA) – Primary
3	Transmit Character Count (Tx CC) – Primary
4	Receive Bus Address (Rx BA) – Secondary
5	Receive Character Count (Rx CC) – Secondary
6	Transmit Bus Address (Tx BA) – Secondary
7	Transmit Character Count (Tx CC) – Secondary
10	Character Detect (CHAR DET)
11	SYNC
12	Miscellaneous (MISC)
13	Transmit Buffer (Tx BUF)
14	Sequence (SEQ)
15	Receive Block Check Character (Rx BCC)
16	Transmit Block Check Character (Tx BCC)
17	Receive/Transmit Polynomial

Programming Note:

During power-up, the program must clear the following registers and bits:

> Bus address registers (secondary registers 0, 2, 4, and 6) and the related MEM EXT/ENTER T/EXIT T bits (REG/ERR register bits 13 and 14).
>
> Character count registers (secondary registers 1, 3, 5, and 7) and the related MEM EXT/ENTER T/EXIT T bits.
>
> Sequence register (secondary 14) and character detect register (secondary 10) if the DQ11-BB option is installed.

3.3 INTERRUPT VECTORS

The DQ11 generates two vector addresses: receive interrupts generate vector addresses of the form XX0, and transmitter interrupts generate vector addresses of the form XX4. The functions that cause the interrupts are:

Receive Status Register (XX0)
- Receive Done Primary (Rx Done P)
- Receive Done Secondary (Rx Done S)
- Character Flag

Transmit Status Register (XX4)
- Transmit Done Primary (Tx Done P)
- Transmit Done Secondary (Tx Done S)
- Error Flag
- Data Set Flag

3.4 PRIORITY SELECTION

The priority selection for transmit and receive interrupts is selectable on the M7813 module via plug-in priority selection card. The DQ11 is shipped with a priority 5 selection card installed that establishes BR5 as the bus request level for interrupts.

RXCSR
76XXX0
VECTOR A (XX0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CHAR FLAG	USERS OPTION (DATA SET IE)		RX ACTIVE	CHAR DET & ADDRESS				RX DONE P	RX DONE S	RX DONE IE	CHAR IE	HALF DUPLEX	RX P/S	STRIP SYNC	RX GO
R/W	R/W		R/W	READ BUT WRITE ONLY IF RX AND TX NOT ACTIVE				R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

TX CSR
76XXX2
VECTOR B (XX4)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA SET FLAG	USERS OPTION	CS	CO	RING	DSR	DTR	RS	TX DONE P	TX DONE S	TX DONE IE	DATA SET IE	ERR IE	TX P/S ACTIVE	IDLE MODE	TX GO
R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

REG/ERR
76XXX4
VECTOR A AND B

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR INTR	MEMORY EXT ENTER T	EXIT T	14,13 WRITE EN	SECONDARY REGISTER POINTER (SEE NOTE)				VRC ERROR	RX BCC ERROR	RX NON-EX MEM	TX NON-EX MEM	RX LATENCY ERROR	TX LATENCY ERROR	RX CLOCK LOSS	TX CLOCK LOSS
R	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MISC

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VRC	TX ACTIVE	SYNC1	SYNC 2	BITS/CHARACTER				SEND DATA	POLY 16-23	MASTER CLEAR	RX NPR	TEST LOOP		STEP MODE	SHIFT CLOCK
R/W	R	R	R	R/W				R/W	R/W	W(1s) R(0)	W(1s) R(0)	R/W	NOT USED	R/W	R/W

SEQ
ALL BITS R/W

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CHAR MATCH SINGLE HB	DOUBLE LB&HB	RX CHAR FLAG SINGLE MATCH	DOUBLE MATCH	RX BCC EXCLUDE	TX PAD	DLE STRIP/ADD	RX CHAR STRIP	RX/TX CLR GO/SET DONE	CLR RX ACTIVE	BCC TEST/APPEND		BCC CLEAR/START	CLR RX TRANS	SET RX/TX TRANS	
															NOT USED

CHAR DET (R/W)
SYNC (R/W), TX BUF (R)
TX/RX DATA (NPR)

15–08	07–00
DOUBLE OR SINGLE CHARACTERS (8 BITS OR LESS) RIGHT JUSTIFIED →	DOUBLE CHARACTERS (8 BITS OR LESS) RIGHT JUSTIFIED →
(UNUSED BITS MUST BE ZEROS) SINGLE CHARACTERS (9-16 BITS) RIGHT JUSTIFIED →	

TX/RX BCC
ALL BITS READ ONLY

15–00
UP TO 16 BITS RIGHT JUSTIFIED → EXPANDABLE TO 24 BITS

TX/RX CC (R/W)
TX/RX BA (R/W)
POLY (R/W)

15–00
BA REGISTERS EXPANDABLE TO 18 BITS POLY REGISTER EXPANDABLE TO 24 BITS 16 BITS RIGHT JUSTIFIED →

NOTE:

Secondary registers addressed by using 76XXX6 and REG/ERR bits 11–8 to specify octal designation.

Octal	Secondary Registers
0	Receive Bus Address (RxBA) – Primary
1	Receive Character Count (RxCC) – Primary
2	Transmit Bus Address (TxBA) – Primary
3	Transmit Character Count (TxCC) – Primary
4	Receive Bus Address (RxBA) – Secondary
5	Receive Character Count (RxCC) – Secondary
6	Transmit Bus Address (TxBA) – Secondary
7	Transmit Character Count (TxCC) – Secondary
10	Character Detect (CHAR DET)
11	Sync
12	Miscellaneous (MISC)
13	Transmit Buffer (TxBUF)
14	Sequence (SEQ)
15	Receive Block Check Character (RxBCC)
16	Transmit Block Check Character (TxBCC)
17	Receive/Transmit Polynomial

11-2665

Figure 3-1 DQ11 Register Configurations and Bit Assignments

3.5 REGISTER BIT ASSIGNMENTS

The register bit assignments for the DQ11 are shown in Figure 3-1. A detailed discussion of each register is given in the following paragraphs.

3.5.1 Receive Status Register (Rx CSR)

The receive status register is a word/byte addressable register. The register format is shown in Figure 3-2.

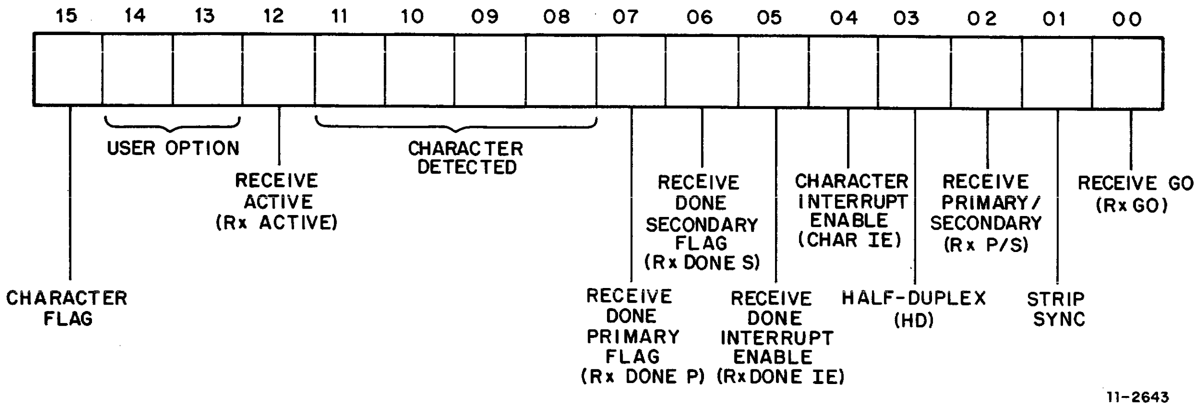

15
14
13
12
11
10
09
08
07
06
05
04
03
02
01
00
USER OPTION
CHARACTER DETECTED
RECEIVE ACTIVE (Rx ACTIVE)
RECEIVE DONE SECONDARY FLAG (Rx DONE S)
CHARACTER INTERRUPT ENABLE (CHAR IE)
RECEIVE PRIMARY/ SECONDARY (Rx P/S)
RECEIVE GO (Rx GO)
CHARACTER FLAG
RECEIVE DONE PRIMARY FLAG (Rx DONE P)
RECEIVE DONE INTERRUPT ENABLE (RxDONE IE)
HALF-DUPLEX (HD)
STRIP SYNC
11-2643

Figure 3-2 Receive Control and Status Register Format

Bit	Function	Description
00	RECEIVE GO (RX GO)	When set, this bit enables receiver data transfers (NPRs) and framing. When cleared, receiver data transfers are inhibited from being set by the hardware. This bit is read/write and is cleared by: 1. Initialize 2. Master Clear 3. The DQ11-BB Character Recognition option (bit 7 of the Sequence register) 4. If Rx Clock Loss, Rx Latency, or Rx Non-Existent Memory are set 5. If the Character Count (CC) goes to zero (primary and secondary registers) Notes: Refer to bit 02 for CC information. Clearing RX GO also clears Receive Active.
01	STRIP SYNC	When this bit is set, all sync characters following Receive Active are stripped from the incoming serial data. In transparent text and in total transparency, the Strip Sync function is inhibited. In transparent text, all DLE-SYNC combinations are stripped if this bit is set. This bit is read/write and is cleared by Initialize and Master Clear.
02	RECEIVE PRIMARY/ SECONDARY (Rx P/S)	Indicates which of the Bus Address (BA) and Character Count (CC) registers is being used. A zero indicates that the primary registers are active. If a transfer is prematurely ended (i.e., the CC did not increment to zero, as in negating GO, or by a transfer-ending flag, or by bit 7 of the Sequence register), the Rx P/S bit does not flip to the next CC or BA register.

Bit	Function	Description
02 (Cont)		This bit is read only and is cleared (set to primary register) by Initialize and Master Clear.
03	HALF-DUPLEX	The setting of this bit indicates that the DQ11 is in the half-duplex mode. When set, the receiver is inhibited when Transmit Active is asserted. This bit is read/write and is cleared by Initialize and Master Clear.
04	CHARACTER INTERRUPT ENABLE (CHAR IE)	When set, this bit allows the Character Detect Flag to generate a program interrupt on Vector A (XX0). For a double-character (≤8 bits/char) transfer, the character that caused the interrupt may not be transferred to memory until one character time later. This bit is read/write and is cleared by Initialize and Master Clear.
05	RECEIVER DONE INTERRUPT ENABLE (Rx DONE IE)	If set, this bit allows interrupts to occur on Vector A (XX0), if Rx DONE P or S is set. This bit is read/write and is cleared by Initialize and Master Clear.
06–07	RECEIVE DONE PRIMARY/ SECONDARY FLAGS (Rx DONE P/S)	These flags are set when their respective character counts (P or S) overflow. These bits are also set by the DQ11-BB Character Recognition option (bit 7 of the Sequence register). Rx Done S is bit 6.
06–07 (Cont)		These bits are read/write and are cleared by Initialize and Master Clear. Note: If Rx DONE is set by the Sequence register, RX P/S (bit 2) does not change state.
08–11	CHARACTER DETECTED (CHAR DET)	These four bits are used to latch the character address which caused a character flag. They represent the switch-selected character flags in the DQ11 Basic Unit. If the Character Recognition option (DQ11-BB) is installed, these four bits reflect the binary address of the character detected at Character Flag time. Character recognition is inhibited if in total transparency mode. Refer to bit 14 of the REG/ERR register for this function. *Basic Unit Only* When applied to the DQ11 Basic System Unit only, bits 8, 9, and 10 represent switch-selected control characters 0, 1, and 2, respectively. Rules for setting the switches are as follows: Switches relating to the High Byte (HB) should be used for detecting characters less than or equal to eight data bits.

Bit	Function	Description
08–11 (Cont)	CHARACTER DETECTED (CHAR DET)	High- and Low-Byte (LB) switches are used for detecting characters with more than eight bits or double characters. All unused bits must be set to zero. If less than three control characters are required, then one or two character switch groups should be set for the same character. For example, if only one control character is needed, all three switch groups must be set for the same character. Bit 11 is connected to the Sync Detection Logic; with switch selection, detection of a sync character causes a Character Detected flag. *Character Recognition and Hardware Sequence Control (Expander Unit)* With the DQ11-BB Character Recognition option installed, bits 8, 9, 10, and 11 contain the binary address (0–17_8) of the character detected (latched) at CHARACTER DETECT Flag time. Refer to description of bits 12 and 13 of the Sequence register. The binary address of the character detected is guaranteed for one character time; i.e., $\frac{\text{Bits/character}}{\text{Baud rate}} = \text{(Seconds)}$ With this option installed, the character address bits 11–8 may be written, if both Transmit Active and Receive Active are not asserted. Any of the 16 characters to be detected can be addressed.
08–11 (Cont)	CHARACTER DETECTED (CHAR DET)	Access is via address 76XXX6 with the REG/ERR register pointer bits (11–8) set to 10_8. The procedure for reading and writing these 16 bits is: 1. Set the REG/ERR register pointer (bits 11–08) to CHARACTER DETECT (octal 10). 2. Write the character address into Receive Status register CHARACTER DETECTED bits 11–8. 3. Read and/or write the character with select 6. Select 6 (76XXX6) is used to access the 16 secondary registers. Refer to description of bits 08–11 of the REG/ERR register for additional information. 4. Repeat steps 2 and 3 until all required characters are accessed. These bits are read/write, if Receive Active or Transmit Active is not enabled and the DQ11-BB Character Recognition option is installed. Bits 08–11 are cleared by Initialize and Master Clear.
12	RECEIVE ACTIVE (Rx ACTIVE)	The setting of this bit indicates that the receiver is now synchronized and in the data transfer mode. The hardware becomes synchronized (S1 and S2 are true) with the incoming data when it recognizes one or two consecutive sync characters (switch option).

Bit	Function	Description
12 (Cont)	RECEIVE ACTIVE (Rx ACTIVE)	At the user's option, the ACTIVE bit can be set at the following times: a. When receiver becomes synchronized. b. On detection of the first non-sync character following synchronization. The conditions for Active to come true are switch-selectable. Clearing Active forces resynchronization if Rx GO is asserted. The normal DQ11 configuration is synchronized on two consecutive sync characters, followed by Rx ACTIVE becoming true on the first non-sync character. This bit is read/write and is cleared by Initialize, Master Clear, bit 6 of the Sequence register, when Rx ACTIVE is cleared and when Rx GO is cleared.
13–14	USER OPTION	These bits are available as part of the DQ11 Data Set control feature. They may be used for generating additional flags or for providing additional modem control. These bits are read/write and are cleared by Initialize and Master Clear.
15	CHARACTER FLAG	The Character Flag bit is set when a character is detected. (Refer to description of bits 8–11.) This bit causes an interrupt if the Character Interrupt Enable bit (bit 4) is set. The CHARACTER FLAG is read/write and is cleared by Initialize and Master Clear.

If the DQ11 is performing double-character transfers ($\leqslant 8$ bits/char), data is shifted in from the MSB of the high byte (HB) toward the LSB of the low byte (LB). The CHARACTER FLAG bit is set when a special character is recognized in the HB position; hence, the special character may not be in memory yet. The special character can either be in the HB position of the previous data transfer (BA register) or in the LB position of the next data transfer.

If the DQ11-BB is not installed and it is required that the special character be in memory at interrupt time, the M7818 module can be set for LB position character recognition; however, diagnostic DZDQ-D will fail the character detection test in this case. At interrupt time, the special character can either be in the LB position of the previous data transfer or in the HB position of the one before that.

3.5.2 Transmit Status Register (Tx STAT)

The Transmit Status register is a word/byte addressable register. The register format is shown in Figure 3-3.

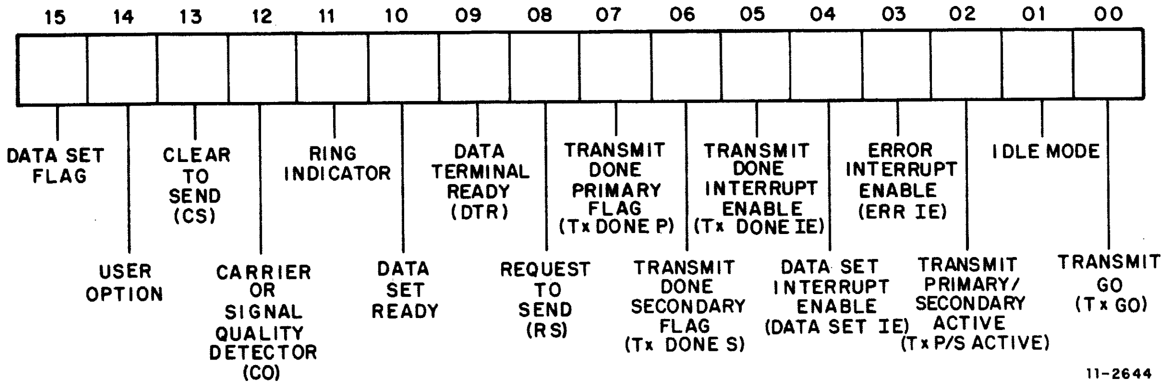

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
DATA SET FLAG
USER OPTION
CLEAR TO SEND (CS)
CARRIER OR SIGNAL QUALITY DETECTOR (CO)
RING INDICATOR
DATA SET READY
DATA TERMINAL READY (DTR)
REQUEST TO SEND (RS)
TRANSMIT DONE PRIMARY FLAG (Tx DONE P)
TRANSMIT DONE SECONDARY FLAG (Tx DONE S)
TRANSMIT DONE INTERRUPT ENABLE (Tx DONE IE)
DATA SET INTERRUPT ENABLE (DATA SET IE)
ERROR INTERRUPT ENABLE (ERR IE)
TRANSMIT PRIMARY/ SECONDARY ACTIVE (Tx P/S ACTIVE)
IDLE MODE
TRANSMIT GO (Tx GO)
11-2644

Figure 3-3 Transmit Control and Status Register Format

Bit	Function	Description
00	TRANSMIT GO (Tx GO)	When set, this bit enables transmit data transfers (NPR). Note: Refer to bit 02 for character count information. This bit is read/write and is cleared by: a. Initialize b. Master Clear c. The DQ11-BB Character Recognition option (bit 07 of the Sequence register). d. By setting the Tx Non-Existent Memory, Tx Latency, or Tx Clock Loss flags. e. By both character counts (CC) going to zero (primary and secondary registers.
01	IDLE MODE	If set, this bit allows the sending of IDLE* characters whenever Tx GO is zero. *Non-transparent mode: The IDLE character is the contents of the Sync register. *Transparent text mode: The IDLE character is Data Link Escape (DLE) followed by the contents of the Sync register, followed by DLE-SYNC, etc. (requires DQ11-BB option).
02	TRANSMIT PRIMARY/ SECONDARY ACTIVE (Tx P/S ACTIVE)	Indicates which of the Character Count and Bus Address registers (CC/BA) will be or are being used. A zero indicates that the Primary (P) register is active; a one indicates that the Secondary (S) register is active. The P register is always the first character count used following Initialize or Master Clear. When Character Count register overflow occurs, the CC/BA register switches (primary to secondary or secondary to primary). If the transfers are prematurely ended, as when clearing Tx GO, the CC/BA register does not switch and is used again when Tx GO is reasserted. This bit is read only and is cleared (set to P register) by Initialize and Master Clear.
03	ERROR INTERRUPT ENABLE (ERR IE)	When set, this bit enables interrupts on Vector B (XX4) from the error flag in the REG/ERR register. The error flag is asserted when any of the error indicators are ON. They are as follows: VRC error BCC error Non-Existent Memory Latency Clock Loss

Bit	Function	Description
03 (Cont)		This bit is read/write and is cleared by Initialize and Master Clear.
04	DATA-SET INTERRUPT ENABLE (DATA SET IE)	When set, this bit enables interrupts (Vector B) from the Data Set flag. The Data Set flag is set from either the leading or trailing edge transition of Carrier Detect (CO), Clear to Send (CS), or RING. This bit is read/write and is cleared by Initialize and Master Clear.
05	TRANSMIT DONE INTERRUPT ENABLE (Tx DONE IE)	If set, this bit allows interrupts to occur on Vector B if the Tx Done bit (06 or 07) is set. This bit is read/write and is cleared by Initialize and Master Clear.
06–07	TRANSMIT DONE PRIMARY/ SECONDARY (Tx DONE P/S)	These bits are set when their respective character counts (P or S) overflow. Bit 06 is TX DONE secondary. These bits are also set by the DQ11-BB Character Recognition option (bit 7 of the Sequence register). Note: If Tx DONE is set by the Sequence register, Tx P/S (bit 2) does not change state. These bits are read/write and are cleared by Initialize and Master Clear.

NOTE

Bits 08–15 are used for Data Set Control functions (Request to Send, Clear to Send, etc). The DQ11 hardware transmits and/or receive data independent of these control functions.

The Data Set Control module has a jumper which, when removed, inhibits Initialize from clearing Data Terminal Ready (DTR) and Request to Send (RS). The user should be aware of required modem and/or hardware delays before Request to Send (RS) can be negated. For instance, Bell 201A modems require a two-bit time delay following the last bit of transmission before negating RS. Due to double-buffered hardware, Tx DONE indicates that data transfers have been completed but not all data has been transmitted. All data has been transmitted only when Tx Active is negated (one-to-four character times after Tx DONE).

The function of each of the following Data Set control bits is given in the format of NAME (EIA/CCITT/PIN EIA/PIN 303).

Bit	Function	Description
08	REQUEST TO SEND (RS) (CA/105/4/D)	Request to Send (RS) is a transmit lead to the data communications equipment (Data Set). This control function is used to condition the local data communications equipment for data transmission and, on a half-duplex channel, to control the direction of data transmission. A program state change directed to RS will be presented to the Data Set on the next positive transition of the transmit clock. When the RS bit is set, an ON signal is transmitted. When cleared, an OFF signal is transmitted. This bit is read/write and is cleared by Initialize and Master Clear (if the jumper is in).
09	DATA TERMINAL READY (DTR) (CD/108.2/ 20/M*) *The shield is the conductor	The Data Terminal Ready (DTR) bit controls switching of the data communications equipment to the communications channel. Auto dial and manual call origination: maintains the established call.

Bit	Function	Description
09 (Cont)	DATA TERMINAL READY (DTR) (CD/108.2/ 20/M*)	Auto Answer: allows handshaking in response to a RING signal. This bit is read/write and is cleared by Master Clear and Initialize (if the jumper is in).
10	DATA SET READY (DSR) (CC/107/6/F)	The Data Set Ready (also referred to as Modem Ready or Interlock) bit reflects the current state of the Data Set Ready lead. The Data Set Ready lead indicates that the modem is powered up and is not in the test, talk, or dial mode. This bit is read only; it is not affected by Initialize or Master Clear.
11	RING (CE/125/22/F*) *The shield is the conductor	This bit reflects the state of the Data Set Ring lead. The trailing and leading edge of the ring lead causes the Data Set flag to be set and an interrupt request follows if the Data Set Interrupt Enable bit is set. This bit is read only; it is not affected by Initialize or Master Clear.
12	CARRIER OR SIGNAL QUALITY DETECTOR (CO) (CR/109/8/M)	This bit reflects the current state of the modem Carrier Control (CO) lead. An OFF indicates that no signal is being received or that the received signal is unsuitable for demodulation. The leading and the trailing edge of CO causes the Data Set flag to be set, and an interrupt request follows if the Data Set IE bit is set. This bit is read only; it is not affected by Initialize or Master Clear.
13	CLEAR TO SEND (CS)	This bit reflects the current state of the modem Clear to Send (CS) lead. An ON state indicates that the modem is ready to transmit data. This signal is raised in response to having sent the request-to-send signal. CS is delayed from RS as a function of the type of modem and the type of lines used (four wire or two wire). The leading and the trailing edge of CS causes the Data Set flag to be set, and an interrupt request follows if the Data Set Interrupt Enable bit is set. This bit is read only; it is not directly affected by Initialize or Master Clear (indirectly via RS).
14	USER OPTION (UO14)	This bit is provided at the backpanel for user connection of a non-standard status bit and/or program interrupt via the Data Set flag. The backpanel connection is TTL only and represents two standard TTL loads. This bit is read/write and is cleared by Initialize and Master Clear.
15	DATA SET FLAG (DS)	If this bit is set and Data Set IE is asserted, a Bus Request (BR) occurs on Vector B. The Data Set flag is asserted by the leading or trailing transitions of Ring, CO, and CS. This bit is read/write and is cleared by Initialize and Master Clear.

3.5.3 REG/ERR Register

The REG/ERR register is a word/byte addressable register. The register format is shown in Figure 3-4.

NOTE

The error bits described below generate an interrupt request on Vector B provided that the Error Interrupt (ERR IE) bit is asserted.

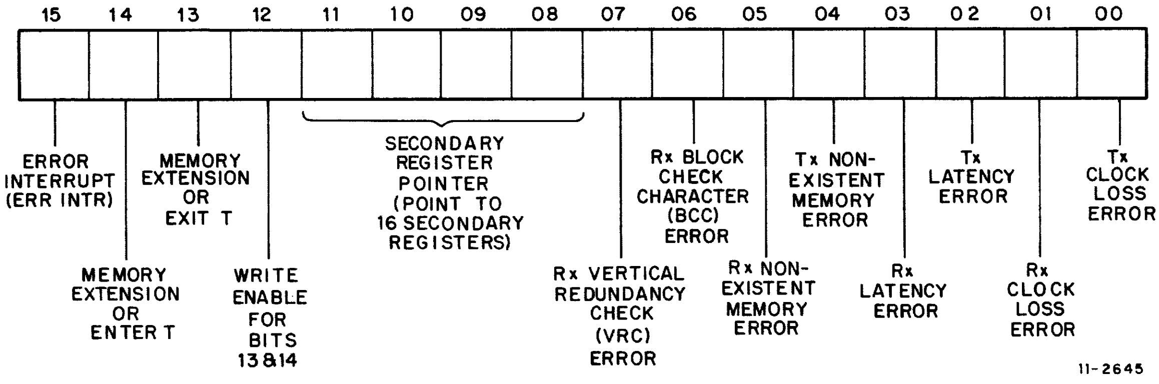

15
14
13
12
11
10
09
08
07
06
05
04
03
02
01
00
ERROR INTERRUPT (ERR INTR)
MEMORY EXTENSION OR EXIT T
SECONDARY REGISTER POINTER (POINT TO 16 SECONDARY REGISTERS)
Rx BLOCK CHECK CHARACTER (BCC) ERROR
Tx NON-EXISTENT MEMORY ERROR
Tx LATENCY ERROR
Tx CLOCK LOSS ERROR
MEMORY EXTENSION OR ENTER T
WRITE ENABLE FOR BITS 13&14
Rx VERTICAL REDUNDANCY CHECK (VRC) ERROR
Rx NON-EXISTENT MEMORY ERROR
Rx LATENCY ERROR
Rx CLOCK LOSS ERROR
11-2645

Figure 3-4 REG/ERR Register Format

Bit	Function	Description
00–01	Tx, Rx CLOCK LOSS	Bits 00, 01 (Tx and Rx respectively) are set if the clock stops with Active Set (Rx or Tx). The Clock Loss flag is set if GO is asserted without the clock or if the clock drops for more than 0.5 second while GO is true. Setting these bits clears the respective GO flip-flop. These bits are read/write and are cleared by Initialize and Master Clear.
02–03	Tx, Rx LATENCY ERROR	Bits 02, 03 (Tx and Rx respectively) are set if an NPR request is not serviced in less than one transfer time (two characters if less than 9 bits/char). Setting this bit clears the respective GO flip-flop.
02–03 (Cont)	Tx, Rx LATENCY ERROR	This error condition implies that the Unibus is overloaded, is malfunctioning, or the baud rate exceeds specifications. Setting these bits clears the respective GO flip-flop. These bits are read/write and are cleared by Initialize and Master Clear.
04–05	Tx, Rx NON-EXISTENT MEMORY ERROR	Bits 04, 05 (Tx and Rx respectively) are set if the DQ11, during an NPR cycle, addresses a non-existent core memory location. This condition implies a program or hardware error and should be dealt with accordingly. Setting these bits clears the respective GO flip-flop. These bits are read/write and are cleared by Initialize and Master Clear.

Bit	Function	Description
06*	Rx BLOCK CHECK CHARACTER (BCC) ERROR *Expander unit only	This bit is asserted if the BCC generated by the received message and the received BCC do not compare. When this bit is set, the Rx BCC is cleared (hardware function) and ready for the next message. Additionally, this does not affect Rx GO. It is recommended that a message retransmit be initiated when this form of error is detected. These bits are read/write and are cleared by Initialize and Master Clear.
07	Rx VERTICAL REDUNDANCY CHECK (VRC) ERROR	This bit is set if the last received character had incorrect character parity. VRC is jumper-selectable for even or odd parity; parity on/off is program-selectable by bit 15 of the Miscellaneous register. If VRC is used with the DQ11-BB Character Recognition option, the control characters transferred to the Transmit Buffer must have correct VRC. Also, the SYNC register must have correct VRC. If the receiver is operating in the double-character mode (≤ 8 bits/char) with an odd character count, the PAD character that immediately follows the message must have correct parity. The PAD character is all 1s so even parity is required for an 8-bit PAD character. Otherwise, a VRC error flag occurs on reception of the last data/PAD character combination. This bit is read/write and is cleared by Initialize and Master Clear.
08–11	SECONDARY POINTER REGISTER	These bits point to 16 secondary registers for read/write operations. The selected register is accessed using select 6 (76XXX6) with word transfers only.

Bits (11–8) Octal No.	Register (Selected Via 76XXX6)
0	Receive Bus Address (Rx BA) – Primary
1	Receive Character Count (Rx CC) – Primary
2	Transmit Bus Address (Tx BA) – Primary
3	Transmit Character Count (Tx CC) – Primary
4	Receive Bus Address (Rx BA) – Secondary
5	Receive Character Count (Rx CC) – Secondary
6	Transmit Bus Address (Tx BA) – Secondary
7	Transmit Character Count (Tx CC) – Secondary
10**	Character Detect (CD)
11	SYNC
12	Miscellaneous (MISC)
13	Transmit Buffer (Tx BUF)
14**	Sequence (SEQ)
15*	Receive Block Check Character (Rx BCC)
16*	Transmit Block Check Character (Tx BCC)
17*	Receive/Transmit (Rx/Tx) Polynomial (Rx, Tx POLY)

*Registers at these addresses are always zero unless the Expander Unit DQ11-AB LRC or CRC Error Detection option (M7816) is installed.

**Registers at these addresses are always zero unless the Expander Unit DQ11-BB Character Recognition option (M7817) is installed.

These bits are read/write and are cleared by Initialize and Master Clear.

12	WRITE ENABLE FOR BITS 14 & 13 (14, 13 WRITE EN)	When set, this bit allows the data written into bits 14 and 13 to be transferred to the Bus Address or the Character Count registers the next time select 6 is used. This bit is self-clearing when the write-to-scratch-pad memory occurs.

Bit	Function	Description
12 (Cont)		This bit is read/write and is cleared by Initialize and Master Clear.
13–14	MEMORY EXTENSION OR ENTER T/EXIT T	The Bus Address (BA) and Character Count (CC) registers are 18-bit registers. The 17th and 18th bits are used for memory extension for the BA and control functions for the CC. Bits 14 and 13 with bit 12 provide a means of reading and/or writing the BA and CC[†] bits (bits 17, 16, are the bits 14 and 13, respectively). In addition, the register pointer bits (bits 11–8) determine what CC or BA is to be accessed. *MEMORY EXTENSION:* Bits 14 and 13 relate to address lines A17 and A16, respectively. These two bits (14, 13) are the read/write ports for transmit and receive extended addresses. *ENTER T (14):* Enter transparency forces transparency (block transfers with BCC) and inhibits all character recognition. This function is used if a message to be transmitted (or received) is completely transparent to all data and control characters. Additionally, this function starts the BCC generation and requires the DQ11-AB LRC/CRC Error Detection option.
13–14 (Cont)	MEMORY EXTENSION OR ENTER T/EXIT T	*EXIT T (13):* If set, this exit transparency bit allows exit from the transparent mode, enables character recognition and appends the TX BCC or tests the RX BCC. This function is used as a companion to ENTER T, a jumper is provided to start the BCC generator which tests/appends one, two, or three BCC characters (selected by jumpers). When used with protocol hardware control, EXIT T starts transmission of a DLE (Data Link Escape) and enables the character recognition circuits to recognize ETX (End of Text), ITB (Intermediate Text Block), and other control characters. SEQ 15 would be used here for character recognition. The ENTER T and EXIT T bits execute their respective functions when the CCs are tested for non-zero by the hardware. This occurs when the current CC register goes to zero and the next CC is tested for non-zero, or at the first transfer following the assertion of GO. When read, bits 14 and 13 always represent the contents of the respective addressed CC or BA registers. Select 6 must be used to transfer a write operation from bits 14 and 13 into the CC or BA registers. Bits 14 and 13 always represent the contents of the hardware memories until address 76XXX6 is used. Once bits 12, 13, and 14 are set, the program must not use read-modify-write instructions

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[†] The two high order bits of the CC registers are used for Enter T/Exit T control functions rather than increasing the character block size. Character blocks are limited to 64K (16 bits). However, the reader must understand that the address for both the CC and the Enter T/Exit T bits are the same.

Bit	Function	Description
13–14 (Cont)	MEMORY EXTENSION OR ENTER T/EXIT T	(BIS, BIT, etc.) on this register (address 76XXX4) until address 76XXX6 is used. During start up, bits 14 and 13 must be cleared by the program. In operation, these bits are self clearing. Refer to programming procedures (Paragraph 3.6) in this chapter.
15	ERROR INTERRUPT (ERR INTR)	This error flag is set if any of the error bits are asserted. The error bits are for VRC, BCC, Rx/Tx Non-Existent Memory, Rx/Tx-Latency, and Rx/Tx Clock Loss. This bit is read only and presents a zero when all error bits are zero and when Master Clear or Initialize has been issued.

3.5.4 Secondary Registers

The secondary registers listed below are addressed by 76XXX6 provided that the previous I/O instruction placed the appropriate 4-bit binary pointer in bits 8–11 of the REG/ERR register.

Register Octal Address	Function
0	Receive Bus Address (Rx BA) – Primary
1	Receive Character Count (Rx CC) – Primary
2	Transmit Bus Address (Tx BA) – Primary
3	Transmit Character Count (Tx CC) – Primary
4	Receive Bus Address (Rx BA) – Secondary
5	Receive Character Count (Rx CC) – Secondary
6	Transmit Bus Address (Tx BA) – Secondary
7	Transmit Character Count (Tx CC) – Secondary
10	Character Detect
11	SYNC
12	Miscellaneous (MISC)
13	Transmit Buffer (Tx BUF)
14	Sequence
15	Receive Block Check Character (Rx BCC)
16	Transmit Block Check Character (Tx BCC)
17	Receive/Transmit (Rx/Tx) Polynomial

A description of each type of secondary register, is given in the subsequent paragraphs.

3.5.4.1 Character Count (CC) and Bus Addressing (BA) Registers – Four Character Count (CC) and four Bus Address (BA) registers are incorporated in the basic unit. Eight are required because there are pairs of registers for each function. Such double-buffering serves to reduce peak load response to CC overflow. The CC registers are loaded with the 2's complement of the number of characters.

The CC and BA are 16-bit registers. The BA register is extended to 18 bits by using bit 12 (14, 13 WRITE EN) and bits 13 and 14 (MEMORY EXTENSION) of the REG/ERR register. Bits 12, 13 and 14 of the REG/ERR register are used with the CC registers to perform special functions. See Paragraph 3.5.3 for an explanation of these bits.

The BA register for transmit and receive must be started on even boundaries (multiple of 16-bit words rather than a half word or 8-bit byte). Ending of the BA (and CC) may be on odd or even boundaries. In the double-character mode ($\leqslant 8$ bits/char) with an odd character count, the PAD character that immediately follows the message must have correct parity; otherwise, a VRC error is generated (if VRC is enabled).

These bits are read/write and are not cleared by Initialize or Master Clear. They must be cleared by a program initialization procedure.

When an Initialize or Master Clear is issued, the Primary/Secondary (P/S) flip-flops select the primary CC and BA registers. When CC overflow occurs, the Secondary register (Tx or Rx – whichever overflowed) is selected. Data transfers cease, and GO is cleared when the flip-flop to the next CC register occurs and is found to be zero. The next GO starts with the last selected CC (the one that terminated the last GO).

NOTE

The hardware does not require or expect the Primary/Secondary (P/S) registers for transmit and receive to be in phase except following Master Clear and Initialize.

3.5.4.2 Character Detection (CHAR-DET) Register – The programmable character recognition option (DQ11-BB) is read/write, for up to sixteen single or double characters (16 bits/character maximum). The hardware reaction upon detection of the characters is also programmable using the Sequence register. The available character fields are as follows:

a. Bits 15–8 are used for single-character recognition (i.e., STX) or for recognizing the second character in double-character recognition. Characters should be right-justified and unused bits must be zero.

b. Bits 7–0 are used for recognizing the first character of double-character recognition (i.e., DLE). Characters should be right-justified and unused bits must be zero.

NOTE

When the DQ11-BB Character Recognition Option is installed, the three standard jumper-selectable characters are inhibited. VRC is not recommended when the DQ11-BB option is being used.

A typical character table for interaction with an IBM 2703 might appear as follows:

	Bits 15–8	Bits 7–10
0	STX	DLE
1	ITB	
2	ETB	
3	ETX	
4	EOT	DLE
5	ENQ	DLE
6	*DLE	*DLE
7	SOH	
8	NAK	
9	◄—— ACK0 ——►	
10	◄—— ACK1 ——►	
11	◄—— RVI ——►	
12	◄—— WACK ——►	
13	Not used (SEQ=0)	
14	Not used (SEQ=0)	
15	Not used (SEQ=0)	

*Required for bit 9 of the Sequence register to identify DLE characters. Use of DLE with ETX makes up a pseudo double character.

These bits are read/write and are NOT cleared by Initialize or Master Clear.

3.5.4.3 Sync Register – The Sync register is programmable for up to sixteen bits. Unused bits must be set to zero. If characters less than or equal to eight bits are used, then the odd and even bytes should contain the same sync character. The least significant bit (LSB) is right-justified, as are the data bits. If VRC is used, the sync character must have correct VRC.

These bits are read/write and are cleared by Master Clear and Initialize.

3.5.4.4 Miscellaneous Register – This register is used mostly for maintenance and bits-per-character selection. The register format is shown in Figure 3-5.

Bit	Function	Description
00*	SHIFT CLOCK	The Shift Clock is used solely for maintenance. The transmit shift register shifts when this bit is set to ONE (transition) and the receiver strobes data when this bit is cleared (transition). This bit is read/write and is cleared by Initialize and Master Clear.
01*	STEP MODE	This bit selects the clocking source for the test loop (see description of bit 3). If this bit is zero, the auto clock source is selected. The source for the auto clock is approximately 14 KHz (RC clock), if loop mode is also selected. If loop mode is not selected, the source clock will be the serial clock receiver leads. If this bit is a one, the Shift Clock (bit 00) is the clock source. This bit is read/write and is cleared by Initialize and Master Clear.
02	NOT USED	
03*	TEST LOOP	If set, this bit causes the transmitter shift register to loop back to the receiver. This bit is read/write and is cleared by Initialize and Master Clear.

*Used for maintenance function.

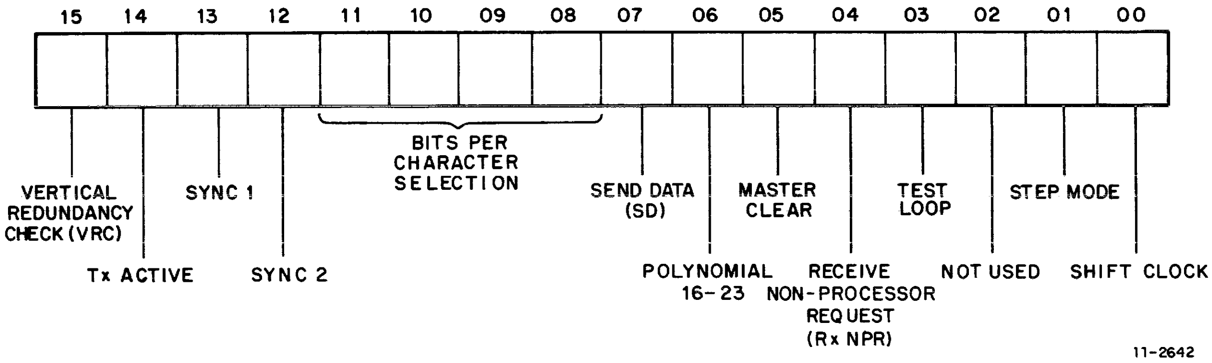


Figure 3-5 Miscellaneous Register Format

Bit	Function	Description
04*	RECEIVE NON-PROCESSOR REQUEST (Rx NPR)	The Rx NPR bit is used for maintenance and is intended for use when Receiver Active is zero. A one written into this bit forces an Rx NPR if Receiver Active is cleared. The data transferred to core is the contents of the receiving shift register (not the buffer) and the Bus Address (BA) and the Character Count (CC) are updated. If Receiver Active is set, the data is taken from the receiver buffer. This bit is write 1s only and always reads as a 0.
05	MASTER CLEAR	The Master Clear function resets all active functions and flags in the DQ11. The CC, BA, MEM EXT, ENTER T, EXIT T, CHAR DET, and the SEQ are not cleared by Master Clear. They are cleared by moving 0s to the respective bits. This bit is write 1s only and always reads as a zero.
06	POLY-NOMIAL 16–23	If set to zero, register pointer 17_8 selects polynomial bits 0–15. In addition, pointers 15_8 and 16_8 select Block Check Characters (BCC) 0–15. If this bit is set to ONE, the register pointer 17_8 selects polynomial bits 16–23 while pointers 15_8 and 16_8 select Block Check Characters (BCC) 16–23. The polynomial and the BCC for bits 16–23 are accessed via bit positions 0–7 respectively. This bit is read/write and is cleared by Master Clear and Initialize.
07*	SEND DATA (SD)	This bit always monitors the transmitted data (contents of transmit shift register LSB). If the Transmit Active bit is a zero and loop mode is selected, this bit is read/write and can be used as an input to the receiver shift register as a maintenance function. A 0 equals MARK and a 1 equals SPACE.

---

*Used for maintenance function.

Bit	Function	Description
07* (Cont)	SEND DATA (SD)	This bit is read/conditional write and is cleared by Initialize and Master Clear.
08–11	BITS PER CHARACTER SELECTION	Bits per character selection is made via bits 11, 10, 9, and 8 as follows:

11	10	9	8	Bits per Char.
0	0	0	0	16
0	0	0	1	15
0	0	1	0	14
0	0	1	1	13
0	1	0	0	12
0	1	0	1	11
0	1	1	0	10
0	1	1	1	9
1	0	0	0	8
1	0	0	1	7
1	0	1	0	6
1	0	1	1	5
1	1	0	0	4
1	1	0	1	3
1	1	1	0	2
1	1	1	1	Not used

Bit	Function	Description
		If VRC is enabled, the selected number of bits per character includes a parity bit in the most significant position. For example, selection of 8 bits/char gives 7 data bits and a parity bit in the most significant position. The transmitter correctly appends the parity bit. The receiver accepts the character (data plus parity bit) checks for correct parity, and transfers the complete character to memory. These bits are read/write and are cleared by Initialize and Master Clear.
12	SYNC 2	SYNC 2 is set when the receiver becomes synchronized (framed). This bit is read only and is cleared by Initialize, Master Clear, and by clearing Active.
13	SYNC 1	A switch is provided on the M7813 module to allow framing after reception of one or two sync characters. SYNC 1 is set when the receiver has received one sync character. With the switch OFF, SYNC 1 directly sets SYNC 2 and allows framing to be completed. If the switch is ON, SYNC 1 conditions SYNC 2 to be set if the next received character is another SYNC. If the next received character is not a SYNC, then SYNC 1 is cleared, and a bit-by-bit search continues for another sync character. This bit is read only and is cleared by Initialize, Master Clear and by clearing Active.
14	Tx ACTIVE	When set, this bit indicates that the transmitter is in the process of transmitting a character; it will remain set until all characters and/or bits have been transmitted. The bit remains set in the idle mode. This bit is read only and is cleared by Initialize, Master Clear, and lack of data to transmit.

Bit	Function	Description
15	VERTICAL REDUNDANCY CHECK (VRC)	When set, the VRC bit enables parity to be generated (transmit) or checked (receive) in the most significant bit position of the selected character. VRC odd/even is switch-selectable. The transmit VRC is corrected, in serial, as the data is presented to the serial line. VRC is corrected on all characters (data, sync, DLE, etc.) with the exception of BCC and PAD. Thus, character recognition is done without corrected VRC and must be taken into account when character recognition is used. With VRC enabled, the sync register must have correct VRC and the bits/char selection must include parity. The received characters that are transferred to memory include the parity bit in the most significant position. When operating in the double-character mode (≤8 bits/char) with an odd character count, the PAD character immediately following the message must have correct parity; otherwise, a VRC error flag is generated on reception of the last data/PAD character combination. This bit is read/write and is cleared by Master Clear and Initialize.

3.5.4.5 Transmit Buffer (Tx BUF) Register – The Transmit Buffer is a 16-bit, read-only maintenance register which monitors the parallel input to the Transmit Shift register. These bits are cleared by Initialize and Master Clear.

3.5.4.6 Sequence (SEQ) Register (Figure 3-6) – The Sequence register (requires DQ11-BB option) is a programmable 16-by-16 bit register which defines hardware functions when a control character is recognized. The control character recognized and the programmed sequence for that character must be at the same character detected address.

The SEQ register is used by both the receive and transmit logic. The following bit descriptions indicate which bits function for receive, transmit, or both.

NOTE

If a character is detected and no bits are set in the respective sequence register, no hardware functions take place and the receive (transmit) characters are handled in the normal way.

All bits are read/write and are not cleared by Master Clear or Initialize. All Sequence register bits must be initialized by the program following power up and preceding the transmission and/or receiving of data.

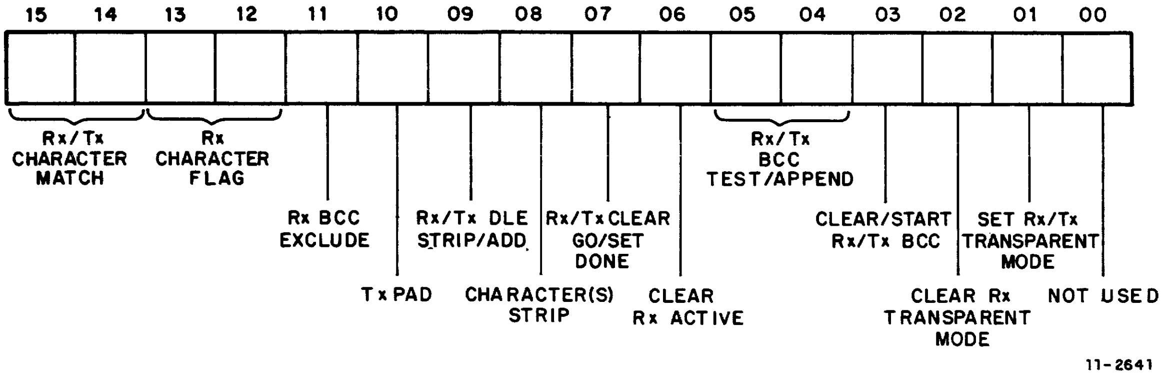


Figure 3-6 Sequence Register Format

Bit	Function	Description
00	NOT USED	
01	SET Rx/Tx TRANSPARENT MODE	Requires double-byte match, (between Tx/Rx shift register and character detection register) to function, i.e., Low Byte and High Byte (LB and HB). (See description of bit 14.) *RECEIVE:* Enters receive transparent text mode and inhibits strip sync. Strip idle and DLE in transparent mode will require the use of bit 9 of the Sequence register. During transparency text, character recognition is disabled except when preceded by DLE which is stripped by bit 9. *TRANSMIT:* Enters transmit transparent text mode which modifies idle from sync character to alternating sync and DLE characters and inhibits character recognition unless preceded by DLE. Using bit 9 also allows DLE stuffing. All SEQ control is inhibited except bit 9. Refer to REG/ERR register to transmit exit transparency (EXIT T).
02	CLEAR Rx TRANS-PARENT MODE	Requires a single-byte match to function (HB). (See description of bit 15.) Detected control character must be preceded by a DLE character. (This is a pseudo double character match.) Refer to discussion of bit 09 of this register. The use of SEQ 09 to strip a DLE that is followed by a control function is treated in the hardware as a double-character match, thus allowing exiting transparency.
02 (Cont)		Reference REG/ERR register, bit 13, for clearing Tx Transparent mode (EXIT T).
03	CLEAR/ START Rx/Tx BCC	Clears and starts the BCC generator with the next character (following the detected control character) if it is the occurrence following Initialize, Master Clear, or GO (OFF to ON). In all other cases, the BCC starts and includes the current control character unless the BCC Exclude bit (bit 11) is used. The first BCC start-up control character (first STX) is excluded from the BCC. However, the next BCC start-up character within the same message is included (second STX) in the BCC unless the BCC exclude bit is used. The BCC start control character (first STX) may be included in the BCC, if desired, via jumpers on the M7816, M7817 modules; however, this mode of operation is not supported by the diagnostics.
04–05	Rx/Tx BCC TEST/ APPEND	These bits select and actually enable the testing (receive mode) or appending (transmit mode) of the selected number of BCC characters immediately following the control character (ETX, ETB, etc.) The bit selections are: **Bits 5, 4 — BCC Character** 00 — None 10 — Three 01 — Two 11 — One

Bit	Function	Description
04–05 (Cont)	Rx/Tx BCC TEST/ APPEND	Each BCC character is the same bit length as the bits per character selection. For example, using 8 bits/char and a 16 bit BCC requires testing or appending two BCC characters. The received BCC characters are not transferred to core and consequently do not affect the CC. Additionally, Rx interrupts are suspended while the respective BCC is being processed. This is particularly useful if the programmer desires a character detect interrupt on the control character which asserted bits 5, 4 as an indication that a block of data has been received without error.
06	CLEAR Rx ACTIVE	Clears Receive Active, SYNC 1, SYNC 2, which is useful for forcing re-sync during a message. GO is not cleared. When framing again occurs, transfers resume with the current CC and BA. The control character that required Receive Active to be cleared is transferred to core before Receive Active is cleared.
07	Rx/Tx CLEAR GO/SET DONE	Clears the GO bit and sets DONE for the current CC register in use (P or S) after the control characters are transferred to core. The CC does not flip to the next register when this bit is used. When framing again occurs, transfers resume with the current CC and BA. If a BCC test/append is in progress, the DONE interrupt is held up until the BCC test/append is completed.

Bit	Function	Description
08	Rx CHARACTER (S) STRIP	This bit strips received characters from transfers to core but not from the BCC register (see description of bit 11 for BCC exclude). If bit 15 is a one, a character less than or equal to eight bits that compares with the character register (right-justified) is stripped. If bit 14 is a one, a double character or a character greater than eight bits is stripped. When both bits are set, bit 14 dominates hardware control.
09	Rx/Tx DLE STRIP/ADD	*RECEIVE:* Single character match (specified by bit 15) strips the first character as with DLE when in the transparent text mode. The next character following DLE is tested for "Exit Text Transparency" and SYNC character. If the next character is a SYNC, it is stripped as was the DLE; however, if the next character is a DLE, it is passed as data. *TRANSMIT:* Adds another character which is used for DLE, DLE in the transparent mode.

NOTE

The character detect register must contain DLE in both bytes at the address where SEQ 9 is set. This is due to the hardware needing to know what a DLE is.

DLE stripped (Rx) or added (Tx) is always deleted from the error detection logic (BCC).

Bit	Function	Description
10	Tx PAD	*TRANSMIT ONLY:* Insert pad character(s) following the last characters to be transmitted, as in EOT, PAD or EOT BCC PAD. The PAD character consists of all 1s. Refer to the appropriate cautions if VRC is enabled. A jumper is available for selecting one or two pad characters. The DQ11 requires one NULL (PAD, SYNC, etc.) character following the last character to be received. This is due to the BCC registers and double-character transfers. The shipping configuration is always set for one pad.
11	Rx BCC EXCLUDE	This bit allows any single control character (as specified by bit 15 if less than or equal to 8 bits and bit 14 if greater than 8 bits) to be excluded from the BCC accumulation when in the non-transparent mode. When this bit is used, the baud rate must not exceed 250K.
12–13	Rx CHARACTER FLAG	These bits cause the character flag to be set and also latch the address of the control character into four CHARACTER DETECT bits (11–8) for a minimum of one character time. The address changes when the next character is detected. Bit 13 causes a character flag if a single (less than or equal to 8 bits) character is detected. Bit 12 causes a character flag if a double or greater than 8-bit character is detected. If a BCC test/append is in progress, the character detected interrupt is held up until the BCC test/append is completed.
14–15	Rx/Tx CHARACTER MATCH	These bits define bytes in the character detect register for comparison with the content of the transmit and receive shift registers. For example, bit 15 should be set to compare with a stored STX (HB character detect), and bit 14 should be set for DLE STX (LB, HB character detect respectively). The effective character detect storage space can be increased by using bits 15 and 14 on a single-character detect address. In this case, the SEQ control function is dominated by bit 14 which is important for character flags, transparency control, etc. The advantage of using bits 14 and 15 on a single entry can be demonstrated on an entry such as DLE STX. If STX alone is detected, bit 15 allows SEQ control functions to be executed. However, if both DLE and STX are detected, bit 15 will be ignored and bit 14 allows the selected SEQ functions to be executed; that is, a double-character match is required to enter text transparency.

3.5.4.7 Receive/Transmit Block Check Character (BCC) Registers – The Rx/Tx BCC register (register pointers 15 and 16, respectively) provide a 16-bit, read-only register for monitoring the BCC register as a maintenance function. The Rx BCC operates on a one-character delay from the incoming data. If an error is detected, the Rx BCC register is cleared immediately, and the Rx BCC error flag is set. The Tx BCC functions one-bit time behind the transmitted data. The Tx BCC is right-justified, and bit zero is the Least Significant Bit (LSB). The BCC length must be a multiple of the character size.

3.5.4.8 Rx/Tx Polynomial Register – A 24-bit programmable register is used to store the polynomial used in generating the BCC character during transmission or checking the BCC character during reception. The polynomial must be common to both transmitting and receiving stations so only one register is required.

The basic register is 16 bits long. It can be expanded to 24 bits. MISC register bit 6 is used to access the additional 8 bits (16–23).

Specific instructions for programming the Rx/Tx POLY register are given below using the CRC 12 polynomials as an example.

1. Assign polynomial terms to register bit positions. Assign the second highest term to the 0 bit position. The highest term is always ignored because the hardware automatically includes it. Proceed from the second highest term, in descending order, with the last term (1 or X^0) in the highest bit position.

2. Put a 1 in each register bit position that contains a term in the polynomial. Put a 0 in each register bit position that does not contain a polynomial term. All other unused bit positions must contain 0s.

The following chart shows the octal value of the Tx/Rx POLY register for some polynomials up to 16 bits in length.

Polynomial	Tx/Rx POLY Register (Octal)
$X^6 + 1$ (LRC 6)	000040
$X^8 + 1$ (LRC 8)	000200
$X^{16} + 1$ (LRC 16)	100000
$X^{12} + X^{11} + X^3 + X^2 + X + 1$ (CRC 12)	007401
$X^{16} + X^{15} + X^2 + 1$ (CRC 16)	120001
$X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)	102010

Example

Load the CRC 12 polynomial into the Tx/Rx POLY register. The polynomial is $X^{12} + X^{11} + X^3 + X^2 + X + 1$.

In accordance with Step 1 above, the bit assignments are shown below:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit Position
				1	X	X^2	X^3	X^4	X^5	X^6	X^7	X^8	X^9	X^{10}	X^{11}	Term

In accordance with Step 2 above, the binary values are assigned as shown below:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit Position
				1	X	X^2	X^3	X^4	X^5	X^6	X^7	X^8	X^9	X^{10}	X^{11}	Term
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	Binary
0		0			7			4			0			1		Octal

3.6 GENERAL PROGRAMMING PROCEDURES

3.6.1 Introduction

This section describes, in general, the operational characteristics of the DQ11 that have programming significance. Specific functions are described in relation to the basic DQ11 and the DQ11-AB and -BB options. Five basic programming examples are shown:

Example 1: Clearing the DQ11 after powering up.

Example 2: Starting the transmitter using the test loop mode.

Example 3: Starting the transmitter and receiver using the test loop mode.

Example 4: Looping the transmitter and receiver and using the BCC feature.

Example 5: Looping the transmitter and receiver and using the BCC and protocol features.

3.6.2 Basic Unit (DQ11-DA/EA)

The basic DQ11 performs the following functions under program control.

1. Bidirectional conversion of signals (voltage levels) between the data set (EIA or current loop) and the DQ11 (TTL).
2. Controls two data set leads: Request to Send (RS) and Data Terminal Ready (DTR). Monitors four data set leads: Carrier Detect (CO), Clear to Send (CS), Ring Indicator (RING), and Data Set Ready.
3. In the receive mode, serial data is converted to parallel data and transferred to the PDP-11 memory. In the transmit mode, parallel data from the PDP-11 memory is converted to serial data for transmission.
4. Data transfers to and from the PDP-11 memory are performed during NPR cycles at the rate of one per cycle. Only word transfers are used; therefore, in double-character operation, a word transfer contains two characters.
5. Character size is selectable up to 16 bits. Single characters must contain more than 8 bits. Double characters are limited to 8 bits or less.
6. Assert RX DONE and TX DONE flags to indicate to the PDP-11 processor that reception or transmission has been completed.
7. Two character count registers and two bus address registers are provided for both the receiver and transmitter which allows maximum PDP-11 processor/program response time for RX and TX DONE flags.
8. Provides three switch-selectable control characters. The Character flag bit is set to notify the program that the selected character has been received.
9. Sets the Data Set flag to notify the program of a change in the status of the data set.

3.6.3 Error Detection Option (DQ11-AB)

An additional module (M7816) provides transparent data block transfers with error control. Under limited program control, it performs the following functions.

1. Provides up to 24-bit polynomials for longitudinal redundancy checking (LRC) or cyclic redundancy checking (CRC).
2. Provides two block check character (BCC) generators. One to test BCCs (receive) and one to append BCCs (transmit).
3. The transparent mode is hardware-controlled, using two bits of the REG/ERR register. When bit 14 (ENTER T) is set, transparency is entered when the related character count is used. When bit 13 (EXIT T) is set, it allows exit from transparency in any subsequent character count field.

   This mode of operation is called total transparency to differentiate it from the same mode when it is initiated by the protocol option (DQ11-BB). Under protocol control, it is called transparent text.

3.6.4 Protocol Option (DQ11-BB)

Adding the M7817 module to the DQ11-AB configuration provides programmable hardware control for characters equal to or less than 8 bits in length (single or double characters).

Under program control, it performs the following functions.

1. Controls BCC computation. Allows exclusion of a character from the BCC computation when operating in the non-transparent mode.
2. Sets the Character Detect flag when a select control character is received.
3. Transmits a PAD character (all 1s) following the last character to be transmitted.
4. Inserts and deletes DLE characters.

3.6.5 Operational Features with Programming Significance

VRC (Parity Check)
The basic DQ11 provides Vertical Redundancy Checking (VRC) or parity checking. VRC in a synchronous communications system is of questionable usefullness; therefore, its use is not recommended.

Odd or even VRC is switch-selectable. Care should be used when implementing VRC during double-character operation in the receive mode with an odd character count. The receiver shift register must contain two characters before its contents are transferred to the receiver buffer register and on to the PDP-11 memory. With an odd count, the receiver shift register contains only one character when the data ends. Another character must be shifted in to fill this register so the transfer to the PDP-11 memory can take place. This fill character must have correct parity or an invalid VRC error flag is generated.

Clearing Registers During Power Up
When the PDP-11 system is powered up, the Initialize (INIT) signal is generated and distributed throughout the system to clear registers, flip-flops, etc. The character count and bus address registers and the memory extension bits (REG/ERR register bits 13 and 14) are not cleared by INIT. It is imperative that these registers and bits be cleared before continuing. They are cleared by writing 0s into them.

Preparation for Transmission
The DQ11 is prepared for transmission by loading the BA and CC registers. The BA is loaded with the address (PDP-11 memory) of the first word to be transferred to the DQ11 for transmission. Data is transmitted LSB first.

The CC register is loaded with the 2's complement of the number of characters to be transmitted. The CC/BA counter is incremented only. When loaded with the 2's complement of the character count, the number of counts remaining until overflow (all 0s) is actual number of characters.

Preparation for Reception
The DQ11 is prepared for reception by loading the BA and CC registers as in preparation for transmission. The BA is loaded with the address (PDP-11 memory) of the first word to be transferred to memory. The SYNC register must be loaded with the correct sync character.

Total Transparency (DQ11-AB Option)
As described in Paragraph 3.6.3, total transparency is implemented by the AB option using REG/ERR bits 14 (ENTER T) and 13 (EXIT T). REG/ERR bit 12 (14, 13 WRITE EN) must be set to allow the state of bits 13 and 14 to be written into the CC/BA register.

3.6.6 Programming Examples

EXAMPLE 1 – Clearing the DQ11 after powering up.

```
1          000000      .ASECT
2          000000      .ENABL ABS
3          160010      RXCSR=160010
4          160012      TXCSR=160012
5          160014      ERREG=160014
6          160016      SECREG=160016
7          004010      CHAR=4010                 ;CHARACTER LENGTH
8          002000      COUNT=2000
9          002002      WENP=2002
10         160015      DQREG=160015
11         177764      TXWC=177764               ;TRANSMITT CHARACTER COUNT
12         177764      RXWC=177764               ;RECEIVE LENGTH
13         002400      RXBUF=2400                ;RECEIVE BUFFER
14         002200      TXBUF=2200                ;TRANSMITT BUFFER
15         013026      SYNC=13026                ;SYNC CHARACTER
16                                               ;
17                                               ;
18                                               ;
19         001000      .=1000
20  01000  105037      CLRB@#DQREG               ;SET POINTER TO 0
           160015
21  01004  012737      MOV#10,@#COUNT            ;SET TO COUNT # OF REGS TO CLEAR
           000010
           002000
22  01012  012737      MOV#10000,@#WENP          ;SET POINTER AND BIT 12 IN WENP
           010000
           002002
23  01020  013737   1$:MOV @#WENP,@#ERREG        ;PUT INTO ERREG
           002002
           160014
24  01026  005037      CLR@#SECREG
           160016
25  01032  062737      ADD #200,@#WENP
           000200
           002002
26  01040  005337      DEC@#COUNT                ;DECREMENT COUNT
           002000
27  01044  001365      BNE 1$                    ;BRANCH IF NOT DONE
28  01046  000000      HALT
29         000001'     .END


SYMBOL TABLE

CHAR   = 004010          COUNT = 002000          DQREG = 160015
ERREG  = 160014          RXBUF = 002400          RXCSR = 160010
RXWC   = 177764          SECREG= 160016          SYNC  = 013026
TXBUF  = 002200          TXCSR = 160012          TXWC  = 177764
WENP   = 002002
. ABS.   001050     000
         000000     001
```

EXAMPLE 2 – Starting the transmitter using the test loop mode. Includes clearing of the DQ11 per Example 1.

```
       000000      .ASECT
       000000      .ENABL ABS
       160010      RXCSR=160010
       160012      TXCSR=160012
       160014      ERREG=160014
       160016      SECREG=160016
       004010      CHAR=4010             ;CHARACTER LENGTH
       002000      COUNT=2000
       002002      WENP=2002
       160015      DQREG=160015
       177764      TXWC=177764           ;TRANSMITT CHARACTER COUNT
       177764      RXWC=177764           ;RECEIVE LENGTH
       002400      RXBUF=2400            ;RECEIVE BUFFER
       002200      TXBUF=2200            ;TRANSMITT BUFFER
       013026      SYNC=13026            ;SYNC CHARACTER
                                         ;
                                         ;
                                         ;
       001000      .=1000
01000  105037      CLRB@#DQREG           ;SET POINTER TO 0
       160015
01004  012737      MOV#10,@#COUNT        ;SET TO COUNT # OF REGS TO CLEAR
       000010
       002000
01012  012737      MOV#10000,@#WENP      ;SET POINTER AND BIT 12 IN WENP
       010000
       002002
01020  013737    1$:MOV @#WENP,@#ERREG   ;PUT INTO ERREG
       002002
       160014
01026  005037      CLR@#SECREG
       160016
01032  062737      ADD #200,@#WENP
       000200
       002002
01040  005337      DEC@#COUNT            ;DECREMENT COUNT
       002000
01044  001365      BNE 1$                ;BRANCH IF NOT DONE
01046  000000      HALT
                          ;THE FOLLOWING CODE IS ADDED TO PROGRAM 1
01050  012737      MOV#5000,@#ERREG        ;SET SEC POINTER TO MISC REG
       005000
       160014
01056  012737      MOV#40,@#SECREG         ;CLEAR REGISTER
       000040
       160016
01064  012737      MOV#11000,@#ERREG       ;SET SEC POINTER TO TXBA REG
       011000
       160014
01072  012737      MOV#TXBUF,@#SECREG      ;LOAD TXBA PRIMARY TO TXBUF
       002200
       160016
01100  012737      MOV#11400,@#ERREG       ;SET SEC REG TO TXCC PRIMARY
       011400
       160014
01106  012737      MOV#TXWC,@#SECREG       ;LOAD TXCC WITH TXWC
       177764
```

```
             160016
36 01114 012737      MOV#5000,@#ERREG       ;SET SEC POINTER TO MISC REG
             005000
             160014
37 01122 012737      MOV#4010,@#SECREG      ;8 BITS/CHAR AND TEST LOOP
             004010
             160016
38 01130 005237      INC@#TXCSR             ;SET TX GO BIT
             160012
39 01134 032737   2$:BIT#200,@#TXCSR        ;LOOK FOR TX DONE
             000200
             160012
40 01142 001774      BEQ 2$                 ;BRANCH IF NOT DONE
41 01144 000000      HALT
42       002200      .=2200
43 02200    026      .BYTE 26,26,01,10,02,101,102,103,104,105,106,03
   02201    026
   02202    001
   02203    010
   02204    002
   02205    101
   02206    102
   02207    103
   02210    104
   02211    105
   02212    106
   02213    003
44       000001'     .END



SYMBOL TABLE

CHAR   = 004010         COUNT = 002000         DQREG = 160015
ERREG  = 160014         RXBUF = 002400         RXCSR = 160010
RXWC   = 177764         SECREG= 160016         SYNC  = 013026
TXBUF  = 002200         TXCSR = 160012         TXWC  = 177764
WENP   = 002002
. ABS.   002214     000
         000000     001
```

EXAMPLE 3 – Starting the transmitter and receiver using the test loop mode. Includes clearing of the DQ11 per Example 1.

```
             000000      .ASECT
             000000      .ENABL ABS
             160010      RXCSR=160010
             160012      TXCSR=160012
             160014      ERREG=160014
             160016      SECREG=160016
             004010      CHAR=4010                ;CHARACTER LENGTH
             002000      COUNT=2000
             002002      WENP=2002
             160015      DQREG=160015
             177764      TXWC=177764              ;TRANSMITT CHARACTER COUNT
             177764      RXWC=177764              ;RECEIVE LENGTH
             002400      RXBUF=2400               ;RECEIVE BUFFER
             002200      TXBUF=2200               ;TRANSMITT BUFFER
             013026      SYNC=13026               ;SYNC CHARACTER
                                                  ;
                                                  ;
                                                  ;
             001000      .=1000
      01000  105037      CLRB@#DQREG              ;SET POINTER TO 0
             160015
      01004  012737      MOV#10,@#COUNT           ;SET TO COUNT # OF REGS TO CLEAR
             000010
             002000
      01012  012737      MOV#10000,@#WENP         ;SET POINTER AND BIT 12 IN WENP
             010000
             002002
      01020  013737    1$:MOV @#WENP,@#ERREG      ;PUT INTO ERREG
             002002
             160014
      01026  005037      CLR@#SECREG
             160016
      01032  062737      ADD#200,@#WENP
             000200
             002002
      01040  005337      DEC@#COUNT               ;DECREMENT COUNT
             002000
      01044  001365      BNE 1$                   ;BRANCH IF NOT DONE
      01046  000000      HALT
      01050  012767      MOV#5000,ERREG             ;SET SEC POINTER TO MISC REG
             005000
             156736
      01056  012737      MOV#40,@#SECREG            ;CLEAR REGISTER
             000040
             160016
      01064  012737      MOV#10000,@#ERREG          ;SELECT RXBA PRIMARY
             010000
             160014
      01072  012737      MOV#RXBUF,@#SECREG         ;LOAD RXBA WITH RXBUF
             002400
             160016
      01100  012737      MOV#10400,@#ERREG        ;SELECT RXCC REGISTER
             010400
             160014
```

```
34 01106 012737         MOV#RXWC,@#SECREG     ;LOAD RXCC WITH RXWC
         177764
         160016
35 01114 012737         MOV#11000,@#ERRREG    ;SELECT TXBA PRIMARY
         011000
         160014
36 01122 012737         MOV#TXBUF,@#SECREG    ;LOAD TXBA WITH TXBUF
         002200
         160016
37 01130 012737         MOV#11400,@#ERRREG    ;SELECT TXCC PRIMARY
         011400
         160014
38 01136 012737         MOV#TXWC,@#SECREG     ;LOAD TXCC WITH TXWC
         177764
         160016
39 01144 012737         MOV#4400,@#ERRREG     ;SELECT SYNC REGISTER
         004400
         160014
40 01152 012737         MOV#SYNC,@#SECREG     ;LOAD SYNC REG WITH SYNC
         013026
         160016
41 01160 012737         MOV#5000,@#ERRREG     ;SELECT MISC REGISTER
         005000
         160014
42 01166 012737         MOV#CHAR,@#SECREG     ;SELECT LENGTH AND TESTLOOP BIT
         004010
         160016
43 01174 005237         INC@#RXCSR            ;SET RX GO BIT IN RXCSR
         160010
44 01200 005237         INC@#TXCSR            ;SET TX GO BIT IN TXCSR
         160012
45 01204 032737      3$:BIT#200,@#RXCSR       ;WAIT FOR DONE BIT
         000200
         160010
46 01212 001774         BEQ 3$                ;BRANCH IF DONE BIT NOT SET
47 01214 000000         HALT
48       002200         .=2200
49 02200    026         .BYTE 26,26,01,10,02,101,102,103,104,105,106,03
   02201    026
   02202    001
   02203    010
   02204    002
   02205    101
   02206    102
   02207    103
   02210    104
   02211    105
   02212    106
   02213    003
50       000001'        .END
```

```
SYMBOL TABLE

CHAR   = 004010          COUNT = 002000          DQREG  = 160015
ERREG  = 160014          RXBUF = 002400          RXCSR  = 160010
RXWC   = 177764          SECREG= 160016          SYNC   = 013026
TXBUF  = 002200          TXCSR = 160012          TXWC   = 177764
WENP   = 002002
. ABS.   002214     000
         000000     001
```

Table 3-1
Message/Data Used in Programming Examples 4 and 5

ASCII Character			BCC Function	Protocol Function	Hardware Function
Symbol	**Binary**	**Octal**			
SYN	00010110	26	None	None	Synchronize receiver
SYN	00010110	26	None	None	
SOH	00000001	1	ENTER T	None	RX Active
BS	00001000	10	Starts BCC.	None	
STX	00000010	2	All characters included until CC overflow and EXIT T tests or appends BCC.	STX starts BCC on next character (a). Include all character until BCC test/append sequence is detected. For TX, add DLE before ETX then send BCC. For RX, strip DLE then test BCC after ETX.	
A	01000001	101			
B	01000010	102			
C	01000011	103			
D	01000100	104			
E	01000101	105			
F	01000110	106			
ETX	00000011	3			
BCC	–	–			
BCC	–	–			

EXAMPLE 4 – Looping the transmitter and receiver and using the BCC feature. This example shows how to program the BCC Option (DQ11-AB) using the ENTER T/EXIT T control bits to provide block transfers in the transparent mode.

The polynomial that is loaded into the RX/TX Polynomial Register is arbitrary and is used only to illustrate the programmability of the register.

```
      000000     .ASECT
      000000     .ENABL ABS
      160010     RXCSR=160010
      160012     TXCSR=160012
      160014     ERREG=160014
      160016     SECREG=160016
      004010     CHAR=4010            ;CHARACTER LENGTH
      002000     COUNT=2000
      002002     WENP=2002
      160015     DQREG=160015
      177764     TXWC=177764          ;TRANSMITT CHARACTER COUNT
      177764     RXWC=177764          ;RECEIVE LENGTH
      002400     RXBUF=2400           ;RECEIVE BUFFER
      002200     TXBUF=2200           ;TRANSMITT BUFFER
      013026     SYNC=13026           ;SYNC CHARACTER
                                      ;
                                      ;
                                      ;
      001000     .=1000
01000 105037     CLRB@#DQREG          ;SET POINTER TO 0
      160015
01004 012737     MOV#10,@#COUNT       ;SET TO COUNT # OF REGS TO CLEAR
      000010
      002000
01012 012737     MOV#10000,@#WENP     ;SET POINTER AND BIT 12 IN WENP
      010000
      002002
01020 013737   1$:MOV @#WENP,@#ERREG  ;PUT INTO ERREG
      002002
      160014
01026 005037     CLR@#SECREG
      160016
01032 062737     ADD#200,@#WENP
      000200
      002002
01040 005337     DEC@#COUNT           ;DECREMENT COUNT
      002000
01044 001365     BNE 1$               ;BRANCH IF NOT DONE
01046 012705     MOV#17,R5            ;MOV ACOUNT INTO R5
      000017
01052 112737   2$:MOVB#10,@#DQREG     ;SEL CHAR ADDRESS
      000010
      160015
01060 005037     CLR@#SECREG          ;CLEAR
      160016
01064 112737     MOVB#14,@#DQREG      ;SELECT SEQ ADDRESS
      000014
      160015
01072 005037     CLR@#SECREG          ;CLEAR
      160016
01076 105237     INCB@#RXCSR          ;INCREMENT CD/SEQ POINTER
      160010
```

```
34 01102 005305       DEC R5                ;DEC COUNT
35 01104 001362       BNE 2$                ;GO BACK IF NOT DONE
36 01106 112737       MOVB#17,@#DQREG       ;LOAD POLY SELECTOR
         000017
         160015
37 01114 005037       CLR@#SECREG           ;CLEAR
         160016
38 01120 000000       HALT
39 01122 012737       MOV#5000,@#ERREG        ;SET SEC POINTER TO MISC REG
         005000
         160014
40 01130 012737       MOV#40,@#SECREG         ;CLEAR REGISTER
         000040
         160016
41 01136 012737       MOV#10000,@#ERREG       ;SELECT RXBA PRIMARY
         010000
         160014
42 01144 012737       MOV#RXBUF,@#SECREG      ;LOAD RXBA WITH RXBUF
         002400
         160016
43 01152 012737       MOV#50400,@#ERREG     ;SELECT RXCC REGISTER
         050400
         160014
44 01160 012737       MOV#RXWC,@#SECREG       ;LOAD RXCC WITH RXWC
         177764
         160016
45 01166 012737       MOV#11000,@#ERREG       ;SELECT TXBA PRIMARY
         011000
         160014
46 01174 012737       MOV#TXBUF,@#SECREG      ;LOAD TXBA WITH TXBUF
         002200
         160016
47 01202 012737       MOV#51400,@#ERREG       ;SELECT TXCC PRIMARY
         051400
         160014
48 01210 012737       MOV#TXWC,@#SECREG       ;LOAD TXCC WITH TXWC
         177764
         160016
49 01216 012737       MOV#4400,@#ERREG        ;SELECT SYNC REGISTER
         004400
         160014
50 01224 012737       MOV#SYNC,@#SECREG       ;LOAD SYNC REG WITH SYNC
         013026
         160016
51 01232 012737       MOV#5000,@#ERREG        ;SELECT MISC REGISTER
         005000
         160014
52 01240 012737       MOV#CHAR,@#SECREG       ;SELECT LENGTH AND TESTLOOP BIT
         004010
         160016
53 01246 012737       MOV#32400,@#ERREG       ;SELECT RXWC SEC
         032400
         160014
54 01254 005037       CLR@#SECREG             ;LOAD EXIT T ,CLR WC
         160016
55 01260 012737       MOV#33400,@#ERREG       ;SELECT TXWC SEC LOAD
         033400
         160014
```

```
56 01266 005037       CLR@#SECREG           ;EXIT T,CLR WC
         160016
57 01272 012737       MOV#7400,@#ERREG      ;SEL BCC POLY
         007400
         160014
58 01300 012737       MOV#115730,@#SECREG   ;LOAD
         115730
         160016
59 01306 005237       INC@#RXCSR            ;SET RX GO BIT IN RXCSR
         160010
60 01312 005237       INC@#TXCSR            ;SET TX GO BIT IN TXCSR
         160012
61 01316 032737    3$:BIT#200,@#RXCSR       ;WAIT FOR DONE BIT
         000200
         160010
62 01324 001774       BEQ 3$                ;BRANCH IF DONE BIT NOT SET
63 01326 000000       HALT
64       002200       .=2200
65 02200    026       .BYTE 26,26,01,10,02,101,102,103,104,105,106,03
   02201    026
   02202    001
   02203    010
   02204    002
   02205    101
   02206    102
   02207    103
   02210    104
   02211    105
   02212    106
   02213    003
66       000001'      .END



SYMBOL TABLE

CHAR   = 004010        COUNT  = 002000        DQREG  = 160015
ERREG  = 160014        RXBUF  = 002400        RXCSR  = 160010
RXWC   = 177764        SECREG= 160016         SYNC   = 013026
TXBUF  = 002200        TXCSR  = 160012        TXWC   = 177764
WENP   = 002002
. ABS.   002214     000
         000000     001
```

EXAMPLE 5 – Looping the transmitter and receiver and using the BCC and protocol features. This example shows how to program the Protocol Option (DQ11-BB) and the BCC Option (DQ11-AB) using the Protocol Option to control the BCC Option.

Detection of STX starts the BCC accumulation on the chracter following the STX. Detection of ETX causes the transmitter protocol control logic to insert a DLE (excluded from BCC) before the ETX and then generate two BCC characters.

The receiver protocol logic detects a DLE and checks the next character. It is an ETX. This sequence (DLE,ETX) generates the BCC test function after the ETX is included in the BCC. The DLE is excluded from the BCC.

```
      000000       .ASECT
      000000       .ENABL ABS
      160010       RXCSR=160010
      160012       TXCSR=160012
      160014       ERREG=160014
      160016       SECREG=160016
      004010       CHAR=4010               ;CHARACTER LENGTH
      002000       COUNT=2000
      002002       WENP=2002
      160015       DQREG=160015
      177764       TXWC=177764             ;TRANSMITT CHARACTER COUNT
      177764       RXWC=177764             ;RECEIVE LENGTH
      002400       RXBUF=2400              ;RECEIVE BUFFER
      002200       TXBUF=2200              ;TRANSMITT BUFFER
      013026       SYNC=13026              ;SYNC CHARACTER
                                           ;
                                           ;
                                           ;
      001000       .=1000
01000 105037       CLRB@#DQREG             ;SET POINTER TO 0
      160015
01004 012737       MOV#10,@#COUNT          ;SET TO COUNT # OF REGS TO CLEAR
      000010
      002000
01012 012737       MOV#10000,@#WENP        ;SET POINTER AND BIT 12 IN WENP
      010000
      002002
01020 013737    1$:MOV @#WENP,@#ERREG      ;PUT INTO ERREG
      002002
      160014
01026 005037       CLR@#SECREG
      160016
01032 062737       ADD#200,@#WENP
      000200
      002002
01040 005337       DEC@#COUNT              ;DECREMENT COUNT
      002000
01044 001365       BNE 1$                  ;BRANCH IF NOT DONE
01046 012705       MOV#17,R5               ;MOV ACOUNT INTO R5
      000017
01052 112737    2$:MOVB#10,@#DQREG         ;SEL CHAR ADDRESS
      000010
      160015
01060 005037       CLR@#SECREG             ;CLEAR
      160016
01064 112737       MOVB#14,@#DQREG         ;SELECT SEG ADDRESS
      000014
      160015
```

```
32 01072 005037       CLR@#SECREG         ;CLEAR
         160016
33 01076 062737       ADD#200,@#RXCSR     ;INCREMENT CD/SEQ POINTER
         000200
         160010
34 01104 005305       DEC R5              ;DEC COUNT
35 01106 001361       BNE 2$              ;GO BACK IF NOT DONE
36 01110 112737       MOVB#17,@#DQREG     ;LOAD POLY SELECTOR
         000017
         160015
37 01116 005037       CLR@#SECREG         ;CLEAR
         160016
38 01122 000000       HALT
39 01124 005037       CLR@#RXCSR              ;SET CHAR DET POINTER TO 0
         160010
40 01130 112737       MOVB#10,@#DQREG         ;SEL CHAR REG
         000010
         160015
41 01136 012737       MOV#001420,@#SECREG     ;LOAD DLE ETX
         001420
         160016
42 01144 112737       MOVB#14,@#DQREG         ;SEL SEQ
         000014
         160015
43 01152 012737       MOV#041024,@#SECREG     ;LOAD FUNCTION 2
         041024
         160016
44 01160 012737       MOV#400,@#RXCSR         ;SET POINTER TO 1
         000400
         160010
45 01166 112737       MOVB#10,@#DQREG         ;SEL CHAR REG
         000010
         160015
46 01174 012737       MOV#1000,@#SECREG       ;LOAD STX
         001000
         160016
47 01202 112737       MOVB#14,@#DQREG         ;SEL SEQ
         000014
         160015
48 01210 012737       MOV#10012,@#SECREG      ;LOAD FUNCTION 1
         010012
         160016
49 01216 112737       MOVB#17,@#DQREG         ;SEL POLY REG
         000017
         160015
50 01224 012737       MOV#102010,@#SECREG     ;LOAD CRC CCITT
         102010
         160016
51 01232 012737       MOV #33400,@#ERREG      ;SELECT TXSEC WC
         033400
         160014
52 01240 005037       CLR@#SECREG             ;AND SET EXIT T
         160016
53 01244 012737       MOV#5000,@#ERREG        ;SET SEC POINTER TO MISC REG
         005000
         160014
54 01252 012737       MOV#40,@#SECREG         ;CLEAR REGISTER
         000040
         160016
```

```
55 01260 012737         MOV#10000,@#ERREG      ;SELECT RXBA PRIMARY
         010000
         160014
56 01266 012737         MOV#RXBUF,@#SECREG     ;LOAD RXBA WITH RXBUF
         002400
         160016
57 01274 012737         MOV#10400,@#ERREG      ;SELECT RXCC REGISTER
         010400
         160014
58 01302 012737         MOV#RXWC,@#SECREG      ;LOAD RXCC WITH RXWC
         177764
         160016
59 01310 012737         MOV#11000,@#ERREG      ;SELECT TXBA PRIMARY
         011000
         160014
60 01316 012737         MOV#TXBUF,@#SECREG     ;LOAD TXBA WITH TXBUF
         002200
         160016
61 01324 012737         MOV#11400,@#ERREG      ;SELECT TXCC PRIMARY
         011400
         160014
62 01332 012737         MOV#TXWC,@#SECREG      ;LOAD TXCC WITH TXWC
         177764
         160016
63 01340 012737         MOV#4400,@#ERREG       ;SELECT SYNC REGISTER
         004400
         160014
64 01346 012737         MOV#SYNC,@#SECREG      ;LOAD SYNC REG WITH SYNC
         013026
         160016
65 01354 012737         MOV#5000,@#ERREG       ;SELECT MISC REGISTER
         005000
         160014
66 01362 012737         MOV#CHAR,@#SECREG      ;SELECT LENGTH AND TESTLOOP BIT
         004010
         160016
67 01370 005237         INC@#RXCSR             ;SET RX GO BIT IN RXCSR
         160010
68 01374 005237         INC@#TXCSR             ;SET TX GO BIT IN TXCSR
         160012
69 01400 032737      3$:BIT#200,@#RXCSR        ;WAIT FOR DONE BIT
         000200
         160010
70 01406 001774         BEQ 3$                 ;BRANCH IF DONE BIT NOT SET
71 01410 000000         HALT
72       002200         .=2200
73 02200    026         .BYTE 26,26,01,10,02,101,102,103,104,105,106,03
   02201    026
   02202    001
   02203    010
   02204    002
   02205    101
   02206    102
   02207    103
   02210    104
   02211    105
   02212    106
   02213    003
74       000001'        .END
```

```
SYMBOL TABLE

CHAR   = 004010         COUNT = 002000          DQREG = 160015
ERREG  = 160014         RXBUF = 002400          RXCSR = 160010
RXWC   = 177764         SECREG= 160016          SYNC  = 013026
TXBUF  = 002200         TXCSR = 160012          TXWC  = 177764
WENP   = 002002
. ABS.   002214     000
         000000     001
```

3.7 DQ11 DIAGNOSTICS

3.7.1 General Information

Seven diagnostic programs are used to check the DQ11. Each one is supported by a separate document that discusses its purpose and use. As a convenience to the user, this section describes the tests performed by each diagnostic. The code and name of each diagnostic is listed below.

1. MAINDEC-11-DZDQA-A-D – Basic Logic Tests, Part 1
2. MAINDEC-11-DZDQB-A-D – Basic Logic Tests, Part 2
3. MAINDEC-11-DZDQC-A-D – Interrupt Logic Tests
4. MAINDEC-11-DZDQD-A-D – Receiver and Transmitter Tests
5. MAINDEC-11-DZDQE-A-D – RX, TX and MISC Register Tests and BCC Tests
6. MAINDEC-11-DZDQF-A-D – Sequence Register Tests
7. MAINDEC-11-DZDQG-A-D – DQ11 Trial Program (Parameter Input)

3.7.1.1 DZDQA-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Address selection test for Receive CSR
3	Address selection test for Transmit CSR
4	Address selection test for REG/ERR CSR
5	Address selection test for secondary register
6	Address test for primary registers. Each primary register is loaded with a different number and read out to verify that the correct register was addressed.
7	RX CSR bit 1 read/write test
10–24	RX CSR bits 3–15 read/write test
25–33	TX CSR bits 3–9 read/write test
34	TX CSR bit 15 read/write test
35	Test for all 0s in TX CSR high byte if Data Set Control Module M7815 is not installed.
36–51	REG/ERR CSR bits 0–11 read/write test
52	Secondary register addressing test. (With or without character detect and BCC options installed.)
53	Secondary register addressing test. (With character detect option installed.)
54	Secondary register addressing test. (With BCC option installed.)
55–74	SEQ register bits 0–15 read/write test
75	MISC register bit 0 read/write test
76	MISC register bit 1 read/write test
77	MISC register bit 3 read/write test
100–105	MISC register bits 6–11 read/write test
106	MISC register bit 15 read/write test
107–126	POLY register bits 0–15 read/write test

3.7.1.2 DZDQB-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Memory extension write enable test. Set 14, 13 WRITE EN bit. Select bus address memory and clear it. Verify that 14,13 WRITE EN bit is cleared.
3	Memory extension bits read/write test. Read MEM EXT bits with 14, 13 WRITE EN bit cleared. Attempt to change MEM EXT bits and verify that no change occurs.
4	Memory extension bits read/write test. Read MEM EXT bits with 14, 13 WRITE EN bit set. Attempt to change MEM EXT bits and verify that change occurs.
5	Bus address memory extension test. Load each bus address with a different number and verify.
6	Bus address and character count memory test. Put a 0 into each CC/BA word and verify.
7	Bus address and character count memory test. Load 177777 into each CC/BA word and verify.
10	Bus address and character count memory test. Load 125252 into each CC/BA word and verify.
11	Bus address and character count memory test. Load 52525 into each CC/BA word and verify.
12	Bus address memory extension data test. Load 40 into memory extension words in CC/BA memory and verify.
13	Bus address memory extension data test. Load 100 into memory extension words in CC/BA memory and verify.
14	Bus address memory extension data test. Load 140 into memory extension words in CC/BA memory and verify.
15	Character memory addressing test. Each CHAR MEM word is loaded with its address and read out to verify that the correct word was addressed.
16	Sequence memory addressing test. Each SEQ MEM word is loaded with its address and read out to verify that the correct word was addressed.
17	Character memory test. Load 0 into each CHAR MEM word and verify.
20	Character memory test. Load 177777 into each CHAR MEM word and verify.
21	Character memory test. Load 125252 into each CHAR MEM word and verify.
22	Character memory test. Load 52525 into each CHAR MEM word and verify.
23	Sequence memory test. Load 0 into each SEQ MEM word and verify.
24	Sequence memory test. Load 177777 into each SEQ MEM word and verify.
25	Sequence memory test. Load 125252 into each SEQ MEM word and verify.
26	Sequence memory test. Load 52525 into each SEQ MEM word and verify.
27	Receive control and status register master clear test (Data Set Control Module M7815 installed). Set all RX CSR read/write bits. Issue MASTER CLEAR and verify that RX CSR is cleared.
30	Receive control and status register master clear test (Data Set Control Module M7815 not installed). Set all RX CSR read/write bits. Issue MASTER CLEAR and verify that RX CSR is cleared.
31	Transmit control and status register master clear test (Data Set Control Module M7815 installed). Set all TX CSR read/write bits. Issue MASTER CLEAR and verify that TX CSR is cleared.

Test No. (Octal)	Function
32	Transmit control and status register master clear test (Data Set Control Module M7815 not installed). Set all TX CSR read/write bits. Issue MASTER CLEAR and verify that TX CSR is cleared.
33	REG/ERR register master clear test. Set all REG/ERR read/write bits. Issue MASTER CLEAR and verify that REG/ERR register is cleared.
34	SYNC register master clear test. Set all bits in SYNC register. Issue MASTER CLEAR and verify that SYNC register is cleared.
35	MISC register master clear test. Set all MISC register read/write bits. Issue MASTER CLEAR and verify that MISC register is cleared.
36	POLY register master clear test. Set all bits in the POLY register. Issue MASTER CLEAR and verify that POLY register is cleared.

3.7.1.3 DZDQC-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Step mode verification and clock loss test
3	Test loop verification
4	Character interrupt enable (CHAR IE) test
5	Receive done interrupt enable (RX DONE IE) test
6	Error interrupt enable (ERROR IE) test
7	Data set interrupt enable (DATA SET IE) test
10	Transmit done interrupt enable (TX DONE IE) test
11	Receive done secondary interrupt flag (RX DONE S INTR) test
12	Receive done primary interrupt flag (RX DONE P INTR) test
13	Transmit done secondary interrupt flag (TX DONE S INTR) test
14	Transmit done primary interrupt flag (TX DONE P INTR) test
15	Data set interrupt flag (DATA SET INTR) test
16	Transmit clock loss interrupt flag (TX CLOCK LOSS INTR) test
17	Receive clock loss interrupt flag (RX CLOCK LOSS INTR) test
20	Transmit latency interrupt flag (TX LATENCY INTR) test
21	Receive latency interrupt flag (RX LATENCY INTR) test
22	Transmit non-existent memory interrupt flag (TX NON-EX MEM INTR) test
23	Receive non-existent memory interrupt flag (RX NON-EX MEM INTR) test
24	Receive BCC error interrupt flag (RX BCC ERROR INTR) test
25	Receive VRC error interrupt flag (RX VRC ERROR INTR) test
26	Verify that an interrupt occurs when CHAR DET INTR and CHAR IE bits are set.
27	Verify that an interrupt occurs when RX DONE IE and RX DONE S INTR bits are set.
30	Verify that an interrupt occurs when RX DONE IE and RX DONE P INTR bits are set.
31	Verify that an interrupt occurs when TX DONE IE and TX DONE S INTR bits are set.

Test No. (Octal)	Function
32	Verify that an interrupt occurs when TX DONE IE and TX DONE P INTR bits are set.
33	Verify that an interrupt occurs when ERR IE and TX CLOCK LOSS INTR bits are set.
34	Verify that an interrupt occurs when ERR IE and RX CLOCK LOSS INTR bits are set.
35	Verify that an interrupt occurs when ERR IE and TX LATENCY INTR bits are set.
36	Verify that an interrupt occurs when ERR IE and RX LATENCY INTR bits are set.
37	Verify that an interrupt occurs when ERR IE and TX NON-EX MEM INTR bits are set.
40	Verify that an interrupt occurs when ERR IE and RX NON-EX MEM INTR bits are set.
41	Verify that an interrupt occurs when ERR IE and RX BCC ERROR INTR bits are set.
42	Verify that an interrupt occurs when ERR IE and RX VRC ERROR INTR bits are set.
43	Verify that the receiver interrupts before the transmitter when they are enabled simultaneously.
44	Verify that the transmitter interrupts only once when it is enabled.
45	Verify that the receiver interrupts only once when it is enabled.
46	Verify that transmitter interrupts at priority level 7.
47	Verify that transmitter interrupts at priority level 6.
50	Verify that transmitter interrupts at priority level 5.
51	Verify that transmitter interrupts at priority level 4.
52	Verify that an interrupt occurs when DATA SET IE and DATA SET INTR bits are set.
53	Receiver basic NPR logic test using primary BA/CC registers.
54	Transmitter basic NPR logic test using primary BA/CC registers.
55	Receiver basic NPR logic test using secondary BA/CC registers.
56	Transmitter basic NPR logic test using secondary BA/CC registers.
57	Receiver non-existent memory test using primary BA/CC registers.
60	Transmitter non-existent memory test using primary BA/CC registers.
61	Receiver P/S master clear test.
62	Transmitter P/S master clear test.
63	Transmitter NPR data test (step mode).

3.7.1.4 DZDQD-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Verify that TX ACTIVE can be set and then cleared by MASTER CLEAR.
3	Transmit one 8-bit character and verify that BA and CC registers increment by 1.
4–22	Transmit a character of each length from 2–16 bits and verify that the data out line goes to a MARK state when transmission is finished.
23	Transmitter idle test. Verify idle operation (transmission of sync characters).

Test No. (Octal)	Function
24	Transmitter data reliability test (for characters up to 8 bits in length).
25	Transmitter data reliability test (for characters from 9–16 bits in length).
26–44	Receiver character length test (from 2–16 bits per character).
45	Verify that SYNC 1 and SYNC 2 set when RX ACTIVE is set and that they can be cleared by MASTER CLEAR.
46	Sync test using an 8-bit character. Verify that RX ACTIVE, SYNC 1, and SYNC 2 all set properly.
47	Sync test using a 16-bit character. Verify that RX ACTIVE, SYNC 1, and SYNC 2 all set properly.
50	Verify that RX CC and RX BA registers increment properly using an odd character count.
51	Verify that RX CC and RX BA registers increment properly using an even character count.
52	Receiver data reliability test (for characters 0–16 bits in length).
53	Receiver parity error test.
54	Receiver half-duplex test.
55	Transmitter and receiver data reliability test using maximum data transfer rate with a 400 character burst.
56	Test of hard-wired character detection (M7817 module not installed).

3.7.1.5 DZDQE-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Test of data reliability through cable and level converters.
3	Test of receiver STRIP SYNC function
4	Memory transfer tests
5	Test of ENTER T and EXIT T functions
6	Test to force an RX BCC error
7	TX BCC test using polynomial represented by 177777.
10	RX BCC test using polynomial represented by 177777.
11	Test of TX BCC and RX BCC using CRC-16 polynomial.
12	Test of TX BCC and RX BCC using CRC-12 polynomial.
13	Test of TX BCC and RX BCC using CRC/CCITT polynomial.
14	Test of TX BCC and RX BCC using LRC-8 polynomial.
15	Test of TX BCC and RX BCC using LRC-16 polynomial.
16	Test of TX BCC and RX BCC using CRC-16 polynomial and using idle mode to get into transparency.
17	Test of TX BCC and RX BCC using polynomial represented by 177777 and using idle mode to get into transparency.

Test No. (Octal)	Function
20	Test of TX BCC and RX BCC with all polynomial representations between 000000 and 177777.
21	Test of MISC register bit 06 (POLY 16–23).

3.7.1.6 DZDQF-A-D Tests

Test No. (Octal)	Function
1	Start-up
2	Exercises RX and TX interrupts, VRC and ENTER T/EXIT T if M7816 module is installed.
3	Verify that every character from 0–377 can be detected in character detect address 00.
4	Verify that every character from 400–177400 can be detected in character detect address 00.
5–24	Verify that character 255 can be detected in each of the 16 character detect addresses.
25	Test function of SEQ bit 1 (SET RX/TX TRANSPARENT MODE).
26	Test function of SEQ bit 2 (CLEAR RX TRANSPARENT MODE).
27	Test function of SEQ bit 3 (CLEAR/START TX/RX BCC).
30	Test function of SEQ bit 6 (CLEAR RX ACTIVE).
31	Test function of SEQ bit 7 (RX/TX CLEAR GO/SET DONE).
32	Test function of SEQ bit 8 (RX CHAR STRIP).
33	Test function of SEQ bit 10 (TX PAD).
34	Test function of SEQ bit 11 (RX BCC EXCLUDE).
35	Test of transmitter transparent text mode.
36	Verify that the transmitter exits the transparent mode via EXIT T after it has entered transparency via ENTER T.
37	Verify that the RX STRIP SYNC function is inhibited in the transparent mode.
40	Verify that the RX CHAR STRIP function (SEQ bit 8) strips characters from core but not from the BCC.
41–43	Test function of SEQ bits 4 and 5 (RX/TX BCC TEST/APPEND) for 1, 2 and 3 BCCs.
44	Multiple function tests.

CHAPTER 4

DETAILED DESCRIPTION

4.1 INTRODUCTION

This chapter provides a detailed description of the DQ11 logic. It is divided into six major sections which represent the six DQ11 modules.

Module	Title	Paragraph
M7818	Hard-Wired Character Detect and NPR Control	4.2
M7815	Data Set Control	4.3
M7812	Bus Selectors Control/Status Registers and Shift Registers	4.4
M7813	Character Count Registers, Bus Address Registers and Shift Register Control	4.5
M7816	AB Selectors and BCC Control	4.6
M7817	Character Detection and Sequence Control	4.7

Further division within modules is by functionally separate logic circuits. The discussion of each circuit consists of a functional description related to a block diagram and a detailed description related to the circuit schematic that appears in the DQ11 print set which is supplied as a separately bound volume. The revision level of the circuit schematic at the time that the description was written is also included. Additional illustrations are used in the detailed descriptions to supplement the text.

4.2 M7818 MODULE (HARD-WIRED CHARACTER DETECT AND NPR CONTROL)

4.2.1 Introduction

The M7818 module is a double height, extended length, module that contains two functionally separate logic circuits – hard-wired character detection logic and NPR control logic.

4.2.2 Hard-Wired Character Detection Logic

4.2.2.1 Functional Description – A simplified block diagram of the hard-wired character detection logic is shown in Figure 4-1. The character to be detected is set into the bit switches of the detectors and the associated enabling switches are closed. Switch SW39 allows a sync character to be detected. (The specific rules for setting the switches are discussed in a subsequent paragraph.) When the received character, as represented by the output of the received data buffer register (D4-5 RD0H–15H), matches the switch selected character, a high is sent to the D input of the associated flip-flop. If the receiver is framed (D5-7 RX ACTIVE (1) H is true), the end of a character is detected (D5-7 TEST JUMPER MATCH L is true), the transparent mode is not enabled (D9-6 DIS RX TRANSFER PULSE L is false), and switch SW40 is ON, the flip-flop is clocked. The output of the flip-flop generates a signal (D6-1 CD 8H, 9H, 10H or 11H) at the associated output gate that represents bit 8, 9, 10, or 11 of the receiver control and status register. The signal that clocks the flip-flop is also sent to the pulse stretcher to increase its period. This signal becomes D6-11 → CHAR INTR L at the associated output gate and is sent to bit 15 of the RX CSR as a prerequisite for generating an interrupt. The output gates are enabled when signal D8-6 BB IT L is false. This interlock signal is false as long as the M7817 module, which contains the programmable character detection logic, is not plugged in.

Selector Switches

Manually operated switches are used to select up to three 16-bit characters that set flags in the receiver control and status register (RX CSR). Each character uses two dual in-line switch packages containing eight switches each (Figure 4-2). For example, character 0 uses packages S1 and S4. Package S1 contains switches SW1–SW8 that correspond to bits 0–7 (low byte) of character 0. Package S4 contains switches SW25–SW32 that correspond to bits 8–15 (high byte) of character 0. Switches SW33 and SW38 of package S5 are used to enable the low and high bytes of character 0 in the character detection logic. Switch SW39 in package S5 allows a detected sync character to be enabled.

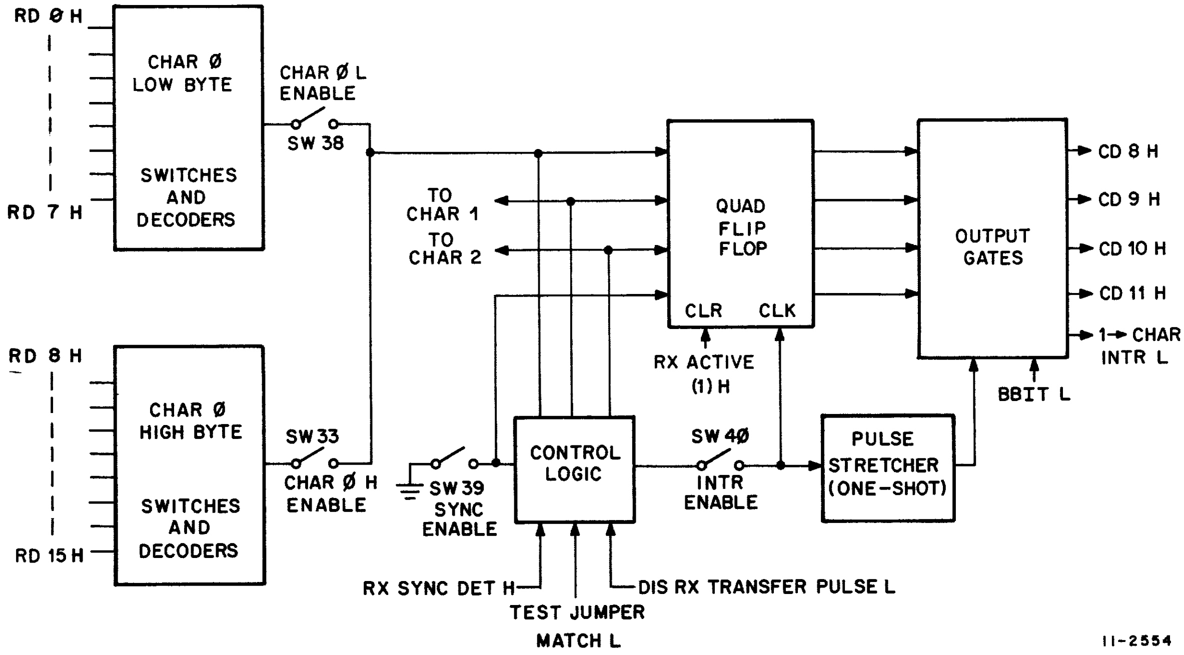


Figure 4-1 Block Diagram of Hard Wired Character Detection Logic

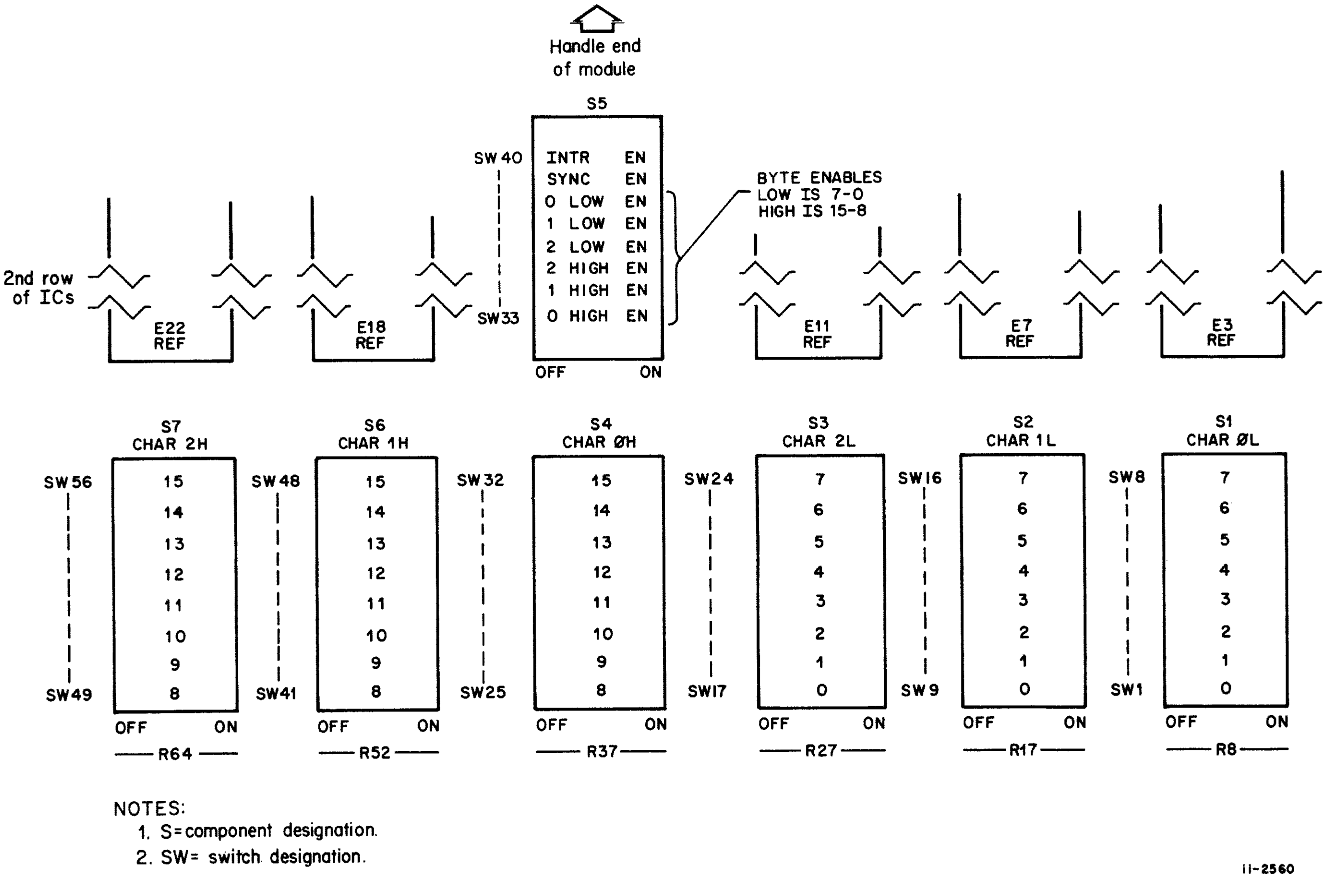


Figure 4-2 Physical Layout of Character Detection Switches

Switch SW40 in package S5 allows any detected character or sync character to set a flag and generate an interrupt if other prerequisites have been satisfied. Table 4-1 lists the switches and their functions.

The following rules must be used when setting the switches.

1. For character detect switches, a 1 is detected with the switch OFF and a 0 is detected with the switch ON. These levels are with respect to the input of the character detection logic.
2. For characters of 8 bits or less, use bit selections for high byte (bits 8–15). Justify character to the least significant bit. All unused bits must be set to 0. Use enabling switch for high byte.
3. For characters from 9–16 bits in length, use bit selections for both high and low bytes. Justify character to the least significant bit. All unused bits must be set to 0. Use enabling switches for both high and low bytes.
4. Three separate characters can be selected. If less than three are required, repeat a used character until all three selections are used. For example, if only two characters are desired, one of them must be duplicated for the third selection. If only one character is desired, all three selections must be identical.

Table 4-1
Function of Character Detection Switches

Package Number	Switch Number	Function
S1	SW1–SW8	Determines low byte of character 0
S2	SW9–SW16	Determines low byte of character 1
S3	SW17–SW24	Determines low byte of character 2
S4	SW25–SW32	Determines high byte of character 0
S6	SW41–SW48	Determines high byte of character 1
S7	SW49–SW56	Determines high byte of character 2
S5	SW33-SW40	SW33 enables high byte of character 0 SW34 enables high byte of character 1 SW35 enables high byte of character 2 SW36 enables low byte of character 2 SW37 enables low byte of character 1 SW38 enables low byte of character 0 SW39 enables a sync compare SW40 allows character 0, 1, 2 or sync to set a flag and generate an interrupt

Notes: 1. For S1, S2, S3, S4, S6 and S7, a 1 is detected with switch OFF and a 0 is detected with switch ON.
2. For S5, selected function is enabled with switch ON.

Two typical examples are shown below:

Example 1: It is desired to detect a single 6-bit character 110111 (LSB).

According to the rules, the character must be justified to the least significant bit of the high byte with unused bits set to 0 and all three selections (character 0, 1 and 2) must be identical. The corresponding high byte enabling switches must be set to the ON position. The format is shown for character 0 and is applicable for characters 1 and 2 also. The low bytes of characters 0, 1 and 2 are not used and their respective enabling switches must be set to the OFF position.

	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	Switch position
Character 0 H	32	31	30	29	28	27	26	25	Switch number
(Package S4)	0	0	1	1	0	1	1	1	Binary value
	15	14	13	12	11	10	9	8	Bit position
								LSB	

Character 1 H (S6) and character 2 H (S7) are set up the same as that shown for character 0 H (S4). The enabling switches (SW33, SW34 and SW35) for these three packages are set to the ON position. The interrupt enabling switch (SW40) must be set to the ON position.

Example 2: It is desired to detect an 8-bit character 10001010 (LSB) for character 0 and a 12-bit character 110000101100 (LSB) for character 1.

The 8-bit character must be justified to the least significant bit of the high byte for character 0 as shown below:

	OFF	ON	ON	ON	OFF	ON	OFF	ON	Switch position
Character 0 H	32	31	30	29	28	27	26	25	Switch number
(Package S4)	1	0	0	0	1	0	1	0	Binary number
	15	14	13	12	11	10	9	8	Bit position
								LSB	

The enabling switch (SW33) for character 0 H is set to the ON position. The corresponding low byte (character 0 L) is not used and its enabling switch (SW38) can be set to the ON or OFF position.

The 12-bit character must be justified to the least significant bit of the low byte for character 1. The four least significant bits of the high byte for character 1 are also used as shown below:

Character 1 H (Package S6)								Character 1 L (Package S2)								
ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	ON	Switch position
48	47	46	45	44	43	42	41	16	15	14	13	12	11	10	9	Switch number
0	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	Binary number
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit position

The enabling switches (SW34 and SW37) for characters 1 H and 1 L must be set to the ON position. Characters 2 H and 2 L must be set identically to characters 1 H and 1 L and their associated enabling switches (SW35 and SW36) must be set to the ON position.

The interrupt enabling switch (SW40) must be set to the ON position. In this example, the 8-bit character can be duplicated rather than the 12-bit character.

4.2.2.2 Detailed Logic Description – The circuit schematic for the hard-wired character detection circuit is contained in drawing D-CS-M7818-0-1 (Rev C) sheet 3 which is designated D6-1.

Comparator Logic

The bit selector switches are used to define a character that is compared to the output of the received data buffer register (D4-5 RD 0 H–15 H). The comparison is on a bit basis, using 16 exclusive-NOR gates (type 8242) whose outputs are wire-ORed to provide a high signal when a successful comparison has been made. Figure 4-3 shows four bits for character 2. The truth table for the 8242 shows that when both inputs are high or low, the output is high.

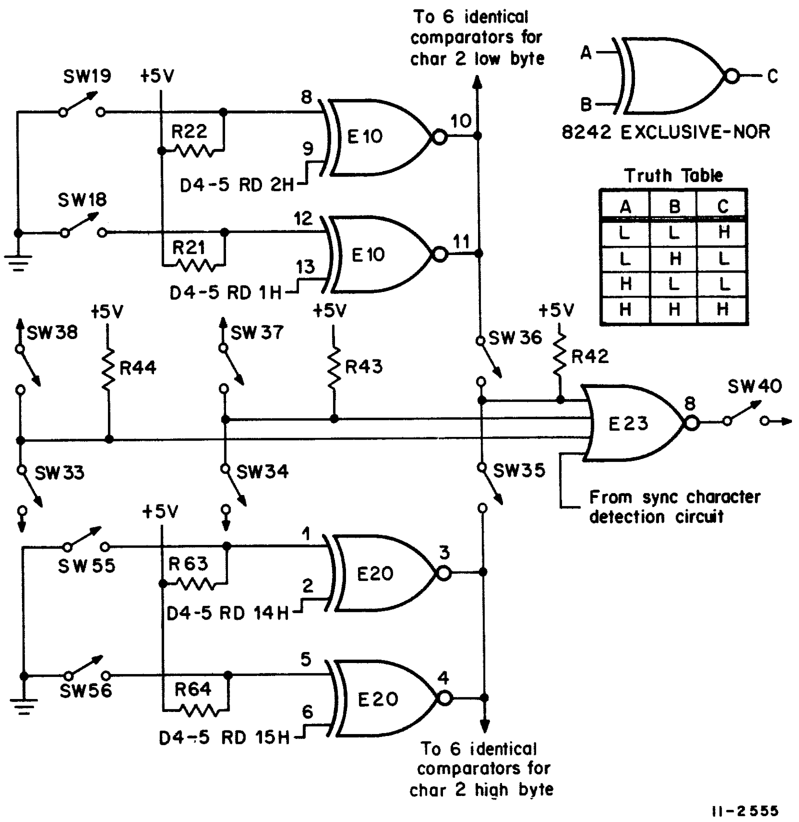
Assume that it is desired to detect a 1 on bit 14 and a 0 on bit 15. Switch SW55 for bit 14 should be open (OFF). The +5 V via R63 puts a high (logical 1) on pin 1 of E20. The comparison is made when D4-5 RD14 H is high. Switch SW56 for bit 15 should be closed (ON). The +5 V is dropped to ground through the switch and puts a low (logical 0) on pin 5 of E20. The comparison is made when D4-5 RD15 H is low.

Each character is arranged in two 8-bit bytes. The outputs of the 8 comparators in each byte are connected together to provide a single output. Each byte can be connected to the detection control logic by an enabling switch.

Using character 2 as an example (Figure 4-3), switch SW36 connects the low byte to E23 pin 9 and switch SW35 connects the high byte to the same pin. If a 9–16-bit character is selected, both switches (SW35 and SW36) are closed. For each character, the common output of all 16 8242s is connected to +5 V through a pull-up resistor. This output also goes to an input of E23 which is a 4-input NOR gate. A high signal on this line indicates a match. The 8242 has a bare collector which facilitates multiple bit comparisons. The output of the 8242 is taken from the collector and the emitter of this output transistor and is connected to ground in the IC package (Figure 4-4). When a match is made, all 8242 output transistors are turned off and there is no path to ground for the +5 V; therefore, the output to E23 is held high. When a match is not made, at least one 8242 output transistor is turned on and the +5 V is dropped to ground; therefore, the output to E23 is held low. If only one character is set up for detection and the other two are not set up identically, two undesirable possibilities arise. First, if the two non-desired characters have their enabling switches closed, an erroneous detection is made if a received character matches the one randomly set in either of the non-desired characters. Second, if either non-desired character has its enabling switches open, a high signal is always present on the associated output line which falsely indicates a match.

Control Logic

Figure 4-5 shows the control logic. The outputs of the three character comparators and the sync character comparator are sent to the D inputs of quad flip-flop E18. They are also sent to 4-input NOR gate E23.

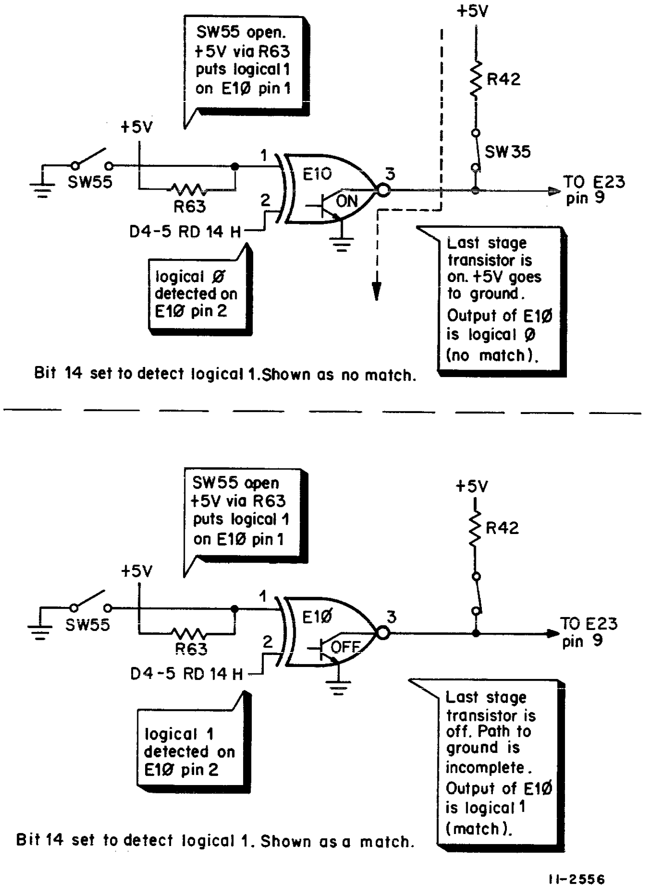


A	B	C
L	L	H
L	H	L
H	L	L
H	H	H

Figure 4-3 Typical Comparator Circuit

The sync character comparator consists of switch SW39 and two 2-input NOR gates (E22). When it is desired to detect a sync character, SW39 is closed (ON position). The +5 V, via R38, is connected to ground through the switch and holds input pin 12 of the E22 low. If a sync character is recognized, signal D4-7 RX SYNC DET H is true. It is inverted by E22 pins 8 and 10 and is sent as a low signal to the other input (pin 11) of E22. The output (pin 13) of this gate goes high and is sent to E23 and quad flip-flop E18.

If it is desired to set a flag in the Receiver Control and Status Register (RX CSR) as the result of a detected character, switch SW40 is closed. Any high at the input of E23 represents a detected character and drives the output (pin 8) of E23 low. This signal passes through SW40 to pins 2 and 4 of E23. Two other conditions must be satisfied to qualify this gate. The first condition is that the receiver must be framed. The end of a character frame is indicated when D5-7 TEST JUMPER MATCH L goes low. This signal is sent to pin 1 of E23. The second condition requires verification that transmission is not in the transparent mode because character detection is not applicable in this mode. Signal D9-6 DIS RX TRANSFER PULSE L is high when the transparent mode is not enabled. This signal is inverted by E22 and sent to pin 5 of E23. When all four inputs of E23 are low, its output (pin 6) goes high. This positive transition clocks all four flip-flops in the E18 package. The 0 output of each flip-flop is sent to one input of a 2-input NAND gate (E19). These gates are shown as logically equivalent, negated-input OR gates; they are enabled when D8-6 BB IT L is high. This occurs when the programmable character detection option is not installed (module M7817 not installed). When this module is installed, interlock circuit D8-6 BB IT L is asserted and the hard-wired character detection logic is inhibited. If a character is detected, the 0 output of the associated flip-flop is inverted by the output gate to generate D6-1 CD X H, where X is 8 for character 0, 9 for character 1, 10 for character 2, and 11 for sync character. These signals (D6-1 CD 8 H, 9 H, 10 H, and 11 H) are bits 8, 9, 10, and 11 of the RX CSR and are sent to the bus selection multiplexers on the M7812 module. Another qualifying signal (D5-7 RX ACTIVE (1) H) is sent to the clear input (pin 1) of E18. If the receiver is not framed, this signal is low and all four flip-flops in E18 are directly cleared which prevents the character detection flags from being asserted.



SW55 open. +5V via R63 puts logical 1 on E1Ø pin 1

logical Ø detected on E1Ø pin 2

Last stage transistor is on. +5V goes to ground. Output of E1Ø is logical Ø (no match).

Bit 14 set to detect logical 1. Shown as no match.

SW55 open +5V via R63 puts logical 1 on E1Ø pin 1

logical 1 detected on E1Ø pin 2

Last stage transistor is off. Path to ground is incomplete. Output of E1Ø is logical 1 (match).

Bit 14 set to detect logical 1. Shown as a match.

Figure 4-4 Operation of 8242 Comparator

The positive-going edge from E23 pin 6 that clocks E18 also triggers one-shot E4 that generates a positive pulse of approximately 500 ns. This pulse is inverted by output gate E15 to assert D6-1 1 → CHAR INTR L. This low pulse is applied to the direct-preset input of the flip-flop that represents bit 15 (CHAR INTR) of the RX CSR (M7812 module print D4-4). This bit and RX CSR bit 4 (CHAR IE) must be set if the detected character is to produce an interrupt. One-shot E4 is used to provide a long enough pulse to prevent any Unibus read/write cycle from changing the state of RX CSR bit 15 during the period required to qualify the interrupt control logic.

4.2.3 NPR Control Logic

4.2.3.1 Functional Description – A simplified block diagram of the NPR logic and associated logic is shown in Figure 4-6. The associated logic is discussed briefly because it is not possible to describe the NPR adequately without mentioning its interrelation with other logic concerned with the NPR cycle.

The NPR control logic serves the same purpose as the M796 Unibus Master Control Module. In response to a signal from the M7821 Interrupt Module, the NPR control logic allows the DQ11 to become bus master and perform a DATI or DATO operation on the PDP-11 memory. The EQ11 takes a character from memory (DATI) for transmission or it sends a received character to memory (DATO) for storage.

The sequence of operation is described below.

1. When either a transmit operation or a receive operation desires a character transfer, an Non-Processor Request (NPR) is initiated.

2. The bus address control logic on the M7813 module generates RX CYCLE H which is high if it is a receive operation and is low if it is a transmit operation. The basic function of signal RX CYCLE H is to generate the Transmitter Buffer Register Load signal (LD TX BUF (1) H), if it is a transmit operation.

3. Also, the bus address control logic generates NPR RQ H and NPR EN (1) H which are sent to the M7821 Interrupt Module to assert BUS NPR L.

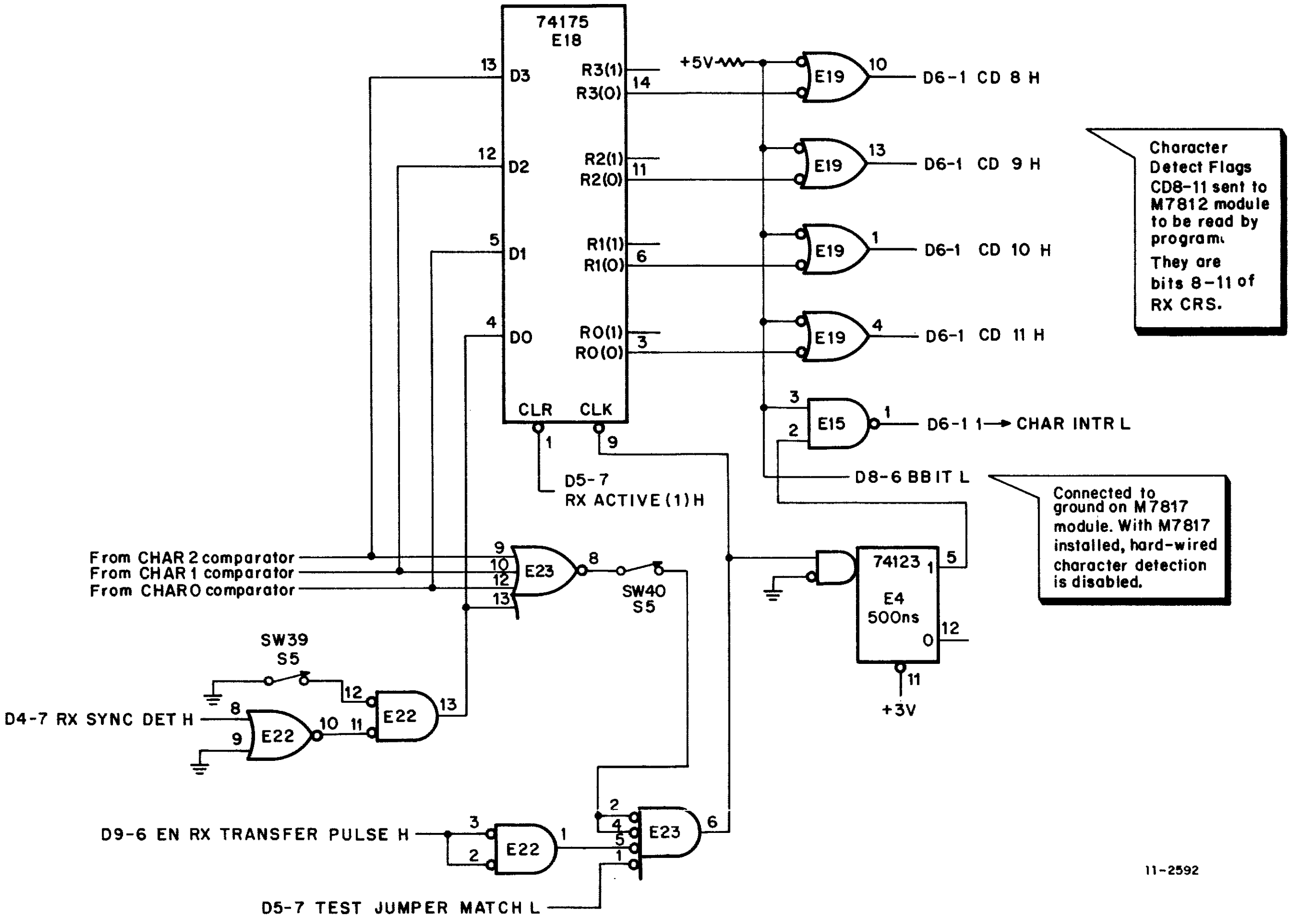
4. If BUS SACK L is clear on the Unibus, the processor asserts grant signal BUS NPG IN H. At the M7821, this signal clears BUS NPG OUT H which stops the bus request at this device (DQ11). It also asserts BUS SACK L and clears bus request signal BUS NPR L.

5. The processor receives BUS SACK L and drops grant signal BUS NPG IN H. When the current bus master completes a data transfer, it clears BUS BBSY L. Signals BUS MSYN L and BUS SSYN L are also cleared. Under these conditions, the M7821 asserts BUS BBSY L indicating that the DQ11 is now bus master.

6. Simultaneously with the assertion of BUS BBSY L, the M7821 asserts MASTER A L which is sent to the NPR control logic to initiate a DATI or DATO bus transaction.

7. The selection of a DATI or DATO operation is made by selecting the state of Unibus control lines C1 and C0. The selection is performed in the M7813 bus address control logic.

   Transmit operation requires DATI (C1=0, C0=0)
   Receive operation requires DATO (C1=1, C0=0)



Character Detect Flags CD8-11 sent to M7812 module to be read by program. They are bits 8-11 of RX CRS.

Connected to ground on M7817 module. With M7817 installed, hard-wired character detection is disabled.

Figure 4-5 Character Detect Control Logic

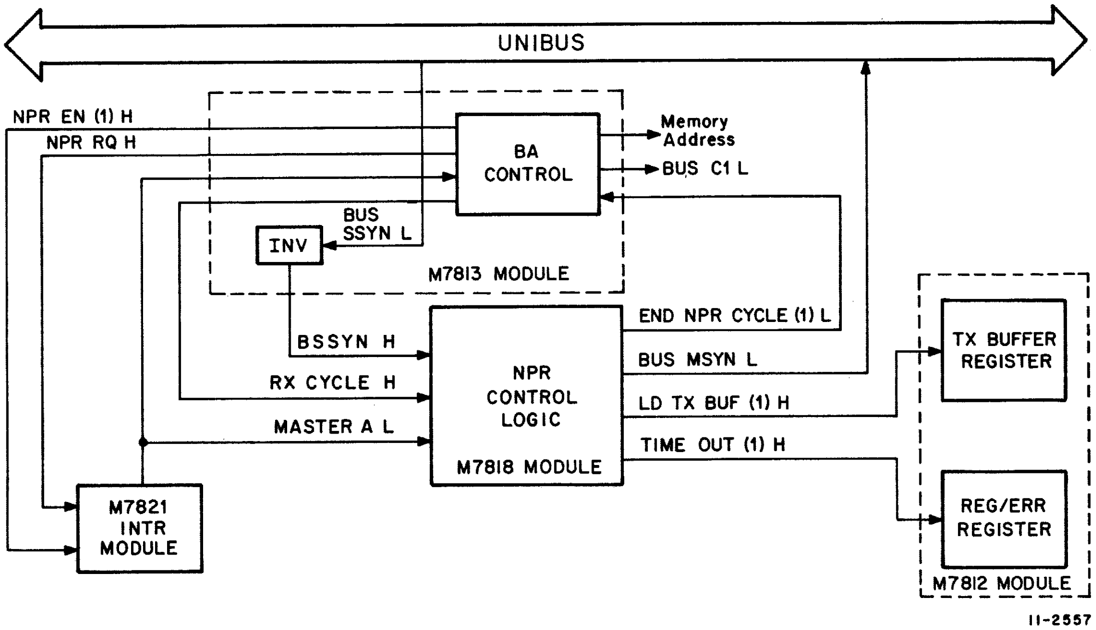


Figure 4-6 Block Diagram of NPR Control and Associated Logic

8. Signal MASTER A L is also sent to the M7813 bus address logic to place the selected memory address on the Unibus address lines.

9. Approximately 150 ns after MASTER A L is asserted, the NPR control logic asserts BUS MSYN L.

10. The PDP-11 memory has already decoded the address and when it receives BUS MSYN L, it places the character on the Unibus data lines (DATI) or accepts the character from the Unibus data lines (DATO) and after a short delay, asserts BUS SSYN L.

11. The M7813 bus address control logic receives BUS SSYN L and sends it to the NPR control logic as B SSYN H to start the sequence that terminates the NPR cycle.

12. At about the same time, the NPR control logic drives signal LD TX BUF (1) H high to load the transmitter buffer register, if a transmit operation requested the NPR.

13. After receiving B SSYN H, the NPR control logic clears BUS MSYN L.

14. When the memory receives the cleared BUS MSYN L signal, it clears BUS SSYN L.

15. The NPR control logic continues the termination sequence by asserting END NPR CYCLE (1) L which is sent to the M7813 bus address control logic. This signal clears NPR EN (1) H which inhibits the issuing of another NPR until NPR EN (1) H is asserted again.

If the DQ11 addresses non-existent memory, BUS SSYN L is not asserted by the memory. If BUS SSYN L is not asserted 20 μs after BUS MSYN L is asserted, the NPR control logic terminates the NPR request normally. Normal termination of the NPR cycle, even though the DATI or DATO was not completed, is a requirement because aborting an NPR cycle is not allowed.

4.2.3.2 Detailed Logic Description – The circuit schematic for the NPR control logic is shown in drawing D-CS-M7818-0-1 (Rev C) sheet 4, which is designated D6-2. Figure 4-7 shows a simplified logic and timing diagram for the NPR control logic.

Normal Operational Sequence

The normal sequence describes how the logic performs during an NPR cycle that terminates normally.

1. Prior to starting the operation, D3-1 MASTER A L is not asserted. This produces a low at E3 pin 1 that directly clears the following elements.

   MSYN flip-flop
   END CYCLE flip-flop
   BUF flip-flop
   TIME OUT flip-flop
   MSYN TIMER one-shot

   As a result, the following conditions exist.

   a. The low from the 1 output (pin 9) of the MSYN flip-flop is sent to three places:

      (1) The D-input of the END CYCLE flip-flop

      (2) The D-input of the TIME OUT flip-flop

      (3) The input (pin 2) of the MSYN TIMER one-shot

   b. The high from the 0 output (pin 8) of the END CYCLE flip-flop is sent to two places:

      (1) The input (pin 10) of one-shot E12 that generates D6-2 END NPR CYCLE (1) L. At this time, E12 is at rest so D6-2 END NPR CYCLE (1) L is not true.

      (2) The input (pin 9) of the CK2 one-shot which inhibits its operation.

2. Assume that a transmit operation requested the NPR transaction. The BA control logic on module M7813 drives D5-3 RX CYCLE H low. This signal, via the three E3 NOR gates, puts a low on the K input of the MSYN flip-flop and a low on the input of the BUF flip-flop.

3. The MSYN TIMER one-shot is at rest and the low from its 1 output (pin 13), via gate E22, puts a high on the J input of the MSYN flip-flop.

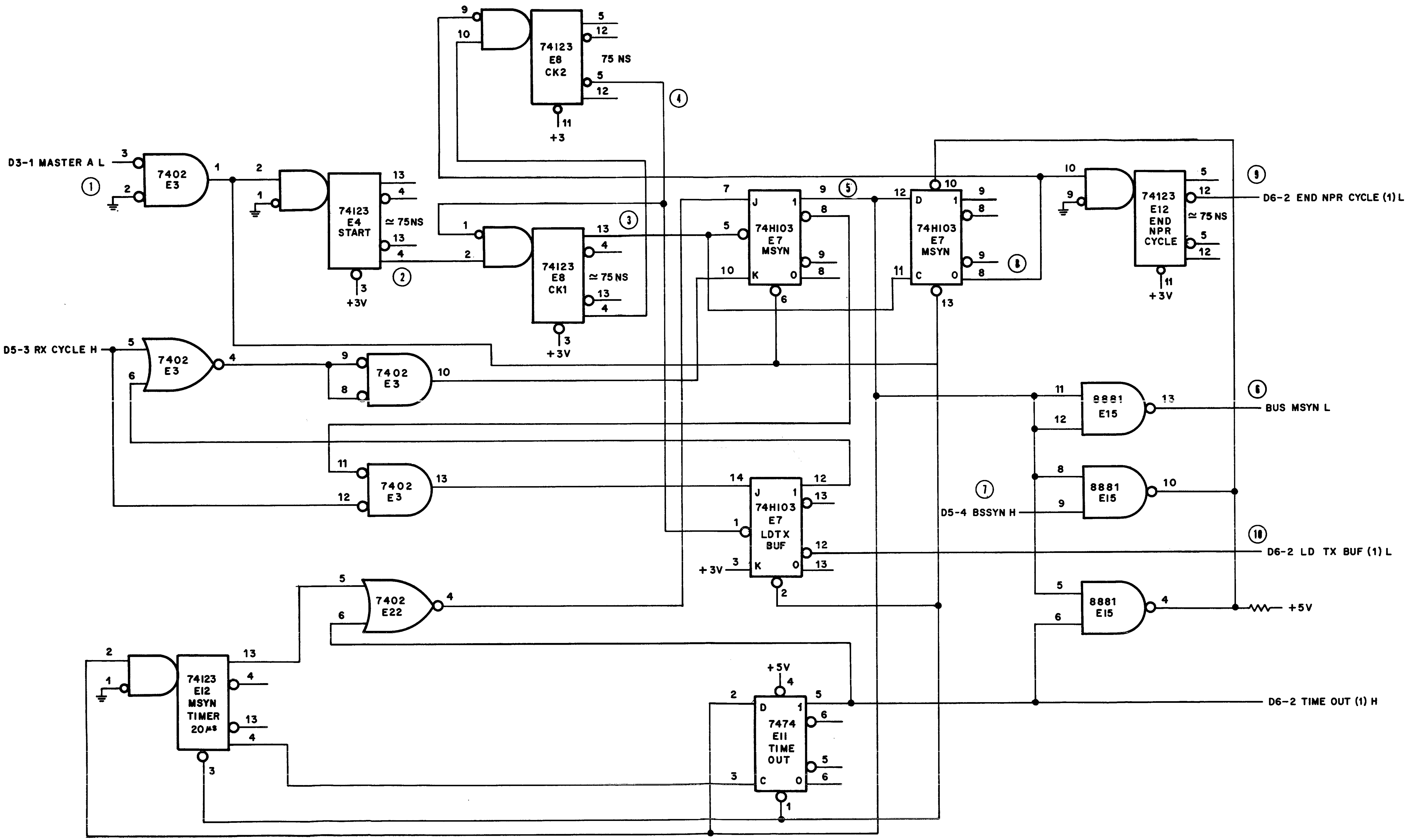
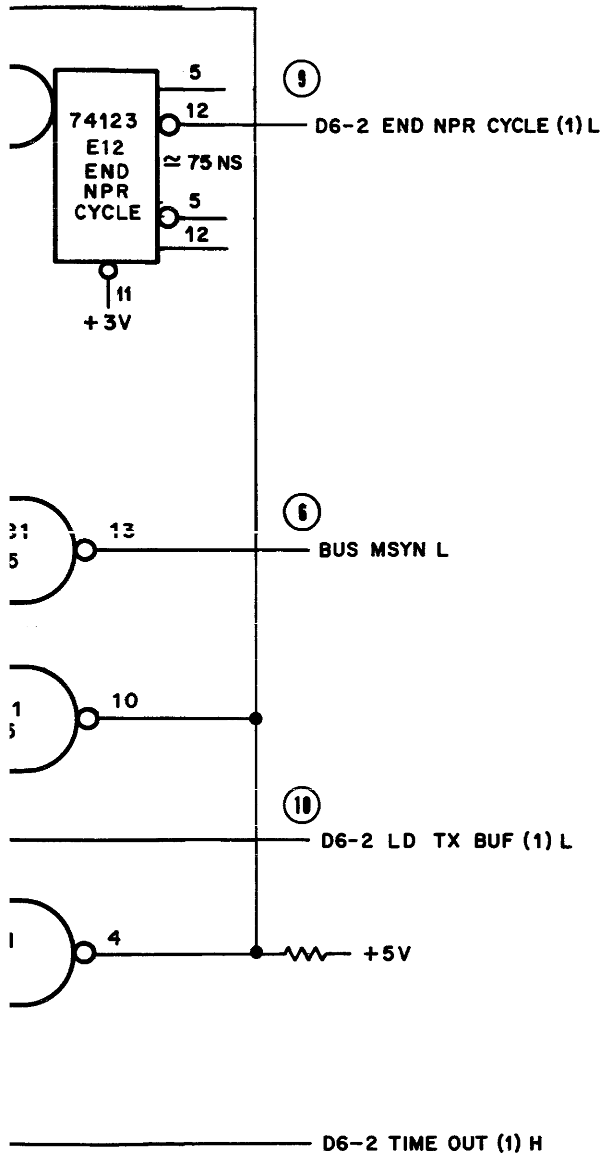
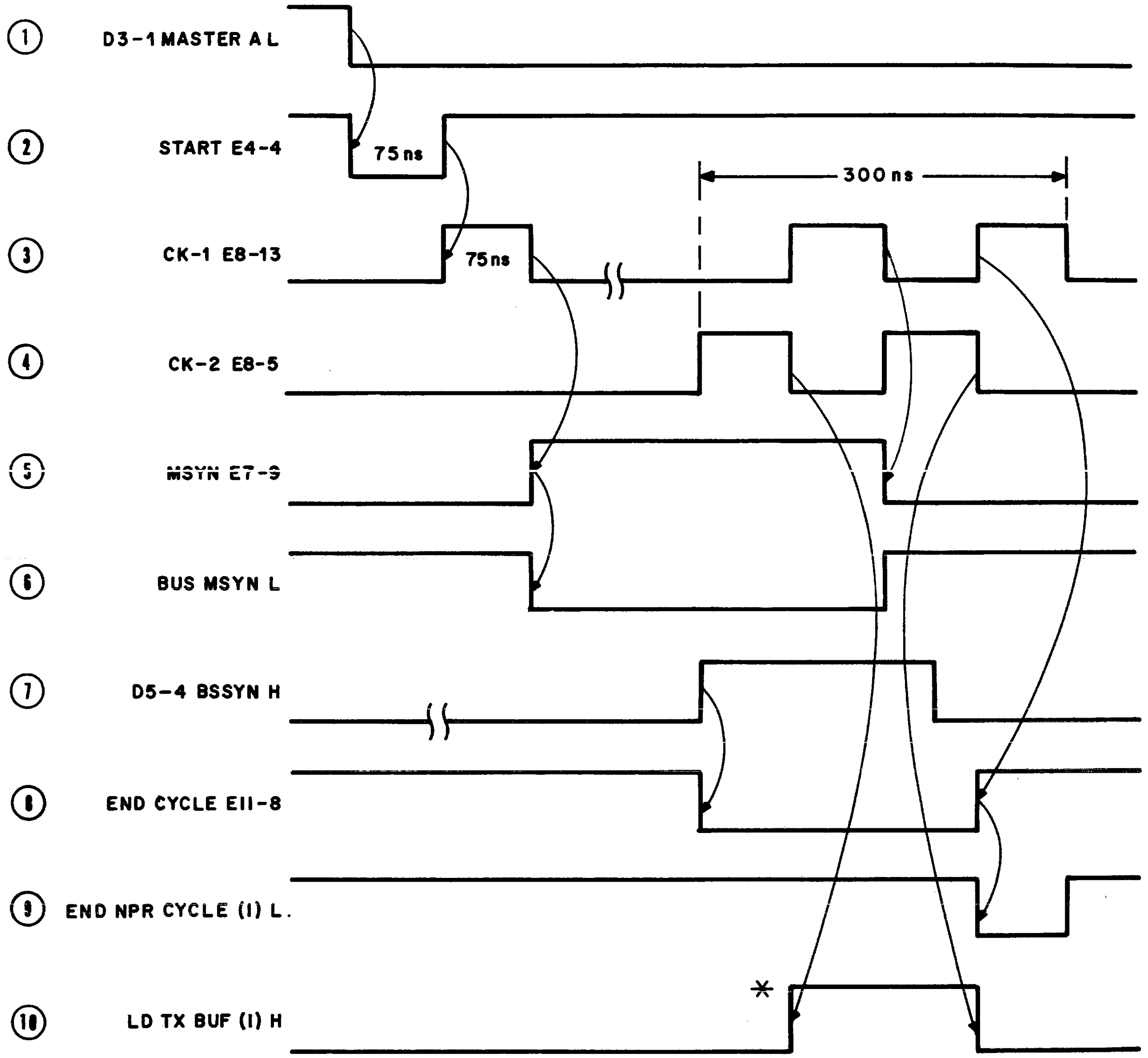


Figure 4-7 NPR Control Logic and Timing Diagram





NOTES:

1. Circled numbers are designated on schematic.
2. * Denotes that LD TX BUF (1) goes high only during transmit operation.
3. ⟆⟆ Denotes bus response time.

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4. When the M7821 Interrupt Module receives an NPR signal from the processor, it asserts D3-1 MASTER A L. This drives the E3 pin 1 high and the positive transition triggers the START one-shot.

5. The START one-shot generates a 75 ns negative pulse from its 0 output (pin 4) that is sent to the input (pin 2) of the CK1 one-shot.

6. The CK1 one-shot generates positive and negative pulses approximately 75 ns each. The negative pulse from pin 4 goes to the input (pin 10) of the CK2 one-shot. It does not trigger CK2 because the other input (pin 9) is inhibited by a high from the END CYCLE flip-flop.

   The positive pulse from pin 13 of the CK1 one-shot goes to the clock input of the MSYN and END CYCLE flip-flops. The END CYCLE is not clocked because it is in the cleared state and its D input is low. The negative-going trailing edge of the pulse clocks the MSYN flip-flop and sets it because its J input is high and its K input is low.

7. Setting the MSYN flip-flop produces the following action.

   a. Signal BUS MSYN L is asserted via bus driver E13 pin 13.

   b. The D input of the END CYCLE flip-flop goes high.

   c. The J input of the BUF flip-flop goes high via E3 pin 13.

   d. Input pins 11, 12, 8 and 5 of the three E15 bus drivers all go high.

   e. The MSYN TIMER one-shot is triggered and it generates positive and negative pulses of 20 μs each. The positive pulse from pin 13 is inverted by E22 and puts a low on the J input of the MSYN flip-flop which conditions it to be cleared at the proper time.

8. The DQ11 is bus master and is in the process of performing a DATI transaction to obtain a character from memory. Shortly after receiving BUS MSYN L, the memory asserts BUS SSYN L.

9. BUS SSYN L is sent to the M7813 module, inverted and sent to E15 pin 9 as D5-4 B SSYN H. The other input (pin 8) of this NAND gate is also high so its output goes low. This low signal directly sets the END CYCLE flip-flop via its preset input (pin 10). The low transition on the 0 output (pin 8) does not trigger one-shot E12 but it does trigger the CK2 one-shot.

10. When the 75 ns positive pulse from the CK2 one-shot times out, it triggers the CK1 one-shot and clocks the BUF flip-flop which toggles it to the set state. This drives D6-2 LD TX BUF (0) L high which is sent to the M7812 module to clock the character to be transmitted into the transmitter buffer register. The high from the 1 output (pin 12) of the BUF flip-flop, via two E3 gates, puts a high on the K input of the MSYN flip-flop. With the K input high and the J input low, the next negative transition of the clock pulse clears the flip-flop.

11. When the 75 ns positive pulse from the CK1 one-shot times out, it clears the MSYN flip-flop which performs the following action.

    a. Puts a low on the D input of the END CYCLE flip-flop.

    b. Clears signal BUS MSYN L.

    c. Puts a low on the D input of the TIME OUT flip-flop. This prevents D6-2 TIME OUT (1) H from being asserted when the MSYN TIMER one-shot times out.

    d. Inhibits retriggering of the MSYN TIMER one-shot until another low-to-high transition occurs at the MSYN flip-flop 1 output.

    e. Puts a low on the D input of the BUF flip-flop via E3 pin 13.

12. When the 75 ns negative pulse from the CK1 one-shot times out, it triggers the CK2 one-shot again. When the 75 ns positive pulse from the CK2 one-shot times out, it triggers the CK1 one-shot again and clocks the BUF flip-flop which clears it. Clearing the BUF flip-flop drives D6-2 LD TX BUF (1) H low again and, via two E3 gates, puts a low on the K input of the MSYN flip-flop.

13. The leading edge of the positive pulse from the CK1 one-shot clocks the END CYCLE flip-flop and clears it. The positive transition at the 0 output (pin 8) of this flip-flop triggers one-shot E12 which generates D6-2 END NPR CYCLE (1) L. This 75 ns pulse goes to the BA control logic on the M7813 logic and then to the M7821 Interrupt Module to clear D3-1 MASTER A L which inhibits further triggering of the CK1 and CK2 one-shots. It also clears the MSYN TIMER one-shot.

14. Clearing D3-1 MASTER A L also clears the MSYN TIMER one-shot. The NPR control logic is now back in its initial state.

The above sequence assumes that a transmit operation requested the NPR transaction. In this case, the BUF flip-flop is set to generate the loading signal (D6-2 LD TX BUF (1) H) for the transmitter buffer register.

If a receive operation requested the NPR transaction, signal D5-3 RX CYCLE H is high. Via E3 pin 13, it keeps a low on the J input of the BUF flip-flop which prevents it from being set.

Termination Due to Addressing Non-Existent Memory
If the DQ11 addresses non-existent PDP-11 memory, BUS SSYN L is not asserted because there is no response from the memory. Aborting an NPR transaction is not allowed; therefore, the NPR control logic must end the NPR transaction normally even though the DQ11 does not complete its DATI or DATO operation.

Assume that the operation has progressed normally to the point at which the MSYN flip-flop has been set and the NPR control logic is waiting for the memory to assert BUS SSYN. Assume further that the memory does not respond by asserting BUS SSYN L. The operation continues as follows.

1. If BUS SSYN L is not asserted 20 μs after BUS MSYN L is asserted, the MSYN TIMER one-shot times out. The trailing edge of the negative pulse from this one-shot (pin 4) clocks the TIME OUT flip-flop and sets it which asserts D6-2 TIME OUT (1) H. This signal is sent to the REG/ERR register in the M7812 module to set either bit 4 or 5 which indicates that non-existent memory has been addressed.

2. When the MSYN TIMER one-shot times out, its 1 output (pin 13) goes low. This signal and the high from the 1 output (pin 5) of the TIME OUT flip-flop are ORed at E22 to keep a low on the J input of the MSYN flip-flop to qualify it (J = L and K = H) to be cleared on the next clock pulse.

3. When D6-2 TIME OUT (1) H is asserted, it is also sent to pin 6 of NAND gate E15 and drives the output (pin 4) of this gate low. This gate is wire-ORed with the gate that accepts D5-4 B SSYN H so the logic now sequences just as if the memory had responded by asserting BUS SSYN L.

   From this point on, the NPR control logic terminates the NPR transaction normally.

4.3 M7815 MODULE (DATA SET CONTROL)

4.3.1 Introduction
The M7815 module is a single height, extended length, module that contains logic to control and monitor certain signals between the data set and the DQ11.

4.3.2 Functional Description
A simplified block diagram of the data set control logic is shown in Figure 4-8.

Three signals from the data set are sent to this logic: Carrier Detector (CO), Clear to Send (CS), and Ring Indicator (RING). Each of these signals is sent to a one-shot that generates a pulse when a positive or negative level transition of the input signal is detected. The outputs of the one-shots associated with these signals plus the output of an unassigned one-shot are sent to the DS INTR selection logic. This allows any active one-shot to set the Data Set Interrupt (DATA SET INTR) flip-flop. If the program has set the Data Set Interrupt Enable (DATA SET IE) flip-flop, signal DS INTR L is generated when the DATA SET INTR flip-flop is set. Signal DS INTR L is sent to the interrupt and vector control logic on the M7813 module to initiate a bus request (BR). Signal DATA SET INTR (1) H represents the state of the DATA SET INTR flip-flop and can be read by the program. Assertion of TEST LOOP H, during on-line testing, prevents the CO, SC, RING and SPARE one-shots from setting the DATA SET INTR flip-flop which prevents the generation of interrupts.

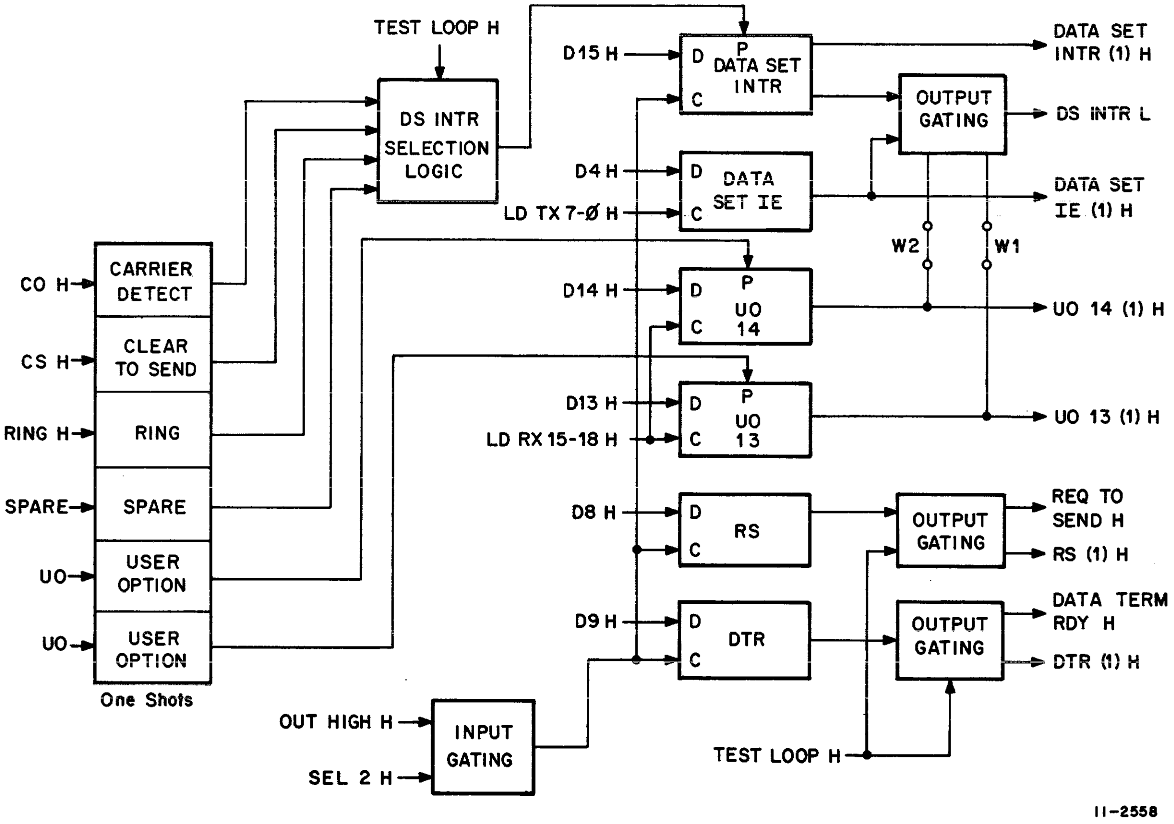


Figure 4-8 Block Diagram of Data Set Control Logic

Two additional User Option (UO) flip-flops are available that can be used to generate signal DS INTR L. They are UO14 and UO13 and are set by associated one-shots. The state of these two flip-flops and the DATA SET IE flip-flop can be read by the program. Jumpers W1 and W2 allow the UO flip-flops to generate interrupts. Removing the jumpers allows the flip-flops to be used only as flags.

The DATA SET IE flip-flop is set and cleared by the program. The DATA SET INTR, UO14, and UO13 flip-flops are set by the hardware and cleared by the program.

Through the program, this logic generates two control signals to the data set: Data Terminal Ready (DTR) and Request to Send (RS).

Two flip-flops are used in the logic to generate RS. The second flip-flop provides a delay to ensure that the Request to Send signal is asserted on the positive-going edge of the data terminal clock.

Signals DTR (1) H and RS (1) H represent the state of the associated flip-flops and can be read by the program. Signal TEST LOOP H, when asserted during on-line testing, inhibits the generation of DTR and DS.

4.3.3 Detailed Logic Description

The circuit schematic for the data set control logic is contained in drawing D-CS-M7815-0-1, sheet 2 which is designated D2-1. A simplified logic diagram is shown in Figure 4-9.

Six identical one-shots are used to allow signals from the data set to generate interrupts or to set flags. A typical one-shot is shown in Figure 4-10. The circuit consists of an RC network, an input inverter and an output exclusive-OR gate. It is triggered by a positive-going or negative-going edge and produces a negative pulse of short duration (approximately 500 ns).

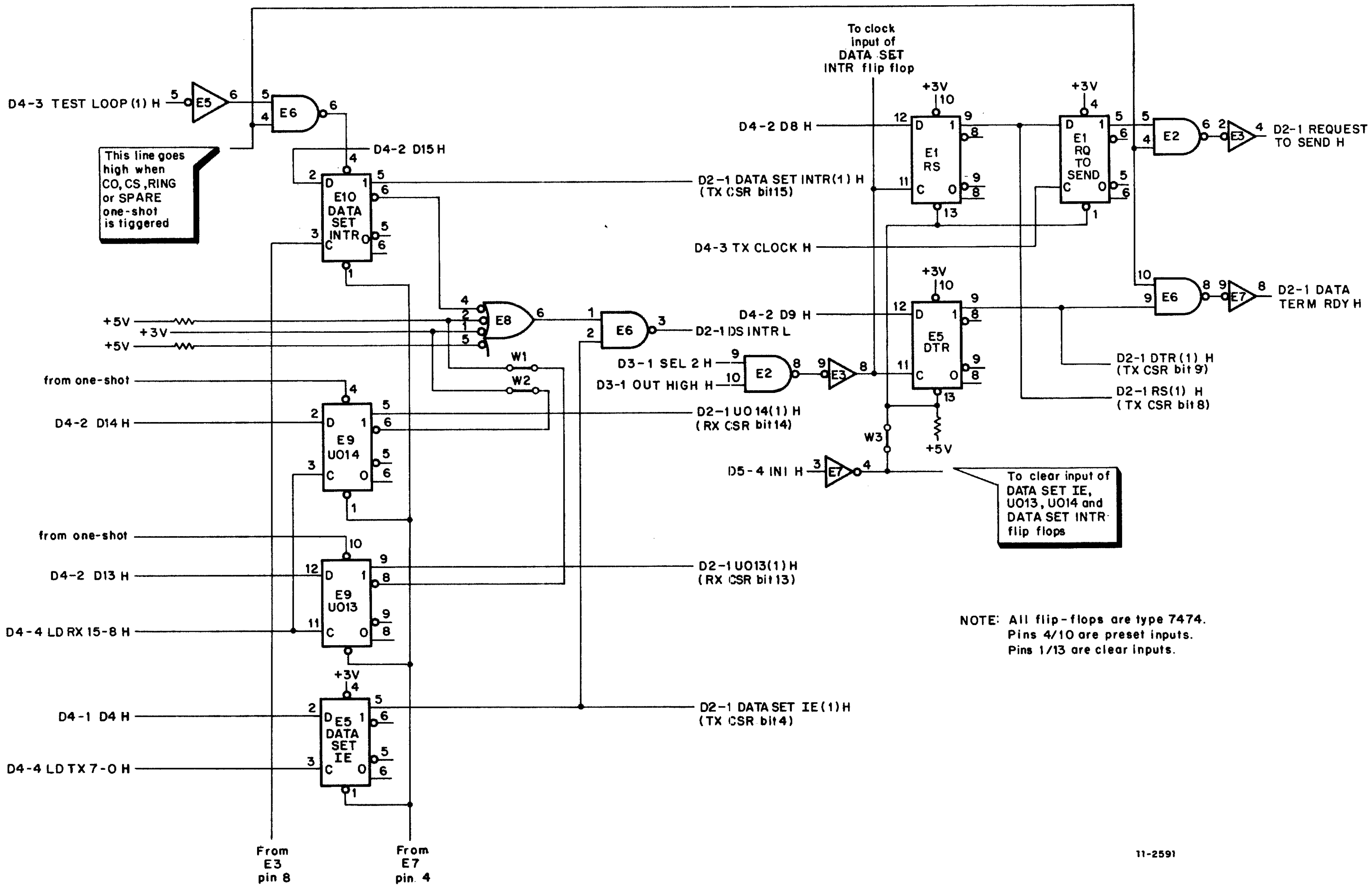
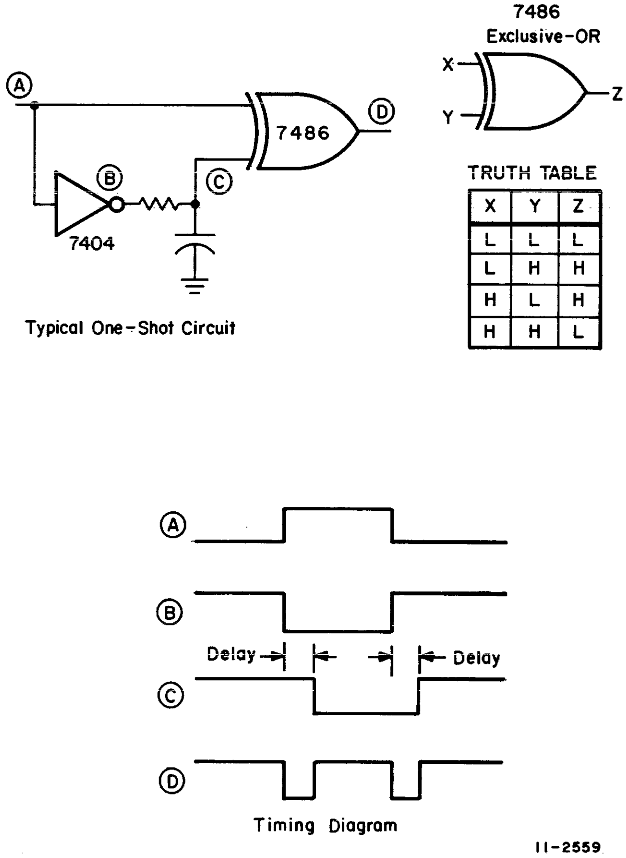

D4-3 TEST LOOP (1) H
E5
E6
This line goes high when CO, CS, RING or SPARE one-shot is tiggered
D4-2 D15 H
E10 DATA SET INTR
D2-1 DATA SET INTR(1) H (TX CSR bit15)
+5V
+3V
+5V
E8
E6
D2-1 DS INTR L
W1
W2
from one-shot
D4-2 D14 H
E9 UO14
D2-1 UO14(1) H (RX CSR bit14)
from one-shot
D4-2 D13 H
E9 UO13
D2-1 UO13(1) H (RX CSR bit13)
D4-4 LD RX 15-8 H
+3V
D4-1 D4 H
E5 DATA SET IE
D2-1 DATA SET IE(1) H (TX CSR bit4)
D4-4 LD TX 7-0 H
From E3 pin 8
From E7 pin 4
To clock input of DATA SET INTR flip flop
+3V
D4-2 D8 H
E1 RS
+3V
E1 RQ TO SEND
E2
E3
D2-1 REQUEST TO SEND H
D4-3 TX CLOCK H
+3V
D4-2 D9 H
E5 DTR
E6
E7
D2-1 DATA TERM RDY H
D3-1 SEL 2 H
D3-1 OUT HIGH H
E2
E3
D2-1 DTR (1) H (TX CSR bit 9)
D2-1 RS(1) H (TX CSR bit 8)
W3
+5V
D5-4 INI H
E7
To clear input of DATA SET IE, UO13, UO14 and DATA SET INTR flip flops
NOTE: All flip-flops are type 7474. Pins 4/10 are preset inputs. Pins 1/13 are clear inputs.
11-2591

Figure 4-9 Data Set Control Logic



X	Y	Z
L	L	L
L	H	H
H	L	H
H	H	L

Figure 4-10 Typical One-Shot Circuit and Timing Diagram

Referring to the circuit and timing diagram in Figure 4-10, assume that input A is low. Points B and C are high so the output (D) is high because the exclusive-OR, inputs (A and C) are complementary. Assume now that input A goes high. Point B goes low, but because of the delay caused by the RC network, point C remains high. Output D goes low because the exclusive-OR inputs (A and C) are the same (both high).

After a delay of approximately 500 ns, point C goes low and output D goes high again because the exclusive-OR inputs are again complementary. The circuit is now stable after generating a negative pulse of approximately 500 ns. The use of an exclusive-OR gate for the output allows a negative transition on the input to generate a negative pulse also.

The outputs of the CO, CS, RING, and unassigned one-shots are sent to E8 which is a 4-input NAND gate (shown as the logically equivalent negated-input OR gate). Jumper W4 is installed in the input line to the RING one-shot. If it is removed, RING interrupts are inhibited. A triggered one-shot drives the output of E8 high and it is sent to pin 4 of NAND gate E6. The other input (pin 5) is also high during normal operation, so the output (pin 6) of E6 is low. This signal is sent to the preset input (pin 4) of the DATA SET INTR flip-flop. A low on this input directly sets the flip-flop. This signal can be inhibited by D4-3 TEST LOOP (1) H which is inverted and sent to pin 5 of E6. This signal comes from bit 3 of the Miscellaneous Register (MISC CSR) on the M7812 module. When the program sets this bit, the DQ11 operates in the on-line test mode and no signals from the data set are allowed to set the DATA SET INTR flip-flop and subsequently cause an interrupt. This is accomplished by asserting D4-3 TEST LOOP (1) H, inverting it and sending the resulting low signal to pin 5 of E6.

When the DATA SET INTR flip-flop is set, its 0 output, via gate E8, puts a high on pin 1 of NAND gate E6. The other input (pin 2) of this gate is high only when the program has set the DATA SET IE flip-flop. If both of these flip-flops are set, D2-1 DS INTR L is asserted at E6 pin 3. This signal is sent to the interrupt control logic on the M7813 module (drawing D5-5). This logic generates the signals that start the request for interrupt via the M7821 Interrupt Module.

The DATA SET INTR flip-flop is set by the hardware using the preset input, and is cleared by the program using the D input and clock signal (D3-1 OUT H) (D3-1 SEL 2 H). The 1 output of this flip-flop is D2-1 DATA SET INTR (1) H which is bit 15 of the Transmitter CSR. The state of this bit is read at bus selector bit 15 on the M7812 module (drawing D4-2).

The DATA SET IE flip-flop is set and cleared by the program using the D input and clock signal D4-4 LDTX 7-0 H. The 1 output of this flip-flop is D2-1 DATA SET IE (1) H which is bit 4 of the Transmitter CSR. The state of this bit is read at bus selector bit 4 on the M7812 module (drawing D4-1).

Both the DATA SET INTR and DATA SET IE flip-flops are directly cleared by D5-4 INI H.

Two unassigned one-shots are provided to allow the presetting of two associated flip-flops, identified as User Options 13 and 14 (UO13 and UO14).

They can be used to provide additional data set control or to generate additional flags. The 1 outputs of these flip-flops (D2-1 UO13 (1) H and D2-1 UO14 (1) H) are bits 13 and 14 of the Receiver CSR. These bits are read at bus selector bits 13 and 14 on the M7812 module (drawing D4-2). Both flip-flops are set by the hardware using the preset input, and are cleared by the program using the D input and clock signal D4-4 LD RX 15-8 H. The 0 outputs of these flip-flops are sent to pins 1 and 2 of E8 via jumpers W2 and W1 respectively. With the jumpers in and DATA SET IE set, D2-1 DS INTR L is asserted if either UO13 or UO14 is set.

The data set control logic also generates two control signals that are sent to the data set: Request to Send (RS) which conditions the local data communications equipment for transmission, and Data Terminal Ready (DTR) which controls switching of the data communications equipment to the communications channel. Both signals are generated by flip-flops that are program-controlled.

To generate the DTR signal, the program puts a high on Unibus data bit 9 that is picked up by a bus receiver on the M7812 module and sent to the D input of the DTR flip-flop as D4-2 D9 H. The program performs a DATOB on the high byte of the Transmitter CSR which asserts D3-1 OUT HIGH H and D3-1 SEL 2 H at the M105 Address Selector Module. These signals are ANDed at pins 9 and 10 of NAND gate E2. The output of E2 goes low and is inverted by E3. The positive-going edge of the output of E3 clocks the DTR flip-flop which sets it. The 1 output of the DTR flip-flop is ANDed with the inverse of D4-3 TEST LOOP (1) H at NAND gate E6. With DTR set and D4-3 TEST LOOP (1) H not asserted, the output of E6 is low. This signal is inverted by E7 to assert D2-1 DATA TERM RDY H which is sent to the data set.

It is a requirement that the RS signal must be asserted by the positive-going edge of the data set clock. This requirement is met by using two flip-flops to generate the RS signal. The program sets the RS flip-flop the same way it sets the DTR flip-flop, except that bit 8 is used to condition the D input of the RS flip-flop. Setting the RS flip-flop is asynchronous with the external clock so it is not allowed to directly generate the RS signal.

When RS is set, its 1 output is sent to the D input of the RQ TO SEND flip-flop. The next positive transition of the external clock (D4-3 TX CLOCK H) sets the RQ TO SEND flip-flop. The 1 output of this flip-flop is ANDed with the inverse of D4-3 TEST LOOP (1) H at NAND gate E2. With RQ TO SEND set and D4-3 TEST LOOP (1) H not asserted, the output of E2 is low. This signal is inverted by E3 to assert D2-1 REQUEST TO SEND H which is sent to the data set.

The RS, RQ TO SEND, and DTR flip-flops are directly cleared by D5-4 INI H. This action can be inhibited by removing jumper W3 at the output (pin 4) of inverter E7.

The 1 output of the DTR flip-flop is D2-1 DTR (1) H which is bit 9 of the Transmitter CSR. The 1 output of the DS flip-flop is D2-1 RS (1) H which is bit 8 of the Transmitter CSR. These bits are read at bus selector bits 9 and 8 on the M7812 module (drawing D4-2).

4.4 M7812 MODULE (BUS SELECTORS)

4.4.1 Introduction

The M7812 module is a hex height, extended length, module that contains several functionally separate logic circuits. They are listed below in the order of discussion.

1. Bus Selectors and Control Logic
2. Miscellaneous (MISC) Register and Internal Clock
3. Transmitter Control and Status Register (TX CSR)
4. Receiver Control and Status Register (RX CSR)
5. Register Pointer and Error Register (REG/ERR)
6. Sync Register (SYNC) and Transmitted Data Output Logic
7. Transmitter Shift Register
8. Receiver Shift Register and Receiver Data Register

4.4.2 Bus Selectors and Control Logic

4.4.2.1 Functional Description – The outputs of the eight registers used in the basic DQ11 are multiplexed to the Unibus data lines through one set of 16 bus drivers. This is accomplished by using 32 4-line to 1-line multiplexers. Two multiplexers handle 1 bit of all 8 registers which are 16 bits long; therefore, 32 multiplexers are required. Figure 4-11 is a simplified block diagram of the arrangement. The Receiver Control and Status Register (RX CSR), Transmitter Control and Status Register (TX CSR), Register Pointer/Error Register (REG/ERR), and the Receiver Data Register are word- or byte-addressable. The Transmitter Buffer Register (TX BUF), Miscellaneous Register (MISC), SYNC Register and Character Count/Bus Address Register (CC/BA REG) are word-addressable only. Refer to Chapter 3 for a detailed discussion of the bit assignments and function of these registers.

The select and enabling signals are generated by the AA selection decoding logic. The "AA" refers to the suffix for the basic DQ11 option designation (DQ11-AA). The enabling signals turn on the multiplexers and the select inputs choose the desired register which is a multiplexer input. The RX CSR, TX CSR and REG/ERR registers are selected as a function of the SEL 0 H, SEL 2 H, and SEL 4 H signals respectively, from the M105 Address Selector Module. The Receiver Data Register is selected during a receiver-initiated NPR cycle.

The TX BUF, MISC, SYNC, and CC/BA registers are secondary registers and are not selected directly by the M105 module. They are selected by bits 8–11 of the REG/ERR register and SEL 6 H from the M105 module. Signal BA IT is an interlock signal that is asserted only when the M7815 Data Set Module is plugged in. It allows the high byte of the TX CSR register to be read. This byte (bits 8–15) represents data set functions that require monitoring only when the M7815 module is installed.

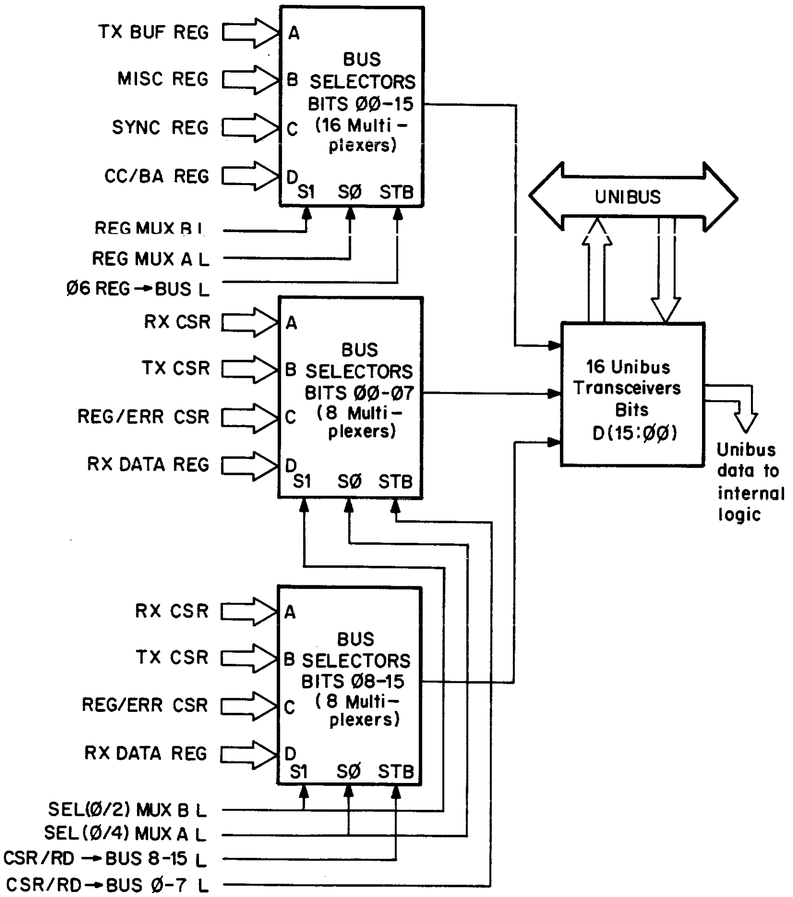


Figure 4-11 Block Diagram of Bus Selection Logic

4.4.2.2 Detailed Logic Description – The circuit schematics for the bus selectors and selection logic are contained in drawing D-CS-M7812-0-0 (Rev D) sheets 2, 3 and 4 which are designated D4-1, D4-2 and D4-3.

Bus Selectors

The bus selectors for bits 00–07 are shown on print D4-1; the bus selectors for bits 08–15 are shown on print D4-2. The multiplexers are arranged similarly on both prints; namely, in two groups of two columns each. The 16 multiplexers in the left column of each group handle the secondary registers as shown below.

Register	MUX Input
TX BUF	A
MISC	B
SYNC	C
CC/BA	D

The 16 multiplexers in the right column of each group handle the primary registers as shown below.

Register	MUX Input
RX CSR	A
TX CSR	B
REG/ERR	C
RECD DATA	D

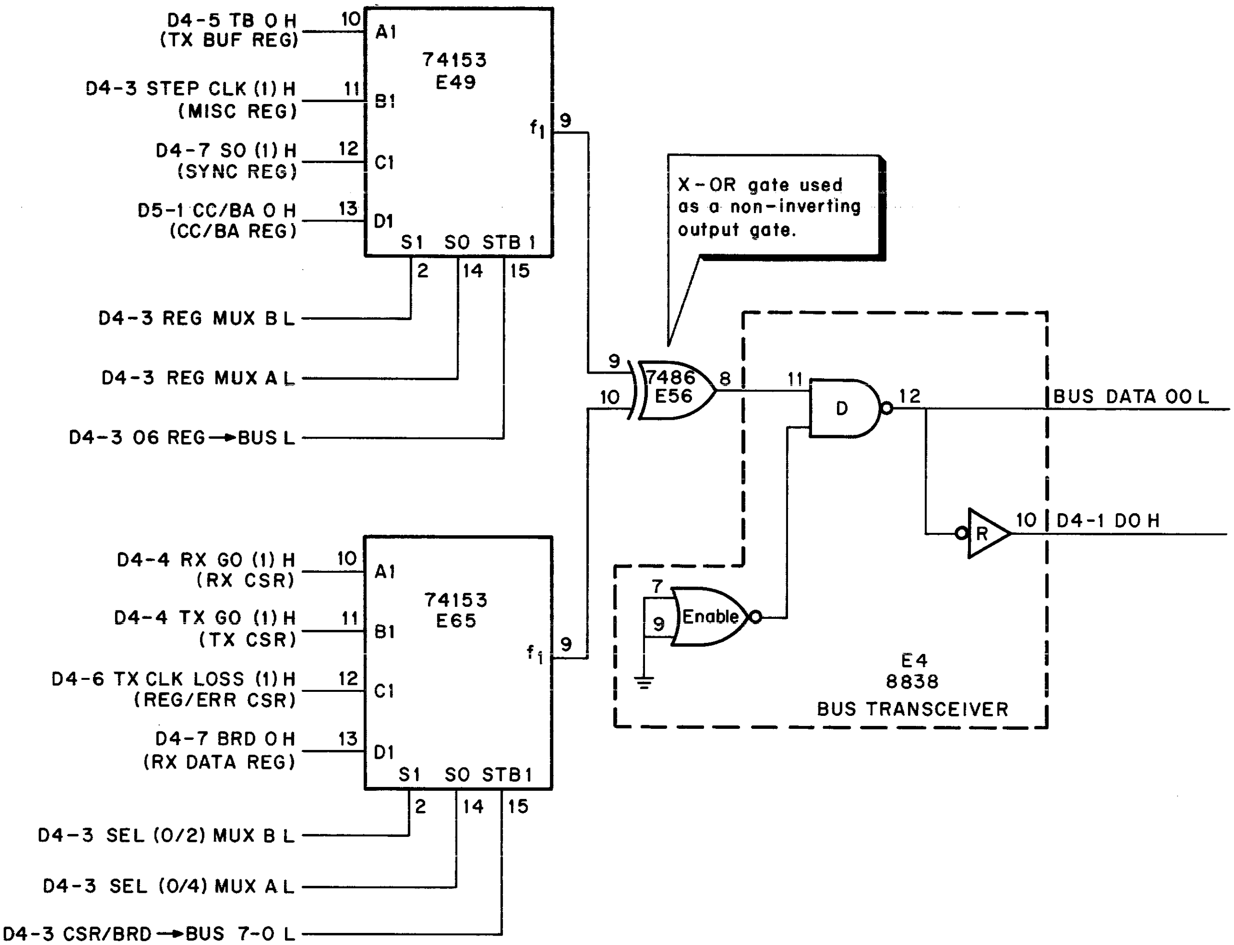
Figure 4-12 shows bit 00 of all eight registers. Multiplexer E49 handles the secondary registers. It is enabled when strobe input D4-3 06 REG → BUS L is low. Select inputs D4-3 REG MUX B L and D4-3 REG MUX A L are decoded to pick the desired input (A, B, C or D). Multiplexer E65 handles the primary registers. Its enabling signal is D4-3 CSR/RD → BUS 0–7 L and its select signals are D4-3 SEL (0/2) MUX B L and D4-3 SEL (0/4) MUX A L. The multiplexer truth table is shown in Figure 4-12. Both multiplexer outputs are sent to exclusive-OR gate E56 which is used as a non-inverting gate to pass the selected multiplexer output to Unibus driver E4. Because the primary and secondary registers are not read simultaneously, the enabling input (STB1) to either E49 or E65 is inhibited (high) while the other enabling input is asserted (low). The output of the inhibited multiplexer is low which holds one input of the exclusive-OR gate low. If the output of the active multiplexer is low, the exclusive-OR inputs are identical and its output is low. If the output of the active multiplexer is high, the exclusive-OR inputs are complemented and its output is high. The bus driver (E4 pin 12) is part of an 8838 quad transceiver. One input of the bus driver is held high and the other input comes from the output of the exclusive-OR gate. The multiplexer output is inverted by the bus driver before being placed on the Unibus.

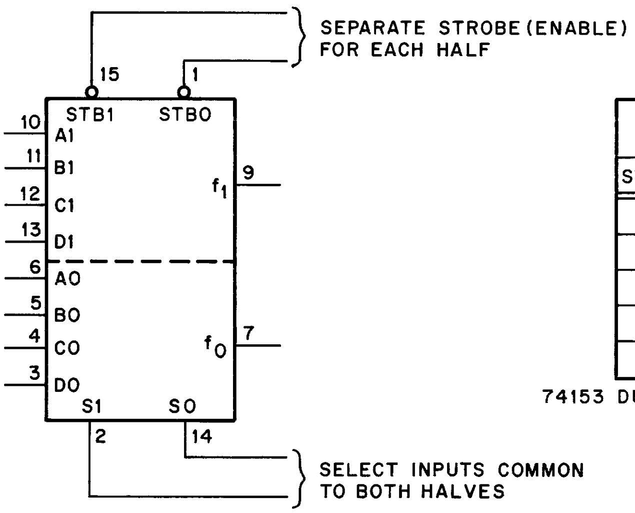
Register Selection Logic

The register selection logic is shown in the left side of print D4-3. Figure 4-13 also shows the register selection gates, plus additional informative comments.

The top half of the logic generates the select and enabling signals for the primary registers. The RX CSR, TX CSR, and PT/ERR registers are addressed directly and are selected by the appropriate signal from the M105 Address Selector Module. These signals are D3-1 SEL 0 H, D3-1 SEL 2 H, and D3-1 SEL 4 H, respectively. They are decoded by two NOR gates (E15) to generate multiplexer select signals D4-3 SEL (0/4) MUX A L and D4-3 SEL (0/2) MUX B L. The state of these select signals determine which register is to be read, as shown in the table in Figure 4-13. During the DATI transaction that is used to read the selected register, the M105 module asserts D3-1 IN H. With this signal asserted and the M7815 Data Set Control Module installed, both multiplexer enabling signals (D4-3 CSR/RD → BUS 0–7 L at E16 pin 6 and D4-3 CSR/RD → BUS 15–8 L at E17 pin 8) are generated when either D3-1 SEL 0 H, D3-1 SEL 2 H or D3-1 SEL 4 H is asserted. When the M7815 module is installed, it asserts D2-1 BA IT L which is a ground level interlock signal that is sent to pin 10 of NAND gate E16. It drives the output (pin 8) of E16 high and this signal is a qualifying input to E17 pin 9. If the M7815 module is not installed, D2-1 BA IT L is not asserted and pin 10 of E16 is held high via the +5 V applied to R1. If the TX CSR register is addressed, D3-1 SEL 2 H is asserted and sent to the other input (pin 9) of E16. This drives the output of E16 low and prevents the assertion of D4-3 CSR/RD → BUS 15–8 L at E17 pin 8. This inhibits the reading of the high byte of the TX CSR register when the M7815 Data Set Module is not installed. This is a logical action because the high byte contains data set signals that are present only when the M7815 module is used.

The RECD DATA register is read during a receiver initiated NPR cycle. During this time, none of the primary registers are addressed so signals D3-1 SEL 0 H, D3-1 SEL 2 H, and D3-1 SEL 4 H are not asserted. Both D4-3 SEL (0/4) MUX A L and D4-3 SEL (0/2) MUX B L are high so the RECD DATA register is selected. The CC/BA control logic on the M7813 module asserts D5-3 RX NPR L. This signal, along with D3-1 SEL 2 H which is not asserted, generates both multiplexer enabling signals (D4-3 CSR/RD → BUS 0–7 L and D4-3 CSR/RD → BUS 15–8 L) whether D2-1 BA IT L is asserted or not.



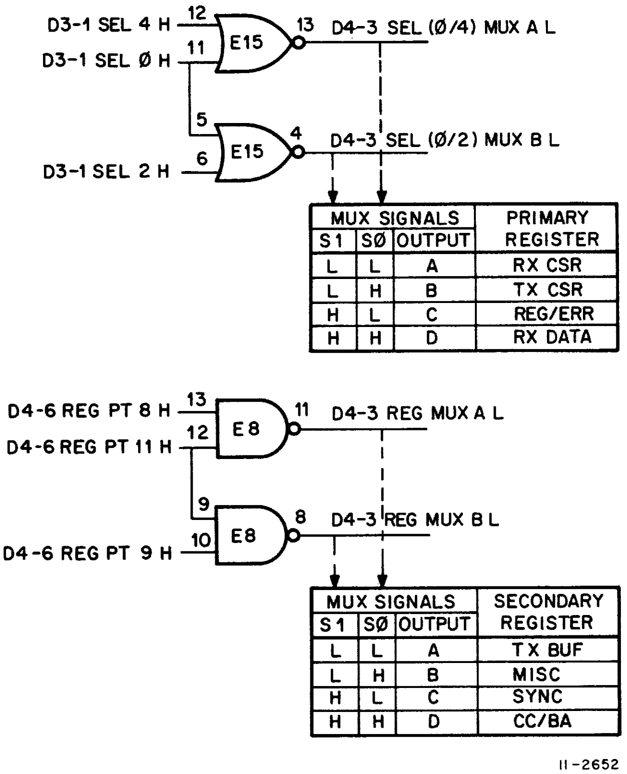

SEPARATE STROBE (ENABLE) FOR EACH HALF
15
1
STB1
STB0
10
A1
11
B1
12
C1
13
D1
f1
9
6
A0
5
B0
4
C0
3
D0
f0
7
S1
S0
2
14
SELECT INPUTS COMMON TO BOTH HALVES

CONTROL INPUT			DATA INPUT SELECTED			
STB	S1	S0	A	B	C	D
L	L	L	*			
L	L	H		*		
L	H	L			*	
L	H	H				*
H	X	X	L	L	L	L

74153 DUAL 4-LINE TO 1-LINE MULTIPLEXER

11-2655

Figure 4-12 One Bit Slice of Bus Selection Multiplexers



MUX SIGNALS			PRIMARY REGISTER
S1	S0	OUTPUT	
L	L	A	RX CSR
L	H	B	TX CSR
H	L	C	REG/ERR
H	H	D	RX DATA

MUX SIGNALS			SECONDARY REGISTER
S1	S0	OUTPUT	
L	L	A	TX BUF
L	H	B	MISC
H	L	C	SYNC
H	H	D	CC/BA

Figure 4-13 Register Selection Logic

The bottom half of the logic generates the select and enabling signals for the secondary registers. There are 16 secondary registers but only 11 are used in the basic DQ11 option. They are: TX BUF, MISC, SYNC, 4 BA registers, and 4 CC registers. The secondary registers are not selected directly by the M105 Address Selected Module. They are selected by addressing the REG/ERR register and using the states of bits 8–11 of this register to point to the desired secondary register. Figure 4-12 shows truth tables that illustrate this selection process.

The inputs to the secondary register selection logic are:

> D3-1 SEL 6 H from the M105 module which is asserted when the REG/ERR register is addressed to set up bits 8–11 for the selected secondary register.
>
> D4-6 REG PT 8 H–11 H from the REG/ERR register which represent the octal designation of the desired secondary register.
>
> D3-1 IN H from the M105 module which is asserted when a DATI bus transaction is initiated to read the selected secondary register.

All these signals are used in the portion of the logic that generates the multiplexer enabling signal D4-3 06 REG → BUS L at E17 pin 6. The multiplexer select signals are generated by two dual-input NAND gates (E8) that require only REG/ERR bits 8, 9, and 11 for decoding. To verify the selection process, choose a secondary register in the table in Figure 4-13 to obtain the state of the REG/ERR bits and follow the signals through the logic. The D input of the multiplexer can be any one of eight registers (four BA registers and four CC registers) which are selected by the CC/BA control logic on the M7813 module.

4.4.3 Miscellaneous Register (MISC) and Internal Clock

4.4.3.1 Functional Description – This discussion, and the detailed discussion that follows, covers the operation of the Miscellaneous Register and its associated logic. A register bit map and functional description of each bit is covered in Chapter 3, Programming.

A simplified block diagram of the Miscellaneous Register and internal clock is shown in Figure 4-14. The register and clock are shown together because several bits of the register are related to operation of the clock or its output logic during servicing.

Five bits (4, 5, 12, 13, and 14) of the Miscellaneous Register are not contained on this module. They are contained on the M7813 module and are described in the discussion of the M7813 module.

The remaining 11 bits are contained in two D-type hex flip-flops (bit 2 is not assigned). All bits are clocked by signal LD MISC L from the M7813 module. The state of each bit is controlled by the program via a Unibus data line.

The RC clock supplies a 14 Kbaud signal during the transmit mode. The receiver clock comes in with the data from the data set during the receive mode. An optional crystal-controlled clock (M4050 module) can be installed in the DQ11 to be used during the transmit mode in place of the RC clock. The crystal clock output is counted down by 16 or by 2 to provide baud rates of 250K and under or over 250K, respectively.

The RC clock is also used in the test loop mode during servicing of the DQ11. If the external clock is lost when receiving data, the RC clock is used to shift a character in completely before the receiver is shut down by the clock loss circuit on the M7813 module.

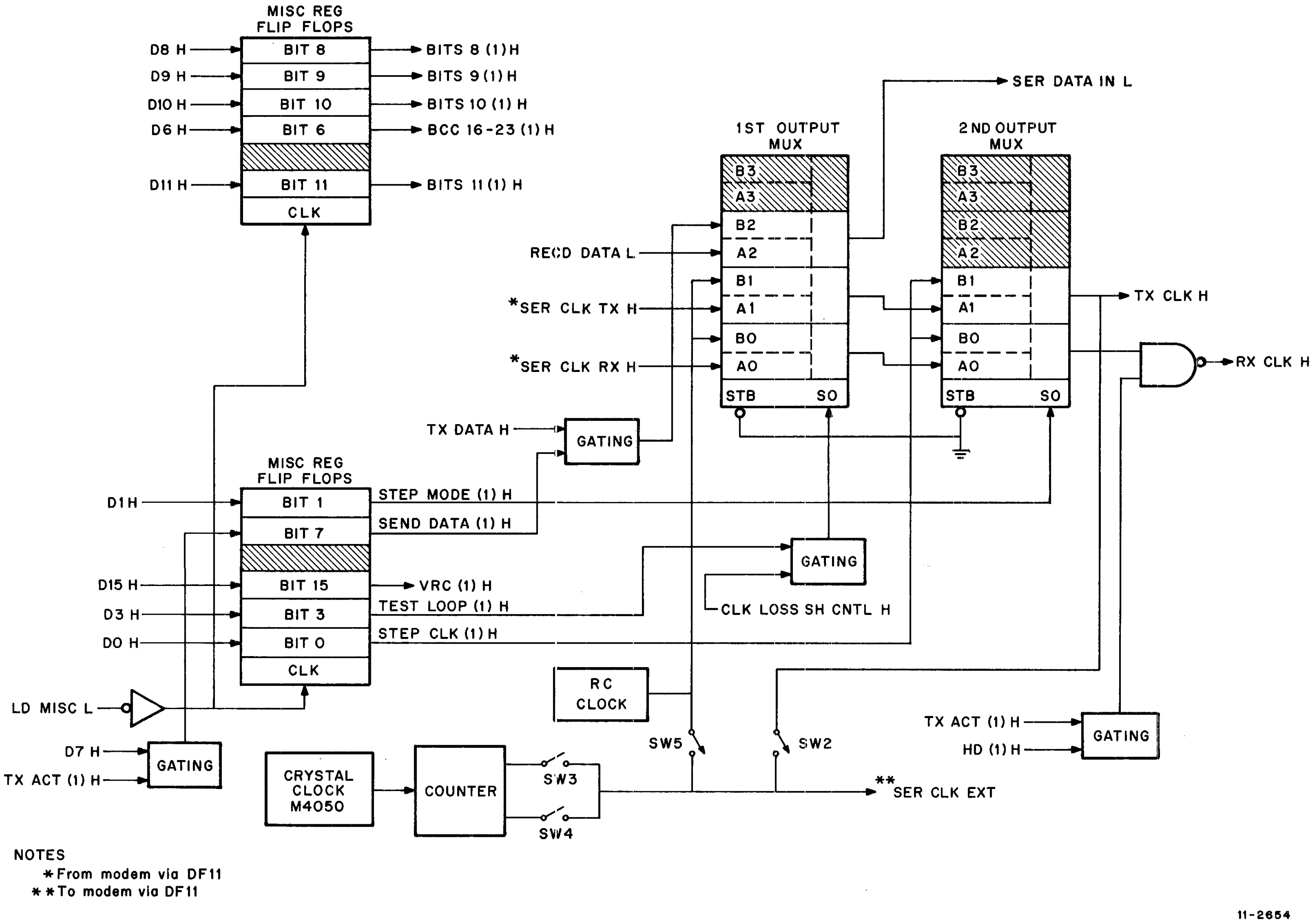


Figure 4-14 Block Diagram of Miscellaneous Register and Internal Clock

During servicing, the test loop mode is initiated by the program to substitute the RC clock for the normal clock at the first multiplexer. The program can also initiate a single step clock operation during servicing. This is done by setting bit 1 (STEP MODE) while in the test loop mode and toggling bit 0 (SHIFT CLOCK). This allows controlled transitions of signals TX CLOCK H and RX CLOCK H.

4.4.3.2 Detailed Logic Description – The circuit schematic for the Miscellaneous Register and internal clock is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 4 which is designated D4-3.

Miscellaneous (MISC) Register

The 11 bits of the MISC register, which are contained in hex flip-flops E61 and E70, are clocked when D5-4 LD MISC L is asserted. When this signal goes low, it is inverted by E58 and the positive transition simultaneously clocks all bits. Signal D5-4 LD MISC L is generated on the M7813 module (print D5-4) by decoder E44 after REG/ERR register bits 8–11 have been set to 12_8 (MISC register) and a write operation has been selected using SEL 6 H. Package E70 contains bits 6 and 8–11. Bit 6 (D4-3 BCC 16–23 (1) H) is not used in the DQ11-AA option. Bits 8–11 D4-3 BITS 8 (1) H–11 (1) H are sent to the receiver shift register (print D4-5) and are discussed later. Package E61 contains bits 0, 1, 2, 3, 7, and 15. Bit 2 is not assigned and bit 15 (D4-3 VRC (1) H) is not used on this module. The other bits (0, 1, 3, and 7) are related to the use of the clock, particularly during servicing, and are covered in the discussion of the clock.

Internal Clock

During a receive operation, the data set sends the receiver clock along with the data to the DQ11. The received data and receiver clock pass through the DF11 converter and are sent to multiplexer E59 (print D4-3). The data passes through the DF11 and is sent to the A2 input of E59 as D1-1 RECEIVE DATA. The receiver clock passes through the DF11 and is sent to the A0 input of E59 as D1-1 SCR H. Package E59 is a quad 2-line-to-1-line multiplexer (74157). It is held enabled by connecting the strobe (STB) input permanently to ground. During normal operation, the select (S0) input is low which chooses the A inputs. S0 is low because bit 3 (TEST LOOP) of the MISC register is not set (D4-3 TEST LOOP (1) H is low) and the clock is operating properly (D5-4 CLK LOSS SH CNTL H is low). These two conditions drive pin 4 of E67 high. This signal is inverted by E58 and applied to the select (S0) input of E59. Signal D1-1 RECEIVE DATA L passes through multiplexer E59 and is called D4-3 SERIAL DATA IN L. It is sent directly to the receiver shift register (print D4-5). Signal D1-1 SCR H passes through E59 and is sent to the A0 input of multiplexer E60. This input is selected (input S0 low) during normal operation because bit 1 (STEP MODE) is cleared (D4-3 STEP MODE (1) H is low). The receiver clock signal passes through multiplexer E60 and is sent to pin 5 of NAND gate E69. The other input (pin 4) of this gate is used to inhibit the clock when half-duplex mode is selected (D4-4 HD (1) H is high) and the transmitter is active (D5-6 TX ACTIVE (1) H is high). The output of E69 is D4-3 RX CLOCK H which is sent to the receiver shift register.

During a transmit operation, the clock can be supplied by the DQ11 or by the data set. If the clock comes from the data set, it passes through the DF11 and is sent to the A1 input of E59 as D1-1 SCT H. During normal operation, the multiplexer A inputs are selected; therefore, D1-1 SCT H passes through E59 and is sent to the A1 input of multiplexer E60. During normal operation, this multiplexer also selects its A inputs so the A1 input appears at the f_1 output as D4-3 TX CLOCK H. This signal is sent to the transmitter shift register control logic.

As previously mentioned, the internal transmit clock source can be from the RC clock or from the optional crystal clock. The RC clock consists of a pair of 7404 inverters (E50), resistor R14 and capacitor C107. It starts when power is applied and is self-sustaining. The output frequency is approximately 28 KHz which is counted down by flip-flop RC÷2 (E51) to provide a clock output of approximately 14 KHz. Switch SW5 (Figure 4-15) must be closed to direct the RC clock output to the DF11 as D4-3 SERIAL CLOCK EXTERNAL. Switches SW3 and SW4 must be open because the optional crystal clock is not used. Switch SW1 must be closed to prevent attenuation of the RC clock signal; switch SW2 must be open. Additional information concerning switches SW1, SW2 and SW5 is contained in subsequent paragraphs in this section.

The optional crystal clock is contained on a module (M4050) that plugs into the DQ11. Its output (D3-1 KA CRYSTAL CLOCK H) is sent to inverter E50 (print D4-3). This inverted clock signal is sent to the CLK0 input of E52 which is a 74197 presettable binary counter. The preset feature is disabled by permanently connecting the LD input to +3 V. The counter cannot be cleared because the CLR input is also connected to +3 V. Counter output R0 (1) is connected to clock input CLK1 which configures E52 as a 4-bit ripple-through counter. The input clock signal (D3-1 KA CRYSTAL CLOCK H) is divided by 2 at output R0 (1) and is divided by 16 at output R3 (1). Either output can be selected as the transmitter clock. With switch SW3 closed and switch SW4 open, the divide by 16 output is connected to the DF11. This is used for a baud rate of 250K or less.

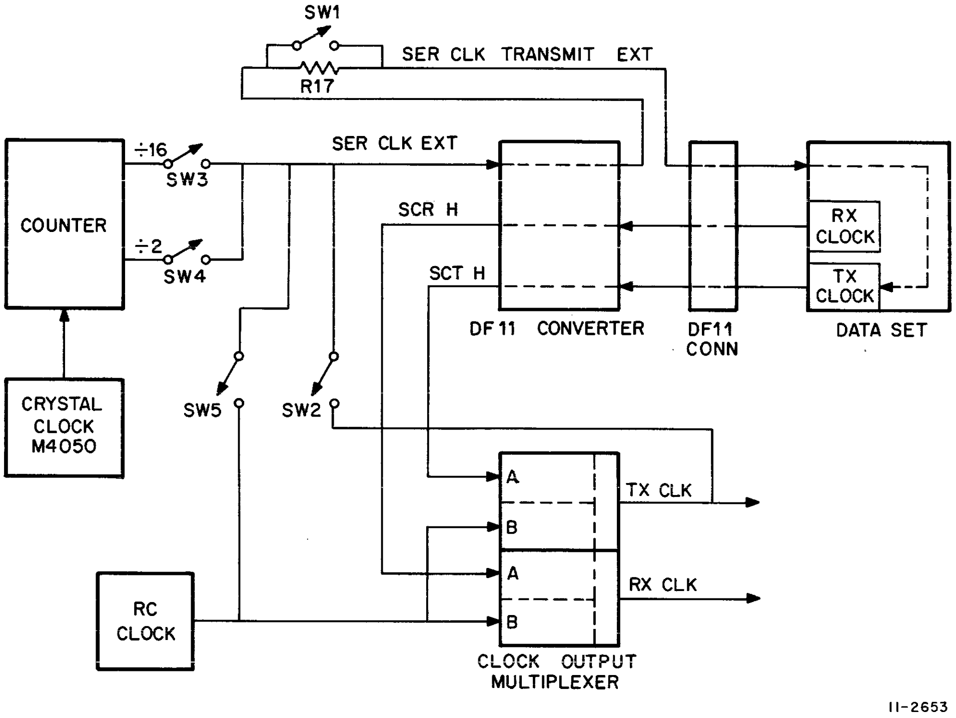


Figure 4-15 Block Diagram of Internal Clock to DF11 Interface

With switch SW4 closed and switch SW3 open, the divide by 2 output is connected to the DF11. This is used for a baud rate greater than 250K. The actual baud rate is a function of the crystal frequency. When the crystal clock is used, switches SW2 and SW5 must be open and SW1 must be closed.

Switch SW2 is closed only when a type 306 modem is used. This modem requires that the transmitter clock signal be returned to the modem.

With switch SW1 open, it is possible to connect the RC clock to the D4-3 SERIAL CLOCK EXTERNAL line (switch SW5 closed) when the transmitter clock is supplied by the data set. The RC clock signal is attenuated by resistor R17 and does not interfere with the data set clock. It does allow the DQ11 to be disconnected from the data set during servicing and to be checked using the RC clock source. Otherwise, the clock is lost when the data set is disconnected, if the data set is supplying the clock.

Several bits of the MISC register are interrelated with the clock to provide special operations during servicing of the DQ11. The test loop mode of operation can be selected by setting bit 3 (TEST LOOP) of the MISC register. During this mode, the transmitter output is fed back to the receiver input and is not sent to the data set. When bit 3 is set by the program, signal D4-3 TEST LOOP (1) H is asserted and selects the B inputs of multiplexer E59. The output of the RC clock is sent to the B0 and B1 inputs of E59. These two clock signals propagate through E59 and E60 to become D4-3 TX CLOCK H and D4-3 RX CLOCK H. Signal D4-3 TEST LOOP (1) H is also sent to E67 pin 9 (print D4-7) which holds the output of this gate low. This signal (D4-7 SERIAL DATA OUT L) is sent to the data set. The other input to this gate is D -7 TX DATA IN which comes from E23 pin 8. This signal is sent also to E68 pin 9. The other input (pin 10) of E68 comes from inverter E58 and remains high as long as bit 7 of the MISC is not set. Under these conditions, the transmitter data (D4-7 TX DATA H) propagates through E68 to the B2 input of multiplexer E59. The B inputs are selected so the transmitter data passes through E59 to the D4-3 SERIAL DATA IN L line which is the data input to the receiver shift register. Hence, the transmitter data is looped back to the receiver input and it is clocked by the internal RC clock.

During the test loop mode, the receiver can be checked directly by toggling bit 7 (SEND DATA) provided the transmitter is inactive. Inverter E58 and E33 (print D4-3) allow bit 7 in the MISC register to be set only if the transmitter is inactive (D5-6 TX ACTIVE (1) H is low) and the program makes bit 7 high (D4-7 D7 H is high). The bit 7 output of the MISC register is inverted by E58 and sent to E68 pin 10. The other input (pin 9) of this gate is D4-7 TX DATA H and it is held low when the transmitter is inactive. The output (pin 8) of E68 is the B2 input of E59 and passes through to become D4-3 SERIAL DATA IN L. By toggling bit 7, the state of this signal can be changed to control the input to the receiver shift register.

During servicing, data can be single stepped through the receiver and transmitter shift registers by selecting the step mode of operation. The program selects the step mode by setting bit 1 (STEP MODE) of the MISC register. This asserts D4-3 STEP MODE (1) H and multiplexer E60 now selects its B inputs. The source for the shift register clock signals (D4-3 TX CLOCK H and D4-3 RX CLOCK H) now becomes the output of bit 0 of the MISC register which is D4-3 STEP CK (1) H. Toggling bit 0 alternately strobes data into the receiver and transmitter shift registers. Setting bit 0 strobes the transmitter shift register and clearing bit 0 strobes the receiver shift register.

4.4.4 Transmitter Control and Status Register

4.4.4.1 Functional Description – A simplified block diagram of the Transmitter Control and Status Register (TX CSR) is shown in Figure 4-16. This discussion, and the detailed discussion that follows, covers the operation of the TX CSR and its associated logic. A register bit map and function 1 description of each bit is covered in Chapter 3, Programming.

Only six bits of the TX CSR are shown on this module. The remaining 10 bits are located on other modules and are described in the discussion of the applicable module. Bit 14 is not assigned but it is available on the backplane as a TTL connection. Bit 2 is located on the M7813 module (print D5-4). Bits 4, 8, 9 and 15 are located on the M7815 module (print D2-1). Bits 10–13 are signals to or from the data set and are picked off the DF11 (print D1-1).

The TX CSR is word- and byte-addressable. The six bits on this module are contained in D-type flip-flops and are clocked simultaneously when the register is addressed during a DATO or DATOB (low byte) transaction.

4.4.4.2 Detailed Logic Description – The circuit schematic for the TX CSR is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 6 which is designated D4-4.

Bits 1, 3, and 5 are contained in a 74174 hex, D-type flip-flop (E36). Three sections of E36 are not used. These bits have a common clock and clear input. Bits 0, 6, and 7 are contained in separate 7474 D-type flip-flops and use the same clock signal as bits 1, 3, and 5. All six bits are directly cleared by D5-4 INI H which is generated as a result of BUS INIT L or MASTER CLEAR which is bit 5 of the MISC register.

The clock signal is generated at the output (pin 3) of AND gate E33. When the TX CSR is addressed during a DATO or DATOB (low byte), the M105 Address Selector asserts D3-1 OUT LOW H and D3-1 SEL 2 H. These signals are sent to E33 pins 2 and 1, respectively. The output (pin 3) goes high and this positive transition clocks all six bits.

As stated previously, direct clearing of all bits is performed by D5-4 INI H. This signal is inverted by E25 and sent to the direct clear input of each flip-flop. A low level clears the flip-flop. Bit 0 of the TX CSR can be directly cleared by two other signals: D4-6 TX ERR L and D5-4 0 → TX GO L. These two signals, plus the inversion of D5-4 INI H, are sent to 3-input AND gate E34 pins 10, 9, and 11, respectively. This gate is shown as the logically-equivalent negative OR. When any input signal is low, the output goes low and bit 0 is directly cleared. Signal D4-6 TX ERR L is generated in the output gating of the REG/ERR when any one of several TX errors is detected. Signal D5-4 0 → TX GO L is generated by the character count control logic when the CC register overflows. Occurrence of these conditions demands that bit 0 (TX GO) be cleared to prevent the transmit data transfer.

Bits 0, 1, 3, and 5 are set by the program. Bits 6 and 7 are directly set by the hardware using the flip-flop preset input. They are cleared by the program using the D-input and clock input. Bit 6 (TX S DONE) is set when D5-4 1 → TX S DONE L goes low. This signal comes from the CC register control logic (print D5-4) and is generated when the transmitter secondary character count register overflows. Bit 7 (TX P DONE) is set when D5-4 → TX P DONE L goes low. This signal is generated when the transmitter primary character count register overflows.

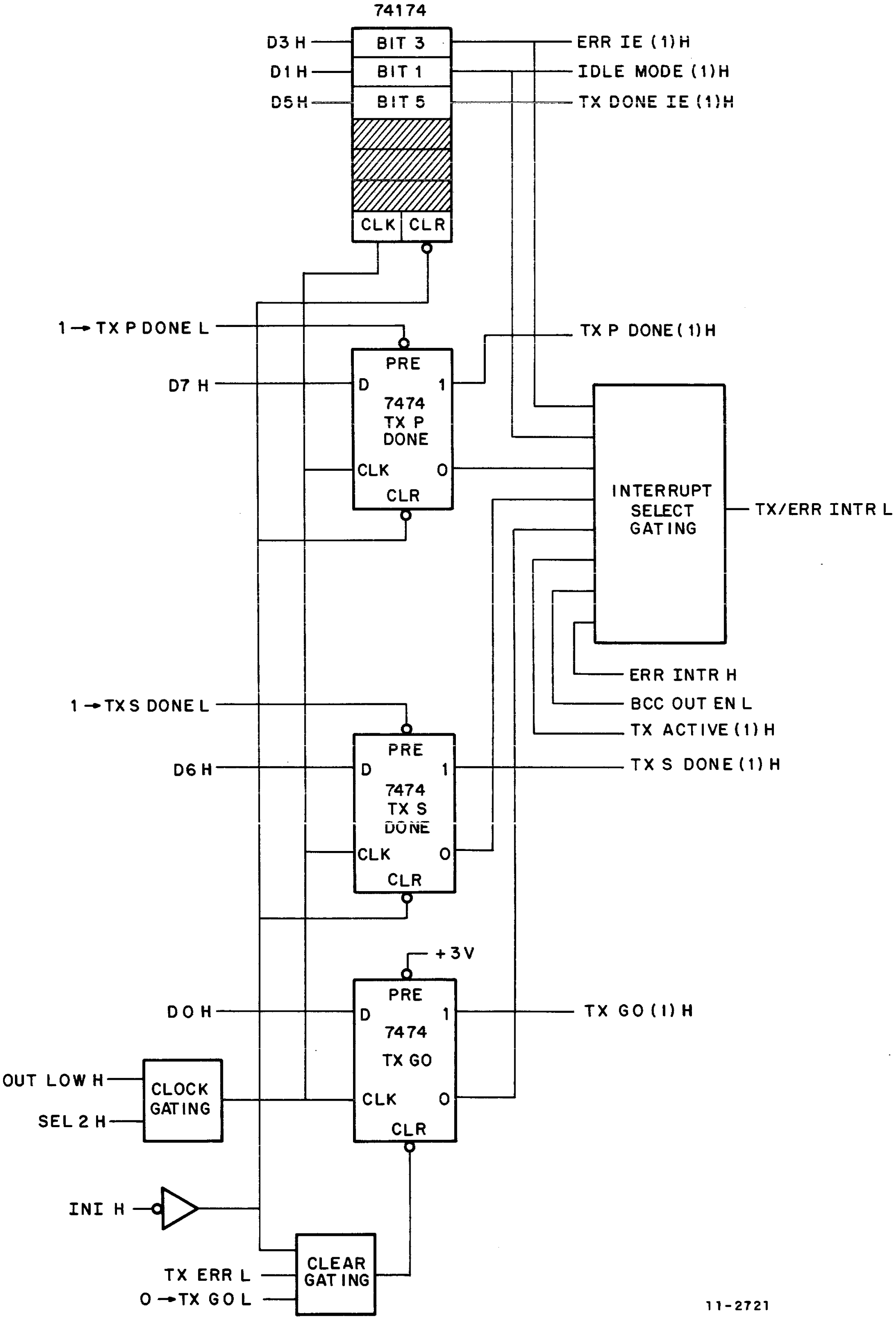


Figure 4-16 Block Diagram of Transmitter Control and Status Register

The outputs of some of these six TX CSR bits are combined in a 74H55 AND-OR-invert gate (E27) to generate D4-4 TX/ERR INTR L which is sent to the interrupt control logic on the M7813 module (print D5-5) to generate the signal that initiates the request for an interrupt under vector B (XX4).

Gate E27 has two input sections; each one is a 4-input AND gate. One section (pins 10–13) allows error conditions, as represented by D4-6 ERR INTR H, to generate D4-4 TX/ERR INTR L, provided the error interrupt enable bit (D4-4 ERR IE (1) H) is asserted. The other section (pins 1–4) allows TX S DONE and TX P DONE to generate D4-4 TX/ERR INTR L, provided the transmit done interrupt enable bit (D4-4 TX DONE IE (1) H) is asserted. Another qualifying input to this section is obtained by combining the 0 output of the TX GO flip-flop and D5-6 TX ACTIVE (1) H at NAND gate E26. With this arrangement, TX S DONE or TX P DONE cannot initiate an interrupt if the TX GO flip-flop is cleared and D5-6 TX ACTIVE (1) H is asserted.

4.4.5 Receiver Control and Status Register

4.4.5.1 Functional Description – A simplified block diagram of the Receiver Control and Status Register (RX CSR) is shown in Figure 4-17. This discussion, and the detailed discussion that follows, covers the operation of the RX CSR and its associated logic. A register bit map and functional description of each bit is covered in Chapter 3, Programming.

Only eight bits of the RX CSR are shown on this module. The remaining eight bits are located on other modules and are described in the discussion of the applicable module. Bits 2 and 12 are located on the M7813 module (prints D5-4 and D5-7, respectively). Bits 8–11 are located on the M7818 module (print D6-1) or on the M7817 module (print D8-3) if the DQ11-BB option is installed. Bits 13 and 14 are located on the M7815 module (print D2-1).

The RX CSR is word- and byte-addressable. On this module, all eight bits are contained in D-type flip-flops and are clocked simultaneously when the register is addressed during a DATO transaction. Bits 0, 1 and 3–7 are clocked during a DATOB (low byte) transaction and bit 15 is clocked during a DATOB (high byte) transaction.

4.4.5.2 Detailed Logic Description – The circuit schematic for the RX CSR is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 6 which is designated D4-4.

Bits 1, 3, 4, and 5 are contained in a 74174 hex, D-type flip-flop (E45). Two sections of E45 are not used. These bits have a common clock and clear input. Bits 0, 6, 7, and 15 are contained in separate 7474 D-type flip-flops. The clock for bits 0, 6 and 7 is the same one that is used for bits 1, 3, 4, and 5. Bit 15 uses a different clock signal. All eight bits are directly cleared by D5-4 INI H which is generated as a result of BUS INIT L or MASTER CLEAR which is bit 5 of the MISC register.

The clock signal for bits 0, 1 and 3–7 is generated at E33 pin 11. A positive transition is generated at this point when the RX CSR is addressed during a DATO or DATOB (low byte) transaction. The signals involved are D3-1 SEL 0 H and D3-1 OUT LOW H from the M105 Address Selector. The clock signal for bit 15 is generated at E33 pin 8. It is generated when the RX CSR is addressed during a DATO or DATOB (high byte) transaction. The signals involved are D3-1 SEL 0 H and D3-1 OUT HIGH H from the M105 Address Selector.

As stated previously, direct clearing of all bits is performed by D5-4 INI H. This signal is inverted by E25 and sent to the direct clear input of each flip-flop. A low level clears the flip-flop. Bit 0 of the RX CSR can be directly cleared by two other signals. D4-6 RX ERR L and D5-4 0 → RX GO L. These two signals, plus the inversion of D5-4 INI H, are sent to 3-input AND gate E34 pins 2, 1, and 13, respectively. This gate is shown as the logically-equivalent negative OR. When any input signal is low, the output goes low and bit 0 is directly cleared. Signal D4-6 RX ERR L is generated in the output gating of the REG/ERR register when any one of several errors is detected. Signal D5-4 0 → RX GO L is generated by the character count control logic when the CC register overflows. Occurrence of these conditions demands that bit 0 (RX GO) be cleared to prevent the receive data transfer.

Bits 0, 1, 3, 4, and 5 are set by the program. Bits 6, 7, and 15 are directly set by the hardware using the flip-flop preset input. They are cleared by the program using the D-input and the clock input. Bit 15 (CHAR INTR) is set when D6-1 1 → CHAR INTR L goes low. This signal comes from the hard-wired character detection logic (M7818 module) when a selected character has been detected or from the programmable character detection logic (M7817 module) if the DQ11-BB option is installed.

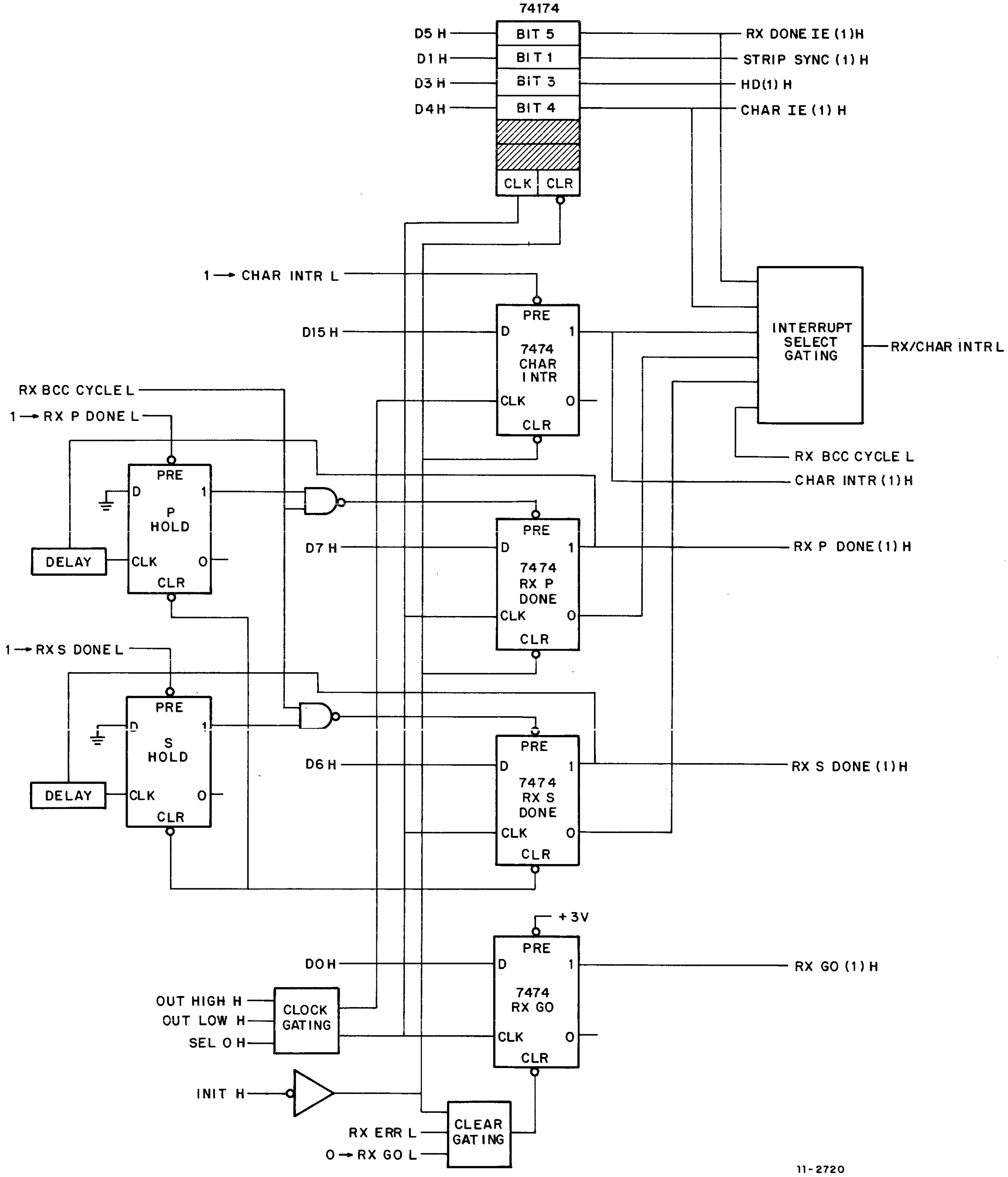


Figure 4-17 Block Diagram of Receiver Control and Status Register

Bits 6 and 7 are set when the respective receiver character count registers overflow (secondary register for bit 6 and primary register for bit 7). In each case, the signal that is generated at overflow (D5-4 1 → RX P DONE L or D5-4 1 → RX S DONE L) is not sent directly to the respective RX CSR flip-flops; that is, RX P DONE and RX S DONE. The overflow signal sets a holding flip-flop (P HOLD or S HOLD) whose output is gated with a signal from the BCC control logic (module M7816) and is then sent to RX P DONE or RX S DONE. This logic is used to prevent these flip-flops from being set until an in-process BCC cycle is finished. The BCC feature is not part of the basic DQ11-AA option but it is appropriate to mention it in this discussion. Both holding circuits are identical; only the one associated with flip-flop RX P DONE is discussed.

When the receiver primary character count register overflows, signal D5-4 1 → RX P DONE L is generated. This signal is sent to the preset input (pin 10) of the P HOLD flip-flop which directly sets it. The high at the 1 output of P HOLD is sent to pin 12 of 2-input NAND gate E41. If the BCC cycle is not in progress, the other E41 input (pin 13) floats high. The low output (pin 11) of E41 sets the RX P DONE flip-flop via its preset input (pin 10). The positive transition at the 1 output of RX P DONE is fed back via an RC delay to clock the P HOLD flip-flop. This clears the flip-flop because its D-input is permanently connected to ground.

The outputs of some of these eight RX CSR bits are combined in a 74H55 AND-OR-invert gate (E44) to generate D4-4 RX/CHAR INTR L, which is sent to the interrupt control logic on the M7813 module (print D5-5) to generate the signal that initiates the request for an interrupt under vector A (XX0).

Gate E44 has two input sections; each one is a 4-input AND gate. One section (pins 10–13) allows CHAR INTR to generate D4-4 RX/CHAR INTR L, provided the character interrupt enable bit (D4-4 CHAR IE (1) H) is asserted. The other section (pins 1–4) allows RX P DONE and RX S DONE to generate D4-4 RX/CHAR INTR L, provided the receiver done interrupt enable bit (D4-4 RX DONE IE (1) H) is asserted.

4.4.6 Register Pointer and Error Control and Status Register (REG/ERR CSR)

4.4.6.1 Functional Description – A simplified block diagram of the REG/ERR CSR is shown in Figure 4-18. This discussion, and the detailed discussion that follows, covers the operation of the REG/ERR CSR and its associated logic. A register map and functional description of each bit is covered in Chapter 3, Programming.

All REG/ERR CSR bits except one (bit 12) are shown on this module. Bit 12 is located on the M7813 module and is described in the discussion of this module.

The REG/ERR CSR is word- and byte-addressable. On this module, 14 bits are contained in D-type flip-flops. The remaining bit (15) is obtained by ORing the outputs of the register low order byte (bits 0–7). All 14 bits (bit 15 excluded) are clocked simultaneously during a DATO transaction. Bits 0–7 are clocked during a DATOB (low byte) transaction. Bits 8–11, 13 and 14 are clocked during a DATOB (high byte) transaction.

4.4.6.2 Detailed Logic Description – The circuit schematic for the REG/ERR CSR is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 8 which is designated D4-6.

Bits 0–7 are contained in two 4015 quad D-type flip-flops (E5 and E6). This type flip-flop has common clock and direct clear inputs; however, each of the four sections has a separate preset input labeled SET. Bits 8–11, 13, and 14 are contained in a 74174 hex, D-type flip-flop (E7) which has common clock and direct clear inputs. All bits in E5, E6 and E7 are directly cleared by D5-4 INI H which is inverted by E25 before being applied to the CLR inputs of E5, E6, and E7.

Bits 0–7 are clocked by signal D5-4 LD ERR H and bits 8–11, 13, and 14 are clocked by signal D5-4 LD PTEE H. These clock signals are generated simultaneously on the M7813 module (print D5-4) when the REG/ERR CSR is addressed during a DATO transaction. Signal D5-4 LD ERR H is generated also during a DATOB (low byte) transaction. Signal D5-4 LD PTEE H is generated also during a DATOB (high byte) transaction.

Bits 0–7 are error bits and are set by the hardware using the flip-flop preset input. They are cleared by the program using the D-input and clock input. In all but two of these bits, the setting signal is sent directly to the preset input of the flip-flop. The exceptions are bits 4 and 5 that detect transmitter and receive non-existent memory errors. When non-existent memory is addressed, the TIME OUT flip-flop on the M7818 module is set which generates D6-2 TIME OUT (1) H. This signal is combined with D5-3 TX CYCLE H and D6-2 TIME OUT H in separate NAND gates (E8). For example, if non-existent memory is addressed during a transmit cycle, both D5-3 TX CYCLE H and D6-2 TIME OUT H are asserted.

The output (pin 6) of E8 goes low and sets bit 4 of the REG/ERR CSR via its preset input. This generates the transmit non-existent memory flag (D4-6 TX NON MEM (1) H).

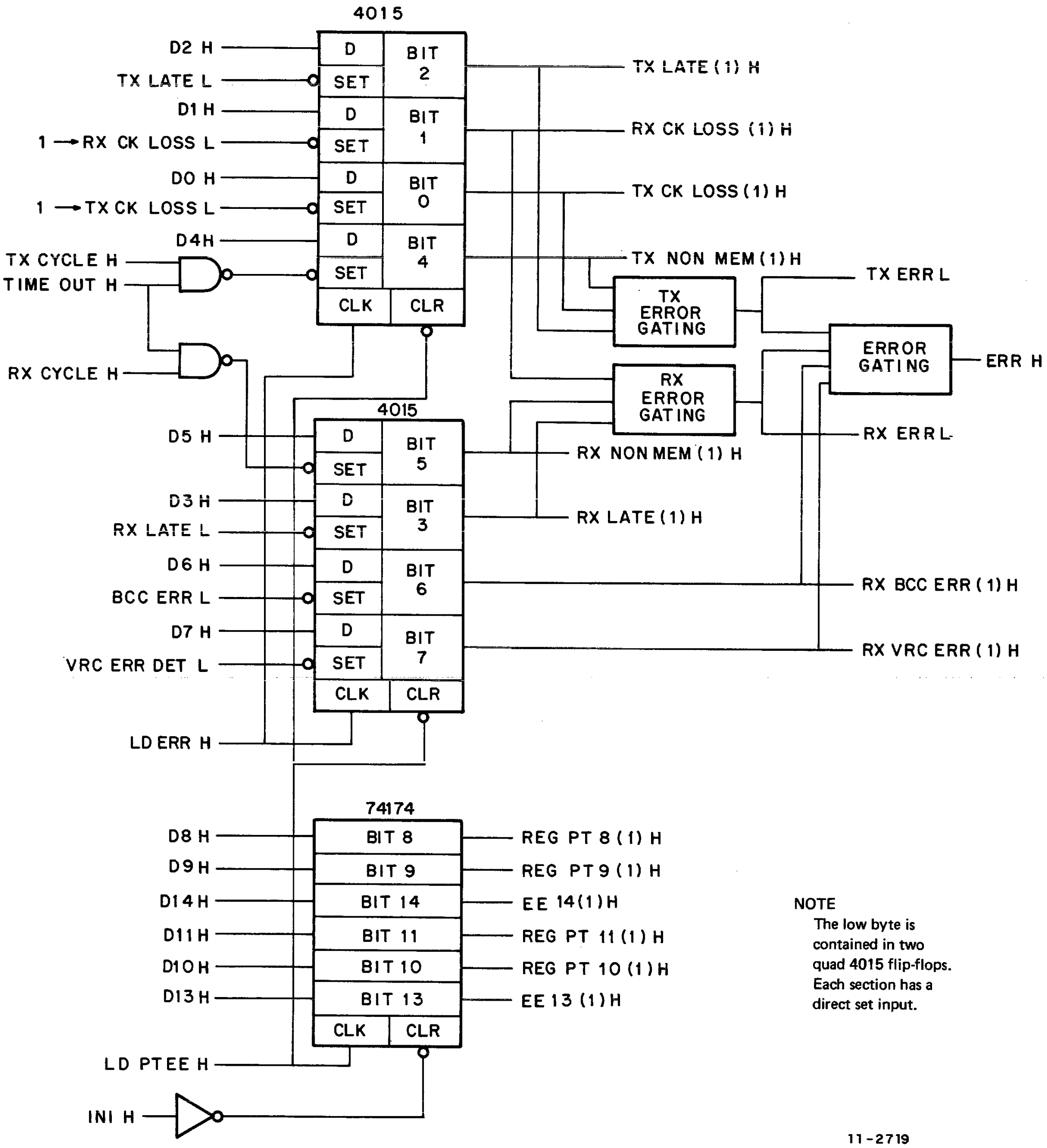


Figure 4-18 Block Diagram of REG/ERR Control and Status Register

The preset input (SET 1) for bit 6 is connected to D9-6 BCC ERR L and to +5 V via resistor R20, in parallel. Signal D9-6 BCC ERR L is not used unless the DQ11-BB option (M7817 module) is installed. Without the M7817 module installed, the preset input is inhibited by the +5 V.

Three receive error flags (bits 1, 3, and 5) are ORed and three transmit error flags (bits 0, 2 and 4) are ORed to generate a signal that clears the respective GO flip-flop in the RX CSR and TX CSR when an error is detected. Signals D4-6 TX CK LOSS (1) H (bit 0), D4-6 TX LATE (1) H (bit 2), and D4-6 TX NON MEM (1) H (bit 4) are sent to 4-input NOR gate E14 pins 9, 12, and 10, respectively. Pin 13 is permanently connected to ground. If an error flag is set, the output (pin 8) of E14 goes low and asserts D4-6 TX ERR L. This signal is sent to the clear input of the TX GO flip-flop (print D4-4). A similar arrangement is used for the RX error flags to generate D4-6 RX ERR L which clears the RX GO flip-flop (print D4-4).

Signals D4-6 RX BCC ERR (1) H (bit 6) and D4-6 RX VRC ERR (1) H are sent to the inputs of NOR gate E15. The output of this gate is sent to pin 9 of NAND gate E24 which is shown as the logically-equivalent, negated-input OR. Pins 10 and 11 of E24 are connected to the outputs of the above mentioned E14 gates. This arrangement allows any one of eight error flags to generate D4-6 ERR INTR H when an error has been detected. This signal is bit 15 of the REG/ERR CSR and allows an error to generate an interrupt.

4.4.7 Sync Register (SYNC) and Transmitted Data Output Logic

4.4.7.1 Functional Description – A simplified diagram of the SYNC register is shown in Figure 4-19. It is a programmable 16-bit register. The desired sync character is loaded by the program into the SYNC register. The output of the SYNC register is compared with the output of the receiver buffer register which contains the received sync word. If they match, signal D4-7 RX SYNC DET H is generated and goes to the M7813, M7816, M7817 and M7818 modules.

The output of the SYNC register is also sent to two 8-bit multiplexers that perform parallel-to-serial conversion of the sync character and send it out as a transmitted character.

4.4.7.2 Detailed Logic Description – The circuit schematic for the SYNC register is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 9 which is designated D4-7. The SYNC register is composed of three 74174 hex flip-flops. Bits 0–5 are stored in E31; bits 6–9 are stored in E30; and bits 10–15 are stored in E28. The inputs come from the Unibus data lines via receivers on prints D4-1 and D4-2. The input signals are identified as D4-1 D0 H to D4-1 D7 H and D4-2 D8 H to D4-2 D15 H. All bits are directly cleared simultaneously by D4-3 CLR SYN L which is the inversion of D5-4 INI H. All bits are clocked simultaneously by D5-4 LD SYNC L. This signal is generated by the secondary register pointer decoder on the M7813 module (print D5-4). The SYNC register is selected when REG/ERR CSR bits 8–11 indicate 11_8.

If the receiver is not framed, a bit-by-bit sync search is performed by loading the RX shift register outputs into the RX buffer. In this way, the RX shift register is compared with the sync register. The SYNC register outputs are D4-7 S0 (1) H to D4-7 S15 (1) H. Each output goes to one input of a 2-input 8242 comparator. The other input of each comparator is connected to the corresponding bit from the output of the receiver buffer (print D4-5). These inputs are identified as D4-5 RD 0 H to D4-5 RD 15 H. The SYNC register is loaded with the desired sync character and when it is detected in the receiver buffer, both inputs to each 8242 comparator are identical. The comparator is an exclusive-NOR and its output is high only when both inputs are identical. It has a bare collector so that several comparator outputs can be connected together (wire-ORed connection). The outputs of the comparators for the high byte (bits 8–15) are connected together and tied to +5 V through common-collector resistor R13. The wire-ORed output of the high byte is also sent to pin 2 of NAND gate E68 and pin 1 of NAND gate E66. A similar arrangement wire-ORs the low bytes (bits 0–7) comparators and sends the output to pin 2 of E66. This hardware configuration requires that if a sync character of eight bits or less is desired, the same character must be loaded into each byte. All unused bits must be set to 0. The least significant bit (LSB) is right-justified.

Gate E66 and two E68 gates form a network that samples the comparator outputs and bit 11 of the MISC register to generate D4-7 RX SYNC DET H. This signal is asserted when a correct sync character is detected and it is sent to the M7813, M7816, M7817 and M7818 modules.

Both bytes are used for characters of 9–16 bits. The high byte only is used for characters of 1–8 bits and the low byte is ignored. This is an operation function of the receiver buffer.

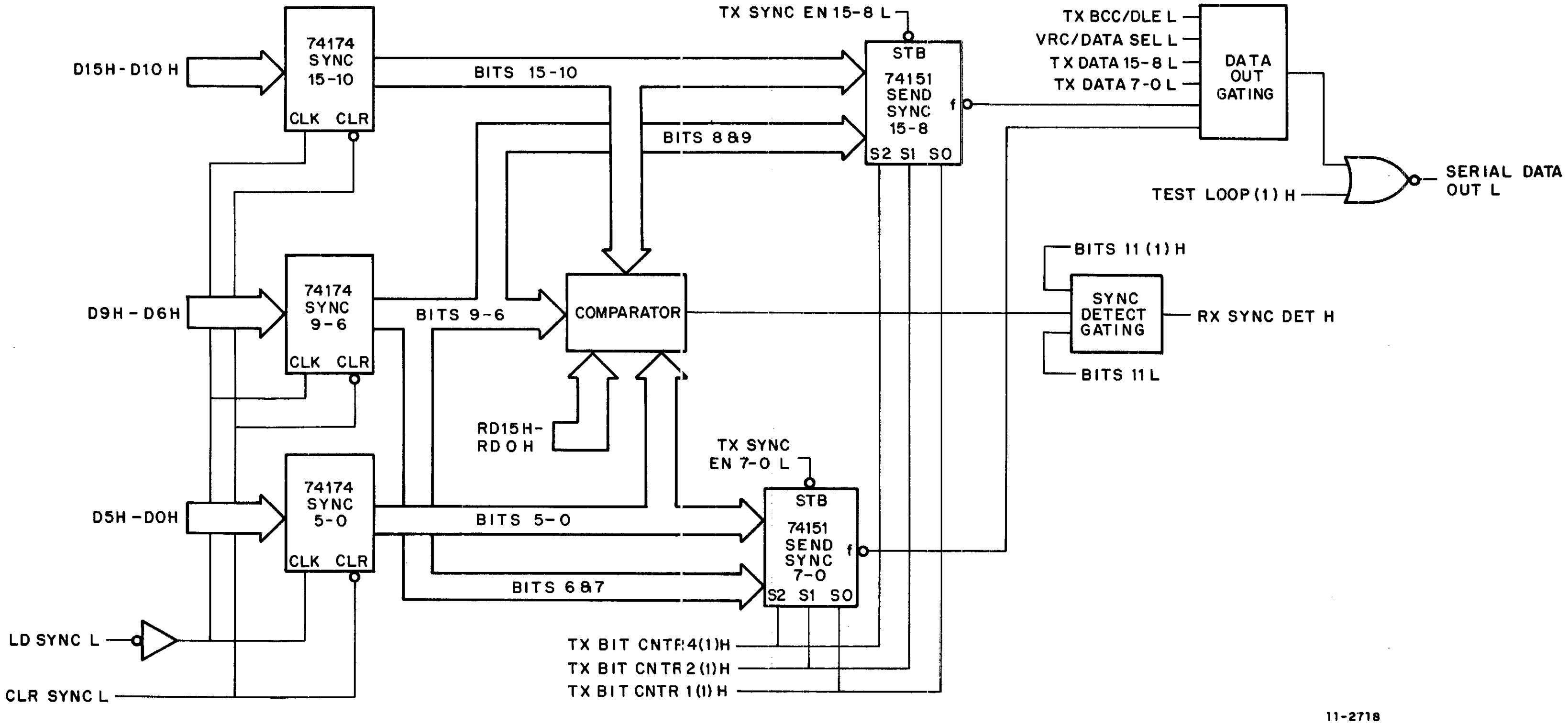


Figure 4-19 Block Diagram of SYNC Register

As stated previously, the wired-OR output of the high byte is sent to pin 2 of E68 and pin 1 of E66; and the wired-OR output of the low byte is sent to pin 2 of E66. The other pin of each gate is connected to the output of bit 11 of the MISC register. This bit is the MSB of the four bits (8–11) that select the bits-per-character. It is high if the bits-per-character selected is 1–8 and is low if the bits-per-character selected is 9–16. Signal D4-3 BITS 11 (1) H is sent to E68 pin 1 and its inversion D4-5 BITS 11 L is sent to E66 pin 13. When a sync character is detected, either E68 pin 3 or E66 pin 12 goes low, depending on the bits-per-character selected. These outputs are connected to pins 4 and 5, or E68, so that either one can generate D4-7 RX SYNC DET H at the output (pin 6) of E68.

During transmission, the selected sync character, which is stored in the SYNC register, is serialized by two 74151 multiplexers (E29 and E32) and sent out to the data set. Each multiplexer handles 8 bits of the SYNC register. Complementary outputs are provided, but only the output (pin 6) that is the inversion of the input is used. The same selection signals are used for both multiplexers: D5-6 TX BIT CNTR 4 (1) H, D5-6 TX BIT CNTR 2 (1) H, and D5-6 TX BIT CNTR 1 (1) H. These signals represent a 3-bit BCD code that selects one of eight inputs (D0–D7). They are outputs of the TX BIT COUNTER (print D5-6) that counts in accordance with the number of bits-per-character selected. Each multiplexer has a separate enable input (pin 7) that must be low to enable the multiplexer. The enabling signal for the low byte (E32) is D5-6 TX SYNC EN 7–0 L and for the high byte (E29) it is D5-6 TX SYNC EN 15–8 L. The transmitter control logic on the M7813 module (print D5-6) controls assertion of the enabling inputs to all of the proper number of bits to be serialized by the multiplexers.

The output of each multiplexer goes to an input of E23. This 8-input NAND gate, which is shown as the logically-equivalent, negated-input OR, is the place where all transmitted information leaves the DQ11 for the data set. This information includes both bytes of the SYNC register, both bytes of the transmitter data register, VRC bit, and BCC information. Signal D9-4 TX BCC/DEL L is used only when the DQ11-AB option (M7816 module) is installed. When the M7816 module is not installed, pin 12 of E23 is held high permanently by the +5 V through R10. Gate E23 inverts each input and sends it to pin 8 of NOR gate E67. The signal on this line (D4-7 TX DATA H) is sent to the BCC register which is present only in the DQ11-AB option. The other input (pin 9) of E67 is D4-3 TEST LOOP (1) H which is low during normal operation. The information to be transmitted (pin 8) is thus inverted and is sent to the data set as D4-7 SERIAL DATA OUT L. When the test loop mode is used during servicing, D4-3 TEST LOOP (1) H is asserted and the output of E67 (D4-7 SERIAL DATA OUT L) is held low.

4.4.8 Transmitter Shift Register

4.4.8.1 Functional Description – A simplified block diagram of the transmitter shift register is shown in Figure 4-20. This discussion, and the detailed description that follows, covers the operation of the transmitter shift register.

The transmitter shift register consists of a buffer, shift holding register and send-data selector. Data to be transmitted comes from the Unibus and is clocked into the buffer by LD TX BUF (1) H. The data is sent from the buffer to the shift hold register and is clocked in by LD TX SH REG H. From this register, the information is sent to the send-data selector. This register is enabled by bytes using signals TX DATA EN 7–0 L and TX DATA EN 15–8 L. A counter in the transmitter shift control logic provides the select signals that ripple through the send-data selector to serialize the input data by bytes.

4.4.8.2 Detailed Logic Description – The circuit schematic for the transmitter shift register is contained in drawing D-CS-M7812-0-1 (Rev D) sheet 7 which is identified as D4-5.

Data to be transmitted comes from the Unibus data lines via bus receivers (prints D4-1 and D4-2). The information is identified as D4-1 D0 H to D4-1 D7 H and D4-2 D8 H to D4-2 D15 H and is sent to the transmitter buffer. This buffer is composed of three 74174 hex flip-flops: E10 for bits 15–10, E12 for bits 9–6, and E13 for bits 5–0. The data goes to the D inputs of the 74174s and is clocked to output on the positive transition of clock signal D6-2 LD TX BUF (1) H. This signal comes from the NPR control logic on the M7818 module.

The output of the buffer goes to the transmitter shift hold register that is composed of three 74174 hex flip-flops: E19 for bits 15–10, E11 for bits 9–6, and E22 for bits 5–0. The 74174s are clocked by D5-6 LD TX SH REG H from the transmitter control logic on the M7813 module.

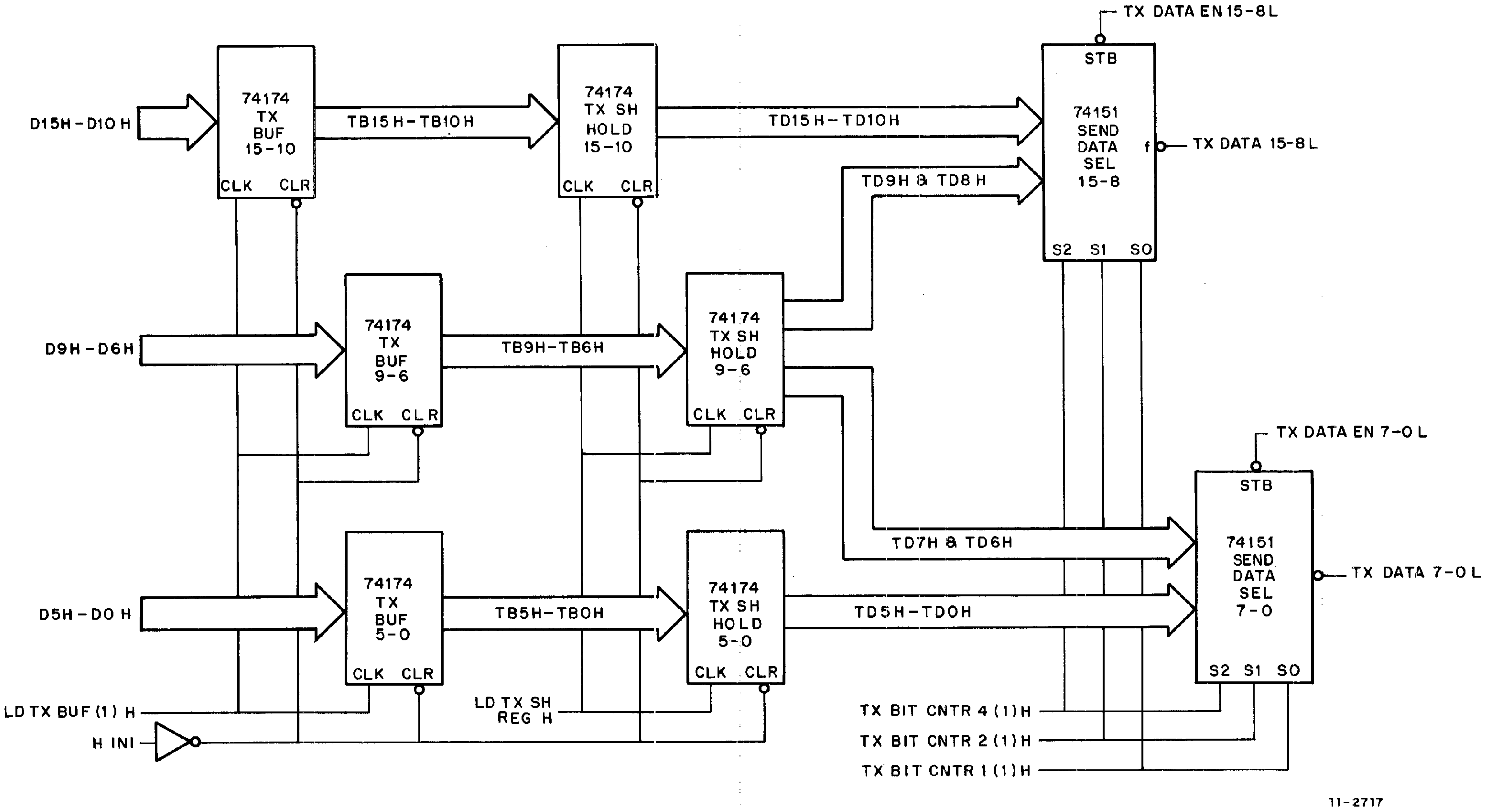


Figure 4-20 Block Diagram of Transmitter Shift Register

The output of the shift hold register is sent to the input of the send-data selector that is composed of two 74151 1-of-8 multiplexers: E20 for the high byte (bits 15–8) and E21 for the low byte (bits 7–0). The multiplexers have complementary outputs but only the one that gives the inverse of the input is used. The select inputs (S2, S1, and S0) of both multiplexers are controlled by the TX BIT counter in the transmitter control logic on the M7813 module. The counter ripples through the selected count (0–7 maximum) to select each input in order which performs a parallel-to-serial conversion of data from input to output. Each multiplexer has a separate enabling (STB) input from the transmitter control logic: D5-6 TX DATA EN 7–0 L for the low byte and D5-6 TX DATA 15–8 L for the high byte. The low byte serial output is D4-5 TX DATA 7–0 L and the high byte serial output is D4-5 TX DATA 15–8 L. The transmitter control logic enables the multiplexers in sequence.

4.4.9 Receiver Shift Register and Receiver Data Register

4.4.9.1 Functional Description – A simplified block diagram of the receiver shift register and data register is shown in Figure 4-21.

The 16-bit shift register stores the received character in accordance with the number of bits per character selected (1 through 16). Characters of nine bits or over are single characters; whereas characters of eight bits or less are shifted into both bytes of the register to provide double characters. Entry of the received serial data into the correct bit position of the register is provided by the receiver data decoder. Bits 8–11 of the MISC register determine the number of bits per character (Chapter 3). The output of MISC register bits 8–11 is sent to the receiver data decoder to control the data entry point.

The receiver shift register is clocked by RX CLOCK H which is the clock signal that comes with the data from the data set.

The shift register output is loaded into the receiver buffer by bytes: signal LD RX BUF 15–8 L loads the high byte and signal LD RX BUF 7–0 L loads the low byte. Loading by bytes is required because of the character stripping function. The output of this buffer is again buffered before being sent to the Unibus data lines.

4.4.9.2 Detailed Logic Description – The circuit schematic for the receiver shift register is contained in drawing D-CS-M7812 (Rev D) sheet 7, which is designated D4-5. The receiver shift register is a unique device that allows serial data to be entered at any 1 of 16 bit positions and shifted until the character reaches the selected length. It is composed of four 74175 quad D-type flip-flops, sixteen 2-input X-OR gates and two 7442 octal decoders. It is called the Lisee Super Shifter (LSS), which is a name worthy of its uniqueness.

The storage section of the register consists of four 74175 quad D-type flip-flops. Each one handles four bits of the register as follows: bits 15–12 (E87), bits 11–8 (E86), bits 7–4 (E85), and bits 3–0 (E84). All bits are clocked by the data set clock that is designated D4-3 RX CLOCK H. All bits are directly cleared by D5-7 CLR RX L which comes from the shift control logic on the M7813 module. The 74175s have complementary outputs. The 1 outputs are sent to the inputs of the receiver buffer. Each 0 output (except bit 0) is fed back to one input of a 2-input X-OR gate that is connected to the D-input of the next least significant bit. The register is divided into two bytes. On a byte basis (8 bits), the other input of each X-OR gate is connected to an output of the 7442 receiver data decoder (E79 for bits 15–8 and E88 for bits 7–0).

The 7442 is a 4-line-to-10-line decoder but in this application it is used as a 3-wire binary-to-octal decoder. Three of the four inputs (D0, D1 and D2) are used to select 1 of 8 outputs that are designated f0–f7. The fourth input (D3) is the enabling input which must be low to enable the decoder.

The selection bits (inputs D0, D1 and D2) come from bits 8–10 of the MISC register which select the number of bits per character. The enabling signal (input D3) for the high byte decoder (E77) is D4-3 SERIAL DATA IN L. The enabling signal for the low byte decoder (E88) is D4-3 BITS 11 (1) H from the MISC register and the 1 output of bit 8 from the receiver shift register combined in NAND gate E69.

The operation of the receiver shift register is described in the following example.

Assume that data is being received and the register has been selected to process the data as 8-bit characters. Remembering that characters of 8 bits or less are handled as double characters, an 8-bit character is loaded into each byte of the register.

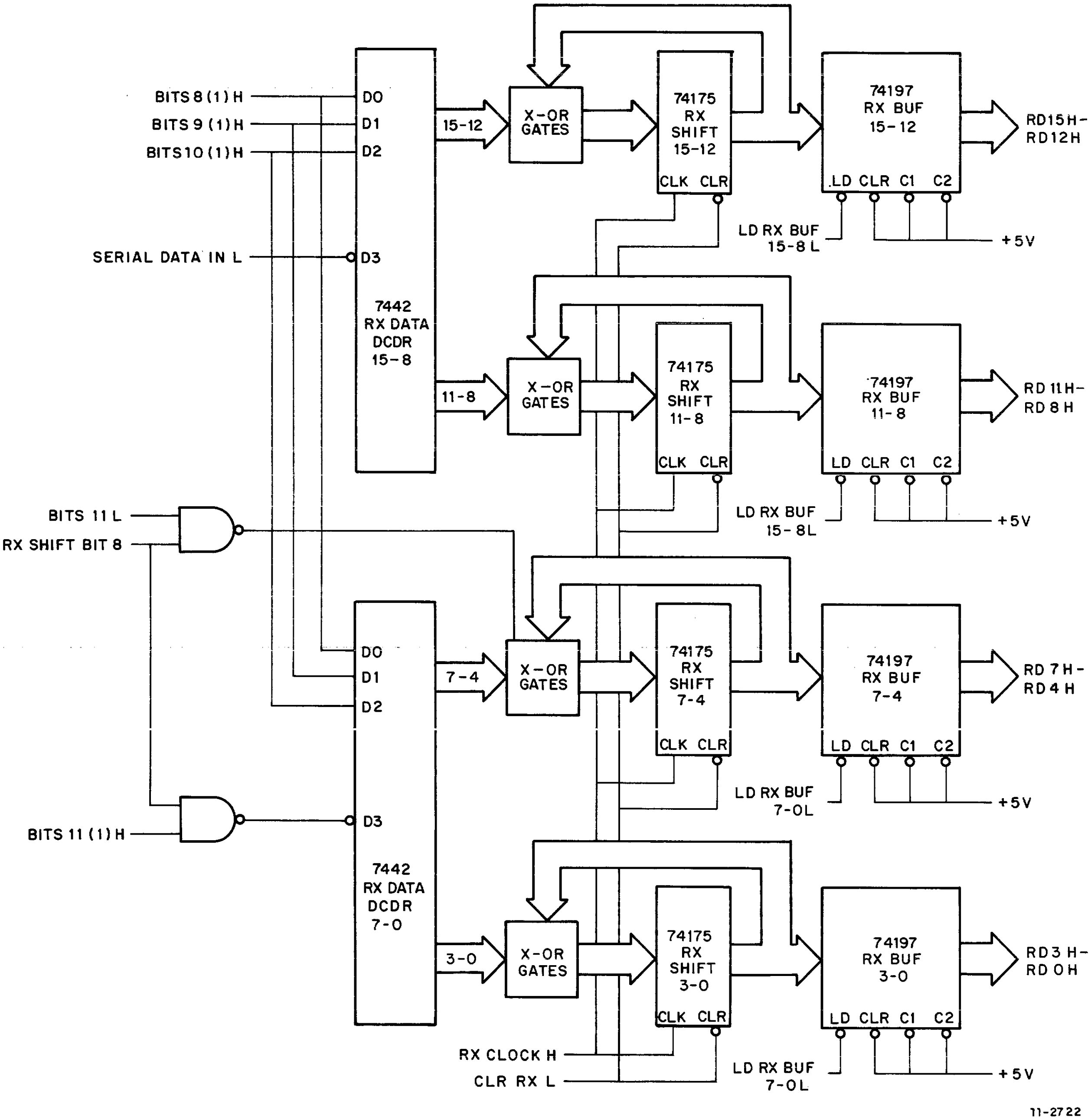


Figure 4-21 Block Diagram of Receiver Shift Register

In the following discussion, the state of the received character bit (D4-3 SERIAL DATA IN L) is stored in complementary form in the register; for example, a low received data bit is stored as a high in the register. This is done to adhere to the convention of representing a mark and space properly as shown below.

Mark Data Set	Unibus Data Lines
Mark = Low = Logical 1	Low = Logical 1 (Mark)
Space = High = Logical 0	High = Logical 0 (Space

The input data (D4-3 SERIAL DATA IN L) is inverted by the X-OR gates to comply with the convention for signal states.

Prior to receiving data, assume that the register has been cleared.

1. The decoder selection signals (D4-3 BITS 8 (1) H, D4-3 BITS 9 (1) H, and D4-3 BITS 10 (1) H) are all low. This selects output f0 of both decoders (E79 and E88). Outputs f1–f7 are not selected and remain high.

2. For decoder E79, output f0 follows signal D4-3 SERIAL DATA IN L which is the strobe input (D3) of the decoder. Actually, the decoder is enabled when D3 is low and is disabled when D3 is high.

3. For decoder E88, output f0 follows strobe input D3; however, the strobe signal comes from NAND gate E69 pin 8. This signal is a function of D4-3 BITS 11 (1) H which is high and the 1 output of receiver shift register bit 8 (E86 pin 2).

4. The 1 output of register bit 8 is also combined with D4-5 BITS 11 L at NAND gate E69 pins 13 and 12, respectively. Signal D4-5 BITS 11 L is the inversion of D4-3 BITS 11 (1) H and so it is low. This means, that the output (pin 11) of E69 remains high, regardless of the state of the 1 output of register bit 8. This keeps a high on input pin 13 of X-OR gate E76 whose output (pin 11) is sent to the D input of register bit 7 (E85 pin 12). The other input (pin 12) of the X-OR gate is low or high depending on whether the E88 decoder is enabled or disabled.

5. The output (pin 6) of inverter E58 keeps a high on input pin 1 of X-OR gate E78 whose output (pin 3) is sent to the D input of register bit 15 (E87 pin 4). The other input (pin 2) of the X-OR gate comes from decoder output f0, therefore, it follows the state of D4-3 SERIAL DATA IN L at input D3 because an 8-bit character length has been selected (output f0 enabled).

6. Outputs f1–f7 from both decoders remain high. Each one goes to an X-OR gate input; specifically, those associated with bits 14–8 and 6–0.

7. Assume now that received data (D4-3 SERIAL DATA IN L) and the receiver clock (D4-3 RX CLOCK H) are present. Each data bit is accompanied by a clock pulse that clocks (shifts) the register on the positive transition of the pulse.

As the data and clock pulses arrive, the receiver shift register functions as follows for this example (double 8-bit characters).

1. The receiver starts in the cleared state. Assume that the first received bit (D4-3 SERIAL DATA IN L) is low. This signal enables decoder E79 and a low, corresponding to the first received bit, is generated at decoder output f0. This puts a low on input pin 2 of X-OR gate E78. The other input (pin 1) of this gate is held high permanently by E58. With a low and a high on its inputs, the output (pin 3) of X-OR gate E78 goes high. This signal goes to the D input of register bit 15 (E87 pin 4). When D4-3 RX CLOCK H goes high, bit 15 is set. Its 1 output (pin 2) is sent to the receiver buffer input. Its 0 output, which is low, is fed back to input pin 13 of X-OR gate E78 that is associated with register bit 14. The other input (pin 12) of this X-OR gate is held high by decoder output f1. The bit 14 X-OR gate is now set up just like the bit 15 X-OR was set previously. When the second clock pulse occurs, bit 14 is set. The high in bit 15 has been shifted down to bit 14. The state of bit 15, after the second clock pulse, is determined by the state of the second bit of the received character and is shifted to bit 14 on the third clock pulse.

2. After the first bit of received data is shifted to register bit 8, the high byte of the register contains an 8-bit character justified to the least significant bit position (bit 8). It is desired to continue the shifting until this character is in the register low byte and a new character is shifted into the high byte.

3. The 1 output of register bit 8 (E86 pin 2) is sent to NAND gate E69 pin 9. The other input (pin 10) of this gate is D4-3 BITS 11 (1) H which is high because 8 bits per character is selected. The output (pin 8) of E69 goes to the strobe input of decoder E88.

4. The eighth clock pulse sets register bit 8. The output of this bit (E86 pin 2) is high, which via E69 pin 8, drives the strobe input of decoder E88 low to enable output f0. The signal from f0 goes to input pin 12 of X-OR gate E76. The other input (pin 13) comes from NAND gate E69 pin 11 which is held high because one of its inputs (D4-5 BITS 11 L) is low when 8 bits per character is selected. The high and low inputs on X-OR gate E76 drive its output (pin 11) high. This signal is the D input to register bit 7. The ninth clock pulse sets register bit 7. The process continues until this high, which represents bit 1 of the first received character, reaches register bit 0. Now, the first 8-bit character is in the register low byte (bits 7–0) and the second 8-bit character is in the register high byte (bits 15–8).

The register functions as described above for all double characters (8 bits per character or less). The only change is the point of entry of data into the register as determined by bits 8–11 of the MISC register. For 7 bits per character, the point of entry is register bit 14 via E79 decoder output f1; for 6 bits per character, it is bit 13 via output f2, etc. For charaers of 7 bits or less, the higher numbered stages of the register do not affect the data where it enters the register.

For single characters (9–16 bits per character), the shift register operates the same as described above with the following exceptions.

1. When characters of 9–16 bits are selected, D4-3 BITS 11 (1) H is always low and D4-5 BITS 11 L is always high.

2. With D4-3 BITS 11 (1) H low, the strobe input on decoder E88 is held high via gate E69 pin 8 which disables the decoder. This means that all decoder outputs (f0–f7) remain high.

3. Signal D4-5 BITS 11 L is sent to input pin 12 of NAND gate E69. The other input (pin 13) of this gate comes from the 1 output of register bit 8. The output (pin 11) of E69 is sent to X-OR gate E76 pin 13 which is the D input to register bit 7. With D4-5 BITS 11 L held high, pin 13 of X-OR gate E76 can be either high or low, depending on the state of register bit 8.

Under these conditions, a character of 9–16 bits in length is shifted into the register starting at the high byte and ends up justified to the least significant bit.

The outputs of the shift register are sent to the inputs of the receiver buffer that is composed of four 4-bit 74197 latches: E69 for bits 15–12, E95 for bits 11–8, E94 for bits 7–4, and E93 for bits 3–0. The 74197s are actually presettable binary counters/latches. In this application they are used as latches, only so the counting function is disabled by connecting the clock and clear inputs permanently to +5 V.

When the received character has been loaded into the shift register, the received character control logic on the M7813 module generates two signals that load the received character into the buffer. The signals are D5-7 LD RX BUF 15–8 L, which is sent to the load (LD) input of latches E96 and E95, and D5-8 LD RX BUF 7–0 L, which is sent to the load input of latches E94 and E93. A low signal on the LD input transfers the information at the inputs to the outputs which are identified as D4-5 RD XX H.

The outputs of the receiver buffer is sent to another buffer called the buffered receiver data register (print D4-7). This register is composed of four 74175 quad flip-flops. The input data (D4-5 RD 0 H to D4-5 RD 15 H) is sent to the D inputs of the 74175s and is clocked by D5-3 RX NPR L from the shift control logic on the M7813 module. The output of the buffered receiver data register (D4-7 BRD 0 H to D4-7 BRD 15 H) is sent to the Unibus data lines via the bus selectors (prints D4-1 and D4-2).

4.5 M7813 MODULE (CC/BA AND SHIFT CONTROL)

4.5.1 Introduction

The M7813 module is a hex height, extended length, module that contains several functionally separate logic circuits. They are listed below in order of discussion.

1. Character Count/Bus Address Register

2. Character Count/Bus Address Control Logic

3. Clock Loss, Register Select, and Done Control Logic

4. Interrupt and Vector Control Logic

5. Transmitter Control Logic

6. Receiver Start Up and VRC Logic

7. Receiver Control Logic

4.5.2 Character Count/Bus Address (CC/BA) Register

4.5.2.1 Functional Description – The Character Count/Bus Address Register consists of eight registers as shown below.

Receiver	Transmitter
Primary BA	Primary BA
Secondary BA	Secondary BA
Primary CC	Primary CC
Secondary CC	Secondary CC

These registers are 16 bits long and are composed of four 3101 64 bit read/write semiconductor (TTL) memories, arranged in a 16 word-by-16 bit format. Only eight words (registers) are used.

NOTE

The system memory is always referred to as the PDP-11 memory. This is where received characters and characters to be transmitted are stored. All other use of the word memory refers to DQ11 hardware memories. The word register always refers to DQ11 hardware registers.

A block diagram of the CC/BA register is shown in Figure 4-22. The memory is addressed by three outputs from the CC/BA address multiplexer to select the desired register. The inputs to this multiplexer differentiate between transmit and receive mode, CC and BA, and primary and secondary to choose the desired register.

The BA registers are expandable to 18 bits to allow addressing memories that contain more than 32K words.

The BA register is loaded with the address of the first character to be transmitted (brought from PDP-11 memory to DQ11) or the address of the first received character (sent from DQ11 to PDP-11 memory). The BA register is incremented by the CC/BA counter as each character is transferred. This selects consecutive memory addresses as the memory is read or written into.

The CC register is loaded by the program with the 2's complement of the number of characters to be transferred. The CC register is incremented by the CC/BA counter as each character is transferred; therefore, it is counting character transfers. The CC register and CC/BA counter are 16 bit devices and therefore have 2^{16} or 65,536 states (0–65,535 inclusive). It is not practical to start the counter at 0 and increment it to the desired character count, then stop it and use its output to perform some function. The procedure is simplified by using the 2's complement method. Assume that the desired character count is 220. Convert this to binary and determine the 2's complement of this binary value. Because the counter contains 16 bits, this is a large negative binary number (equivalent decimal magnitude is 65,316). This number is loaded into the counter and it is incremented after each character is processed. After 219 increments, the counter is at its maximum count (65,535) which means that the 16 counter outputs are all 1s (minus 1). At this point, the counter carry-out signal goes high. At the 220th increment, the counter overflows (all outputs go to 0) and the carry-out signal goes low. This positive carry-out pulse is used throughout the logic to perform various functions. All 220 characters have been counted and the fact that the last one has been counted is shown by the carry-out pulse. The carry-out pulse is used by the CC/BA control logic to stop transfers or to continue if the associated CC register (primary or secondary) is loaded with some value, which denotes additional characters to be transferred.

The operation of the CC/BA register in the transmit mode is described below in general.

1. Assume that the selected CC and BA registers have been loaded.

2. The transmit mode requests an NPR transaction.

3. The M7813 control logic sends the request signals to the M7821 Interrupt Module which in turn generates an NPR to the processor.

4. When the processor responds with an NPG, the M7821 asserts MASTER A L.

5. MASTER A L is sent to the NPR control logic on the M7818 module to allow the DQ11 to become bus master and perform a DATI transaction to bring the first character for transmission from memory to the DQ11. MASTER A L also places the bus address on the Unibus data lines for decoding by the memory during the DATI transaction.

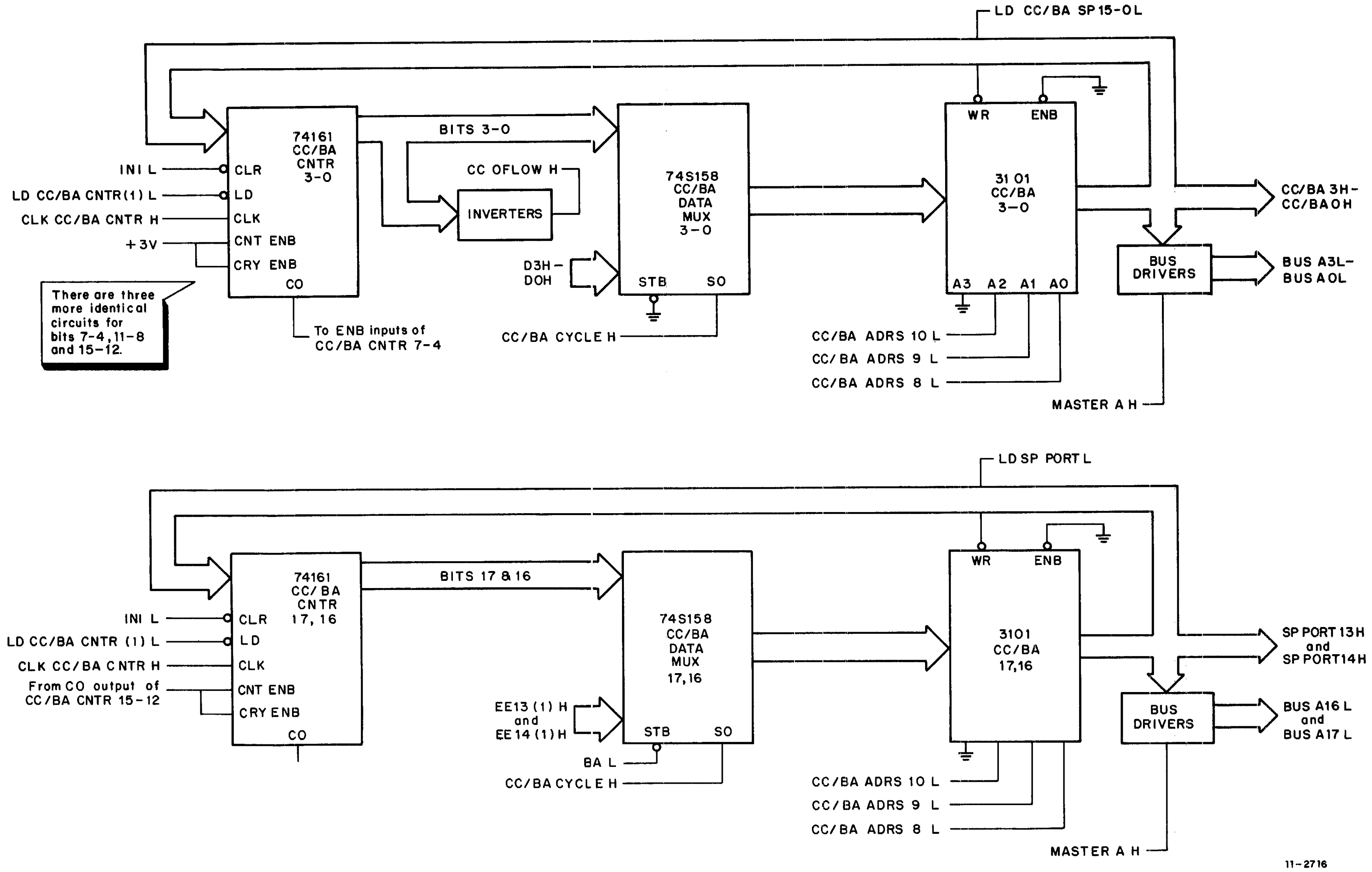


Figure 4-22 Block Diagram of CC/BA Register

6. MASTER A L is also sent to the CC/BA control logic on the M7813 module to generate the signals that increment the CC and BA registers.

7. The CC/BA counter is incremented after the NPR cycle and the updated information is written into the CC/BA registers. The BA register now contains the address of the next character to be transmitted from the PDP-11 memory and the CC register indicates the number of characters remaining. The output of the CC/BA register is sent to the bus selectors on the M7812 module where it can be read by the program.

4.5.2.2 Detailed Logic Description – The circuit schematic for the CC/BA register is contained in drawing D-CS-M7813-0-1 (Rev H) sheets 3 and 4 which are designated D5-1 and D5-2.

Register Components
The CC/BA register consists of the following major components:

a. Five type 3101 64-bit read/write memories (E6, E16, E26, E36, and E46) with common address lines and enabling inputs to form a 16 word by 18-bit memory. In this application, only eight words (registers) are used so only the three least significant addressing inputs are used.

b. Five type 74S158 quad 2-line to 1-line multiplexer (E7, E17, E27, E37, and E47) with a common select signal to provide an 18-bit multiplexer.

c. Five type 74161 synchronous 4-bit counters (E2, E12, E22, E32, and E42) are cascaded to provide an 18-bit synchronous counter.

In terms of devices, a counter, multiplexer, and memory are interconnected to accommodate 4 bits of the CC/BA register. All but 2 bits of one group of devices (E42, E47, and E46) are used to handle the 18 bits of the BA register. These devices (E42, E47, and E46) are not used as part of the CC register which requires only 16 bits. A typical 4-bit section of the CC/BA register is shown in Figure 4-23.

E6 (CC/BA 3-0) is a type 3101 64-bit read/write semiconductor (TTL) memory organized in 16 4-bit words; however, only 8 words are used. The 8 words (registers) are addressed by the 3-bit binary number sent to address lines A2, A1, and A0. Input A3 is permanently connected to ground to hold it low. The 4-bit data word is sent to inputs D0–D3. In this application, the enabling input (ENB) is permanently held low; therefore, for a selected word, a write operation is performed when the write (WR) input is low and a read operation is performed when the write input is high. A write operation places the input data into the selected word. In a read operation, the complement of the information that has been written into the selected word is non-destructively read out at the four outputs which are M0 (1)–M3 (1). The write input is connected to D5-3 LD CC/BA SP 15–0 L which is generated by the CC/BA control logic.

E7 (CC/BA DATA MUX 3–0) is a type 74S158 quad 2-line to 1-line multiplexer. The four outputs (F0–F3) represent either the A word input or the B word input as selected by the state of the select (S0) input. The strobe (STB) input is permanently held low which enables the multiplexer: with S0 low, the A word is selected and with S0 high, the B word is selected.

E2 (CC/BA CNTR 3–0) is a type 74161 synchronous 4-bit counter. The MSB input is pin 6 and the LSB input is pin 3. The MSB output is pin 11 and the LSB output is pin 14. Both count-enable inputs (CNT EN and CRY EN) are held high by +3 V so that the counter is permanently enabled. The positive-going edge of D5-3 CK CC/BA CNTR H applied to the CLK input increments or loads the counter. Placing a low (D5-3 LD CC/BA CNTR (1) L) on the load (LD) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. A low signal at the clear (CLR) input drives all outputs low. Counters are cascaded by connecting the carry output (CARRY OUT) of one counter to the enabling inputs (CNT EN and CRY EN) of the next counter. The carry output (CO) generates a positive pulse that starts at the minus 1 count and ends at the next count which is overflow (zero).

The counter data outputs are sent to the B inputs of the multiplexer but they are also sent to individual 7416 open-collector inverters. The outputs of the inverters are wire-ORed to produce a signal (D5-1 CC OFLOW H) that is used in the CC/BA control logic.

The output of the CC/BA register is picked off the 3101 memory and sent to the bus selectors on the M7812 module where it can be read by the program. These signals are identified as D5-1 CC/BA XX H and are also sent to one input of the associated bus drivers. The other input of the bus drivers is the inversion of D3-1 MASTER A L which enables the bus address to the Unibus address lines. These signals are identified as BUS AXX L.

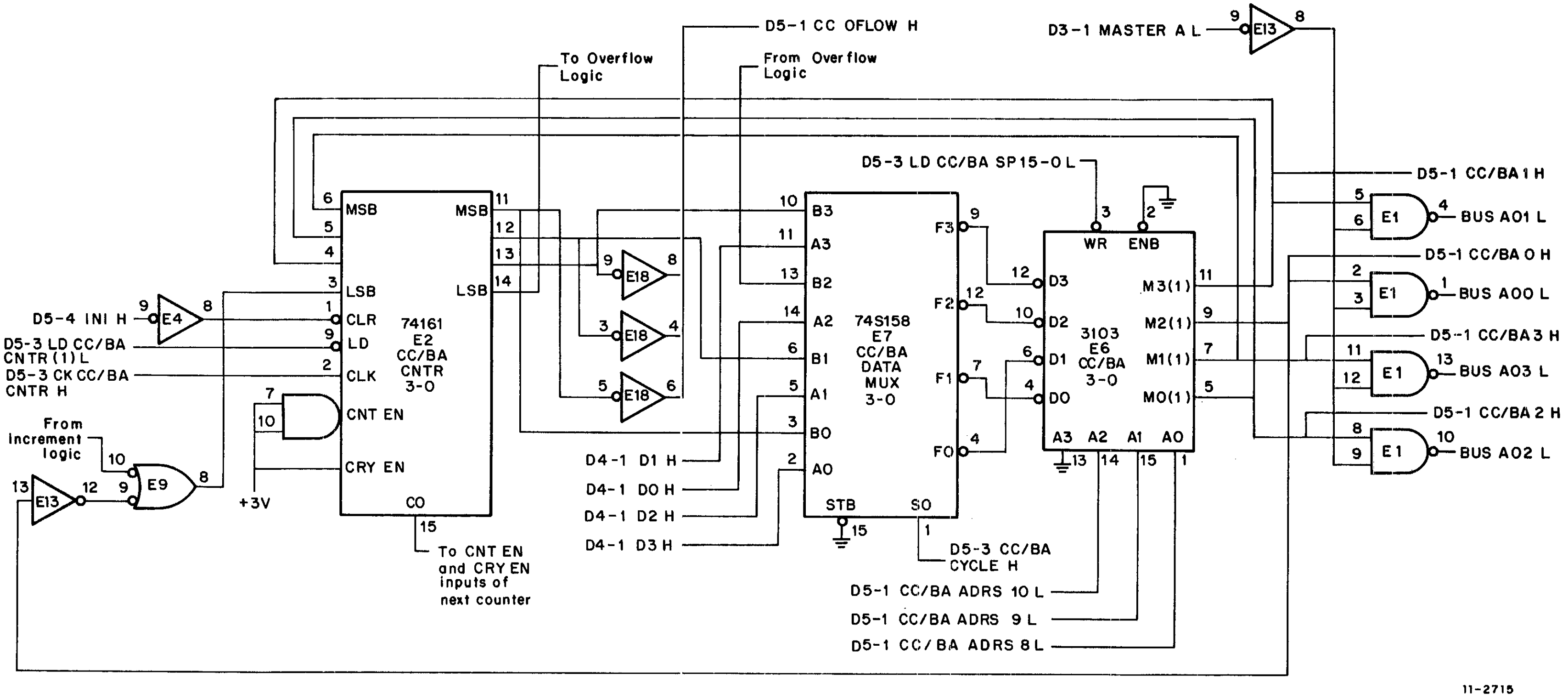


Figure 4-23 4-Bit Section of CC/BA Register

CC/BA Address Multiplexer

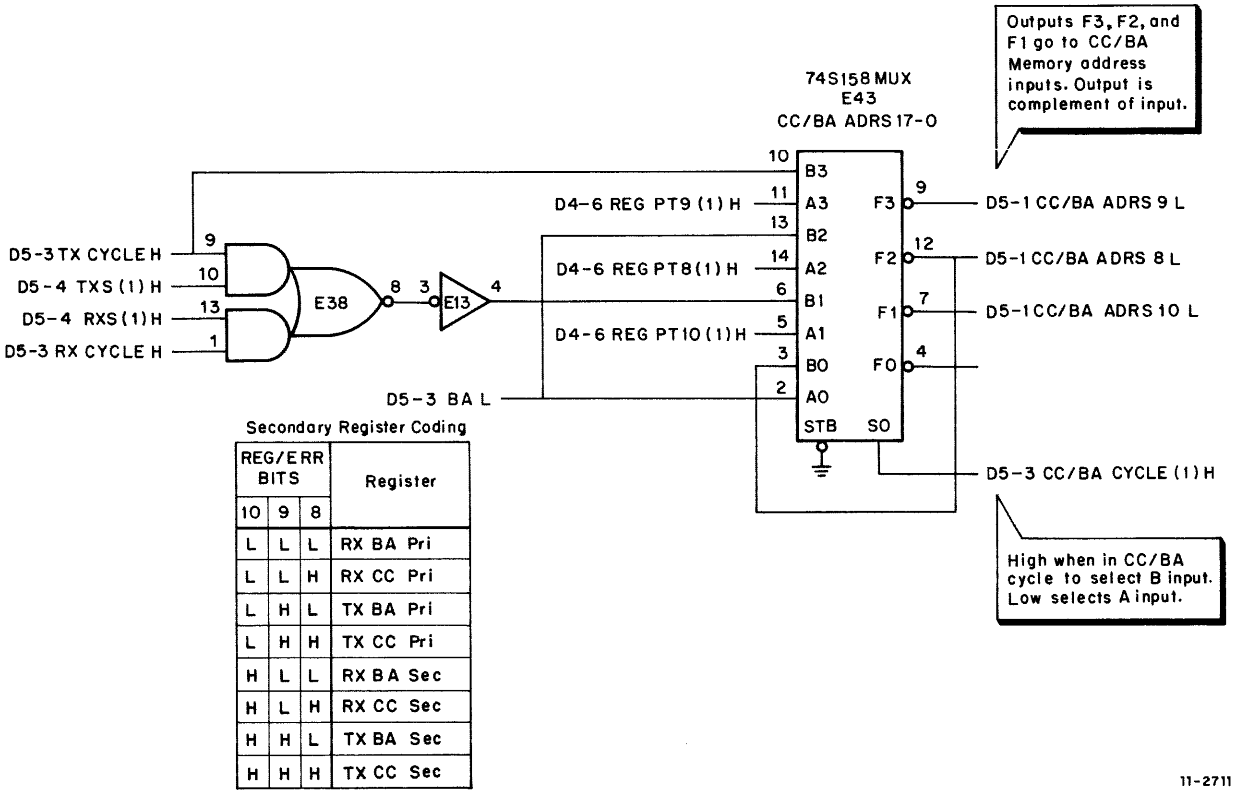
Multiplexer E43 (Figure 4-24) is used to address the eight registers in the 3101 memories. These registers are selected by bits 11–8 of the REG/ERR CSR as shown below. Because only eight address bits are required, bit 11 is not used and the MSB address input on the memory is held low permanently.

10	9	8	Octal No.	Selected Register
0	0	0	0	RX BA Primary
0	0	1	1	RX CC Primary
0	1	0	2	TX BA Primary
0	1	1	3	TX CC Primary
1	0	0	4	RX BA Secondary
1	0	1	5	RX CC Secondary
1	1	0	6	TX BA Secondary
1	1	1	7	TX CC Secondary

Three of the four multiplexer outputs are used to address the memory as shown below:

Mux Output	Signal Name	Memory Input
F1	D5-1 CC/BA ADRS 10 L	A2
F3	D5-1 CC/BA ADRS 9 L	A1
F2	D5-1 CC/BA ADRS 8 L	A0 (LSB)

Three inputs to the multiplexer come from bits 8, 9, and 10 of the REG/ERR CSR. They are: D4-6 REG PT 9 (1) H to input B3, D4-6 REG PT 8 (1) H to input A2, D4-6 REG PT 10 (1) H to input A1. Signal D5-3 BA L goes to input B2. This signal comes from the CC/BA control logic and is low when the DQ11 is in the BA cycle. An input gating network is connected to input B1. Four signals are sensed by



Secondary Register Coding

REG/ERR BITS 10	9	8	Register
L	L	L	RX BA Pri
L	L	H	RX CC Pri
L	H	L	TX BA Pri
L	H	H	TX CC Pri
H	L	L	RX BA Sec
H	L	H	RX CC Sec
H	H	L	TX BA Sec
H	H	H	TX CC Sec

Figure 4-24 CC/BA Address Multiplexer (E43)

AND-OR-invert gate E38 whose output is then inverted by E13 and sent to mux input B1. Two signals indicate whether the transmit or receive mode is enabled. Signal D5-3 TX CYCLE H is high if the transmitter requested the NPR. D5-3 RX CYCLE H is high if the receiver requested the NPR. Two signals indicate whether the primary or secondary register for the selected mode is enabled and they are a function of TX/RX NPR selection. Signal D5-4 TX S (1) H is high if the secondary register is enabled in the transmit mode and signal D5-4 RX S (1) H is high if the secondary register is enabled in the receive mode.

In the CC/BA cycle mode (mux B input selected), the following signals control the CC/BA memory address inputs (A2, A1 and A0) listed below:

Input A2 – controlled by inverted output of E38 (function of RX/TX cycle and primary/secondary selection)

Input A1 – controlled by D4-6 REG PT 9 (1) H

Input A0 (LSB) – controlled by D5-3 BA L

As an example, assume that the DQ11 is in the CC/BA cycle which means that D5-3 CC/BA CYCLE (1) H is high. This selects the B input of multiplexer E43. Assume also that it is desired to select the RX BA secondary register. This register has an octal designation of 4 as determined by REG/ERR bits 10, 9, and 8. The state of the B inputs of mux E43 should be as follows:

B1=1=H B3=0=L B2=0=L (LSB)

Input B1 – Signal D5-3 RX CYCLE H is high because the DQ11 is in the receive mode. Signal D5-4 RX S (1) H is high because the RX BA secondary register is selected. The output (pin 8) of E38 is therefore low. It is inverted by E13 which puts a high on input B1 of mux E43.

Input B3 – Signal D5-3 TX CYCLE H is low which puts a low on input B3 of mux E43.

Input B2 – Signal D5-3 BA L is low because the DQ11 is in the BA cycle which puts a low on input B2 of mux E43.

The B inputs of mux E43 are set up to select the RX BA secondary register and the complement of the B inputs appear at the mux outputs. This inversion of the B inputs merely means that the physical location of the RX BA secondary register is word 3. Its address, as selected by REG/ERR bits 10, 9 and 8, is always 4. The fact that the register address and the address of the word in memory where it is stored do not coincide is of no consequence.

The following discussion covers loading and incrementing the CC/BA register. Several signals from the CC/BA control logic (print D5-3) are used but are not explained in detail. They are covered in the subsequent discussion of the CC/BA control logic.

Loading the BA Register
Assume that it is desired to load the starting address in the TX BA primary register (address 2_8).

The DQ11 is not yet in the CC/BA cycle.

1. D5-3 CC/BA CYCLE H is low which selects the A input of the CC/BA ADRS mux (E43). Inputs A3, A2, and A1 (LSB) represent 2_8 because these inputs come from bits 10, 9, and 8, respectively, of the REG/ERR CSR which has selected the TX BA primary register. The output of mux E43 has therefore selected the 16-bit word in the 3101 memory that represents the TX BA primary register.

2. D5-3 CC/BA CYCLE H, which is low, also selects the A input of the CC/BA DATA MUX. The A input represents the 16-bit or 18-bit address, via Unibus data lines, that the program desires to load into the TX BA primary register. The mux is permanently enabled so this address appears at the data input of the memory.

3. REG/ERR bits 11–8 are set to give 2_8. These bits, via the register selection logic, assert D5-4 LD CC/BA L as a pulse, which in turn drives D5-3 LD CC/BA SP 15–0 L low. This signal goes to the write (WR) input of the memory. When WR is low, the input data (starting bus address) is written into the selected word (TX BA primary register).

   If extended PDP-11 memory is used, 18 address bits are required. The program sets REG/ERR register bit 12 which allows D5-3 LD SP PORT L to be asserted and write the two additional bits (16 and 17) into the selected BA register.

4. At the end of the D5-4 LD CC BA L pulse, signal D5-3 LD CC/BA SP 15–0 L goes high which places the complement of the contents of the TX BA primary register at the memory output. This output, which represents the bus address, is enabled to the Unibus via bus drivers, by the inversion of D3-1 MASTER A L.

Loading the CC Register
Assume that it is desired to load the character count in the TX CC primary register (address 3_8). The DQ11 is in the transmit mode but is not yet in the CC/BA cycle.

The sequence for loading the TX CC primary register is the same as that described above for loading the TX BA primary register with the following exceptions:

1. The A3, A2, and A1 inputs of the CC/BA ADRS MUX (E43) represent 3_8 which is the octal address of the TX CC primary register.
2. The data on the A input of the CC/BA DATA MUX is the 2's complement of the character count to be loaded into the register.

The output of the CC register (D5-1 CC/BA 0 H–15 H) is sent to the bus selectors on the M7812 module where it can be read by the program.

Incrementing the BA Register
Transfers to and from the memory are accomplished on a word basis only. Word addresses occur on even boundaries; that is, the last octal digit is 0, 2, 4, or 6. This means that the least significant bit of a word address is always 0.

Assume that the starting address has been loaded into the TX BA primary register. It is sent out to the Unibus and the memory responds by sending the word located at that address to the DQ11. After the word has been processed, another NPR cycle occurs which requests the next successive memory word. Remember that the word can contain one character having 9–16 bits (single-character operation) or two characters having 8 bits or less (double-character operation). This information is vital to the CC register but not to the BA register because it deals in word addresses and is looking only for the next successive word address. In double-character operation, the BA register is incremented by one by each character. Since this occurs twice during the NPR cycle, the next address is even.

The output of the BA register from the CC/BA memory is fed back to the input of the CC/BA counter. The output of the counter is sent via the B input of the CC/BA data mux to the CC/BA memory input. Once each NPR cycle, the counter is clocked (incremented) and the updated bus address is sent to the CC/BA memory where it is written into the BA register.

Clocking the counter only increments its output by one; however, a logic network connected to the LSB input (bit 0) allows the count to be increased by one using the counter input-preset feature. When the counter is subsequently clocked, the BA register input is incremented by one again which results in an increment by two. This occurs only in single-character operation.

The logic network (print D5-1) consists of AND-OR-invert gate E8, negated-input OR gate E9 and inverter E13. The 0 output of the CC ODD flip-flop is always high during the BA cycle. This high is sent to pins 1 and 10 of E8. Pin 13 of E8 is connected to D5-3 BA H and is high during the BA cycle. With pins 1 and 13 high, one input to the NOR section of E8 is always high. Thus, the output (pin 8) is held low despite the state of the other input which is the ANDing of pins 9 and 10. This means that signal D4-3 BITS 11 (1) H, which goes to E8 pin 9, has no effect on the output of E8 during a BA cycle. Signal D4-3 BITS 11 (1) H determines whether single or double characters are to be processed.

The output (pin 8) of E8 is sent to pin 10 of negated-input OR gate E9. This low signal drives the output (pin 8) of E9 high and it is sent to the LSB input (pin 3) of counter E2. The other input (pin 9) of E9 comes from the LSB of the BA register (E6 pin 9). The state of this input is irrelevant. The 0 (low) sensed at the LSB of the BA register has been fed back to the LSB of the counter as a 1 (high).

The incrementing (CC/BA register updating) cycle first requires that the output of the register be loaded into the counter. Then the counter is clocked once. This sequence is controlled by the CC/BA control logic (print D5-3). Signal D5-3 LD CC/BA CNTR (1) L is connected to the load (LD) input of the counter. When it goes low, the information at the input is transferred to the output at the next clock pulse. In this case, the LSB of the counter goes from a 0 to a 1. During this load cycle, the 0 from the LSB of the BA register has been forced into the counter LSB as a 1. The count has been increased by one. Now, signal D5-3 CK CC/BA CNTR H again goes high and clocks the counter which increments it by one. The net effect is that the bus address has been incremented by two. This updated address is written into the BA register and is put on the Unibus address lines during the next NPR cycle.

The LSB counter bit is not fed back directly to the CC/BA mux input as all other bits are; rather, it passes through a small logic network consisting of two E13 inverters and an AND-OR-invert gate (E8). This gate provides two paths for restoring or updating the CC/BA register. The path from the ODD CNT BYPASS flip-flop is used only for incrementing the CC register by two on an odd count. The path from the LSB output of the counter is used for incrementing the CC register in all other situations plus incrementing the BA register.

Incrementing the CC Register

The CC register handles single or double characters and can be loaded with odd or even counts. As a result, it has the capability of being incremented by one or two for both odd and even counts.

In addition to the logic mentioned in the above discussion of incrementing the BA register, two additional flip-flops are used in the CC register incrementing and overflow logic. They are the CC ODD and ODD CNT BYPASS flip-flops (both labeled E3).

The following examples explain how the CC register is incremented.

The first example assumes that the CC register shows an even count, incrementing does not cause overflow, and single characters are being handled. The desired result is incrementation by one to produce an odd count.

At the start of the sequence, the assumptions cause the following results:

1. The even count is reflected as a low (0) from the LSB of the CC register (E6 pin 9) being fed back to pin 13 of inverter E13 and the D input of the ODD CNT BYPASS flip-flop.
2. No overflow is to be produced, so the CC ODD flip-flop is cleared and remains so during the sequence. The 0 output of this flip-flop puts a high on pins 10 and 1 of gate E8.
3. Single characters are being handled so D4-3 BITS 11 (1) H, which is connected to E8 pin 9, is low.
4. This is a CC cycle so D5-3 BA H, which is connected to E8 pin 13, is low.
5. The conditions in step 4 drive the output (pin 8) of E8 high. This signal is sent to E8 pin 4 and is inverted by E13 and sent as a low to E8 pin 3. This sets up the restore path for bit 0 from the counter not the ODD CNT BYPASS flip-flop.
6. The high output (pin 8) of E8 also goes to pin 10 of E9. The high from pin 12 of inverter E13 goes to the other input (pin 9) of E9. This drives the output (pin 8) of E9 low which represents an even count (0) to the LSB input of counter E22.
7. The LSB output of the counter is also low (even count). This low is sent to E8 pin 5. Both OR inputs of this gate are low so its output (pin 6) is driven high. This signal is inverted by E13 and sent as a low to input B2 of CC/BA DATA MUX E7.
8. The next event in the sequence is the loading of the counter, which is performed when D5-3 LD CC/BA CNTR (1) L goes low and D5-3 CK CC/BA CNTR H goes high. The CC count does not change because the LSB is low (0) and a low (0) is trying to be loaded in.
9. Now D5-3 CK CC/BA CNTR H goes high again which clocks the counter and increments it by one. The LSB output goes high which drives E8 pin 6 low. This signal is inverted by E13 and sent as a high to the B2 input of mux E7 along with the other 15 bits of the counter which represent the updated character count (incremented by one from the previous count).
10. During the sequence, the CC ODD and ODD CNT BYPASS flip-flops are clocked. Both flip-flops started in the cleared state and are clocked with their D-inputs low so they do not change state and have no effect on the incrementing operation.

The second example assumes that the CC register shows an odd count, incrementing does not cause overflow, and single characters are being handled. The desired result is incrementation by one to produce an even count. This example proceeds like example 1 except that the counter LSB input and output are high. When the counter is loaded, the count does not change because the LSB is high (1) and a high (1) is trying to be loaded in. When the counter is clocked, it is incremented by one which drives the LSB output low (0).

The third example assumes that the CC register shows an even count, incrementing does not cause overflow, and double characters are being handled. The desired result is incrementation by two to produce the next even count. This example is similar to incrementing the BA register. The LSB output of the counter is low (0) but the low LSB output from the CC register is fed back to the counter LSB input as a high (1). When the counter is loaded, a high is forced into the LSB which is an increment by one. When the counter is clocked, it is incremented again. The CC count, which has been incremented by two, is restored in the CC register.

The fourth example assumes that the CC register shows an odd count, incrementing does not cause overflow, and double characters are being handled. The desired result is incrementation by two to produce the next odd count. This example is similar to example 3 except that the counter LSB input and output are high. When the counter is loaded, the count does not change. When the counter is clocked, it is incremented by one (LSB output goes low); however, this low does not get through E8 and E13 to the mux. The ODD CNT BYPASS flip-flop is clocked and it is set because its D input is high. The 1 output of the flip-flop, which is high, gets through E8 and E13 to the mux. The character count has been incremented by two which is the next odd count as desired.

Counter Overflow Detection Logic
When the counter overflows in the CC mode, its outputs go from all 1s (which is a count of minus 1) to all 0s. This indicates that the character count for the selected CC register is now zero. The next step is to look at the associated register (primary or secondary) to see if it contains anything. If it does, the character count is picked up from the associated register. The overflow logic generates D5-1 CC OFLOW H which is used in the CC/BA control logic (print D5-3) to test the associated register.

CC/BA counter output bits 0–15 are sent to type 7416 bare collector inverters. All bits except bit 0 go directly to the inverter inputs. Bit 0 goes through the restore logic path before reaching its associated 7416 inverter. All 16 inverter outputs are wire-ORed and this point is D5-1 CC OFLOW H. All inverter inputs must be 0 simultaneously to assert D5-1 CC OFLOW H.

Whenever bit 0 of the CC register is 1, the D input of the ODD CNT BYPASS flip-flop is high. When this flip-flop is clocked during the increment sequence, its 1-output (which is high) is sent to pin 4 of AND gate E33. The other input (pin 5) of this gate is D5-2 CC/BA CARRY 10–0 H. This signal comes from the carry output of bit 15 of the counter (E32 pin 15 on print D5-2). It goes high when the counter reaches minus 1 (all 1s). This drives the output (pin 6) of E33 high so the CC ODD flip-flop is set when it is clocked by D5-3 TEST ODD CNT H. This sets up the restore logic path for bit 0 from the counter.

Assuming that the counter is at minus 1 (all 1s), all outputs go to 0 (overflow) on the next clock pulse. All the wire-ORed inverter inputs go low and D5-1 CC OFLOW H is asserted and sent to the CC/BA control logic.

When the CC ODD flip-flop is set, it asserts D5-1 CC ODD (1) H at its 1 output. This signal is sent to the transmitter control logic (print D5-6) and the receiver control logic (print D5-8).

4.5.3 Character Count/Bus Address Control Logic

4.5.3.1 Functional Description – A simplified block diagram of the CC/BA control logic is shown in Figure 4-25. The primary purpose of this logic is to control the updating of the CC/BA register following an NPR cycle. Normally, it loads and increments the CC register, loads and increments the BA register, then shuts down until it is started again during the next NPR cycle.

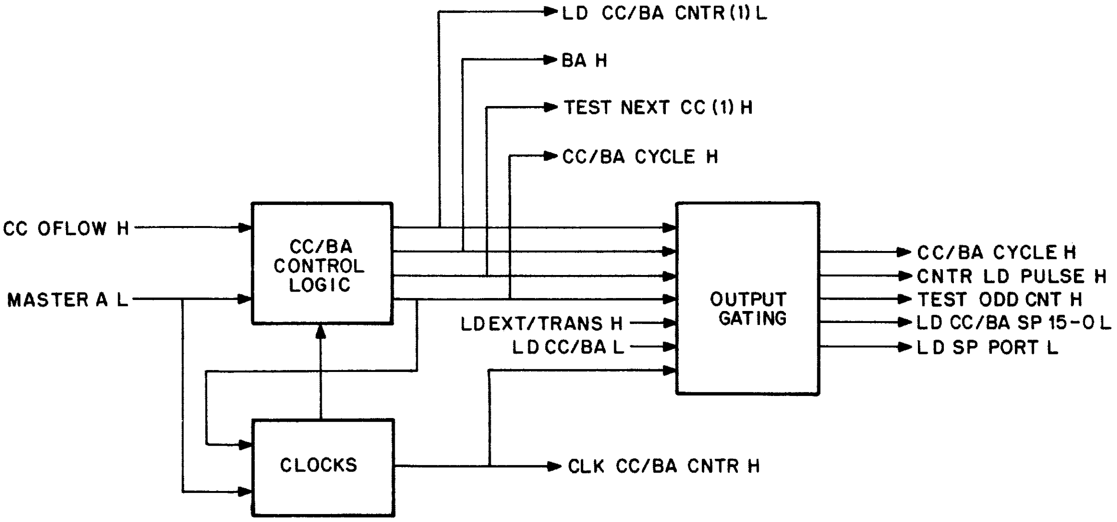


Figure 4-25 Block Diagram of the CC/BA Control Logic

The normal operating sequence is altered if an overflow is detected when the CC register is incremented. Overflow occurs when the CC/BA counter reaches a count of 0 for the selected CC register. This means that the selected CC register reads 0 and the last character has been processed. This is decision time for the CC/BA control logic. The associated CC register must be tested to see if it contains additional characters. If it does, control is switched to the associated register and additional characters are processed during subsequent NPR cycles. If it is empty, there are no more characters to be processed. The appropriate DONE flag is set and the GO bit is cleared.

The overflow is detected when the CC register is incremented and the overflow indication is held until the BA register has been loaded and incremented. Another CC load operation is started and when it is completed the sequence is shut down until the next NPR cycle. If the associated CC register indicates 0, no more characters are processed. If the associated CC register contains a character count, additional characters are processed starting with the next NPR cycle.

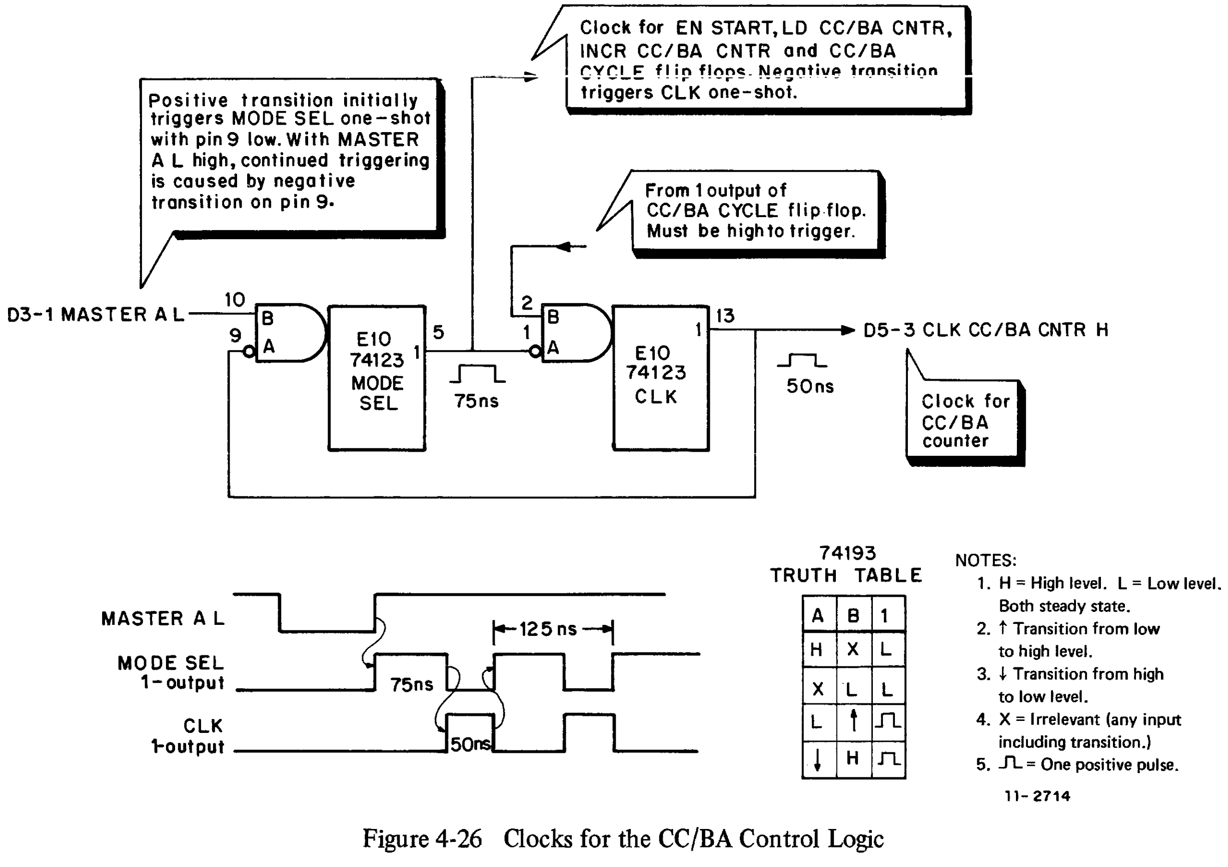
Another section of the CC/BA control logic responds to the NPR request signals from the transmit control logic and receive control logic. It generates a group of signals that are used in various places in the M7813, M7812, and M7818 modules. This logic is inhibited while the CC/BA register is being updated.

4.5.3.2 Detailed Logic Description – The circuit schematic for the CC/BA control logic is contained in drawing D-CS-M7813-0-1 sheet 5 which is designated D5-3.

The major element of the CC/BA updating logic is a string of five D-type flip-flops that control the loading and incrementing sequence of the CC register and BA register. They are: EN START, LD CC/BA CNTR, INCR CC/BA CNTR, CC/BA SEL, and CC/BA CYCLE. Two additional D-type flip-flops (OFLOW HOLD and TEST NEXT CC) are used when overflow is detected. Two one-shot clocks are used: CLK clocks the CC/BA counter and MODE SEL clocks all the sequence flip-flops except CC/BA SEL.

Before discussing the CC/BA register loading and incrementing sequence, the operation of the clock is described.

Two 74123 retriggerable monostable multivibrators (one-shots) are connected back-to-back to form an oscillator (Figure 4-26). The 1 output of each is used to trigger the other. Two qualifying signals are required to start the clock and it is self-sustaining thereafter.



Positive transition initially triggers MODE SEL one-shot with pin 9 low. With MASTER A L high, continued triggering is caused by negative transition on pin 9.

Clock for EN START, LD CC/BA CNTR, INCR CC/BA CNTR and CC/BA CYCLE flip flops. Negative transition triggers CLK one-shot.

From 1 output of CC/BA CYCLE flip flop. Must be high to trigger.

Clock for CC/BA counter

74193 TRUTH TABLE

A	B	1
H	X	L
X	L	L
L	↑	⎍
↓	H	⎍

NOTES:
1. H = High level. L = Low level. Both steady state.
2. ↑ Transition from low to high level.
3. ↓ Transition from high to low level.
4. X = Irrelevant (any input including transition.)
5. ⎍ = One positive pulse.

11-2714

Figure 4-26 Clocks for the CC/BA Control Logic

At the start of the NPR cycle, D3-1 MASTER A L goes low. This inhibits the MODE SEL one-shot; however, it sets the CC/BA cycle flip-flop which triggers the CLK one-shot. One pulse is produced and the CLK one-shot returns to rest; this pulse does nothing. Pin 2 of the CLK one-shot remains high which means that a negative transition at pin 1 will trigger the CLK one-shot. The low from the 1 output (pin 13) of the CLK one-shot is fed back to pin 9 of the MODE SEL one-shot. Now, a positive transition at pin 10 of the MODE SEL one-shot will trigger it.

At the end of the NPR cycle, D3-1 MASTER A L goes high and triggers the MODE SEL one-shot which generates a positive pulse at its 1 output. When this pulse times out, its negative-going trailing edge triggers the CLK one-shot which generates a positive pulse at its 1 output. When the CLK pulse times out, its negative-going trailing edge triggers the MODE SEL one-shot again. The clocks are self-sustaining as long as D3-1 MASTER A L remains high and the CC/BA CYCLE flip-flop remains set. Ignoring propagation delays in the devices, the MODE SEL one-shot generates 75 ns positive pulses every 125 ns and the CLK one-shot generates 50 ns positive pulses every 125 ns.

Updating the CC/BA Register (No Overflow)

This discussion covers the operation of the CC/BA control logic during the sequence that places the bus address on the Unibus and then updates the CC register and BA register without overflow. Refer to print D5-3 and the timing diagram in Figure 4-27.

1. Assume that the starting bus address has been loaded into the selected BA register and this address appears at the input of the 8881 bus drivers. D3-1 MASTER A L is high, all CC/BA control flip-flops are cleared, and both one-shots are at rest. D5-3 CC/BA CYCLE H is low which means that the A inputs of the CC/BA data mux and address mux are selected. D5-3 LD CC/BA SP 15–0 L is high which means that the CC/BA memory is in the read mode.

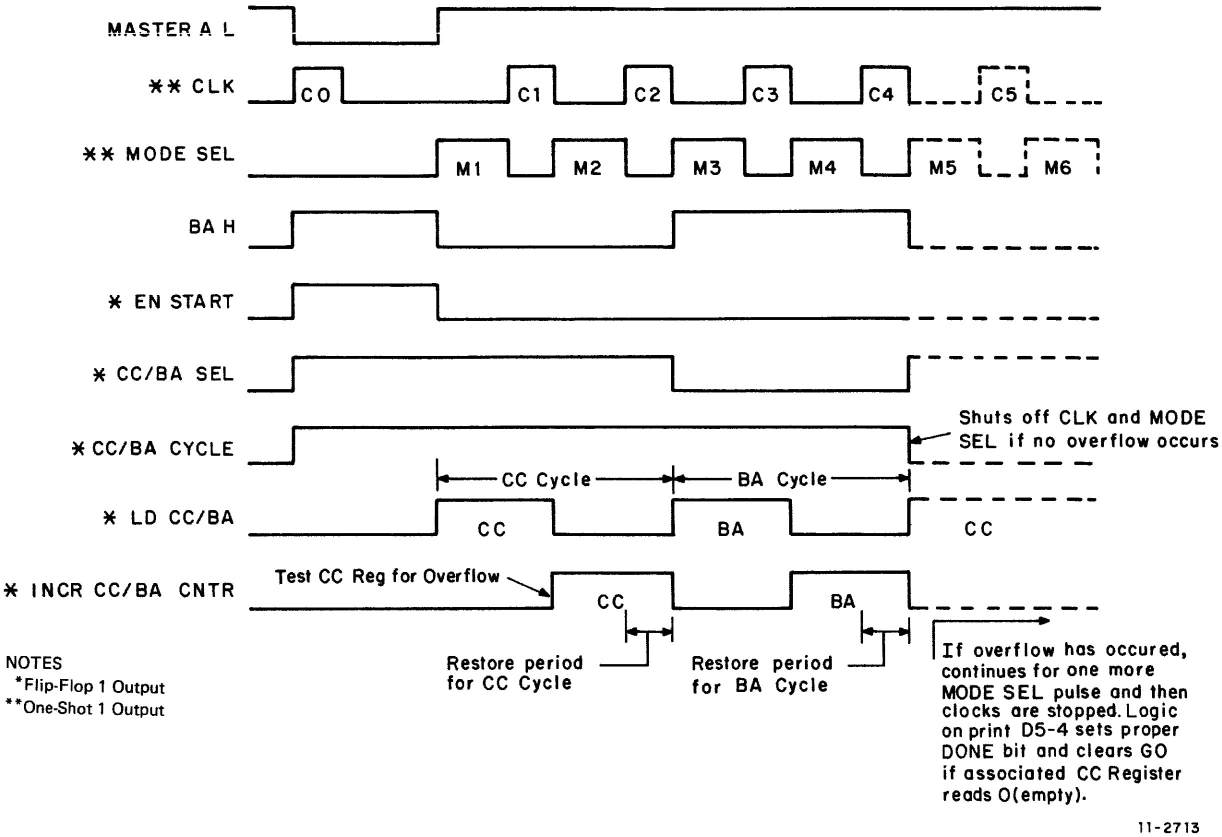

MASTER A L
** CLK
C0
C1
C2
C3
C4
C5
** MODE SEL
M1
M2
M3
M4
M5
M6
BA H
* EN START
* CC/BA SEL
* CC/BA CYCLE
Shuts off CLK and MODE SEL if no overflow occurs
CC Cycle
BA Cycle
* LD CC/BA
CC
BA
CC
* INCR CC/BA CNTR
Test CC Reg for Overflow
CC
BA
Restore period for CC Cycle
Restore period for BA Cycle
If overflow has occured, continues for one more MODE SEL pulse and then clocks are stopped. Logic on print D5-4 sets proper DONE bit and clears GO if associated CC Register reads 0(empty).
NOTES
*Flip-Flop 1 Output
**One-Shot 1 Output
11-2713

Figure 4-27 Timing Diagram for CC/BA Control Logic

2. D3-1 MASTER A L goes low and enables the current bus address to the Unibus. The CC/BA control flip-flops respond as follows:

   EN START – Set via preset input. D-input is low (permanently connected to ground).

   LD CC/BA CNTR – Remains cleared. D-input is high.

   INCR CC/BA CNTR – Remains cleared. D-input is low.

   CC/BA SEL – Set via preset input. D-input is low.

   CC/BA CYCLE H – Set via preset input. D-input is high. Drives D5-3 CC/BA CYCLE H high which selects the B input of the data and address multiplexers.

3. D3-1 MASTER A L goes high at the end of the NPR cycle which drives D5-3 BA H low to indicate that the logic has entered the CC portion of the update cycle. The MODE SEL one-shot is triggered and it generates pulse M1 (Figure 4-26). The CC/BA control flip-flops respond as follows:

   EN START – Cleared (stays cleared through the end of the updating cycle).

   LD CC/BA CNTR – Set. D-input is low. Asserts D5-3 LD CC/BA CNTR (1) L that goes to the load input of the CC/BA counter. When the counter is subsequently clocked with the load input low, the counter outputs agree with the inputs; that is, the CC register output from the memory is loaded into the counter.

   INCR CC/BA CNTR – Remains cleared. D-input is high.

   CC/BA SEL – Remains set. D-input is high.

   CC/BA CYCLE – Remains set. D-input is high.

   This step describes how the logic is set up for subsequent loading of the character count into the counter.

4. When the MODE SEL one-shot times out, it triggers the CLK one-shot which generates pulse C1. This asserts D5-3 CLK CC/BA CNTR H. The positive transition of this signal clocks the CC/BA counter which loads in the character count. Pulse C1 also drives D5-3 CNTR LD PULSE H high which clocks the ODD CNT BYPASS flip-flop in the CC/BA register logic.

5. When pulse C1 times out, it triggers the MODE SEL one-shot which generates pulse M2. The CC/BA control flip-flops respond as follows:

   LD CC/BA CNTR – Cleared. D-input is high.

   INCR CC/BA CNTR – Set. D-input is low. Drives D5-3 TEST ODD CNT H high at E5 pin 6 which clocks the CC ODD flip-flop in the CC/BA register logic.

   CC/BA SEL – Remains set. D-input is low.

   CC/BA CYCLE – Remains set. D-input is high.

   This step describes how the logic is set up for subsequent incrementing of the character count.

6. When pulse M2 times out, it triggers the CLK one-shot which generates pulse C2. This asserts D5-3 CLK CC/BA CNTR H which clocks the CC/BA counter and increments it. Pulse C2 also drives D5-3 LD CC/BA SP 15–0 L low which puts the CC/BA memory in the write mode. The CC register now has been loaded and incremented; it contains the updated character count.

7. When pulse C2 times out, it triggers the MODE SEL one-shot which generates pulse M3. The CC/BA control flip-flops respond as follows:

   LD CC/BA CNTR – Set. D-input is low. Asserts D5-3 LD CC/BA CNTR (1) L to enable the CC/BA counter load input.

   INCR CC/BA CNTR – Cleared. D-input is high. When this flip-flop is cleared, it clocks the CC/BA SEL flip-flop.

CC/BA SEL – Cleared. D-input is high. When CC/BA SEL is cleared, it asserts D5-3 BA H which indicates the start of the BA portion of the updating sequence.

CC/BA CYCLE – Remains set. D-input is high.

This step describes how the logic is set up for subsequent loading of the bus address into the counter.

8. When pulse M3 times out, it triggers the CLK one-shot which generates pulse C3. This asserts D5-3 CLK CC/BA CNTR H which clocks the CC/BA counter and loads in the bus address. Pulse C3 also drives D5-3 CNTR LD PULSE H high which clocks the ODD CNT BYPASS flip-flop in the CC/BA register logic.

9. When pulse C3 times out, it triggers the MODE SEL one-shot which generates pulse M4. The CC/BA control flip-flops respond as follows:

   LD CC/BA CNTR – Cleared. D-input is high.

   INCR CC/BA CNTR – Set. D-input is low.

   CC/BA SEL – Remains cleared. D-input is high.

   CC/BA CYCLE – Remains set. D-input is now low.

   This step describes how the logic is set up for subsequent incrementing of the bus address.

10. When pulse M4 times out, it triggers the CLK one-shot which generates pulse C4. This asserts D5-3 CLK CC/BA CNTR H which clocks the CC/BA counter and increments it. Pulse C4 also drives D5-3 LD CC/BA SP 15–0 L low which puts the CC/BA memory in the write mode. The BA register now has been loaded and incremented; it contains the next bus address to be used.

11. When pulse C4 times out, it triggers the MODE SEL one-shot which generates pulse M5. This pulse clocks the CC/BA CYCLE flip-flop which clears it and disables both clocks (CLK and MODE SEL). This ends the updating cycle. The other flip-flops respond as follows:

    LD CC/BA CNTR – Set. D-input is low.

    INCR CC/BA CNTR – Cleared. D-input is high.

    CC/BA SEL – Set. D-input is low.

    CC/BA CYCLE – Cleared. D-input is high.

Updating the CC/BA Register (Overflow Occurs)

Two additional flip-flops (OFLOW HOLD and TEST NEXT CC) are used to alter the CC/BA updating cycle if an overflow is detected when the CC register is incremented.

At the start of the updating cycle, both flip-flops are cleared. The clock signal for these flip-flops comes from the 0 output of the INCR CC/BA CNTR flip-flops. The positive transition that is required for clocking is generated when the INCR CC/BA CNTR flip-flops go from the set state to the clear state. This occurs first at the leading edge of pulse M3. Assuming that an overflow has occurred, the D-input of OFLOW HOLD is high so the flip-flop is set. The TEST NEXT CC flip-flop does not change state (remains cleared) because its D-input was low at the time it was clocked. When OFLOW HOLD is set, it puts a high on pin 2 of NOR gate E25 and puts a high on the D-input of the TEST NEXT CC flip-flop. At this point, this is all that happens. The indication of an overflow has been recorded and saved and the logic, via E25 pin 2, has been conditioned so that pulse M5 does not disable the clocks. No further action is taken, due to the overflow, until the BA register has been loaded and incremented.

When pulse M5 occurs, the OFLOW HOLD flip-flop is cleared. Now, the logic via E25 pin 2 has been conditioned so that the next MODE SEL pulse (M6) disables the clocks. The TEST NEXT CC flip-flop is set which asserts D5-3 TEST NEXT CC (1) H. This signal is sent to the logic on print D5-4 to generate the signal that switches the addressing from the current CC register to the associated CC register (primary to secondary or secondary to primary).

The logic is in the CC load cycle. When pulse C5 is generated, the CC/BA counter is loaded with the contents of the associated CC register.

When pulse M6 occurs, the CC/BA CYCLE flip-flop is cleared which disables the clocks (CLK and MODE SEL). The contents of the associated CC register have been loaded but the logic needs to perform two more functions.

1. Generate the appropriate DONE flag to indicate that it is finished with the first selected CC register.

2. Check the contents of the next CC register. If it contains a count, pick it up at the next NPR cycle and continue to process characters. If it is 0, reset GO to shut down because there are no more characters to process.

When the CC/BA CYCLE flip-flop was cleared by pulse M6, the low at its 1 output directly clears the TEST NEXT CC flip-flop. The 0 output of this flip-flop is sent to a pulse generator (Figure 4-28) which generates a positive pulse of 100 ns. This pulse (D5-3 NEXT CC PULSE H) is sent to the logic on print D5-4 to set the appropriate DONE flag. If the associated CC register is empty, GO is reset and the unit shuts down.

NPR Request Logic

At the top of print D5-3 there is a logic network that responds to the NPR request signals from the receive and transmit control logic and generates several signals that are used throughout the DQ11.

The NPR EN flip-flop asserts D5-3 NPR EN (1) H when the CC/BA control logic is not in the CC/BA update cycle. Signal D5-3 NPR EN (1) H comes from the 0 output of the flip-flop and goes to the NPR control section of the M7821 Interrupt Module. This signal must be high for the M7821 to respond to an NPR request from the receive or transmit control logic. The D input of the NPR EN flip-flop is permanently connected to ground so when it is clocked it is cleared which asserts D5-3 NPR EN (1) H. The clocking signal comes from the 0 output of the CC/BA CYCLE flip-flop. The required positive transition occurs when the CC/BA CYCLE flip-flop goes from the set to the cleared state. This happens at the end of the CC/BA updating cycle so now the M7821 is ready to respond to an NPR request.

Signal D5-3 NPR EN (1) H must be cleared and then reasserted before another NPR request can be honored by the M7821 module. This signal is cleared by D6-2 END NPR CYCLE (1) L which goes low at the end of the NPR cycle and directly sets the NPR EN flip-flop which drives D5-3 NPR EN (1) H low.

Two NPR request signals are sensed by this logic: D5-6 TX NPR RQ (1) L from the transmit control logic and D5-8 RX NPR RQ (1) L from the receive control logic. A request signal is generated when the associated NPR RQ flip-flop (TX or RX) is set. Both request signals are sent to negated-input OR gate E20. When either signal is asserted, D5-3 NPR RQ H is generated at the output (pin 3) of E20. This signal is sent to the M7821 Interrupt Module to request the NPR, providing D5-3 NPR EN (1) H is asserted. Signal D5-8 RX NPR RQ (1) L is also sent to the D-input of the TX/RX CYCLE flip-flop. The clock signal for this flip-flop is the ANDing of D5-3 NPR RQ H and the 0 output of the CC/BA CYCLE flip-flop at AND gate E5.

For example, assume that the transmit control logic is requesting the NPR. Signal D5-6 TX NPR RQ (1) L is low and it drives pin 1 of E5 high. This logic will not generate any signals until the CC/BA updating cycle is complete which is indicated when the CC/BA CYCLE flip-flop is cleared. When it is cleared, pin 2 of E5 goes high which drives its output (pin 3) high. This positive transition is delayed by R4, C109 and C110 and then clocks the TX/RX CYCLE flip-flop.

The RX control logic is not requesting the NPR so D5-8 RX NPR (1) L is high, which puts a high on the D-input of the TX/RX CYCLE flip-flop, so that it sets and asserts D5-3 TX CYCLE H.

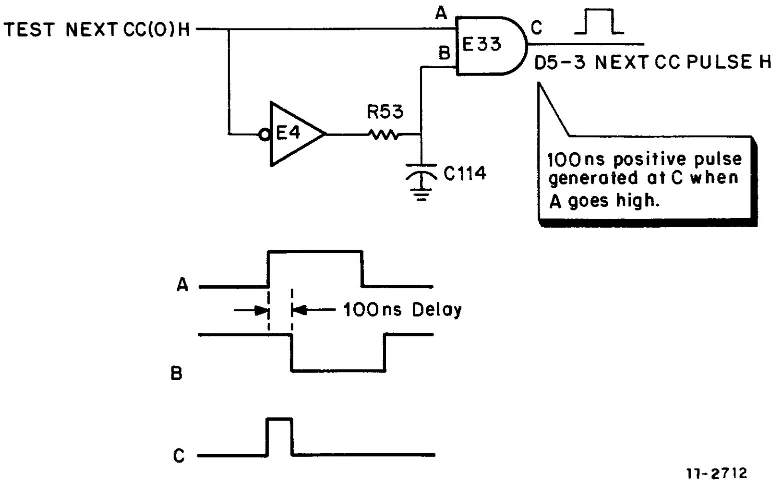


Figure 4-28 Pulse Generator In Overflow Detection Logic

The delay allows settling time for the CC/BA control logic before initiating another NPR sequence. Signal D5-3 TX CYCLE H is sent to the CC/BA addressing mux (print D5-1), the DONE logic (print D5-4), the TX control logic (print D5-6) and the REG/ERR register (print D4-6) on the M7812 module.

When the NPR cycle is complete, D6-2 END NPR CYCLE (1) L is asserted. This low signal is sent to E30 pin 6 where it is ANDed with the low from the TX/RX CYCLE flip-flop at the other input (pin 5) of E30. This drives the output (pin 4) of E30 high to assert D5-3 TX NPR DONE H. This signal is sent to the TX control logic (print D5-6) where it clears the TX NPR RQ flip-flop and drives D5-6 TX NPR RQ (1) L high. The transmit control logic no longer requests the NPR. At the same time, D6-2 END NPR CYCLE (1) L directly sets the NPR EN flip-flop which clears D5-3 NPR EN (1) H.

If the receive control logic is requesting the NPR, the sequence is identical, with the following exceptions. The D-input of the RX/TX CYCLE flip-flop is low because D5-8 RX NPR RQ (1) L is low. When clocked, the flip-flop is cleared and D5-3 RX CYCLE H is asserted. This signal is sent to the CC/BA addressing mux (print D5-1), the DONE logic (print D5-4), the RX control logic (print D5-8), the REG/ERR register (print D4-6) on the M7812 module, and the NPR control logic (print D6-2) on the M7818 module. When the NPR cycle is complete, signal D5-3 RX NPR DONE H is asserted. This signal is sent to the RX control logic (print D5-8) where it clears the RX NPR RQ flip-flop and drives D5-8 RX NPR RQ (1) L high.

In addition, during a RX NPR sequence, D5-3 RX CYCLE H is used to generate two other signals. When the CC/BA logic is not in the updating cycle, D3-1 MASTER A L is low. It is inverted by E15 pin 6 and is ANDed with D5-3 RX CYCLE H to generate D5-3 RX NPR L. This signal clocks the buffered receiver data register (print D4-7) on the M7812 module and is used in the register selection logic (print D4-3) on the M7812 module. These two signals are also ANDed at bus driver E41 to assert BUS C1 L on the Unibus. This signal is asserted when the DQ11 becomes bus master and performs a DATO transaction to put a received character into memory.

4.5.4 Clock Loss, Register Select, and Done Control Logic

4.5.4.1 Functional Description – A simplified block diagram of the clock loss, register select, and DONE control logic is shown in Figure 4-29. The clock loss logic monitors the receive and transmit clocks. If either clock signal is lost, the logic generates a signal (RX CK LOSS L or TX CK LOSS L) that is used to set the appropriate flag in the REG/ERR CSR (bit 1 for RX and bit 0 for TX).

In addition, the RX clock loss logic turns on the DQ11 internal RC clock which continues the shifting operation until the sequence is ended normally at the end of the NPR cycle. Although received data is lost when the RX clock is lost, this method can save the good data that was shifted in before the RX clock loss.

Signal TEST LOOP (1) H is used to disable the clock loss logic when the DQ11 is operating in the test loop mode during servicing.

The register select logic decodes signals from the M105 Address Module (OUT HIGH H, OUT LOW H, SEL 4 H, and SEL 6 H) and bits 8–11 from the REG/ERR CSR (REG PT 8 (1) H–REG PT 11 (1) H), and generates the following signals:

1. Load signal for the MISC register (LD MISC L).
2. Load signal for the SYNC register (LD SYNC L).
3. Load signal for the REG/ERR CSR high byte (LD PTEE H) and low byte (LD ERR H).
4. LD CC/BA L that provides read/write control for bits 0–15 of the CC/BA memory.
5. LD EXT/TRANS H that provides read/write control for bits 16 and 17 of the CC/BA memory.
6. WEN (1) H which is the flag for bit 12 of the REG/ERR CSR.

The DONE control logic generates the signals that clear the RX and TX GO bits, RX and TX primary and secondary register DONE bits, and provides signals (TXS (1) H and RXS (1) H) to the CC/BA addressing mux to select the proper CC and BA registers. The logic has the capability to pick the correct address and DONE bit when the CC overflow causes a CC register to switch to primary or secondary.

Bit 5 (MASTER CLEAR) of the MISC register is also shown.

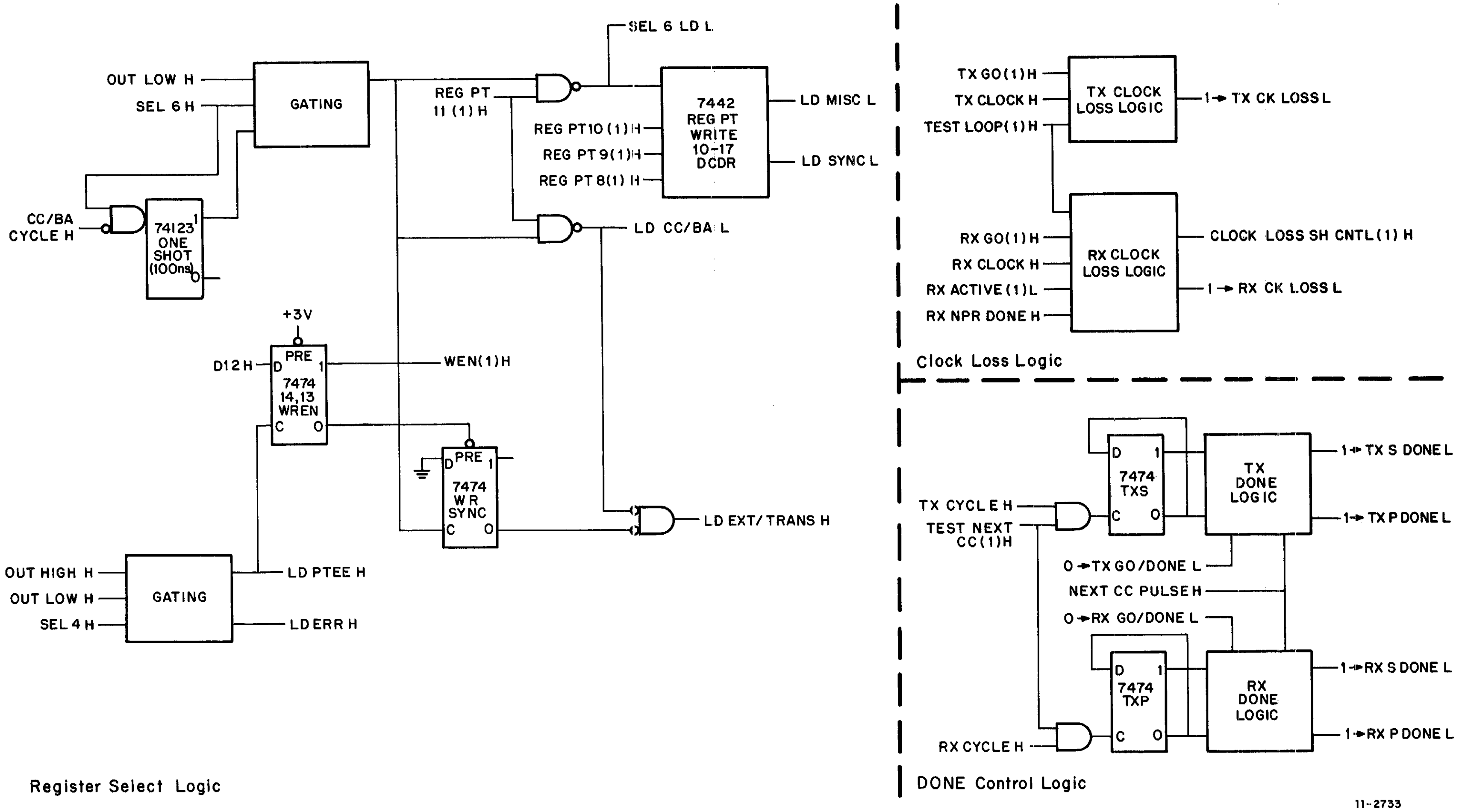


Figure 4-29 Block Diagram of the Clock Loss, Register Select and DONE Control Logic

4.5.4.2 Detailed Logic Description –

Clock Loss Logic

The clock loss logic is shown in the lower-left of drawing D-CS-M7813-0-1, sheet 6 which is designated D5-4.

The transmit clock signal D4-3 TX CLOCK H is sent to the input of one-shot TX CLOCK LOSS DLY. The other input of the one-shot is permanently connected to ground. The one-shot is a type 74123 which is retriggerable. This means that if the one-shot has been triggered and another triggering pulse (positive-going edge at pin 2) occurs before the one-shot times out, another pulse is generated. The one-shot pulse duration is set for approximately 500 ms. The duration of the triggering pulse is much shorter, so as long as signal D4-3 TX CLOCK H is present, the one-shot remains in the active state. The 0 output (pin 4) remains low once the one-shot is triggered and is sent to pin 10 of 3-input NAND gate E45. Pin 9 of E45 is high because signal D4-4 TX GO (1) H is asserted. The third input (pin 11) is connected to the inversion of D4-3 TEST LOOP (1) H. During normal operation, this signal is low; therefore, pin 11 is high. As long as the one-shot remains in the active state, the output (pin 8) of E45 remains high. This signal (D5-4 1 → TX CK LOSS L) indicates a loss of the transmit clock when it goes low.

If the transmit clock signal is interrupted for more than 500 ms, the TX CLOCK LOSS DLY one-shot times out. Its 0 output goes high and D4-4 1 → TX CK LOSS L goes low to indicate the loss of the transmit clock. This signal goes to the REG/ERR CSR (print D4-6) where it sets bit 0 and asserts flag D4-6 TX CK LOSS (1) H which is sent to the bus selectors to be read by the program. This signal also generates D4-6 TX ERR L which clears the error flag (TX GO and D4-6 ERR INTR H).

The clock loss flag is generated also if TX GO is set while the TX clock is not present.

The RX clock loss logic is more complex. The receive clock signal D4-3 RX CLOCK H is sent to one-shot RX CLOCK LOSS DLY. This retriggerable one-shot is identical to the TX clock loss one-shot. The 0 output of RX CLOCK LOSS DLY is sent to the clock input of flip-flop CK LOSS SH CNTL. When the one-shot times out, the positive transition at its 0 output clocks the CK LOSS SH CNTL flip-flop. The D-input of this flip-flop is connected to the output (pin 8) of AND gate E50 which is high when RX GO is set (D4-4 RX GO (1) H is high) and the normal operating mode is selected (D4-3 TEST LOOP (1) H is low). If the RX clock is interrupted for more than 500 ms, one-shot RX CLOCK LOSS DLY times out. This action clocks the CK LOSS SH CNTL flip-flop which sets it and asserts D5-4 CLOCK LOSS SH CNTL (1) H. This signal is sent to the M7812 module (print D4-3) and turns on the internal RC clock. This clock continues shifting in the character from the point at which the RX clock was lost. When the NPR cycle is complete, D5-3 RX NPR DONE H is asserted. This signal is inverted by E35 pin 4 and directly clears the CK LOSS SH CNTL flip-flop which shuts off the internal RC clock. When the CK LOSS SH CNTL flip-flop is cleared, the positive transition at its 0 output triggers one-shot RX CLOCK LOSS PULSE. This one-shot produces a 75 ns positive pulse that is ANDed with D4-4 RX GO (1) H at E39 to generate D5-4 1 → RX CK LOSS L. This signal goes to the REG/ERR CSR (print D4-6) where it sets bit 1 and asserts flag D4-6 RX CK LOSS (1) H. This signal generates D4-6 RX ERR L which clears RX GO and D4-6 ERR INTR H which is the error flag.

Register Select Logic

The register select logic is located in the upper left of drawing D-CS-M7813-0-1, sheet 6 which is designated D5-4.

Inputs to the register select logic are: D3-1 OUT LOW H, D3-1 OUT HIGH H, D3-1 SEL 4 H, and D3-1 SEL 6 H from the M105 Addressing Module; and D4-6 REG PT 8 (1) H–D4-6 REG PT 11 (1) H from bits 8–11 of the REG/ERR CSR.

When the REG/ERR CSR is addressed, D3-1 SEL 4 H is asserted. If the high byte of the register is selected, this signal is ANDed with D3-1 OUT HIGH H to assert D5-4 LD PTEE H at the output (pin 3) of AND gate E50. If the low byte is selected, D3-1 SEL 4 H is ANDed with D3-1 OUT LOW H to assert D5-4 LD ERR H at the output (pin 11) of the other E50 gate. D5-4 LD PTEE H and D5-4 LD ERR H are asserted simultaneously if the register is addressed with a word transfer selected.

When it is desired to select a secondary register, the REG/ERR CSR is addressed and bits 8–11 are set up to point to the desired register (Table 4-2). Then D3-1 SEL 6 H is asserted for a word operation to enable the selected register. This logic generates enabling signals for the MISC and SYNC registers only.

Table 4-2
Selection of Secondary Registers

REG/ERR Bits				Octal	Register
11	10	9	8		
0	0	0	0	0	Rx BA Primary
0	0	0	1	1	Rx CC Primary
0	0	1	0	2	Tx BA Primary
0	0	1	1	3	Tx CC Primary
0	1	0	0	4	Rx BA Secondary
0	1	0	1	5	Rx CC Secondary
0	1	1	0	6	Tx BA Secondary
0	1	1	1	7	Tx CC Secondary
1	0	0	0	10	Character Detect
1	0	0	1	11	Sync
1	0	1	0	12	Miscellaneous
1	0	1	1	13	Tx Buffer
1	1	0	0	14	Sequence
1	1	0	1	15	Rx BCC
1	1	1	0	16	Tx BCC
1	1	1	1	17	Polynomial

Selection of the MISC and SYNC registers is made with the REG PT WRITE DCDR (E44). It is a 7442 4-line to 10-line decoder, but it is connected to function as a 3 wire, binary-to-octal decoder. The three least significant inputs (D0, D1, and D2) are used as the binary code and the fourth input (D3) is used as the strobe or enabling input. The strobe (D3) must be low to enable the decoder.

The input signals are:

D0 = D4-6 REG PT8 (1) H

D1 = D4-6 REG PT9 (1) H

D2 = D4-6 REG PT10 (1) H

D3 = ANDing of D4-6 REG PT 11 (1) H and positive pulse from E40 pin 4.

Figure 4-30 shows the decoder and associated truth table. The binary coded octal designations for the SYNC and MISC registers are 11_8 and 12_8, respectively. In each case bit 11 is a 1.

For example, assume that it is desired to select the MISC register (12_8). In accordance with Table 4-2, bits 8–11 of the REG/ERR CSR are conditioned as follows:

bit 11 = 1 (D4-6 REG PT11 (1) H is high)
bit 10 = 0 (D4-6 REG PT10 (1) H is low)
bit 9 = 1 (D4-6 REG PT9 (1) H is high)
bit 8 = 0 (D4-6 REG PT8 (1) H is low)

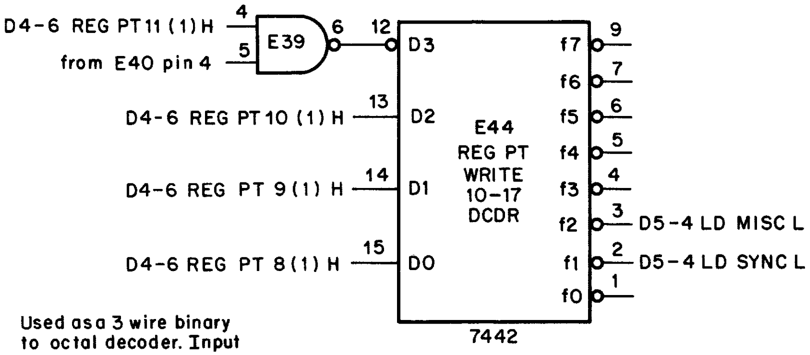
Decoder E44 inputs are therefore:

D2 = Low
D1 = High
D0 = Low

This selects output f2 (D5-4 LD MISC L) when the decoder is enabled (Figure 4-30). The M105 Address Module now asserts D3-1 OUT LOW H and D3-1 SEL 6 H. These signals go to 3-input NAND gate E45 pins 3 and 4, respectively. When D5-3 CC/BA CYCLE H goes high, one-shot E93 sends a 100 ns positive pulse to the third input (pin 5) of E45. This action generates a 100 ns negative pulse at E45 pin 6 (Figure 4-31) that is inverted by E40 and sent to pin 5 of NAND gate E39. The other input of E39 is held high by D4-6 REG PT11 (1) H. This drives E39 pin 6 low which enables the decoder and asserts D5-4 LD MISC L. The output of E39 is also sent to the DQ11 expander unit as D5-4 SEL 6 LD L.

There are four CC registers and four BA registers designated $0–7_8$. In each case, bit 11 (D4-6 REG PT11 (1) H) is low when a CC or BA register is selected. The inversion of D4-6 REG PT11 (1) H and the inversion of the pulse from E45 pin 6 are ANDed at E39 pins 1 and 2 to drive D5-4 LD CC/BA L low whenever a CC or BA register is selected. This signal is sent to E5 pin 10 (print D5-3) to generate D5-3 LD CC/BA SP 15–0 L that controls the read/write state of the CC/BA memory.

Bit 12 (14, 13 WRITE EN) of the REG/ERR CSR is associated with the register selection logic. The bit is stored in the 14, 13 WR EN flip-flop. The D-input of the flip-flop is controlled by the program via D4-2 D12 H. This bit is used in systems that require 18 bit memory addresses and allows bits 16 and 17 of the BA registers to be used.



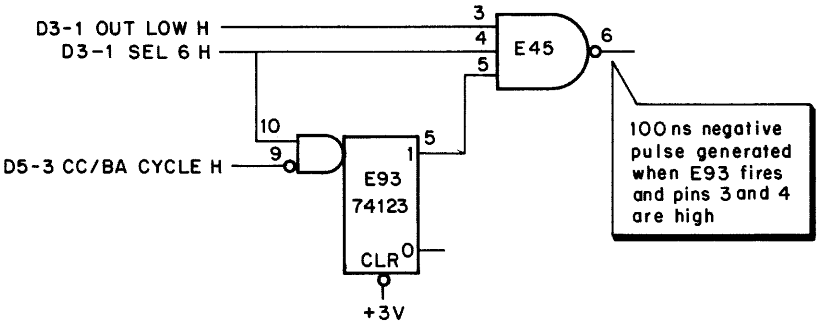
Used as a 3 wire binary to octal decoder. Input D3 is a strobe. Output is enabled low when D3 is low.

TRUTH TABLE

INPUTS				OUTPUTS							
D3	D2	D1	D0	f0	f1	f2	f3	f4	f5	f6	f7
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	H	H	H	H	H	H	H	H

11-2728

Figure 4-30 Register Select Decoder (E44)



100 ns negative pulse generated when E93 fires and pins 3 and 4 are high

11-2729

Figure 4-31 Pulse Generator in Register Select Logic

Assume that memory extension is required and the program asserts D4-2 D12 H. When the high byte of the REG/ERR CSR is addressed, D5-4 LD PTEE H goes high and clocks the 14, 13 WR EN flip-flop which sets it. This asserts D5-4 WEN (1) H which is the bit 12 flag. This signal is sent to the M7812 bus selectors where it can be read by the program. When the 14, 13 WR EN is set, the low from its 0 output directly sets the WR SYNC flip-flop. The low from the 0 output of this flip-flop is sent to E35 pin 2. The program uses address 76XXX6 during a DATO transaction to enable the selected BA register. The M105 Address Module asserts D3-1 OUT LOW H and D3-1 SEL 6 H which generates the 100 ns negative pulse at E45 pin 6. This pulse directly clears the 14, 13 WR EN flip-flop via gate E50. As previously described, this pulse enables D5-4 LD CC/BA L which controls the read/write operation for bits 0–15 of the CC/BA memory. D5-4 LD CC/BA L also goes to the other input (pin 3) of E35 which asserts D5-4 LD EXT/TRANS H. This signal controls the read/write operation for bits 16 and 17 of the CC/BA memory. The positive-going trailing edge of the 100 ns pulse from E45 pin 6 clocks the WR SYNC flip-flop which clears it and drives D5-4 LD EXT/TRANS H low.

DONE Control Logic

The DONE control logic is located in the right side of drawing D-CS-M7813-0-1, sheet 6 which is designated D5-4. The logic is divided into two identical sections: one for the transmit mode and one for the receive mode. Each section has four outputs that perform the following functions:

1. Clear the GO bit.
2. Set the primary DONE flag.
3. Set the secondary DONE flag.
4. Indicate whether the primary or secondary register is selected.

These output signals are generated by type 7450, dual 2-wide 2-input, AND-OR-invert gates. The outputs can be asserted by signals from the CC overflow detection logic or by signals from the sequence decoding logic on the M7817 module that is used only in the DQ11 expander unit. This discussion deals only with the signals from the CC overflow detection logic.

The operation of the logic is explained by discussing a specific example. Assume that a transmit operation is in process and the TX primary CC register is selected. In addition, the present CC updating cycle causes an overflow. The following conditions exist through the loading and incrementing of the current CC and BA registers.

1. The TXS flip-flop is cleared because the primary CC register is being used. The low from the 1 output of the TXS flip-flop inhibits both E57 gates. Neither D5-4 1 → TXS DONE L nor D5-4 1 → TXP DONE L is asserted.
2. D5-4 TXS (1) H is low which indicates that the primary register is being used. This signal goes to the CC/BA addressing logic (print D5-1).
3. D5-1 CC OFLOW H is high. It was asserted when the overflow occurred.
4. D5-3 NEXT CC PULSE H is low which inhibits gate E48 pin 6. D5-4 0 → TX GO L is not asserted.
5. D5-3 TX CYCLE H is asserted because a transmit operation is in process.
6. D5-3 TEST NEXT CC (1) H is low.

When it is time to load the next CC, D5-3 TEST NEXT CC (1) H is asserted which clocks the TXS flip-flop and sets it. This flip-flop is complemented with each clocking pulse. When TXS is set, D5-4 TXS (1) H is asserted which addresses the TX secondary CC register and it is loaded into the CC/BA counter. The 1 output of TXS puts a high on pin 9 of E57 which qualifies it.

Now, D5-3 NEXT CC PULSE H is asserted which puts a high on pin 10 of E57. This drives the output (pin 8) of E57 low which asserts D5-4 1 → TX P DONE L. This signal goes to the TX CSR (print D4-4) to directly set the TXP DONE bit which indicates that the use of the TX primary CC register has been completed.

If the TX secondary CC register (which is in the CC/BA counter) is empty, the counter reads all 0s and D5-1 CC OFLOW H remains asserted. This signal puts a high on pin 4 of E48; the other input (pin 5) is already high due to D5-3 NEXT CC PULSE H. This drives the output (pin 6) of E48 low which asserts D5-4 0 → TX GO L. This signal goes to the TX CSR (print D4-4) to directly clear the TX GO bit which inhibits further NPR cycles because there are no more characters to transfer to the transmit buffer.

If the TX secondary CC register contains a count, TX GO is not cleared. At the next NPR cycle, the transmit operation picks up the count from the secondary register.

4.5.5 Interrupt and Vector Control Logic

4.5.5.1 Functional Description – The interrupt and vector control logic is the controlling link between the interrupt requesting logic in the DQ11 and the M7821 Interrupt Module that actually initiates the interrupt request.

Rather than discuss the interrupt and vector control logic alone, its interaction with the requesting logic and the M7821 is discussed for a typical example in the detailed logic discussion that follows.

The remainder of this section discusses certain topics that are prerequisites to the discussion of the interrupt transaction.

Interrupt Request Signals

Three interrupt requesting signals are used:

D4-4 TX/ERR INTR L
D4-4 RX/CHAR INTR L
D2-1 DS INTR L.

Signal D4-4 TX/ERR INTR L is sent to the interrupt and vector control logic from the TX CSR. This signal is asserted by the following conditions, providing the appropriate interrupt enable bit is set by the program.

1. Setting the TX DONE primary or secondary bits in the TX CSR.
2. Setting the ERR INTR bit in the REG/ERR CSR. This bit is set when any one of the following error bits is set in the REG/ERR CSR. The error bits are: RX clock loss, TX clock loss, RX latency, TX latency, RX non-existent memory, TX non-existent memory, RX BCC, and VRC.

Signal D4-4 RX/CHAR INTR L is sent to the interrupt and vector control logic from the RX CSR. This signal is asserted by the following conditions, providing the appropriate interrupt enable bit is set by the program.

1. Setting the RX DONE primary or secondary bits in the RX CSR.
2. Setting the CHAR INT bit in the RX CSR. This bit is set when any one of three hard-wired characters is detected in the M7818 module. This bit is also set by the programmable character detection logic if the DQ11-BB option is used.

Signal D2-1 DS INTR L is sent to the interrupt and vector control logic from the Data Set Control Module M7818. When any one of the following three data set signals are detected coming on or off, the DATA SET INTR bit (TX CSR bit 15) is set and D2-1 DS INTR L is asserted. The signals are: RING (ring indicator), CO (carrier or signal quality detector), and CS (clear to send). In addition, two user option bits (UO13 and UO14) can be connected via jumpers to assert D2-1 DS INTR L.

Features of the M7821 Interrupt Module

The M7821 Interrupt Module does not have two identical master control sections. In the case of the DQ11, master control section A (identified by request input pins U1 and V1) is used to allow the DQ11 to become bus master with an NPR. Pin U2 is permanently connected to ground so that the DQ11 performs one bus cycle per NPR (print D3-1).

Master control section B is used for BRs. The jumper for vector bit 2 is left installed and pin D2 is connected to D5-5 VECTOR BIT 2 (1) H from the interrupt and vector control logic. This allows the BR section to generate two vector addresses per device.

The BR section has a special circuit that improves NPR latency time. It requires that the NPR jumper associated with pin J1 be left installed and pin J1 be connected to BUS NPR L from pin U2 (print D3-1). If D5-5 BG IN H is asserted while BUS NPR L is asserted, the circuit blocks the grant signal and asserts BUS SACK L. When BUS BBSY L is cleared by the last bus master, the M7821 clears BUS SACK L. The processor now services the NPR which improves the NPR latency time for the DQ11. The M7821 keeps D3-1 BR L asserted so that when the NPR transaction is finished the processor asserts D5-5 BG IN H again.

Priority Select Card

Socket E89 on the M7813 module (print D5-5) is wired to accept the priority select card. Four cards are available; one for each BR level (4, 5, 6 and 7). The recommended level for the DQ11 is BR5 and it is shipped with a BR5 priority select card installed. Figure 4-32 shows the BR5 priority select card and how it interconnects with the M7821 Interrupt Module and the interrupt and vector control logic. On the BR5 priority select card, the bus request signals for levels 4, 6, and 7 are not connected. The bus grant in signals for levels 4, 6, and 7 are directly connected to the grant out signals for the corresponding levels. This allows bus grant signals for levels 4, 6, and 7 to pass through the DQ11 to other devices.

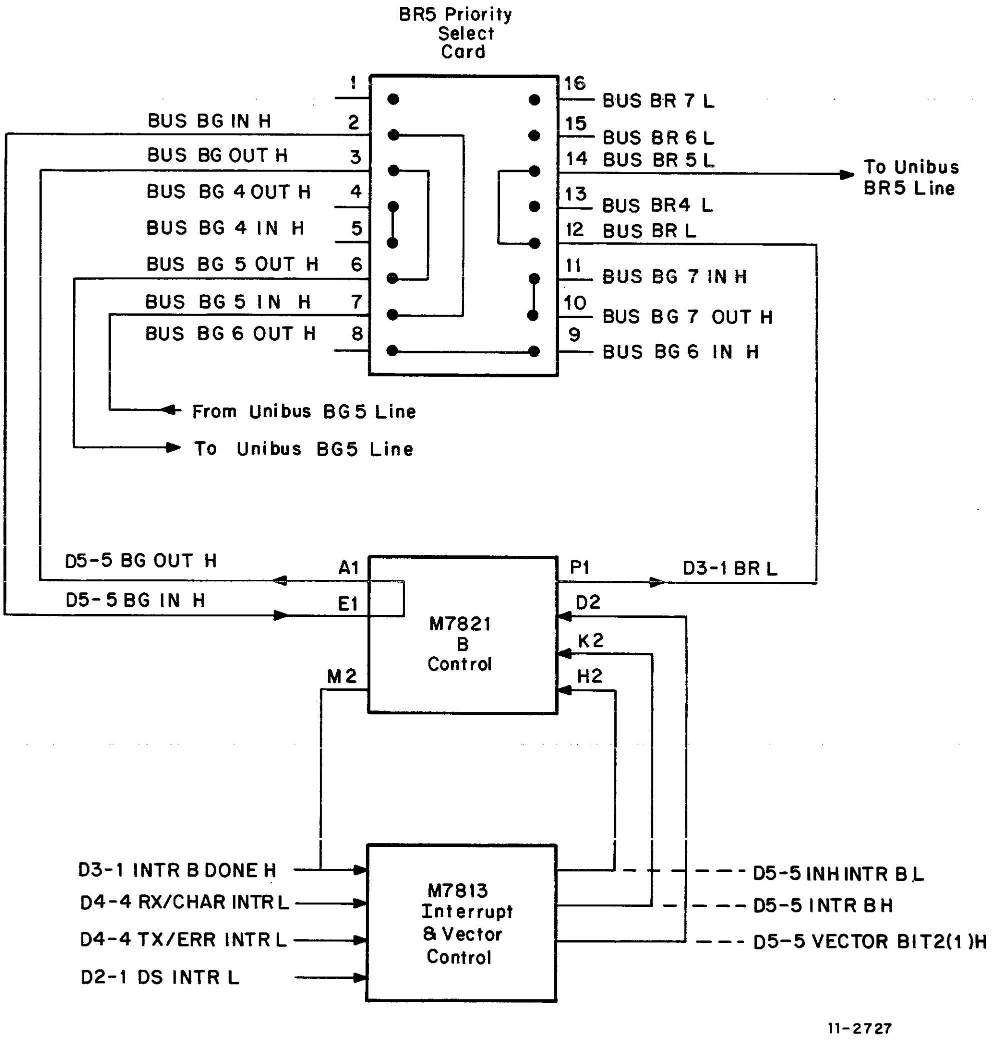


Figure 4-32 BR5 Priority Select Card Interconnection

When the M7821 is requesting a BR, it asserts D3-1 BR L on pin P1. This signal goes to pin 12 (BUS BR L) of the priority card and out pin 14 (BUS BR 5 L) which is connected to the Unibus. A BR on level 5 has been requested. The processor responds with the bus grant signal (BUS BG 5 IN H) to pin 7 on the priority card. It passes through the card and out pin 2 (BUS BG IN H) to pin E1 (D5-5 BG IN H) of the M7821 module. It is blocked by the M7821 to start the interrupt sequence. If the DQ11 is not requesting a BR on level 5 but another device further down the line is requesting a BR5, the bus grant signal is not blocked by the DQ11's M7821 module. The grant signal enters pin E1 of the M7821 and out pin A1 (D5-5 BT OUT H) to pin 3 (BUS BG OUT H) of the priority card. It passes through the card and out pin 6 (BUS BG 5 OUT H) which is connected to the Unibus. The grant travels along this Unibus line (BG5) until it is blocked by the requesting device.

4.5.5.2 Detailed Logic Description – This discussion covers a typical interrupt transaction and shows the interaction among the interrupt and vector control logic, M7821 Interrupt Module, and other sections of the DQ11 logic.

Assume that the RX DONE primary bit in the RX CSR has been set. This event starts the sequence that requests an interrupt on vector A (XX0).

1. In order to allow the setting of the RX DONE primary bit to request an interrupt, the program must first set the RX DONE IE bit in the CSR. This asserts D4-4 RX DONE IE (1) H and when the RXP DONE flip-flop (print D4-4) is set, D4-4 RX/CHAR INTR L is asserted at the output (pin 8) of gate E44.

2. D4-4 RX/CHAR INTR L is sent to the interrupt and vector control logic (print D5-5). This signal is inverted by E40 and puts a high on pin 12 of E62. The other input (pin 13) of E62 is already high because the RX/CHAR INTR is cleared. The output (pin 11) of E62 goes low which asserts D5-5 INTR B H at E62 pin 6.

3. Signal D3-1 INTR B DONE H from M7821 pin M2 is low and is sent to the interrupt and vector control logic. It is inverted by E40 to hold D5-5 INH INTR B L high.

4. Signals D5-5 INTR B H and D5-5 INH INTR B L (which are both high) are sent to M7821 pins K2 and H2, respectively. When both these signals are high, the M7821 asserts D3-1 BR L at pin P1 (print D3-1).

5. D3-1 BR L leaves the M7821 module and passes through the priority card to the Unibus as BUS BR 5 L (Figure 4-31). This is a request for bus mastership.

6. The processor examines BUS BR 5 L and, if it has the highest request priority, the processor asserts BUS BG 5 IN H provided BUS SACK L is clear. BUS BG5 IN H passes through the priority card to pin E1 of the M7821 module where it is identified as D5-5 BG IN H because it also goes to the interrupt and vector control logic. This signal clears D5-5 BG OUT H on pin A1 of the M7821 module which blocks the bus grant signal and prevents it from reaching any following devices on the BR 5 level on the Unibus.

7. D5-5 BG IN H is sent to pin 13 of NAND gate E53. It is inverted by this gate and again by E15. The positive transition at E15 pin 8 clocks the VECTOR BIT 2 flip-flop. The flip-flop is cleared because its D-input is low. The D input of VECTOR BIT 2 is connected to E62 pin 11 which is low (step 2). When the flip-flop is cleared, it drives D5-5 VECTOR BIT 2 (1) H low.

8. D5-5 VECTOR BIT 2 (1) H, which is low, is sent to pin D2 of the M7821 module. When this signal is low, the interrupt is requested on vector A (XX0). This is described in detail in a subsequent section.

9. Signal D5-5 BG IN H on pin E1 of the M7821 also causes the bus request signal (D3-1 BR L) to be cleared and BUS SACK L to be asserted on pin T2.

10. The processor receives BUS SACK L and clears BUS BG 5 IN H which prevents the issuance of further grants from the processor during this interrupt transaction.

11. When the current bus master completes its transaction, it clears BUS BBSY L and BUS SSYN L. In response to this action, the M7821 asserts its own BUS BBSY L (pin D1) and clears BUS SACK L (pin T2). When BUS BBSY L is asserted, signal MASTER B L is asserted at pin S2 and is sent to pins P2 and R2 of the M7821 module. This asserts BUS INTR L at pin M1 and places the vector address (XX0) on Unibus data lines BUS D02–D08 L. The DQ11 is now bus master.

12. The processor receives BUS INTR L, reads the vector address, and responds by asserting BUS SSYN L.

13. In response to BUS SSYN L (pin C1), the M7821 module asserts D3-1 INTR B DONE H at pin M2 which is sent to pin S1 (not labeled but sometimes identified as B MASTER CLEAR H). This clears BUS BBSY L, MASTER B L, BUS INTR L, and the vector address. This constitutes active release of the bus to the processor which clears BUS SSYN L when it receives the cleared BUS INTR L signal. The processor goes to the interrupt service routine at the specified vector address (XX0).

14. Signal D3-1 INTR B DONE H from the M7821 module is also sent to the interrupt and vector control logic (print D5-5). When it goes high (step 13), the positive transition clocks the RX/CHAR INTR flip-flop. It sets the flip-flop because its D-input is high as a result of the VECTOR BIT 2 flip-flop being previously cleared (step 7).

15. When the RX/CHAR INTR flip-flop is set, it drives D5-5 INTR B H low which prevents the M7821 from requesting another interrupt until a requesting signal (D4-4 TX/ERR INTR L, D2-1 DS INTR L or D4-4 RX/CHAR INTR L) is asserted (goes high) again.

16. The situation that requested the interrupt (setting the RX DONE primary bit of the RX CSR) must be cleared by the program. When it is done, D4-4 RX/CHAR INTR L goes high. This signal is inverted by E40 and directly clears the RX/CHAR INTR flip-flop.

It is possible for the program to leave the RX DONE primary bit of the RX CSR set (D4-4 RX/CHAR INTR flip-flop remains set) and request another interrupt via signal D2-1 DS INTR L or D4-4 TX/ERR INTR L (print D5-5). Assuming that this is done, pin 1 of E62 is high because one of these request signals is asserted. Pin 2 of E62 is also high because the TX/ERR/DS INTR flip-flop is cleared. The output (pin 3) of E62 goes low which asserts D5-5 INTR B H.

The interrupt request sequence proceeds as described in the previous example. D5-5 BG IN H is asserted by the M7821 module and clocks the VECTOR BIT 2 flip-flop. The flip-flop is set because its D-input is high. When the flip-flop is set, it drives D5-5 VECTOR BIT 2 (1) H high which sets up the request on vector B (XX4). The 0 output of the VECTOR BIT 2 flip-flop puts a high on the D-input of the TX/ERR/DS INTR flip-flop and a low on the D-input of the RX/CHAR INTR flip-flop. The interrupt transaction continues and D3-1 INTR B DONE H is asserted. This signal clocks the TX/ERR/DS INTR flip-flop which sets it and drives D5-5 INTR B H high. D3-1 INTR B DONE H also clocks the RX/CHAR INTR flip-flop. Because of the hold-set feature used in this flip-flop, the clocking signal has no effect. If the clocking signal was effective, the RX/CHAR INTR flip-flop would have been cleared and it would have kept D5-5 INTR B H asserted despite the action of the TX/ERR/DS INTR flip-flop.

Both the RX/CHAR INTR and TX/ERR/DS INTR flip-flops have the hold-set features. In the situation just described, the RX/CHAR INTR is set and its D-input is low. Its 0 output (pin 8), which is low, is fed back to the preset input (pin 10). As long as this input is low, the flip-flop remains in the set state. This situation overrides the clock input; therefore, if the flip-flop is clocked with the D-input low, it cannot be cleared. If the clear input (pin 13) is made low while the preset input (pin 10) is still held low, the 1 output does not change state but the 0 output goes high. This releases the preset input and the 1 output goes low so the flip-flop now is in the cleared state.

This feature prevents the RX/CHAR INTR and TX/ERR/DS INTR flip-flops from interfering with one another but allows them to be cleared when the appropriate request signal is dropped.

Vector Address Generated by M7821 Module

Each device interrupt vector requires four address locations (two words) which implies only even-numbered addresses.

A further constraint is that all vector addresses must end in 0 or 4. The vector address is specified as a three-digit, binary-coded, octal number using Unibus data bits D08–D00. Because the vector must end in 0 or 4, bits D01 and D00 are not specified (they are always 0) and bit D02 determines the least significant octal digit of the vector address (0 or 4). The logic on the M7821 module sends only seven bits (D08–D02) to the PDP-11 processor to represent the vector address.

The vector address is configured by jumpers in the lines for bits D08–D02. In this case, the M7821 module is required to generate two vector addresses so the jumper for bit 2 must be left in. The two most significant octal digits of the vector address are determined by jumpers in lines D08–D03. With the jumper in, a 1 is generated on the associated Unibus data line. With the jumper out, a 0 is generated on the associated Unibus data line.

Figure 4-33 shows the determination of vector addresses for two DQ11s in a system. It is desired to have the first DQ11 generate 300 for vector A and 304 for vector B. The second DQ11 follows with 310 for vector A and 314 for vector B. Using the first DQ11 as the example, the jumper configuration is as follows: jumpers 8, 5, 4, and 3 out and jumpers 7 and 6 in. The circuit above the table in Figure 4-33 shows the gates inside the M7821 module that are associated with bit D02. Assume that D4-4 RX/CHAR INTR L is requesting the interrupt. This request is for vector A (300). As the sequence progresses, the VECTOR BIT 2 flip-flop (print D5-5) is cleared which drives D5-5 VECTOR BIT 2 (1) H low. This signal is sent to E9 pin 12 in the M7821 module (Figure 4-32). Later in the sequence, MASTER B L is asserted at pin S2 of the M7821 and fed back in to pins P2 and R2 of this module. This low signal is inverted by E7 and puts a high on the other input (pin 11) of E9. The output (pin 13) of E9 goes high and this signal appears on Unibus data line D02. The Unibus data lines use negative logic so this high signal represents a logical 0. With the jumper configuration as shown and bit D02 = 0, the M7821 module generates vector address 300.

If D4-4 TX/ERR INTR L or D2-1 DS INTR L requests the interrupt, signal D5-5 VECTOR BIT 2 (1) H is high and bit D02 = 1; therefore, the M7821 module generates vector address 304.

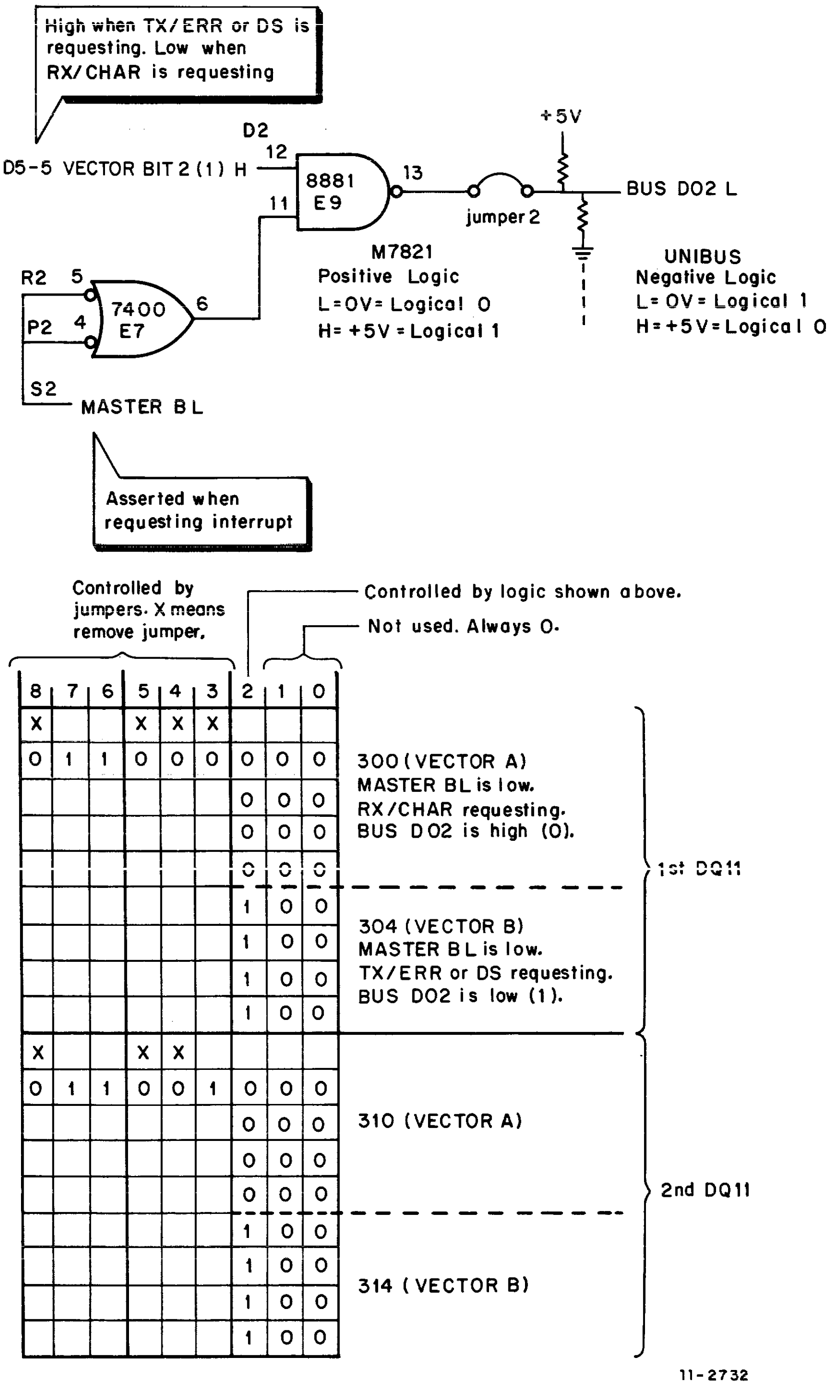
The logic within the M7821 module for vector bits D08–D03 is identical and is shown in Figure 4-34. The output of gate E7 goes to both inputs of the 8881 bus drivers associated with vector bits D08–D03 (bit D03 is shown as typical). The first case is for the jumper installed. When MASTER B L is asserted, it puts a high on both inputs (pins 8 and 9) of E9 which drives its output low. This low signal appears on Unibus data line D03 where it is represented as a logical 1 (on the Unibus, L = 0 V = logical 1). The 8881 driver (E9) is a bare collector NAND gate. When both inputs are high, the last stage transistor in the gate is turned on. The emitter of this transistor is connected to ground in the device so the +5 V, via the Unibus terminator network, is connected to ground and the driver output is low.

With the jumper out, driver E9 has no effect. The +5 V in the bus terminator holds Unibus bit D03 high which is represented as a logical 0 (on the Unibus H = +5 V = logical 0).

4.5.6 Transmit Control Logic

4.5.6.1 Functional Description – A simplified block diagram of the transmit control logic is shown in Figure 4-35. The logic performs several functions that are interrelated but can be described separately. The major functional areas are listed below in order of discussion.

1. Transmit Shift Counter (E81) and Transmit Bit Counter (E86)
    a. TX Shift Counter (E81). This counter is loaded with the 2's complement of the number of bits per character selected by the program. It counts upward toward overflow (count 0) which denotes the end of the character. At overflow, the counter generates a carry out (CO) pulse which returns this counter and the TX bit counter (E86) to the load mode. The CO pulse also initiates other functions in the TX control logic.
    b. TX Bit Counter (E86). This counter is loaded and clocked by the same signals that load and clock the shift counter (E81). The TX bit counter is always loaded with count 0. It starts at zero and is incremented in synchronism with the shift counter (E81). The TX bit counter outputs are the select inputs for the output multiplexers in the TX shift register. As the counter is incremented, these outputs change and select each multiplexer input, in sequence, to perform the parallel-to-serial conversion of the character to be transmitted.



8	7	6	5	4	3	2	1	0		
X			X	X	X					1st DQ11
0	1	1	0	0	0	0	0	0	300 (VECTOR A) MASTER BL is low. RX/CHAR requesting. BUS DO2 is high (0).	
						0	0	0		
						0	0	0		
						0	0	0		
						1	0	0	304 (VECTOR B) MASTER BL is low. TX/ERR or DS requesting. BUS DO2 is low (1).	
						1	0	0		
						1	0	0		
						1	0	0		
X			X	X						2nd DQ11
0	1	1	0	0	1	0	0	0	310 (VECTOR A)	
						0	0	0		
						0	0	0		
						0	0	0		
						1	0	0	314 (VECTOR B)	
						1	0	0		
						1	0	0		
						1	0	0		

Figure 4-33 Generation of Two Vector Addresses on M7821 Interrupt Module

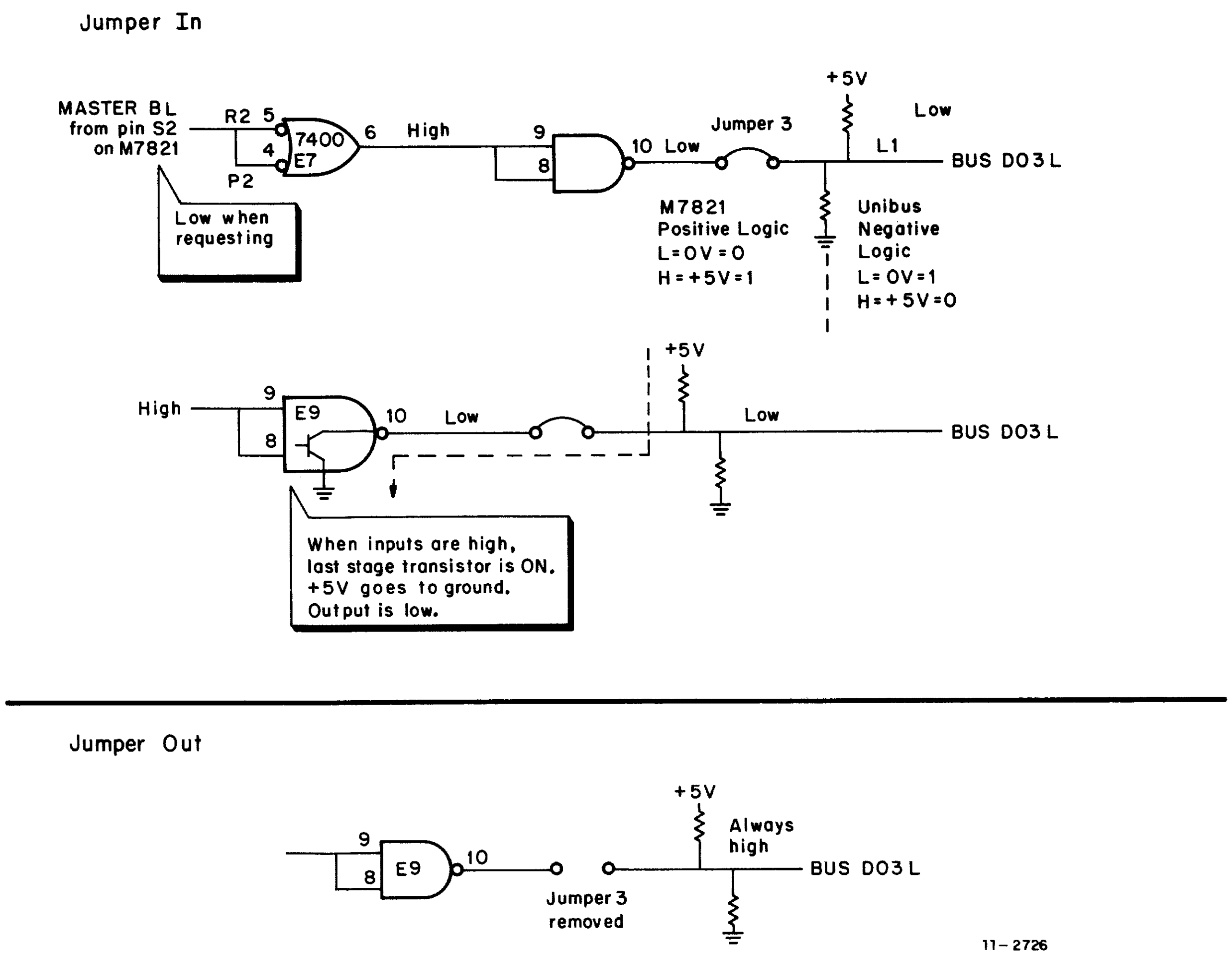


Figure 4-34 Configuration of Vector Bits 03–08

2. Send Enable Flip-Flops and Input Priority Gating. The flip-flop outputs are enabling signals that are used as inputs to the sync/data enable multiplexer. These signals are also sent to other modules. The input gating to the flip-flops establishes the priority for selecting the enabling signals based on the type of character. The priority, in descending order, is: DLE, BCC, SYNC, Data and PAD.

3. Sync/Data Enable Multiplexer. The sync and data signals from the send enable flip-flops are sent to the inputs of the sync/data enable multiplexer. They are selected to provide enabling signals for the sync register and TX data register. Selection is a function of the TX counter MSB input and output and the output of the character count logic.

4. Character Count Logic. When handling data in the double-character mode, this logic controls the select input of the sync/data enable multiplexer to allow both bytes of the TX data register to be enabled.

5. Save Sync Logic. The idle character, in the transparent mode, is Data Link Escape (DLE) followed by the contents of the sync register; that is, DLE-SYNC, DLE-SYNC, etc. This logic allows the sync register to be enabled and disabled so that idle characters can be transmitted.

6. Vertical Redundancy Check (VRC) Logic. When VRC is selected, this logic examines the data to be transmitted and puts a 1 in the most significant bit of each character in which the selected VRC (odd or even) is detected to be in error.

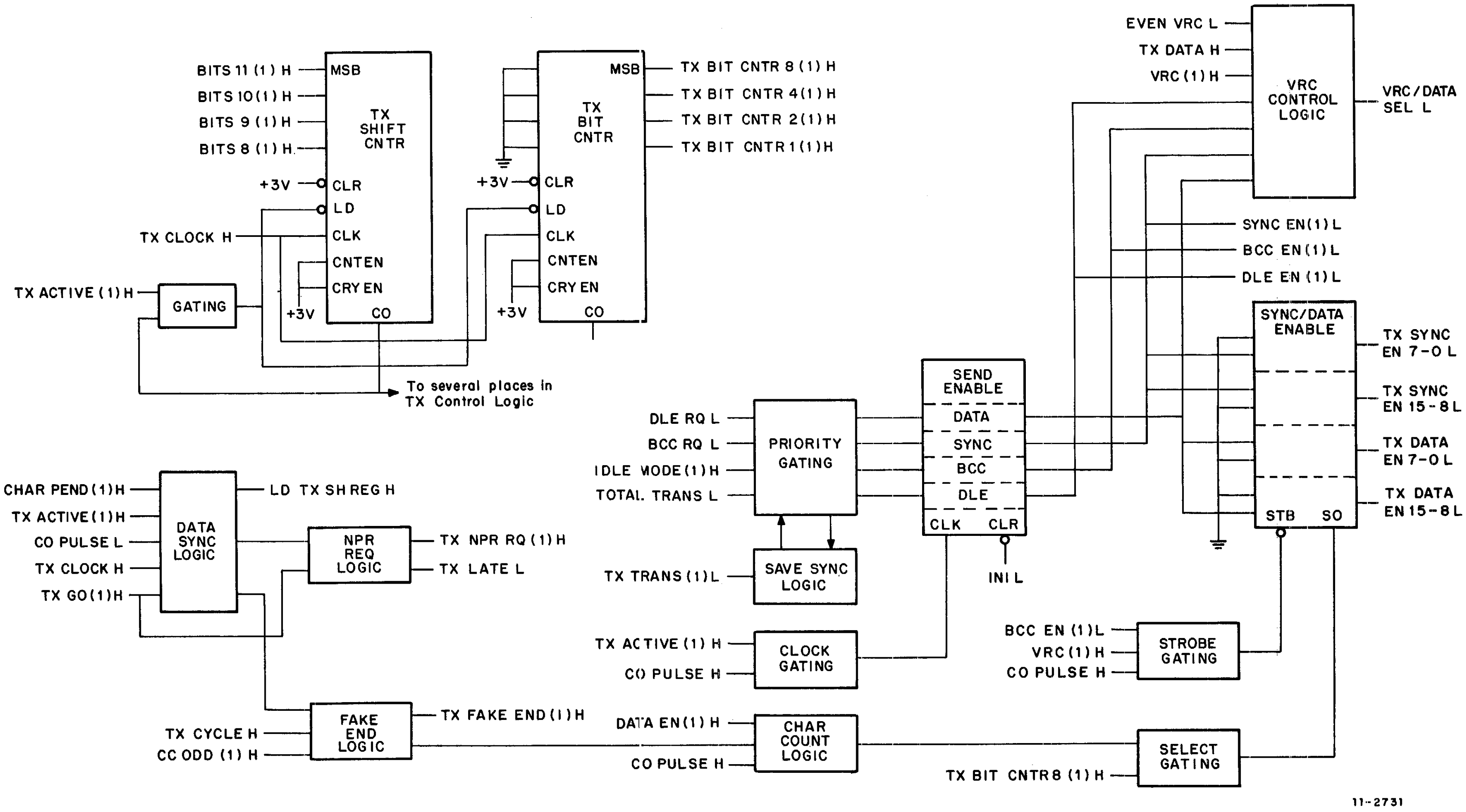


Figure 4-35 Block Diagram of Transmit Control Logic

7. Fake End Logic. In the double character mode with an odd count detected, only one byte of the last word contains a character to be transmitted. This logic detects the situation and allows the empty byte to be ignored and fakes the end of the current transmission. This permits the next NPR to be started sooner. It also sends a signal to the TX BCC logic to allow the appending of the BCC character in the correct place.

8. Data Sync/NPR Logic. At the start of a transmission, this logic generates a data enable and synchronizes the loading of the TX shift register. It also generates an NPR request after data is moved from the TX buffer to the TX shift register.

4.5.6.2 Detailed Logic Description – The circuit schematic for the transmit control logic is contained in drawing D-CS-M7813-0-1 (Rev H) sheet 8 which is designated D5-6.

Transmit Shift Counter (E81) and Transmit Bit Counter (E86)

The transmit shift counter (TX SHIFT CNTR) is designated E81 and is located in the right center section of print D5-6. The transmit bit counter (TX BIT CNTR) is designated E86 and is located in the lower left section of print D5-6. Both devices are 74161 synchronous 4-bit counters. The configuration of these counters is described below.

Both Counters

1. Count enable inputs (CNT EN and CRY EN) are held high by +3 V so that the counter is permanently enabled.

2. The clear input (CLR) is disabled by holding it permanently high with +3 V.

3. D4-3 TX CLOCK H is sent to the clock input (CLK). The positive-going edge of this signal increments the counter.

4. When the load input (LD) of the counter is low, the counter is inhibited and the outputs agree with the data inputs after the next clock pulse. The load input is enabled (driven low) under two conditions; when the TX ACTIVE flip-flop is cleared or when TX BIT CNTR (E81) overflows.

Transmit Shift Counter (E81)

1. The data inputs come from MISC register bits 8–11 that select the number of bits per character. The signals are listed below.

   D4-3 BITS 11 (1) H (MSB)
   D4-3 BITS 10 (1) H
   D4-3 BITS 9 (1) H
   D4-3 BITS 8 (1) H

2. The outputs are not used.

3. The carry out (CO) output is used. This output goes high at the count of minus 1 (2's complement notation) and goes low at the next clock pulse when the counter overflows. This denotes the end of the character. In subsequent references to this operation, it is stated that a CO pulse is generated at overflow.

Transmit Bit Counter (E86)

1. The data inputs are permanently connected to ground so that the counter is always loaded with count 0.

2. The four outputs are listed below.

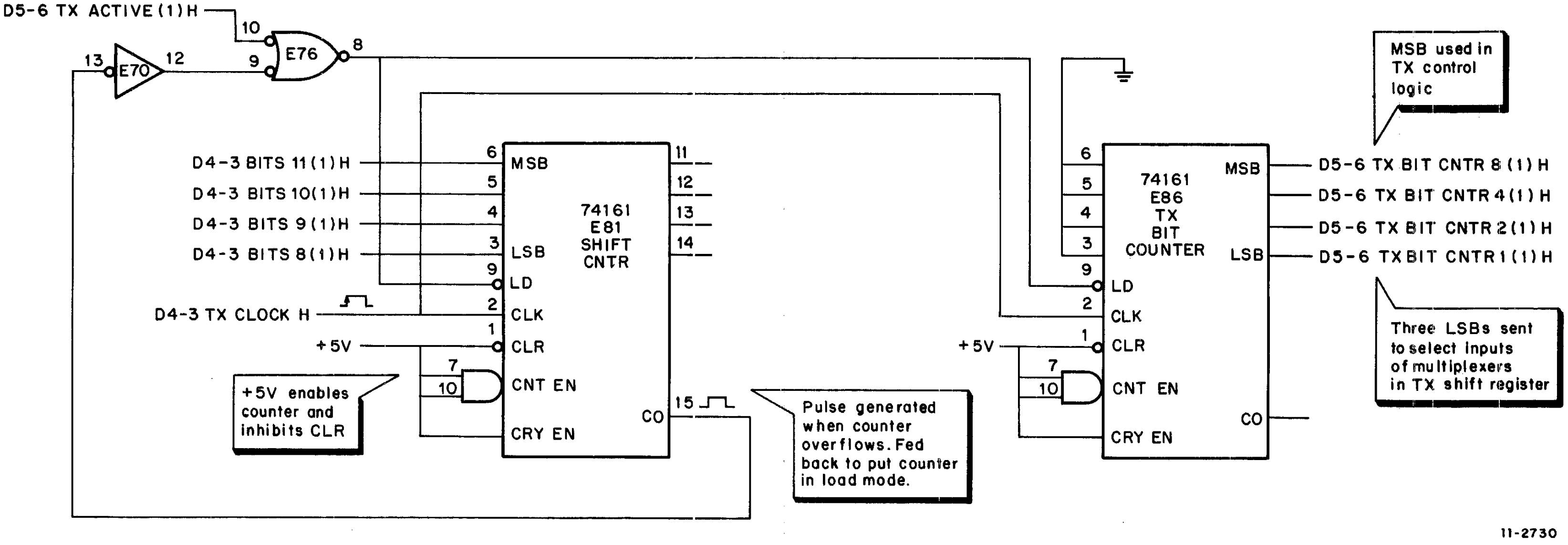
   D5-6 TX BIT CNTR 8 (1) H (MSB)
   D5-6 TX BIT CNTR 4 (1) H
   D5-6 TX BIT CNTR 2 (1) H
   D5-6 TX BIT CNTR 1 (1) H

   The most significant bit (MSB) is used in the TX control logic. The other three bits are used as select signals for the output multiplexer in the TX shift register and the SYNC register.

3. The carry out (CO) pulse is not used.

A typical load and count operation for the TX SHIFT CNTR and TX BIT CNTR is described. Figure 4-36 shows the counters and some associated logic. The operation that is described assumes that 12 bits per character has been selected. Figure 4-37 shows the load and count sequence graphically.

The TX SHIFT CNTR (E81) is to be loaded with the binary value of MISC register bits that represent the selection of 12 bits per character (Figure 4-37). The value is 0100 (MSB to the left) which is the 2's complement of 12_{10}.



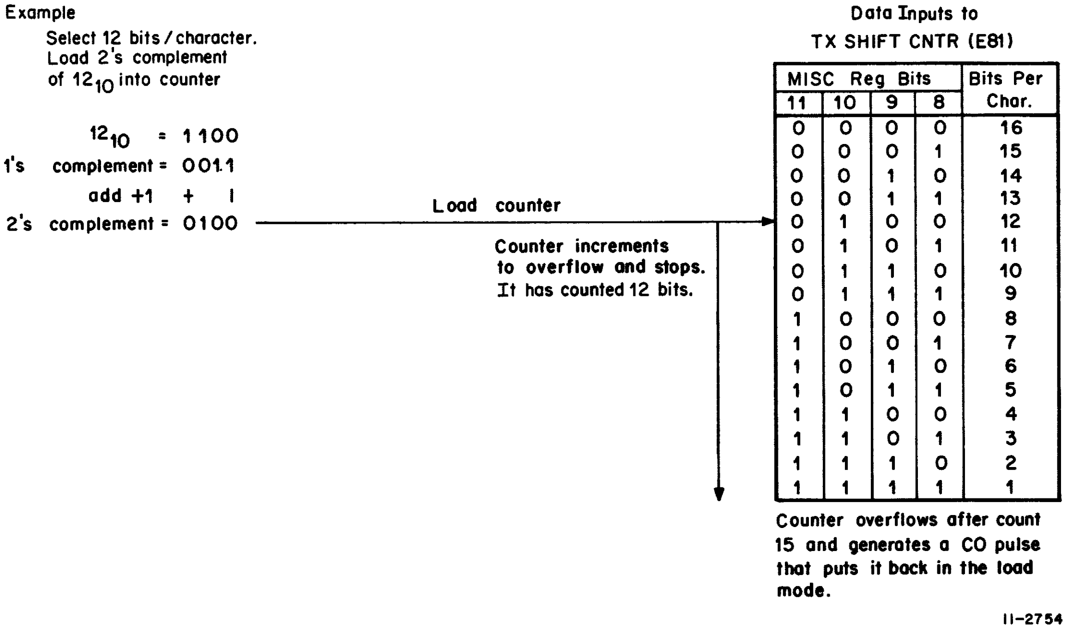
+5V enables counter and inhibits CLR

Pulse generated when counter overflows. Fed back to put counter in load mode.

MSB used in TX control logic

Three LSBs sent to select inputs of multiplexers in TX shift register

Figure 4-36 TX Shift Counter, TX Bit Counter and Load Logic



MISC Reg Bits 11	10	9	8	Bits Per Char.
0	0	0	0	16
0	0	0	1	15
0	0	1	0	14
0	0	1	1	13
0	1	0	0	12
0	1	0	1	11
0	1	1	0	10
0	1	1	1	9
1	0	0	0	8
1	0	0	1	7
1	0	1	0	6
1	0	1	1	5
1	1	0	0	4
1	1	0	1	3
1	1	1	0	2
1	1	1	1	1

Figure 4-37 Graphical Representation of TX Shift Counter Load and Count Sequence

The program sets the value in bits 8–11 of the MISC register which in turn sends it to the data inputs of TX SHIFT CNTR (E81). This operation is performed before the first character is brought in for transmission; therefore, the TX ACTIVE flip-flop is cleared and D5-6 TX ACTIVE (1) H is low. This signal, via E79 pin 8, puts a low on the load input (LD) of both counters (E81 and E86). The next positive transition of D4-3 TX CLOCK H inhibits both counters and loads them. TX SHIFT CNTR (E81) is loaded with the 2's complement of 12_{10} and TX BIT CNTR (E86) is loaded with 0s. As long as the load inputs are held low, the counters are not incremented by the clock signal. Assume now that the first sync character is transferred to the DQ11 for transmission.

Signal D5-6 TX ACTIVE (1) H goes high which inhibits the load inputs of both counters and allows them to be incremented by the clock. D5-6 TX ACTIVE (1) H remains high as long as there is anything to transmit (SYNC, BCC, data, etc.). Under these conditions, subsequent load operations are accomplished by the CO pulse from TX SHIFT CNTR when it overflows. Both counters continue to increment together. The three least significant outputs of TX BIT CNTR are sent to the select inputs of the SYNC register output multiplexers (print D4-7). The first value selects input 4 and as TX BIT CNTR (E86) is incremented the multiplexers ripple up through input 15 (total of 12 bits). This operation serializes the 12-bit sync character and sends it out on the serial data line. On the next count, the counter overflows and generates a positive CO pulse that permits another load operation. This load, count and overflow process continues until there are no more characters to transmit.

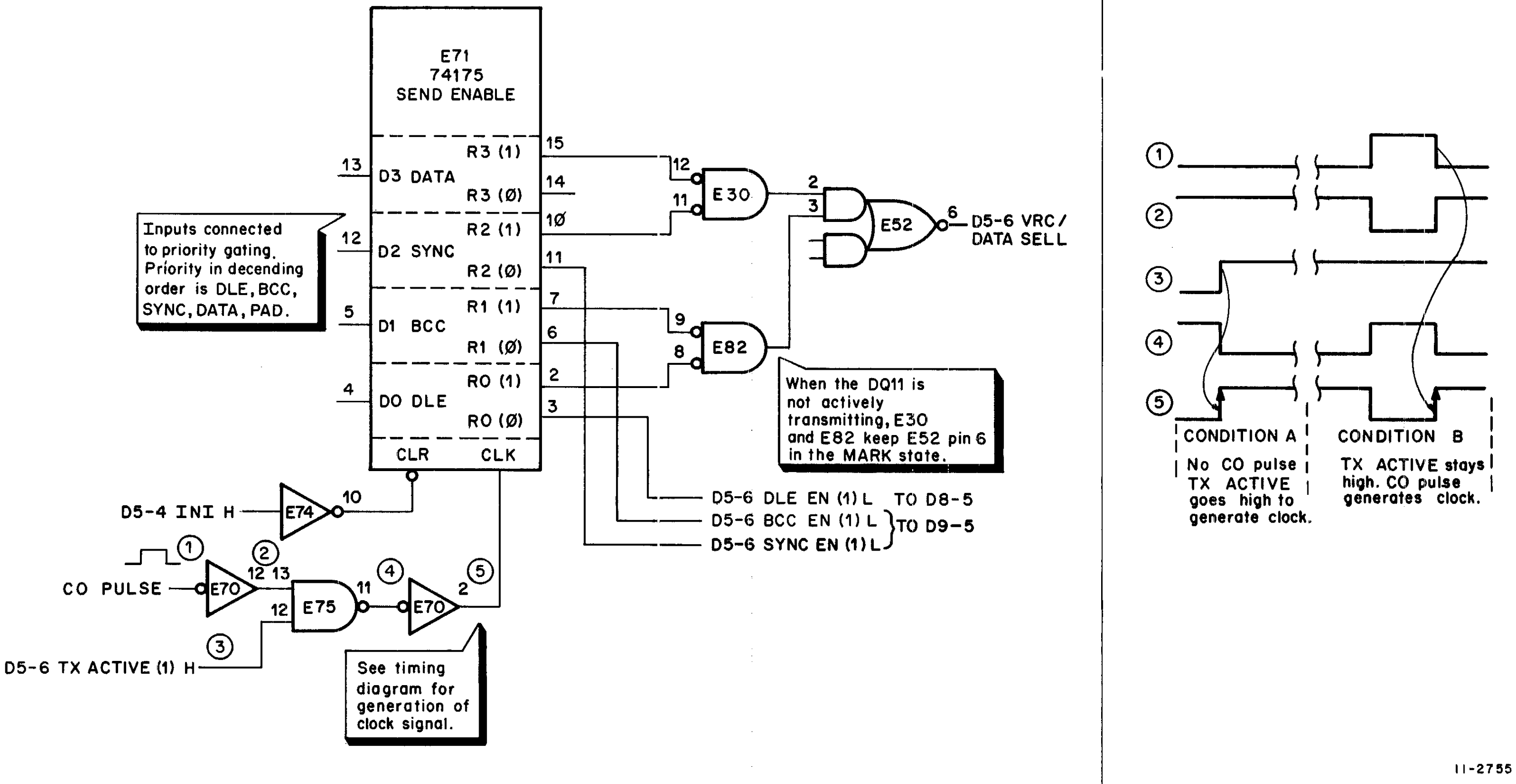
Send Enable Flip-Flops and Input Priority Gating

The SEND ENABLE flip-flop (E71) is a quad flip-flop package (74175) with complementary outputs and a common clock. It produces enabling signals for DLE, BCC, SYNC and data characters which are sent externally to the following places.

Output	Destination
D5-6 DLE EN (1) L	M7817 Module (D8-5)
D5-6 BCC EN (1) L	M7816 Module (D9-5)
D5-6 SYNC EN (1) L	M7816 Module (D9-5)

Some of the E71 outputs are used in the TX control logic as described below.

Figure 4-38 shows the SEND ENABLE flip-flops with associated output gating and clock input gating. The input priority gating is not shown. The gating network (D5-6) that is connected to the SEND ENABLE inputs establishes the priority for selecting the enabling signals. The priority, in descending order, is DLE, BCC, SYNC, Data and PAD.



Inputs connected to priority gating. Priority in decending order is DLE, BCC, SYNC, DATA, PAD.

When the DQ11 is not actively transmitting, E30 and E82 keep E52 pin 6 in the MARK state.

See timing diagram for generation of clock signal.

CONDITION A
No CO pulse TX ACTIVE goes high to generate clock.

CONDITION B
TX ACTIVE stays high. CO pulse generates clock.

Figure 4-38 Send Enable Flip-Flops and Associated Logic

For example, if a DLE character is to be transmitted, D8-5 DLE RQL goes low. This drives the output (pin 3) of E65 high. This signal is sent to input D0 of E71. When E71 is clocked, D5-6 DLE EN (1) L is asserted at output R0 (0). This signal is sent to the M7817 module (D8-5). The high signal from E65 pin 3 is sent to E56 pin 12 to block assertion of the other enable signals (BCC, SYNC and Data). This signal also drives E25 pin 6 low which, via E60 pin 6, puts a high on the D input of the TX ACTIVE (1) H which is sent to the 8-input OR gate on the M7812 module (D4-7). Enabling any type character (DLE, BCC, SYNC or Data) allows the TX ACTIVE flip-flop to be set.

The timing diagram in Figure 4-38 shows the two conditions that generate clock pulses for the SEND ENABLE flip-flops. At the start of transmission, when TX ACTIVE is set, signal D5-6 TX ACTIVE (1) H goes high which generates a positive-going transition at E10 pin 2 to clock E71. During transmission, TX ACTIVE remains set and additional clocking pulses are generated only by the CO positive pulse from TX SHIFT CNTR (E81) counter at overflow.

When the DQ11 is not actively transmitting, it is desired to keep the line to the data set in the MARK state (outside the DQ11, MARK = low = logical 1.) This is done by gating the four 1 outputs from the SEND ENABLE flip-flops, via E30 and E82, to one section of AND-OR-invert gate E52. All four 1 outputs are low which asserts D5-6 VRC/DATA SEL L at the output (pin 6) of E52. This signal is sent to the M7812 module (D4-5) and on via the DF11 to the data set.

The 1 outputs of the SYNC and Data sections of E71 are sent to the inputs of the SYNC/DATA ENABLE multiplexer (E76) which is described below.

SYNC/DATA ENABLE Multiplexer

The SYNC/DATA ENABLE multiplexer (E76) generates the enabling signals for the output multiplexers in the TX shift register (D4-5) and the SYN register (D4-6).

These signals are listed below:

Signal Name	Register/Byte
D5-6 TX SYNC EN 7–0 L	SYNC/low
D5-6 TX SYNC EN 15–8 L	SYNC/high
D5-6 TX DATA EN 7–0 L	TX/low
D5-6 TX DATA EN 15–8 L	TX/high

E76 is a quad 2-line-to-1-line multiplexer with common select (S0) and enable (STB) inputs. The STB input must be held low to enable the mux. With S0 low, the A inputs are selected; and with S0 high, the B inputs are selected. The outputs are the complements of the inputs. The 1 output from the SYNC section of the SEND ENABLE flip-flop (E71) is sent to inputs A3 and B2. The 1 output from the Data section of SEND ENABLE is sent to inputs B1 and A0.

All other inputs (B3, A2, A1 and B0) are permanently connected to ground.

Figure 4-39 shows the SYNC/DATA ENABLE mux and associated gating for the STB and S0 inputs. It also shows the character count logic which is not active during this discussion. Operation of the SYNC/DATA ENABLE mux is explained by showing two typical examples using sync characters only. Examples using data characters are described in the subsequent discussion of the character count logic because it is used in conjunction with the SYNC/DATA ENABLE Mux only when data is enabled.

Example 1 *(Sync character of 8 bits or less.)*
When a sync character of 8 bits or less is used, it must be loaded into both bytes of the SYNC register. As a result, only one byte of the SYNC register output mux has to be enabled. It happens to be the low byte mux (E32 SEND SYNC 7–0 on print D4-7).

1. For characters of 8 bits or less, the MSB output of TX BIT CNTR (E86) is always low. This signal (D5-6 TX BIT CNTR 8 (1) H) is inverted by E15 and sent to pins 10 and 11 of 3-input NAND gate E88. The third input (pin 9) comes from the 0 output of the CHAR CNT flip-flop. It is also high because CHAR CNT is cleared. This drives the output (pin 8) of E88 low. This signal is sent to the select (S0) input of the SYNC/DATA ENABLE multiplexer. The A input of the multiplexer is selected when this select input is low.

2. Because a sync character is to be transmitted, output R2 (1) of the SEND ENABLE flip-flop is high. This signal is sent to inputs A3 and B2 of E76.

3. The carry (CO) output of TX SHIFT CNTR (E81) is not active so it is held low. This signal goes to E61 pin 4 and drives the output (pin 6) of this gate high. This high is inverted by E95 to put a low on the STB input of E76 which enables it.

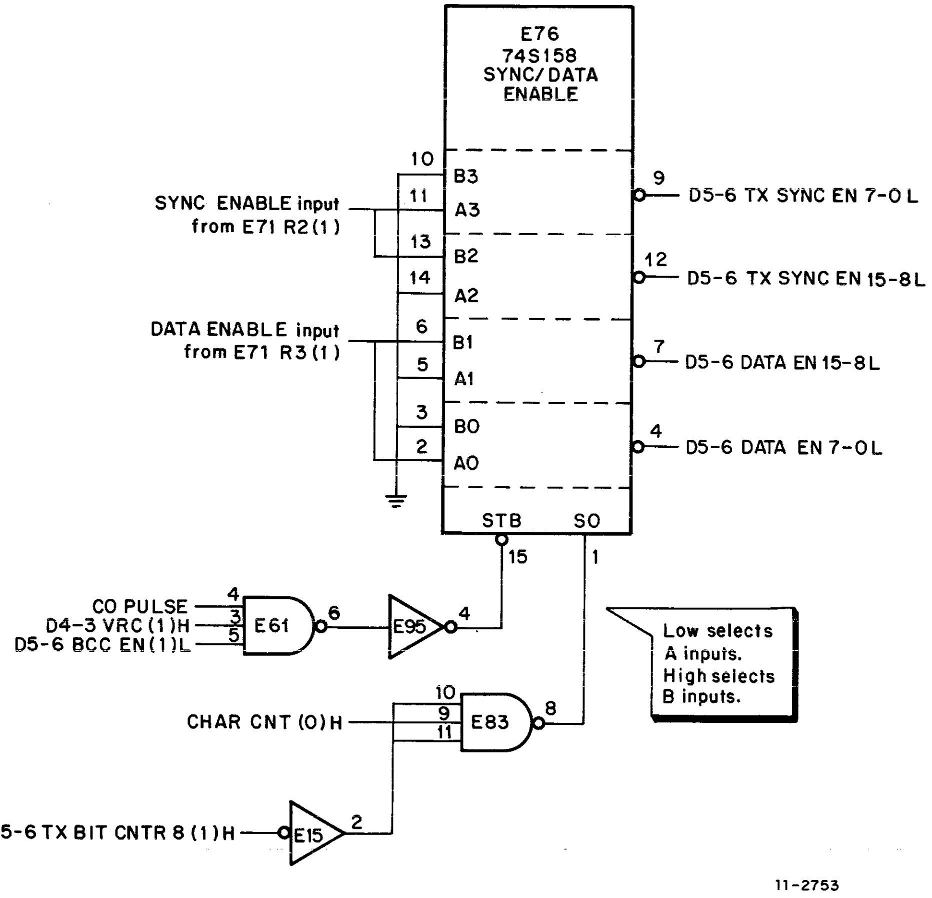


Figure 4-39 Sync/Data Enable Multiplexer and Associated Logic

4. The A inputs of E76 are transferred in complemented form to the four outputs (F3–F0). Disregarding the data enable signals (F1 and F0), the sync enable signals appear as follows.

   D5-6 TX SYNC EN 15–8 L is high at output F2 because input A2 is low (ground). This signal is not asserted.

   D5-6 TX SYNC EN 7–0 L is low at output F3 because input A3 is high. This signal is asserted. It is sent to SYNC register output multiplexer E32 (print D4-7) to enable the low byte.

5. As the counter is incremented, this byte is serialized and sent to the serial data out line.

Example 2 *(Sync characters of from 9 to 16 bits.)*
Characters of this length require both bytes of the SYNC register output multiplexer to be enabled. This example assumes 12-bit characters.

1. At the time of loading, the MSB output of TX BIT CNTR (E86) is low. This signal (D5-6 TX BIT CNTR 8 (1) H) selects the A input of the SYNC/DATA ENABLE multiplexer as described in step 1 of Example 1.

2. The SYNC/DATA ENABLE multiplexer is enabled as described in Example 1. Only signal D5-6 TX SYNC EN 7–0 L is asserted which enables SYNC register multiplexer E32 (print D4-7) which serializes the low byte of the sync character as the counter is incremented from count 0 through 7_{10}.

3. On the next count (8_{10}), the MSB output of TX BIT CNTR (E86) goes high. This drives E88 pin 8 high which selects the B input of the SYNC/DATA ENABLE multiplexer. This asserts D5-6 TX SYNC 15–8 L at output F2 of the mux because input B2 is high.

4. D5-6 TX SYNC 15–8 L enables SYNC register multiplexer E29 (print D4-7) and the serialization of the high byte starts. It stops at count 11_{10} (12th bit) when TX SHIFT CNTR (E81) overflows and puts itself and TX BIT CNTR (E86) in the load mode. The 12-bit sync character has been serialized and sent to the data out line.

Character Count Logic

The character count logic (Figure 4-40) is used to switch the SYNC/DATA ENABLE mux inputs to generate both low and high byte enabling signals for the TX data register output multiplexers when in the double-character mode (8 bits or less per character).

This logic is not used when TX data is being processed in the single-character mode (9 to 16 bits per character). When in this mode, the TX bit counter MSB input (D4-3 BITS 11 (1) H) is always low. This signal is sent to the clear input of the CHAR PENDING flip-flop and holds it in the clear state which inhibits the character count logic.

The character count logic is not required when processing sync characters in the double-character mode as described in Example 1 of the SYNC/DATA ENABLE Multiplexer discussion. It is rendered inactive by blocking the clock pulses for the CHAR PENDING flip-flop. When data is not enabled, output R3 (1) from the SEND ENABLE flip-flop is held low. This signal is sent to E66 pin 1 to prevent a clock pulse when the CO pulse from the counter is generated.

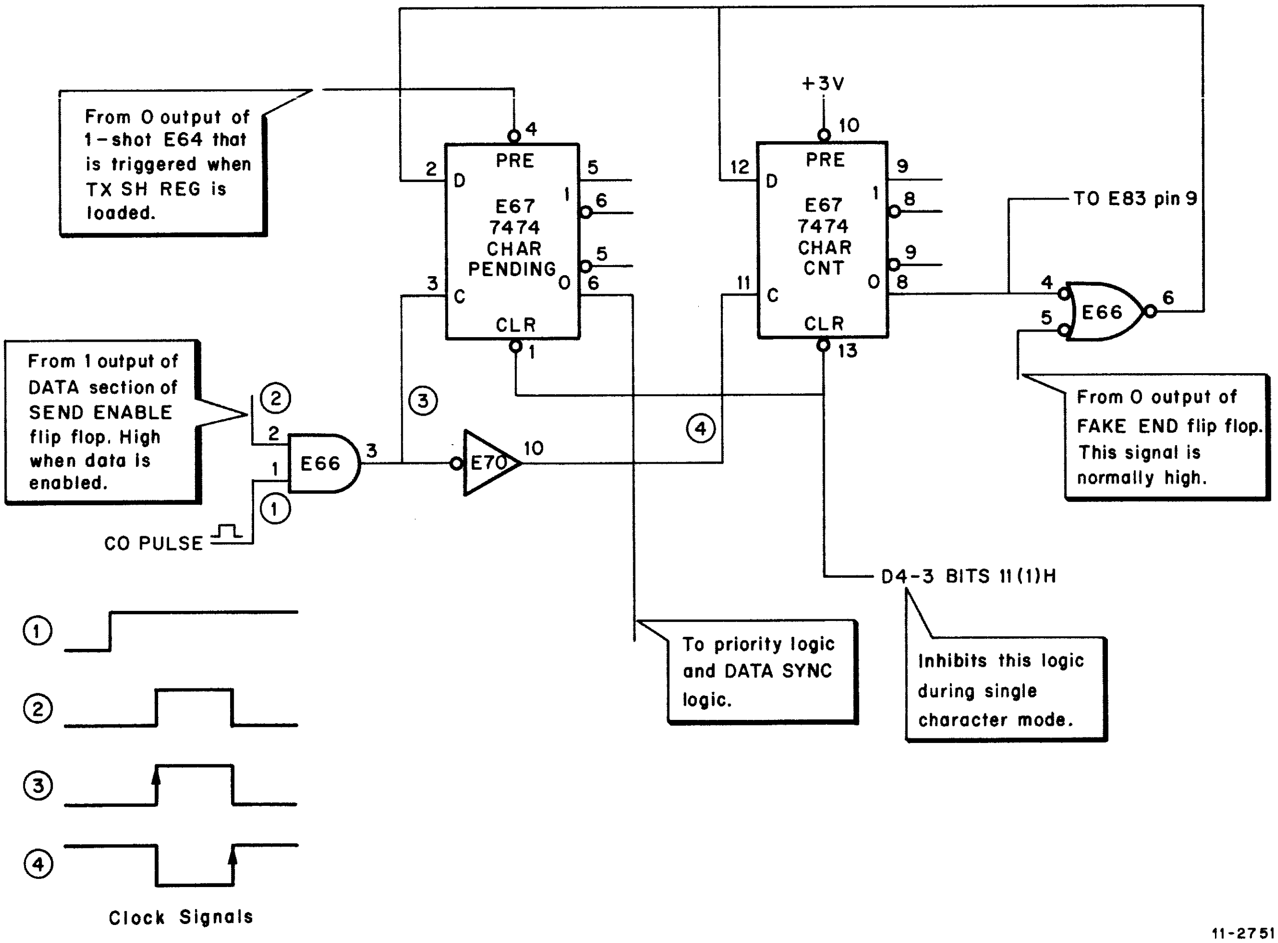

From 0 output of 1-shot E64 that is triggered when TX SH REG is loaded.
PRE
D
E67
7474
CHAR
PENDING
C
CLR
+3V
PRE
D
E67
7474
CHAR
CNT
C
CLR
TO E83 pin 9
E66
From 0 output of FAKE END flip flop. This signal is normally high.
From 1 output of DATA section of SEND ENABLE flip flop. High when data is enabled.
E66
E70
CO PULSE
D4-3 BITS 11(1)H
To priority logic and DATA SYNC logic.
Inhibits this logic during single character mode.
①
②
③
④
Clock Signals
11-2751

Figure 4-40 Character Count Logic

To describe the typical operation of the character count logic, assume that 8 bit data characters are being processed (double-character mode).

1. Initial conditions are as follows.

   a. CHAR PENDING flip-flop is directly set by one-shot E64 when TX shift register is loaded. CHAR CNT flip-flop is cleared. The D inputs of both flip-flops are high via E66 pin 6. This pin is high because both E66 inputs are high: pin 4 is high because CHAR CNT is cleared and pin 5 is high because the FAKE END flip-flop is cleared.

   b. TX SHIFT CNTR (E81) is loaded with 1000 (LSB to the left) to designate that 8 bits per character has been selected. TX BIT CNTR input MSB is high which inhibits the clear inputs of the CHAR PENDING and CHAR CNT flip-flops.

2. Under the initial conditions, all three inputs (pins 9, 10 and 11) of E88 are high which drives its output (pin 8) low. This signal puts a low on the select (S0) input of the SYNC/DATA ENABLE mux (E76).

3. The carry out pulse (CO) output of TX SHIFT CNTR (E81) is low which enables E76 via gates E61 and E95. Data is enabled so the R3 (1) output from the SEND ENABLE flip-flop puts a high on inputs B1 and A0 of the SYNC/DATA ENABLE mux.

4. With the mux enabled and its S0 input low, the A input is selected. This asserts D5-6 TX DATA EN 7–0 L which is sent to the TX shift register output mux E21 (print D4-5) to enable the low byte of the register. This 8-bit character is serialized as the counter increments toward overflow.

5. At overflow, TX SHIFT CNTR (E81) generates a positive pulse at the CO output. This pulse is sent to E66 pin 2 and drives the output (pin 3) high. (The other input (pin 1) is high because data is enabled.) The positive-going transition at E66 pin 3 clocks the CHAR PENDING flip-flop which has no effect because it is already set.

6. The output of E66 pin 3 that clocks CHAR PENDING is in the form of a positive pulse because it is controlled by the CO pulse from TX SHIFT CNTR. The output of E66 is inverted by E70 and sent to the clock input of the CHAR CNT flip-flop. When the positive CO pulse times out, a positive-going transition is generated at E70 pin 10 which clocks CHAR CNT and sets it.

7. When CHAR CNT is clocked it is set. Its 0 output goes to E88 pin 9 and drives the output (pin 8) of this gate high.

8. The high from E88 pin 8 is the select signal for the SYNC/DATA ENABLE mux which now switches from the A input to the B input. This asserts D5-6 TX DATA EN 15–8 L which is sent to the TX shift register output mux (E20) to enable the high byte of the register. This 8-bit character is serialized as the counter increments toward overflow.

9. The 0 output of CHAR CNT, via E66 pin 6, puts a low on the D input of CHAR PENDING and CHAR CNT. When the overflow occurs after serializing the high byte, the CO pulse leading edge clocks CHAR PENDING which clears it. When the CO pulse times out, its trailing edge clocks CHAR CNT which clears it also.

The character count logic is now in its original state. Both 8-bit characters have been serialized.

Save Sync Logic

When the DQ11 is not transmitting (TX GO cleared), idle characters can be selected for transmission. In the non-transparent mode, the idle character is the contents of the sync register. In the transparent mode, the idle character is Data Link Escape (DLE) followed by the contents of the sync register; that is, DLE-SYNC, DLE-SYNC, etc.

The save sync logic controls the enabling of sync and DLE characters during the idle mode. This logic consists of the SAVE SYNC flip-flop and some gating (E70 and E61) to its D input. The logic is located at the left center of print D5-6.

Assume that idle characters are to be transmitted in the non-transparent mode. SAVE SYNC starts in the set state which is accomplished by D5-6 INI L to its preset input (pin 4). D8-5 TX TRANS (1) L is high and is inverted by E70 to put a low on E61 pin 2. This holds the output of E61 (pin 12) high which is sent to the D input of SAVE SYNC. With this flip-flop in the set state and with its D input held high, it cannot change state when it is clocked by the CO pulse from TX SHIFT CNTR (E81).

With the total transparent mode inhibited and idle mode active, the output (pin 8) of E65 is low. This puts a low on E56 pin 6. The other input (pin 5) of E56 is also low because the CHAR PENDING and DATA RDY flip-flops are cleared. The resulting high from E56 pin 4 drives the output (pin 1) of the next E56 gate low. This low is sent to pin 11 of the third E56 gate in the priority logic. The other input (pin 12) of this gate is also low because a DLE character is not being requested. The output (pin 13) of the third E56 gate is high and is sent to the D input (E71 pin 12) of the sync section of the SEND ENABLE flip-flop. This sets up the SYNC/DATA ENABLE mux to generate the enabling signal for the sync register.

Assume now that idle characters are to be transmitted in the transparent text mode; that is, DLE-SYNC, DLE-SYNC, etc. SAVE SYNC starts in the set state but its D input is low via E61 pin 12. When the transparent text mode is selected, D8-5 TX TRANS (1) L is asserted, inverted by E70, and makes the third input (pin 2) of NAND gate E61 high which drives its output low. This low signal is also sent to E65 pin 2 which drives its output high regardless of the state of the other input. This high signal goes to the D input (E71 pin 4) of the DLE section of the SEND ENABLE flip-flop. This results in assertion of the DLE enabling signal. Thus, the signal from E61 pin 12 allows the enabling of a DLE character without a DLE request being asserted.

The DLE character is counted up and overflow occurs. The CO pulse from TX SHIFT CNTR (E81) clocks SAVE SYNC which clears it. The low from the 1 output of SAVE SYNC is fed back to E61 which drives its output (pin 12) high. This high goes to E65 pin 2 and drives the output (pin 3) of this gate low. This signal inhibits the enabling of DLE. It also goes to E56 pin 12 which drives its output (pin 13) high to allow enabling of the sync character.

At the end of the sync character, the CO pulse clocks SAVE SYNC which sets it and allows another DLE character to be enabled. Hence, the DLE-SYNC cycle is repeated.

Vertical Redundancy Check (VRC) Logic

When selected, the VRC logic examines the data to be transmitted and puts a MARK (logical 1) in the most significant bit of each character if required to make the total number of MARKs, including the VRC bit, even or odd as selected.

Before discussing the VRC logic, the following prerequisite information is presented.

1. Total data character length, with VRC activated, includes a VRC bit in the most significant place. The maximum length of a single character is 16 bits but only 15 bits contain data. The data bits/character should be selected as 15 with the VRC logic adding the last bit. For double characters, the data bits/character should be selected as 7.

2. MARK and SPACE are the terms used to identify the binary states of a communications line. Because of the signal inversion performed by the DF11 converters that interface the line with the DQ11, MARK and SPACE are defined as follows.

   Outside the DQ11. After passing through the DF11 (transmit mode) or prior to entering the DF11 (receive mode), the definition is:

   SPACE = HIGH = LOGICAL 0
   MARK = LOW = LOGICAL 1

   Inside the DQ11. Prior to entering the DF11 (transmit mode) and after passing through the DF11 (receive mode), the definition is:

   SPACE = HIGH = LOGICAL 1
   MARK = LOW = LOGICAL 0

   Internally, reference points for transmit and receive data are as follows.

   TRANSMIT DATA – Signal D4-7 SERIAL DATA OUT L (Prints D4-7 and D1-1)

   RECEIVE DATA – Signal D1-1 RECEIVE DATA L (Prints D1-1 and D4-3)

3. If even parity is selected, the VRC logic counts MARKs in the character and puts a MARK in the MSB position only if an odd number of MARKs is detected. With even parity, the total number of MARKs, including the VRC bit, is always even. Similarly, with odd parity, the total number of MARKs, including the VRC bit, is always odd.

To describe the operation of the VRC logic, assume the following conditions.

1. Even VRC is selected.
2. An 8-bit character is to be transmitted and that three MARKs appear in the 7 data bits of this character.

Under these conditions, the VRC logic should detect the odd number of MARKs and put a MARK in the 8th bit position.

Figure 4-41 shows the VRC logic and graphical representation of the data character used in the example.

The transmitter data to be examined is D4-7 TX DATA H. It is inverted by E74 and is sent to pin 2 of exlcusive-OR gate E84. At this point, the data is equivalent to D4-7 SERIAL DATA OUT L which is sent to the DF11. The other input (pin 1) of E84 is connected to the 0 output of the ONES CNT flip-flop. The output of E84 goes to the D input of this flip-flop.

As an aid to understanding the operation of the ONES CNT flip-flop, Figure 4-42 shows the truth table for the X-OR gate and a chart that shows the conditions necessary to change the state of the flip-flop. ONES CNT is clocked by D4-3 TX CLOCK H which is the transmit clock signal. Input gating to the clear input (pin 1) of ONES CNT allows it to be cleared by the CO pulse when the counter overflows. If TX ACTIVE is not asserted, ONES CNT is cleared and held in that state.

The sample data character (Figure 4-41) is sent to the VRC logic via signal D4-7 TX DATA H. As indicated, the 1 output of the ONES CNT flip-flop is low during the 7th (last) data bit. This signal is sent to pin 5 of X-OR gate E84. The other input of this gate (pin 4) is low because even parity is selected (SW4 is ON). The output (pin 6) of E84 is low and is sent to the D input of the VRC HOLD flip-flop. The TX bit counter overflows at the 7th data bit and the CO pulse clocks VRC HOLD which clears it. The low signal from the 1 output of VRC HOLD goes to input pin 4 of AND-OR-invert gate E52. The output of E52 goes high because its other input is held low. This output signal is D5-6 VRC/DATA SEL L and it is sent to pin 5 of E23 on the M7812 module (print D4-7). E23 is an 8-input NAND gate (shown as the logically-equivalent, negated-input OR gate). The last (7th) data bit has been sent and BCC is not selected so all 8 inputs are high which drives the output low. This low is inverted by E67 (print D4-7) to put a high (SPACE) in the 8th bit of the transmitted character. At this point (E67 pin 10) the signal is D4-7 SERIAL DATA OUT L. This is the transmit serial data signal line that goes to the DF11.

The VRC logic detected four MARKs in the 7-bit data character and put a SPACE in the 8th bit because even parity is selected.

Fake End Logic

In the double-character mode with an odd count detected, only the low byte of the last character contains a character to be transmitted. Under these conditions, it is desired to end the transmission and not waste time with the empty byte. This permits the next NPR to be started sooner and allows the TX BCC logic, if selected, to append the BCC character in the correct place.

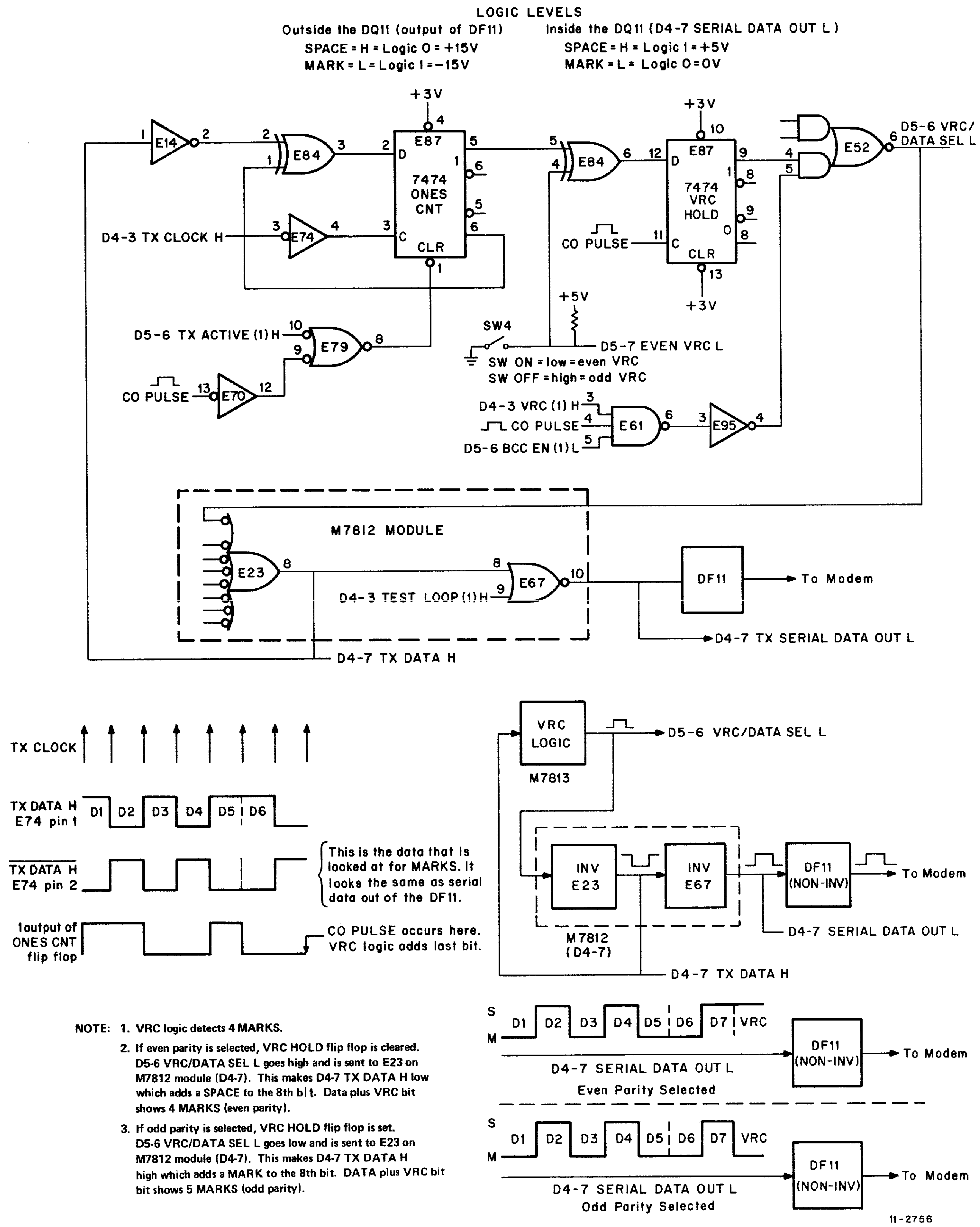
The fake end logic consists of the SAVE ODD CC and FAKE END flip-flops and NAND gate E65.

When the transmit control logic requests an NPR, the TX/RX CYCLE flip-flop in the NPR control logic is set and asserts D5-3 TX CYCLE H which is sent to E65 pin 4. During updating of the CC register, the CC ODD flip-flop is set if an odd count is detected. This asserts D5-1 CC ODD (1) H which is sent to the other input (pin 5) of E65. This drives the output of E65 low which sets SAVE ODD CC via its present input (pin 4).

The 1 output of SAVE ODD CC puts a high on the D input of FAKE END. In the process of starting the next NPR, the DATA SYNC flip-flop is cleared. The positive-going transition from its 0 output clocks both FAKE END and SAVE ODD CC.

FAKE END is set and its 1 output, which is designated D5-6 TX FAKE END (1) H, is sent to module M7816 to get the BCC logic started sooner. The 0 output of FAKE END is sent to E66 pin 5 to put a low on the D input of the CHAR PENDING flip-flop to inhibit the character count logic because there is no need to enable the high byte.

SAVE CC ODD is cleared when it is clocked. This inhibits the logic until a subsequent odd count presets SAVE CC ODD.

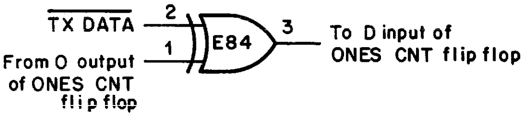


This is the data that is looked at for MARKS. It looks the same as serial data out of the DF11.

CO PULSE occurs here. VRC logic adds last bit.

NOTE:
1. VRC logic detects 4 MARKS.
2. If even parity is selected, VRC HOLD flip flop is cleared. D5-6 VRC/DATA SEL L goes high and is sent to E23 on M7812 module (D4-7). This makes D4-7 TX DATA H low which adds a SPACE to the 8th bit. Data plus VRC bit shows 4 MARKS (even parity).
3. If odd parity is selected, VRC HOLD flip flop is set. D5-6 VRC/DATA SEL L goes low and is sent to E23 on M7812 module (D4-7). This makes D4-7 TX DATA H high which adds a MARK to the 8th bit. DATA plus VRC bit shows 5 MARKS (odd parity).

Figure 4-41 Transmit VRC Logic and Sample Data Character


$\overline{\text{TX DATA}}$
2
1
E84
3
From 0 output of ONES CNT flip flop
To D input of ONES CNT flip flop

X-OR Gate

X-OR Truth Table

1	2	3
L	L	L
L	H	H
H	L	H
H	H	L

State Table for ONES CNT flip flop

	ONES CNT flip flop		
$\overline{\text{TX DATA}}$	Present State	D Input	State After Clock
low	cleared	high	set
high	cleared	low	no change
low	set	low	cleared
high	set	high	no change

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Figure 4-42 X-OR Truth Table and State Chart

Data Sync/NPR Logic

The data sync/NPR logic is shown in Figure 4-43. Although both sections of this logic are interrelated, they can be discussed separately in sequence.

The data sync section consists of the DATA SYNC and DATA RDY flip-flops and associated gating.

The discussion begins at the start of a transmit operation with the following conditions.

1. DATA SYNC is in the set state. This was accomplished by D5-3 TX NPR DONE H at the end of the previous NPR cycle.
2. DATA RDY is in the cleared state.
3. The TX shift register is empty.

Certain conditions relating to a TX NPR request are sensed by signals that are sent to NAND gate E45. This gate and E79 provide a delay in setting up the DATA RDY flip-flop to ensure that a transmit NPR is in progress. The CC/BA register is in the BA mode (D5-3 CC/BA CYCLE H is not asserted); D5-3 TX CYCLE H is asserted by the NPR control logic; and D5-6 TX ACTIVE (0) H is asserted because the TX ACTIVE flip-flop is cleared. The resulting high from E45 pin 12 is ANDed with the high from the 1 output of DATA SYNC at AND gate E79. This puts a high on the D input of DATA RDY. The next positive transition of the inverted TX clock signal from E74 pin 4 clocks DATA RDY and sets it. The 0 output of DATA RDY sets up the TX ACTIVE flip-flop and the data section of the SEND ENABLE flip-flop to allow the next positive transition of D4-3 TX CLOCK H to set TX ACTIVE which in turn allows data to be enabled.

Return in time to the point at which the DATA RDY flip-flop is clocked by the positive transition of the inverted TX clock signal from E74 pin 4. This signal puts a high on pin 10 of E60. Pin 12 is high because CHAR PENDING is cleared; and now pin 9 is high because DATA RDY is set. With all four inputs high, the output (pin 8) of E60 goes low. When the inverted TX clock signal goes low again, E60 pin 8 goes high. This positive edge is D5-6 LD TX SH REG H which clocks the data from the transmit buffer into the shift holding register (E22, E11 and E19 on print D4-5). This edge also clocks the DATA SYNC flip-flop which clears it. It also triggers one-shot E64 which generates a negative pulse that directly sets the CHAR PENDING flip-flop. The 1 output of DATA SYNC, which is low, drives the D input of DATA RDY low via E79 pin 6. When the inverted TX clock signal goes high again, this positive transition clocks DATA RDY which clears it.

When DATA SYNC is cleared, its 0 output goes high. This positive-going transition clocks NPR RQ and TX LATE simultaneously. Both of these flip-flops start in the cleared state. The D input of TX LATE is low because NPR RQ is cleared and the D input of NPR RQ is high because D4-4 TX GO (1) H is asserted. Therefore, NPR RQ is set which asserts D5-6 TX NPR RQ (1) L. This signal goes to the NPR request logic (print D5-3). TX LATE is cleared which keeps D5-6 TX LATE L unasserted. If NPR RQ is still set when DATA SYNC gets cleared, TX LATE is set which asserts D5-6 TX LATE L. This action denotes that the previous NPR request was not serviced in less than one character time. D5-6 TX LATE L sets bit 2 (TX LATENCY) of the REG/ERR CSR which in turn generates an error interrupt flag and clears TX GO to stop further TX NPR requests.

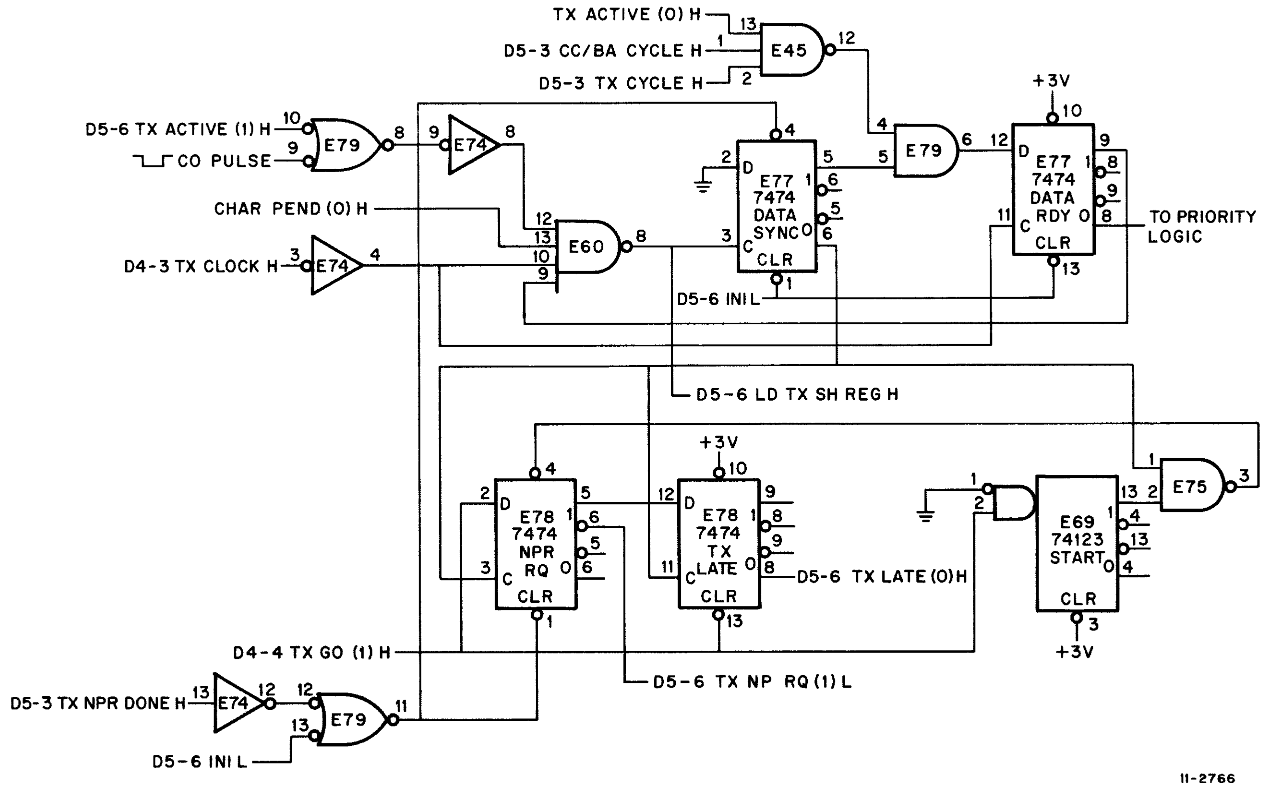


Figure 4-43 Data Sync/NPR Logic

The START one-shot is used to force the NPR request if D4-4 TX GO (1) H is asserted when DATA SYNC is cleared. In this situation, D4-4 TX GO (1) H going high, triggers one-shot START. The 50 ns positive pulse from the 1 output of START is ANDed with the high from the 0 output of DATA SYNC at E75. The resulting low from the output (pin 3) of E75 sets NPR RQ directly via its preset input (pin 4).

4.5.7 Receive Start Up and VRC Logic

4.5.7.1 Functional Description – In the receive mode, the start up logic searches for sync characters and when the proper pattern is detected, it asserts the RX ACTIVE signal which indicates that the receiver is in the data transfer mode. It also generates the load signals for the RX buffer register. Provisions are included to clear the receive start up logic from three sources: program control of RX ACTIVE, loss of RX GO, or via the sequence control logic on the M7817 module.

The VRC logic, when enabled, checks the received character for correct parity. If incorrect parity is detected, a signal is generated that sets the RX VRC error flag (bit 7 of the REG/ERR CSR).

Three switches are used in this logic.

Switch	Description
SW1	Set to ON for two sync characters to frame.
	Set to OFF for one sync character to frame.
SW2	Set to ON to assert RX ACTIVE on first non-sync character after framing.
	Set to OFF to assert RX ACTIVE when framing occurs.
SW4	Set to ON for even VRC or OFF for odd VRC.

4.5.7.2 Detailed Logic Description – The circuit schematics for the receive start up logic and VRC logic are contained in drawing D-CS-M7813-0-1 (Rev H) sheet 9 which is designated D5-7.

Receive Start Up Logic

The receive start up logic is discussed by setting up specific sync detection and framing requirements and following the sequence of operations.

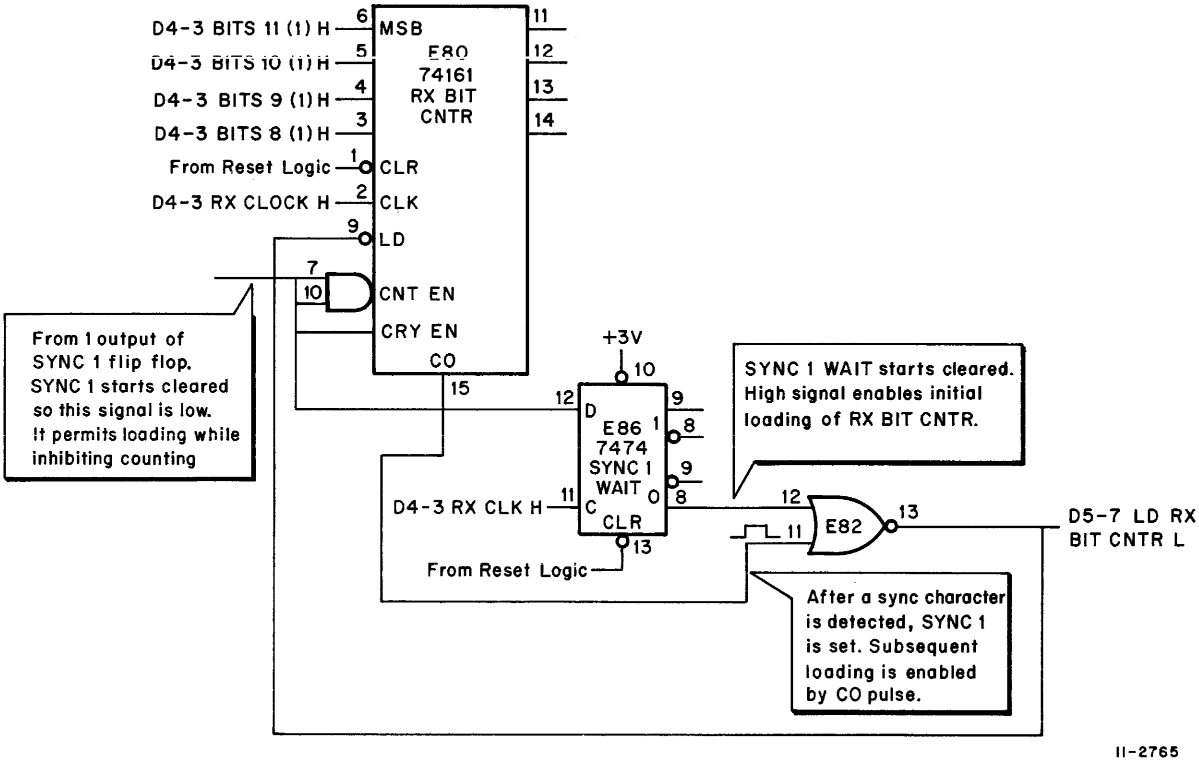
Before discussing the specific example, it is advisable to describe the operation of the RX bit counter which is an integral part of the logic.

The RX BIT CNTR (E80) is a 74161 synchronous 4-bit counter (Figure 4-44). The four inputs (pins 3–6) come from MISC register bits 8–11 which select the number of bits per character. The outputs are not used. The counter is used only to detect the end of the frame which occurs when the counter overflows and generates the carry out (CO) pulse. The counter can be cleared by D5-4 INI H or by the reset logic. In either case, the clear signal comes from E82 pin 1.

The load signal for the counter is D5-7 LD RX BIT CNTR L. When it is low, the counting function is disabled and the outputs are forced to agree with the inputs after the next clock pulse. The clock signal is D4-3 RX CLOCK H and clocks the counter on the positive-going transition. The count enable (CNT EN) and carry enable (CRY EN) inputs are connected to the 1 output of the SYNC 1 flip-flop. Both these signals must be high to permit the counting function. If they are low, counting is inhibited but the load function can still be performed.

At the start of the sync detect operation, the SYNC 1 flip-flop is cleared which inhibits counting by putting a low on the counter CNT EN and CRY EN inputs. The SYNC 1 WAIT flip-flop starts in the cleared state. The high signal from its 0 output asserts D5-7 LD RX BIT CNTR L at E82 pin 13. This is the load signal for the counter and the selected number of bits per character is loaded into the counter because the clock (D4-3 RX CLOCK H) is running. As the sync detect operation progresses, the SYNC 1 flip-flop is set and counter inputs CNT EN and CRY EN go high which allows RX BIT CNTR to count up. Subsequently, the SYNC 1 WAIT flip-flop is set which puts a low on pin 12 of E82. Now the counter load signal can be generated only when the counter overflows and sends the positive CO pulse to E82 pin 11.

The discussion now explains the operation of the start up logic for a specific situation. Assume that SW1 is ON which requires that two sync characters be detected to ensure framing and the DQ11 is operating in the single-character mode with an even number of characters in the message.



From 1 output of SYNC 1 flip flop. SYNC 1 starts cleared so this signal is low. It permits loading while inhibiting counting

SYNC 1 WAIT starts cleared. High signal enables initial loading of RX BIT CNTR.

After a sync character is detected, SYNC 1 is set. Subsequent loading is enabled by CO pulse.

Figure 4-44 RX Bit Counter and Associated Logic

Assume that SW2 is ON which allows RX ACTIVE to be set on the first non-sync character after framing (Figure 4-45).

1. The starting conditions are as follows:

   a. D4-4 RX GO (1) H is asserted.

   b. A sync character has not been detected yet. D4-7 RX SYNC DET H is low. This puts a low on the D input of both SYNC 1 and SYNC 2.

   c. SYNC 1 and SYNC 2 are both cleared. The feedback from the 0 outputs of SYNC 1 and SYNC 2 and one-shot CNTL PULSE conditions the clock steering gates (three E85s) to allow the receiver clock signal (D4-3 RX CLOCK H) to reach SYNC 1 and SYNC 2.

   d. SYNC 1 WAIT is cleared. This allows assertion of D5-7 LD RX BIT CNTR L at E82 pin 13. The counter is loaded but it cannot count because the CNT EN and CRY EN inputs are held low via the 1 output of SYNC 1.

2. The first sync character is shifted into the RX shift register and then into the RX buffer at which point it is detected so D4-7 RX SYNC DET H is asserted. E96 pin 11 goes high and is sent to the D input of SYNC 1. The low signal from the 1 output of SYNC 1 (which is cleared) goes through SW1 to keep a low on the D input of SYNC 2.

3. The next negative-going transition of D4-3 RX CLOCK H is inverted three times by the clock steering gates and appears as a positive-going transition at E85 pin 8. This transition clocks SYNC 1 which sets it. SYNC 2 remains cleared.

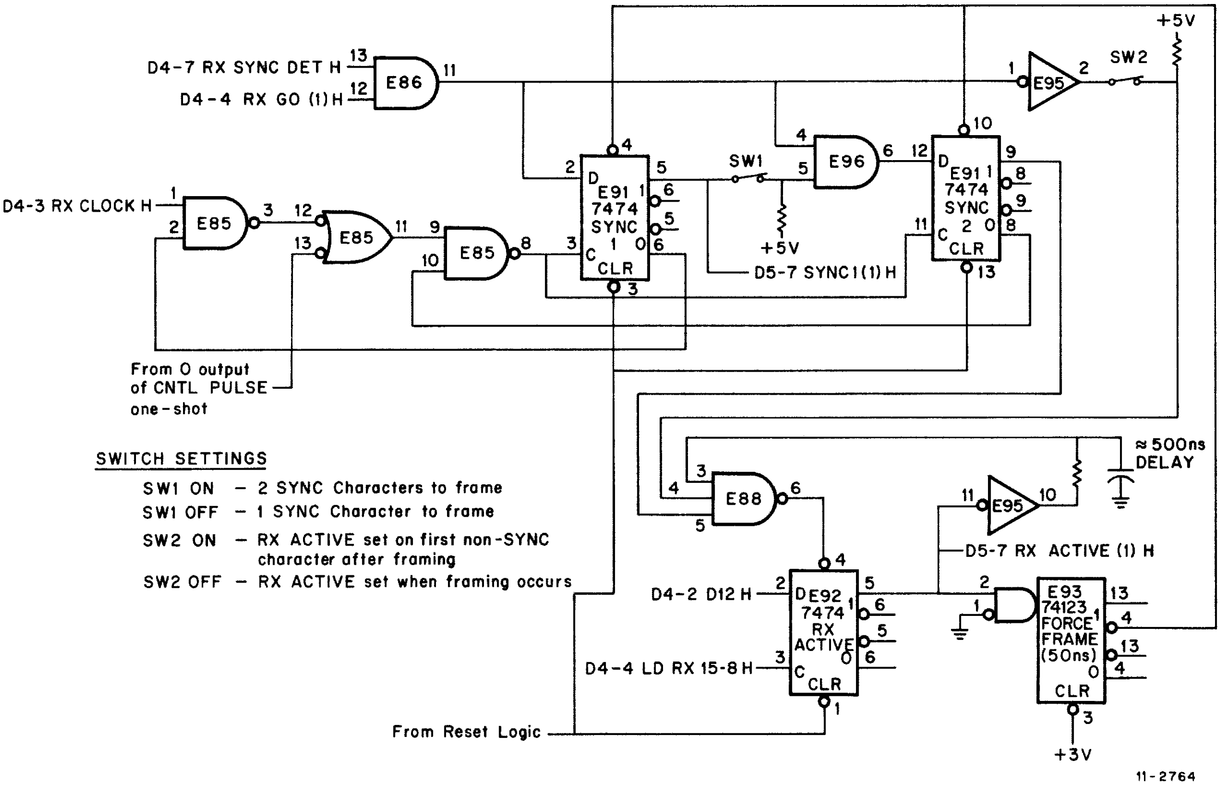


Figure 4-45 Receiver Start Up Logic

4. When SYNC 1 sets, the low signal from its 0 output is fed back to E85 pin 2. This drives the output (pin 3) of E85 high and blocks the clocking signal for SYNC 1 and SYNC 2. The high signal from the 1 output of SYNC 1 is sent to the D input of SYNC 2 via SW1 and E96 pin 6.

5. The 1 output of SYNC 1 drives the CNT EN and CRY EN inputs of the counter high. Normally, this would enable the counter and allow it to start counting; however, the load (LD) input is still low. This inhibits the counting operation even when CNT EN and CRY EN are enabled.

6. The 1 output of SYNC 1 also puts a high on the D input of SYNC 1 WAIT. The next positive-going transition of D4-3 RX CLOCK H sets SYNC 1 WAIT. The 0 output of SYNC 1 WAIT puts a low on E82 pin 12. The other input (pin 11) is low because the CO pulse is not enabled. This drives the output (pin 13) of E82 high which inhibits the counter load signal (D5-7 LD RX BIT CNTR L is high). The next positive-going transition of D4-3 RX CLOCK H increments the counter which starts the count up sequence. SYNC 1 WAIT forced a one clock pulse time delay in allowing RX BIT CNTR to count after SYNC 1 was set.

7. Nothing happens in this logic while the second sync character is shifted into the RX shift register until the last bit is counted. At the last bit, RX BIT CNTR overflows and generates the positive carry out (CO) pulse. This generates another load pulse (D5-7 LD RX BIT CNTR L) for the counter.

8. The positive-leading edge of the CO pulse triggers one-shot LD BUF which generates complementary 100 ns pulses. The positive pulse goes to E82 pin 5 which asserts D5-7 LD RX BUF 15–8 L at the output of this gate. This is the load signal for the high byte of the RX buffer register (D4-5). This signal is sent to the RX character control logic (print D5-8) where it is used to assert D5-8 LD RX BUF 7–0 L which is the load signal for the low byte of the RX buffer register. The second sync character has been loaded into the RX buffer register and is detected at this point.

9. When the negative pulse from the LD BUF one-shot times out, its positive-going trailing edge triggers one-shot CNTL PULSE which generates complementary 50 ns pulses. When the negative pulse from the CNTL PULSE one-shot times out it drives E85 pin 8 high (Figure 4-44). This positive-going transition clocks SYNC 2 and sets it.

10. When SYNC 2 sets, the low signal from its 0 output is fed back to E85 pin 10 to block further clocking of SYNC 1 and SYNC 2. The 1 output of SYNC 2 puts a high on pin 5 of 3-input NAND gate E88. Pin 3 of this gate is high because the RX ACTIVE flip-flop is cleared. The third input (pin 4) of E88 is low because of the inverted output (pin 11) of E96. The second sync character has been detected so this point (E96 pin 11) remains high.

11. When the first data character is shifted in, D4-7 RX SYNC DET H goes low because this character is a non-sync character. Pin 4 of E88 now goes high which drives the output (pin 6) of this gate low. This signal directly sets the RX ACTIVE flip-flop via its preset input (pin 4). The 1 output of RX ACTIVE (D5-7 RX ACTIVE (1) H) is inverted by E95, delayed 500 ns by RC network R44–C115 and drives the output (pin 6) of E88 high which inhibits the preset input of the RX ACTIVE flip-flop.

12. At the last bit of the second sync character, RX BIT CNTR overflows and generates the CO pulse which in turn generates another load pulse for the counter. The second sync character is loaded into the RX buffer register as described in item 8.

The start up logic has accomplished its job; that is, it recognized two sync characters to frame the message and set RX ACTIVE on the first non-sync character following framing. SYNC 1, SYNC 2 and TX ACTIVE remain set until they are directly cleared by the reset logic.

Force Framing

The start up logic can be conditioned to be framed at the first received character. This can be accomplished through program control.

The RX ACTIVE flip-flop is bit 12 of the RX CSR. The program puts a high on the D input of RX ACTIVE using

D4-2 D12 H from a bus receiver. When the RX CSR is addressed, the register decoding logic asserts D4-4 LD RX 15–8 H which clocks RX ACTIVE and sets it. The 1 output of RX ACTIVE triggers one-shot FORCE FRAME. The negative 50 ns pulse from this one-shot directly sets SYNC 1 and SYNC 2 via their preset inputs. This synchronizes the hardware just as if sync characters were detected.

Resetting the Start Up Logic

Once the start up logic has performed its job, it is not returned automatically to its original state. The reset logic performs the task of clearing the start up logic. The reset action can be initiated from four outside sources:

1. Assertion of D5-4 INI H which is caused by a BUS INIT L signal or MASTER CLEAR (MISC register bit 5).
2. Clearing RX ACTIVE (RX CSR bit 12) by program control.
3. Clearing RX GO when character count goes to zero or if RX GO is inadvertently cleared during a receive operation.
4. Assertion of D5-8 CRA DLY L which is a function of the M7817 module.

The normal way of clearing the start up logic is by program control of the RX ACTIVE flip-flop. The program forces the RX ACTIVE flip-flop to the cleared state. When cleared, the 0 output of RX ACTIVE triggers the ACTIVE RESET one-shot. The 50 ns negative pulse from ACTIVE RESET drives E83 pin 6 high which in turn drives the output (pin 1) of E82 low. This low signal directly clears SYNC 1, SYNC 2, SYNC 1 WAIT, RX ACTIVE, and RX BIT CNTR.

When RX GO is cleared, D4-4 RX GO (1) H goes low and triggers the GO RESET one-shot. The negative pulse from GO RESET clears the start up logic the same way that ACTIVE RESET clears it.

The previous discussion assumed that switches SW1 and SW2 were both ON which required detection of two sync characters and allowed RX ACTIVE to be set on the first non-sync character register framing.

Assume that SW1 remains ON but SW2 is now OFF. This allows RX ACTIVE to be set when framing occurs; that is, right after the second sync character is detected. With SW2 OFF, pin 4 of E88 is high. When SYNC 2 is set, its 1 output drives the third input (pin 5) of E88 high. The output (pin 6) of this gate goes low and directly sets RX ACTIVE.

As another example, assume that SW1 is OFF which requires one sync character to frame. With SW1 off, pin 5 of E96 is high. When a sync character is detected, the other input (pin 4) of E96 goes high and puts a high on the D input of SYNC 2. The D input of SYNC 1 is also high. SYNC 1 and SYNC 2 are set simultaneously. The subsequent setting of RX ACTIVE depends on the state of SW2. Both conditions (SW2 ON and OFF) have been discussed previously.

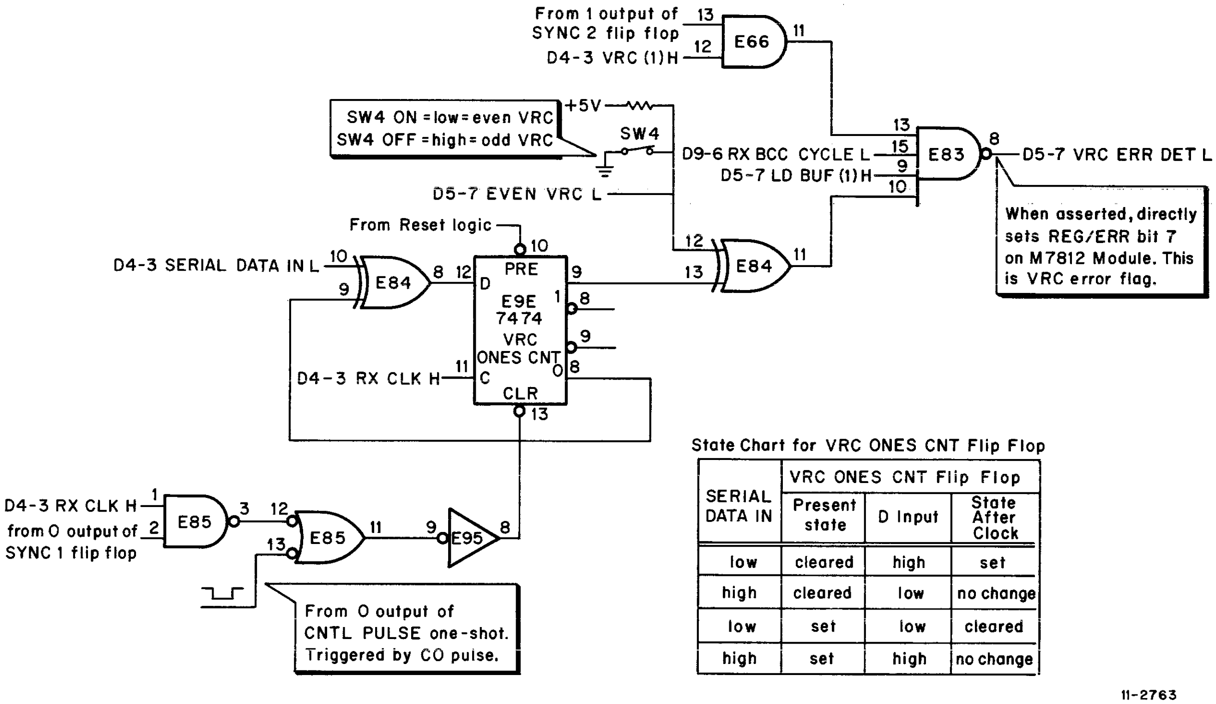
RX VRC Logic

The basic principles of operation of the RX VRC logic are the same as those described in the TX VRC logic discussion in Paragraph 4.5.6.2.

When selected, the RX VRC logic examines each received character to verify that the selected VRC (odd or even) has been correctly indicated at the source. The RX VRC logic is shown in Figure 4-46.

For example, assume that the remote location sends an 8-bit character with even parity and that it is received without error. The sample character is shown in Figure 4-47 and contains four MARKs including the VRC bit in the MSB position.

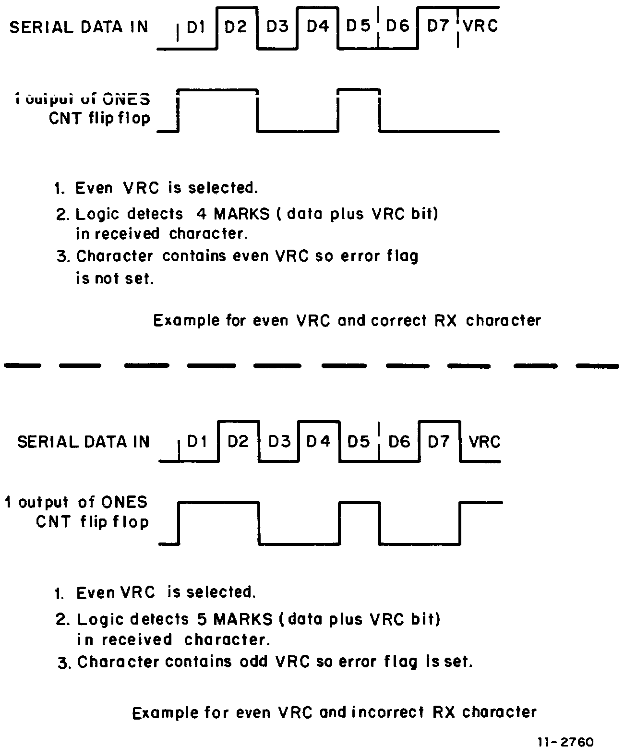
The VRC logic receives this character and it is set to detect even parity. This is accomplished by setting switch SW4 to the ON position which asserts D5-7 EVEN VRC L at X-OR gate E84 pin 12. Assuming that the start up logic has done its job, the SYNC 1 flip-flop is set and the clear input (pin 13) is high (inhibited). The VRC ONES CNT flip-flop changes state as it is clocked in accordance with the table in Figure 4-46. At the last character bit, VRC ONES CNT is cleared. Its 1 output, which is low, is sent to E84 pin 13. Because even parity is selected (SW4 is ON), the output (pin 11) of X-OR gate E84 is low. This drives the output of E83 high. This signal is D5-7 VRC ERR DET L and goes to the preset input of the flip-flop that represents the RX VRC ERR flag (bit 7) of the REG/ERR CSR. Being high, it does not activate the RX VRC error flag. The message has been received with the correct parity.



State Chart for VRC ONES CNT Flip Flop

SERIAL DATA IN	VRC ONES CNT Flip Flop		
	Present state	D Input	State After Clock
low	cleared	high	set
high	cleared	low	no change
low	set	low	cleared
high	set	high	no change

Figure 4-46 Receiver VRC Logic



1. Even VRC is selected.
2. Logic detects 4 MARKS (data plus VRC bit) in received character.
3. Character contains even VRC so error flag is not set.

Example for even VRC and correct RX character

1. Even VRC is selected.
2. Logic detects 5 MARKS (data plus VRC bit) in received character.
3. Character contains odd VRC so error flag is set.

Example for even VRC and incorrect RX character

Figure 4-47 Sample Message With Received Data Character and VRC

At the 8th bit, the counter overflows and the positive CO pulse is generated. It is double inverted by E85 and E95 and directly clears the VRC ONES CNT flip-flop so that it is ready to check the next received character.

Assume that the sample message in Figure 4-47 is received in error with odd parity. Specifically, assume that the parity bit is a SPACE. After looking at the whole character, VRC ONES CNT is set. The output of E84 pin 11, which goes to E83 pin 10, is high now. The other three inputs to this 4-input NAND are also high for the following reasons:

E83 pin 13 is high via AND gate E66 because VRC is activated and SYNC 1 is set.

E83 pin 12 is high because BCC is not active.

E83 pin 9 is high because LD BUF is triggered.

With all inputs high, the output of E83 goes low which asserts D5-7 VRC ERR DET L. This signal sets the VRC error flag to indicate that the received character has the incorrect parity.

4.5.8 Receive Character Control Logic

4.5.8.1 Functional Description – A simplified block diagram of the receive character control logic is shown in Figure 4-48. This logic counts a character as being received or not. It is conditioned to respond to single-character or double-character operation. Further discrimination is made between odd and even character counts.

When this logic determines that the received character is what was expected, an NPR request is generated, the character is sent to the receiver buffer and the receive character control logic is prepared for the next count.

Additional biasing circuits are used to block character transfers under certain conditions during character recognition, transparent text or total transparent modes.

4.5.8.2 Detailed Logic Description – The circuit schematic for the receive character control logic is contained in drawing D-CS-M7813-0-1 (Rev H) sheet 10 which is designated D5-8.

A specific example is used to describe the operation of the receive character control logic.

1. The initial conditions are as follows:
   a. The receive cycle is just starting. The SYNC 1 flip-flop is cleared (D5-7 SYNC 1 (1) H is low) which puts a high on E98 pin 4 (top gate) and E98 pin 9 (middle gate). The clear input (pin 13) of the SKIP LD NEXT FRAME flip-flop is also driven low which directly clears it.
   b. Single-character operation is selected. D4-3 BITS 11 (1) H is low which puts a low on E98 pin 5 (top gate) and a high on E98 pin 10 (middle gate).
   c. The output (pin 6) of the top E98 gate is high which inhibits the clear input (pin 1) of the XFER FRAME START flip-flop.

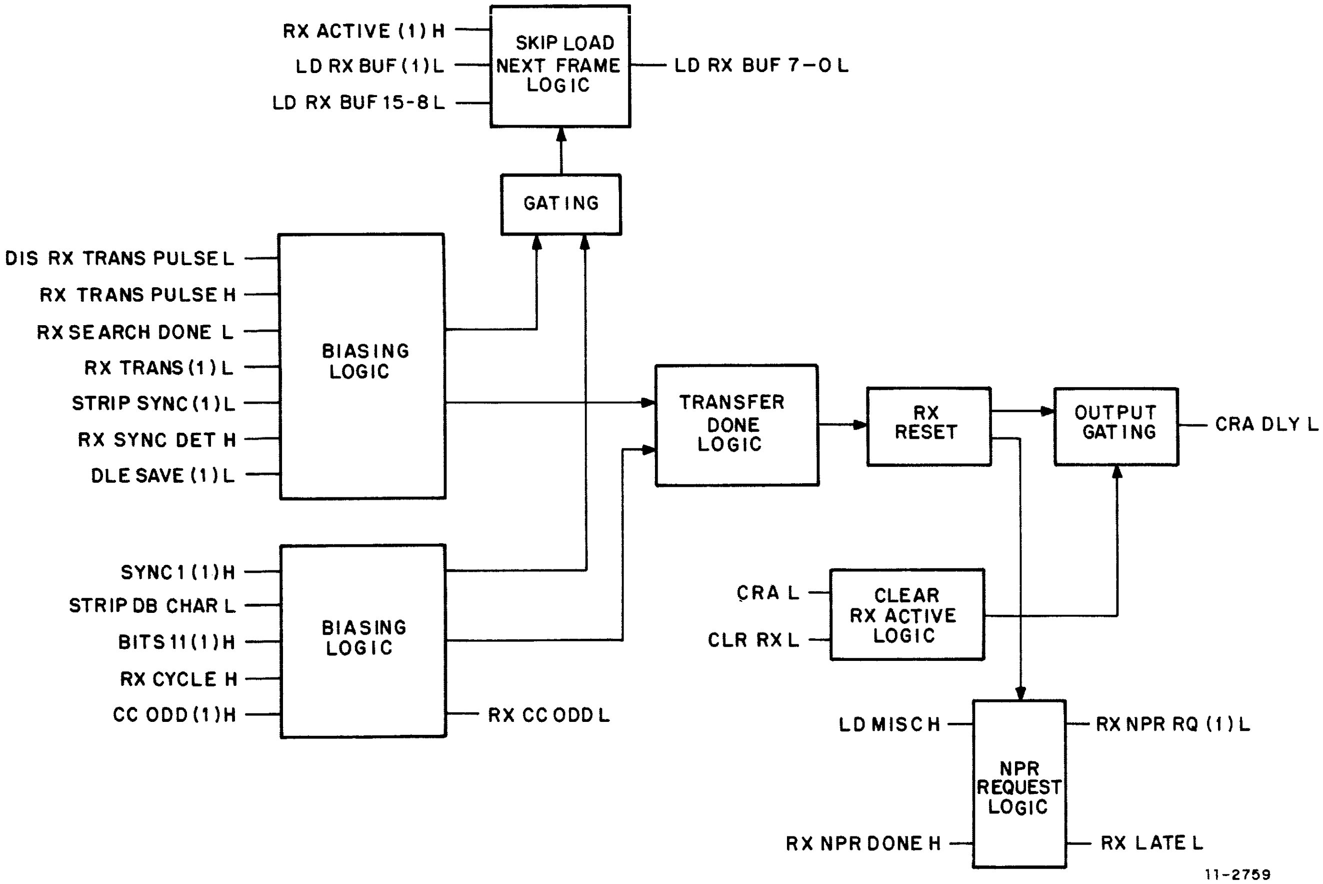


Figure 4-48 Block Diagram of Receive Character Control Logic

d. The output (pin 8) of the middle E98 gate is low which puts a low on the preset input (pin 4) of the XFER FRAME START flip-flop which directly sets the flip-flop.

e. No character recognition functions are enabled; therefore, the clock source for the XFER FRAME START and XFER FRAME DONE flip-flops comes from D5-7 RX TRANSFER PULSE H. XFER FRAME START is set and XFER FRAME DONE is cleared but its clear input (pin 13) is not active now.

2. Assume that a sync character is the first one received. The SYNC 1 flip-flop is set which inhibits the preset input of XFER FRAME START.

3. At the end of the character bit count, the RX start up logic (D5-7) generates D5-7 LD RX BUF 15–8 L which in turn generates D5-8 LD RX BUF 7–0 L because SKIP LD NEXT FRAME is cleared. These signals load the character in the RX buffer register (D4-6). The outputs of this register go to the inputs of the buffered RX data register (D4-7). Coincident with the assertion of D5-7 LD RX BUF 15–8 L, the 0 output of the LD BUF one-shot (D5-7 LD BUF (0) H), which is low for 100 ns, is sent to the clock input of SKIP LD NEXT FRAME. The positive-going trailing edge of this pulse sets SKIP LD NEXT FRAME. Normally, this flip-flop is cleared before the next character arrives. However, it can remain set if in double-character operation in the character recognition mode and a subsequent SYNC character is to be stripped. (This action is described later.)

4. Approximately 100 ns after D5-7 LD RX BUF 15–8 L is asserted, D5-7 RX TRANSFER PULSE H is asserted for approximately 50 ns. When this signal goes high, it generates a positive-going transition at E99 pin 6 that clocks XFER FRAME START and XFER FRAME DONE. The XFER FRAME DONE flip-flop is set when clocked and its 1 output triggers the RX RESET one-shot.

   The high at E99 pin 6 is inverted by E35 and directly clears SKIP LD NEXT FRAME which puts this flip-flop in the correct state for the next character.

5. The 50 ns pulse from the RX RESET one-shot directly sets the RX NPR RQ flip-flop via gate E38. When the flip-flop is set, it asserts D5-8 RX NPR RQ (1) L. This signal starts the NPR request sequence. It also generates D5-3 RX NPR L that clocks the buffered RX data register and puts the character on the Unibus data lines to be transferred to memory during the NPR cycle.

   The negative pulse from the RX RESET one-shot directly clears the XFER FRAME DONE flip-flop.

   Normally, the RX NPR RQ flip-flop starts in the cleared state. If it was still set when RX RESET is triggered, the leading edge of the positive pulse from RX RESET clocks the RX LATE flip-flop and sets it. This asserts D5-8 RX LATE L which denotes that the previous NPR request was not serviced in less than one character time. D5-8 RX LATE L sets bit 3 (RX LATENCY) of the REG/ERR CSR which in turn generates an error interrupt flag and clears RX GO which shuts off the receiver.

   The other input to AND-OR-invert gate E38 (pins 4 and 5) is bit 4 (RX NPR) of the MISC register. It is used during servicing, when RX ACTIVE is cleared, to force an RX NPR. In this mode, the data transferred to memory is the contents of the RX shift register rather than the contents of the buffer register. The BA/CC register is also updated.

   In the character recognition mode, certain conditions bias the logic to prevent an NPR request from being generated. The received character is not sent to memory; in effect, it is stripped from the message.

   If the receiver is not in the transparent mode (D8-6 RX TRANS (1) L is high) and the strip sync function is selected (D4-4 STRIP SYNC (1) H is high), sync characters are stripped from the message. This is accomplished by blocking the clock pulse to the XFER FRAME START and XFER FRAME DONE flip-flops. A low on E99 pin 5 via E90 pin 8 blocks the clock signal.

   During the DLE-SYNC, DLE-SYNC sequence in the transparent mode, the sync characters are also stripped using the same logic by asserting D4-6 RX SYNC DET H and D8-6 DLE SAVE (1) L.

A double character can be stripped (in character recognition mode) when the M7817 logic asserts D8-4 STRIP DB CHAR L. This signal, via gates E88 and E98, holds XFER FRAME START cleared to prevent generation of the NPR request signal.

SKIP LD NEXT FRAME Flip-Flop

In the non-character detect receive mode, the SKIP LD NEXT FRAME flip-flop starts cleared. Approximately 100 ns after D5-7 LD RX BUF 15–8 L and D5-7 LD RX BUF 7–0 L are asserted, SKIP LD NEXT FRAME is clocked by a pulse from the LD BUF one-shot which sets it. Shortly after being set, SKIP LD NEXT FRAME is directly cleared as a result of the D5-7 RX TRANSFER PULSE H signal. The SKIP LD NEXT FRAME flip-flop is now in the proper state for the next character.

In the character detect mode, the SKIP LD NEXT FRAME flip-flop can be held in the set state if the next received character is a sync to be stripped, provided double characters are being processed.

Assume that 8 bit double characters are being processed and that the character detection logic is conditioned to strip sync characters. The character sequence for this example is SYNC, Data 1, Data 2.

1. SKIP LD NEXT FRAME starts cleared. Both XFER FRAME START and XFER FRAME DONE start cleared. This is the situation for double characters and requires two clock pulses to get the XFER flip-flops set so that an NPR request can be generated.

2. When the SYNC character is detected, D4-7 RX SYNC DET H is asserted. D4-4 STRIP SYNC (1) H is also asserted by the program. This blocks the clock signal for the XFER flip-flop which normally occurs when the character is shifted in.

3. When the SYNC character is shifted in, the RX bit counter overflows. The RX buffer load signals (D5-7 LD RX BUF 15–8 L and 7–0 L) are asserted, SKIP LD NEXT FRAME is set, but D5-7 RX TRANSFER PULSE H does not cause SKIP LD NEXT FRAME to be cleared. The SYNC character is loaded into the high byte of the RX buffer and the previous contents of the RX shift register are loaded into the RX buffer low byte. The XFER flip-flops have not changed state because the clock signal is blocked (step 2).

4. When character Data 1 appears, the clock inhibiting action caused by the sync strip function is removed. When Data 1 is shifted in, only the high byte RX buffer load signal is asserted and D5-7 RX TRANSFER PULSE H clears SKIP LD NEXT FRAME. The XFER FRAME START flip-flop is set. Data 1 is loaded in the RX buffer high byte, which obliterates the SYNC character that was there. The SYNC character resides in the RX shift register low byte but it was not loaded into the RX buffer because the low byte load signal was inhibited by SKIP LD NEXT FRAME being set.

5. When Data 2 is shifted in, it resides in the RX shift register and Data 1 is shifted to the low byte which obliterates the SYNC character. A normal load sequence moves both bytes (Data 2 and Data 1) to the RX buffer. XFER FRAME DONE is set and it triggers the logic that generates D5-8 RX NPR RQ (1) L. This signal goes to the NPR control logic and generates D5-3 RX NPR L which clocks the RX buffer data register (D4-7) and puts Data 2 and Data 1 on the Unibus data lines. These characters are sent to memory and the SYNC character has been stripped from the message.

4.6 M7816 (AB SELECTORS AND BCC CONTROL)

4.6.1 Introduction

The M7816 module is a hex-height, extended-length, module that contains several functionally-separate logic circuits. They are listed in order of discussion.

1. Bus Selectors and Decoding Logic
2. Polynomial Register
3. Receive Block Check Character Generator
4. Transmit Block Check Character Generator
5. Transmit BCC Control
6. Receive BCC Control

4.6.2 Bus Selectors and Decoding Logic

4.6.2.1 Functional Description – The outputs of three registers on the M7816 module and one on the M7817 module are multiplexed to the Unibus data lines through one set of 16 bus drivers. This is accomplished by using 8 dual 4-line-to-1-line multiplexers; that is, each multiplexer handles two bits of each register. The registers are listed below:

Sequence Register (M7817)
Polynomial Register (M7816)
Receive BCC Register (M7816)
Transmit BCC Register (M7816)

Figure 4-49 is a simplified block diagram of the bus selectors and decoding logic. The decoding logic generates enabling signals for the multiplexers and bus drivers. It also generates select signals to choose the proper register.

The SEQ, POLY, RX BCC and TX BCC registers are secondary registers and are not selected directly by the M105 Address Selection Module. They are selected by bits 8–11 of the REG/ERR register and SELECT 6 from the M105 module.

The SEQ register contains 16 bits; the POLY, RX BCC and TX BCC registers contain 24 bits. In these registers, the low byte (bits 7–0) and extended byte (bits 23–16) are multiplexed and sent to the low byte of the bus selectors. For example, POLY MUX 0 H can be bit 0 or bit 16.

4.6.2.2 Detailed Logic Description – The circuit schematic for the bus selectors and decoding logic are contained in drawing D-CS-M7816-0-1 (Rev E) sheets 3 and 4 which are designated D9-1 and D9-2.

Before explaining the details of the bus selectors, it is useful to show the architecture of the registers that are inputs to the bus selectors. Figure 4-50 shows the architecture as a simplified block diagram.

Bus Selectors

The bus selectors are shown in print D9-1. Register selection is the same for both bytes but the method of enabling the multiplexers and bus drivers is different for each byte. This is due to the requirement of multiplexing the low byte (bits 7–0) and extended byte (bits 23–16) of the POLY, TX BCC and RX BCC registers as inputs to the low byte of the bus selectors.

Figure 4-51 shows a typical two bit slice of the high and low bytes of the bus selectors. The high byte example uses bits 08 and 09 (mux E4); the low byte example uses bits 00 and 01 (mux E8). Because the POLY, TX BCC and RX BCC low byte and extended byte are multiplexed, these bits can also represent bits 16 and 17.

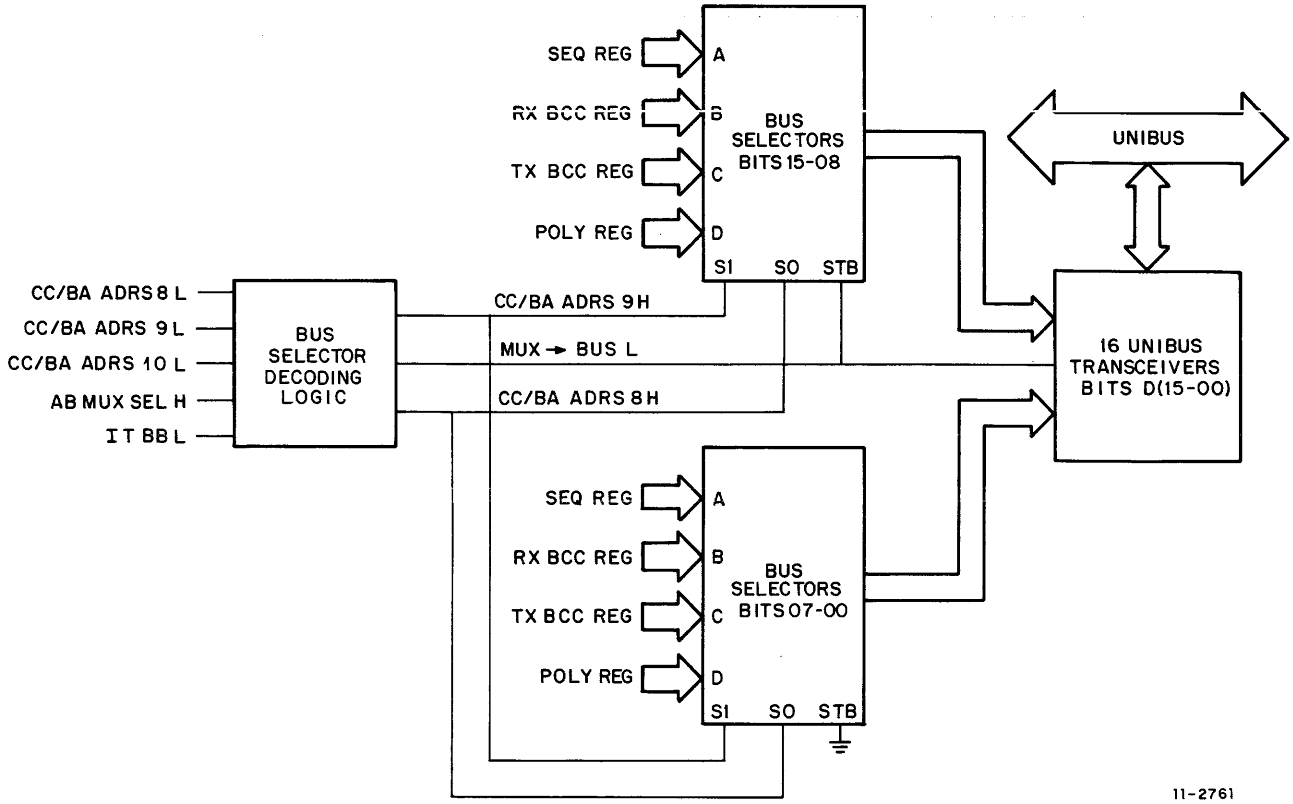


Figure 4-49 Block Diagram of AB Bus Selectors and Decoding Logic

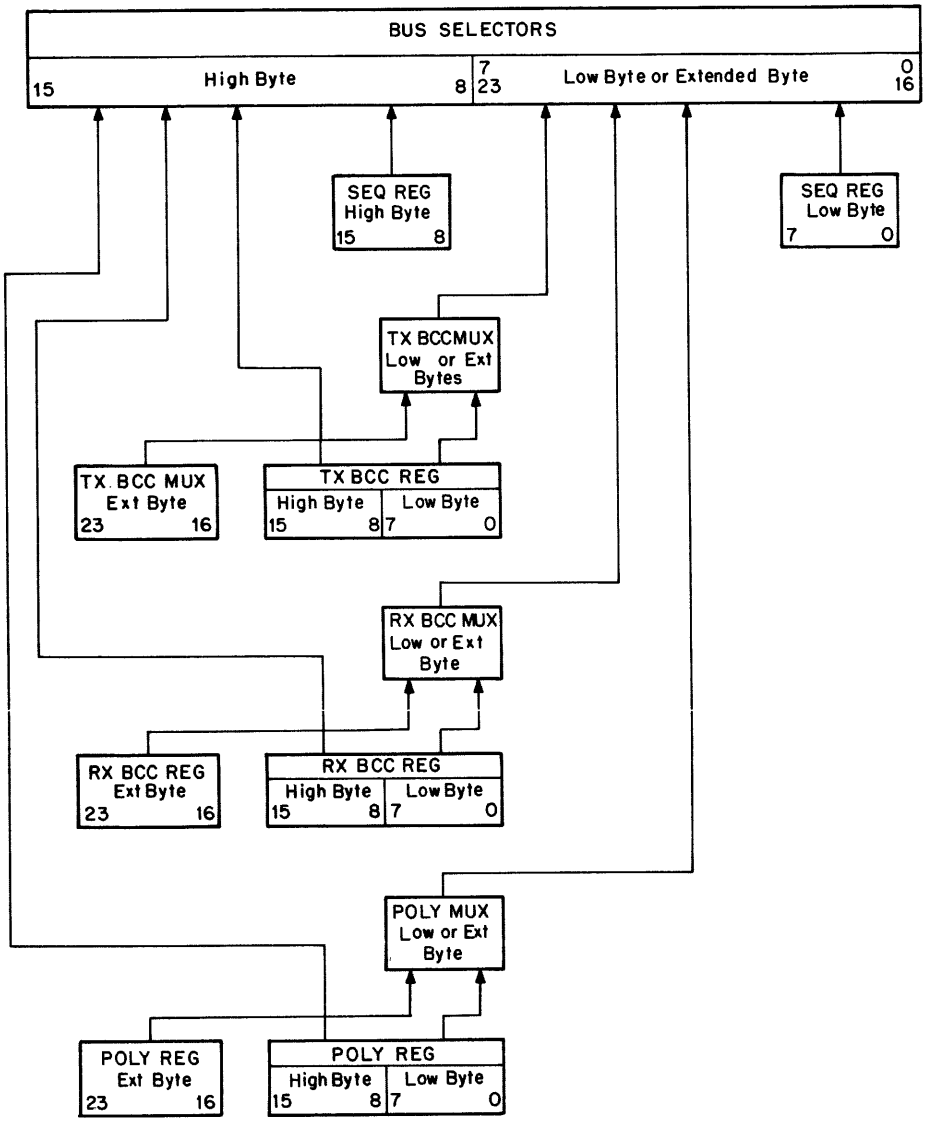
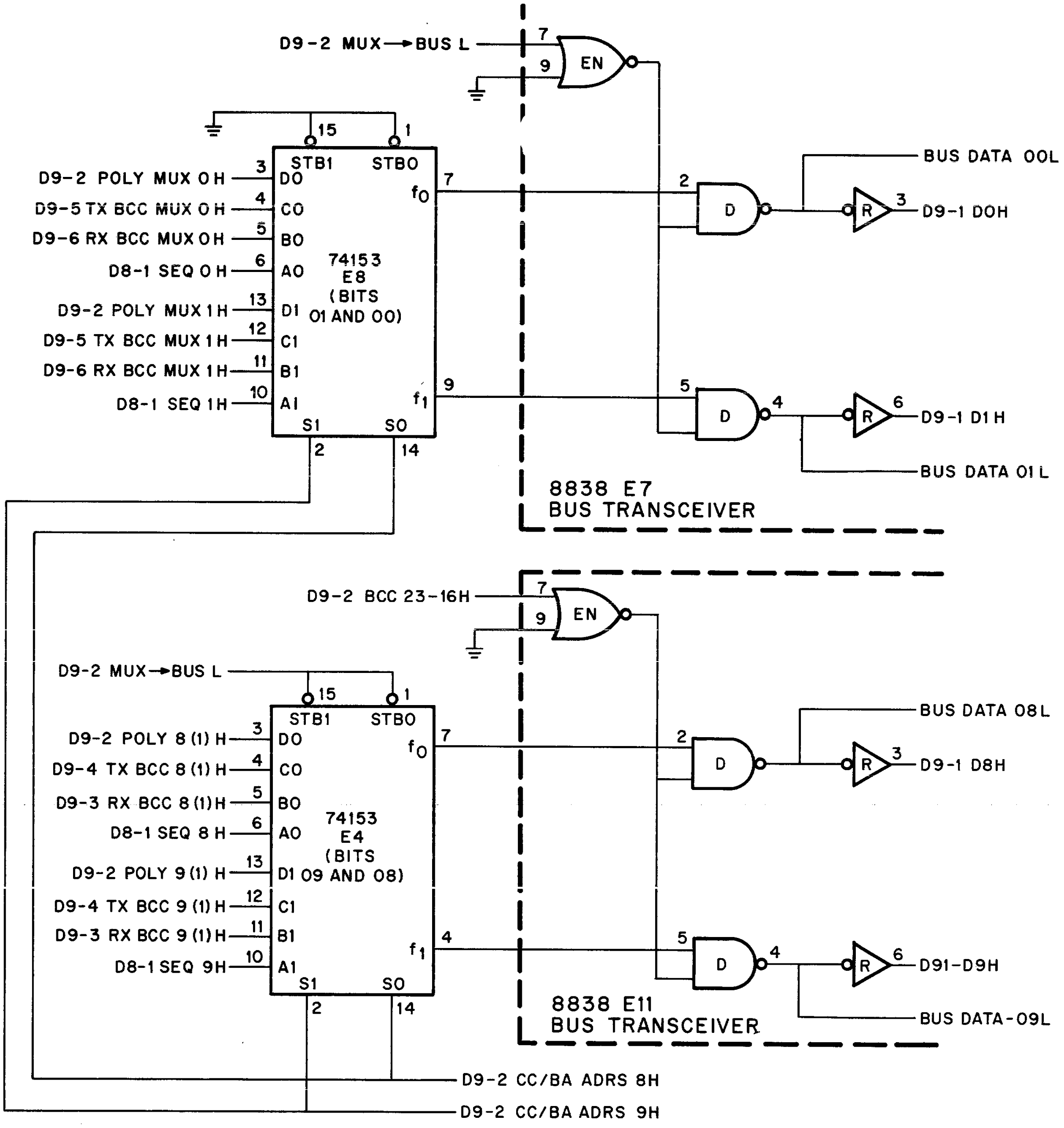


Figure 4-50 Block Diagram of Architecture of RX BCC, TX BCC, POLY and SEQ Registers



74153 TRUTH TABLE

ADRS INPUTS		STROBE	SELECTED INPUT
S1	SO		
L	L	L	A (SEQ)
L	H	L	B (RX BCC)
H	L	L	C (TX BCC)
H	H	L	D (POLY)
X	X	H	all outputs low

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Figure 4-51 Typical Two Bit Slice of the High and Low Bytes of the Bus Selectors

The low byte mux (E8) has its strobe or enabling inputs (STB1 and STB0) permanently connected to ground. The mux outputs are placed on the Unibus via bus drivers that are enabled when D9-2 MUX → BUS L is asserted. The high byte mux (E4) has its strobe inputs enabled when D9-2 MUX → BUS L is asserted and the associated bus drivers are enabled when D9-2 BCC 23–16 H is not asserted. This signal is only asserted when bits 23–16 of the POLY, TX BCC, and RX BCC registers are to be read. When the multiplexers are enabled, the select inputs (S1 and S0) choose the register to be read. The signals are D9-2 CC/BA ADRS 9 H for S1 and D9-2 CC/BA ADRS 8 H for S0. They are common for both bytes.

Assume that the RX BCC is operating in the 16 bit configuration and the program desires to read the contents of this register. The bus selector decoding logic drives S1 low and S0 high to select the RX BCC register. This is in accordance with the mux truth table in Figure 4-51. The decoding logic asserts D9-2 MUX → BUS L and holds D9-2 BCC 23–16 H low. Signal D9-2 MUX → BUS L puts the low byte on the Unibus. This signal also enables the high byte multiplexers and because D9-2 BCC 23–16 H is low, the high byte is put on the Unibus. Thus, the contents (bits 16–00) of the RX BCC register have been read.

Assume now that the RX BCC is operating in the 24 bit configuration and the program desires to read the contents of this register. Two steps are required to read the 24 bits. Bits 15–00 are read exactly as described in the previous example. Bits 23–16 are read as follows. The program sets bit 6 of the MISC register which results in assertion of D9-2 BCC 23–16 H. This signal inhibits the bus drivers for the high byte of the bus selectors. Signal D9-2 MUX → BUS L is asserted by the decoding logic and puts D9-6 RX BCC MUX 7 H–0 H on the Unibus. In this case, because MISC register bit 6 is set, these bits are actually bits 23–16 of the RX BCC register. Thus, in two steps, the contents (bits 23–00) of the RX BCC register have been read.

Bus Selector Decoding Logic

The bus selector decoding logic is shown in print D-CS-M7816-0-1 (Rev E) sheet 4 (D9-2). Figure 4-52 also shows this logic with some additional informative comments.

This logic also generates the signal (D9-2 CM → BUS H) that enables the output of the character detection register on the M7817 module. The discussion includes the decoding logic for this register plus the POLY, TX BCC, RX BCC, and the SEQ registers.

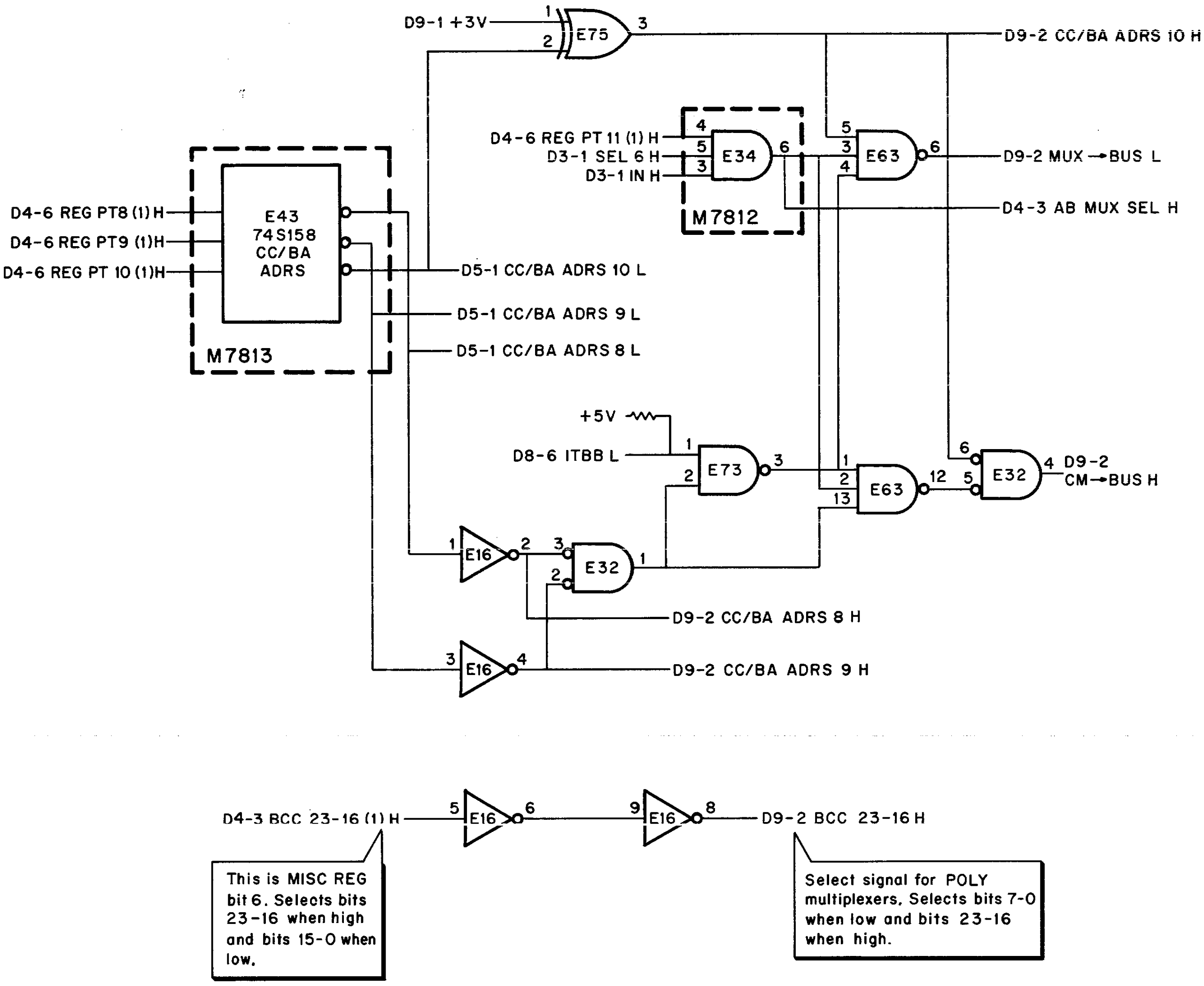
These registers are secondary registers that are selected by the secondary register pointer bits (11–08) of the REG/ERR CSR as shown below:

REG/ERR Bits					
11	**10**	**9**	**8**	**Octal**	**Register**
1	0	0	0	10	CHAR DET
1	1	0	0	14	SEQ
1	1	0	1	15	RX BCC
1	1	1	0	16	TX BCC
1	1	1	1	17	POLY

Bit 11 is a 1 for all five registers. The CHAR DET register is differentiated from the other four by bit 10. Differentiation between the SEQ, RX BCC, TX BCC, and POLY registers is accomplished by bits 8 and 9.

The enabling signal for the CHAR DET register is D9-2 CM → BUS H which is generated at gate E32 pin 4. Signal D8-6 IT BB L is an interlock signal that is generated on the M7817 module which contains the CHAR DET register. If the M7817 module is not installed, D8-6 IT BB L is not asserted and pin 1 of gate E73 remains high due to the connection to +5 V via R21. This inhibits D9-2 CM → BUS H even if the CHAR DET register is addressed.

Assume that the program desires to read the POLY register and it is in the 16 bit configuration. The program addresses the REG/ERR register and sets bits 11–8 to all 1s which points to the POLY register. The DQ11 is addressed again using 76XXX6 and a DATI transaction is performed. As a result, the M105 Address Module asserts D3-1 SEL 6 H and D3-1 IN H which go to pins 5 and 3 of E34 on the M7812 module (print D4-3). The third input (pin 4) of this gate is D4-6 REG PT 11 (1) H which is also high. This asserts D4-3 AB MUX SEL H at the output of E34 and it is sent to E63 pin 3 in the bus selector decoding logic (M7816, D9-2). Pin 5 of E63 is high because it is the double inversion of D4-6 REG PT 10 (1) H. Signal D4-6 REG PT 8 (1) H is double inverted by the CC/BA ADRS mux (print D5-1) and E16 to assert D9-2 CC/BA ADRS 8 H. This signal also goes to E32 pin 3. Signal D4-6 REG PT 9 (1) H is similarly double inverted to assert D9-2 CC/BA ADRS 9 H and is also sent to the other input (pin 2) of E32. The output (pin 1) of E32 is driven low and is sent to E73 pin 2. It is inverted by E73 and sent to E63 pin 4. All three inputs (pins 3, 4 and 5) of E63 are high so its output goes low which asserts D9-2 MUX → BUS L.



This is MISC REG bit 6. Selects bits 23-16 when high and bits 15-0 when low.

Select signal for POLY multiplexers. Selects bits 7-0 when low and bits 23-16 when high.

REGISTER SELECTION

REG PT BITS				OCTAL	REGISTER
11	10	9	8		
1	0	0	0	10	CHAR DET
1	1	0	0	14	SEQ
1	1	0	1	15	RX BCC
1	1	1	0	16	TX BCC
1	1	1	1	17	POLY

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Figure 4-52 Bus Selector Decoding Logic

The decoding logic has asserted D9-2 MUX→ BUS L which enables the high byte multiplexers for the bus selectors and the low byte bus drivers. Signals D9-2 CC/BA ADRS 8 H and D9-2 CC/BA ADRS 9 H are both high which selects the POLY register. Because the POLY register is in the 16 bit configuration, the program did not set MISC register bit 6. Signal D4-3 BCC 23–16 (1) H is low. It is double inverted by two E16 inverters to become D9-2 BCC 23–16 H. It is the enabling signal for the bus drivers of the bus selector high byte. Being low, it enables the drivers.

4.6.3 Polynomial Register

4.6.3.1 Functional Description – The polynomial register (POLY) is a 24 bit read/write register that stores the polynomial used in generating the BCC character during transmission or checking the BCC character during reception.

Any polynomial, up to 24 bits, can be used; however, there are a few that are commonly used. Appendix A contains a general discussion of BCC computation.

There are some specific rules for loading the POLY which are stated below and emphasized by a typical example.

The polynomial is an algebraic representation of a binary word. The example used is $X^{16} + X^{15} + X^2 + 1$. It is the generator polynomial for a cyclic redundancy checking (CRC) error detecting code called CRC-16. This code is applied to synchronous systems that use 8-bit characters. The rules for loading the generator polynomial using CRC-16 are as follows:

1. Disregard the polynomial's highest order term. The hardware automatically includes this bit. The polynomial is $X^{16} + X^{15} + X^2 + 1$. The highest order term is X^{16} which is ignored. This polynomial provides 17 term positions; from X^{16} (highest order) to X^0 or 1 (lowest order). It contains only four terms.

2. Assign the polynomial second highest order term position to bit 0 of the POLY register. Assign the remaining term positions in descending order to the register bits in ascending order. In this example the lowest order term, which is X^0 or 1, is assigned to register bit 15.

3. Examine the polynomial and for each term present (except the highest order term) set the corresponding register position to a 1. Figure 4-53 shows this graphically.

Figure 4-54 is a simplified block diagram that shows the structure of the POLY register. The high byte (POLY 8 (1) H–POLY 15 (1) H) goes directly to the bus selector high byte multiplexer. The low byte (POLY 0 (1) H–POLY 7 (1) H) and extended byte (POLY 16 (1) H–POLY 23 (1) H) are multiplexed and sent to the bus selector low byte multiplexer as POLY MUX 0 H–POLY MUX 7 H. These signals can be bits 0–7 or 16–23 depending on the POLY register decoding logic. This logic also generates two register clock signals: one for bits 0–15 and one for bits 16–23.

4.6.3.2 Detailed Logic Description – The circuit schematic for the POLY register and associated decoding logic is contained in drawing D-CM-M7816-0-1 (Rev E) sheet 4 which is designated D9-2.

The 24 bits of the POLY register are stored in four 74175 quad flip-flops and two 74174 hex flip-flops as shown below.

Designation and Name	Input Signals	Output Signals
E12 POLY 3–0	D9-1 D0 H – D9-1 D3 H	D9-2 POLY 0 (1) H – D9-2 POLY 3 (1) H
E17 POLY 9–4	D9-1 D4 H – D9-1 D9 H	D9-2 POLY 4 (1) H – D9-2 POLY 9 (1) H
E6 POLY 15–10	D9-1 D10 H – D9-1 D15 H	D9-2 POLY 10 (1) H – D9-2 POLY 15 (1) H
E19 POLY 19–16	D9-1 D0 H – D9-1 D3 H	D9-2 POLY 16 (1) H – D9-2 POLY 19 (1) H
E18 POLY 23–20	D9-1 D4 H – D9-1 D7 H	D9-2 POLY 20 (1) H – D9-2 POLY 23 (1) H

The 74174 and 74175 flip-flops are D type with common clock and clear inputs. The 74175s have complementary outputs and the 74174s do not. All register outputs come from the 1 side of the flip-flops. The six devices use a common direct clear signal. It is D9-2 INI L which is the inversion of D5-4 INI H from gate E58.

The POLY register uses two clock signals: one for bits 0–15 and one for bits 16–23. They are both generated by D9-6 LD POLY L.

Figure 4-55 shows the logic for generating the clock signals. It also shows how D9-6 LD POLY L is generated to add continuity to the discussion.

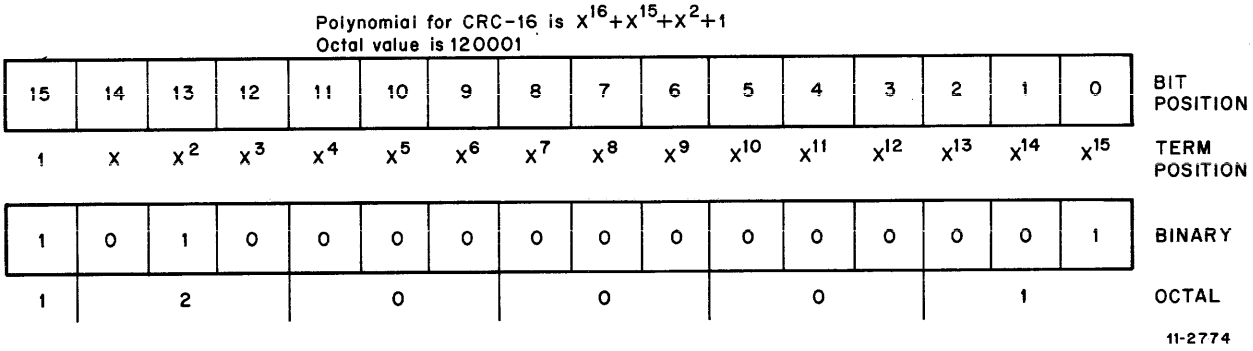


Figure 4-53 Configuration of POLY Register for Polynomial $X^{16} + X^{15} + X^2 + 1$ (CRC-16)

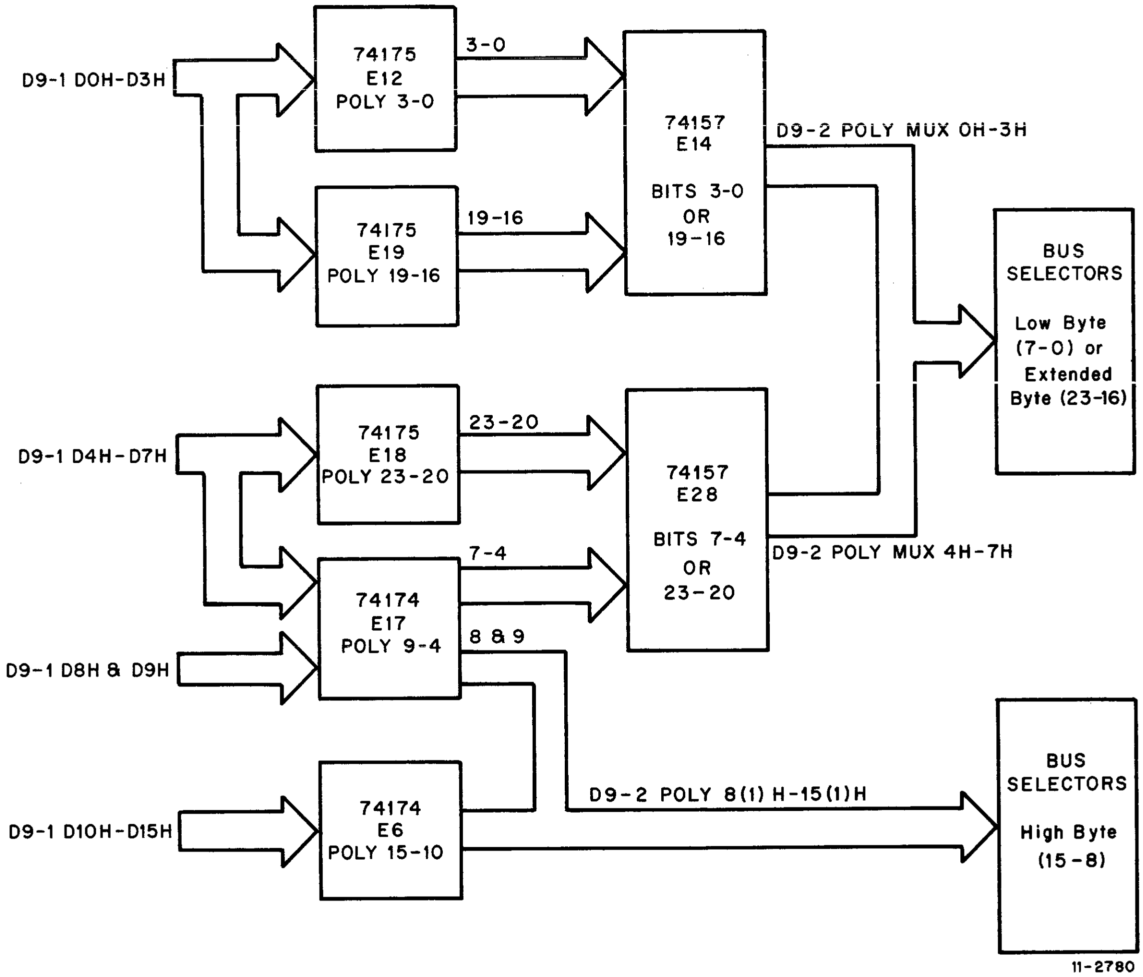


Figure 4-54 Architecture of POLY Register

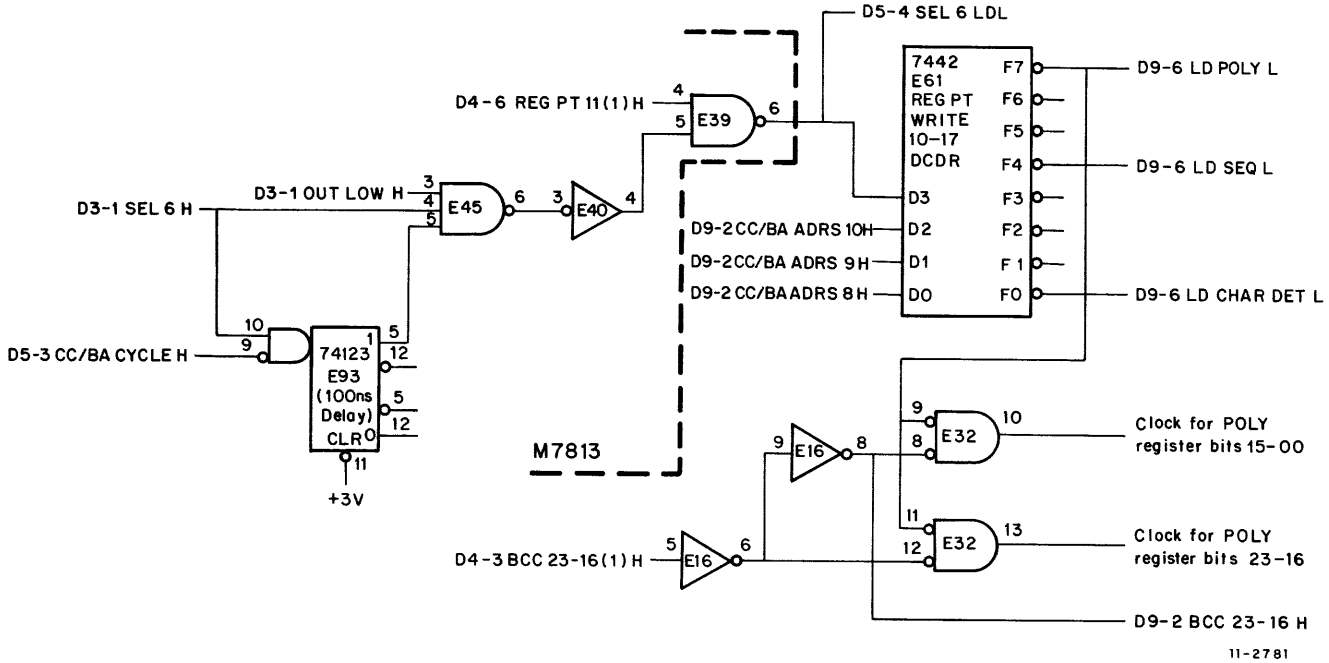


Figure 4-55 Logic for Generating Clock Signals for POLY Register

Assume that a polynomial is to be loaded that requires 16 bits. The program selects the POLY register via bits 11–8 of the REG/ERR register. It addresses the DQ11 again using 76XXX6 and a DATO transaction is performed. As a result, the M105 Address Module asserts D3-1 SEL 6 H and D3-1 OUT LOW H which go to the pulse generator on the M7813 module (Figure 4-55). This produces a 100 ns negative pulse (D5-4 SEL 6 LD L) at E39 pin 6. This signal is sent to the RG PT WRITE 10, 14, 17 decoder (E61) on the M7816 module (print D9-6). E61 is a 7442 4-line-to-10-line decoder but it is connected to operate as a 3-wire, binary to octal decoder. The three least significant inputs (D0, D1 and D2) are the binary code and the most significant input (D3) is the strobe or enabling input. The strobe (D5-4 SEL 6 LD L) must be low to enable the decoder. Because the POLY register is selected, the binary code inputs (D9-2 CC/BA ADRS 10 H, 9 H and 8 H) are all high. This selects output f7 and asserts D9-6 LD POLY L.

Because POLY register bits 0–15 are selected, bit 6 of the MISC REG is not set. As a result, D4-3 BCC 23–16 (1) H is low. This signal is inverted once and sent to pin 12 of gate E32. This drives the output (pin 13) of this gate low which inhibits the clock for POLY register bits 23–16. Signal D4-3 BCC 23–16 (1) H is also double inverted and puts a low on pin 8 of the other E32 gate. D9-6 LD POLY L puts a low on the other input (pin 9) of this gate which drives the output (pin 10) high. This positive transition clocks data into bits 0–15 of the POLY register.

If a 24 bit polynomial is to be loaded into the register, the sequence is the same. However, D4-3 BCC 23–16 (1) H is now high (set by program) and only the clock from E32 pin 13 is generated, thus POLY 23–16 is clocked (E17, E18).

4.6.4 Receive BCC Generator

4.6.4.1 Functional Description – A simplified block diagram of the RX BCC generator is shown in Figure 4-56. The inputs of the BCC generator are conditioned by the outputs of the POLY register which holds the polynomial that represents the LRC or CRC code being used. The remote station sends a message with a BCC character appended. Both stations must use the same code. The RX BCC generator examines the received data and computes a BCC character. It examines the received BCC character and the register goes to all 0s if the received BCC character agrees with the computed one. This means that the message has been received without error.

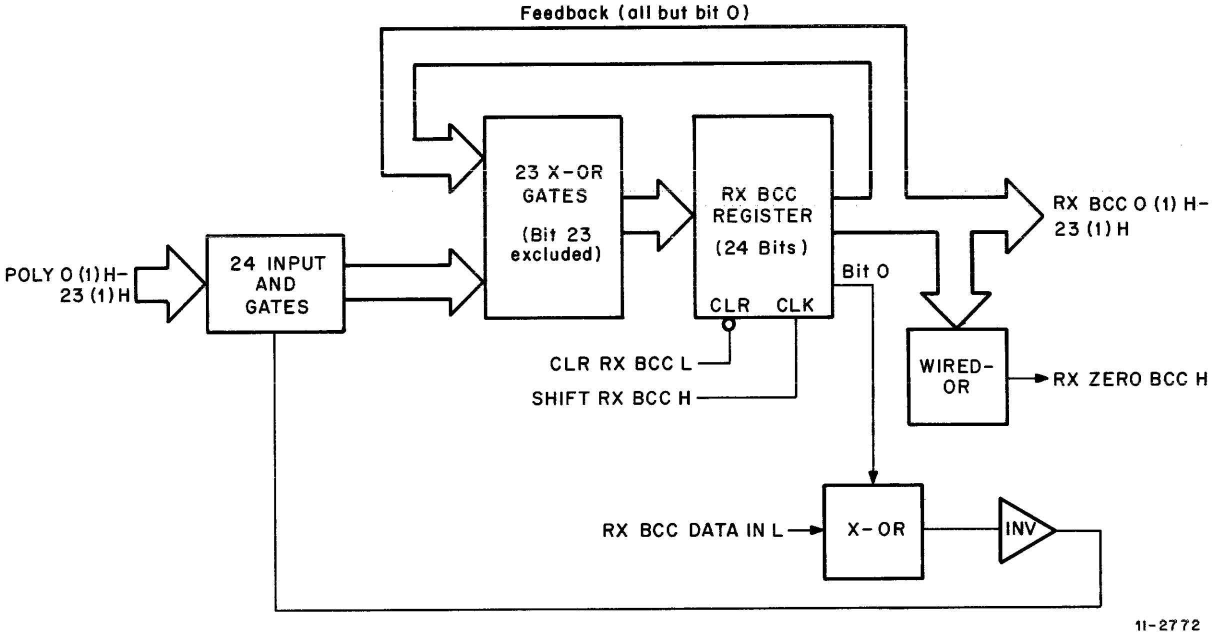


Figure 4-56 Block Diagram of RX BCC Generator

If the BCC characters do not agree, one or more errors are present in the message. In this case, RX ZERO BCC H is low. It is sent to the RX BCC control logic (D9-6) and generates the BCC ERR L flag which denotes that an incorrect message has been received. The receiving station requests that the message be retransmitted.

The RX BCC generator just checks for errors; it does not locate them.

To be compatible with the DQ11 method of handling characters, the BCC character must be a multiple of the bits per character selected. For example, CRC-16 is used with 8 bit characters and provides a 16 bit BCC character. Other common codes also provide a multiple of 2 and some provide a multiple of 1. The user could implement a code with a different multiple. The DQ11 provides multiples of 1, 2 and 3 only.

The M7817 module provides programmable BCC multiple selection using bits 4 and 5 of the SEQ register. The M7816 module provides jumpers to select the number of BCCs. When both modules are installed, either selection method can be used, depending on system programming.

4.6.4.2 Detailed Logic Description – The circuit schematic for the RX BCC generator is contained in drawing D-CS-M7816-0-1 (Rev E) sheet 5 which is designated D9-3.

The BCC accumulation (24 bits maximum) is stored in four 74174 hex D-type flip-flops. These 24 flip-flops operate as a shift register and are clocked simultaneously by D9-6 SHIFT RX BCC H from the RX BCC control logic. All bits are cleared simultaneously by D9-6 CLR RX BCC L. (The generation of these control signals is discussed in a subsequent section.)

At the remote station, the TX BCC generator produces a BCC character, using a specific LRC or CRC generator polynomial, and appends it to the data. The RX BCC generator regards the complete transmission (data plus BCC) as a code message polynomial which it divides by the same generator polynomial. If there is no error, the division produces no remainder (BCC register reads all 0s) and it is assumed that the message is correct.

The inputs to the RX BCC flip-flops are programmable, using the POLY generator, to allow any generator polynomial up to 24 bits to be used. Of course, the selected RX BCC generator polynomial must be the same as the one used by the transmitting station.

Each D-input of bits 0–23 of the RX BCC flip-flops is connected to the output of an exclusive-OR gate (7486 2-input X-OR). One input of each X-OR gate is connected to the previous flip-flop output. The single exception is the MSB (bit 23) which has no exclusive-OR gate. The other input of each X-OR gate is connected to the output of an AND gate (7408 2-input AND). The single exception is the MSB (bit 23) whose AND gate is connected directly to the associated flip-flop input. There are 24 AND gates and 23 X-OR gates (bit 23 has no X-OR gate).

One input of each AND gate is connected to the associated output of the POLY register; for example, D9-2 POLY 18 (1) H goes to pin 4 of AND gate E47 which is associated with RX BCC generator bit 18. The other input of all AND gates is connected to the output (pin 8) of E58. This is the inversion of the result of the X-ORing of D4-5 RX BCC DATA IN L and the output of the 0 bit of the RX BCC generator.

Each RX BCC generator output is sent to a 7416 inverter. All the inverter outputs are wire-ORed to assert D9-3 RX ZERO BCC H when all bits are 0. If the BCC accumulation is not all 0s, this signal is low and results in generation of the RX BCC ERR flag and ERR INTR signal on the M7812 module (print D4-6). Figure 4-57 shows bits 0, 1, 2, 22 and 23 of the RX BCC generator to illustrate the architecture.

If a particular stage of the RX BCC generator is conditioned by having its associated POLY register bit set (high or logical 1), the information stored in that bit is the X-OR function of the data and feedback from the previous stage. If the associated POLY register bit is cleared (low or logical 0), the X-OR gate acts as a non-inverting gate and stores what was in the previous stage just as if the AND gate was not there.

Operationally, these facts are pointed out when a polynomial of less than 24 bits is used. Assume the use of the polynomial for CRC 16 which is $X^{16} + X^{15} + X^2 + 1$. The lowest order term is X^0 or 1 and is assigned to bit 15. (Refer to rules for loading the POLY register in Paragraph 4.6.3.1). POLY register bits 16–24 must be cleared. Regardless of the state of the data, stages 16–24 cannot pass along anything but 0s. The RX BCC generator acts as if it is only 16 bits long.

The serial data into the RX BCC generator is D4-5 RX BCC DATA IN L which is sent to pin 13 of E48 where it is X-ORed with the output of bit 0. This signal comes from the output of E97 on the M7812 module (Figure 4-58). E97 is a 2-wide, 2-input, AND-OR-invert gate (7450). The qualifying signal for both halves of this gate is D4-3 BITS 11 (1) H which is high for double-character operation and low for single-character operation. For double-character

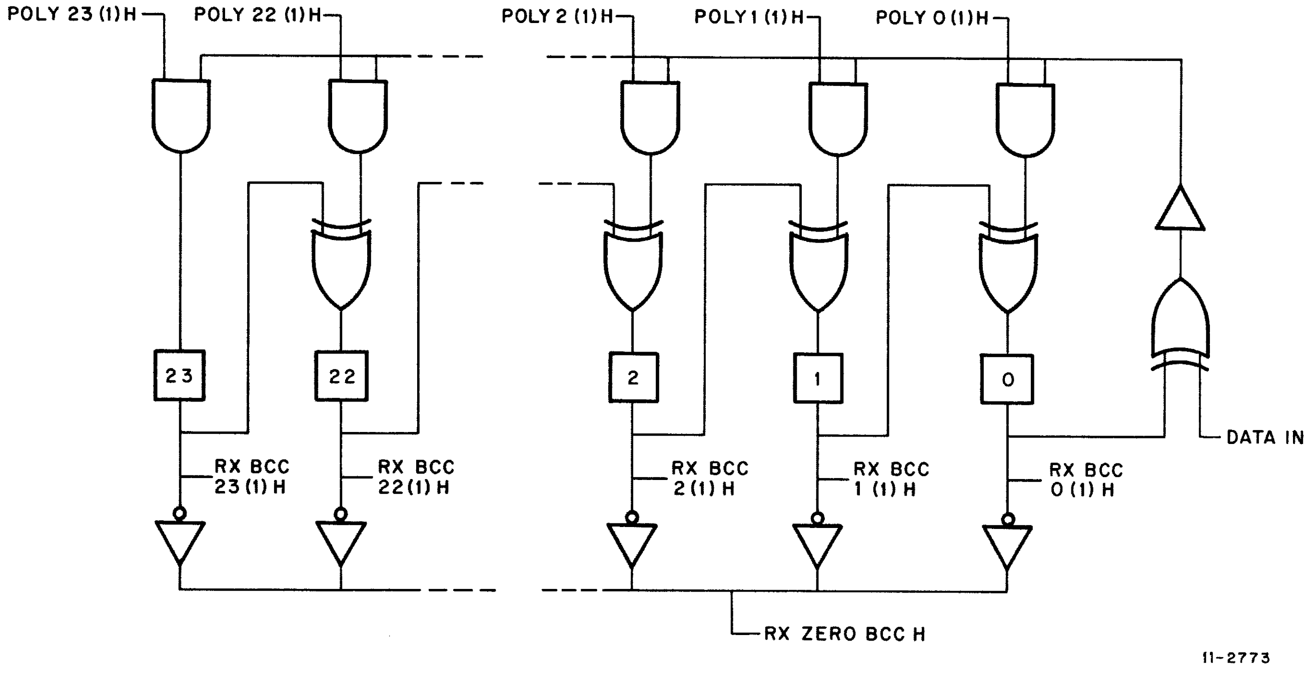


Figure 4-57 Architecture of RX BCC Generator

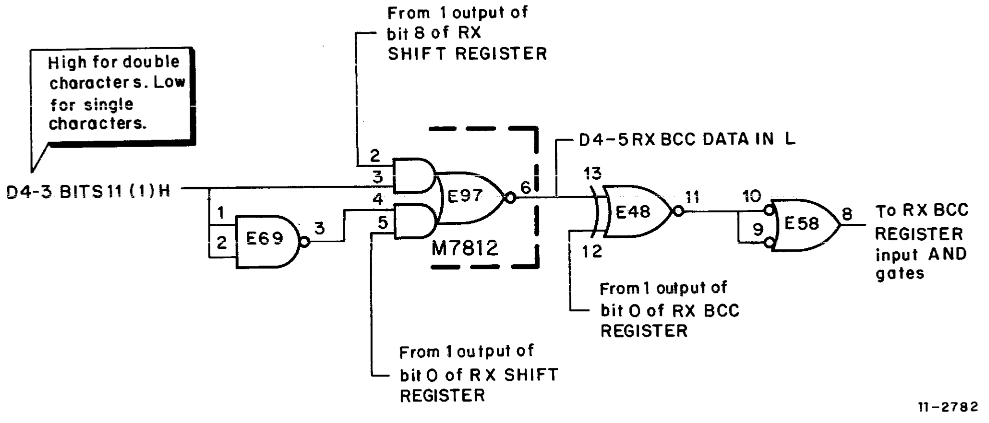


Figure 4-58 Data Input Gating for RX BCC Generator

operation, it is directly ANDed with the 1 output of bit 8 of the RX shift register. For single-character operation, it is inverted and then ANDed with the 1 output of bit 0 of the RX shift register. The first bit to be processed by the RX BCC generator occurs after one complete character has been shifted into the RX shift register.

Figure 4-59 shows a sample RX BCC accumulation using CRC-16. A graphical representation of this process is used because it is the most comprehensible and the least cumbersome. The polynomial for CRC-16 is $X^{16} + X^{15} + X^2 + 1$ which puts a 1 on the input of the AND gates associated with bits 0, 13, and 15. In this example, a 16-bit data word (two 8-bit characters) and a 16-bit BCC character are received and processed LSB first. The column on the far right shows the X-OR of the data bit and the LSB (bit 0) of the RX BCC generator prior to shifting. This column is the feedback path which goes to all AND gates in the RX BCC generator. The column on the far left identifies the time state of the generator. The states of all 16 bits are shown starting with all 0s. Subsequent rows show the states after shifting. The sample shows the BCC accumulation after shifting in the 16 data bits. It is the same as the received BCC character. When this BCC character is received (after shift number 32), the RX BCC generator reads all 0s which indicates that the message has been received without error.

4.6.5 Transmit BCC Generator

4.6.5.1 Functional Description – The architecture of the TX BCC generator is very similar to the RX BCC generator. The input gating, storage, and feedback system are identical for both generators. The individual outputs of the TX BCC generator are not used to generate a flag signal so the 24 inverters are omitted. The output gating is different because the serial output (BCC character) of the TX generator can be transmitted.

The TX BCC generator examines the data being transmitted and accumulates a BCC character. This character can be transmitted when the TX BCC control logic generates the BCC enabling signal.

4.6.5.2 Detailed Logic Description – The circuit schematic for the TX BCC generator is contained in drawing D-CS-M7816-0-1 (Rev E) sheet 6 which is designated D9-4.

The BCC accumulation (24 bits maximum) is stored in four 74174 hex D-type flip-flops. These 24 flip-flops operate as a shift register and are clocked simultaneously by D9-5 SHIFT TX BCC H from the TX BCC control logic. All bits are cleared simultaneously by D9-5 CLR TX BCC L. (The generation of these control signals is discussed in a subsequent section.) The inputs to the TX BCC generator are programmable, using the POLY register, exactly like the RX BCC generator. Refer to Paragraph 4.6.4.2 for a discussion of the conditioning of the inputs and operation of the feedback loop.

The serial data into the TX BCC generator is D4-7 TX DATA H which comes from OR gate E23 on the M7812 module. This signal is inverted by E67 (print D4-7) and sent to the DF11 as D4-7 SERIAL DATA OUT L. The information to be transmitted can be data, VRC bit, PAD character or BCC character.

SHIFT NO.	RX BCC GENERATOR BITS 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Data In		Feedback Before Shift
Start	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–		1
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	LSB	1
2	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0		1
3	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0		1
4	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0		1
5	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0		1
6	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0		1
7	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	DATA	1
8	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0		1
9	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0		1
10	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0		1
11	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0		1
12	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0		1
13	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0		1
14	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0		0
15	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0		1
16	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	MSB	1
17	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	LSB	0
18	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0		0
19	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0		0
20	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0		0
21	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0		0
22	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0		0
23	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0		0
24	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	BCC	0
25	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0		0
26	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0		0
27	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0		0
28	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0		0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1		0
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0		0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	MSB	0

Arrows Indicate Exclusive-OR of Data Bit and LSB of BCC Register Prior to Shift

BCC Register ALL 0s
Received Message Assumed
To Be Correct

16 Bit Data Word
and BCC Received

NOTE

At shift no. 16, the BCC accumulation in the RX BCC generator snould be identical to the BCC character about to be received.

Figure 4-59 RX BCC Accumulation Using CRC-16

Assume that it is desired to transmit a BCC character directly after a block of data. As the data is being transmitted, it is also sent to pin 13 of X-OR gate E70 as D4-4 TX DATA H. The other input (pin 12) of E70 is D9-4 TX BCC 0 (1) H which is the 0 bit of the TX BCC generator. The output (pin 11) of X-OR gate E70 is sent to E64 pin 5. The other input (pin 4) of this gate is connected to D5-6 BCC EN (1) L. This is the BCC enabling signal which comes from the BCC SEND ENABLE flip-flop on the M7813 module. This signal is low when a BCC character is being transmitted. At this time, D5-6 BCC EN (1) L is high because data is being transmitted. This enables E64 and allows the X-ORing of data and bit 0 to be fed back to the TX BCC generator via E58. This permits the BCC character to be accumulated.

D5-6 BCC EN (1) L, which is high, is inverted by E69 and sent to pin 10 of E64. This inhibits D9-4 BCC/DLE L and prevents the contents of the TX BCC generator from being shifted out while data is transmitted.

When the data transmission is complete and it is time to transmit the BCC character, the TX BCC generator control logic asserts D9-5 BCC RQ L. This signal allows the BCC SEND ENABLE flip-flop to be set and asserts D5-6 BCC EN (1) L which holds the feedback signal line low from E58 pin 6. This action prevents alteration of the contents of the generator and allows the contents to be shifted out. With D5-6 BCC EN (1) L low, the contents of the TX BCC generator (which is the BCC character), are shifted out the bit 0 position via E64 pin 8 as D9-4 BCC/DLE L.

4.6.6 TX BCC Control Logic

4.6.6.1 Functional Description – A simplified block diagram of the TX BCC control logic is shown in Figure 4-60. The logic performs several functions that are interrelated but can be described separately. The major functional areas are listed below in order of discussion.

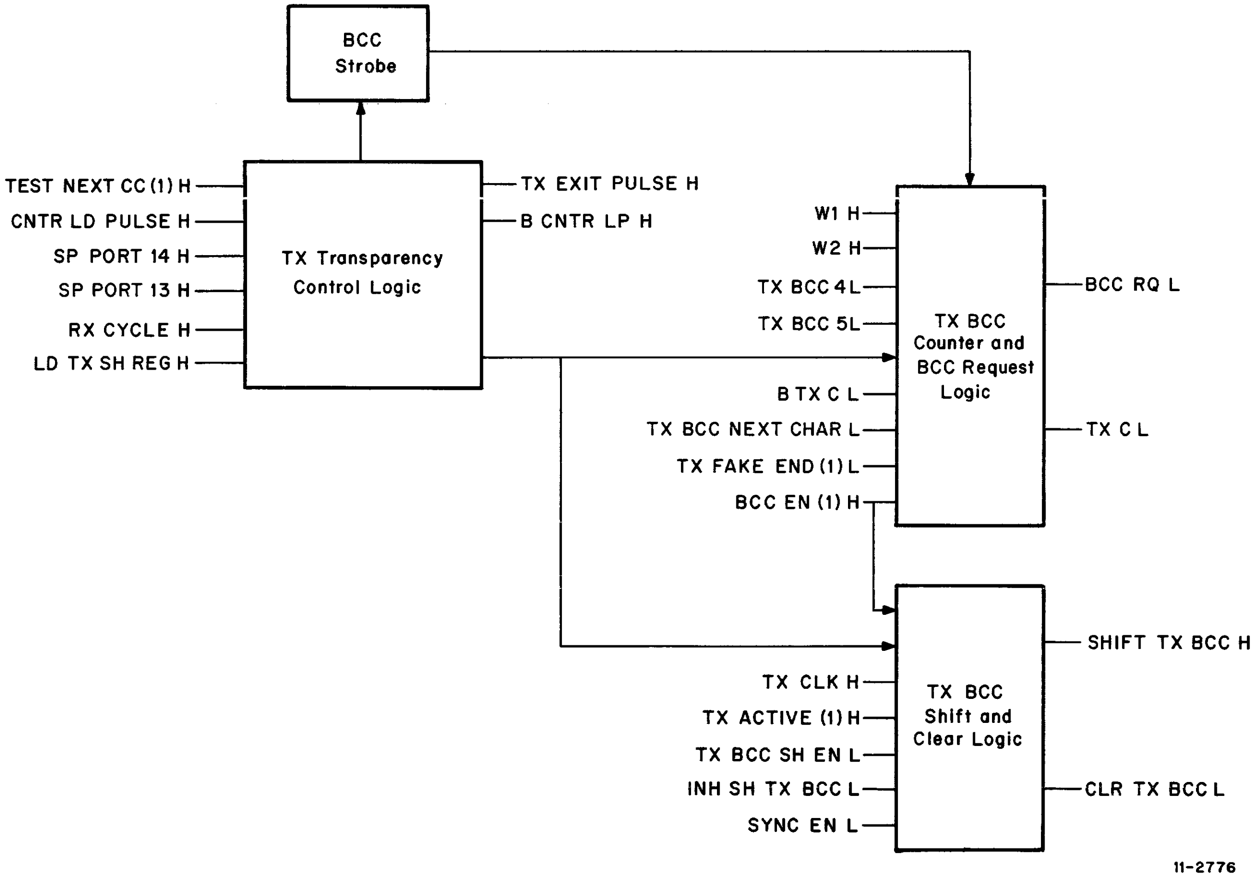


Figure 4-60 Simplified Block Diagram of TX BCC Control Logic

1. TX Transparency Control Logic. This logic allows the transmitter to enter and exit the transparent mode under control of REG/ERR CSR bits 14 (ENTER T) and 13 (EXIT T). This is a function of the M7816 module only and is called total transparency to differentiate it from the control of the transparent text mode provided by the M7817 module, when it is installed. When the transmitter enters total transparency, this logic sends a signal to the TX BCC shift and control logic that starts the TX BCC generator and turns off all character recognition logic. When the transmitter exits total transparency, this logic generates a signal that enables the TX BCC counter logic and allows the selected number of BCC characters to be appended to the message prior to the shutdown of the TX BCC generator. It also turns on the character recognition logic.

2. TX BCC Counter and BCC Request Logic. Jumpers W1 and W2 on the M7816 module allow selection of 1, 2 or 3 BCC characters. If the M7817 module is installed, control signals are used instead of jumpers to make the selection. In both cases, qualification of two TX BCC counter flip-flops by the jumpers (or M7817 signals) allow the TX BCC generator to operate long enough to append the selected number of BCC characters. This logic normally provides a one character delay to ensure that the last data character is included in the BCC accumulation before the BCC characters are appended.

3. TX BCC Shift and Clear Logic. This logic generates the pulses that shift the TX BCC generator. It also provides a signal to clear the generator. One section of the logic converts the TX clock signal to positive 50 ns pulses that shift the TX BCC generator. It is controlled by signals from the transparency control and counter logic and by signals from the M7817 module. The other section of the logic generates a signal that clears the TX BCC generator and a signal that clears various flip-flops in the transparency control and counter logic.

4.6.6.2 Detailed Logic Description – The circuit schematic for the TX BCC control logic is contained in drawing D-CS-M7816-0-1 (Rev E) sheet 7 which is designated D9-5.

TX Transparency Control Logic
The TX total transparency control logic is shown in the left center section of print D9-5. It is also shown in Figure 4-61.

The basic controlling functions for this logic are REG/ERR CSR bits 14 (ENTER T) and 13 (EXIT T). When bit 14 is set, the TX transparency control logic forces the DQ11 into the total transparent mode and starts the TX BCC generator. When bit 13 is set, this logic allows the DQ to exit from the total transparent mode. It triggers the TX BCC counter logic which allows the selected number of BCC characters to be transmitted; then it turns off the TX BCC generator.

Bits 14 and 13 perform their functions when the character count register is tested for non-zero by the hardware. This occurs when the current character count register goes to zero (overflows) or at the first transfer following the assertion of GO.

The following example is used to discuss the operation of the logic. It is desired to transmit a message in total transparent mode with two BCC characters appended. The transmitter is turned on, bit 14 (ENTER T) is set, the TX primary CC register is loaded with the specified character count, and the TX BCC generator is turned on. In this example, the message length does not exceed the character count loaded in the TX primary CC register; therefore, the TX secondary CC register contains a count of zero. When the last data character is transmitted, the TX primary CC register goes to zero and bit 13 (EXIT T) is set to take the transmitter out of the transparent mode. The two BCC characters are transmitted and then the BCC generator is shut off.

The operation of the TX transparency control logic during this example is discussed below.

1. The program sets REG/ERR CSR bit 14 (ENTER T). This asserts D5-2 SP PORT 14 H which is sent to pin 5 of 3-input NAND gate E89. The DQ11 is in the transmit mode so signal D5-3 RX CYCLE H is low. It is inverted by E82 and puts a high on the second input (pin 4) of E89. Signal D5-3 TEST NEXT CC (1) H is low (it is asserted only at CC register overflow). It is inverted by E69 and puts a high on pin 2 of 2-input AND gate E80. The other input (pin 1) of this gate goes high when D5-3 CNTR LD PULSE H is asserted. This occurs when the TX primary CC register is loaded. The output (pin 3) of E80 goes high and is sent to the third input (pin 3) of E89.

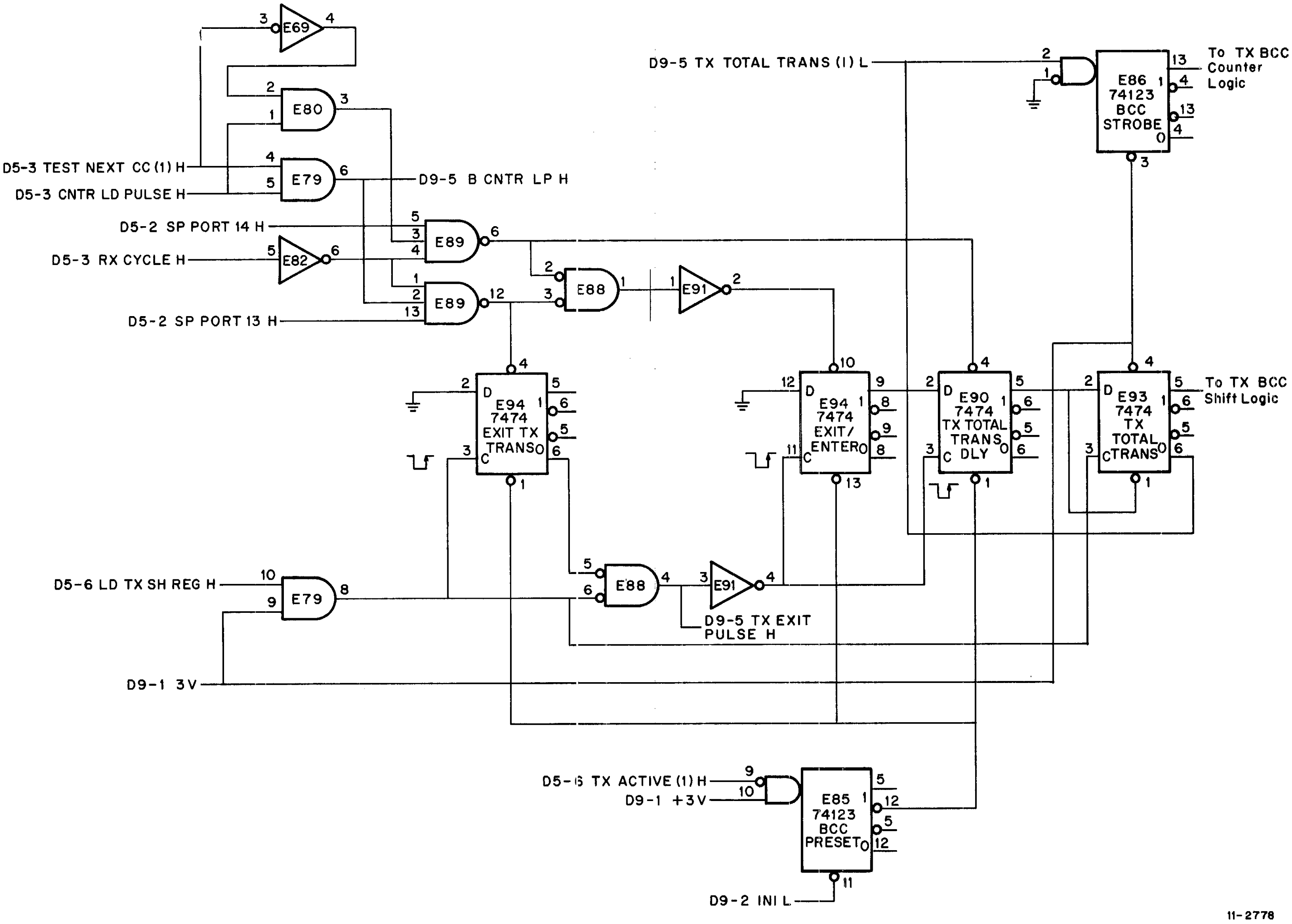


Figure 4-61 TX Total Transparency Control Logic

2. With the three inputs high, the output (pin 6) of NAND gate E89 goes low. This signal directly sets the TX TOTAL TRANS DLY flip-flop via its preset input.

3. The high signal from the 1 output of TX TOTAL TRANS DLY is sent to the D input of the TX TOTAL TRANS flip-flop. One or two clock pulses later, D5-6 LD TX SH REG H is asserted and sent to E79 pin 10. The other input of this gate is connected to +3 V so its output (pin 8) goes high. This signal clocks TX TOTAL TRANS and sets it.

4. The high signal from the 1 output of TX TOTAL TRANS goes to pin 9 of E83. The other input (pin 10) is also high because D5-6 TX ACTIVE (1) H is asserted. This drives the output of E83 low and after a delay caused by RC network C96, C97 and R22, it passes through E76 and E89 to qualify E71 and allow generation of the TX BCC shift pulses (D9-5 SHIFT TX BCC H). This turns on the TX BCC generator.

   The transparent data is transmitted and now the control logic must allow the transmitter to exit from the total transparent mode.

5. The program sets REG/ERR CSR bit 13 (EXIT T). This asserts D5-2 SP PORT 13 H which is sent to pin 13 of 3-input NAND gate E89. The second input (pin 1) is high because the DQ11 is in the transmit mode (D5-3 RX CYCLE H is not asserted). When the TX primary CC register overflows, both D5-3 TEST NEXT CC (1) H and D5-3 CNTR LD PULSE H are asserted. They are ANDed at E79 pins 4 and 5 and drive the third input (pin 2) of E89 high.

6. With the three inputs high, the output (pin 12) of NAND gate E89 goes low. This signal directly sets the EXIT TX TRANS flip-flop via its preset input. The low signal from the 0 output of EXIT TX TRANS goes to E88 pin 5. The other input (pin 6) of this gate is also low so the output (pin 4) goes high. It is inverted by E91 and is sent to the clock input of TX TOTAL TRANS DLY.

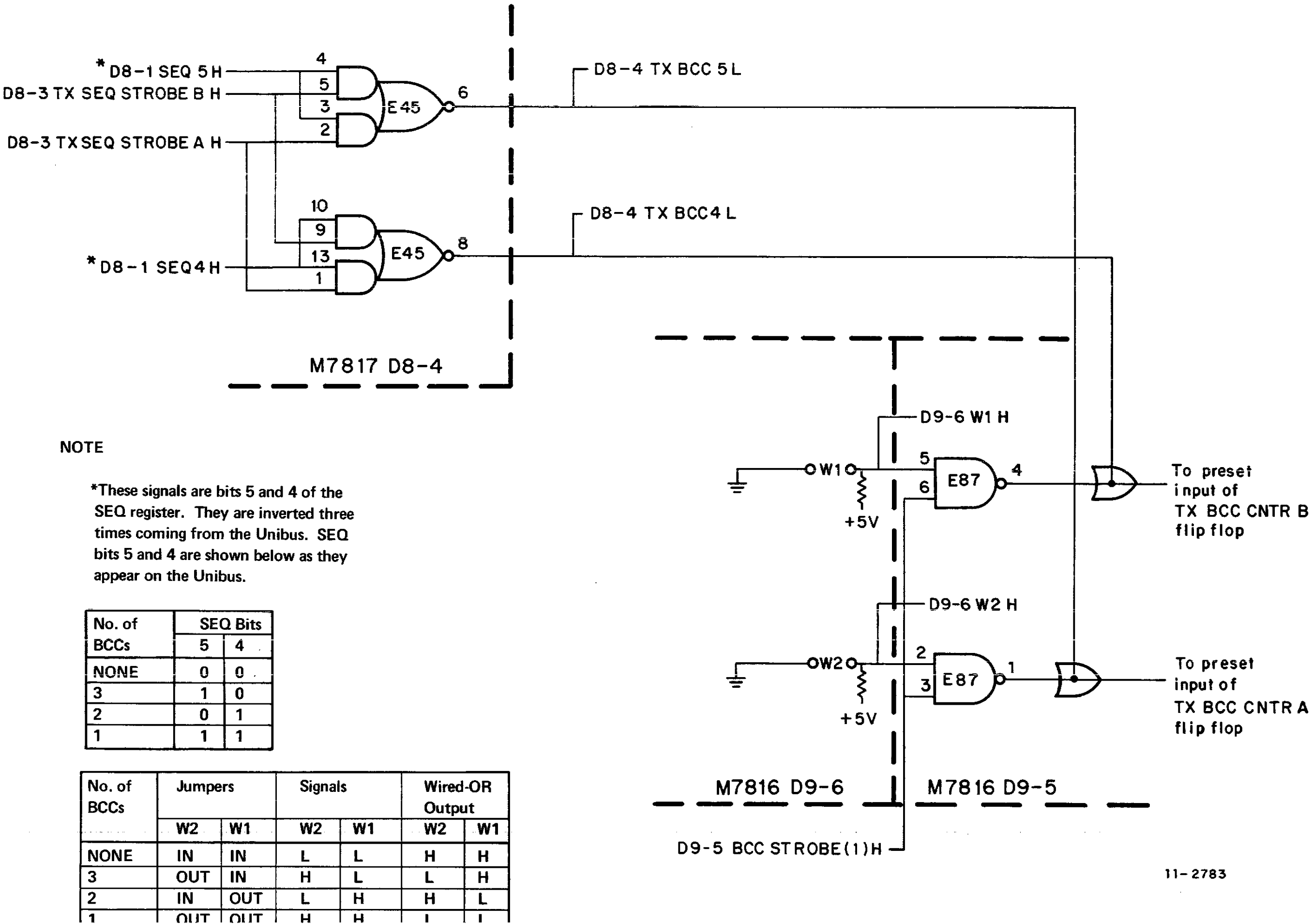
7. One or two clock pulses later, D5-6 LD TX SH REG H is asserted and drives the output (pin 4) of E88 low. It is inverted and this positive-going transition clocks TX TOTAL TRANS DLY which clears it (the D input of this flip-flop is held low by EXIT/ENTER which remains cleared).

8. When TX TOTAL TRANS DLY is cleared, the low signal at its 1 output directly clears TX TOTAL TRANS. The high signal from TX TOTAL TRANS triggers the BCC STROBE one-shot which enables the BCC counter logic to allow transmission of the two BCC characters and subsequent shutdown of the TX BCC generator by inhibiting D9-5 SHIFT TX BCC H pulses.

TX BCC Counter and BCC Request Logic

The TX BCC counter and BCC request logic is shown in the upper right section of print D9-5. This logic generates a request signal (D9-5 BCC RQ L) when it is time to append a BCC to the data being transmitted. The counter is qualified to allow 1, 2 or 3 BCC characters to be appended. The qualification signals come from the M7817 module (BB option) or from the M7816 module (AB option).

The qualification logic is shown in Figure 4-62. The preset input of each counter flip-flop is connected to the output of a NAND gate. For flip-flop TX BCC CNTR A, the gate is E87 pin 1. For flip-flop TX BCC CNTR B, it is E87 pin 4. One input of each of these E87 gates is connected to the 1 output of one-shot BCC STROBE which is triggered when coming out of total transparency (AB option). The other input of each gate is controlled by a jumper on the M7816 (print D9-6) to control the number of BCC characters selected. Jumper W2 (signal D9-6 W2 H) is associated with TX BCC CNTR A and Jumper W1 (signal D9-6 W1 H) is associated with TX BCC CNTR B. Jumper selection of the number of BCC characters is used for the AB option. the output of each of the E87 gates is wire-ORed with a signal from the M7817 (BB option). The signals are: D8-4 TX BCC 5 L for TX BCC CNTR A and D8-4 TX BCC 4 L for TX BCC CNTR B. These signals are programmable and are controlled by bits 4 and 5 of the SEQ register. The truth table in Figure 4-62 also shows the signal states and jumper configurations for selecting the number of BCCs.



NOTE

*These signals are bits 5 and 4 of the SEQ register. They are inverted three times coming from the Unibus. SEQ bits 5 and 4 are shown below as they appear on the Unibus.

No. of BCCs	SEQ Bits	
	5	4
NONE	0	0
3	1	0
2	0	1
1	1	1

No. of BCCs	Jumpers		Signals		Wired-OR Output	
	W2	W1	W2	W1	W2	W1
NONE	IN	IN	L	L	H	H
3	OUT	IN	H	L	L	H
2	IN	OUT	L	H	H	L
1	OUT	OUT	H	H	L	L

Figure 4-62 Qualification Logic for TX BCC Counter

The wired-OR connection at the outputs of the E87 gates allows qualification of the TX BCC counter flip-flops by the M7817 module (BB option) using bits 4 and 5 of the SEQ register or by jumpers on the M7816 module (AB option) when coming out of total transparency.

The TX BCC NEXT FR flip-flop in the request logic provides a one character delay before asserting D9-5 BCC RQ L to ensure that the last character is included in the BCC accumulation. In cases that do not require the one character delay, the TX BCC NEXT FR flip-flop can be preset by the M7816 or M7817 module to assert D9-5 BCC RQ L. A similar wired-OR connection is used to generate the low signal required to preset the flip-flop. For the M7817 module, the preset signal is D8-4 TX BCC NEXT CHAR L. For the M7816 module it is the ANDing of D5-6 TX FAKE END (1) H and the positive pulse from the BCC STROBE one-shot at NAND gate E87 pin 10.

The following example assumes that the M7817 module is not installed and that transparency is controlled by the M7816 module. To describe the operation of the counter and request logic, assume that the counter flip-flops have been qualified to select two BCC characters. Qualification is made by the M7816 module: D9-6 W1 H is high (jumper W1 is out) and D9-6 W2 H is low (jumper W2 is in). Assume that the flip-flops start in the cleared state.

1. After qualification, TX BCC CNTR A is cleared and its D input is lo . TX BCC CNTR B is set and its D input is low. TX BCC NEXT FR is cleared and its D input is high.

2. When the TX bit counter on the M7813 module overflows, the carry pulse is buffered to become D5-6 BTXC L which is sent to pin 5 of inverter E91. It is inverted again by another E91 gate. The positive-going trailing edge of this pulse (E91 pin 12) clocks the TX BCC NEXT FR flip-flops and sets it.

3. The high from the 1 output of TX BCC NEXT FR goes to pin 5 of NAND gate E83. The other input (pin 4) is also high because TX BCC CNTR B is set. This asserts D9-5 BCC RQ L at the output of this gate. The clocking signal does not affect TX BCC CNTR A because gate E88 is disqualified by a high on its pin 9 input. This high signal is D5-6 BCC EN (1) L which comes from the BCC section of the SEND ENABLE flip-flop (M7813) which is cleared at present.

4. When D9-5 BCC RQ L is asserted, it is sent to the TX control logic on the M7813 module (print D5-5). It is inverted and puts a high on the D input of the BCC section of the SEND ENABLE flip-flop. The next overflow pulse from the TX bit counter sets the BCC SEND ENABLE flip-flop and asserts D5-6 BCC EN (1) L. This signal is sent to E88 pin 9 which allows subsequent overflow pulses to clock TX BCC CNTR A.

5. The first eight bits of the BCC are shifted out of the TX BCC generator and the TX bit counter overflows again. The TX BCC CNTR A flip-flop is clocked via E88 pin 10 which sets it. The TX BCC CNTR B and TX BCC NEXT FR flip-flops do not change state; therefore, D9-5 BCC RQ L remains asserted and the last eight bits of the BCC are shifted out of the TX BCC generator. The D input of TX BCC CNTR A is low.

6. When the last bit of the BCC is shifted out, the TX bit counter overflows again. Both TX BCC CNTR A and TX BCC CNTR B are cleared. Exclusive-OR gate E76 puts a low on the D input of TX BCC CNTR A so further clocking does not change its state. TX BCC NEXT FR is still set but its D input is low. The 0 outputs of TX BCC CNTR A and TX BCC CNTR B puts highs on pins 1 and 2 of E83 which drives its output low. In turn, this drives D9-5 BCC REQ L high.

7. Signal D9-5 BCC REQ L, which is high, is sent to the M7813 module and puts a low on the D input of the BCC section of the SEND ENABLE flip-flop. The next overflow pulse clears the BCC SEND ENABLE flip-flop and drives D5-6 BCC EN (1) L high which inhibits further clocking of TX BCC CNTR A and TX BCC CNTR B. The overflow pulse clears TX BCC NEXT FR.

8. All during this operation, the TX TOTAL TRANS flip-flop is cleared which puts a high on E89 pin 11. When TX BCC CNTR A and TX BCC CNTR B were cleared (step 6), E89 pin 9 went high. Signal D5-6 BCC EN (1) L goes to E89 pin 10 and when it goes high (step 7) the output of E89 goes low and inhibits the generation of D9-5 SHIFT TX BCC H pulses which turns off the TX BCC generator.

TX BCC Shift and Clear Logic

The TX BCC shift and clear logic is shown in the lower right section of drawing D-CS-M7816-0-1 (Rev E) sheet 7 which is designated D9-5.

One-shot BCC PRESET is triggered by the negative-going transition that occurs when TX ACTIVE is cleared. The actual signal is D5-6 TX ACTIVE (1) H to input pin 9 of BCC PRESET. When the one-shot is triggered, a 700 ns negative pulse from the 0 output directly clears the following flip-flops in the TX BCC control logic. The flip-flops are listed below:

- EXIT TX TRANS
- EXIT/ENTER
- TX TOTAL TRANS
- TX BCC CNTR A
- TX BCC CNTR B
- TX BCC NEXT FR

The CLEAR START one-shot clears the TX BCC generator prior to the accumulation of a BCC character to ensure that nothing is left over from the previous accumulation. The BCC EN PULSE one-shot converts the TX clock symmetrical squarewave signal to positive pulses to shift the TX BCC generator. These one-shots and associated logic are shown in Figure 4-63.

The CLEAR START one-shot is triggered when the output (pin 8) of E89 goes high. The three inputs to this gate respond to enabling of the BCC function in different ways.

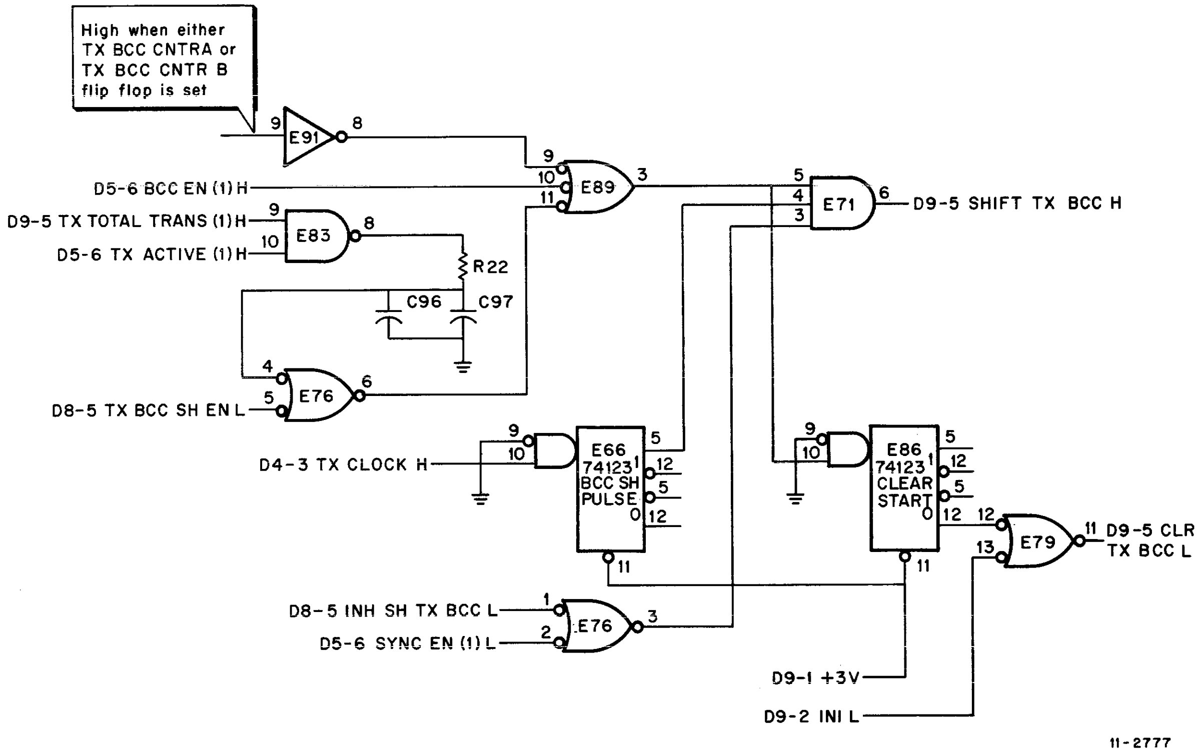


Figure 4-63 TX BCC Shift and Start/Clear Logic

Input pin 9 responds when either the TX BCC CNTR A or TX BCC CNTR B flip-flop is set. This occurs when the TX BCC control logic is in process of generating D9-5 BCC REQ L for the condition requiring 2 or 3 BCC characters. Input pin 10 responds when the BCC SEND ENABLE flip-flop on the M7813 module is set (D5-6 BCC EN (1) L asserted). This occurs when the BCC function is requested via the logic at the top of this print (D9-5) which is discussed later. This situation is appropriate when one BCC character is desired. Pin 11 responds in two ways. The first is when the M7817 module is installed and asserts D8-5 TX BCC SH EN L. This signal enters pin 11 of E89 via E76 pin 6. The second method is used when the M7817 module is not used. The fact that the TX TOTAL TRANS flip-flop is set and the fact that TX ACTIVE is set (D5-6 TX ACTIVE (1) H asserted) are ANDed at E83. The resulting low signal is delayed and sent to E89 pin 11 via E76 pin 6.

When the CLEAR START one-shot is triggered, the 50 ns negative pulse from its 0 output asserts D9-5 CLR TX BCC L at E79 pin 11. This signal can also be asserted by D9-2 INI L.

The signal that shifts the TX BCC generator is called D9-5 SHIFT TX BCC H. It is produced at the output (pin 6) of 3-input AND gate E71. Input pin 5 is high whenever the BCC function is selected, as described above. Pin 3 is high when two conditions are met at the inputs (pin 1 and 2) of E76. One condition is that the M7817 module is not inhibiting the BCC function; that is, D8-5 INH SH TX BCC L is high at E76 pin 1. If the M7817 module is not installed, this pin is held permanently high by +5 V via resistor R19.

The other condition is that the BCC, DLE, or data section of the SEND ENABLE flip-flop on the M7813 module (D5-6) is set. This fact is sensed by using the 0 output of the SYNC section of the SEND ENABLE flip-flop which must be cleared if either the BCC, DLE or data sections are set. In the case of BCC, the TX BCC shift signal is used to transmit the accumulated BCC character. In the case of DLE or data, the shift signal is necessary to accumulate the BCC character while DLEs or data are being transmitted. With this condition true, D5-6 SYNC EN (1) L is high to E76 pin 2. The third input (pin 4) of E71 is connected to the 1 output of the BCC SH PULSE one-shot. Whenever D4-3 TX CLOCK H goes high, the BCC SH PULSE one-shot is triggered. The 50 ns positive pulse from its 1 output is the third input to E71 which asserts D4-5 SHIFT TX BCC H.

4.6.7 RX BCC Control Logic

4.6.7.1 Functional Description – A simplified block diagram of the RX BCC control logic is shown in Figure 4-64. The logic performs several functions that are interrelated but can be described separately. The major functional areas are listed below in order of discussion.

1. RXP and RXS Save Logic. This logic looks ahead to see if the receiver is going to enter the total transparency mode. If it is, the logic allows total transparency to be turned on one transfer time sooner. The controlling factor is a signal that represents the state of REG/ERR CSR bit 14 (ENTER T).

2. RX Transparency Control and BCC Counter Logic. The section of the logic that controls total transparency is a function of the M7816 module only. It allows the receiver to enter and exit total transparency under control of REG/ERR CSR bits 14 (ENTER T) and 13 (EXIT T). When the receiver enters total transparency, this logic sends a signal to the RX BCC turn-on logic that starts the RX BCC generator. When the receiver exits total transparency, this logic enables the RX BCC counter and allows reception of the selected number of BCC characters before turning off the RX BCC generator. The BCC counter logic can be qualified by the M7816 module (jumpers) or the M7817 module (signals) to select 1, 2 or 3 BCC characters. This logic normally provides a one-character delay to ensure that the last data character is included in the BCC accumulation. It can be overridden in case the message contains an odd number of characters. This prevents a character time delay between receiving the last data character and the first BCC character.

3. RX BCC Turn-On Logic. This logic generates pulses that shift the RX BCC generator. It converts the RX clock signal to positive 50 ns pulses that perform the shifting operation. It is controlled by a signal from the RX transparency control and BCC counter logic (M7816) or a signal from the M7817 module.

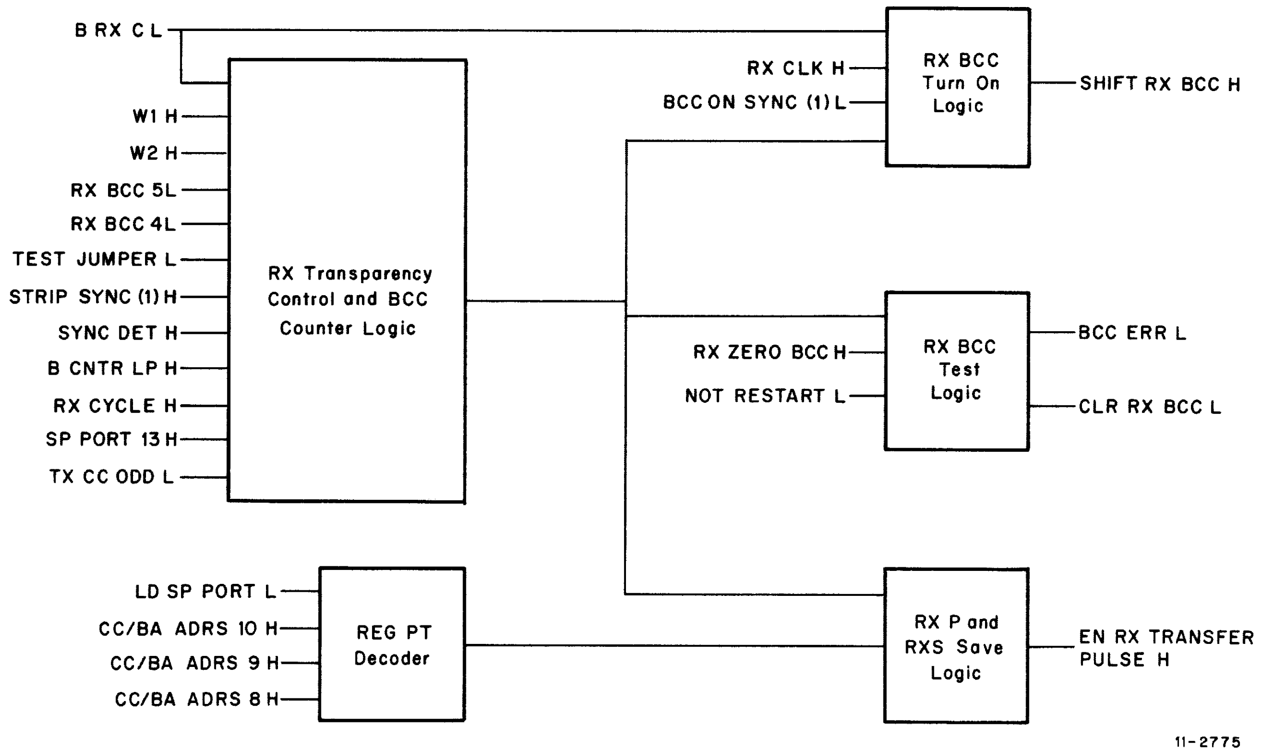


Figure 4-64 Block Diagram of RX BCC Control Logic

4. Test RX BCC Logic. This logic responds to a signal from the RX BCC generator after the data and BCC characters have been received. If an erroneous message has been received (RX BCC register not all 0s), the logic generates a signal that sets two error flags in the REG/ERR CSR: BCC ERR (bit 6) and ERR INTR (bit 15).

4.6.7.2 Detailed Logic Description –

RX P and RX S Save Logic

The RX P and RX S save logic is shown in the lower right section of drawing D-CS-M7816-0-1 (Rev E) sheet 8 which is designated D9-6.

This logic looks ahead to see if the receiver is going to enter total transparency mode (block transfers with AA plus AB option). If it is, this logic allows total transparency to be turned on one transfer time sooner. Without this logic, time would be lost because total transparency can only be entered at the time that the character count is first used (first transfer); and at this time, the character recognition circuitry is disabled, which inhibits entering total transparency.

Figure 4-65 shows the RX P/S save logic plus the logic that generates D5-2 DI PORT 14 L and D5-3 LD SP PORT L. Derivation of these signals is discussed because it is an important event in the sequence of activating the RX P/S save logic.

When REG/ERR CSR bit 14 (ENTER T) is set, the RX BCC control logic is conditioned to force the receiver into the total transparency mode. The RX P/S save logic examines signal D5-2 DI PORT 14 L which reflects the state of REG/ERR CSR bit 14.

Assume that the program sets bit 14 (ENTER T) and D4-6 EE 14 (1) H is asserted by the REG/ERR CSR (M7812 module). This signal is sent to input A3 of CC/BA DATA MUX 17, 16 (E47 on the M7813 module). This mux is

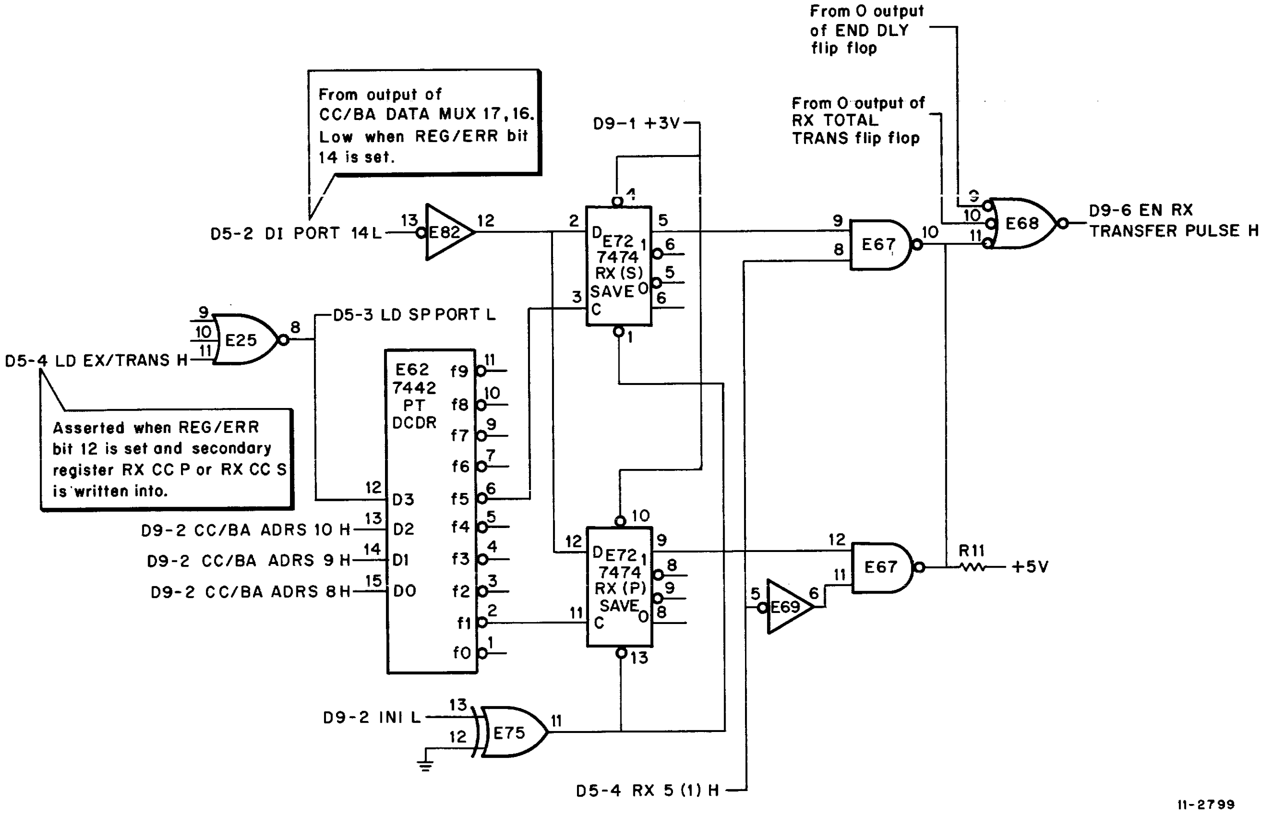

From O output of END DLY flip flop
From output of CC/BA DATA MUX 17,16. Low when REG/ERR bit 14 is set.
D9-1 +3V
From O output of RX TOTAL TRANS flip flop
D5-2 DI PORT 14L
E82
E72 7474 RX (S) SAVE
E67
E68
D9-6 EN RX TRANSFER PULSE H
D5-3 LD SP PORT L
E25
D5-4 LD EX/TRANS H
Asserted when REG/ERR bit 12 is set and secondary register RX CC P or RX CC S is written into.
E62 7442 PT DCDR
D9-2 CC/BA ADRS 10 H
D9-2 CC/BA ADRS 9 H
D9-2 CC/BA ADRS 8H
E72 7474 RX (P) SAVE
R11
+5V
E69
D9-2 INI L
E75
D5-4 RX 5 (1) H
11-2799

Figure 4-65 RXP and RXS Save Logic

enabled (D5-3 BA L asserted) when the DQ11 is not in the CC/BA cycle. This means that the mux select input (S0) is low (D5-3 CC/BA CYCLE H not asserted). The A input is selected, so D4-6 EE 14 (1) H is transformed to D5-2 DI PORT 14 L at output f1. This mux (E47) is a type 74S158 that provides an output that is the complement of the input. Signal D5-2 DI PORT 14 L is sent to the input (pin 13) of inverter E82 in the RX P/S save logic. It is also written into the CC/BA 17, 16 memory (E46) and read out as D5-2 SP PORT 14 H which is used in the TX BCC control logic.

In order to write into one of the eight secondary registers, it is necessary to select the register using memory address inputs A0, A1 and A2 and to put a low on the write (WR) input. In this discussion, only two secondary registers are involved: RX CC primary (1_8) and RX CC secondary (5_8). The address selection signals are D5-1 CC/BA ADRS 10 L, 9 L, and 8 L. The read/write control signal is D5-3 LD SP PORT L which is also the enabling signal for the PT decoder (E62) in the RX P/S save logic. It is generated as follows.

REG/ERR CSR bit 12 (14, 13 WRITE EN) must be set to allow the data in bits 13 (EXIT T) and 14 (ENTER T) of the same register to be written into the CC/BA memory. When bit 12 is set by the program and a DATO transaction is performed on a secondary register (address 76XXX6 asserted), D5-4 LD EXT/TRANS H is asserted by the register selection logic on the M7813 module. This signal is sent to NOR gate E25 (M7813 module, print D5-3) to generate a negative pulse at the output of E25 that is called D5-3 LD SP PORT L. When this signal goes low, it allows the data in REG/ERR CSR bit 14 or 13 to be written into bits 17 and 16, respectively, of the CC/BA memory (E46). It also enables decoder E62 in the RX P/S save logic. This decoder is used as a 3-wire, binary-to-octal decoder that is enabled when D5-3 LD SP PORT L is low. Binary coded inputs D2, D1 and D0 are used to select the outputs. These signals are D9-2 CC/BA ADRS 10 H, 9 H, and 8 H which are the inversions of D5-1 CC/BA ADRS 10 H, 9 H, and 8 H. The RX P/S save logic uses only two outputs: f1 and f5 which correspond to the RX CC P (1_8) and RX CC S (5_8) registers.

Assume that the receiver is running and it is using the RX CC primary register which is nearing overflow. The program sets REG/ERR CSR bits 14 (ENTER T) and 12 (14, 13 WRITE EN), selects the RX CC secondary register and loads a character count into it.

1. The following conditions exist:

   a. D5-2 DI PORT 14 L is asserted which puts a high on the D input of the RX (S) SAVE and RX (P) SAVE flip-flops.

   b. D5-3 LD SP PORT L is high because neither the RX CC primary or RX CC secondary registers are being loaded. As a result, the clock inputs to RX (S) SAVE and RX (P) SAVE are high because the E62 decoder is not enabled (input D3 is low).

   c. Both RX (S) SAVE and RX (P) SAVE are cleared which drives the output of both wire-ORed E67 gates high. This signal inhibits the presetting of the RX TOTAL TRANS flip-flop via gates E88 and E84. It also puts a high on pin 11 of E68. The other inputs (pins 9 and 10) of E68 are also high so the output of this gate (D9-6 DIS RX TRANSFER PULSE L) is high. This is a qualifying signal for the programmable character recognition logic (M7817 module) and the hard-wired character recognition logic (M7818 module). When D9-6 DIS RX TRANSFER PULSE L is high, the character recognition can be enabled at the next character count overflow.

   d. The receiver is using the RX CC primary register so D5-4 RX S (1) H is low. This puts a low on pin 8 of E67 and is inverted to put a high on bit 11 of the other E67 gate.

2. At overflow, the DONE logic (M7813 print D5-4) switches from the RX CC primary register to the RX CC secondary register. When the RX CC secondary register is written into, D5-3 LD SP PORT L goes low which enables output f5 (RX CC secondary register). When the D5-3 LD SP PORT L negative pulse times out, its positive-going trailing edge clocks the RX (S) SAVE flip-flop and sets it.

3. When the switch was made to the RX CC secondary register, D5-4 RX S (1) H goes high. This signal is sent to pin 8 of NAND gate E69. Its other input (pin 9) is high because RX (S) SAVE is set; therefore, its output (pin 10) goes low. This signal asserts D9-6 DIS TRANSFER PULSE L at E68 pin 8 which inhibits the character recognition logic (M7817 and M7818 modules).

4. Signal D9-6 DIS TRANSFER PULSE L goes to E88 pin 11. The other input (pin 10) is also low because the overflow pulse from the RX bit counter (M7813 print D5-7) caused the assertion of D5-7 TEST JUMPER MATCH L. The high output of E88 is sent to E84 pin 11. The other inputs (pins 9 and 10) of this gate are also high because D4-6 SYNC DET H is low. This drives the output of E84 low which directly sets the RX TOTAL TRANS flip-flop via its preset input. The low from the 0 output of RX TOTAL TRANS asserts D9-6 RX TOTAL TRANS (1) L.

The RX P/S SAVE logic has looked ahead and determined that the receiver wants to enter the total transparent mode. At the next character count overflow, when RX CC registers are switched, it inhibits character recognition and asserts the signals to put the receiver in total transparency.

REG/ERR CSR bit 13 (EXIT T) is set by the program to allow the receiver to exit from the total transparent mode and to enable character recognition.

At the next character count overflow (which assumed that the next CC contained an EXIT T character), D9-5 B CNTR LP H clocks the RX TOTAL TRANS flip-flop which clears it. The details of this operation are discussed in subsequent paragraphs.

RX Transparency Control and BCC Counter Logic

The RX transparency control and BCC counter logic is located in the left center section of print D9-6. It is also shown in Figure 4-66.

The transparency control logic allows the receiver to enter and exit the transparent text mode by using REG/ERR CSR bits 14 (ENTER T) and 13 (EXIT T). This mode of operation is termed total transparency to differentiate it from the control of transparent text provided by the M7817 module, when it is installed.

The BCC counter logic is conditioned by the transparency control logic (M7816 only) or by signals from the M7817 module.

The following example is used to discuss the operation of the logic. It is desired to force the receiver into the total transparent mode, accept the data, exit total transparency, accept two BCC characters and shut off the RX BCC generator. The example assumes that transparency control is provided by the M7816 module and that the message contains an even number of characters (odd count logic not enabled). The M7817 module is not installed.

1. The program sets REG/ERR CSR bit 14 (ENTER T) which is a requirement to force the receiver into the transparent text mode. When the RX CC primary or secondary register is loaded, the RXP/RXS save logic sends a low signal to E88 pin 11 (print D9-6). (The RXP/RXS save logic is discussed in a subsequent section.)

2. The receiver start up logic (print D5-7) asserts D5-7 TEST JUMPER MATCH L which is sent to the other input (pin 12) of E88. This drives the output of E88 high and this signal goes to pin 11 of 3-input NAND gate E84. The other inputs of this gate are also high via E64 pin 11 because D4-4 STRIP SYNC (1) H is low. This signal comes from bit 1 of the RX CSR and is not used when the transparency mode is used; that is, stripping of sync characters is inhibited in this mode; however, it is still used between total transparent blocks.

3. The output of E84 goes low and directly sets the RX TOTAL TRANS flip-flop. The 0 output of RX TOTAL TRANS causes the RX BCC turn-on logic to generate RX BCC shift pulses (D9-6 SHIFT RX BCC H) which starts the RX BCC generator. (The operation of the RX BCC turn-on logic is discussed in a subsequent section.)

   The receiver accepts the message and examines each bit via the RX BCC generator. When the end of data appears, the receiver is brought out of the transparent mode. The RX BCC counter logic is enabled to allow reception of the two BCC characters before the RX BCC generator is turned off. This sequence is described below.

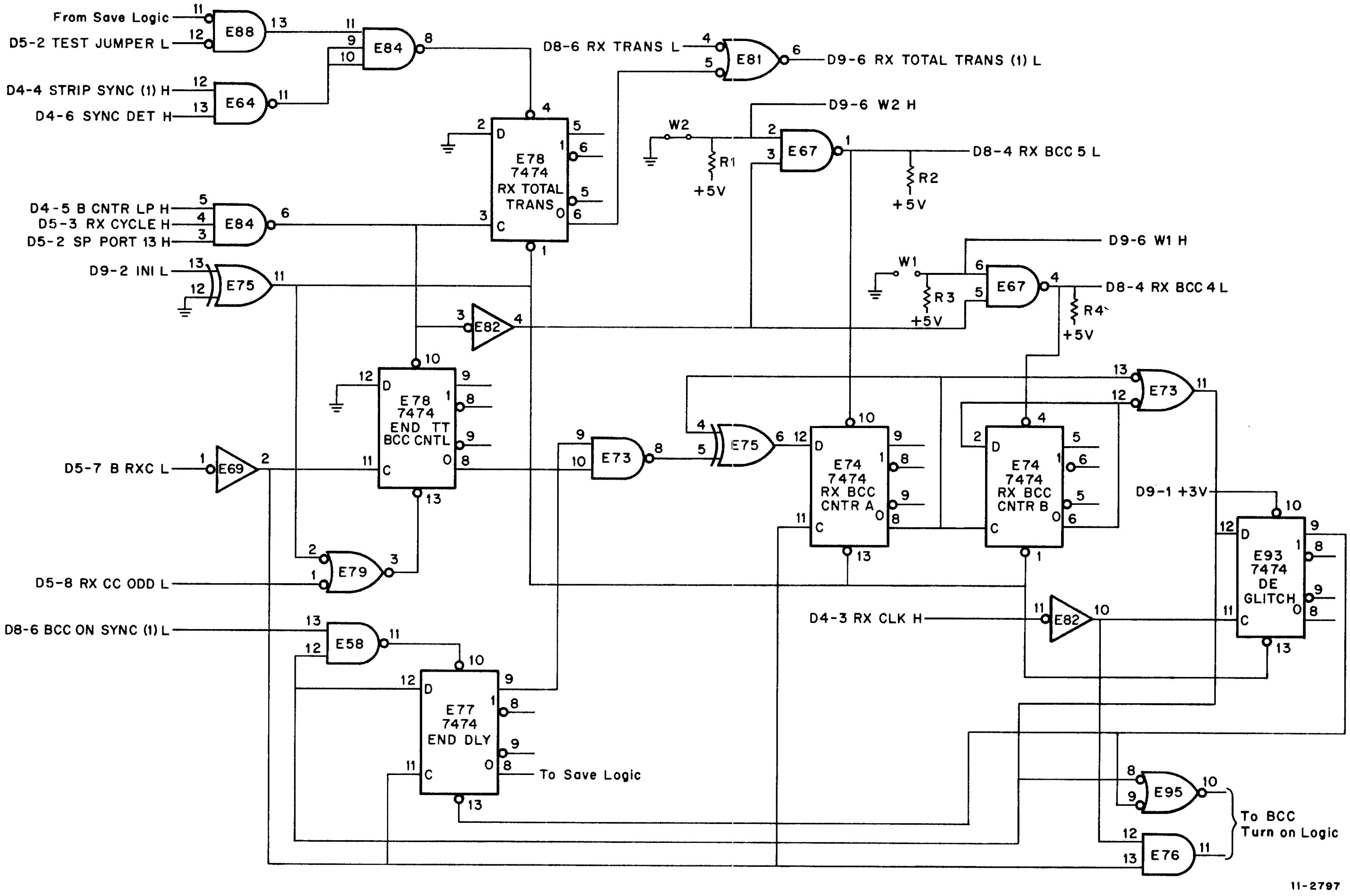


Figure 4-66 RX Transparency Control and BCC Counter Logic

4. The program sets REG/ERR CSR bit 13 (EXIT T) which is a requirement for allowing the receiver to exit the transparent text mode. When bit 13 is set and CC/BA is in the CC cycle signal D5-2 SP PORT 13 H is asserted and sent to pin 3 of 3-input NAND gate E84. The DQ11 is in the receive mode so D5-3 RX CYCLE H is asserted. This puts a high on the second input (pin 4) of E84. When the CC/BA counter is loaded after overflow, signal D9-5 B CNTR LP H is asserted. This is the third input to E84; and when it goes high, the output (pin 6) of E84 goes low.

5. Signal D9-5 B CNTR LP H is a pulse so the output of E84 is a negative pulse. The positive-going trailing edge at E84 pin 6 clocks the RX TOTAL TRANS flip-flop and clears it. The high signal from the 0 output of this flip-flop enables the two E67 gates associated with jumpers W1 and W2. The jumpers are set to select two BCC characters (W2 is in and W1 is out). The outputs of these gates are connected to the preset inputs of the BCC counter flip-flops. In this case, RX BCC CNTR A is not affected and remains cleared; RX BCC CNTR B is directly set. This sets up the counter logic to allow reception of two BCC characters.

6. The low signal from E84 pin 6 also directly sets the END TT BCC CONT L flip-flop. The END DLY flip-flop is set and remains in this state until cleared by the GLITCH flip-flop. The outputs of these flip-flops via gates E73 and E75 put a low on the D input of RX BCC CNTR A. This provides a one-character delay before starting the BCC character count.

7. When the RX bit counter overflows, signal D5-7 B RX C L is asserted and sent to pin 1 of inverter E69. This inverted signal clocks RX BCC CNTR A which does not change state because its D input is low. This represents the one-character delay. This signal also clocks END TT BCC CNTL which clears it. This in turn puts a high on the D input of RX BCC CNTR A.

8. The second RX bit counter overflow causes RX BCC CNTR A to be set. There is no change in state for RX BCC CNTR B (remains set).

9. The third RX bit counter overflow causes RX BCC CNTR A to be cleared. When this occurs, the 0 output of this flip-flop clocks RX BCC CNTR B and clears it. At this point, both BCC characters have been received. Both RX BCC CNTR A and RX BCC CNTR B are cleared. The high signal from the 0 output of each flip-flop is sent to an input of E73. With both flip-flops cleared, both inputs (pins 12 and 13) of E73 are high which drives the output (pin 11) low. This low signal goes to pin 8 of E95. The other input (pin 9) of E95 is also low via the DEGLITCH flip-flop. This drives the output (pin 10) of E95 high which is sent to the RX BCC turn on logic to inhibit D9-6 SHIFT RX BCC H and thus turn off the RX BCC generator.

The DEGLITCH flip-flop mentioned in step 9 latches the state of the signal at the output (pin 11) of E73. This signal is controlled by the states of RX BCC CNTR A and RX BCC CNTR B and is sent to the BCC start logic. The DEGLITCH flip-flop prevents transients that could occur when the counter flip-flops change state. A transient could arbitrarily change the state of the signal at E73 pin 11 and cause an unwanted triggering of the BCC start logic.

BCC Turn-On Logic

The BCC turn-on logic is located in the upper right section of print D9-6. It is also shown in Figure 4-67.

It turns on the RX BCC generator by asserting D9-6 SHIFT RX BCC H which shifts the generator. The BCC turn-on logic is controlled by the total transparency logic on the M7816 module or by the M7817 module, if the protocol option is installed. Once the receiver accepts the required number of BCC characters, the appropriate control logic (M7816 or M7817) shuts off the RX BCC generator by inhibiting the shift pulses.

Operation of the logic is explained by discussing two examples of BCC turn-on. One example assumes that only the M7816 module is used (total transparency control logic activates the BCC turn-on logic). The other example assumes that the protocol option (M7817) is installed and it generates the control signals to activate the BCC turn-on logic.

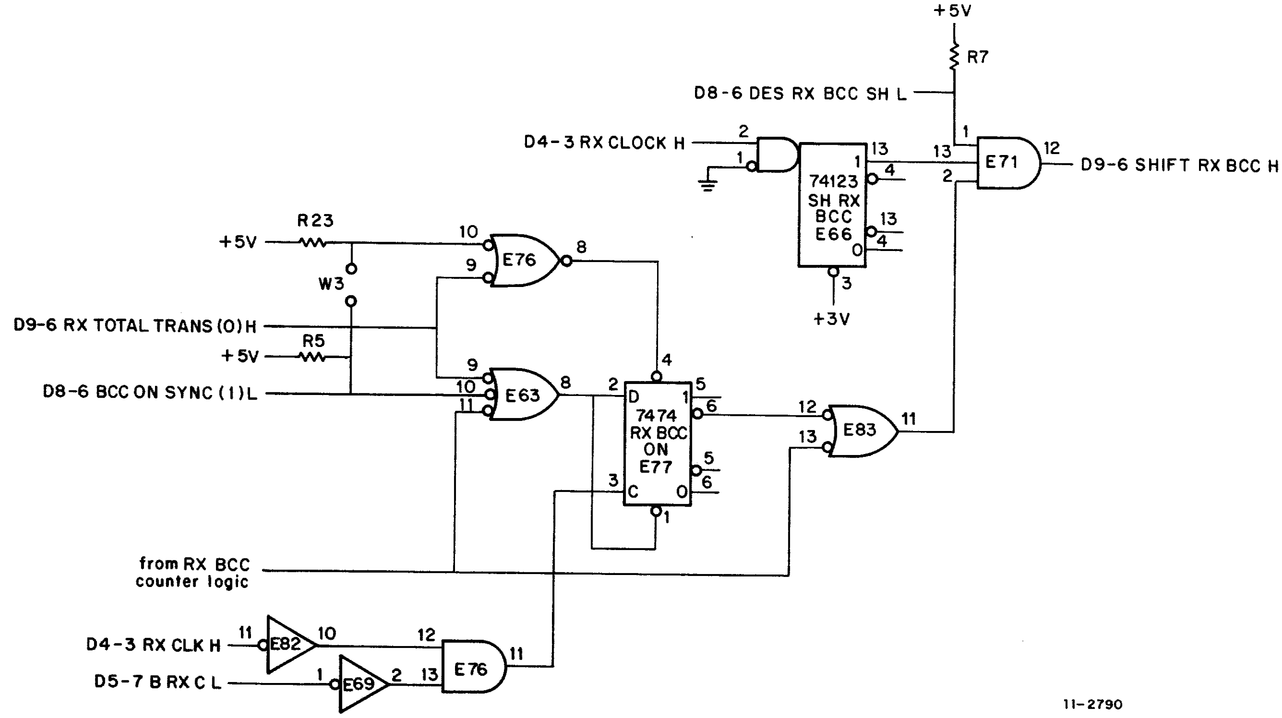


Figure 4-67 BCC Turn On Logic

Example 1
M7817 module not installed. The total transparency logic on the M7816 controls the operation of the BCC turn-on logic.

1. When entering RX total transparency, the RX TOTAL TRANS flip-flop is set. The low from its 0 output is sent to E76 pin 9 which directly sets the RX BCC ON flip-flop via its preset input.
2. The low from the 0 output of the RX BCC ON flip-flop is sent to pin 12 of E83 which drives its output high. (The other input of E83 is held high until the BCC counter logic is qualified.)
3. The high from E83 goes to pin 2 of 3-input AND gate E71. Pin 1 is held high by +5 V because the M7817 module is not installed and signal D8-6 DES RX BCC SH L is not present. The third input (pin 13) is pulsed high for approximately 50 ns by the 1 output of one-shot SH RX BCC that is triggered by the receiver clock (D4-3 RX CLOCK H). The positive output pulse at E71 pin 12 is D9-6 SHIFT RX BCC H which shifts the RX BCC generator.

As the transparent data is being received by the DQ11 and transferred to memory, it is examined by the RX BCC generator. When data ends, the DQ11 exits the total transparency mode and accepts two BCC characters. At this point, the RX BCC generator is shut off as follows.

4. When the DQ11 exits the total transparency mode, the RX BCC control logic clears the RX TOTAL TRANS flip-flop which puts a high on E63 pin 9. Pin 10 is high via +5 V because the M7817 module is not installed and signal D8-6 BCC ON SYNC (1) L is not present.
5. When the two BCC characters are received, the BCC counter logic drives the third input (pin 11) of E63 high. Now, with all inputs high, the output of E63 goes low and directly clears the RX BCC ON flip-flop. Both inputs of E83 are now high so its output goes low. This signal is sent to E71 and inhibits the RX BCC generator shift signal (D9-6 SHIFT RX BCC H is held low). The RX BCC generator is turned off.

Example 2
M7817 module installed. Protocol logic on the M7817 controls the operation of the BCC turn-on logic.

1. The M7817 module drives D8-6 DES RX BCC SH L high to produce a qualifying input (pin 1) for 3-input AND gate E71. At this time, pin 2 of E71 is low because both inputs (pins 12 and 13) to E83 are high, due to the fact that the RX BCC ON flip-flop and both BCC counter flip-flops are cleared.
2. The M7817 module asserts D8-6 BCC ON SYNC (1) L at E63 pin 10 which puts a high on the input of the RX BCC ON flip-flop (E63 pins 9 and 11 are high).
3. The clock input of RX BCC ON is connected to the output (pin 11) of AND gate E76. One input (pin 12) is connected to the inversion of D4-3 RX CLK H which is the receiver clock signal. The other input (pin 13) is connected to the inversion of D5-7 B RXC L which is the buffered overflow pulse from the RX bit counter (M7813 module print D5-7).
4. At the first overflow of the RX bit counter, D5-7 B RXC L is asserted and puts a high on E76 pin 13. When pin 12 goes high due to the RX clock signal, the output (pin 11) of E76 goes high and clocks the RX BCC ON flip-flop which sets it.
5. The low from the 0 output of RX BCC ON puts a high on E71 pin 2 via E83. Now, the positive pulses from one-shot SH RX BCC assert D9-6 SHIFT RX BCC H which shifts the RX BCC generator.

As noted in step 4, the RX BCC generator is started one character time after the receiver enters the BCC mode. This prevents the protocol character that caused BCC to start from being included in the BCC accumulation. Jumper W3 on the M7816 module determines whether or not the control character is included in the RX BCC accumulation. With the jumper out, the control character is not included. With the jumper in, the RX BCC ON flip-flop is preset via E76 pin 8 when D8-6 BCC ON SYNC (1) L is asserted. This turns on the RX BCC generator at the start of the first character, which is the control character.

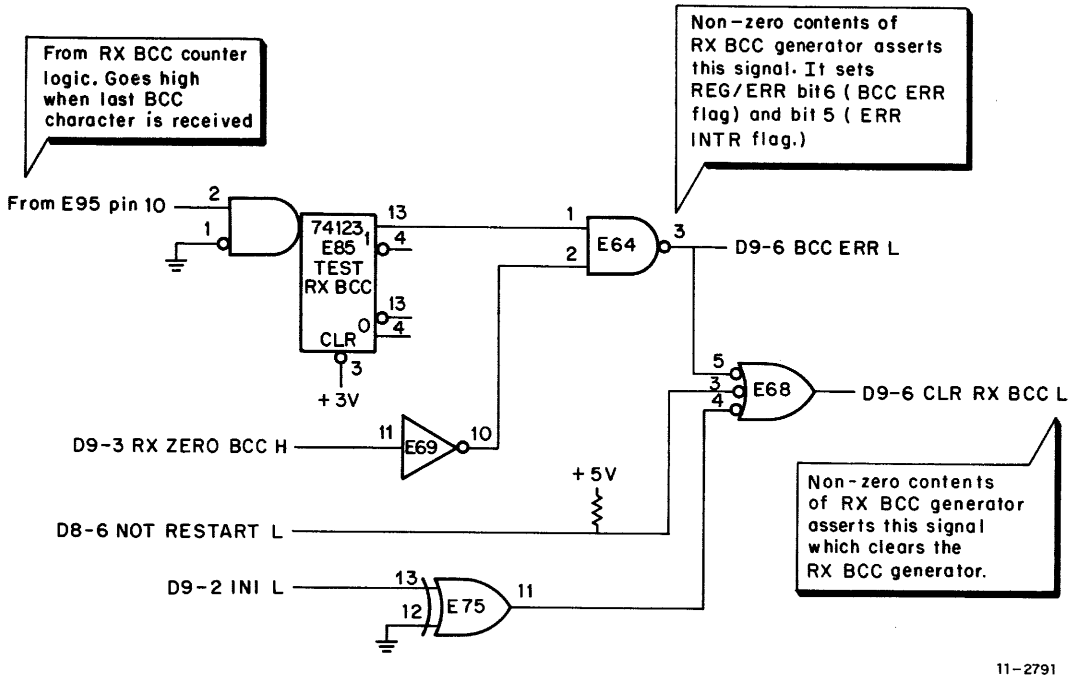
When the DQ11 exits the BCC mode and the two BCC characters have been received, the RX BCC generator is shut off in a manner similar to that discussed in Example 1, except that D8-6 BCC ON SYNC (1) L going high is the controlling factor.

Test RX BCC Logic
The test RX BCC logic is located in the right center section of print D9-6. It is also shown in Figure 4-68.

When the last BCC character is received, input pin 2 of the TEST RX BCC one-shot goes high which triggers it. The positive pulse from the 1 output of this one-shot goes to pin 1 of NAND gate E64. The other input (pin 2) of this gate is connected to the inversion of D9-3 RX ZERO BCC H via inverter E69. If the received message (including the BCC character) is received correctly, D9-3 RX ZERO BCC H goes high. In this case, D9-6 BCC ERR L is not asserted at the output (pin 3) of E64. If the received message contains an error, the contents of the RX BCC generator is not zero and D9-3 RX ZERO BCC H goes low which asserts D9-6 BCC ERR L at E64. This signal sets two error flags in the REG/ERR CSR: BCC ERR (bit 6) and ERR INTR (bit 15). These flags indicate that the received message contains one or more errors. The RX BCC generator only indicates the reception of an erroneous message. It cannot correct errors or even locate them. The message must be retransmitted.

If an erroneous message is received, the assertion of D9-6 BCC ERR L in turn asserts D9-6 CLR RX BCC L which clears the RX BCC generator. This is required to clear out the bits that contains 1s because an erroneous message has been received. This must be done before the next BCC accumulation is started.

Signal D9-6 CLR RX BCC L is also asserted by D9-2 INI L and D8-6 NOT RESTART L. The latter signal is generated by the M7817 module and its function is covered in the discussion of this module. This signal is not present when the M7817 module is not installed; therefore, +5 V is applied to pin 3 of E68 to inhibit this function.



From RX BCC counter logic. Goes high when last BCC character is received

Non-zero contents of RX BCC generator asserts this signal. It sets REG/ERR bit6 (BCC ERR flag) and bit 5 (ERR INTR flag.)

Non-zero contents of RX BCC generator asserts this signal which clears the RX BCC generator.

Figure 4-68 Test RX BCC Logic

4.7 M7817 MODULE (CHARACTER DETECT AND SEQUENCE CONTROL)

4.7.1 Introduction

The M7817 module is a hex-height, extended-length, module that contains several functionally separate logic circuits. They are listed below in the order of discussion.

1. Character Detect and Sequence Registers
2. Transmit and Receive Compare Logic
3. Character Detect Control Logic
4. Sequence Decoding Logic
5. Transmitter Protocol Control Logic
6. Receiver Protocol Control Logic

4.7.2 Character Detect and Sequence Registers

4.7.2.1 Functional Description – The character detect and sequence registers are 16 word by 16 bit, random access, semiconductor (TTL) memories that provide non-destructive readout.

With character recognition enabled, characters to be detected are written into the character detect memory by the program. The desired functions to be performed by the hardware are selected by setting the appropriate bits in the corresponding word of the sequence register.

The output of the receiver buffer register and the output of the transmitter shift hold register are compared with each word of the character detect memory in succession. When a received character (in RX buffer register) or a character to be transmitted (in TX shift hold register) matches any character in the character detect memory, a hardware control sequence is initiated in accordance with the bits set in the sequence register for the associated word.

The outputs of the character detect register go to Unibus drivers on this module so they can be read by the program. The outputs of the sequence register are read by sending them to the bus selectors on the M7816 module and then to the driver section of the bus transceivers. The data inputs to both memories come from the Unibus to receivers in the M7816 transceivers and then to buffers on this module.

The character detect register and sequence register use separate read/write control signals; they use common address select signals.

Figure 4-69 is a simplified block diagram showing only data flow for the character detect and sequence registers.

4.7.2.2 Detailed Logic Description – The circuit schematics for the character detect and sequence registers are contained in drawing D-CS-M7817-0-1 (Rev C) sheet 3, which is designated D8-1. A typical 4-bit section of the character detect and sequence register is shown in Figure 4-70.

In each case, 16 4-bit words are contained in a single TTL 64-bit read/write semiconductor memory (type 3101).

The 16 words are addressed by the 4-bit binary number sent to the address inputs (A0–A3) of the memories and are represented by signals D8-3 CHAR CNTR 1 (1) H, 2 (1) H, 4 (1) H, and 8 (1) H. These signals are generated by a counter and are common to all 3101 memories that make up the character detect and sequence registers. The counter increments through 16 states, overflows and continues incrementing. This provides continual sequential addressing of the character detect and sequence registers as long as the character detect logic keeps the counter active.

The enable (ENB) input of each 3101 is permanently connected to ground which holds it enabled. For a selected word, a write operation is performed when the write (WR) input is low and a read operation is performed when this input is high. A write operation places the input data into the selected word. In a read operation, the complement of the information that has been written into the selected word is non-destructively read out at the four outputs which are M0 (1)–M3 (1). The write input for the character detect register is D8-3. CM WE L and for the sequence register it is D8-3 SEQ WE L.

Both registers use common data inputs (D9-1 D0 H–D9-1 D15 H) which are buffered and inverted before being sent to the 3101 inputs. These signals come from the receiver section of the bus transceivers on the M7816 module. They are picked off the Unibus data lines and inverted by these receivers.

The outputs of the sequence register are sent to the bus selectors on the M7816 module where they can be read by the program.

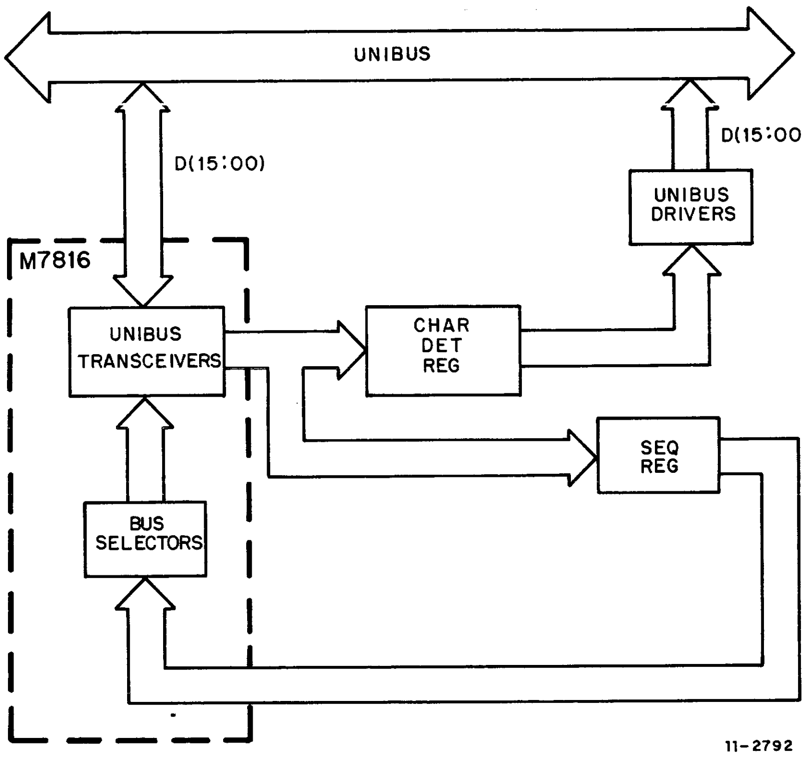


Figure 4-69 Data Flow for Character Detect and Sequence Registers

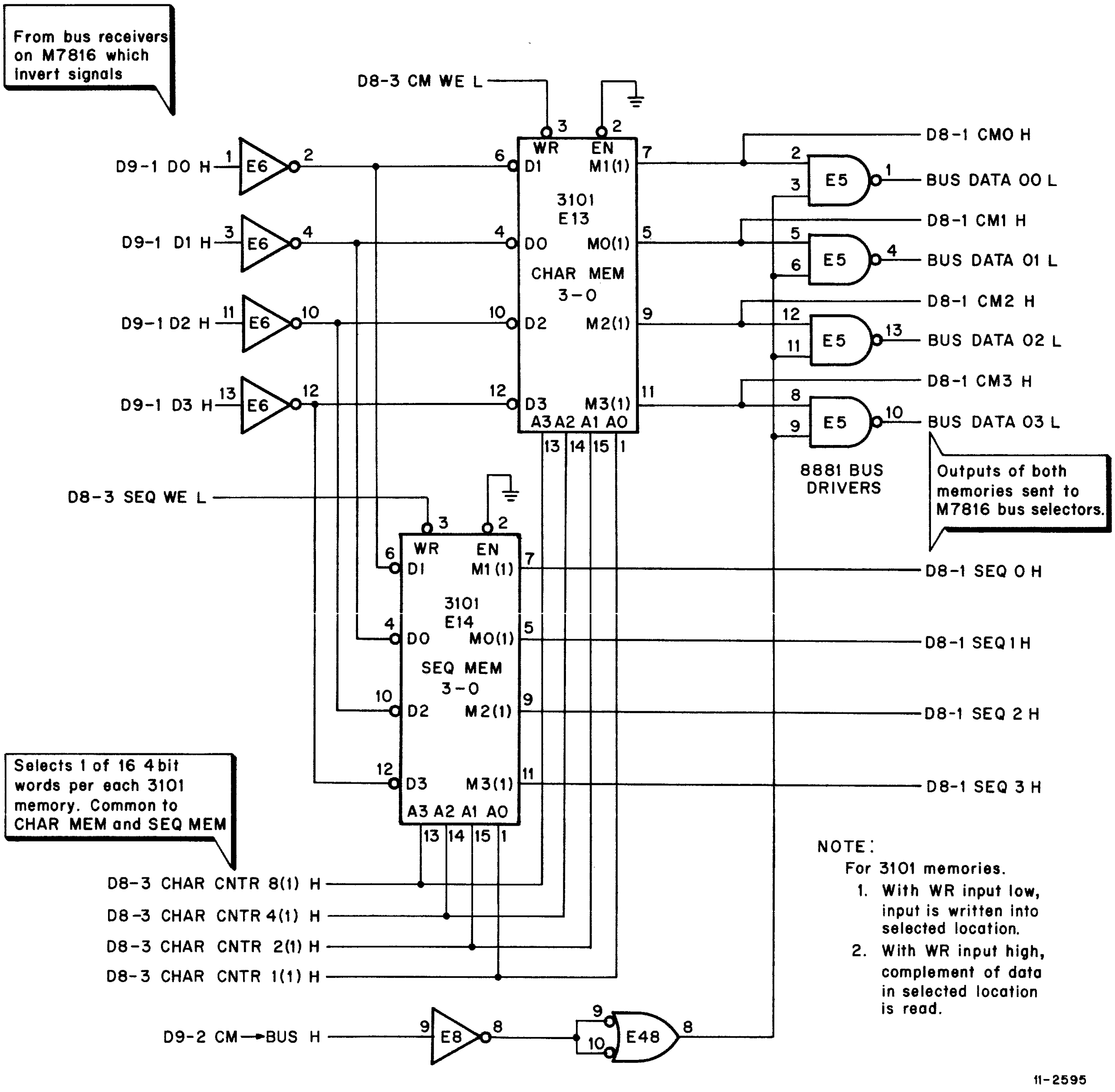


Figure 4-70 4-Bit Slice of Character Detect and Sequence Registers

The outputs of the character detect register are sent to type 8881 bus drivers. The enabling signal for the drivers is D9-2 CM → BUS H which comes from decoding logic on the M7816 module. This signal is double-inverted before being applied to the bus drivers.

4.7.3 Transmit and Receive Compare Logic

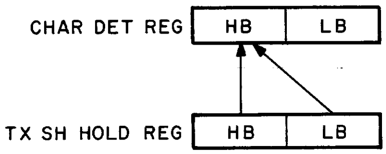
4.7.3.1 Functional Description – Each received character and character to be transmitted is compared with each word in the character detect memory. When character detection is enabled, only characters of 8 bits or less can be processed. Practically speaking, word matches are double-character matches.

In the receive mode, two simultaneous comparisons are made using the output of the receiver buffer. Each incoming character in the high byte of the RX buffer is compared to the high byte of the character detect word. Each RX buffer word is compared with the character detect word.

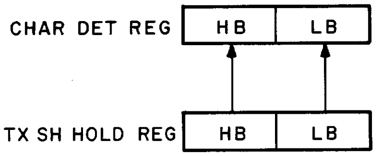
In the transmit mode, four simultaneous comparisons are made using the output of the TX shift hold register. This register is parallel-loaded on a word basis (double characters). The comparisons are listed below.

1. High byte with character detect high byte.
2. Low byte with character detect high byte.
3. Complete word with character detect word.
4. Saved word with character detect word. This consists of present low byte with character detect high byte and previous high byte with character detect low byte. This comparison is used to detect a double-character match that consists of the high byte of the previous word and the low byte of the current word. That is, it detects a successive double-character control sequence that is split between two words.

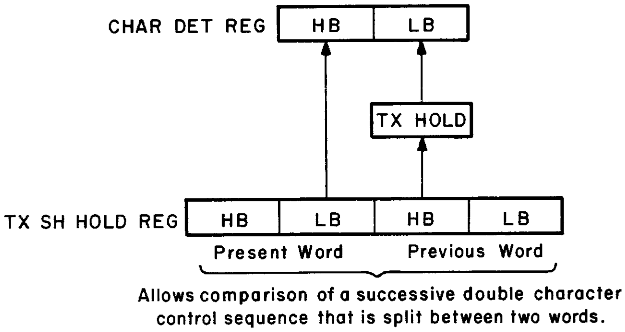
Figure 4-71 graphically illustrates the various comparisons.



Byte Comparisons



Word Comparison


CHAR DET REG
HB
LB
TX HOLD
TX SH HOLD REG
HB
LB
HB
LB
Present Word
Previous Word
Allows comparison of a successive double character control sequence that is split between two words.

Saved Word Comparison

Figure 4-71 Graphical Representation of RX and TX Character Comparisons

A simplified block diagram of the comparison logic is shown in Figure 4-72. Multiplexers are used to select the received characters and characters to be transmitted for comparison with the characters in the character detect register. Bit-by-bit comparisons are made in digital comparators whose outputs are wire-ORed to produce the desired output only if all bits match. A flip-flop register is used to store the TX high byte that is to be used in the saved word match.

The comparator output and two control signals (bits 14 and 15 of the SEQ register) are used in the comparator output logic to select the desired match configuration.

4.7.3.2 Detailed Description – The circuit schematic for the transmit and receive compare logic is shown in drawing D-CS-M7817-0-1 (Rev C) sheet 4, which is designated D8-2.

The 16 outputs of the receiver buffer (D4-5 RD 0 H–D4-5 RD 15 H) and the 16 outputs of the transmitter shift hold register (D4-5 TD 0 H–D4-5 TD 15 H) are sent to the inputs of 4 type 74157 quad 2-input multiplexers (E42, E46, E19 and E21) that are labeled RX/TX SEL. For each multiplexer, the strobe (STB) input is permanently connected to ground which keeps the multiplexer enabled. The select (S0) input is connected to D8-3 RX SEARCH H which is generated by the character detect logic. This signal is high when received character matches are desired; hence, it selects the received character inputs (B0–B3) of the multiplexers. When transmitted character matches are desired, this signal is low and it selects the transmitter inputs (A0–A3) of the multiplexer.

Each of the 16 multiplexer outputs goes to one input of an 8242 exclusive-NOR that is used as a digital comparator. The other input of each 8242 is connected to the same numbered bit in the character detect memory. The 8242 is an exclusive-NOR; hence, its output is high only when both inputs are the same. The output is a bare collector so multiple-bit comparisons can be made by a wire-ORed connection of several 8242s.

The low byte (bits 7–0) comparator outputs are wire-ORed and the high byte (bits 15–8) comparator outputs are wire-ORed and the resulting signals are sent to the match decoding logic.

The low byte of the transmitter shift hold register (D4-5 TD 0 H–D4-5 TD 7 H) is sent directly to eight wire-ORed 8242s to be compared with the high byte of the character detect register (D8-1 CM 8 H–D8-1 CM 15 H). The match signal is sent to the match decoding logic.

The high byte of the transmitter shift hold register (D4-5 TD 8 H–D4-5 TD 15 H) is sent to the TX hold register that is composed of two 74175 quad flip-flops (E41 and E47). This byte is held in the register to be used in the saved word comparison. The clock signal for the TX hold register is D5-6 LD TX SH REG H and is generated by the TX control logic on the M7813 module. The output of the TX hold register is compared with the low byte of the character detect register using eight wire-ORed 8242s. The match signal is sent to the match decoding logic.

The match decoding logic consists of four 74H11 3-input AND gates and one 7402 2-input NAND gate. The upper two AND gates (E20 pin 8 and E20 pin 12) produce byte-match signals. D8-2 LB MATCH H is generated at E20 pin 8 when a match is detected between the TX low byte and the character detect memory high byte. D8-2 HB MATCH H is generated at E20 pin 12 when a match is detected between the RX or TX high byte and the character detect high byte. However, two qualifying signals must be present at both gates before the match signals can be asserted at their outputs. One qualifying signal is D8-1 SEQ 15 H which is asserted when bit 15 of the sequence register is set by the program. The other qualifying signal is D8-2 DBL MATCH L from NOR gate E59 pin 4. This signal is asserted when a word or saved word match is detected and bit 14 of the sequence register is set by the program (D8-1 SEQ 14 H is asserted). Under these conditions, double-character detections take priority over single-character detections because when D8-2 DBL MATCH L is low it inhibits the generation of both D8-2 LB MATCH H and D8-2 HB MATCH H. This occurs even if D8-1 SEQ 15 H is asserted to qualify the logic for single-character (byte) detections.

The lower two AND gates (E20 pin 6 and E28 pin 6) produce word match signals. D8-2 WORD MATCH H is generated at E20 pin 6 when a match is detected between the RX or TX word (2 characters) and the character detect memory word. D8-2 SAVED WORD MATCH H is generated at E28 pin 6 when a match is detected between the TX saved word and the character detect memory word. These match signals cannot be asserted unless bit 15 of the sequence register is set by the program (D8-1 SEQ 15 H is asserted).

4.7.4 Character Detect Control Logic

4.7.4.1 Functional Description – A simplified block diagram of the character detect control logic is shown in Figure 4-73.

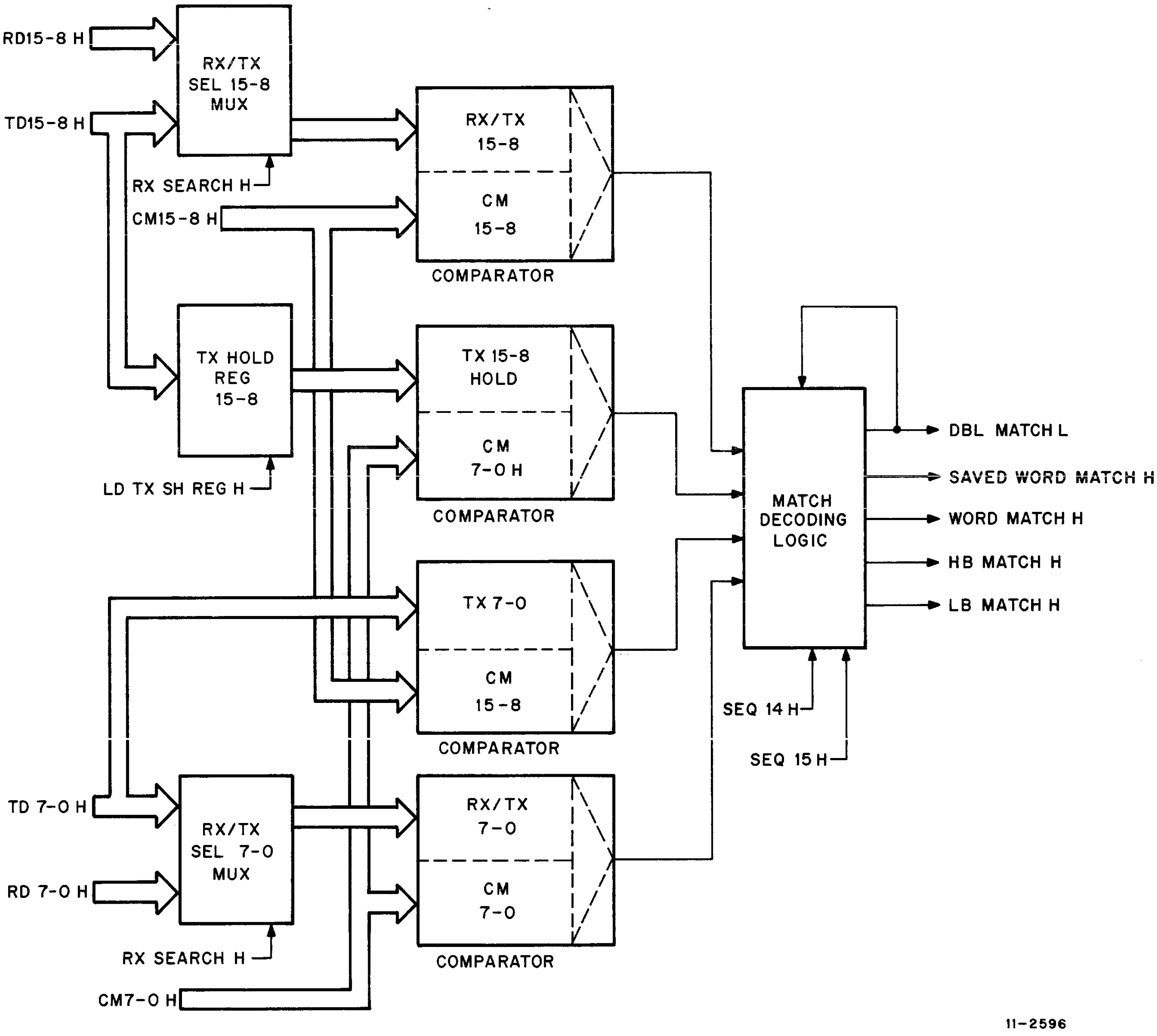


Figure 4-72 Block Diagram of Comparison Logic

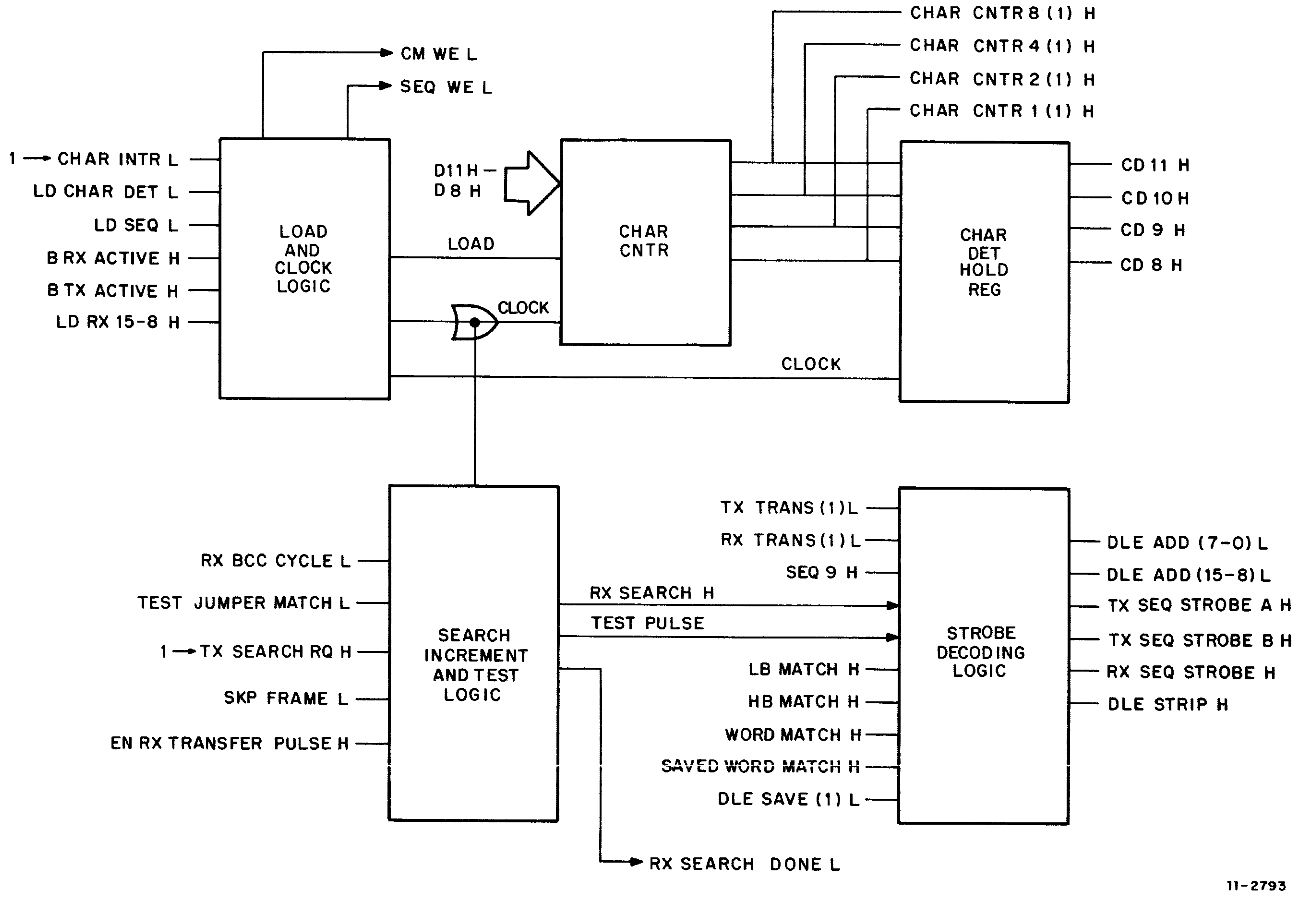


Figure 4-73 Block Diagram of Character Detect Control Logic

The search, increment and test logic responds to each received character and each character to be transmitted by causing the character detect register to step through all 16 words, starting at word 0 and ending at word 15. The stepping action is controlled by the character counter which is clocked by this logic. The counter outputs (D8-3 CHAR CNTR 1 (1) H, 2 (1) H, 4 (1) H and 8 (1) H are the address lines for the character detect memory. At each step, the character detect memory word is compared with the character being processed and a match signal is generated if they agree. The match signal is sent to the strobe decoding logic. After clocking (incrementing) the character counter, the search, increment and test logic generates a pulse that tests the strobe decoding logic. One of three strobe signals is generated depending on the type of match that occurred. The strobe signal is used to initiate a hardware control function, determined by the bit set in the corresponding word of the sequence register. When the character counter reaches a count of 15, the next clocking pulse causes the counter to overflow (return to count 0) which stops the search operation until another character (receive or transmit) enables the search, increment and test logic again.

Setting bit 12 or 13 of the sequence register allows the received character that caused the match to set the character flag bit (bit 15 of the RX CSR). In this case, the character counter output is also latched in the character detect hold register. The output of this register (D6-1 CD8 H–11 H) represents the address of the control word in the character detect memory at the time the match occurred. This address is sent to the bus selectors on the M7812 module where it can be read by the program.

The counter load logic is used to load the character counter with the address of the word in the character detect register or sequence register that requires access for a write or read operation. This logic is enabled only when both the receiver and transmitter are not active.

4.7.4.2 Detailed Logic Description – The circuit schematic for the character detect control logic is contained in drawing D-CS-M7817-0-1 (Rev C) sheet 5, which is designated D8-3.

Search, Increment and Control Logic

The search, increment and control logic is located in the left center portion of D8-3. This logic is explained by describing a typical operation.

1. Assume the following conditions

    a. CHAR CNTR is at count 0.

    b. The control characters have been loaded into the character detect register and the appropriate bits have been set in the sequence register.

    c. The search operation is to be initiated by a character to be transmitted.

2. During a TX NPR cycle, the TX control logic on the M7813 module generates D5-6 1 → TX SEARCH RQ H which clocks the TX SEARCH RQ flip-flop and sets it because its D input is held permanently high by E6 pin 6.

3. The low at the 0 output of TX SEARCH RQ is inverted by E73 pin 11 and puts a high on pin 10 of AND gate E65. The other input (pin 9) of this gate is high because the CARRY HOLD flip-flop is cleared. This puts a high (via E65 pin 8) on the D input of the CHAR SEARCH ACTIVE flip-flop, which at this point is cleared and therefore puts a high on pin 4 of E65.

4. The high at E73 pin 11 also triggers the INCR one-shot. The positive pulse from the 1 output of INCR drives E65 pin 6 high which clocks the TX/RX SEARCH flip-flop and sets it. The D input of this flip-flop was high because the RX SEARCH flip-flop is cleared. This positive pulse cannot get through E73 pin 3 to clock CHAR CNTR because this gate is disqualified by the low from the 1 output of CHAR SEARCH ACTIVE.

5. When TX/RX SEARCH is set, the high from its 1 output goes to E33 pin 9. The other input to this gate is also high because total transparency is not activated by the M7816 module (D9-5 TX TOTAL TRANS L not asserted). The output (pin 8) of E33 goes low and is inverted by E4. This signal is applied to the strobe decoding logic as a qualifying input.

6. The trailing edge of the negative pulse from the 0 output of the INCR one-shot triggers the TEST one-shot. The positive pulse from its 1 output is sent to all input gates in the strobe decoding logic as an enabling signal.

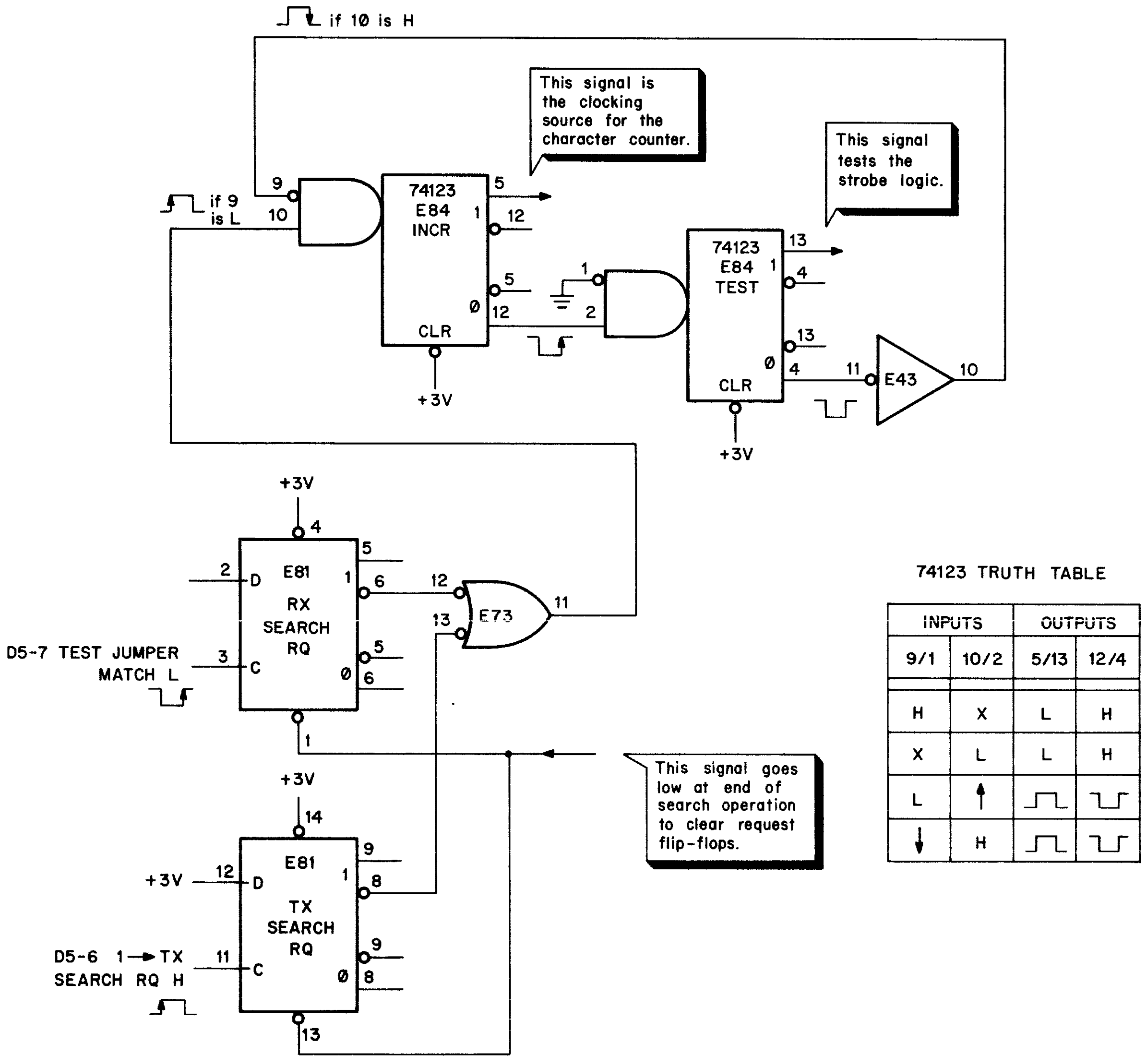
7. The negative pulse from the 0 output of TEST is inverted by E43 and clocks the CHAR SEARCH ACTIVE flip-flop and sets it. The high from the 1 output of this flip-flop goes to E73 pin 1. The high signal qualifies this gate so that subsequent positive pulses from the INCR flip-flop to the other input (pin 2) of E73 can clock CHAR CNTR.

8. The 0 output of TEST, which is inverted by E43, is fed back to the input (pin 9) of INCR which retriggers it. The INCR and TEST one-shots are connected as a multivibrator and alternately retrigger until the TX REQUEST flip-flop is cleared (Figure 4-74).

    SUMMARY OF OPERATION

    The TX search request initiates the increment/test operation which is to step through the character register to compare each of the 16 control words in the register with the character to be transmitted. The character counter starts at 0 so word 0 is to be examined first. The increment phase is inhibited and word 0 is tested for a match. The logic is now set up so that the next increment phase clocks the character counter to count 1 and then tests word 1 for a match.

9. When the INCR is retriggered, the positive pulse from its 1 output now gets through E73 pin 3 as a low and is sent to pin 1 of E33. The other input (pin 2) of this gate is high because D8-5 B TX ACTIVE H is asserted. This drives the output (pin 3) of E33 high which clocks CHAR CNTR and increments it to count 1. This selects word 1 in the character detect register for comparison with the character to be transmitted. The INCR one-shot retriggers TEST which sends the enabling signal to the strobe decoding logic.



74123 TRUTH TABLE

INPUTS		OUTPUTS	
9/1	10/2	5/13	12/4
H	X	L	H
X	L	L	H
L	↑	⊓	⊔
↓	H	⊓	⊔

Figure 4-74 Clock for Incrementing the Character Counter and Testing the Strobe Logic

10. Because of the INCR/TEST multivibrator, this process continues until the counter reaches a count of 15 which means that all 16 words (0–15) in the character detect register have been compared with the character to be transmitted.

11. When CHAR CNTR reaches the count of 15, a positive overflow pulse is produced at the CO output (pin 15). This signal puts a high on the D input of the CARRY HOLD flip-flop. The TEST pulse associated with the INCR pulse, which produced the count of 15, clocks CARRY HOLD and sets it. The low from the 0 output of CARRY HOLD puts a low on the D input of CHAR SEARCH ACTIVE.

12. The next INCR pulse clocks CHAR CNTR to the count of 0. It also clocks CARRY HOLD and clears it because the CO pulse has gone away and the D input of CARRY HOLD is low again. The associated TEST pulse clocks CHAR SEARCH ACTIVE and clears it. The low from the 1 output of this flip-flop disqualifies E73 and prevents further clocking of CHAR CNTR.

13. When CHAR SEARCH ACTIVE is cleared, its 0 output triggers the END SEARCH one-shot. The high pulse from the 1 output of END SEARCH drives the output (pin 8) of E73 low. This signal is buffered without a state change and directly clears TX SEARCH. Both inputs (pins 12 and 13) of E73 are now high so its output goes low which inhibits the INCR one-shot.

    SUMMARY OF OPERATION
    All 16 words in the character detect register have been compared with the character to be transmitted. The character counter is at count 0, the increment/test operation is not active and the TX search request is cleared. The search, increment and test logic is awaiting another TX or RX search request to start the sequence again.

Strobe Decoding Logic
The strobe decoding logic is located in the right center portion of D8-3.

This logic generates three strobe signals (one for RX and two for TX) that are used to enable the hardware operations chosen by the sequence register. The RX strobe signal is D8-3 RX SEQ STROBE H. TX strobe signal D8-3 TX SEQ STROBE A H is used for operations to be performed on the current character. TX strobe signal D8-3 TX SEQ STROBE B H is used for operations to be performed on the next character. Only one RX strobe signal is needed because received characters are looked at on a per-character basis. Characters to be transmitted are loaded as double characters so two strobe signals are required.

The strobe decoding logic also generates three other signals related to operations performed on DLE characters. If a DLE character is to be stripped, D8-3 DLE STRIP H is used. If a DLE character is to be added, two signals are available to choose the proper location of the DLE. If it is to be added in the low byte position, D8-3 DLE ADD (7–0) L is used; for the high byte position, D8-3 DLE ADD (15–8) L is used.

The enabling input to the strobe decoding logic is the high pulse from the TEST one-shot. This pulse tests or samples the strobe decoding logic each time the character detect register is stepped.

Several qualifying signals are sent to the strobe decoding logic.

1. Four match signals are sent from the RX/TX compare logic (D8-2). They represent low byte, high byte, word and saved word matches.

2. Bit 9 of the sequence register is used to control DLE strip/add. The signal is D8-1 SEQ 9 H and when it is asserted the DLE is stripped in receive mode and added to the specified byte in transmit mode.

3. Neither TX strobe signal can be generated when the DQ11 is in the transparent text mode which is indicated by the assertion of D8-5 TX TRANS (1) L.

4. When a TX search request has started the search, increment and test logic, a qualifying signal is sent to that portion of the strobe logic concerned with TX functions (TX strobes A and B and both DLE add functions).

5. When an RX search request has started the search, increment and test logic, a qualifying signal (D8-3 RX SEARCH H) is sent to that portion of the strobe logic concerned with the RX strobe signals. D8-3 RX SEARCH H cannot be asserted if the M7816 is in the total transparency mode. This condition is represented by D9-6 EN RX TRANSFER PULSE H which must be asserted to allow character detect operation in the receive mode.

6. The RX strobe signal can be generated when the DQ11 is in the transparent text mode which is indicated by the assertion of D8-5 RX TRANS (1) L, provided that D8-6 DLE SAVE (1) L is also asserted.

7. The DLE strip operation also depends on D8-5 RX TRANS (1) L being asserted along with the assertion of D8-6 DLE SAVE (1) L.

Character Counter and Character Detect Holding Register
The character counter (CHAR CNTR), character detect holding register (CHAR DET HOLD) and associated logic is located in the top section of D8-3. This logic is shown in Figure 4-75.

The character counter (E40) is a 74161 synchronous 4-bit counter. The four inputs (pins 3–6) come from the Unibus data lines via the receivers on the M7816 module. The signals are D9-1 D8 H–D9-1 D11 H. The outputs are:

D8-3 CHAR CNTR 9 (1) H	(MSB)
D8-3 CHAR CNTR 4 (1) H	
D8-3 CHAR CNTR 2 (1) H	
D8-3 CHAR CNTR 1 (1) H	(LSB)

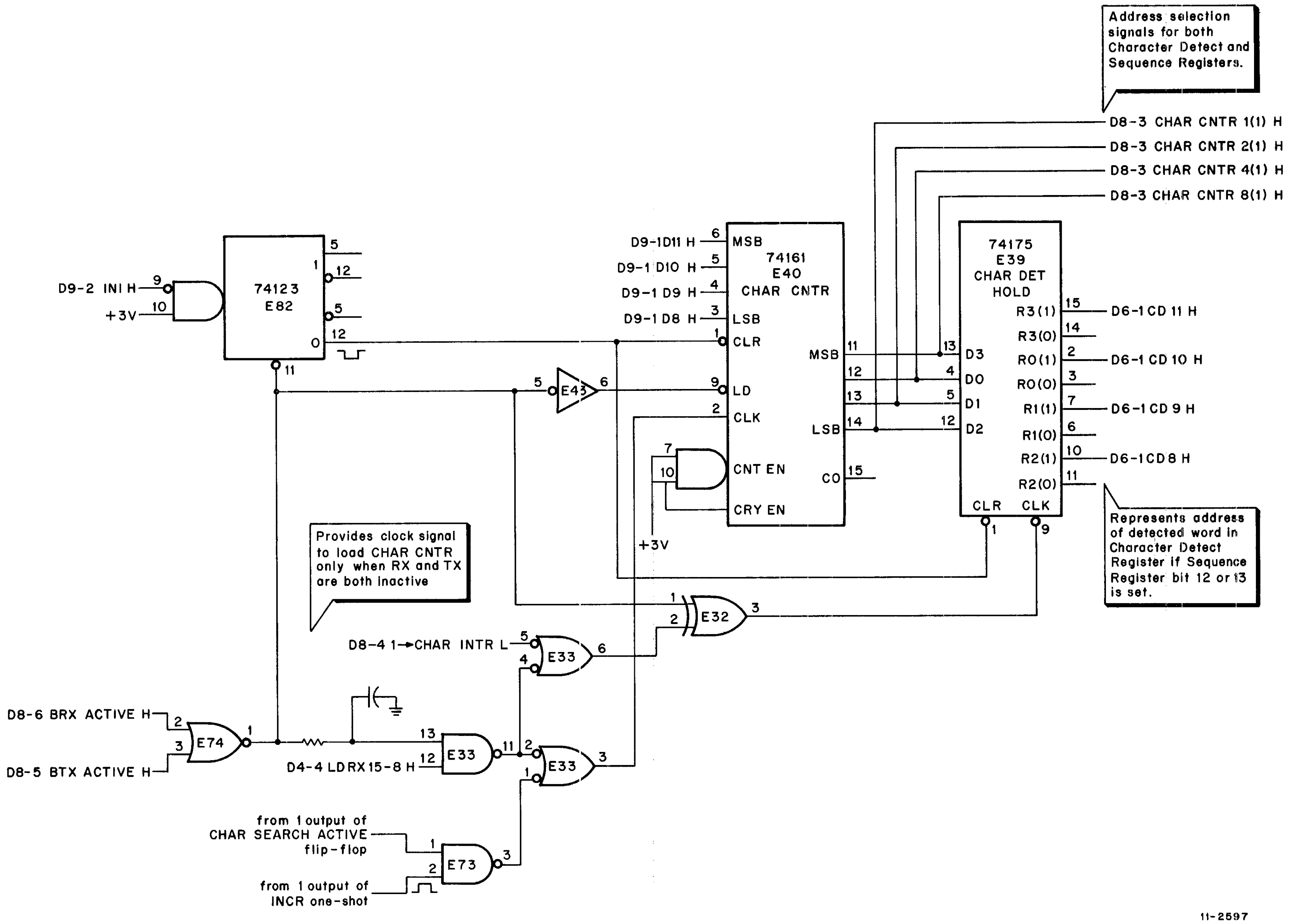
These signals are the address selection bits for the character detect and sequence registers. Both count enable inputs (CNT EN and CRY EN) are held permanently high so the counter is always enabled. A positive-going edge to the CLK input increments the counter. Placing a low on the load (LD) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear (CLR) input is connected to the 0 output of one-shot E82 which is triggered on the trailing edge of initialize signal D9-2 INI H. The clear input of the one-shot prevents triggering of E82 if either RX or TX is active.

When the search, increment and test logic is operating, CHAR CNTR is clocked by the INCR one-shot via gates E73 and E33 pin 3. As CHAR CNTR is incremented, its outputs are sent to the D inputs of flip-flop register CHAR DET HOLD. If the program desires to know the address of the control word in the character detect memory that resulted in a match, the output of CHAR CNTR can be latched into CHAR DET HOLD and read as bits 8–11 of the RX CSR via the bus selectors on the M7812 modules. This operation can be performed only if bit 12 or 13 (RX CHARACTER FLAG) of the sequence register is set. Under these conditions, the sequence decoding logic asserts D8-4 1 → CHAR INTR L which is sent to E33 pin 5. The other input of this gate is high because TX or RX is active. The output (pin 6) of E33 goes high and is sent to pin 2 of X-OR gate E32. The other input of this gate is low (via E74 pin 1) because TX or RX is active. This drives the output (pin 3) of E32 high and the positive transition clocks CHAR DET HOLD which latches the address of the detected character in the outputs of CHAR DET HOLD. The outputs of this register are wire-ORed with signals D6-1 CD 8 H–D6-1 CD 11 H on the M7818 module that represent character detect flags when only the basic DQ11 is used (Figure 4-76).

When search is inactive; that is, neither RX or TX is active, CHAR CNTR can be loaded. This operation is required to specify the address of the word in the character detect register or sequence register to be read or written into. Assume that a control character is to be written into a word of the character detect register. The following steps are required.

1. Address the REG/ERR register (76XXX4) and set the secondary register pointer (bits 8–11) to designate the character detect register (10_8).

2. Access the RX CSR (76XXX0) and write the address of the selected word into bits 8–11. The address is represented by signals D9-1 D 8 H–D9-1 D 11 H which are also sent to the input of CHAR CNTR. When the RX CSR is addressed, the M7812 module generates D4-4 LD RX 15–8 H which is sent to E33 pin 12. This drives the output (pin 11) of E33 low which is inverted by E33 pin 3 and sent to the clock input of CHAR CNTR.



Address selection signals for both Character Detect and Sequence Registers.

Represents address of detected word in Character Detect Register if Sequence Register bit 12 or 13 is set.

Provides clock signal to load CHAR CNTR only when RX and TX are both inactive

Figure 4-75 Clocking and Loading Logic for the Character Counter and Holding Register

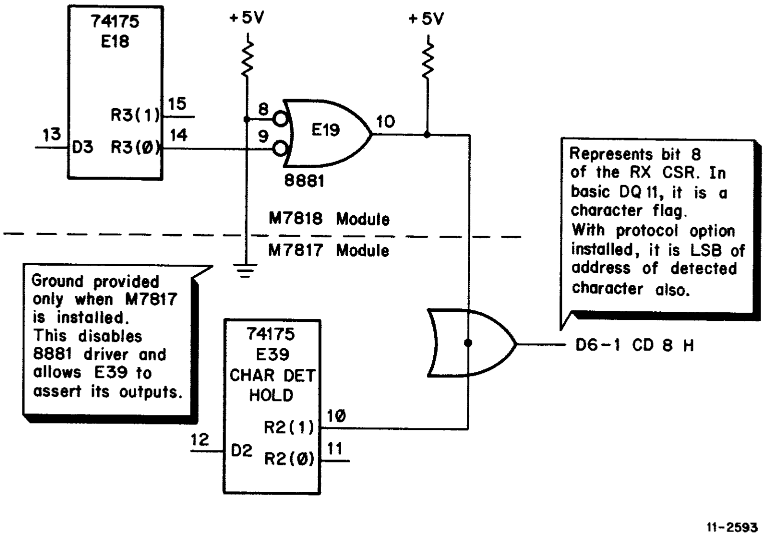

74175
E18
R3(1)
15
13
D3 R3(0)
14
+5V
+5V
8
9
E19
10
8881
M7818 Module
M7817 Module
Ground provided only when M7817 is installed. This disables 8881 driver and allows E39 to assert its outputs.
74175
E39
CHAR DET
HOLD
R2(1)
10
12
D2 R2(0)
11
Represents bit 8 of the RX CSR. In basic DQ11, it is a character flag. With protocol option installed, it is LSB of address of detected character also.
D6-1 CD 8 H
11-2593

Figure 4-76 One Bit of the Character Detect Flags/CD Address

3. The load (LD) input of CHAR CNTR is low because RX and TX are both inactive. When CHAR CNTR is clocked, it is loaded with the address of the word in the character detect register into which the control character is to be written. This address appears at the output of CHAR CNTR as D8-3 CHAR CNTR 8 (1) H, 4 (1) H, 2 (1) H, and 1 (1) H which are sent to the address selection inputs of the character detect register.

4. With the secondary register pointer bits set for the character detect register (10_8), address 76XXX6 is asserted to gain access to the character detect register. This results in the assertion of D9-6 LD CHAR DET L (via some decoding logic on M7813 print D5-4). This signal is inverted by E43 pin 2 and is sent to E60 pin 1. The other input (pin 2) of this gate is high because RX and TX are inactive. This drives the output (pin 3) of E60 low which asserts D8-3 CM WE L. This signal is sent to the write (WR) input of the character detect memory. When it is low, a write operation is performed; therefore, the control word is written into the selected address of the character detect register.

A similar procedure is used to write into the sequence memory using its octal designation (14_8) and write signal D8-3 SEQ WE L. The octal designation is determined by the secondary register pointer (bits 8–11) in the REG/ERR register.

4.7.5 Sequence Decoding Logic

4.7.5.1 Functional Description – Primarily, the sequence decoding logic examines the outputs of the sequence register to generate control signals that are used to implement hardware operations. The basic enabling signals are the RX and TX strobe signals. All but three bits (9, 14 and 15) of the sequence register are decoded in this logic. Bit 9 is used in the character detect control logic (D8-3) and bits 14 and 15 are used in the TX/RX compare logic (D8-2).

4.7.5.2 Detailed Logic Description – The circuit schematic for the sequence decoding logic is contained in drawing D-CS-M7817-0-1 (Rev C) sheet 6, which is designated D8-4.

In most cases, the decoding is done simply by ANDing a signal from the sequence register with the appropriate strobe signal.

For example, bit 3 of the sequence register is used to clear and start the BCC logic during receive or transmit operations. Signal D8-1 SEQ 3 H from the sequence register is sent as one input to three 2-input NAND gates. This signal is high when the bit is set which means that the BCC generator is to be cleared and started. The other input of each gate is connected to the appropriate strobe signal. If bit 3 is set and a match is detected, the resulting strobe pulse enables the gate and generates the hardware control signal.

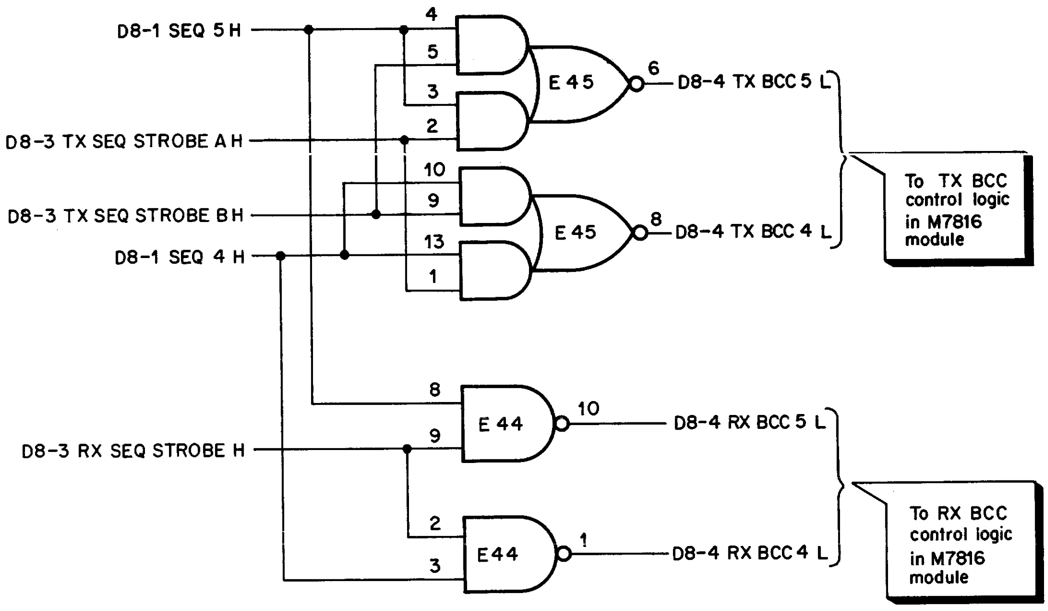
Specifically, D8-4 RX BCC ON L is generated at E54 pin 8 when D8-3 RX SEQ STROBE H is asserted; D8-4 TX BCC ON L is generated at E54 pin 6 when D8-3 TX SEQ STROBE A H is asserted, and D8-4 TX BCC ON NEXT FRAME L is generated at E54 pin 3 when D8-3 TX SEQ STROBE B H is asserted.

Most of the decoding is as simple as the example described above. The resulting control signals are appropriately named; however, reference to the sequence register bit assignments in Chapter 3 provides more information concerning the control functions.

Two sections of this logic require additional discussion which follows.

Selection of Number of BCC Characters

Sequence register bits 4 and 5 determine the number of BCC characters to be tested (receive mode) or appended (transmit mode) following the control character. This logic and BCC selection table are shown in Figure 4-77. Signals D8-4 RX BCC 5 L (E44 pin 10) and D8-4 RX BCC 4 L (E44 pin 1) are generated as a function of the state of D8-1 SEQ 5 H and D8-1 SEQ 4 H, respectively, plus the assertion of D8-3 RX SEQ STROBE H. These signals (D8-4 RX BCC 5 L and 4 L) are sent to the RX BCC control logic (D9-6) in the M7816 module. The associated signals for the TX mode (D8-4 TX BCC 5 L and D8-4 TX BCC 4 L) require more complex decoding because two TX strobe signals are used. Signal D8-3 TX SEQ STROBE A H is asserted if the hardware operation is to be performed on the current character. Signal D8-3 TX SEQ STROBE B H is asserted if the hardware operation is to be performed on the next character. The decoding is accomplished by using two 7450 2-wide 2-input AND-OR-INVERT gates (E45). The decoded outputs (D8-4 TX BCC 5 L and D8-4 TX BCC 4 L) are sent to the TX BCC control logic (D9-5) in the M7816 module.



Seq Reg Bit 5	Seq Reg Bit 4	Number of BCC Characters
0	0	None
1	0	1
0	1	2
1	1	3

11-2609

Figure 4-77 Logic for Selection of Number of BCC Characters

Character Detect Interrupt

With the M7817 installed, programmable character detection is used and the hard-wired three-character detection logic in the M7818 module is disabled. When a control character is detected and it is desired to set the character detect flag (RX CSR bit 15), signal D6-1 1 → CHAR INTR L is generated and sent to the preset input of the flip-flop that represents RX CSR bit 15 on the M7812 module (print D4-4). As a prerequisite, sequence register bit 12 or 13 must be set; that is, D8-1 SEQ 12 H or D8-1 SEQ 13 H must be asserted. This is the same signal that is generated as the result of a match when the hard-wired character detect logic is used (M7818 in and M7817 out). To accommodate this situation, a wired-OR connection is used for this signal (Figure 4-78).

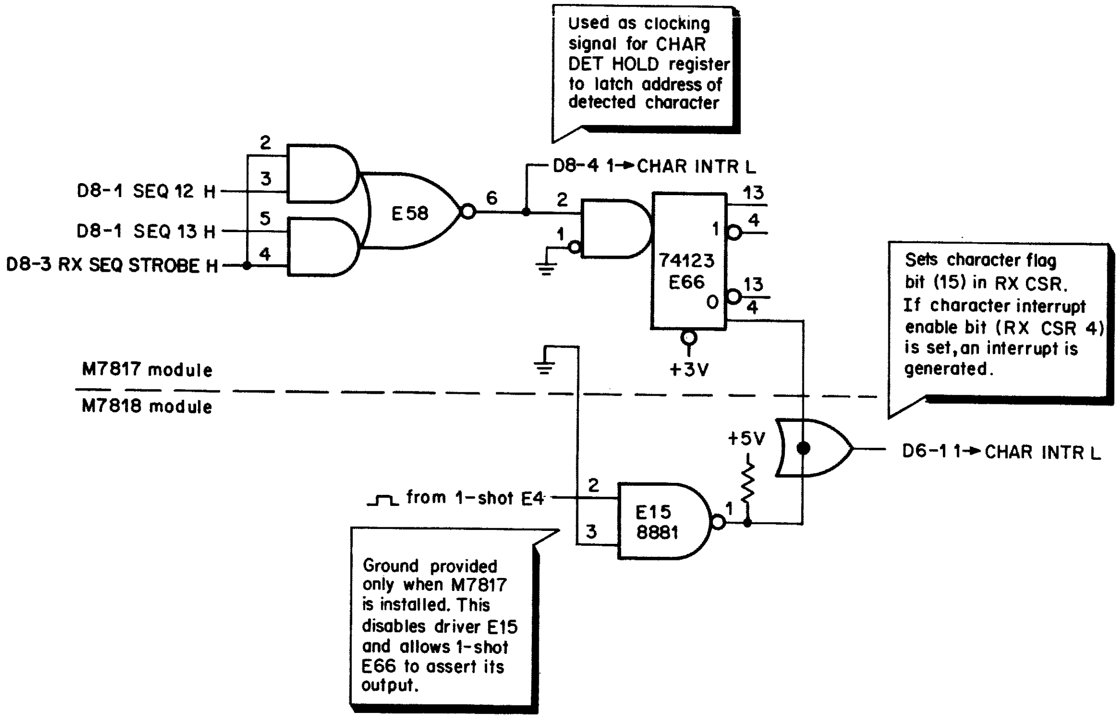
If the program has set the character interrupt enable bit (RX CSR bit 4), an interrupt is generated as a result of setting the character detect flag (RX CSR bit 15).

4.7.6 Transmitter Protocol Control Logic

4.7.6.1 Functional Description – A simplified block diagram of the transmitter protocol control logic is shown in Figure 4-79. The logic performs several functions that can be discussed separately. The major functional areas are listed below in order of discussion.

DLE Logic

The DLE logic provides a register to store the low byte output of the character detect memory when the memory being loaded and the corresponding word in the sequence register has bit 9 set. Bit 9 is the RX/TX DLE STRIP/ADD function and when it is set the control word being loaded in the associated word of the character detect memory represents a DLE character. This stored DLE is used when a DLE is to be transmitted. It is also compared with the received character for fast detection to ensure DLE deletion from the RX BCC accumulation during transparent text operation.



Used as clocking signal for CHAR DET HOLD register to latch address of detected character

Sets character flag bit (15) in RX CSR. If character interrupt enable bit (RX CSR 4) is set, an interrupt is generated.

Ground provided only when M7817 is installed. This disables driver E15 and allows 1-shot E66 to assert its output.

Figure 4-78 Character Detect Interrupt Logic

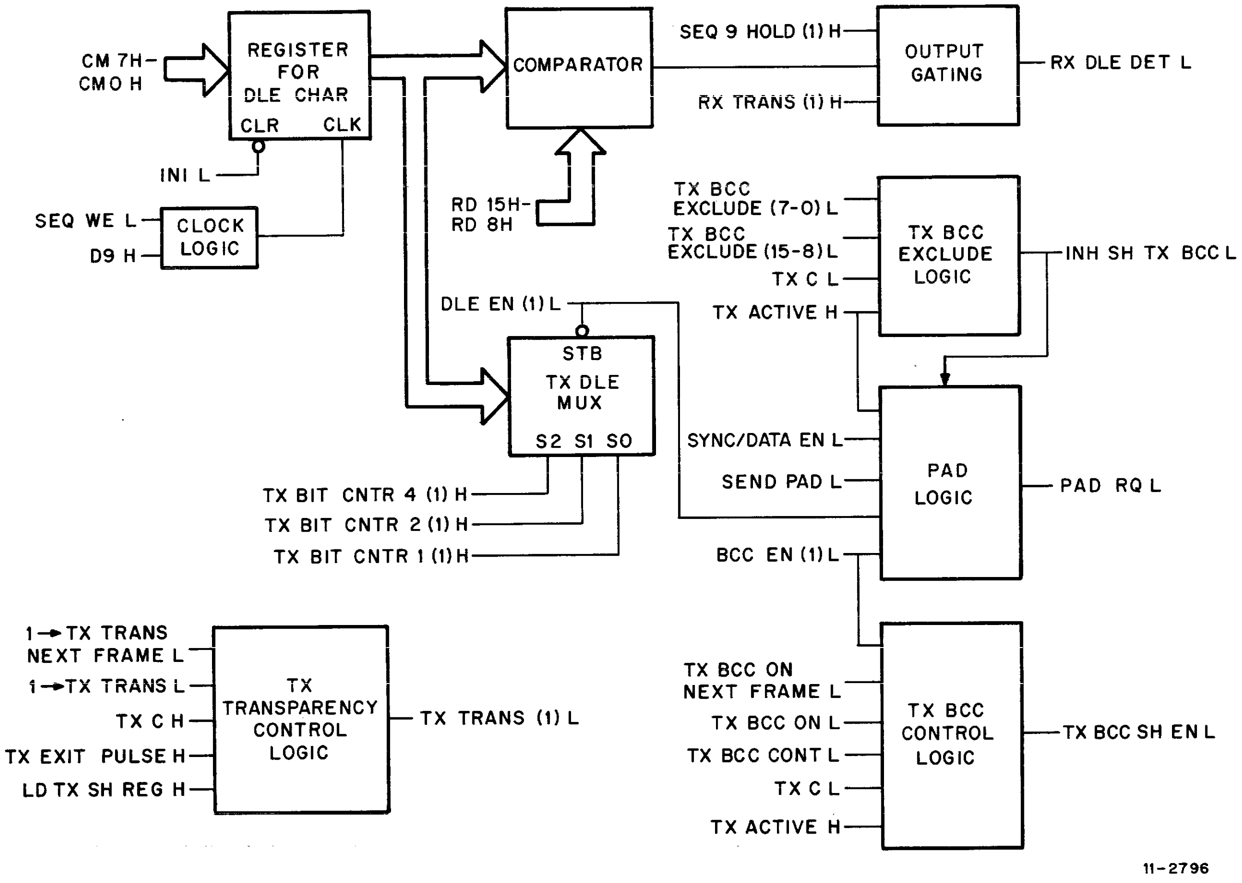


Figure 4-79 Block Diagram of Transmitter Protocol Control Logic

BCC EXCLUDE Logic
This logic allows exclusion of a received character or a character to be transmitted from the BCC accumulation when not in the transparent text mode. This function is controlled by bit 11 (RX/TX BCC EXCLUDE) of the sequence register. Exclusion can be on the next character to be transmitted or on the one following.

PAD Logic
This logic allows insertion of a PAD character following the last character to be transmitted. A jumper allows selection of one or two PAD characters.

TX Transparency Control Logic
This logic allows entry into transparent text on the next character to be transmitted or on the one following. It is tied into the DLE add logic to allow transmission of a DLE character before exiting transparency.

TX BCC Control Logic
Because of protocol rules, this logic excludes the first TX BCC start-up control character from the TX BCC accumulation. The next TX BCC start-up control character within this message is included in the BCC accumulation. It can be omitted only by using the BCC exclude logic.

4.7.6.2 Detailed Logic Description – The circuit schematic for the transmitter protocol control logic is contained in drawing D-CS-M7817-0-1 (Rev C) sheet 7, which is designated D8-5.

DLE Logic
Adding a DLE character to the message being transmitted is a function provided by the TX protocol control logic. In order to perform this function, the hardware must be able to recognize a DLE. The control word representing a DLE is located only in the character detect memory and cannot

be retrieved for use by this logic. It is obtained by latching the low byte output of the character detect memory in a register (E35 and E37) when this memory is loaded and the corresponding word in the sequence memory has bit 9 set. This bit (RX/TX DLE STRIP/ADD) is used to strip (receive mode) or add (transmit mode) a DLE character. Both the character detect and sequence memories use common address lines, so when bit 9 is set in a particular word in the sequence memory, the control word representing a DLE character is being loaded into the associated word of the character detect memory.

Specifically, when sequence register bit 9 (via the bus receiver on the M7816 module) is set, D9-1 D9 H is asserted and sent to the D input of the SEQ 9 HOLD flip-flop (Figure 4-79). When the character detect register is loaded (written into), D8-3 SEQ WE L goes low and is inverted by E80. The positive-going transition at the output (pin 12) of E80 clocks SEQ 9 HOLD and sets it. The 0 output of this flip-flop is fed back to its preset input (pin 10) to latch the flip-flop in this set state.

The inversion of D8-3 SEQ WE L is ANDed with D9-1 D9 H at AND gate E88. The output (pin 8) of E88 goes high and clocks 74175 flip-flops E35 and E37 (DLE 7-1 and DLE 3-0) which stores the contents of the low byte of the character detect register (D8-1 CM 0 H–D8-1 CM 8 H). The 8-bit register composed of DLE 7-4 and DLE 3-0 now contains the control word that represents the DLE character.

If a DLE is to be added to the transmitted message, the character detect control logic (print D8-3) asserts D8-3 DLE ADD (7-0) L or D8-3 DLE ADD (15-8) L which control the location of the DLE (after the low byte or after the high byte). Assume that D8-3 DLE ADD (7-0) L is asserted. This signal is sent to E77 pin 2 which is a negative AND gate that serves as a non-inverting buffer. Its other input is high so the output (pin 3) goes low and directly sets the DLE NEXT FRAME flip-flop which asserts the DLE request signal D8-5 DLE RQ L. If D8-3 DLE ADD (15-8) L is asserted instead of D8-3 DLE ADD (7-0) L, the TX DLE flip-flop is directly set and DLE NEXT FRAME remains cleared. When the TX bit counter overflows (end of character), its overflow pulse generates D9-5 TX CL via the M7813 and M7816 modules. When this pulse times out, its positive-going trailing edge clocks DLE NEXT FRAME which sets it and asserts D8-5 DLE RQ L.

Signal D8-5 DLE RQ L is sent to the TX control logic (print D5-6) on the M7813 module to generate D5-6 DLE EN (1) L. This signal returns to the M7817 module as the enabling signal for the TX DLE 7-0 multiplexer (E36 pin 7). The select signals for TX DLE 7-0 are D5-6 TX BIT CNTR 1 (1) H, 2 (1) H, and 4 (1) H which are the three least significant bits of the TX bit counter. The counter ripples through the selected count (0 to 7 maximum) to select each input, in ascending order, which performs a parallel-to-serial conversion of data from input to output. The serialized DLE character is sent to E44 and emerges as D9-4 AB TX DATA L. This signal is sent to the M7812 module (print D4-7) and then out as serial data.

When operating in the receive transparent text mode, a stripped DLE character is not only prevented from being transferred to the PDP-11 memory but it is excluded from the BCC accumulation. Fast recognition of the DLE is required to ensure that the BCC generator is turned off in time to exclude the DLE from the BCC accumulation. In this case, recognition by the character detect memory is not fast enough so the DLE stored in E35 and E37 is compared directly with the high byte of the RX buffer register (D4-5 RD 9 H–D4-5 RD 15 H) using 8242 digital comparators. When a match occurs (DLE detected), the wired-OR output of the eight 8242s goes high and is sent to pin 2 of 3-input NAND gate E86. Pin 1 of E86 is high because SEQ 9 HOLD is set. The third input (pin 13) is high because the DQ11 is in transparent text mode and D8-6 RX TRANS (1) H is asserted. With all inputs high, D8-5 RX DLE DET L is asserted at the output (pin 12) of E86. This signal is sent to the RX protocol control logic (print D8-6) to shut off the RX BCC generator.

BCC EXCLUDE Logic

Bit 11 of the sequence register (RX/TX BCC EXCLUDE) allows a received character to be excluded from the BCC accumulation when not in the transparent text mode. The baud rate must not exceed 250K when this bit is used.

The logic consists of negative AND gate E88 and flip-flops TX BCC EX (E71) and TX BCC EX NEXT (E70).

If it is desired to exclude the next character to be transmitted, the sequence decoding logic asserts D8-4 TX BCC EXCLUDE (7-0) L. This signal directly sets the TX BCC EX NEXT flip-flop. The low from the 0 output of this flip-flop is sent to E88 pin 2. The other input (pin 1) of this gate is high so it acts as a non-inverting buffer and D8-5 INH SHTX BCC L is asserted at its output. This signal goes to the TX BCC control logic on the M7816 module (print D9-5) and inhibits the pulses that clock the TX BCC generator which shuts it off.

If it is desired to exclude the character after next, D8-4 TX BCC EXCLUDE (15-8) L is asserted. This signal directly sets the TX BCC EX flip-flop which puts a high on the D input of TX BCC EX NEXT. When the TX bit counter overflows (end of character), its overflow pulse generates D9-5 TX CL via the M7813 and M7816 modules. When this pulse times out, its positive-going trailing edge clocks TX BCC EX NEXT which sets it and asserts D8-5 INH SHTX BCC L. This pulse also clocks TX BCC EX which clears it because its D input is permanently connected to ground. Both flip-flops are cleared whenever TX ACTIVE is cleared (D5-6 TX ACTIVE (1) H goes low).

PAD Logic

When nothing else is being transmitted, a PAD character is sent. A PAD character consists of all 1s; that is, the serial data out line is held in the mark state. Protocol control logic allows insertion of a PAD character following the last character to be transmitted. A PAD character is required to ensure that the BCC register is empty (BCC character is flushed). During an odd-character count, a PAD is required to fill the receiver shift register so a word transfer can be made. A jumper (W1) on the M7817 module allows selection of 1 or 2 PAD characters. The module is shipped with jumper W1 out which selects one PAD. Inserting W1 allows two PAD characters but this configuration is not supported by the DQ11 diagnostics.

Assume that jumper W1 is out and it is desired to send a PAD character. The PAD 2 and PAD 1 flip-flops start cleared. PAD 1 is not involved in this case. When it is desired to send the PAD character, the sequence decoding logic asserts D8-5 SEND PAD L. This signal directly sets PAD 1 and asserts D8-5 PAD RQ L. This request signal is sent to the TX control logic on the M7813 module (print D5-6) and allows transmission of a PAD character. When the TX bit counter overflows, pulse D9-5 TX CH is generated which clocks PAD 1 and clears it because its D input is low via the 1 output of PAD 2. When PAD 1 is cleared, D8-5 PAD RQ L goes high which removes the request for a PAD character.

If two PAD characters are desired, jumper W1 must be installed. When D8-4 SEND PAD L is asserted, both PAD 1 and PAD 2 are directly set. Request signal D8-5 PAD RQ L is asserted and the first PAD character is initiated. When the TX bit counter overflows, PAD 1 and PAD 2 are clocked. PAD 1 does not change state and the request signal remains asserted so the second PAD character is initiated; however, PAD 2 is cleared and puts a low on the D input of PAD 1. When the TX bit counter overflows again, PAD 1 is cleared and the request signal is removed.

TX Transparency Control Logic

To enter TX transparency text requires a TX double-character match, sequence register bit 1 set and a TX strobe pulse. TX strobe A allows entry on the next character while TX strobe B allows entry on the character after that.

To exit TX transparent text requires the use of REG/ERR CSR bit 13 (EXIT T). The circuitry is located on the M7816 module (print D9-5). However, with TX protocol control, EXIT T allows transmission of a DLE character and then permits character recognition to function again.

The TX transparency control logic is shown in the right center section of print D8-5 and in Figure 4-80.

In addition to flip-flops TX TRANS NEXT (E61) and TX TRANS (E60), flip-flop EXIT ONLY (E26) and one-shot E66 are part of this logic.

As an example, assume that it is desired to enter the TX transparent text mode during the next character.

1. At the start, flip-flops TX TRANS NEXT, TX TRANS, and EXIT DLY and one-shot E66 are cleared.
2. The sequence decoding logic asserts D8-4 1 → TX TRANS L which is sent to the E77 pin 5. The other input (pin 4) of this gate is high so its output (pin 6) goes low and directly sets TX TRANS.
3. Setting TX TRANS asserts D8-5 TX TRANS (1) L which is sent to the strobe logic (print D8-3). This signal inhibits the character detect logic but serves as a qualifying input to the DLE add logic.
4. D5-6 LD TX SH REG H is generated each time the TX shift register is to be loaded. This signal is the clock signal for EXIT DLY and the trigger for one-shot E66. While in transparency, EXIT DLY does not change state because D9-5 TX EXIT PULSE H is low and is sent to its D input. EXIT DLY remains cleared and the low from its 1 output inhibits triggering of one-shot E66 by the negative transitions of D9-5 TX EXIT PULSE H.

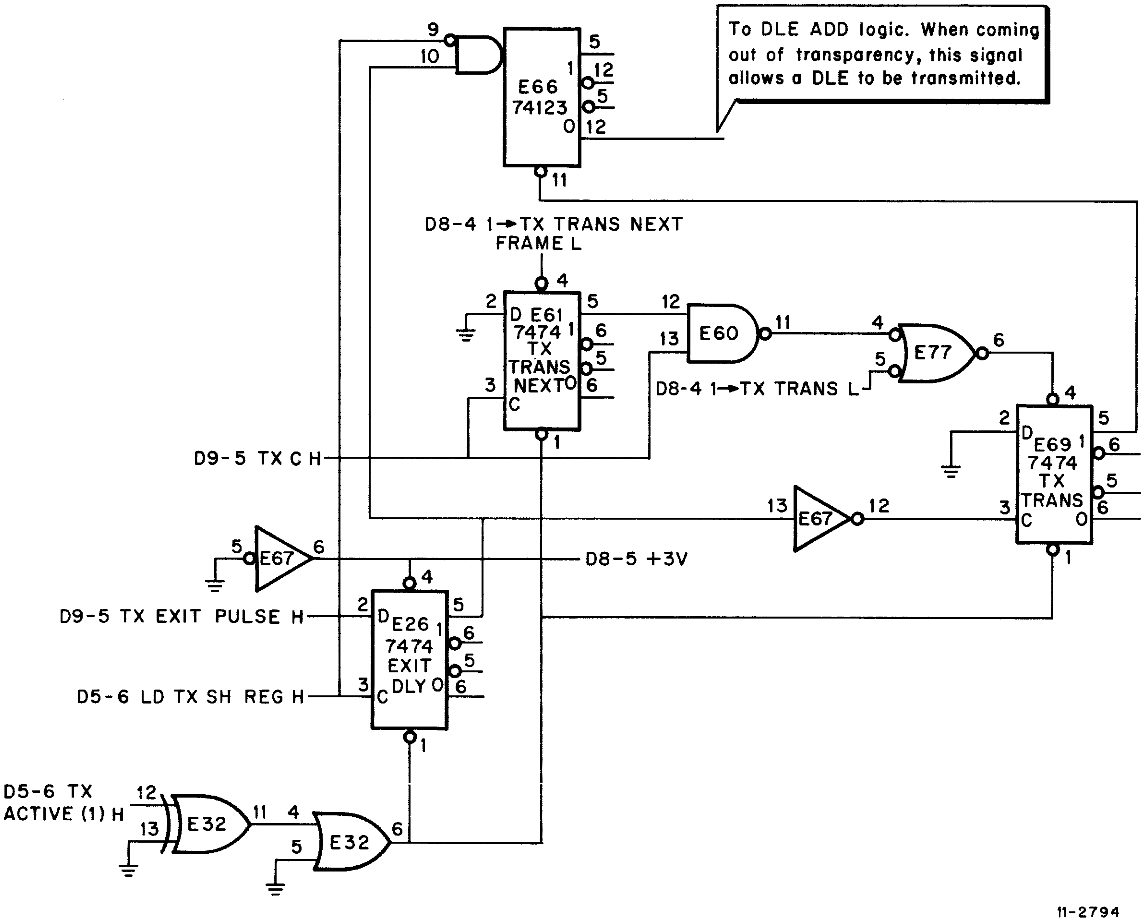


Figure 4-80 TX Transparency Control Logic

5. When coming out of transparency (controlled by M7816 module), D9-5 TX EXIT PULSE H goes high. The next TX load pulse (D5-6 LD TX SH REG H) clocks EXIT DLY and sets it. The 1 output of EXIT DLY puts a high on pin 10 of one-shot E66. This same TX load pulse drives D9-5 TX EXIT PULSE H low via the M7816 TX BCC control logic.

6. The next TX load pulse (D5-6 LD TX SH REG H) triggers one-shot E66 which directly sets DLE NEXT FRAME to assert D8-5 DLE RQ L and allows a DLE character to be transmitted. This load pulse also clocks EXIT DLY and clears it. The negative-going transition at the 1 output of EXIT DLY clocks TX TRANS which clears it. This drives D8-5 TX TRANS (1) L high which enables character recognition again.

TX BCC Control Logic

Under protocol control, the first TX BCC start-up control character is excluded from the TX BCC accumulation. On a message basis, the first BCC occurrence is the one immediately following Initialize, Master Clear, or the enabling of TX GO. Within the same message, if the TX BCC generator is stopped and restarted then the start-up control character is included in the BCC accumulation.

The first TX BCC start-up control character can be included in the TX BCC accumulation if jumper W2 is installed on the M7817 module. This mode of operation is not supported by diagnostics.

The TX BCC control logic is shown in the lower right section of print D8-5.

As an example, assume that the first TX BCC start-up character desires to turn on the TX BCC generator.

1. At the start, the following flip-flops are cleared: TX BCC, TX BCC NEXT, TX BCC CONT, TX BCC ON, and BCC SH ON.

2. With sequence register bit 3 set (CLEAR/START RX/TX BCC) and a control word match detected (TX strobe A generated), the sequence decoding logic asserts D8-4 TX BCC ON L.

3. D8-4 TX BCC ON L directly sets TX BCC NEXT. The high from the 1 output of this flip-flop goes to pins 1 and 2 of 3-input AND gate E28. The other input (pin 13) is also high because D9-5 TX C L is not asserted (no overflow pulse from the TX bit counter). The output of E28 is driven high, inverted by E2 and directly sets TX BCC ON.

4. The high from the 1 output of TX BCC puts a high on the D input of BCC SH ON and also goes to E85 pin 9. The other two inputs (pins 10 and 11) of this NAND gate are low because BCC SH ON is cleared. At this point, the protocol logic has tried to turn on the TX BCC generator but it has been delayed one character time.

5. When the current character has been serialized, the TX bit counter overflows and generates a positive carry out (CO) pulse. This pulse is inverted once on the M7813 module and twice on the M7816 module to become D9-5 TX C L on this module.

6. The trailing edge of D9-5 TX C L clocks BCC SH ON which sets it. This drives E85 pins 10 and 11 high (pin 9 is already high) and asserts D8-5 TX BCC SH EN L. This is a qualifying signal for the TX BCC control logic on the M7816 module (print D9-5). The low from the 0 output of BCC SH ON is double inverted by E55 and E60 and is fed back to its own preset input (pin 10) which holds it in the set state. This state can be overridden only by a low to the direct clear input (pin 13) when TX ACTIVE is cleared (message completed).

SUMMARY OF OPERATION
At this point, the TX BCC generator is running and the BCC character for the particular block of data within the message is being accumulated.

Assume now that it is desired to end the current data block, transmit the required number of BCC characters and restart the BCC generator immediately to accumulate the BCC for the next data block. An Intermediate Block Check Character (ITB) appears right after the current data block. It must tell the logic to append the correct number of BCCs (SEQ bits 4 and 5) and clear and restart the BCC generator (SEQ bit 3). The word in the SEQ register corresponding to the ITB in the CHAR DET register must have SEQ bits 3, 4 and 5 set to perform these functions. The BCC character(s) follows the ITB and then the next data block starts. In the logic, the assertion of D8-4 TX BCC ON L allows the BCC generator to restart without another control character.

7. The program sets sequence register bits 3, 4 and 5 to select the required number of BCC characters to append (transmit) then clear and restart the BCC generator. When a control word match is detected (TX strobe enabled), the sequence decoding logic asserts D8-4 TX BCC ON L.

8. D8-4 TX BCC ON L directly sets TX BCC CONT and its 1 output puts a high on the D input of TX BCC ON.

9. The TX BCC control logic on the M7816 module (print D9-5) stops the BCC generator and automatically appends the required number of BCC characters. When the last BCC has been appended, D5-6 BCC EN (1) L goes high and clocks TX BCC CONT which clears it and puts a low on the D input of TX BCC ON. This flip-flop (TX BCC ON) is clocked simultaneously with TX BCC CONT, but at that time its D input is low so it does not change state. D8-5 TX BCC SH EN L stays asserted so the TX BCC generator is still running.

SUMMARY OF OPERATION
The current block of data ends and the selected number of BCC characters have been transmitted. The hardware restarts the BCC generator and it accumulates the BCC for the next block of data.

As previously mentioned, if jumper W2 is installed, the first TX BCC start-up control character can be included in the TX BCC accumulation. The jumper completes the circuit between the 0 output of TX BCC ON and pin 5 of E55. When TX BCC ON is directly set, the low from its 0 output is double inverted by E55 and E60 and directly sets BCC SH ON. This enables D8-5 TX BCC SH EN L without the character time delay.

4.7.7 Receiver Protocol Control Logic

4.7.7.1 Functional Description – A simplified block diagram of the receiver protocol control logic is shown in Figure 4-81. The logic performs several functions that can be discussed separately. The major functional areas are listed below in order of discussion.

RX BCC Control Logic
This logic functions similarly to the TX BCC control logic in that it excludes the first RX BCC start-up control character from the RX BCC accumulation. The next RX BCC start-up control character within this message is included in the BCC accumulation. It can be omitted only by using the BCC exclude logic.

Character Strip Logic
This logic prevents the detected character from being transferred to the PDP-11 memory but allows it to be included in the RX BCC accumulation.

RX BCC Disabling Logic
The RX BCC generator can be stopped by this logic to exclude a detected character from the BCC accumulation. The categories of characters to be excluded are listed below.

1. All DLE characters during transparent text mode.
2. A SYNC character following a DLE character.
3. SYNC characters in non-transparent text operation.
4. Any detected character, if sequence register bit 11 (RX BCC EXCLUDE) is set.

Clear GO/Set DONE Logic
This logic allows RX GO to be cleared and RX DONE to be set at the end of an NPR transfer only. The circuit is independent of the clearing of RX ACTIVE.

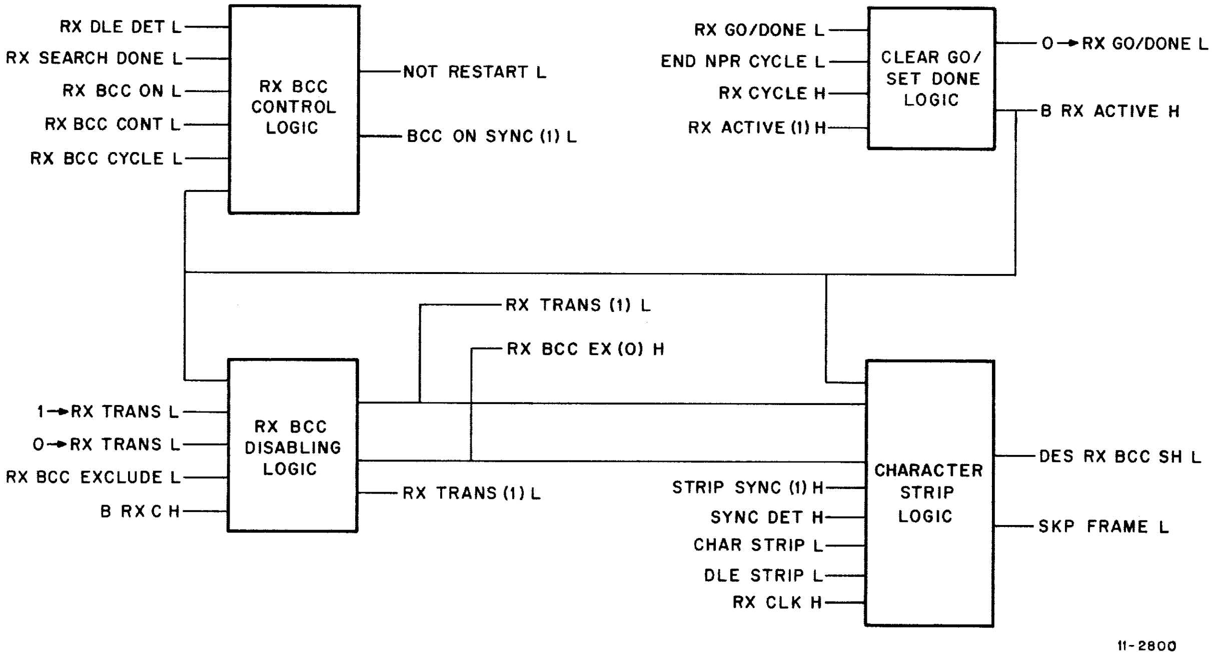


Figure 4-81 Block Diagram of Receiver Protocol Control Logic

4.7.7.2 Detailed Description

RX BCC Control Logic

The RX BCC control logic is located in the upper left portion of print D8-6. In general, it operates similarly to the TX BCC control logic in that it excludes the first BCC start-up control character from the RX BCC accumulation but includes subsequent RX BCC start-up control characters within a message.

As an example, assume that the first RX BCC start-up control character occurs and the data block within the message ends with a BCC character.

1. At the start, the following flip-flops are cleared: BCC CONT, BCC RESTART, and BCC ON SYNC.

2. When the RX BCC start-up control character is detected, D8-4 RX BCC ON L is asserted. It directly sets BCC RESTART and puts a high on the D input of BCC ON SYNC.

3. The next positive transition of the receiver clock (D4-3 RX CLOCK H) clocks BCC ON SYNC and sets it. The low from its 0 output is D8-6 BCC ON SYNC (1) L which is fed back to the preset input (pin 10) of BCC ON SYNC to hold it in the set state until it is directly cleared at the end of the message (RX ACTIVE cleared).

4. Signal D8-6 BCC ON SYNC (1) L is sent to the RX BCC control logic on the M7816 module (print D9-6). This signal is required to turn on the RX BCC generator. The RX BCC generator stays on as long as D8-6 BCC ON SYNC (1) L remains low. A one character time delay is built into the M7816 RX BCC turn-on logic.

   SUMMARY OF OPERATION
   The first RX BCC start-up control character requests that the RX BCC generator be started. The RX BCC start-up logic on the M7816 module starts the RX BCC generator after a one character time delay. This excludes the start-up control character from the RX BCC accumulation. The data in this block is being run through the RX BCC generator.

Assume that it is desired to end this block of data, receive the required number of BCC characters and restart the RX BCC generator immediately.

5. The program sets sequence register bits 4 and 5 which allows the M7816 RX BCC control logic to test the selected number of BCC characters. Sequence register bit 3 is also set to allow restarting of the RX BCC logic. Actually, the RX BCC generator does not turn off. This set of conditions prevents the RX BCC control logic on the M7817 module from clearing the RX BCC generator.

6. When the control character defined in step 5 arrives, D8-4 RX BCC CONT L is asserted. This signal directly sets BCC CONT and puts a high on the D input of BCC RESTART.

7. When the selected number of BCC characters is tested, the M7816 logic drives D9-6 RX BCC CYCLE L high. This signal clocks BCC CONT and BCC RESTART simultaneously. BCC RESTART does not change state. BCC CONT is cleared which puts a low on the D input of BCC RESTART. Signal D8-6 NOT RESTART L remains high so the RX BCC generator is not cleared. Instead, it keeps running and the restart control character is included in the BCC accumulation.

   SUMMARY OF OPERATION
   The first RX BCC start-up control character is excluded from the BCC accumulation but the first block data is included. The required number of BCC characters are tested. The RX BCC generator keeps running so that the next control character that requested immediate RX BCC start-up is included in the BCC accumulation for the second block. The data in the second block is being run through the RX BCC generator.

Assume now that it is desired to end the second block of data, receive the required number of BCC characters and not restart the RX BCC generator.

8. The program sets sequence register bits 4 and 5 which allows the M7816 RX BCC control logic to test the selected number of BCC characters. Bit 3 of the sequence register is cleared because it is not desired to restart the RX BCC generator.

9. As in step 6, when the control character arrives, the M7816 RX BCC control logic tests the selected number of BCC characters and then drives D9-6 RX BCC CYCLE L high. Because sequence register bit 3 is cleared, D8-4 RX BCC CONT L is not asserted. BCC CONT remains cleared and when D9-6 RX BCC CYCLE L goes high, BCC RESTART is cleared. This puts a high on pin 10 of 3-input NAND gate E86. Pin 9 is high because BCC ON SYNC is set. After every character detect search operation, D8-3 RX DONE (SEARCH) H is asserted and via E88, it drives pin 11 of E86 high. The output of E86 goes low which asserts D8-6 NOT RESTART L. This signal directly clears the BCC generator. The RX BCC generator is allowed to run and if the accumulation is not wanted the RX BCC generator is cleared. This is accomplished on a character basis. This method is used because in the receive mode only one character time is available to react to BCC turn on/off.

Character Strip Logic

The character strip logic is located in the right center portion of print D8-6. It is also shown in Figure 4-82.

Normally, an RX character strip operation prevents the detected character from being transferred to the PDP-11 memory but allows it to be included in the RX BCC accumulation.

Sequence register bit 8 (RX CHARACTER STRIP) is used to control this function. When this bit is set and a control character match is detected, D8-4 CHAR STRIP L is asserted as a negative pulse. It directly sets SKP FRAME via gate E77. The high from the 1 output of SKP FRAME goes to pins 1 and 13 of AND-OR-invert gate E58 which asserts D8-6 SKP FRAME L at the output of E58. Signal D8-6 SKP FRAME L is ANDed with D8-3 RX DONE in the character detect control logic (print D8-3) to generate D8-3 RX SEARCH DONE L. This signal goes to the RX character control logic on the M7813 module (print D5-8).

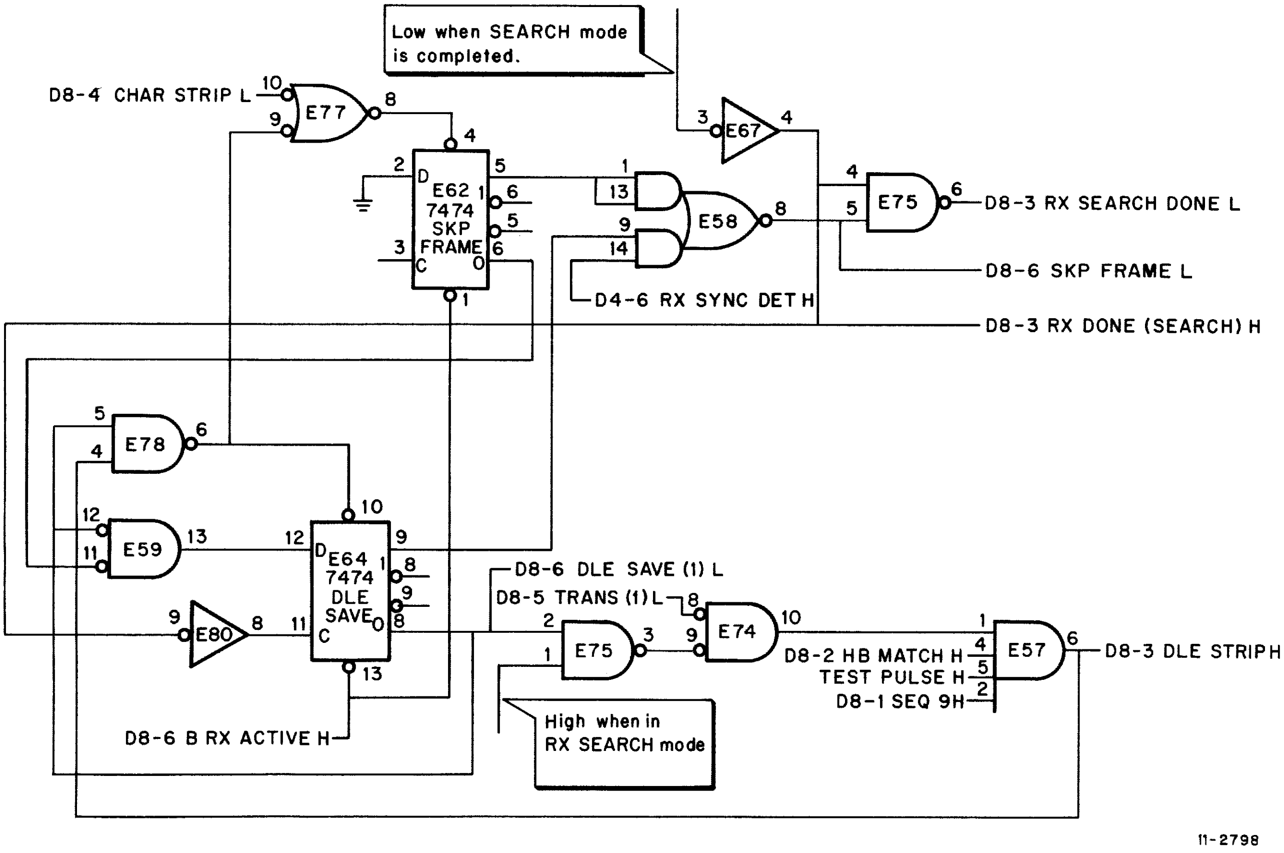


Figure 4-82 Character Strip Logic

It is this logic that actually inhibits the transfer of the detected character. When the RX bit counter overflows (end of current character), it generates a positive carry out pulse which is double buffered and goes to the M7817 module as D9-6 B RX C H. At overflow, this pulse clocks SKP FRAME which clears it because its D input is permanently connected to ground. The strip logic is back in its original state and the detected character has been stripped.

The character strip logic also includes some associated logic to strip the DLE, SYNC sequence encountered in the receive transparent text mode. In this case, the DLE is stripped; and if the next character is SYNC, it is stripped also.

To clarify this discussion, some logic on print D8-3 is shown in Figure 4-82.

1. The SKP FRAME and DLE SAVE flip-flops are cleared; therefore, D8-6 DLE SAVE (1) L is high.
2. D8-6 DLE SAVE (1) L goes to E75 pin 2. The other input (pin 1) of this gate is high also because the DQ11 is in the RX search mode and the M7816 module is not inhibiting character recognition. This drives the output of E75 low and it goes to E74 pin 9. The other input of this gate is low also because the DQ11 is in the transparent text mode (D8-5 RX TRANS (1) L is asserted). This drives the output of E74 high.
3. The high from E74 goes to pin 1 of 4-input AND gate E57. This represents one qualifying input to the gate that asserts D8-3 DLE STRIP H. The other three inputs are high, providing the following conditions have been met: sequence register bit 9 set, RX search active, transparent text mode active, high byte match detected and a TEST pulse generated.
4. With all inputs high, the output of E57 goes high and asserts D8-3 DLE STRIP H. This signal goes to E78 pin 4 (print D8-6) and drives its output low.
5. The low output of E78 directly sets SKP FRAME which asserts D8-6 SKP FRAME L. This signal also directly sets DLE SAVE and asserts D8-6 DLE SAVE (1) L.
6. Signal D8-6 DLE SAVE (1) L drives D8-3 DLE STRIP H low which inhibits the stripping of the next character if it is a DLE.
7. Signal D8-6 SKP FRAME L generates D8-3 RX SEARCH DONE L when the RX search operation is finished. Signal D8-3 RX SEARCH DONE L goes to the RX character control logic on the M7813 module (print D5-8) to strip the current DLE character.
8. At the end of the RX search operation, D8-3 RX DONE (SEARCH) H is asserted. This signal clocks DLE SAVE but it does not change state because its D input is high via E59 pin 13. This action saves the fact that a DLE has been detected and puts a high on pin 9 of E58.
9. When the RX bit counter overflows, D9-6 B RX C H clocks SKP FRAME and clears it which drives D8-6 SKP FRAME L high. At this point, the DLE character has been stripped and the strip character logic is conditioned to respond only to a SYNC character.
10. When the SYNC character arrives, D4-7 RX SYNC DET H is asserted on the M7812 module and goes to pin 10 of E58. The other input (pin 9) is already high (step 8); therefore, D8-6 SKP FRAME L is asserted and the RX character control logic on the M7813 logic strips the SYNC character.
11. At the end of this RX search operation, D8-3 RX DONE (SEARCH) H clocks DLE SAVE and clears it because its D input is low. The character strip logic and associated DLE SAVE logic are now back in their original states.

RX BCC Disabling Logic

Once started, the RX BCC generator can be stopped by the RX protocol logic to exclude a detected character from the BCC accumulation. This logic is located in the right center position of print D8-6.

When the character to be excluded is detected, the logic asserts D8-6 DES RX BCC SH L. This signal goes to the RX BCC control logic on the M7816 module (print D9-6) which inhibits the clock for the RX BCC generator. D8-6 DES RX BCC SH L is the inverted output of E76 and can be generated by any one of four inputs to this gate. The conditions that cause a detected character to be excluded from the RX BCC accumulation are discussed below.

1. In transparent text, all DLE characters are excluded. When a DLE is detected in the transparent text mode, D8-5 RX DLE DET L is asserted, inverted by E80 and sent to pin 1 of E87. Pin 2 of this gate is high because RX TRANS is set in transparent text mode. The third input (pin 13) of E87 is also high because BCC DLE SAVE is cleared. The output (pin 12) of E87 goes low and is double inverted by E76 and E67 to assert D8-6 DES RX BCC SH L.

2. A SYNC character following a DLE is stripped also because the DLE, SYN sequence is an idle condition. As a continuation of condition 1 above, the BCC DLE SAVE flip-flop is clocked when the RX bit counter overflows (end of current character). This sets BCC DLE SAVE and puts a high on pin 9 of E87. If the next character is a SYNC, pin 10 goes high via E79 pin 3 because a SYNC character is detected and RX CSR bit 1 (STRIP SYNC) is set. The third input (pin 11) of E87 is also high because RX TRANS is set. These conditions drive E87 pin 8 low which asserts D8-6 DES RX BCC SH L.

3. In non-transparent text or non-total transparency operation, SYNC characters can be stripped from the BCC. When a SYNC character is detected (D4-7 RX SYNC DET H asserted) and RX CSR bit 1 is set (D4-4 STRIP SYNC (1) H asserted), the high from E79 pin 3 is ANDed with the fact that the DQ11 is not in total transparency (D9-6 RX TOTAL TRANS (1) L is high) to assert D8-6 DES RX BCC SH L.

4. Any detected character is excluded from the RX BCC accumulation if sequence register bit 11 (RX BCC EXCLUDE) is set. Setting this bit generates D8-4 RX BCC EXCLUDE L which directly sets the RX BCC EX flip-flop. The low from the 0 output of this flip-flop asserts D8-6 DES RX BCC SH L.

Clear GO/Set DONE Logic

In the character recognition mode, sequence register bit 6 clears RX ACTIVE and sequence register bit 7 clears RX GO and sets RX DONE. The logic for clearing RX ACTIVE is shown in print D8-4. The logic for clearing RX GO and setting RX DONE is located in the lower left portion of print D8-6. The output of this logic is D8-6 0 → RX GO/DONE L. It goes to the M7813 module (print D5-4) and when it is asserted RX GO is cleared and RX DONE is set. Signal D8-6 0 → RX GO/DONE L can be asserted only when the following conditions exist: the RS flip-flop (two E48 gates) has been set by D8-4 RX GO/DONE L being asserted, D5-3 RX CYCLE H is asserted, and D6-2 END NPR CYCLE (1) L is asserted. Signal D6-2 END NPR CYCLE (1) L is asserted only at the end of an RX transfer; therefore, RX GO is cleared only after completion of the transfer.

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTIONS

A.1 INTRODUCTION

The MSI integrated circuits (ICs) shown in the engineering drawings are discussed in the following paragraphs. The descriptions include one or more of the following items: pin/signal designations, equivalent logic schematic, and truth table. This information is intended as a maintenance aid for troubleshooting to the IC level. Table A-1 lists the ICs by manufacturer's part number, name, and paragraph number.

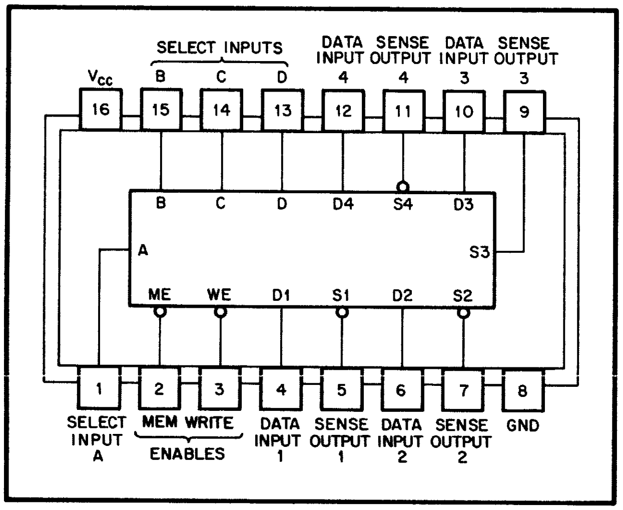
Table A-1
Integrated Circuits

Manufacturer's Part Number	Name	Paragraph
3101	64-Bit Read/Write Memory	A.2
4015	Quad D-Type Flip-Flop	A.3
7442	4-Line to 10-Line Decoder	A.4
7474/74H74	Dual D-Type Edge-Triggered Flip-Flop	A.5
8838	Quad Bus Transceiver	A.6
74123	Retriggerable Monostable Multivibrator with Clear	A.7
74153	Dual 4-Line to 1-Line Data Selector/Multiplexer	A.8
74157/74S158	Quad 2-Line to 1-Line Data Selector/Multiplexer	A.9
74161	Synchronous 4-Bit Counter	A.10
74174/74175	Hex/Quad D-Type Flip-Flop with Clear	A.11
74197	Presettable Binary Counter/Latch	A.12

A.2 3101 64-BIT READ/WRITE MEMORY

Function Table

ME	WE	Operation	Condition of Outputs
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High



11-1117

A.3 4015 QUAD D-TYPE FLIP-FLOP

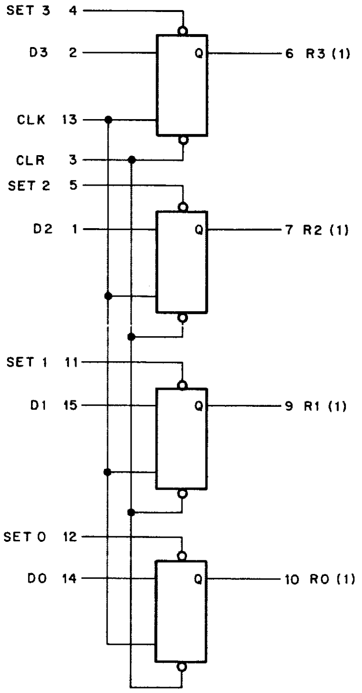
The 4015 contains four flip-flops with single-rail outputs (Q only). Each flip-flop has its own preset input ($\overline{\text{SET}}$). All flip-flops are cleared by a common clear input ($\overline{\text{RESET}}$).

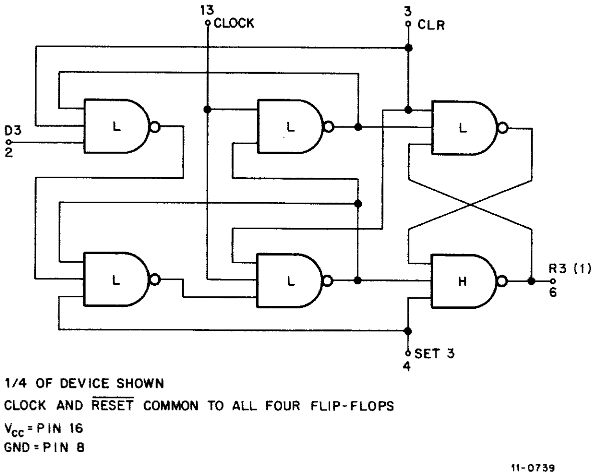
Truth Table

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse

Q_n = time period following clock pulse



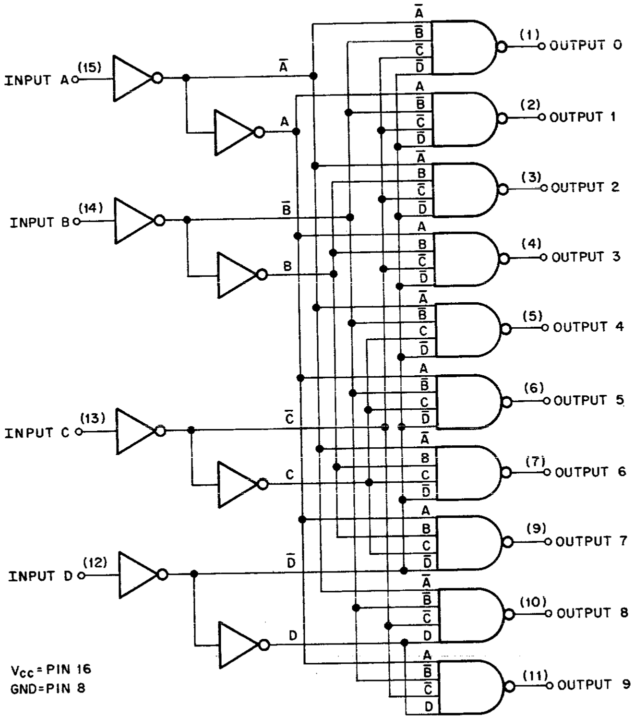


1/4 OF DEVICE SHOWN
CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS
V_{CC} = PIN 16
GND = PIN 8

11-0739

A.4 7442 4-LINE TO 10-LINE DECODER

In the DQ11, the 7442 is used as a 3-wire binary to octal decoder. Input D is used as a strobe and when it is low, data is taken from outputs 0–7.



11-0734

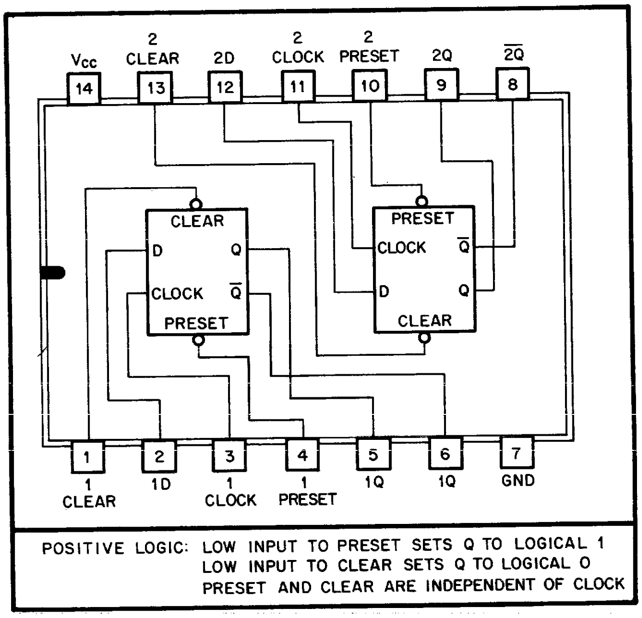
Truth Table

BCD Input				Octal Output							
D	C	B	A	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

X = Irrelevant

A.5 7474/74H74 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

The 7474/74H74 D-type flip-flops are triggered by the positive edge of the clock pulse. They feature direct-clear and direct-preset inputs and complementary outputs.



POSITIVE LOGIC: LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

11-0766

Truth Table (Each Flip-Flop)

t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
0	0	1
1	1	0

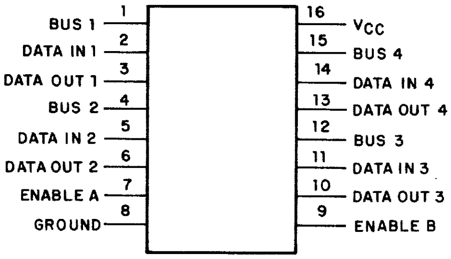
Notes:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

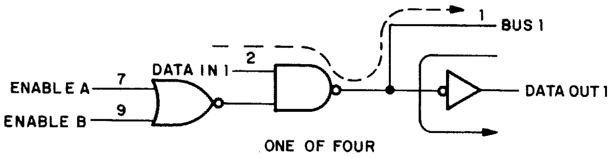
A.6 8838 QUAD BUS TRANSCEIVER

The 8838 consists of four identical receiver/driver combinations in one package for use on the PDP-11 Unibus. Data from the equipment on DATA IN 1, e.g., appearing on pin 2 will be driven out of pin 1 (BUS 1) to the Unibus (if enabled). A BUS 1 signal received from the Unibus on pin 1 will be fed out of pin 3 (DATA OUT 1) to the equipment.

Signal/Pin Designations

Signal Name	Circuit			
	1	2	3	4
BUS	1	4	12	15
DATA IN	2	5	11	14
DATA OUT	3	6	10	13
ENABLE	A		B	
	7		9	
GROUND	8			

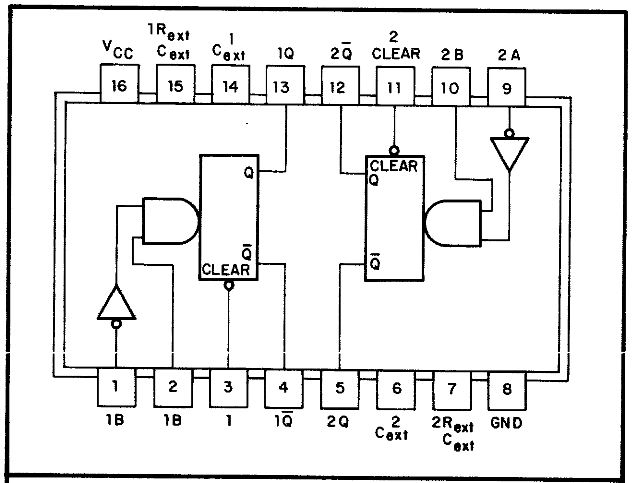




11-1860

A.7 74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

The 74123 Multivibrator provides dc triggering from gated low level active (A) and high level active (B) inputs. It also provides overriding direct clear inputs and complementary outputs. The retriggering capability simplifies generation of extremely long duration output pulses. If the input is triggered before the output pulse is terminated, the output pulse is extended. An overriding clear feature allows any output pulse to be terminated at a predetermined time, independent of timing components.



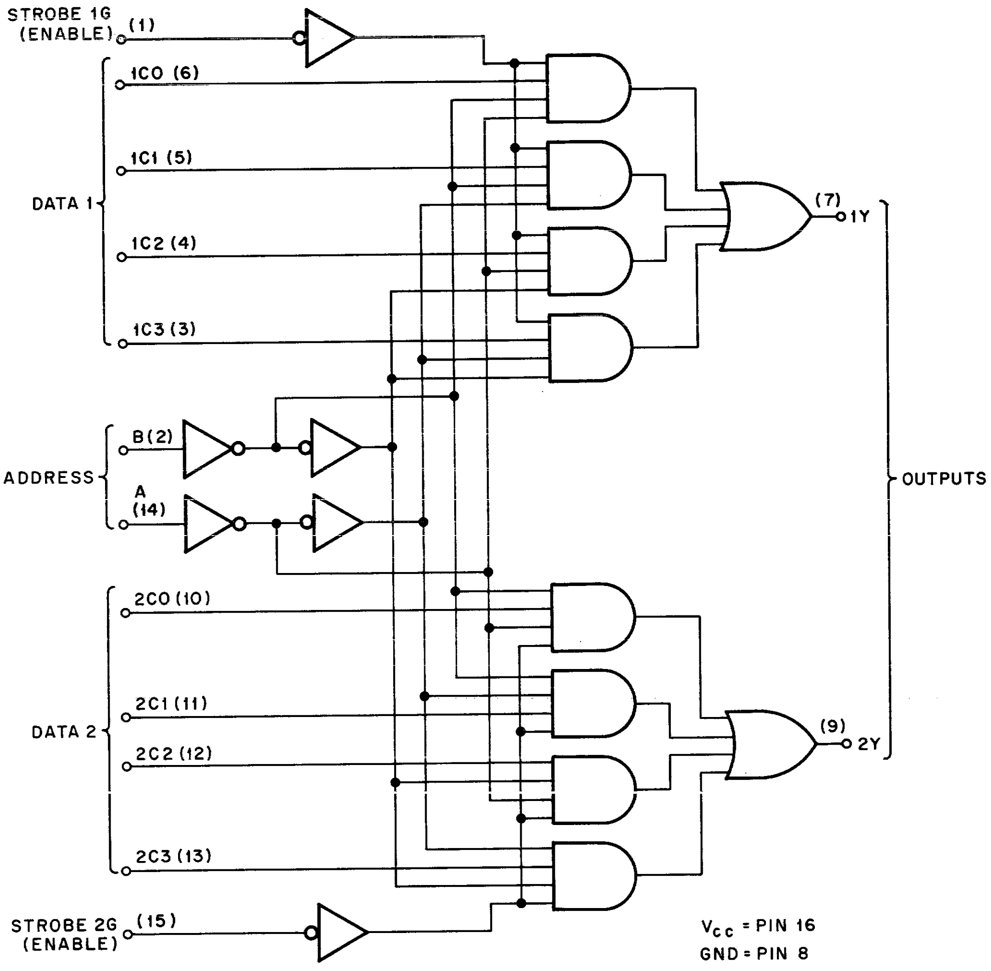
positive logic
Low input to clear resets Q to low level and inhibits data inputs

11-1864

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	Q̄
H	X	L	H
X	L	L	H
L	↑	⊓	⊔
↑	H	⊓	⊔

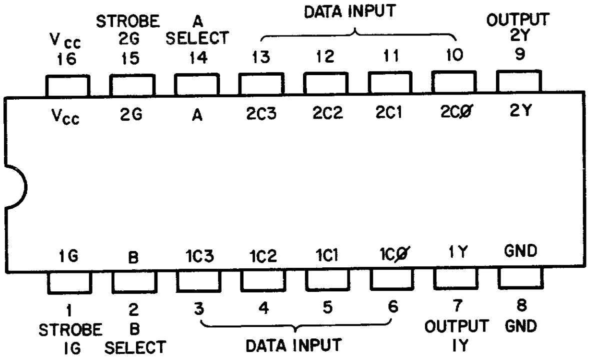
A.8 74153 DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXERS



LOGIC DIAGRAM

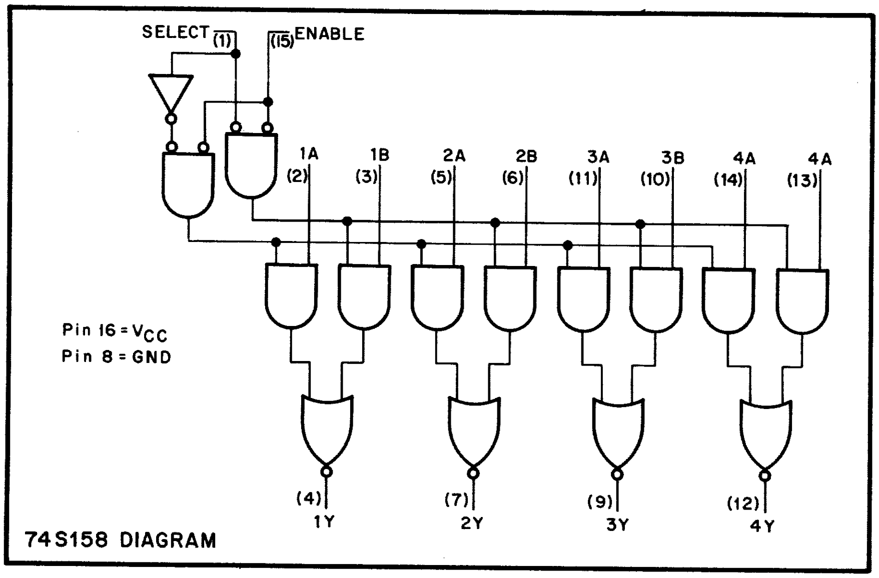
CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



8E-0138

A.9 74157/74S158 QUADRUPLE 2-LINE-TO-1-LINE MULTIPLEXER



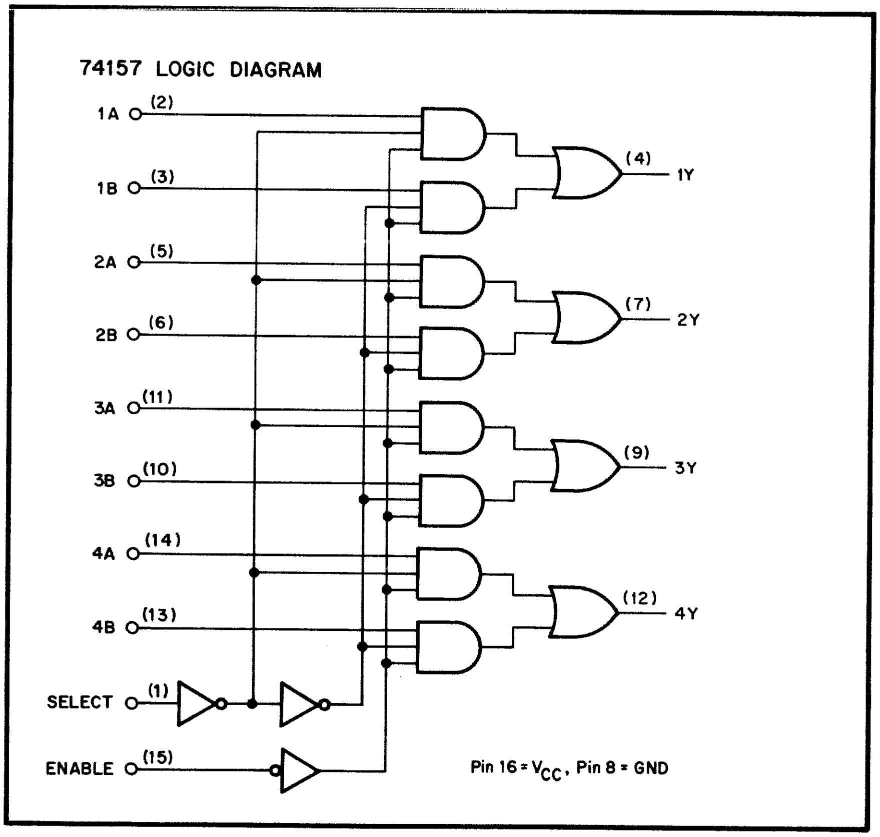
74S158 DIAGRAM

TRUTH TABLE

INPUTS			OUTPUT Y	
ENABLE	SELECT	A B	74157	74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

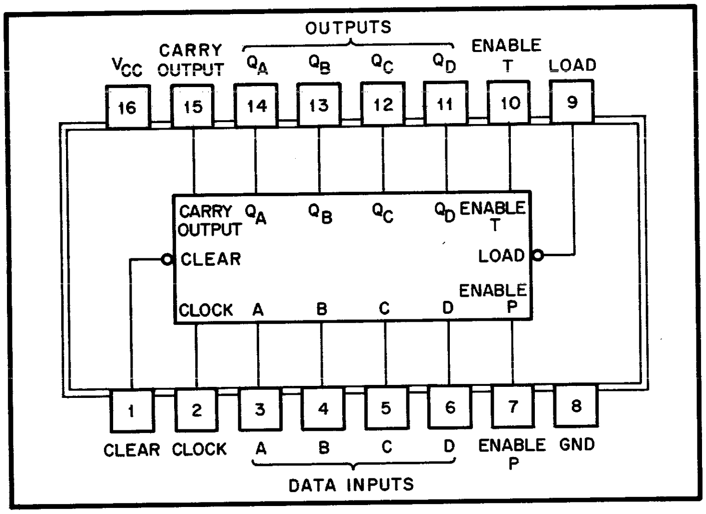
H=High level, L=Low level, X=Irrelevant

74157 LOGIC DIAGRAM

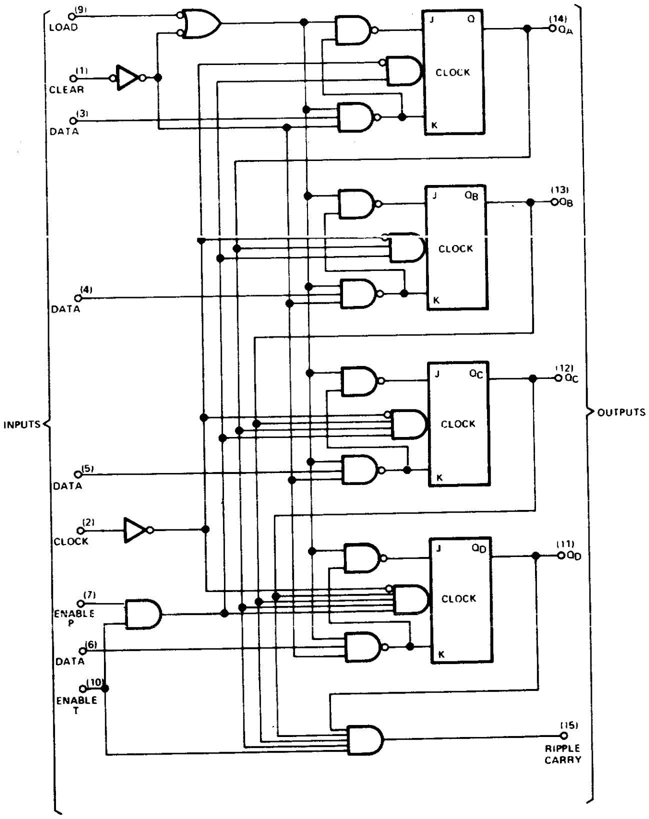


11-1131

A.10 74161 SYNCHRONOUS 4-BIT COUNTER

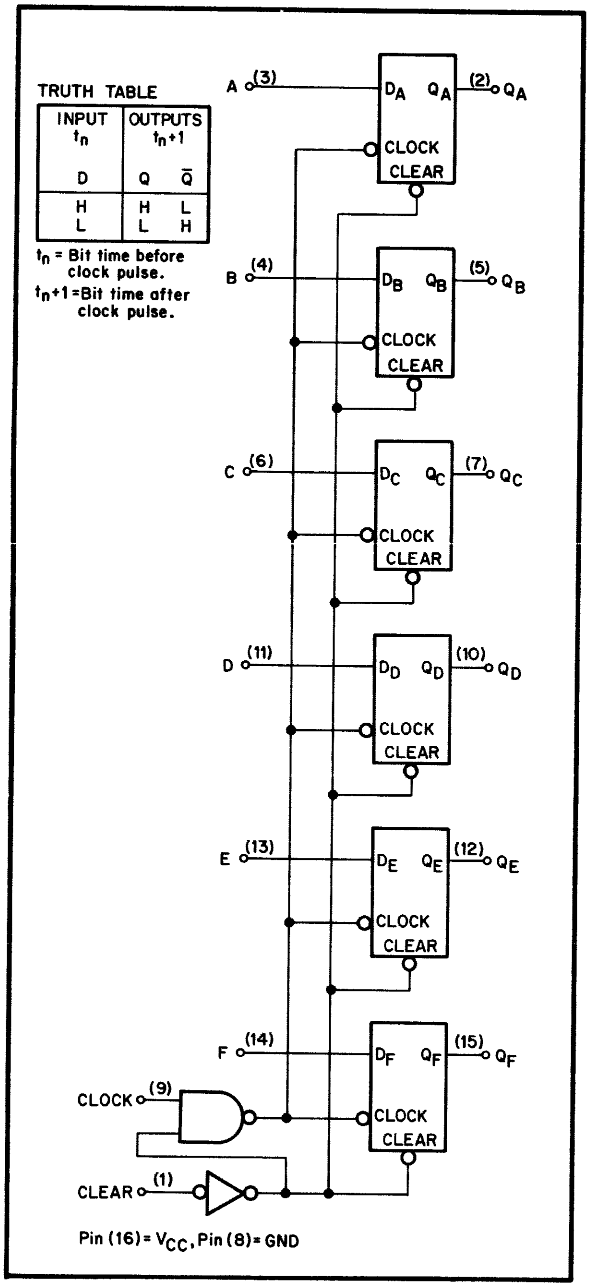


11-2201



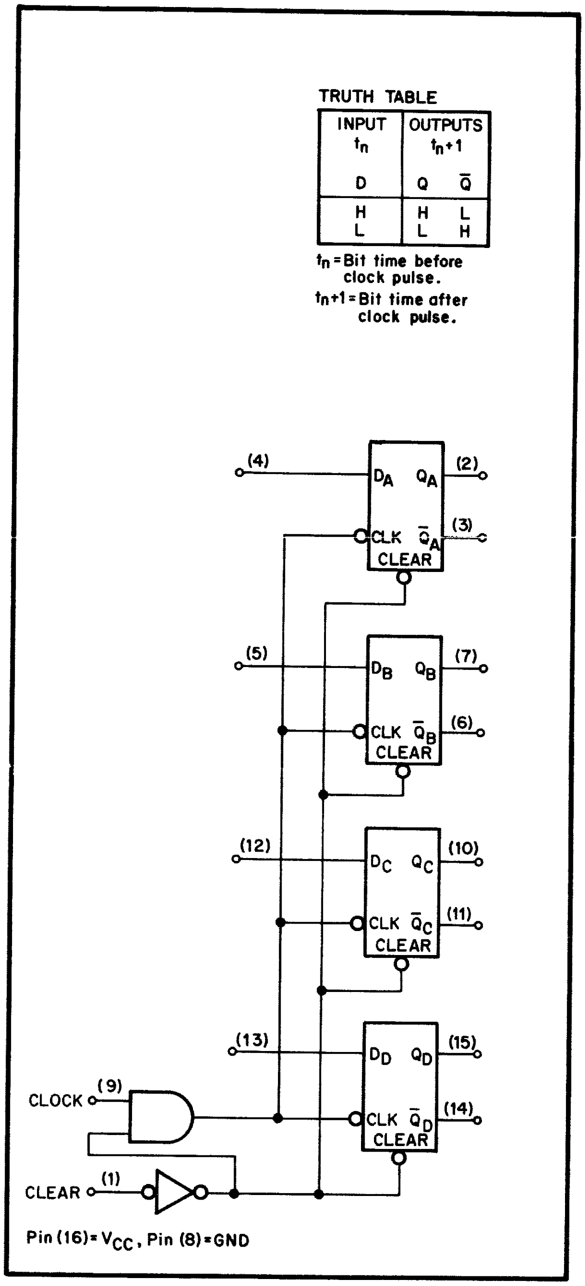
A.11 74174 HEX/74175 QUAD D-TYPE FLIP-FLOPS WITH CLEAR

The 74174 contains six flip-flops with single-rail outputs (Q only). The 74175 contains four flip-flops with double-rail outputs (complementary Q and $\overline{Q}$). Both devices have common clock and clear inputs.



11-1112

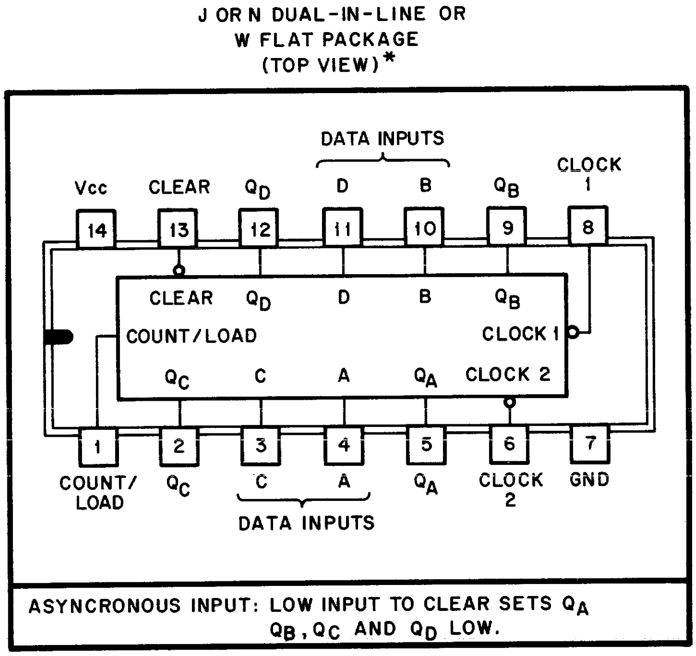
74174 Diagram



11-1113

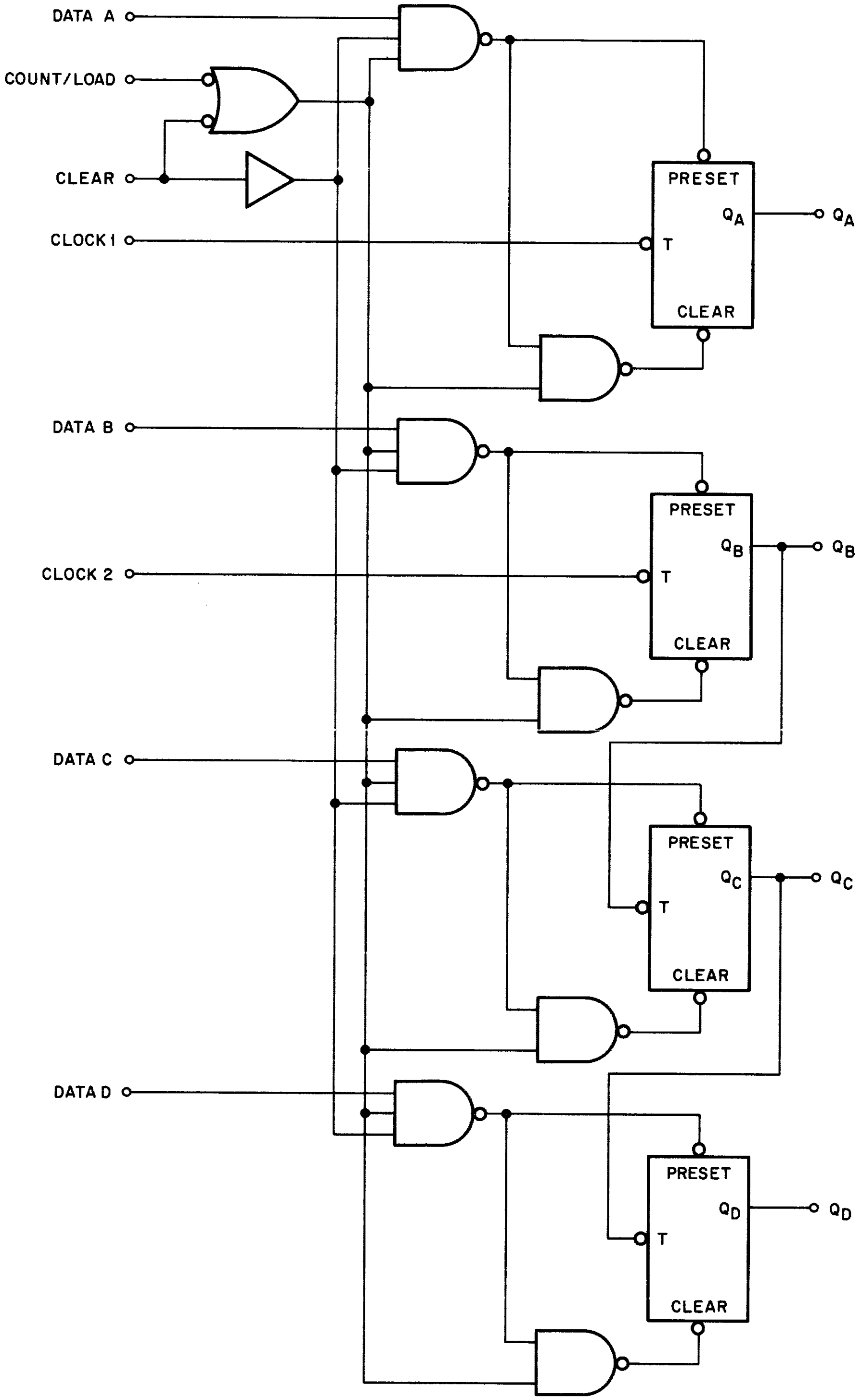
74175 Diagram

A.12 74197 PRESETTABLE BINARY COUNTER/ LATCH



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

11-0482


DATA A
COUNT/LOAD
CLEAR
CLOCK 1
DATA B
CLOCK 2
DATA C
DATA D
PRESET
Q_A
T
CLEAR
Q_A
PRESET
Q_B
T
CLEAR
Q_B
PRESET
Q_C
T
CLEAR
Q_C
PRESET
Q_D
T
CLEAR
Q_D
11-0481

APPENDIX B
PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized in 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location: low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only and the high (odd) byte of the word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00). Eighteen bits provide the capability of addressing 256K memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multiplier K equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. This maximum memory size can be used only by a PDP-11 processor with a memory management unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure B-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 2^{18} or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the processor uses as shown below.

The highest 8K address locations (760000–777777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248K bytes or 124K words to program.

A PDP-11 processor without the memory management unit provides 16 address bits that specify 2^{16} or 65,536 (64K) locations (Figure B-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s when the processor is master to allow generation of addresses in the reserved area with only 16-bit control.

Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777 which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Address Bit
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	Binary
1			1			7			6			0			1			Octal

Address Word Format

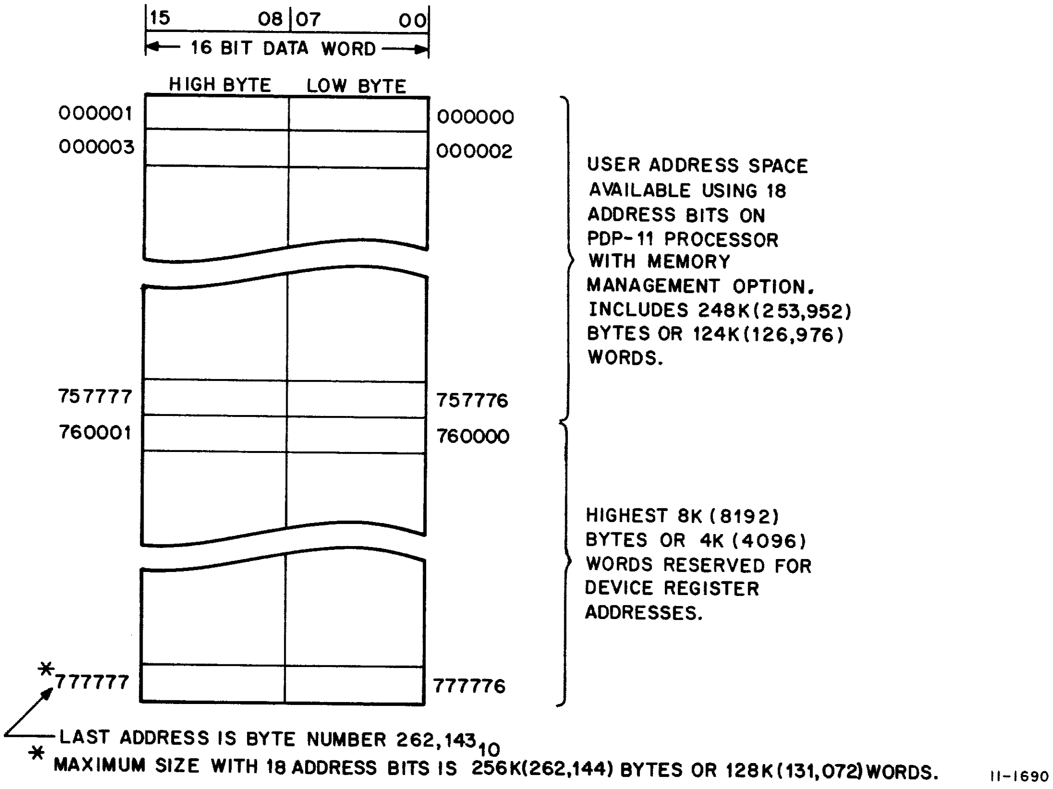

15
08
07
00
16 BIT DATA WORD
HIGH BYTE
LOW BYTE
000001
000000
000003
000002
USER ADDRESS SPACE AVAILABLE USING 18 ADDRESS BITS ON PDP-11 PROCESSOR WITH MEMORY MANAGEMENT OPTION. INCLUDES 248K(253,952) BYTES OR 124K(126,976) WORDS.
757777
757776
760001
760000
HIGHEST 8K (8192) BYTES OR 4K (4096) WORDS RESERVED FOR DEVICE REGISTER ADDRESSES.
*777777
777776
LAST ADDRESS IS BYTE NUMBER 262,143₁₀
* MAXIMUM SIZE WITH 18 ADDRESS BITS IS 256K(262,144) BYTES OR 128K(131,072) WORDS.
11-1690

Figure B-1 Memory Organization for Maximum Size Using 18 Address Bits

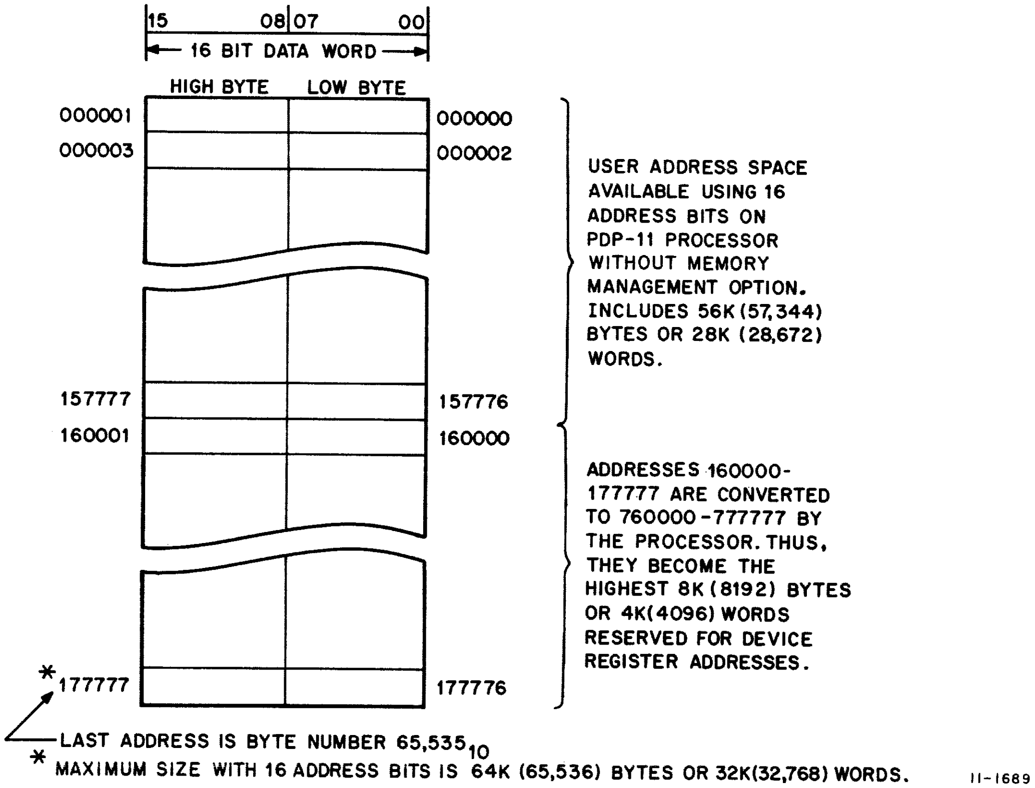

15
08
07
00
16 BIT DATA WORD
HIGH BYTE
LOW BYTE
000001
000000
000003
000002
USER ADDRESS SPACE AVAILABLE USING 16 ADDRESS BITS ON PDP-11 PROCESSOR WITHOUT MEMORY MANAGEMENT OPTION. INCLUDES 56K(57,344) BYTES OR 28K (28,672) WORDS.
157777
157776
160001
160000
ADDRESSES 160000-177777 ARE CONVERTED TO 760000-777777 BY THE PROCESSOR. THUS, THEY BECOME THE HIGHEST 8K (8192) BYTES OR 4K(4096) WORDS RESERVED FOR DEVICE REGISTER ADDRESSES.
*177777
177776
LAST ADDRESS IS BYTE NUMBER 65,535₁₀
* MAXIMUM SIZE WITH 16 ADDRESS BITS IS 64K (65,536) BYTES OR 32K(32,768) WORDS.
11-1689

Figure B-2 Memory Organization for Maximum Size Using 16 Address Bits

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interfering with the reserved space.

PDP-11 core memories are available in 4K or 8K increments. The highest location of various size core memories are shown below.

Memory Size		**Highest Location**
K-Words	**K-Bytes**	**(Octal)**
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

DQ11 NPR SYNCHRONOUS LINE
INTERFACE MANUAL
EK-DQ11-MM-002

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