EK-DL11W-TM-002

DL11-W Serial Line Unit/Real-Time Clock Option Technical Manual

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DL11-W Serial Line Unit/Real-Time Clock Option Technical Manual

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PREFACE

This manual describes the DL11-W Serial Line Unit/Real-Time Clock Option (M7856). Complete understanding of its contents requires that the user have a general knowledge of digital circuitry and a basic understanding of PDP-11 computers. The *PDP-11 Processor Handbook*, the *PDP-11 Peripherals Handbook*, the *PDP-11 Paper Tape Software Handbook*, and the appropriate system user's manual will be valuable as references.

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual is divided into four major chapters: Introduction; Configuration, Installation, and Testing; Programming; and Detailed Description. Although control signals and data are transferred between the interface and the Unibus and between the interface and the communications device, this manual is limited to coverage of the interface itself.

The purpose of this manual is to present the user with information necessary to understand normal system operation of the DL11-W. This information will be useful when analyzing trouble symptoms and determining corrective action. However, presentation of detailed troubleshooting techniques is beyond the scope of the manual.

1.2 ENGINEERING DRAWINGS

A complete set of engineering and circuit schematics is provided in a companion volume to this manual entitled *DL11-W SLU/RTC Option Engineering Drawings*. The general logic symbols used on these drawings are described in the *DIGITAL Logic Handbook*. Specific symbols and conventions are also included in certain PDP-11 system manuals. The following paragraphs describe the signal nomenclature convention used on the drawing set.

Signal names in the DL11-W print set are given in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right corner of the print title block (DL-1, DL-2, DL-3, etc.). SIGNAL NAME is the proper name of the signal. The names used on the print set are also used in this manual. POLARITY is either H or L to indicate the voltage level of the signal. H means +3 V; L means ground. As an example, the signal:

DL-1 RCVR DONE H

orignates on sheet 1 of the M7856 module drawing and is read, "When RCVR DONE is true, this signal is at +3 V."

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

1.3 GENERAL DESCRIPTION

The DL11-W Serial Line Unit/Real-Time Clock Option provides two distinct functions. First, the DL11-W is a character-buffered communications interface designed to assemble or disassemble the serial information required by a communications device for parallel transfer to or from the PDP-11 Unibus. Second, the DL11-W is a line frequency clock which can provide timed interrupts, allowing a program to measure the passage of time. The DL11-W consists of a single integrated circuit quad board (Figure 1-1) containing two independent communications units (receiver and transmitter) that are capable of simultaneous 2-way communication, and an independent line frequency real-time clock. Note that a quad board has four connectors (groups of fingers).

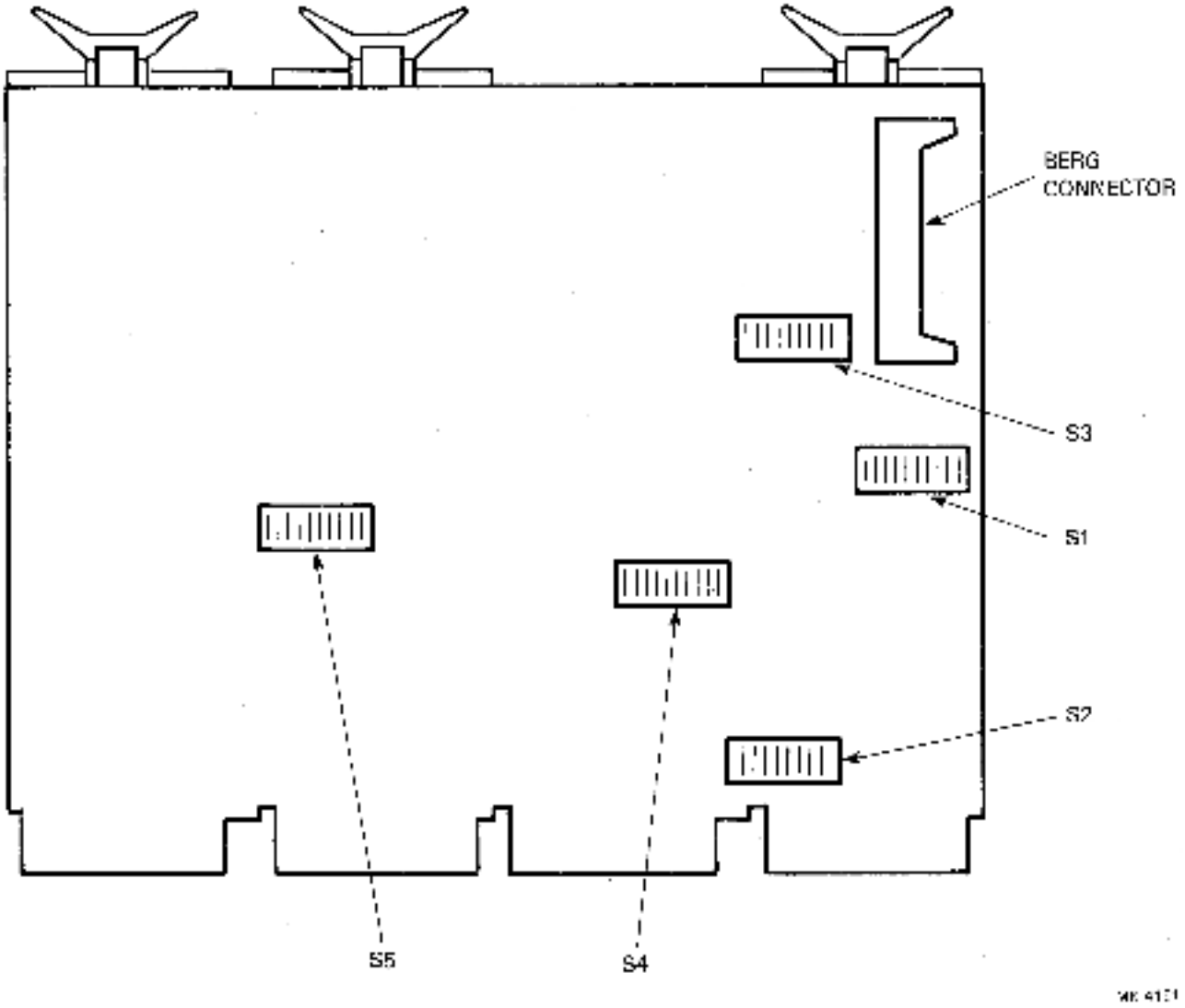


Figure 1-1 DL11-W (M7856)

The DL11-W interface provides the logic and buffer registers necessary for program-controlled transfer of data between a PDP-11 system requiring parallel data and an external device requiring serial data. The interface also includes status and control bits that may be controlled by the program, the interface, or an external device for command, monitoring, and interrupt functions.

The DL11-W interface provides the flexibility needed to handle a variety of terminals. For example, the user can use a DL11-W as a Teletype® control; or, in conjunction with another serial line interface, the DL11-W can be used as a communications link between two processor systems. The DL11-W provides the user with a choice of line speeds (baud rates), character size, stop code length, parity selection, and status indications.

The DL11-W can replace DL11-A, DL11-B, DL11-C, and DL11-D modules in most applications. However, the DL11-E is still required for use with communications data sets such as Bell Model 103 or 202. All of the features of the DL11-A through DL11-D modules are combined on the DL11-W and are switch-selectable to allow for interchangeability.

As a receiver of serial data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the Unibus. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When the DL11-W is used as a transmitter, a parallel character from the bus is converted to a serial character for transmission to an external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions and a data buffer register for storing data prior to transfer to the bus or external device. The line frequency clock uses a signal derived from the ac input voltage by the power supply to generate timed interrupts. The clock portion utilizes a register for command and monitoring functions.

Typically, the DL11-W is operated in one of two functionally different configurations. The DL11-W used as a Teletype control and the DL11-W used with EIA level converters will be discussed individually in the following paragraphs. The real-time clock functions will also be described.

1.3.1 DL11-W Teletype Control

The DL11-W (Figure 1-2) can be used to interface to Model 33, Model 35, and Model 38 Teletypes, and to the LA36.

Serial information read or written by the Teletype unit is assembled or disassembled by the DL11-W interface for parallel transfer to or from the Unibus. When the processor puts an address on the bus, the DL11-W interface decodes the address to determine if the Teletype is the selected external device and, if selected, whether it is to perform an input or output operation.

If, for example, the Teletype has been selected to accept information for printout, parallel data from the Unibus is loaded into the DL11-W transmitter (punch) buffer. At this point, the XMIT RDY flag drops because the transmitter (punch) logic has been activated. (The flag comes back after a fraction of a bit time if the transmitter is not presently active.) The interface generates a START bit, shifts the data from the buffer into the Teletype one bit at a time, resets the XMIT RDY flag (as soon as the holding register of the double-buffer is empty, even though the shift register is active), and then puts out the required number of STOP bits.

®Teletype is a registered trademark of Teletype Corporation.

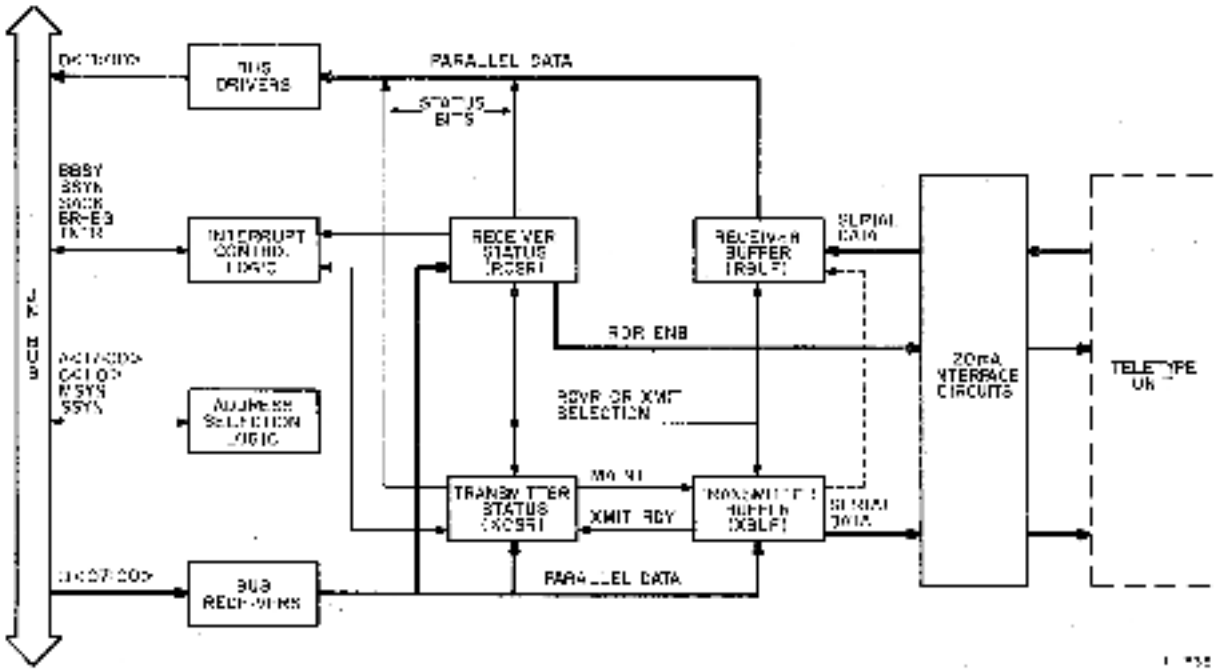


Figure 1-2 DL11-W Teletype Control

Thus, if the DL11-W is interfaced to a Model 33 Teletype, the 8-bit parallel bus data is converted to the 11-bit serial input required by the Teletype. Note that whenever a series of characters is to be output to the Teletype, the XMIT RDY flag is set prior to generation of the STOP bits and the shifting out of the character in the holding register, thus allowing another character to be loaded from the bus as soon as the transmitter holding buffer is empty. The XMIT RDY flag is used with XMIT INT ENB to initiate an interrupt sequence, informing the processor that the interface is ready to accept another character for transfer to the Teletype for printing.

When receiving data from the Teletype unit, the operation is essentially the reverse. The START bit of the Teletype serial data activates the interface receiver logic, and data is loaded one bit at a time into the reader buffer register. When buffer loading is complete, the buffer contents are transferred to the holding register and the interface sets the RCVR DONE flag, indicating to the program that a character has been assembled and is ready for transfer to the bus. If RCVR INT ENB is also set, the RCVR DONE flag initiates an interrupt sequence, thereby causing a vectored interrupt.

The DL11-W has a reader enable (RDR ENB) bit that can be set to advance the paper tape reader in the Teletype. When set, this bit clears the RCVR DONE flag. As soon as the Teletype sends another character, the START bit clears the RDR ENB bit, thus allowing just one character to be read.

The DL11-W also has a receiver active (RCVR ACT) bit, which indicates that the DL11-W interface is receiving data from the Teletype. This bit is set at the center of the START bit, which is the beginning of the input serial data, and is cleared by the leading edge of the RCVR DONE bit. The DL11-W also has a BREAK bit which can be switch-enabled. This bit can be set by the program to transmit a continuous space to the Teletype.

The DL11-W can be operated in a maintenance mode, which is program-selected by setting the MAINT bit in the transmitter status register. When in this mode, special logic is used to perform a closed loop test of interface logic circuits. A character from the bus is loaded into the transmitter (punch) buffer register. The serial output of the register enters the receiver (reader) buffer register, where it is converted back into parallel data and transferred to the bus. In the maintenance mode, the data is not transmitted to the Teletype. If the DL11-W is functioning properly, the character in the reader buffer (RBUF) is identical to the character loaded into the transmitter buffer (XBUF).

1.3.2 DL11-W EIA Terminal Control

The DL11-W also provides the control logic required for interfacing EIA terminals such as the VT06 display or the Model 37 Teletype (Figure 1-3).

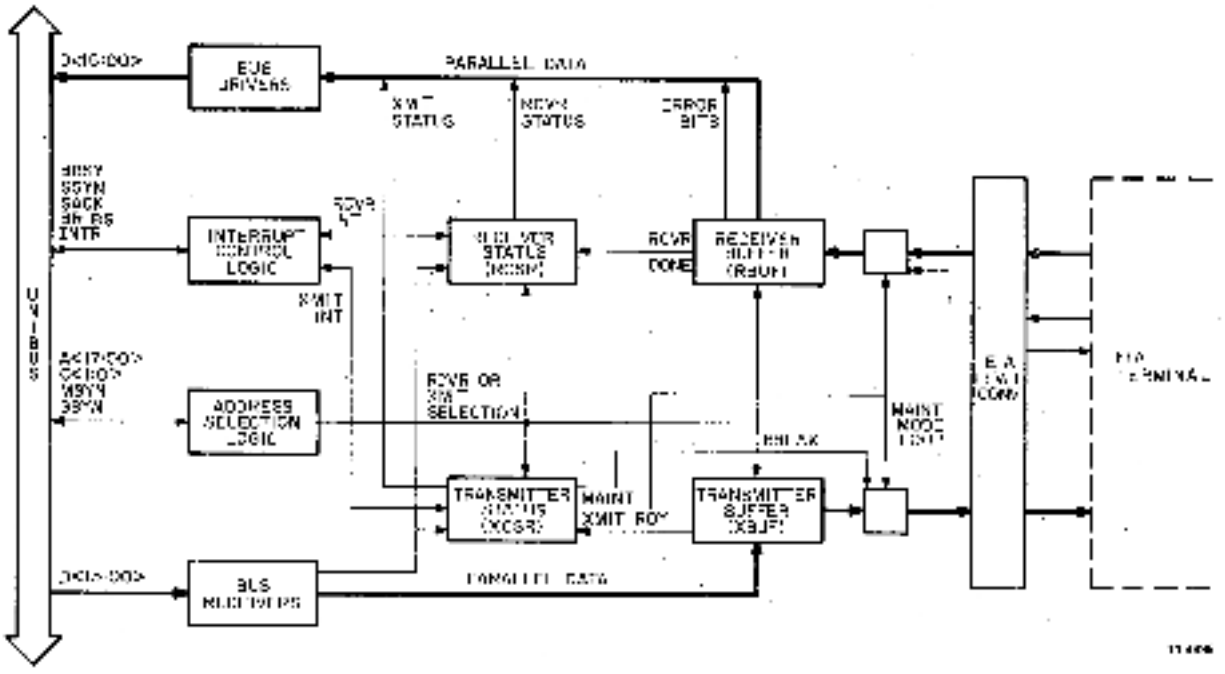


Figure 1-3 DL11-W Terminal Control

Functionally the EIA terminal control configuration is nearly identical to the Teletype control configurations. In the EIA terminal control configuration, EIA level converters on the DL11-W are used to change bipolar serial input data to TTL logic levels and TTL logic level serial output to the bipolar signals required by EIA terminals. EIA level outputs for the signals DATA TERMINAL RDY and REQ TO SEND are permanently strapped on. However, RDR ENB has no EIA level equivalent.

1.3.3 Line Time Clock (Figure 1-4)

A signal generated from the ac input line voltage by the power supply is received by the DL11-W. This signal is a square wave identical in frequency to the ac line voltage. A monitor bit (LTC MONITOR) on the line clock status register (LKS) is set once for each cycle by the hardware but must be cleared by the program. By monitoring this bit, the program can count unit time intervals of 16-2/3 ms (60 Hz) or 20 ms (50 Hz). If the LTC INT ENB bit is set, a vectored interrupt will be generated on each cycle.

The terms real-time clock (RTC) and line clock (LTC) are used interchangeably in other contexts, but line clock will be used generally in this manual for consistency.

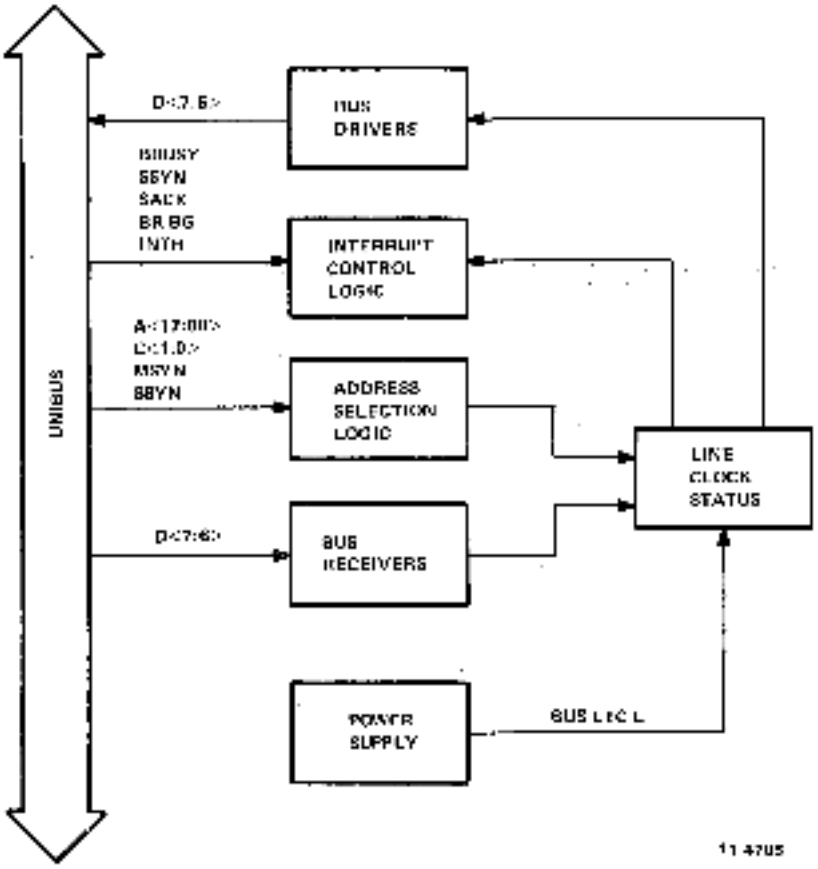


Figure 1-4 Line Clock Block Diagram

1.4 PHYSICAL DESCRIPTION

The DL11-W SLU/RTC option is packaged on a single M7856 quad integrated circuit module that can easily be plugged into a small peripheral controller slot in the processor or one of the slots in a DD11-D peripheral mounting panel.

Power is applied to the logic through the power harness already provided in the BA11 mounting box. The required current is approximately 2.0 A at +5 V and 150 mA at −15 V. If the EIA level outputs are used, then 50 mA of current, at a level between +9 V and +15 V, is also required.

The M7856 module has a Berg connector for all user input/output signals. The specific signals fed to this connector depend on the external device interfaced to, and the specific cable used. Mounting, cabling, and connector information is given in Chapter 2.

Figure 1-1 shows the position of the Berg connector and the five switch packs.

1.5 SPECIFICATIONS

Operating and physical specifications for the DL11-W Serial Line Unit/Real-Time Clock are given in Table 1-1.

Table 1-1 DL11-W Operating Specifications

Specification	Description
Registers	Receiver Status Register (RCSR) Receiver Buffer Register (RBUF) Transmitter Status Register (XCSR) Transmitter Buffer Register (XBUF) Line Clock Status Register (LKS)
Register Addresses	RCSR 777560 RBUF 777562 When used as console device XCSR 777564 XBUF 777566 LKS 777546 Valid when SLU is used as console or DL11-W is used as a line clock only. (See Table 4-2 for addresses other than console device).
Interrupt Vector Address	060 Receiver when used as console 064 Transmitter 100 Line Clock Floating Vectors (Appendix B)
Priority Level	BR4 SLU BR6 RTC
Interrupt Types	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor

Table 1-1 DL11-W Operating Specifications (Cont)

Specification	Description
Commands	Receiver Interrupt Enable (RCVR INT ENB) Transmitter Interrupt Enable (XMIT INT ENB) Line Clock Interrupt Enable (LKS INT ENB) Reader Enable (RDR ENB) Maintenance Mode (MAINT) Break (BREAK)
Status Indicators	Receiver Active (RCVR ACT) Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor Error (ERROR) Overrun (OR ERR) Framing Error (FR ERR) Parity Error (P ERR)
Data Input/Output	Serial data, 20 mA active current loop Serial data, 20 mA passive current loop Serial data, conforms to EIA and CCITT specifications.
Data Format	One START bit; 5-, 6-, 7-, or 8-bit DATA character; PARITY bit (odd, even, or unused); 1 or 2 STOP bits with 6, 7, 8 DATA bits selected; 1 or 1.5 STOP bits with 5 DATA bits selected.
Data Rates	Baud rates may be 110, 150, 300, 600, 1200, 2400, 4800, or 9600. Any split speed combination possible (transmitter and receiver speeds may differ).
Bit Transfer Order	Low-order bit (LSB) first
Parity	Computed on incoming data or inserted on outgoing data, depending on type of parity (odd or even) used. Parity may be odd, even, or unused.
Size	Consists of a single quad module (M7856) that occupies a slot in a DD11-C, DD11-D, or DD11-P backplane.
Power Required	2.0 A at +5 V 150 mA at –15 V 50 mA at level between +9 V and +15 V.
Temperature Range	10° to 50° C.

1.6 CABLES

The DL11-W comes in a package with a 7008360-9 cable and an H3009 panel assembly for use when interfacing via a 20 mA current loop. This kit is called the DL11-WA. The DL11-W also comes with a BC27C cable/panel assembly and a BC22D cable for interfacing to EIA devices. This kit is called the DL11-WB. The Berg connector on the M7856 module accepts the 7008360-9 cable and the BC27C cable.

CHAPTER 2
CONFIGURATION, INSTALLATION, AND TESTING

2.1 CONFIGURATION

The DL11-W includes an M7856 quad module, either of two distribution panels (BC27C or H3009), and associated interconnecting cables. Also included is an adaptor bracket for use in cabinets which do not require compliance with FCC regulations for electromagnetic interference (EMI) suppression. Table 2-1 lists the option specific components. Figure 2-1 shows all of the parts associated with the DL11-W interface.

The M7856 quad module includes five dip-mounted switch packs. Each pack contains either eight or ten individual slide or toggle switches. The packs are labeled S1 through S5 on the board; each switch on the packs is numbered 1 through 8 or 10. Positions for on and off are clearly indicated on the hardware. "SX-Y" is the convention used in this manual to refer to specific switches where X indicates the switch pack number and Y indicates the particular switch on that switch pack. For example, "S2-9" refers to switch number 9 on switch pack 2.

Switch selections on the DL11-W interface provide the flexibility needed to handle a variety of functions. For example, the user can set up switches so that the DL11-W can interface to a Teletypewriter or to a high-speed CRT terminal. The user has a choice of speeds, character size, stop code length, parity, error detection, 20 mA current loop or EIA, addresses and vectors, active or passive modes, and the specific type of interface which the DL11-W is to replace.

2.1.1 Baud Rates

Table 2-2 lists the eight different baud rates available on the DL11-W. Completely independent split-speed operation is provided so that the receiver and transmitter may operate at different rates. The user should be careful to set the correct speeds when replacing other interface modules (DL11-A, DL11-B, and so on).

2.1.2 Address and Vector Selection

The DL11-W interface is addressed through the address selection logic, and its interrupt vector is determined by the interrupt control logic. Each DL11-W interface within a system has a unique address and a unique vector. These are determined by the switches on the module. However, the line clock address and vector are fixed at 777546 and 100, respectively. Figure 2-2 shows the relation of specific switches to the address and vector of the device used (Teletypewriter and so on).

Thus, for address selection, switch S5-3 corresponds to address bit 10, and it indicates a logical 1 when turned off. For vector selection, on the other hand, switch S2-3 corresponds to vector bit 5, and it indicates a logical 1 when it is on.

All PDP-11 systems have enough I/O addresses reserved to handle up to 47 devices. Each one of these devices could be a DL11-W. However, only one DL11-W per system is allowed to have the LTC enabled. The LTC sections of other DL11-Ws can be disabled by turning switches S5-9 on S5-10 off. See Table 4-2 for more specific address configuration information.

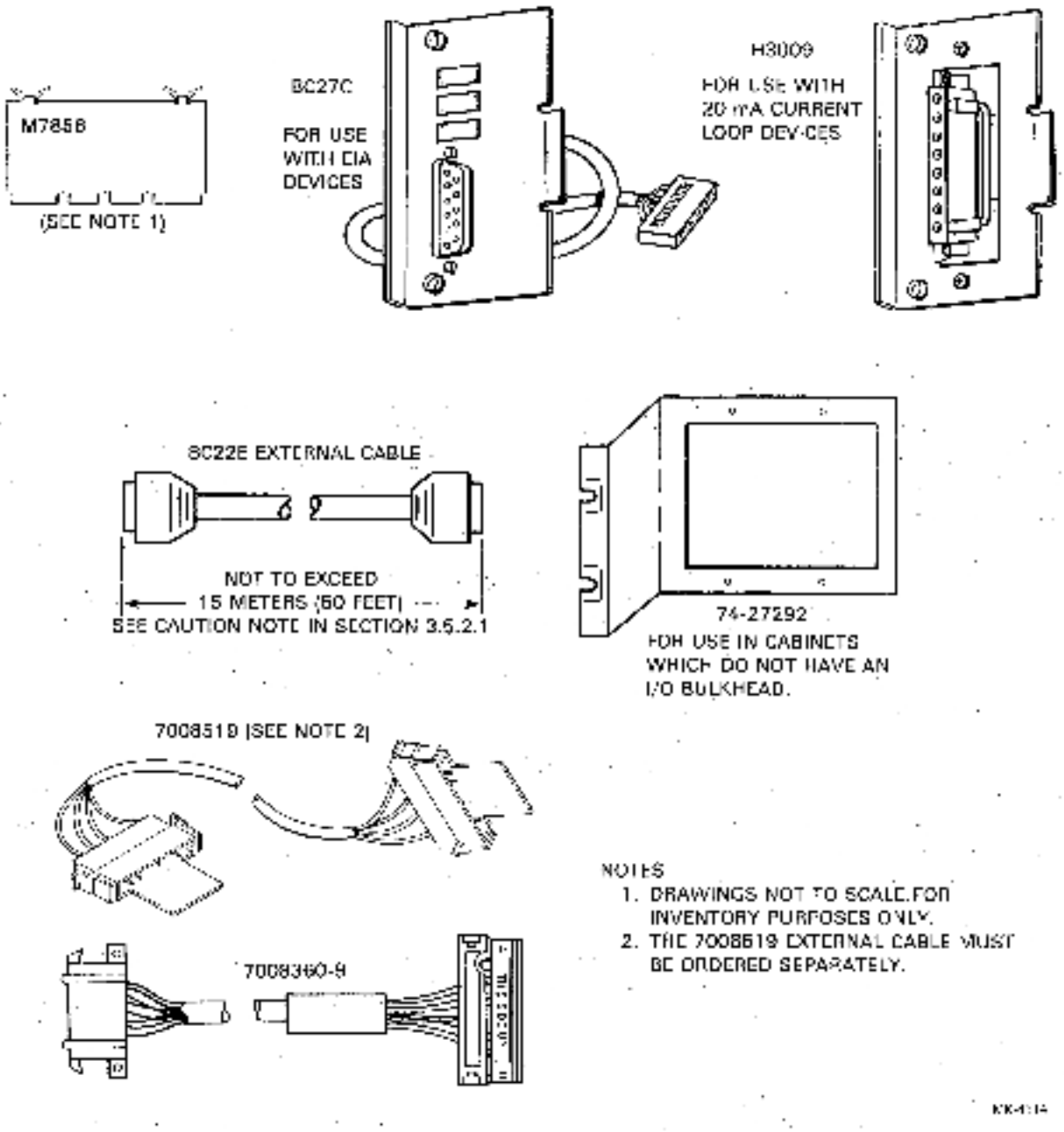


Figure 2-1 DL11-W Parts Diagram

Table 2-1 Option Configurations

Configuration	Module	Cable	Distribution Panel
DL11-W	M7856	NONE	NONE
DL11-WA	M7856	7008360-9	H3009
DL11-WB	M7856	BC05C* BC22E	BC27C

* A BC05C cable and BC27C panel comprise the BC27C cable/panel assembly.

Table 2-2 DL11-W Baud Rates

Baud Rate	Transmit			Receive		
	S4-10	S3-1	S3-4	S3-2	S3-3	S3-5
110	ON	ON	ON	OFF	OFF	OFF
150	OFF	ON	ON	ON	OFF	OFF
300	ON	OFF	OFF	OFF	ON	ON
600	ON	OFF	ON	OFF	ON	OFF
1200	ON	ON	OFF	OFF	OFF	ON
2400	OFF	OFF	OFF	ON	ON	ON
4800	OFF	OFF	ON	ON	ON	OFF
9600	OFF	ON	OFF	ON	OFF	ON

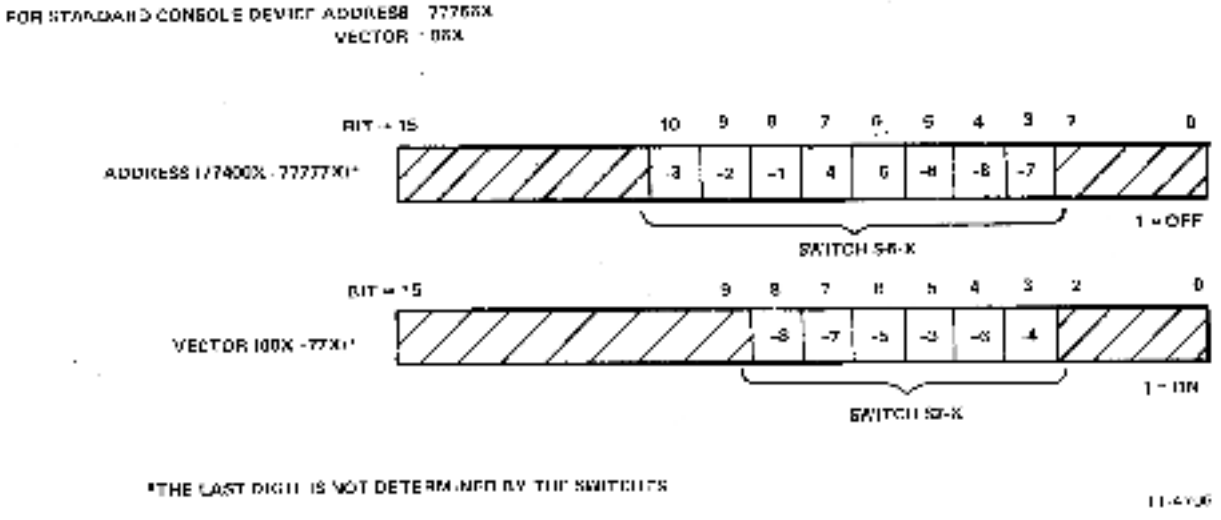


Figure 2-2 Address and Vector Selection

2.1.3 Address Selection Modes

The DL11-W can be operated in any of three different address selection modes. Normally, a DL11-W used as console terminal control would operate in the first mode, whereas additional DL11s would be operated in the second mode. The third mode is not normally used, but is discussed here for completeness.

Mode 1: Both the serial line unit and the line clock sections can be addressed. Due to common address selection logic, operation in this mode requires that the serial line unit addresses be restricted to 77756X. The line clock address is 777546.

Mode 2: Only the serial line unit section can be addressed. Address selection ranges from 774000 to 777776. The line clock is disabled and does not respond to address 777546.

Mode 3: Only the line clock section can be addressed at 777546. The serial line unit section does not respond to any address.

Table 2-3 indicates the correct switch setting for selection of the desired address and address mode.

Table 2-3 Address and Mode Selection

Address Bit	A10	A09	A08	A07	A06	A05	A04	A03	LTC	LTC
Switch	S5-3	S5-2	S5-1	S5-4	S5-5	S5-6	S5-8	S5-7	S5-9	S5-10
Mode 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
Mode 2*	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
Mode 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

* Address 77756X is selected for the serial line interface. Other addresses may be selected using switches shown in Figure 2-2, where OFF = 1 and ON = 0.

2.1.4 Active and Passive Modes

Two switch-selectable modes of operation are available for the 20 mA current loop. In the active mode, the DL11-W is the source for the 20 mA of current; in the passive mode, the external device must provide the current. As an example, two processing systems could be connected using two DL11-Ws via the 20 mA current loop. One DL11-W would be the active device. The other DL11-W would be passive. Table 2-4 shows the appropriate switch settings. Normal configuration is in the active mode.

2.1.5 Data Format

The data format (Figure 2-3) consists of a START bit, five to eight DATA bits, a PARITY bit or no PARITY bit, and one, one and one-half, or two STOP bits.

When less than eight DATA bits are selected, the hardware justifies the bits into the least significant bit positions for characters received by the interface. When transmitting characters, the program provides the justification into the least significant bits. The PARITY bit may be either on or off; when on, it can be selected for checking either odd or even parity when receiving and for providing an extra PARITY bit during transmission.

Table 2-4 Switch Settings

	Transmitter				
	S1-1	S1-2	S1-3	S1-6	S1-7
Active	ON	ON	OFF	OFF	ON
Passive	OFF	OFF	ON	ON	OFF
	Receiver				
	S3-6	S3-7	S3-8	S3-9	S3-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF
	Paper Tape Reader Enable				
	S1-4	S1-5	S1-8	S1-9	S1-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

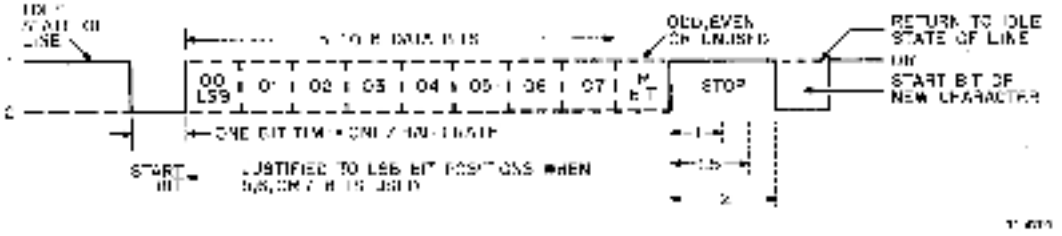


Figure 2-3 DL11-W Data Format

All variable items within any data format are selected by switches on the DL11-W module. None of the variables can be controlled by the program. These switches are listed in Table 2-5 and described more fully in Chapter 4.

Figure 2-4 shows typical switch settings for a DL11-W when interfacing with a standard DIGITAL terminal (console device only).

Table 2-6 gives a complete listing of the switches and their functions.

2.1.6 Cabling

Figure 2-5 illustrates the proper cabling configuration for selecting and connecting cables between the DL11-W and various peripheral devices.

2.2 PREINSTALLATION AND SET-UP PROCEDURES

Before installing the DL11-W, assign device and vector addresses in accordance with Section 2.1.2.

Table 2-5 Data Format Switches

Name	Switch	UART Pin No.	Function
No Parity	S4-6	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select (S4-2) switch. When disabled, the STOP bits immediately follow the last DATA bit during transmission. During reception, the receiver does not check for parity. Switch ON = parity enabled Switch OFF = parity disabled
Even Parity	S4-2	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. Switch ON = odd parity Switch OFF = even parity
STOP Bit	S4-5	36	Selects the desired number of stop bits. Switch ON = One STOP bit. Switch OFF = Two STOP bits, but if five DATA bits are selected, one and one-half STOP bits will be selected.
Number of DATA bits	S4-3 S4-4	38 37	These two switches are used together to provide a code that selects the desired number of DATA bits in the character.

S4-4	S4-3	No. of DATA Bits
ON	ON	5
ON	OFF	6
OFF	ON	7
OFF	OFF	8

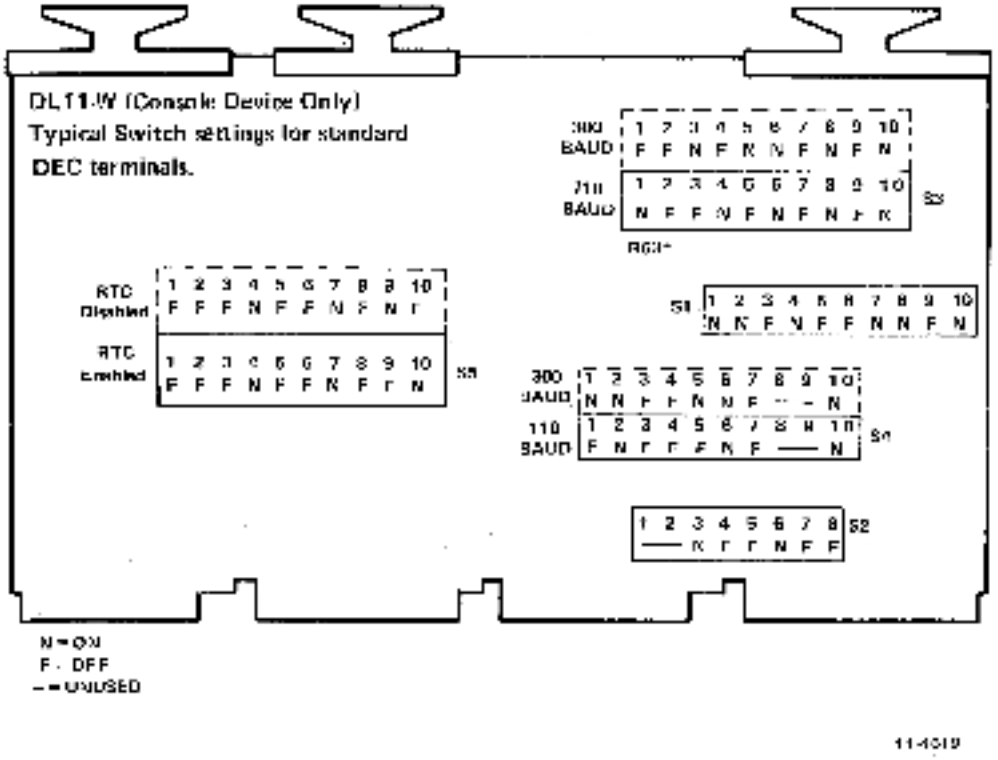


Figure 2-4 Typical Switch Settings

Table 2-6 DL11-W Switch Functions

Switch Pack	Switch No.	Function
1	1 2 3	Transmitter (active/passive mode of 20 mA loop)
	4 5	Reader enable (active/passive mode of 20 mA loop)
	6 7	Transmitter (active/passive mode of 20 mA loop)
	8 9 10	Reader enable (active/passive mode of 20 mA loop)
2	1 2	Not functional
	3 4 5 6 7 8	Vector address

Table 2-6 DL11-W Switch Functions (Cont)

Switch Pack	Switch No.	Function
3	1	Transmitter baud rate
	2, 3	Receiver baud rate
	4	Transmitter baud rate
	5	Receiver baud rate
	6, 7, 8, 9, 10	Receiver (active/passive mode of 20 mA loop)
4	1	Break enable
	2	Parity select (odd or even)
	3, 4	Number of DATA bits
	5	Number of STOP bits
	6	Parity enable
	7	Error bit enable
	8, 9	Not functional
	10	Transmitter baud select
5	1, 2, 3, 4, 5, 6, 7, 8	Device address
	9, 10	Line clock enable

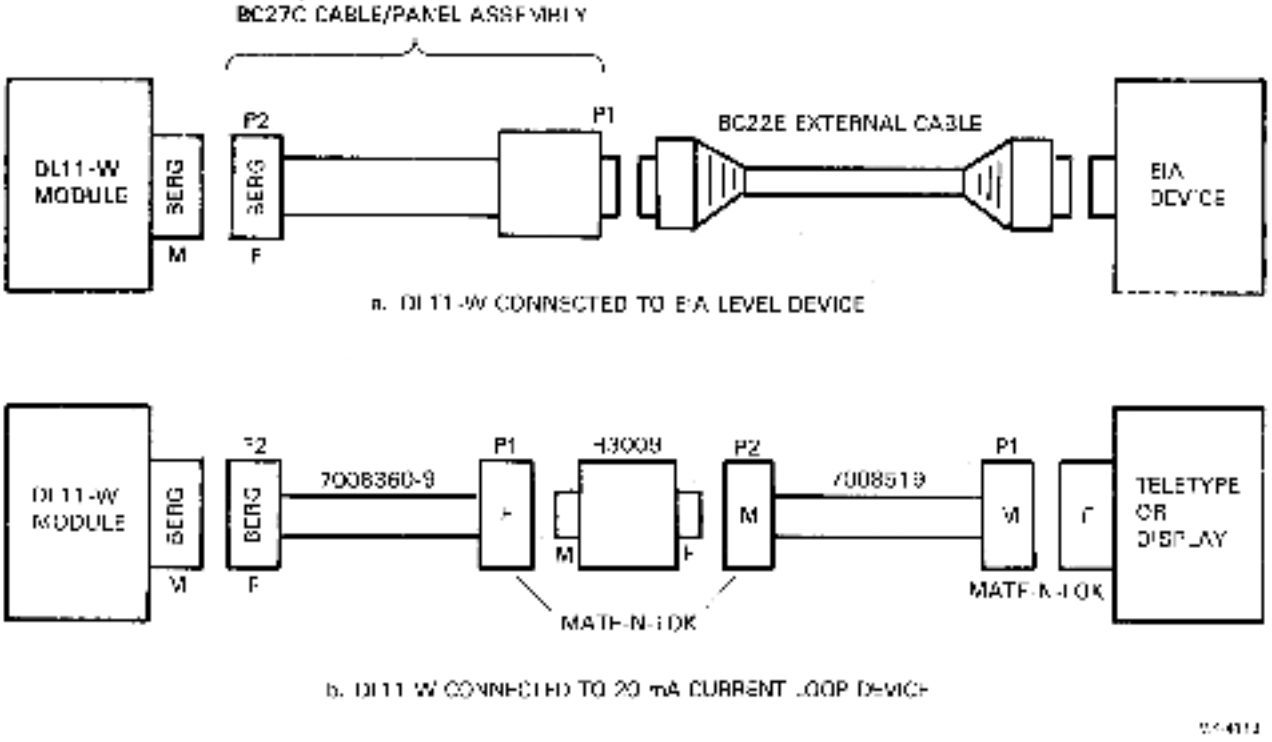


Figure 2-5 DL11-W Cable Connections

2.3 INSTALLATION

This section identifies the installation procedures for the DL11-W. Installation is broken down into M7856 module installation and distribution panel installation.

WARNING
When performing any installation procedures, turn all power OFF.

2.3.1 M7856 Module Installation

The DL11-W can be installed in any small peripheral controller (SPC) slot of the PDP-11 processor. Figure 2-6 illustrates a typical 9-slot backplane configuration (DD11-D).

1. Plug the female Berg connector (P-1) of the desired internal cable (see Figure 2-5) into the Berg connector (J1) of the M7856 module. The Berg connector is shown in Figure 1-1.

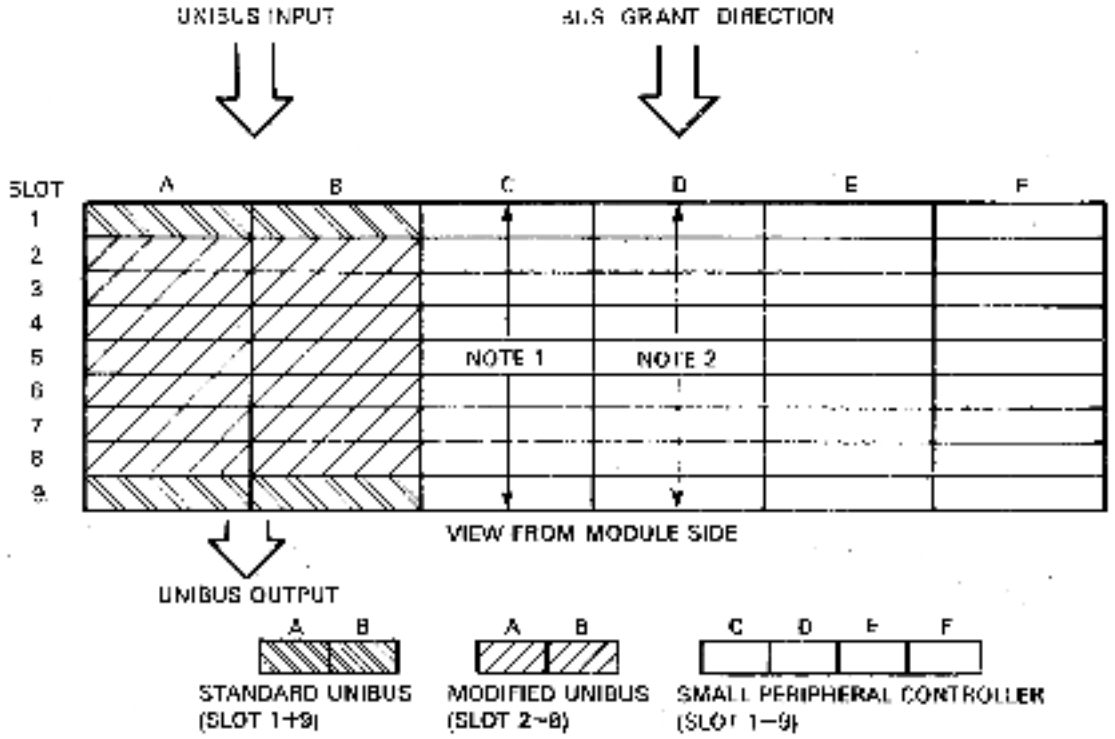
2. Install the M7856 module into the system unit.

3. Perform resistance checks between the backplane voltage sources and ground to ensure that no short circuit conditions exist on the M7856 module. Refer to the engineering print set *DL11-W SLI/RTC Option Engineering Drawings* for pin assignments.

4. Proceed to Section 2.3.2.

2.3.2 Distribution Panel Installation

Because the installation procedures for installing the BC27C and H3009 distribution panels are similar, the following instructions pertain to both panels.



NOTES:

1. REMOVE CA1 TO CB1 WIRE WRAP JUMPER TO INSTALL AN NPR OPTION IN ANY SPC SLOT.
2. G727 REQUIRED IN ANY UNUSED SPC SLOT TO PROVIDE BUS GRANT CONTINUITY

MR-1130

Figure 2-6 DD31-D Backplane

Two different approaches for installing distribution panel assemblies are included in this manual.

Most new installations utilize I/O bulkheads to comply with TCC regulations limiting EMI leakage. For installations utilizing an I/O bulkhead, follow the steps outlined in Section 2.3.2.1.

Alternate instructions are included for those cabinets that do not require I/O bulkheads and thus require a slightly modified installation procedure. If the system does not incorporate an I/O bulkhead, follow the steps outlined in Section 2.3.2.2.

2.3.2.1 Installation in Cabinets with an I/O Bulkhead – Though there may be differences in the positioning of the I/O bulkheads of the PDP-11 kernel cabinet, the universal expansion cabinet, and other cabinets, the installation concept is the same. Once the BC27C or H3089 distribution panel is installed, there should be no openings left (panels omitted) in the I/O frame on the rear of the cabinet which could permit EMI leakage. For this reason, it is important to tighten all mounting screws in the distribution panel. Figures 2-7 and 2-8 show the various I/O bulkhead types and illustrate the correct approach to each.

1. Gain access to the I/O bulkhead through the door on the rear of the system cabinet and remove one of the 4.57 cm (2 in) wide panels from the bulkhead. This is where the distribution panel is mounted.

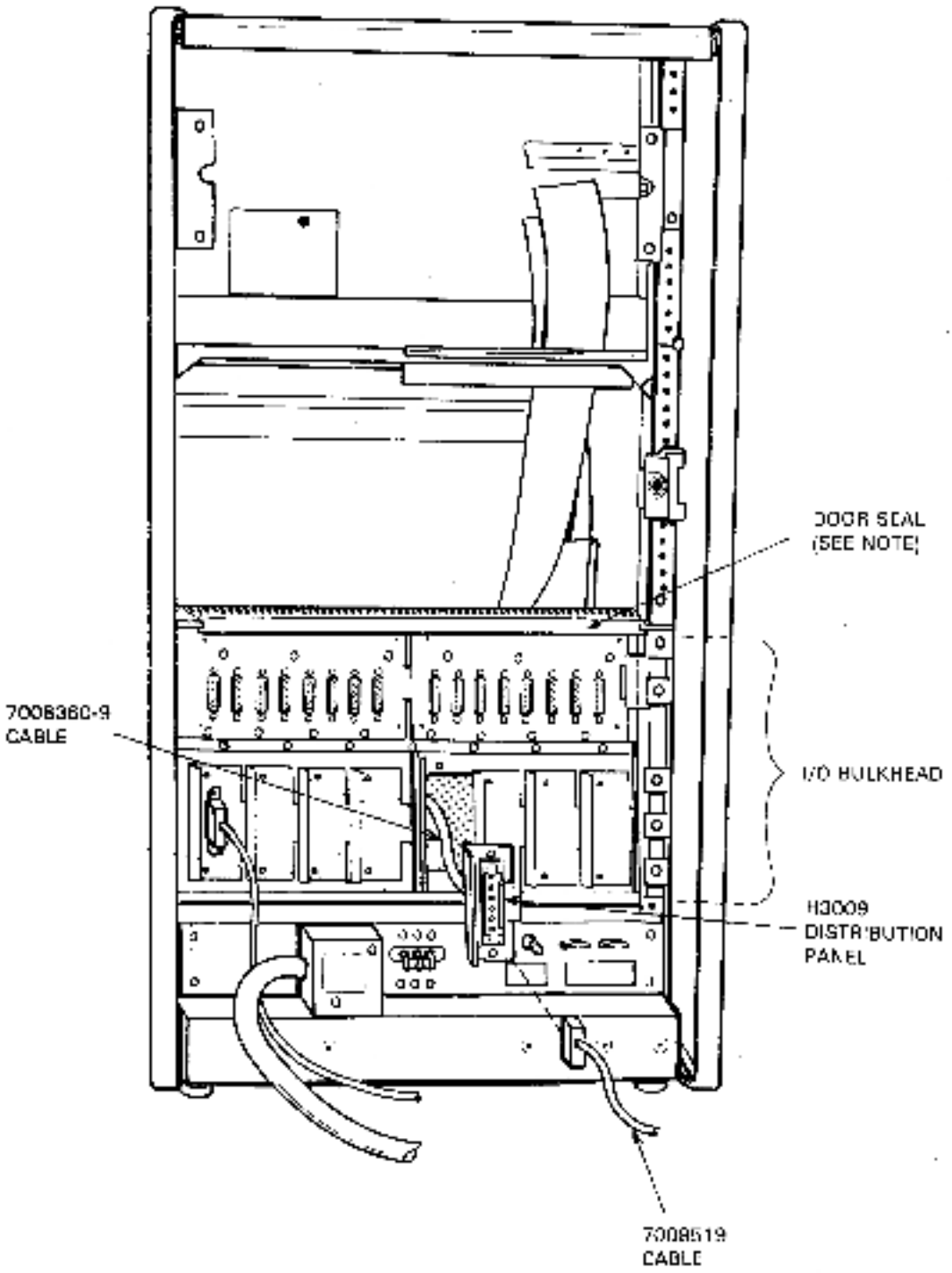


Figure 2-7 H3009 Installation in a Horizontally Oriented I/O Bulkhead

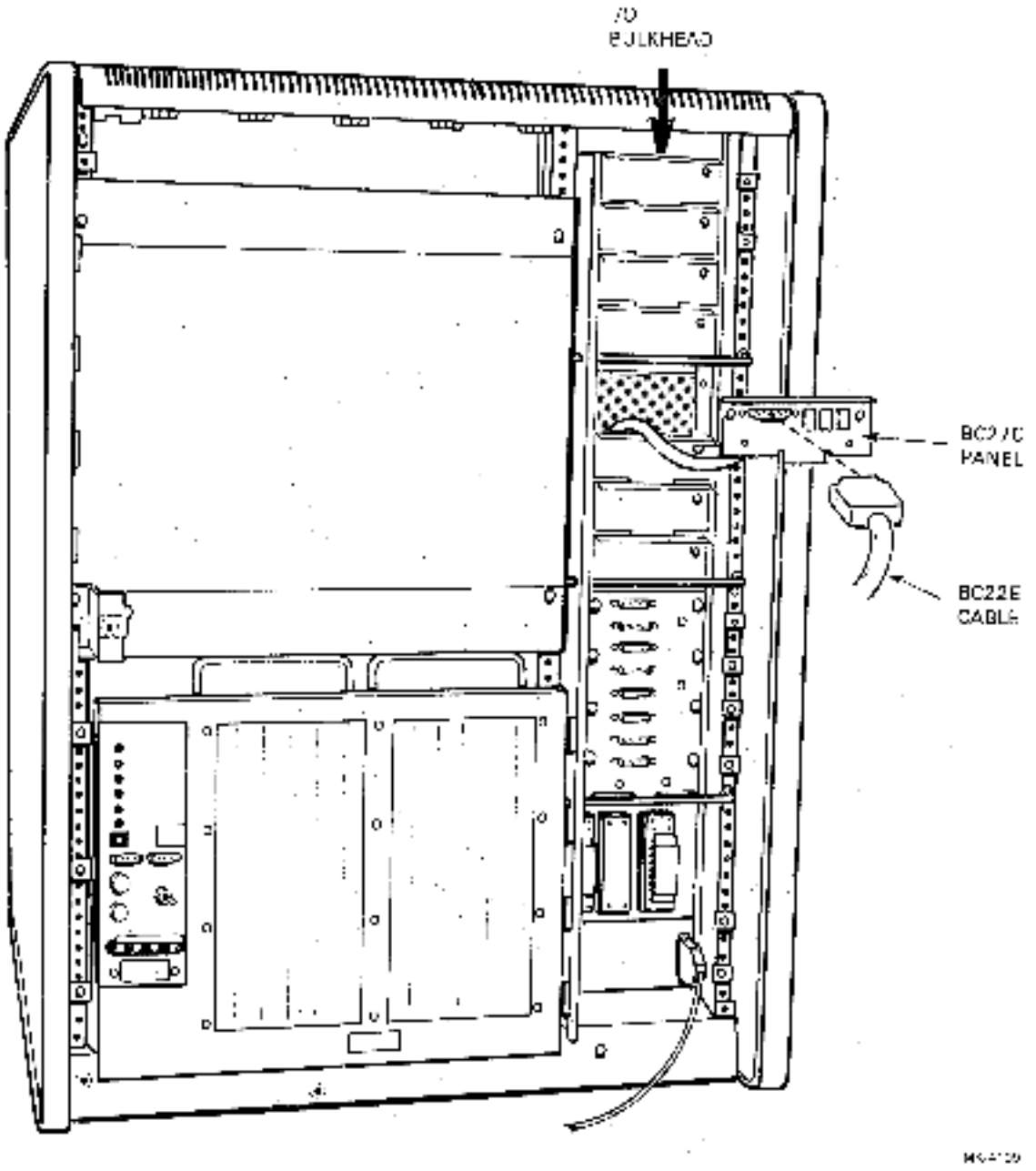


Figure 2-8 BC27C Installation in a Vertically Oriented I/O Bulkhead

2. When using the 7008360-9 cable and H3009 panel, plug the connector (P-2) of the free end of the cable into the male connector on the rear of the H3009 panel. When using the BC27C cable/panel assembly, this step may be omitted since the cable and panel are already connected.

3. Route the remaining internal cable and distribution panel through the cabinet and through the opening in the I/O bulkhead at the rear of the cabinet. Keep in mind that the cable must be routed and dressed in a manner compatible with existing cabinet cabling.

4. Install the distribution panel into the opening of the I/O bulkhead (see Figures 2-7 and 2-8) in place of the 4.57 cm (2 in) wide panel that was removed in Step 1.

NOTE

It is necessary to maintain an interference-free environment outside the cabinet enclosure. Any additional panels that may have been removed to facilitate easier installation of the distribution panel must be replaced.

5. Connect the correct external cable to the connector on the rear of the distribution panel (see Section 2.1.6). The cable should exit the cabinet with the other signal cables.

CAUTION

BC22E cable lengths in excess of 7.62 m (25 feet) may violate the maximum capacitance allowed by the RS-232-C specification. Note, however, that up to 15 m (50 feet) provides satisfactory DL11-W performance levels.

6. Connect the other end of the external cable to the connector on the peripheral device.

7. Turn the power ON.

2.3.2.2 Installation in Cabinets Without an I/O Bulkhead –

1. Gain access to the rear of the system cabinet and mount the adaptor bracket (Part No. 74-27292) to one of the rear vertical mounting rails as shown in Figure 2-9. Mounting the bracket on either side of the cabinet is permissable.

2. When using the 7008360-9 cable and H3009 panel, plug the connector (P-2) of the free end of the cable into the male connector on the rear of the H3009 panel. When using the BC27C cable/panel assembly, this step may be omitted since the cable and panel are already connected.

3. Route the remaining internal cable and distribution panel through the cabinet and through the adaptor bracket at the rear of the cabinet. Keep in mind that the cable must be routed and dressed in a manner compatible with existing cabinet cabling.

4. Connect the external cable to the connector on the rear of the distribution panel (see Section 2.1.6). The cable should exit the cabinet with the other signal cables.

CAUTION

BC22E cable lengths in excess of 7.62 m (25 feet) may violate the maximum capacitance allowed by the RS-232-C specification. Note, however, that up to 15 m (50 feet) provides satisfactory DL11-W performance levels.

5. Connect the other end of the external cable to the connector on the peripheral device.

6. Turn the power ON.

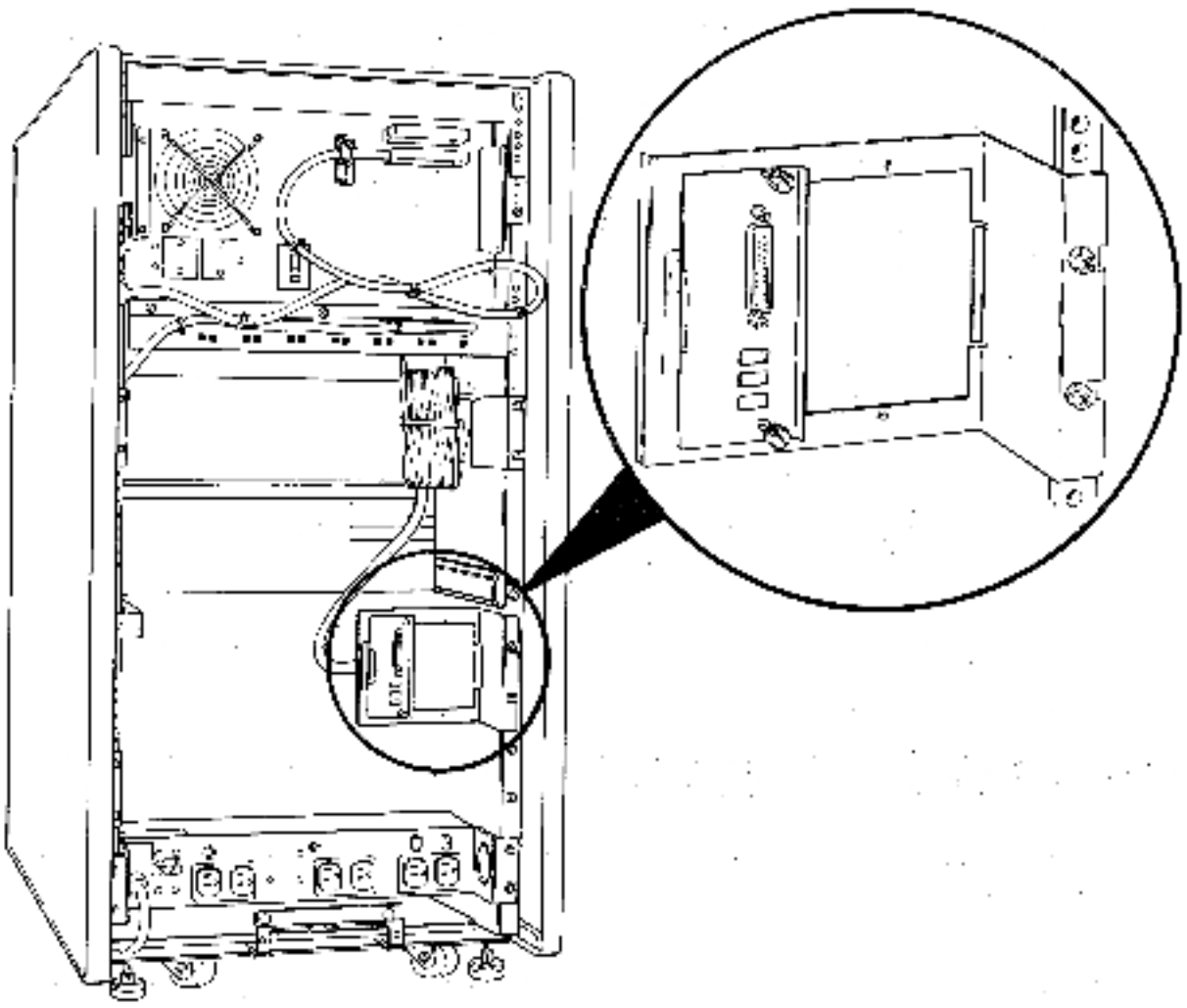


Figure 2-9 BC27C Panel Installed in an Adaptor Bracket

2.4 PIN INTERCONNECTION

Table 2-7 lists the signal names and associated pins on the Berg connector mounted on the M7856 module. This table also lists the signals supplied on the 7008360-9/H3009 and BC27C cables.

Table 2-8 provides a quick reference of M7856 input/output signals for TTL, EIA, and 20 mA current loop devices.

Table 2-9 lists connector pin numbers and signals for the 7008360-9 cable.

Table 2-10 lists connector pin numbers and signals for the 7008519 external cable which is used in conjunction with the 7008360-9/H3009 assembly cable.

Table 2-11 lists connector pin numbers for the BC27C cable connectors.

Table 2-7 Pin Connections

Berg Pin	M7856 Module	BC27C Modem Cable	7008360-9 Cable
A	Ground	Ground	Ground
B	Ground	Ground	
C		Force Busy	
D		Secondary Clear to Send	
E	Serial Input (TTL)	Interlock In	Interlock In
F	Serial Output (EIA)	Transmitted Data	
H	20 mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	+Serial Input (20 mA)		+Received Data
L		External Clock	
M	EIA Interlock	Interlock Out	
N		Serial Clock Xmit	
P		Secondary Request to Send	
R		Serial Clock Receiver	
S	-Serial Input (20 mA)		-Received Data
T		Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W		-Power	
X		Ring	
Y		+ Power	
Z		Data Set Ready	
AA	+Serial Output (20 mA)		+Transmitted Data
BB		Carrier	
CC			
DD	Data Terminal Ready (EIA)	Data Terminal Ready	
EE	-Reader Run (20 mA)		-Reader Run
FF		202 Secondary Transmit	
HH			
JJ		202 Secondary Receive	
KK	-Serial Output (20 mA)		-Transmitted Data
LL		EIA Secondary Transmit	
MM		Signal Quality	
NN		EIA Secondary Receive	
PP	+Reader Run (20 mA)		+Reader Run
RR		Signal Rate	
SS			
TT	+5 V		
UU	Ground	Ground	Ground
VV	Ground	Ground	Ground

Table 2-8 Input/Output Signals M7856

Type	Signals		Pin No.
TTL Signals	INPUT	Serial Data	E
20 mA Current Loop Signals	INPUT	+Serial Data	K
		−Serial Data	S
	OUTPUT	+Serial Data	AA
		−Serial Data	KK
		+Reader Run	PP
		−Reader Run	EE
EIA Signals	INPUT	Serial Data	J
	OUTPUT	Serial Data	F
		Request to Send	V
		Data Terminal Ready	DD

Table 2-9 7008360-9 Connections

Twisted Pair	Color	Mate-N-Lok Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Black/Red	Black	2	KK	−Transmitted Data
	Red	3	S	−Received Data
Black/White	Black	3	EE	−Reader Run
	White	5	AA	+Transmitted Data
Black/Green	Black	6	PP	+Reader Run
	Green	7	K	+Received Data
			E	Interlock In
			H	Interlock Out

NOTES:

1. Connector on ASR Teletype uses all pins (2–7).
2. Connector on KSR Teletype does not use pins 4 or 6 (Reader Run, – and +).

Table 2-10 7008519 Connections

7008360-9 Mate-N-Lok Connector P1	Mate-N-Lok Connector P2 (To 7008360-9)	Color	Mate-N-Lok Connector P1 (To Device)	Signal
2	2	Black	2	−Transmitted Data
3	3	Red	3	−Received Data
5	5	White	5	+Transmitted Data
7	7	Green	7	+Received Data

Table 2-11 BC27C Connections

Color	Cinch Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Blue/White	1	A	Ground
		VV	Ground
White/Blue	2	F	Transmitted Data
Orange/White	3	J	Received Data
White/Orange	4	V	Request to Send
Green/White	5	T	Clear to Send
White/Green	6	Z	Data Set Ready
Brown/White	7	B	Ground
		UU	Ground
White/Brown	8	BB	Carrier
Slate/White	9	Y	+Power
White/Slate	10	W	−Power
Blue/Red	11	FF	202 Secondary Transmit
Red/Blue	12	JJ	202 Secondary Receive
Orange/Red	13	D	Secondary Clear to Send
Slate/Red	14	LL	EIA Secondary Transmit
Slate/Green	15	N	Serial Clock Transmit
Red/Brown	16	NN	EIA Secondary Receive
Slate	17	R	Serial Clock Receive
Red/Slate	18	O	Unassigned
Blue/Black	19	P	Secondary Request to Send
Black/Blue	20	DD	Data Terminal Ready
Orange/Black	21	MM	Signal Quality
Black/Orange	22	X	Ring
Green/Black	23	RR	Signal Rate
Brown/Red	24	L	External Clock
Red/Orange	25	C	Force Busy
		E	Interlock In
		M	Interlock Out

2.5 INSTALLATION TESTING

Installation testing is performed by running the diagnostic programs after the DL11-W interface has been completely installed. The diagnostic programs and their operating instructions are supplied with the DL11-W interface.

The diagnostics supplied with the interface are:

1. MD-11-CZDLA**
2. MD-11-CZDLB**
3. DEC/X11 CXDLA**

Make three error-free passes of each diagnostic to ensure proper DL11 operation.

CHAPTER 3
PROGRAMMING INFORMATION

3.1 SCOPE

This chapter presents general programming information for software control of the DL11-W Serial Line Unit/Real-Time Clock Option. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook* (DEC-11-GGPB-D).

This chapter is divided into three major portions: device registers, interrupts, and fitting considerations.

3.2 DEVICE REGISTERS

All software control of the DL11-W SLU/RTC Option is performed by means of five device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction which refers to their addresses. Address assignments can be changed by altering the setting of switches on the address selection logic to correspond to any address within the range of 774000 to 777777. However, register addresses for the DL11-W normally fall within the range of 775610 to 776176 or 776500 to 776670. An explanation of the addressing scheme is offered in Chapter 4 of this manual. For the remainder of this discussion, it is assumed that the DL11-W is being used as a console terminal control.

The five device registers and associated bus addresses are listed in Table 3-1.

Table 3-1 Standard DL11-W Register Assignments

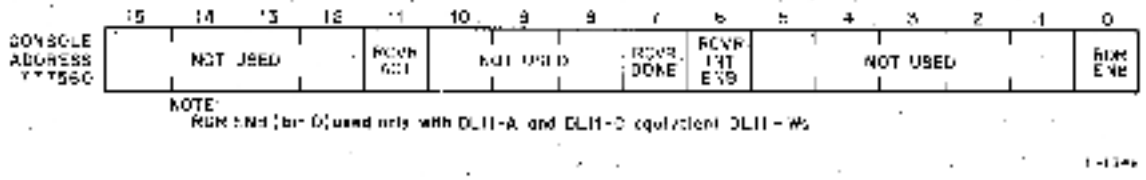
Register	Mnemonic	Address*
Receiver Status	RCSR	777560
Receiver Buffer	RBUF	777562
Transmitter Status	XCSR	777564
Transmitter Buffer	XBUF	777566
Line Clock Status	LKS	777546†

*These addresses are only for a DL11-W used as console terminal control. For other address assignments for these registers, refer to Table 4-2.

†This address is valid only on a DL11-W used as a console terminal. On any other DL11-Ws used in a system, this register should be disabled.

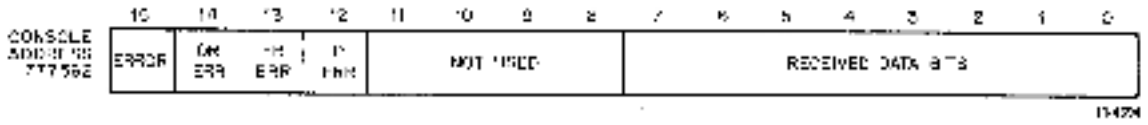
Figures 3-1 through 3-5 show the bit assignments for the device registers. The unused and write-only bits are always read as 0s. Writing unused or read-only bits has no effect on the bit position but is not considered good programming practice. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction, pressing the START switch on the processor console, or the occurrence of a power-up or power-down condition on the processor power supply.

In the descriptions accompanying the figures, "transmitter" refers to those registers and bits involved in accepting a parallel character from the Unibus for serial transmission to the external device. "Receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the Unibus.



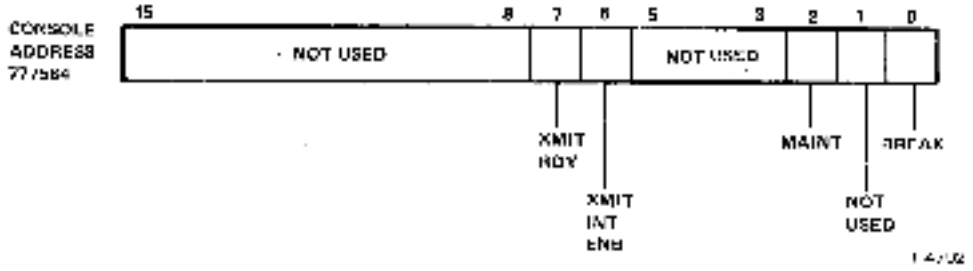
Bit	Meaning and Operation
15–12	Unused
11	Receiver Active – Read-only. When set, this bit indicates that the receiver interface is active. This bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and cleared by the leading edge of Receiver Done. Also may be cleared by INIT.
10–8	Unused
7	Receiver Done – Read-only. Set when an entire character has been received and is ready for transfer to the Unibus. Cleared by setting Reader Enable, addressing (read or write) RBUF, or INIT. Starts an interrupt sequence when receiver interrupt enable (bit 6) is also set.
6	Receiver Interrupt Enable – Read/write. Cleared by INIT. Starts an interrupt sequence when Receiver Done is set.
5–1	Unused
0	Reader Enable – Write-only. Cleared by INIT or at the middle of a START bit. Advances paper tape reader of ASR Teletypes. Clears Receiver Done. The 20 mA current loop circuit output is associated with this bit.

Figure 3-1 Receiver Status Register Bit Format



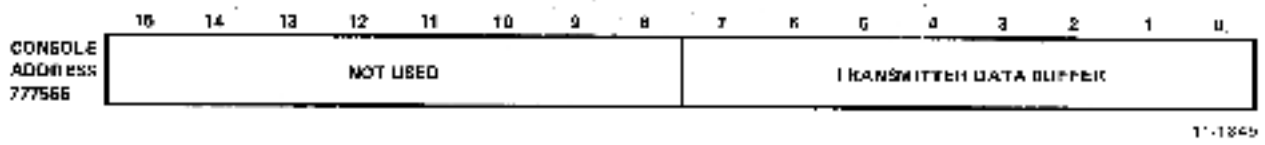
Bit	Meaning and Operation
15	Error – Read-only. Logical OR of Overrun, Framing Error, and Parity Error. Cleared by removing the error conditions. Error is not tied to the interrupt logic.
14	Overrun – Read-only. Set if previously received character is not read (Receiver Done not reset) before the present character is received.
13	Framing Error – Read-only. Set if the character read has no valid STOP bit. Also used to detect Break.
12	Receive Parity Error – Read-only. Set if received parity does not agree with the expected parity. Always 0 if no parity is selected.
	NOTE Error conditions remain until the next character is received, at which time the error bits are updated. INIT does not necessarily clear the error bits. Error bits may be disabled altogether via a switch, but not individually.
11–8	Unused
7–0	Received Data Bits – Read-only. These bits contain the character just read. If less than 8 bits are selected, the data will be right-justified into the least significant bits, and the higher unused bit or bits will be read as 0s. Not cleared by INIT.

Figure 3-2 Receiver Data Buffer Bit Format



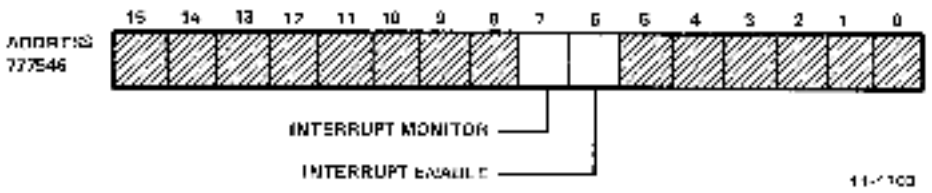
Bit	Meaning and Operation
15–8	Unused
7	Transmitter Ready – Read-only. Set by INIT. Cleared when XBUF is loaded; set when XBUF can accept another character. When set it will start an interrupt sequence if Transmitter Interrupt Enable is also set.
6	Transmitter Interrupt Enable – Read/write. Cleared by INIT. When set it will start an interrupt sequence if Transmitter Ready is also set.
5–3	Unused
2	Maintenance – Read/write. Cleared by INIT. When set, it disables the serial line input to the receiver and sends the serial output of the transmitter into the serial input of the receiver. Forces receiver to run at transmitter speed.
1	Unused
0	Break – Read/Write. Cleared by INIT. When set, it transmits a continuous space. May be disabled via a switch.

Figure 3-3 Transmitter Status Register Bit Format



Bit	Meaning and Operation
15–8	Unused
7–0	Transmitted Data Buffer – Write-only. If less than eight bits are selected, the character must be right-justified into the least significant bits.

Figure 3-4 Transmitter Data Buffer Bit Format



Bit	Meaning and Operation
15–8	Unused
7	Line Clock Monitor – Read/clear. Set by the line frequency clock signal and cleared only by the program. Set by INIT.
6	Line Clock Interrupt Enable – Read/write. Cleared by INIT. When set, starts an interrupt sequence if Line Clock Monitor is also set. An interrupt sequence will also be initiated upon the reception of the line frequency clock signal if the Line Clock Monitor bit is set from a previous clock signal.
5–0	Unused

Figure 3-5 Clock Status Register Bit Format

3.3 INTERRUPTS

The DL11-W interface uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing transfer of control to a handling routine. The DL11-W has three interrupt channels: one for the receiver section, one for the transmitter section, and one for the line clock section. These three channels operate independently. However, if simultaneous interrupt requests occur, the line clock has highest priority, followed by the receiver. The transmitter is last.

A line clock interrupt can occur only if the LKS interrupt enable bit (bit 6) in the line clock status register is set. With LKS interrupt enable set, falling edges of the signal LTC IN L will generate interrupt requests. The signal LTC IN L is derived from the ac power input by the power supply and is a square wave of the same frequency as the ac input voltage.

A transmitter interrupt can occur only if the interrupt enable (XMIT INT ENAB) bit in the transmitter status register is set. With XMIT INT ENAB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. Setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus.

The interrupt priority level is 6 for the line clock and 4 for the receiver and transmitter.

The vector address for the line clock is fixed at 100, whereas floating vector addresses are used for the receiver and transmitter of nonconsole DL11-Ws. The receiver vector is XX0 and the transmitter vector is XX4, where XX is assigned according to Table 4-2. If the DL11-W is used as console terminal interface, then the receiver and transmitter vector addresses will be 60 and 64, respectively. The vector address can be changed by resetting switches in the interrupt control logic.

All DIGITAL programs and other software which refer to the standard vector addresses must also be changed if the vector addresses are changed.

3.4 TIMING CONSIDERATIONS

When programming the DL11-W SLU/RTC option, it is important to consider the timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter, break generation logic, and line clock are discussed in the following paragraphs.

3.4.1 Receiver

The RCVR DONE flag (bit 7 in the RCSR) sets when the universal asynchronous receiver/transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double-buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

3.4.2 Transmitter

The transmitter section of the UART is also double-buffered. The XMIT RDY flag (bit 7 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded which clears the flag again. The flag then remains cleared for nearly one full character time.

3.4.3 Break Generation Logic

When the BREAK bit (bit 0 in the XCSR) is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. However, because the transmitter section of the UART is double-buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be null.

3.4.4 Line Clock

An initial synchronization period will be required when the LKS interrupt is initially turned on. In other words, the interval from setting LKS interrupt enable to the first interrupt will be some fraction of an ac power cycle period. All subsequent interrupts will occur at the proper intervals, depending on the ac power frequency.

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

This chapter provides a detailed description of the DL11-W Serial Line Unit/Real-Time Clock Option. The complete DL11-W may be divided into 12 functional areas. Table 4-1 lists these areas and explains the general purpose of each.

Table 4-1 DL11-W Functional Units

Functional Unit	Purpose
Selection Logic	Determines if the DL11-W interface has been selected for use and what type of operation (transmitter, receiver, or clock) has been selected. Permits selection of one of five internal registers and determines if the register is to perform an input or output function.
Register Logic	Five internal registers, addressable by the program, provide data transfer, command and control, and status monitoring functions for the interface.
Interrupt Request Logic	The line clock, receiver, or transmitter can request control of the Unibus for a vectored interrupt.
Interrupt Logic	Permits the DL11-W to gain control of the bus for a vectored interrupt.
Transmitter Control Logic	Provides necessary input control signals for the UART when it is used to convert parallel data from the Unibus to serial data required by the external device.
Receiver Control Logic	Provides necessary input control signals for the UART when it is used to convert serial data to parallel data required for transmission to the bus.
Universal Asynchronous Receiver/Transmitter (UART)	Performs the necessary serial-to-parallel or parallel-to-serial conversion on the data, and supplies control and error detecting bits.

Table 4-1 DL11-W Functional Units (Cont)

Functional Unit	Purpose
Baud Rate Logic	Determines the clock frequencies and, therefore, the baud rates for the transmitter and receiver sections of the UART. Eight baud rates are derived from a single oscillator and are independently switch-selectable.
Maintenance Mode Logic	Performs a closed-loop test of the serial line unit control logic by tying the serial output of the transmitter into the receiver input, forcing the receiver clock to the same frequency as the transmitter clock
Break Generation Logic	Permits the transmission of a continuous space or "break." The duration of the break can be timed by the pseudo-transmission of a specific number of characters.
20 mA Current Loop Logic	Provides active or passive 20 mA current loops for use with 20 mA current loop devices.
EIA Logic	Provides necessary level converters for use with EIA level devices.

4.2 ADDRESS SELECTION

The address selection logic (drawings DL-4 and DL-7) decodes the incoming address information from the bus to determine if the DL11-W has been selected for use, and provides the signals that determine which register has been selected and whether it is to perform an input or output function. Switches on the logic can be altered so that the module responds to any address within the range of 774000 to 777777. However, standard address assignments for the DL11-W normally fall within the ranges of 775610 to 776177 or 776500 to 776677.

The standard address assignments for DL11-W modules are listed in Table 4-2.

When the DL11-W is to be used as a console terminal control, switches are arranged so that the serial line section responds only to the standard device register addresses 777560, 777562, 777564, 777566, and, if the LTC is enabled, 777540. Although these addresses have been selected by DIGITAL as the standard assignments for the DL11-W when used as a console terminal control, the user may change the switches to assign any address desired, within the range of the address switches. However, the serial line address must be 77756X in order for the LTC and the SLU to both be used on the same DL11-W. Any MAINDEC program or other software that references the DL11-W standard assignments must be modified accordingly if other than the standard assignments are used.

Table 4-2 DL11-W Standard Address Assignments

Unit	Address	Remarks
Console	777560	Receiver Status Register (RCSR)
	777562	Receiver Data Buffer (RBUF)
	777564	Transmitter Status Register (XCSR)
	777566	Transmitter Data Buffer (XBUF)
1	776500	RCSR unit 1
	776502	RBUF unit 1
	776504	XCSR unit 1
	776506	XBUF unit 1
2	776510	RCSR unit 2
	776512	RBUF unit 2
	776514	XCSR unit 2
	776516	XBUF unit 2
		NOTE **Address space in the range 776500–776676 is reserved for DL11-A and -B equivalent devices.**
16	777670	RCSR unit 16
	777672	RBUF unit 16
	777674	XCSR unit 16
	777676	XBUF unit 16
		NOTE **For DL11-C and -D equivalent devices, address as follows.**
1	775610	RCSR
	775612	RBUF
	775614	XCSR
	775616	XBUF
		NOTE **Unit numbers in the first column are only for showing address sequencing. DL11-A, -B, -C, and -D equivalent DL11-Ws may be mixed in any manner as long as they remain in their respective address space.**
31	776170	RCSR
	776172	RBUF
	776174	XCSR
	776176	XBUF

Discussion of the three address selection modes is included here as well as in Chapter 2 for the sake of completeness. Normally, a DL11-W used as console terminal control would operate in the first mode, whereas additional DL11s would be operated in the second mode. While the third mode is a possibility, it is not normally used.

Mode 1 – Both the serial line unit and the line clock sections can be addressed. Due to common address selection logic, operation in this mode requires that the serial line unit addresses be restricted to 77756X. The line clock address is 777546.

Mode 2 – Only the serial line unit section can be addressed. Address selection ranges from 774000 to 777776. The line clock is disabled and does not respond to address 777546.

Mode 3 – Only the line clock section can be addressed at 777546. The serial line unit section does not respond to any address.

Table 4-3 indicates the correct switch settings for selection of the desired address and address mode.

Table 4-3 Address and Mode Selection

Address Bit	A10	A09	A08	A07	A06	A05	A04	A03	LTC	LTC
Switch	S5-3	S5-2	S5-1	S5-4	S5-5	S5-6	S5-8	S5-7	S5-9	S5-10
Mode 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
Mode 2*	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
Mode 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

*Address 77756X is selected for serial line interface. Other addresses may be selected using the switches shown. Note that OFF = 1 and ON = 0.

The following discussions assume that the DL11-W is operated as a console terminal control with the line clock enabled (mode 1).

The first five octal digits of address 77756X indicate that the serial line unit has been selected. The final octal digit (X), consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. To select the line clock register, 777546, the first 17 binary bits are decoded, and A00 is used to distinguish between a word and a byte operation. In both cases, the two mode control lines C00 and C01 determine whether the selected register is to perform an input or output operation (provided that the selected register is a read/write register).

The address decoding is performed by a series of logic gates that provide inputs to two 32 × 8 read-only memory (ROM) IC chips (D1-7). Basically, the state of the five input lines defines 1 of 32 unique addresses. The contents of the ROM corresponding to that unique address are then available at the output of the ROM. Each ROM provides 8 outputs for a total of 16, although only 14 of the 16 available outputs are used.

One input to the ROMs is address bit A04. This bit selects either the line clock or the serial line unit. When the line clock is disabled, this line is always high. Two inputs, address bits A02 and A01, are used to select one of the four registers in the serial line unit and are also used in decoding the line clock address; the fourth input is a combination of A00, C00, and C01, providing necessary decoding of word or byte and input or output operations. The fifth input is an address enable which must be true for the ROMs to decode the other inputs. This address enable signal is derived from a series of gates that are true when MSYN is present and when the address line conditions indicate that one of the valid addresses is true on the bus.

4.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 4-1. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the DL11-W is used, an OUT transfer is a transfer of data out of the master (the processor) and into the interface. Similarly, an IN transfer is the operation of the interface furnishing data to the processor.

The address selection lines (drawing DL-7) consist of 18 address lines on the bus (A17–00), bus control lines C1 and C0, and a master synchronization (MSYN) line. The address selection logic decodes the address on the bus as described below. This address format is shown in Figure 4-2. Note that all input gates are standard bus receivers.

1. Address lines A17–11 must be all 1s. This specifies an address within the top 4K addresses for device registers.

2. Decoding of address lines A10–05 and A03 is determined by switches. When a given line switch is ON, the address logic searches for a 0 on that line. If the switch is OFF, the logic searches for a 1. If only the serial line unit is to be enabled, then decoding of A04 will also be determined by a switch.

3. Lines A01, A02, and A04 are decoded to select one of the five addressable device registers.

4. Line C1 is used to select either an input (DATI) or output (DATO) function. When C1 is false, an input (read) operation is selected. When it is true, an output (write or load) operation is selected.

5. Line A00 is used for byte control in such a manner that no register control signals are generated when a byte operation (DATOB) is performed on the high-order byte of any register.

4.2.2 Outputs

The address selection logic output signals are used to permit selection of five 16-bit registers, and determine whether information is to be gated into or out of the master device. All of these output signals are listed in Table 4-4.

RCSR CLK ENB L and XCSR CLK ENB L are ANDed with BMSYN DEL L to provide the register loading pulses RCSR CLK H and XCSR CLK H (drawing DL-4).

LD XBUF H is used to trigger a 500 ns one-shot multivibrator to generate the transmitter buffer loading signal, LD X DEL L (drawing DL-4).

RBUF → BUS H triggers a 1 μs one-shot multivibrator to produce the signal SEL 2 L, which clears R DONE (drawing DL-4).

SSYN EN L is ANDed with BMSYN DEL L and delayed to produce BUS SSYN L (drawing DL-4).

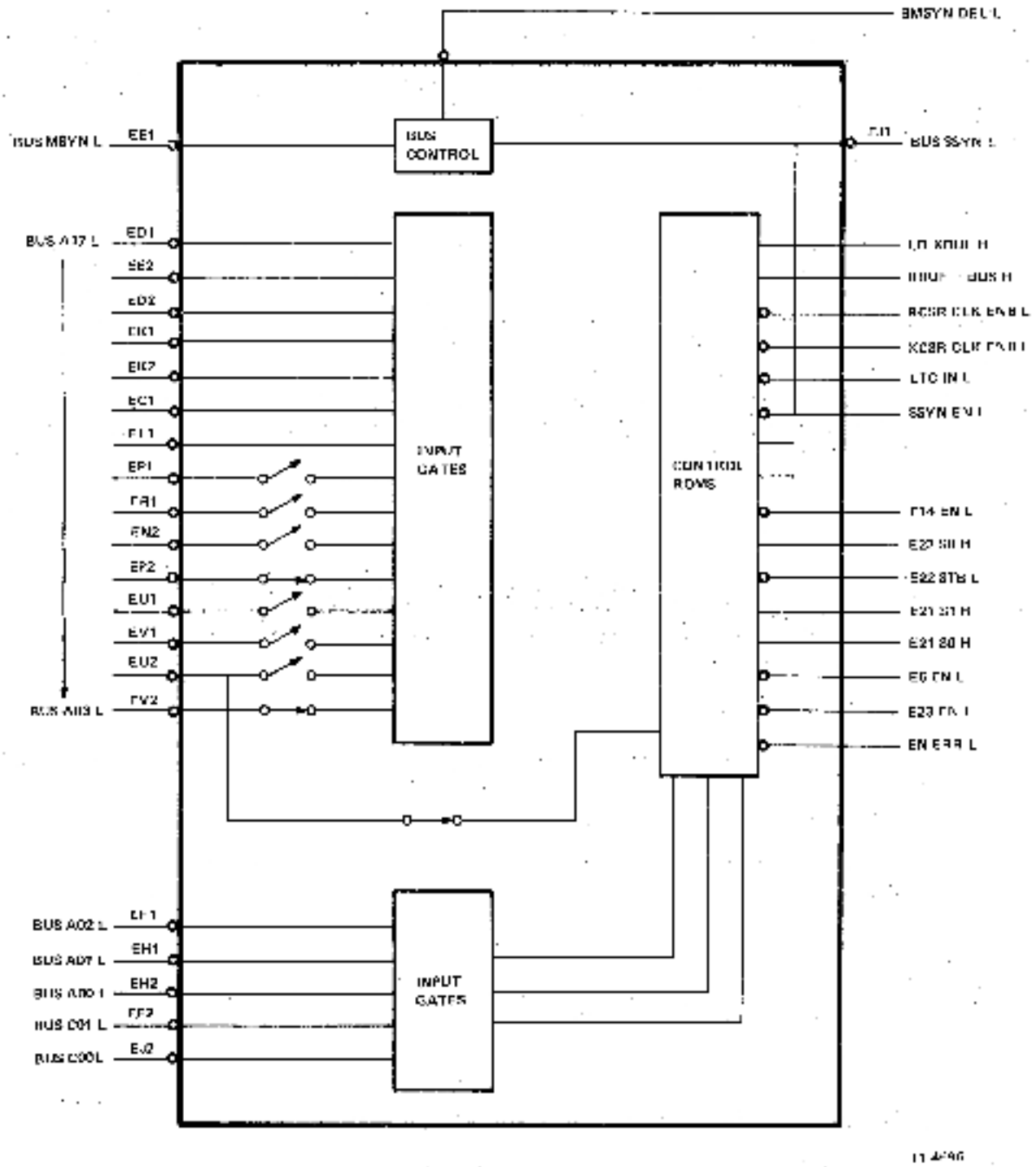


Figure 4-1 Address Selection Logic Simplified Diagram

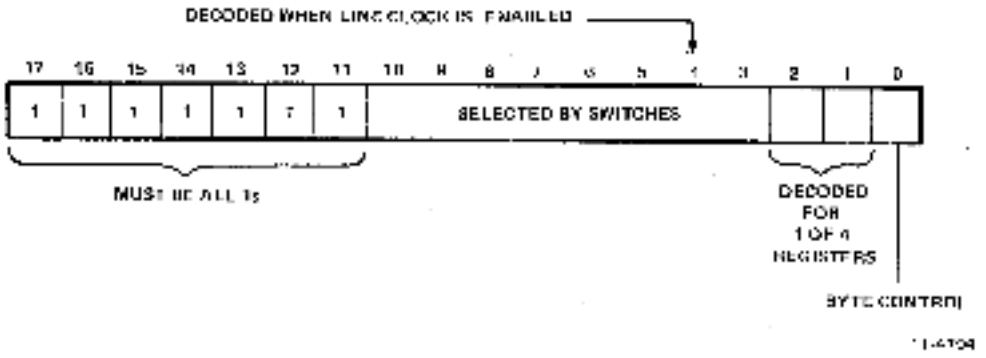


Figure 4-2 Interface Select Address Format

Table 4-4 Address Selection Logic Output Signals

Signal	Function Selected	Bus Cycle
LD XBUF H	Bus to transmitter buffer	DATO or DATOB*
RBUF BUS H	Receiver buffer to bus	DATI or DATIP
RCSR CLK ENB L	Bus to receiver status	DATO or DATOB*
XCSR CLK ENB L	Bus to transmitter status	DATO or DATOB*
LTC IN L	Bus to line clock status	DATO or DATOB
SSYN EN L	Returns BUS SSYN on a valid address selection	DATO, DATOB*, DATI, or DATIP
014 EN L	Enables bus drivers 003, 003, 004 and 005	DATI or DATIP
B22 SEL H	Selects either buffer (H) or transmitter status (L) to bus (bits 0 and 2)	DATI or DATIP
B22 STB L	Enables bits 0 and 2 (above) to bus drivers	DATI or DATIP

Table 4-4 Address Selection Logic Output Signals (Cont)

Signal	Function Selected	Bus Cycle
E21 S1 H E22 S0 H	Bits 6 and 7 of receiver buffer (S0 = L, S1 = L) receiver status (S0 = L, S1 = H) transmitter status (S0 = H, S1 = L) line clock status (S0 = H, S1 = H) to bus	DATI or DATIP
E6 EN L	Enables bus drivers D00, D02, D06, and D07	DATI or DATIP
E23 EN L	Receiver status (bit 11) to bus	DATI or DATIP
EN ERR L	Receiver buffer (bits 15, 14, 13, and 12) to bus	DATI or DATIP

*DATOB to low byte only.

4.3 REGISTER LOGIC

4.3.1 Receiver Status Register (RCSR)

The receiver status register (Figure 4-3) is used to monitor the status of receiver logic operations when the DL11-W accepts a character. It is also used to initiate interrupt sequences.

Each of the bits in the receiver status register is discussed separately in the following paragraphs, beginning with the most significant bit.

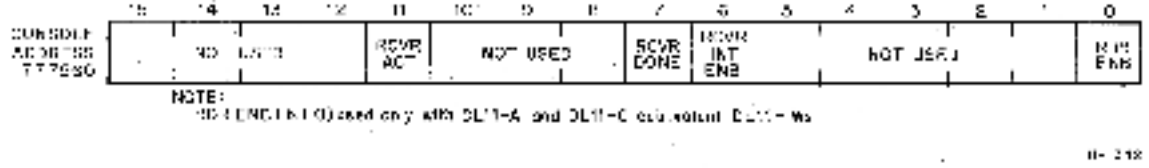


Figure 4-3 Receiver Status Register (RCSR)

4.3.1.1 Receiver Active (Bit 11) – The receiver active (RCVR ACT) flag indicates that the receiver logic is in the process of receiving and assembling an incoming character. This bit is read-only and is normally set and cleared by the receiver logic.

The RCVR ACT flag is set at the center of an incoming START bit. It is clocked on the eighth RCVR CLK period from the beginning of a START bit. (XMIT CLK and RCVR CLK frequencies are 16 times the respective baud rates.) RCVR ACT will remain set until the receiver done (RCVR DONE) flag is set. The RCVR ACT flip-flop is also cleared by B INIT L.

4.3.1.2 Receiver Done (Bit 7) – This is a read-only bit. The receiver done (RCVR DONE) flag indicates that a full character has been received. This bit, when set, clears the receiver active (RCVR ACT) flag and initiates an interrupt sequence provided the associated interrupt enable bit (RCVR INT ENB) is also set.

Once an entire character has been received and is stored in the UART holding register, the UART issues a received data available (R DONE) signal (drawing DL-1, C3), which is buffered, inverted, and fed to the direct clear input of the RCVR ACT flip-flop to clear it; this indicates that the receiver is no longer in use and is capable of receiving a new character.

The buffered R DONE signal, which becomes RCVR DONE H, is ANDed with RCVR INTR ENB (1) H to produce a clock signal to set the receiver interrupt request flip-flop. The setting of this flip-flop will initiate an interrupt sequence as described in Paragraph 4.5. The RCVR DONE H signal is gated to the Unibus (drawing DL-4) through a 4-to-1 multiplexer and through a bus driver enabled by the signals E6 EN L and BMSYN DEL L. This allows the status of the RCVR DONE bit to be read by the program from bus data line BUS D07 L.

The RCVR DONE bit can be cleared by B INIT L or by the occurrence of CLR R DONE. CLR R DONE occurs under two conditions.

1. Whenever the receiver buffer (RBUF) is addressed, indicating that a new character may be loaded into the receiver. SEL 2 L is true and passes through an OR gate to produce CLR R DONE on the UART.

2. If the reader enable (RDR ENB) flip-flop is set, indicating that the tape reader in a Teletype unit is being advanced, then the 0 side is low and passes through the same OR gate as before to reset CLR R DONE.

4.3.1.3 Receiver Interrupt Enable (Bit 6) – This is a read/write bit. The receiver interrupt enable bit (RCVR INT ENB) permits an interrupt sequence to be initiated when the RCVR DONE bit sets to indicate that a character has been received and is ready for transfer to the bus. This bit is set by using the RCSR CLK H signal as a load pulse to load a 1 from bus line BUS D06 L. This line is buffered to BBD 6 H (drawing DL-4), the D input of the RCVR INTR ENB flip-flop (drawing DL-1).

The output of the flip-flop, RCVR INTR ENB (1) H, ANDed with RCVR DONE H, clocks the receiver interrupt request flip-flop, setting it.

The RCVR INT ENB bit can be read onto the Unibus via the 4-to-1 multiplexer (drawing DL-4, C-3) and through the bus driver enabled by E6 EN L and BMSYN DEL L onto bus data line BUS D06 L.

The RCVR INTR ENB flip-flop is cleared by B INIT L.

4.3.1.4 Render Enable (Bit 0) – The reader enable (RDR ENB) bit, when set, advances the paper tape reader in ASR Teletype units via a 20 mA output circuit. The BBD 0 H signal, which is derived from receiving BUS D00 L, is applied to the data input of the RDR ENB flip-flop (drawing DL-1, C-6). The clock input receives the loading signal RCSR CLK H. When the flip-flop is set, the 0 side, which is low, is applied to the 20 mA circuit (drawing DL-8), which advances the paper tape reader in the Teletype via pin PP on the Berg connector. The 0 side of the flip-flop is also gated through an OR gate (drawing DL-1) to reset the RCVR DONE bit via CLR R DONE as described in Paragraph 4.3.1.2.

The RDR ENB bit is a write-only bit; it cannot be read by the program.

Whenever the Teletype starts sending data to the interface, the RDR ENB bit is cleared so that the reader does not advance another frame while it is transmitting information to the DL11-W.

The RDR ENB flip-flop is cleared when the RCVR ACT flip-flop becomes set, which is at the middle of a START bit as explained in Paragraph 4.3.1.1. The RDR ENB flip-flop can also be cleared by B INIT L.

4.3.2 Receiver Buffer Register (RBUF)

The receiver buffer register (Figure 4-4) is an 8-bit read-only register in the UART (drawing DL-1, C-4). Serial information is converted to parallel data by the UART and then gated to the Unibus. The RBUF consists of gating logic rather than a flip-flop register. Therefore, the data output lines from the UART must be held until read onto the bus. Because the UART is double-buffered, data on these output lines is valid until the next character is received and assembled. The RBUF register is read by a DATI sequence and the data is transmitted to the Unibus for transfer to the processor or some other PDP-11 device.

If less than eight data bits are selected, the buffer is justified into the least significant bit positions. This justification is performed by the UART. The data loaded into the buffer is coded so that binary 0s correspond to spaces and binary 1s correspond to marks (or holes).

The four most significant bits in the high-order byte of the register are used for error indications. The error bits and the data portion of the receiver buffer register are covered separately in the following paragraphs.

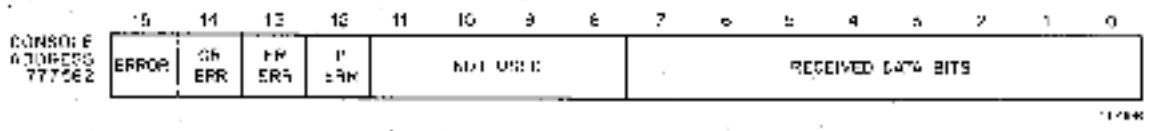


Figure 4-4 Receiver Data Buffer (RBUF)

4.3.2.1 Receiver Error Bits (Bits 15, 14, 13, 12) – The high-order byte of the receiver buffer register (RBUF) contains four error bits that set to indicate improper receiver operation. These bits are read-only and can be disabled by having switch S4-7 in the OFF position.

Three of the four error bits are generated in the UART as follows:

1. OR ERROR – (overrun error, bit 14) – Indicates that R DONE was not reset (previously received character was not read) prior to receiving a new character. When this condition exists, the UART generates an OR ERR H signal.

2. FR ERROR – (framing error, bit 13) – Indicates that a framing error exists because the character read had no valid STOP bit. When this condition exists, the UART generates a FR ERR H signal.

3. P ERROR – (parity error, bit 12) – Indicates that the parity received does not agree with the expected parity. If parity has been selected and this condition exists, the UART generates a P ERR H signal.

Bit 15, which is the error (ERROR) bit, is the inclusive-OR of the OR ERROR, FR ERROR, and P ERROR bits (DL-1, C-2). Whenever one of these errors occurs, the appropriate signal from the UART [OR ERR H, FR ERR H (DL-4, B-4), or P ERR H] passes through a buffer and qualifies an OR gate (drawing DL-1). The output of the OR gate is ERROR H. Each of the four error signals (drawing DL-4) qualifies one leg of a 2-input NAND gate (DL-4, B-4). The other leg is qualified by BMSYN DEL L ANDed with EN ERR L. The output of each NAND gate is tied to an associated bus data line (BUS D15 L, BUS D14 L, BUS D13 L, and BUS D12 L) so that the status of each error bit can be monitored by the program. Note that the enabling signal EN ERR L is applied via switch S4-7 and if this switch is off the error bits cannot be read onto the bus.

It should be noted that none of the error bits is tied to the interrupt logic. Therefore, occurrence of a receiver error does not cause the program to be interrupted for a branch to a handling routine. However, these flags are updated each time a character is received, at which point an interrupt may occur by means of R DONE.

The initialize signal (B INIT H) may have an effect on these bit positions depending on the UART used. A bit is cleared by clearing the error-producing condition. When the next character is received by the UART, the error bits are updated and the new status is available when the receiver buffer register is read.

4.3.2.2 Receiver Data Bits (Bits 7 through 0) – These bits are read-only bits. The receiver buffer register is not a flip-flop register, but consists simply of gates that strobe data from the output lines of the UART onto the Unibus. The UART receives the incoming serial data from the external device, converts it to parallel data, and places it on eight parallel output lines. Each of these lines (RD0 through RD7) is fed to one leg of a NAND gate as shown on drawing DL-4 (RD0 and RD2 through the 2-to-1 multiplexer; RD6 and RD7 through the 4-to-1 multiplexer). When the receiver buffer is addressed for reading, E14 EN L and E6 EN L will also be true, and, ANDed with BMSYN DEL L, will gate the receiver buffer levels to bus data lines BUS D07 L through BUS D00 L.

Figure 4-5 is a simplified diagram of both receiver and transmitter gating logic showing a single bit position. When the receiver gating is used, the output of the UART is gated through to the Unibus. When the transmitter is used, data from the Unibus is gated through to the transmitter inputs of the UART.

The receiver buffer can only be read by the program. It is loaded by the UART. Note that the initialize signal (B INIT L) has no effect on this register.

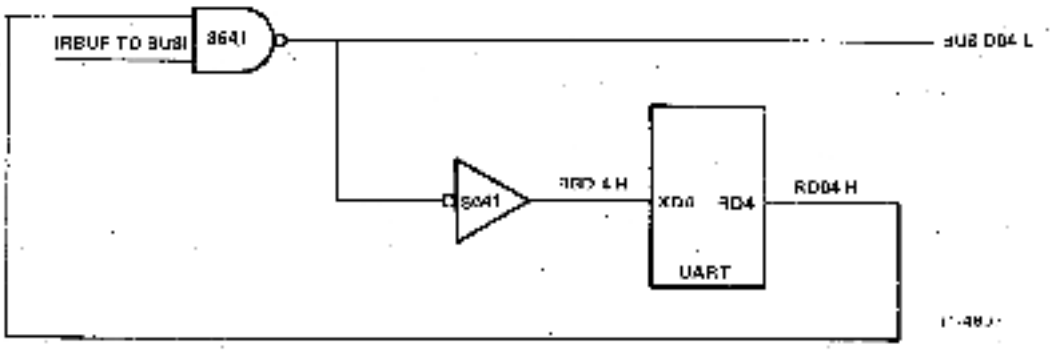


Figure 4-5 Receiver Data Buffer and Transmitter Data Buffer Gating Logic

4.3.3 Transmitter Status Register (XCSR)

The transmitter status register (Figure 4-6) consists of control and status monitoring bits for the transmitter portion of the DL11-W. The register contains two bits associated with transmitter operation: a transmitter ready flag to indicate that the transmitter buffer can be loaded, and an interrupt enable to allow the transmitter to initiate an interrupt sequence. Both of these bits are described in subsequent paragraphs.

A maintenance (MAINT) bit is also provided so that a closed loop test of the serial line unit operation can be performed. The maintenance function is covered in detail in Paragraph 4.10.

A BREAK bit (bit 0) is provided and permits transmission of a continuous space to the external device. This bit may be disabled via switch S4-1. The associated logic is described in Paragraph 4.6.

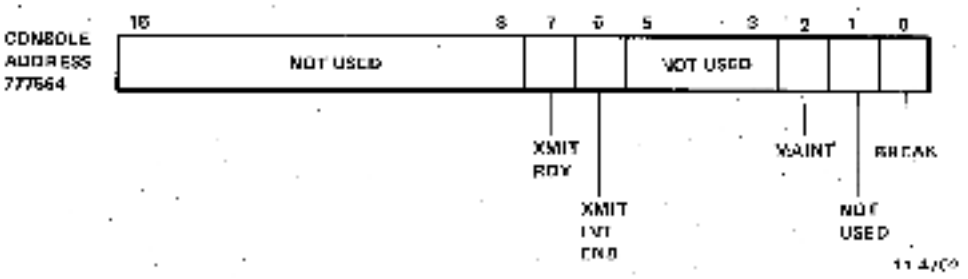


Figure 4-6 Transmitter Status Register (XCSR)

4.3.3.1 Transmitter Ready (Bit 7) – The transmitter ready (XMIT RDY) flag indicates that the transmitter buffer (XBUF) is ready to accept another character from the Unibus for transfer to the external device. This bit, when set, initiates an interrupt sequence, provided the associated interrupt enable bit (XMIT INT ENB – bit 6) is also set.

The flag is controlled by the XRDY output of the UART, which indicates that the transmitter buffer is empty. It is set by the initialize signal (B INIT H) to indicate that the data bit holding register within the UART may be loaded with another character. It is also set whenever the holding register is empty. Once loading of the transmitter buffer begins, the bit is cleared. The XRDY output of the UART is buffered to produce the XMIT RDY H flag.

As shown in drawing DL-1, the XMIT RDY H signal is ANDed with XMIT INTR ENB (1) H, which is true if bit 6 is set, to clock the 7474 flip-flop, setting it. The 0 side of this flip-flop, which is now low, is ANDed with XMIT INTR ENB (1) L, and the output of this gate initiates an interrupt sequence. The interrupt sequence allows the program to branch to a handling routine for loading a character for transmission to the external device.

The XMIT RDY flag can be read by the program from bus data line BUS D07 L via the 4-to-1 multiplexer and associated bus driver.

4.3.3.2 Transmitter Interrupt Enable (Bit 6) – The transmitter interrupt enable bit (XMIT INT ENB) is a read/write bit that permits an interrupt sequence to be initiated when the XMIT RDY bit sets to indicate that the transmitter buffer can accept another character from the Unibus. This bit is set by using XCSR CLK H as a load pulse to load a 1 from bus line BBD 6 H into the XMIT INTR ENB flip-flop (DL-1).

The output of flip-flop XMIT INTR ENB (1) H is applied to one leg of a 2-input AND gate. The other input of this AND gate is the XMIT RDY H signal, which is produced when the transmitter buffer is clear and capable of receiving a character from the bus. When both inputs are true, the output clocks the 7474 flip-flop, initiating an interrupt sequence.

As shown on drawing DL-4, the XMIT INTR ENB (1) H signal is applied to an input of the 4-to-1 multiplexer, which can be read onto bus data line BUS D06 L (DL-4, C-2) so that the program can read the status of this bit.

The XMIT INT ENB flip-flop is cleared by B INIT L.

4.3.3.3 Maintenance (Bit 2) – This read/write bit is cleared by B INIT L. It is read onto the bus through the 2-to-1 multiplexer E22 (DL-4). The program can set the bit through bus line BUS D02 L. When set, the maintenance bit disables the serial line input to the receiver and sends the serial output of the transmitter into the serial input of the receiver. The receiver is forced to run at transmitter speed.

4.3.3.4 Break (Bit 0) – The break flip-flop, together with the maintenance flip-flop and the interrupt enable flip-flop, is located on E8 on drawing DL-1. It is a read/write bit that is cleared by B INIT L. The output is gated to Unibus line BUS D00 L through the 2-to-1 multiplexer on drawing DL-4. When set it transmits a continuous space. It may be disabled via switch S4-1.

4.3.4 Transmitter Buffer Register (XBUF)

The transmitter buffer (Figure 4-7) is an 8-bit write-only register that receives the parallel character from the Unibus and loads it into the UART for serial conversion and transmission.

Some switch selections may cause the UART to be operated with a data format of less than eight data bits. In these cases, the data character must be justified into the least significant bit positions by the program. Bit positions within the UART itself are enabled or disabled according to the format code selected (Table 2-4). Thus, for example, if a 5-bit code is selected, bit positions 5, 6, and 7 are disabled. If the program does not justify the character and the character is loaded into the most significant bit positions, data loaded into bits 5, 6, and 7 will be lost.

When the interface is initialized, the XMIT RDY flag (DL-1, C-4) is set to indicate that the XBUF can be loaded. When the buffer is loaded with the first character, the flag clears and then sets again within a fraction of a bit time. A second character can then be loaded because the UART transmitter section is double-buffered. When the second character is loaded, the flag clears again, but this time remains clear for nearly a full character time.

The transmitter buffer (drawing DL-1) is not a flip-flop register, but consists of bus data buffers and a strobe pulse to load data from the Unibus to the input lines of the UART. Transfer of data is accomplished by a DATO or DATOB bus cycle.

The character to be transmitted to the device is loaded onto the bus data lines BUS D00 L through BUS D07 L and gated to the UART input lines as BBD 0 through BBD 7. Once on the input lines, the data is strobed into the UART by the LD X DEL L signal. (See Figure 4-5.)

Loading of the transmitter buffer is such that a logic 1 causes a mark (or hole) to be transmitted, and a logic 0 causes a space.

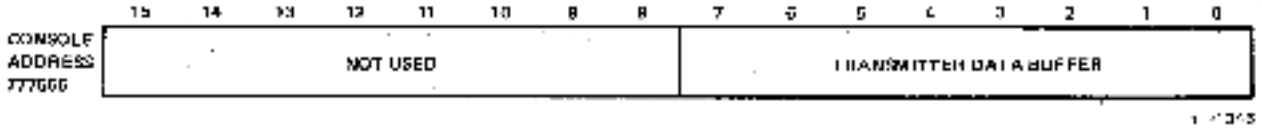


Figure 4-7 Transmitter Data Buffer (XBUF)

4.3.5 Line Clock Status Register (LKS)

The line clock status register (Figure 4-8) consists of control and status monitoring bits for the line clock portion of the DLI1-W.

The line clock status register contains two bits associated with line clock operation: a line clock monitor bit to provide noninterrupt mode timing information and an interrupt enable bit to allow the line clock to initiate an interrupt sequence. Both of these bits are described in subsequent paragraphs.

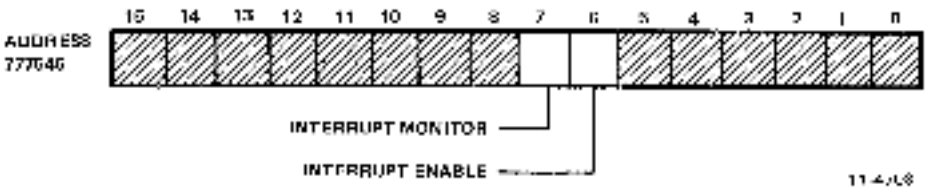


Figure 4-8 Clock Status Register (LKS)

4.3.5.1 Line Clock Monitor (Bit 7) – The line clock monitor read-only bit provides the software with a means of measuring a time interval in a noninterrupt mode. The line clock monitor bit is set once for each cycle of the ac power. The program must clear the bit after noting that it was set each time.

As shown in drawing DL-2, the LTC flip-flop (LKS bit 7) is set when clocked by BUS LTC L. BUS LTC L is a square wave with the same frequency as the ac power, and it is generated in the power supply.

This flip-flop is cleared only by the program. This occurs when bus data line BUS D07 L has a logic 0 and is loaded into the line clock monitor bit (BIT 07). The inverted bus data line (BBD 7 H) is again inverted (drawing DL-2) and is ANDed with LTC IN L, BMSYN DEL L, and BSSYN L to generate a pulse which direct-clears flip-flop LTC BIT 07. Note that if bus data line BUS D07 L were a logical 1, the monitor bit would not be cleared by the program. This bit can be read by a program via the 4-to-1 multiplexer and bus driver in drawing DL-4. LKS BIT 07 is cleared by B INIT L.

4.3.5.2 Line Clock Interrupt Enable (Bit 6) – The line clock interrupt enable read/write bit allows the line clock portion of the DL11-W to generate timed interrupt sequences. Interrupt sequences will occur at time intervals of 16-2/3 ms (60 Hz) or 20 ms (50 Hz), depending on the frequency of the ac input voltage.

A logical 1 on bus data line BUS D06 L is inverted and applied to the data input of the LKS BIT 06 flip-flop (DL-2, D-7). The 1 is then loaded into the flip-flop, using the ANDed combination of BMSYN DEL L and LTC IN L as a load pulse.

With LKS BIT 06 set, the direct-clear signal would normally be removed from the interrupt request flip-flop. The next falling edge of BUS LTC L from the power supply would clock the interrupt request flip-flop, initiating an interrupt sequence.

LKS BIT 06 II can be read onto bus data line BUS D06 L via the 4-to-1 multiplexer and bus driver (drawing DL-6).

Line clock interrupt enable (LKS BIT 06) will be cleared by B INIT L.

4.4 INTERRUPT REQUEST LOGIC

The DL11-W contains two separate interrupt request logic circuits. One initiates interrupt sequences for the line clock portion and the other initiates interrupt sequence for the serial line portion.

4.4.1 Line Clock

The line clock interrupt request logic consists of an interrupt request flip-flop and a bus driver (DL-2). The interrupt request flip-flop is set on the falling edge of signal BUS LTC L. When set, the 1 side output enables one leg of a 2-input bus driver gate. The other input is enabled until the processor acknowledges the interrupt request. The bus driver enables the Unibus signal BUS BR 6 L, which initiates the interrupt sequence. The interrupt request flip-flop can be cleared by obtaining control of the bus (RTC MASTER L), by writing a 0 into LKS BIT 07, or by clearing LKS BIT 06.

4.4.2 Serial Line Unit

The interrupt request logic for the serial line unit consists of two interrupts request flip-flops (one for the receiver and one for the transmitter), an arbitrator circuit, and a bus driver.

The receiver interrupt request flip-flop is shown on drawing DL-1 in an inverted manner. Note that pin 6 is used as the true output. The flip-flop is set by the ANDed conditions of RCVR DONE H and RCVR INTR ENB (1) H. The 1 side of this flip-flop is ANDed with RCVR INTR ENB (1) H to generate an interrupt request signal, which is applied to the arbitrator circuit. The receiver interrupt request flip-flop can be cleared by one of the following conditions: B INIT L; RCVR becoming bus master (MASTER H ANDed with REC SEL H, E68-5 on drawing DL-3); or CLR R DONE.

The transmitter interrupt request flip-flop (DL-1) is also shown as inverted. It is set by XMIT RDY H ANDed with XMIT INTR ENB (1) H or by B INIT L. When set, the 0 side output, which is low, is ANDed with XMIT INTR ENB (1) L to generate an interrupt request signal, which is applied to the arbitrator circuit. This flip-flop can be cleared if the transmitter becomes bus master (MASTER H ANDed with XMIT SEL H, E68-6 on drawing DL-3) or if the transmit buffer is loaded (LD X DEL L).

The function of the arbitrator circuit is to arbitrate simultaneous interrupt requests from both the receiver and transmitter. The arbitrator circuit has two inputs and two outputs. The two inputs are the gated outputs of the receiver interrupt request flip-flop and the transmitter interrupt request flip-flop. The outputs of the arbitrator circuit are the two signals RCVR INTR RQST H and XMIT INTR RQST H. Only one output is true at one time; generally the flip-flop which sets first generates the interrupt request. In the normal state of this flip-flop, both the set and clear inputs are held low. This forces the Q and $\overline{Q}$ outputs both high. Then, when either the clear or the set input goes high, the other input is enabled. For example, if the set input signal goes high first (requesting a receiver interrupt), then the flip-flop will reset, enabling the receiver interrupt request low signal and thus RCVR INT REQ H.

4.5 INTERRUPT CONTROL LOGIC

The interrupt control logic permits the DL11-W to gain control of the bus (become bus master) and perform an interrupt operation. The DL11-W contains two separate interrupt controls, one for the line clock and one for the serial line unit. The vector for the line clock is fixed at 100 but the serial line unit vector may be altered via switches so that the logic has a normal address within the range of 000 to 776. However, the specific vector used with a particular DL11-W depends on its use within a system.

The standard vector addresses for the DL11-W, when used as a console interface, are 060 and 064. Other DL11-Ws in the system are assigned "floating" vectors according to the addressing scheme given in Appendix B.

NOTE

The final octal digit of the vector address is not affected by the switches; therefore, regardless of the vector address selected by the switches, the final octal digit is always 0 for the receiver and 4 for the transmitter.

Since both the line clock and serial line unit interrupt controls are basically the same, only the serial line unit interrupt control logic will be discussed in subsequent paragraphs. Figure 4-9 is a simplified diagram of the interrupt control logic.

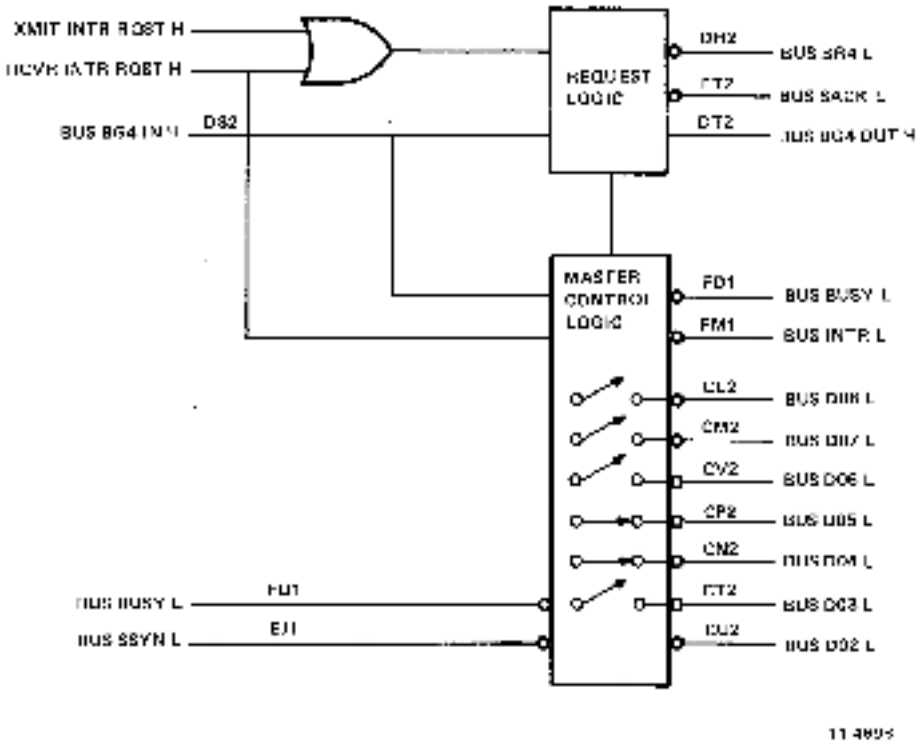


Figure 4-9 Interrupt Control

The serial line unit interrupt control logic is shown on drawing DL-3. If either a receiver interrupt request or transmitter interrupt request, or both, is generated, the arbitrator circuit in the interrupt request logic (Paragraph 4.4) will generate one of the two signals: RCVR INTR RQST H or XMIT INTR RQST H. These two signals are ORed and applied to one leg of the bus request driver on BUS BR4 L. The other leg is enabled if the interrupt control logic is not currently master (BUSY) or already the next master (SACK).

The processor will arbitrate the request and send a bus grant if no device of higher priority is making a request. Normally, the processor will continue the interrupt sequence by the issuance of BUS BG4 IN H. Because bus grants are "daisy-chained" from device to device, the DL11-W must decide either to accept the bus grant signal or to pass it on to the next device.

This decision is made by another arbitrator circuit shown in the simplified diagram in Figure 4-10. Basically, if the serial line unit generates an interrupt request before the reception of the bus grant, the DL11-W will accept the grant and, if the request is raised after the grant, pass it on. The arbitrator will decide one way or the other when both events occur simultaneously. If the grant is passed on, then the bus driver on BUS BG4 OUT H will be enabled. If the arbitrator circuit accepts the bus grant, then the grant accept signal is ANDed with bus grant to generate a set signal for the SACK R-S flip-flop. The SACK flip-flop enables the BUS SACK driver and, ORed with the BUSY flip-flop, disables the BUS BR4 driver. The processor will respond to the signal BUS SACK L by unasserting BUS BG4 IN H.

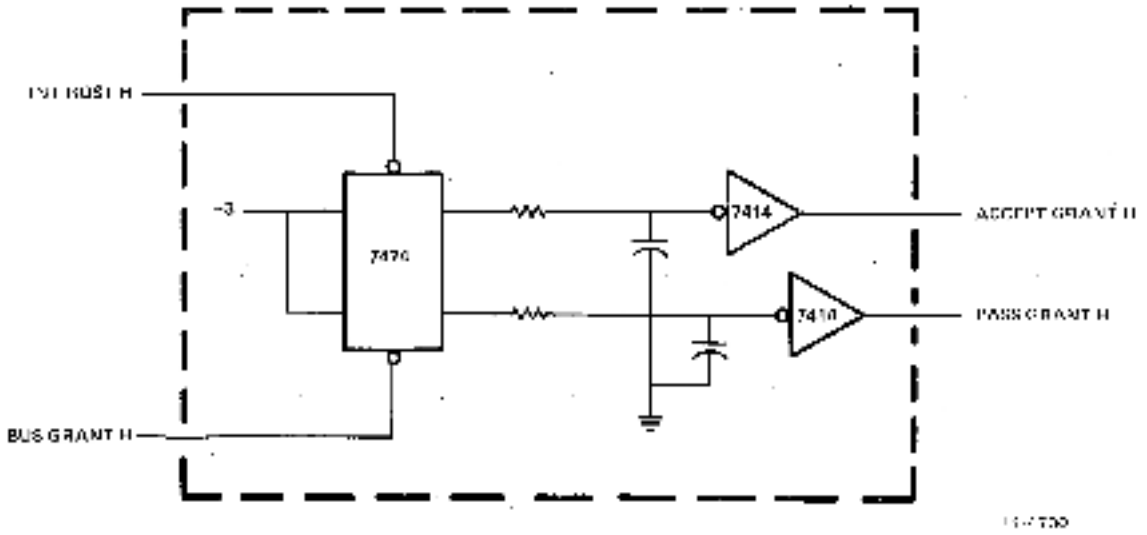


Figure 4-10 Arbitrator Circuit

With the assertion of BUS SACK L, the DL11-W is prepared to become bus master when the bus becomes free. The data input of the BUSY flip-flop is primed with the 1 side of the SACK flip-flop. A clock edge is generated when the bus becomes free by the ANDed condition of BUS BUSY, BUS SSYN, and BUS BG4 IN. When the BUSY flip-flop is set, the 1 side output is applied to the BUS BUSY driver to indicate that the bus is in use. The 0 side of the flip-flop, which is now low, is used as MASTER L, indicating that the interrupt control logic is now master of the bus.

MASTER L is inverted and used to place the vector address on the Unibus and to assert BUS INTR L. The processor responds to BUS INTR L by asserting BUS SSYN L, which, after being inverted by the bus receiver, clears the BUSY flip-flop.

B INIT H also clears both the SACK flip-flop and the BUSY flip-flop.

Note that any vector address switch is ON for a 1 and OFF for a 0.

4.6 TRANSMITTER CONTROL LOGIC

The transmitter control logic provides the necessary input, control, and output logic for the UART when it is used to convert parallel data from the Unibus to the serial data required for output. This logic may be divided into three functional areas: control and input, format selection, and data output.

Control and input signals to the UART are described in Table 4-5.

Table 4-5 Transmitter Control and Input Logic

Signal Mnemonic	Signal Name	Description
XRDY	Transmitter Ready	The XMIT RDY flag indicates that the buffer is empty and may be loaded with another character from the Unibus.
LDXD	Load Transmitter Data	The signal that strobes data from the bus into the UART when the XBUF is addressed for loading.
XCLK	Transmitter Clock Pulse	Provides the required transmitter clock rate. This rate is 16 times the selected baud rate.
XD0-XD7	Data Buffer	Represents the character (five to eight bits) loaded from the Unibus into the UART.

The format selection logic basically consists of switches that are arranged to select the number of DATA bits, STOP bits, and type of parity. Format selection is covered in Table 2-4.

The output logic of the transmitter is described in the following paragraphs.

Once the UART has converted the parallel character from the Unibus (UART operation is described in Paragraph 4.8), it shifts the character out, one bit at a time, onto the serial output (SERIAL OUT) line. The first bit shifted out is the START bit, followed by the DATA bits (LSB first), then the PARITY bit (if selected), and finally the STOP bits. The output of the line passes through a NAND gate to produce SERIAL OUT L. This gate is used to generate a space when the BREAK bit is used.

SERIAL OUT L is connected to a circuit that converts the signal to the bipolar levels required by the 20 mA current loop (drawing DL-2). The resultant positive serial data is applied to pin AA of the Berg connector and the negative serial data is applied to pin KK.

SERIAL OUT L passes through an inverter and is applied to an EIA level converter which drives pin F of the Berg connector.

The selection of the 20 mA current loop or the EIA level converter depends on the type of cable used at the Berg connector. A kit containing the quad board and a cable (7008360) for the 20 mA current loop is called a DL11-WA. The DL11-WB kit contains the cable (BC05C) for the EIA level converter.

The inverter output SERIAL OUT H is also applied to the MAINT multiplexer circuit for use during maintenance mode as described in Paragraph 4.10.

4.7 RECEIVER CONTROL LOGIC

The receiver control logic provides the necessary input, output, and control logic for the UART when it is used to convert serial data to the parallel data required by the Unibus. This logic may be divided into three functional areas: status and control, format selection, and data input.

The status and control portion of the logic consists of both input control and output status signals, a clock frequency, and an output data character. These signals are listed in Table 4-6.

Table 4-6 Receiver Status and Control Logic

Signal Mnemonic	Signal Name	Description
R DONE	Reader Done	The R DONE flag indicates that a full character has been received from the device and is ready for transfer to the Unibus.
P ERR	Parity Error	A status signal indicating that the received character has a parity error. Can be read by the program.
FR ERR	Framing Error	A status signal indicating that the received character has no valid stop code. Can be read by the program.
OR ERR	Overrun Error	A status signal indicating that the character was not read prior to receiving another character from the device. Can be read by the program.
R CLK	Receiver Clock Pulse	Provides the required receiver clock rate. This rate is 16 times the selected baud rate.
RD7–RD0	Receiver Data Buffer	Represent the character (five to eight data bits) transferred from the UART to the Unibus after serial-to-parallel conversion.

The format selection is basically the same as that used for the transmitter control, and is described in Table 2-4.

The input logic of the receiver is described in the following paragraphs.

Regardless of the device used, the serial input from the device is loaded into the DL11-W one bit at a time, beginning with the START bit, then the DATA bits (LSB first), the PARITY bit (if used), and the STOP bits.

The bipolar levels of the serial data are applied to pins K (+) and S (-) of the Berg connector. The bipolar level is converted to a TTL level (DL-5) and fed to pin H. EIA level serial data is received on pin J of the connector and converted to a TTL level which is presented at pin H. Either pin M or pin H is connected to pin E (depending upon the type of interface to the external device) and becomes the signal TTL SERIAL DATA IN. The serial data is connected to a 2-to-1 multiplexer which, when the interface is not in the maintenance mode, passes the TTL SERIAL DATA IN signal through to the output, which is then applied to the input (SERIAL IN) of the UART (as shown in DL-1). The output of the multiplexer is also inverted and fed to a counter used to detect the center of a START bit.

4.8 UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The universal asynchronous receiver/transmitter (UART) is an LSI subsystem that accepts binary characters from either a terminal device or a computer, and receives or transmits this character with appended control and error detecting bits. In order to make this subsystem universal, the baud rate, bits per word, parity mode, and number of stop bits are selected by external logic circuits.

The UART is a full duplex receiver/transmitter. The receiver section accepts asynchronous serial binary characters and converts them to a parallel format for transmission to the Unibus. The transmitter section accepts parallel binary characters from the bus and converts them to a serial asynchronous output with START and STOP bits added.

All UART characters contain a START bit, five to eight DATA bits, one, one and a one-half, or two STOP bits, and a PARITY bit which may be odd, even, or turned off. The STOP bits are opposite in polarity to the START bit.

Both the receiver and transmitter are double-buffered. The UART internally synchronizes the START bit with the clock input to ensure a full 16-element (clock periods) START bit independent of the time of data loading. Transmitter distortion (assuming perfect clock input) is less than 3 percent on any bit up to 10 kilobaud. The receiver strobes the input within ±8 percent of the theoretical center of the bit. The receiver also rejects any START bit that lasts less than one-half of a bit time.

The UART input and output lines are shown on drawing DL-1. A description of the receiver is given in Paragraph 4.8.1 and a description of the transmitter is given in Paragraph 4.8.2. Note that in the following discussions the mnemonics and pin numbers of UART input and output lines are given in parentheses.

4.8.1 Receiver Operation (UART)

A block diagram of the UART receiver is shown in Figure 4-11. When the receiver is in the idle state, it samples the serial input line (SERIAL IN, pin 20) at the selected clock edges (R CLK, pin 17) after the first mark-to-space transition of the serial input line. If the first sample is a mark (high), the receiver returns to the idle state and is ready to detect another mark-to-space transition. If, however, the first sample is a space (low), then the receiver enters the data entry state.

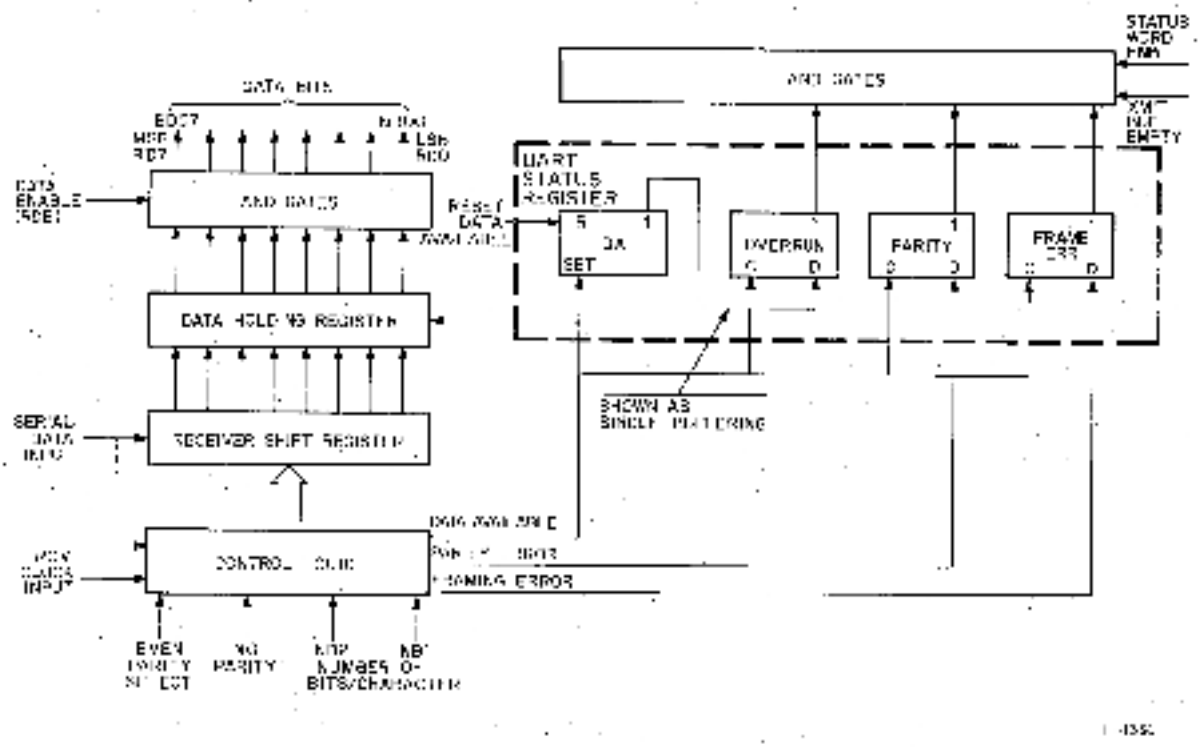


Figure 4-11. UART Receiver

If the receiver control logic has not been conditioned to the no parity state (a low on pin 35), then the receiver checks the parity of the DATA bits plus the PARITY bit following the DATA bits and compares it with the parity sense on the parity select line (pin 30). If the parity sense of the received character differs from the parity of the UART control logic, then the receiver parity error line (P ERR, pin 13) goes high and causes the P ERR bit in the RBUF register to set.

If the receiver control logic has been conditioned to the no parity state (a high on pin 35), then the receiver takes no action with respect to parity and maintains the parity error line (P ERR, pin 13) in the false (low) state. When the control logic senses a parity error, it generates a P ERR signal. The DATA AVAILABLE signal updates the parity error indicator.

The receiver samples the first STOP bit, which occurs either after the PARITY bit or after the DATA bits (if no parity is selected). If a valid (high) STOP bit exists, no further action is taken. If, however, the STOP bit is false (low), indicating an invalid STOP code, then the UART control logic provides a framing error indication (a high on FR ERR, pin 13). The status of the framing error bit can also be read from the RBUF if enabled.

Because the serial input from the external device is shifted into the UART a bit at a time (SERIAL IN, pin 20), occurrence of a STOP code indicates that the entire data character has been received and shifted into the receiver shift register. After the STOP bit has been sampled, the receiver control logic parallel transfers the contents of the shift register into the receiver data holding register, and then sets the data available (R DONE) flag.

The data available signal also functions as the clock input to the FRAME ERR, PARITY, and OVERRUN flip-flops in the UART status register. At this point, the data available (DA) flip-flop is set, the OVERRUN flip-flop is cleared but has a high on the data input because of the output from the DA flip-flop, and the PARITY and FRAME ERR flip-flops are set or cleared depending on the signal (true or false) strobed in from the control logic.

An overrun condition indicates that another data character is being sent to the UART before the previous character has been transferred to the DL11-W receiver buffer register. If the DA flip-flop is set, indicating that a character is stored in the holding register, and the UART control logic attempts to set the DA flip-flop again (indicating that a new character has been shifted into the shift register), the DA signal from the control logic provides a clock input to the OVERRUN flip-flop. This flip-flop then sets because the data input is high (DA flip-flop was already set by the previous DA signal).

During normal operation (no overrun condition), the character in the receiver data holding register is strobed onto the Unibus by a reading of RBUF which produces SEL 2 L. This signal is applied to the UART reset data available line (pin 18) to clear the flip-flop.

Whenever the serial input line goes from a mark (high) to a space (low) and remains at the low level, the receiver shifts in one character, which is all spaces, then sets the FR ERR indicator and waits until the input line goes high (marking) before shifting in another character

4.8.2 Transmitter Operation (UART)

A block diagram of the UART transmitter is shown in Figure 4-12. When the UART transmitter is in the idle state, the serial output line (pin 15) is a mark (high). When it is desired to transmit data, a parallel character is placed on bus data lines BUS D00 through D07 and strobed into the UART transmitter data buffer (lines connected to pins 26–33) by means of the data strobe signal (pin 12). The time between the low-to-high transition of data strobe and the corresponding mark-to-space transition of the serial output line is within one clock cycle (1/16 of a bit time) if the transmitter has been idle. The data strobe signal is LD XD DEL L, which is used to load a character from the Unibus into the transmitter buffer register (XBUF).

When the data has been loaded into the UART data buffer, it is next transferred to the transmitter shift register under control of signals from an encoder which selects the format determined by the control logic. This permits selection of parity or no parity (pin 35), the type of parity (pin 39), the number of STOP bits (pin 36), and the number of DATA bits per character (pins 37 and 38).

The transmitter logic converts the parallel character from the Unibus into a serial output that is in a format selected by the control logic.

The clock input to the timing generator (pin 40) is derived from the DL11-W baud rate circuits (Paragraph 4.9). The other input to the timing generator is the end-of-character (pin 24) signal from the output logic. This line goes high each time a full character (including STOP bits) is transmitted. If this line goes low, it prevents the timing generator from loading another character into the shift register. The line is normally high when data is not being transmitted and goes low at the start of transmission of the next character.

Whenever the transmitter data buffer is loaded while the previous character is being shifted through to the output line, the START bit of the new character immediately follows the last STOP bit of the previous character.

When the data strobe (pin 23) signal loads the UART data buffer, the DL11-W transmitter buffer (XBUF) is unloaded. Therefore, the data strobe signal sets the transmitter buffer empty (TRMT) flip-flop to provide a signal that becomes XRDY (transmitter ready). This XRDY signal can be read by the program and indicates that a new character can be loaded into the DL11-W transmitter buffer.

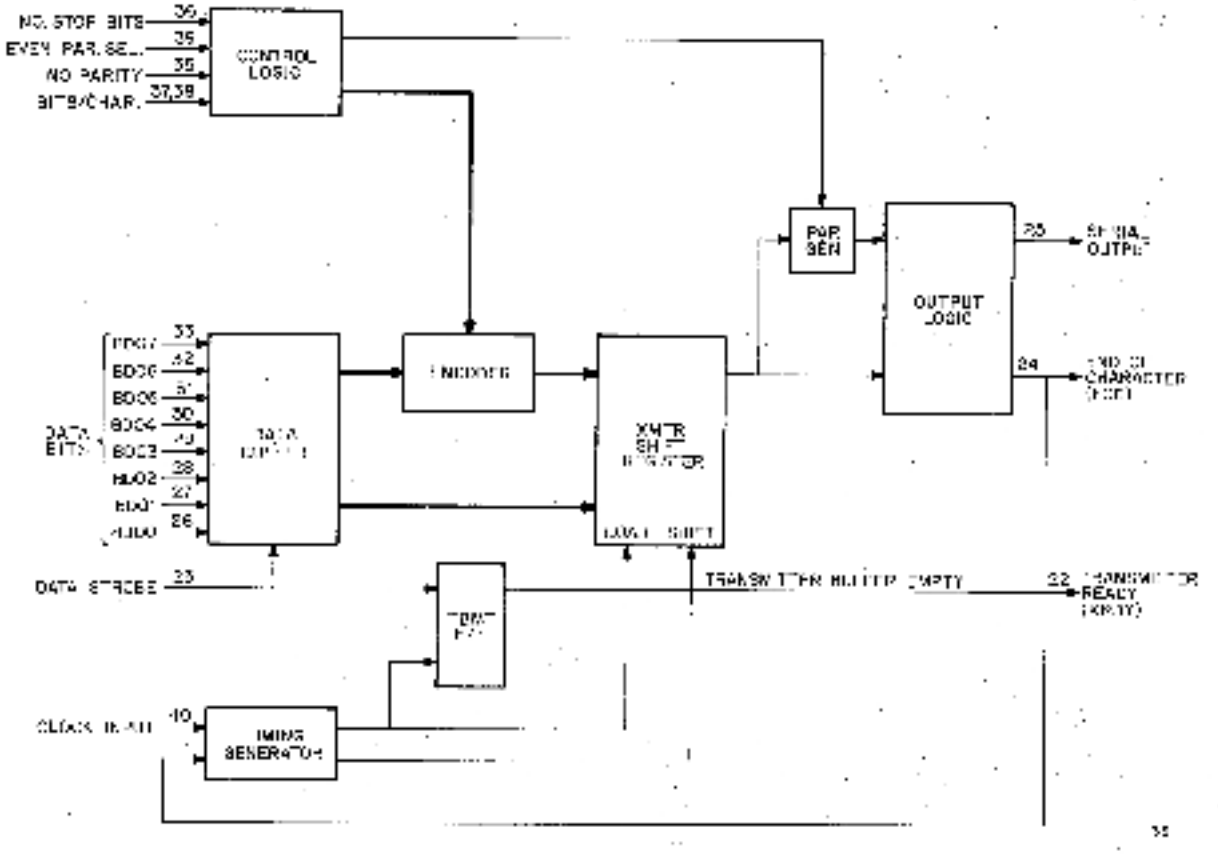


Figure 4-12 UART Transmitter

4.9 BAUD RATE LOGIC

The baud rate logic provides the clock frequencies and, therefore, the baud rates for both the receiver and transmitter sections of the DL11-W interface. The switch-selected baud rates on the DL11-W are all generated by a single crystal-controlled oscillator applied to two frequency divider circuits. Since all eight baud rates are simultaneously generated, any one of the eight baud rates may be selected for the receiver and transmitter sections. (Note that the frequencies required by the UART are 16 times the desired baud rates.)

The master oscillator operates at a frequency of 5.0688 MHz (DL-6). The output of this oscillator supplies two divider circuits. One divider circuit divides the oscillator output into seven frequencies which are multiples of 2400 Hz. The frequency of 2400 Hz is divided by 16 in the UART to provide a baud rate of 150. Thus, the seven baud rates put out by the first divider circuit are 150, 300, 600, 1200, 2400, 4800, and 9600. The other divider circuit produces a frequency of 1760 Hz, providing a baud rate of 110 at the UART.

The eight different baud rates are applied to two 8-to-1 multiplexers, one for the receiver clock and one for the transmitter clock.

Each of the multiplexers is controlled by three switches so that the RCVR CLK signal and XMIT CLK signal can be independently controlled. The switch settings for the various baud rate selections are shown in Table 2-1.

4.10 MAINTENANCE MODE LOGIC

The maintenance mode is used to check operation of the DL11-W control logic. Figure 4-13 is a simplified diagram of both the normal and maintenance modes. During normal operation, data from the bus is converted by the transmitter and sent to the external device, or data from the external device is converted by the receiver and sent to the bus.

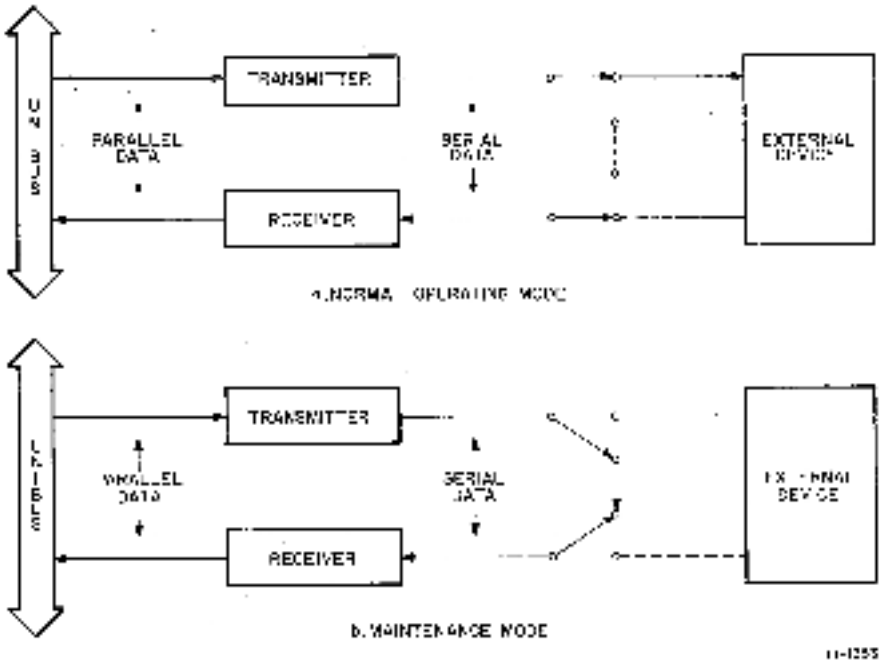


Figure 4-13 Operating Modes

During the maintenance mode, a character is loaded into the transmitter buffer (XBUF) from the Unibus. This parallel character is then converted to a serial output by the UART transmitter section. However, the serial data is fed back into the receiver, which converts it back to parallel data and places it on the bus. If the character received by the bus is identical to the character sent out on the bus, then both the transmitter and the receiver are functioning properly. In the maintenance mode, no data is sent to the external device.

Before the maintenance loop can be used, the transmitter must be selected for use and the transmitter buffer (XBUF) loaded with a character. The program selects the maintenance mode by setting bit 2 (MAINT bit) in the transmitter status register (XCSR). This sets the MAINT flip-flop in the transmitter logic (drawing D L-1, B-5).

The MAINT (1) H output of the flip-flop is used as an enabling level for a 4-to-1 multiplexer (a 74157 on drawing DL-1). A simplified version of this multiplexer is shown in Figure 4-14. Normally, the gates shown enabled by the MAINT (1) H signal in the figure are inhibited, and the serial output from the transmitter, as well as the clock signals, are fed to the logic used during the normal operating mode. However, when MAINT (1) H is present, the gates are qualified and perform two basic functions.

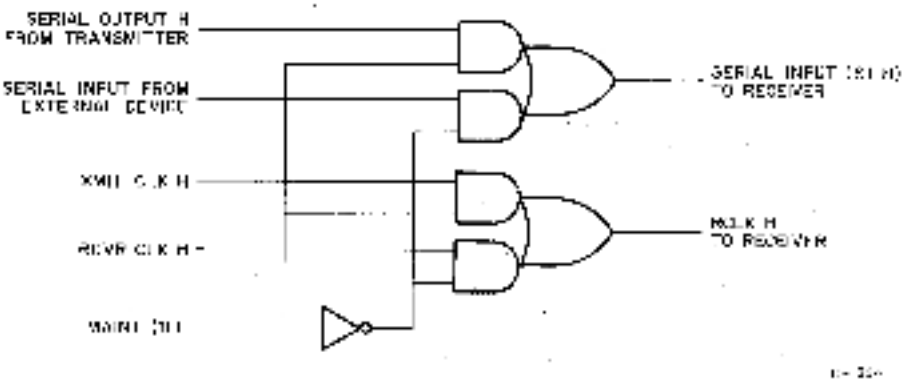


Figure 4-14 Maintenance Mode Logic

The first function is to gate the serial output of the transmitter (SERIAL OUT H) to the serial input line (SERIAL IN) of the receiver. The second function is to force the RCVR CLK pulse to be the same as the XMIT CLK, regardless of the switch position of the RCVR CLK. When MAINT (1) H is present, the gate receiving RCVR CLK H is inhibited and the XMIT CLK H pulse is gated through to the RCLK H line of the receiver. Although not shown in the figure, XMIT CLK H is also applied to the clock line of the transmitter.

Because the receiver logic is activated by a START bit (regardless of where the START bit comes from), the receiver is activated as soon as it receives the first input from the transmitter. After the receiver assembles the data, the program can compare the received character with the transmitted character to determine if the DL11-W interface is functioning properly.

4.11 20 mA CURRENT LOOP LOGIC

The 20 mA current loop circuits are provided for the serial data transmitter and receiver and for the paper tape reader control. Two modes of operation are available for the 20 mA current loop circuits: active and passive. In active mode, the DL11-W is the source of the 20 mA of current which is switched on or off, depending on the level of the SERIAL OUT line. In passive mode, the current loop circuit switches on or off current which is sourced by the external device. Figures 4-15 and 4-16 show simplified diagrams of the receiver and transmitter circuits in active and passive modes.

See Table 2-3 and Paragraph 2.1.4 for active and passive mode switch selection in connection with the transmitter, receiver, and paper tape reader enable circuits.

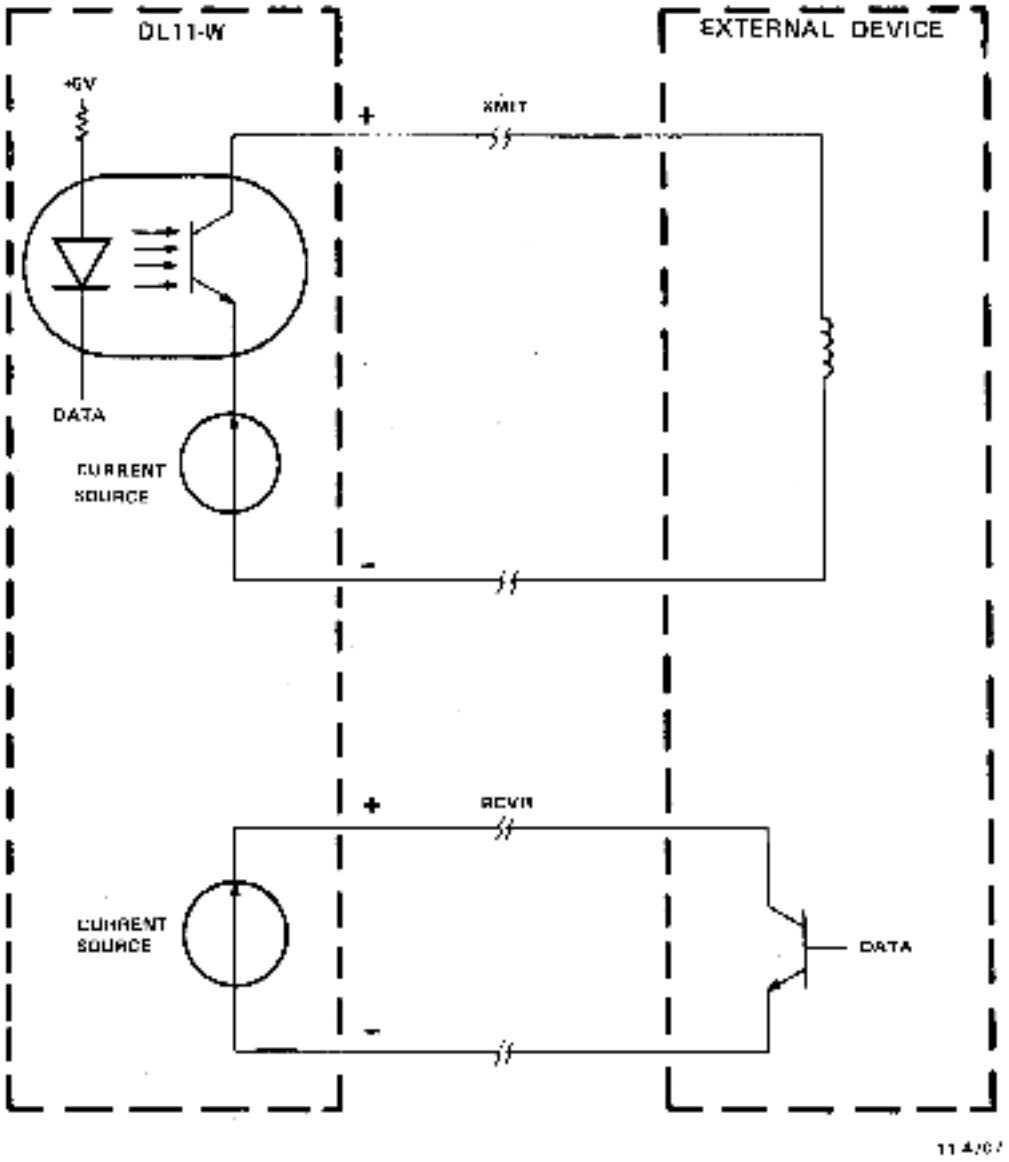


Figure 4-15 DL11-W in Active Mode

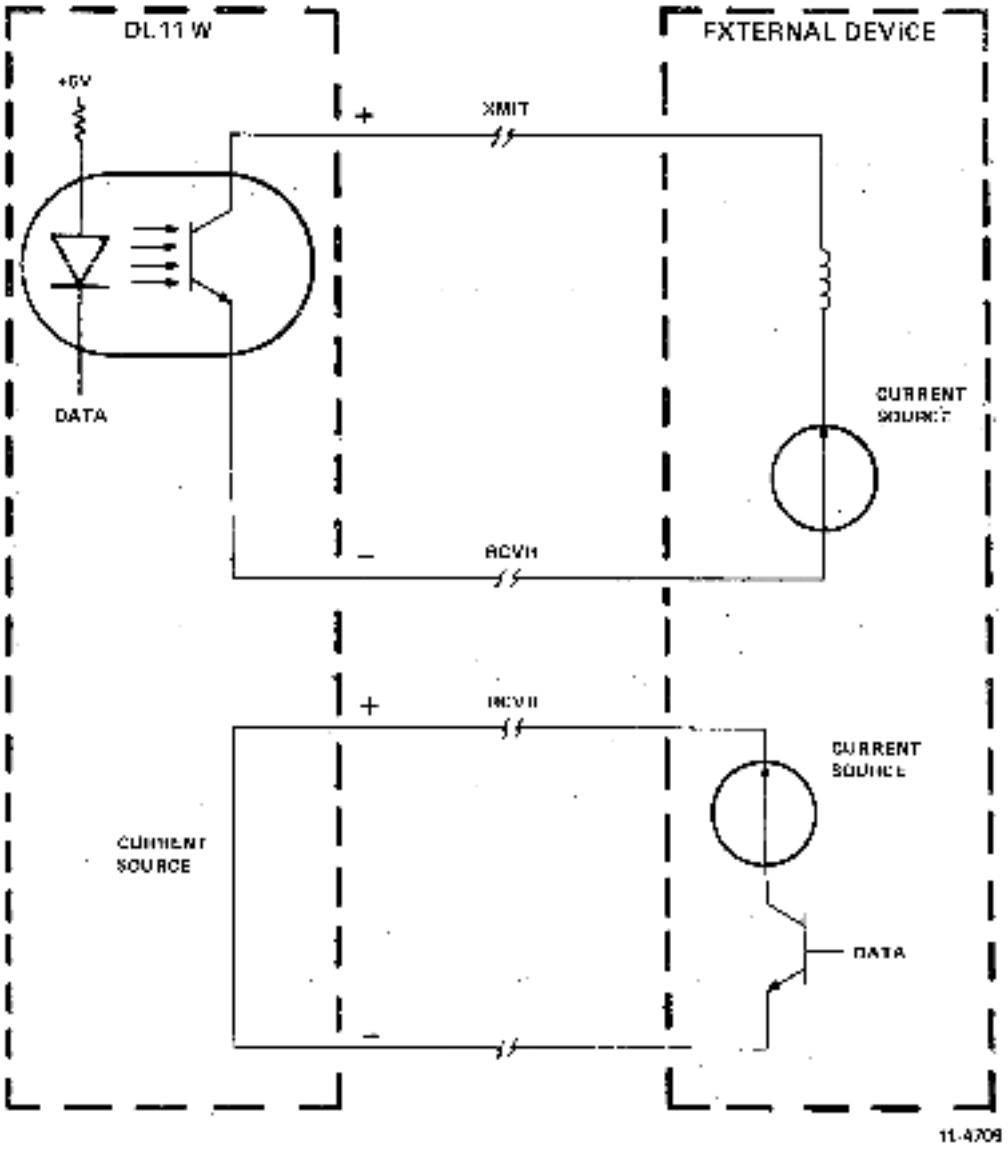


Figure 4-16 DL11-W in Passive Mode

4.12 EIA LEVEL CONVERTER LOGIC

Bipolar EIA level converters are provided for serial data out and serial data in interfacing. Serial output data, SERIAL OUT H, is applied to an EIA level converter and the output, which is a bipolar signal (approximately ±10 V), is available at pin F on the Berg connector. Bipolar EIA level input serial data is received at pin J on the Berg connector and converted to a TTL level signal, which is then available at pin H on the Berg connector. If EIA level interfacing is being used, pin M must be connected to pin E of the Berg connector. This is normally done by the connector on the cable used to interface the DL11-W and the external device.

The signals DATA TERMINAL RDY and RQT TO SEND are permanently strapped on (high) and are available at pins DD and V of the Berg connector, respectively.

APPENDIX A
IC SCHEMATICS

This appendix describes the integrated circuits listed below.

7492 Divide-By-Twelve Counter (Divide-by-Two and Divide-by-Six)

7493 4-Bit Binary Counter

74153 Dual 4-Line-to-1-Line Multiplexer

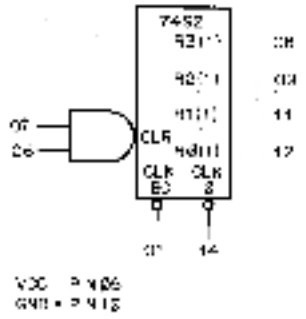
74175 Quad D-Type Edge-Triggered Flip-Flop

7492 DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

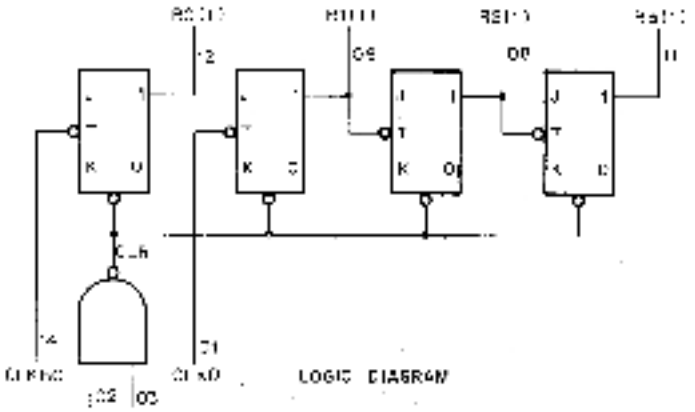
The 7496 is a monolithic 4-bit binary counter consisting of four master slave flip-flops that are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop R(0) is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

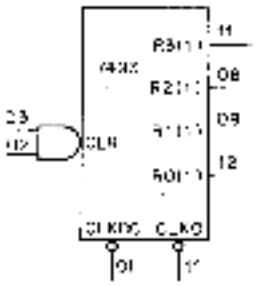
1. When used as a divide-by-twelve counter, output R0(1) must be externally connected to input CLKBC. The input count pulses are applied to input CLK0. Simultaneous divisions of 2, 6, and 12 are performed at the R0(1), R2(1), and R3(1) outputs as shown in the truth table.

2. When used as a divide-by-six counter, the input count pulses are applied to input CLKBC. Simultaneously, frequency divisions of 3 and 6 are available at the R2(1) and R3(1) outputs. Independent use of flip-flop R0 is available if the reset function coincides with reset of the divide-by-six counter.



7493 4-BIT BINARY COUNTER





V_{CC} = PIN 5
GND = PIN 10

7493A TRUTH TABLE
(SEE NOTES)

CLOCK INPUT PULSE	OUTPUT			
	Q$_D$	Q$_C$	Q$_B$	Q$_A$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

0 = LOW 1 = HIGH

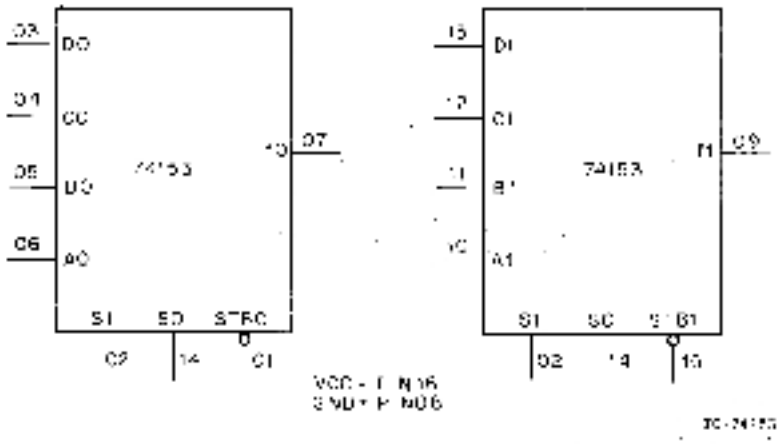
Notes:

1. [illegible] when 7493 [illegible] bit ripple-through counter.
2. Output R$_{0(1)}$ [illegible] input CLK$_D$.
3. To reset all outputs to logical 0 both pins R0 and R0 inputs must be high.
4. Either or both reset inputs R$_{9(1)}$ [pins 02 and 03] must be low to count.

74153 DUAL 4-LINE-TO-1-LINE MULTIPLEXER

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
S1	S0	A	B	C	D	STB	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S0 and S1 are common to both sections.
H = high level, L = low level, X = irrelevant.

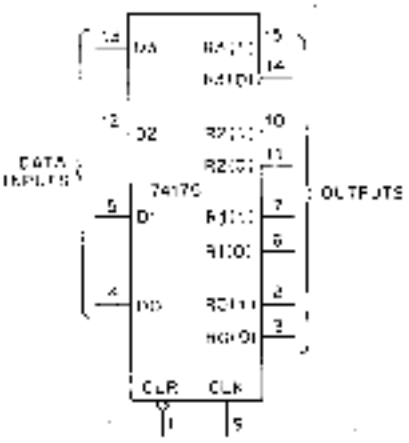


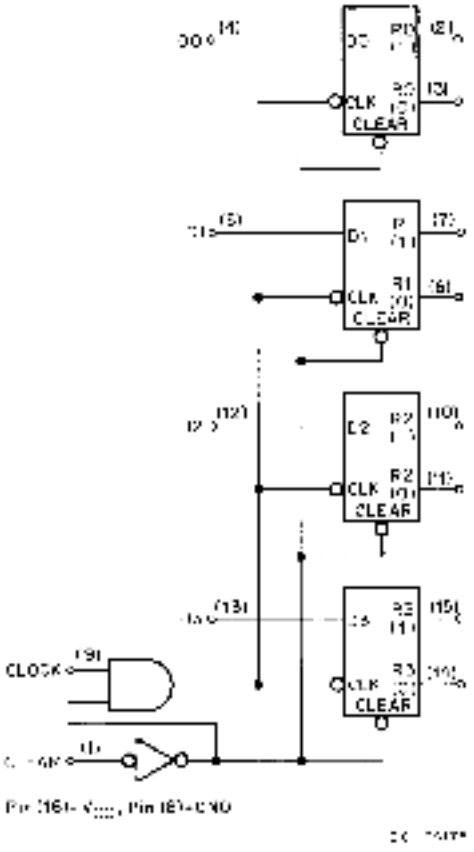
74175 QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOP

TRUTH TABLE

INPUT	OUTPUTS
t_n	t_{n+1}
D	Q1 Q1 Q2 Q2
H	H L L H
L	L H H L

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.





APPENDIX B
VECTOR ADDRESSING

Because the DL11-W SLU/RTC option is basically a communications device, interrupt vectors must be assigned according to the floating vector convention used for all communications devices. These vector addresses are assigned in order from 300 to 777, according to a specific method that ranks the types of devices in a particular PDP-11 system.

The first vector address (300) is assigned to the first DC11 Serial Asynchronous Line Interface in the system. The next DC11 (if used) is then assigned vector address 310, etc. The vector addresses are assigned consecutively to each unit of the second-ranked device type (KL11, DL11-A, DL11-B, or DL11-W), then to the third-ranked device (DBI1), and so on in accordance with the following list:

1. DC11 Asynchronous Line Interface
2. KL11 Teletype Control (or DL11-A, DL11-B, or DL11-W)
3. DP11 Synchronous Serial Modem Interface
4. DM11 Asynchronous Serial Line Multiplexer
5. DN11 Automatic Calling Unit
6. DM11-BB Modem Control
7. DR11-A Device Registers
8. DR11-C General Device Interface
9. DT11 Bus Switch
10. DL11-C Asynchronous Line Interface or DL11-W
11. DL11-D Asynchronous Line Interface or DL11-W
12. DL11-E Asynchronous Line Interface

If any of these devices is not included in a system, the vector address assignments move up to fill the vacancy. If a device is added to an existing system, its vector address must be inserted in the normal position and all other addresses must be moved accordingly. If this procedure is not followed, DIGITAL software cannot test the system.

Note that while the floating vectors range from addresses 300 to 777, addresses 500 through 534 are reserved for special bus testers. In addition, address 1000 is used for the DS11 Synchronous Serial Line Multiplexer.

An address map is shown in Figure B-1 and a list of the vector addresses is given in Table B-1. It should be noted that the system Teletype (KL11) is not part of the floating vector scheme and is assigned vector addresses 060 and 064; therefore, if a DL11-W is used as a control for the system Teletype console, it should be assigned addresses 060 and 064. All other DL11-Ws would follow the floating vector conventions

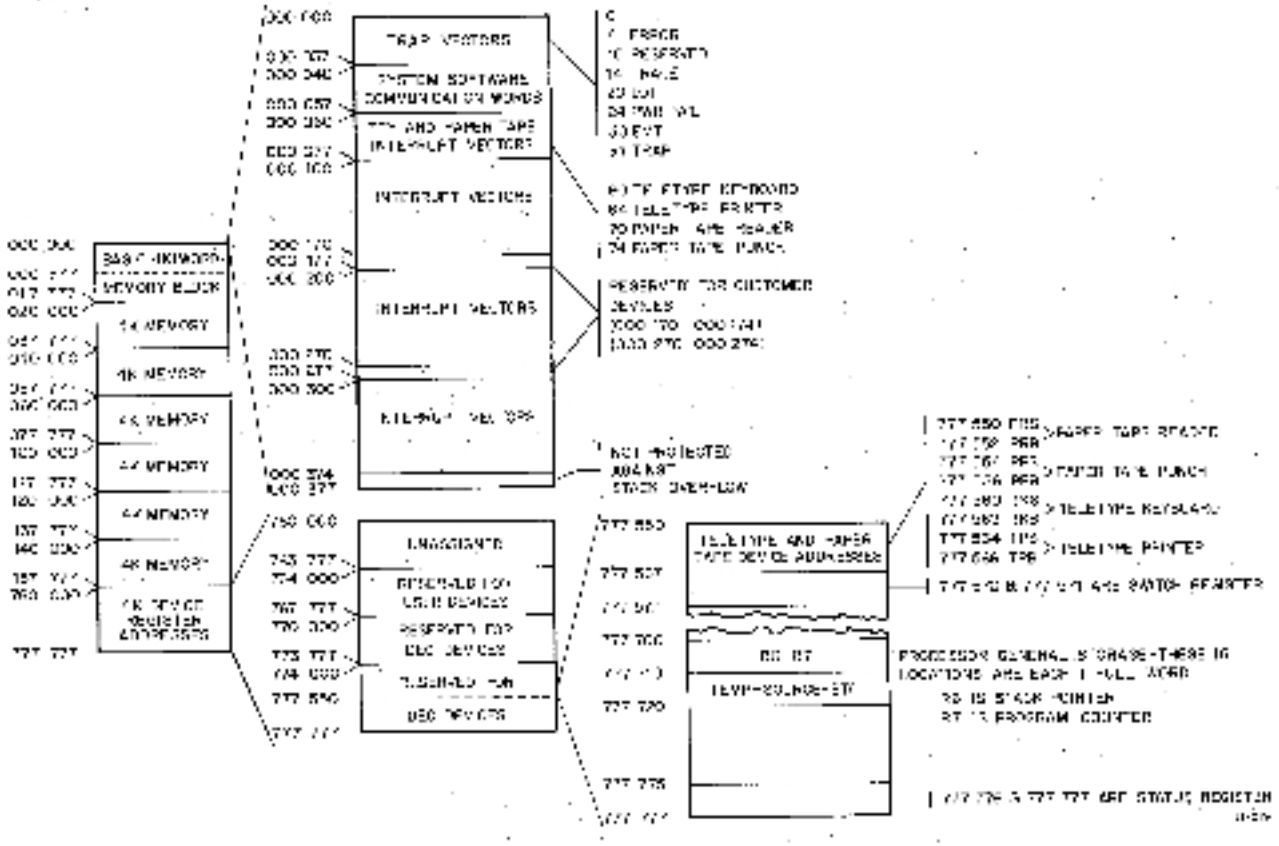


Figure B-1 Address Map

Table B-1 Interrupt Vectors

Address	Assignment
000	Reserved
004	Error Trap
010	Reserved Instruction Trap
014	Debugging Trap
020	IOT Trap
024	Power Fail Trap
030	EMT Trap
034	"Trap" Trap
040	System Software Communication Words
044	System Software Communication Words
050	System Software Communication Words
054	System Software Communication Words
060	Teletype In or DL11-W Console Interface
064	Teletype Out or DL11-W Console Interface
070	PC11 High-Speed Reader
074	PC11 High-Speed Punch
100	KW11-L Line Clock or DL11-W Line Clock
100	KW11-P Programmable Clock
110	DR11-A (Request A)
114	DR11-A (Request B)
120	XY11 X-Y Plotter
124	DR11-B
130	ADII
134	AFC11
140	AA11-A, -B, -C, -E Scope
144	AA11 Light Pen
150	
154	
160	
164	
170	User Reserved
174	User Reserved
200	LP11 Line Printer Control
204	RF11 Disk Control
210	RC11 Disk Control
214	TC11 DECtape Control
220	RK11 Disk Control
224	TM11 Magtape Control
230	CR11 Card Reader Control
234	UDC11
240	PDP-11/45 PIRQ
244	FPU Error
250	
254	RP11 Disk Pack Control
260	
264	
270	User Reserved
274	User Reserved
300	Floating vectors start at this address.

Table B-1 Interrupt Vectors (Cont)

Address	Assignment
304	
310	
314	
320	NOTE
324	Floating vectors start at address 300 and are assigned in the
330	following order:
334	
340	1. All DC11s
344	2. All KL11s*
350	3. All DP11s
354	4. All DM11s
360	5. All DN11s
364	6. All DM11-BBs
370	7. All DR11s
374	8. All DT11s
400	9. All DL11-Cs†
404	10. All DL11-Ds†
410	11. All DL11-Es
414	
420	
424	
430	
434	
440	
444	
450	
454	
460	
464	
470	
474	
500	Special Bus Testers
504	Special Bus Testers
510	Special Bus Testers
514	Special Bus Testers
520	Special Bus Testers
524	Special Bus Testers
530	Special Bus Testers
534	Special Bus Testers
540	
544	
550	
554	
560	
564	
570	
574	
600–774	Floating vectors end here.
1000	DS11

*Or DL11-As, DL11-Bs, DL11-Ws
†Or DL11-Ws

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