DL11
asynchronous line interface
user's manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The DL11 Asynchronous Line Interface is a character-buffered communications interface designed to assemble or disassemble the serial information required by a communications device for parallel transfer to, or from, the PDP-11 Unibus. The interface consists of a single integrated circuit quad module containing two independent units (receiver and transmitter) capable of simultaneous 2-way communication.

The DL11 interface provides the logic and buffer register necessary for program-controlled transfer of data between a PDP-11 system requiring parallel data and an external device requiring serial data. The interface also includes status and control bits that may be controlled by the program, the interface, or the external device for command, monitoring, and interrupt functions.

Five available DL11 options (DL11-A through DL11-E) provide the flexibility needed to handle a variety of terminals. For example, the user can use a DL11-A as a Teletype® Control or a DL11-E for complete dataset control of communications datasets such as the Bell Model 103 or 202. Depending on the option used, the user has a choice of line speeds (baud rates), character size, stop-code length, parity selection, line control functions, and status indications.

Although each option uses an M7800 module, certain discrete component variations exist for each specific option so that the interface performs the intended function. Therefore, although generally similar, each option uses a slightly different M7800 variation which is not interchangeable with other options. These variations are installed at the factory only. For example, an M7800 used as a DL11-A could be used as another DL11-A but not in place of a DL11-B, C, D, or E.

A description of the individual options is given in Chapter 2 of this manual.

1.2 SCOPE

This manual provides the user with the introductory, installation, and programming information necessary to understand and operate the DL11 Asynchronous Line Interface. The level of discussion assumes that the reader is familiar with basic digital computer theory.

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The manual is divided into five major chapters: General Description, Installation and Configuration, and Programming. A complete set of engineering drawings is provided with each DL11 interface and is bound in a separate volume entitled *DL11 Asynchronous Line Interface, Engineering Drawings.*

In all cases, the information contained in this manual refers to all five options (DL11-A through DL11-E) unless specifically stated otherwise. Although control signals and data are transferred between the interface and the Unibus, and between the interface and the communications device, this manual is limited to coverage of only the interface itself.

Table 1-1 lists related PDP-11 system documents that are applicable to the DL11 Asynchronous Line Interface. Table 1-2 lists documents applicable to communications devices that may be used with the interface. Note that this latter table lists only representative manuals and is not intended to be an all-inclusive list.

Table 1-1
Applicable PDP-11 Documents

Title	Number	Description
PDP-11 System Manual		Provides detailed theory of operation, flow, logic diagrams, operation, installation, and maintenance for components of the applicable PDP-11 system including processor, memory, console, and power supply.
PDP-11 Peripherals Handbook		Provides a discussion of the various peripherals used with PDP-11 systems. It also provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
Paper-Tape Software Programming Handbook	DEC-11-XPTSA-A-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming and the floating-point and math package.

Table 1-2
Applicable Device Documents

Title	Number	Description
Automatic Send-Receive Sets, Manual	Bulletin 273B (two volumes) Teletype Corp.	Describes operation and maintenance of the Model 33 ASR Teletype unit used as an input/output device.
Model 33 Page Printer Set, Parts	Bulletin 1184B Teletype Corp.	Contains an illustrated parts breakdown to serve as a guide for disassembly, reassembly, and parts ordering for the Model 33 ASR Teletype unit.
		NOTE **Comparable manuals exist for other available Teletypes such as the Model 28, Model 35, and Model 37.**
VT05 Alphanumeric Display Terminal	EK-VT05-HR-002	Describes purpose and operation of the VT05 Display used as an input/output device.
VT05 Alphanumeric Display Terminal, Maintenance Manuals,	EK-VT05-MM-005	Provides detailed theory of operation and maintenance procedures for the VT05 Display.
VT06 Maintenance Manual	Datapoint Corp.	Provides detailed theory of operation and maintenance data for the VT06 Data Display Terminal.
Bell System Data Communications Data Sets 103 E/G/H		Provides dataset interface specifications; includes dataset description and options including interface signals and timing.
Bell System Data Communications Data Sets 202 C/D		Provides dataset interface specifications; includes dataset description and options including interface signals and timing.

1.3 MAINTENANCE

The basic maintenance philosophy of the DL11 Asynchronous Line Interface is to present the user with the information necessary to understand normal system operation. The user can utilize this information when analyzing trouble symptoms to determine necessary corrective action. A Modem Test Connector (Engineering Drawing D-CS-H315-0-1) can be used in troubleshooting the DL11.

1.4 ENGINEERING DRAWINGS

A complete set of engineering drawings and circuit schematics is provided in a companion volume to this manual entitled *DL11 Asynchronous Line Interface, Engineering Drawings.* The following paragraphs describe the signal nomenclature conventions used on the drawing set.

Signal names in the DL11 print set are in the following basic form:

SOURCE	SIGNAL NAME	POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block (DL-1, DL-2, DL-3, etc.).

SIGNAL NAME is the name proper of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3V; L means ground.

As an example, the signal:

DL-4 RCVR DONE H

originates on sheet 4 of the M7800 module drawing and is read, "when RCVR DONE is true, this signal is at +3V."

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

Interface signals fed to, or received from, the Berg connector on the M7800 module are preceded by the pin number in parentheses:

(DD) EIA DATA TERMINAL READY

CHAPTER 2
GENERAL DESCRIPTION

2.1 INTRODUCTION

The DL11 Asynchronous Line Interface is a character-buffered communications interface designed to translate serial bit stream data to parallel character data. The interface contains two independent units (receiver and transmitter) capable of simultaneous 2-way communication.

The five available DL11 options (DL11-A through DL11-E) provide the flexibility needed to handle a variety of terminals. For example, the user can select an option for interfacing a Teletype or display keyboard, for handling EIA data, or for handling dataset devices. In addition, depending on the option used, the user has a choice of line speeds, character size, stop-code length, and parity.

This chapter is divided into five major portions: available options, data format, functional description, physical description, and specifications.

2.2 AVAILABLE OPTIONS

There are five available DL11 options: DL11-A through DL11-E. The major differences among these options are the data code, baud rates, and certain control and monitoring bits in the status registers. Although there are five options, they may be divided into the following functional groups:

a.	Teletype Control	–	DL11-A DL11-C	–	The DL11-A and DL11-C both use a 20-mA current loop for receive, transmit, and reader run operations necessary for Teletype or display terminal control. The DL11-C is simply a more flexible version of the DL11-A and includes data code and baud rate selection.
b.	EIA Terminal Control	–	DL11-B DL11-D	–	The DL11-B and DL11-D both contain EIA drivers and receivers for compatibility with the logic levels required for EIA terminals such as the VT06 display. The DL11-D is simply a more flexible version of the DL11-B and includes data code and baud rate selection.
c.	Data Set Control	–	DL11-E	–	The DL11-E provides complete data set control for communications modems such as Bell Model 103 or 202.

A brief description of each of these options is included in Table 2-1 and a listing of available standard baud rates is given in Table 2-2. Note that these baud rates are based on the standard crystals supplied by DEC; however, the user may order special crystals, if desired. The physical differences of each option (cables, connectors, etc.) are described in Paragraph 2.5.

Table 2-1
DL11 Options

Option	Data Code	Typical Use	Baud Rates	Notes	Description
DL11-A	Restricted(1)	Model 33 or 35 Teletype Model VT05 Display Terminal	110 150 300 600 1200 2400	a. No dataset bits a. No BREAK or ERROR bits c. No 1200/110 split	Uses 20-mA current loop operation for receive, transmit, and reader run.
DL11-B	Restricted(1)	Model VT05 or VT06 Display Terminal	Same as DL11-A	a. No dataset bits b. No BREAK or ERROR bits c. No 1200/110 split d. DATA TERMINAL RDY and REQ TO SEND bits strapped on permanently e. Null modem usually required for local EIA terminal	Has EIA drivers and receivers for compatibility with EIA terminals.
DL11-C	Full Selection(2)	Model 28 Teletype	Crystal and switch selectable(3)	a. No dataset bits b. BREAK and ERROR bits enabled	Basically identical to DL11-A except has full code and baud rate selection. Also includes both BREAK and ERROR bits.
DL11-D	Full Selection(2)	Model 37 Teletype (null modem required)	Crystal and switch selectable(3)	a. No dataset bits b. BREAK and ERROR bits enabled c. DATA TERMINAL RDY and REQ TO SEND bits strapped on permanently	Basically identical to DL11-B except has full code and baud rate selection. Also includes both BREAK and ERROR bits.

(continued on next page)

Table 2-1 (Cont)
DL11 Options

Option	Data Code	Typical Use	Baud Rates	Notes	Description
DL11-E	Full Selection[2]	Model 103 or 202 modems	Crystal and switch select-able[3]	a. Full dataset control	Provides complete dataset control. Dataset lines monitored by this interface are: RING, RECEIVE DATA, CARRIER DETECT, CLEAR TO SEND, and SECONDARY RECEIVE DATA. Dataset lines controlled by the program are: TRANS-MITTED DATA, REQUEST TO SEND, SECONDARY TRANSMITTED DATA, and DATA TERMINAL READY.

NOTES: 1. Restricted data code = 8 data bits, no partiy, 1 or 2 stop bits.
2. Full selection data code = 5, 6, 7, or 8 data bits; parity off, even, or odd; and 1, 1.5, or 2 stop bits.
3. Baud rates that may be selected by the crystal and switch are listed in Table 2-2.

Table 2-2
Baud Rates with Standard Crystals

Switch Position	Crystal #1 (844.8 kHz)	Crystal #2 (1.03296 MHz)	Crystal #3 (1.152 MHz)	Crystal #4 (4.608 MHz)
1	36.7	44.8	*50*	200
2	55	67.3	*75*	*300*
3	*110*	*134.5*	*150*	*600*
4	220	269	*300*	*1200*
5	440	538	*600*	*2400*
6	880	1076	*1200*	*4800*
7	1320	1614	*1800*	*7200*
8	1760	2152	*2400*	*9600*
9*	–	–	–	–
10*	–	–	–	–

*These switch positions are for external clock inputs and do not tap off the crystal oscillator.
NOTE: The baud rates in italics are the most commonly used.

2.3 DATA FORMAT

There are two basic data formats used with the DL11 interface options. The first format (Figure 2-1,a) is referred to as "restricted" because the only variable is the number of STOP bits. A character in this format consists of a START bit, eight DATA bits, and one or two STOP bits. This code is used only with the DL11-A and DL11-B options.

The second format (Figure 2-1,b) is referred to as "full selection" because there is a number of variables. This format consists of a START bit, five to eight DATA bits, a PARITY bit or no PARITY bit, and one, one and one-half, or two STOP bits.

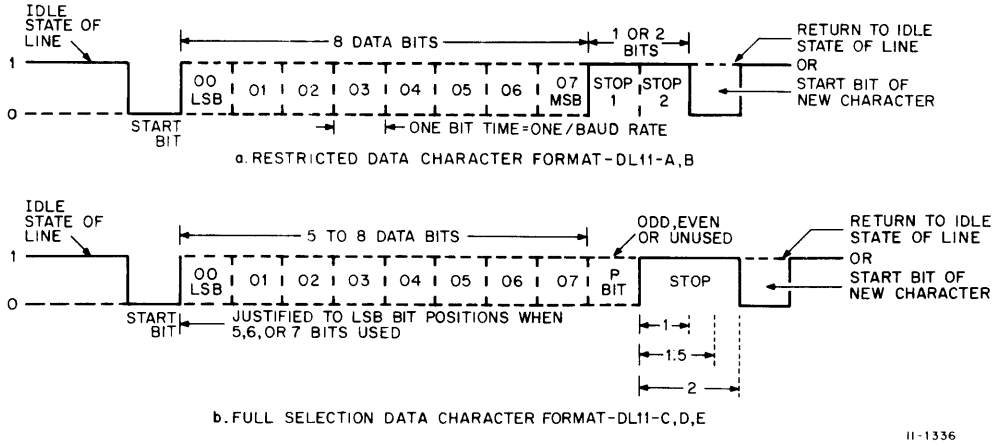


Figure 2-1 DL11 Data Formats

When less than eight DATA bits are selected in the second format, the hardware justifies the bits into the least significant bit positions for characters received by the interface. When transmitting characters, the program provides the justification into the least significant bits. The PARITY bit may be either on or off; when on, it can be selected for checking either odd or even parity during receive and for providing an extra PARITY bit during transmit.

All variable items within any data format are selected by jumpers on the DL11 module. None of the variables can be controlled by the program. Split lugs are provided on the module for installation of appropriate jumpers. These jumpers are listed in Table 2-3.

Note that a jumper indicates a low (0) and no jumper indicates a high (1). The jumper locations are shown on DL11 drawing DL-4.

Table 2-3
Data Format Jumpers

Name	Jumper	UART Pin No.	Function
No Parity	NP	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select (EPS) jumper. When disabled, the STOP bits immediately follow the last DATA bit during transmission. During reception, the receiver does not check for parity. jumper – parity enabled no jumper – parity disabled
Even Parity	EPS	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. jumper – odd parity no jumper – even parity
STOP Bit	2SB	36	Used in conjunction with three other jumpers (J9, J10, and J11) to select the desired number of STOP bits. 1 STOP bit – jumper in 2SB jumper in J10 no jumpers in J9, J11 2 STOP bits – no jumper in 2SB no jumpers in J9, J11 jumper in J10 1.5 STOP bits – jumper in 2SB jumper in J9 or J11 no jumper in J10
Number of Data Bits	NB1 NB2	38 37	These two jumpers are used together to provide a code that selects the desired number of DATA bits in the character. Note that in the following code, a 0 indicates a jumper, a 1 indicates no jumper: **NB2 NB1 No. of DATA Bits** 0 0 5 0 1 6 1 0 7 1 1 8

2.4 FUNCTIONAL DESCRIPTION

The DL11 is a character-buffered communications interface that performs two basic operations: receiving and transmitting asynchronous data. When receiving data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the Unibus. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or the external device.

Although there are actually five DL11 options, the prime functional differences can be shown by presenting three typical cases: a DL11 used for dataset devices, a DL11 used as a Teletype control, and a DL11 used with EIA level converters. Each of these three cases is covered separately in Paragraphs 2.4.1 through 2.4.3, respectively.

2.4.1 DL11 Dataset Interface

Only the DL11-E (Figure 2-2) option can be used to interface to datasets. The DL11 uses call and acknowledge signals from the computer and the dataset, translates these signals to set up a handshaking sequence, and thus establish a data communication channel.

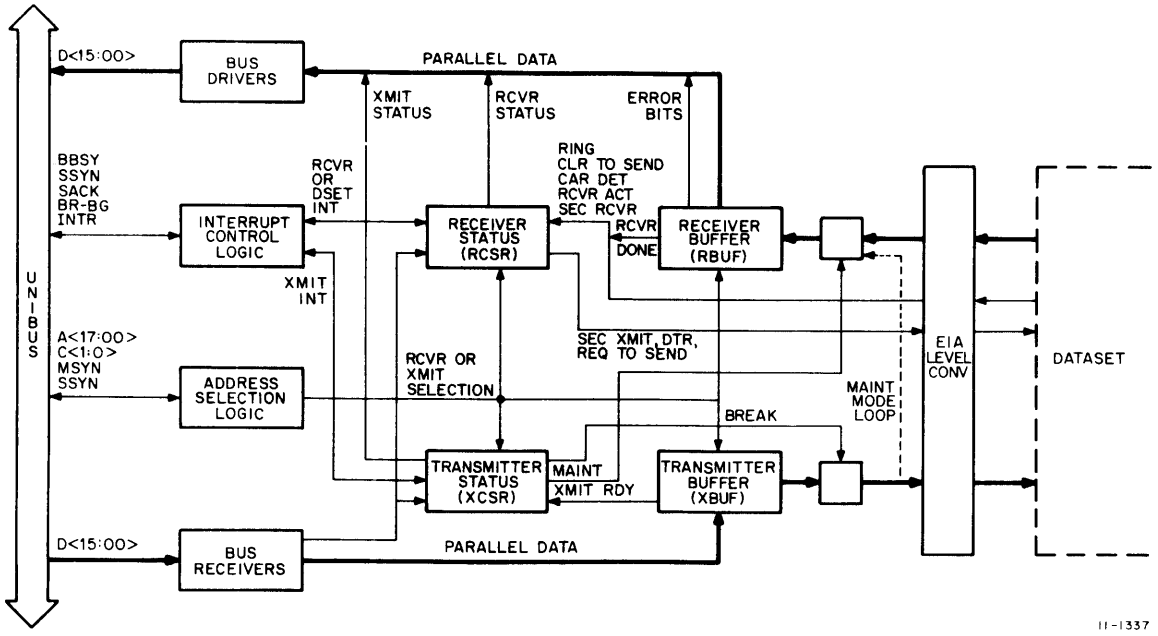


Figure 2-2 DL11-E Block Diagram

A typical method of establishing a data communication channel is as follows: the dataset at the computer is called by another remote dataset and a RING signal is transmitted to the DL11 interface. This RING signal initiates an interrupt provided the DATASET INT ENB bit in the DL11 register is set. The program then determines if the interrupt was caused by RING and, through a service routine, issues a DATA TERMINAL READY and a REQ TO SEND signal. These signals cause the dataset to answer the call and send a carrier signal or tone to the caller. The caller acknowledges the carrier signal with its own carrier signal which, when detected by the dataset, causes another interrupt (CARRIER) sequence to be initiated. Upon recognizing the CARRIER interrupt, the program can then either receive or transmit data. The only two prerequisites for the handshaking sequence are that the program use appropriate service routines and that the DATASET INT ENB bit in the DL11 status register is set prior to setting up the data channel.

Once the data channel is set up, the DL11-E receiver accepts incoming serial data from the dataset lines for parallel conversion and transfer to the Unibus. The transmitter converts parallel data from the bus and shifts the resultant serial data onto the dataset lines.

The receiver offers serial-to-parallel conversion of 5, 6, 7, or 8 level codes. This serial character code is described in Paragraph 2.3. Once the character has been received, a parity error flag, if selected, is available to the programmer for testing. An interrupt request (RCVR DONE flag) is initiated in the middle of the first STOP bit of the character being received. This indicates that the character is stored in the receiver holding register. If the program does not transfer the character from the holding register before the middle of the first STOP bit of the next character, a data overflow error (OR ERR) bit is set in the receiver buffer register. This buffer also provides other error indications such as framing error (FR ERR) which indicates that the character had no valid STOP bit, and partiy error (P ERR) which indicates that the received parity did not agree with the expected parity. It should be noted that both the receiver and transmitter character length and format are controlled by jumpers on the module and are always identical.

The transmitter performs parallel-to-serial conversion of 5, 6, 7, or 8 level codes. Data from the Unibus is loaded in parallel into the holding register. When the transmitter shift register is empty, the contents of the holding register is shifted into the transmitter shift register and the XMIT RDY flag comes up. A second character from the bus can then be loaded into the holding register. However, because the shift register is still working on previous data, the shifting operation of the second character is delayed until the previous character has been completely transmitted. Once the last bit of a character is transferred to the dataset (because of double-buffering, this is actually the last bit of the first character in a 2-character pair), the interface initiates an interrupt request (XMIT RDY) to indicate that the buffer is empty and can now be loaded with another character for transfer to the dataset. The transmitter status register contains a BREAK bit that can be set to transmit a continuous space to the dataset. A maintenance (MAINT) bit is also available for connecting the serial output of the transmitter to the input of the receiver and to force the receiver clock speed to be the same as the transmitter speed.

The rest of the control portion of the DL11-E is available through the receiver status register, and provides the necessary command and monitoring functions for use with Bell 103 and 202 type datasets. This register monitors such functions as: CLEAR TO SEND, which indicates the operating condition of the dataset; CAR DET, which indicates that the carrier is being received; RCVR ACT, which indicates that the receiver is accepting a character; and RCVR DONE, which indicates that a full character is stored in the receiver buffer.

Dataset interrupt requests are initiated at the transition of RING, CAR DET, CLR TO SEND, or SEC REC signals. The SEC REC (secondary or supervisory received data) and the SEC XMIT (secondary or supervisory transmitted data) bits provide receive and transmit capabilities for the reverse channel of a remote station. The DTR bit functions as a control lead for the dataset communication channel and permits the channel to be either connected or disconnected.

The DL11-E option contains EIA level converters for changing the bipolar inputs to TTL logic levels and the TTL logic level outputs to the bipolar signals required by the dataset. The EIA converters provide failsafe operation of the control leads because they appear off if the dataset loses power.

2.4.2 DL11 Teletype Control

Both the DL11-A and DL11-C options can be used to interface Teletype units. The prime difference between the two is that the DL11-C can operate with a variable character format and is available in several different baud rates. The DL11-A option (Figure 2-3) is normally used to interface Model 33 and 35 Teletypes; the DL11-C option could be used to interface Model 28 Teletypes.

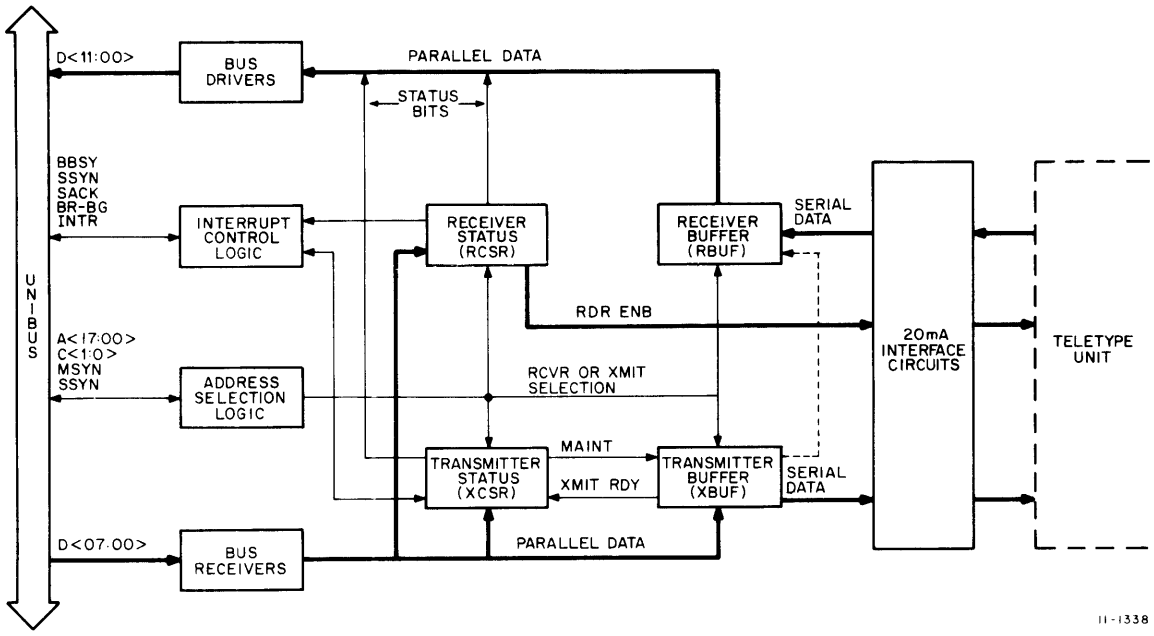


Figure 2-3 DL11-A Block Diagram

Serial information read or written by the Teletype unit is assembled or disassembled by the DL11 interface for parallel transfer to, or from, the Unibus. When the processor addresses the bus, the DL11 interface decodes the address to determine if the Teletype is the selected external device and, if selected, whether it is to perform an input (read) or output (punch) operation.

If, for example, the Teletype has been selected to accept information for printout, parallel data from the Unibus is loaded into the DL11 transmitter (punch) buffer. At this point, the XMIT RDY flag drops because the transmitter (punch) logic has been activated (the flag comes back after a fraction of a bit time if the transmitter is not presently active). The interface generates a START bit, shifts the data from the buffer into the Teletype one bit at a time, again sets the XMIT RDY flag (as soon as the holding register of the double-buffering is empty, even though the shift register is active), and then times out the required number of STOP bits.

Thus, if the DL11-A option is being used, the 8-bit parallel bus data is converted to the 11-bit serial input required by the Teletype. If the DL11-C option is used, the format and character length may be different, but the parallel-to-serial conversion is accomplished in the same manner. Note that whenever a series of characters is to be loaded into the Teletype, the XMIT RDY flag is set prior to generation of the STOP bits and the shifting out of the character in the holding register, thus allowing another character to be loaded from the bus as soon as the transmitter holding buffer is empty. The XMIT RDY flag is used to initiate an interrupt sequence to inform the processor that the interface is ready to transfer another character to the Teletype for printing.

When receiving data from the Teletype unit, the operation is essentially the reverse. The START bit of the Teletype serial data activates the interface receiver logic, and data is loaded one bit at a time into the reader buffer register. When loading of the buffer is complete, the buffer contents is transferred to the holding register and the interface sets the RCVR DONE flag, indicating to the program that a character has been assembled and is ready for transfer to the bus. The RCVR DONE flag, if RCVR INT ENB is also set, initiates an interrupt sequence, thereby causing a vectored interrupt.

The DL11-A and DL11-C options both have a reader enable (RDR ENB) bit that can be set to advance the paper-tape reader in the Teletype. When set, this bit clears the RCVR DONE flag. As soon as the Teletype sends another character, the START bit clears the RDR ENB bit, thus allowing just one character to be read.

The DL11-A and DL11-C options also have a receiver active (RCVR ACT) bit which indicates that the DL11 interface is receiving data from the Teletype. This bit is set at the center of the START bit, which is the beginning of the input serial data, and is cleared by the leading edge of the RCVR DONE bit. The DL11-C also has a BREAK bit which can be set by the program to transmit a continuous space to the Teletype.

The DL11-A and DL11-C options, as well as all other DL11 options, can be operated in a maintenance mode which is selected by the program by setting the MAINT bit in the transmitter status register. When in this mode, special logic is used to perform a closed loop test of interface logic circuits. A character from the bus is loaded in parallel into the transmitter (punch) buffer register. The serial output of this register, besides entering the Teletype, enters the receiver (reader) buffer register where it is converted back into parallel data and transferred to the bus. If the DL11 is functioning properly, the character in the reader buffer (RBUF) is identical to the character loaded into the transmitter buffer (XBUF).

2.4.3 DL11 EIA Terminal Control

Both the DL11-B and DL11-D options provide the control logic required for interfacing EIA terminals such as the VT06 Display or the Model 37 Teletype. The prime difference between these two options is that the DL11-D can operate with a variable format and is available in several baud rates.

Functionally, the DL11-B and DL11-D operate in an identical manner to the DL11-A and DL11-C, respectively (Paragraph 2.4.2). However, both the DL11-B and DL11-D options have additional logic consisting of EIA level converters for changing bipolar inputs to TTL logic levels and for changing the TTL logic level outputs to the bipolar signals required by EIA terminals.

2.5 PHYSICAL DESCRIPTION

The DL11 interface is packaged on a single M7800 Quad Intergrated Circuit Module that can easily be plugged into either a small peripheral controller slot in the processor or into one of the four slots in a DD11-A Peripheral Mounting Panel. When the DD11-A is used, up to four DL11 interfaces can be mounted in a single system unit.

Power is applied to the logic through the power harness already provided in the BA11 Mounting Box. The required current is approximately 1.8A at +5V and 150 mA at -15V. If one of the EIA options is used (DL11-B, D, or E), then 50 mA of current, at a level between +9V and +15V, is also required.

The M7800 module has a Berg connector for all user input/output signals. The specific signals fed to this connector depend on the particular option used. The signals transferred between the M7800 and the external device are dependent on the specific cable used with the selected option. Mounting, cabling, and connector information is given in Chapter 3.

The specific baud rate used with the DL11 interface is selected by a switch which taps off the frequency divider output of a crystal oscillator.

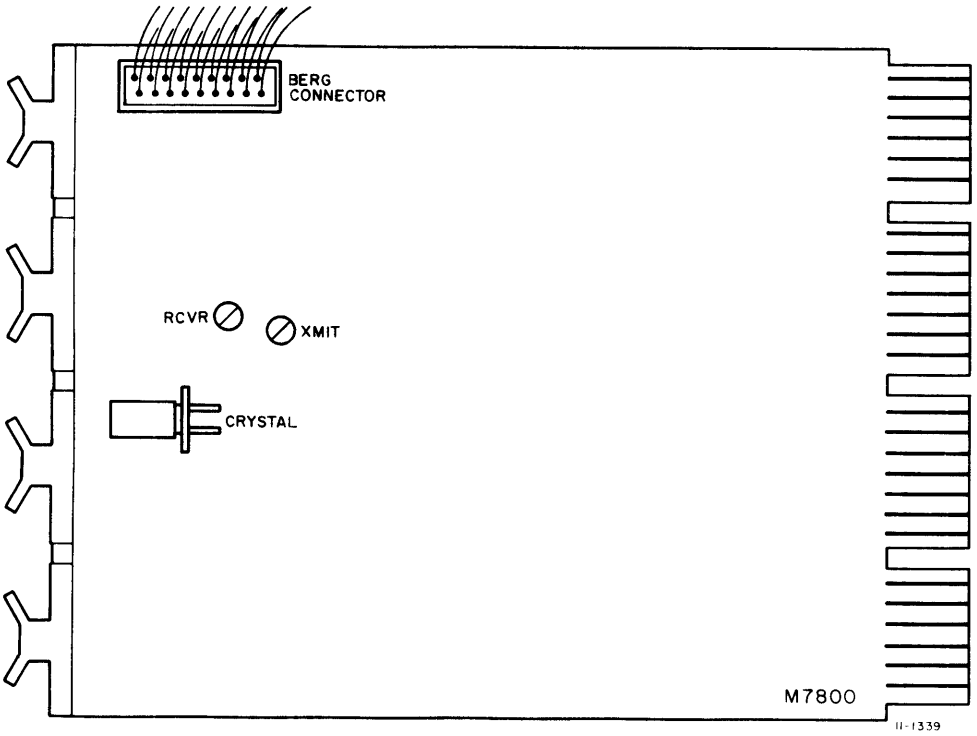


Figure 2-4 Crystal and Switch Location

One of four available crystals (1.03296 MHz, 844.8 kHz, 1.152 MHz, or 4.608 MHz) is mounted on the M7800 module as shown on Figure 2-4. The user may use a different crystal if desired, but the DL11 operating speed is limited from 40 baud to 10K baud.

Figure 2-4 also shows the position of the two switches used to select the baud rate. Both switches are identical: one is used for the receiver portion of the interface, the other is used for the transmitter. Each switch is a 10-position rotary switch. Positions 9 and 10 are used to select an external clock. Positions 1 through 8 are used to select the baud rate from the crystal. The standard available baud rates selected by each switch position are listed in Table 2-2.

2.6 SPECIFICATIONS

Operating and physical specifications for the DL11 Asynchronous Line Interface are given in Table 2-4. Unless otherwise specified in the table, the specifications refer to all five DL11 options.

Table 2-4
DL11 Operating Specifications

Specification	Options	Description
Registers	All	Receiver Status Register (RCSR) Receiver Buffer Register (RBUF) Transmitter Status Register (XCSR) Transmitter Buffer Register (XBUF)
Register Addresses	DL11-A or DL11-B	RCSR 777560 RBUF 777562 XCSR 777564 XBUF 777566 } when used as console
		RCSR 776XX0 RBUF 776XX2 XCSR 776XX4 XBUF 776XX6 } XX = 50 through 67 for up to 16 interfaces
	DL11-C, D, or E	RCSR 77XXX0 RBUF 77XXX2 XCSR 77XXX4 XBUF 77XXX6 } XXX = 561 through 617 for up to 31 interfaces
Interrupt Vector Address	DL11-A or DL11-B	060 = Receiver 064 = Transmitter } when used as console
	All	Floating Vectors (Appendix A)
Priority Level	DL11-A, B, C, D, or E	BR4 (may be changed by jumper plug)

(continued on next page)

Table 2-4 (Cont)
DL11 Operating Specifications

Specification	Options	Description
Interrupt Types	DL11-A, B, C, or D	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE)
	DL11-E	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Dataset Interrupt (DATASET INT) which is caused by one of the following: CAR DET (carrier detect) RCV ACT (receiver active) SEC REC (secondary receiver) RING (ringing signal)
Commands	DL11-A, B	Receiver Interrupt Enable (RCVR INT ENB) Transmitter Interrupt Enable (XMIT INT ENB) Reader Enable (RDR ENB) Maintenance Mode (MAINT)
	DL11-C, D	All of the above commands plus BREAK.
	DL11-E	All of the above commands plus the following commands: Dataset Interrupt Enable (DATASET INT ENB) Secondary Transmit (SEC XMIT) Request to Send (REQ TO SEND) Data Terminal Ready (DTR)
Status Indications	DL11-A, B	Receiver Active (RCVR ACT) Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE)
	DL11-C, D	Same as DL11-A plus the following: Error (ERROR) Overrun (OR ERR) Framing Error (FR ERR) Parity Error (P ERR)
	DL11-E	Same as DL11-C plus the following: Clear to Send (CLR TO SEND) Carrier Detect (CAR DET) Secondary Receive (SEC REC) Ring (RING)

(continued on next page)

Table 2-4 (Cont)
DL11 Operating Specifications

Specification	Options	Description
Data Input and Output	DL11-A, C	Serial data, 20-mA active current loop.
	DL11-B, D	Serial data, conforms to EIA and CCITT specifications.
	DL11-E	Serial data, EIA and CCITT specifications, compatible with Bell 103 and 202 datasets.
Data Format	DL11-A, B	1 START bit, 8-bit DATA character, 1 or 2 STOP bits.
	DL11-C, D or E	1 START bit; 5, 6, 7, or 8 bit DATA character; PARITY bit (odd, even, or unused); 1, 1.5, or 2 STOP bits.
Data Rates	DL11-A, B	Baud rate restricted to 110, 150, 300, 600, 1200, and 2400. No 1200/110 split.
	DL11-C, D, or E	Baud rate dependent on crystal used and switch position (Table 2-2).
Clock Rates	DL11-A, B	Crystal oscillator at one of two standard frequencies; 844.8 kHz or 1.152 MHz.
		External clock can be connected to two switch positions (9 and 10).
	DL11-C, D, or E	Crystal oscillator at one of four standard frequencies: 1.03296 MHz, 844.8 kHz, 1.152 MHz, or 4.608 MHz.
		External clock can be connected to two switch positions (9 and 10).
		Special crystal frequencies can be ordered from DEC.
Bit Transfer Order	All	Low-order bit (LSB) first.
Parity	DL11-C, D, or E	Computed on incoming data or inserted on outgoing data dependent on type of parity (odd or even) used.
		Parity may be odd, even, or unused.
Size	All	Consists of a single quad module (M7800) that occupies ¼ of a DD11-A or one of two controller slots in a KA11, KC11, or other PDP-11 processor system unit.

(continued on next page)

Table 2-4 (Cont)
DL11 Operating Specifications

Specification	Options	Description
Cables	DL11-A, C	One 7008360 cable (2-ft length) with Berg connector for mating to M7800 and female Mate-N-Lok for mating to device.
	DL11-B, D, or E	One BC05C-25 (25-ft length) cable with Berg connector for mating to M7800 and male Cinch connector for mating to device.
Power Required	DL11-A, C	1.8A at +5V 150 mA at -15V
	DL11-B, D, or E	1.8A at +5V 150 mA at -15V 50 mA at level between +9V and +15V

CHAPTER 3
INSTALLATION AND CONFIGURATION

3.1 INTRODUCTION

This chapter describes the physical components which constitute each of the five DL11 Asynchronous Line Interface options, and methods of mounting and connecting the DL11 to other devices. The chapter is divided into three major parts: configuration, installation, and cabling.

3.2 CONFIGURATION

Each DL11 option basically consists of an M7800 quad module, either a standard crystal (one of four available from DEC) or a special crystal (also available from DEC), and associated cabling. The specific components of each of the five options are listed in Table 3-1.

Although general operation of the M7800 is similar for each option, specific functions of this module differ from option to option. This is due partially to the jumpers which may be added to or removed from the logic to enable or disable certain signals, partially due to the specific cable used with the module which may or may not connect all lines between the module and the external device, and partially due to the addition or deletion of certain discrete components on the module so that the M7800 can perform the logic functions required for a particular option. In effect, there are five different versions of the M7800.

The crystals covered in Table 3-1 are the standard crystals available from DEC. The customer may substitute a special crystal, if desired. However, the resultant baud rate must remain within the range of 40 baud to 10K baud.

3.3 INSTALLATION

The DL11 interface can be mounted in either a small peripheral controller slot in the PDP-11 processor or in one of the four slots in a DD11-A Peripheral Mounting Panel as shown in Figure 3-1. Note that the DL11 can be mounted in any one of the four slots and up to four DL11 interfaces can be mounted in a single system unit.

A DL11 interface can also be mounted in one of the four slots of a BB11 system unit, provided that slot has been wired as a DD11-A or equivalent. Once the M7800 module has been installed, the appropriate cable must be connected as described in Paragraph 3.4.

Table 3-1
Option Configurations

Option	Module	Cables	Crystal	Notes
DL11-A	M7800	7008360 (2-1/4 ft)	#1 or #3 only	Cable mates to Model 33 or Model 35 Teletype.
DL11-B	M7800	BC05C-25 (25 ft)	#1 or #3 only	
DL11-C	M7800	7008360 (2-1/4 ft)	#1, #2, #3, or #4	
DL11-D	M7800	BC05C-25 (25 ft)	#1, #2, #3, or #4	Model 37 Teletype, VT05, or VT06 null modem required.
DL11-E	M7800	BC05C-25 (25 ft)	#1, #2, #3, or #4	Cable mates to Bell 103 or 202 modem.

NOTES: 1. Crystal frequencies are: #1 = 844.8 kHz
#2 = 1.03296 MHz
#3 = 1.152 MHz
#4 = 4.608 MHz

2. Although each option uses an M7800 module, the signals supplied on the specific module depend on the option used.

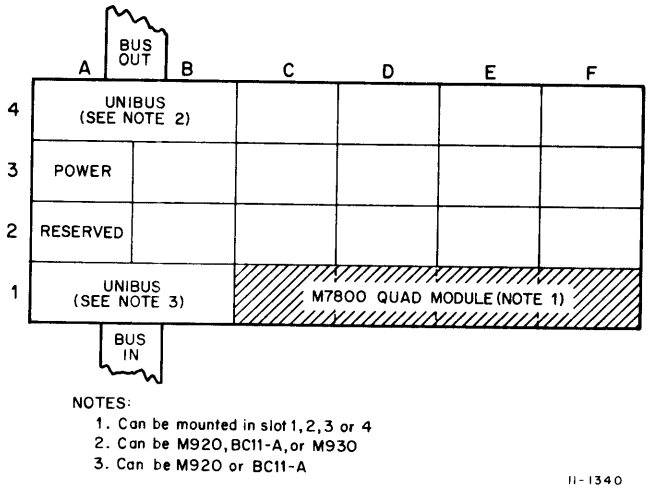


Figure 3-1 DL11 (M7800 module) Mounted in DD11-A

3.3.1 Power Connections

Power connections to the DL11 interface are provided by the associated PDP-11 system via the power supply in the BA11 mounting box. When power is applied to the PDP-11 system, the DL11 receives power also. These power connections are described in detail in the *PDP-11 Peripherals Handbook.*

When using the DL11-B, D, or E option, a positive voltage is required between 9 and 15V to operate the EIA drivers. For PDP-11/15 and PDP-11/20 systems with an H720 Power Supply, a G8000 module must be installed to provide this voltage. This module uses a filter network to convert the full-wave rectified +8V/rms signal to a positive dc voltage. Installation of the G8000 module is performed as follows:

1. Install the G8000 module into slot A02 of the DD11-A.
2. Connect a wire between A03V2 and A02V2.
3. Connect a wire between A02N2 and C*XX*U1 where *XX* is the slot location of the M7800 module.

3.3.2 Address and Priority Assignments

The DL11 interface is addressed through the address selection logic and its interrupt vector determined by the interrupt control logic. Each specific DL11 interface has a unique address and vector, both determined by jumpers on the M7800 module. Figure 3-2 shows the locations of the jumpers on the M7800 module. The priority level is determined by the priority plug on the module and is normally a BR4 level for options DL11-A through DL11-D (refer to Engineering Drawing C-IA-5408776-0-0). However, this priority level may be changed, if desired, by changing the priority plug.

3.3.3 Installation Testing

Installation testing is performed by running the appropriate diagnostic program after the DL11 interface has been completely installed. This program is contained on the diagnostic tape supplied with the interface. Instructions for running the diagnostic are included with the program tape.

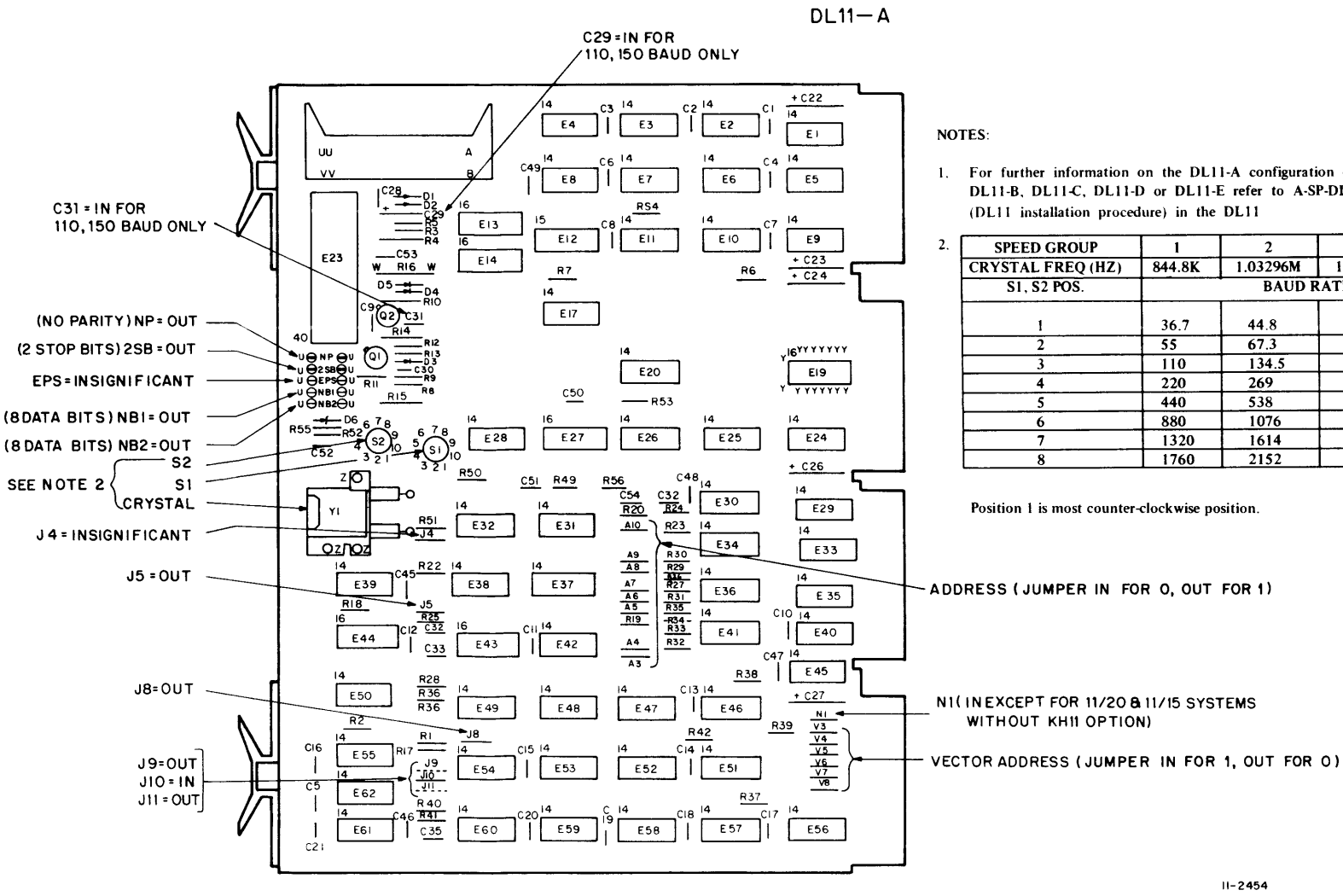
Depending on the option used, the following diagnostic programs are supplied:

a.	DL11-A option	KL11 Teletype Tests	MAINDEC-11-DZKLA
b.	DL11-B option	VT05 Tests	MAINDEC-11-DZVTB
c.	DL11-C option	Off-Line Test	MAINDEC-11-DZDLA
d.	DL11-D option	Off-Line Test	MAINDEC-11-DZDLA
e.	DL11-E option	Off-Line Test	MAINDEC-11-DZDLA
		On-Line Test	MAINDEC-11-DZDLB

3.4 CABLING

Figure 3-3 illustrates the method of connecting cables between the various DL11 options and associated external devices.

Table 3-2 lists the signal names and associated pins on the Berg connector mounted on the M7800 module. This table also lists the associated signals supplied on the 7008360 and BC05C cables.



NOTES:

1. For further information on the DL11-A configuration or the installation of DL11-B, DL11-C, DL11-D or DL11-E refer to A-SP-DL11-0-2 (DL11 installation procedure) in the DL11

2.

SPEED GROUP	1	2	3	4
CRYSTAL FREQ (HZ)	844.8K	1.03296M	1.152M	4.608M
S1, S2 POS.	BAUD RATE			
1	36.7	44.8	50	200
2	55	67.3	75	300
3	110	134.5	150	600
4	220	269	300	1200
5	440	538	600	2400
6	880	1076	1200	4800
7	1320	1614	1800	7200
8	1760	2152	2400	9600

Position 1 is most counter-clockwise position.

Figure 3-2 Jumper Locations on the M7800 Module

Table 3-3 provides a quick reference of M7800 input/output signals for TTL, EIA, and 20-mA current loop devices.

Table 3-4 lists connector pin numbers and signals for the 7008360 cable.

Table 3-5 lists connector pin numbers and signals for the 7008519 cable connector which is used in conjunction with the 7008360 cable.

Table 3-6 lists connector pin numbers for the BC05C cable connectors.

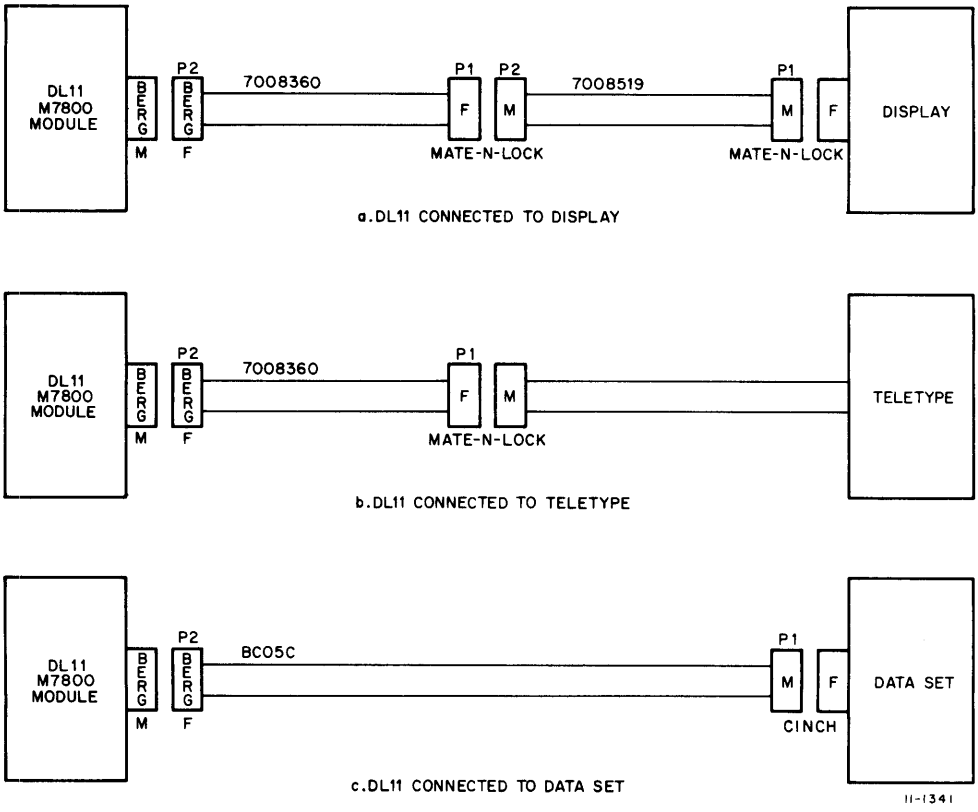


Figure 3-3 DL11 Cable Connections

Table 3-2
Pin Connections

Berg Pin	M7800 Module	BC05C Modem Cable	7008360 Cable
A	Ground	Ground	Ground
B	Ground	Ground	
C	Force Busy (EIA)	Force Busy	
D		Sec. Clear to Send	
E	Serial Input (TTL)	Interlock In	Interlock In
F	Serial Output (EIA)	Transmitted Data	
H	20 mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	Serial Input + (20 mA)		Received Data +
L		External Clock	
M	EIA Interlock	Interlock Out	
N		Serial Clock Xmit	
P		Sec. Request to Send	
R		Serial Clock Rcvr	
S	Serial Input - (20 mA)		Received Data -
T	Clear to Send (EIA)	Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W		- Power	
X	Ring (EIA)	Ring	
Y		+ Power	
Z		Data Set Ready	
AA	Serial Output + (20 mA)		Transmitted Data +
BB	Carrier (EIA)	Carrier	
CC	Clock Input (TTL)		
DD	Data Terminal Rdy (EIA)	Data Terminal Ready	
EE	Reader Run - (20 mA)		Reader Run -
FF	Secondary Xmit (EIA)	202 Sec. Xmit	
HH	Berg Clock Enb		
JJ	Secondary Rec (EIA)	202 Sec. Rcvr	
KK	Serial Output - (20 mA)		Transmitted Data -
LL		EIA Sec. Xmit	
MM		Signal Quality	
NN		EIA Sec. Rcvr	
PP	Reader Run + (20 mA)		Reader Run +
RR		Signal Rate	
SS	Serial Output (TTL)		
TT	+5V		
UU	Ground	Ground	Ground
VV	Ground	Ground	Ground

Table 3-3
Input/Output Signals

Type	Signals		Pin No.
TTL Signals	INPUT:	Serial Data	E
		Clock	CC
		Clock Enable	HH
	OUTPUT:	Serial Data	SS
20-mA Current Loop Signals	INPUT:	+ Serial Data	K
		- Serial Data	S
	OUTPUT:	+ Serial Data	AA
		- Serial Data	KK
		+ Reader Run } (RDR ENB)	PP
		- Reader Run } (RDR ENB)	EE
EIA Signals	INPUT:	Serial Data	J
		Clear to Send	T
		Ring	X
		Carrier	BB
		Secondary Receive	JJ
	OUTPUT:	Serial Data	F
		Force Busy	C
		Request to Send	V
		Data Terminal Ready	DD
		Secondary Transmit	FF

Table 3-4
7008360 Connections

Twisted Pair	Color	Mate-N-Lok Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Black/Red	Black	2	KK	- Transmitted Data
	Red	3	S	- Received Data
Black/White	Black	4	EE	- Reader Run
	White	5	AA	+ Transmitted Data
Black/Green	Black	6	PP	+ Reader Run
	Green	7	K	+ Received Data
			black E	Interlock In
			black H	Interlock Out

NOTES: 1. Connector on ASR Teletype uses all pins (2–7).
2. Connector on KSR Teletype does not use pins 4 or 6 (Reader Run - and +).

Table 3-5
7008519 Connections

7008360 Mate-N-Lok Connector P1	Mate-N-Lok Connector P2 (To 7008360)	Color	Mate-N-Lok Connector P1 (To Device)	Signal
2	2	Black	2	- Transmitted Data
3	3	Red	3	- Received Data
4				
5	5	White	5	+ Transmitted Data
6				
7	7	Green	7	+ Received Data

Table 3-6
BC05C Connections

Color	Cinch Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Blue/White	1	A	Ground
		VV	Ground
White/Blue	2	F	Transmitted Data
Orange/White	3	J	Received Data
White/Orange	4 ← black	V	Request to Send
Green/White	5	T	Clear to Send
White/Green	6	Z	Data Set Ready
Brown/White	7	B	Ground
		UU	Ground
White/Brown	8	BB	Carrier
Slate/White	9	Y	+ Power
White/Slate	10	W	- Power
Blue/Red	11	FF	202 Secondary Transmit
Red/Blue	12	JJ	202 Secondary Receive
Orange/Red	13	D	Secondary Clear to Send
Slate/Red	14	LL	EIA Secondary Transmit
Slate/Green	15	N	Serial Clock Transmit
Red/Brown	16	NN	EIA Secondary Receive
Slate	17	R	Serial Clock Receive
Red/Slate	18	U	Unassigned
Blue/Black	19	P	Secondary Request to Send
Black/Blue	20	DD	Data Terminal Ready
Orange/Black	21	MM	Signal Quality
Black/Orange	22	X	Ring
Green/Black	23	RR	Signal Rate
Brown/Red	24	L	External Clock
Red/Orange	25	C	Force Busy
		red→ E	Interlock In
		M	Interlock Out

CHAPTER 4
PROGRAMMING INFORMATION

4.1 SCOPE

This chapter presents general programming information for software control of the DL11 Asynchronous Line Interface. Although a few typical program examples are included, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook*, DEC-11-XPTSA-A-D.

This chapter of the manual is divided into five major portions: device registers, interrupts, timing considerations, programming notes, programming examples.

4.2 DEVICE REGISTERS

All software control of the DL11 Asynchronous Line Interface is performed by means of four device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction referring to their addresses. Address assignments can be changed by altering jumpers on the address selection logic to correspond to any address within the range of 774000 to 777777. However, register addresses for the various DL11 options normally fall within the range of 775610 to 776177 or 776500 to 776677. For the remainder of this discussion, it is assumed that a DL11-A option is being used as a Teletype (console) control. The description is valid for all options; only the specific device register address changes.

The four device registers and associated DL11-A addresses are listed in Table 4-1.

Table 4-1
Standard DL11 Register Assignments

Register	Mnemonic	Address*
Receiver Status Register	RCSR	777560
Receiver Buffer Register	RBUF	777562
Transmitter Status Register	XCSR	777564
Transmitter Buffer Register	XBUF	777566

*These addresses are only for the DL11-A or DL11-B option when used as a Teletype (console) control. For other address assignments for these registers, refer to Table 5-2.

Figures 4-1 through 4-4 show the bit assignments for the four device registers. Note that the number of bits within a specific register may vary, dependent on the particular option being used. However, when a specific bit is used in all options, it always retains the same bit position in the register.

The unused and load-only bits are always read as 0s. Loading unused or read-only bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or the occurrence of a power-up or power-down condition of the processor power supply.

In the following descriptions, "transmitter" refers to those registers and bits involved in accepting a parallel character from the Unibus for serial transmission to the external device; "receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the Unibus.

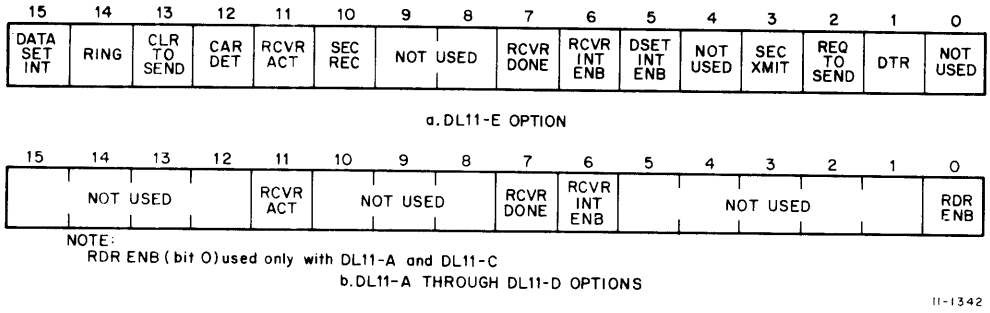
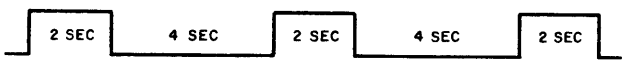


Figure 4-1 Receiver Status Register (RCSR) – Bit Assignments

Bit	Name	Option	Meaning and Operation
15	DATASET INT (Dataset Interrupt)	DL11-E only	This bit initiates an interrupt sequence provided the DATASET INT ENB bit (05) is also set. This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state; i.e., on a 0 to 1 or 1 to 0 transition of any one of these bits. It is also set when RING changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.
14	RING	DL11-E only	When set, indicates that a RINGING signal is being received from the dataset. Note that the RINGING signal is not a level but an EIA control signal with the cycle time as shown below:  Read-only bit.

Bit	Name	Option	Meaning and Operation
13	CLR TO SEND (Clear to Send)	DL11-E only	The state of this bit is dependent on the state of the CLEAR TO SEND signal from the dataset. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition. Read-only bit.
12	CAR DET (Carrier Detect)	DL11-E only	This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition. Read-only bit.
11	RCVR ACT (Receiver Active)	All	When set, this bit indicates that the DL11 interface receiver is active. The bit is set at the center of the START bit which is the beginning of the input serial data from the device and is cleared by the leading edge of RCVR DONE. Read-only bit; cleared by INIT or by RCVR DONE (bit 07).
10	SEC REC (Secondary Receive or Supervisory Received Data)	DL11-E only	This bit provides a receive capability for the reverse channel of a remote station. A space (+6V) is read as a 1. (A transmit capability is provided by bit 03.) Read-only bit; cleared by INIT.
9–8	Unused	All	Not applicable.
07	RCVR DONE (Receiver Done)	All	This bit is set when an entire character has been received and is ready for transfer to the Unibus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 06) is also set. Cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 00) is set. Also cleared by INIT. Read-only bit.
06	RCVR INT ENB (Receiver Interrupt Enable)	All	When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets. Read/write bit; cleared by INIT.
05	DATASET INT ENB (Dataset Interrupt Enable)	DL11-E only	When set, allows an interrupt sequence to start when DATASET INT (bit 15) sets. Read/write bit; cleared by INIT.
04	Unused	All	Not applicable.

Bit	Name	Option	Meaning and Operation
03	SEC XMIT (Secondary Transmit or Supervisory Transmitted Data)	**DL11-E only**	This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (+6V). (A receive capability is provided by bit 10.) Read/write bit; cleared by INIT.
02	REQ TO SEND (Request to Send)	**DL11-E only**	A control lead to the dataset which is required for transmission. A jumper ties this bit to REQ TO SEND or FORCE BUSY in the dataset. Read/write bit; cleared by INIT.
01	DTR (Data Terminal Ready)	**DL11-E only**	A control lead for the dataset communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel. Read/write bit; must be cleared by the program, is *not* cleared by INIT. **NOTE** **The state of this bit is not defined after power-up.**
00	RDR ENB (Reader Enable)	**All**	When set, this bit advances the paper-tape reader in ASR Teletype units and clears the RCVR DONE bit (bit 07). This bit is cleared at the middle of a START bit which is the beginning of the serial input from an external device. Also cleared by INIT. Only the DL11-A and DL11-C options connect to the 20-mA current loop. Write-only bit.

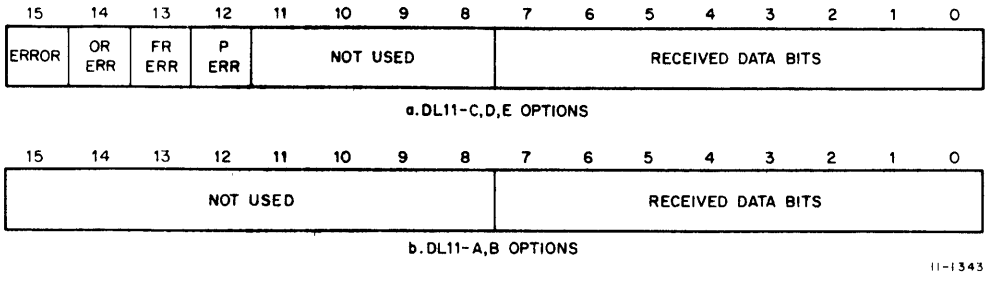


Figure 4-2 Receiver Buffer Register (RBUF) – Bit Assignments

Bit	Name	Option	Meaning and Operation
15	ERROR (Error)	DL11-C,D,E only	Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is *not* connected to the interrupt logic. Read-only bit; cleared by removing the error-producing condition.
			NOTE **Error indications remain present until the next character is received, at which time the error bits are updated. INIT does not necessarily clear the error bits.**
14	OR ERR (Overrun Error)	DL11-C,D,E only	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit. Cleared in the same manner as ERROR (bit 15).
13	FR ERR (Framing Error)	DL11-C,D,E only	When set, indicates that the character that was read had no valid STOP bit. Read-only bit. Cleared in the same manner as ERROR (bit 15).
12	P ERR (Parity Error)	DL11-C,D,E only	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit. Cleared in the same manner as ERROR (bit 15).
11–08	Unused	All	Not applicable.
07–00	RECEIVED DATA BITS	All	Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits read as 0s. Read-only bits; *not* cleared by INIT.

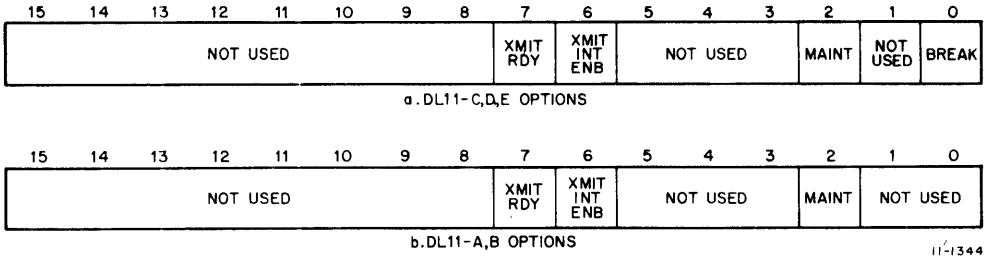


Figure 4-3 Transmitter Status Register (XCSR) – Bit Assignments

Bit	Name	Option	Meaning and Operation
15–08	Unused	All	Not applicable.
07	XMIT RDY (Transmitter Ready)	All	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set. Read-only bit. Set by INIT. Cleared by loading the transmitter buffer.
06	XMIT INT ENB (Transmitter Interrupt Enable)	All	When set, allows an interrupt sequence to start when XMIT RDY (bit 07) sets. Read/write bit; cleared by INIT.
05–03	Unused	All	Not applicable.
02	MAINT (Maintenance)	All	Used for maintenance function. When set, disables the serial line input to the receiver and connects the transmitter output to the receiver input which disconnects the external device input. It also forces the receiver to run at transmitter speed. Read/write bit; cleared by INIT.
01	Unused	All	Not applicable.
00	BREAK	DL11-C,D,E, only	When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.

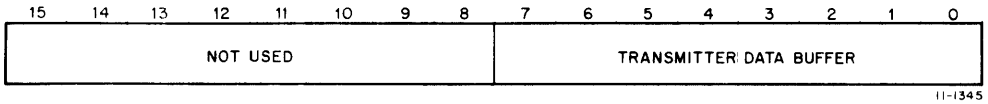


Figure 4-4 Transmitter Buffer Register (XBUF) – Bit Assignments

Bit	Name	Option	Meaning and Operation
15–08	Unused	All	Not applicable.
07–00	TRANSMITTER DATA BUFFER	All	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits. Write-only bits.

4.3 INTERRUPTS

The DL11 Interface uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing a branch to a handling routine. The DL11 has two interrupt channels: one for the receiver section and one for the transmitter section. These two channels operate independently; however, if simultaneous interrupt requests occur, the receiver has priority. In addition, the DL11-E (dataset option) receiver section handles multiple source interrupts.

A transmitter interrupt can occur only if the interrupt enable bit (XMIT INT ENB) in the transmitter status register is set. With XMIT INT ENB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver data interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. With RCVR INT ENB set, setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus. The additional interrupt request sources for the DL11-E option are discussed in the following paragraphs.

The receiver portion of the DL11-E dataset option handles multiple source interrupts. One of the receiver interrupt circuits is activated by RCVR INT ENB and RCVR DONE. The additional interrupt circuit can cause an interrupt only if the dataset interrupt enable bit (bit 05, DATASET INT ENB) in the receiver status register is set. With DATASET INT ENB set, setting the DATASET INT bit initiates an interrupt request. The DATASET INT bit can be set by one of four other bits: CAR DET, CLR TO SEND, SEC REC, or RING.

When servicing an interrupt for one condition, if a second interrupt condition develops, a unique second interrupt, as well as all subsequent interrupts, may not occur. To prevent this, either all possible interrupt conditions should be checked after servicing one condition or both interrupt enable bits (bits 05 and 06) should be cleared upon entry to the service routine for vector XX0 and then set again at the end of service.

The interrupt priority level is 4 for all options, with the receiver having a slightly higher priority than the transmitter in all cases. Note that the priority level can be changed with a priority plug.

Floating vector addresses are used for all options and are assigned by the interrupt control logic. If the DL11-A or B option is used as a console, then the vector address is 060. The vector address can be changed by jumpers in the interrupt control logic.

Any DEC programs or other software referring to the standard BR level or vector addresses must also be changed if the priority plug or vector address is changed.

4.4 TIMING CONSIDERATIONS

When programming the DL11 Asynchronous Line Interface, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter, and break generation logic are discussed in the following paragraphs.

4.4.1 Receiver

The RCVR DONE flag (bit 07 in the RCSR) sets when the Universal Asynchronous Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

4.4.2 Transmitter

The transmitter section of the UART is also double buffered. The XMIT RDY flag (bit 07 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

4.4.3 Break Generation Logic

When the BREAK bit (bit 00 in the XCSR of DL11-C, D, and E options) is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. However, because the transmitter section of the UART is double buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be null.

4.5 PROGRAM NOTES

The following notes pertain to programming the DL11 interface and contain information that may be useful to the programmer. More detailed programming information is given in the *Paper Tape Software Programming Handbook*, DEC-11-XPTSA-A-D and in the individual program listings.

a. **Character Format** – The character formats for the different DL11 options are given below. Note that when less than eight DATA bits are used, the character must be right-justified to the least significant bit. The character format pertains to both the receiver and the transmitter.

   1. *DL11-A and B Options* – A character consists of a START bit, eight DATA bits, and 1 or 2 STOP bits.

   2. *DL11-C, D, and E Options* – A character consists of a START bit, five to eight DATA bits, 1, 1.5, or 2 STOP bits and the option of PARITY (odd or even) or no parity.

b. **Maintenance Mode** – The maintenance mode is selected by setting the MAINT bit (bit 02) in the XCSR. In this mode, the interface disables the normal input to the receiver and replaces it with the output of the transmitter. The programmer can then load various bits into the transmitter and read them back from the receiver to verify proper operation of the DL11 logic circuits.

4.6 PROGRAM EXAMPLE

The following is an example of a typical program that can be used as an echo program for a Type 103 dataset. When a remote terminal dials in, this program answers the call and provides a character-by-character echo. Characters are also copied onto the console device.

```
                    000200                      .=200
000200  000167  001616          START:  JMP     BEGIN           ;JUMP TO BEGINNING OF PROGRAM

                                        ;SYMBOL DEFINITIONS

                    040000              RING=   040000          ;BIT 14 OF RCSR, RING
                    020000              CTS=    020000          ;BIT 13 OF RCSR, CLEAR TO SEND
                    000200              RDONE=  000200          ;BIT 07 OF RCSR, RECEIVER DONE
                    000002              DTR=    000002          ;BIT 01 OF RCSR, DATA TERMINAL READY
                    000200              XRDY=   000200          ;BIT 07 OF XCSR, TRANSMITTER READY

                    002000                      .=2000
002000  175610              RCSR:   175610          ;CSR OF RECEIVER
002002  175612              RBUF:   175612          ;BUF OF RECEIVER
002004  175614              XCSR:   175614          ;CSR OF TRANSMITTER
002006  175616              XBUF:   175616          ;BUF OF TRANSMITTER
002010  177564              CXCSR:  177564          ;CSR OF CONSOLE TRANSMITTER
002012  177566              CXBUF:  177566          ;BUF OF CONSOLE TRANSMITTER
002014  000000              BUFFER: 0               ;HOLDS CHARACTER RECEIVED
002016  000000              DELAY:  0               ;HOLDS DELAY COUNT, HIGH ORDER
002020  000000                      0               ;HOLDS DELAY COUNT, LOW ORDER

                                        ;BEGINNING OF ECHO PROGRAM

002022  005077  177752      BEGIN:  CLR     @RCSR           ;START BY INITIALIZING ALL BITS TO ZERO

002026  032777  040000  177744  LOOP1:  BIT     #RING,@RCSR     ;CHECK FOR INCOMING CALL
002034  001774                  BEQ     LOOP1           ;BRANCH IF PHONE IS NOT RINGING
002036  052777  000002  177734          BIS     #DTR,@RCSR      ;PHONE IS RINGING, SO ANSWER WITH DTR
002044  012767  000005  177744          MOV     #5,DELAY        ;SET UP COUNT FOR DELAY

002052  032777  020000  177720  LOOP2:  BIT     #CTS,@RCSR      ;CHECK FOR CLEAR TO SEND
002060  001007                  BNE     LOOP3           ;BRANCH IF ON
002062  162767  000001  177730          SUB     #1,DELAY+2      ;CHECK DELAY
002070  005667  177722                  SBC     DELAY           ;DECREMENT A TWO-WORD INTEGER
002074  001752                  BEQ     BEGIN           ;BRANCH IF WE HAVE WAITED TOO LONG
002076  000765                  BR      LOOP2           ;BRANCH AND CONTINUE TO WAIT FOR CTS

002100  032777  020000  177672  LOOP3:  BIT     #CTS,@RCSR      ;IS CHANNEL STILL ESTABLISHED?
002106  001745                  BEQ     BEGIN           ;BRANCH IF CTS NOT PRESENT
002110  032777  000200  177662          BIT     #RDONE,@RCSR    ;CHECK FOR RECEIVED CHARACTER
002116  001770                  BEQ     LOOP3           ;BRANCH IF NO CHARACTER RECEIVED
002120  017767  177656  177666          MOV     @RBUF,BUFFER    ;READ RECEIVED CHARACTER INTO BUFFER

002126  032777  000200  177650  LOOP4:  BIT     #XRDY,@XCSR     ;CHECK FOR TRANSMITTER READY
002134  001774                  BEQ     LOOP4           ;BRANCH IF NOT READY
002136  016777  177652  177642          MOV     BUFFER,@XBUF    ;TRANSMIT CHARACTER TO REMOTE TERMINAL

002144  032777  000200  177636  LOOP5:  BIT     #XRDY,@CXCSR    ;CHECK FOR CONSOLE TRANSMITTER READY
002152  001774                  BEQ     LOOP5           ;BRANCH IF NOT READY
002154  016777  177634  177630          MOV     BUFFER,@CXBUF   ;TRANSMIT CHARACTER TO CONSOLE
002162  000746                  BR      LOOP3           ;BRANCH AND WAIT FOR NEXT CHARACTER
```

APPENDIX A
VECTOR ADDRESSING

A.1 INTRODUCTION

Because the DL11 Asynchronous Line Interface is basically a communications device, interrupt vectors must be assigned according to the floating vector convention used for all communications devices. These vector addresses are assigned in order from 300 to 777 according to a specific method that ranks the type of devices in a particular PDP-11 System.

The first vector address (300) is assigned to the first DC11 Serial Asynchronous Line Interface in the system, the next DC11 (if used) is then assigned vector address 310, etc. The vector addresses are assigned consecutively to each unit of the second ranked device type (KL11 or DL11-A or DL11-B), then to the third ranked device (DP11), and so on in accordance with the following list:

1. DC11 Asynchronous Line Interface
2. KL11 Teletype Control (or DL11-A or DL11-B)
3. DP11 Synchronous Serial Modem Interface
4. DM11 Asynchronous Serial Line Multiplexer
5. DN11 Automatic Calling Unit
6. DM11-BB Modem Control
7. DR11-A Device Registers
8. DR11-C General Device Interface
9. DT11 Bus Switch
10. DL11-C Asynchronous Line Interface
11. DL11-D Asynchronous Line Interface
12. DL11-E Asynchronous Line Interface

If any of these devices is not included in a system, the vector address assignments move up to fill the vacancies. If a device is added to an existing system, its vector address must be inserted in the normal position and all other addresses must be moved accordingly. If this procedure is not followed, DEC software cannot test the system.

Note that the floating vectors range from addresses 300 to 777 but addresses 500 through 534 are reserved for special bus testers. In addition, address 1000 is used for the DS11 Synchronous Serial Line Multiplexer.

An address map is shown in Figure A-1 and a list of the vector addresses is given in Paragraph A.2. It should be noted that the system Teletype (KL11) is not part of the floating vector scheme and is assigned vector addresses 060 and 064. Therefore, if a DL11 is used as a control for the system Teletype console, it should be assigned addresses 060 and 064. All other DL11s would follow the floating vector conventions.

A.2 INTERRUPT VECTORS

000	RESERVED	
004	ERROR TRAP	
010	RESERVED INSTRUCTION TRAP	
014	DEBUGGING TRAP	
020	IOT TRAP	
024	POWER FAIL TRAP	
030	EMT TRAP	
034	"TRAP" TRAP	
040	SYSTEM SOFTWARE	COMMUNICATION WORDS
044	SYSTEM SOFTWARE	
050	SYSTEM SOFTWARE	
054	SYSTEM SOFTWARE	
060	TELETYPE IN	
064	TELETYPE OUT	
070	PC11 HIGH-SPEED READER	
074	PC11 HIGH-SPEED PUNCH	
100	KW11-L LINE CLOCK	
104	KW11-P PROGRAMMABLE CLOCK	
110	DR11-A (Request A)	
114	DR11-A (Request B)	
120	XY11 XY PLOTTER	
124	DR11-B	
130	AD01	
134	AFC11	
140	AA11-A,B,C,E SCOPE	
144	AA11 LIGHT PEN	
150		
154		
160		
164		
170	USER RESERVED	
174	USER RESERVED	
200	LP11 LINE PRINTER CONTROL	
204	RF11 DISK CONTROL	
210	RC11 DISK CONTROL	
214	TC11 DECTAPE CONTROL	
220	RK11 DISK CONTROL	
224	TM11 MAGTAPE CONTROL	
230	CR11 CARD READER CONTROL	
234	UDC11	
240	11/45 PIRQ	
244	FPU ERROR	
250		

(continued on next page)

254 RP11 DISK PACK CONTROL
260
264
270 USER RESERVED
274 USER RESERVED
300 ← FLOATING VECTORS START AT THIS ADDRESS
304
310
314 **NOTE**
320
324 **Floating vectors start at address 300 and are assigned**
330 **in the following order:**
334
340
344 **all DC11s, then**
350 **all KL11s,* then**
354 **all DP11s, then**
360 **all DM11s, then**
364 **all DN11s, then**
370 **all DM11-BBs, then**
374 **all DR11s, then**
400 **all DT11s, then**
404 **all DL11-Cs, then**
410 **all DL11-Ds, then**
414 **all DL11-Es**
420
424
430 ***or DL11-As or DL11-Bs**
434
440
444
450
454
460
464
470
474
500
504
510
514 SPECIAL BUS TESTERS
520
524
530
534
540
544
550
554
560
564
570
574
600 through 774 ← FLOATING VECTORS END HERE
1000 ← DS11

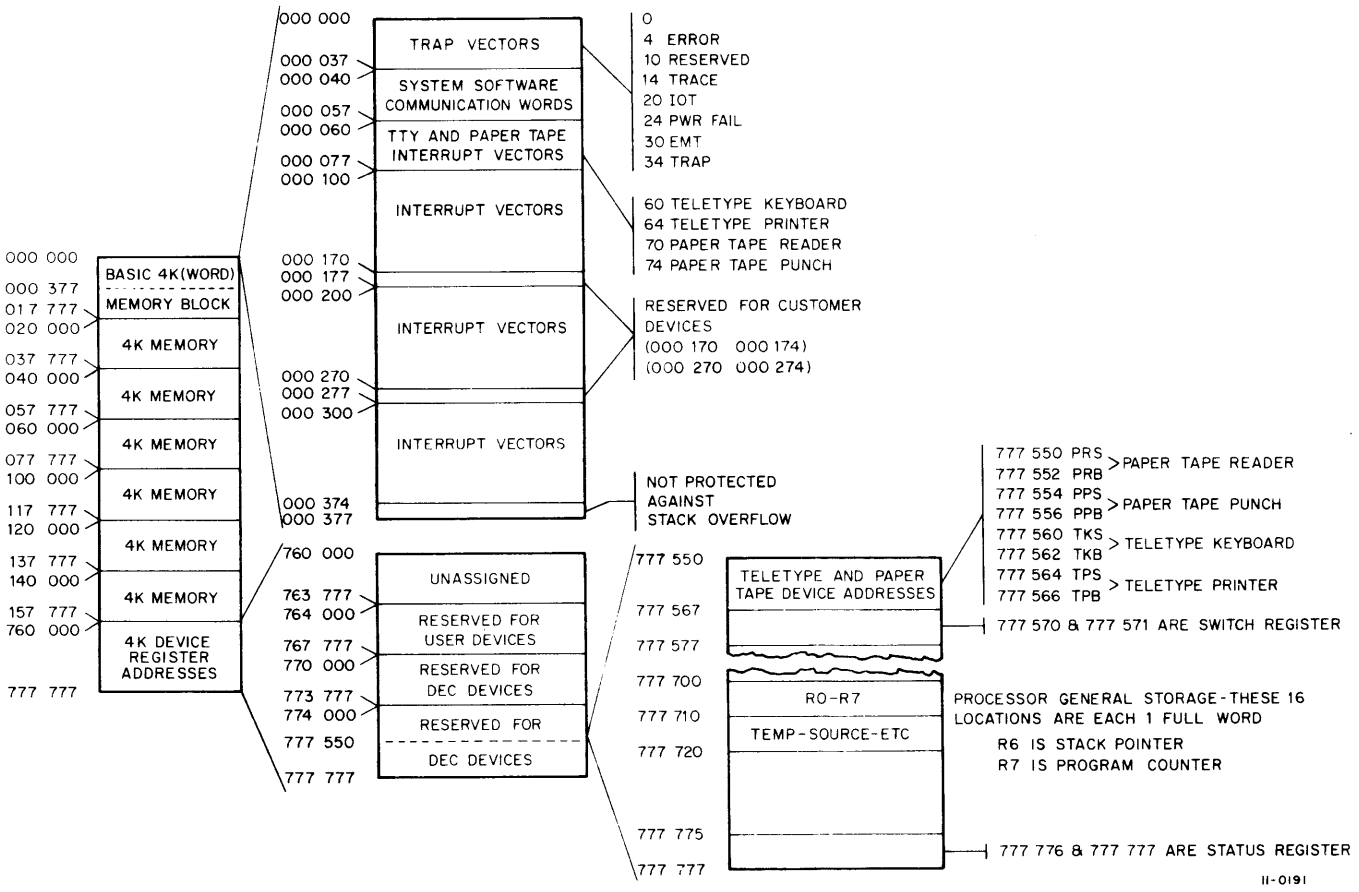


Figure A-1 Address Map

Reader's Comments

DL11 ASYNCHRONOUS LINE INTERFACE
USER'S MANUAL
EK-DL11-OP-001

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

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What features are most useful? _____

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Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

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Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT (OTTED LINE

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

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