EK-DJ11-MM-003

DJ11 asynchronous 16-line multiplexer maintenance manual

digital equipment corporation · maynard, massachusetts

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CHAPTER 1
GENERAL DESCRIPTION

1.1 SCOPE

This chapter provides a general description of the DJ11 Asynchronous 16-Line Multiplexer. Included is a definition of its purpose in a PDP-11 system, a typical system block diagram, a mechanical description of the unit, and a brief list of unit specifications of particular interest to maintenance personnel.

1.2 PURPOSE

The DJ11 Asynchronous Multiplexer provides the PDP-11 Unibus with connection to as many as sixteen serial asynchronous communication lines operating at standard rates of between 75 and 9600 baud. Character lengths used on the lines can be mixed 5-, 6-, 7-, or 8-level code, with or without either odd or even parity. Stop codes can be either 1 or 2 units, except on lines employing 5-level codes in which cases stop codes are set to 1 or 1.5 units. Line parameters are jumper selectable in four line groups with split-speed capability.

1.3 TYPICAL SYSTEM BLOCK DIAGRAM

A typical DJ11 system is shown in Figure 1-1. Note that up to 16 DJ11s can be connected to one Unibus, providing a maximum of interfacing for 256 serial communications type devices.

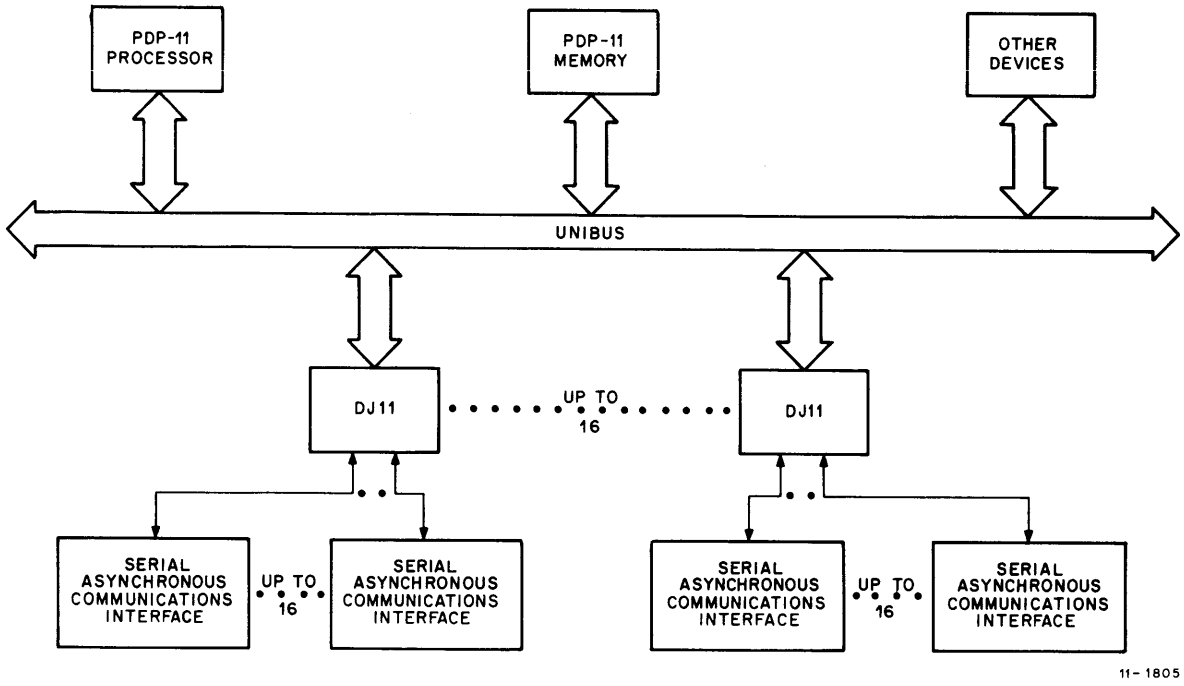


Figure 1-1 DJ11 Typical System Block Diagram

1.4 OPTIONS

Three DJ11s are provided as standard options; each option is capable of either 50- or 60-Hz operation. The options are listed in Table 1-1 and described below. For characteristics other than those listed, contact DEC Computer Special Systems.

Table 1-1
DJ11 Options

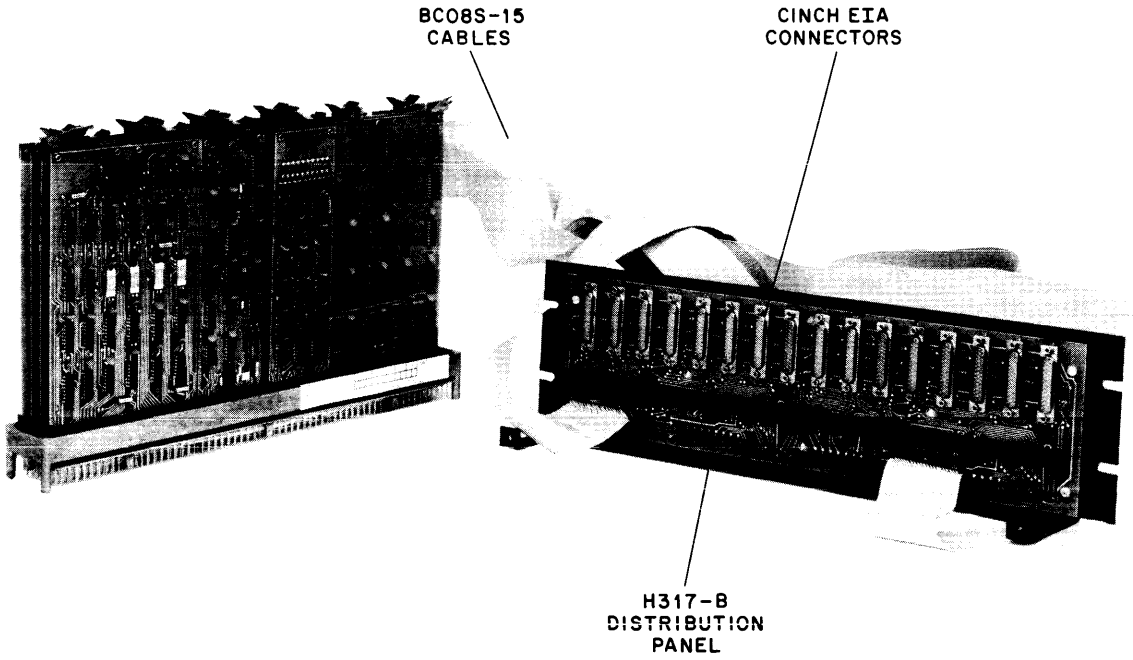
Variation	Characteristics
DJ11-AA	16 lines (data only) Input/output EIA
DJ11-AB	16 lines (data only) No level conversion
DJ11-AC	16 lines (data only) Input/output 20 mA current loop

The DJ11-AA (Figure 1-2) is a prewired system unit containing all modules to implement a 16-line data-only multiplexer. EIA level conversion is provided on the interfacing input and output lines. These lines are available on a passive distribution panel that mounts either on an H960 19-in. cabinet or to a wall. Connections to the panel are made by Cinch EIA connectors. Interconnecting cables are provided between the system unit and the distribution panel. These cables provide a positive (ON) voltage to the Data Terminal Ready and Request To Send leads of the Cinch plugs. Hardware for this option is as follows:

1 7009179 Wired Assembly System Unit
2 M7280 UART Card
1 M7279 Receive Silo Card
1 M105 Address Select
1 M7821 Interrupt Control
1 M7285 Hex Mux Control
1 M5901 EIA Level Converter Card
2 BC08S-15 Cables
1 H317-B Distribution Panel
1 M920 Unibus Connector
1 H315 Test Connector

The DJ11-AB Multiplexer is identical to the DJ11-AA except that no level conversion is provided. The system unit is provided with a TTL interface card that contains two Berg headers and the mating cables; a distribution panel is **not** provided. Also, no test connector is provided. Hardware for this option is identical to that listed for the DJ11-AA except for the following:

1 M5900 TTL Output Card
No Distribution Panel
No Test Connector



NOTE:
Test connector not shown.

Figure 1-2 DJ11-AA Asynchronous 16-Line Multiplexer

The DJ11-AC (Figure 1-3) is identical to the DJ11-AA except that 20 mA current loop operation is provided. The passive distribution panel is a different model that provides screw-type connectors. No test connector is provided. Hardware is identical to the DJ11-AA except for the following:

1 M5902 TTY Level Converter Card
1 H317-A Distribution Panel
No Test Connector

1.5 MODULE UTILIZATION

The multiplexer is contained in a single system unit. Module utilization is shown in Figure 1-4. Note that only functional names are assigned in those locations where the module designation varies with the option. Note also that a hex card is used; because of this, the unit cannot be utilized with the older PDP-11/20 BA11 boxes. It must be installed in the newer PDP-11/40 or PDP-11/45 extender box.

1.6 SPECIFICATIONS

Environmental

Operating Temperature Range	+40 to +120°F
Operating Humidity Range (without condensation)	10 to 95% Relative

Power Requirements

	DJ11-AA	DJ11-AB	DJ11-AC
-15 Vdc	0.250A	0.250A	1.0A
+5 Vdc	4.7A	4.7A	5.3A
+15 Vdc	0.250A	N.A.	N.A.

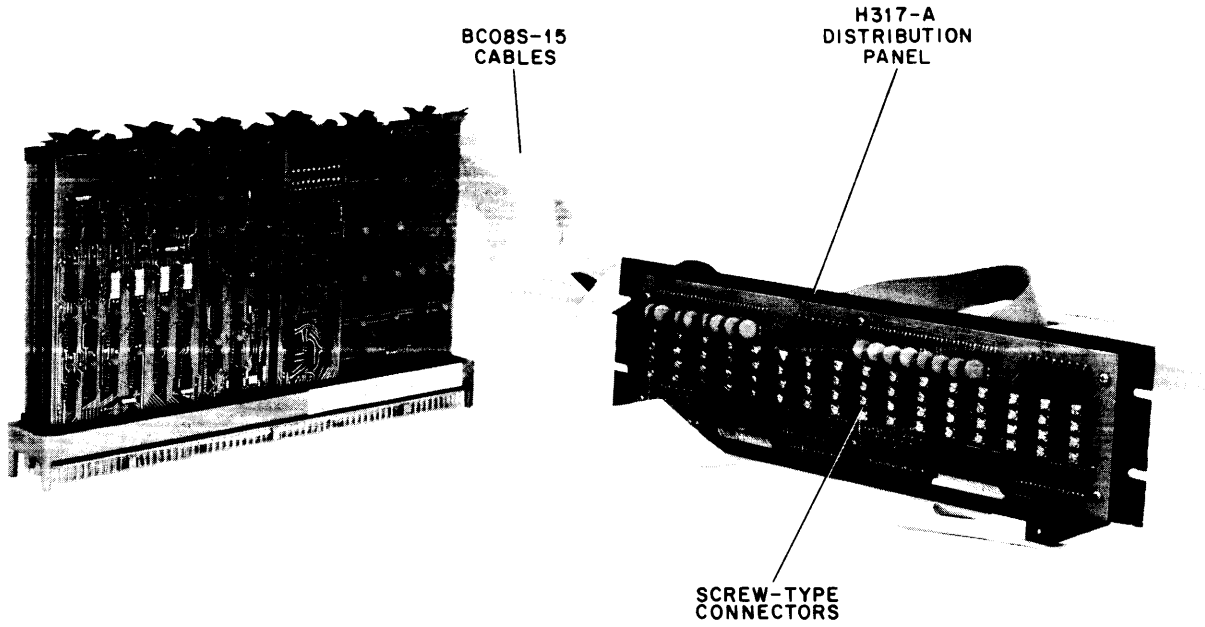


Figure 1-3 DJ11-AC Asynchronous 16-Line Multiplexer

	A	B	C	D	E	F
4	M920 UNIBUS CONN		M7280 UART CARD # 1			
3	LEVEL CONVERTER & OUT (M5900,5901,5902)		M7280 UART CARD # 2			
2	M7285 HEX MUX CONTROL					
1	UNIBUS		M105 ADDRESS SELECT	M7821 INTERRUPT CONTROL	M7279 SILO	RECEIVE CARD

11-1806

Figure 1-4 DJ11 Module Utilization

Power Consumption 35W

Performance

Receivers

Conversion Serial to Parallel

Levels 5 + 1 Start and 1 or 1.5 Stop
6,7,8 + 1 Start and 1 or 2 Stop
Jumperable in 4-line groups

Parity Odd, even, or none; jumperable in 4-line groups

Data Rate Independent of transmitter (split-speed)
Jumperable in 4-line groups

BAUD	TOL
50	±0.1%
75	±0.1%
110	±0.1%
134.5	±0.24–0.00%
150	±0.1%
300	±0.1%
600	±0.1%
1200	±0.1%
1800	±0.1%
2400	±0.1%
4800	±0.1%
9600	±0.1%

Allowable Input Distortion per Bit 42% Mark to Space

Input Speed Tolerance ±5% with at least 1.5 Stop marks

Breaks Detection provided

Transmitters

Conversion Parallel to Serial

Levels 5 + 1 Start and 1 or 1.5 Stop
6,7,8 + 1 Start and 1 or 2 Stop
Jumperable in 4-line groups

Parity Odd, even, or none; jumperable in 4-line groups

Data Rate Independent of receiver (split-speed);
Jumperable in 4-line groups;
Same rates and tolerances as listed for receiver

Allowable Output Distortion 2.5% Mark to Space + Gross Start to Stop as measured at TTL output

Breaks Allowable on any line

Input Requirements/Option

Item	DJ11-AA	DJ11-AB	DJ11-AC	
			Active Receiver	Passive Receiver
Mark	-15 to -3V	0.8V @ 5 mA	20 to 30 mA @ 200Ω (loop+load)	+20 to +30 mA @ 220Ω
Space	+3 to +15V	2.0V @ 40 μA	0 to 5 mA	+5 to -30 mA @ 220Ω

Input Requirements/Option

Item	DJ11-AA	DJ11-AB	DJ11-AC	
			Active Receiver	Passive Receiver
Impedance	3 to 7 kΩ	0.9 to 1.2 kΩ	440Ω	220Ω
Open Ckt Voltg.	NMT 3V	NMT 6V	NMT 16V	NMT 60 μs
Max. Distance	50 ft up to 9600 baud if C_{cable} < 2500 pF	25 ft any speed		
Rise & Fall Times	NMT 50 μs	NMT 50 μs	NMT 50 μs	NMT 50 μs
Speed Range	75 – 9.6 kbaud	75 – 9.6 kbaud	Low NMT 300 baud Med NMT 2400 baud Hi NMT 9.6 kbaud	Low NMT 300 baud Med NMT 2400 baud Hi NMT 9.6 kbaud

Output Requirements/Option

Item	DJ11-AA	DJ11-AB	DJ11-AC
Mark	-15 to -6V	0.4V @ 10 mA	20 mA @ NMT 200Ω (loop+load)
Space	+6 to +15V	2.4V @ 1 mA	NMT 1 mA
Impedance	NMT 300Ω	100 to 125Ω	NMT 800Ω
Open Ckt Voltg.	NMT 30V	NMT 6V	22V
Slew Rate	30V/μs	60V/μs max	60V/μs max
Max. Distance	50 ft up to 9600 baud if C_{cable} < 2500 pF	25 ft up to 9600 baud if C_{cable} < 500 pF	

Bus Load 1 unit load to Unibus (1 receiver and 2 drivers)

Max Configuration 16 DJ11s/Unibus

Single Device Throughput

(Theoretical)	43,840 char/sec*
(Processor Limited 11/05, 11/15 11/20)	20,000 char/sec**
(Processor Limited 11/45)	80,000 char/sec

Interrupts Available

CHARACTER DONE INT – Occurs each time a character appears at output of FI/FO buffer. Enabled or disabled from the bus. Can be jumpered to interrupt **only** when there are 5, 9, or 17 characters in the silo.

TRANSMIT INT – Occurs when transmit scanner finds a UART buffer empty condition and the transmitter control register bit for that line is set. Enabled or disabled from the bus.

FI/FO OVERRUN INT – Occurs when FI/FO is full and receiver scanner stops attempting input to FI/FO. This interrupt vector is same as RCV vector but is separately enabled.

Interrupt Level Normally 5 as supplied. Can be modified by priority plug.

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* Computed on the following:

$$\frac{\text{9600 bits/second/line/direction}}{\text{7 bits/character}}$$

**Based on 50 μs processor time per character.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures necessary to install the DJ11 Asynchronous 16-Line Multiplexer. It is not intended to supersede the installation requirements given in the Customer's Site Plan. Included is a brief checkout procedure to ensure proper operation once installation is complete. Detailed test and checkout procedures are found in Chapter 5 of this manual.

CAUTION

OEMs should not attempt installation until DEC has been notified and a Field Service representative is present. Failure to do so can void equipment warranty.

2.2 CONFIGURATION DIFFERENCES

Installation procedures can vary, dependent upon the particular system configuration. For example, the DJ11 can be supplied with or without a distribution panel. There are two possible distribution panels supplied which differ mechanically and electrically. There are variations in level converter cards and in the type of cable connectors used.

A listing of the basic option designations, with functional differences, is given in Table 2-1. For a complete list of differences in nomenclature, refer to Paragraph 1.6, Specifications.

Table 2-1
DJ11 Option Designations

Nomenclature	Functional Differences
DJ11-AA	EIA level conversion
DJ11-AB	No level conversion
DJ11-AC	20 mA current loop conversion

2.3 UNPACKING AND INSPECTION

The DJ11 is packaged in accordance with commercial packaging practices. Remove the packaging material and check the equipment against the shipping list. Any damage or shortages must be reported immediately to the shipper and the DEC representative. Check all wiring and inspect the modules for obvious damage.

2.4 INSTALLATION

Because the DJ11 is capable of operating at many different baud rates and signal parameters, it is necessary to obtain the customer's preferences when installing the unit. Obtaining this information prior to installation will simplify installation.

The DJ11 allows the user to have independent speeds and parameters in 4-line groups. For example, the first four lines may operate at 110 baud, 8 bits per character, with no parity; while the second four lines might operate at 300 baud, 6 level, with odd parity, etc. These parameters are selectable by means of switches and solderable jumpers that are part of the M7285 Hex Control Board.

The parameters to be selected by the switches are given in Table 2-2, with the settings to achieve a given condition. These switches are illustrated in Figure 2-1. Note that the switches are called out as E80 and E82 on the Hex control board and that the switches are numbered 1 through 10, similar to the pins on an IC. If all switches are open (dot on switch up away from the board), all lines are set for 8 level, no parity, and 2 stop bits. The switch settings must be made four times for the four groups of lines, and must be set in 4-line groups for all additional DJ11s used in the installation.

Table 2-2
Parameter Switch Settings

Function	Switch	Parameter/Settings			
Character Length		**8 bit/char**	**7 bit/char**	**6 bit/char**	**5 bit/char**
	NB1 NB2	open open	closed open	open closed	closed closed
Parity		**No Parity**	**Odd Parity**	**Even Parity**	
	NP POE	open open	closed closed	closed open	
Stop Code		1 Stop	2 Stop*		
	NSB	closed	open		

Note: An open switch setting is indicated when the white dot on the rocker arm is in the up position, away from the board.

* For 5-level code, this setting provides 1.5 unit Stop.

Speed selection is set by an array of split lugs mounted on the M7285 board (Figure 2-1). These split lugs should be wired with no. 30 insulated solid wire.

The eight split lugs on the left are arranged in two groups of four, the upper group for transmit speed and the lower group for receive speed. The line groups are as shown and are not necessarily in order. The lug numbers are marked on the board adjacent to the lugs.

The eleven split lugs on the right provide the selectable speeds. The lug numbers are as they appear on the board. Figure 2-1 shows the speeds for each lug. To set speeds, one of the split lugs on the right-hand side must be wired to one or more split lugs on the left-hand side. Figure 2-1 illustrates the wiring for the examples given in this chapter. Actual wiring must be determined from the tables in this chapter.

CAUTION

Speed selection must be arranged in descending order, with line 15 set to the highest speed desired and line 0 set to the lowest.

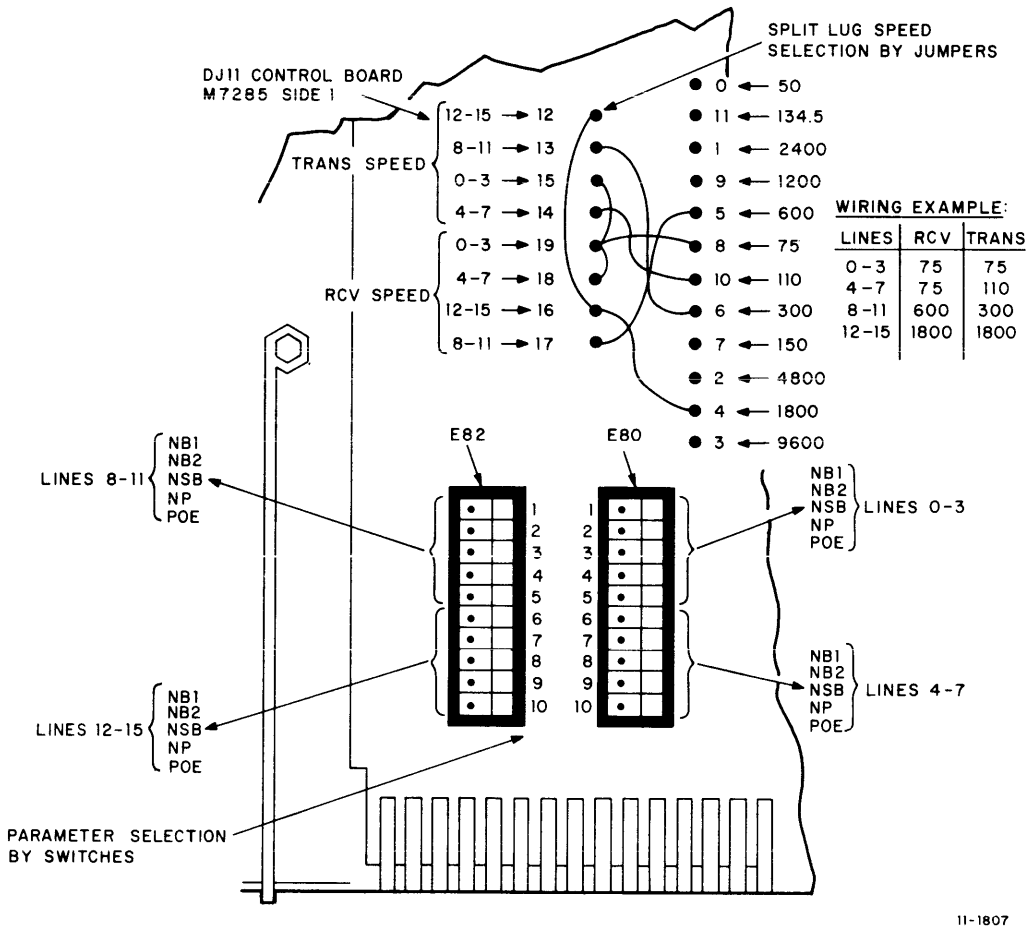


Figure 2-1 M7285 Board Showing Jumper and Switch Selection

The example in the figure is wired for the following requirements:

Lines	Receive Speed	Transmit Speed
0–3	75	75
4–7	75	110
8–11	600	300
12–15	1800	1800

Table 2-3
Sample Customer's Preference Chart

Group	Level	Parity	Stop Bits	Speed Selection		
				XTR	RCV	Split
Lines 0–3	8	No	1	75	75	No
Lines 4–7	6	Odd	2	75	110	Yes
Lines 8–11	5	Even	1.5	600	300	Yes
Lines 12–15	7	No	2	1800	1800	No

Note: Have customer prepare one of these for each DJ11 (up to sixteen) in the system. See Appendix D for blank chart.

Table 2-3 is given as an *example* of a Customer's Preference Chart, which should be prepared prior to installation and filled out by the customer. From this, an installation chart based on the information in Table 2-1 and Figure 2-1 can be prepared before installation begins. A *sample* installation chart, Table 2-4, is based on the examples used in this chapter.

Table 2-4
Sample Installation Chart

Installation Chart				
Lines	**Switch**	**Pin No.**	**Position**	**Jumper Pins**
0–3	E80	1	Open	8 to 19
				19 to 15
		2	Open	
		3	Open	
		4	Open	
		5	Closed	
4–7	E80	6	Open	8 to 18
				14 to 10
		7	Closed	
		8	Closed	
		9	Closed	
		10	Open	
8–11	E82	1	Closed	5 to 17
				6 to 13
		2	Closed	
		3	Closed	
		4	Open	
		5	Closed	
12–15	E82	6	Closed	4 to 16
				16 to 12
		7	Open	
		8	Open	
		9	Open	
		10	Open	

Note: Entries based on examples given in this chapter.

2.4.1 Installation Procedure

To install any DJ11, proceed as follows:

1. Mount logic system unit into suitable customer supplied box (either PDP-11/40, PDP-11/45, or PDP-11/35) and attach power to spade lugs located on front (Figure 2-2).

NOTE
Do not install connections to distribution panel at this time.

PIN	SIGNAL	COLOR
1	DCLO	VIO
2	ACLO	YEL
3	-15VDC	BLU
4	GND	BLK
9	+5VDC	RED
7	LTC	BRN
8	+15VDC	GRY

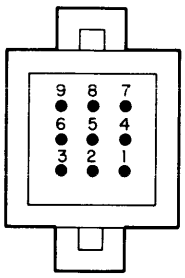


Figure 2-2 Power Harness Color Code

2. Install all modules per Figure 1-2.

NOTE

If DJ11 is last device on the bus, the terminator module (M930) plugs into slots A4–B4.

3. Apply power to the unit, load and run the logic diagnostic (MAINDEC-11-DZDJA-A-PB) on the equipment *as it is received* from the manufacturer. Note that no modifications as to line parameters should as yet be made, except address and vector jumpers as required. Run the diagnostic for a single pass.

NOTE

All shipments from the factory are set for 8-level, no parity, 2 stop bits, and single speed. Use these parameters in the diagnostic opening dialogue. (Standard configuration is all switches off.)

4. If a failure occurs in this initial run, refer to the diagnostic for type of error and location of probable fault. Note in the Installation Report that the unit did not function as shipped. (Refer to Chapter 5.)

5. Set all parameters per the installation chart (Table 2-4) prepared from the customer's preference chart (Table 2-3).

6. When all parameters have been set, rerun the DJ11 logic test; enter the new parameter information for the opening dialogue. Run the test for two passes or five minutes, whichever occurs first.

7. When installing the DJ11-AB proceed to step 10. When installing either the DJ11-AA or DJ11-AC, mount the H317 Distribution Panel at the location specified by the customer. This can be in a cabinet or along a wall. It must be located at a point where incoming lines can be attached, and it must be within the constraint of the 15 ft BC08S Cable.

8. Connect the BC08S-15 Cable between the output card in the logic (location 3-A/B on backplane) and the H317 Panel. On the H317A, interconnect J1 with J1 of the M5902 module, and J2 with J2 of that same module. On the H317B, interconnect J17 with J2 of the M5901 module, and J20 with J1 of that same module.

CAUTION

Cables are neither marked nor keyed and if improperly connected can damage equipment. On the H317, the rib side of the cable must be away from the board. On the M5901 or M5902, the smooth side of the cable must be away from the board (Figure 2-3).

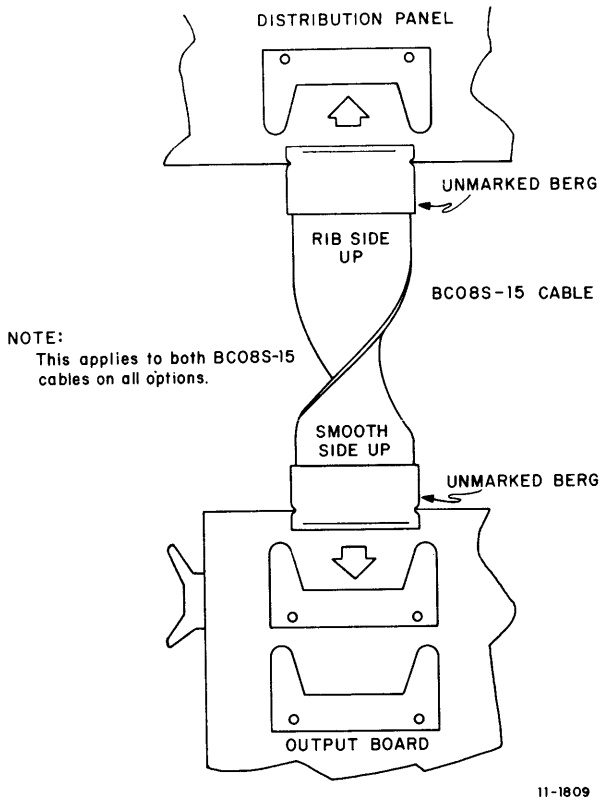
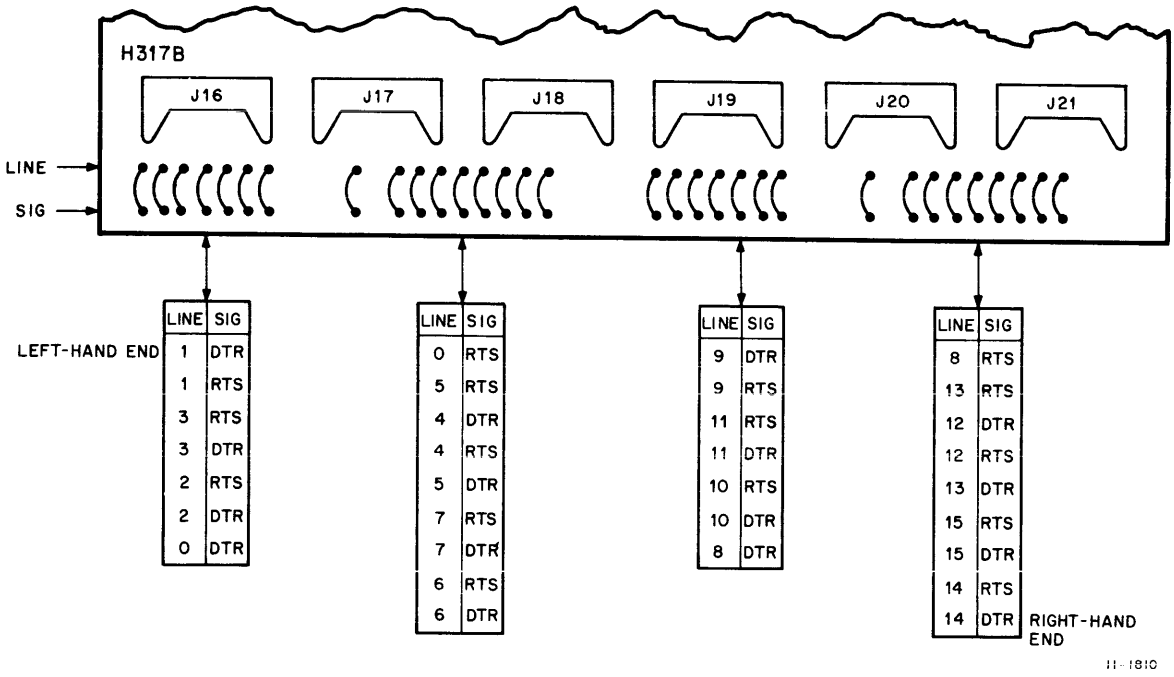


Figure 2-3 BC08S-15 Polarization

9. There are jumpers on the distribution panel that must be set. Refer to Figures 2-4 and 2-5 for particulars. These jumpers have to do with RTS and DTR strapping on the H317B Distribution Panel, and the Cinch connector strapping on that panel.

10. When installing the DJ11-AC, the H317A Distribution Panel must be strapped active or passive according to the various line requirements. In addition, the proper filtering must be set for the particular line speeds used. This strapping is shown in Figure 2-6. Refer to D-CS-5410262-0-1 for capacitor values.

11. When installing the DJ11-AB, the output lines can connect to either the DC08-CS Telegraph Interface, a DM11 Distribution Panel (7008483-0-0), or to some special interface. In these cases, refer to pertinent documentation for those equipments, to the interconnection diagrams in the print set, and to the 1975 *Peripherals Handbook,* Page 4-124.



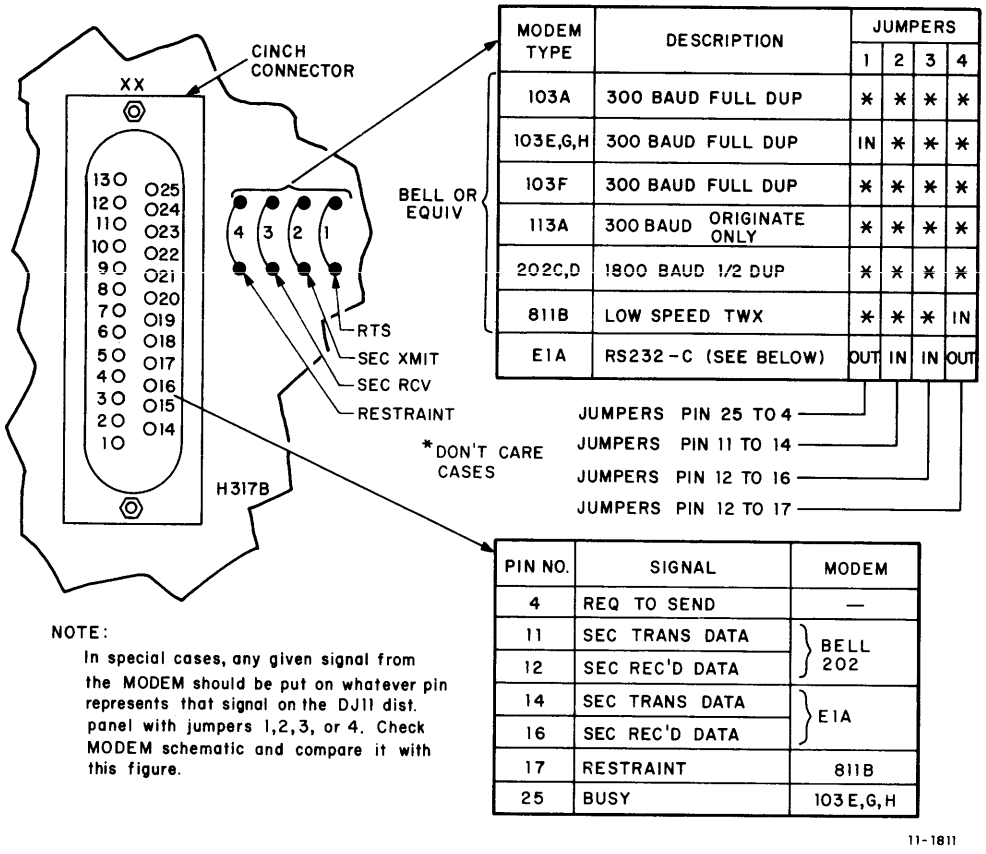
LINE	SIG
1	DTR
1	RTS
3	RTS
3	DTR
2	RTS
2	DTR
0	DTR

LINE	SIG
0	RTS
5	RTS
4	DTR
4	RTS
5	DTR
7	RTS
7	DTR
6	RTS
6	DTR

LINE	SIG
9	DTR
9	RTS
11	RTS
11	DTR
10	RTS
10	DTR
8	DTR

LINE	SIG
8	RTS
13	RTS
12	DTR
12	RTS
13	DTR
15	RTS
15	DTR
14	RTS
14	DTR

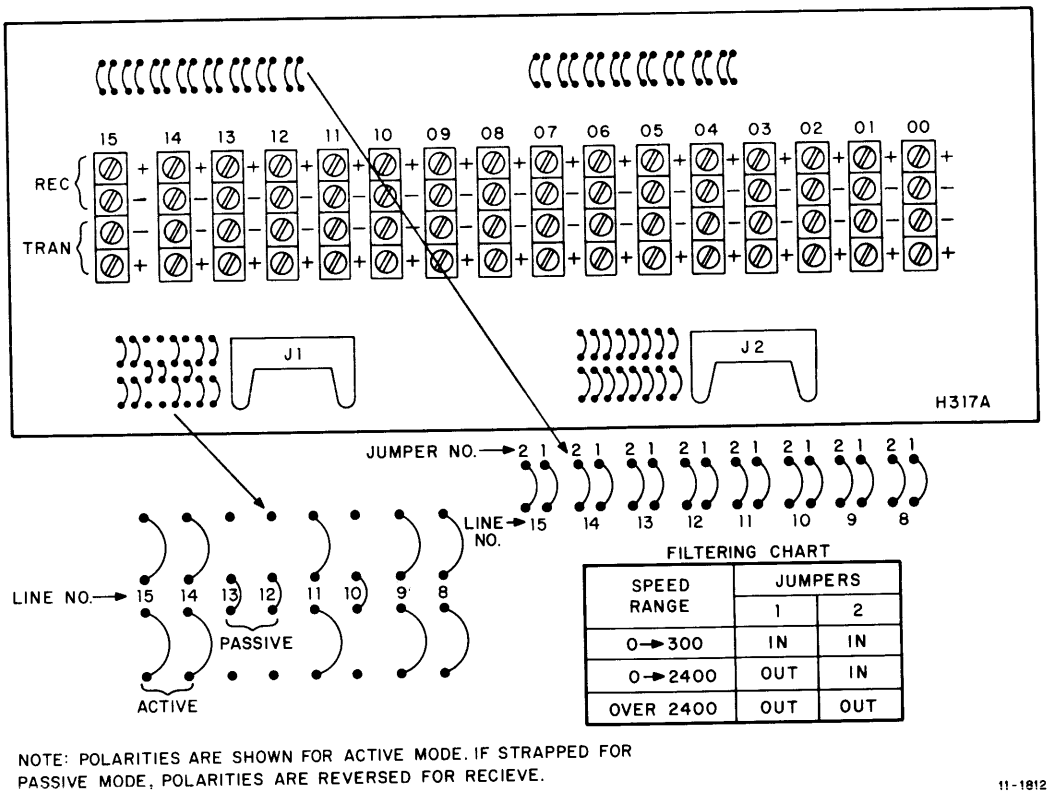
Figure 2-4 Strapping on H317B Distribution Panel



MODEM TYPE	DESCRIPTION	JUMPERS 1	2	3	4
103A	300 BAUD FULL DUP	*	*	*	*
103E,G,H	300 BAUD FULL DUP	IN	*	*	*
103F	300 BAUD FULL DUP	*	*	*	*
113A	300 BAUD ORIGINATE ONLY	*	*	*	*
202C,D	1800 BAUD 1/2 DUP	*	*	*	*
811B	LOW SPEED TWX	*	*	*	IN
E1A	RS232-C (SEE BELOW)	OUT	IN	IN	OUT

PIN NO.	SIGNAL	MODEM
4	REQ TO SEND	—
11	SEC TRANS DATA	BELL 202
12	SEC REC'D DATA	BELL 202
14	SEC TRANS DATA	E1A
16	SEC REC'D DATA	E1A
17	RESTRAINT	811B
25	BUSY	103E,G,H

Figure 2-5 Cinch Connector Strapping on H317B Distribution Panel



NOTE: Polarities are shown for Active mode. If strapped for Passive mode, polarities are reversed for receive.

Figure 2-6 Filtering and Mode Strapping on H317A Distribution Panel

2.4.2 Setting Character Done Interrupt Constant

The CHARACTER DONE INT occurs each time a character appears at the output of the FI/FO buffer (or silo). This interrupt is enabled or disabled from the bus. As described in more detail in Paragraph 4.4.12, this is a result of a comparator signal in the silo control circuit shown on drawing D-BS-M7279, sheet D11-3 (CHARACTER AVAILABLE).

These signals, against which the Silo Status Register is compared, are actually shown on the lower left-hand side of drawing M7285, sheet D2-9, where jumpers W1, W2, and W3 apply ground to signals G REG (04:02). When all three jumpers are installed, the interrupt occurs on each character loaded in the silo. When cut, a discrete number of characters must be loaded before the interrupt will occur. The cutable jumpers and associated character delays are as follows:

Signal	Jumper	Number of Characters
G REG 02	W1	5
G REG 03	W2	9
G REG 04	W3	17

By cutting any one, that many characters will be loaded before CHARACTER AVAILABLE is generated. By cutting all three, the sum of all possibilities, or 31 characters, will be loaded before the interrupt is generated on the 32nd character loaded (FI/FO half full).

This preference must be solicited from the customer and the appropriate jumpers removed (Figure 2-7).

NOTE

The diagnostic requires that this delay be set for *one* character. When running the diagnostic, these jumpers must be replaced temporarily.

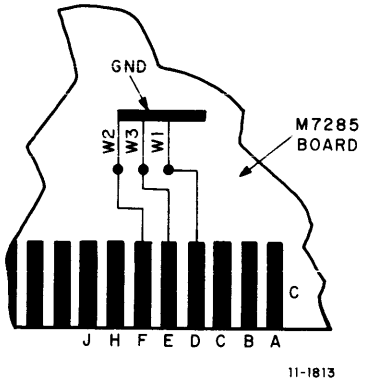


Figure 2-7 CHARACTER DONE INT Jumpers

CHAPTER 3
PROGRAMMING

3.1 SCOPE

This chapter is intended to provide a basis for DJ11 programming. It does not contain detailed software information. This data is contained in the pertinent software specifications and documentation for this equipment. Included is a description of the addressable registers with their formats illustrated, together with a description of the addresses assigned to these registers and vector information.

3.2 ADDRESSABLE REGISTERS

The DJ11 contains five addressable registers:

a. Control Status Register (CSR) 76xxx0

b. Receive Buffer Register (RBUF) 76xxx2

c. Transmit Control Register (TCR) 76xxx4

d. Transmit Buffer Register (TBUF) 76xxx6

e. Break Control Status Register (BCSR) 76xxx4

The addresses assigned to the DJ11 reside in the floating address space of the PDP-11. The DJ11 addresses are assigned contiguously before the DH11 address in the floating address space.

This floating address space is from 760010_8 to 764000_8. Each DJ11 requires increments of $+10_8$ octal locations. The unit uses two interrupt vectors, one each for transmit and receive. The CHARACTER DONE INT is at xx0; TRANSMITTER INT is at xx4. The DJ11 vectors are assigned after the DH11 vectors.

3.2.1 Control Status Register (CSR) 76xxx0

The Control Status Register is a 16-bit register that maintains the status of various control functions in the device. By their setting or clearing, these bits exert control functions on the device and cause interrupts to be generated. This register format is illustrated in Figure 3-1 and described in Table 3-1.

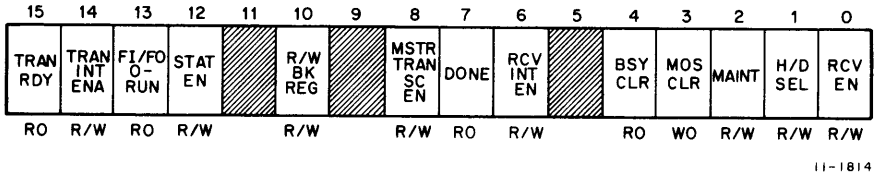


Figure 3-1 Control Status Register Bit Assignments

Table 3-1
Control Status Register Bit Assignments

Bit	Name	Function
15	Transmit Ready (TRAN RDY)	Read only bit. Set by the hardware when transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. This bit clears when TBUF is loaded, or when TCR bit for line pointed to by scan is cleared, or by reset. When cleared, this bit enables transmit clock if MSTR TRAN SC EN (bit 8) is set. When loading a character into TBUF, ready will clear, but if another line needs service, flag will reappear in less than 1.3 μs from completion of load TBUF bus cycle.
14	Transmit Interrupt Enable (TRAN INT EN)	Read/write bit, cleared by reset. Must be set for transmit ready to cause an interrupt.
13	FI/FO Overrun (FI/FO ORUN)	Read only bit. Set by hardware when FI/FO buffer is full and the RCV scanner attempts to place a character in the FI/FO buffer. Cleared on a read of the receive buffer. Note that the receive scanner does not halt at this line number, but continues to scan other lines.
12	Status Enable (STATUS EN)	Read/write bit, cleared by the hardware. Must be set for FI/FO ORUN to cause an interrupt.
11		Not used.
10	Read/Write Break Register (R/W BK REG)	Read/write bit, cleared by reset. When set, causes a read or write command issued to address 76xxx4 to access the Break Register instead of the TCR. When clear, addressing 76xxx4 accesses the TCR.
9		Not used.
8	Master Transmit Scan Enable (MSTR TRAN SC EN)	Read/write bit, cleared by reset. Must be set by program. When set, enables the transmitter clock to run. When clear, TRAN RDY (bit 15) is inhibited from setting.
7	Done (DONE)	Read only bit. Set by the hardware and cleared by a read of the RBUF. Sets when character appears at the output of the FI/FO buffer. Clears only if silo is empty after the read. Will always toggle low and come back up if FI/FO buffer has another character. In this event it stays low a maximum of 1 μs. Causes an interrupt if bit 6 is set.
6	Receiver Interrupt Enable (RCV INT EN)	Read/write bit cleared by reset. Must be set for DONE to cause an interrupt.
5		Not used.

Table 3-1 (Cont)
Control Status Register Bit Assignments

Bit	Name	Function
4	Busy Clear (BSY CLR)	Read only bit. Set when the 2 μs MOS CLR pulse is in process.
3	MOS Clear (MOS CLR)	Write only bit. When set produces a 2 μs clear pulse to silo and UARTs but does not affect any other registers. Should be written to a one only with RCV EN clear.
2	Maintenance (MAINT)	Read/write bit, cleared by reset. When set, loops all transmitter lines into corresponding receivers. In addition, forces transmitter speed of each group into the receiver clock for each group. As such, any split-speed groups are forced to run at transmitter speeds.
1	Half Duplex Select (H/D SEL)	Read/write bit, cleared by reset. When set, forces all lines to operate in half duplex mode by disabling receivers of lines that are currently transmitting. Refer to Paragraph 4.4.3.
0	Receive Enable (RCV EN)	Read/write bit, cleared by reset. When clear, prevents receiver from depositing characters in the FI/FO buffer and inhibits scan of the receiver.

3.2.2 Receive Buffer Register (RBUF) 76xxx2

This is a 16-bit read only register that contains the received character at the output of the FI/FO buffer. A read of the register causes the data to disappear and the next character stored in the FI/FO buffer to appear at the output. As each character is read, the register is updated with the next character. When the silo is empty, bit 15 reads back as a 0. This register format is illustrated in Figure 3-2 and described in Table 3-2.

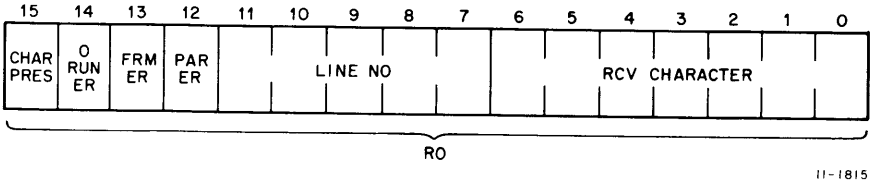


Figure 3-2 Receive Buffer Register Bit Assignments

3.2.3 Transmit Control Register (TCR) 76xxx4 (if CSR10 clear)

This is a 16-bit register that contains a control bit for each channel or line. Any bit, when set, will stop the scan if TBMT for that line is set, and will cause an interrupt to be generated if MSTR INT EN is set. Restart of the clock occurs when the TBUF is loaded with a character or if the TCR bit for the line on which the clock is stopped is cleared. TCR bits must be cleared only when the scanner is not running, i.e., when RDY is set or when MSTR TRAN SC EN (CSR bit 8) is clear. Bits are read/write; the register is cleared by reset. Line 15 has the highest priority and line 0 has the lowest. The format for this register is shown in Figure 3-3.

Table 3-2
Receive Buffer Register Bit Assignments

Bit	Name	Function
15	Character Present (CHAR PRES)	Read only bit. Set to 1 when a character is present at the output of the silo. Cleared when silo is empty. Note that the last character is never emptied from the silo even if this bit *is* cleared.
14	Overrun Error Indicator (ORUN ERR)	Read only bit. Set if character had not been removed from UART buffer before next character was received on that line. Indicates a character was lost on this line.
13	Framing Error Indicator (FRM ERR)	Read only bit. Set if character did not have valid stop bit.
12	Parity Error Indication (PAR ERR)	Read only bit. Set if parity error occurred for this character.
11:8	Line Number (LINE NO.)	Read only bits. Set by program. Indicate the line number of this received character.
7:0	Received Character (RCV CHARACTER)	Read only bits. Contain the character just received, right-justified.

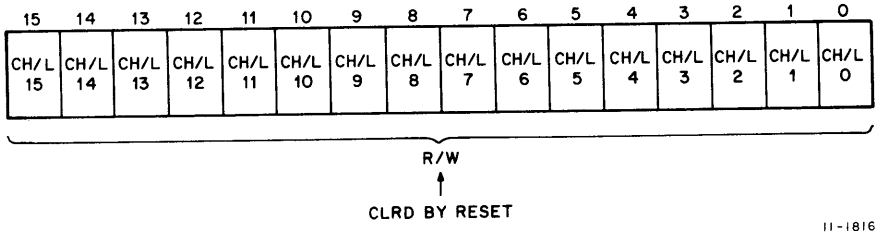


Figure 3-3 Transmit Control Register Bit Assignments

3.2.4 Transmit Buffer Register (TBUF) 76xxx6

This is a 16-bit register used to load characters into the multiplexer for transmission. The low byte is write only. Characters to be transmitted are written in the low byte. Bits 11:8 contain a 4-bit transmitter channel number. These bits are read only, but only if the transmitter scan clock is stopped by TRAN RDY (CSR bit 15) being set. These bits indicate the line into which the character is to be loaded. This register is illustrated in Figure 3-4.

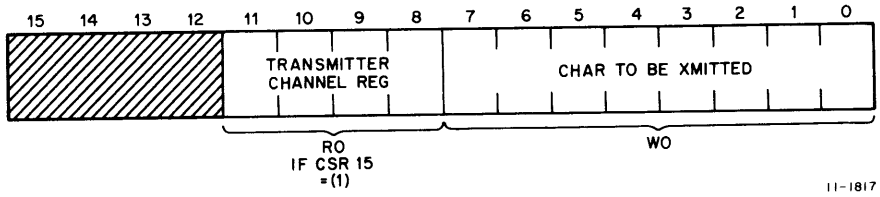


Figure 3-4 Transmit Buffer Register Bit Assignments

3.2.5 Break Control Status Register (BCSR) 76xxx4 (if CSR 10 set)

This is a 16-bit register containing a control bit for each line. Setting a bit will force a space on that line's output causing a break condition. This condition prevails until that bit is cleared by the processor. Break timing must be done by the software using the clock interrupts. All bits are read/write and the register is cleared by reset. This register is illustrated in Figure 3-5.

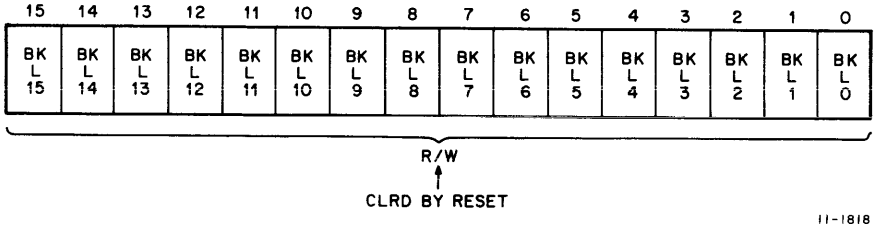


Figure 3-5 Break Control Status Register Bit Assignments

CHAPTER 4
DETAILED DESCRIPTION

4.1 SCOPE

This chapter provides a detailed description of the DJ11 Asynchronous Multiplexer. The discussions in this chapter are supported by a complete set of engineering drawings contained in a companion volume entitled *DJ11 Asynchronous Multiplexer Engineering Drawings.*

4.2 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

The DJ11, shown in Figure 4-1, comprises twelve basic functional blocks: Selection Logic, Interrupt Logic, Internal Register Logic (RBUF, CSR, TCR, BCSR, and TBUF), Universal Asynchronous Receiver/Transmitter (UART), Transmitter Control Logic, Receiver Control Logic, Clock Logic, Maintenance Mode Logic, Bus Drivers and Receivers, Break Generation Logic, Level Conversion, a First In/First Out Buffer, and a Unibus Transceiver. As shown in the figure, a common level conversion board (when used) applies 16 communication line interfaces to 16 individual UARTs which, by selection, feed a common set of logic for the data transfer to the Unibus.

The selection logic determines if the DJ11 multiplexer has been selected, which line has been selected, and what type of operation (transmit or receive) is to be performed. It permits selection of one of four internal registers and determines if the register is to perform an input or output function.

The interrupt logic permits the multiplexer to gain bus control and perform a program interrupt. Either the receiver or transmitter can issue an interrupt request. The priority level of a bus request (BR) can be changed by the user. Communication line priority is fixed and is arbitrated within the DJ11 logic in ascending order by line number.

Five internal registers, addressable by the program, provide data transfer, command and control, and status monitoring functions for the multiplexer. Transmitter control logic provides necessary input control signals from the UARTs when they are used to convert parallel data from the bus to serial data required by the external lines. Receiver control logic provides necessary input control signals from the UARTs when they are used to convert serial data to the parallel data required for transmission to the Unibus. The buffer registers are used to double buffer the data to and from the Unibus. The break generation logic permits the transmission of a continuous "break" on any of the 16 lines and maintains a status of those lines.

The UARTs perform the necessary serial-to-parallel or parallel-to-serial data conversion, supplying control and error detecting bits. There is a separate UART for each line. They are selectable from within the DJ11.

The First In/First Out Buffer (FI/FO or silo), provides a sequential accumulation of up to 64 words for transmission to the Unibus. Each word contains not only the data but also the line number on which it was received, error bits, and an indication of whether or not that character is valid. Loading is at the top, and readout to the bus is from the bottom; each character moves down to the output as a character is removed.

Clock logic determines the clock frequency and, therefore, the baud rates for the transmitter and receiver sections of the UARTs. Thirteen baud rates are derived from a single crystal and distributed to the various UARTs. The frequencies distributed are hard-wired in 4-line groups, settable at installation time by switches and jumpers.

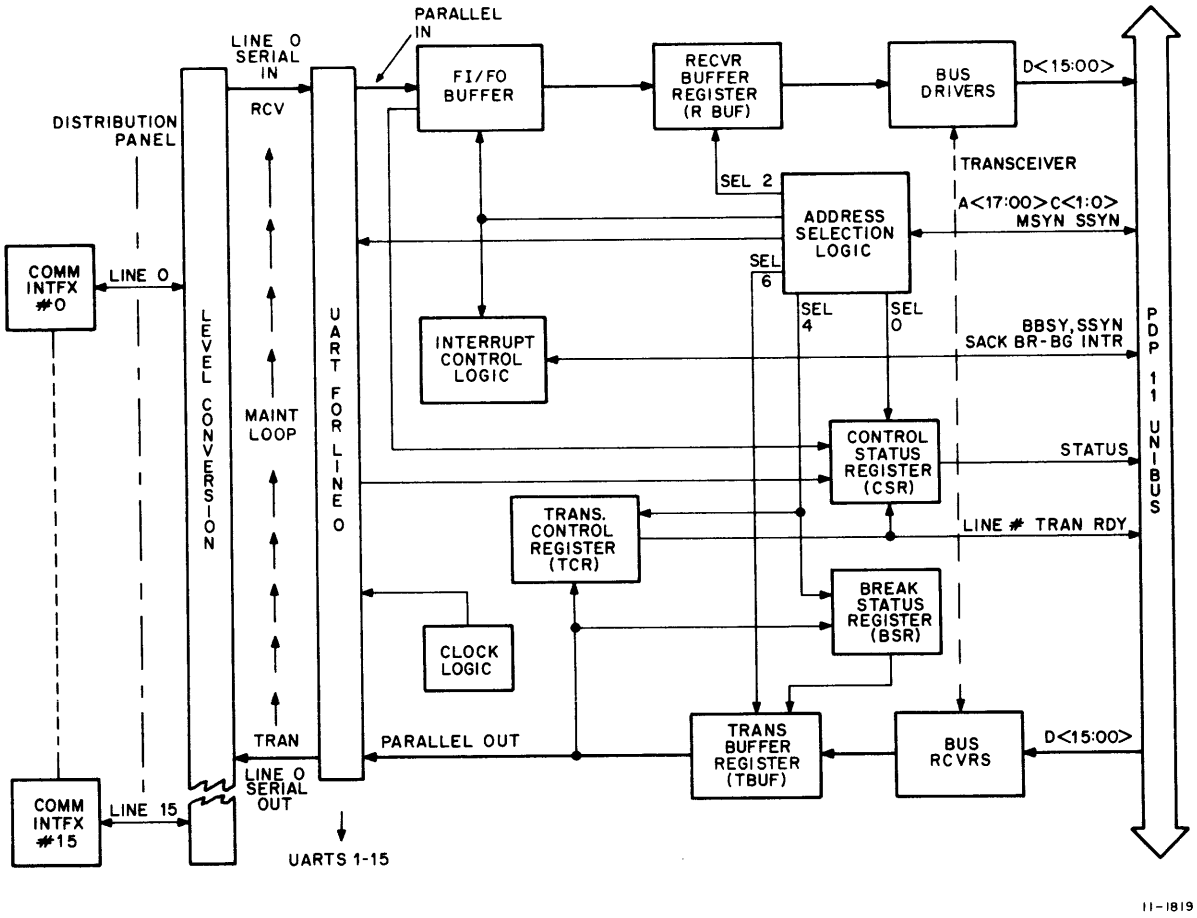


Figure 4-1 DJ11 Functional Block Diagram

Maintenance mode logic performs a closed loop test of the DJ11 control logic by tying the serial output of the transmitter into the receiver input and forcing the receiver clock to be the same frequency as the transmitter clock.

The bus drivers and receivers are part of the Unibus transceiver logic that interfaces the Unibus to the DJ11 buffer registers. The level conversion logic comprises one of three different arrangements in which the levels are converted for use with EIA levels, a 20 mA current loop environment, or straight TTL output conditions (no conversion).

Finally, jumper arrangements are provided on the distribution panels to adapt the DJ11 to various line conditions. By jumpering, active or passive operation can be implemented, response characteristics can be modified, and current limiting resistors can be added.

4.3 DETAILED BLOCK DIAGRAM DISCUSSIONS

4.3.1 Receiver Section

The DJ11 receiver section contains a separate UART for each of the 16 lines. The UART provides serial assembly of the characters, parity error checking, break detection, and overrun detection. The UART is double buffered, allowing a full character time to remove the received character to the hardware buffer. A complete description of the UART is given in DEC Specification 19-10459. The UART uses a 16x clock that provides a 42 percent distortion margin on incoming characters.

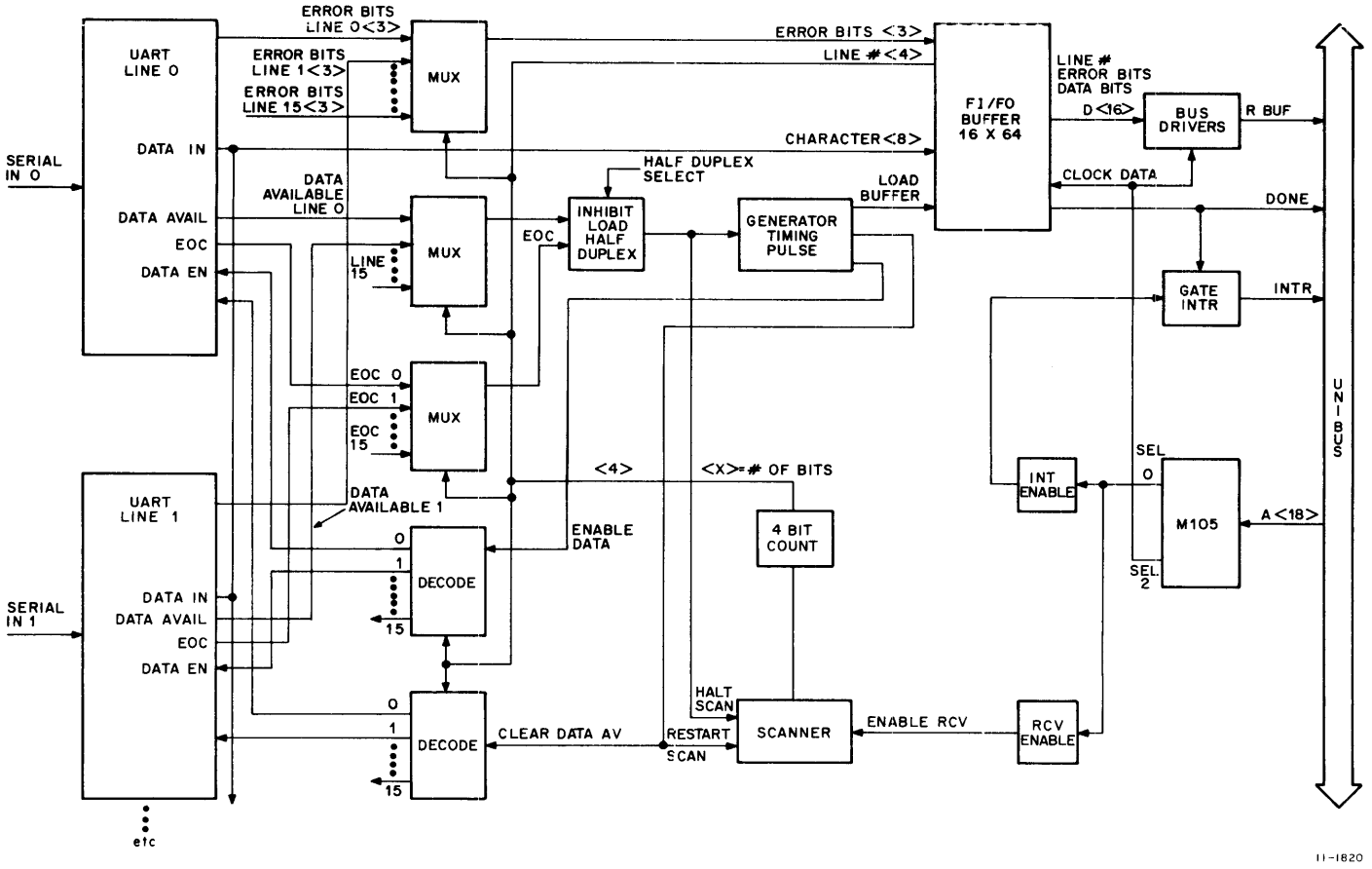


Figure 4-2 Receiver Detailed Block Diagram

Figure 4-2 is a detailed block diagram of the DJ11 receiver section. The UART is scanned by a receiver scanner that runs at a nominal 1 mHz. This scanner sequentially checks for a Data Available flag. When a flag is found, the scanner stops and the character is automatically stored in a 16 bit X 64 word FI/FO buffer.

If space is available in this buffer, the character is written into it. The character is then automatically propagated down to the first available open slot where it remains until a character is removed from the output side. As each character is removed, remaining characters propagate toward the output.

The format of the FI/FO is shown in Figure 4-3. Data bits are stored in the low byte or first 8 bits, the channel number is stored in the low 4 bits of the upper byte, with bits 14:12 holding the status bits for parity, overrun, and framing errors. Bit 15 is used as a Valid Entry Present bit.

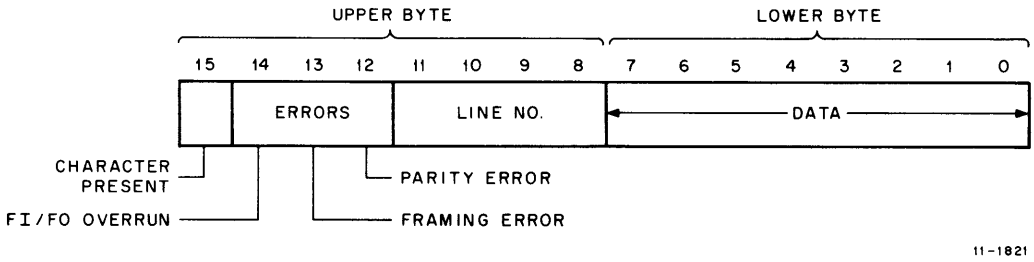


Figure 4-3 FI/FO Format

Once any character reaches the output of the buffer, a CHARACTER DONE INT occurs (normal jumpering), and the computer must service the interrupt and read the buffer to obtain the character. As the character is read, the FI/FO buffer output is incremented, causing the contents to propagate down, thus providing the next character stored in the buffer.

The software services the character Done flag on either an interrupt or flag checking basis. In either case, characters are serviced out of the FI/FO buffer; as each character is read from the buffer, the next character present is made available at the output.

The service routine should process all characters in the FI/FO to avoid the overhead involved in entering and leaving the service routine. In the block diagram of Figure 4-2, note that the scanner state is not capable of being altered or read by the program. The program deals only with the output of the FI/FO buffer.

The multiplexer has a half duplex capability. By setting a bit in the CSR, the receivers of any lines that are currently transmitting are disabled by inhibiting the deposit of the assembled characters into the silo. This is done by means of the EOC signal from the UARTs.

4.3.2 Transmitter Section

The transmitter utilizes UARTs for parallel-to-serial conversion of each line. A detailed block diagram of this section is given in Figure 4-4. A single 16-bit TCR is used to enable transmitters on a per line basis. Setting the bit for a particular line causes the "pseudo-scanner" to stop at this line if TBMT (Transmit Buffer Empty) is set and sets the TRAN RDY bit. If the TRAN INT EN bit is set, an interrupt is generated. Note that if all TCR bits are clear, the TRAN RDY bit will be clear. This is a departure from conventional single line unit ready flags.

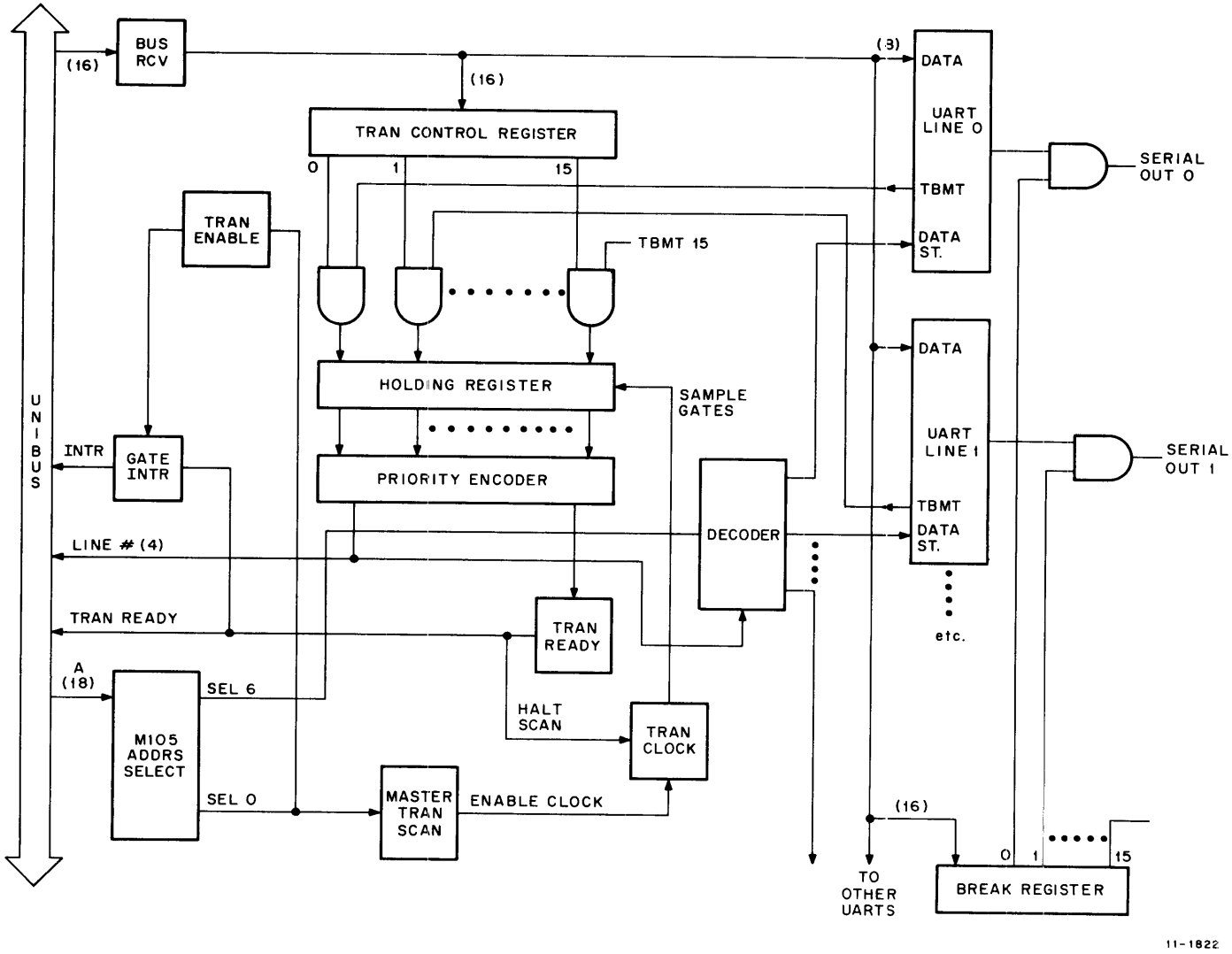


Figure 4-4 Transmitter Detailed Block Diagram

If the TCR bit is set for a particular line, the "pseudo-scan" will halt when it detects the AND condition of TCR and TBMT (from the UART) for this particular line, and set Ready. If TRAN INT EN is set, an interrupt will be generated. The program then reads, from the high byte of TBUF, the line number to which the channel number points. The program then loads the appropriate character into the low byte of TBUF, and the hardware automatically clears Ready and begins searching for another AND condition of TBMT and TCR.

The "pseudo-scan" is really a 16-level priority encoder. A clock samples the state of the 16 AND gates for TBMT and TCR. The output of these gates is presented to the priority encoder, which provides the channel number of the highest priority line needing service. The clock then stops and waits for the character to be loaded. Once loaded, the clock is restarted. New samples are taken every 400 ns and presented to the priority encoder. If two lines come up at the same time, the encoder will put out the line with the highest priority. Line 15 has the highest priority, line 00 has the lowest.

When operating in interrupt mode, the program should service the channel at which the clock stopped; but, before leaving the service routine, it should check to ensure that no other lines have TBMT or TCR flags up. This procedure reduces the number of times that the service routine must be entered, thereby reducing overhead per character.

Breaks can be transmitted on any line by asserting the corresponding bit in the Break Status Register (BSR). This pulls the output line to a space and holds it there until the bit is cleared. Timing of the breaks must be done by the software.

4.3.3 Address Selection Logic

The address selection logic (drawing C-CS-M105-0-1) decodes the signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers on this logic can be altered so that the module responds to any address within the range of 760000 to 767777.

Although these addresses have been selected by DEC as the standard assignments for the DJ11, the user may change the jumpers to any address desired. However, any MAINDEC program or other software that references these standard assignments must be modified accordingly if other than the standard assignments are used.

The first five octal digits of the address indicate that the DJ11 has been selected as the device on the Unibus to be used. The final octal digit, consisting of address lines A02, A01 and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected DJ11 register is to perform an input or output operation (provided the selected register is a read/write register).

A block diagram of this module (M105) is given in Figure 4-5. Note that IN and OUT are always used with respect to the master (controlling) device; thus an OUT transfer is a transfer of data from the Unibus to the DJ11 and an IN transfer transfers data from the DJ11 to the Unibus. Inputs consists of 18 address lines, A(17:C0), 2 bus control lines (1:0), and a master synchronization (MSYN) line. Decoding of lines A(12:03) is determined by jumpers. When a line is jumpered, the address selector searches for a 0 on that line. If none exists, the selector searches for a 1. Lines A(17:13) must be all 1s thereby specifying an address within the top 8K byte address bounds for device registers.

Note that in the DJ11 five internal registers are selected by four addresses. The duplicate address 76xxx4 selects two registers (TCR and BSR), depending on the state of bit 10 in the CSR.

The Device Register select address format is given in Figure 4-6.

4.3.4 Interrupt Control Logic

The interrupt control logic permits the DJ11 to gain control of the bus (become bus master) and perform an interrupt operation. Jumpers on the logic can be altered so that the logic has a normal vector address within the range of 000 and 776.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control. One input, A, is connected to the receiver section and provides a vector address of xx0. The other, B, connects to the transmitter section and provides a vector address of xx4. The two circuits operate independently; however, if simultaneous interrupt requests occur, the receiver section has priority over the transmitter section.

NOTE

The final octal digit of the vector address is not affected by the jumpers; therefore, regardless of the vector address selected by the jumpers, the final octal digit is always 0 for receive and 4 for transmit.

The block diagram for this module is shown in drawing D-BS-DJ11-0-7.

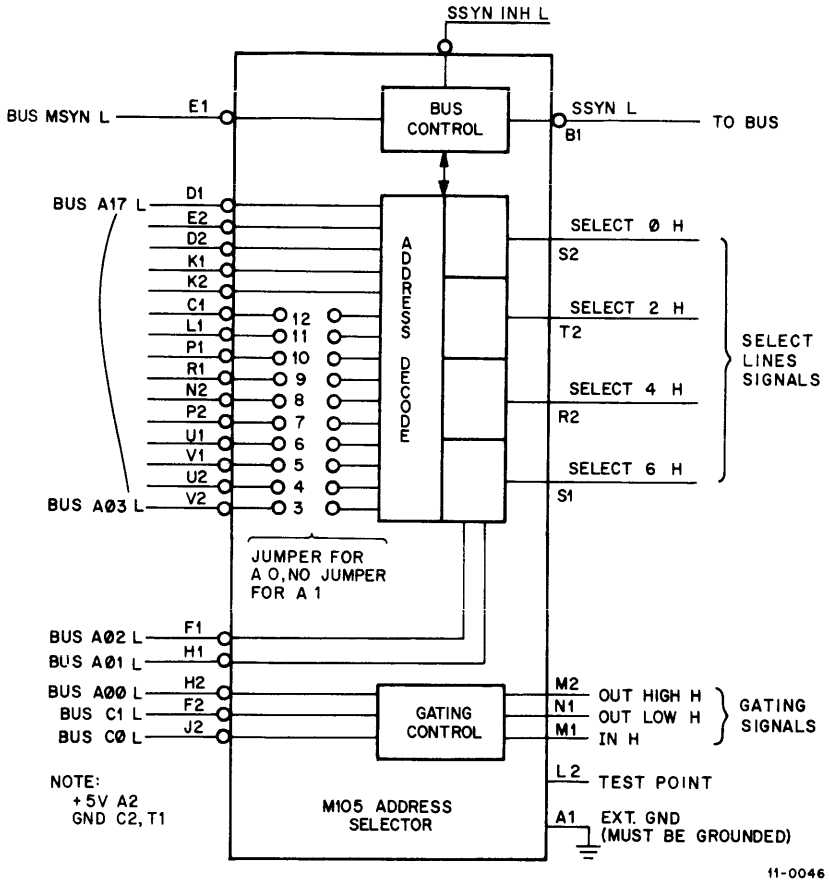


Figure 4-5 M105 Address Selector Block Diagram

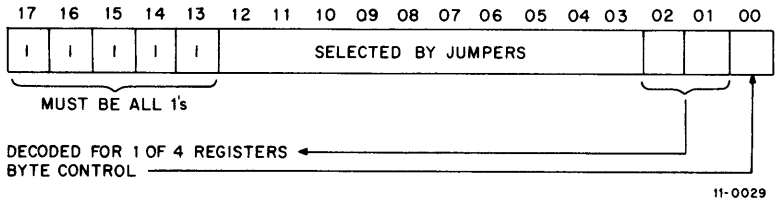


Figure 4-6 Device Register Select Address Format

4.3.5 Distribution Panels H317A/B

The distribution panels (shown as a dotted line in Figure 4-1) supplied with the DJ11-AA and DJ11-AC are used to fan out the lines to the communciation interfaces. Neither panel type requires power. They are completely passive.

Data is sent from the DJ11 to the distribution panel with its level conversion already performed. Interconnection with the panel is by two flat cables that terminate in Berg connectors. The panel fans out the lines either to individual Cinch EIA connectors on the H317B, or to 4-wire terminal strips on the H317A. Note that the PC board for the TTY (H317A) panel contains several components of the TTY circuit.

Several jumper selections are available on the distribution panels. In the EIA case, the DTR lead and the REQUEST TO SEND lead will normally be strapped to a positive or ON voltage. This strapping can be removed on a per line basis. Removal would be in order, for example, if the panel was used for a full modem control arrangement in which the modem control signals were combined with the data signals on the distribution panel. This is done with the four additional Berg connectors on the H317B panel. The modem control signals must be presented at the distribution panel already converted to EIA levels.

On the H317A panel (20 mA current loop operation), two jumpers are used to convert the receiver portion of the TTY circuit from active to passive operation. The active receiver is required for Teletypes ® and similar devices that merely provide a switch opening or closing for a binary 1 or 0. The disadvantage of this mode is that the signaling is single-ended and noise introduced on the line can cause errors. When wired as a passive receiver, the device has common mode rejection, since any noise introduced on the wires appears on both wires and hence causes no net change in the current through the diode (Figure 4-7).

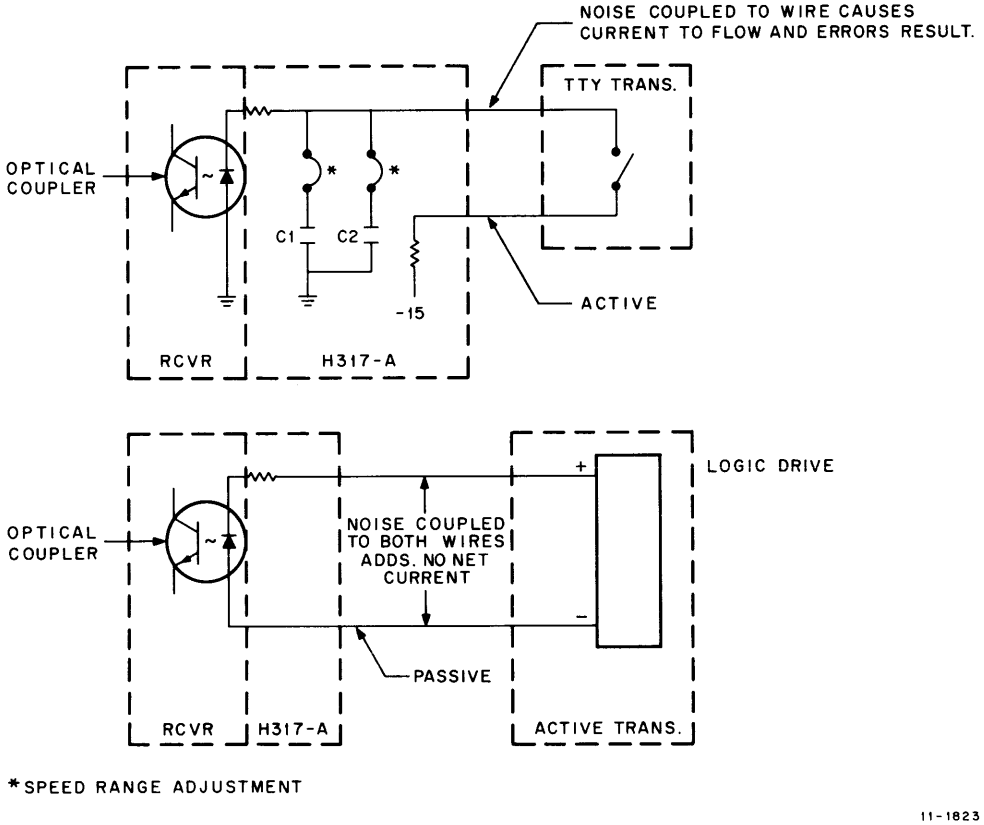


Figure 4-7 Active and Passive Receiver Wiring

® Teletype is a registered trademark of Teletype Corporation.

The H317A also contains two other jumpers for each line. They are used to insert capacitors to slow the response of the circuit. There are three speed ranges. The low speed range should be used for 300 baud and below. Both capacitors are left in for this range. Filtering adds 10 percent distortion maximum to a 300 baud signaling rate. The medium range is used for 2400 baud and below. Capacitor C1 is removed, and the filtering will cause a 10 percent distortion maximum to a 2400 baud signal. The high range occurs when both capacitors are removed and should be used above 2400 baud (Figure 4-7). For the higher speed ranges it is preferable that the remote device be the current source so that the DJ11 receiver can be strapped as a passive receiver with common mode rejection.

4.3.6 Maintenance Logic

When set, the Maintenance (MAINT) bit (bit 2 of CSR) loops back all 16 lines internally. If split speed is selected on any or all groups, the transmitter speed is forced into the receiver so that loop back can occur. This can be seen on any of the interface card schematics. The signal MAINT (H), generated on D-CS-M7285-0-1, sheet 5, is used to switch 74157 or 8266 Multiplexers and thereby bring in the output signals from the transmit side to the second set of gates on those multiplexers. This feeds the outputs to the inputs. In the clock (D-CS-M7285-0-1, sheet 10), MAINT (H) forces an 8266 Multiplexer to feed TRANS SPEED to RCV SPEED outputs, thereby tying the receive speed to the transmit speed.

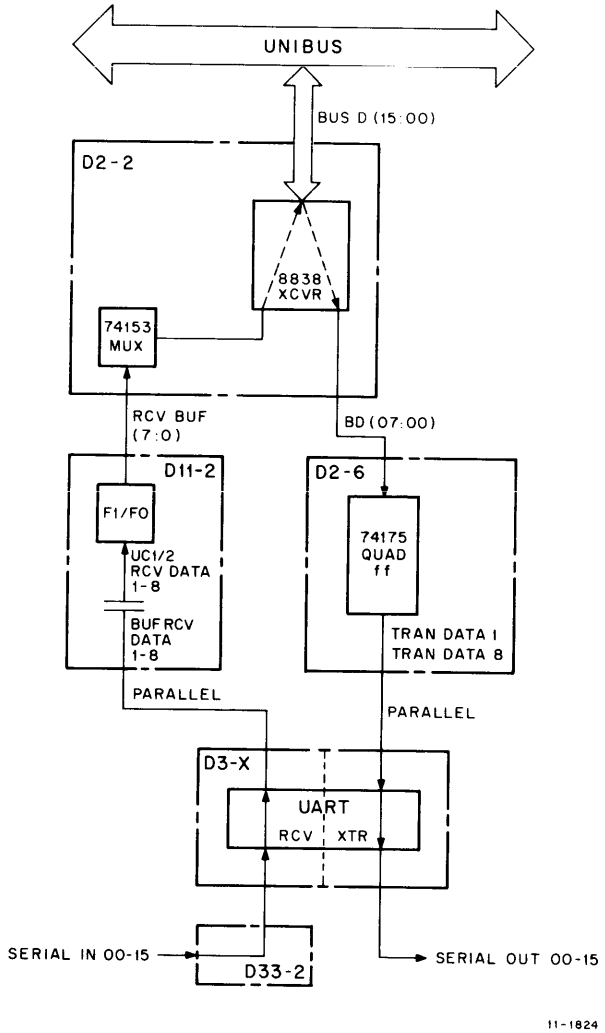


Figure 4-8 DJ11 Data Path

4.3.7 Universal Asynchronous Receiver/Transmitter (UART)

The UART, a fundamental part of DJ11 operation, converts serial data to parallel data and parallel data to a serial bit stream. The data path of the DJ11 is illustrated in Figure 4-8. Data from a single communications line is traced through to the Unibus and back through the principle hardware blocks in that path, indicating the drawing numbers on which those blocks are located in the block schematics. The transceiver shown takes the place of the receiver and transmitter buffers shown in Figure 4-1. This device (8838) is described in more detail in Paragraph 4.4 (under the description of drawing D-CS-M7285-0-1, sheet 3).

As can be seen from the figure, serial data in from the line is fed to the UART and from there transferred, in parallel, to the FI/FO where the line number is inserted in the parallel character together with error information and a bit for validity. The output of the FI/FO is then multiplexed to the transceiver and out onto the Unibus when the control handshaking sequence has been satisfied.

Information from the Unibus is fed through the same transceiver to a Quad F/F register from which it is applied, in parallel, to the transmit side of the UART (dedicated to that line) and then out on the serial line.

Sixteen separate UARTs are assigned, one to each line, in the DJ11 (Figure 4-9). The Unibus data lines are applied to all UARTs, for both DATI and DATO, and selection signals are used to select the proper UART (line number) as determined prior to the transfer transaction.

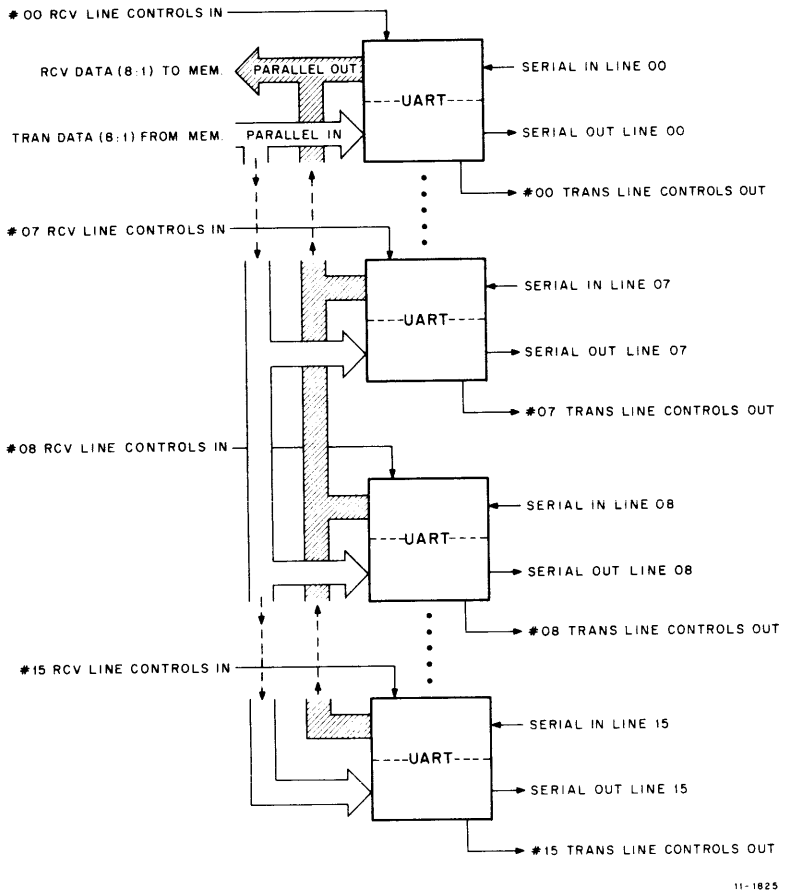


Figure 4-9 DJ11 Multiple UART Functional Block Diagram

In order to make the UART universal, the baud rate, bits per word, parity mode, and number of stop bits are selected by external logic circuits (external, i.e., from the UART).

The UART is a full duplex receiver/transmitter. The receiver section accepts asynchronous serial binary characters and converts them to a parallel format for transmission to the Unibus. The transmitter section accepts parallel binary characters from the bus and converts them to a serial asynchronous output with start and stop bits added.

All serial characters contain a Start bit, five to eight Data bits, one, one and a half, or two Stop bits, and a Parity bit, which may be odd, even, or turned off completely. The Stop bits are opposite in polarity to the Start bit.

Both the receiver and transmitter are double buffered. The UART internally synchronizes the Start bit with the clock input to ensure a full 16-element (clock periods) Start bit independent of the time of data loading. Transmitter distortion (assuming perfect clock input) is less than 2.5 percent on any bit up to 10 kbaud. The receiver strobes the input bit within ±8 percent of the theoretical center of the bit. The receiver also rejects any Start bit that lasts less than one-half of a bit time.

Figure 4-10 is a block diagram of the UART receiver. When the receiver is in the idle state, it samples the serial input line at the selected clock edges after the first mark-to-space transition of the serial input line. If the first sample is a mark (high), the receiver returns to the idle state and is ready to detect another mark-to-space transition. If, however, the first sample is a space (low), then the receiver enters the data entry state.

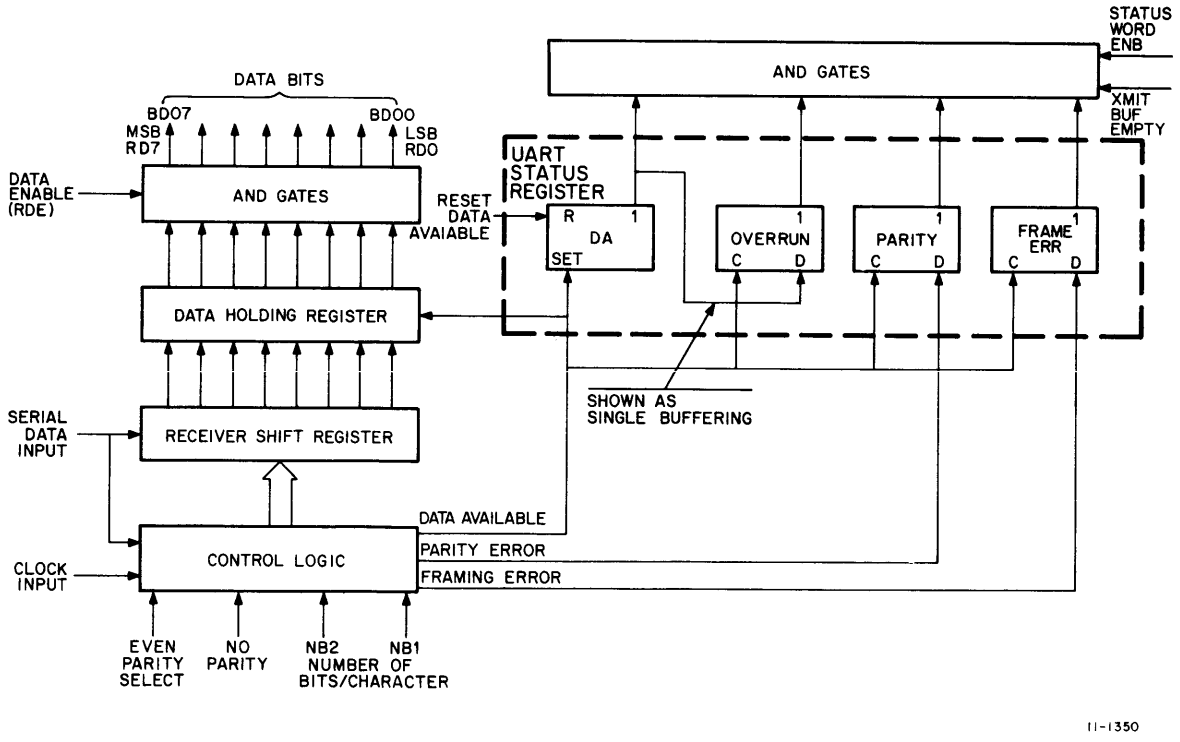


Figure 4-10 UART Receiver, Block Diagram

If the receiver control logic has not been conditioned to the no parity state, then the receiver checks the parity of the data bits plus the parity bit following the data bits and compares it with the parity sense on the parity select line. If the parity sense of the received character differs from the parity of the UART control logic, then the receive parity error line goes high and causes the parity error bit in RBUF to set.

If the receiver control logic has been conditioned to the no parity state, then the receiver takes no action with respect to parity and maintains the parity error line in the false (low) state. When the control logic senses a parity error, it generates a P ERR signal. The DATA AVAILABLE signal updates the parity error indicator.

The receiver samples the first Stop bit that occurs either after the Parity bit, or after the data bits if no parity is selected. If a valid (high) Stop bit exists, no further action is taken. If, however, the Stop bit is false (low), indicating an invalid Stop code, then the UART control logic provides a framing error indication. The status of the framing error bit can also be read from the RBUF.

Because the serial input from the line is shifted into the UART a bit at a time, the occurrence of a Stop code indicates that the entire data character has been received and shifted into the receiver shift register. After the Stop bit has been sampled, the receiver control logic parallel transfers the contents of the shift register into the receiver data holding register and then sets the data available (R DONE) flag.

The data available signal also functions as the clock input to the FRAME ERR, PARITY, and OVERRUN flip-flops in the UART status register. At this point, the DA flip-flop is set, the OVERRUN flip-flop is clear but has a high on the data input because of the output from the DA flip-flop, and the PARITY and FRAME ERR flip-flops are set or cleared depending on the signal (true or false) strobed in from the control logic.

An Overrun condition indicates that another data character is being sent to the UART holding register before the previous character has been transferred to the DJ11 receive buffer (FI/FO).

Whenever the serial input line goes from a mark (high) to a space (low) and remains at a low level, the receiver shifts in one character, which is all spaces, then sets the FRAME ERR indicator and waits until the input line goes high before shifting in another character.

A block diagram of the transmitter portion of the UART is shown in Figure 4-11. When in the idle state, the transmitter sends out a mark (high) on its serial output line. When data is transmitted, a parallel character is placed on the bus data lines and strobed into the UART transmitter data buffer by means of the data strobe signal. The time between the low-to-high transition of the data strobe and the corresponding mark-to-space transition of the serial output line is within one clock cycle (1/16 of a bit time) if the transmitter has been idle. The data strobe is used to strobe a character from the Unibus into the TBUF.

After the data has been loaded into the UART data buffer, it is transferred to the transmitter shift register under control of signals from an encoder that selects the format determined by the control logic. This permits selection of either parity or no parity, the type of parity, the number of Stop bits, and the number of Data bits per character.

The transmitter logic converts the parallel character from the Unibus into serial output that is in a format selected by the control logic.

Whenever the transmitter data buffer is loaded while the previous character is being shifted through to the output line, the Start bit of the new character immediately follows the last Stop bit of the previous character.

When the data strobe loads the UART data buffer, the DJ11 transmitter buffer is unloaded. Therefore, the data strobe sets the condition TBMT to yield a signal that indicates transmitter ready. It is this signal that is ANDed with TCR and allows the clock to stop and set TRAN RDY (CSR bit 15).

4.4 LOGIC DISCUSSION

The discussions in this paragraph are referenced to the block schematics that are part of the manufacturing drawing set supplied with the equipment and part of the manual entitled *DJ11 Engineering Drawings.* In these discussions, each sheet of each drawing is discussed separately, in numerical order, as they appear in the schematics. Discussing the circuits in this order does not imply a logical sequence.

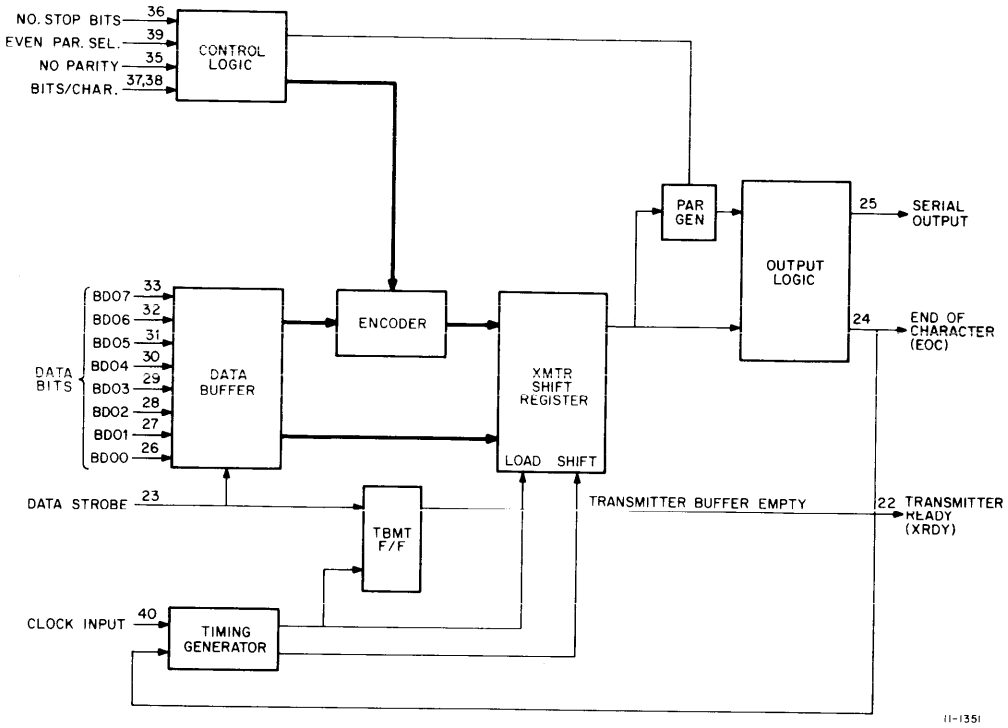


Figure 4-11 UART Transmitter, Block Diagram

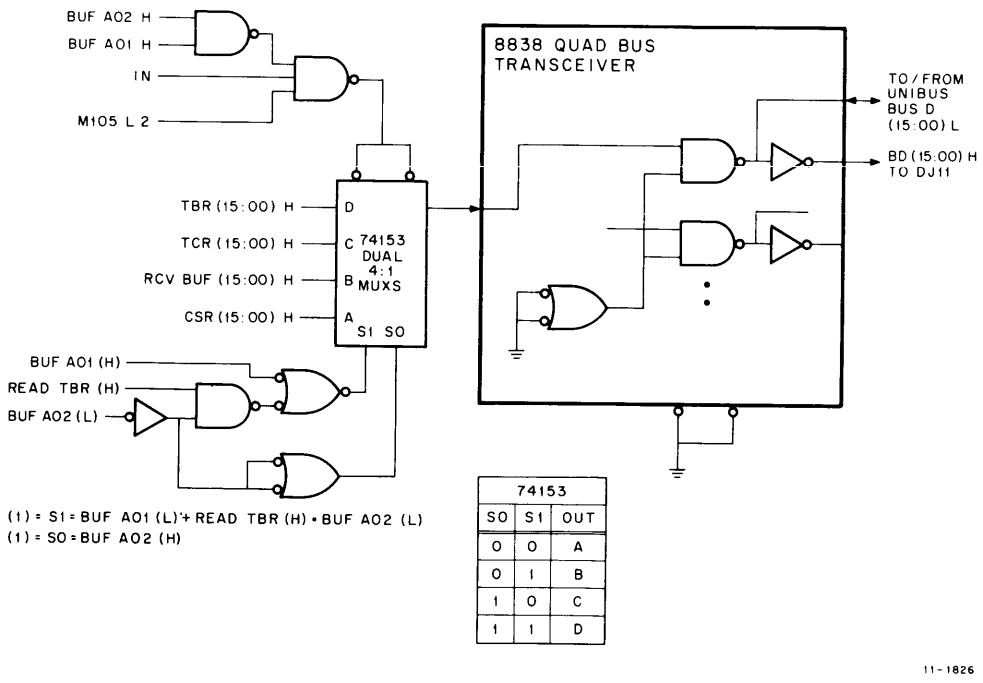


Figure 4-12 DJ11 Mux Bus Interface

4.4.1 Bus Interface (drawing D-CS-M7285-0-1, sheet 3)

The logic on this sheet comprises the data bus interface. This is made up of Dual 4:1 Multiplexers (74153s) with each pair feeding Quad Bus Transceivers (8838s). Figure 4-12 is a functional block diagram of this logic showing that 16 bits each from the TBR, the TCR, the RBUF, and the CSR are multiplexed out onto the Unibus through the transceivers as a function of BUS A01 and A02.

Note that pins 7 and 9 on all transceivers are grounded so that they are enabled all the time. Signals out to the Unibus are gated on and off by the control logic at the 74153 Multiplexer. The presence of an IN signal at DM2 indicates a DATI to the master, signaling that data from some register is to be presented to the bus. Data from the bus is received, for example, as BUS D15 L at pin 4 of the 8838 at E1. This is fed back out of the transceiver as BD15 H from pin 6.

4.4.2 Output Interface and TBR, TCR Registers (D-CS-M7285-0-1, sheet 4)

This logic, simplified in Figure 4-13, comprises the two major registers in the DJ11, the TCR and TBR. These registers are fed by BD (15:00) H, one bit for each line in the installation. These registers are byte-operable with one gate enabling the high byte, and the other gate the low byte. The registers are made up of 74175 Quad D-Type flip-flops. Both registers are addressed at the same location (76xxx4). Selection is made by CSR bit 10, used on sheet 5 to generate READ TBR (H), when set, and READ TCR (H), when clear. The registers are cleared by RESET, and the byte control is by OUTLOW or OUTHIGH generated on drawing D-BS-DJ11-0-7.

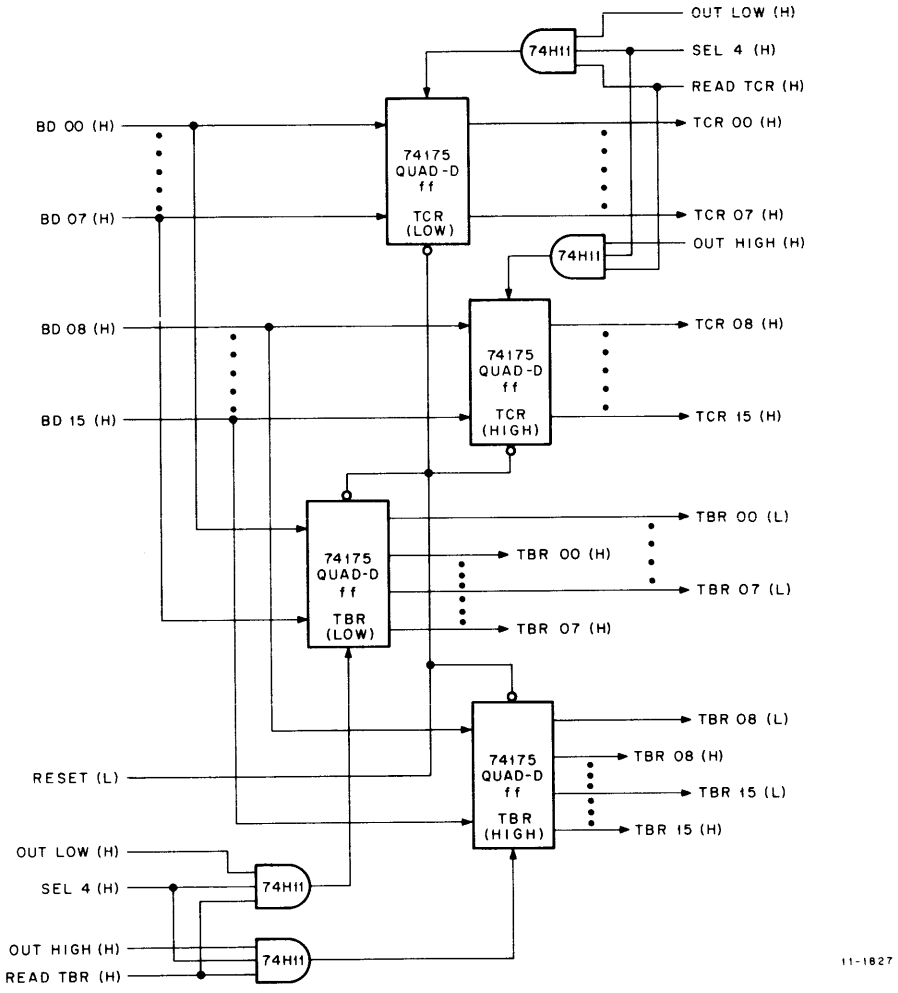


Figure 4-13 DJ11 Interface and Registers TCR and TBR

4.4.3 H/D Gating and CSR Bits (D-CS-M7285-0-1, sheet 5)

This logic is simplified in Figure 4-14. This print contains two sections, the CSR bits on the right and the half duplex gating logic on the left.

The CSR bits are set by bits BDxx (H), as shown, into two 74175 Quad-D Registers that are read/writeable. The register is byte selected by OUTHIGH and OUTLOW in combination with SEL 0 (H). They are cleared by RESET.

The logic on the left-hand side of the sheet is concerned with half duplex selection. In the DJ11, the term "half duplex" means that if any line is transmitting, that line is inhibited from receiving for that period. This mode is selectable on a 16 line basis, i.e., either *all* 16 lines are half duplex or none are.

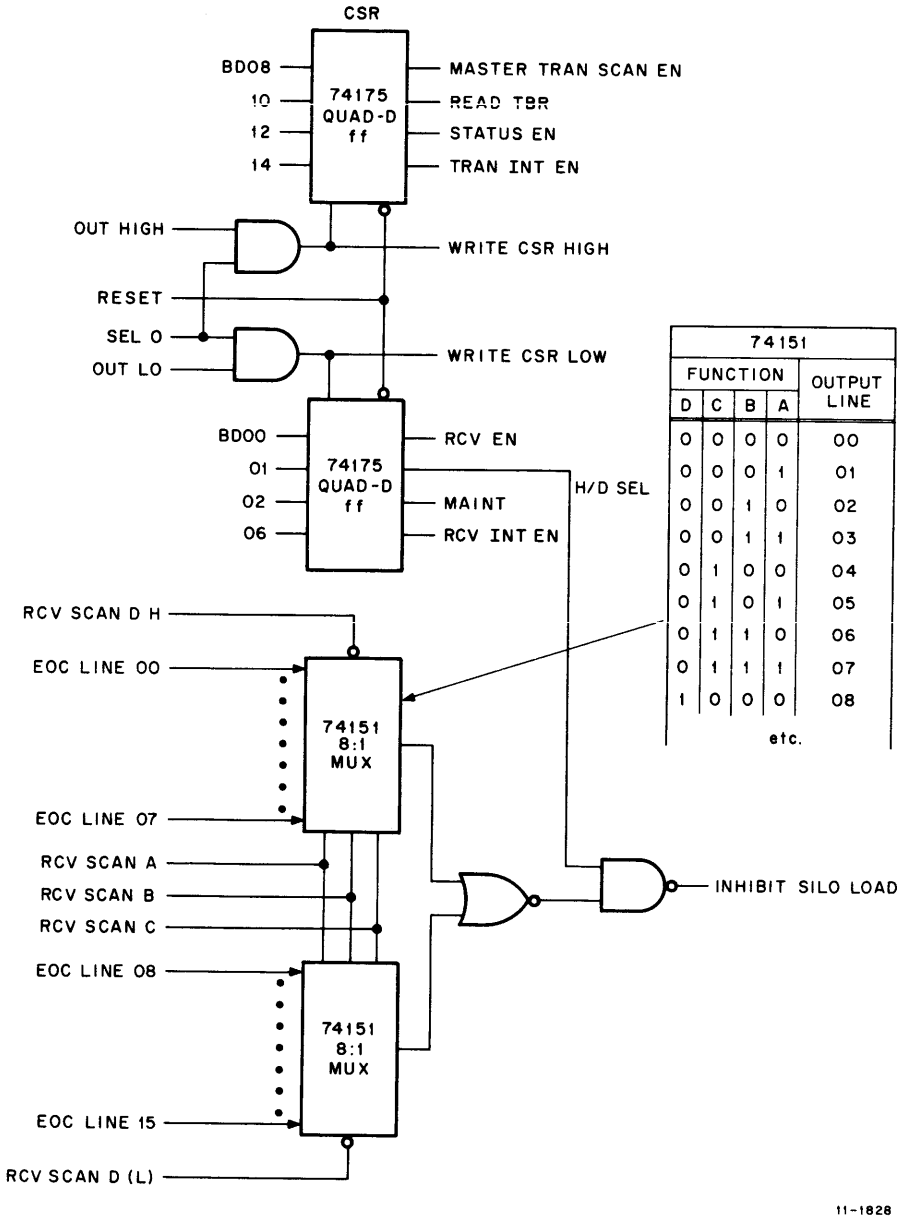


Figure 4-14 DJ11 H/D Gating and CSR Bits

When this mode is imposed on the DJ11, the UART is permitted to assemble the received character but that character is never loaded into the FI/FO. The end of character signal (EOC H), generated by the UART (M7280 module), is used to indicate that a given line is transmitting. The combinations of RCV SCAN (D:A) are used to select the particular line on 74151 8:1 Multiplexers. The resultant output is ANDed with H/D SELECT (H) to generate INHIBIT SILO LOAD (L). This signal, in turn, is used on sheet 8 to disqualify the 74H11 gate at E41 and thereby disable the LOAD SILO CONTROL flip-flop. This prevents the loading of that character into the silo.

The low version of INHIBIT SILO LOAD is then used to qualify the gate at E42 where it fires the RESET one-shot and clears the data available flag for that character, effectively throwing it away.

NOTE

For proper half duplex operation, there must be no more than one half bit time between serial transmit and serial receive.

4.4.4 Transmit Line Request Detect (D-CS-M7285-0-1, sheet 6)

Figure 4-15 is a simplified block diagram of this logic. This logic is used to sense when a request to transmit is raised on a particular line and to translate that line number to selection signals (TRANS SCAN x) that are used throughout the DJ11 to multiplex operation.

The DJ11 "scanner" is not the traditional type used in most equipments. This is not a sequential stepping scanner that would rotate through the lines in a systematic manner before any line could be brought up. *This* logic, in a sense, looks at all lines simultaneously and responds to the request immediately. When more than one request is raised, it responds to that line with the highest assigned priority. So, in addition to being able to respond to lines in a random fashion, it has the added feature of assigning priorities to those lines.

The TCR controls transmission such that if the program sets the control bit for a particular line, and if the TBMT flag is set for that line, the so-called scanner will "stop" at that line. This is what is accomplished by the row of AND gates down the left-hand side of the sheet. Their outputs feed 74175 Quad-D Registers.

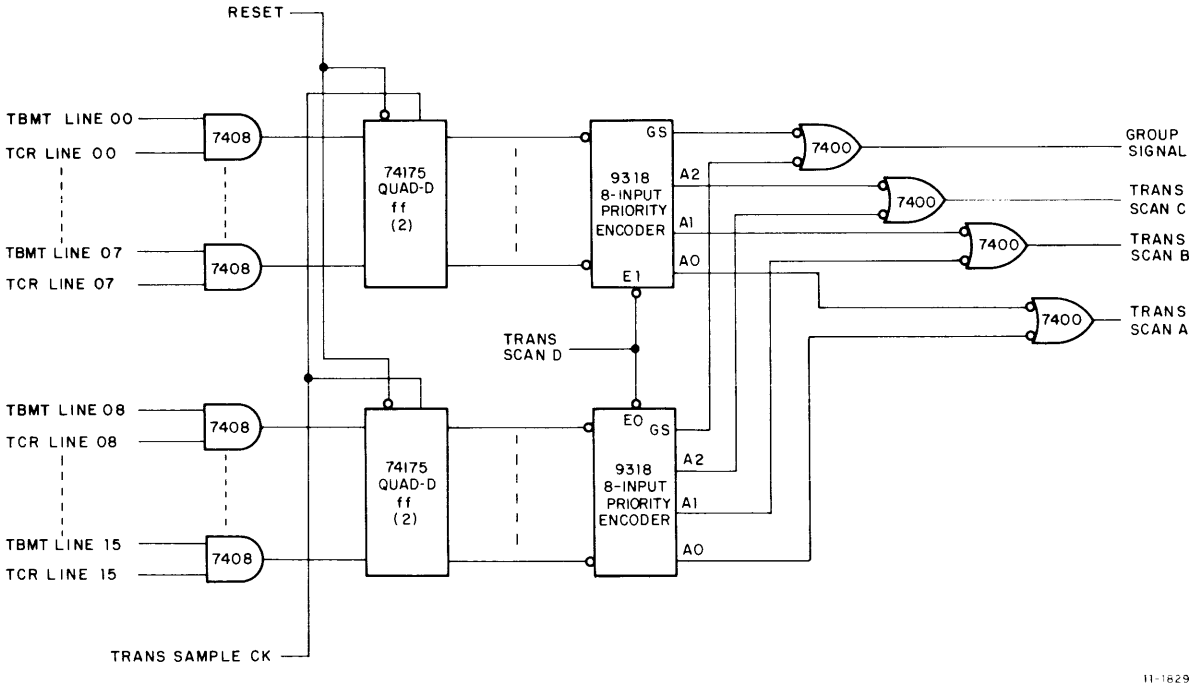


Figure 4-15 Transmit Line Request Detect Block Diagram

The inputs to these registers are sampled every 400 ns by TRANS SAMPLE CK, which is used to clock-load these registers. TRANS SAMPLE CK clocks the 74175 on its leading edge and remains high for approximately 400 ns to give the input signals time to propagate through the 9318 Priority Encoders.

The priority encoders are designed to yield the binary combination representing the line number at their inputs. When an input goes low, if for example it was line 4, the output would be 100; but if two or more inputs go low at the same time, the output of the encoder will be the binary combination representing the highest numbered input, e.g., line 7 output would be 111. When any input goes low, the inverting OR at E52 pin 11 yields GROUP SIGNAL (H).

The signal GROUP SIGNAL (H) is used on sheet 7 to set the Ready flag when TRANS SCAN CLOCK goes low. In addition, when the Ready flip-flop sets, its 0 side is used to force a high out of the OR gate at E32, thereby shutting off the clock and causing the scanner to not proceed from the line number on which it stopped.

The line number to which the TRANS SCAN x outputs on sheet 6 are pointing are readable by the program when it accesses the high byte of register 06. At this point the data to be transmitted is fetched from the appropriate buffer and loaded into the low byte of register 06, from which it is loaded into a buffer register (TBUF) on sheet 7.

Note that TRANS SCAN D is not ORed on its output as are the other trans scan signals. Instead, both the high and low versions are made available to select between UART lines 0–7 (low version) and lines 8–15 (high version).

4.4.5 Trans Scan Control (D-CS-M7285-0-1, sheet 7)

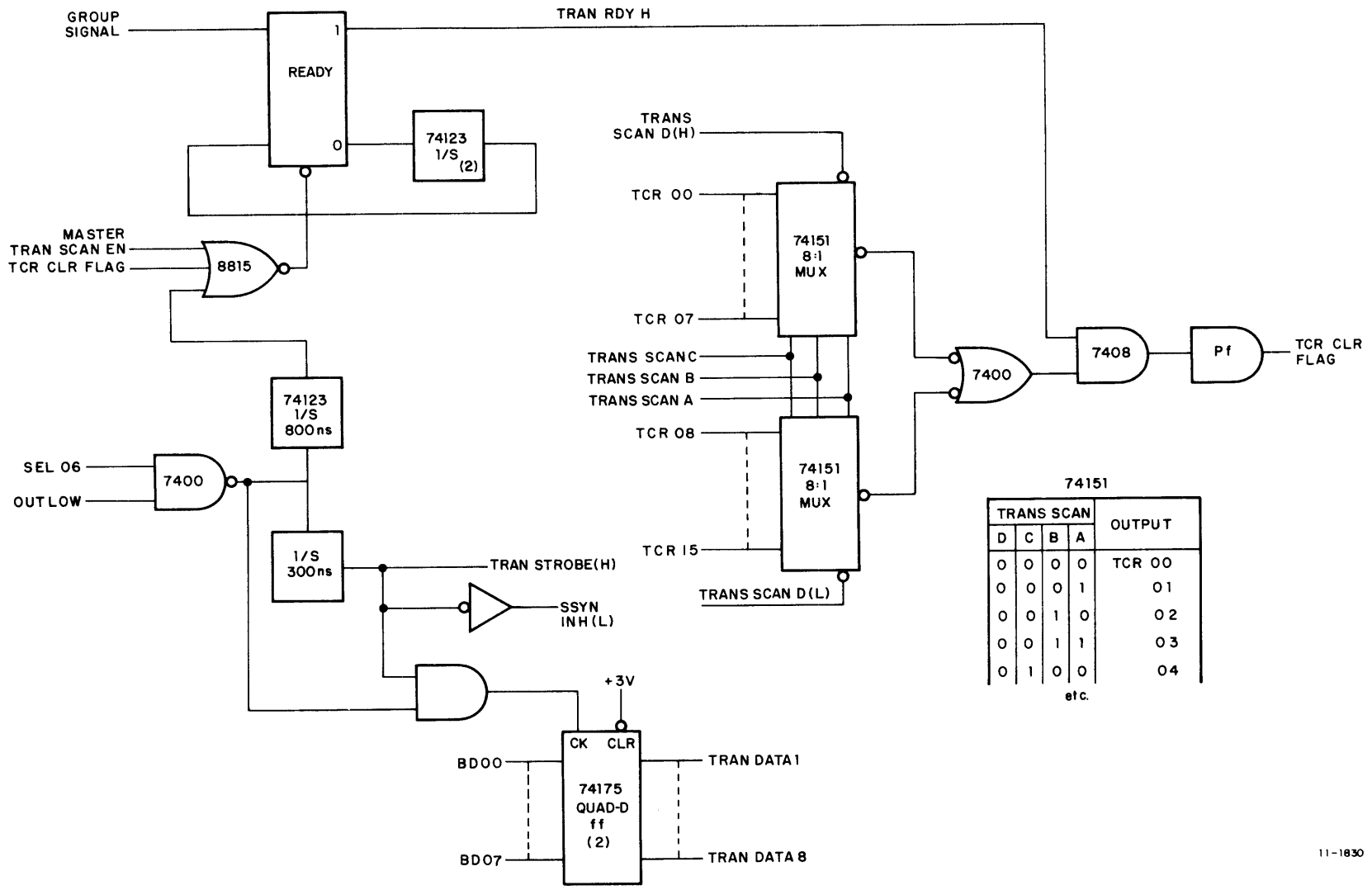
This logic is simplified in Figure 4-16. It is here that the control signals for the transmit scan function are generated, and a means is provided to permit the programmer to leave a line that he has erroneously selected, without having to load a character to achieve it.

The clock TRANS SAMPLE CK (H), shown at the top of the page, is the result of two 74123 one-shots that produce the 400 ns/50 ns duty cycle shown at the top of the page. The operation of this pulse train is under the control of an OR of MSTR TRAN SC EN (CSR bit 8), GROUP SIGNAL (READY) and a 1 μs one-shot at E39. The assertion of any of these signals will, by virtue of the logic mismatch into the clock, stop the clock from running.

The character to be transmitted is stored in the holding register at the bottom of the page. This TBUF, a pair of 74175 Quad-D flip-flops, was loaded from the low byte of register 06 [BD (07:00)] by the combination of SEL 06 (H) and OUTLOW (H).

The timing arrangement of these signals is shown in Figure 4-17. The ANDing of SEL 06 (H) and OUTLOW (H) fires both the 1 μs and 300 ns one-shot. The signal TRANSMIT STROBE (H) is only sent to the UART selected by the trans scan combination. The second one-shot, however, is used to hold off the clock an additional amount of time to allow TBMT to decay in the MOS device. This decay time is approximately 500 ns, well within the 1.2-μs delay. Delaying the start of the clock in this way prevents overlaying characters into the UART that would occur if the same TBMT were to be seen a second time by the next TRANS SCAN CLOCK.

The two 8:1 Multiplexers (74151s) on the right-hand side of the sheet are used to restart the scanner should the program stop the clock on a line and then not wish to transmit a character. Here all TCR bits are multiplexed by the TRANS SCAN x combination. All that is necessary is for the program to clear that TCR bit for the line on which the clock is stopped. This output, ANDed with TRAN RDY yields a TCR CLR flag. That 50-ns pulse through the 8815 gate at E49 will direct clear the Ready flip-flop and restart the clock.



74151

TRANS SCAN				OUTPUT
D	C	B	A	
0	0	0	0	TCR 00
0	0	0	1	01
0	0	1	0	02
0	0	1	1	03
0	1	0	0	04

etc.

Figure 4-16 Trans Scan Control Block Diagram

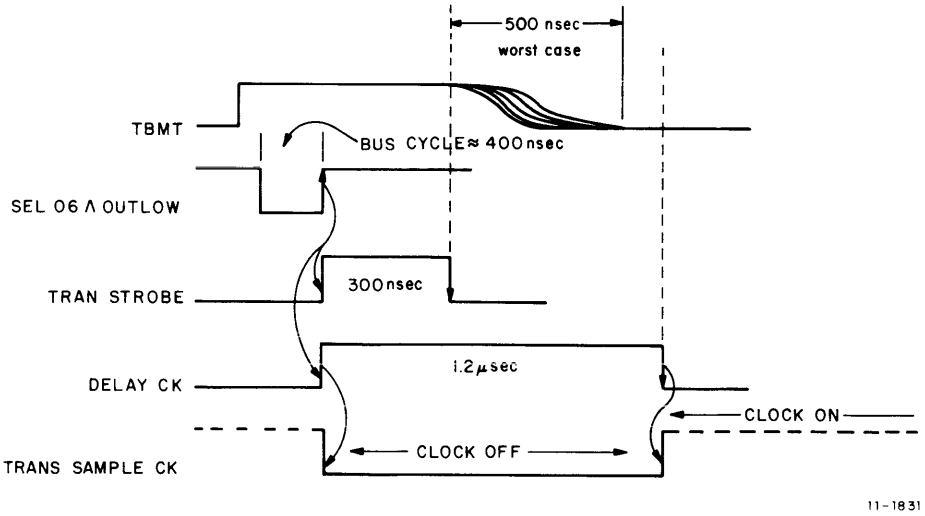


Figure 4-17 TBMT MOS Decay Protection

4.4.6 Receiver Scanner (D-CS-M7285-0-1, sheet 8)

The DJ11 receiver, unlike the transmitter, uses the standard scanning technique. This logic, simplified in Figure 4-18, uses a scanning counter to sequentially look at each line. Once it has looked at a line, it will not look at that line again until all other lines have been looked at in order.

The counter, designated RCV CH # CT, (Receive Channel No. Count) is a 74193 that yields outputs, RCV SCAN A:D (H), that are sent to decoders on the UARTs (M7280 cards). To take care of the full 16 lines, two polarities of RCV SCAN D are sent back with the low version sent to UARTs 0–7 and the high version to UARTs 8–15.

The counter is incremented by the setting of the INC SCAN flip-flop at E44 which is, in turn, clocked by a 74123 RCV SCAN OSC clock at E15. The clock is enabled by RCV ENABLE (H), a function of CSR bit 0. Characters cannot be received, and the scanner cannot run, unless this bit is set.

The operation of this logic can best be described by first assuming that there are no characters coming into the DJ11 and hence no characters being assembled in the UARTs. If these conditions are assumed, no DATA AVAILABLE signals will be generated, and four lows will exist on the 8815 gate at E49. When this is true, the D input of the INC SCAN flip-flop will be high and on the next clock from RCV SCAN OSC, the RCV CH # CT increments.

When INC SCAN sets, it enables the SAMPLE LINE flip-flop causing its 0 side to go low. This yields a 50-ns pulse from the 7402 pulse-former at E34 that feeds a 74H11 at E41 to clock the LOAD SILO CONTROL flip-flop if INH SILO LD is false, and if the silo is READY IN (L).

If the silo is ready, a signal is generated on that board that indicates that the silo can accept another character. If it is assumed that this is the case, and that no MASTER DAs are present, or that no UART had a character assembled, the next clock will drive LOAD SILO CONTROL (1) low and the resulting mismatch on the 8815 and at E49 causes a low on the D input of INC SCAN. The next succeeding clock will then complement SAMPLE LINE, causing the next clock to set INC SCAN and increment the RCV CH # CT (Figure 4-19).

The scan line outputs of the counter go out to enable multiplexers on the M7280 board to yield one UCx MASTER DA from all the data available signals on that UART card. When the 50-ns pulse from the pulse-former at E34 is generated, the multiplexers look at only one DA, the one pertaining to the UART on the line selected.

The counter then performs the same test on the next line in order, checking to see if the DA is up and if the silo is ready. If the silo is ready, it is clocked; if no DA is asserted, the scanner moves to the next line. If, however, on that second clock pulse, the MASTER DA shows that a character *is* assembled in the UART (high), when the 50-ns pulse is asserted, the LOAD SILO CONTROL flip-flop is set. This forces a low on the D input of INC SCAN by disqualifying the AND at E49, and forces a high on the D input of RCV ENA flip-flop. When this occurs, the third clock pulse in the series just described sets RCV ENA sending RCV DATA ENA (H) out to that UART where it enables the received data leads of the selected UART.

NOTE

The UARTs are tri-state outputs on the receive lines. They are wire ORed and, when they are enabled, data is sent out on the received data lines.

When RCV ENA sets, its 0 side fires a 74123 1-μs one-shot that generates TEMP INHIBIT. This is doubled back to the input of the clock and causes it to turn off. This is done because the width of the basic clock pulse is 300 ns which is not enough time to allow the data to set up in the FI/FO.

Once RCV ENA is set, after TEMP INHIBIT times out, the next clock will set START LOAD causing LOAD SILO (L) to be issued to the FI/FO on D-BS-DJ11-0-6, sheet 1. Combinational logic on that sheet converts this to LOAD SILO (H), which is used to clock the FI/FO chips on sheet 2. Here, along with loading in the data, the line number and status information pertinent to that data is also loaded. On sheet 1, LOAD SILO L clocks the 74H74 at E25, yielding LOAD IN PROGRESS L. This flip-flop clears once the silo is loaded. LOAD IN PROGRESS then is used to stop the clock on D-CS-M7285-0-1, sheet 8, during the period that the silo is being loaded, providing an interlocked communication between the receive scanner clock and the FI/FO.

Once loading is complete, the clock resumes, thereby setting the CLEAR DA flip-flop which, in turn, fires a 1-μs one-shot at E28. This generates both RESET DA and TEMP INHIBIT, stopping the clock and resetting the data available flag for that UART. The opposite side of the one-shot is used to clear both the LOAD SILO CONTROL flip-flop and the last three flip-flops in the chain just described.

The next clock after the end of TEMP INHIBIT L increments the count to the next line and the sequence begins again.

If at this time MASTER DA is asserted but READY is not, the indication is that the silo is full. In this case, the program must be warned that the UART has assembled a character but is unable to put it into the silo. This warning is accomplished by FI/FO OVERRUN, which sets on this combination of conditions. The signal does not indicate an overrun but it does say that an overrun is imminent. It gives the program an opportunity to unload a character from the FI/FO before any characters are lost.

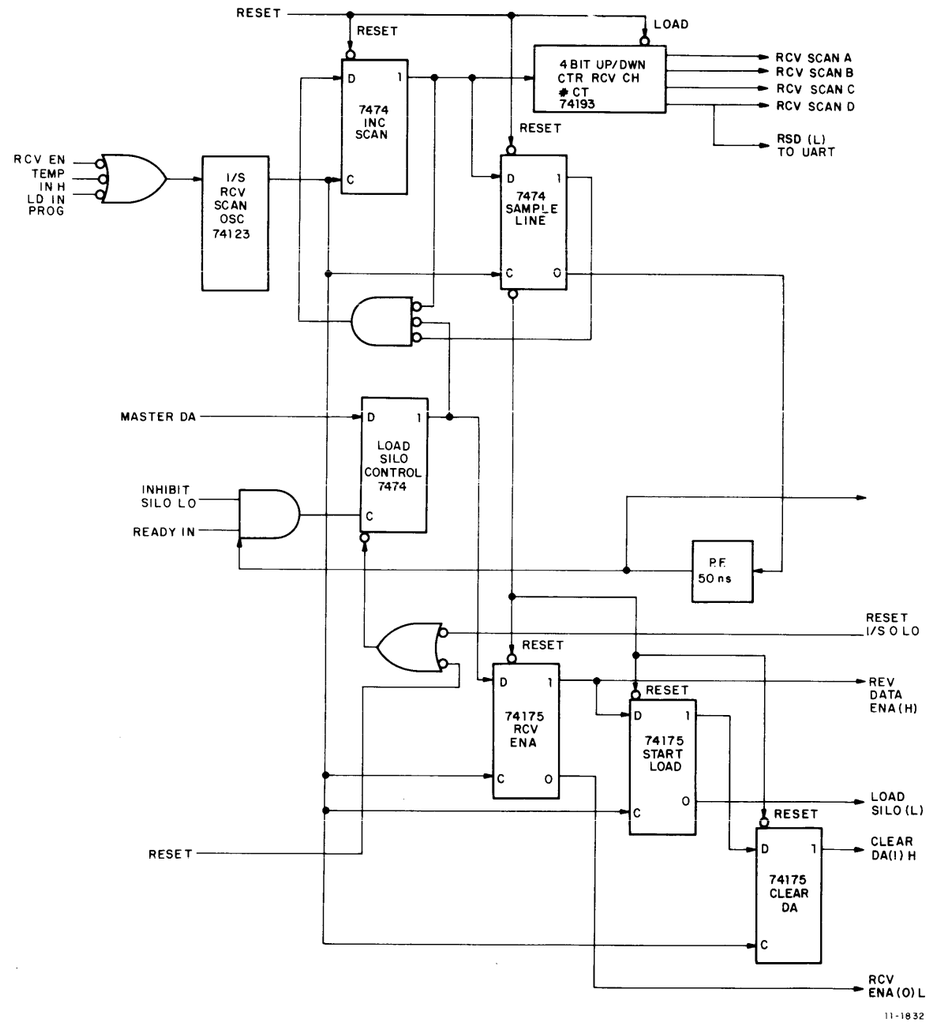
When anything is read out of the silo, READ RCV BUFFER (H) clears the FI/FO OVERRUN flip-flop.

4.4.7 Miscellaneous Control (D-CS-M7285-0-1, sheet 9)

This print contains various pieces of combinational logic that perform control functions in the DJ11. The MASTER DA signals from the two UART cards (UC1 and UC2) are ORed to produce MASTER DA (H). REQ RCV INT (H) is sent to the M7821 Interrupt Card on the presence of an FI/FO OVERRUN when status is enabled, or when a RCV INT is enabled and there are characters available.

BUS INIT produces two polarities of reset. It also ORs to clear out all the UARTs, i.e., initializes all the UARTs and FI/FO without initializing any of the other registers. When BD03 is set, a 2-μs one-shot fires to clear out all the UARTs or flush the FI/FO buffer.

This sheet also shows the priority jumper at E45.



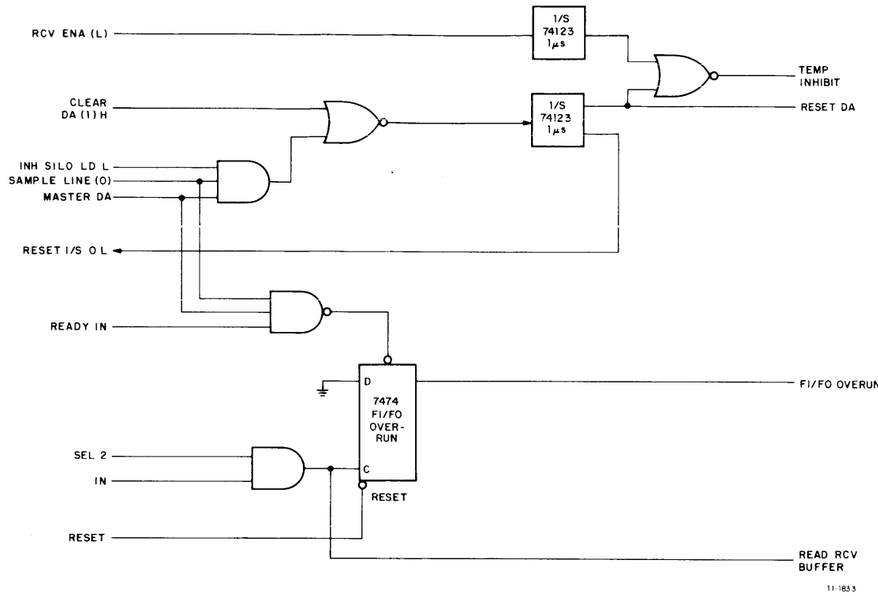


Figure 4-18 Receive Scanner Block Diagram

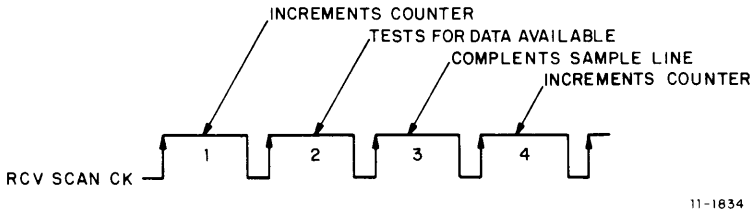


Figure 4-19 Receive Scan Clock Events

4.4.8 Clock and Distribution (D-CS-M7285-0-1, sheet 10)

This logic is shown in simplified form in Figure 4-20. The figure has been keyed to the block schematic by chip and pin number to facilitate correlation. The description is referenced to the simplified diagram, but should be simultaneously traced by the reader on the block schematic since the actual interconnection of ICs is looped in a complex fashion.

The basic crystal-controlled 5-MHz oscillator (5.0688) is fed first to a divide by 11 to yield 460.8 kHz. This frequency, in turn, is divided by 3 to give the 9600 baud rate.

The 460.8 kHz output is also divided by 6 in the same chip to yield 76.8 kHz or 4800 baud. The 76.8 kHz output is then divided sequentially by 2 to produce the 2400, 1200, and 600 baud rates. The 600 baud output (9.6 kHz) is then divided by 2, 4, and 8 to yield the 300, 150, and 75 baud outputs.

The 460.8 kHz output of the divide by 11 chip is also fed to a divide by 2 chip to yield 230.4 kHz, which is then divided by 2, 4, and 8 to produce the 7200, 3600, and 1800 baud set.

Finally, the basic oscillator frequency is also used to feed a divide by 16 string producing 316.8 kHz. This latter frequency is fed first to a 3, 7, 7 combination for the 134.5 baud output, and to a 6, 6, 5 string for the 110 baud output.

Note that the UART specifications require the frequency to be 16 times the baud rate. This relationship can be seen by the frequencies shown in Figure 4-20.

The odd value counters used in this logic are designed so that they will count to 16 when unmodified. They can be preset to any number below 16 to count the difference and thereby divide by that difference factor. In the 74161 divide by 11 chip at E84, the counter is preset to 3 so that it will count 11 places to 15 (1111), where the next carry will reset it to 100 or 4.

4.4.9 Multiple UART Card Lines 15:00 (D-BS-DJ11-0-3, sheets 2–5 and D-BS-DJ11-0-4, sheets 2–5)

This logic is simplified in Figures 4-22 and 4-23. These eight sheets represent the identical circuitry for the 16 lines multiplexed by the DJ11. Each sheet contains two UARTs with identical input and output signals. The leads on the upper portions of each UART block pertain to the receive function with the received serial data from the line fed in at pin 20. The assembled character is then fed out to the memory from pins 5 (MSB) through 12 (LSB). These outputs are wire-ORed from all UARTs. The output of the UART is a tristate totem-pole construction with a transistor for a 1 and a separate transistor for a 0. When both transistors are turned off, the output floats. When an output is enabled, no others are enabled and the data is sent out on the line(s) selected.

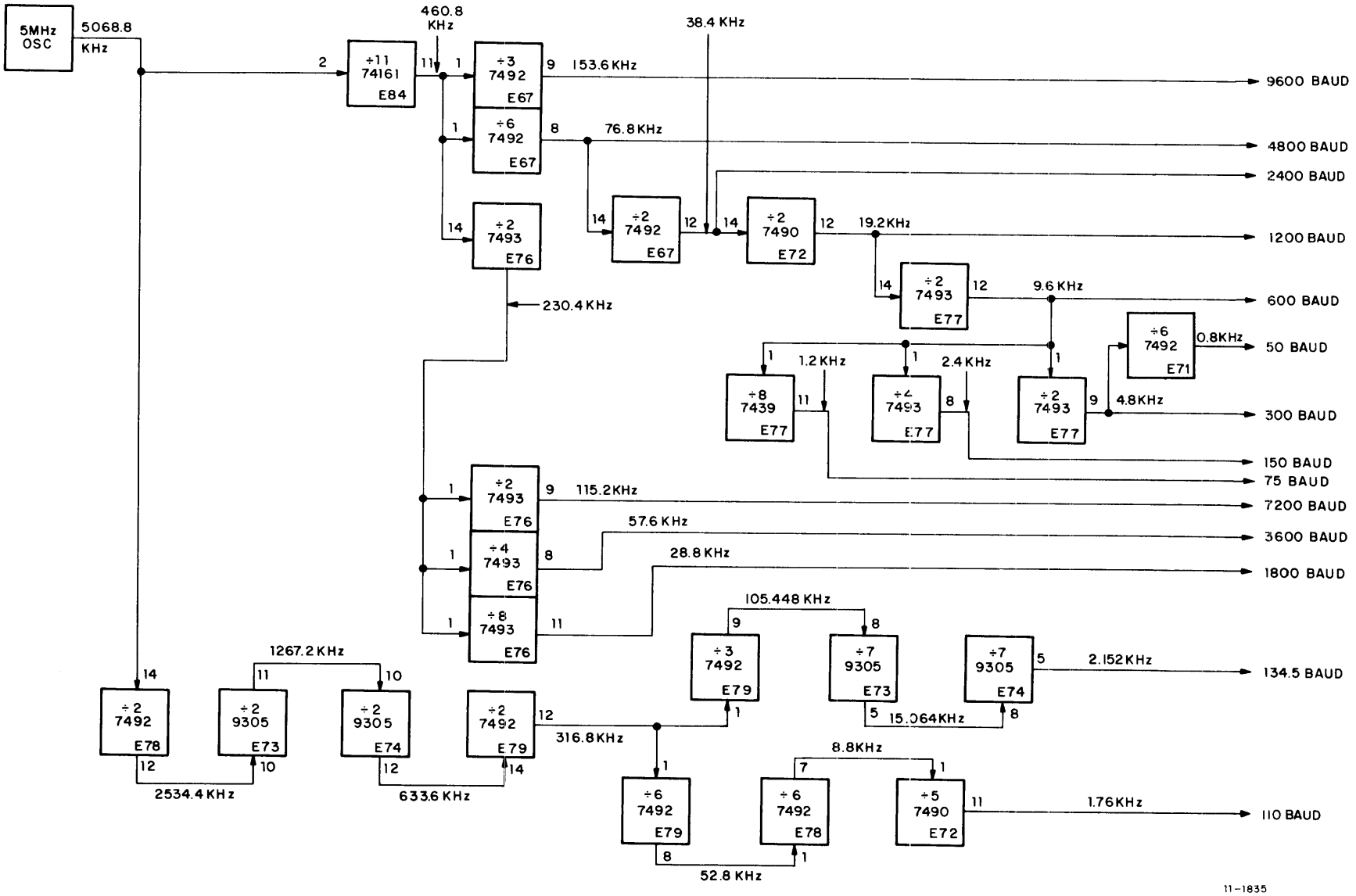


Figure 4-20 DJ11 Clock, Functional Block Diagram

The leads on the lower portion of the UART block pertain to the transmit function. Here the parallel data to be transmitted from memory is fed to pins 26 (LSB) through 33 (MSB), converted to a serial stream, and fed out to the line from pin 25.

On the schematic, the various UART parameter controls are fed into the bottom of the block.

All the BUF RCV DATA x bits, converted from SERIAL IN on the UARTs are commonly inverted on sheet D3-3 to UC1 RCV DATA x bits and on sheet D4-3 to UC2 RCV DATA x bits and sent to the input gates on the FI/FO on drawing D-BS-DJ11-0-6, sheet 2. The parallel characters from memory to be transmitted out on the lines are buffered on sheets D3-4 and D4-4 to BUF TRAN DATA x bits. The data input to these sheets is from the transmit buffer on drawing D-CS-M7285-0-1, sheet 7.

The selection schemes of a specific UART for reception or transmission are shown simplified in Figures 4-21 and 4-22, respectively. For actual UART blocks, refer to the drawing set.

In the receive case, 74155 1:8 Multiplexers are used to convert the combinations of RCV SCAN A:D to discrete Read Data Enable and Read Data Available signals for the UARTs. Note that the inverse sensing of RCV SCAN D is located on drawing D-CS-M7285-0-1, sheet 8, and not on this card. This permits the enabling of the upper set of UARTs and the disabling of the lower set when any line between 8 and 15 is called for. The 74155 Multiplexers are also used in similar fashion to select the BUF DS LINE control signals for the UARTs. This is the transmit strobe line.

In the transmit case, shown in Figure 4-22, 74155 8:1 Multiplexers are used in a similar selection scheme to produce a single set of control (MASTER) signals from the various UART outputs.

The operation of the UART is described earlier in the block diagram discussions and is also described in detail in UART specification A-PS-1910459-0-0; therefore, this discussion is not repeated here. However, a timing diagram of the UART data format is given in Figure 4-23 for reference.

4.4.10 DJ11 Control Interface (C-CS-M105-0-1 and D-CS-M7821-0-1)

These sheets show the block diagram representation of these standard PDP-11 modules. Their operation is standard and is described in detail in Paragraphs 4.3.3. and 4.3.4. The one deviation from ordinary use is that A01 and A02 are buffered versions of these bus signals received in the DJ11 on sheet 3 of the M7285 module.

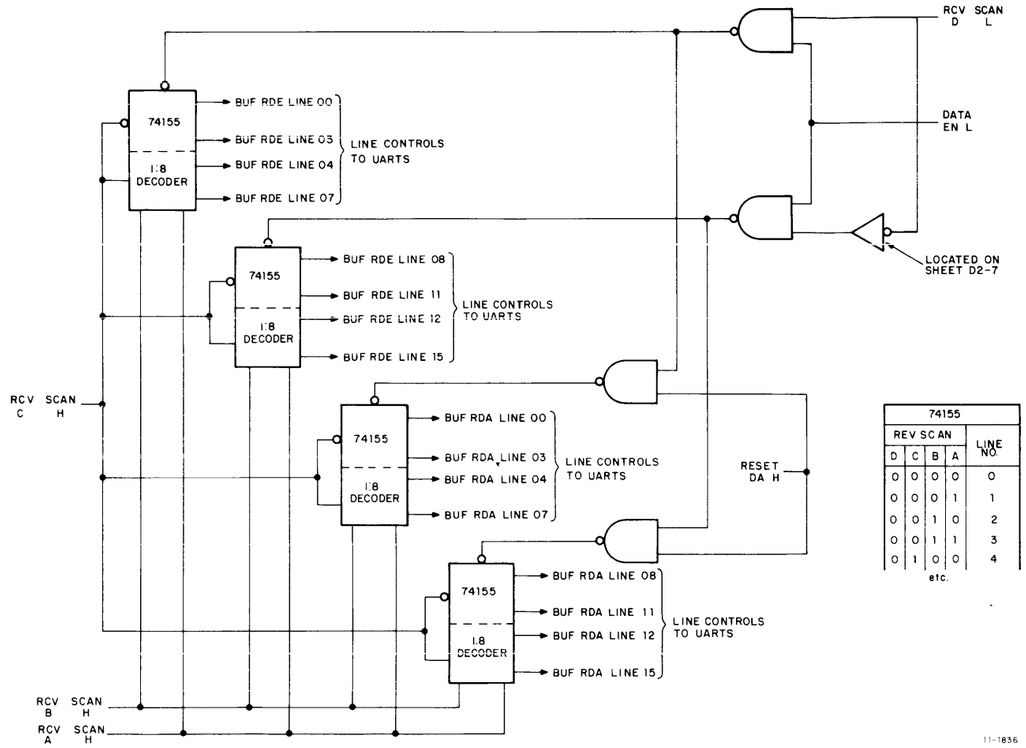
4.4.11 DJ11 FI/FO Buffer (D-BS-DJ11-0-6, sheet 2)

This sheet shows the logic for the FI/FO buffer used in the DJ11 to accumulate and buffer characters received from the various serial lines (via their UARTs) and transmit them to the host computer when Unibus dialogue has been satisfied.

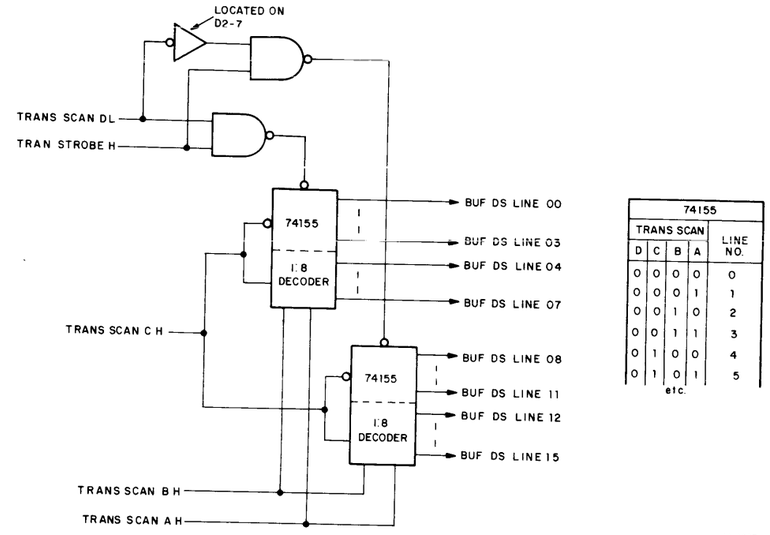
The FI/FO (or silo) is a set of four 3341 4 bit wide X 64 word propagateable registers which, when concatenated, provide the Unibus with a 16-bit word that contains a data character and pertinent data as to the line number on which it was received and various status conditions about that character (Figure 4-24).

The silo is fed from four 74157 4-bit 2-input multiplexers that feed the 15 bits required for one FI/FO word. These multiplexers are normally selected by a 01 combination that causes them to send out the ORed inputs from the UARTs, the RCV SCAN x combinations, and the Master status information from either of the UART cards (UC1 or UC2). When the select combination is 11, by jumpering E01R1 to E01T1, the alternate inputs to the multiplexers are sent to the FI/FO allowing alternate 1s and 0s in adjacent bit positions to be deposited into the silo for maintenance purposes.

Data multiplexed to the input pins of the 3341s is loaded into the top position by LOAD SILO H generated on sheet 1. That character or word is then propagated down to the last open word position in the chip by internal logic. The data residing in the bottom position of the chip is read out by READ SILO H, also generated on sheet 1. There are two flags, READY IN that indicates that a character may be loaded in, and READY OUT that indicates that a valid character is available at the bottom of the silo.



74155 REV SCAN D	C	B	A	LINE NO.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
etc.				



74155 TRANS SCAN D	C	B	A	LINE NO.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
etc.				

Figure 4-21 Multiple UART RCV SCAN Selection Scheme

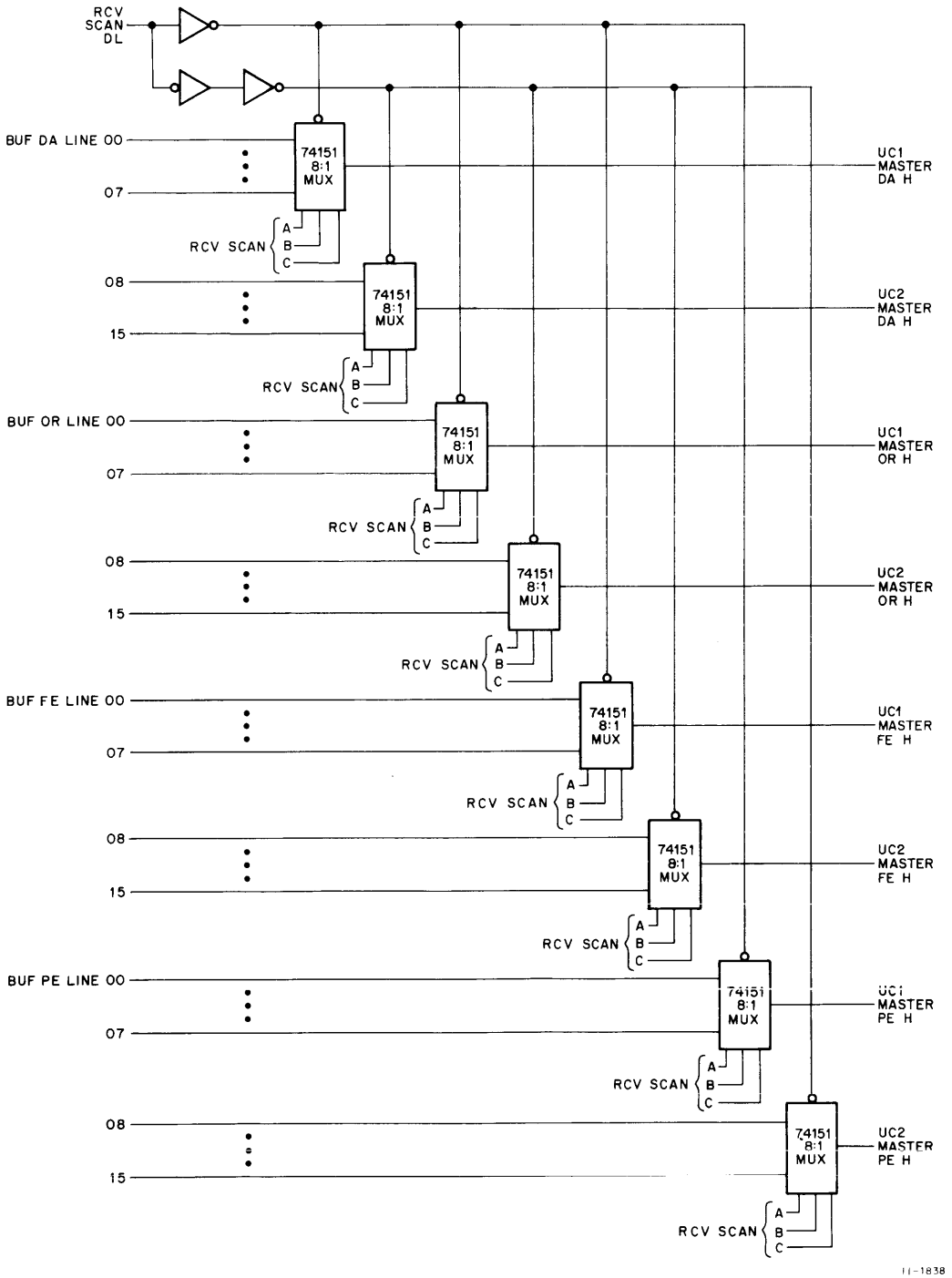


Figure 4-22 Multiple UART Trans Line Selection Scheme

Note that bit 15 of each word (Valid Data) is the product of combinational logic and is not a stored bit in the FI/FO. This bit is a copy of Valid Data which is produced on sheet 1 as a function of READY OUT.

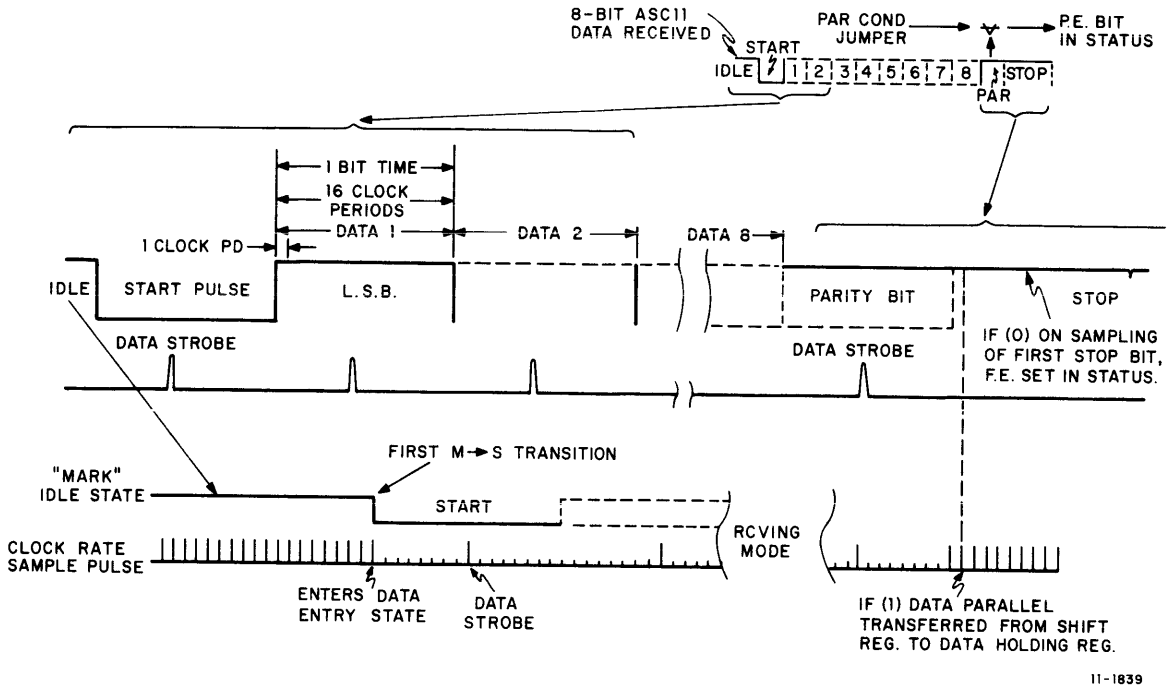


Figure 4-23 UART Data Format Breakdown

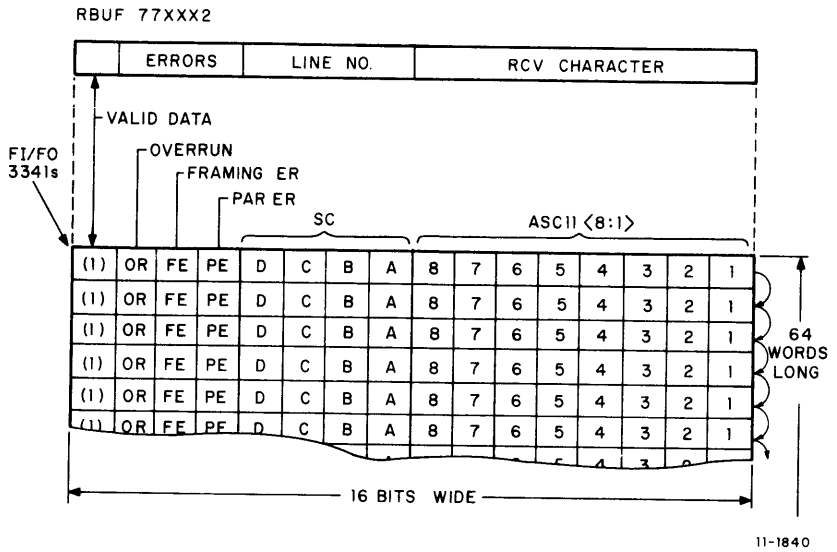


Figure 4-24 FI/FO Buffer Format

4.4.12 FI/FO Buffer Control Logic (D-BS-DJ11-0-6, sheet 1)

This logic is simplified in Figure 4-25. It is the control logic for the FI/FO buffer discussed in the preceding paragraph.

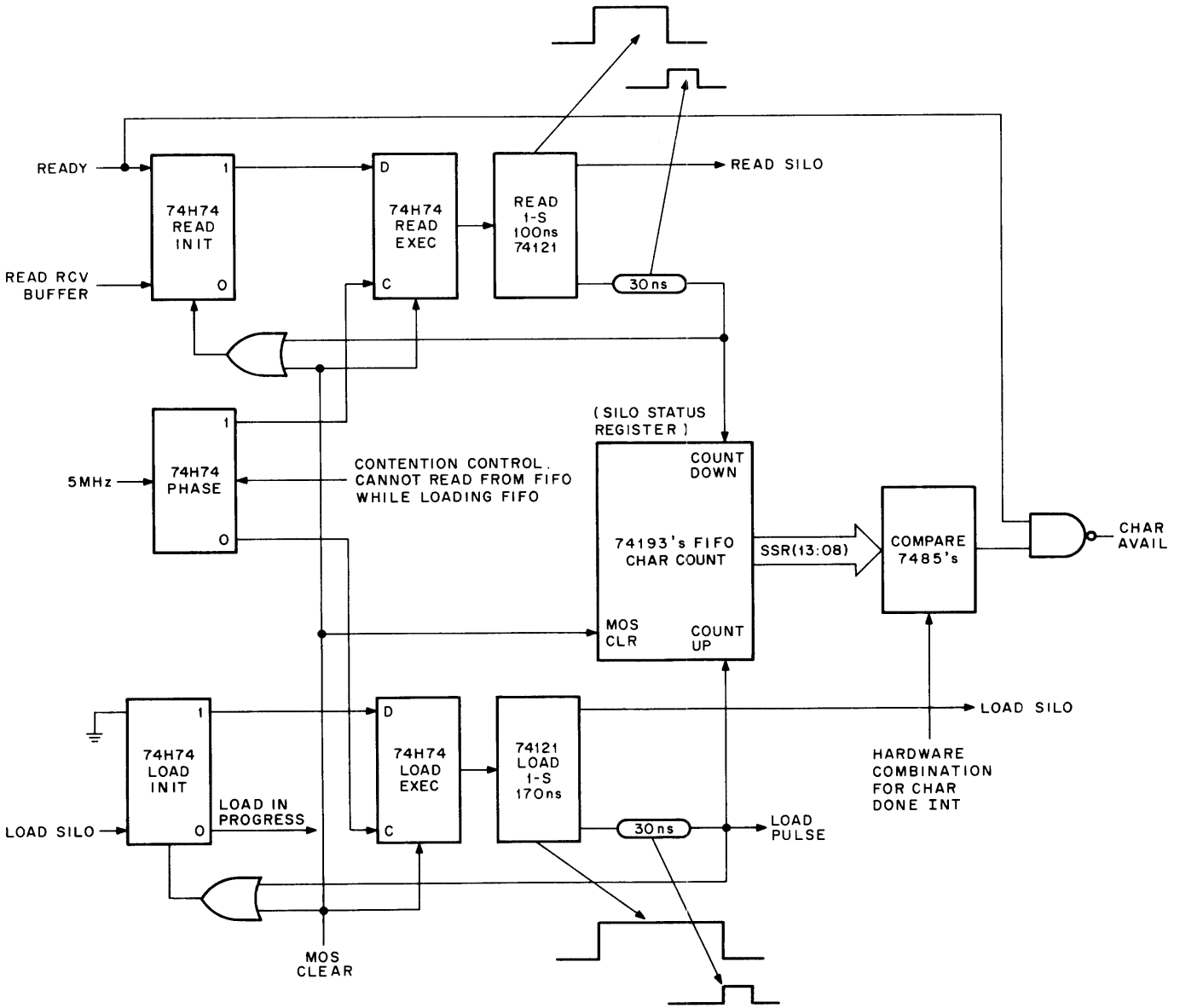


Figure 4-25 FI/FO Buffer Control Block Diagram

When a character is to be loaded into the FI/FO, the Load Silo command is issued and used to clock the LOAD INT flip-flop at E25 (74H74). This is an inverted flip-flop which then enables the LOAD EXEC flip-flop (74H74, E18).

This flip-flop is clocked by the 0 side of the PHASE flip-flop at E25. This is a complementing flip-flop fed by the basic 5-MHz clock signal. Note that it's outputs are arranged to clock either a loading chain *or* a reading chain to avoid any contention problems.

When the LOAD EXEC flip-flop sets, its low 0 side fires a 170-ns one-shot to produce the LOAD SILO signal sent back to sheet 2, where it clocks the data into the FI/FO. Once data is clocked in, the one-shot falls back; but the 30-ns delay on the 0 side of that one-shot is fed back to clear the LOAD INIT flip-flop. This delayed pulse also feeds the FI/FO character counter (74193s) that keeps track of the amount of data in the silo.

These counters are up/down counters that are activated by READ SILO L + 30 ns for down-counting and LOAD PULSE, which is LOAD SILO + 30 ns for up-counting.

The sequence of control for reading out of the FI/FO is identical as shown in the figure except that the initializing flip-flop is enabled by READY and clocked by READ RCV BUFFER. The EXEC flip-flop is clocked by the opposite phase of the PHASE flip-flop which, in this case, fires a 100-ns one-shot for reading. Clearing of the chain and character decrementing are identical.

The two 7485s at the left-hand side of the sheet are used to compare the SSR (Silo Status Register) outputs of the up/down counters with the hardwired combination on its other input. When comparison is found, a CHARACTER AVAILABLE is generated on READY OUT. Based on that preset combination, this signal will either come up on the first character moved, or it will wait until a number of characters have been moved. Normally on a character-for-character basis, the pins are all grounded, but they can be selectively cut to cause comparison on 5, 9, or 17 characters. This provides the delayed CHARACTER DONE INT feature described in Chapter 1.

In operation, read out of the FI/FO is continued until bit 15 is found to be cleared, indicating that the silo has been flushed. The signal MOS CLR is used to clear the FI/FO but it is used merely to clear the flag (bit 15), it does *not* clear any of the information in the FI/FO. However, once cleared in this way, new information can be loaded into the FI/FO, it will propagate down to the last position, overlay the now invalid data that was in that position, and will set bit 15, indicating that that new information is now valid.

4.4.13 TTL Output Interface (D-CS-M5900-0-1)

The M5900 TTL Output Interface Card is shown simplified in Figure 4-26. The 16 receive lines (LINE 15:00 IN) are applied to the normally enabled B inputs of 8266 Multiplexers and fed out as SERIAL IN (15:00) H to the DJ11. The 16 transmit lines [SERIAL OUT (15:00) H] are each ANDed with the fact that the break bit in the TBR for that line is set and thence to the transmit line.

If the MAINT bit is set in the CSR (bit 02), the B inputs of the multiplexers are disabled, preventing reception from the line, and the A inputs are enabled. This provides the loop around feature used by maintenance activities to check out the DJ11.

In the receive case, line signals of 0.8 Vdc (mark) and +2 Vdc (space) are transferred in as +3 Vdc (mark) and ground (space) signals to the DJ11 circuits.

In the transmit case, +3 Vdc (mark) and ground (space) signals are transferred to the line as +2.4 Vdc (mark) and +0.4 Vdc (space) signals to the line.

As can be seen, in maintenance mode the TTL signals are not inverted but are received back as they are transmitted.

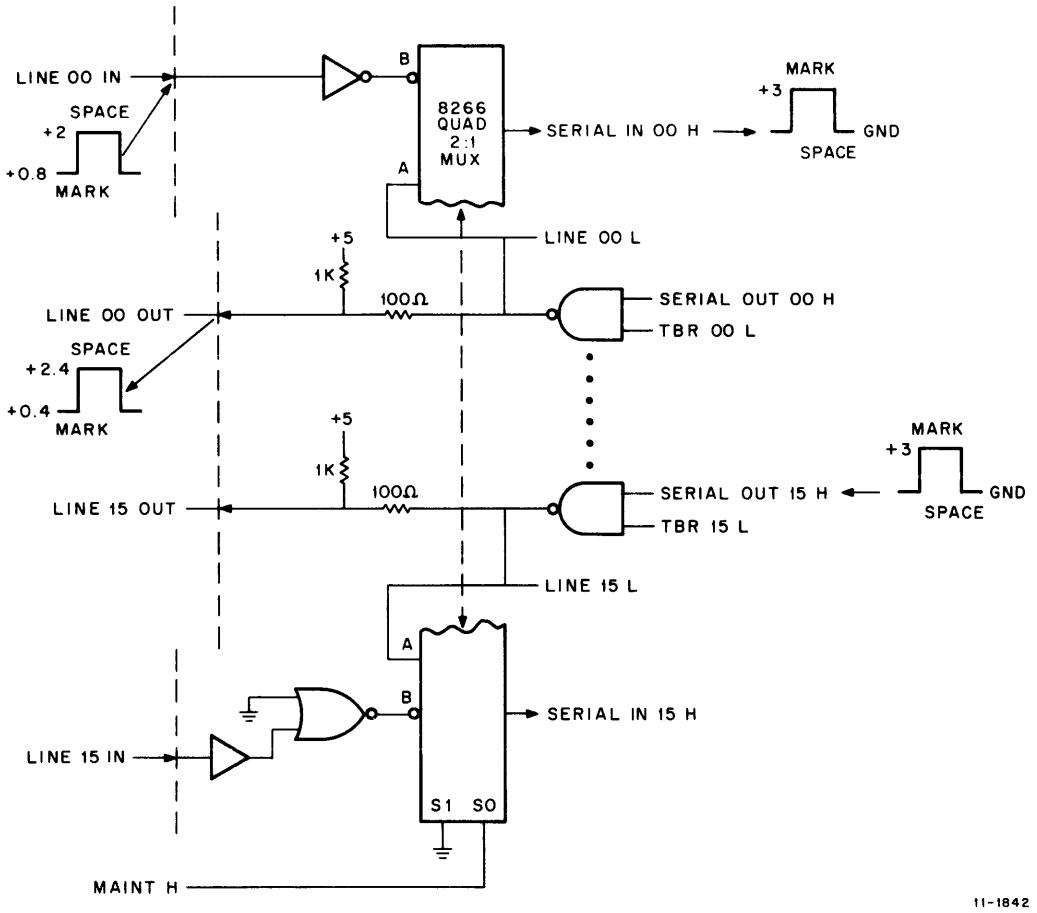


Figure 4-26 M5900 Level Converter Block Diagram

4.4.14 EIA Output Interface (D-CS-M5901-0-1)

The M5901 EIA Output Interface Card is shown in Figure 4-27. The multiplexing arrangement is identical to that of the M5900 with the MAINT bit creating the same loop around feature. The modules make the conversion between standard EIA signals on the lines to signal levels suitable for the DJ11.

In the receive case, line signals between -3 and -15 Vdc (mark), and between +3 and +15 Vdc (space) are transferred in as +3 Vdc (mark) and ground (space) to the DJ11 circuits.

In the transmit case, +3 Vdc (mark) signals and ground (space) signals are converted and transferred to the line as -6 to -15 Vdc marking signals, and +6 to +15 Vdc spacing signals.

4.4.15 TTY Output Interface (D-CS-M5902-0-1)

The M5902 20 mA Current Loop Output Interface Card is shown in Figure 4-28. The multiplexers (8266) are used to provide the maintenance feature described for all of these cards.

The card uses an opti-coupler on the receiver side to provide the total line isolation required. The coupler (Ex) comprises a light-emitting diode, that is excited by signals on the line, to activate a light-sensitive transistor feeding a transistor buffer (Qx). The resultant signals are fed to the B inputs of the line multiplexers (8266 2:1). On the transmit side the signals are transistor-coupled to the line.

In the receive case, 20 mA (mark) and no current (space) signals are converted to the standard +3 Vdc mark and ground space in the DJ11.

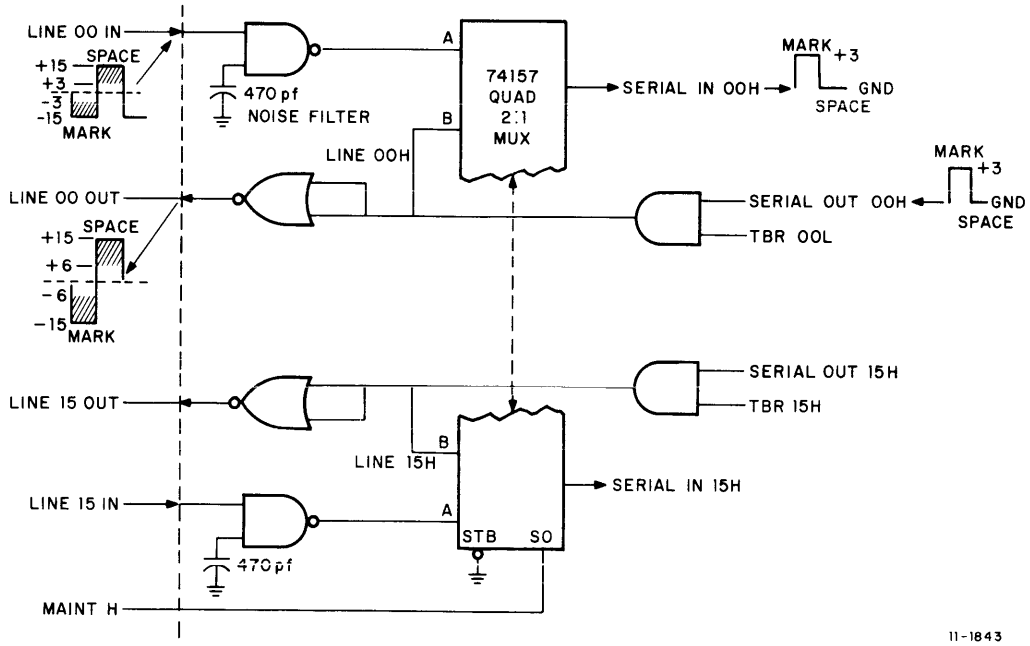


Figure 4-27 M5901 Level Converter Block Diagram

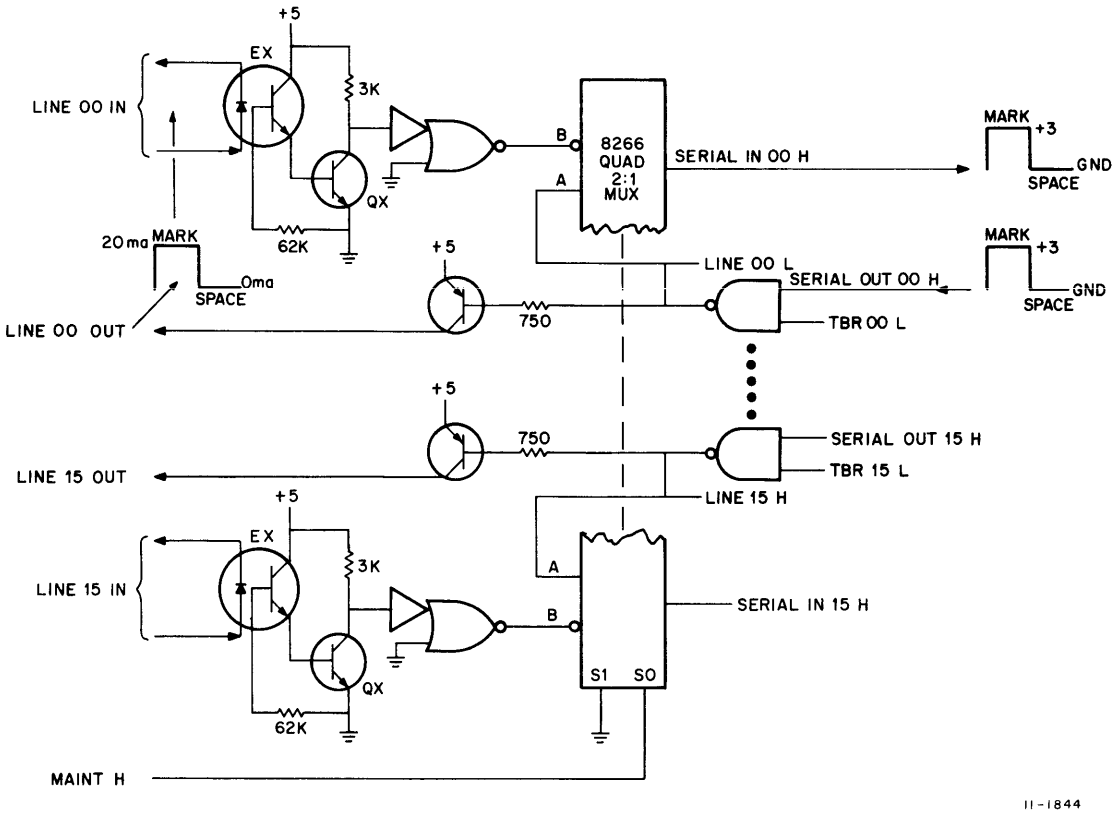


Figure 4-28 M5902 Level Converter Block Diagram

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

DJ11 maintenance philosophy is based on the premise that an optimum amount of preventive procedures, performed regularly, can eliminate many costly equipment breakdowns and forecast failures before they occur. The design is such that, in the event a specific item fails, module replacement can restore the equipment to service in a minimum of time.

In the event that a module is found to be faulty, a module should be substituted from spares (Table 5-1) and the faulty module returned to DEC for repair. Depot repair facilities have been located strategically throughout the world to enable users of DEC equipment to receive prompt, efficient service. At the user's option, a national transportation firm, contracted by DEC, can be used to route equipment to and from the depot facility.

Table 5-1
List of Recommended Spares

Module	Quantity		
	AA	AB	AC
M7285	1	1	1
M5900	0	1	0
M5901	1	0	0
M5902	0	0	1
M7280	2	2	2
M7821	1	1	1
M105	1	1	1
M7279	1	1	1

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of running diagnostics, visual inspection, operational checks, adjustment, and replacement of marginal components.

The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Normally, preventive maintenance consists of inspection and cleaning every 600 hours of operation or every 4 months, whichever occurs first. For extreme conditions of temperature, humidity, or dust, and with abnormally heavy work loads, more frequent maintenance may be necessary. It is recommended that the exerciser tests, part of the diagnostic for the DJ11, MAINDEC-11-DZDJB-A-PB, be run once a week as part of the normal preventive maintenance schedule.

5.2.1 Mechanical Checks

Periodically inspect the DJ11 and it's distribution panel for general condition. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Check all modules to see that they are properly seated. Check seating of EIA plugs in H317B. Check security of connections at screw terminals of H317A. Tape, solder, or replace any defective wiring or cable covering.

5.2.2 Test Equipment Required

Maintenance activities for the DJ11 require the standard test equipment and diagnostic programs listed in Table 5-2, in addition to standard hand tools, cleaners, test cables, and probes. Special test equipment required for any adjustments are given as part of that procedure.

Table 5-2
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 454 or better
Module Extenders	DEC	W982 (Single) W984 (Double) W989 (Quad) **NOTE** **For Hex Boards use a quad and a double.**
Diagnostic Self-Test Routines	DEC	MAINDEC-11-DZDJA-A-PB (tape) MAINDEC-11-DZDJA-A-D (abst) MAINDEC-11-DZDJB-A-PB (tape) MAINDEC-11-DZDJB-A-D (abst)

5.3 CORRECTIVE MAINTENANCE

The procedures that follow are based on standard troubleshooting techniques. Once the defective module has been located, replace it with a spare module and return the defective module to DEC for repair or replacement.

5.3.1 General Corrective Procedures

Before beginning troubleshooting procedures, ensure that the equipment external to the DJ11 is operating correctly. Refer to the pertinent maintenance manuals for procedures. Also examine the DJ11 Maintenance Log to determine if the fault has occurred before and, if so, note what steps were taken to correct the condition.

NOTE
A recurring fault can indicate a common uncorrected fault elsewhere.

Visually inspect the physical and electrical security of all cables, connectors, modules, and wiring. In particular, check the security of ground connections between racks. Faulty grounds can produce a variety of faults.

5.3.2 Diagnostic Testing

DEC provides special diagnostic programs (MAINDECs) to assist in localizing faults within the equipment. Functionally, the programs fall into two categories: test and reliability. Test programs isolate genuine go/no-go type hardware failures that are more easily recognizable; reliability programs isolate failures that are difficult to detect because they are marginal and occur infrequently or sporadically.

The family of test programs are written so that, when run successfully, they test the equipment beginning with small portions of the hardware then gradually expand until they involve the entire machine. To accomplish this, they are built around instructions and portions of instructions whose demands on equipment capabilities progress from simple operations to the most involved manipulations. As portions of the system are proven operable, they become available to succeeding tests for use in checking unproven portions of the machine.

There are two MAINDECs for the DJ11, MAINDEC-11-DZDJA-A-PB (Logic Tests) and MAINDEC-11-DZDJB-A-PB (Exerciser and On-Line Tests).

The Logic Tests diagnose problems with the DJ11 in maintenance mode. They check that all the control registers function properly, that interrupts occur at the right level, and that data can be transmitted and received correctly. Note that this set of programs does *not* test if the input and output leads are functioning.

The various tests within this diagnostic are listed in Table 5-3, together with the fault they find and the board location of the component that is probably producing that fault.

This diagnostic will test up to 16 DJ11s. Each subtest is run 16 times before continuing to the next. To run each test only once, set SW(11) to 1. To loop on an error, set SW(9) to 1. To loop on any subtest, set the test number in the right-hand byte of the switch register, and set SW(8) to 1. The test will continue to loop until either the test number is changed or SW(8) is set to 0. The program will run as usual on a nonexistent test. When testing more than one DJ11, if multiple DJ11s are selected, this diagnostic performs all tests on one DJ11 at a time. The bell will ring when the first DJ11 tests are complete and before the second DJ11 tests are started. Each test can be Power Fail tested without errors. At any time, a power down followed by a power up will cause the routine to type "POWER" and then restart with no other error printouts.

This test uses memory locations 0 to 17500. It should always be started at location 200 and can be restarted at location 1000 after parameters have been set. To load, use standard procedure for ABS tapes.

Worst-case testing is with all switches down. Refer to Diagnostic Abstract for further information.

A Scope subroutine call (via a Trap instruction) is placed between each subtest in the instruction section. It records the starting address of each subtest as it is being entered in location "LAD". If a scope loop is requested, the current subtest will be looped upon. SW(11) on a 1 inhibits iteration of subtests. The contents of "LAD" may be used to determine the last subtest successfully completed.

A HLT routine (called by an EMT instruction) prints out an error message. If SW(9) is on a 1 and an HLT is executed, the subtest will be looped upon until 16 consecutive good passes are completed. To inhibit typeouts, put SW(13) on a 1. To ring the bell on an error, put SW(10) on a 1.

Table 5-3
DJ11 Diagnostic Logic Tests and Fault Location

Test No.	Test Description	Probable Fault	Dwg.	Comp. Loca.
1	Tests ability to reference CSR without trapping and ability to clear CSR.	M105 M7285	D2-6	E29
2	Tests that CSR 01 can be set and cleared.	M7285	D2-2 D2-4	E25 E7 E47 E64
3	Tests that CSR 02 can be set and cleared.	M7285	D2-2 D2-4	E25 E7 E47 E64
4	Tests that CSR 06 can be set and cleared.	M7285	D2-2 D2-4	E4 E18 E47 E64
5	Tests that CSR 08 can be set and cleared.	M7285	D2-2 D2-4	E6 E18 E47 E31
6	Tests that CSR 10 can be set and cleared.	M7285	D2-2 D2-4	E30 E24 E47 E31
7	Tests that CSR 12 can be set and cleared.	M7285	D2-2 D2-4	E5 E1 E47 E31
10	Tests that CSR 14 can be set and cleared.	M7285	D2-2 D2-4	E3 E1 E47 E31
11	Tests that CSR 00 (Receiver enable) can be set and cleared, and that CSR 03 (MOS CLR) is write only.	M7285	D2-2 D2-8	E26 E36 E7 E24 E17 E14 E15

Table 5-3 (Cont)
DJ11 Diagnostic Logic Tests and Fault Location

Test No.	Test Description	Probable Fault	Dwg.	Comp. Loca.
12	Tests that CSR responds properly to byte commands.	M7285	D2-4	E47
13	Tests that BIS and BIC instructions set and clear R/W bits of CSR.	M7285	D2-4	E47
14	Tests that TCR is R/W.	M7285	D2-2 D2-3	A11 E8 E20 E21 E43 E41
15	Tests that TCR responds properly to byte commands.	M7285	D2-3	E41
16	Tests that the BIS and BIC instructions set and clear TCR R/W bits.	M7285	D2-3	E41
17	Tests that CSR 15 (Transmit Ready) sets and clears when TCR 00 is set and cleared, and that proper line number (0) appears in TBUF.	M7285	D2-5 D2-6 D2-2	A11 E23 E32 E33 E49 E3 E1
20	Tests that CSR 15 (Transmit Ready) sets and clears when each TCR bit is set and cleared, and that proper line number appears in TBUF.	M7285	D2-5 D2-6 D2-2	A11 E23 E32 E33 E49 E3 E1
21	Tests that CSR 08 (TRAN SCAN ENABLE) on (0) disables CSR 15 (Transmitter Ready) when TCR bit, line 0, is set.	M7285	D2-6	E49 E23 E32 E33
22	Tests that interrupt does not occur at level 7.	M7821 (Jumper wiring and proper parity chip)		
23	Tests that interrupt does not occur at level 6.	M7821 (Jumper wiring and proper parity chip)		
24	Tests that interrupt does not occur at level 5.	M7821 (Jumper wiring and proper parity chip)		

Table 5-3 (Cont)
DJ11 Diagnostic Logic Tests and Fault Location

Test No.	Test Description	Probable Fault	Dwg.	Comp. Loca.
25	Tests that interrupt does occur at level 4.	M7821 (Jumper wiring and proper parity chip)		
26	Tests that interrupt does occur at level 3.	M7821 (Jumper wiring and proper parity chip)		
27	Tests that interrupt does occur at level 2.	M7821 (Jumper wiring and proper parity chip)		
30	Tests that interrupt does occur at level 1.	M7821 (Jumper wiring and proper parity chip)		
31	Tests that interrupt does occur at level 0.	M7821 (Jumper wiring and proper parity chip)		
32	Tests that line 0 can transmit and receive a character (377). 1$: checks that DONE sets in a reasonable time. 2$: checks that valid data (CHAR PRESENT) is in FI/FO. 3$: checks that no errors are in FI/FO. 4$: checks that right line no. (0) is in FI/FO. 5$: checks that character length is right. 6$: checks that correct data received. 7$: checks that CHAR PRESENT clears. 8$: checks that DONE clears.	M7285 M7279	D2-7	A11 A11
33 thru 51	Tests that lines 1 through 15 can transmit and receive a character (377), in similar fashion to above.	(Same as above)		

Table 5-3 (Cont)
DJ11 Diagnostic Logic Tests and Fault Location

Test No.	Test Description	Probable Fault	Dwg.	Comp. Loca.
52	Tests that RBUF 15 Valid Data (CHAR PRESENT) is cleared by CLR MOS.	M7285	D2-8	E17 E14 E15
		M7279		A11
		M7280		A11
53	Test that Transmitter Ready clears when TBUF is loaded. **NOTE** **Because UART is double-buffered, load two characters to insure seeing Transmitter Ready Clear.**	M7285	D2-6	E39 E23 E49
54	Tests that Receiver Enable on a 0 inhibits DONE and Character Present.	M7285	D2-7	E32 E15
55	Test that CSR 01 (H/D Select) disables receiver UARTs.	M7285	D2-4	E32 E17 E22
			D2-2	E5 E1
56	Tests that Receiver Interrupt does not occur at level 5.	M7281 (Jumper wiring and proper parity chip)		
57	Tests that Receiver Interrupt does occur at level 4.	M7281 (Jumper wiring and proper parity chip)		
60	Tests FI/FO Overrun. Note the FI/FO should hold 64 characters.	M7285	D1-7	E32 E17 E22
			D2-2	E5 E1
60A	Tests that FI/FO comes up when 65th character is received without reading FI/FO.			
60B	Tests that reading the receiver buffer causes FI/FO overrun to clear. **NOTE** **Because of FI/FO timing, overrun can come up after reading one character, so a second must be read to insure that FI/FO overrun is clear.**			

Table 5-3 (Cont)
DJ11 Diagnostic Logic Tests and Fault Location

Test No.	Test Description	Probable Fault	Dwg.	Comp. Loca.
60C	Tests that FI/FO overrun interrupt doesn't occur when the processor is at level 5.			
60D	Tests that FI/FO overrun interrupt does occur when processor is at level 4.			
61	Tests that UART overrun is detected on all lines.	M7285 M7279 M7280	D2-2	E3 E1 A11 A11
62	Tests that BCSR bits are R/W.	M7285	D2-2 D2-3	E5 E1 E16 E2 E19 E35
63	Tests that line 0 can transmit and receive a break, and checks RBUF 13 (framing error) and RBUF 12 (parity error) if odd parity selected.	M7285	D2-2 D2-3	E5 E1 E16 E2 E19 E35
64	Tests each line as in test 63.		(Same as above)	
65	Tests that RESET clears all buffers. **NOTE** **Only CHARACTER PRESENT (bit 15) is cleared.**	M7285	D2-8	E13
66	Sends a binary count pattern on each line.		(Anywhere)	

The error message printout is in the following format:

ADR DJADR (R1) (R2) (R3) (R4)

where:

ADR is the address of error HLT
DJADR is the CSR address of DJ11 under test
(Rn) is the contents of general register "n".

NOTE

From none to four of these register contents will be typed depending on the number following the HLT; e.g., "HLT+3" would type (R1 through R3), whereas "HLT" would stop after ADR and DJADR.

To find the failing test, look at the listing above the address typed. In most cases the comment beside the HLT indicates what logic was checked and what result was expected. Table 5-3 gives possible starting points in the determination of probable failing logic. Refer also to Figures 5-1 and 5-2, that provide signal flow information for maintenance purposes and aid in troubleshooting.

To recover from an error, restart test at location 200 or 1000. An error count is kept in ERRORS, location 1202. This count can be cleared from the console by restarting at 200 or by reloading the program.

Note that this diagnostic is configuration independent.

The Exerciser and ON-Line tests comprise three subprograms that exercise up to 16 DJ11s.

NOTE

ACT11 and DDP monitors will run only Program 1 of this diagnostic.

Program 1 is an off-line exerciser that operates on up to 16 lines simultaneously in maintenance mode. Three different data patterns, selectable from the switch register, are repeated a minimum of 16 times for each pass. The program should be run for at least 2 passes with all switches down. SW(9) on a 1 disables the maintenance mode, requiring turn-around cards at the termination of each line being tested. This simultaneous feature, however, is not always available in the field as only one turn-around card is supplied with the option.

CAUTION

When using the Exerciser Program in non-maintenance mode on either the DJ11-AB or DJ11-AC options, a single error message will be reported for all unselected lines. These messages can be ignored. This is explained below. Refer to print D-IC-DJ11-0-10 for notes on termination of unused lines.

The DJ11-AB uses an M5900 Interface Module and the DJ11-AC uses an M5902. When unterminated lines are connected to these boards, they input a space causing the UART to assemble a break character and then dump it into the FI/FO. The program will then see a character from an unselected line and print out an error message. Only one message will be printed for each unterminated line so long as that spacing condition continues. This does not occur on the DJ11-AA since the M5901 module inputs a mark for unterminated lines.

Program 2 is an On-Line Continuous Echo Exerciser that continuously transmits the last character received on the respective line. A null (000) will echo 72 times and then turn off the transmitter. This program is operator dependent, it will not loop. Program 3 is an On-Line Echo Test that first transmits the text heading "Echo Test" and then echoes everything that it receives.

CAUTION

On Program 3, if characters are received faster than they are transmitted, software buffers may overflow.

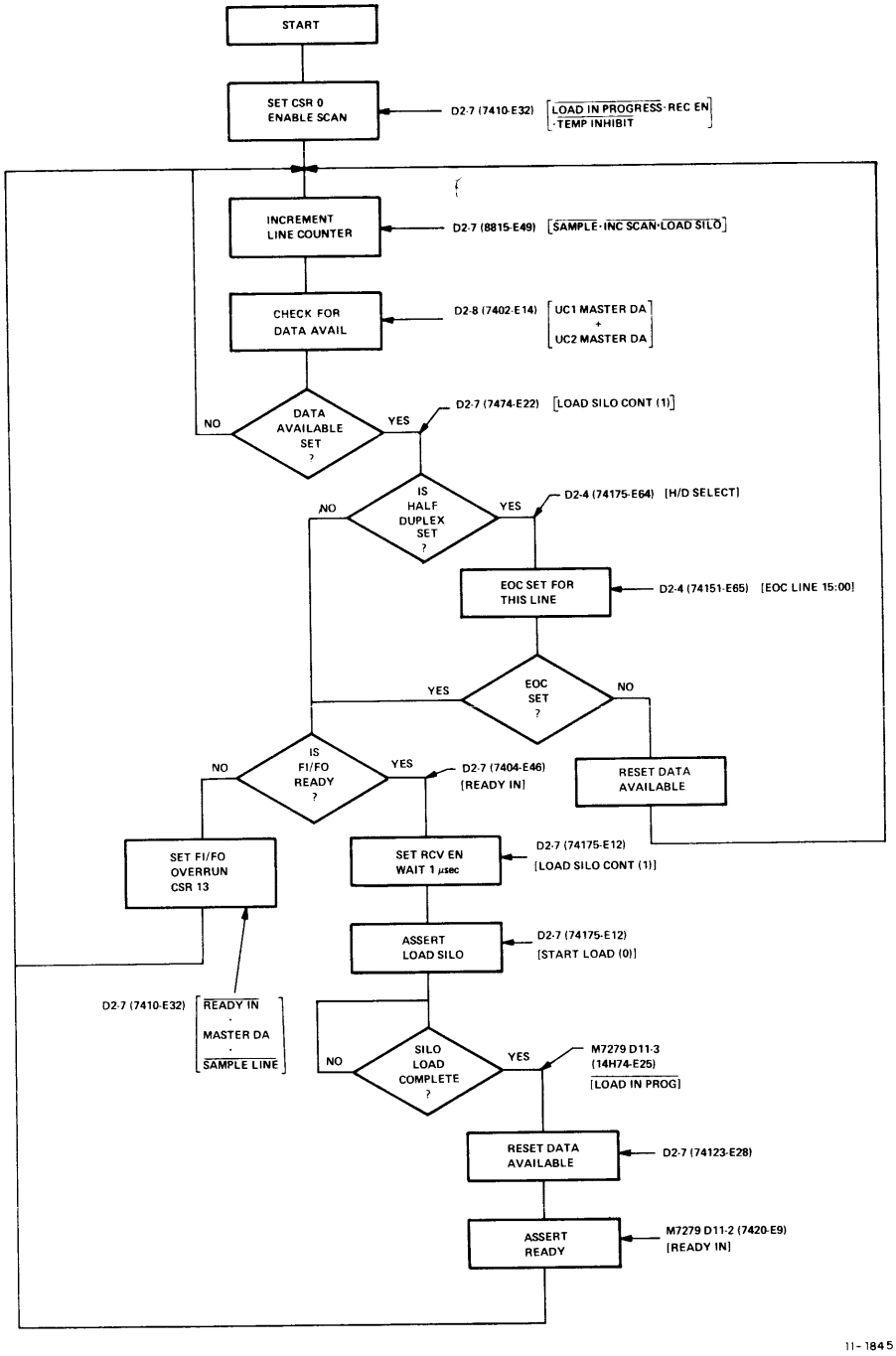


Figure 5-1 DJ11 Receiver, Maintenance Flow Diagram

Program 3 is also operator dependent. It is loaded with the standard ABS tape procedures. For worst-case testing, set all switches down. The program should be started at 200 but may be restarted at 1000. For Program 1 only, the bell will ring upon completion of a pass of the entire program, and alternate passes will run with T bit set. To set the T bit, put SW(12) on a 0. When T is set, the processor traps after each instruction.

HLT operation and Error Printout Format are the same as the logic test diagnostic. For more information, refer to the Diagnostic Abstract.

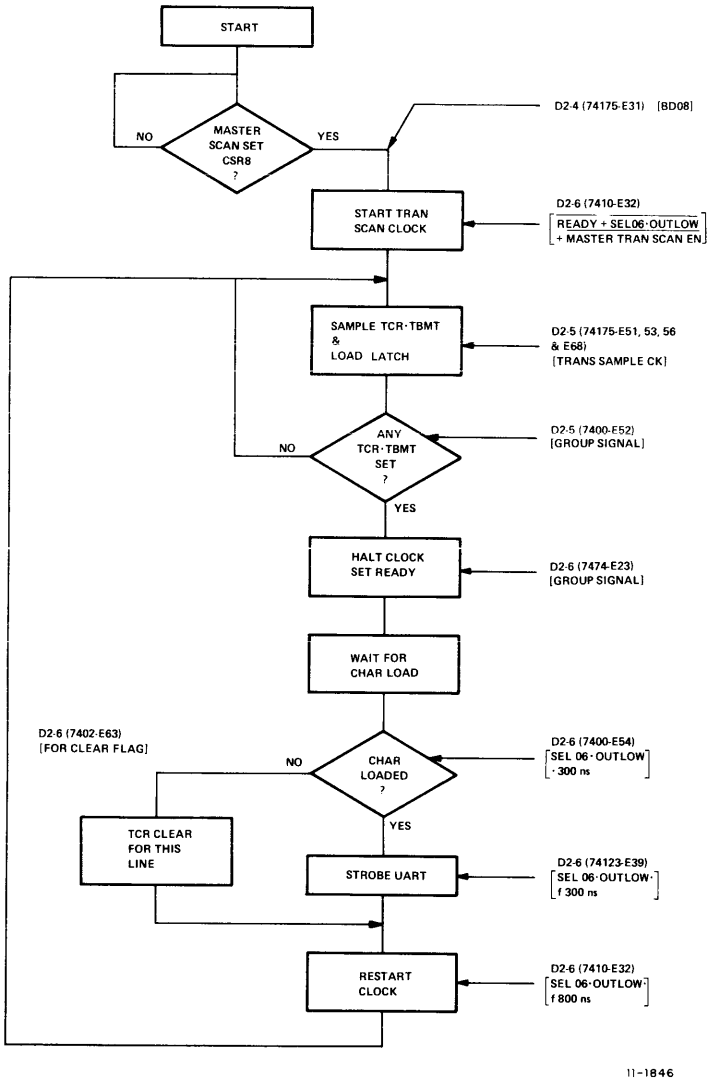


Figure 5-2 DJ11 Transmitter, Maintenance Flow Diagram

5.4 DJ11 TEST PROCEDURE

This procedure is in two parts: a) verifies the internal logic in maintenance mode, and b) checks the unit output interface logic by driving signals to a terminal or by looping signals beyond the output interface card. For maintenance procedures, only those lines in question can be tested. For initial checkout, *all* lines should be checked.

5.4.1 Logic Verification DJ11-AA, AB, AC

For this procedure, the output cables need not be connected to the M5900, M5901, or M5902 Output Interface Card. All speeds should be strapped to 9.6 kbaud (split lug no. 3) to shorten test time.

1. Using the scope, verify that the pulse trains listed below exist at all split lugs from 1 through 11.

NOTE

They will not all be square waves. Do not verify frequency tolerance. They are all crystal controlled and will be more accurate than any scope measurement.

Lug No.	Period (μs)
1	26
2	13
3	6.5
4	34.8
5	104
6	208
7	416
8	832
9	52
10	566
11	465

If any signals are not present, check divider chain on M7285, sheet D2-9.

2. Load logic test (DZDJA-A-PB). Refer to document for startup procedure.

3. Run unit for 5 minutes. If errors occur, refer to Paragraph 5.4.5 for more information. Also, check the diagnostic document for hints in troubleshooting. Use Table 5-3 as a guide in locating the probable fault. Once the fault has been located, rerun exerciser for at least two passes to verify fault correction.

NOTE
Proceed to proper test below for configuration being tested.

5.4.2 Interface Check DJ11-AA

This is the EIA version of the DJ11. In addition to regular test equipment, this test requires an EIA terminal, such as a VT05 and a BC05 cable, plus an H312 Null Modem. In addition, an H315 Test Connector is required.

1. With the unit still set for 9.6 kbaud, attach the H317B Distribution Panel to the M5901 card using the two BC08S-15 cables supplied. These cables must be carefully polarized. Refer to Figure 2-3 for instructions.

2. Add the H315 Test Connector to the first line to be tested.

3. Load exerciser tape DZDJB-A-PB, select the first line to be tested, and run one pass of Program 1 in standard configuration.

4. Run one pass of Program 1 with SW(9) up.

NOTE
This forces test to run in non-maintenance mode, and shows up cable problems along with problems with H317B and/or M5901.

5. Repeat steps 1 through 4 for each of the other lines to be tested, resetting the test connector, resetting the program, and reselecting the appropriate line each time.

6. Strap DJ11 to 2400 baud (lug 1) and set VT05 accordingly. Attach VT05 to first line to be tested using VT05 cable and an H312 Null Modem.

7. Run Program 2 (Echo Test). Hit several keys on keyboard to ensure proper operation.

8. Move cable down a line at a time for each line to be tested, hitting several keys for each line until all questionable lines are verified.

NOTE

The following tests require either a DM11 Distribution Panel or a DC08-CS Telegraph Line System Option. If these are not available, the following tests cannot be performed as described.

5.4.3 Interface Check DJ11-AB

This is the TTL version of the DJ11. In addition to regular test equipment, this test requires a DM11 Distribution Panel (7008443). If this is not available, the lines *can* be looped through a DC08-CS. In this case, proceed to step 6 below.

1. With the unit still set for 9.6 kbaud, attach DJ11 to DM11 Distribution Panel using a single BC08S-15 cable plugged into J1 connector of M5900 at one end, and the M971 plugged into slot B1 of 7008443 assembly at the other end. Be careful to observe cable polarities. Use the M974 DM11 Test Connector to turn the lines around at the DM11 panel (slot B3).

2. Load exerciser tape DZDJB-A-PB and run one pass of Program 1 in standard configuration.

3. Run one pass of Program 1 with SW(9) up.

NOTE

This forces test to run in non-maintenance mode, and shows up cable problems along with M5900 problems.

4. Connect BC08S-15 cable to connector J2 and slot B1 of DM11 panel observing proper cable polarities.

5. Run one pass of Program 1 with SW(9) up, plus select only lines 0–7 to run [SW(8) up, see program listing]. This verifies connector J2 on the M5900. This step concludes this test when a DM11 distribution panel is used.

6. If the DJ11-AB is to be tested with a DC08-CS (a current loop telegraph interface), the DJ11 MAINDEC must be run with data looped at the output of the DC08-CS. This unit uses TTL to switch high voltage (60 to 80 Vdc approximately).

CAUTION

Do not wire the DC08-CS Receiver directly to the transmitter or smoke may result. Refer to the DC08 documentation.

7. The only resistance in the circuit when the transmitter is looped to the receiver is 100Ω located in the relay coil. Since the maximum current through the coil is 100 mA, a current limiting resistor must be used between the transmitter and receiver. The value of the resistor is a function of the voltage used with the DC08-CS Interface. A typical resistor value would be 2.2 kΩ, 2W for a 60V battery (refer to Figure 5-3 for pins to jumper).

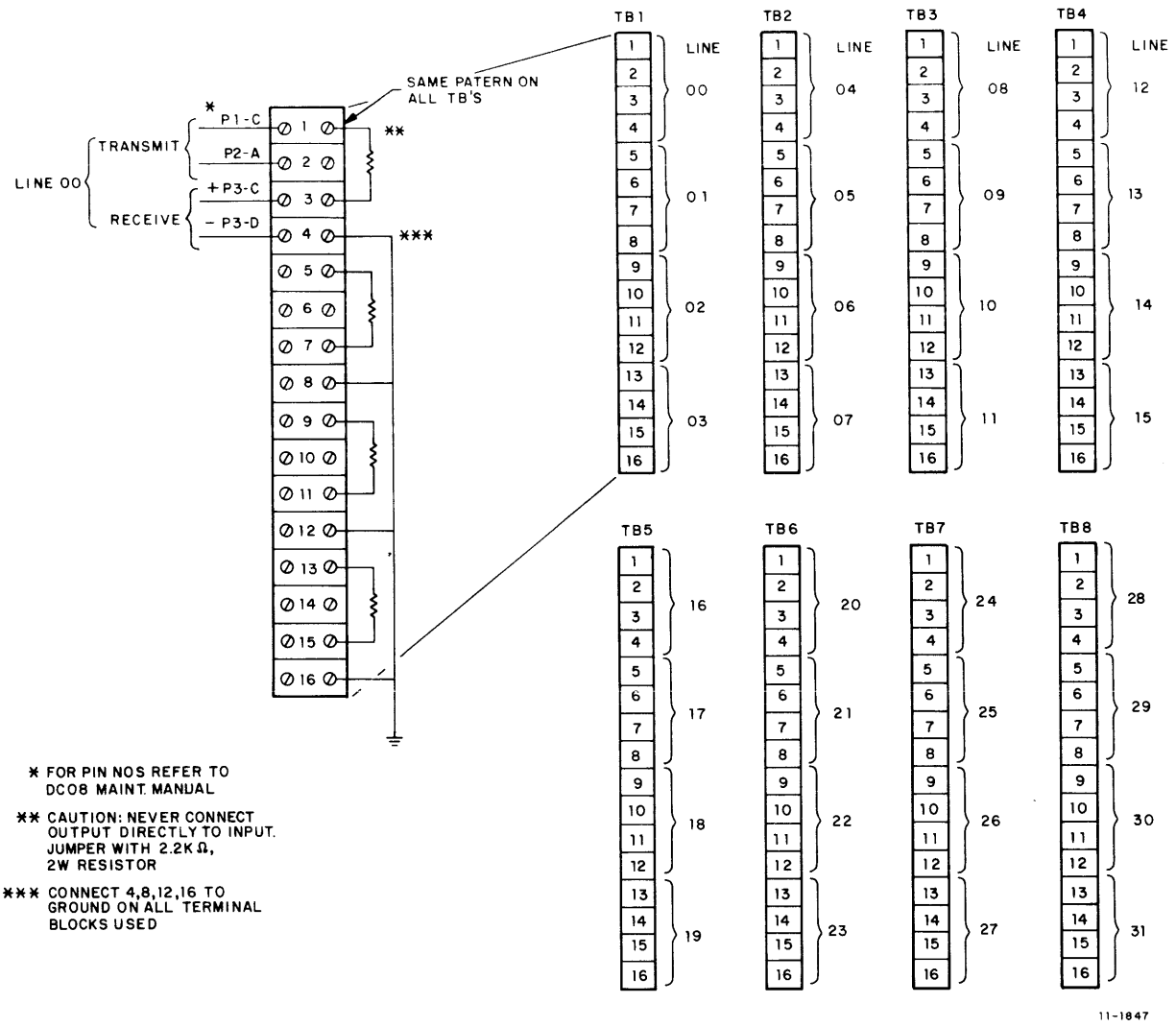


Figure 5-3 DC08-CS Test Jumper Chart

8. When the DC08-CS output terminals have been jumpered (including the limiting resistor), run Exerciser Program no. 1.

NOTE

Test will have no meaning unless SW(9) is on a 1, disabling maintenance mode.

9. Run the diagnostic long enough to ensure that the DC08-CS can pass data. This should be about 15 minutes or 2 passes, whichever occurs first. This concludes this test when a DC08-CS is used.

5.4.4 Interface Check DJ11-AC

This is the 20 mA current loop version of the DJ11. In addition to the regular test equipment, this test requires a special cable assembly (BC04-R, P/N 7006594-0-0 or equivalent) with a Mate-N-Lok connector at one end and screw-type terminals at the other end. In addition, a TTY type terminal, preferably a VT05 set for 2400 baud, is required.

1. Strap DJ11 to 300 baud (lug 6) and connect cables between M5902 and H317A Distribution Panel.

CAUTION

Cables are neither marked nor keyed and, if improperly connected, can damage equipment. On the H317A the rib side of cable must be away from the board. On the M5902, the smooth side of the cable must be away from the board (Figure 2-3).

2. Run Program 1 of DZDJB-A-PB for one pass under standard configuration.

3. Using the special cable, connect the VT05 to line 00 and set the VT05 for 300 baud.

4. Run Program 2 (Echo Test). Hit several keys on keyboard to ensure proper operation. Line 00 must be selected in response to opening program dialogue.

5. Repeat steps 3 and 4 for each line, hitting several keys for each line until all 16 lines are verified. For maintenance purposes, only those lines in question need be verified.

5.4.5 Error Analysis During Test

As explained under diagnostic testing, error typeouts that occur during the logic tests provide the ERROR PC, the CSR address of the faulty DJ11, and other information such as expected data and received data that are a function of the test being run. There are 66 individual routines in the logic program alone. The sections of the logic that these tests check can be grouped into various categories as follows:

Test 1	Checks M105 response.
Tests 2–17	Check all R/W register bits.
Tests 20–22	Check transmitter scanner.
Tests 23–32	Verify the capability of the DJ11 to interrupt and to interrupt at correct level.
Tests 33–52	Do a transmit and receive character check for each line. See description of items checked in program listing.
Tests 53–56	Check various miscellaneous features such as clear MOS bits, half duplex, etc.
Tests 57–60	Check receiver interrupt level.
Test 61	Tests FI/FO overrun bit.
Test 62	Tests UART overrun.
Tests 63–64	Check break operations.
Test 65	Checks reset operation.
Test 66	Does a binary count data check.

These tests are listed in the Diagnostic Abstract. In the listing, references are made to the suspected IC that could be at fault. This information is also listed in Table 5-3. It should be noted that these references are merely the most obvious location of trouble; trouble could exist elsewhere in the logic chain either leading to or from that IC. It will be necessary to trace back or forward through the logic levels to locate the specific faulty component.

When analyzing various problems with the transmitter and receiver sections of the DJ11, several static checks can be made to simplify the troubleshooting process.

To checkout the transmitter section, use the following procedure:

1. Remove both M7280 cards.

2. Set only CSR (08).

3. With the scope, check E33, pin 13, for the clock signal shown in Figure 5-4. Trace the signal through to all destinations (pins 9 of E51, E53, E56, and E68). This verifies that the clock is running and that it is present at all its destinations. At any point that it does not appear, of course, further standard techniques should be followed.

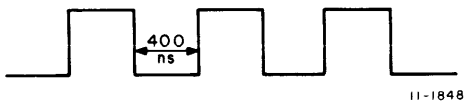


Figure 5-4 Clock Signal

4. Set any TCR bit (register 04).

5. The transmit clock signal, E33 pin 13, should have stopped, and the high byte of TBUF should contain the line number. If the clock has not stopped, check Ready flip-flop E23 or E32. If necessary, trace back from these points to find the fault.

6. If the results of step 5 are correct, the following program should be toggled in to determine if the UART can be loaded with characters.

NOTE

The addresses given are dependent upon which DJ11 in the system is being tested.

```
200 :  MOV # 400, CSR        12737
                             000400
                             160020
       MOV # 100000, TCR     12737
                             100000
                             160024
       TST CSR               005737
                             160020
       BPL .-4               100375
       MOV # 0, TBUF         12737
                             00000
                             160026
       JMP 200               000137
                             000200
```

7. With the above program running, check that pulses appear at E39, pins 5 and 13. The pulse at pin 5 should be 1 μs ±200 ns. The pulse at pin 13 should be 300 ns ±50 ns. This check verifies that the transmit buffers (E9 and E40) are being clocked. If pulses do not appear, troubleshoot further.

8. The above procedure should have verified all transmitter logic on the M7285 card. If the transmitter still does not function, check the M7280 (UART) cards and the M5900/01/02 output interface cards.

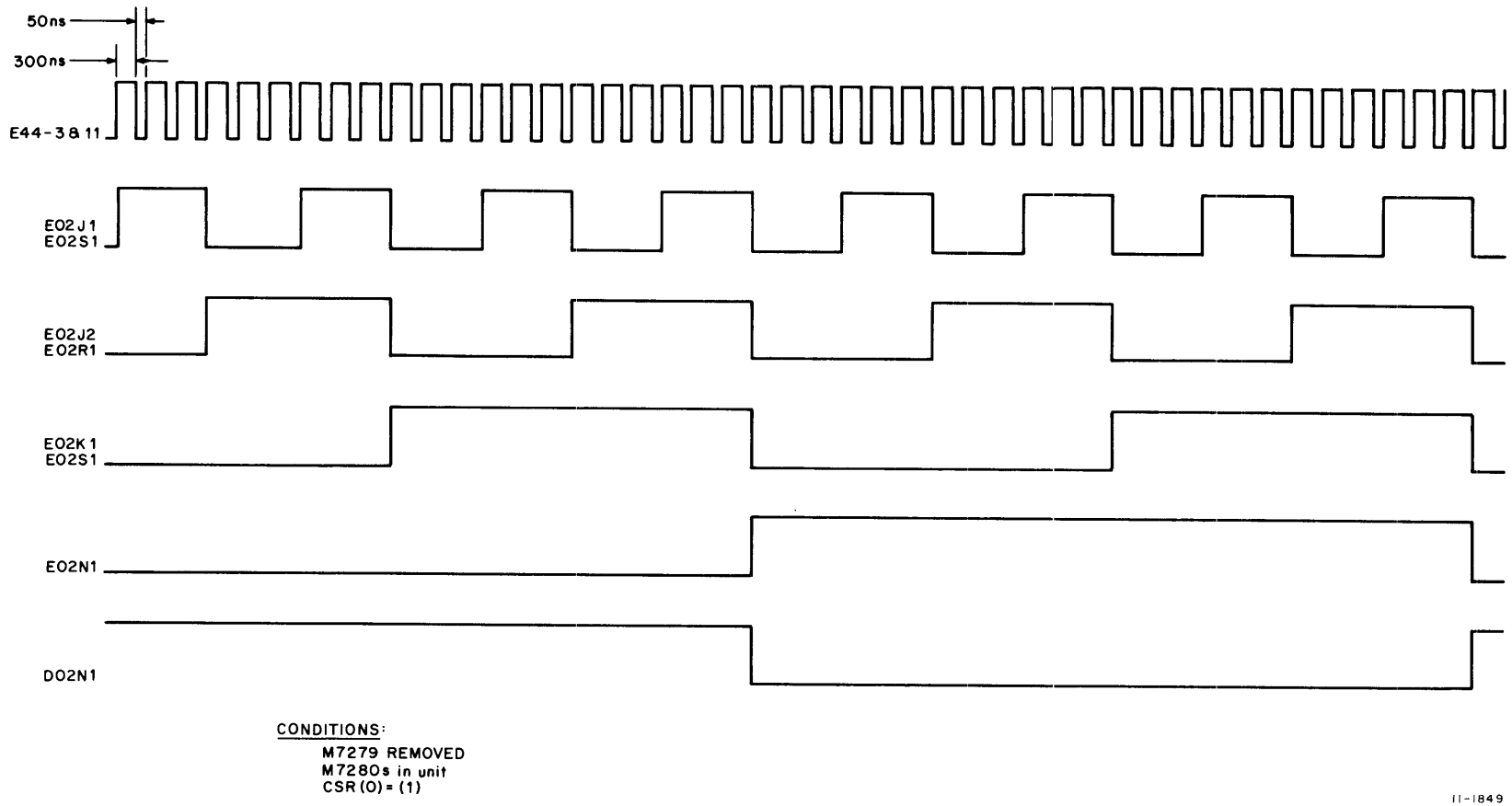


Figure 5-5 Receive Scan Timing, Waveform No. 1

To checkout the receiver section, use the following procedure:

1. Remove silo card M7279 from unit. UART cards are left in unit.

2. Set CSR (00).

3. The pulse train shown in Figure 5-5 should appear at E44 pin 3 and 11. All other signals shown on Figure 5-5 should appear at the pins indicated.

4. Remove both UART cards and jumper pin C2L2 to ground on the back plane. Remove power for this step.

5. Replace power and reset CSR (0). Refer to Figure 5-6 and verify all pulses illustrated. If any signals do not appear, further troubleshooting is required from these points. If all pulses are found and trouble still persists, refer to the schematics on either the M7280 board or the Silo board, M7279.

NOTE

The above procedure has merely verified that the receiver scanner is capable of providing all signals to remove the character from the UART and place it in the silo. It has not verified that data errors have not existed or occurred in those characters.

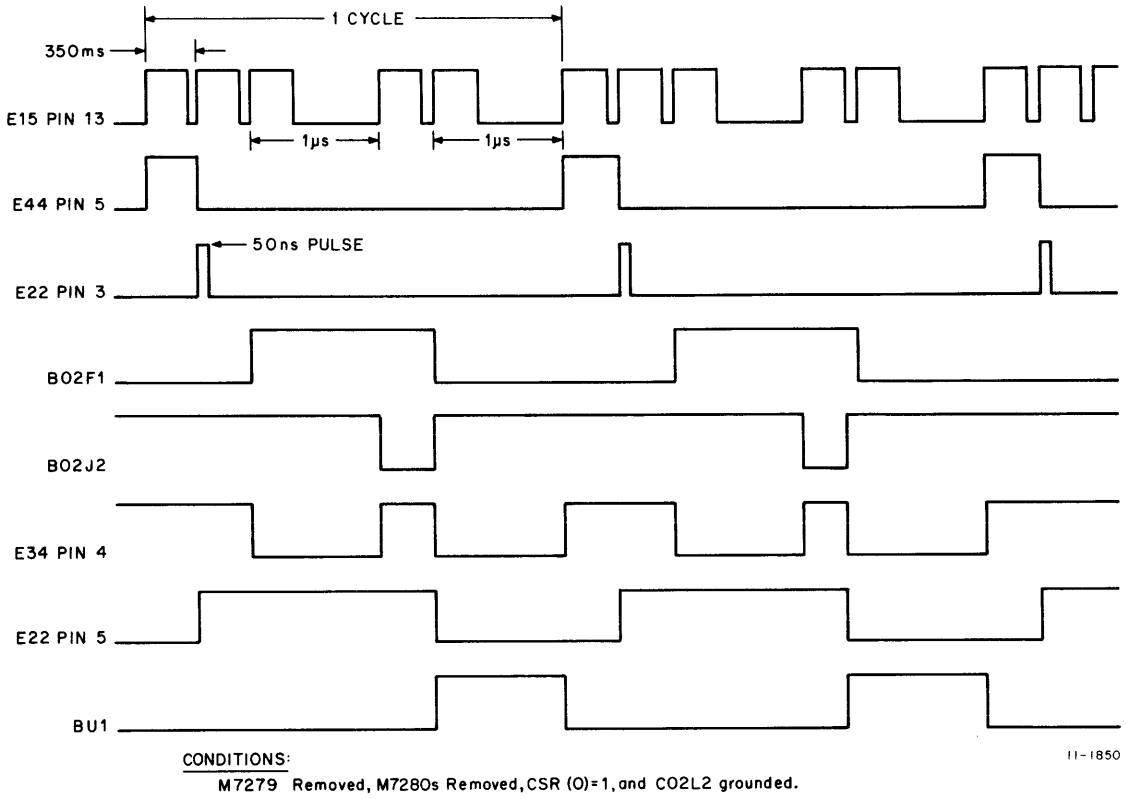


Figure 5-6 Receive Scan Timing, Waveform No. 2

CHAPTER 6
ENGINEERING DRAWINGS

6.1 GENERAL

Table 6-1 contains a brief list of applicable engineering drawings for the DJ11 including those drawings referenced in this manual. For a complete set of engineering drawings, refer to *DJ11 Asynchronous Multiplexer Engineering Drawings.*

Table 6-1
DJ11 Engineering Drawings

Eng. Sketch No.	Eng. Drawing No.	Title
D1-1	D-BS-DJ11-0-7	DJ11 Control Interface
D2-2 thru D2-9	D-CS-M7285-0-1 Sheets 3–10	DJ11 Mux Control Board
D3-2 thru D3-5	D-BS-DJ11-0-3 Sheets 2–5 D-CS-M7280-0-1 Sheets 3–6	Multiple UART Card, Lines 00–07
D4-2 thru D4-5	D-BS-DJ11-0-4 Sheets 2–5 D-CS-M7280-0-1 Sheets 3–6	Multiple UART Card, Lines 08–15
D11-2	D-BS-DJ11-0-6 Sheet 2	FI/FO Buffer
D11-3	D-BS-DJ11-0-6 Sheet 1 D-CS-M7289-0-1 Sheets 1&2	
D33-2	D-CS-M5900-0-1	DJ11 TTL Output Interface

Table 6-1 (Cont)
DJ11 Engineering Drawings

Eng. Sketch No.	Eng. Drawing No.	Title
D33-2	D-CS-M5901-0-1	DJ11 EIA Output Interface
D33-2	D-CS-M5902-0-1	DJ11 TTY Output Interface
–	D-IC-DJ11-0-8 Sheets 1&2	Interconnection Diagram (DJ11-AB)
–	D-IC-DJ11-0-9 Sheets 1&2	Interconnection Diagram (DJ11-AA)
–	D-IC-DJ11-0-10 Sheets 1&2	Interconnection Diagram (DJ11-AC)
D10-1	D-IC-DJ11-0-5	Unibus Connectors
–	D-CS-H315-0-1	Modem Test Connector
–	C-IA-BC08S-0-0	I/O Cable Assembly (Diag Jumper)
–	C-CS-M105-0-1	Address Selector (M105)
–	C-CS-M920-0-1	Internal Bus Connector (M920)
–	D-CS-M7821-0-1	Interrupt Control (M7821)
–	D-CS-M971-0-1	Cable Interface Board no. 2
–	C-IA-7009179-0-0	Wired Assy (DJ11)
–	D-MU-DJ11-0-12	Module Utilization
–	B-DD-H317-0	H317 Cable Box Assy
–	D-UA-DJ11-0-0	Unit Assembly DJ11

APPENDIX A
IC SCHEMATICS

A.1 GENERAL

The DJ11 16-Line Asynchronous Multiplexer uses 21 types of integrated circuit chips (IC). A logic diagram of each, including a packaging diagram with pin number designations and a truth table, is given in this appendix.

The following IC schematics are included:

3341	4-bit X 64-word Propagateable Register (FI/FO)
7474	Dual D-Type Edge-Triggered Flip-Flops
74H74	D-Type Edge-Triggered Flip-Flops
7485	4-Bit Comparator
7490	Frequency Divider
7492	Frequency Divider
7493	Frequency Divider
8266	2-Input 4-Bit Multiplexer
8837	Hex, Unibus Receiver
8838	Quad Bus Transceiver
9305	Frequency Divider
9318	8-Input Priority Encoder
74121	Monostable Multivibrator
74123	Retriggerable Monostable Multivibrator with Clear
74151	8:1 Multiplexer
74153	Dual 4:1 Multiplexer
74155	3:8 Line Decoder
74157	Quad 2:1 Multiplexer
74161	4-Bit Binary Counter
74175	Quad D-Type Flip-Flops
74193	4-Bit Binary Counter

A.2 3341 4-BIT X 64-WORD PROPAGATEABLE REGISTER (FI/FO) (Figure A-1)

The 3341 is a 64-word X 4-bit memory that operates in a first in/first out (FI/FO) mode. Inputs and outputs are completely independent (no common clocks). The device is used in the DJ11 as an asynchronous buffer. When both INPUT READY and SHIFT IN are high, the four bits on D0 through D3 are loaded into the first bit position where they stay until INPUT READY and SHIFT IN go low. This causes the bits to propagate to the second bit position (if empty) where they are propagated to the bottom of the silo by internal control signals.

When data has been transferred to the bottom of the memory, OUTPUT READY goes high indicating the presence of valid data. When both OUTPUT READY and SHIFT OUT are high, data is shifted out of the silo. This causes OUTPUT READY to go low. Data is maintained until both OUTPUT READY and SHIFT OUT are low. At this time the bits in the adjacent upstream cell are transferred into the last cell causing OUTPUT READY to go high again. If the memory has been emptied, OUTPUT READY will stay low.

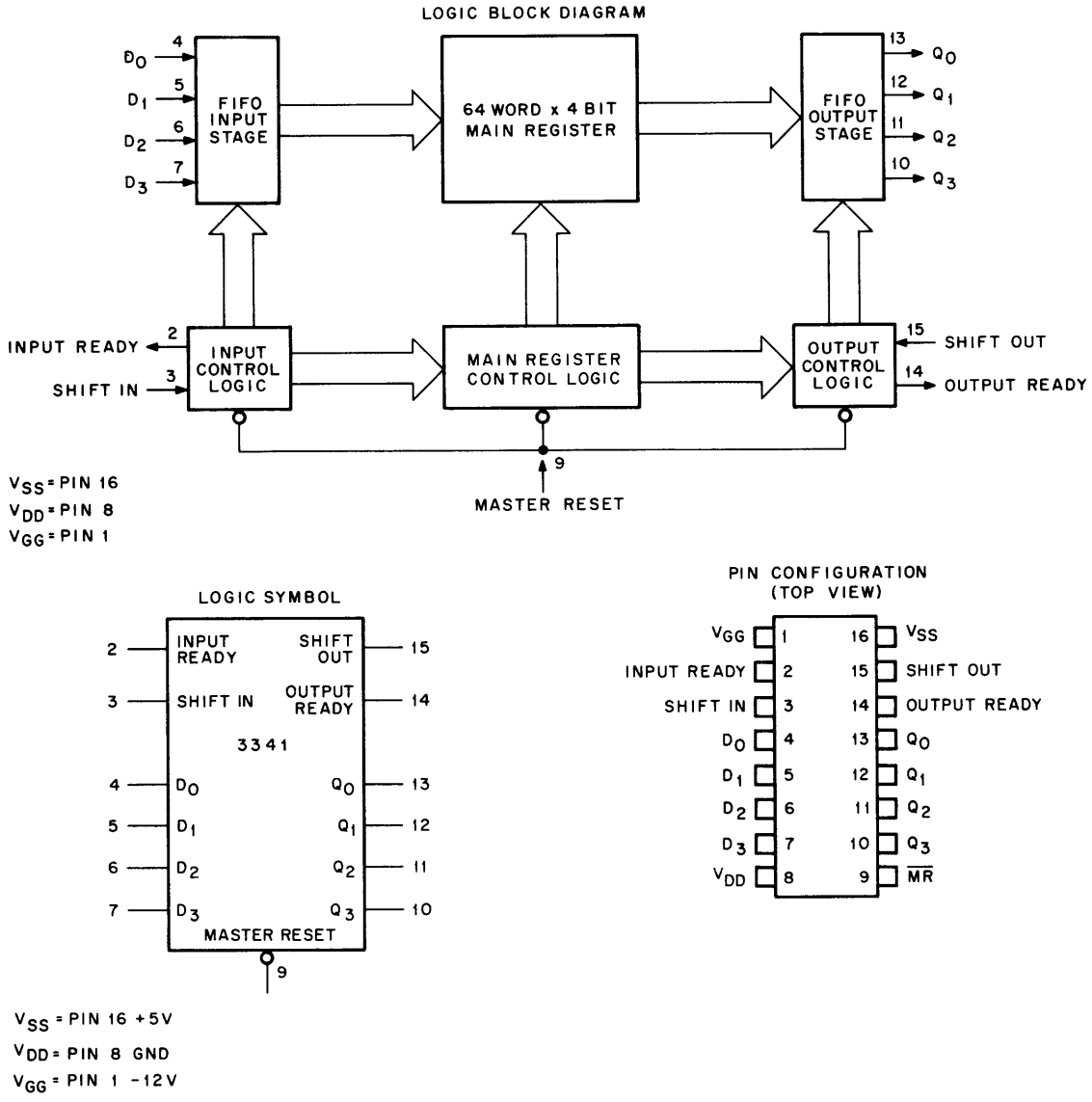


Figure A-1 3341 4-Bit X 64-Word Propagateable Register

A.3 7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS (Figure A-2)

The 7474 consists of two D-type edge-triggered flip-flops. Each flip-flop has individual direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Truth Table (Each Flip-Flop)

t_n	t_n+1	
Input D	Output Q	Output $\overline{Q}$
0	0	1
1	1	0

NOTES:
1. t_n = bit time before clock pulse.
2. t_n+1 = bit time after clock pulse.

Signal/Pin Designations

Signal Name	Circuit no. 1	Circuit no. 2
D	2	12
CLOCK	3	11
CLEAR	1	13
PRESET	4	10
Q	5	9
$\overline{Q}$	6	8

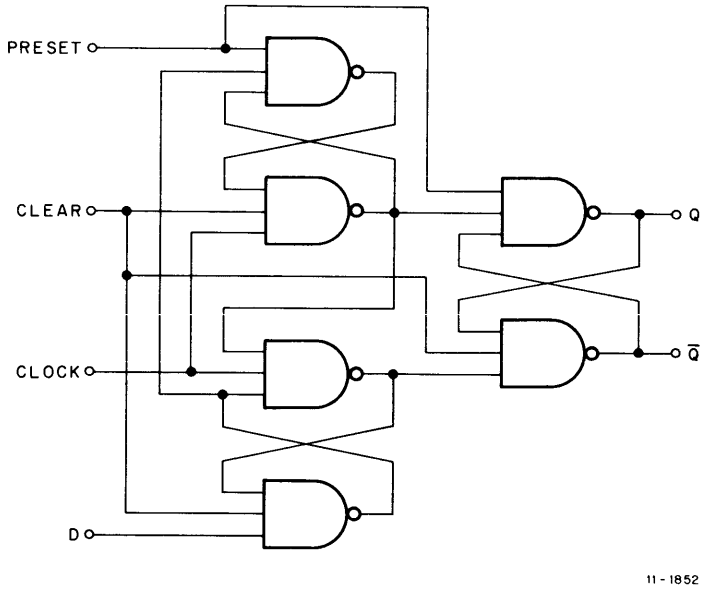


Figure A-2 7474 Dual D-Type Edge-Triggered Flip-Flop

A.4 74H74 D-TYPE EDGE-TRIGGERED FLIP-FLOPS (Figure A-3)

The 74H74 consists of two D-type edge-triggered flip-flops. Each flip-flop has individual clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse.

Truth Table (Each Flip-Flop)

t_n	t_n+1	
Input D	Output Q	Output $\overline{Q}$
L	L	H
H	H	L

H = high level, L = low level

Signal/Pin Designation

Signal Name	Circuit no. 1	Circuit no. 2
D	2	12
CLOCK	3	11
CLEAR	1	13
PRESET	4	10
Q	5	9
$\overline{Q}$	6	8

NOTES: A. t_n = bit time before clock pulse.

B. t_n+1 = bit time after clock pulse.

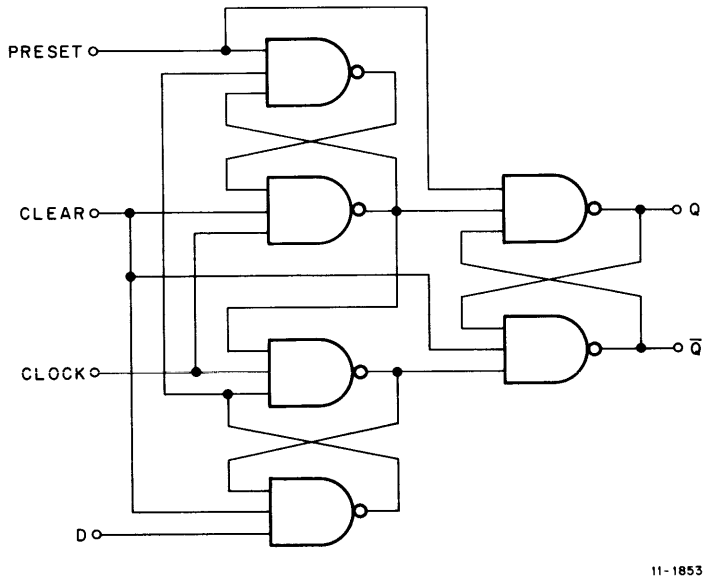


Figure A-3 74H74 D-Type Edge-Triggered Flip-Flops

A.5 7485 4-BIT COMPARATOR (Figure A-4)

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B), about two 4-bit words (A,B), are made and are externally available at three outputs.

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

Signal/Pin Designation

	Signal Name	Pin Designation
Inputs	A0	10
	A1	12
	A2	13
	A3	15
	B0	9
	B1	11
	B2	14
	B3	1
	A < B	2
	A > B	4
	A = B	3
Outputs	A > B	5
	A = B	6
	A < B	7

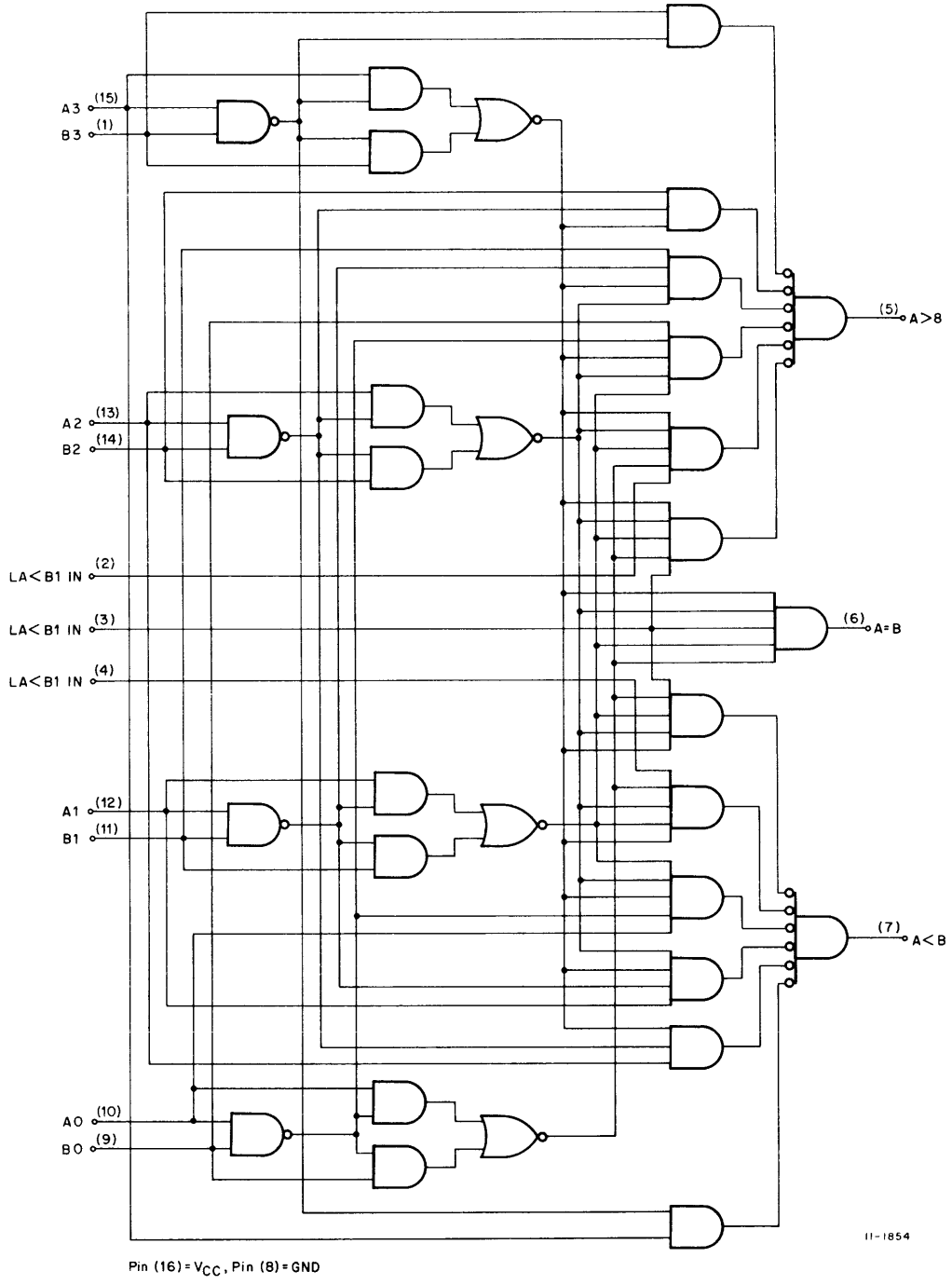


Figure A-4 7485 4-Bit Comparator

A.6 7490 FREQUENCY DIVIDER (Figure A-5)

The 7490 consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines inhibit count inputs and return all outputs to 0 or to a binary coded decimal (BCD) count of 9.

Truth Tables

BCD Count Sequence
(See Note 1)

Count	Output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Reset Count
(See Note 2)

Reset Inputs				Output
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC = No Internal Connection

Notes: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

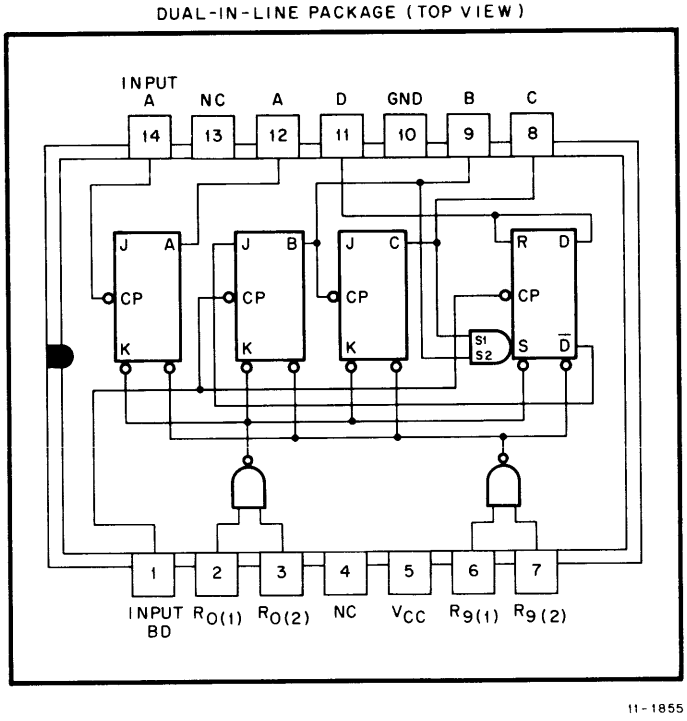


Figure A-5 7490 Frequency Divider

A.7 7492 FREQUENCY DIVIDER (Figure A-6)

The 7492 is a 4-bit binary counter comprising four master-slave flip-flops internally connected to form a divide-by-two and a divide-by-six counter. A gated direct reset line inhibits the count inputs and simultaneously returns the four flip-flop outputs to logical 0.

Truth Table

Count	Outputs			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

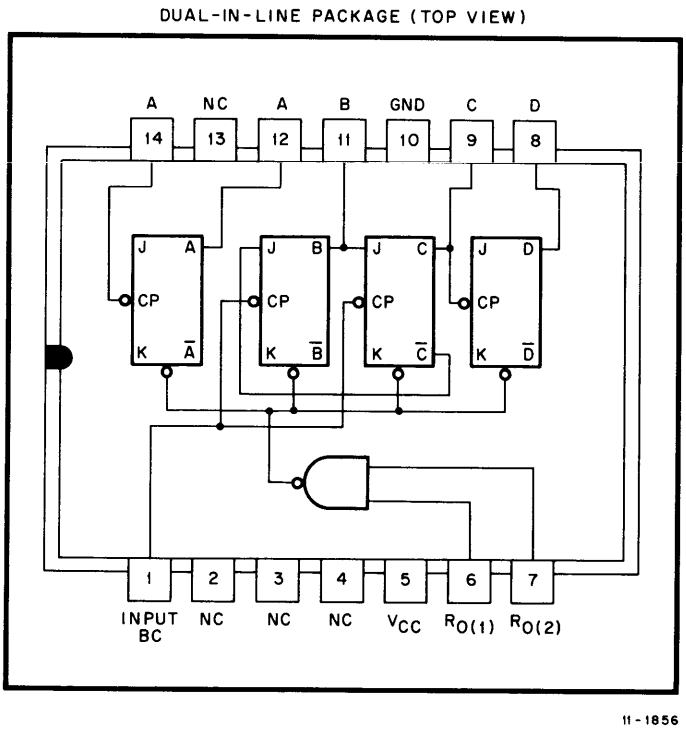


Figure A-6 7492 Frequency Divider

A.8 7493 FREQUENCY DIVIDER (Figure A-7)

The 7493 is a 4-bit binary counter comprising four master-slave flip-flops internally connected to form a divide-by-two and a divide-by-eight counter. A gated direct reset inhibits the count inputs and simultaneously returns the four flip-flop outputs to logical 0.

Truth Table

Count	Output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

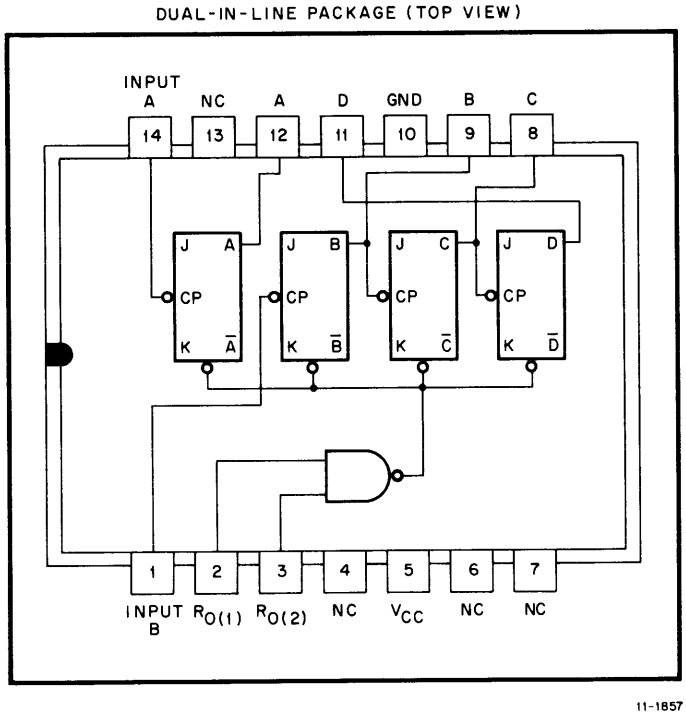


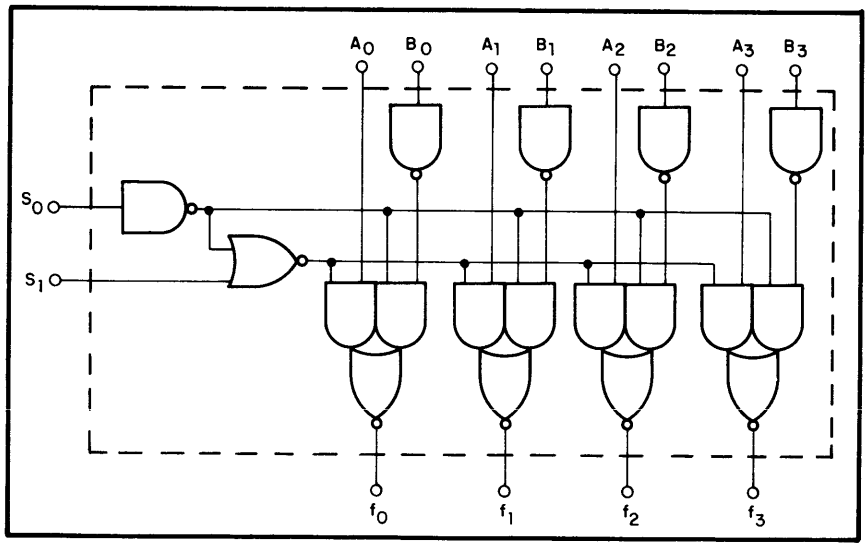
Figure A-7 7493 Frequency Divider

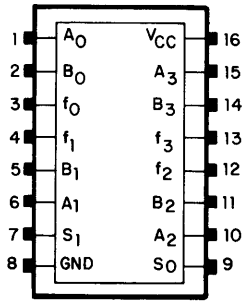
A.9 8266 2-INPUT 4-BIT MULTIPLEXER (Figure A-8)

The 8266 is a 2-input 4-bit digital multiplexer that has the capability of choosing between two different 4-bit input sources as controlled by one selection input while the other input is held to 0.

Truth Table

Select Lines		Output
S_0	S_1	f_n (0,1,2,3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1





11-1858

Figure A-8 8266 2-Input 4-Bit Multiplexer

A.10 8837 HEX UNIBUS RECEIVER (Figure A-9)

The 8837 consists of six inverters whose inputs have Unibus characteristics with common enable on sets of three. When the strobe disables the receivers, all outputs are forced low.

Signal/Pin Designations

Signal Name	Pin Designation
IN 1	1
IN 2	3
IN 3	5
IN 4	11
IN 5	13
IN 6	15
OUT 1	2
OUT 2	4
OUT 3	6
OUT 4	10
OUT 5	12
OUT 6	14
STROBE 1,2,3	7
STROBE 4,5,6	9
V_{cc}	16
Grd	8

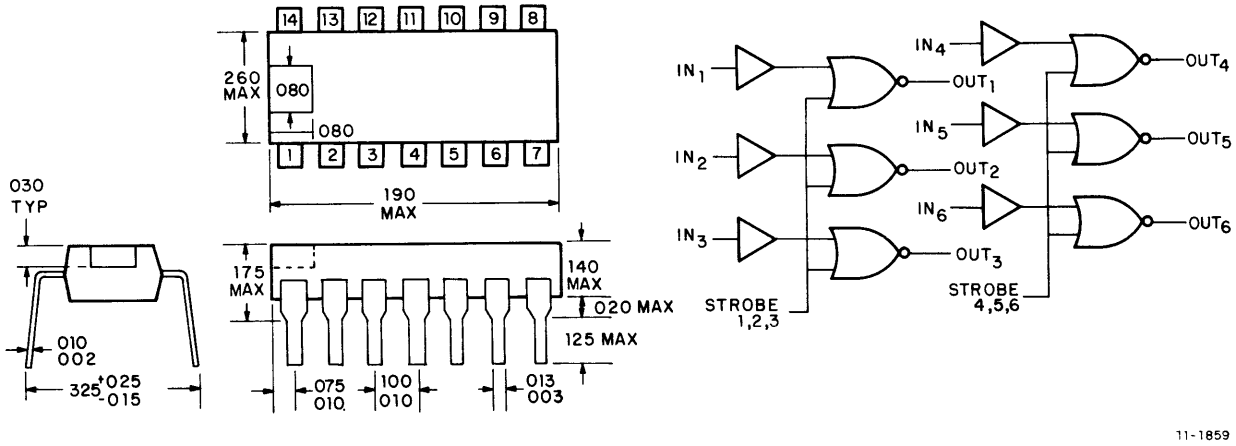


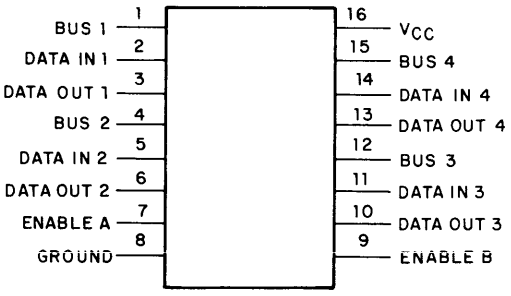
Figure A-9 8837 Hex Unibus Receiver

A.11 8838 QUAD BUS TRANSCEIVER (Figure A-10)

The 8838 consists of four identical receiver/driver combinations in one package for use on the PDP-11 Unibus. Data from the equipment on DATA IN 1, e.g., appearing on pin 2 will be driven out of pin 1 (BUS 1) to the Unibus (if enabled). A BUS 1 signal received from the Unibus on pin 1 will be fed out of pin 3 (DATA OUT 1) to the equipment.

Signal/Pin Designations

Signal Name	Circuit			
	1	2	3	4
BUS	1	4	12	15
DATA IN	2	5	11	14
DATA OUT	3	6	10	13
ENABLE	A		B	
	7		9	
GROUND	8			



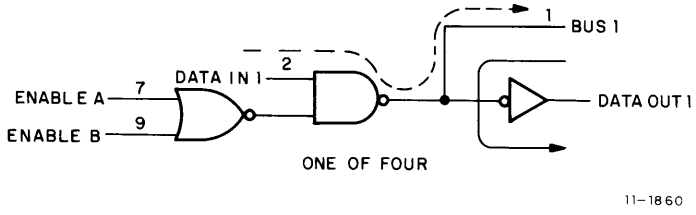


Figure A-10 8838 Quad Bus Transceiver

A.12 9305 FREQUENCY DIVIDER (VARIABLE MODULO COUNTER) (Figure A-11)

The 9305 consists of four master-slave flip-flops that are separated into a single toggle stage and a three-stage synchronous counter. By external connections, the device can be programmed to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. This configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

Asynchronous Mode

$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q_0}$	Q_1	Q_2	Q_3	$\overline{Q_3}$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT					

Programming Connections For Last Three Stages

S_0	S_1	Modulo
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = Not Connected

Alternate Programming Connections For Last Three Stages

S_0	S_1	Modulo
Q_3	Q_3	5
Q_1	Q_1	6
Q_2	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

Connections for Modulo 10, 12, 14, 16 Binary Counters and 50 Percent Duty Cycle Dividers

For Binary Counting $\overline{Q_0}$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q_3}$ connected to CP_0 Incoming clock to CP_1

Modulo	Output	Available Output Fanout
5	Q_3	14/8
6	Q_1	14/7
7	Q_2	14/7
8	Q_1	15/7
8	Q_2	15/7

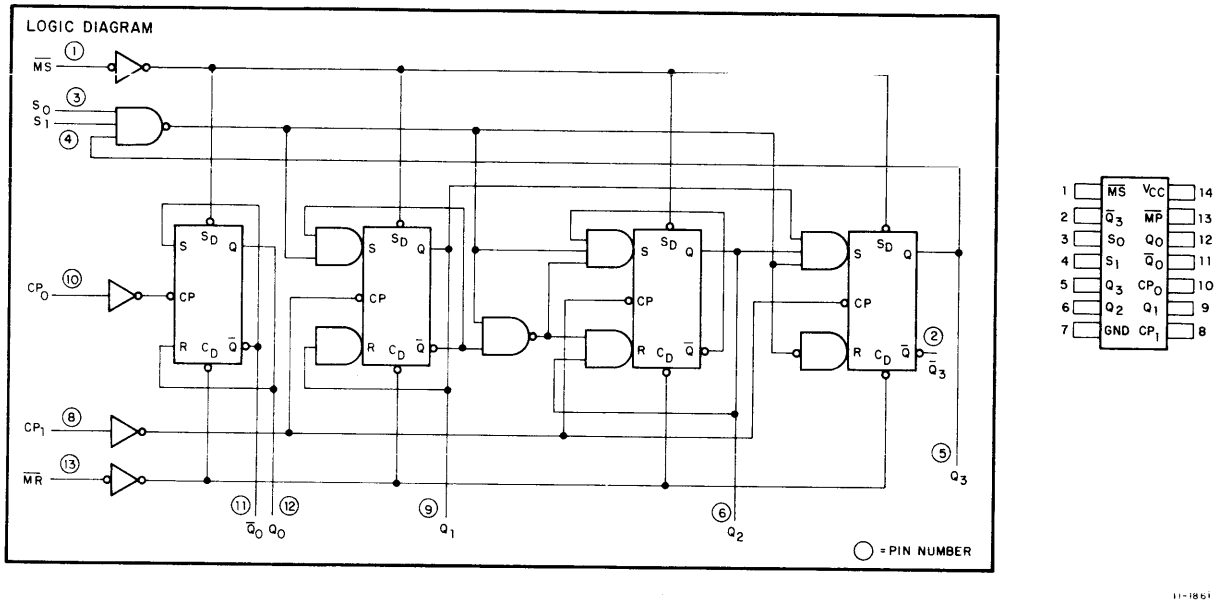


Figure A-11 9305 Frequency Divider (Variable Modulo Counter)

A.13 9318 8-INPUT PRIORITY ENCODER (Figure A-12)

The 9318 8-Input Priority Encoder accepts data from eight active low inputs and yields a binary representation on its three active low outputs. Each output is assigned a priority such that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output. Input line 7 has the highest priority.

The number of priority levels is increased by cascading encoders by connecting the most significant output (EO) to the next most significant encoder's enable input (EI).

A group signal output (GS) is active level low when any input is low indicating when *any* input is active. An enable output (EO) is also active level low when *all* inputs are high.

Truth Table

EI	0	1	2	3	4	5	6	7	GS	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Do Not Care

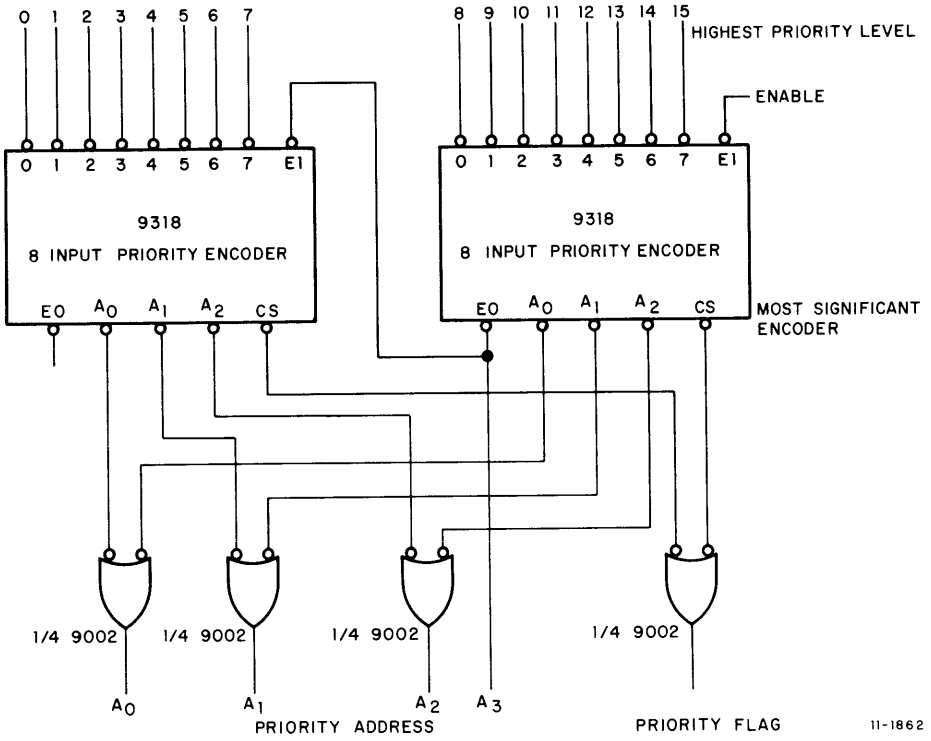


Figure A-12 9318 8-Input Priority Encoder

A.14 74121 MONOSTABLE MULTIVIBRATOR (Figure A-13)

The 74121 is a monostable multivibrator that provides dc triggering from positive or gated negative-going inputs with inhibit capability. Pulse triggering, at a particular voltage level, is not directly related to input pulse transition time. Once fired, outputs are not dependent on further input transitions, but rather are a function of timing parameters.

Truth Table

t_n Input			t_n+1 Input			Output
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2V$

$0 = V_{in(0)} \leq 0.8V$

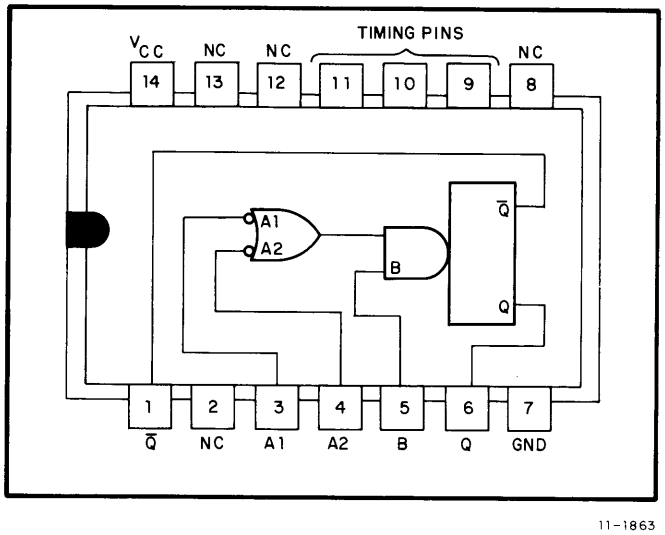


Figure A-13 74121 Monostable Multivibrator

A.15 74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR (Figure A-14)

The 74123 Multivibrator provides dc triggering from gated low level active (A) and high level active (B) inputs. It also provides overriding direct clear inputs and complementary outputs. The retriggering capability simplifies generation of extremely long duration output pulses. If the input is triggered before the output pulse is terminated, the output pulse is extended. An overriding clear feature allows any output pulse to be terminated at a predetermined time, independent of timing components.

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎏
↑	H	⎍	⎏

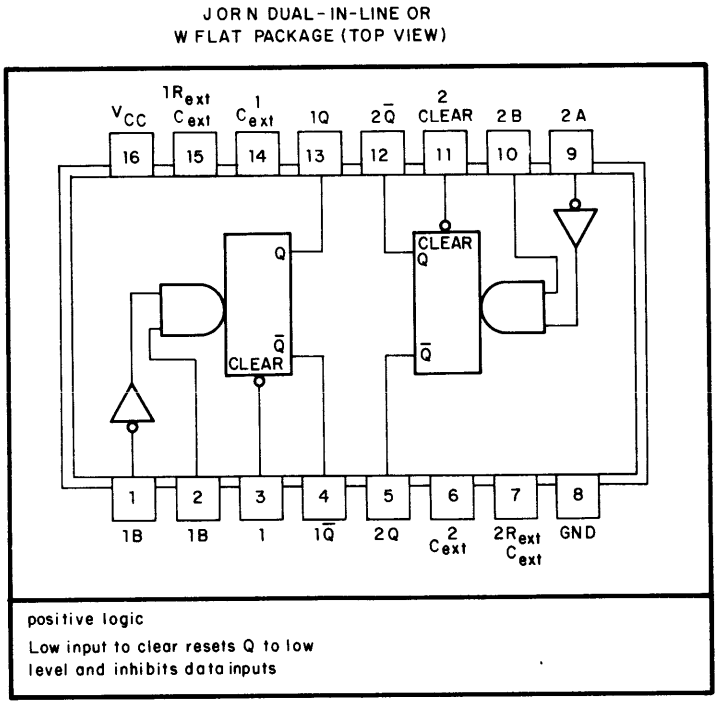


Figure A-14 74123 Retriggerable Monostable Multivibrator With Clear

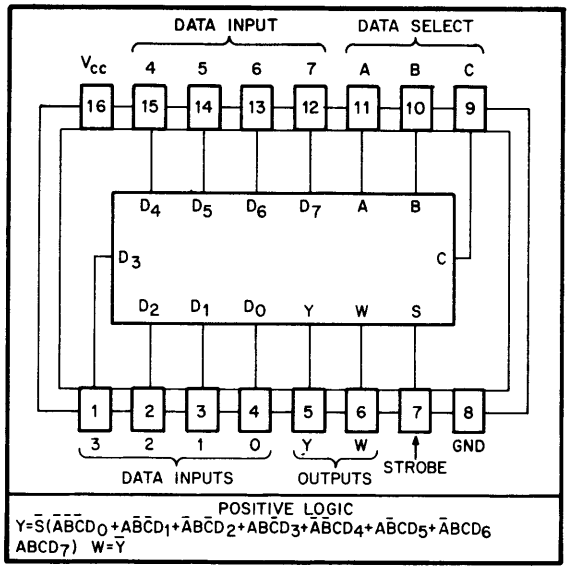
A.16 74151 8-LINE TO 1-LINE MULTIPLEXER (Figure A-15)

The 74151 selects one of eight data sources for multiplexing the output onto one line. The circuit can be used for parallel-to-serial conversion or as a five-variable function operator.

Truth Table

Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.



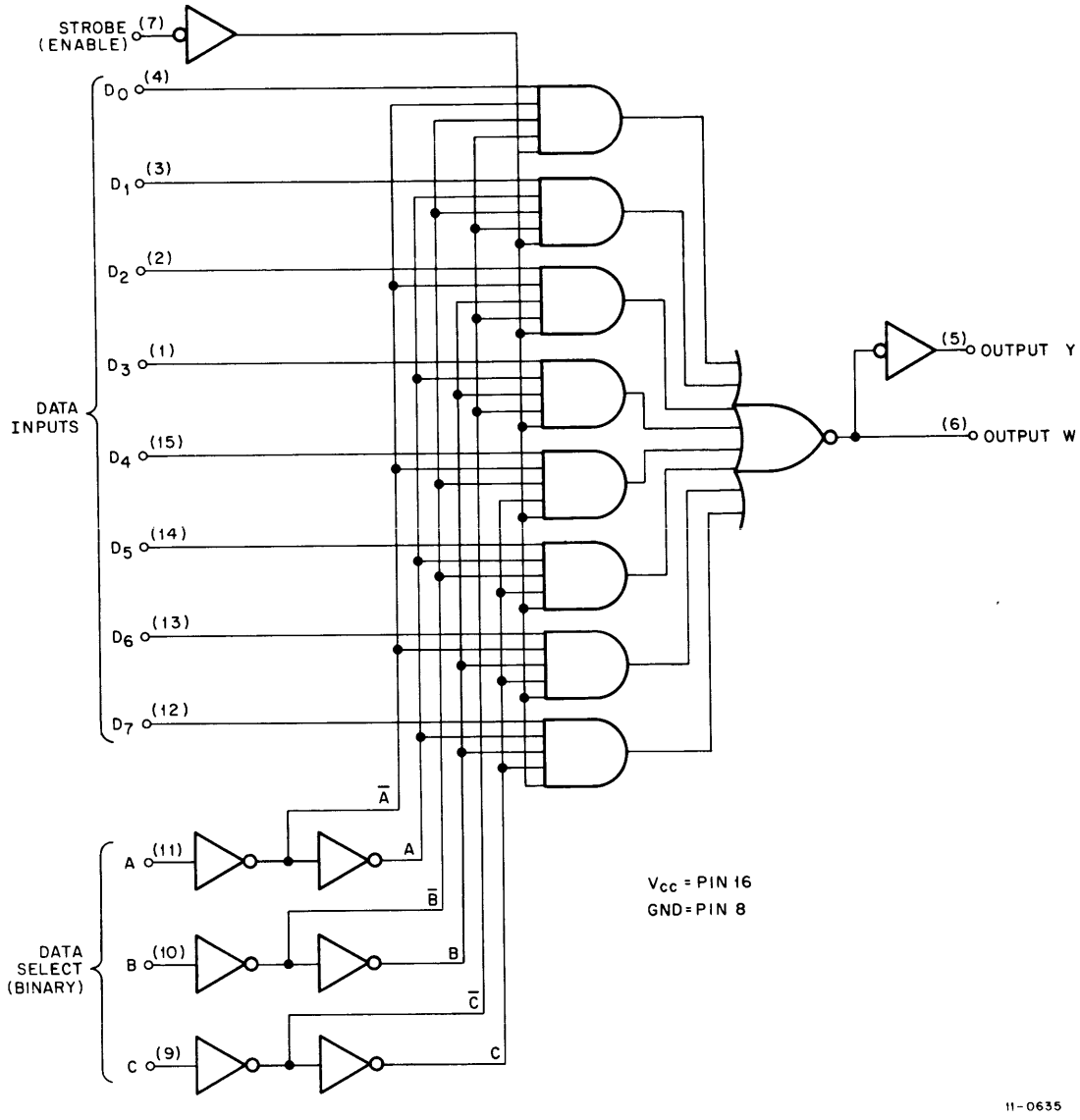


Figure A-15 74151 8-Line to 1-Line Multiplexer

A.17 74153 DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (Figure A-16)

The 74153 is a dual 4-line to 1-line multiplexer with separate strobe lines applied to each section. It can be used for data multiplexing, parallel-to-serial conversion, pulse pattern generation, and as a Boolean function generation.

Address Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

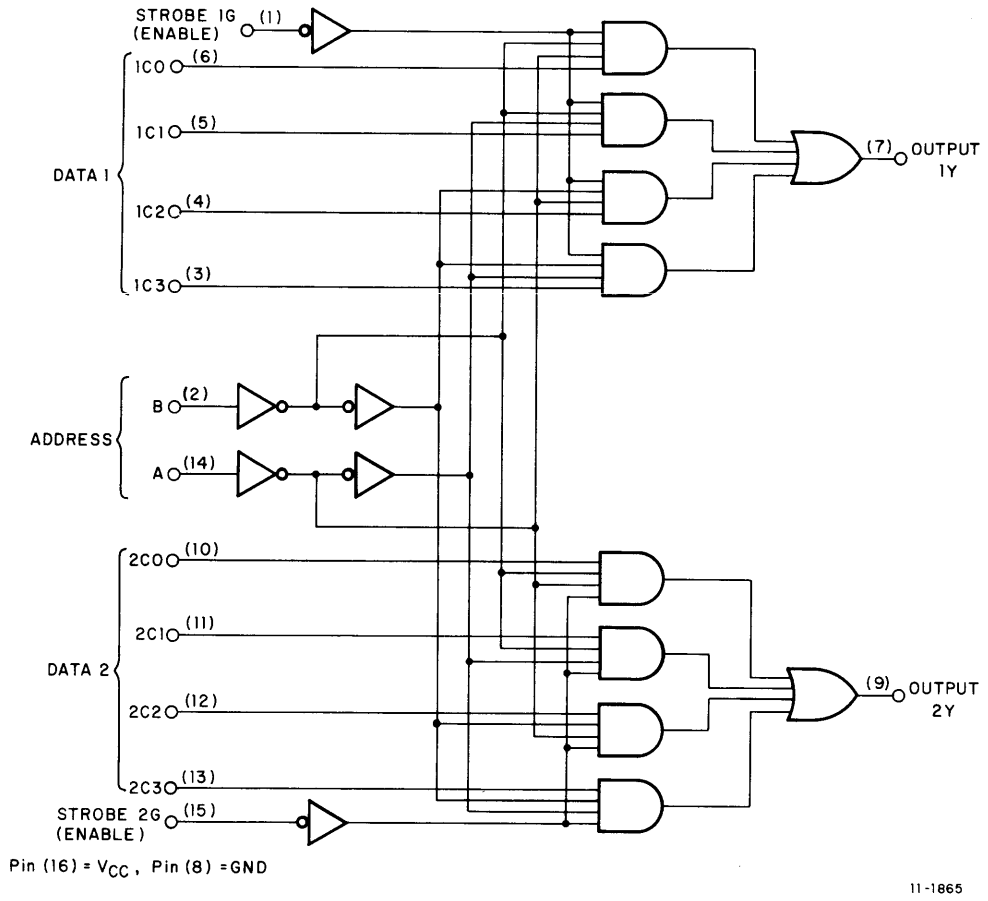


Figure A-16 74153 Dual 4-Line to 1-Line Data Selector/Multiplexer

A.18 74155 3-LINE TO 8-LINE DECODER (Figure A-17)

The 74155 3-Line to 8-Line Decoder consists of 1-to-4 line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to an input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8 line decoder or 1-to-8 line demultiplexer without external gating. When used as a decoder, data inputs 1C and 2C are connected to each other and used for enabling and for cascading.

3-Line To 8-Line Decoder

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Signal/Pin Designation

Signal Name	Pin Designation
STROBE 1G	2
STROBE 2G	14
SELECT A	13
SELECT B	3
DATA 1C	1
DATA 2C	15
OUTPUT 1Y0	7
OUTPUT 1Y1	6
OUTPUT 1Y2	5
OUTPUT 1Y3	4
OUTPUT 2Y0	9
OUTPUT 2Y1	10
OUTPUT 2Y2	11
OUTPUT 2Y3	12

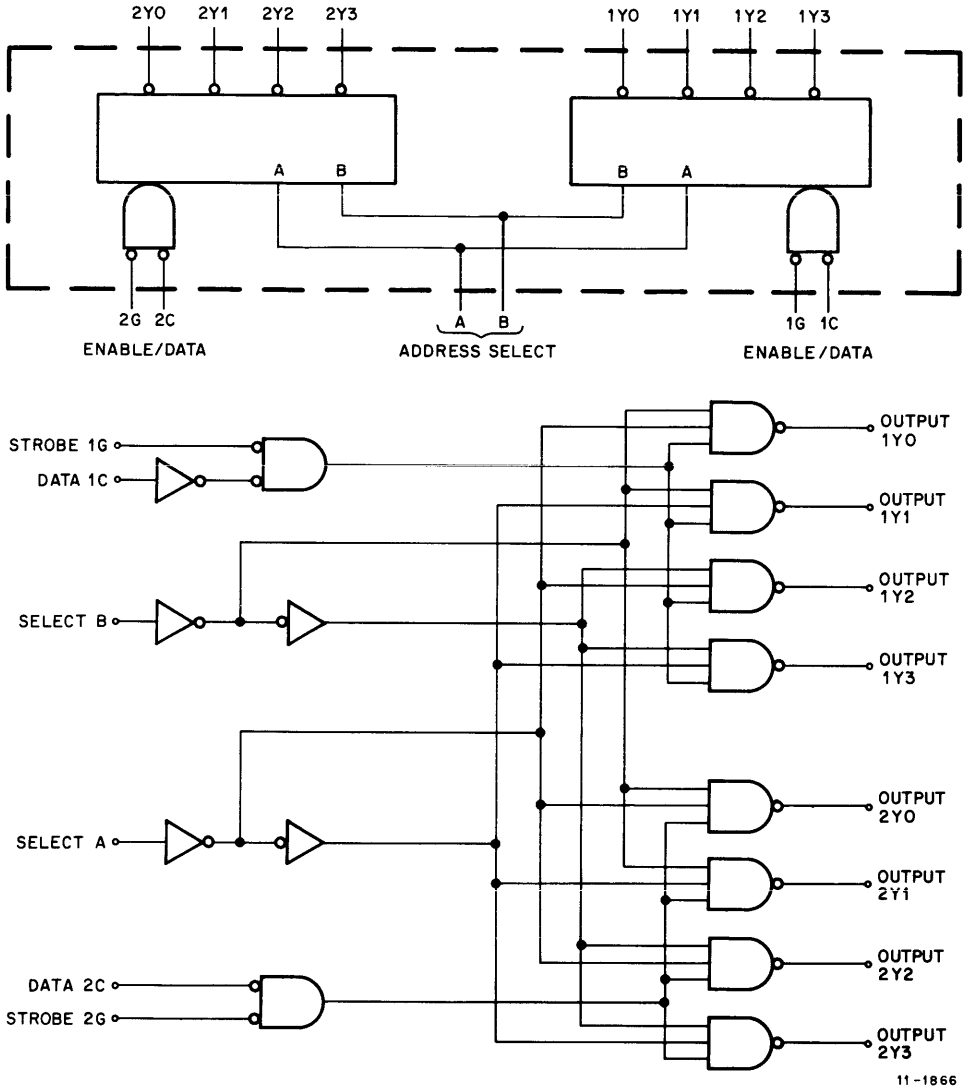


Figure A-17 74155 3-Line to 8-Line Decoder

A.19 74157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER (Figure A-18)

The 74157 Quadruple 2-Line to 1-Line Multiplexer provides buffered inputs and outputs. All inputs are low when disabled (enable high). The truth table and logic diagram are shown below.

Inputs				Output Y
Enable	Select	A	B	SN54/74157 SN54S/74S157
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

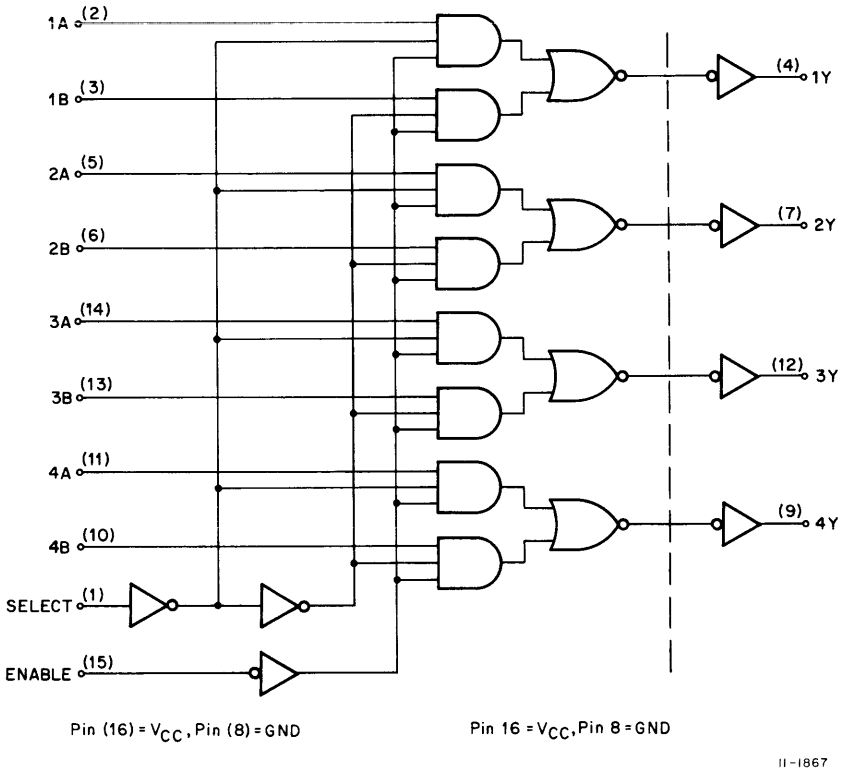


Figure A-18 74157 Quadruple 2-Line to 1-Line Multiplexer

A.20 74161 4-BIT BINARY COUNTER (Figure A-19)

The 74161 binary counter is a 4-bit counter with internal look ahead for fast counting and a carry output for n bit cascading.

Load	Count Enable (CEP · CET)	Mode
H	H	Count Up
H	L	No Change
L	X	Parallel Load

H = high level, L = low level, X = irrelevant

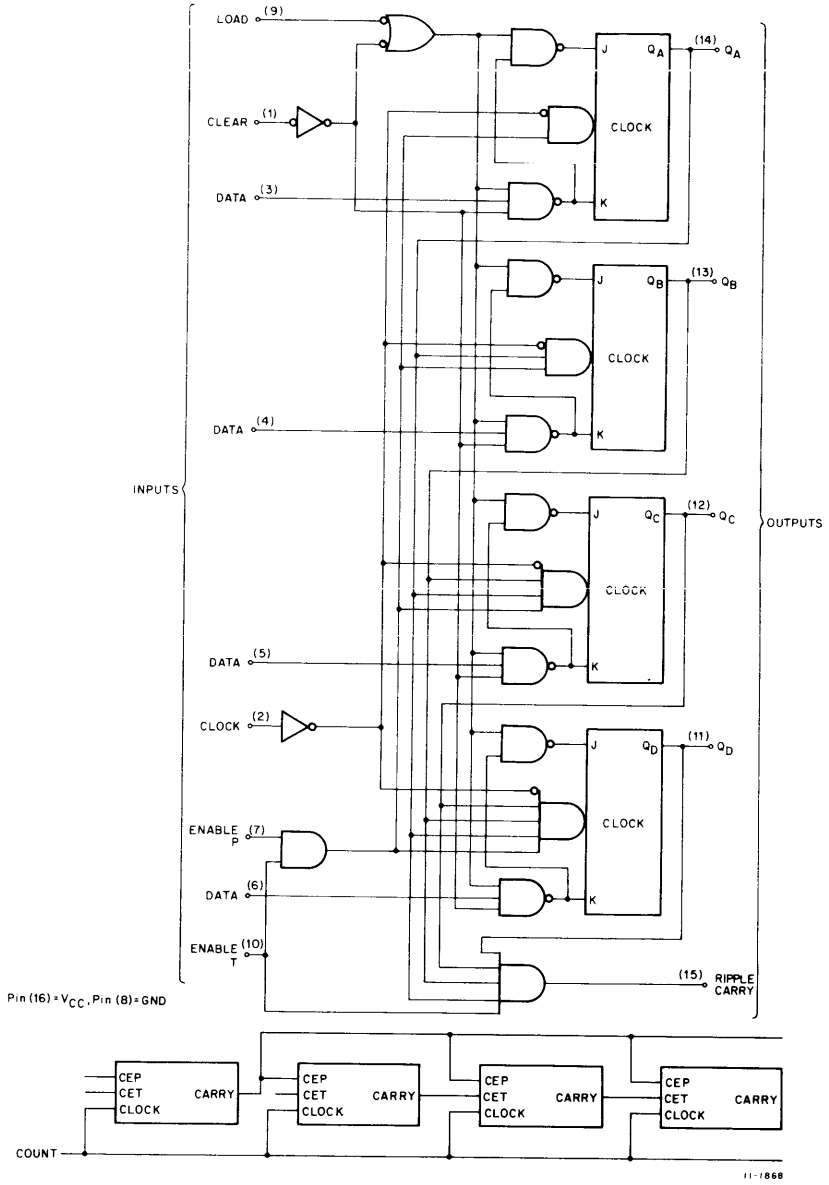


Figure A-19 74161 4-Bit Binary Counter

A.21 74175 QUAD D-TYPE FLIP-FLOPS (Figure A-20)

The 74175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct clear and buffered clock inputs.

Input	Outputs	
t_n	t_n+1	
D	Q	$\overline{Q}$
H	H	L
L	L	H

t_n = bit time before clock pulse.
t_n+1 = bit time after clock pulse.

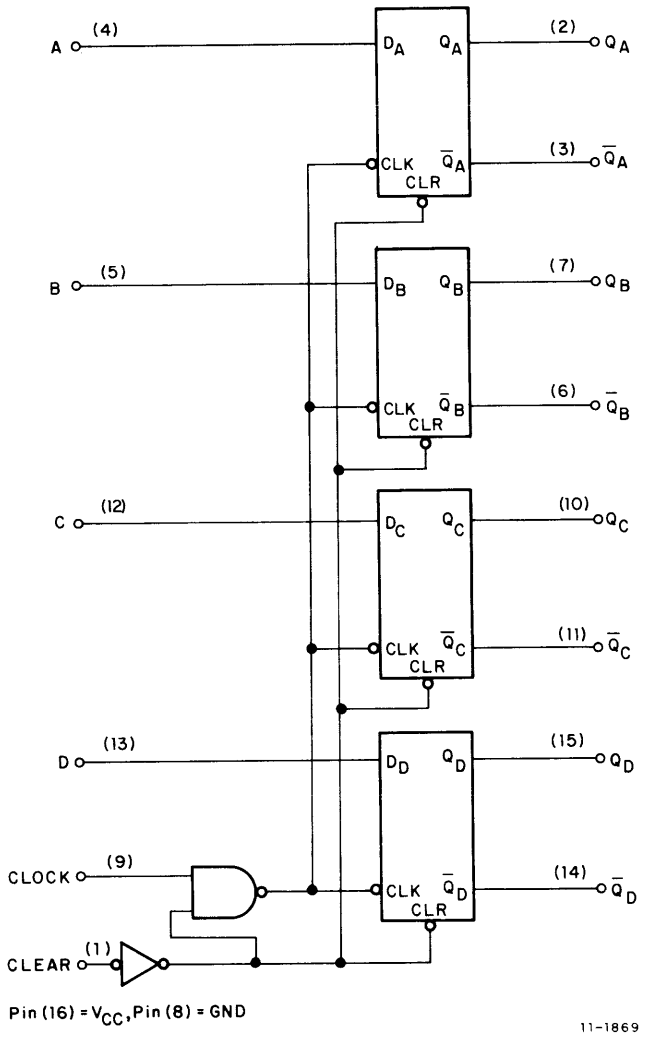


Figure A-20 74175 Quad D-Type Flip-Flops

A.22 74193 4-BIT BINARY COUNTER (Figure A-21)

The 74193 Binary Counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.

Signal/Pin Designation

Signal Name	Pin Designation
DATA INPUT A	15
DATA INPUT B	1
DATA INPUT C	10
DATA INPUT D	9
CLEAR	14
LOAD	11
DOWN COUNT	4
BORROW OUTPUT	13
CARRY OUTPUT	12
UP COUNT	5
OUTPUT Q_A	3
OUTPUT Q_B	2
OUTPUT Q_C	6
OUTPUT Q_D	7

Count Up	Count Down	Load	Mode
X	X	L	Parallel Load
CLOCK	H	H	Count Up
H	CLOCK	H	Count Down

H = high level, L = low level, X = irrelevant

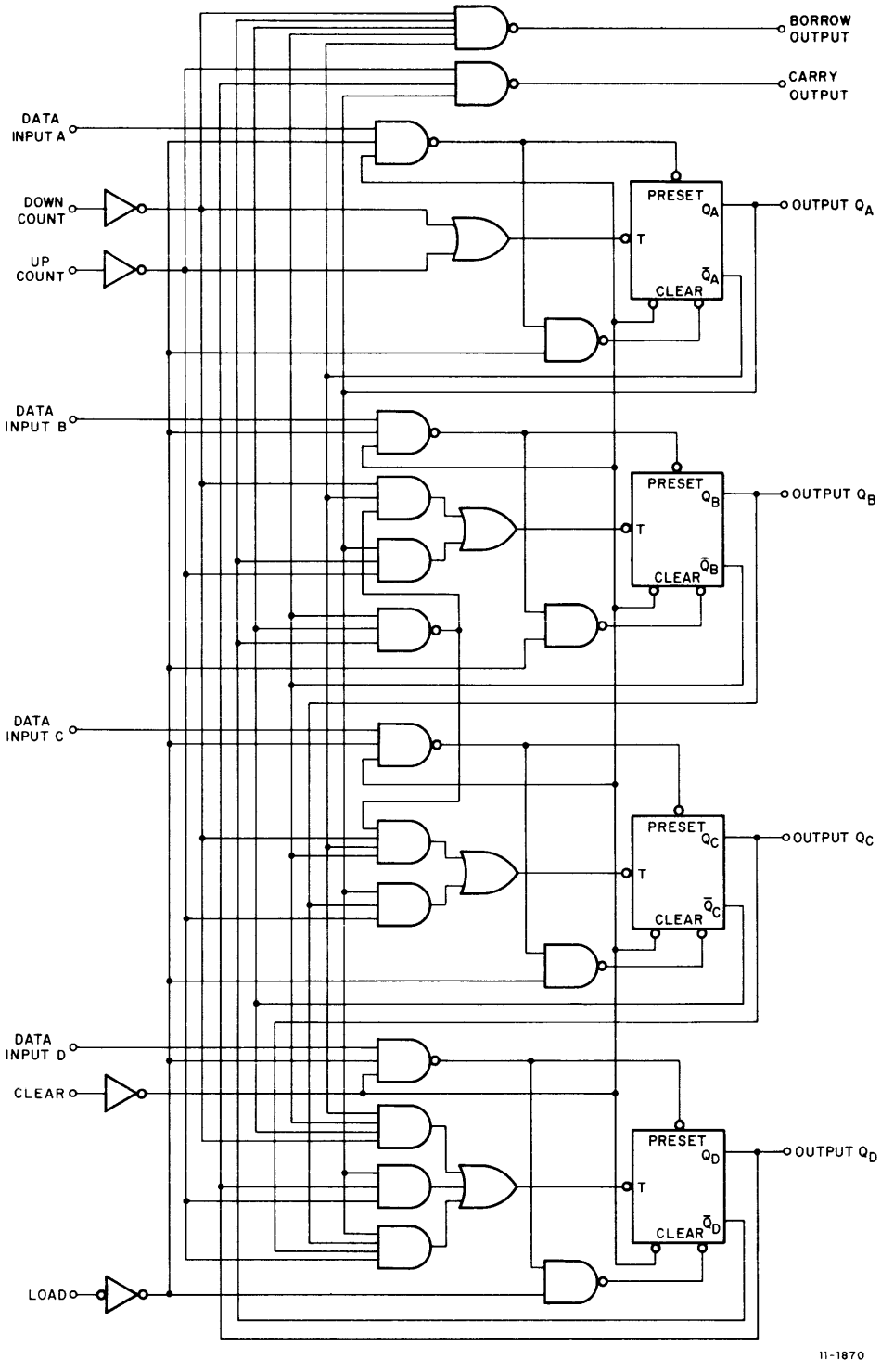


Figure A-21 74193 4-Bit Binary Counter

APPENDIX B
SIGNAL GLOSSARY

B.1 GENERAL

Table B-1 lists selected DJ11 signals in alphabetical order with their meanings. This table is provided for reference use throughout the text.

Table B-1
DJ11 Signal Glossary

Mnemonic		Definition
D1-1	IN H	A gating control signal used to gate data from the device register onto the bus (DATI + DATIP).
D1-1	INT REQ L	This is the Interrupt Request sent out to the Unibus by the 7821 module.
D1-1	M105 L2	A gating control signal used to gate data from the device register onto the bus (DATI + DATIP).
D1-1	OUTHIGH H	A gating control signal used to gate D(15:08) into the high byte of the device register.
D1-1	OUTLOW H	A gating control signal used to gate D(07:00) into the low byte of the device register.
D1-1	SEL 0 H	Selects the CSR as a result of address decoding.
D1-1	SEL 2 H	Selects the RBUF as a result of address decoding.
D1-1	SEL 4 H	Selects either the TCR (if CSR 10 is 0) or the BSR (if CSR 10 is 1) as a result of address decoding.
D1-1	SEL 6 H	Selects the TBUF as a result of address decoding.
D2-2	BUF A(02:01) L	Buffered version of Unibus signals A(02:01), used to control which set of 16 bits from either TBR, TCR, RBUF, or CSR are sent out onto the Unibus.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic		Definition
D2-2	BD 15(H):00(H)	Bus data from the Unibus fed back out to the DJ11 from the bus transceivers.
D2-2	D 15(L):00(L)	Data lines 15:00 from/to the Unibus.
D2-3	TBR 15:00(L)/(H)	Transmitter Break Register bits 15:00 used to issue a break on one of 16 lines designated by a discrete bit in this register.
D2-3	TCR 15:00 (H)	Transmitter Control Register. A specific bit is assigned to each line. When asserted, allows selection of that line if TBMT for that same line is also asserted.
D2-4	H/D SELECT (H)	Used to prevent reception on any line when that line is transmitting.
D2-4	INHIBIT SILO LOAD (L)	Used during half duplex select to prevent loading of an assembled UART character into the FI/FO.
D2-4	MAINT (H)	Asserted on BD02 to force entrance into the maintenance mode.
D2-4	MASTER TRAN SCAN ENABLE (H)/(L)	Asserted on BD08 by program to enable running of the transmitter clock. When clear, prevents TRAN RDY from setting.
D2-4	RCV ENABLE (H)/(L)	When asserted on BD00, enables receiver scan which allows characters to be loaded into FI/FO. When clear, inhibits same.
D2-4	RCV INT ENABLE (H)	When asserted on BD06, permits DONE to cause an interrupt.
D2-4	READ TBR (H)/(L)	When asserted on BD10, permits access of TBR on SEL 04. When clear, permits access of TCR on SEL 04.
D2-4	STATUS ENABLE (H)	When asserted on BD12, permits an interrupt to be generated on a FI/FO overrun.
D2-4	TRAN INT ENABLE (H)/(L)	When asserted on BD14, permits TRAN RDY to cause an interrupt. When clear, negates same.
D2-4	WRITE CSR HIGH (H)	When asserted, permits reporting of the high byte of the CSR.
D2-4	WRITE CSR LOW (H)	When asserted, permits reporting of the low byte of the CSR.
D2-5	GROUP SIGNAL (H)	Asserted whenever the TBMT and TCR for any line is set. Sets the READY flag and stops the scanner on that line.
D2-5	TRANS SCAN A:D (H)	Four outputs of a priority encoder that provides the binary address of the line number of the line selected. Used to select the proper UART and to indicate line number for each entry in the FI/FO.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic		Definition
D2-6	SSYN INHIBIT (L)	Delays the generation of SSYN by the M105.
D2-6	TCR CLEAR FLAG	Asserted when the program clears the TCR bit for the line on which the scanner has stopped. Used to restart the transmit scanner when stopped on a line over which transmission is not desired.
D2-6	TRAN DATA 1:8	Output of the transmit buffer holding register which drives the UART during character loading. Represent the character to be transmitted.
D2-6	TRAN READY (H)	Indicates that scanner has stopped on a line whose TCR and TBMT bits are set. Shows that the UART can be loaded with a character.
D2-6	TRAN STROBE (H)	A Transmit Strobe sent only to the UART that has been selected. Used to strobe the character into the selected UART.
D2-6	TRANS SAMPLE CK (H)	Used to sample all line inputs of the TCR and TBMT.
D2-7	FI/FO OVERRUN (H)	Indicates to the program that the FI/FO is full and that a character must be unloaded from the FI/FO before another received character can be loaded.
D2-7	LOAD SILO (L)	When asserted on START LOAD, provides half of the interlocked communication with the FI/FO enabling clocking of the FI/FO chips.
D2-7	RCV DATA ENABLE (H)	Used to enable the received data leads of the selected UART when a character has been assembled by that UART.
D2-7	RCV SCAN A:C (H) BUF RCV SCAN A:C (H) RCV SCAN D (H)/(L)	Selection signals to the UARTs. Result of output of RCV CHAN # COUNT. Used as Receive Line selection signals throughout the DJ11. Note that the two versions of Scan "D" allows selection of either the high 8 or low 8 lines.
D2-7	READ RCV BUFFER (H)	Asserted anytime a character is read out of the FI/FO and is used to increment the output of the FI/FO and to clear a FI/FO OVERRUN condition.
D2-7	RESET DA (H)	Indicates that the FI/FO has been loaded. Used to clear the data available flag for the UART from which that data has just been taken.
D2-7	TEMP INHIBIT (L)	Asserted on RCV EN and RESET DA to inhibit receive scan clock until setup time is adequate.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic		Definition
D2-8	BUSY CLEAR (H)	This bit reads back as bit 4 on the bus indicating that MOS CLR is in process.
D2-8	DONE (H)	Indicates that a received character has been placed in the FI/FO and is available for reading out.
D2-8	MOS CLEAR (L)	Used to clear bit 15 in all word locations of the FI/FO rendering their contents invalid, and clears all UARTs.
D2-8	MASTER DA (H)	Indicates that data is available in the selected UART.
D2-8	REQ RCV INT (H)	Sent to the interrupt card if a FI/FO OVERRUN exists with status enabled, or when characters are available and the receiver interrupt is enabled.
D2-8	RESET (H)/(L)	Asserted on BUS INIT and used to clear all DJ11 registers.
D2-9	RCV SPEED 0–3	Receive baud rate for lines 0–3 as jumpered.
D2-9	RCV SPEED 4–7	Receive baud rate for lines 4–7 as jumpered.
D2-9	RCV SPEED 8–11	Receive baud rate for lines 8–11 as jumpered.
D2-9	RCV SPEED 12–15	Receive baud rate for lines 12–15 as jumpered.
D2-9	TRANS SPEED 0–3	Transmit baud rate for lines 0–3 as jumpered.
D2-9	TRANS SPEED 4–7	Transmit baud rate for lines 4–7 as jumpered.
D2-9	TRANS SPEED 8–11	Transmit baud rate for lines 8–11 as jumpered.
D2-9	TRANS SPEED 12–15	Transmit baud rate for lines 12–15 as jumpered.
D2-9	5 MHZ	Basic clock frequency output. Used on FI/FO board to eliminate contention between FI/FO read and write functions.
D3-2 thru D3-5	BUF DA LINE 07:00	Buffered version of signal indicating that data is available within the UART receiver holding register for transmittal to FI/FO.
D3-2 thru D3-5	BUF FE LINE 07:00	Buffered version of signal indicating that a framing error (invalid Stop code) has been detected in data character received on this line.
D3-2 thru D3-5	BUF OR LINE 07:00	Buffered version of signal indicating that an overrun has been detected on character received on this line. This means that another character was received by the UART before the previous character had been transferred to the FI/FO.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic	Definition
D3-2 thru D3-5 BUF PE LINE 07:00	Buffered version of signal indicating that a parity error has been detected in character received on this line.
D3-2 thru D3-5 EOC LINE 07:00 H	Indicates that a full character (including Stop bits) has been transmitted from this line. Used to condition silo loading only on half duplex operation.
D3-2 thru D3-5 RCV DATA 1:8	Represents the assembled ASCII characters received on lines 07:00 and sent to the FI/FO.
D3-2 thru D3-5 SERIAL OUT 07:00 H	The serial bit stream as transmitted on these lines.
D3-2 thru D3-5 TBMT LINE 07:00 H	A signal from each of these UARTs indicating that the TBUF is empty.
D3-2 BUF RCV SCAN D	Buffered version of one of four binary outputs from the receiver scanner used in line selection.
D3-2 BUF RDA LINE 07:00	A selected signal to the UART receivers on these lines used to reset the Data Available flag in the UART status register.
D3-2 BUF RDE LINE 07:00	A selected signal to the UART receivers that enables the reading of characters out of the selected UART.
D3-2 BUF RESET	A buffered version of MOS CLR that clears the UART holding register.
D3-4 BUF TRAN DATA 8:1	Buffered versions of the ASCII character to be transmitted as fed to the UART.
D3-2 UC1 MASTER DA H	Indicates that data is available on any of lines 07:00. Used to generate a MASTER DA to control silo loading.
D3-2 UC1 MASTER OR H	Indicates an overrun error has been detected in a character of any of lines 07:00. Used to feed bit 14 of the FI/FO.
D3-3 UC1 RCV DATA 8:1 L	Wire-ORed data outputs of UARTs 07:00. Used to feed the data inputs of the FI/FO.
D3-4 UC1 MASTER FE H	Indicates a framing error has been detected in a character on any of lines 07:00. Used to feed bit 13 of the FI/FO.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic		Definition
D3-4	UC1 MASTER PE H	Indicates that a parity error has been detected in a character on any of lines 07:00. Used to feed bit 12 of the FI/FO.
D4-2 thru D4-5	BUF DA LINE 15:08	Buffered version of signal indicating that data is available within the UART receiver holding register for transmittal to FI/FO.
D4-2 thru D4-5	BUF FE LINE 15:08	Buffered version of signal indicating that a framing error (invalid Stop code) has been detected in data character received on this line.
D4-2 thru D4-5	BUF OR LINE 15:08	Buffered version of signal indicating that an overrun has been detected on character received on this line. This means that another character was received by the UART before the previous character had been transferred to the FI/FO.
D4-2 thru D4-5	BUF PE LINE 15:08	Buffered version of signal indicating that a parity error has been detected in character received on this line.
D4-2 thru D4-5	EOC LINE 15:08 H	Indicates that a full character (including Stop bits) has been transmitted from this line. Used to condition silo loading only on half duplex operation.
D4-2 thru D4-5	RCV DATA 1:8	Represents the assembled ASCII characters received on lines 15:08 and sent to the FI/FO.
D4-2 thru D4-5	SERIAL OUT 15:08	The serial bit stream as transmitted on these lines.
D4-2 thru D4-5	TBMT LINE 15:08 H	A signal from each of these UARTs indicating that the TBUF is empty.
D4-2	BUF RCV SCAN D	Buffered version of one of four binary outputs from the receiver scanner used in line selection.
D4-2	BUF RDA LINE 15:08	A selected signal to the UART receivers on these lines. Used to reset the data available flag in the UART status register.
D4-2	BUF RDE LINE 15:08	A selected signal to the UART receivers that enables the reading of characters out of the UART.
D4-2	BUF RESET	A buffered version of MOS CLR that clears the UART holding register.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic		Definition
D4-2	UC2 MASTER DA H	Indicates that data is available on any of lines 15:08. Used to generate a MASTER DA to control silo loading.
D4-2	UC2 MASTER OR H	Indicates an overrun error has been detected in a character on any of lines 15:08. Used to feed bit 14 of the FI/FO.
D4-3	UC2 RCV DATA 8:1 L	Wire-ORed data outputs of UARTs 15:08. Used to feed the data inputs of the FI/FO.
D4-4	BUF TRAN DATA 8:1	Buffered versions of the ASCII characters to be transmitted as fed to the UART.
D4-4	UC2 MASTER FE H	Indicates a framing error has been detected in a character on any of lines 15:08. Used to feed bit 13 of the FI/FO.
D4-4	UC2 MASTER PE H	Indicates that a parity error has been detected in a character on any of lines 15:08. Used to feed bit 12 of the FI/FO.
D11-2	CHARACTER AVAILABLE L	Generated by the FI/FO buffer whenever a valid character is available at its output pins.
D11-2	RCV BUF 15:00 H	Represents one 16-bit character including line number, errors, and a valid data bit as stored in the FI/FO buffer.
D11-2	READY IN L	Generated by the FI/FO buffer. Used by the receive scanner to indicate that a character can be loaded in the FI/FO.
D11-2	READY OUT L	Generated by the FI/FO buffer. Indicates that a character is ready for reading at the bottom of the buffer.
D11-3	CK CHARACTER AVAILABLE L	Output of a hard-wired comparator that is used to vary the amount of characters that can be accumulated in the FI/FO before a CHARACTER DONE INT is generated.
D11-3	LOAD IN PROGRESS L	Generated by the FI/FO buffer control logic while a character is being loaded in the FI/FO.
D11-3	LOAD PULSE L	Generated when the FI/FO is loaded. Used to increment the silo status register.
D11-3	LOAD SILO H	Results from LOAD SILO L in the receiver scanner and is used to clock the FI/FO chips.
D11-3	MOS CLEAR H	Buffered version of D2-8 MOS CLEAR L. Used to initialize the silo control, to clear the silo status register, and to clear CHARACTER AVAILABLE indication.

Table B-1 (Cont)
DJ11 Signal Glossary

Mnemonic	Definition
D11-3 READ SILO H	Generated when a character is READY OUT in the FI/FO and reading is enabled. Used to read a character out of the FI/FO. Delayed version is used to decrement the silo status register.
D11-3 SSR 13:08 H	Outputs of the silo status register, used by a comparator to enable generation of a CHARACTER DONE INT.
D11-3 VALID DATA H	Generated on READY OUT and READ RCV BUFFER. Used to set bit 15 in the FI/FO word to indicate that that word is valid for reading.

APPENDIX C
FLOATING DEVICE AND VECTOR ADDRESSES FOR COMMUNICATION DEVICES

C.1 INTRODUCTION

Starting with the DJ11, new communications devices are to be assigned floating addresses. The addresses for current production devices are to be retained.

The word "floating" means that addresses are not assigned absolutely for the maximum number of each communications device that can be used in a system.

C.2 DEVICE ADDRESSES

Floating device addresses are assigned as follows:

a. The floating address space starts at location 760010 and extends to location 764000 (octal designations).

b. The devices are assigned in order by type: the DJ11 first, followed by the DH11, and then the next device introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

c. The first address of a new type device must start on a modulo 10_8 boundary.

d. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used, if the device following is used.

e. No new type device can be inserted ahead of a device on the list.

f. If additional devices on the list are to be added to a system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required to make room for the additions.

g. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 utilizes eight device addresses.

The following examples show typical floating device address assignments for communication devices in a system.

Example 1: 2 DJ11s, 1 DH11, and 2 XX11s (future device with 2 registers)

760010	DJ11 #0	first address	DJ11 requires 4 addresses
760012	DJ11 #0		
760014	DJ11 #0		
760016	DJ11 #0	last address	
760020	DJ11 #1	first address	
760022	DJ11 #1		
760024	DJ11 #1		
760026	DJ11 #1	last address	
760030	DJ11 Gap (indicates that there are no more DJ11s)		
760040	DH11 #0	first address	DH11 requires 8 addresses
760042	DH11 #0		
760044	DH11 #0		
760046	DH11 #0		
760050	DH11 #0		
760052	DH11 #0		
760054	DH11 #0		
760056	DH11 #0	last address	
760060	DH11 Gap		
760070	XX11 #0	first address	XX11 requires 2 addresses
760072	XX11 #0	last address	

etc.

Example 2: 1 DJ11 and 1 DH11

760010	DJ11 #0	first address
760012	DJ11 #0	
760014	DJ11 #0	
760016	DJ11 #0	last address
760020	DJ11 Gap	
760030	Cannot be used for DH11. Not a modulo 20_8 boundary.	
760040	DH11 #0	first address
760042	DH11 #0	
760044	DH11 #0	
760046	DH11 #0	
760050	DH11 #0	
760052	DH11 #0	
760054	DH11 #0	
760056	DH11 #0	last address
760060	DH11 Gap	

etc.

C.3 VECTOR ADDRESSES

The floating vector addresses are assigned starting at 300 and proceed upward. The addresses are assigned to devices in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C, D, E; DJ11; DH11.

New devices are added as they are introduced into production.

APPENDIX D
FORMS

Table D-1

Customer's Preference Chart

DJ11 #	Line Groups	Levels	Parity	Stop Bits	Speed Selection		
					XTR	RCV	Split
0	0–3						
	4–7						
	8–11						
	12–15						
1	0–3						
	4–7						
	8–11						
	12–15						
2	0–3						
	4–7						
	8–11						
	12–15						
3	0–3						
	4–7						
	8–11						
	12–15						
4	0–3						
	4–7						
	8–11						
	12–15						
5	0–3						
	4–7						
	8–11						
	12–15						
6	0–3						
	4–7						
	8–11						
	12–15						
7	0–3						
	4–7						
	8–11						
	12–15						
8	0–3						
	4–7						
	8–11						
	12–15						
9	0–3						
	4–7						
	8–11						
	12–15						
10	0–3						
	4–7						
	8–11						
	12–15						

Table D-1

Customer's Preference Chart (Cont)

DJ11 #	Line Groups	Levels	Parity	Stop Bits	Speed Selection		
					XTR	RCV	Split
11	0–3						
	4–7						
	8–11						
	12–15						
12	0–3						
	4–7						
	8–11						
	12–15						
13	0–3						
	4–7						
	8–11						
	12–15						
14	0–3						
	4–7						
	8–11						
	12–15						
15	0–3						
	4–7						
	8–11						
	12–15						

DJ11 Asynchronous
16-Line Multiplexer
Maintenance Manual
EK-DJ11-MM-003

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Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

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What features are most useful? _____

_____

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What faults do you find with the manual? _____

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Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT ON DOTTED LINE

— — — — — — — — — — — Fold Here — — — — — — — — — —

— — — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

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