EK-DHV11-TM-001

DHV11
Technical Manual

digital

EK-DHV11-TM-001

DHV11
Technical Manual

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of
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PREFACE

This document describes the installation requirements and servicing procedures for the DHV11 asynchronous multiplexer. It contains information for first-line service, field service support, and for customer engineers. A substantial programming chapter is included. Appendix C contains a glossary of terms used in this manual.

The manual is organized into five chapters plus appendices.

Chapter 1	–	Introduction
Chapter 2	–	Installation
Chapter 3	–	Programming
Chapter 4	–	Technical Description
Chapter 5	–	Maintenance
Appendix A	–	Integrated Circuit Descriptions
Appendix B	–	Modem Control
Appendix C	–	Glossary of Terms

The following is a list of related titles and document numbers.

Document	Number
LSI-11 Microcomputer Interfaces Handbook	EB-20175-20
LSI-11 Systems Service Manual	EK-LSIFS-SV
Communications Mini-Reference Guide	EK-CMINI-RM
Terminals and Communications Handbook	EB-20752-20
Microcomputers and Memories	EB-20912-20
DHV11 Print Set	MP01793
DHV11 Maintenance Card	EK-DHV11-MC

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

Chapter 1 provides general information and specifications. It describes how the module can be configured, and how it interfaces with the system bus and the serial data lines. Physical and functional descriptions are also included.

1.2 OVERVIEW

The DHV11 is an LSI-11/Q-bus option. All future references to the bus will be by the global term Q-bus. The specific terms Q16, Q18, or Q22 will be used where needed to identify versions with 16-, 18-, or 22-bit addresses.

1.2.1 General Description

The DHV11 option is an asynchronous multiplexer which provides eight full-duplex asynchronous serial data channels on Q-bus systems. The option can be used in many applications. These include data concentration, terminal interfacing, and cluster controlling.

The main features of the DHV11 are as follows:

- Eight full-duplex asynchronous data channels
- Direct Memory Access (DMA) or single-character programmed transfers on transmit
- Large 256-entry First-In-First-Out (FIFO) buffer for received characters, dataset status changes, and diagnostic information
- RS-423-A/V.10/X.26 and RS-232-C/V.28 compatible
- Full-duplex point-to-point or auto-answer dial-up operation
- Programmable split speed per line
- Total module throughput of 15000 characters per second
- Q16, Q18, and Q22 bus compatible
- Automatic flow control of transmitted and received data
- Self-test and background monitor diagnostics
- Programmable test facilities
- Single quad-height module (M3104)
- All functions are programmable, except for device address and vector selection which are done by hardware switches on the module.

Enough modem control is provided on all eight channels to allow auto-answer dial-up operation over the Public Switched Telephone Network (PSTN). Suitable modems to use this facility are the Bell models 103, 113, 212, or equivalent. The DHV11 can also be used for point-to-point operation over private lines. Modem control is implemented by software in the host.

The module provides DMA or single-character transfers from the host system to the serial lines. A 256-character FIFO buffer is provided for data received from the serial lines.

By using microcomputers (referred to as PROC 1 and PROC 2 in this manual), the DHV11 releases the host system from many of the data handling tasks.

One 8051 microcomputer controls DMA and single-character transmissions from the host system to the DHV11. A second 8051 controls four SC2681 Dual Universal Asynchronous Receiver Transmitters (DUARTs) which carry out the serial/parallel and parallel/serial conversion of data.

The DHV11 carries ROM-based diagnostics which are executed independently of the host. A full range of diagnostic programs is also available. These run under the PDP-11 Diagnostic Run-time Services (DRS).

A green LED gives the GO/NO-GO status of the module. More detailed diagnostic information is also made available to the host system via the FIFO buffer. Loopback test connectors are available for use with the system-based diagnostics.

I/O addresses and interrupt vectors for the module are selected on two Dual-In-Line (DIL) switchpacks. All other DHV11 functions and configurations are programmable.

To prevent data loss at high throughput levels, the DHV11 can be programmed for automatic X-ON and X-OFF operation.

1.2.2 Physical Description

The option is based on a standard quad-height module (M3104). The layout of this module is shown in Figure 1-1. The dimensions are 21.6 cm x 26.5 cm (8.51 inches x 10.44 inches).

The module is connected to the Q-bus via connectors A and B. J1 and J2 are connected to the communications lines via BC05L-xx cables and H3173-A distribution panels.

On some backplanes, jumpers W1 (BIAK) and W2 (BDMG) extend the bus grant signals to the next module slot via connectors C and D.

DIL switchpacks E58 and E43 select the device address and vector address of the module.

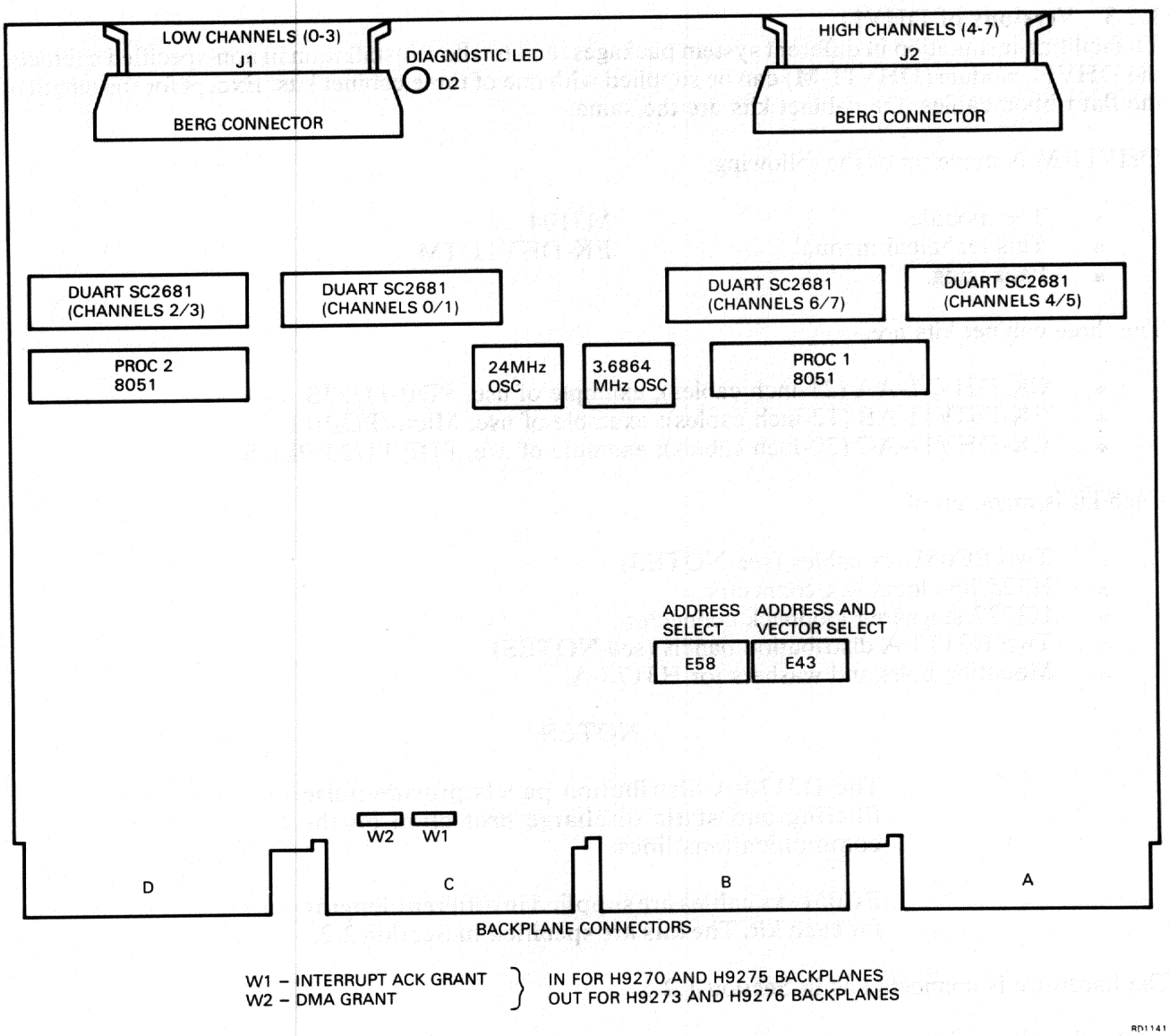


Figure 1-1 M3104 Module

1.2.3 Versions of DHV11

To facilitate installation in different system packages, and to allow installation in non-specified cabinets, the DHV11 module (DHV11-M) can be supplied with one of three cabinet kits. Except for the length of the flat ribbon cables, the cabinet kits are the same.

DHV11-M is made up of the following:

- The module — M3104
- This technical manual — EK-DHV11-TM
- Packaging.

The three cabinet kits are:

- CK-DHV11-AA (21-inch cables); example of use, PDP-11/23S
- CK-DHV11-AB (12-inch cables); example of use, Micro/PDP-11
- CK-DHV11-AC (30-inch cables); example of use, PDP-11/23 PLUS

Each kit is made up of:

- Two BC05L-xx cables (see NOTES)
- H325 line loopback connector
- H3277 staggered loopback connector
- Two H3173-A distribution panels (see NOTES)
- Mounting bolts and washers for H3173-A.

NOTES

The H3173-A distribution panels provide noise filtering and static discharge protection on the communications lines.

BC05L-xx cables are supplied in different lengths for each kit. The kits are specified in Section 2.2.

The hardware is connected as in Section 1.2.5.

1.2.4 Configurations

Figure 1-2 shows some possible DHV11 configurations. The position of the module on the bus (backplane) determines its DMA and interrupt priorities. A guide to positioning is given in Section 2.4. Any or all of the data channels can be connected to a terminal or to a data communications line.

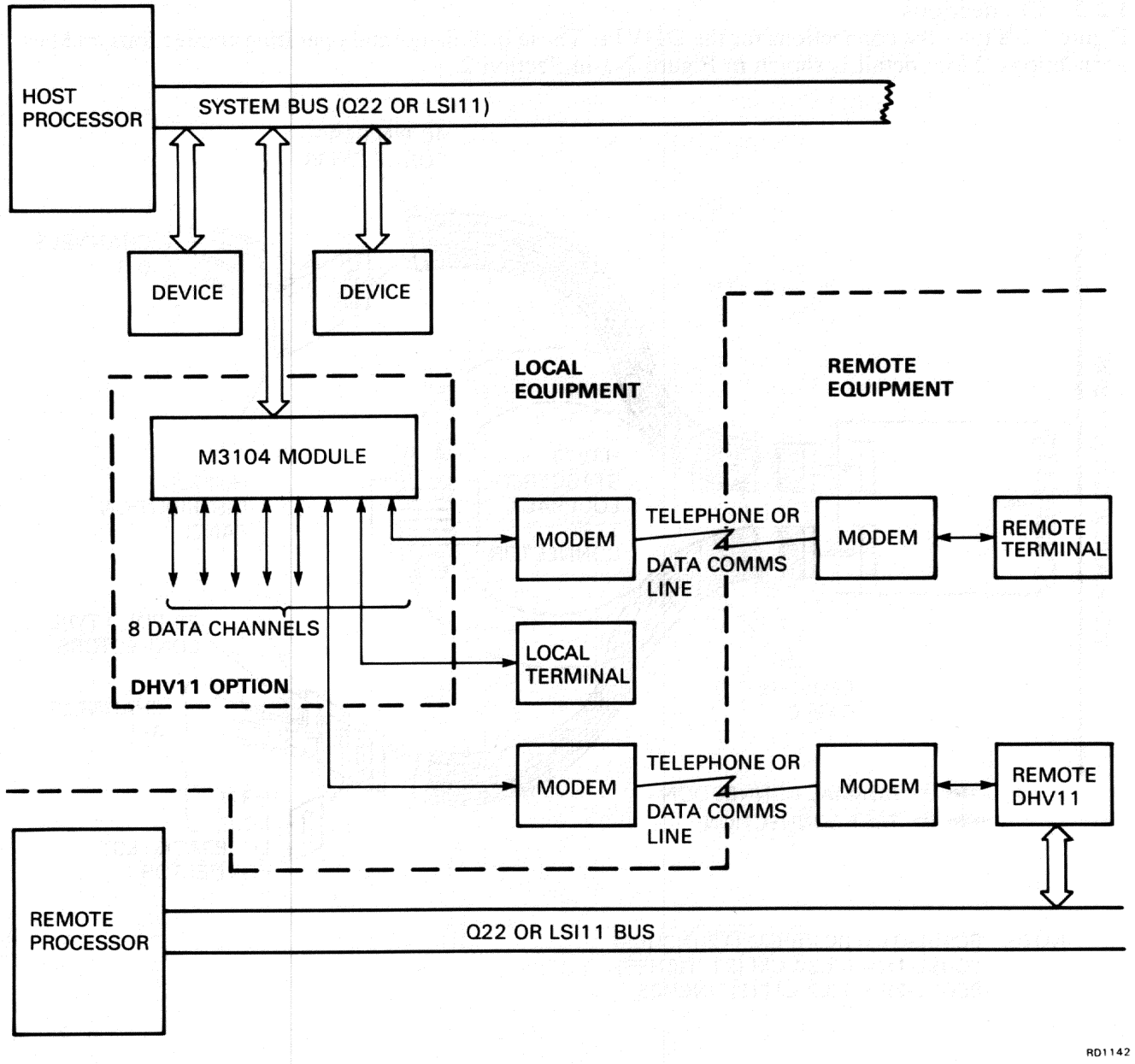
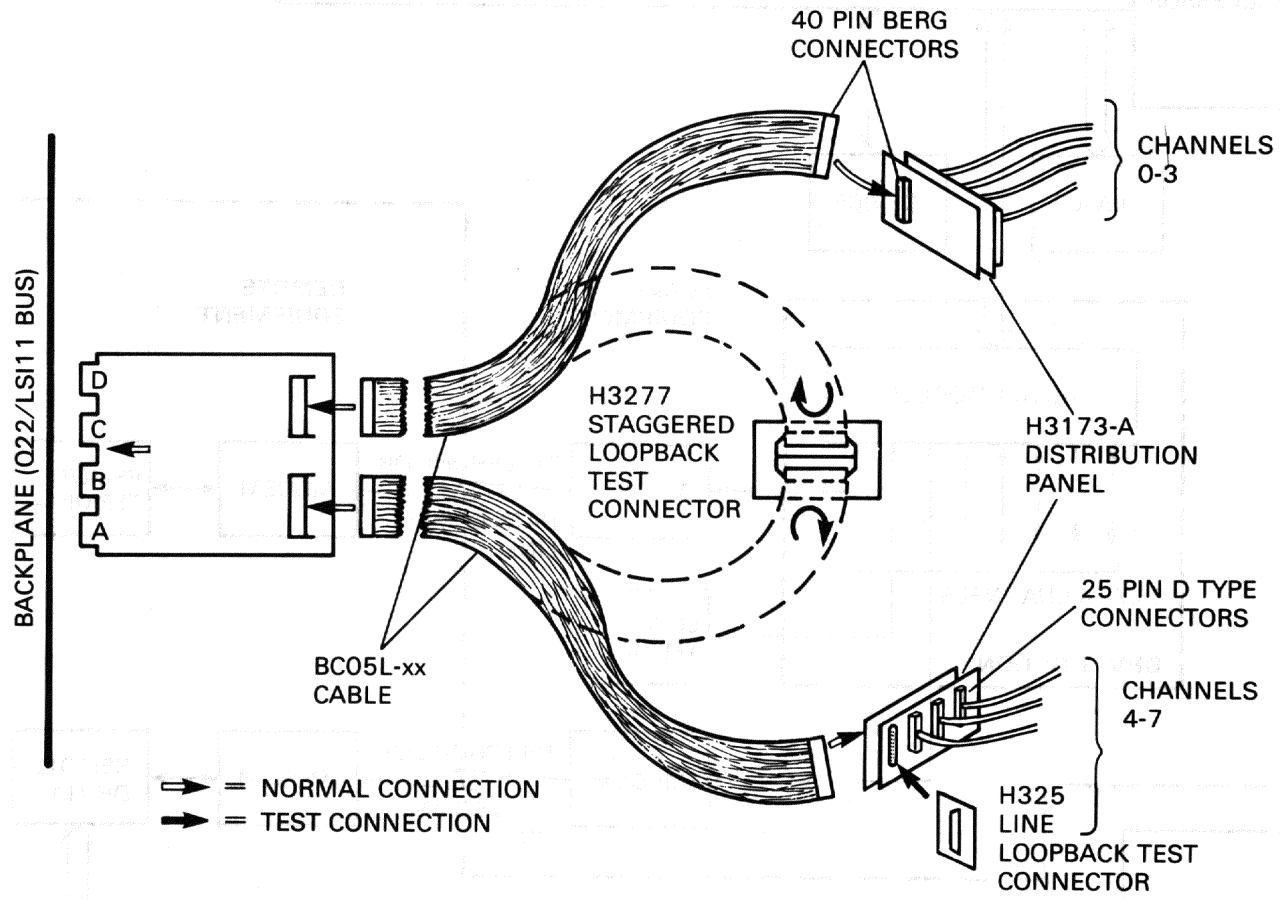


Figure 1-2 Example of DHV11 Configuration

1.2.5 Connections

Figure 1-3 shows the connections for the DHV11. These include normal operating connections and test connections. More detail is shown in Figure 2-3 in Section 2.



NOTE: BC05L-01 = 30.48 CM (12 INCHES)
BC05L-1K = 53.34 CM (21 INCHES)
BC05L-2F = 76.2 CM (30 INCHES)

Figure 1-3 DHV11 Connections

1.3 SPECIFICATION

1.3.1 Environment Conditions

- Storage temperature: 0°C to 66°C (32°F to 151°F)
- Operating temperature: 5°C to 60°C (41°F to 140°F)
- Relative humidity: 10% to 95% non-condensing (complies with DEC STD 102 class C)

1.3.2 Electrical Requirements

+5 V dc + or – 5% at 4.3 A (typical), 6.6 A (maximum)
+12 V dc + or – 3% at 475 mA (typical), 980 mA (maximum)

Negative 12 V dc is generated by a Switch Mode Power Supply (SMPS) circuit on the DHV11. It has the following specification:

–11.85 V dc + or – 7.25% at 400 mA (maximum)
Output ripple is 200 mV peak to peak at 33.3 kHz

Loads applied to the Q-bus are as follows:

Q-bus ac loads – 2.9 ac loads
Q-bus dc loads – 1.0 dc loads

1.3.3 Performance

1.3.3.1 Data Rates – Each channel can be programmed to operate at one of a number of speeds. If needed, the transmission and reception rates can be different (split speed). Table 1-1 shows the data rates which are possible. The maximum rate per channel is 38400 bits per second (bits/s).

The eight serial channels are implemented with four DUART ICs (Integrated Circuits). Channels are paired as follows: 0/1, 2/3, 4/5, 6/7. Because of the method of data rate generation, all transmit and receive rates for a DUART channel-pair must be in the same group (A or B).

Table 1-1 DHV11 Data Rates

Speed (Bits/s)	Groups
50	A
75	B
110	A and B
134.5	A and B
150	B
300	A and B
600	A and B
1200	A and B
1800	B
2000	B
2400	A and B
4800	A and B
7200	A
9600	A and B
19200	B
38400	A

Data rate selection is covered in Chapter 3 (Programming).

1.3.3.2 **Throughput** – Each channel is capable of full-duplex operation at data rates of up to 38400 bits/s. The DHV11, however, cannot handle eight channels operating at this rate at the same time. Total maximum throughput is also dependent on the application and configuration.

Maximum throughput:

Per channel (send)	–	1000 characters per second in single-character transfer mode
		2000 characters per second in DMA mode
(receive)	–	4000 characters per second.

On any channel, the DHV11 can send at one of the above transmit rates and receive at 4000 characters per second at the same time.

Total (8 channels)	–	15000 characters per second

NOTES

The DMA firmware cannot handle transmit data faster than 2000 characters per second (19200 bits/s). If the transmit data rate is increased to 38400 bits/s, the duration of each character will be halved but there will be gaps in transmission.

15000 characters per second is the sum of both transmitted and received characters on all channels. This throughput could support all channels transmitting or receiving at 19200 bits/s, or all channels transmitting and receiving at 9600 bits/s. The above figures are based on a 7-bit character with start bit, parity bit, and one stop bit.

1.4 INTERFACES

1.4.1 System Bus Interface

The M3104 module will connect directly to the Q-bus via connectors A and B. To make the module compatible with backplanes which have Q-bus on C and D also, two jumpers (W1 and W2) are provided. The use of these jumpers is described in Section 2.3. Backplane signals, together with pin details, are listed in Table 2-3.

1.4.2 Serial Interfaces

1.4.2.1 **Interface Standards** – The DHV11 provides interface signals which conform to a subset of the EIA/CCITT standard RS-232-C/V.24. The electrical characteristics conform to EIA/CCITT standards RS-232-C/V.24 and RS-423-A/V.28 (unbalanced interface). The interface is compatible with X.26/V.10 standards but does not comply with the slew rate requirements.

Connections to the external equipment are via 25-pin male subminiature D-type connectors, as specified for RS-232-C.

By means of suitable cables and connectors (not supplied or supported by DIGITAL) the channels can be made compatible with the following:

1. Subset of EIA interchange standard RS-449
2. EIA electrical standard RS-422 (balanced).

NOTE

Even when RS-422 is implemented; RS-423-A cable length/data rate recommendations should be followed.

Table 1-2 shows RS-232-C/V.24/RS-449 signal relationships, and pin connections for the male subminiature D-type connectors.

Table 1-2 EIA/CCITT Signal Relationships

Signal Name		D-Type Pin	RS-232-C	Circuit CCITT V.24	Circuit RS-449
Protective Ground	(GND)	1	AA		
Signal Ground	(SIG GND)	7	AB	102	SG
Transmitted Data	(TXD)	2	BA	103	SD
Received Data	(RXD)	3	BB	104	RD
Request to Send	(RTS)	4	CA	105	RS
Clear to Send	(CTS)	5	CB	106	CS
Data Set Ready	(DSR)	6	CC	107	DM
Data Terminal Ready	(DTR)	20	CD	108/2	TR
Ring Indicator	(RI)	22	CE	125	IC
Data Carrier Detect	(DCD)	8	CF	109	RR

NOTE

The backward channels listed below are not supported. However, by using another channel for this function, and by connecting a suitable cable (H1200 or H1201 for example), backward channel operation is possible.

Circuit No.	Function
118	Transmitted backward channel data
120	Transmit backward channel line signal
119	Received backward channel data
121	Backward channel ready
122	Backward channel received line signal detector

1.4.2.2 Serial Data Format – Serial characters are made up of a coded sequence of bits which are enclosed between a start and a stop signal. The start signal is always 1 bit long but the stop signal is programmable to 1, 1.5, or 2 bits. The duration of a bit is dependent on the selected data rate.

Character codes may be 5, 6, 7, or 8 bits long, optionally followed by a parity bit. Parity can be programmed as even, odd, or no parity.

On serial data channels controlled via the DHV11, the data line is held marking when inactive. Transfer of each character begins with a start bit (space) and ends with one or more stop bits (mark).

Figure 1-4 shows the reception of an 8-bit character with parity. The Least-Significant Bit (LSB) of the character code is transmitted first. If another character is not ready for transmission, the line will stay marking. The figure shows 1, 1.5, and 2 stop bits.

NOTE

This description applies to signals at the DUART pins. Signals measured on the interchange circuits will have the opposite polarity to those shown.

The data rate clock which times the serial data, is 16 times the programmed data rate. Arrows show when the bits are tested for polarity.

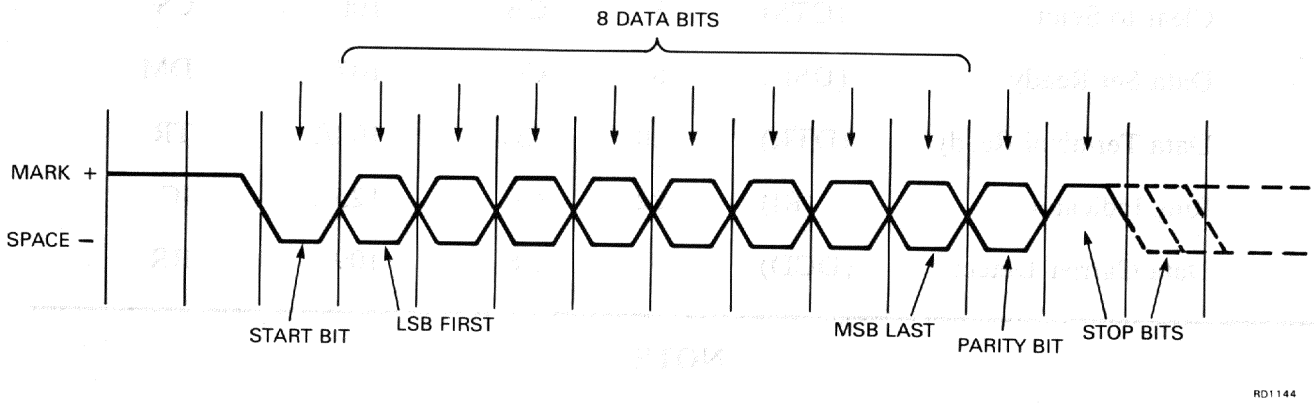


Figure 1-4 Serial Character Format

The DHV11 allows the following serial character formats:

- Characters of 5, 6, 7, or 8 bits with or without parity and with 1 stop bit
- Characters of 6, 7, or 8 bits with or without parity and with 2 stop bits
- Characters of 5 bits with or without parity and with 1.5 stop bits.

1.4.2.3 Line Receivers – The serial line receivers used in this module are 9637AC or equivalent. They convert the EIA input signals to TTL levels suitable for the DUARTs.

Signals are inverted by the receivers.

1.4.2.4 Line Transmitters – The serial line transmitters used in this module are 9636AC or equivalent. They convert TTL level signals from the DUARTs to EIA levels on the data lines.

Signals are inverted by the transmitters.

1.4.2.5 Speed/Distance Considerations – The maximum data rate which can be used on a line depends upon a number of factors. These are:

1. The characteristics of the line transmitters and receivers
2. The characteristics of the serial cable (or link)
3. The length of the cable
4. Noise (interference) which affects the line.

A 'speed against distance' table for typical conditions is provided in Section 2.6.6.

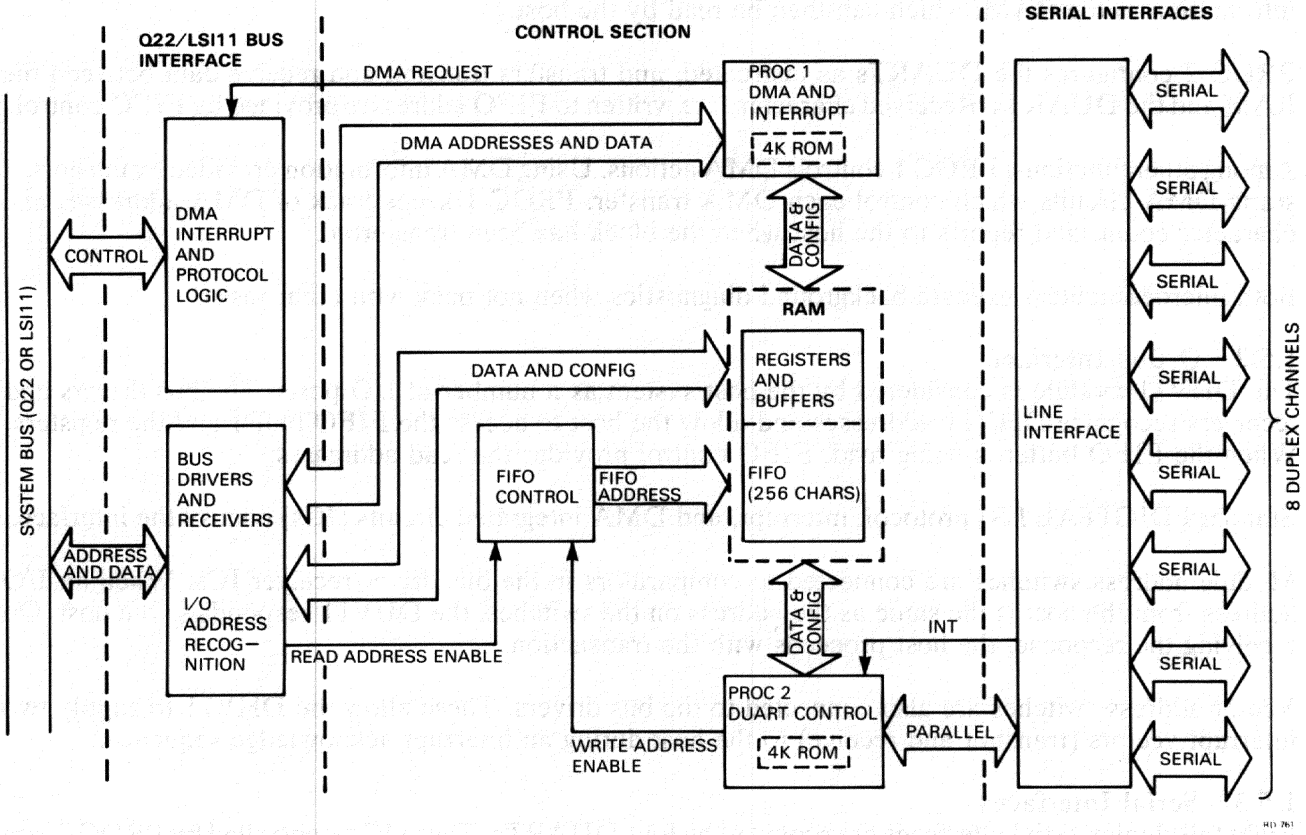


Figure 1-5 DHV11 Functional Block

1.5 FUNCTIONAL DESCRIPTION

1.5.1 Control Function

In the DHV11 module (Figure 1-5), data is transferred by three methods:

1. By DMA. Blocks of data are transferred from system memory to the serial interface. DMA data is routed via the bus receivers, PROC1, the RAM, and PROC2.

2. In the non-DMA mode, single characters can be transferred from the host system to the serial interface. The route for single characters is via the bus receivers, the RAM, PROC1, the RAM, and PROC2.

3. Single characters can be transferred from the serial interface to the host system. The route for received characters is via PROC2, the FIFO buffer, and the bus drivers.

At the center of the control section is a 1K-word RAM. By writing control words to registers in the RAM, the host can indirectly configure and command the module. The host can also write data bytes to registers in the RAM.

Two microcomputers (PROC 1 and PROC 2), which contain their own programs in internal ROM, scan the RAM in order to detect a new configuration, or data to be transferred. They also write status information to the RAM, which can then be read by the host.

PROC 2 configures the DUARTs as instructed, and transfers transmit and receive data between the RAM and the DUARTs. Received characters are written to FIFO addresses provided by FIFO control.

Among other functions, PROC 1 controls DMA actions. Using DMA information provided by the host, it starts DMA circuits which control each DMA transfer. PROC 1 keeps track of DMA addresses and character count, and reports to the host when the block has been transferred.

Both microcomputers execute background diagnostics when not busy with other tasks.

1.5.2 Q-Bus Interface

The DHV11 module is considered by the host system as a number of I/O ports. The bus drivers and receivers recognize DHV11 addresses and allow the host to access the FIFO buffer and the registers. When the FIFO buffer is being read, FIFO control provides the read addresses.

Standard DIGITAL LSI protocol, interrupt, and DMA integrated circuits (ICs) control the interface.

Module address switches are connected to comparators in the bus driver/receiver ICs. When an I/O address from the host is the same as the address on the switches, the DHV11 responds to the host. On receiving the response, the host proceeds with the transaction.

Vector address switches are also connected to the bus drivers. These allow the DHV11 to supply two interrupt vectors (transmit and receive) to the host during an interrupt acknowledge sequence.

1.5.3 Serial Interfaces

Eight full-duplex serial interfaces are provided by four DUARTs. These ICs, controlled by PROC 2, are configured as needed by the host system. They carry out the serial/parallel and parallel/serial conversion. When a received character is assembled PROC 2 is interrupted.

The status of modem control lines for each channel is polled by PROC 2. If programmed to do so, the DHV11 will report changes of modem status to the host. Such reports are made via the FIFO buffer and the device registers.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains information on how to prepare and install the DHV11 option. It contains sections on the following:

- Device and vector address selection
- Rules for backplane positioning
- Recommended cables
- Test connectors
- Floating address and vector assignment
- Testing after installation.

2.2 UNPACKING AND INSPECTION

There are a number of versions of the DHV11, all of which are based on the module kit DHV11-M. This may be ordered with one of the three cabinet kits listed below. Examine all parts for physical damage. Report damaged or missing items to the shipper and the DIGITAL representative.

DHV11-M:

Part Number	Description	Quantity
M3104	DHV11 module	1
EK-DHV11-TM	Technical manual	1

CK-DHV11-AA, 21-inch cab-kit:

Part Number	Description	Quantity
H3173-A	Distribution panel	2
BC05L-1K	40-conductor cable	2
H325	Line loopback connector	1
H3277	Staggered loopback connector	1
90-06021-01	Bolt	8
90-06633-00	Washer	8

CK-DHV11-AB, 12-inch cab-kit:

As for 21-inch cab-kit but with BC05L-01 cables.

CK-DHV11-AC, 30-inch cab-kit:

As for 21-inch cab-kit but with BC05L-2F cables.

NOTE

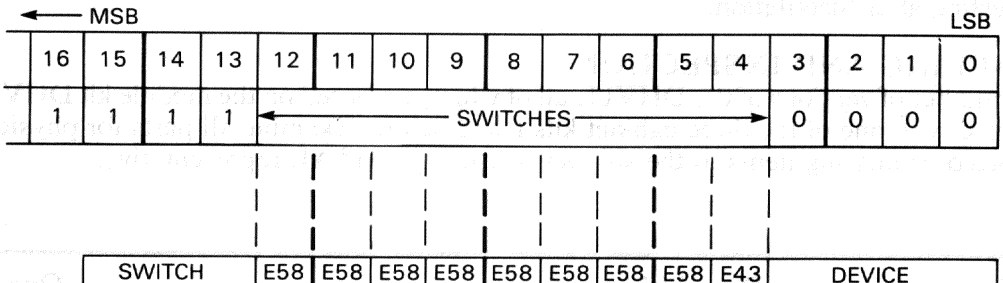
BC05L-1K is 53.34 cm (21 inches) long
BC05L-01 is 30.48 cm (12 inches) long
BC05L-2F is 76.20 cm (30 inches) long

2.3 INSTALLATION CHECKS

2.3.1 Address Switches

The device address for the DHV11 is set on switchpacks E58 and E43 (Figure 2-1). Table 2-1 explains the relationship between device addresses and switch positions. The table gives the Q22 bus address for each entry. The equivalent Q16 and Q18 bus addresses will be 16xxxx and 76xxxx respectively.

Table 2-1 Device Address Selection Guide



SWITCH NUMBER	E58 1	E58 2	E58 3	E58 4	E58 5	E58 6	E58 7	E58 8	E43 1	DEVICE ADDRESS
									ON	17760020
								ON		17760040
								ON	ON	17760060
							ON			17760100
						ON				17760200
						ON	ON			17760300
					ON					17760400
					ON		ON			17760500
					ON	ON				17760600
					ON	ON	ON			17760700
				ON						17761000
			ON							17762000
			ON	ON						17763000
		ON								17764000
	ON									17770000

ON = SWITCH CLOSED TO RESPOND TO A LOGICAL 1 ON THE BUS

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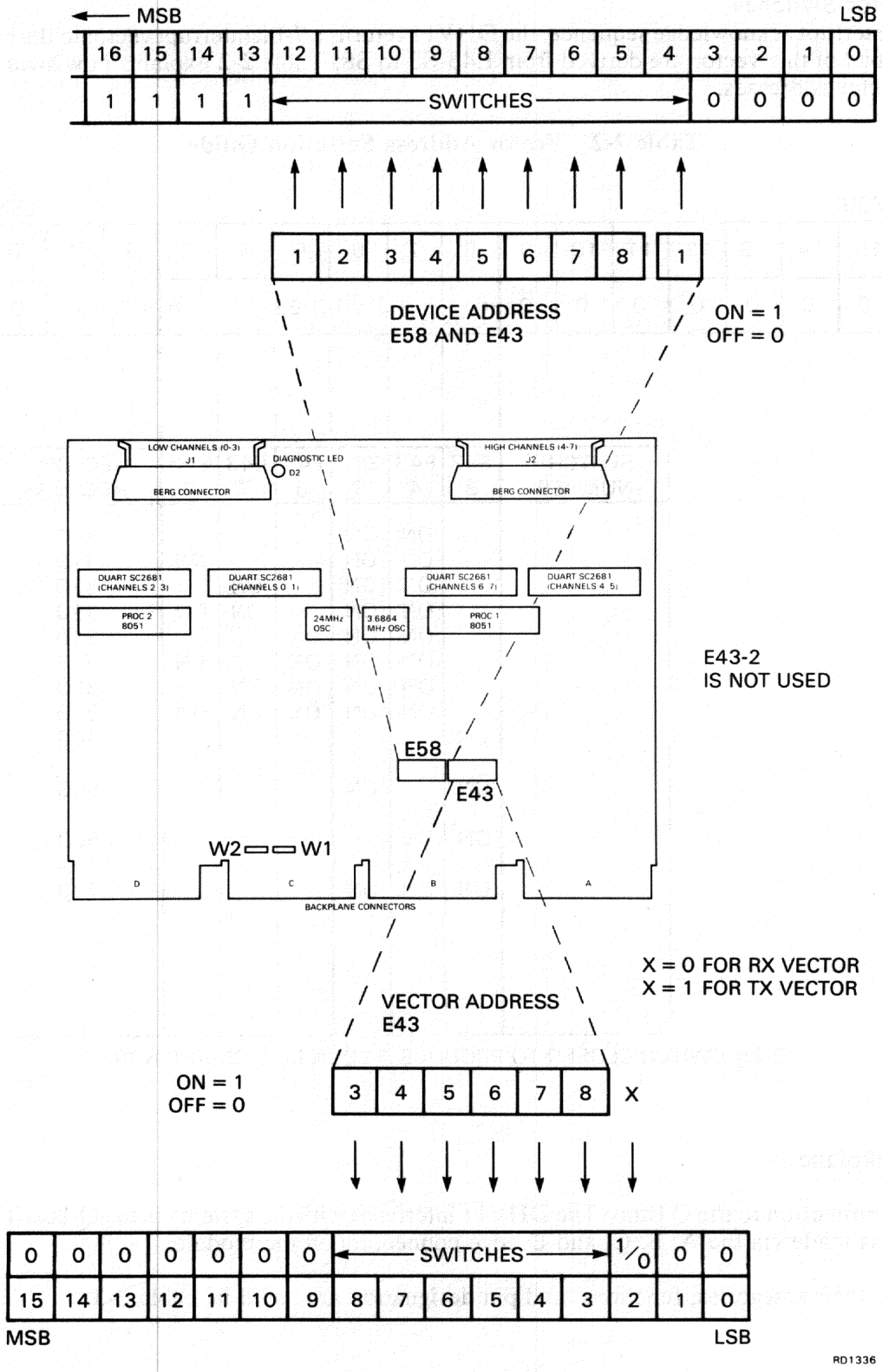

Figure 2-1 Switch and Jumper Locations

2.3.2 Vector Switches

During an interrupt acknowledge sequence, the DHV11 returns a 7-bit interrupt vector to the host. The six high-order bits of this vector are derived from E43-S3 to S8. Table 2-2 explains how switch positions relate to vector addresses.

Table 2-2 Vector Address Selection Guide

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	← SWITCHES →						1/0	0	0

SWITCH NUMBER	E43 3	E43 4	E43 5	E43 6	E43 7	E43 8	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700

ON = SWITCH CLOSED TO PRODUCE A LOGICAL 1 ON THE BUS

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2.3.3 Backplane

2.3.3.1 Connection to the Q Bus – The DHV11 interfaces with the system via the Q-bus. The physical connection is made via the A, B, C, and D edge connectors on the module.

Bus signals, their categories, functions, and pin designation are listed in Table 2-3.

Table 2-3 DHV11 Bus Connections

Category	Signal	Function	Pin Number
Data/Address	BDAL0.L – 1.L	Data/Address Lines	AU2 – AV2
	BDAL1.L – 15.L		BE2 – BV2
	BDAL16.L – 17.L		AC1 – AD1
	BDAL18.L – 21.L		BC1 – BF1
Data Control	BDOUT.L	Data Output Strobe	AE2
	BRPLY.L	Reply Handshake	AF2
	BDIN.L	Data Input Strobe	AH2
	BSYNC.L	Synchronize Strobe	AJ2
	BWTBT.L	Write Byte Control	AK2
	BBS7.L	I/O Page Select	AP2
Interrupt Control	BIRQ.L	Int. Req. Level 4	AL2
	BIAKI.L	Int. Ack. Input	AM2
	BIAKO.L	Int. Ack. Output	AN2
DMA Control	BDMR.L	DMA Request	AN1
	BDMGI.L	DMA Grant Input	AR2
	BDMGO.L	DMA Grant Output	AS2
	BSACK.L	Bus Grant Acknowledge	BN1
System Control	BINIT.L	Initialization Strobe	AT2
Power Supplies	+5 V	DC Volts	AA2 – DA2
	+12 V	DC Volts	BD2
Grounds	GND	Ground Connections	AC2 – DC2
	GND	Ground Connections	AT1 – DT1
	GND	Ground Connections	AJ1 – BJ1
	GND	Ground Connections	AM1 – BM1

2.3.3.2 Bus Grant Continuity Jumpers – Backplanes suitable for DHV11 fall into two groups:

Q/CD – Q-bus on A and B connectors, user-defined signals on C and D
Q/Q – Q-bus on A and B, and C and D connectors.

In Q/CD backplanes, bus grant signals pass through each installed module via the A and B connectors of each bus slot.

Q/Q backplanes are designed so that two dual-height options can be installed in a quad-height bus slot. The Q-bus lines are routed as follows:

AB, first slot
CD, first slot
CD, second slot
AB, second slot and so on.

Lines AM2, AN2, CM2, and CN2 (BIAK) and AR2, AS2, CR2, and CS2 (BDMG) carry the bus grant signals. Figure 2-2 uses BIAK as an example of bus grant routing. The same method is used for continuity of BDMG.

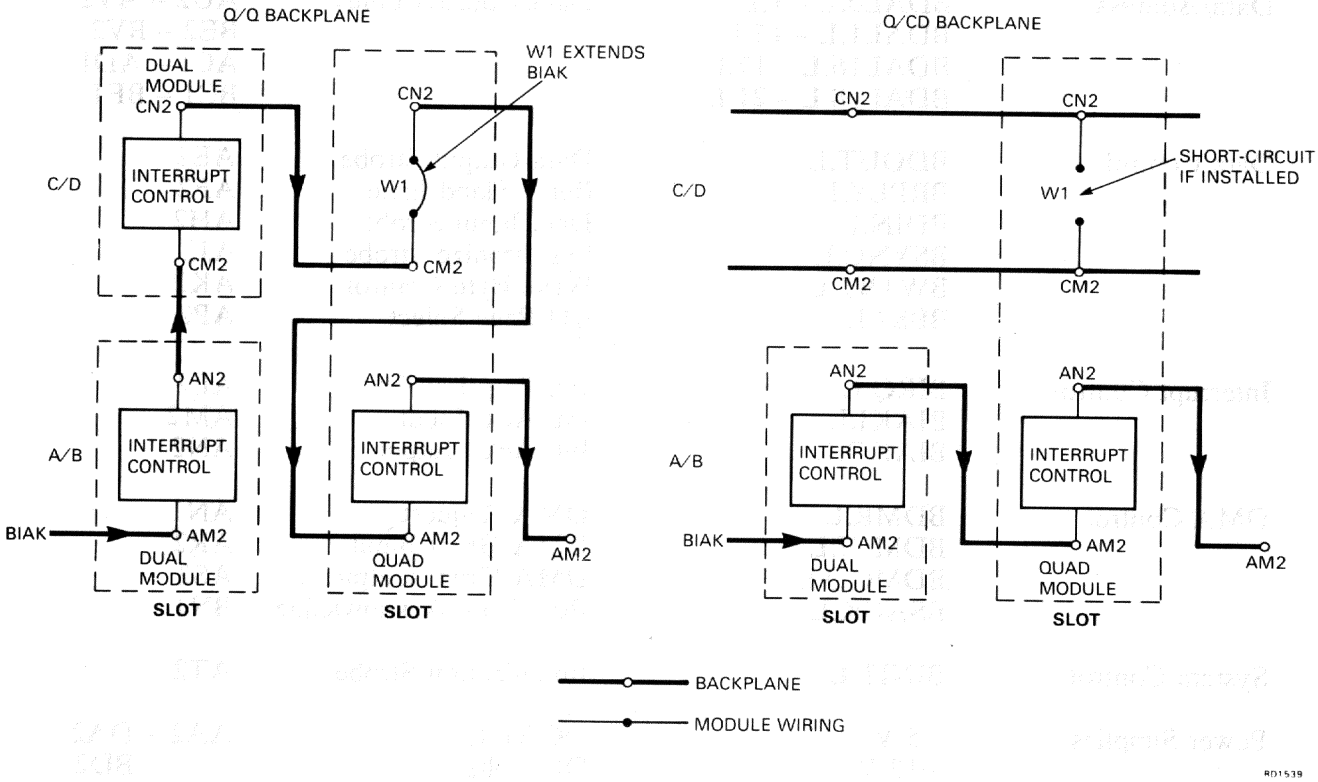


Figure 2-2 Bus Grant Continuity

Each dual-height module will extend the continuity of bus grant signals BIAK and BDMG to the next module.

If a quad-height option is installed, jumpers perform the grant continuity function of a dual option installed on C and D.

Therefore, with a Q/Q backplane, W1 and W2 should be installed. H9275 and H9270 are examples of this type of backplane.

In a Q/CD backplane, pins CM2, CN2, CR2, and CS2 are available for user-defined signals. Therefore W1 and W2 must be removed. H9276 and H9273 are examples of this type of backplane.

2.4 PRIORITY SELECTION

The DHV11 uses the BIRQ4 line to request interrupt service. It does not monitor any of the higher-level interrupt request lines. Because of this, both the interrupt request and DMA (non-processor request) priorities of the DHV11, are selected by the position of the DHV11 on the bus.

The bus (backplane) position may be a compromise between DMA and interrupt priority requirements. As a general rule, DMA request priorities should be considered first, and then interrupt (bus) requests.

2.4.1 DMA Request

DMA request priority is usually selected on a basis of throughput. The faster devices (higher throughput) will usually have priority over slower DMA devices; for example, disk, tape, and then communications devices. This is because a fast device will usually reach an overrun/underrun condition sooner than a slower device.

The simple approach can be further complicated by hardware buffering in the device. For example, a disk controller may read a full sector of information into a hardware buffer. It may then raise a DMA request to move the data to system memory. If the request is not serviced immediately, there is no danger of data loss. However, a magnetic tape unit or a communications device without buffering may need to be serviced quickly. In this case the slower unit might be serviced first. This method of priority selection could, of course, reduce disk throughput.

The system designer should consider the following four factors in determining DMA priorities:

1. Device average service time
2. Maximum wait time to be allowed (before loss of data)
3. Average time between DMA requests
4. Slack time.

Using the above parameters, the system designer should assume that all DMA requests are made at the same time. He should then check that his selected priority sequence does not violate the parameters of any DMA device.

If there is only one DMA device in the system there is no DMA contention. The device's position on the bus will be determined by its interrupt (BIRQ) priority.

NOTE

If the system memory needs refresh cycles via the bus, these should be considered as DMA requests.

2.4.2 Interrupt Request

Interrupt requests have four levels of priority. The lowest is Level 4 and the highest is Level 7. Requests are made on bus interrupt request lines BIRQ4 to BIRQ7. To avoid contention, lower-priority devices usually monitor the higher request lines.

Within any priority group, priority is decided by backplane position. The most time-critical interrupts must be nearer the CPU.

There are two common types of configuration for devices which need interrupt service:

1. The position-independent configuration
2. The position-dependent configuration.

In the position-independent configuration, devices of different priority groups can be placed anywhere in the backplane.

In the position-dependent configuration, devices of different priority groups are positioned in descending order of priority from the CPU.

Because the DHV11 is a Level 4 device which does not monitor higher request lines, it must be positioned after all devices that do. Therefore DHV11 priority is position dependent in either configuration.

By assuming that all interrupts are raised at the same time, the system designer can check his priority sequence as for DMA requests.

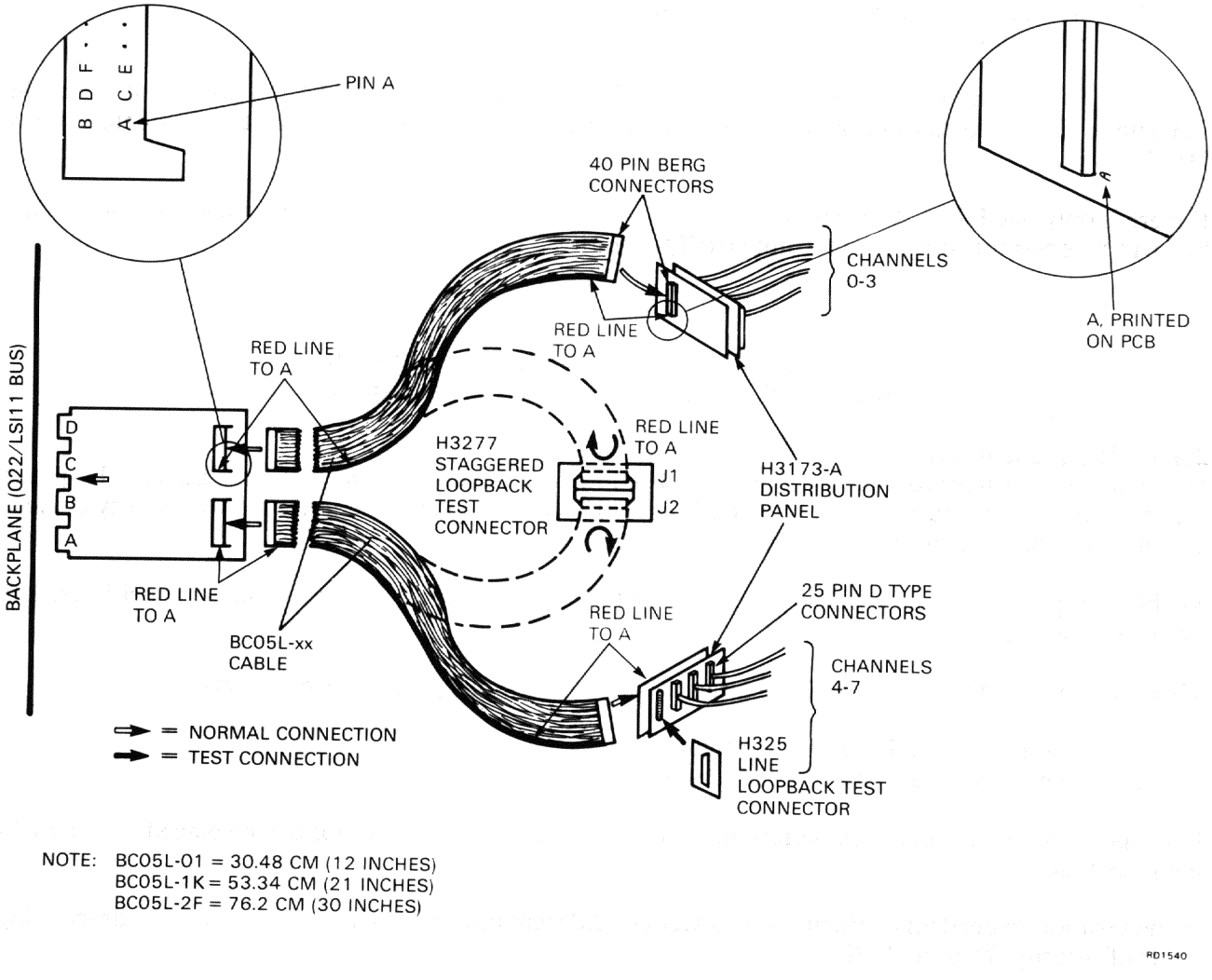
The final configuration can be tested to some extent by the DECX/11 diagnostic. Some changes may be needed for optimum performance.

2.5 MODULE INSTALLATION

Once the backplane position of the DHV11 has been defined, the module can be installed and the backplane checked with a testmeter.

CAUTION

Switch off power before inserting or removing modules. Be careful not to snag module components on the card guides or adjacent modules.



NOTE: BC05L-01 = 30.48 CM (12 INCHES)
BC05L-1K = 53.34 CM (21 INCHES)
BC05L-2F = 76.2 CM (30 INCHES)

RD1540

Figure 2-3 DHV11 Installation

1. Connect the BC05L cables to J1 and J2. Figure 2-3 shows how the parts of the option connect together.

2. Install the module in its correct backplane position as defined in Section 2.4.

3. Check that +5 V is present between AA2 and ground.

4. Check that +12 V is present between BD2 and ground.

2.6 CABLES AND CONNECTORS

2.6.1 Distribution Panel

Each H3173-A distribution panel adapts one of the DHV11's berg connectors to four subminiature D-type RS-232-C connectors. Noise filtering is provided on each pin of the RS-232-C connectors. This reduces electromagnetic radiation from the cables. It also provides the logic with some protection against static discharge.

Figure 2-4 shows the layout and Figure 2-5 shows the circuit. There is no CCITT equivalent of EIA circuit AA (protective ground). The 0-ohm link W1 can be removed to disconnect this circuit as needed.

Table 2-4 is for two distribution panels. Information in parentheses applies to channels 4 to 7.

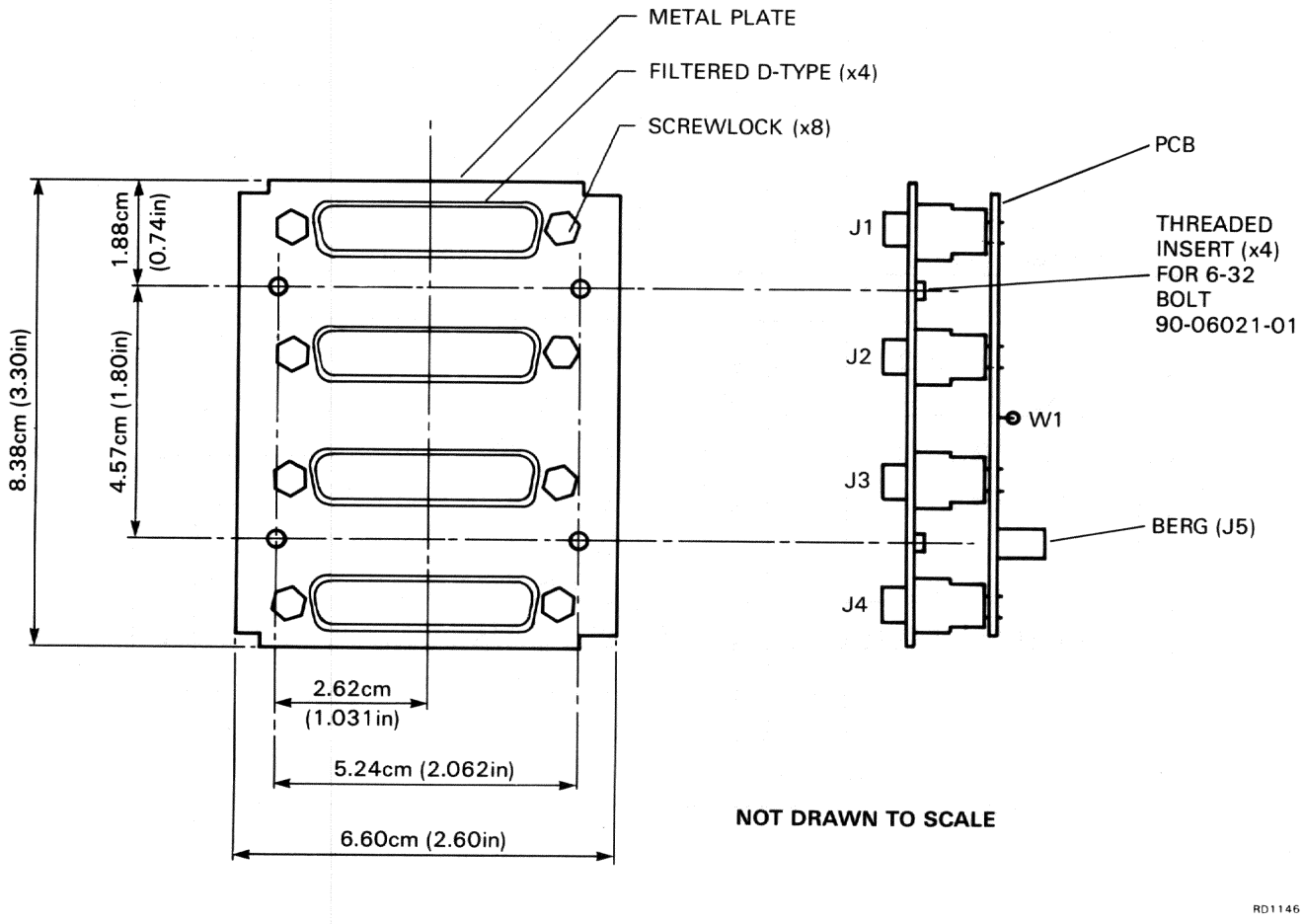


Figure 2-4 H3173-A Layout

The following is an example of the use of Table 2-4.

Signal TXD0 is the Transmitted Data line for channel 0. Its CCITT circuit number is 103. It is connected to J5 pin B on the H3173-A for channels 0 to 3.

Signal TXD4 is the Transmitted Data line for channel 4. Its CCITT circuit number is 103. It is connected to J5 pin B on the H3173-A for channels 4 to 7.

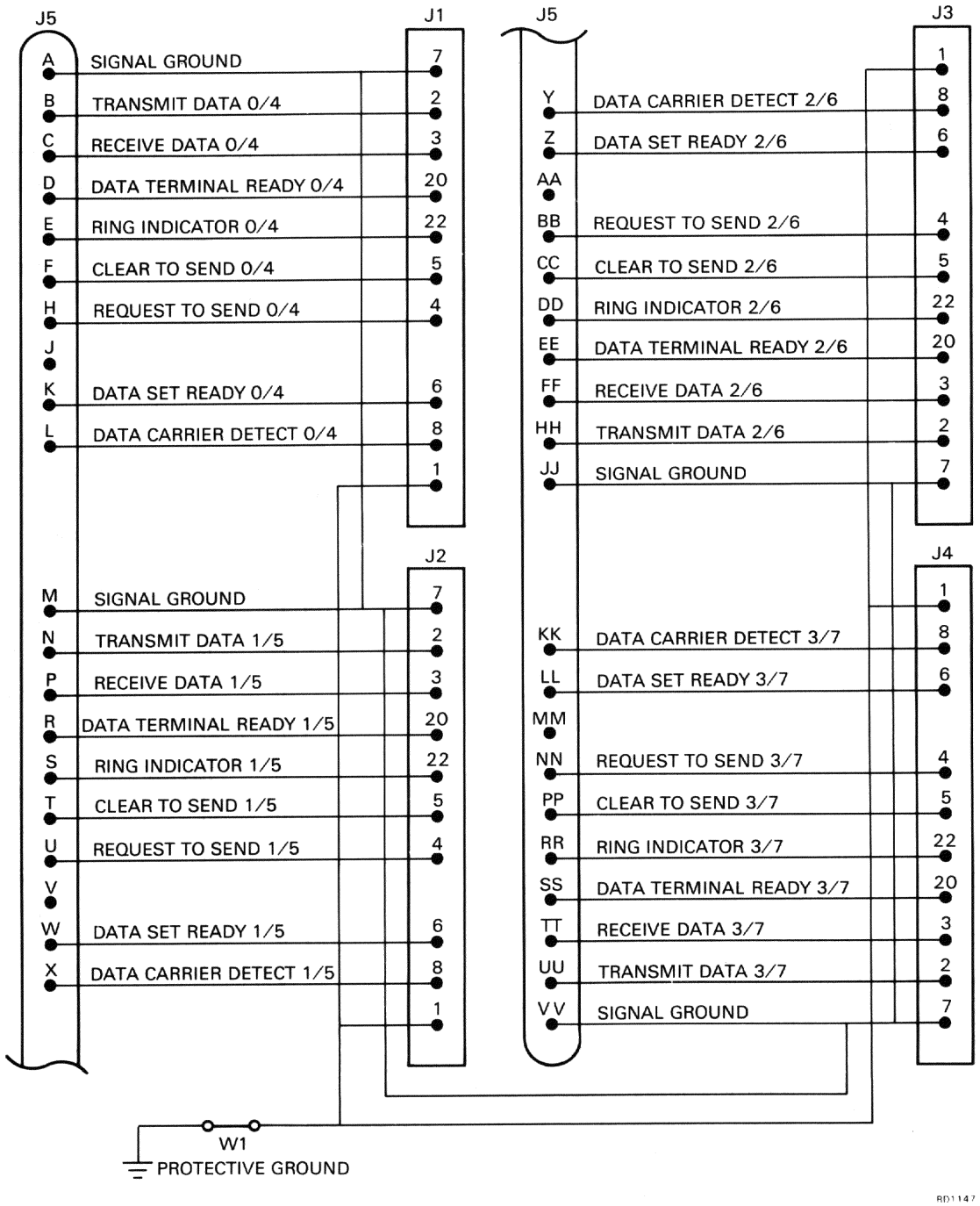


Figure 2-5 H3173-A Circuit Diagram

Table 2-4 H3173-A Connections

Signal	Name	Circuit No.	J5 Pin No.
SIG GND 0(4)		102	1-A (2-A)
TXD0(4)	Transmitted Data	103	1-B (2-B)
RXD0(4)	Received Data	104	1-C (2-C)
DTR0(4)	Data Terminal Ready	108/2	1-D (2-D)
RI0(4)	Ringing Indicator	125	1-E (2-E)
CTS0(4)	Clear to Send	106	1-F (2-F)
RTS0(4)	Request to Send	105	1-H (2-H)
DSR0(4)	Data Set Ready	107	1-K (2-K)
DCD0(4)	Data Carrier Detected	109	1-L (2-L)
SIGGND 1(5)		102	1-M (2-M)
TXD1(5)		103	1-N (2-N)
RXD1(5)		104	1-P (2-P)
DTR1(5)		108/2	1-R (2-R)
RI1(5)		125	1-S (2-S)
CTS1(5)		106	1-T (2-T)
RTS1(5)		105	1-U (2-U)
DSR1(5)		107	1-W (2-W)
DCD1(5)		109	1-X (2-X)
DCD2(6)		109	1-Y (2-Y)
DSR2(6)		107	1-Z (2-Z)
RTS2(6)		105	1-BB (2-BB)
CTS2(6)		106	1-CC (2-CC)
RI2(6)		125	1-DD (2-DD)
DTR2(6)		108/2	1-EE (2-EE)
RXD2(6)		104	1-FF (2-FF)
TXD2(6)		103	1-HH (2-HH)
SIG GND 2(6)		102	1-JJ (2-JJ)
DCD3(7)		109	1-KK (2-KK)
DSR3(7)		107	1-LL (2-LL)
RTS3(7)		105	1-NN (2-NN)
CTS3(7)		106	1-PP (2-PP)
RI3(7)		125	1-RR (2-RR)
DTR3(7)		108/2	1-SS (2-SS)
RXD3(7)		104	1-TT (2-TT)
TXD3(7)		103	1-UU (2-UU)
SIG GND 3(7)		102	1-VV (2-VV)

2.6.2 Staggered Loopback Test Connector H3277

(See Figure 2-6.) The H3277 test connector is used during diagnostic tests. It allows all channels to be tested. Using this connector, you can trace a channel fault to one of two channels.

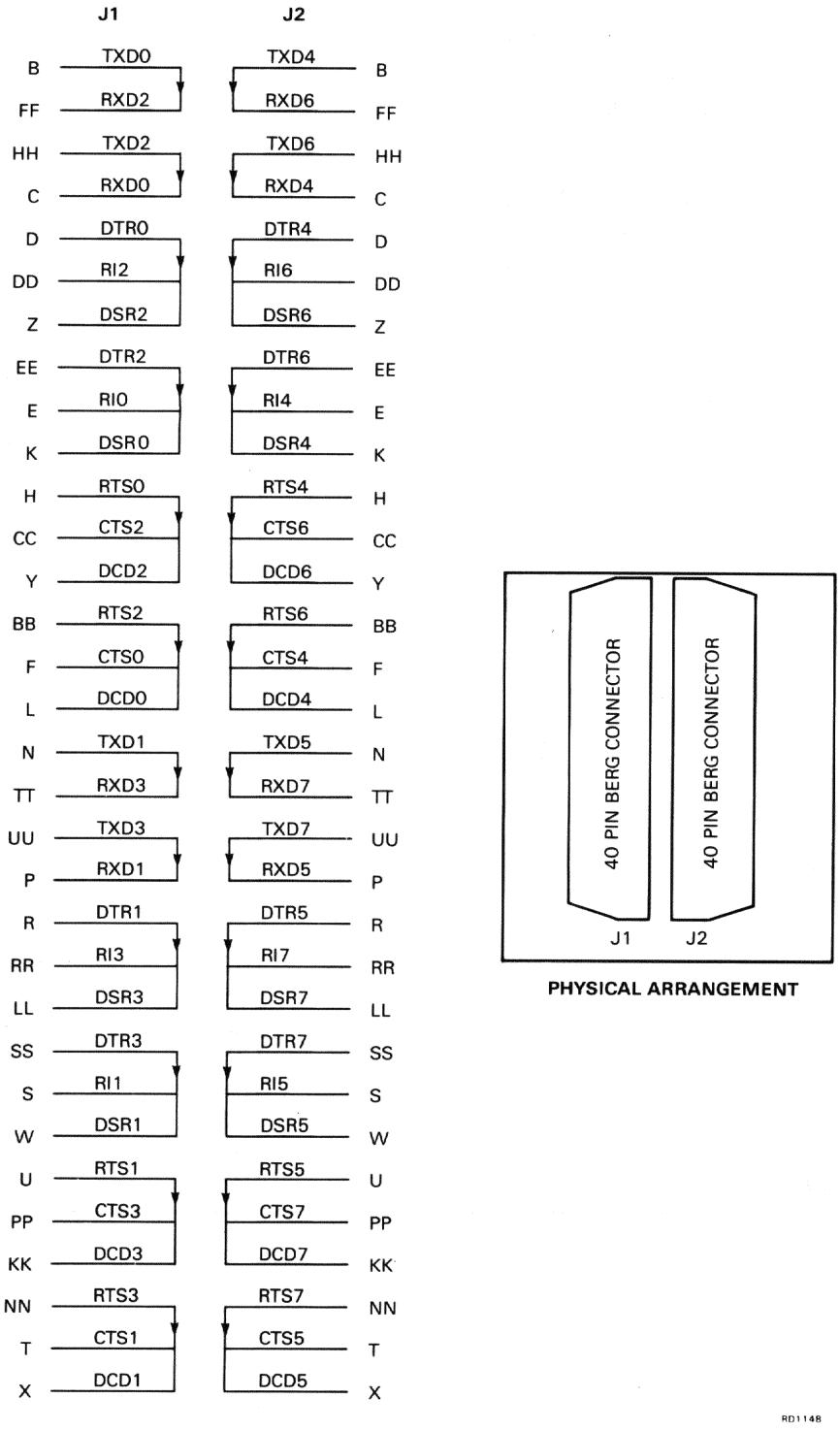


Figure 2-6 Staggered Loopback Test Connector

2.6.3 Line Loopback Test Connector H325

This connector is shown in Figure 2-7. It can be used during diagnostic tests to trace a fault to a single channel.

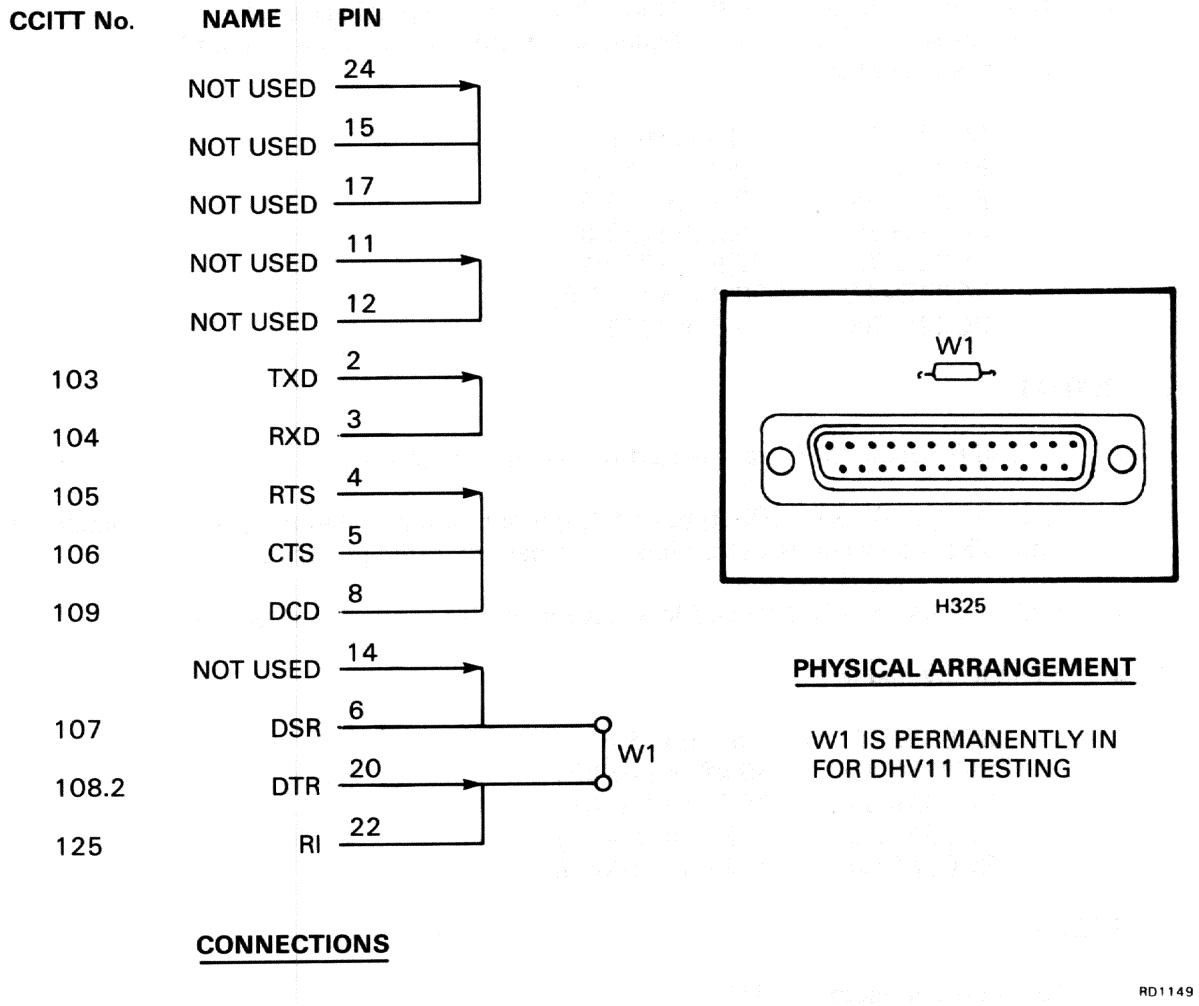


Figure 2-7 Line Loopback Test Connector

2.6.4 Null Modem Cables

Null modem cables are used for local RS-232-C connection. Because of Federal Communications Commission (FCC) regulations, the cable specifications for the United States and Canada are different from those for non-FCC countries. Other countries may also have similar ElectroMagnetic Interference (EMI) control regulations. EMC/RFI shielded cabinets (see glossary) are now available for systems which conform to FCC requirements.

Recommended null modem cables are as follows:

1. BC22D (for EMC/RFI shielded cabinets)

   - Round 6-conductor fully shielded cable to FCC specification
   - Subminiature 25-pin D-type female connector moulded on each end
   - Lengths available:

     BC22D-10 – 3.1 m (10 ft)
     BC22D-25 – 7.62 m (25 ft)
     BC22D-35 – 10.72 m (35 ft)
     BC22D-50 – 15.24 m (50 ft)
     BC22D-75 – 22.9 m (75 ft)
     BC22D-A0 – 30.48 m (100 ft)
     BC22D-B5 – 76.2 m (250 ft).

2. BC03M

   - Round 6-conductor (three twisted pairs), each pair shielded
   - Cables over 30.48 m (100 ft) have a 25-pin subminiature D-type female connector at one end. The other end is unterminated for passing through conduit.
   - Cables 30.48 m (100 ft) and less have a similar connector at each end.
   - Lengths available:

     BC03M-25 – 7.62 m (25 ft)
     BC03M-A0 – 30.48 m (100 ft)
     BC03M-B5 – 76.2 m (250 ft)
     BC03M-E0 – 152.4 m (500 ft)
     BC03M-L0 – 304.8 m (1000 ft).

3. BC22A

   - Round 6-conductor cable
   - Subminiature 25-pin D-type female connector moulded at each end
   - Lengths available:

     BC22A-10 – 3.1 m (10 ft)
     BC22A-25 – 7.62 m (25 ft).

Cables of groups 1, 2, and 3 are all connected as in Figure 2-8. The cables are not polarized. They can be connected either way round.

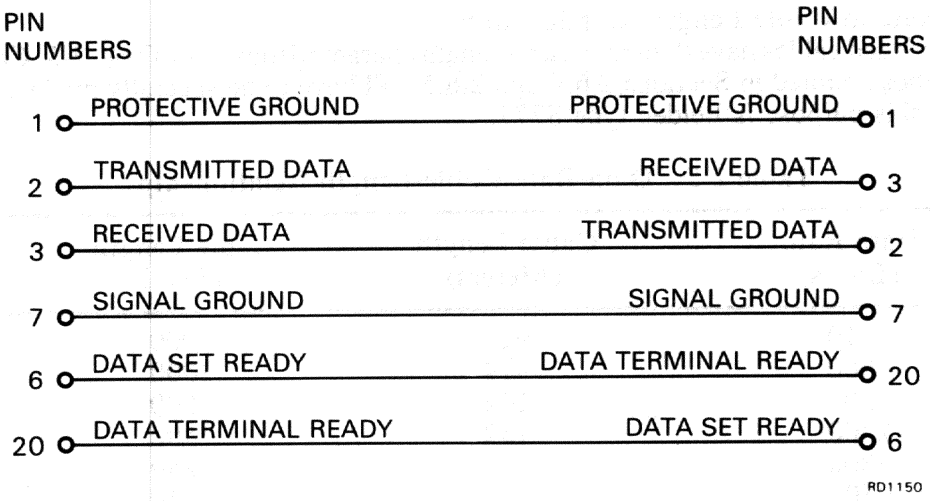


Figure 2-8 Null Modem Cable Connections

2.6.5 Full Modem Cables

Recommended full modem cables are as follows:

1. BC22F (for EMC/RFI shielded cabinets)

   - Round 25-conductor fully shielded cable
   - Subminiature 25-pin D-type female connector on one end, male connector on the other
   - Lengths available:

     BC22F-10 – 3.1 m (10 ft)
     BC22F-25 – 7.62 m (25 ft)
     BC22F-35 – 10.72 m (35 ft)
     BC22F-50 – 15.24 m (50 ft)
     BC22F-75 – 22.9 m (75 ft)

2. BC05D

   - Round 25-conductor cable
   - Subminiature 25-pin D-type female connector on one end, male connector on the other
   - Lengths available:

     BC05D-10 – 3.1 m (10 ft)
     BC05D-25 – 7.62 m (25 ft)
     BC05D-50 – 15.24 m (50 ft)
     BC05D-60 – 18.6 m (60 ft)
     BC05D-A0 – 30.48 m (100 ft).

CAUTION

In some countries, protective hardware may be needed when connecting to certain lines. Refer to the national regulations before making a connection.

2.6.6 Data Rate to Cable Length Relationships

All the recommended cables have data rate/cable length characteristics as in Table 2-5. Cables of lengths different from those quoted in Sections 2.6.4 and 2.6.5 will have to be specially made. A suitable non-FCC cable for this purpose is Belden type 8777.

Table 2-5 Data-Rate/Cable-Length Relationships

Data Rate (Bits/s)	Cable Length (Meters)	Cable Length (Feet)
110	914	3000
300	914	3000
1200	152	500
2400	152	500
4800	76	250
9600	76	250

NOTE

Cables longer than 15.24 m (50 ft) or with a capacitance greater than 2.5 nanofarads, violate RS-232-C and V.28 specifications. These are not supported by DIGITAL.

2.7 MULTIPLE COMMUNICATIONS OPTIONS

2.7.1 Floating Device Addresses

On UNIBUS and Q-bus systems, a band of addresses ($xxx60010_8$ to $xxx63776_8$) in the top 4K words is assigned as floating address space (xxx means all top address bits = 1).

Options which can be assigned floating device addresses are listed in Table 2-6. This table gives the sequence of addresses for both UNIBUS and Q-bus options. For example, the address sequences could be:

UNIBUS	Q-Bus	
DJ11	DJ11	
DH11	DH11	
DQ11	DQ11	
DU11	DUV11	
DUP11	DUP11	
DMC11	DMC11	
DZ11	DZV11	and so on.

Having one list allows us to use one set of configuration rules and one configuration program.

Table 2-6 Floating Device Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)	
1	DJ11	4	10	
2	DH11	8	20	
3	DQ11	4	10	
4	DU11, DUV11	4	10	
5	DUP11	4	10	
6	LK11A	4	10	
7	DMC11/DMR11	4	10	(DMC before DMR)
8	DZ11/DZV11, DZS11, DZ32	4	10	(DZ11 before DZ32)
9	KMC11	4	10	
10	LPP11	4	10	
11	VMV21	4	10	
12	VMV31	8	20	
13	DWR70	4	10	
14	RL11, RLV11	4	10	*
15	LPA11-K	8	20	*
16	KW11-C	4	10	
17	Reserved	4	10	
18	RX11/RX211, RXV11/RXV21	4	10	* (RX11 before RX211)
19	DR11-W	4	10	
20	DR11-B	4	10	**
21	DMP11	4	10	
22	DPV11	4	10	
23	ISB11	4	10	
24	DMV11	8	20	
25	DEUNA	4	10	*
26	UDA50	2	4	*
27	DMF32	16	40	
28	KMS11	6	20	
29	VS100	8	20	
30	Reserved	2	4	
31	KMV11	8	20	
32	DHV11	8	20	

NOTES

1. DZ11-E and DZ11-F are treated as two DZ11s.

2. * = First device of this type has a fixed address. Any extra devices have a floating address.

3. ** = First two devices of this type have a fixed address. Any extra devices have a floating address.

Devices of the same type are given addresses in sequence, so all DZV11s have addresses higher than DUV11s and lower than RLV11s.

The column Size (Decimal), in Table 2-6, shows how many words of address space are needed for each device. The column Modulus (Octal) is the modulus used for starting addresses. For example, devices with an octal modulus of 10 must start at an address which is a multiple of 10_8. The same rule is used to select a gap address (see assignment rules) after an option, or for a nonexistent device.

The address assignment rules are as follows:

1. Addresses, starting at 17760010_8 are assigned according to the sequence of Table 2-6
2. Option and gap addresses are assigned according to the octal modulus as follows:
   a. Devices with an octal modulus of 4 are assigned an address on a 4_8 boundary (the two lowest-order address bits = 0)
   b. Devices with an octal modulus of 10 are assigned an address on a 10_8 boundary (the three lowest-order address bits = 0)
   c. Devices with an octal modulus of 20 are assigned an address on a 20_8 boundary (the four lowest-order address bits = 0)
   d. Devices with an octal modulus of 40 are assigned an address on a 40_8 boundary (the five lowest-order address bits = 0)
3. Address space equal to the device's modulus must be allowed for each device which is connected to the bus
4. A 1-word gap, assigned according to rule 2, must be allowed after the last device of each type. This gap could be bigger when rule 2 is applied to the following rank
5. A 1-word gap, assigned according to rule 2, must be allowed for each unused rank on the list if a device with a higher address is used. This gap could be bigger when rule 2 is applied to the following rank.

If extra devices are added to a system, the floating addresses may have to be reassigned in agreement with these rules.

In the following example, a brief description of address assignment is given. Note that the list includes floating vector addresses. These are explained in Section 2.6.2.

Example: One DUV11, one RLV11, and two DHV11s

Address	(Octal)	Vector
xxx60010	DJ11 gap	
xxx60020	H11 gap	
xxx60030	DQ11 gap	
xxx60040	DUV11	300
xxx60050	DUV11 gap	

Address	(Octal)	Vector
xxx60060	DUP11 gap	
xxx60070	LK11A gap	
xxx60100	DMC11 gap	
xxx60110	DZV11 gap	
xxx60120	KMC11 gap	
xxx60130	LPP11 gap	
xxx60140	VMV21 gap	
xxx60160	VMV31 gap	
xxx60170	DWR70 gap	
xxx60200	RLV11	310
xxx60210	RLV11 gap	
xxx60220	LPA11-K gap	
xxx60230	KW11-C gap	
xxx60240	reserved gap	
xxx60250	RXV11 gap	
xxx60260	DR11-W gap	
xxx60270	DR11-B gap	
xxx60300	DMP11 gap	
xxx60310	DPV11 gap	
xxx60320	ISB11 gap	
xxx60340	DMV11 gap	
xxx60350	DUENA gap	
xxx60354	UDA50 gap	
xxx60400	DMF32 gap	
xxx60420	KMS11 gap	
xxx60440	VS100 gap	
xxx60444	reserved	
xxx60460	KMV11 gap	
xxx60500	1st DHV11	320
xxx60520	2nd DHV11	330
xxx60540	DHV11 gap	

The first floating address is xxx60010. As the DJ11 has a modulus of 10_8, its gap can be assigned to xxx60010. The next available location becomes xxx60012.

As the DH11 has a modulus of 10_8, it cannot be assigned to xxx60012. The next modulo 10 boundary is xxx60020, so the DH11 gap is assigned to this address. The next available location is therefore xxx60022.

A DQ11 has a modulus of 10_8. It cannot be assigned to xxx60022. Its gap is therefore assigned to xxx60030. The next available location is xxx60032.

A DUV11 has a modulus of 10_8. It cannot be assigned to xxx60032. It is therefore assigned to xxx60040. As the 'size' of DUV11 is four words, the next available address is xxx60050.

There is no second DUV11, so a gap must be left to indicate that there are no more DUV11s. As xxx60050 is on a 10_8 boundary, the DUV11 gap can be assigned to this address. The next available address is xxx60052.

And so on.

2.7.2 Floating Vectors

Addresses between 300_8 and 774_8 are designated as the floating vector space. These addresses are assigned in sequence as in Table 2-7.

Each device needs two 16-bit locations for each vector. For example, a device with one receive and one transmit vector needs four words of vector space.

The vector assignment rules are as follows:

1. Each device occupies vector address space equal to 'Size' words. For example, the DLV11-J occupies 16 words of vector space. If its vector was 300_8, the next available vector would be at 340_8.

2. There are no gaps, except those needed to align an octal modulus.

An example of floating vector address assignment is given in Section 2.7.1.

Table 2-7 Floating Vector Address Assignments

Rank	Device	Size (Decimal)	Modulus (Octal)
1	DC11	4	10
1	TU58	4	10
2	KL11	4	10
2	DL11-A	4	10
2	DL11-B	4	10
2	DLV11-J	16	10
2	DLV11, DLV11-F	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB/BA	2	4
7	DH11 modem control	2	4
8	DR11-A, DRV11-B	4	10
9	DR11-C, DRV11	4	10
10	PA611 (reader + punch)	8	10
11	LPD11	4	10
12	DI07	4	10
13	DX11	4	10
14	DL11-C to DLV11-F	4	10
15	DJ11	4	10

Table 2-7 Floating Vector Address Assignments (Cont)

Rank	Device	Size (Decimal)	Modulus (Octal)	
16	DH11	4	10	
17	VT40	8	10	
17	VSV11	8	10	
18	LPS11	12	10	
19	DQ11	4	10	
20	KW11-W, KWV11	4	10	
21	DU11, DUV11	4	10	
22	DUP11	4	10	
23	DV11 + modem control	6	10	
24	LK11-A	4	10	
25	DWUN	4	10	
26	DMC11/DMR11	4	10	(DMC before DMR)
27	DZ11/DZS11/DZV11, DZ32	4	10	(DZ11 before DZ32)
28	KMC11	4	10	
29	LPP11	4	10	
30	VMV21	4	10	
31	VMV31	4	10	
32	VTV01	4	10	
33	DWR70	4	10	
34	RL11/RLV11	2	4	*
35	TS11, TU80	2	4	*
36	LPA11-K	4	10	
37	IP11/IP300	2	4	*
38	KW11-C	4	10	
39	RX11/RX211 RXV11/RXV21	2	4	* (RX11 before RX211)
40	DR11-W	2	4	
41	DR11-B	2	4	*
42	DMP11	4	10	
43	DPV11	4	10	
44	ML11	2	4	(MASSBUS device)
45	ISB11	4	10	
46	DMV11	4	10	
47	DUENA	2	4	*
48	UDA50	2	4	*
49	DMF32	16	4	
50	KMS11	6	10	
51	PCL11-B	4	10	
52	VS100	2	4	

Table 2-7 Floating Vector Address Assignments (Cont)

Rank	Device	Size (Decimal)	Modulus (Octal)
53	reserved	2	4
54	KMV11	4	10
55	reserved	4	10
56	IEX	4	10
57	DHV11	4	10

NOTES

1. A KL11 or DL11 used as the console, has a fixed vector.

2. * = First device of this type has a fixed vector. Any extra devices have a floating vector.

3. ML11 is a MASSBUS device which can connect to UNIBUS via a bus adapter.

2.8 INSTALLATION TESTING

The diagnostics for DHV11 are the self-test, the CVDH?? functional verification test, and DECX/11. The self-test runs automatically. CVDH?? and DECX/11 programs run under the XXDP+ monitor.

All individual device diagnostics should be run without error before DECX/11 is used.

2.8.1 Installation Tests

The following tests should be run after installation:

1. Self-test
2. CVHDA?, CVDHB?, and CVDHC? diagnostics
3. DECX/11 exerciser.

The self-test runs automatically when the bus or DHV11 is reset. If no fault is found, the diagnostic LED will flash OFF/ON/OFF and then come ON permanently. The first off state is very short and may not be seen. However, if the LED goes off before coming on permanently the diagnostic has found no faults. This does not prove that the option is serviceable.

During the self-test diagnostic operation, bytes are written to the FIFO. By reading these bytes, the engineer can receive more detailed information about the state of the DHV11. Diagnostic bytes and their interpretation are described in Section 3 of this document. The self-test can take up to 2.5 seconds.

CVDHB? and CVDHC? have four modes of operation:

1. Internal loopback
2. Staggered loopback
3. Line loopback
4. Modem loopback.

The mode can be selected by answering a prompt from the diagnostic program. Example printouts, together with a summary of the use of the diagnostic supervisor, are provided in Chapter 5.

Test the module in the following sequence. For a test flowchart see the maintenance card or Section 5.7 of this document.

1. Switch on power, or reset the system. Check the diagnostic LED sequence.

2. Run the CVDH?? diagnostics for one error-free pass (CVDHB? and CVDHC? in the internal loopback mode). Any fault message indicates a defective module.

3. Connect the H3277 staggered loopback connector and run CVDHB? and CVDHC? for one error-free pass in the staggered loopback mode. Any fault message indicates a defective DHV11 or cable. Swap cables (as in Figure 5-2, configuration C) and repeat the test in order to find the defective component.

4. Connect the BC05L-xx cables as for normal operation. Install an H325 line loopback connector at line number 0 of the distribution panel. Run CVDHB? and CVDHC? in line loopback mode on line number 0 for one error-free pass. Repeat for all lines.

5. Run the DECX/11 exerciser to verify that the DHV11 will run with other options of the system.

NOTES

The DHV11 should now be ready for connection to external equipment. See Section 2.6 if necessary, for recommended modem and null-modem cables.

The CVDH?? diagnostics can be used, in modem loopback mode, to check the communications link. The modem must be set up manually. The diagnostic will test to the point where the line is looped back.

CHAPTER 3
PROGRAMMING

3.1 SCOPE

This chapter describes the CSR and control registers, and how they are used to control and monitor the DHV11. The chapter covers:

- The bit functions and format of each register
- Programming features available to the host.

Some programming examples are also included.

Chapter 4, Sections 4.1 to 4.6, is recommended reading for anyone programming this device.

3.2 REGISTERS

The host system controls and monitors the DHV11 module via several registers which are implemented in RAM.

Command words or bytes written to the registers are interpreted and executed by the firmware. Status reports and data are also transferred via the registers.

One of the functions of the microcomputers is to scan the registers for new instructions or data.

3.2.1 Register Access

DHV11 registers occupy eight words (16 bytes) of Q-bus, memory-mapped I/O space. However, by indexing, this is expanded on the DHV11 to 114 words.

The position of the eight words within the top 4K words of memory, is switch-selected on the DHV11. In order to access the module, bits <12:4> of an I/O address must match the address switch coding.

Table 3-1 lists the DHV11 registers and their addresses. The suffix (M) means that there are eight of these registers; one for each channel. When an (M) register is accessed, the address (Table 3-1) is indexed by the contents of CSR<3:0>.

NOTE

CSR<3:0> allows 16 registers to be addressed. However, only the bottom eight registers of each block are used. Therefore CSR bit 3 must always be 0.

The term 'Base' means the lowest I/O address on the module. That is to say, when the four low-order address bits = 0.

Table 3-1 DHV11 Registers

Register		Address (Octal)	Type
Control/Status Register	(CSR)	Base	Read/Write
Receive Buffer	(RBUF)	Base + 2	Read Only
Transmit Character	(TXCHAR)	Base + 2 (M)	Write Only
Line Parameter Register	(LPR)	Base + 4 (M)	Read/Write
Line Status	(STAT)	Base + 6 (M)	Read Only
Line Control	(LNCTRL)	Base + 10 (M)	Read/Write
Transmit Buffer Address 1	(TBUFFAD1)	Base + 12 (M)	Read/Write
Transmit Buffer Address 2	(TBUFFAD2)	Base + 14 (M)	Read/Write
Transmit Buffer Count	(TBUFFCT)	Base + 16 (M)	Read/Write

NOTE

It is physically possible to write to the line status register. However, this register must not be written by the host.

Registers are accessed by instructions which use 'base + n' as a source or destination. However, before multiple (M) registers are accessed, the channel number must be written to the CSR. The following example explains this.

To read the line status register of channel 3, the following I/O commands would be executed:

```
MOVB #CHAN,@#BASE     ;WRITE CHANNEL NUMBER (SEE BELOW) TO CSR
MOV @#BASE+6,R0       ;READ THE LINE STATUS REGISTER
```

In the above example:

CHAN = 0er00011 – Where e = the RXIE bit
and r = the MRST bit (would be 0)
and 0011 = channel number 3

'Base + 6' will address a block of 16 line status registers, only eight of which are used. The DHV11 hardware will index this address by three, thereby selecting line status register number 3.

NOTE

1. **Not all register bits are specified. In a write action, all unspecified bits must be written as 0s. In a read action, unspecified bits are undefined.**

2. **The exception to the above rule is that a bit may be written as logical 1 or 0 if it is read as logical 1. That is to say, read-modify-write instructions work correctly.**

3.2.2 Register Bit Definitions

Register formats which precede the definitions of register bits, are coded as follows:

- Bits marked * may hold data set status, or special information from the diagnostic programs. These are covered in Section 3.3.10.
- Registers which are modified by reset sequences are coded as shown in Figure 3-1.

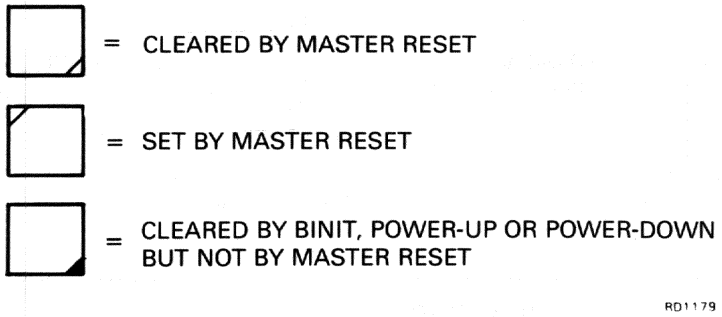
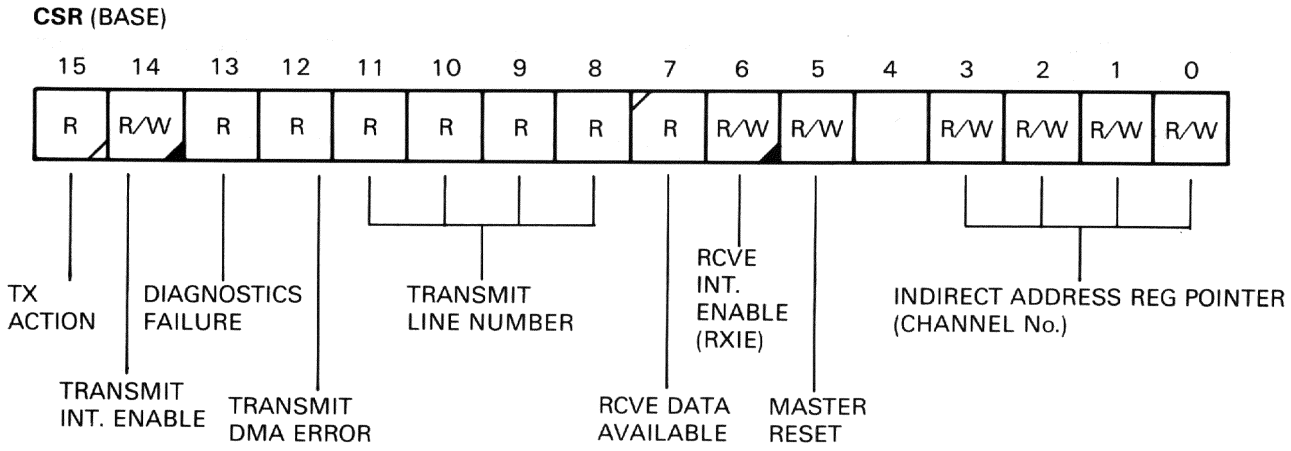


Figure 3-1 Register Coding

3.2.2.1 Control and Status Register (CSR) –

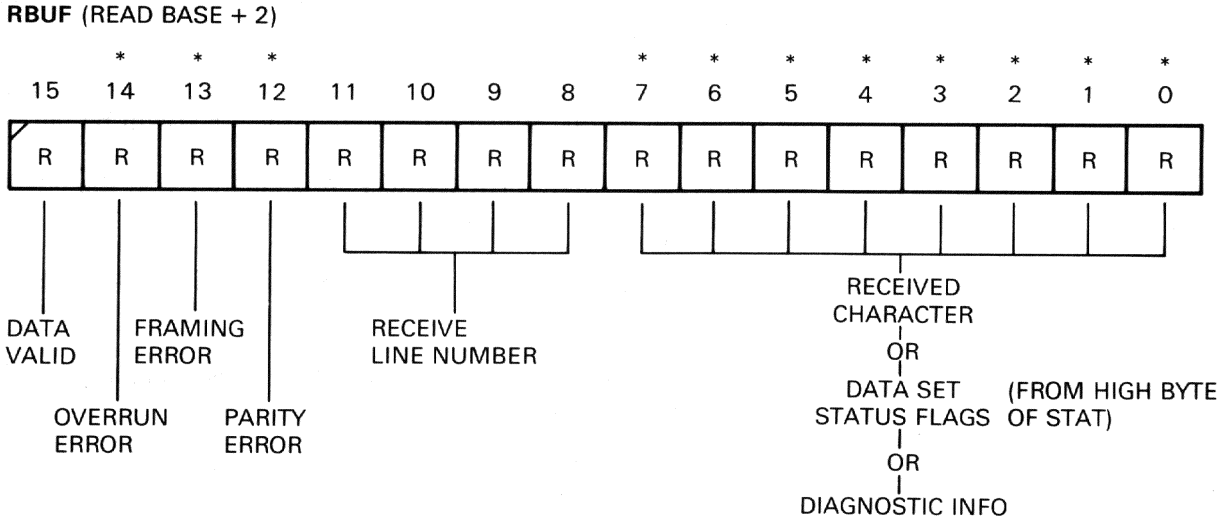


Bit	Name	Description
<3:0>	IND.ADDR.REG (Indirect Address Register) (R/W)	These bits are used to select the wanted channel register when accessing a block of indexed (M) registers. They form the binary number of the channel which is to be accessed.
5	MASTER.RESET (Master Reset) (R/W)	Set by the host, in order to reset DHV11. Stays set while DHV11 runs a self-test diagnostic, and then performs an initialization sequence. The bit is then cleared to tell the host that the process is complete. This bit is set by BINIT (bus initialization signal), or by the host processor setting CSR<5>. The host should not write to this bit when it is already set.
6	RXIE (Receiver Interrupt Enable) (R/W)	When set, this bit allows the DHV11 to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated under the following conditions: 1. RXIE is set and a character is placed into an empty FIFO 2. The FIFO is not empty and RXIE is changed from 0 to 1. Cleared by BINIT but not by MASTER.RESET.
7	RX.DATA. AVAIL (Received Data Available) (RD)	When set, indicates that a received character is available. This bit is clear when the FIFO is empty. It is used to request an RX interrupt. Set after MASTER.RESET because the FIFO contains diagnostic information.

Bit	Name	Description
<11:8>	TX.LINE (Transmit Line Number) (RD)	If TX.ACTION is set, these bits hold the binary number of the channel which has just: 1. Completed a DMA block transfer 2. Accepted a single character for transmission 3. Aborted a DMA block transfer. If TX.DMA.ERR is also set, these bits contain the binary number of the channel which has failed during a DMA transfer.
12	TX.DMA. ERROR (Transmit DMA Error) (RD)	If set with TX.ACTION also set, means that the channel indicated by CSR<11:8> has failed to transfer DMA data within 10.7 microseconds of the bus request being acknowledged, or that there is a memory parity error. TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which could not be accessed. TBUFFCT will be cleared.
13	DIAG.FAIL (Diagnostic Fail) (RD)	When set, indicates that DHV11 internal diagnostics have detected an error. The error may have been detected by the self-test diagnostic or by the BMP. This bit is associated with the diagnostic-passed LED. When it is set, the LED will be off. When it is cleared, the LED will be on. The bit is set by MASTER.RESET. It is cleared after the internal diagnostic programs have been run successfully. It is only valid after the MASTER.RESET bit CSR<5> has been - cleared.
14	TXIE (Transmit Interrupt Enable) (R/W)	When set, allows the DHV11 to interrupt the host when CSR<15> (TX.ACTION) becomes set. Cleared by BINIT but not by MASTER.RESET.
15	TX.ACTION (Transmitter Action) (RD)	This bit is set by DHV11 when: 1. The last character of a DMA buffer has left the DUART 2. A DMA transfer has been aborted 3. A DMA transfer has been terminated by the DHV11 because of nonexistent memory being addressed, or because of a memory parity error

Bit	Name	Description
		4. When a single-character programmed output has been accepted. That is to say, the character has been taken from TX.BUFF. This bit is cleared when the CSR is read by the host. Also cleared by MASTER.RESET. **NOTE** **CSR contents should only be changed by a MOV or MOVB instruction. Other instructions may lose the state of the TX ACTION bit (CSR<15>).**

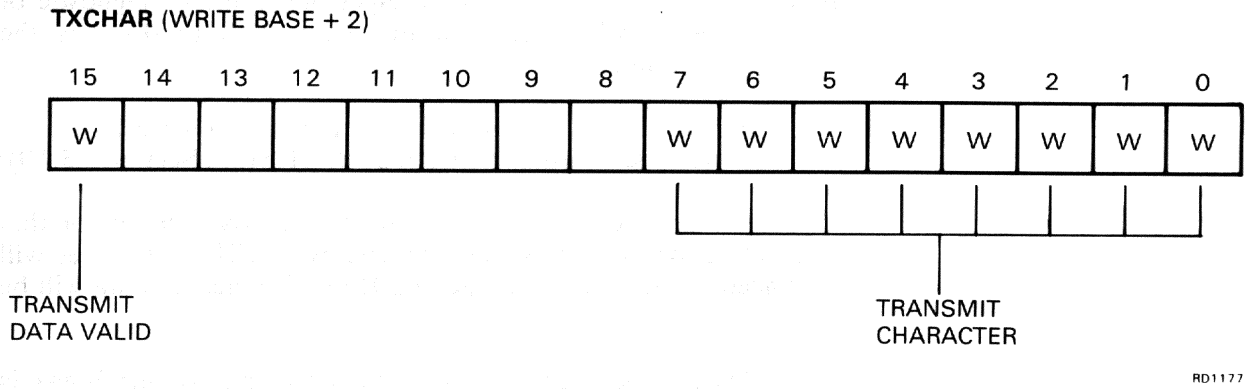
3.2.2.2 Receive Buffer (RBUF) – This register has the same address as the Transmit Character register (TXCHAR). However, a READ from 'base + 2' is interpreted by the DHV11 hardware as a READ from the FIFO. Therefore, RBUF is a 256-character register with a single-word address. The Least Significant Bit (LSB) of the character is in bit 0.



Bit	Name	Description
<7:0>	RX.CHAR (Received Character) (RD)	If RBUF<14:12> = 000, these eight bits contain the oldest character in the FIFO. The character is good. If RBUF<14:12> = 001, 010, or 011, these eight bits contain the oldest character in the FIFO. The character is bad.

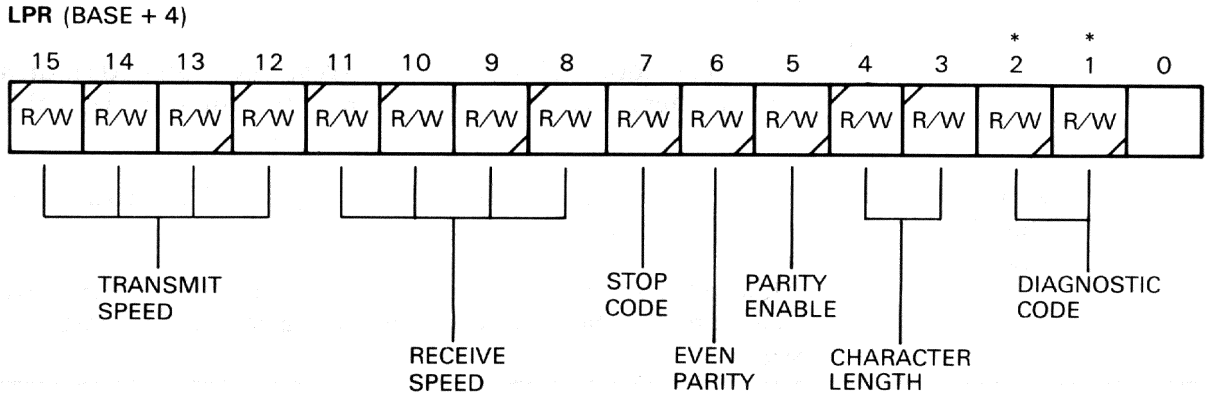
Bit	Name	Description
		If RBUF<14:12> = 111, these eight bits contain diagnostic or modem status information. In this case, RBUF<0> has the following meanings: 0 = Modem status in RBUF<7:1> (see Section 3.2.2.5) 1 = Diagnostic information in RBUF<7:1> (see Section 3.3.10). If there is an overrun condition, the UART data buffer for that channel will be cleared. A null character, with RBUF<14> set, will be placed in the receive character FIFO. The cleared data will be lost. The DHV11 does not have a break detect bit. A line break is indicated to the program as a null character with the FRAME.ERR set.
<11:8>	RX.LINE (Receive Line Number) (RD)	These bits hold the binary number of the channel on which the character of RBUF<7:0> was received or on which a data set change was reported.
12	PARITY.ERR (Parity Error) (RD)	Set if this character has a parity error and parity is enabled for the channel indicated by bits <11:8> (also see RX.CHAR).
13	FRAME.ERR (Framing Error) (RD)	Set if the first stop bit of the received character was not detected (also see RX.CHAR).
14	OVERRUN.ERR (Overrun Error) (RD)	Set if one or more previous characters of the channel indicated by bits <11:8> were lost because of a full FIFO or failure to service the UARTs (also see RX.CHAR). NOTE **The 'all 1s' code for bits <14:12> is reserved. This code indicates that modem status or diagnostic information is held in RBUF<7:0>.**
15	DATA.VALID (Data Valid) (RD)	Set if the FIFO is not empty. Cleared by MASTER.RESET or by the FIFO becoming empty. After self-test, diagnostic information is loaded into the FIFO. Therefore this bit is always set after a successful master reset sequence.

3.2.2.3 Transmit Character Register (TXCHAR) – Single-character programmed transfers are made via the transmit character register. Bit function is as follows:



Bit	Name	Description
<7:0>	TX.CHAR (Transmit Character) (WR)	Character to be transmitted. The LSB is bit 0. For 7-, 6-, or 5-bit characters, unused bits must be '0'.
15	TX.DATA. VALID (Transmit Data Valid) (WR)	When set, instructs the DHV11 to transmit the character held in bits <7:0>. The bit is sensed by the DHV11 which then transfers the character, clears the bit, and sets TX.ACTION. TX.DATA.VALID and the character can be written together, or by separate MOVB instructions.

3.2.2.4 Line Parameter Register (LPR) – This register is used to configure its associated channel. Bit function is as follows:



Bit	Name	Description
<2:1>	DIAG (Diagnostic Code) (R/W)	Diagnostic control codes. Used by the host as follows: 00 = Normal operation 01 = Causes the Background Monitor Program (BMP) to report the DHV11 status via the FIFO. BMP reports are covered in Section 3.3.10.
<4:3>	CHAR.LGTH (Character Length) (R/W)	Defines the length of characters. Does not include start, stop, and parity bits. 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits Set to 11 by MASTER.RESET.
5	PARITY.ENAB (Parity Enable) (R/W)	Parity enable. Causes a parity bit to be generated on transmit, and checked and stripped on receive. 1 = Parity enabled 0 = Parity disabled Cleared by MASTER.RESET.
6	EVEN.PARITY (Even Parity) (R/W)	If LPR<5> is set, this bit defines the type of parity. 1 = Even parity 0 = Odd parity Cleared by MASTER.RESET.
7	STOP.CODE (Stop Code) (R/W)	Defines the length of the transmitted stop bit. 0 = 1 stop bit for 5-, 6-, 7-, or 8-bit characters 1 = 2 stop bits for 6-, 7-, or 8-bit characters, or 1.5 stop bits for 5-bit characters Cleared by MASTER.RESET.
<11:8>	RX.SPEED (Received Data Rate) (R/W)	Set to 1101 by MASTER.RESET (9600 bits/s). Defines the receive data rate (Table 3-2).
<15:12>	TX.SPEED (Transmitted Data Rate) (R/W)	Set to 1101 by MASTER.RESET. Defines the transmit data rate (Table 3-2).

Table 3-2 Data Rates

Code	Data Rate (Bits/s)	Maximum Error (%)	Groups
0000	50	0.01	A
0001	75	0.01	B
0010	110	0.08	A and B
0011	134.5	0.07	A and B
0100	150	0.01	B
0101	300	0.01	A and B
0110	600	0.01	A and B
0111	1200	0.01	A and B
1000	1800	0.01	B
1001	2000	0.19	B
1010	2400	0.01	A and B
1011	4800	0.01	A and B
1100	7200	0.01	A
1101	9600	0.01	A and B
1110	19200	0.01	B
1111	38400	0.01	A

NOTE

The 8-channel interface uses four dual-channel ICs. Channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7 are paired. It is the responsibility of the user to select transmit and receive data rates of the same group (A or B) for any pair of channels.

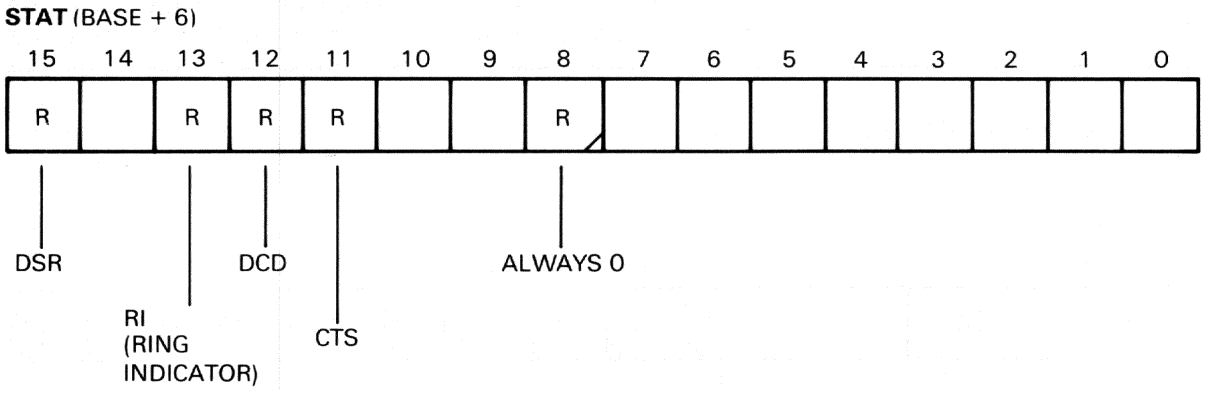
If the transmitter and receiver of a channel are configured in different groups, the group of the receiver is selected.

If a 'pair' of channels are configured in different groups, the group of the most recently configured channel is selected. This changes the data rate of a channel when its paired channel is reconfigured to the other group.

The effect can be predicted as follows:

Original Speed (Bits/s)	Changes to (Bits/s)
50	75
75	50
150	200
1800	7200
2000	1050
7200	1800
19200	38400
38400	19200

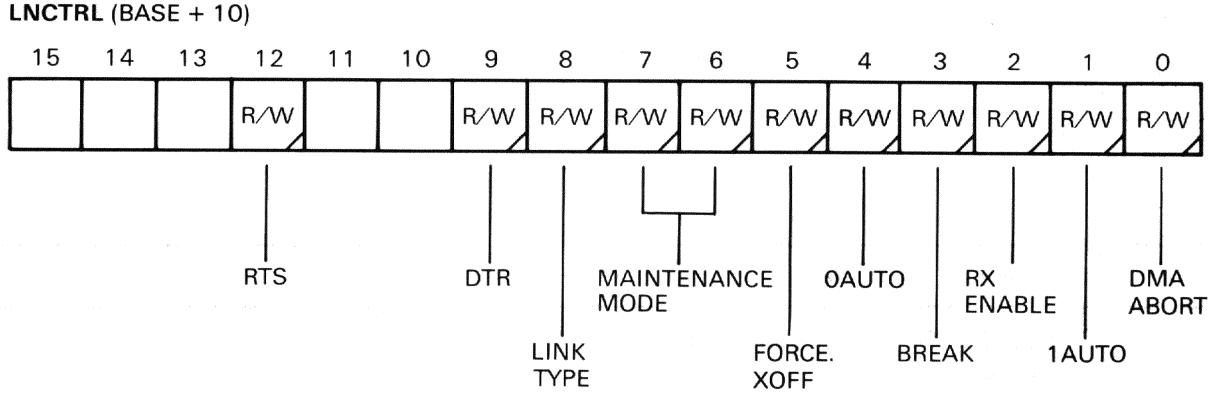
3.2.2.5 Line Status Register (STAT) – The high byte of this register holds modem status information. The low byte is undefined.



Bit	Name	Description
8	STAT<8> (Status Register, bit 8) (RD)	Always 0.
11	CTS (Clear to Send) (RD)	Gives the present status of the Clear To Send (CTS) signal from the modem. 1 = ON 0 = OFF
12	DCD (Data Carrier Detected) (RD)	Gives the present status of the Data Carrier Detected (DCD) signal from the modem. 1 = ON 0 = OFF

Bit	Name	Description
13	RI (Ring Indicator) (RD)	Gives the present status of the Ring Indicator (RI) signal from the modem. 1 = ON 0 = OFF
15	DSR (Data Set Ready) (RD)	Gives the present status of the Data Set Ready (DSR) signal from the modem. 1 = ON 0 = OFF NOTE **In order to report a change of modem status, the DHV11 writes the high byte of STAT into the low byte of RBUF. RBUF<14:12> = 111 to tell the host that RBUF<7:0> do not hold a received character (see modem control, Section 3.3.8).**

3.2.2.6 Line Control Register (LNCTRL) – The main function of this register is to control the line interface.

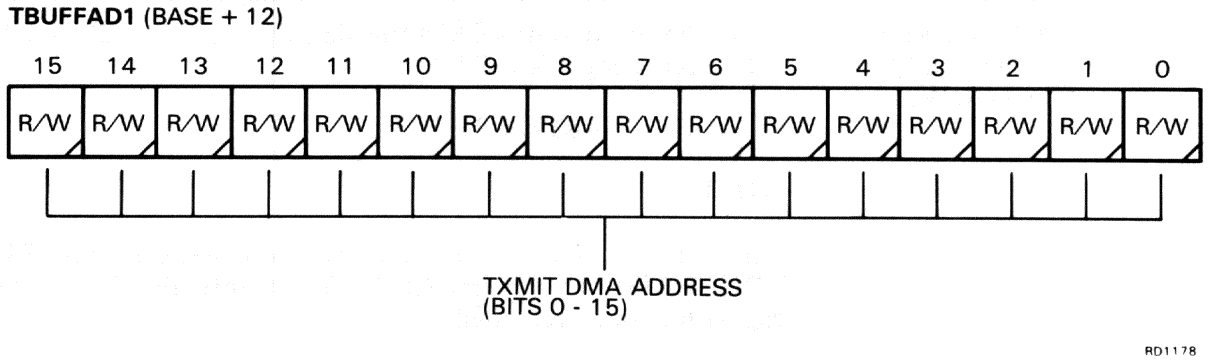


Bit	Name	Description
0	TX.DMA.ABORT (Transmit DMA Abort) (R/W)	Set by the driver program to halt the transfer of a DMA buffer. The transfer can be continued by clearing TX.DMA.ABORT and then setting TX.DMA.START. No characters will be lost. The program must make sure that TX.DMA.ABORT is clear before setting TX.DMA.START. Otherwise the transfer will be aborted before any characters are transmitted. See Section 3.3.3.1, DMA Transfers, for the use of TX.DMA.ABORT. Cleared by MASTER.RESET.

Bit	Name	Description
1	IAUTO (Incoming Auto Flow) (R/W)	This is the auto-flow control bit for incoming characters. If it is set, the DHV11 will control incoming characters by transmitting X-ON and X-OFF codes. If the FIFO becomes congested, the DHV11 will send an X-OFF code to channels with this bit set. An X-ON will be sent when the congestion is reduced. See Auto X-ON and X-OFF, Section 3.3.6. **NOTE** **An X-ON code $= 21_8 =$ DC1 = CTRL/Q.** **An X-OFF code $= 23_8 =$ DC3 = CTRL/S.** **No other codes are specified for the interface.**
2	RX.ENA (Receiver Enable) (R/W)	If set, this receiver channel is enabled. If reset when this DUART channel is assembling a character, that character is lost. Cleared by MASTER.RESET.
3	BREAK (Break Control) (R/W)	If set, this bit forces the transmitter of this channel to the spacing state. Transmission is restarted when the bit is cleared. **NOTE** **There is a short delay between writing the bit and the channel changing state. The delay is dependent on throughput. Because of the normal length of a BREAK signal, this should not cause problems.**
4	OAUTO (Outgoing Auto Flow) (R/W)	This bit is the auto-flow control bit for outgoing characters. When set, if RX.ENA is also set, the DHV11 will automatically respond to X-ON and X-OFF codes received from a channel. The DHV11 uses the TX.ENA bit in TBUFFAD2 to stop and start the flow. See Auto X-ON and X-OFF, Section 3.3.6.
5	FORCE.XOFF (Force X-OFF) (R/W)	This bit can be set by the program to indicate that this channel is congested at the host system (for example, if the typeahead buffer is full). When it sees this bit set, the DHV11 will send an X-OFF code. Until the bit is reset, X-OFFs will be sent after every alternate character received on that channel. When the bit is reset, an X-ON will be sent unless IAUTO is set and the FIFO is critical. See Auto X-ON and X-OFF, Section 3.3.6.

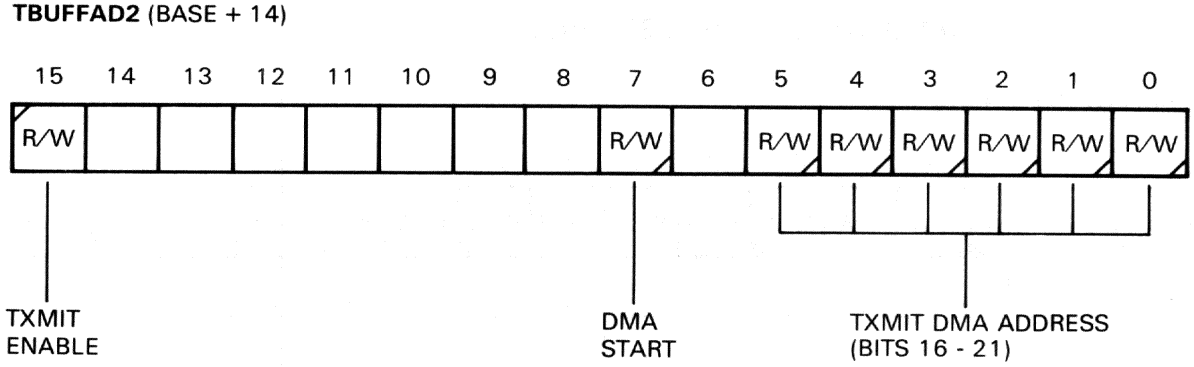
Bit	Name	Description
<7:6>	MAINT (Maintenance Mode) (R/W)	These bits can be written by the driver or test programs, in order to test the channel. The coding is as follows: 00 = Normal operation 01 = Automatic echo mode – Received data is retransmitted (regardless of the state of TX.ENA) at the data rate selected for the receiver. The received characters are processed normally and placed in the received character FIFO. In this mode, the DHV11 will not transmit any characters (this includes internally generated flow-control characters). The RX.ENA bit must be set when operating in this mode. 10 = Local loopback – The DUART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held marking. In this mode, flow-control characters will be looped back instead of being transmitted. The data rate selected for the transmitter is used for both transmission and reception. The TX.ENA bit still controls transmission in this mode. 11 = Remote loopback – In this mode, received data is retransmitted at a clock rate equal to the received clock rate. The data is not placed in the receiver FIFO. The state of TX.ENA is ignored.
8	LINK.TYPE (Link Type) (R/W)	This bit must be set if the channel is to be connected to a modem. When the bit is set, any change in modem status will be reported via the FIFO as well as the STAT register. If this bit is reset, this channel becomes a 'data leads only' channel. Modem status information is loaded in the high byte of STAT but is not placed in the FIFO.
9	DTR (Data Terminal Ready) (R/W)	This bit controls the Data Terminal Ready (DTR) signal. 1 = ON 0 = OFF
12	RTS (Request To Send) (R/W)	This bit controls the Request To Send (RTS) signal. 1 = ON 0 = OFF

3.2.2.7 Transmit Buffer Address Register Number 1 (TBUFFAD1) –



Bit	Name	Description
<15:0>	TBUFFAD<15:0> (Transmit Buffer Address [Low]) (R/W)	Bits <15:0> of the DMA address (see Section 3.2.2.8).

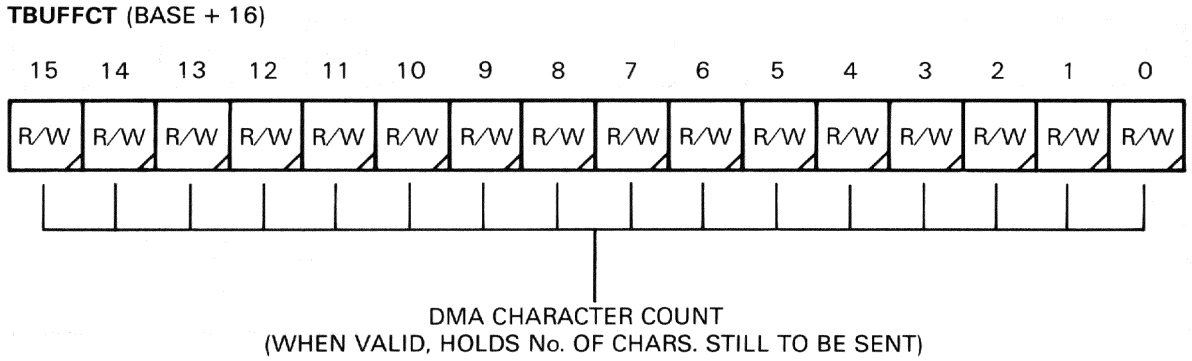
3.2.2.8 Transmit Buffer Address Register Number 2 (TBUFFAD2) –



Bit	Name	Description
<5:0>	TBUFFAD<21:16> (Transmit Buffer Address [High]) (R/W)	Bits <21:16> of the DMA address. Before a DMA transfer, TBUFFAD1 and the low byte of TBUFFAD2 are loaded with the start address of the DMA buffer. This address is not valid during a DMA transfer. When TX.ACTION is returned, the address will be valid.

Bit	Name	Description
7	TX.DMA.START (Transmit DMA Start) (R/W)	Set by the host to start a DMA transfer. The DHV11 will reset the bit before returning TX.ACTION. Cleared by MASTER.RESET. NOTE **After setting this bit, the host must not write to TBUFFCT, TBUFFAD1, or TBUFFAD2 <7:0> until the TX.ACTION report has been returned.**
15	TX.ENA (Transmitter Enable) (R/W)	When set, the DHV11 will transmit all characters. When cleared, the DHV11 will only transmit **internally** generated flow-control characters. Set by MASTER.RESET. In the OAUTO mode, this bit is used by the DHV11 to control outgoing characters. See Auto X-ON and X-OFF, Section 3.3.6.

3.2.2.9 Transmit DMA Buffer Counter (TBUFFCT) –



Bit	Name	Description
<15:0>	TX.CHAR.CT (Transmit Character Count) (R/W)	Loaded with the number of characters to be transferred by DMA. The number of characters is specified as a 16-bit unsigned integer. After a DMA transfer has been aborted, this location will hold the number of characters still to be transferred. See also the previous NOTE.

3.3 PROGRAMMING FEATURES

3.3.1 Initialization

The DHV11 is initialized by its on-board firmware.

Initialization takes place after a bus reset sequence, or when the host sets CSR<5> (MASTER.RESET).

Before starting initialization, the on-board diagnostics run a self-test program. The results of this test are reported by eight diagnostic bytes in the FIFO.

NOTE

This self-test diagnostic can be skipped on command from the program. This is covered in Section 3.3.10.3.

The DHV11 state, after a successful self-test, is as follows:

1. Eight diagnostic codes are placed in the FIFO
2. The diagnostic fail bit (CSR<13>) is reset
3. All channels set for:

    a. Send and receive 9600 bits/s
    b. Eight data bits
    c. One stop bit
    d. No parity
    e. Parity odd
    f. Auto-flow off
    g. RX disabled
    h. TX enabled
    i. No break on line
    j. No loopback
    k. No modem control
    l. DTR and RTS off
    m. DMA character counters zero
    n. DMA start addresses zero
    o. TX.DMA.START cleared
    p. TX.DMA.ABORT cleared.

The DHV11 clears the MASTER.RESET bit (CSR<5>) when initialization and self-test are complete.

3.3.2 Configuration

After DHV11 self-initialization, the driver program can configure the DHV11 as needed. This is done via the LPR and LNCTRL registers.

By writing to the associated LPR and LNCTRL the program can select data rate, character length, parity, and stop bit length for each channel. Individual receivers and transmitters can be enabled and auto-flow selected.

For operation with any device which uses modem-type signals, LINK.TYPE of the associated LNCTRL register should be set.

NOTE

If RX.ENA is reset while a receive character is being assembled, that character will be lost

3.3.3 Transmitting

Each channel of the DHV11 can be programmed to transmit blocks of characters by DMA, or single characters only. Such transfers are covered in the following three subsections. For data flow and timing considerations see Chapter 4, Section 4.6.

3.3.3.1 **DMA Transfers** – Before setting up the transfer of a DMA buffer, the program should make sure that TX.DMA.START is not set. TBUFFCT, TBUFFAD1, and TBUFFAD2 should not be written unless TX.DMA.START is clear.

Transmission will start when the program sets TX.DMA.START.

The size of the DMA buffer, and its start address, can be written to TBUFFCT, TBUFFAD1, and TBUFFAD2 in any order. However, TBUFFAD2 contains TX.ENA and TX.DMA.START, so it is probably simpler to write TBUFFAD2 last. By using byte operations on this register, TX.ENA and TX.DMA.START can be separated.

The DHV11 will perform the transfer and set TX.ACTION when it is complete. If TXIE is set, the program will be interrupted at the transmit vector. Otherwise, TX.ACTION must be polled.

To abort a DMA transfer, the program must set TX.DMA.ABORT. The DHV11 will stop transmission, and update TBUFFCT, TBUFFAD1, and TBUFFAD2<7:0> to reflect the number of characters which have been transmitted. TX.DMA.START will be cleared. If the interrupt is enabled, TX.ACTION will interrupt the program at the transmit vector. If the program clears TX.DMA.ABORT and sets TX.DMA.START, the transfer can be continued without loss of characters.

If a DMA transfer fails because of a memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location. TBUFFCT will be cleared.

3.3.3.2 **Single Character Programmed Transfers** – Single characters are transferred via a channel's TX.CHAR register. The character and the DATA.VALID bit must be written as defined in Section 3.2.2.3. Note that the character and the DATA.VALID bit can be written by separate MOVB instructions.

The DHV11 returns TX.ACTION when it reads the character from TX.CHAR. As with DMA transfers, this bit can be sensed via interrupt or by polling the CSR.

In single-character mode, TX.ACTION is returned when the DHV11 accepts the character, **not** when it has been transmitted. Each channel has a 3-character buffer. Therefore, if modem status bits or line parameters are changed immediately after the last TX.ACTION of a message, the end of the message could be lost. The program can prevent loss by adding three null characters to the end of each single-character programmed transfer message.

3.3.3.3 **Methods of Control** – Examples of control by polling or by the use of interrupts are given in Section 3.4, Programming Examples.

3.3.4 Receiving

Received characters, tagged with the channel number and DATA.VALID, are placed in the FIFO buffer (RBUF). If a character is put in an empty RBUF, the DHV11 sets RX.DATA.AVAIL. It stays set while there is valid data in there. If RXIE is set, the program will be interrupted at the receive vector. The program's interrupt routine should read RBUF until DATA.VALID is reset.

NOTE

The interrupt is dynamic. It is raised as RX.DATA.AVAIL is set after RXIE, or as RXIE is set after RX.DATA.AVAIL. If the interrupt routine does not empty the FIFO, RXIE must be toggled to raise another interrupt.

If RXIE is not set the program must poll RBUF often enough to prevent data loss.

3.3.5 Interrupt Control

During an interrupt request sequence, assuming that interrupts are enabled, the DHV11 can provide two vectors:

1. The 'base' vector set on the interrupt vector switches
2. 'Base' vector + 4.

The base vector is supplied each time data is put into an empty FIFO.

The 'base + 4' vector is supplied when:

1. A DMA block has been transferred.
2. A DMA transfer has been aborted, or terminated because of a memory error.
3. A single-character programmed transfer is complete.

At the two vectors, the host must provide the addresses of suitable routines to deal with the above conditions.

3.3.6 Auto X-ON and X-OFF

X-ON and X-OFF codes are commonly used to control data flow on communications channels. To use this facility, interfaces must have suitable decoding hardware or software.

A channel which receives an X-OFF stops sending characters until it receives an X-ON. A channel which is becoming overrun by received data sends an X-OFF. It sends an X-ON when the congestion is relieved.

If the DHV11 is programmed for automatic flow control (auto-flow), it can automatically control the flow of characters. Three bits control this function:

1. IAUTO – LNCTRL<1>
2. FORCE.XOFF – LNCTRL<5>
3. OAUTO – LNCTRL<4>

IAUTO and FORCE.XOFF both control incoming characters. IAUTO is an enable bit which allows the state of the FIFO counters to control the generation of XOFF and XON codes. The FORCE.XOFF bit is a direct command from the program.

1. The DHV11 hardware recognizes when the FIFO is three-quarters full and half full. The firmware uses these states for auto-flow control.

   If the program sets a channel's IAUTO bit, the DHV11 will send that channel an X-OFF if it receives a character after the FIFO becomes three-quarters full. If the channel does not respond to X-OFF, the DHV11 will send an X-OFF in response to every alternate character received. An X-ON will be sent when the FIFO becomes less than half full, unless FORCE.XOFF for that channel is set. X-ONs are only sent to channels to which an X-OFF has been sent.

   By inserting X-ON and X-OFF characters into the data stream, the program can perform flow control directly. However, if the DHV11 is in the IAUTO mode, the results will be unpredictable.

   In IAUTO mode, if RX.ENA is set, X-ONs and X-OFFs will be transmitted even if TX.ENA is cleared.

2. When FORCE.XOFF is set, the DHV11 sends an X-OFF and then acts as if IAUTO is set and the FIFO is critical (was three-quarters full, and is not yet less than half full). When FORCE.XOFF is reset, an X-ON will be sent unless the FIFO is critical and IAUTO is set.

3. If the program sets OAUTO, the DHV11 will automatically respond to X-ON and X-OFF characters from the channel. It does this by clearing and setting the TX.ENA bit.

   The program may also control the TX.ENA bit, so in this case it is important to keep track of received X-ON AND X-OFF characters.

   Received X-ON and X-OFF characters will always be reported via the FIFO. It is possible during read/modify/write operations by the program, for the DHV11 to change the TX.ENA bit between the read and the write action. For this reason, if DMA transfers are started while OAUTO is set, it is advisable to write to the low byte of TBUFFAD2 only.

NOTES

1. **The DHV11 may change the state of TX.ENA for up to 20 microseconds after OAUTO is cleared by the program.**

2. **When checking for flow-control characters, the DHV11 only checks characters which do not contain transmission errors. The parity bit is stripped and the remaining bits are checked for X-ON (21_8) and X-OFF (23_8) codes.**

3.3.7 Error Indication

The program is informed of transmission and reception errors by means of four bits:

1. TX.DMA.ERR – CSR<12>. See Section 3.2.2.1
2. PARITY.ERR – RBUF<12>. See Section 3.2.2.2
3. FRAME.ERR – RBUF <13>. See Section 3.2.2.2
4. OVERRUN.ERR – RBUF <14>. See Section 3.2.2.2.

RBUF<14:12> are also used to identify a diagnostic or modem status code.

3.3.8 Modem Control

Each channel of the module provides modem control bits for RTS and DTR. Also on each channel are modem status inputs CTS, DSR RI and DCD. These bits can be used for modem control or as general purpose outputs and inputs (see STAT register).

CTS, DSR, and DCD are sampled by PROC2 every 10 ms. Therefore, for a change to be detected, these bits must stay steady for at least 10 ms after a change. RI is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. There are no hardware controls between the modem control logic and the receiver and transmitter logic. Any coordination should be done under program control. Modem status change reports are placed in the received character FIFO at the correct position relative to the received characters.

By setting LINK.TYPE (LNCTRL<8>), a channel can be selected for modem operation. Any change of the modem status inputs will be reported to the program via the received character FIFO. Modem control bits must be driven by the program's communication routines. Control bits are written to LNCTRL.

Appendix B gives more detail of modem control.

By clearing LINK.TYPE the channel is selected as a 'data lines only' channel. Modem control and status bits can still be managed by the program but status bits must be polled at the line status register. Changes of modem status will not be reported to the program.

NOTE

When transmitting by the single-character programmed transfer method, up to three characters can be buffered in DHV11 hardware. If modem control bits are to be changed at the end of a transmission, three null characters should be added. When TX.ACTION is set after the third null character, the last true character has left the UART.

Status change reporting is done via the FIFO as follows:

- When OVERRUN.ERR, FRAME,ERR, and PARITY.ERR are all set, the eight low-order bits contain either status change or diagnostic information. In this case:
  - If RBUF<0> = 0, RBUF<7:1> holds STAT<15:9> (see Section 3.2.2.5).
  - If RBUF<0> = 1, RBUF<7:1> holds diagnostic information (see Section 3.3.10).

3.3.9 Maintenance Programming

As well as using on-board and external diagnostic programs, the host can also test each channel directly. Bits 7 and 6 of LNCTRL allow each channel to be configured in normal, automatic echo, local loopback, and remote loopback modes (see LNCTRL Section 3.2.2.6).

The host must provide suitable software to test these configurations.

3.3.10 Diagnostic Codes

3.3.10.1 Self-Test Diagnostic Codes – After bus reset or master reset, the DHV11 executes a self-test and initialization sequence. At the end of the sequence, eight diagnostic codes are put in the FIFO. RX.DATA.AVAIL is set and MASTER.RESET is cleared.

After an error-free test, DIAG.FAIL will be reset. The 'diagnostic passed' LED will be on. If an error is detected, DIAG.FAIL will be set and the LED will be off.

An example program which reads and checks the diagnostic codes from RBUF, is included in Section 3.4.

3.3.10.2 Interpretation of Self-Test Codes – The high byte of diagnostic codes in RBUF can be interpreted as in Section 3.2.2.2, except that bits <11:8> are not the line number. They indicate the sequence of the diagnostic byte. That is to say, 0 = first byte, 1 = second byte, and so on.

Figure 3-2 shows how the diagnostic code in the low byte of RBUF, should be interpreted. Table 3-3 gives the meaning of each implemented diagnostic byte.

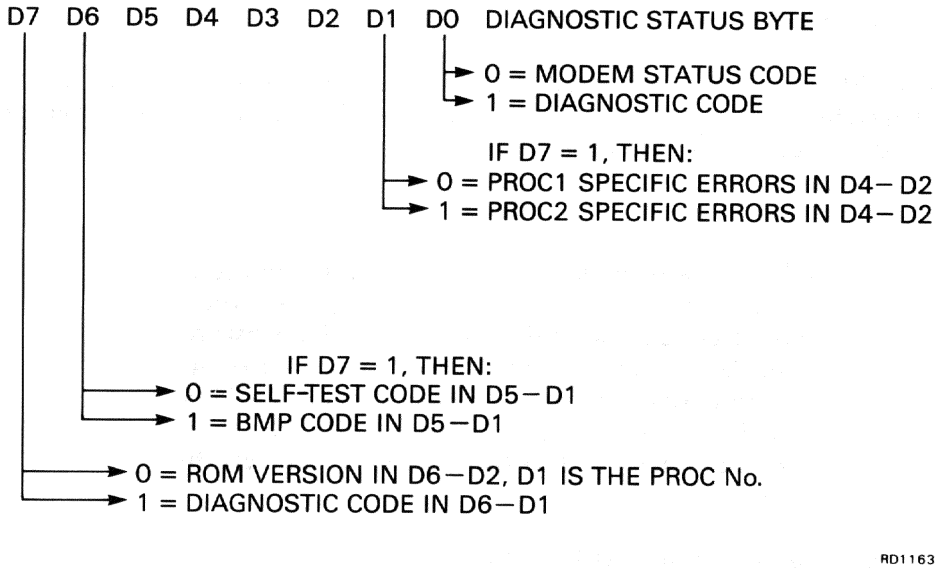


Figure 3-2 Diagnostic/Status Byte

Table 3-3 DHV11 Self-Test Error Codes

Code (Octal)	Test
201	Self-test null code (used as a filler)
203	Self-test skipped
211	Basic data path error from PROC2
213	Undefined UART error
217	Received character FIFO, logic error
225	PROC1 to common RAM error
227	PROC2 to common RAM error
231	PROC1 internal RAM error
233	PROC2 internal RAM error
235	PROC1 ROM error
237	PROC2 ROM error

If D7 = 0 and D0 = 1, ROM version number is in D6 – D2.

D1 = PROC number (0 = PROC1)

NOTE

Codes not shown in this table indicate undefined errors.

After self-test, the eight codes in the FIFO will consist of six diagnostic codes and two ROM version codes. If there are less than six errors to report, null codes (201_8) fill the unused places.

After an error-free test, six null codes and two ROM version codes will be returned.

If self-test is skipped (see next section), six 203_8 codes and two ROM version codes will be returned.

3.3.10.3 **Skipping Self-Test** – Self-test takes up to 2.5 seconds to complete. Depending on system software, this may cause a 2.5-second hangup. The Skip Self-Test facility allows the program to bypass the self-test diagnostic.

Skipping self-test is done as follows:

1. The program resets the DHV11
2. The diagnostic firmware writes 125252_8 throughout the common RAM within eight milliseconds (ms) of reset
3. The program waits 10 ms (+ or – 1 ms) after issuing reset. It then writes 052525_8 throughout the control registers (not the CSR), within the next 4 ms

4. The diagnostic firmware waits until 16 ms after reset. It then checks for a 052525_8 code in common RAM.

   If it finds the code, self-test is skipped. The DIAG.FAIL bit is cleared and control is passed to the communications firmware which starts initialization.

   If the code is not found, self-test starts.

NOTE

The program must not write to the CSR or the control registers during the period starting 15 ms after reset and ending when the MASTER.RESET bit is cleared. This could cause a diagnostic fail condition.

3.3.10.4 **Background Monitor Program(BMP)** – When not busy with other tasks, the DHV11's microcomputers perform background tests on the option. This is done by checking the timer-generated interrupts used by the firmware (one interrupt in PROC1 and two in PROC2). One of two codes is returned to the FIFO:

305_8 – DHV11 running
307_8 – DHV11 defective.

A single diagnostic word is returned via the FIFO. The low byte contains the diagnostic code. In the high byte, OVERRUN.ERR, FRAME.ERR, and PARITY.ERR are all set to indicate that bits<7:0> do not hold a normal character. The line number (RBUF<11:8>) = 0.

If PROC2 stops running, PROC1 will set DIAG.FAIL and will turn off the LED. The LED will stay off, even if the fault clears. If PROC1 stops running, PROC2 will load a 307 code into the FIFO.

Normally, the BMP will only report when it finds an error. However, if the program suspects that the DHV11 is not working it can get a BMP report at any time. This is done by setting DIAG (LPR<2:1>) of any channel to 01. The line number returned is that of the LPR used to request the report.

On completion of the check, the BMP will clear the 01 code in DIAG. The host should not write to the LPR of that channel until DIAG has been cleared.

3.4 PROGRAMMING EXAMPLES

This section contains programming examples. They are not given as the only method of driving the option. These programs are not guaranteed or supported.

3.4.1 Resetting the DHV11

In the following example:

- DIAG is a routine to check the diagnostic codes. It returns with CARRY set if it detects an error code (see Section 3.3.10).

- The loop at 1$ can take up to 2.5 seconds, so the programmer could poll via a timer or poll at interrupt level zero.

```
;
; A ROUTINE TO RESET THE DHV11 AND CHECK THAT IT IS FUNCTIONING
; CORRECTLY.
;
;
; NOTE: A SOPHISTICATED PROGRAM WOULD TIME OUT AFTER 3 SECONDS
;       IF THE RESET DID NOT COMPLETE.
;

DHVRES::
        MOV     #40,@#DHVCSR            ; SET MASTER.RESET AND
                                        ; CLEAR INTERRUPT ENABLES.
1$:     BIT     #40,@#DHVCSR            ; WAIT FOR MASTER.RESET TO
        BNE     1$                      ; CLEAR.
        BIT     #20000,@#DHVCSR         ; CHECK THE DIAGNOSTICS FAIL
        BNE     DIAGER                  ; BIT.
                                        ; NOTE: TEST INSTRUCTION IS
                                        ;         OK BECAUSE THERE ARE
                                        ;         NO TX.ACTS PENDING.
        MOV     #8.,R5                  ; PROCESS THE EIGHT SELF
                                        ; TEST CODES.
2$:     MOV     @#RBUFF,R0              ; GET NEXT DIAGNOSTIC CODE.
        JSR     PC,DIAG                 ; PROCESS IT.
        BCS     DIAGER                  ; CARRY SET - MUST HAVE BEEN
                                        ; AN ERROR.
        SOB     R5,2$                   ; GO BACK FOR NEXT CODE.

        RTS     PC                      ; RETURN - CARD IS RESET.

;
; DHV11 HAS FAILED TO RESET PROPERLY, SO HALT AND WAIT FOR
; THE FIELD SERVICE ENGINEER.
;

DIAGER: HALT
        BR      DIAGER
```

3.4.2 Configuration

This routine sets the characteristics of channel 1 as follows:

1. Transmit and receive at 300 bits/s
2. Seven data bits with even parity and one stop bit
3. Transmitters and receivers enabled
4. No modem control
5. No automatic flow control.

```
;
; SET CHARACTERISTICS OF CHANNEL 1 TO THE FOLLOWING STATE:-
;
;
;       1)      TRANSMIT AND RECEIVE AT 300 B.P.S.
;
;       2)      7 DATA BITS WITH EVEN PARITY AND ONE STOP BIT.
;
;       3)      TRANSMITTERS AND RECEIVERS ENABLED.
;
;       4)      NO MODEM CONTROL.
;
;       5)      NO AUTOMATIC FLOW CONTROL.
;
```

```
SETUP::
        MOV     #1,@#DHVCSR             ; SELECT THE LINE WE'RE
                                        ; INTERESTED IN.
        MOV     #Ø52560,@#LPR           ; DATA RATE, STOP BITS,
                                        ; PARITY AND LENGTH
        MOV     #4,@#LNCTRL             ; ENABLE THE RECEIVER.
        MOVB    #2ØØ,@#TBFAD2+1         ; ENABLE THE TRANSMITTER.

        RTS     PC                      ; RETURN - CHANNEL 1 DONE.
```

3.4.3 Transmitting

3.4.3.1 Single Character Programmed Transfer – This is a program to send a message on channel 1. The message (MESS) is an ASCII string with a null character as terminator.

Polling is used but a TX.ACTION interrupt could also be used.

This program would function on a DHV11 with only this channel active. Otherwise it would lose TX.ACTION reports of other channels. However, a program to control all channels would be too big to use as an example.

```
;
; A ROUTINE TO WRITE A MESSAGE TO CHANNEL 1 USING SINGLE CHARACTER
; MODE.
;

SINGOT::
        MOV     #1,@#DHVCSR             ; POINT TO CHANNEL WE WISH
                                        ; TO TALK TO.
        MOV     #MESS,RØ                ; POINT TO MESSAGE.
1$:
        MOVB    (RØ)+,@#TXCHAR          ; MOVE CHARACTER TO TRANSMIT BUFFER
        BEQ     3$                      ; GO RETURN IF ALL CHARACTERS GONE.
        MOVB    #2ØØ,@#TXCHAR+1         ; SET DATA VALID BIT TO START.
2$:
        MOV     @#DHVCSR,R1             ; WAIT FOR TX.ACT
        BPL     2$

        BIC     #17Ø377,R1              ; ISOLATE CHANNEL NUMBER.
        CMP     #ØØØ4ØØ,R1
        BNE     2$                      ; IGNORE THE TX.ACT IF ITS
                                        ; NOT OURS (SHOULDN'T HAPPEN)
        BR      1$                      ; GO BACK FOR NEXT CHARACTER.

3$:
        RTS     PC                      ; MESSAGE SENT.

MESS:   .ASCIZ  /A SINGLE CHARACTER MESSAGE FOR CHANNEL 1/
        .EVEN
```

3.4.3.2 DMA Transfer –

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF THE DHV11 AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE, AND INTERRUPTS ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;

DMAINT::
        MOV     #TXINT,@#TXVECT         ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#TXPSW            ; INTERRUPT PRIORITY FOUR.

        MOV     #8.,R0                  ; EIGHT LINES TO START.
        CLR     R1                      ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHVCSR             ; SELECT THE REGISTER BANK.
        MOV     #DMASIZ,@#TBFCNT        ; SET LENGTH OF MESSAGE.
        MOV     #DMAMES,@#TBFAD1        ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2        ; START DMA WITH TRANSMITTER
                                        ; ENABLED (ASSUME UPPER ADDRESS
                                        ; BITS ARE ZERO).
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; REPEAT FOR ALL LINES.

        CLR     R5                      ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHVCSR+1         ; ENABLE TRANSMITTER INTERRUPTS.
2$:
        CMP     #8.,R5                  ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                            ; ALL DONE, SO STOP.
        BR      3$

;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

TXINT::
        MOV     @#DHVCSR,R0             ; GET LINE NUMBER OF FINISHED LINE.
        BIT     #10000,R0               ; CHECK FOR DMA FAILURE.
        BNE     4$                      ; GO HALT - MEMORY PROBLEM.

        INC     R5                      ; FLAG THAT ANOTHER LINE HAS FINISHED.
        RTI
4$:
        HALT                            ; MEMORY PROBLEM
        BR      4$

DMAMES: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
DMASIZ  =       .-DMAMES
        .EVEN
```

3.4.3.3 Aborting a DMA Transfer –

```
;
; THIS ROUTINE IS CALLED TO ABORT A DMA TRANSFER IN PROGRESS ON A
; SPECIFIED LINE.  THIS ROUTINE MAKES THE (RATHER RASH) ASSUMPTION
; THAT THERE ARE NO OTHER TRANSFERS IN PROGRESS.
;
; ON ENTRY, R0 CONTAINS THE NUMBER OF THE LINE TO BE ABORTED.
;

DMABRT::
        MOV     R0,@#DHVCSR             ; POINT TO THE CHANNEL TO BE ABORTED.
        BIS     #1,@#LNCTRL             ; SET THE DMA ABORT BIT.
1$:
        MOV     @#DHVCSR,R1             ; WAIT FOR THE TX.ACT
        BPL     1$
        SWAB    R1                      ; CHECK ITS OUR LINE.
        BIC     #177760,R1
        CMP     R0,R1
        BNE     1$                      ; IGNORE IT IF ITS NOT (OUR
                                        ; ASSUMPTION WAS WRONG!)

        BIC     #1,@#LNCTRL             ; CLEAR DOWN THE ABORT FLAG
                                        ; FOR NEXT TIME.

        RTS     PC                      ; BUFFER COMPLETELY ABORTED,
                                        ; THE DMA REGISTERS REFLECT
                                        ; WHERE THE DHV11 GOT TO.
```

3.4.4 Receiving

```
;
; THIS ROUTINE PROCESSES RECEIVED CHARACTERS UNDER INTERRUPT CONTROL.
; IF AN XOFF IS RECEIVED, THE TRANSMITTER FOR THAT CHANNEL IS TURNED
; OFF. IF AN XON IS RECEIVED, THE TRANSMITTER IS TURNED BACK ON.  ALL
; OTHER CHARACTERS ARE IGNORED.
;
; THIS IS JUST AN EXAMPLE, A BETTER WAY TO PERFORM FLOW CONTROL IS TO
; USE THE AUTOMATIC CAPABILITIES OF THE DHV11.
;

RXAUTO::
        MOV     #RXINT,@#RXVECT         ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#RXPSW            ; PRIORITY LEVEL FOUR.

        MOV     #8.,R0                  ; ENABLE ALL THE RECEIVERS,
        CLR     R1                      ; STARTING AT CHANNEL ZERO,
1$:
        MOVB    R1,@#DHVCSR             ; SELECT THE LINE.
        BIS     #4,@#LNCTRL             ; ENABLE THIS RECEIVER.
        INC     R1                      ; SET POINTER TO NEXT CHANNEL.
        SOB     R0,1$

        MOVB    #100,@#DHVCSR           ; ENABLE THE RECEIVER INTERRUPTS.

        RTS     PC                      ; RETURN - INTERRUPTS DO THE RESET.

;
; INTERRUPT ROUTINE TO DO THE MAIN TASK.
;
```

```
RXINT::
        MOV     R0,-(SP)                ; SAVE CALLERS REGISTERS.
RXNXTC:
        MOV     @#RBUFF,R0              ; GET THE CHARACTER.
        BPL     RXIEND                  ; IF NO DATA VALID, WE'VE FINISHED.
        MOV     R0,-(SP)                ; CHECK FOR ERRORS, MODEM AND
        BIC     #107777,(SP)+           ; DIAGNOSTICS CODES.
        BNE     RXNXTC                  ;  - JUST IGNORE THEM.

        BIC     #170200,R0              ; REMOVE UNNECESSARY BITS.
        SWAB    R0                      ; POINT TO THIS CHARACTERS LINE.
        BIS     #100,R0                 ; (ADD THE INTERRUPT ENABLE BIT.)
        MOVB    R0,@#DHVCSR
        SWAB    R0                      ; PUT CHARACTER BACK IN LOWER BYTE.
        CMPB    #21,R0                  ; WAS IT AN "XON"?
        BNE     1$                      ; NO - GO CHECK FOR AN "XOFF"

        BISB    #200,@#TBFAD2+1         ; ENABLE THE TRANSMITTER.
        BR      RXNXTC                  ; GO CHECK FOR MORE CHARACTERS.
1$:
        CMPB    #23,R0                  ; WAS IT AN "XOFF"?
        BNE     RXNXTC                  ; NO - GO CHECK FOR MORE CHARACTERS.

        BICB    #200,@#TBFAD2+1         ; DISABLE THE TRANSMITTER.
        BR      RXNXTC                  ; GO CHECK FOR MORE CHARACTERS.

RXIEND:
        MOV     (SP)+,R0                ; RESTORE THE DESTROYED REGISTER.
        RTI
```

3.4.5 Auto X-ON and X-OFF

```
;
; THIS PROGRAM SENDS A MESSAGE OUT ON EACH LINE OF THE DHV11 AND
; HALTS THE MACHINE WHEN ALL TRANSMISSIONS HAVE COMPLETED.
;
; THE MESSAGES ARE TRANSMITTED USING DMA MODE, AND INTERRUPTS ARE
; USED TO SIGNAL TRANSMISSION COMPLETION.
;
; AUTOMATIC FLOW CONTROL IS ENABLED ON THE OUTGOING DATA.
;

TXAUTO::
        MOV     #ATOINT,@#TXVECT        ; SET UP THE INTERRUPT VECTORS.
        MOV     #200,@#TXPSW            ; INTERRUPT PRIORITY FOUR.

        MOV     #8.,R0                  ; EIGHT LINES TO START.
        CLR     R1                      ; START AT LINE ZERO.
1$:
        MOVB    R1,@#DHVCSR             ; SELECT THE REGISTER BANK.
        BIS     #24,@#LNCTRL            ; ENABLE AUTOMATIC FLOW CONTROL
                                        ; ON THE TRANSMITTED DATA.
        MOV     #AUTOSZ,@#TBFCNT        ; SET LENGTH OF MESSAGE.
        MOV     #AUTOMS,@#TBFAD1        ; SET LOWER 16 ADDRESS BITS.
        MOV     #100200,@#TBFAD2        ; START DMA WITH TRANSMITTER
                                        ; ENABLED (ASSUME UPPER ADDRESS
                                        ; BITS ARE ZERO).
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; REPEAT FOR ALL LINES.

        CLR     R5                      ; R5 IS USED BY INTERRUPT ROUTINE.
        MOVB    #100,@#DHVCSR+1         ; ENABLE TRANSMITTER INTERRUPTS.
```

```
2$:
        CMP     #8.,R5                  ; WAIT FOR ALL LINES TO FINISH.
        BNE     2$
3$:
        HALT                            ; ALL DONE, SO STOP.
        BR      3$

;
; TRANSMITTER INTERRUPT ROUTINE.
;
; R5 IS INCREMENTED AS EACH LINE COMPLETES.
;

ATOINT::
        MOV     @#DHVCSR,R0             ; GET LINE NUMBER OF FINISHED LINE.
        BIT     #10000,R0               ; CHECK FOR DMA FAILURE.
        BNE     4$                      ; GO HALT - MEMORY PROBLEM.

        INC     R5                      ; FLAG THAT ANOTHER LINE HAS FINISHED.
        RTI
4$:
        HALT                            ; MEMORY PROBLEM
        BR      4$

AUTOMS: .ASCII  <15><12><7><7><7>/SYSTEM CLOSING DOWN NOW/
AUTOSZ  =       .-AUTOMS
        .EVEN
```

3.4.6 Checking Diagnostic Codes

```
 ;
 ; THIS ROUTINE CHECKS THE DIAGNOSTICS CODES RETURNED FROM THE DHV11.
 ;
 ; ON ENTRY, R0 CONTAINS THE CHARACTER RECEIVED FROM THE DHV11.
 ;
 ; ON EXIT, THE CARRY BIT WILL BE CLEAR FOR SUCCESS, SET FOR FAILURE.
 ;

 DIAG::
        MOV     R0,-(SP)                ; SAVE THE CODE FOR LATER.

        BIC     #107776,R0              ; CHECK THAT IT'S A DIAG. CODE.
        CMP     #070001,R0
        BNE     DIAGEX                  ; IF NOT, JUST EXIT NORMALLY.

        MOV     (SP),R0                 ; GET THE CODE BACK.

        BITB    #200,R0                 ; CHECK FOR ROM VERSION NUMBER.
        BEQ     DIAGEX
        CMPB    #201,R0                 ; SELF TEST NULL CODE.
        BEQ     DIAGEX
        CMPB    #203,R0                 ; SELF TEST SKIPPED CODE.
        BEQ     DIAGEX
        CMPB    #305,R0                 ; DHV RUNNING CODE.
        BEQ     DIAGEX
                                        ; ALL THE REST ARE ERROR CODES.

        SEC                             ; AN ERROR CODE WAS RECEIVED, SO
        BR      DIAGXX                  ; SET THE CARRY FLAG.
```

```
DIAGEX:
        CLC                             ; EVERYTHING OK, SO CLEAR CARRY.
DIAGXX:
        MOV     (SP)+,RØ                ; RESTORE THE CHARACTER/INFO.
        RTS     PC
```

3.4.7 Modem Control

```
;
; THIS ROUTINE WILL ANSWER A MODEM CALL, PRINT OUT A MESSAGE AND
; HANG UP THE PHONE.
;
; DMA MODE IS USED.  IF  SINGLE CHARACTER MODE WERE USED, THEN
; THE MESSAGE WOULD NEED TO BE PADDED OUT WITH THREE NULLS DUE
; TO INTERNAL BUFFERING OF THE DHV11.
;

MODEM::
        MOV     #8.,R0                  ; SET UP ALL CHANNELS FOR MODEMS.
        CLR     R1
1$:
        MOVB    R1,@#DHVCSR             ; POINT TO CHANNEL TO BE SET UP.
        MOVB    #125,@#LPR+1            ; 300 BPS DATA RATE.
        MOV     #400,@#LNCTRL           ; SET MODEM & DISABLE RECEIVER.
        INC     R1                      ; POINT TO NEXT CHANNEL.
        SOB     R0,1$                   ; SET UP ALL CHANNELS.

        MOV     #MRXINT,@#RXVECT        ; SET UP INTERRUPT VECTORS.
        MOV     #200,@#RXPSW            ; (INTERRUPT LEVEL FOUR)
        MOV     #MTXINT,@#TXVECT
        MOV     #200,@#RXPSW
        MOV     #40100,@#DHVCSR         ; ENABLE THE INTERRUPTS.
2$:
        BR      2$                      ; LET INTERRUPT ROUTINES DO EVERYTHING

;
; TRANSMITTER INTERRUPT ROUTINE.
;

MTXINT:
        MOV     R0,-(SP)                ; SAVE THE REGISTER WE USE.
        MOV     @#DHVCSR,R0             ; GET INTERRUPTING LINE NUMBER.
        SWAB    R0                      ; SELECT THIS CHANNELS REGISTERS.
        BIC     #177760,R0
        BIS     #100,R0                 ; (RETAIN INTERRUPT ENABLE)
        MOVB    R0,@#DHVCSR
        MOV     #400,@#LNCTRL           ; DROP DTR, RTS AND CLEAR ABORT.
        MOV     (SP)+,R0                ; RESTORE THE REGISTER WE USED.
        RTI
```

```
;
; RECEIVER INTERRUPT ROUTINE.
;

MRXINT::
        MOV     R0,-(SP)                ; SAVE THE REGISTER WE USE.
MRXLOP:
        MOV     @#RBUFF,R0              ; GET INTERRUPTING LINE.
        BPL     MRXEND                  ; EXIT IF ALL DONE.
        MOV     R0,-(SP)                ; SAVE FOR LATER USE.
        BIC     #107776,R0              ; TEST FOR MODEM INFO.
        CMP     #070000,R0
        BNE     MRXNXT                  ; SKIP IF NOT.
        MOV     (SP),R0                 ; SELECT REGISTERS FOR THIS LINE.
        SWAB    R0
        BIC     #177760,R0
        BIS     #100,R0                 ; (RETAIN INTERRUPT ENABLE)
        MOVB    R0,@#DHVCSR

        MOV     (SP),R0                 ; CHECK FOR READY FOR TRANSMISSION.
        BIC     #177547,R0
        CMP     #230,R0
        BNE     1$                      ; DSR, DCD & CTS NOT SET, TRY START.
        BIC     #1,@#LNCTRL             ; CLEAR DOWN ABORT BIT (IN CASE WE
                                        ; SET IT WITHOUT A DMA IN PROGRESS).
        MOVB    #23,@#LNCTRL+1          ; ASSERT RTS IN CASE CTS AND DSR
                                        ; WERE ASSERTED AT THE SAME TIME.
        MOV     #NOSYSZ,@#TBFCNT        ; OUTPUT MESSAGE.
        MOV     #NOSYS,@#TBFAD1         ; (TRANSMITTER INTERRUPT ROUTINE
        MOV     #100200,@#TBFAD2        ;  CLEARS DOWN THE CALL.)
        BR      MRXNXT                  ; GO LOOK FOR MORE.
1$:
        BIT     #200,R0                 ; CHECK FOR DSR.
        BEQ     2$                      ; NO - GO CHECK FOR NEW CALL.
        MOVB    #23,@#LNCTRL+1          ; ASSERT RTS.
        BR      MRXNXT                  ; GO LOOK FOR MORE.
2$:
        BIT     #40,(SP)                ; CHECK FOR RING INDICATOR.
        BEQ     3$                      ; NO - GO CLOSEDOWN CALL.
        MOVB    #3,@#LNCTRL+1           ; ASSERT DTR.
        BR      MRXNXT                  ; GO LOOK FOR MORE.
3$:
        BISB    #1,@#LNCTRL             ; ABORT ANY CURRENT DMA TRANSFERS.
        MOVB    #1,@#LNCTRL+1           ; DROP MODEM SIGNALS.
MRXNXT:
        TST     (SP)+                   ; REMOVE SIGNALS FROM THE STACK.
        BR      MRXLOP                  ; GO ROUND AGAIN.
MRXEND:
        MOV     (SP)+,R0                ; RESTORE THE REGISTER WE USED.
        RTI

NOSYS:  .ASCII  <15><12><7><7><7>/SYSTEM UNAVAILABLE, PLEASE TRY LATER/
NOSYSZ  =       .-NOSYS
        .EVEN
```

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 SCOPE

This chapter describes:

- Operation of the main hardware blocks
- Data flow
- Control of address and data
- Operation of the microcomputers
- Use and control of the RAM
- Internal diagnostics.

The chapter starts with a description at block diagram level. This is followed by a section on data flow, and then specific areas are described in more detail. A basic description of the DHV11's ROM-based diagnostics completes the chapter.

It is assumed that the reader has read Chapter 3, Sections 1, 2, and 3 of this document.

Refer to Figure 4-1 throughout this description.

4.2 Q-BUS INTERFACE

The simplified block of the Q-bus interface in Figure 1-5 is expanded in Figure 4-1. The interface is made up of all the components between the external and internal buses.

DC005 bus transceivers control the address and data lines BDAL<17:0> and BAL<21:18>. Bus transceivers also:

1. Recognize device addresses
2. Provide vectors during interrupt sequences.

When (1) the DHV11 is bus slave, access to the DHV11 is allowed when BBS7 is asserted (I/O operation) and BDAL<12:4> 'matches' the address on the module address switches. By this means, the DHV11 recognizes a valid device register address. Transceiver direction is controlled by BDIN and BDOUT, which indirectly generate XMIT.H and REC.H. The 'match' condition generates the signal MATCH.

In an interrupt acknowledge cycle (2), the DC003 interrupt IC responds to BIAKI. The signal VECTOR enables the vector switches onto the BDAL lines via the DC005s. VECT.2.H is the low bit of the vector address. It identifies a receive (0) or transmit (1) interrupt vector. VECTOR also generates BRPLY via DC004 protocol logic.

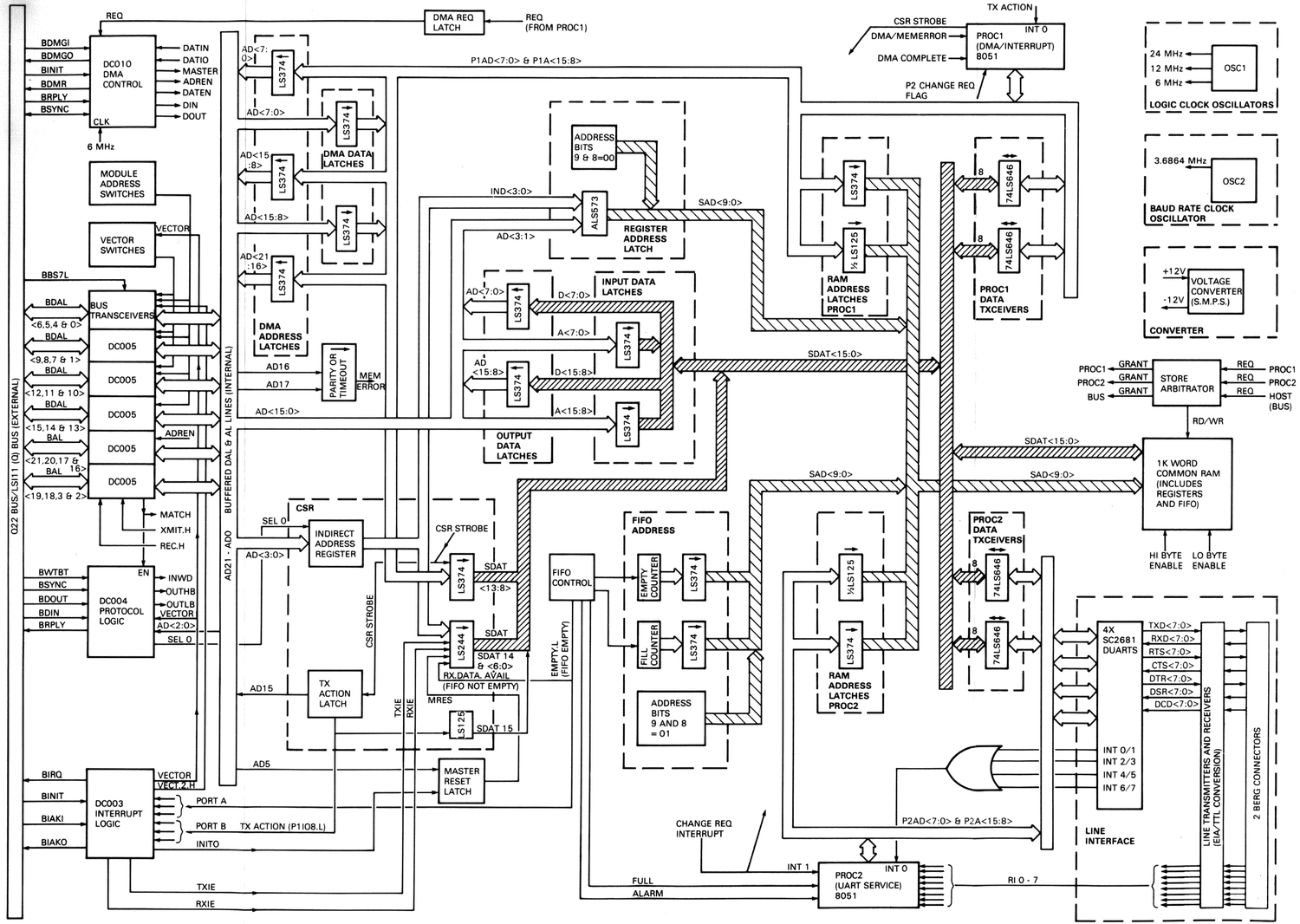


Figure 4-1 DHV11 Block Diagram

When the bus transceivers recognize a valid device register address, the DC004 is enabled. MATCH allows BDIN or BDOUT to generate BRPLY. The external bus signals are decoded by the DC004 which generates the following as necessary:

INWD	–	Word transfer, DHV11 to the bus master
OUTLB	–	Low byte (AD<7:0>) transfer, bus master to DHV11
OUTHB	–	High byte (AD<15:8>) transfer, bus master to DHV11.

Both OUTHB and OUTLB are generated to transfer a word to DHV11.

The DC004 also decodes the low address lines to generate a number of register select (SEL) signals. SEL0 is the signal which selects the CSR.

If a condition which needs interrupt service occurs, the DC003 interrupt logic interrupts the host (BIRQ). When the acknowledge signal (BIAKI) is returned, VECTOR and VECT.2 are generated as previously described. BIAKO provides bus grant continuity.

BINIT is the bus initialize signal. It resets the DHV11 to a known state.

DC010 DMA control is used by the DHV11 to perform a DMA block transfer. A hardware DMA request enables the IC, which then makes a request via BDMR (bus DMA request) for control of the bus. The DC010 provides the appropriate bus-control signals to transfer a word of data to DHV11. After each transfer the bus is released. Another DMA request is needed for the transfer of the next word. DMA data does not pass through the DC010.

Figures 4-2 and 4-3 show the DATI (INWD), DATOB (OUTLB or OUTHB), and DATO (OUTLB and OUTHB) handshake sequences. In each case the DHV11 is bus slave.

Figure 4-4 shows an interrupt request/acknowledge sequence which requests the host processor to read an interrupt vector from the DHV11. This sequence is followed by a DATI operation which transfers the vector.

In Figure 4-5, a DMA request/grant sequence is shown. Note that when bus grant (BDMGO) is received, the DC010 becomes bus master. It generates the signals for an INWD transfer from system memory to the DMA data latches.

NOTE

A DATIO or DATIOB sequence is made up of a DATI followed by DATO or DATOB.

NOTE

On Q-bus systems, BDAL<17:16> are used to provide data parity information to the bus master. To prevent the DHV11 from generating false parity information, AD<17:16> are only enabled onto the BDALs when the DHV11 is bus master. ADREN from the DMA controller performs the enable function.

A description of DC003, DC004, DC005, and DC010 is included in Appendix A.

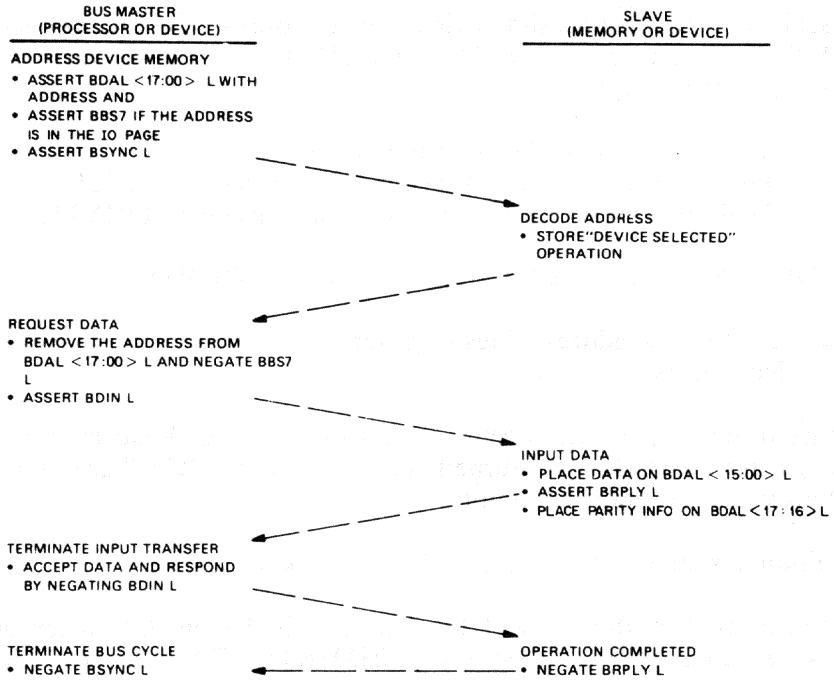


Figure 4-2 DATI Bus Cycle

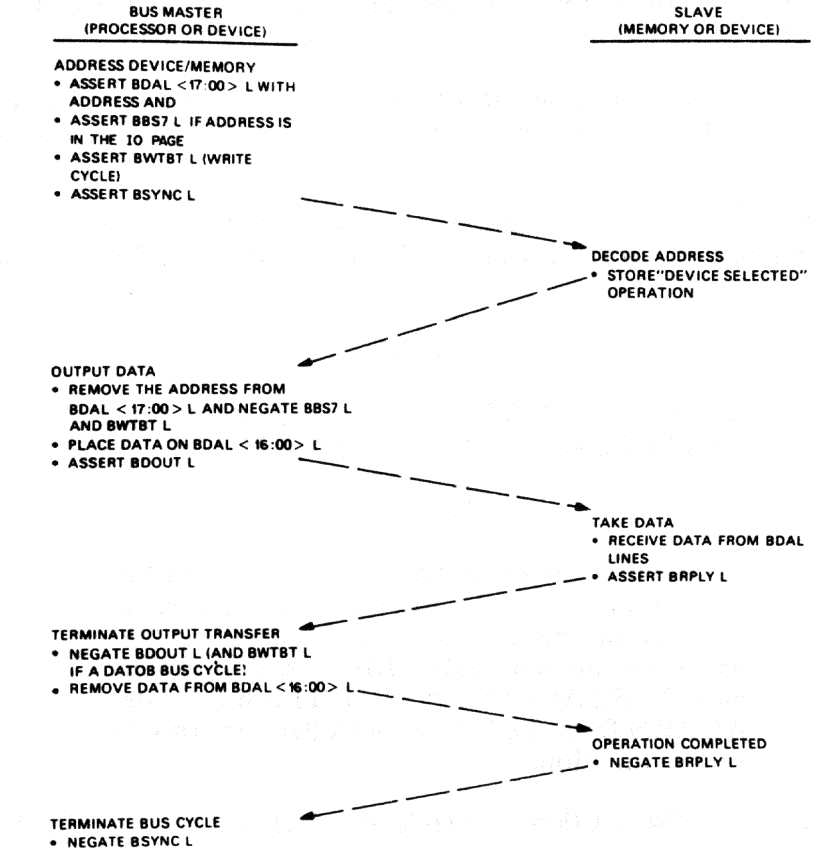


Figure 4-3 DATO or DATOB Bus Cycle

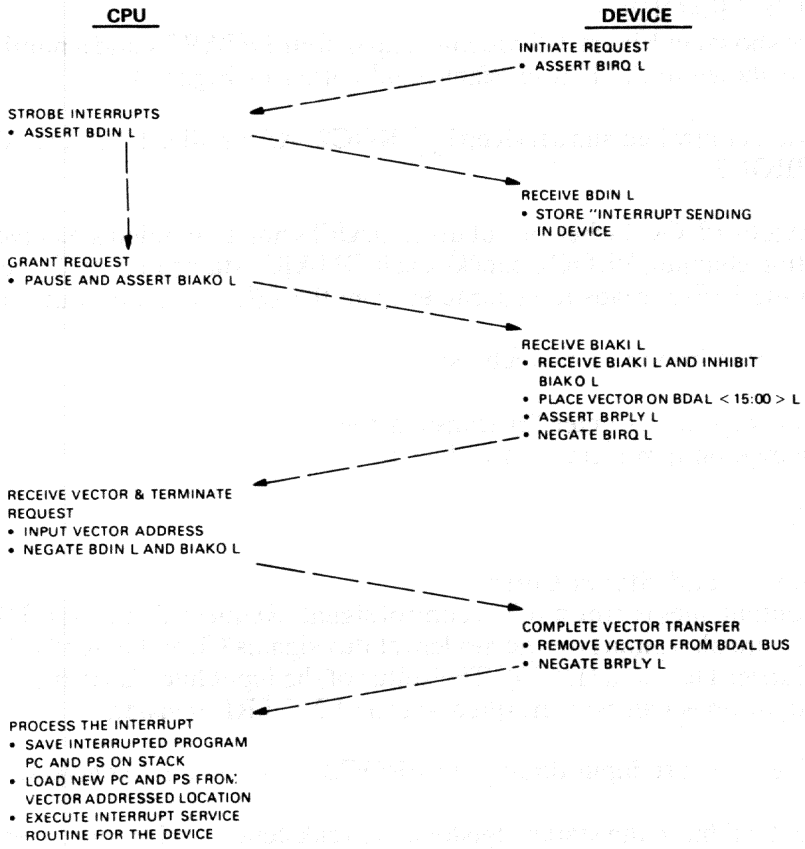


Figure 4-4 Interrupt Request/Acknowledge Sequence

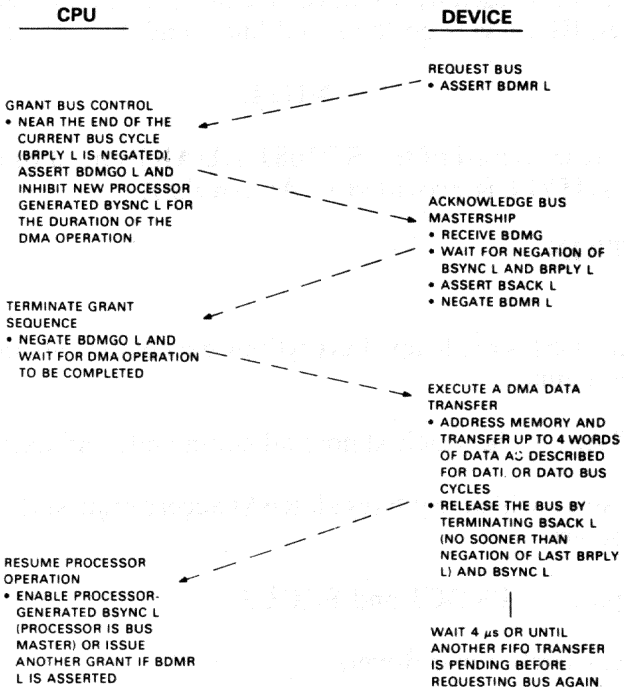


Figure 4-5 DMA Request/Grant Sequence

4.3 SERIAL INTERFACES

The serial interfaces shown in Figure 1-5 are made up of four DUARTs and a number of line drivers and receivers. These are shown in the bottom right-hand corner of Figure 4-1.

The four DUARTs are controlled and serviced by PROC2. All parallel data into and out of the DUARTs is transferred via PROC2.

A common interrupt tells PROC2 when one of the DUARTs has assembled a received character. In order to find the interrupting channel, PROC2 checks each DUART status in turn. It then constructs a status byte, transfers it to the FIFO, reads the character from the DUART, and transfers that to the FIFO.

All other DUART status information, such as:

- Ready to accept a character for transmission
- Status change on a modem control line

is polled by PROC2.

4.3.1 Modem Control and Status Lines

Each DUART has output lines for the modem control signals Request To Send (RTS) and Data Terminal Ready (DTR). There are also inputs for the modem status signals Clear To Send (CTS), Data Set Ready (DSR), and Data Carrier Detected (DCD). The status of the input lines is visible to the host through the STAT register. Output lines can be controlled via the LNCTRL register.

Ring Indicator (RI) signals are input directly to PROC2 from the line receivers.

There is no 'break detect' bit in the status registers. A break condition is reported via the FIFO as a null character with the framing error bit set.

4.3.2. EIA/TTL Level Conversion

Interface to the serial lines is provided by 9636AC line drivers and 9637AC receivers. These inverting amplifiers convert between EIA levels on the serial lines, and TTL levels at the DUARTs.

NOTE

More detail of the SC2681 DUARTs used in the DHV11 is provided in Appendix A3.

4.4 CONTROL SECTION

4.4.1 General

The control section (Figure 1-5) is made up of everything except the two interfaces which have just been described. This section contains:

- The common RAM – via which almost all commands and data are routed
- The store arbitrator – which regulates all RAM access requests from the host and the DHV11's two microcomputers
- The microcomputers – PROC1 and PROC2
- Data and address latches and drivers

- FIFO control and address circuits – which supply the appropriate FIFO addresses
- The CSR – which is the main control register.

The CSR is a separate set of latches and is not part of common RAM.

4.4.2 Common RAM

4.4.2.1 Memory Map – The common RAM (common to both microcomputers) is mapped to microcomputer addresses 8000_{16} to $87FF_{16}$ as shown in Figure 4-6.

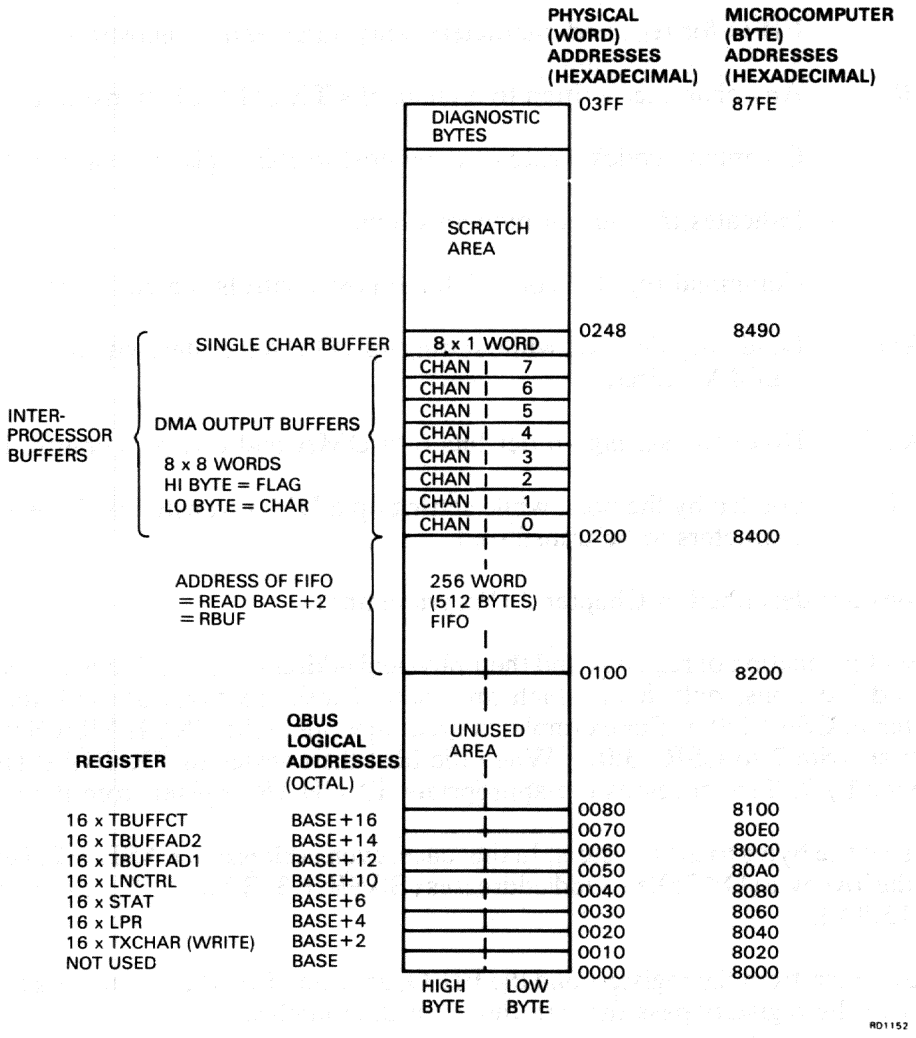


Figure 4-6 Common RAM – Memory Map

The top 1K bytes (above the FIFO) are used by PROC1 and PROC2 for interprocessor buffers and a scratch area.

Each channel has an 8-word buffer for DMA characters. There are also eight 1-word buffers (one for each channel) for single-character programmed transfers. By using buffers, the DHV11 is able to transmit more efficiently. Buffers are filled by PROC1 and emptied by PROC2.

Each word of a buffer has a flag byte (D<15:8>) and a character byte (D<7:0>). When PROC1 transfers a character to a buffer, it sets the flag byte to a non-zero condition. When PROC2 transfers a character to a UART, it clears the flag byte to zero. In this way, the flag byte is used as a handshake between PROC1 and PROC2.

The top eight words are reserved for self-test diagnostic bytes.

4.4.2.2 **Registers** – The DHV11 is controlled via registers. There are seven for each channel, plus the FIFO (RBUF) and a common CSR. The functions of registers are as follows:

CSR – Main control register for channel selection, important flags, and control bits

RBUF – FIFO for received characters, and status and diagnostic information

TXCHAR – Any character written to a channel's TXCHAR is transmitted on that channel

LPR – Command codes written by the host to this register configure the channel

STAT – Indicates the current modem status

LNCTRL – Command register via which the host controls the channels

TBUFFAD1 – Loaded by the host, while setting up a DMA transfer, with the 15 low-order bits of a DMA address

TBUFFAD2 – Holds the six high-order bits of a DMA address, plus control bits

TBUFFCT – Loaded by the host, while setting up a DMA transfer, with the number of DMA characters to be transferred.

Register functions are described in Chapter 3 (Programming).

Figure 4-6 shows the location of registers and their physical addresses. Each block allocated to a register contains 16 word locations, only 8 of which are used. These locations are indexed by an address previously written to CSR<3:0>. For example, in order to write to the TXCHAR register for channel 7, the host must first write 7 to CSR<3:0>. When the host then writes to TXCHAR (BASE + 2), the address is indexed by 7. This accesses the appropriate TXCHAR register from the block of 16.

The host can also write bytes to the registers. In that case, even addresses (BASE + 2, BASE + 4, and so on) will access the low byte (D<7:0>). Odd addresses (BASE + 3, BASE + 5, and so on) will access the high byte (D<15:8>).

Transfers to the master, from the registers and the FIFO, are routed via the output data latches. Transfers from the master to the registers pass through the input data latches.

4.4.2.3 **FIFO** – This 256-word RAM area usually contains received characters and status information. When the host reads from BASE + 2(RBUF), the oldest word in the FIFO is transferred.

There is only one received character buffer (RBUF). The index bits (CSR<3:0>) are ignored during a read action from RBUF.

4.4.3 RAM Access

(See Figure 4-7.) The common RAM can be accessed by the host, or by each of the DHV11 microcomputers. Therefore, it is a 3-port memory.

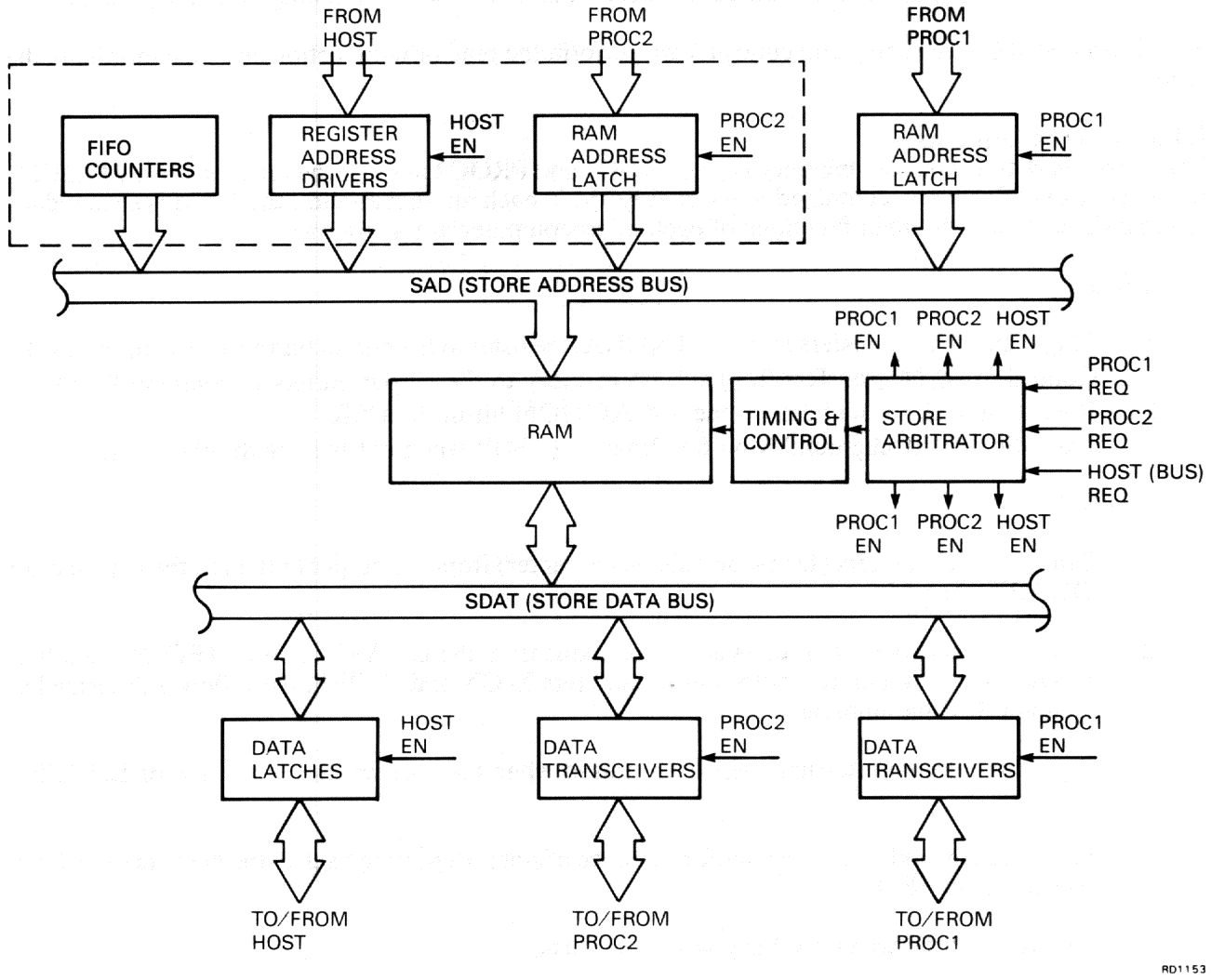


Figure 4-7 Common RAM Access

Addresses (Figure 4-7) come from four sources:

- PROC1
- PROC2
- The host processor (via translation logic)
- The FIFO Fill and Empty counters.

During a write to FIFO (by PROC2) or a read from FIFO (by the host), the RAM address is given by one of the FIFO counters. Dotted lines in Figure 4-7 indicate that this area is oversimplified.

Figure 4-1 shows more detail of the same circuit.

4.4.4 Store Arbitrator

When one of the microcomputers or the host needs to access the RAM, it will generate a request for store access. The store arbitrator (Figures 4-7 and 4-1) sequentially scans the request lines. When it detects a request, that request is granted and the other two requests are locked out. The arbitrator issues enable signals for the appropriate address and data sources, and starts memory timing and control logic.

Signals produced by the timing and control logic perform the read or write action and then terminate the access.

4.4.5 Microcomputers

Using the RAM as a common reference point, PROC1 and PROC2 manage the functions of the DHV11. Under control of firmware, contained in internal ROM in each microcomputer, the RAM is scanned for commands or data. The main functions of each microcomputer are as follows:

PROC1

1. Single-character transfers from the TXCHAR register to the output buffers in common RAM.
2. Control of DMA transfers from system memory to the output buffers in common RAM.
3. Reporting back to the host via the TX.ACTION bit in the CSR.
4. Executing the Background Monitor Program (BMP) when not busy with other tasks.

PROC2

1. Transfer of characters (DMA and single character) from the output buffers to the appropriate DUART channel.

2. Transfer of received characters and error status from the DUARTs to the FIFO. Recognition of automatic flow control (auto-flow) characters X-ON and X-OFF. Auto-flow is described in Chapter 3, Programming.

3. Servicing internal interrupts which are raised when the host writes to the LPR or LNCTRL registers.

4. Scanning the modem status lines for a change of state. Reporting back to the host via the STAT register and FIFO.

5. Executing BMP when not busy with other tasks.

4.4.6 Address and Data Latches

To meet the interface timing demands, latches are used for all transfers between the host and the DHV11. For example, to transmit a single character, the host writes the character to the TXCHAR register. During this action the TXCHAR address is latched into the register address latch. The data is latched into the input data latches. The arbitration and timing and control circuits complete the transfer to TXCHAR.

Characters transferred by DMA are not routed through the TXCHAR register. Special DMA latches are provided for this purpose.

At the beginning of a DMA cycle the next DMA address is written to the DMA address latches (Figure 4-1). This generates a DMA request to the DMA control IC, DC010, which transfers the next word from host memory to the DMA data latches. PROC1 will transfer the word (two characters) from the latches to the DMA buffer area in common RAM.

4.4.7 FIFO Addresses

The FIFO is implemented in common RAM. It is filled by PROC2 and emptied by the host. It is made to act like a FIFO by the action of two counters.

The Fill counter provides addresses during PROC2 FIFO WRITE actions. It points to the next available location. The counter is incremented after each word (two separate bytes) is written.

The Empty counter provides addresses during a FIFO READ action by the host. It addresses the oldest word in the FIFO. It is incremented after each word is read.

4.4.8 FIFO Control

Received characters are transferred from the DUARTs to the FIFO in order to be read by the host. PROC2 loads the status (high) byte and then the character (low) byte. The host reads this information as a full word. A FIFO control circuit manages these actions by monitoring GRANT signals from the store arbitrator and READ or WRITE signals from the host or PROC2.

The functions of the FIFO control circuit are as follows:

- Gating the appropriate FIFO counter onto the store address (SAD<9:0>) bus
- Incrementing the appropriate counter after access
- Disabling both FIFO addresses when the FIFO is not being accessed
- Reporting the state of the FIFO (FULL, ALARM, EMPTY) to PROC2 and the CSR.

4.5 OTHER CIRCUITS

4.5.1 Voltage Converter

Line drivers and receivers need both +12 V and –12 V in order to generate line signals at EIA levels. The voltage converter, which is a small Switch Mode Power Supply (SMPS), produces –12 V from the +12 V supply.

4.5.2 Oscillators

Also on the module are the following circuits:

- Oscillator to provide 24 MHz, 12 MHz and 6 MHz clock signals for the timing circuits
- Oscillator of 3.6864 MHz to provide the basic clock for DUART data rates.

4.6 DATA FLOW

DHV11 firmware uses interrupt timers in PROC1 and PROC2 to enter certain routines which handle data and check the control registers. Therefore a delay, dependent on the timer interval, can be introduced into some data paths. When referring to Figures 4-8 to 4-14, these delays must be considered.

The delays are as follows:

1. TXCHAR to single-character transmit buffers:

   Every 780 microseconds PROC1 checks for characters in each TXCHAR register. If available, one character will be transferred to the buffers from each register.

2. DMA data latch to DMA buffer area:

   Each time PROC1 services the single-character buffers it also checks, and services if needed, one pair of channels for DMA. The channels are serviced in rotation. This means that a specific channel is serviced every 4 × 780 microseconds = 3.12 milliseconds. PROC1 will transfer up to eight characters to each of the two DMA output buffers in common RAM (Figure 4-6). It is this timer which limits single-character transmission to 1000 characters per second.

3. Single-character or DMA output buffer to DUART:

   Every 480 microseconds PROC2 checks the interprocessor buffers for valid data. If there is data waiting, a character will be transferred to each DUART channel which is ready to take a character. It is this timer which limits DMA transmission per channel to 2000 characters per second.

4. DUART to FIFO:

   Received characters are not handled by timer-driven interrupts, but by direct interrupt from the DUART. Therefore, in comparison with transmitted characters, the delay is not significant.

5. The DMA start bit is sampled every 3.12 milliseconds. There is also a delay of up to 480 microseconds in PROC2. This gives an average delay of 1.8 milliseconds before a DMA transfer is started.

Timer dependent tasks of PROC2 may be delayed by:

1. The receive interrupt

2. The parameter change interrupt which is raised (by hardware) when the host writes to the LPR or LNCTRL registers. (It may have to change the DUART configuration or the state of modem control lines)

3. The need to monitor modem status lines. These are sampled every 10 milliseconds.

From the foregoing it should be clear that PROC2 delays are to a great extent dependent on application and on throughput.

In the following descriptions of data flow, the basic timer delays are noted against the appropriate data paths on the diagrams.

4.6.1 Host Read from a Register

(See Figure 4-8.) Except for RBUF or the CSR, the channel number must first be written to CSR<3:0>. This is followed by a READ from BASE + n (see Figure 4-6).

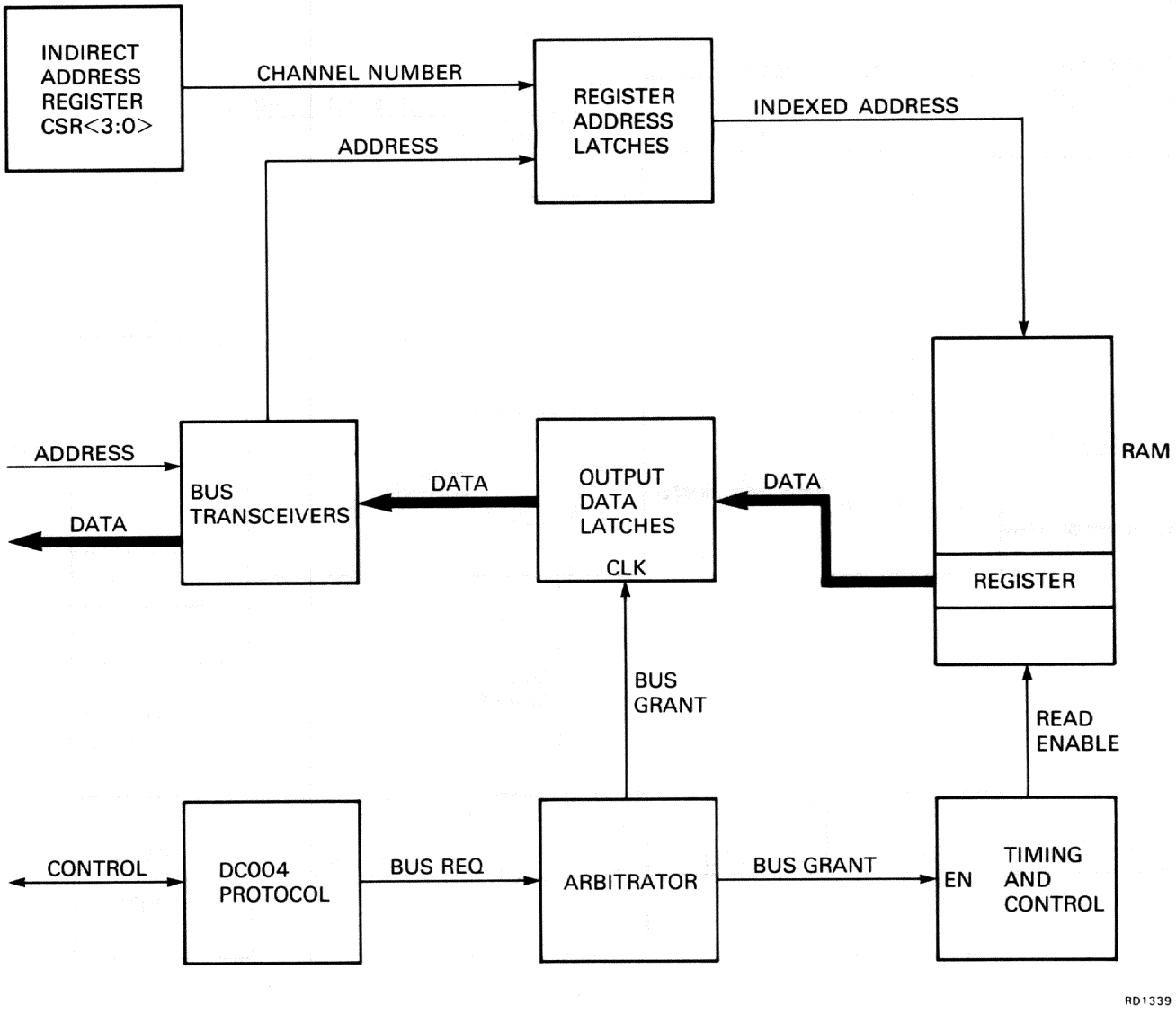


Figure 4-8 Reading from a Register

The register address is latched into the register address latches, to be applied to the RAM when bus access is granted.

The READ action from the host generates a BUS REQUEST to the store arbitrator, which generates BUS GRANT. This starts the timing signals which read a word from the addressed register. When BUS GRANT is deasserted, the data is latched into the output data latches.

BRPLY (Figure 4-2) is inhibited until data transfer to the output latches is complete. BRPLY is then asserted. READ signals on the Q-bus transfer the word to the host.

4.6.2 Writing to a Register

(See Figure 4-9.) In order to write to a register the channel number is first written to CSR bits <3:0>. This is followed by a WRITE to BASE + n (see Figure 4-6).

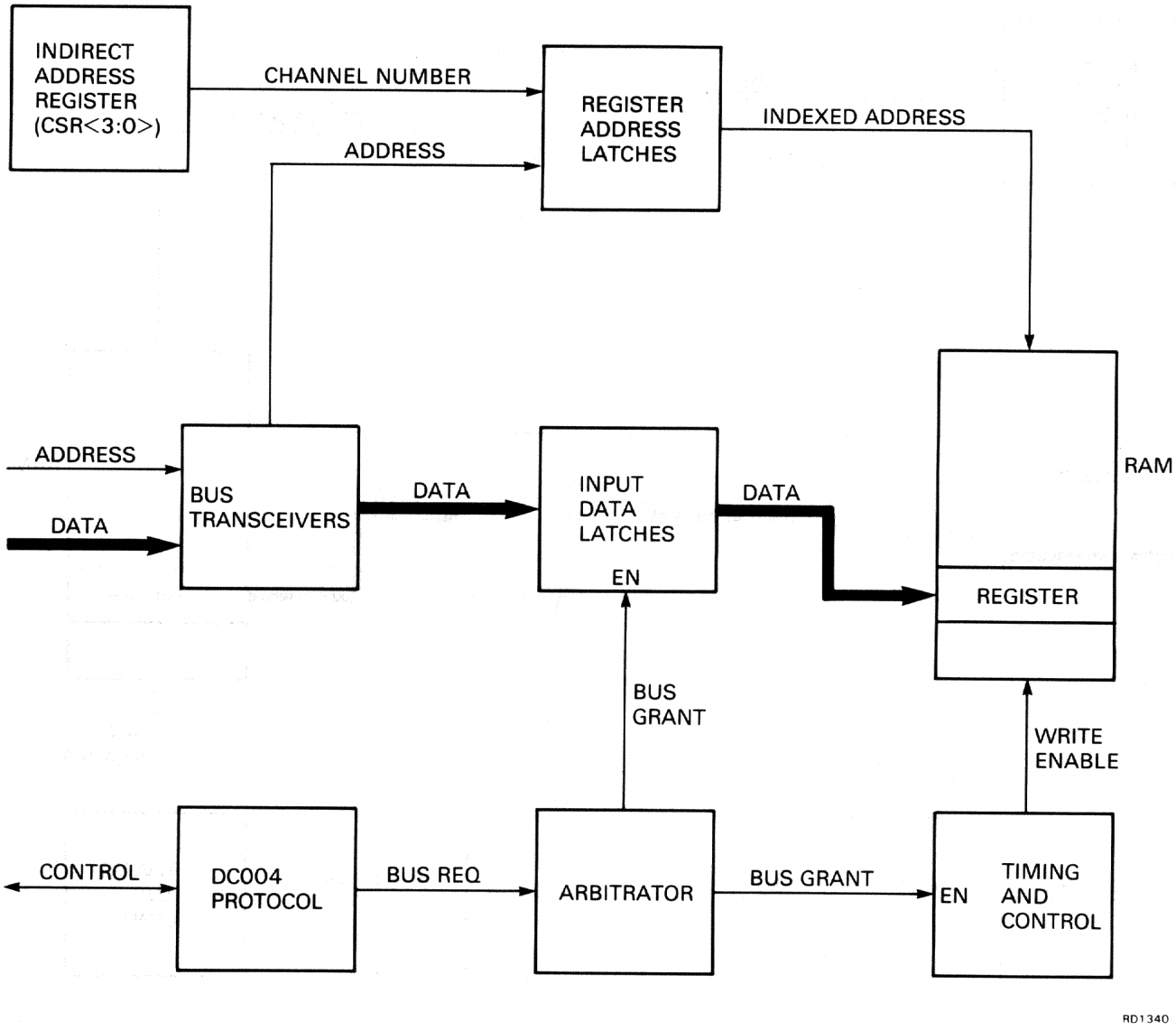


Figure 4-9 Writing to a Register

The register address is latched into the register address latches and is applied to the RAM when the bus access is granted. The data to be written is latched into the input data latches.

The WRITE action from the host generates a BUS REQUEST to the store arbitrator. BUS GRANT enables the data from the input data latches and provides RAM timing signals. Data will be written to the addressed register.

For a WRITE BYTE action, address line 0 will select the high or low byte of a word.

4.6.3 Single-Character Transmit

(See Figure 4-10.) To transmit a character by use of the single-character transmit facility, the character and the DATA.VALID bit can be written to the TXCHAR register. This would be done exactly as in Section 4.6.2. To transmit subsequent characters, the TX.ACTION bit for this channel must be checked by polling or via interrupts.

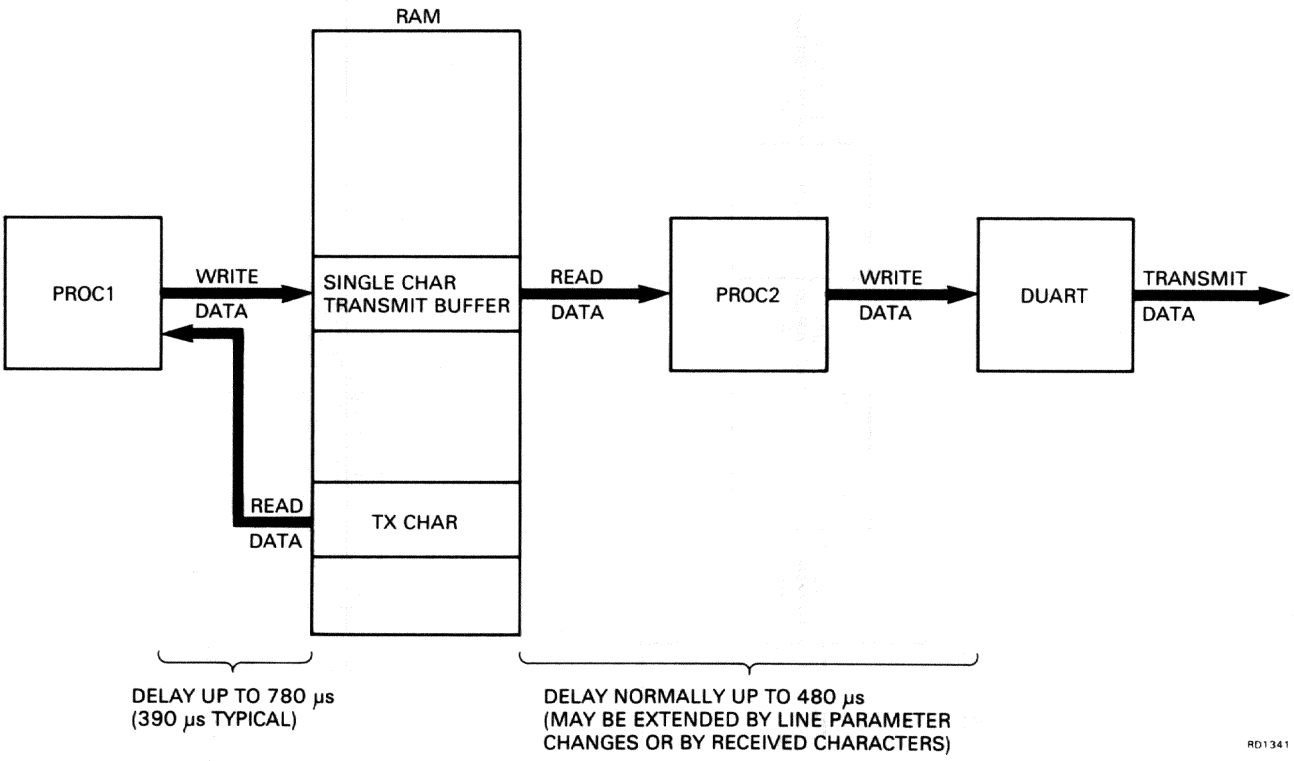


Figure 4-10 Single-Character Transmit

PROC1, which scans the TXCHAR register, detects from the data valid bit that a new character has been written. It reads the character and then transfers it to the single-character buffer area in the common RAM (Figure 4-6). PROC1 writes the channel number and the TX.ACTION bit to report acceptance of the character.

PROC2, which scans the buffer area, reads the character from the buffer area and writes it to the appropriate DUART. The DUART then transmits the character serially on the appropriate channel.

4.6.4 DMA Transmissions

Section 3 (Programming) describes how a DMA block transfer is set up. The host writes a DMA buffer start address, the number of characters to be transferred, and a TX.DMA.START bit to TBUFFAD1, TBUFFAD2, and TBUFFCT.

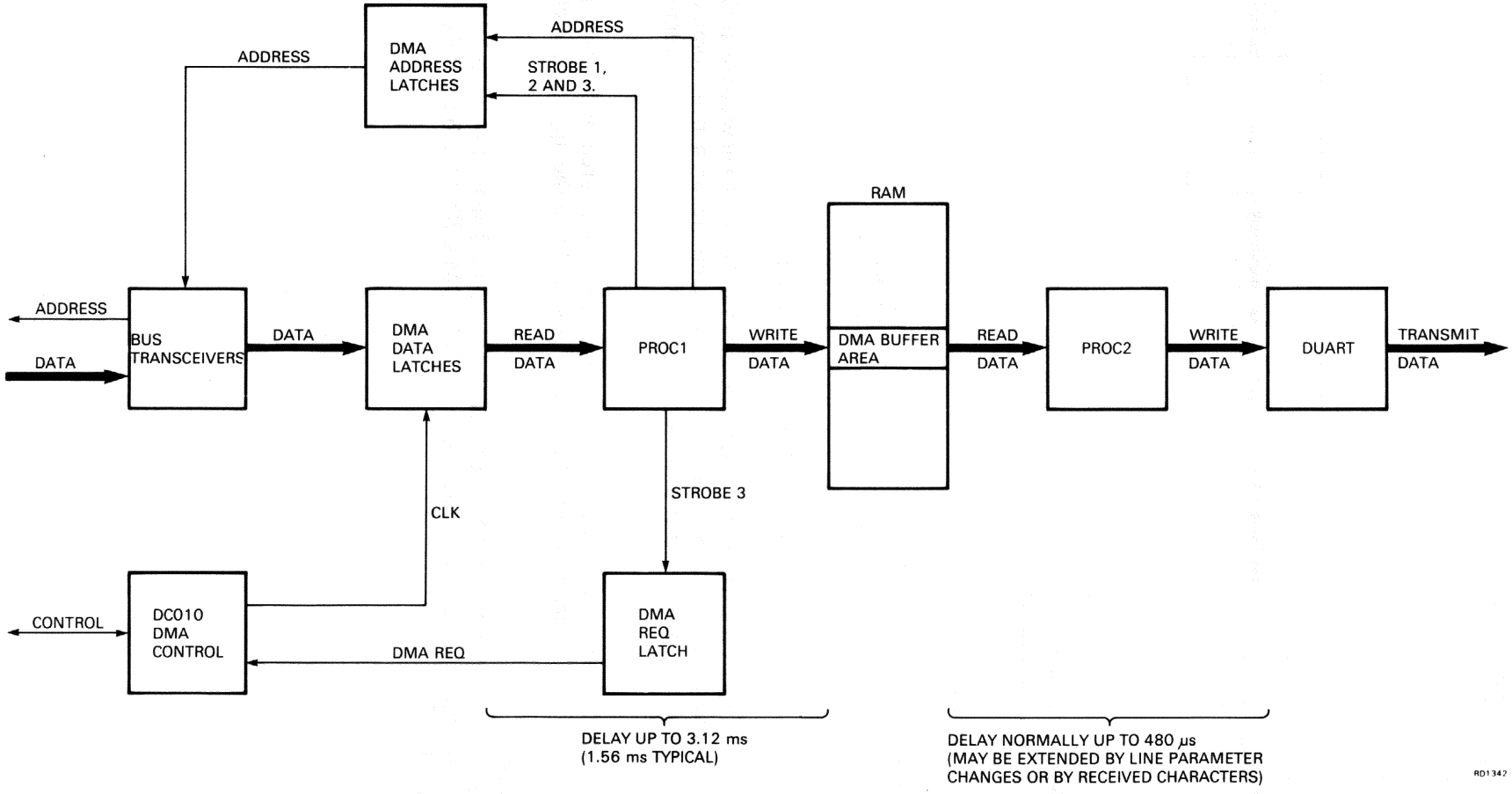


Figure 4-11 DMA Data Transfer

4.6.4.1 DMA Block Transmit – Figure 4-11 shows the data flow for a DMA transfer.

When the host sets TX.DMA.START, PROC1 writes the DMA address (in three bytes) to the DMA address latches. Writing the most significant address byte sets the DMA request latch, which starts a DMA transfer.

The DC010 performs a READ from memory, using the DMA address held in the address latches.

The DMA cycle always transfers a word from system memory to the DMA data latches. PROC1 reads the word (two characters) one byte at a time, and transfers them, via its data transceivers, to a buffer area in RAM. Note that PROC1 can only write to the buffer area if there is space for at least two characters.

PROC2, which scans the buffer area, reads the character from the buffer area and writes it to the appropriate DUART.

The DUART transmits the character serially on the appropriate channel.

4.6.4.2 DMA Data Management – When a DMA block starts with an odd address, or ends with an even address, PROC1 will transfer the addressed character only, to the output buffer.

Figure 4-12 shows how DHV11 manages a 9-byte DMA transfer. The start address is 1061_8 and the end address is 1072_8.

PROC2 transfers characters from the buffer area, exactly as in Section 4.6.4.1.

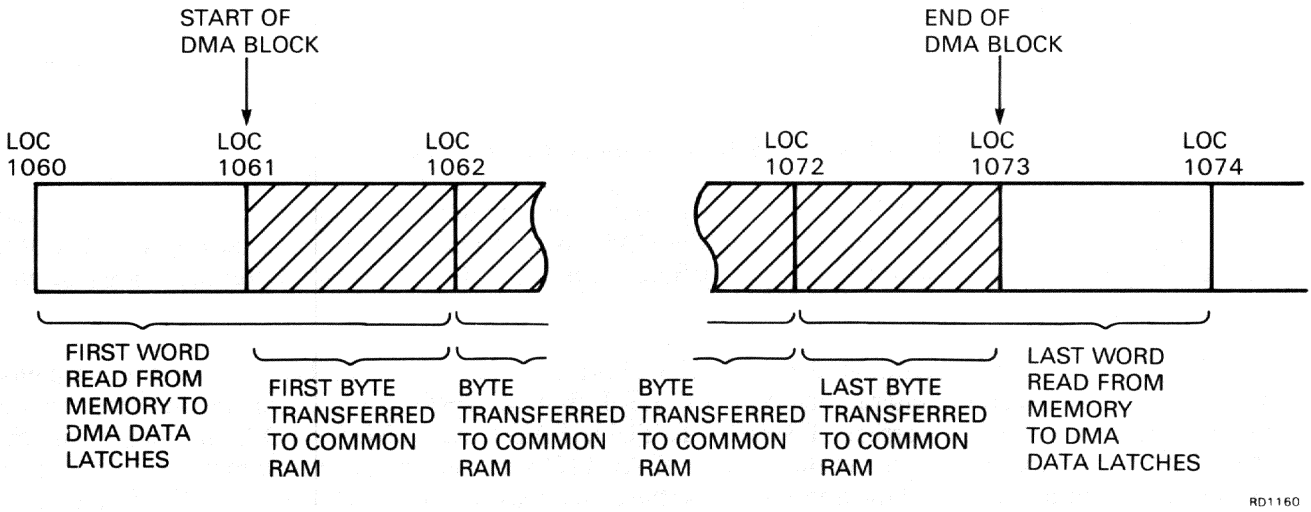


Figure 4-12 DMA Character Handling

4.6.4.3 DMA Error Detection and Timeout – Q-bus protocol demands that, during a bus transaction, a bus master which does not receive BRPLY within 10 microseconds of sending BSYNC should terminate the transaction. For a DMA transfer the DHV11 becomes bus master; therefore it must obey the timeout rule. The DHV11 also checks parity bits BDAL 17 and 16.

At the beginning of each DMA cycle the DMA controller uses ADREN (address enable) to gate the DMA address onto the Q-bus. The trailing edge of this signal starts a hardware counter (Figure 4-13) which will time out after 10.7 microseconds if there is no reply from the bus. The counter is cleared by its own timeout or by a bus reply.

The DMA error status is cleared by a DMA request. It will generate a DMA error signal (DMA ERROR) if the timer times out or if a memory parity error (BDAL 17 and 16 asserted) is detected. The parity error is latched when the bus reply goes false at the end of the transaction.

At the end of the DMA cycle, when the DC010 deasserts BDIN, a DMA COMPLETE signal (Section 4.7.1.2) is generated. When PROC1 detects DMA COMPLETE it checks the state of DMA ERROR. If an error is detected, the DHV11 will read the same location once more before reporting an error to the host.

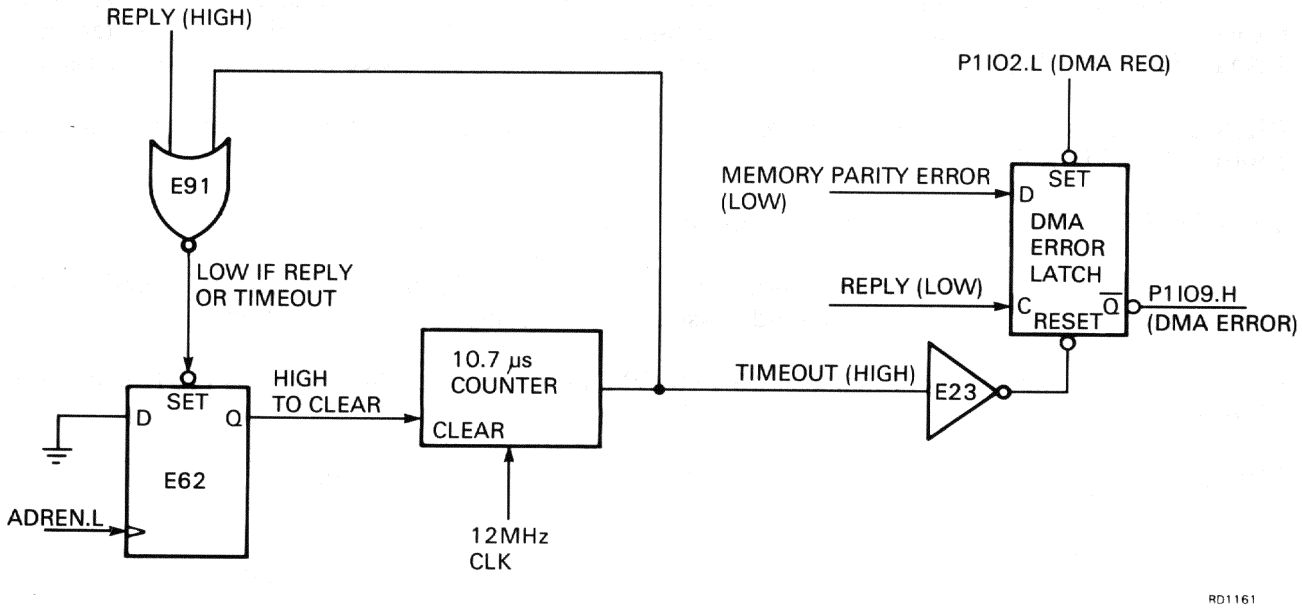


Figure 4-13 DMA/Memory Error Generation

4.6.4.4 DMA Abort – PROC1 transfers DMA data from the host, in blocks of up to eight characters (four words). The data is held temporarily in the DMA output buffer area in common RAM. PROC2 scans the buffer for data, and transfers it byte by byte to the DUARTs. Separate buffer areas are reserved for each channel.

A DMA sequence can be terminated by a DMA abort command from the host. When this happens, PROC2 stops the transfer of characters to the DUART channel. PROC1 stops transferring data, counts the characters in the buffer, corrects TBUFFCT, TBUFFAD1, and TBUFFAD2, and then clears the DMA buffer area for this block. It then sets TX.ACTION to report that the transmission has been aborted. To continue transfer of the aborted block, the host need only clear TX.DMA.ABORT and set the TX.DMA.START bit. The transfer will continue without losing characters.

4.6.5 Receiving

(See Figure 4-14.) When a serial channel has assembled a character, it will raise an interrupt. PROC2 will respond by reading status from each DUART in turn. When it finds the interrupting channel, PROC2 will transfer an error/line-number status byte and the character byte to the FIFO.

PROC2 writes all receive information to a 1-word address in the RAM; C040 = low byte, C041 = high byte. These addresses are decoded and ANDed with 'PROC2 grant' to enable the FIFO Fill counter. This counter provides the actual FIFO address. The counter is incremented after each character byte is transferred. Therefore the character (low byte of RBUF) is transferred last.

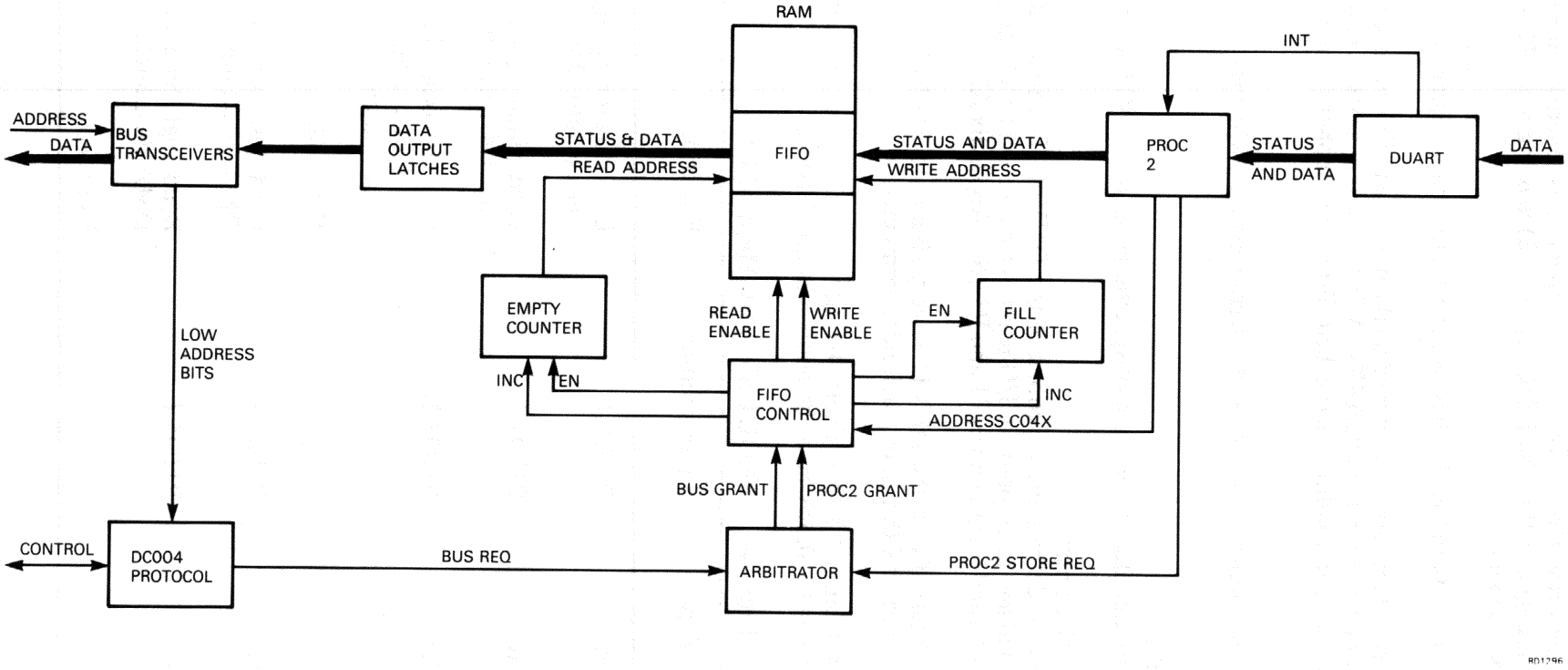


Figure 4-14 Receiving a Character

To read the FIFO, the host performs a 'read from register' sequence as described in Section 4.6.1. In this case, however, the DC004 recognizes that the FIFO (Base + 2) is being read. This causes the Empty counter and the FIFO to be enabled.

The data is transferred via the data output latches as for a 'read from register' operation.

If characters are received faster than they are removed by the host, the FIFO will eventually become full. PROC2 will stop taking characters from the DUARTs. A further four characters can be buffered in any DUART channel before the overrun condition is reached. When this happens, any overrun channel will be flushed.

When space is available, a null character (one for each overrun channel) with the overrun error bit set will be placed in the FIFO.

4.7 TECHNICAL DETAIL

This section provides a more detailed description of specific areas of DHV11 logic and electronics.

4.7.1 DHV11 Internal I/O Control

PROC1 and PROC2 firmware defines the functions of the DHV11. The functions managed by the microcomputers are controlled and monitored via I/O ports associated with each microcomputer. These are memory-mapped I/O ports, and integral ports P1 and P3. (See Appendix A2, 8051 Microcomputer.)

Memory-mapped I/O used internally on the DHV11 is very similar to PDP-11 memory-mapped I/O architecture. I/O addresses start at $C000_{16}$ on each microcomputer.

4.7.1.1 PROC1 Memory Mapped I/O – Table 4-1 lists the addresses and functions of PROC1 memory-mapped I/O. Figure 4-15 shows how the addresses are decoded.

Table 4-1 PROC1 Memory-Mapped I/O

Address (Hexadecimal)	I/O Type	Signal Name	Function
C000	Write	P1IO0.L	Load low-order eight bits of DMA address into DMA address latch.
C001	Write	P1IO1.L	Load middle eight bits of DMA address into DMA address latch.
C002	Write	P1IO2.L	Load high-order six bits of DMA address into DMA address latch. Set DMA request latch.
C003			Not used.
C004	Read	P1IO4.L	Read low byte of DMA data from DMA data latch.
C005	Read	P1IO5.L	Read high byte of DMA data from DMA data latch.
C006			Not used.

Table 4-1 PROC1 Memory-Mapped I/O (Cont)

Address (Hexadecimal)	I/O Type	Signal Name	Function
C007	Write	P1IO7.L	PROC1 CSR write. Also starts a dummy store-access sequence. This is to prevent access conflicts to this register.

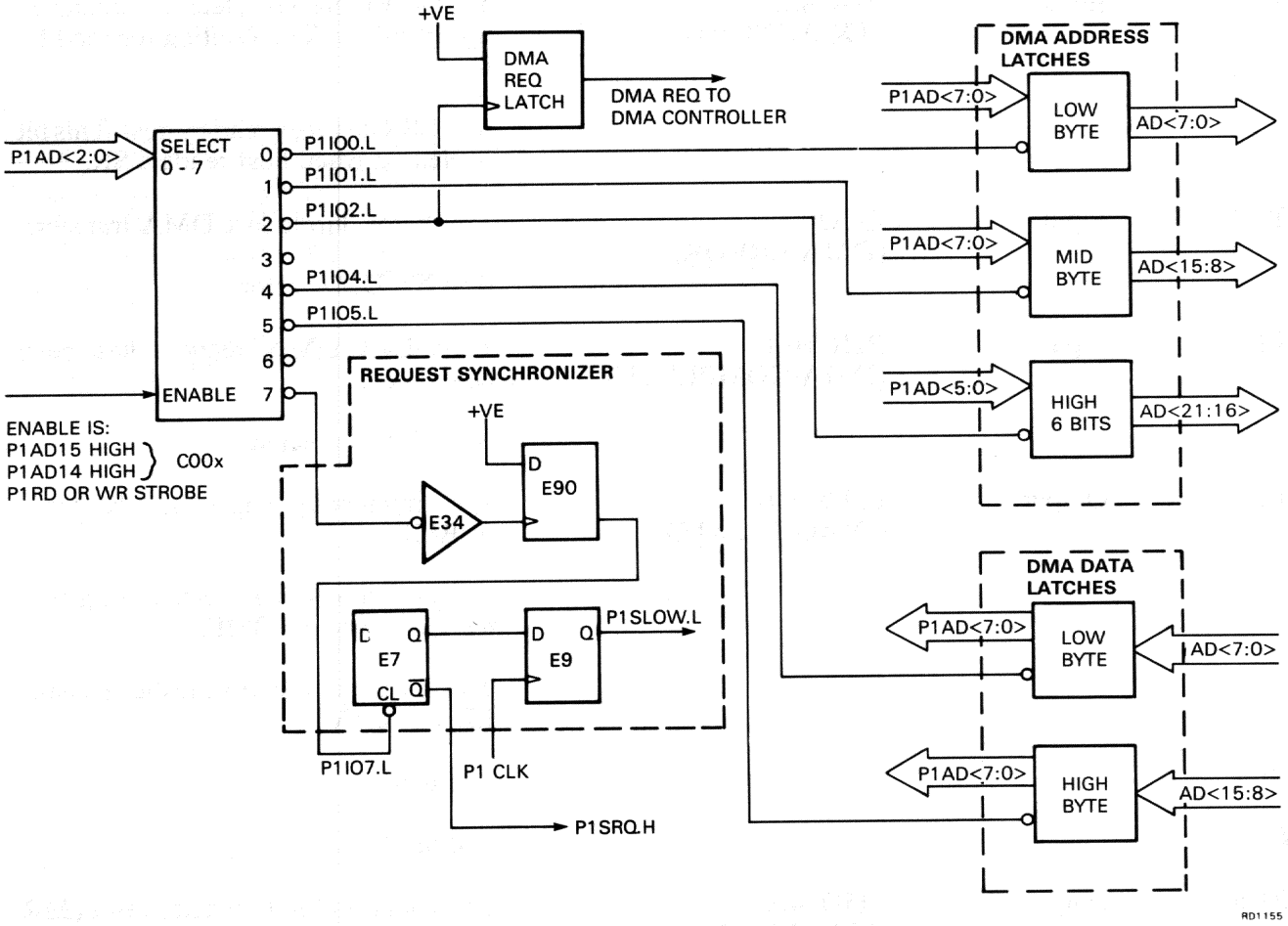


Figure 4-15 PROC1 I/O Decoding

4.7.1.2 PROC1 Integral I/O Port Functions – Table 4-2 lists the functions of the integral ports used by PROC1.

Table 4-2 PROC1 Integral I/O Port Functions

Port	Direction	Signal Name (Explanatory Title)	Function
P1.0	Input	P1IO8.L (TX ACTION)	1 = DHV11 has completed or terminated a transmit action. Waiting for read by host. 0 = CSR has been read by host. This bit is cleared when host reads CSR.
P1.1	Input	P1IO9.H (DMA ERROR)	1 = Error during last DMA transfer. 0 = No DMA error.
P1.2	Input	P1IO10.H (DMA COMPLETE)	1 = Last DMA request has been completed. 0 = Not completed.
P1.3	Output	P1IO11.H (DIAG ERROR)	1 = Error found during self-test diagnostic or BMP. 0 = No error was detected during self-test diagnostic or BMP. This bit drives the 'diagnostics passed' LED directly.
P1.4			Not used.
P1.5			Not used.
P1.6	Output	P1IO14.L (MR CLEAR)	0 = Clear and hold master reset (MR CLEAR) latch. 1 = Release hold.
P1.7			Not used.
P3.0	Input	IPSL0	Serial input line to PROC1 internal UART.
P3.1	Output	IPSL1	Serial output line from PROC1 internal UART. The above two serial lines connect to PROC2 internal UART for direct reporting during diagnostics.

Table 4-2 PROC1 Integral I/O Port Functions (Cont)

Port	Direction	Signal Name (Explanatory Title)	Function
P3.2			Not used.
P3.3			Not used.
P3.4	Input	P2INT1.L	PROC2 interrupt monitor 0 = Pending change to LPR or LNCTRL registers. 1 = No pending change.
P3.5			Not used.
P3.6	Output	P1WR.L	Common RAM write strobe.
P3.7	Output	P1RD.L	Common RAM read strobe.

4.7.1.3 PROC2 Memory-Mapped I/O – Table 4-3 shows the addresses and functions of PROC2 memory-mapped I/O. Figure 4-16 shows how the addresses are decoded. The low address lines are used to select one of 16 registers in each DUART.

Table 4-3 PROC2 Memory-Mapped I/O

Address (Hexadecimal)	I/O Type	Signal Name	Function
C000 to C00F	Read/Write	UART0.L	Chip select DUART 0. Internal registers addressed by AD0 to AD3.
C010 to C01F	Read/Write	UART1.L	Chip select DUART 1. As above.
C020 to C02F	Read/Write	UART2.L	Chip select DUART 2. As above.
C030 to C03F	Read/Write	UART3.L	Chip select DUART 3. As above.
C040	Write	FIWR.L	Writes the low byte of the FIFO word (usually the received character) to the FIFO. The trailing edge increments the FIFO address pointer (so it is written after the status byte). AD0 = 0.

Table 4-3 PROC2 Memory-Mapped I/O (Cont)

Address (Hexadecimal)	I/O Type	Signal Name	Function
C041	Write	FIWR.L	Writes the high byte (status) to the FIFO. Written before the low byte. AD0 = 1.
C050	Write	FICL.L	Clears the FIFO address counters at bus or DHV11 reset. (In effect empties the FIFO.)
C060			Not used.
C070	Write	INTCL.L	Clear interrupt request PROC2. When the LPR and LNCTRL registers are written, a hardware interrupt request is raised to alert PROC2. During the interrupt routine, PROC2 clears the interrupt request via INTCL.L.

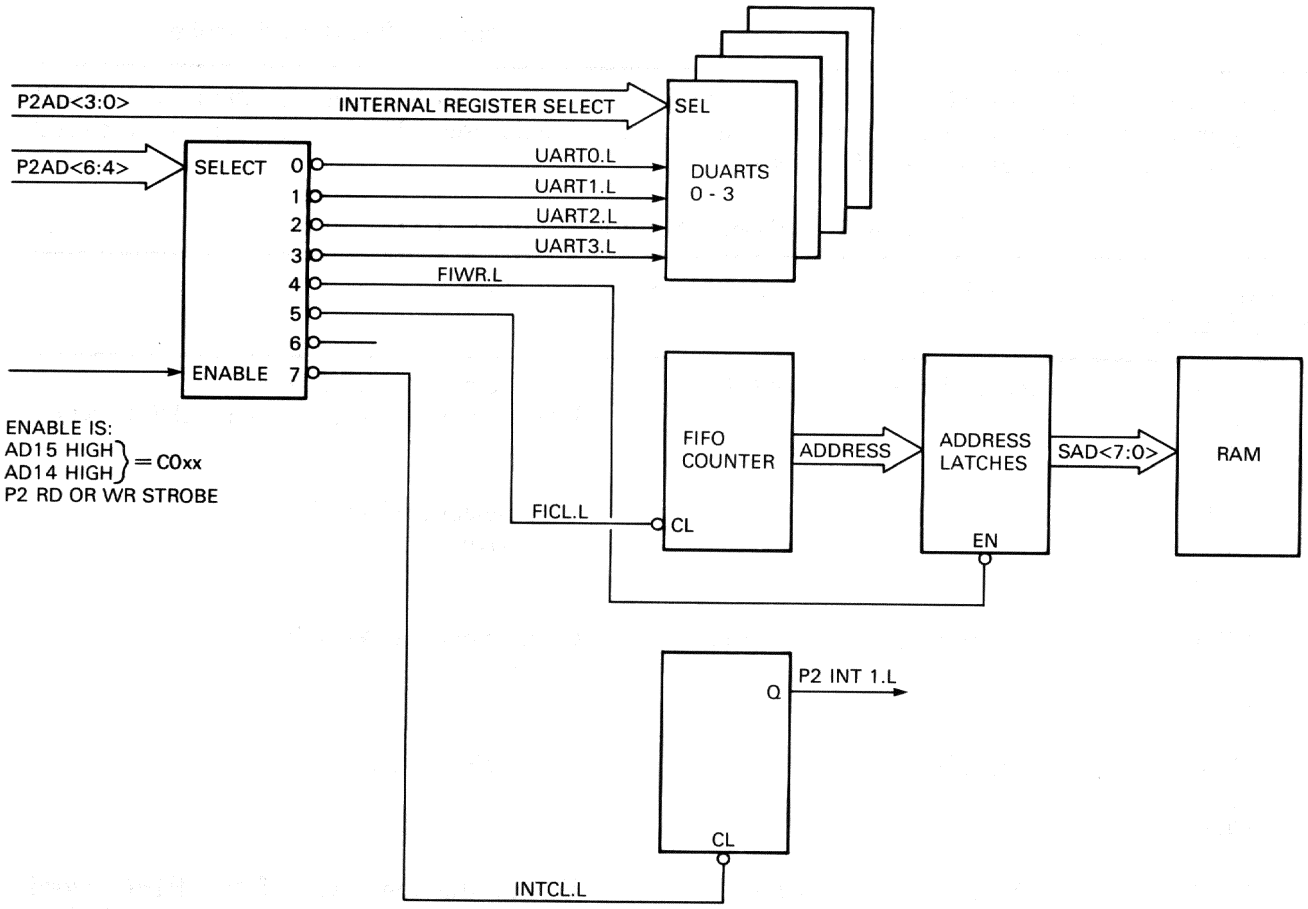


Figure 4-16 PROC2 I/O Decoding

4.7.1.4 PROC2 Integral I/O Port Functions – Table 4-4 shows the function of the integral ports used by PROC2.

Table 4-4 PROC2 Integral I/O Port Functions

Port	Direction	Signal Name	Function
P1.0 to P1.7	Inputs	RIB0.L to RIB7.L	Indicates the state of the Ring Indicator lines 0 to 7 from modems. 0 = ON, 1 = OFF.
P3.0	Input	IPSL1	Serial input line to internal UART, PROC2.
P3.1	Output	IPSL0	Serial output line from internal UART, PROC2. **The above two serial lines connect to the PROC1 internal UART for direct reporting during diagnostics.**
P3.2	Input	P2INT0.L	0 = DUART service interrupt request active. 1 = Interrupt inactive.
P3.3	Input	P2INT1.L	0 = CHANGE interrupt request active. Becomes active each time the host writes to LPR or LNCTRL. 1 = Interrupt inactive.
P3.4	Input	FULL.L	0 = FIFO is full 1 = FIFO is not full
P3.5	Input	ALARM.L	0 = FIFO has reached three-quarters full condition and has not yet been emptied below half full. 1 = FIFO not in the above state.
P3.6	Output	P2WR.L	Common RAM write strobe
P3.7	Output	P2RD.L	Common RAM read strobe

4.7.2 Q-Bus Interrupts

(See Figure 4-17.) The function of the DC003 interrupt logic is to make interrupt requests and to supply a vector to the host. Signal sequences for interrupt request and acknowledge are given in Figure 4-4.

If interrupts are enabled, they are generated under the following conditions:

1. When a received character is loaded into a previously empty FIFO (EMPTY.L is asserted to indicate this state)

2. When, with data in the FIFO, RXIE is changed to the enable state

3. When, during a single-character programmed transfer, a character is removed from a TXCHAR register

4. When a DMA block transfer is completed, or has been aborted, or has failed because of a DMA error.

For conditions 3 and 4, the signal TX.ACTION.H is generated.

EMPTY.L, when it goes false, causes a receive interrupt request (RQA) and TX.ACTION.H causes a transmit interrupt request (RQB).

Interrupts are enabled by writing a 1 to CSR bit 6 and/or CSR bit 14. This action generates receive interrupt enable (RXIE) and transmit interrupt enable (TXIE) respectively. The host can read the status of these lines by a CSR read action.

The enable signals are ANDed with the appropriate request, and latched to generate RQA or RQB. If both are true, priority is given to RQA.

For both RX and TX interrupts, bus interrupt request (BIRQ.L) is generated. The request is cleared again by RDIN.L at the start of an interrupt acknowledge cycle.

NOTE

Both RX and TX interrupt requests are latched by a rising edge. Therefore in order to raise another interrupt request, one of the inputs to AND gates A or B must be deasserted and then asserted.

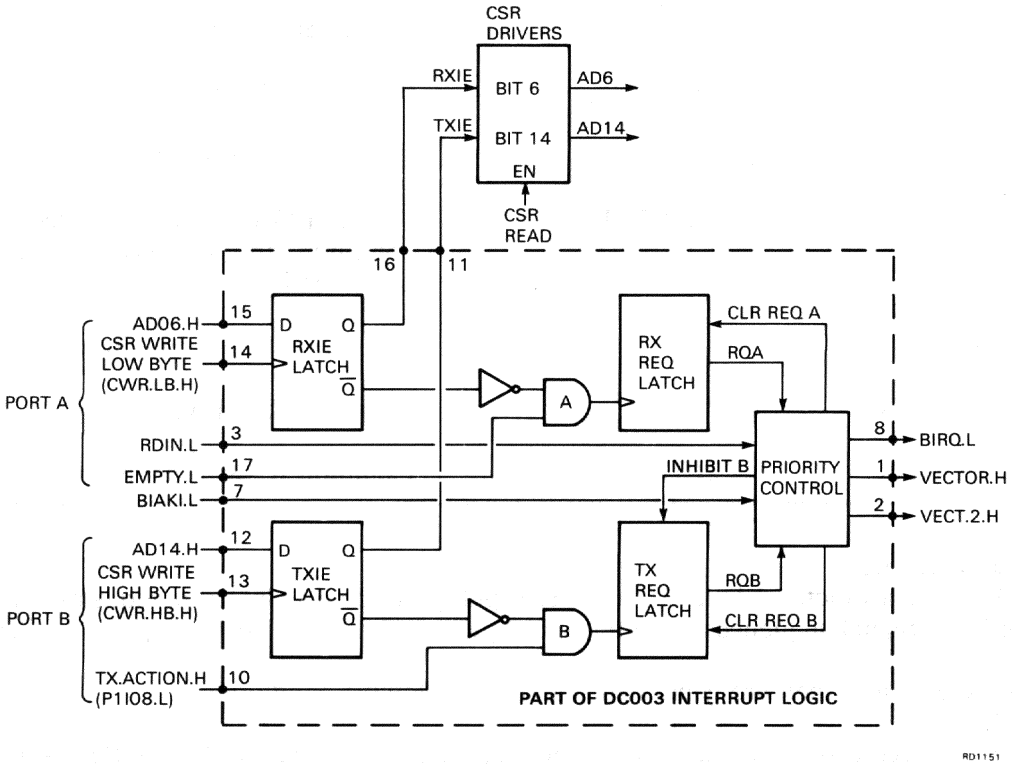


Figure 4-17 Interrupt Logic

In an interrupt acknowledge cycle, the DC003 interrupt IC responds to BIAKI.L. The signal VECTOR.H enables the vector switches onto BDAL<3:8>. VECT.2.H provides the low bit of the vector address on BDAL<2>. It identifies a receive (0) or transmit (1) interrupt vector. VECTOR.H also generates BRPLY via DC004 protocol logic. The vector is transferred to the host by a DATI sequence which follows the interrupt request/grant sequence.

4.7.3 Common RAM Arbitration

(See Figure 4-18.) To allow the common RAM to be accessed by the microcomputers and by the host, the DHV11 provides arbitration circuitry. However, arbitration introduces a delay into a memory access sequence. To account for this delay, the store access cycle of the requesting device must be extended.

Data addresses and control signals from the external bus are extended by delaying BRPLY.L. This signal is disabled until the store access is complete. The 8051 microcomputers, however, cannot be controlled in this way. They have no handshake signal such as WAIT, and because they are dynamic it is not possible to stop the clock.

The DHV11 solves the problem by slowing down the related microcomputer clock every time PROC1 or PROC2 tries to access the RAM. The normal clock frequency is 12 MHz. This is reduced to 1.5 MHz during RAM access. Approximately 330 nanoseconds after a store request has been granted, the normal clock frequency is enabled.

Figure 4-18 provides more information on the RAM arbitration and timing blocks. A description of the operation follows.

A 4-state scan counter (0 to 3) is driven by the 12 MHz clock. The output is used as a synchronized count for a request multiplexer and two accept decoders.

On each positive edge of the clock one of the latched store request lines (SRQDs) from PROC1, PROC2 or the bus is connected to the request latch. On each negative edge the input to the latch is sampled. A valid store request will set the latch. The scan counter will be stopped and the RAM state counter will be enabled.

With the scan counter stopped, the MUX and the decoders will also stop. One of the grant signals, ACP1, ACP2, or ACB (accept PROC1, PROC2, or BUS), will be true. The equivalent SCS (store chip select) signal will be selected but not enabled.

Now that the RAM state counter is enabled, it is incremented by the 12 MHz clock from 000 to 101. The counter is then held in the 101 state by END.L.

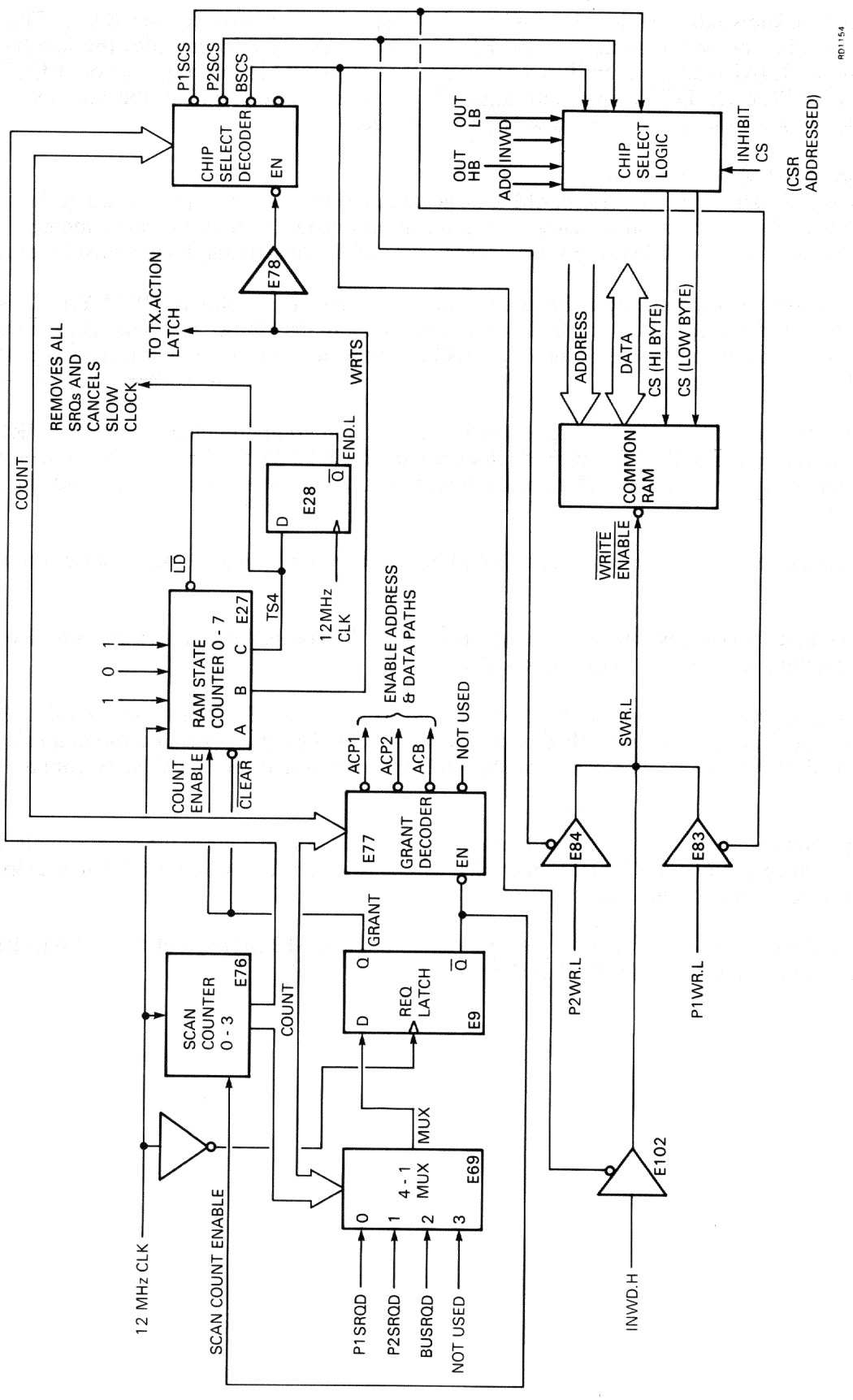


Figure 4-18 RAM Arbitration and Timing

Figure 4-19 gives timing details for a store access cycle.

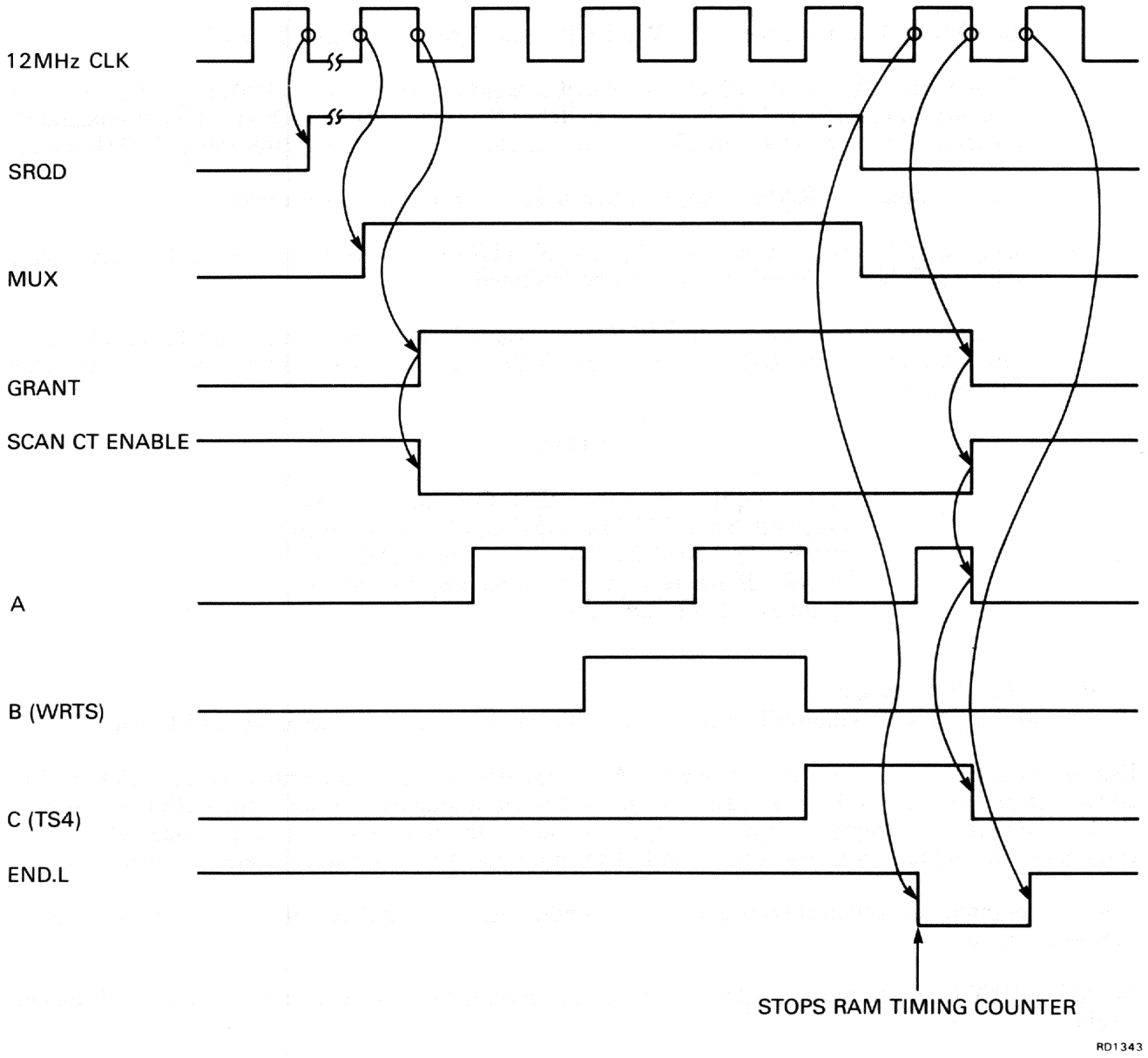


Figure 4-19 Store Access Timing Cycle

In Figure 4-19:

- Write Time State (WRTS) is inverted to enable the selected Store Chip Select (SCS) signal via the decoder. This action performs two functions:

  1. It enables the appropriate Chip Select (CS) signals via the chip select logic

  2. It enables the appropriate write enable line. SWR.L will be true when one of the gates E83, E84, or E102 is enabled and its input is low. That is to say, when PROC1, PROC2, or the host are writing to the RAM.

- SWR.L, and CS signals for the high and/or low byte, perform the RAM access. If SWR.L is false, a read action is performed.
- In a PROC1 write to the CSR, WRTS is used to set the TX.ACTION bit.
- Time State 4 (TS4) – If a PROC1 or PROC2 request is valid, the related microcomputer clock will be running slow at 1.5 MHz. TS4 switches the clock back to 12 MHz. TS4 also deasserts any active store request. SRQD will be deasserted on the next negative-going 12 MHz clock.
- END.L holds the RAM timing counter at 101 as previously described.
- Chip select logic uses AD0, OUTHB, and OUTLB to select a byte or word. If the CSR is being addressed, both chip select lines will be inhibited.
- At the end of the memory cycle, SRQD is deasserted. On the next negative 12 MHz clock, the request latch and the RAM state counter will be reset, and the arbitrator will continue to scan for requests.

NOTE

Store request signals (SRQDs) to E69 are supplied by a 74S374 octal latch (E70), part number 19-13671-51. This IC has special timing/ stability characteristics and must only be replaced by an IC of the same type.

4.7.4 FIFO Counter Control

(See Figure 4-1.) It is the action of FIFO counters which makes a section of common RAM act as a FIFO.

During initialization, the counters are cleared. As characters and status are written to the FIFO, the Fill counter steps ahead of the Empty counter which is still addressing the bottom of the FIFO. As the host reads each word the Empty counter is stepped to address the next word. The difference between the counters is the number of characters in the FIFO. Both counters will roll over after a count of 255.

Comparator circuits check the two counters. The conditions, empty, half full, three-quarters full, and full can be detected.

When EMPTY is deasserted, a hardware request is generated for receive interrupt service. This can be disabled by software.

FULL is a signal which stops PROC2 from putting more characters into the FIFO.

ALARM is asserted when the FIFO becomes three-quarters full. It stays asserted until the FIFO becomes less than half full. These signals are used when the DHV11 is programmed for auto-flow on incoming characters. X-OFF characters are generated when the FIFO is more than three-quarters full. X-ON characters are generated when it becomes less than half full.

To address the appropriate FIFO location, address bits SAD9 and SAD8 must be set to 0 and 1 respectively and the appropriate address counter must be enabled. The correct SAD<9:8> code is generated for any FIFO access, that is to say:

1. When the FIFO (READ from base + 2) is addressed and ACB (Figure 4-18) is asserted

2. When PROC2 generates a FIFO WRITE signal (FIWR.L) and ACP2 (Figure 4-18) is asserted.

4.7.4.1 Host Read from the FIFO – During a host READ from the FIFO the contents of the Empty counter are latched onto SAD<7:0> by a decode of:

1. INWD from the DC004 protocol IC
2. The RBUF address (base + 2)
3. ACB from the RAM arbitrator.

By the same signals, a strobe is generated to increment the counter ready for the next action. If the FIFO is empty (EMPTY.L asserted), the strobe is inhibited.

Chip select logic decodes BSCS and INWD to generate CS signals for both bytes of the addressed word.

4.7.4.2 PROC2 Write to the FIFO – When PROC2 writes to the FIFO (FIWR.L asserted), the contents of the Fill counter are latched onto SAD<7:0> by an AND of:

1. FIWR.L from PROC2 (see Table 4-3)
2. PROC2 accept signal (ACP2).

By the same signals, a strobe is generated to increment the counter ready for the next action. However, because PROC2 can only write bytes, the strobe is only enabled when the low byte is written. For this reason the low byte is always written last.

The high or low byte is selected by AD0 from PROC2 (see Table 4-3). Chip select logic decodes the state of AD0 in order to generate the correct CS signal. The AD0 = 0 state is used to enable the strobe which increments the Fill counter.

4.7.5 Control/Status Register (CSR)

This is the main control register of the module. PROC1 updates the high byte as necessary. The host can poll the CSR to find the DHV11 status.

Associated with the CSR (see Figure 4-20) are the following:

- Indirect Address Register – a 4-bit latch (AD0 to AD3) which holds the number of the channel which is to be accessed. The contents of this register are used to index the addresses supplied by the host. Figure 4-20 shows how indexing is performed.

NOTE

The indirect address register holds the channel number. Therefore, to configure a channel, the register has only to be loaded once. The control registers for that channel can then be loaded in sequence. Only when the host needs to access another channel must the indirect address register be reloaded.

- Master Reset Latch – set by BINIT or by writing a 1 to bit 5 of the CSR. Cleared by P1IO14.L from PROC1.

  P1IO14.L and MRST.L are ORed at E29 to make sure that MRST does not go false until the end of P1IO14.L strobe.

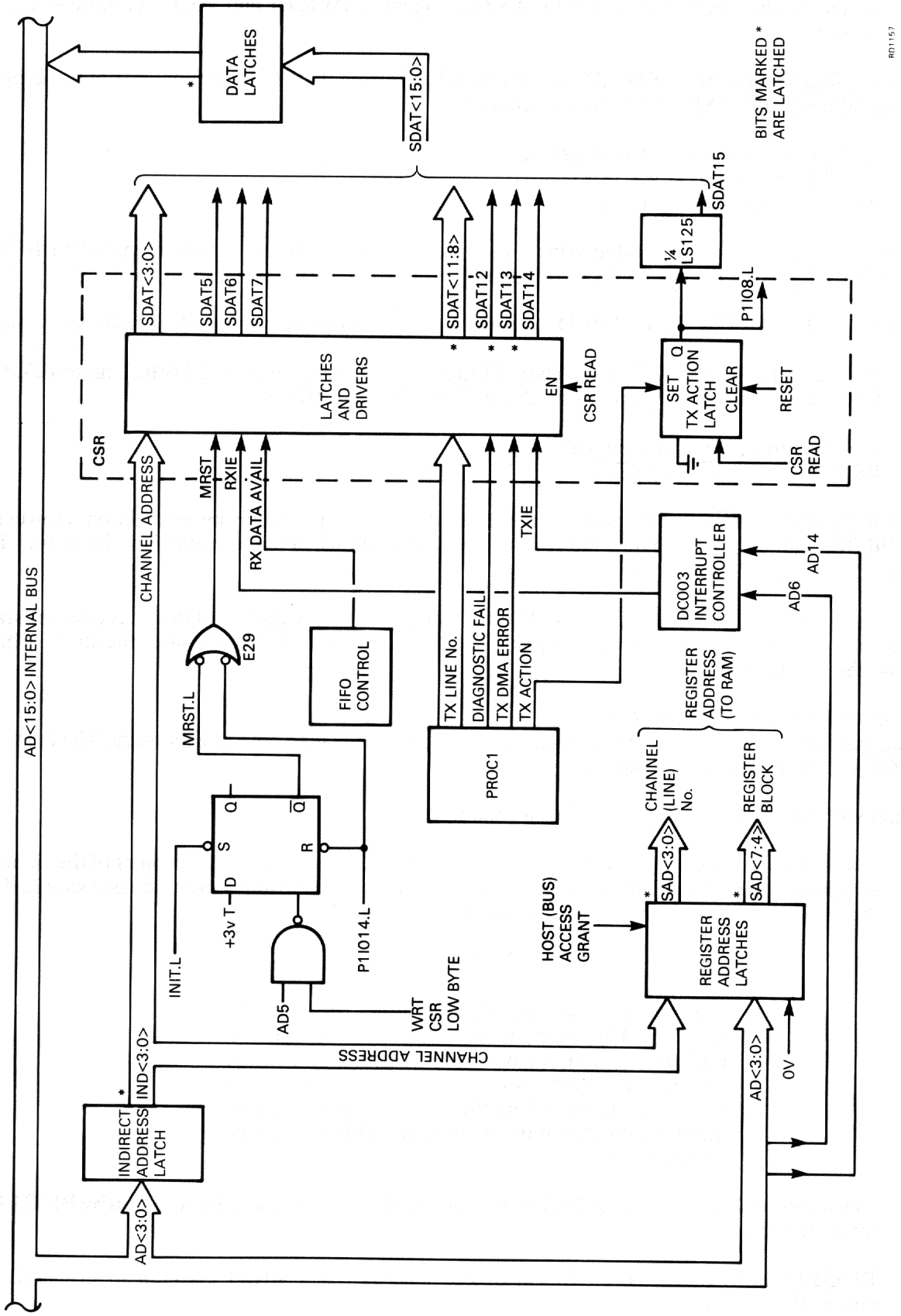


Figure 4-20 CSR and Register Address Circuits

- DC003 interrupt controller – provides interrupt enable status to the CSR. If bit 6 is set, receive interrupt is enabled. If bit 14 is set, transmit interrupt is enabled.

- FIFO Control – indicates that there is valid data in the FIFO.

- TX ACTION Latch – indicates when a transmit action has been completed. It is cleared when the CSR is read.

- PROC1 – provides the following information:

  On SDAT<11:8> – The related transmit channel number
  On SDAT12 – Diagnostic fail bit
  On SDAT13 – TX.DMA.ERROR bit
  On SDAT15 – TX.ACTION bit.

4.7.6 Voltage Converter (SMPS)

The DHV11's line drivers and receivers need both +12 V and –12 V supplies. The +12 V is supplied from the backplane, but –12 V is derived from +12 V by a voltage converter. This device uses switch-mode power supply techniques to generate the negative voltage.

The circuit is built around a TL494 switching regulator which uses pulse-width modulation to regulate the –12 V output. Maximum current is approximately 400 mA.

Switch-mode power supplies of the type used by DHV11 operate according to the following principles (refer to the simplified circuit diagram of Figure 4-21).

Switching pulses from a pulse width modulator/regulator switch a transistor (Q1) to convert a dc input (V IN) to a pulsed dc current in an inductor (L).

When Q1 is switched on, point X becomes positive causing current to flow through L. This generates a magnetic field around L.

When Q1 is switched off, the current stops and the field collapses. This drives point X negative, and puts a forward bias on diode D. Current generated by the collapsing field is transferred via the forward-biased diode to the smoothing capacitors. In this way a negative voltage (V OUT) is generated.

As current is transferred to the output, the voltage at X rises until the diode is cut off again. The circuit will stay in this state until the next switching pulse opens Q1.

The inset of Figure 4-21 shows waveforms of the current through L, as seen by an oscilloscope across R14. When Q1 is switched on, current rises linearly until Q1 is switched off again. The collapsing field generates current, which reduces linearly as it is transferred to the output. With wider switching pulses, more current is transferred to the output. Therefore, the power transferred (shaded in the inset) is proportional to the width of switching pulses.

Feedback (VAR) from V OUT to the pulse width modulator is compared with a reference voltage (REF). If VAR is too negative (V OUT is too high), the width of switching pulses is reduced. If VAR is too positive, the width is increased. This action maintains V OUT at the correct level.

The same method of comparison is used to detect an over-current condition. When the voltage (proportional to output current) across R14 gets too high, the switching pulse width is reduced. This reduces the current.

The switching frequency, selected by R12 and C9, does not change. In DHV11 this frequency is 33.3 kHz. If the oscillator is working, a sawtoothed 33.3 kHz waveform can be detected on pin 5 or 6.

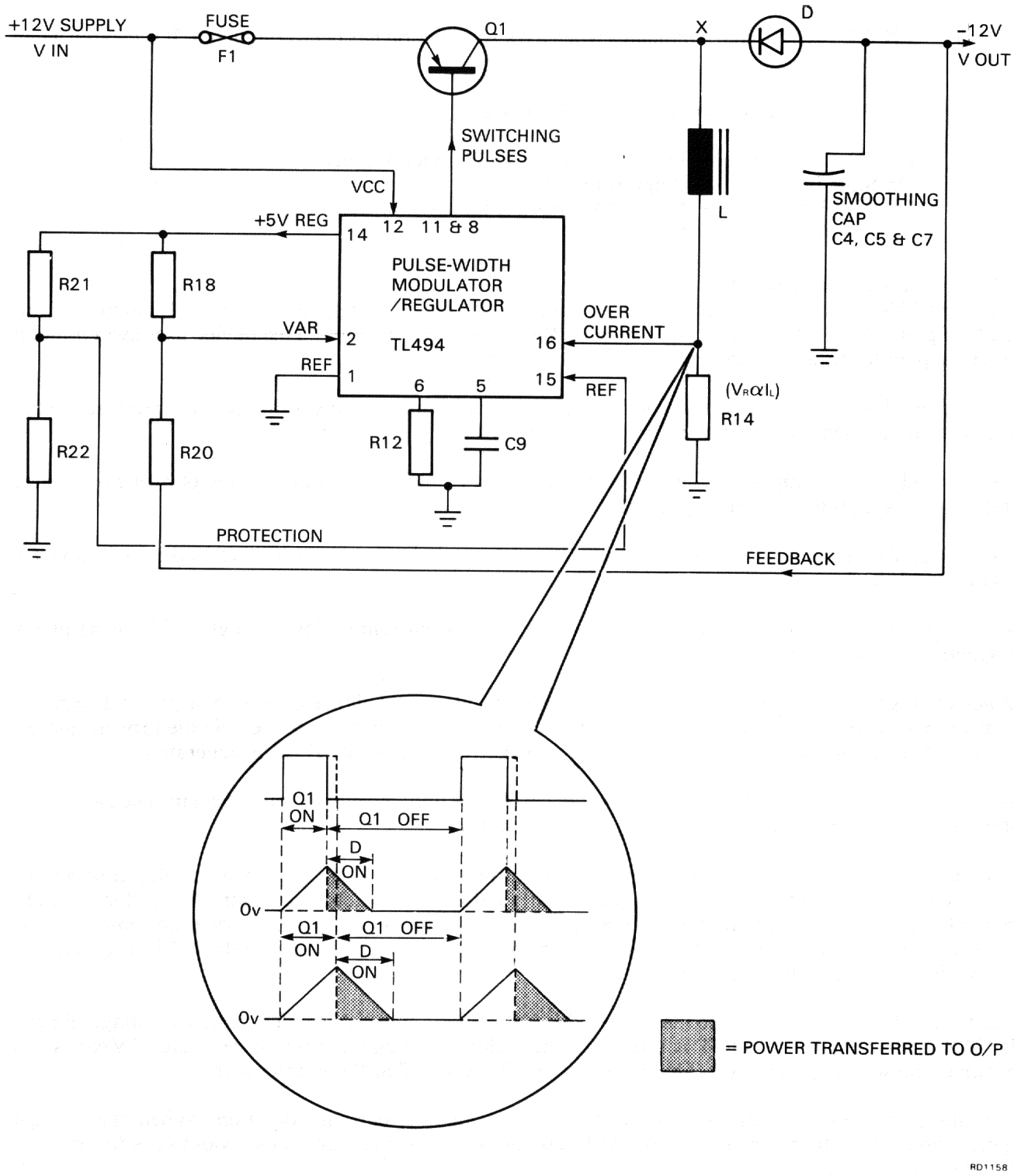


Figure 4-21 DHV11 Voltage Converter

4.8 ROM-BASED DIAGNOSTICS

4.8.1 Self-Test

4.8.1.1 General – When DHV11 or the Q-bus is reset, the DHV11's master reset latch is set. This causes the microcomputers to execute a DHV11 self-test sequence.

During self-test, diagnostic codes are stored in the top six words of the common RAM, and also in the top two bytes of PROC2's internal RAM.

At the end of self-test, control is passed to the communications firmware, which starts the initialization routine. During initialization the diagnostic codes are transferred to the FIFO.

At the end of the initialization process, the master reset latch is reset, thereby clearing CSR bit 5 (MRST). This bit is polled by the host. When MRST is cleared the host can read and interpret the diagnostic codes.

The 'diagnostic fail' bit in the CSR indicates whether the diagnostic program detected an error condition. The green 'diagnostic passed' LED is on when the bit is cleared and vice-versa.

When a serviceable DHV11 is reset, the LED follows this sequence:

1. Off for about 0.03 seconds
2. On for about 0.2 seconds
3. Off for 1 to 2.5 seconds
4. On permanently.

If the LED does not follow this sequence, the DHV11 is defective.

4.8.1.2 Location and Interpretation of Diagnostic Codes – Figure 4.22 shows where diagnostic information is loaded immediately after self-test. DIAG 0 to DIAG 7 are the diagnostic bytes stored during self-test. Diag 0 to Diag 7 are the same bytes which are transferred during initialization.

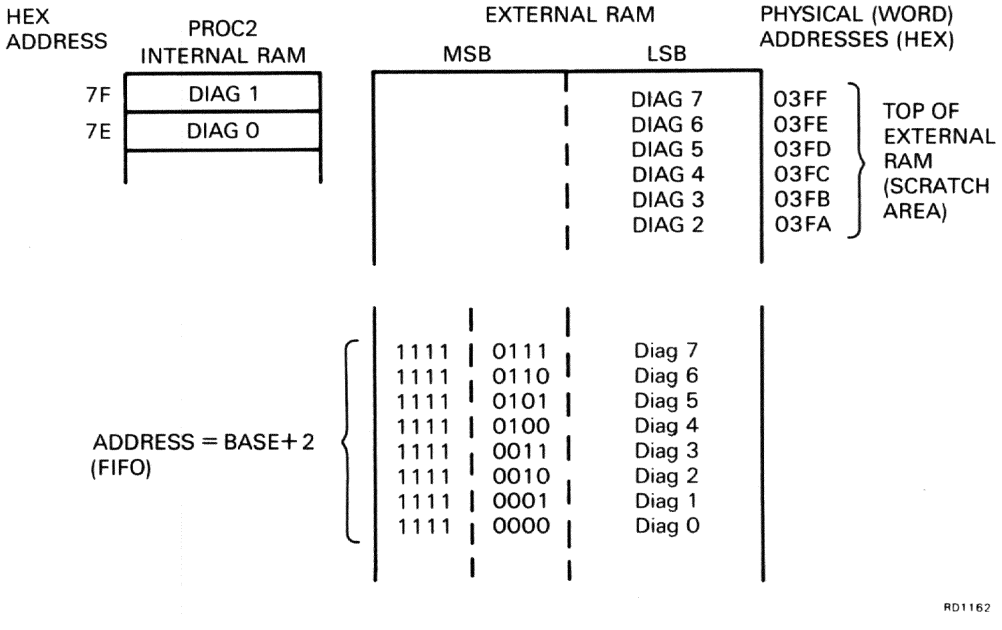


Figure 4-22 Register Contents After Self-Test

The high byte of RBUF can be interpreted as in Chapter 3, Section 3.2.2.2, except that bits 11 to 8 are not the line number. They indicate the sequence of the diagnostic byte. That is to say, 0 = first diagnostic byte, 1 = second diagnostic byte, and so on.

Chapter 3, Programming, explains how to interpret diagnostic codes.

4.8.2 Background Monitor Program (BMP)

Many of the regular operations by PROC1 and PROC2 are controlled by internal timers. The timers generate internal interrupts which vector the microcomputers to the appropriate routine.

When they are not busy with other tasks, PROC1 and PROC2 check their timer-generated interrupts. If there is an error, a NOGO report is passed to the host via the FIFO.

BMP can also be activated by command from the host. In this case a GO/NOGO report is passed to the host.

Any time the BMP finds an error, DIAG.FAIL is set in the CSR and the diagnostic LED is switched off. The LED will stay off, even if the fault clears.

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This chapter explains the maintenance strategy and how the diagnostic programs are used to find a defective Field Replaceable Unit (FRU). The description is supplemented by a troubleshooting flowchart.

5.2 MAINTENANCE STRATEGY

5.2.1 Preventive Maintenance

No preventive maintenance is planned for this option. However, if the host system is being serviced, a visual check should be made for loose connectors and damaged cables.

5.2.2 Corrective Maintenance

The M3104 module, BC05L-xx cables, and H3173-A distribution panels are all FRUs. Corrective maintenance is therefore based on finding and replacing the defective FRU. However, if the fault is not in the option, it may be possible to perform tests of external equipment. Figure 5-1 can be used as a basis for troubleshooting.

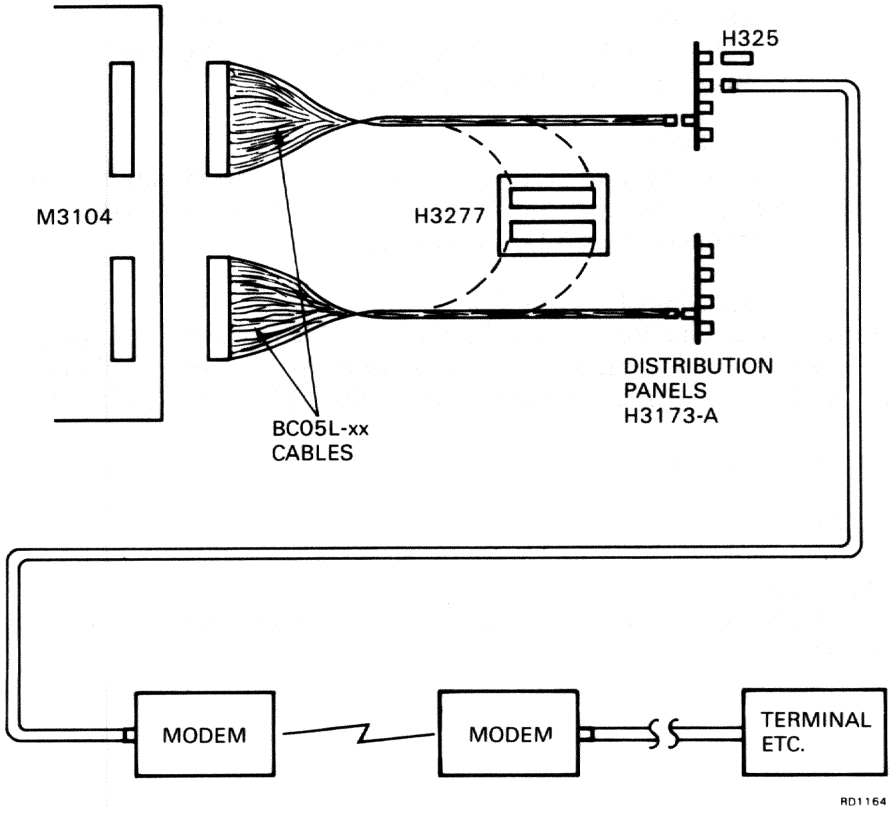


Figure 5-1 Troubleshooting Connection Diagram

5.3 INTERNAL DIAGNOSTICS

Internal diagnostics run without intervention from the operator. There are two tests, called self-test and background monitor test.

5.3.1 Self-Test

This test starts immediately after bus or device reset. It is a limited test, which checks the internally accessible parts of the DHV11 and gives a GO/NOGO indication via the DIAG.FAIL bit and the 'diagnostics passed' LED. Self-test also reports error or status information to the host via the FIFO. This information is used by system-based diagnostics such as CVDH??.

During a successful (no defects) self-test, the LED flashes OFF/ON/OFF before coming ON permanently. The first OFF period is very short and may not be seen. However, if the LED goes off and then comes on permanently, the diagnostic has found no faults. If self-test is skipped (see Chapter 3, Section 3.3.10.3), the LED will just go on.

Because of the limitations of self-test, a correct sequence does not guarantee that all sections of the module are good.

5.3.2 Background Monitor Program (BMP)

The BMP carries out tests on the DHV11 when the option is not engaged in other tasks. If it detects an error, the BMP reports to the host via the FIFO. It also switches off the 'diagnostics passed' LED.

By writing codes to the LPR, the host can cause the BMP to report the DHV11 status even if an error has not been detected. It is used if the host suspects that the DHV11 is dead.

NOTE

More detail of the self-test and BMP diagnostics is given in the technical description and programming sections of this manual.

5.4. XXDP+ DIAGNOSTICS

In order to run these diagnostics, the host system must have at least the minimum configuration specified. Loopback connectors will be needed for some of the tests. For more information, refer to the program documentation at the beginning of the CVDH?? listings.

5.4.1 CVDHA?, CVDHB?, and CVDHC?

These programs form a Functional Verification Test (FVT) which runs on Q-bus members of the PDP-11 processor family. This test runs under the PDP-11 Diagnostic Supervisor. It will run standalone using the XXDP+ monitor, or it can be run automatically under the Automatic Product Test (APT) system.

The minimum system requirements are:

- Q-bus CPU
- 32K bytes memory
- Console terminal
- XXDP+ load device with Diagnostic Runtime Services (DRS) supervisor
- DHV11 option.

In order to test the full DMA address capability of the DHV11, the diagnostic uses the following address patterns. If the high address lines are to be tested, the host must have memory at the following locations as well as the 32K bytes defined in the previous paragraph:

Address bits	21	20	19	18	17	16	15	14	13	–	–
Memory address (High bank)	1	0	1	0	1	0	1	X	X	X	X
Memory address (Low bank)	0	1	0	1	0	1	0	X	X	X	X

If memory is not available at these locations, some high DMA address bits will not be tested. This will not be considered as an error. The operator, by answering a prompt, can display information specifying the bits which were tested.

5.4.1.1 Functions of CVDHA? – This program checks the reset and the register access functions, and verifies that the handshake between the DHV11 and the host is operating correctly. It also checks reports from the self-test and BMP.

Loopback connectors are not used in this test.

5.4.1.2 Functions of CVDHB? – This program checks the major communication functions of the DHV11. It verifies the correct operation of modem control signals and the register bits which control and report them. CVDHB? does not perform extensive data transmission and reception tests.

Loopback connectors can be used in this test.

5.4.1.3 Functions of CVDHC? – This program checks the major communication functions which use the DUARTs. It checks split-speed operation, and verifies that DUART errors are reported correctly. Extensive data transfer tests are performed in both DMA and single-character modes.

Loopback connectors can be used in this test.

5.4.2 DECX/11 Exerciser

When a DHV11 or other option is installed or replaced, it is necessary to run the DECX/11 exerciser CXDHVxx. The exerciser must first be configured to match the host system. For more information, refer to the DECX/11 User Manual (AC-FO35B-MC) and DECX/11 Cross-Reference (AC-FO55C-MC).

DECX/11 should not be run until all modules have passed their own diagnostic tests. Therefore, before running the exerciser, the DHV11 must pass all phases of CVDH??.

5.5 DIAGNOSTIC SUPERVISOR SUMMARY

The CVDH?? diagnostics have been written for use with the Diagnostic Runtime Services (DRS) supervisor. DRS, which provides the interface between the operator and the diagnostic programs, can be used with load systems such as ACT, APT, SLIDE, XXDP+, and ABS loader. By answering prompt questions supplied by the supervisor the operator can define the following:

1. The hardware configuration of the DHV11s being tested
2. The type of test information to be reported
3. The conditions under which the test should be terminated or continued.

5.5.1 Loading the Supervisor Diagnostic

The diagnostic program may be loaded and started in the normal way, using any of the supported load systems. For example, using XXDP+, the program CVDHBA.BIN is loaded and started by typing R CVDHBA.

The diagnostic and the supervisor will be loaded and the program started. The program types the following message:

```
RS LOADED
DIAG.RUN-TIME SERVICES
CVDHB-A-0
DHV11 FUNCTIONAL VERIFICATION TEST
UNIT IS DHV11
RESTART ADDRESS xxxxxx
DR>
```

DR> is the prompt for the diagnostic supervisor routine. At this point a supervisor command must be entered (supervisor commands are listed in Section 5.5.3).

A0 on the end of CVDHB indicates the revision level (A) and the patch level (0).

5.5.2 Four Steps to Run a Supervisor Diagnostic

1. Enter the start command.

   When the prompt DR> is issued, type:

   ```
   STA/PASS:1/FLAGS:HOE<CR>
   ```

   The switches and flags are optional.

2. Answer the hardware parameter questions.

   The program prompts with:

   ```
   CHANGE HW?
   ```

   You must answer Y to this query if you want to change the hardware parameter tables. The program will then ask a number of hardware parameter questions in sequence. For example, the first question is:

   ```
   # UNITS?
   ```

   At this point, enter the number of units to be tested.

NOTE

Some versions of the diagnostic supervisor do not ask the CHANGE HW? question at the first start command. Instead they go straight into the hardware parameter question sequence.

The answers to the questions are used to build hardware parameter tables (P-tables) in memory. A series of questions is posed for each device to be tested. A hardware P-table is built for each device.

3. Answer the software parameter questions.

   When all the hardware P-tables are built the program responds with:

   CHANGE SW?

   If other than default parameters are wanted for the software, type Y. If the default parameters are wanted, type N.

   If you type Y, a series of software questions will be asked and the answers to these will be entered into the software P-table in memory. The software questions will be asked only once, regardless of the number of units to be tested.

4. Diagnostic execution

   After the software questions have been answered, the diagnostic starts to run.

   What happens next is determined by the switch options selected with the start command, or errors occurring during execution of the diagnostic.

5.5.3 Supervisor Commands

The supervisor commands that may be issued in response to the DR> prompt are as follows:

- START — Starts a diagnostic program
- RESTART — When a diagnostic has stopped and control is given back to the supervisor, this command restarts the program from the beginning
- CONTINUE — Allows a diagnostic to continue running from where it was stopped
- PROCEED — Causes the diagnostic to resume with the next test after the one in which it halted
- EXIT — Transfers control to the XXDP+ monitor
- DROP — Drops units specified until an ADD or START command is given
- ADD — Adds units specified. These units must have previously been dropped
- PRINT — Prints out statistics if available
- DISPLAY — Displays P-Tables
- FLAGS — Used to change flags
- ZFLAGS — Clears flags.

All of the supervisor commands except EXIT, PRINT, FLAGS, and ZFLAGS can be used with switch options.

5.5.3.1 Command Switches

Switch options may be used with most supervisor commands. The available switches and their functions are as follows:

- /TESTS: Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the start command to run tests 1 to 5, 19, and 34 to 38 would be:

  DR> START/TESTS:1-5:19:34-38<CR>

- /PASS: Used to specify the number of passes for the diagnostic to run. For example:

  DR> START/PASS:1<CR>

  In this example, the diagnostic would complete one pass and give control back to the supervisor.

- /EOP: Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one).

- /UNITS: Used to specify the units to be run. This switch is valid only if N was entered in response to the CHANGE HW? question.

- /FLAGS: Used to check for conditions and modify program execution accordingly. The conditions checked for are as follows:

:HOE	Halt on error (transfers control back to the supervisor)
:LOE	Loop on error
:IER	Inhibit error reports
:IBE	Inhibit basic error information
:IXE	Inhibit extended error information
:PRI	Print errors on line printer
:PNT	Print the number of the test being executed before execution
:BOE	Ring bell on error
:UAM	Run in unattended mode, bypass manual intervention tests
:ISR	Inhibit statistical reports
:IOU	Inhibit dropping of units by program.

5.5.4 Control/Escape Characters Supported

The keyboard functions supported by the diagnostic supervisor are as follows:

- CTRL/C (^C) Returns control to the supervisor. The DR> prompt would be typed in response to CTRL/C. This function can be typed at any time.

- CTRL/Z (^Z) Used during hardware or software dialogue to terminate the dialogue and select default values.

- CTRL/O (^O) Disables all printouts. This is valid only during a printout.

- CTRL/S (^S) Used during a printout to temporarily freeze the printout.

- CTRL/Q (^Q) Resumes a printout after a CTRL/S.

5.5.5 Example Printouts

Two examples of diagnostic printouts follow. The first is error-free. In the second test, the device address is incorrect.

Entries by the operator are underlined. An underline without an entry shows that the operator has pressed the RETURN key to select the default parameter.

1. Error-free pass

```
R CVDHBA
CVDHBA.BIN

DRSC7
CVDHB-A-0
DHV-11 FUNCT TEST PART2
UNIT 1 IS DHV-11
RESTART ADDR: 147670

DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1

UNIT 0

CSR ADDRESS: (0) 160460 ? 160500
INTERRUPT VECTOR ADDRESS: (0) 300 ?_
ACTIVE LINE BIT MAP: (0) 377?_

TYPE OF LOOPBACK (1=INTERNAL, 2=STAGGERED,
                  3=25 PIN CONNECTOR, 4=MODEM): (0) 2 ?_

INTERRUPT BR LEVEL: (0) 4 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
NUMBER OF INDIVIDUAL DATA ERROR TO REPORT ON A LINE:  (D) 0 ?_

CVDHB EOP 1
    0 CUMULATIVE ERRORS

DR>EXIT
```

2. Test with wrong device address selected

```
R CVDHBA
CVDHBA.BIN
DRSC7
CVDHB-A-0
DHV-11 FUNCT TEST PART2
UNIT IS DHV-11
RESTART ADDR: 147670
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1

UNIT 0
CSR ADDRESS: (0) 160460 ? 160500
INTERRUPT VECTOR ADDRESS: (0) 377 ?_
ACTIVE LINE BIT MAP: (0) 377 ?_
TYPE OF LOOPBACK (1=INTERNAL, S=STAGGERED,
                  3=25PIN CONNECTOR, 4=MODEM): (0) 2 ?_
INTERRUPT BR LEVEL: (0) 4 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE (D) 0 ?_

CVDHB DVC FTL ERROR 00101 ON UNIT 00 TST 001 SUB 000 PC: 021354

DEVICE REGISTER ACCESS ERRORS
BUS TIME-OUT TRAP CAUSED BY READ ATTEMPT
BUS TIME-OUT TRAP CAUSED BY WRITE ATTEMPT
DHV MAY BE AT THE WRONG Q-BUS ADDRESS.

 UNIT     0 DROPPED FROM FURTHER TESTING

PASS ABORTED FOR THIS UNIT
CVDHB EOP  1
    1 CUMULATIVE ERRORS

DR>
```

5.6 FIELD REPLACEABLE UNITS (FRUs)

The FRUs are:

Reference No.	Item
M3104	Quad-height module
BC05L-xx	Flat cable, 40 conductor
H3173-A	Distribution panel
H3277	Staggered loopback test connector
H325	Line loopback test connector

The last two items do not affect the operation of the system.

Depending on local maintenance strategy, modems and/or external cables may also be FRUs. See Figure 5-1.

5.7 TROUBLESHOOTING FLOWCHART

When troubleshooting is necessary, the flowchart sequence of Figure 5-2 should be used as a guide.

The flowchart is based on the CVDH?? diagnostics. Note that CVDHA? has no loopback mode.

5.8 COMPONENT REPLACEMENT

The M3104 module is a multilayer fine-line-etch PCB. Only the microcomputers, which are on sockets, can be replaced in the field. This should only happen if the firmware is updated.

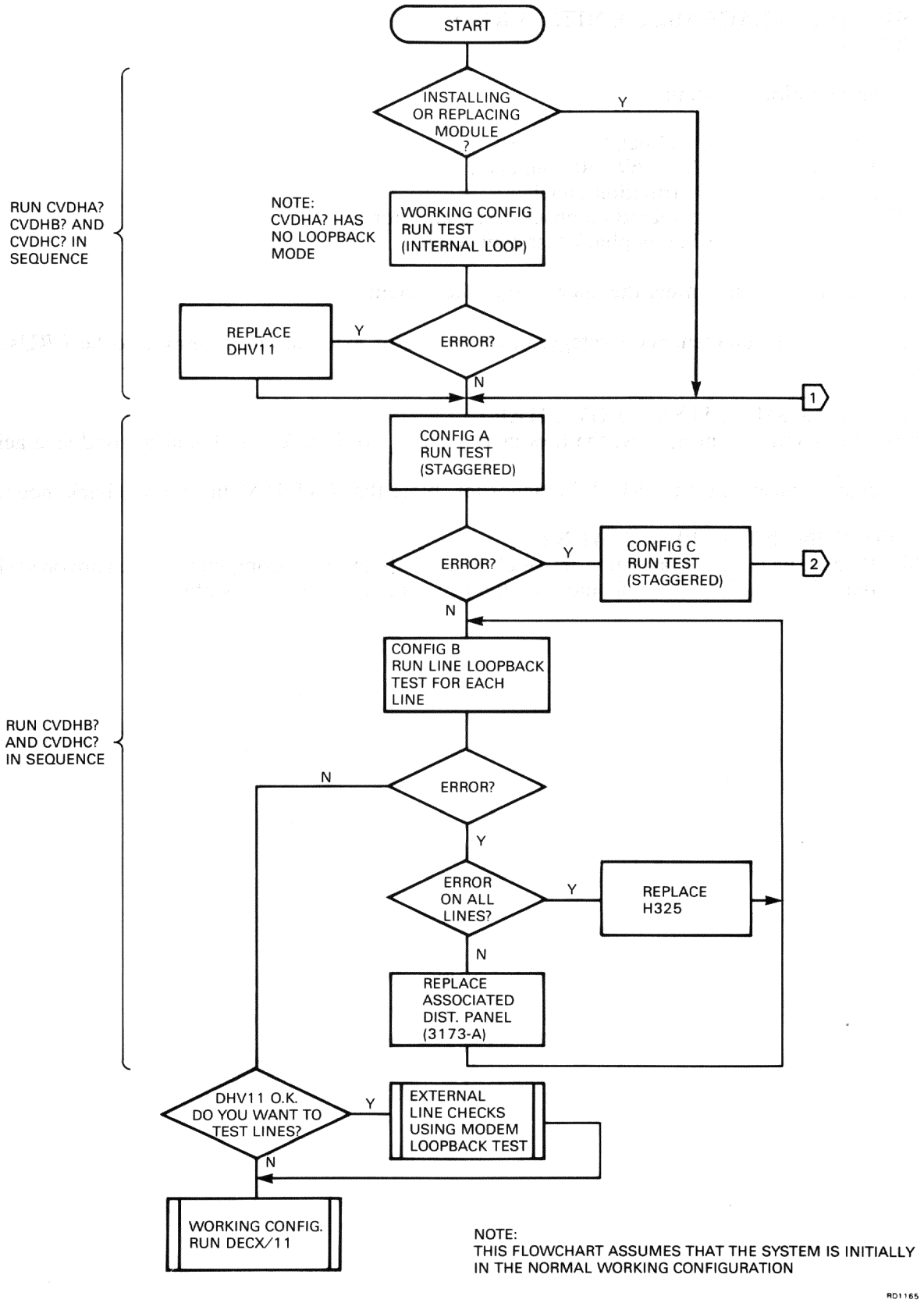


Figure 5-2 Troubleshooting Flowchart

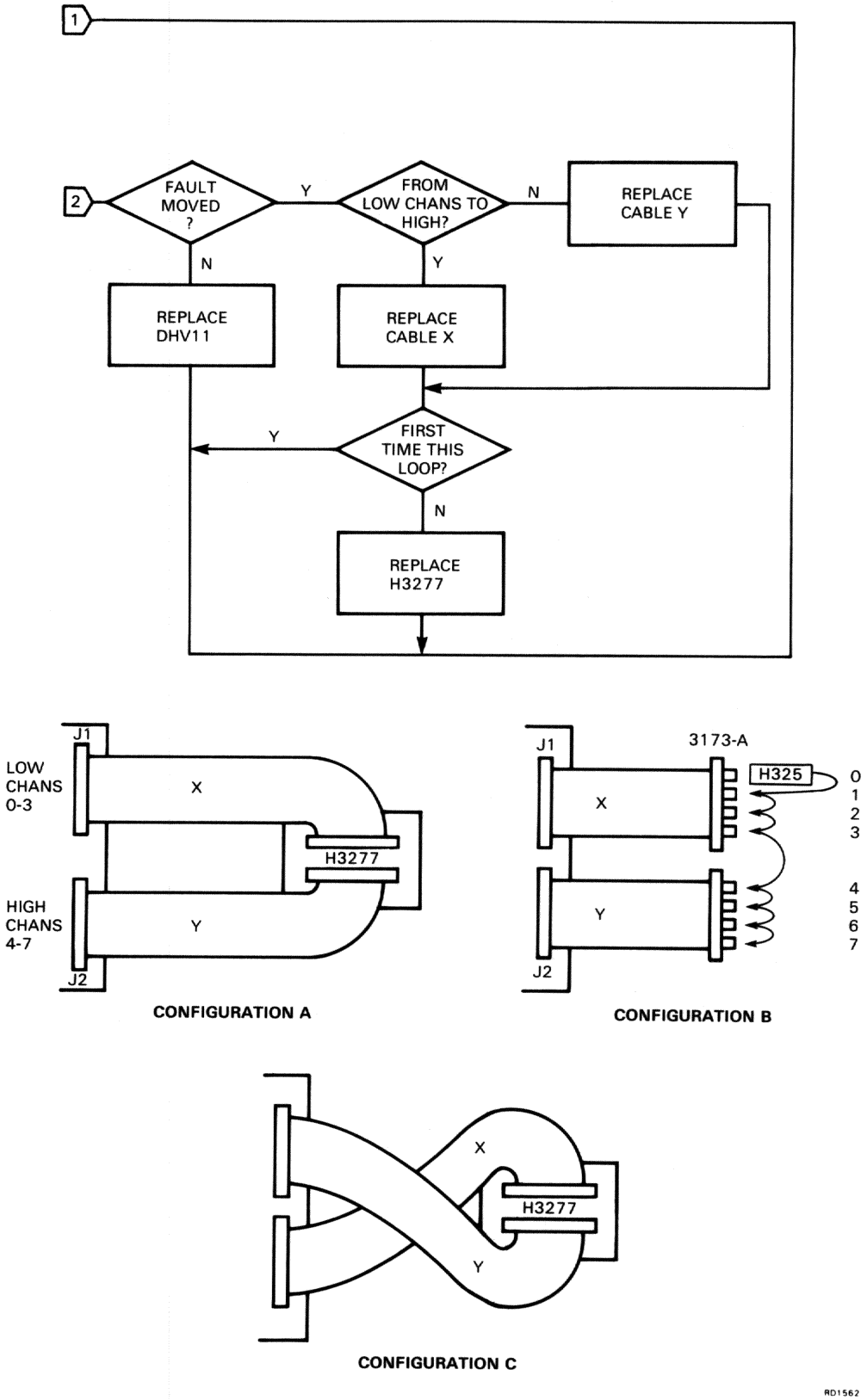


Figure 5-2 Troubleshooting Flowchart (Cont)

APPENDIX A
IC DESCRIPTIONS

A.1 SCOPE

This appendix contains data on the 8051 microcomputers and other LSI chips used in the DHV11. The smaller common ICs, which are well described in standard reference books, are not included. For information not included in this document, read the appropriate manufacturer's data sheets.

A.2 8051 MICROPROCESSOR/MICROCOMPUTER

A.2.1 8051 Block Description

The 8051 is a microcomputer based on the Intel 8048. Its configuration is programmable. The block diagram is shown in Figure A-1.

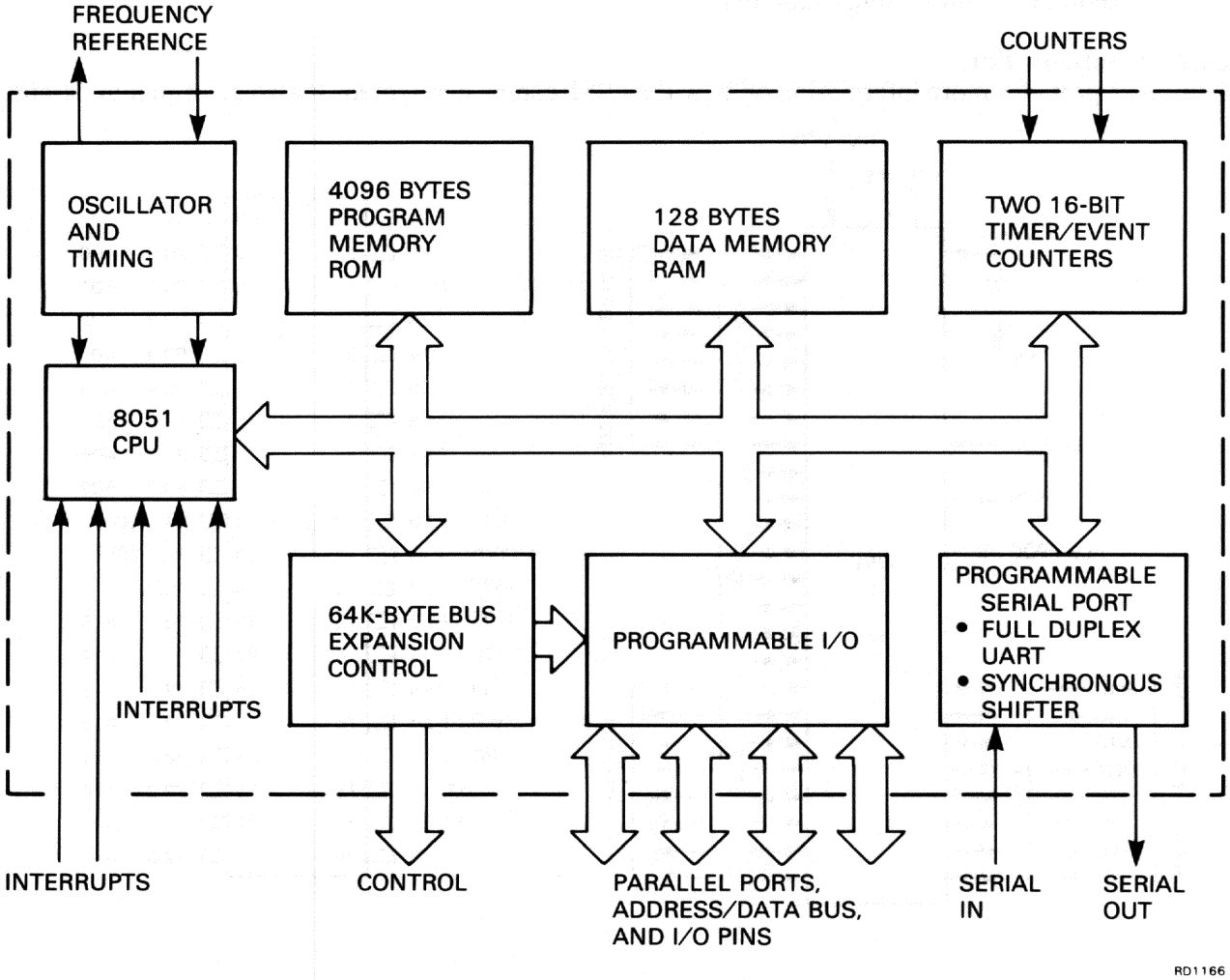


Figure A-1 8051 Block Diagram

As well as having 128 bytes of RAM for register space, stack, and data memory, the IC contains:

- 4K bytes of program memory ROM
- Two 16-bit programmable timer/counters
- A full-duplex programmable serial UART capable of data rates up to 31250 bits/s
- 32 programmable I/O lines arranged as four 8-bit ports.

Other features not indicated in the diagram are:

- Single +5 V supply
- 64K bytes program memory and 64K bytes data memory addressing capability
- Up to 128 bytes stack
- Four 8-byte register banks
- Two-level interrupt system with programmable priority. Interrupts may also be triggered by the counter/timers.
- Byte or bit addressing capability.

A.2.2 Configuration

Figure A-2 provides more information on how the 8051 can be configured. It also gives pinout details.

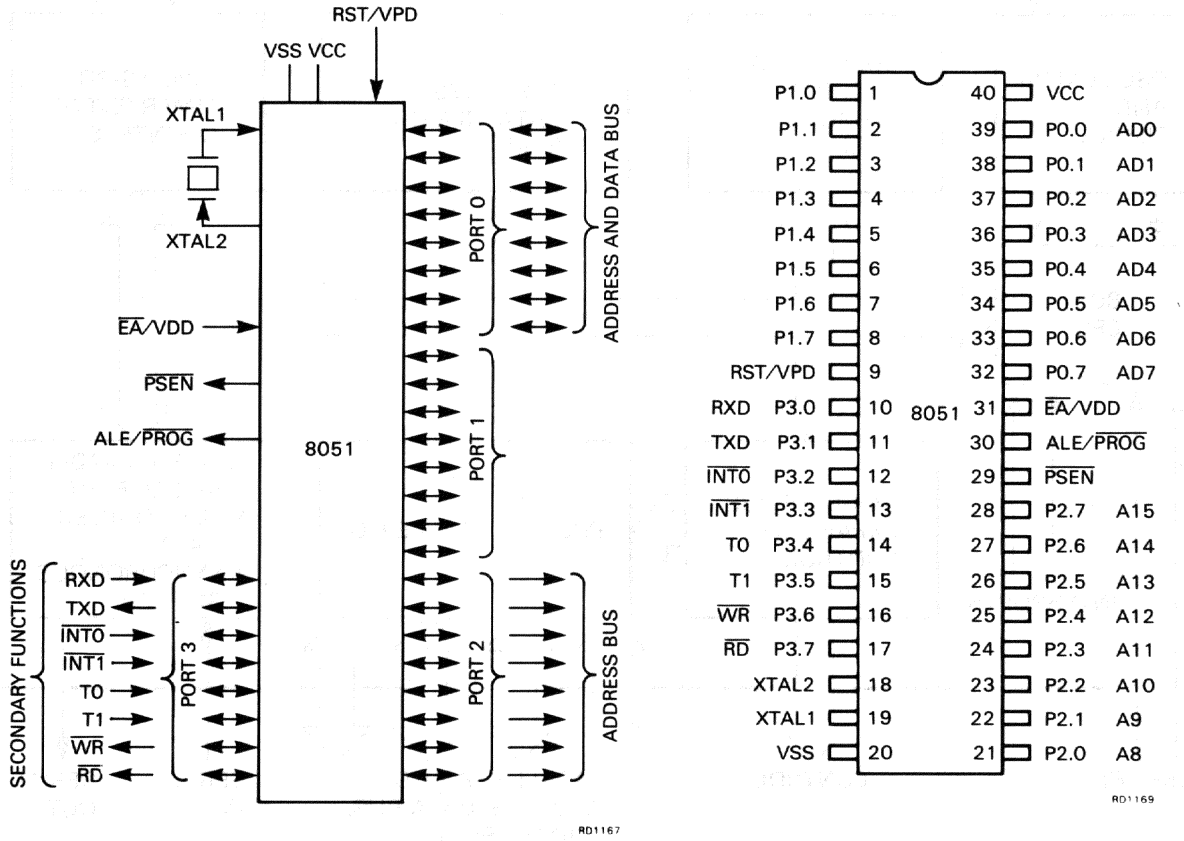


Figure A-2 8051 Symbol and Pinout Diagrams

When external memory is addressed, port 0 becomes a multiplexed 8-bit data bus / low-order (A7 to A0) address bus. If the external address is higher than 255, port 2 provides A15 to A8. When not being used in combination with port 0, port 2 returns to its programmed condition.

The 8051 signals are briefly described in Table A-1.

Table A-1 8051 Pin Description

Vss
Circuit ground potential.

Vcc
+5 V power supply during operation, programming, and verification.

PORT
Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data input and output during programming and verification. Port 0 can sink/source eight LSTTL loads.

PORT 1
Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during programming and verification. Port 1 can sink/source four LSTTL loads.

PORT 2
Port 2 is an 8-bit quasi-bidirectional I/O port. It also issues the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during programming and verification. Port 2 can sink/source four LSTTL loads.

PORT 3
Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port, and RD and WR pins that are used by a number of options. The output latch corresponding to a secondary function must be programmed to a 1 for that function to operate. Port 3 can sink/source four LSTTL loads. The secondary functions are assigned to the pins of port 3, as follows:

- RXD/data (P3.0). Serial port receiver data input (asynchronous) or data input/output (synchronous)
- TXD/clock (P3.1). Serial port transmitter data output (asynchronous) or clock output (synchronous)
- INT0 (P3.2). Interrupt 0 input or gate control input for counter 0
- INT1 (P3.3). Interrupt 1 input or gate control input for counter 1
- T0 (P3.4). Input to counter 0
- T1 (P3.5). Input to counter 1
- WR (P3.6). The write control signal latches the data byte from port 0 into the external data memory
- RD (P3.7). The read control signal enables external data memory to port 0.

Table A-1 8051 Pin Description (Cont)

RST/VPD
A change of level from low to high on this pin (at approximately 3 V) resets the 8051. If VPD is held within its specification (approximately +5 V) while Vcc drops below specification, VPD will provide standby power to the RAM. When VPD is low, the RAM's current flows from Vcc. A small internal resistor permits power-on reset using only a capacitor connected to Vcc.

PSEN L
The Program Store Enable output is a control signal that enables the external program memory to the bus during normal fetch operations. Not connected on DHV11.

EA L/VDD
When held at a TTL high level, the 8051 executes instructions from the internal ROM/EPROM when the PC is less than 4096. When held at a TTL low level, the 8051 fetches all instructions from external program memory. The pin also receives the 21 V EPROM programming supply voltage. Connected to a high TTL level on the DHV11.

XTAL1
Input to the oscillator's high-gain amplifier. Driven by a 12 MHz clock on the DHV11.

XTAL2
Output from the oscillator's amplifier. Grounded on the DHV11.

A.2.3 Read/Write Timing

Read/write timing cycles are shown in Figures A-3, A-4, and A-5.

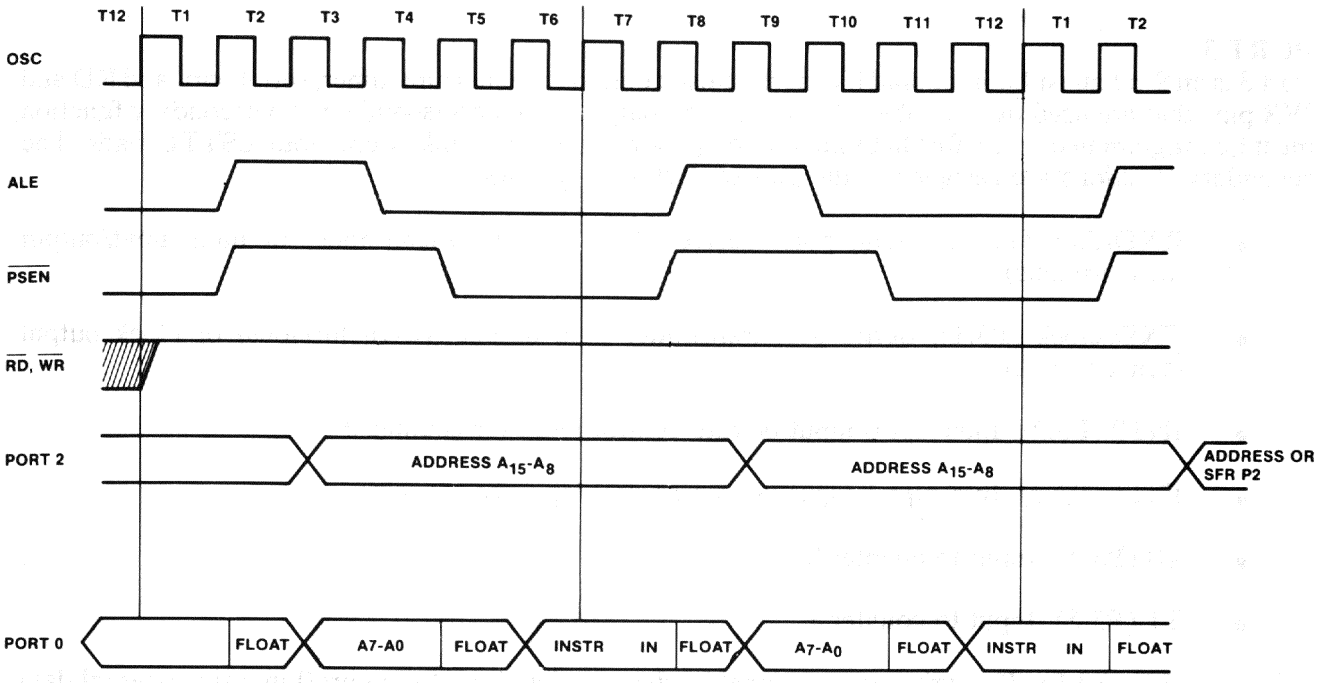


Figure A-3 Program Memory Read Cycle

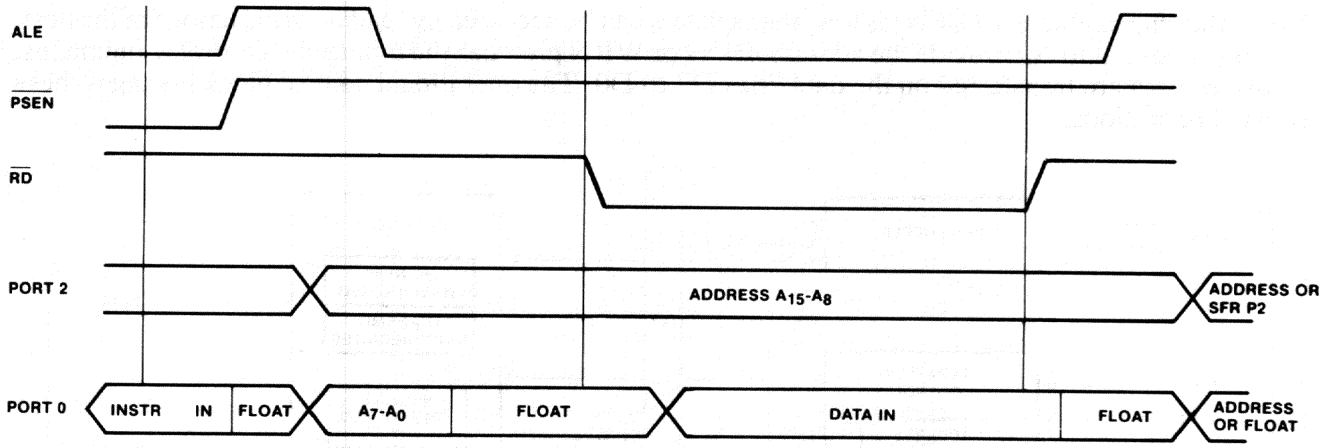


Figure A-4 Data Memory Read Cycle

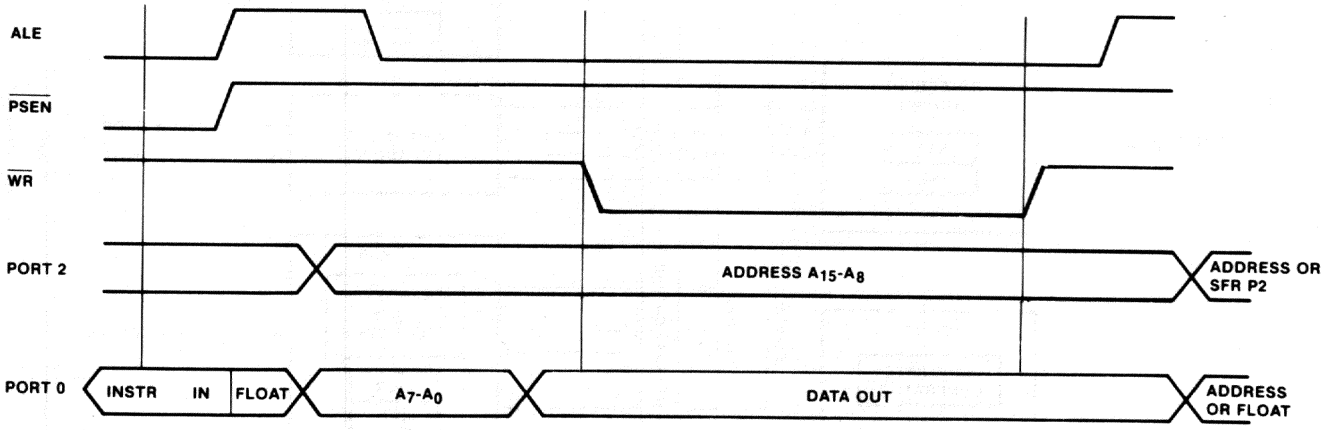


Figure A-5 Data Memory Write Cycle

In each cycle, ALE (Address Latch Enable) is issued as a latching signal for A7 to A0. Latching occurs on the negative-going edge of ALE. Once the low address bits are latched, port 0 can be used to transfer data.

If program memory is being read, Program Store Enable (PSEN L) must be asserted before the instruction is read in. RD L and WR L will both be invalid.

When data memory is being accessed PSEN L is false and RD L or WR L are asserted.

Note that with a 12 MHz clock (OSC), a program memory cycle takes 500 nanoseconds. A data memory cycle takes one microsecond.

A.3 SC2681 DUAL UART (DUART)

A.3.1 Block Description

Block diagram Figure A-6 shows the functional blocks of the DUART. Except for the bus buffer, which is a parallel holding register, there are control registers in every block. It is via these registers that the DUART is programmed and monitored.

When the chip enable line (CEN) is low, the registers can be accessed by read or write actions of the host. Address lines A3 to A0 provide the address. RDN or WRN provides the timing and control. Commands, status, or data are transferred on the data lines D7 to D0. The operational control block manages these parallel operations.

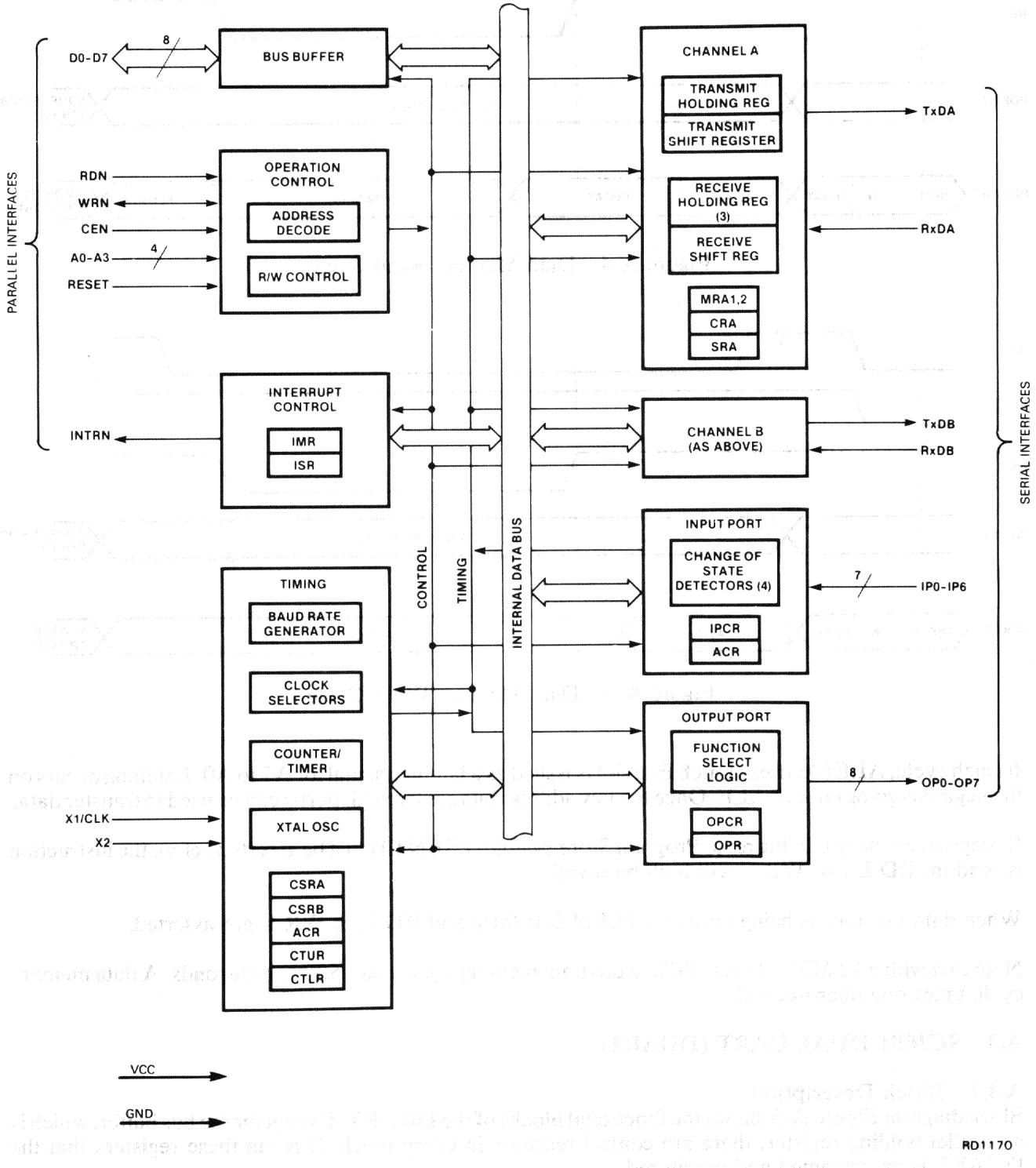


Figure A-6 SC2681 Dual Universal Asynchronous Receiver Transmitter (DUART)

Two serial data channels (A and B) perform the parallel/serial and serial/parallel conversion. Each TRANSMIT channel has a 2-byte buffer. This allows the next character to be loaded while the previous one is being transmitted. Each RECEIVE channel has a 4-byte buffer to allow for delays in interrupt response.

Also related to the serial interface are a 7-bit input port and an 8-bit output port. These lines can be used as individual, sense, and flag lines. Each line has a secondary function which may be used to provide modem control for the serial data lines.

A 3.6864 MHz crystal provides the basic timing for the timing block. This section contains a programmable counter/timer which can be programmed for many RECEIVE and TRANSMIT baud rates. The counter timer can also be clocked by input port 2.

Interrupts are generated when at least one of eight maskable interrupt conditions occurs. INTRN will inform the controlling processor of changes in the DUART status. The interrupt routine should read status and then take the appropriate action. INTRN is commonly used to indicate that a received character has been assembled or that the DUART can accept a new character for transmission.

The DUART can also be operated in the polled mode.

Characters to be transmitted must be written to the appropriate transmit holding register.

Received characters must be read from the appropriate receive holding register.

A.3.2 Pin-Out Information

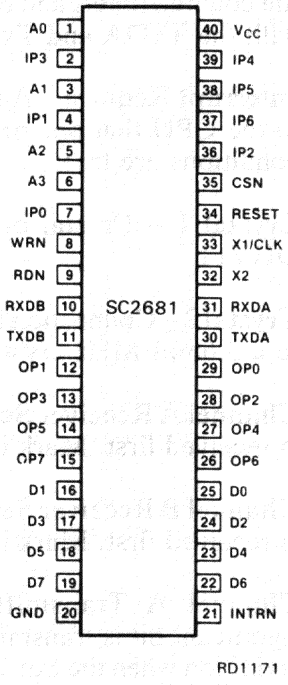


Figure A-7 SC2681 Pin-Out Diagram

A pin-out diagram is provided in Figure A-7. The related pin functions are listed in Table A-2. This information applies to the 40-pin DIL version of SC2681 only.

Table A-2 SC2681 Pin Designation

Mnemonic	Direction	Pin Name and Function
D0 to D7	I/O	Data Bus – Bidirectional 3-state data bus used to transfer commands, data, and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	Chip Enable – Active-low input signal. When low, data transfers between the CPU and the DUART are enabled on D0 to D7 as controlled by the WRN, RDN, and A0 to A3 inputs. When high, places the D0 to D7 lines in the 3-state condition.
WRN	I	Write Strobe – When low, and CEN is also low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the positive-going edge of the signal.
RDN	I	Read Strobe – When low and CEN is also low, causes the contents of the addressed register to be placed on the data bus. The read cycle starts on the negative-going edge of RN.
A0 to A3	I	Address Inputs – Select the DUART internal registers and ports for read/write operations.
RESET	I	Reset – A high level clears the internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0 to OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state with the TxDA and TxDB outputs in the mark (high) state.
INTRN	O	Interrupt Request – Active-low open-drain output which signals to the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	Crystal 1 – Crystal or external clock input. Grounded on the DHV11.
X2	I	Crystal 2 – Connection for the other side of the crystal. Connected to a 3.6864 MHz crystal on the DHV11.
RxDA	I	Channel A Receiver Serial Data Input – The least significant bit is received first. Mark is high, space is low.
RxDB	I	Channel B Receiver Serial Data Input – The least significant bit is received first. Mark is high, space is low.
TxDA	O	Channel A Transmitter Serial Data Output – The least significant bit is transmitted first. This output is held in the mark condition when the transmitter is disabled, idle, or when operating in local loopback mode. Mark is high, space is low.
OP0 to OP7	O	General Purpose Outputs – Used by the DHV11 for modem control.

Table A-2 SC2681 Pin Designation (Cont)

Mnemonic	Direction	Pin Name and Function
IP0 to IP6	I	General Purpose Inputs – Used by the DHV11 to monitor modem status.
Vcc	I	Power Supply – +5 V supply input
GND	I	Ground

A.4 DC003 INTERRUPT IC

The interrupt controller is an 18-pin DIL device that provides the circuits to perform an interrupt transaction in a computer system that uses a 'pass-the-pulse' type arbitration. The device provides two interrupt channels, A and B, with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or open-collector outputs, which allow the device to be attached directly to the computer system bus. Maximum current taken from the Vcc supply is 140 mA.

Figure A-8 is a simplified logic diagram of the DC003 IC. Timing for the interrupt section is shown in Figure A-9, while Figure A-10 shows the timing for both A and B interrupt sections. Table A-3 describes the signals and pins of the DC003 by pin and signal name.

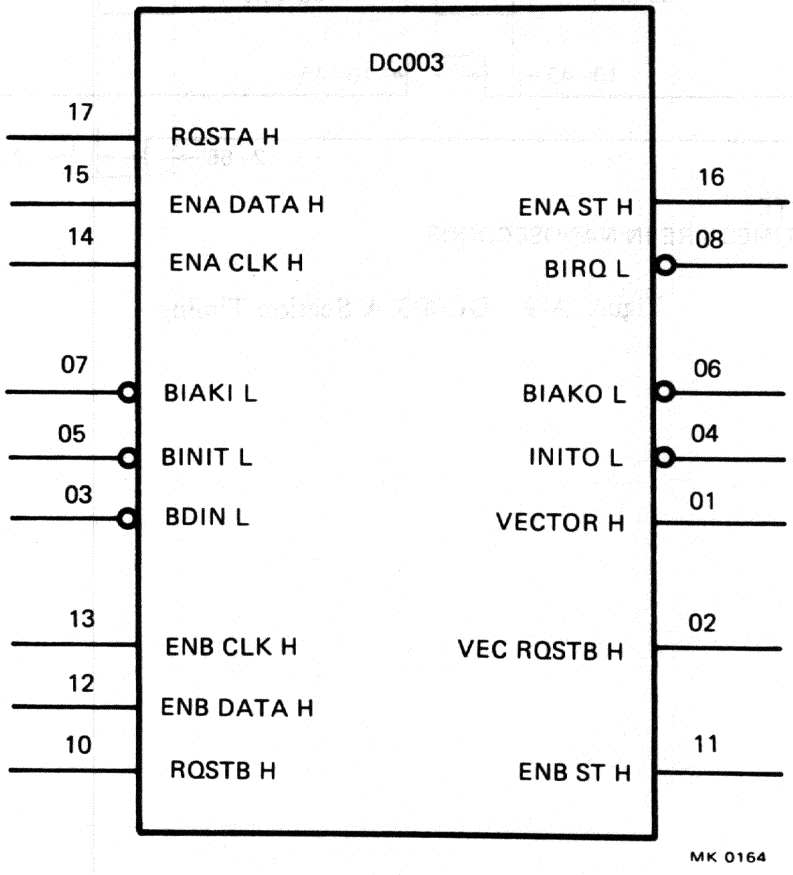


Figure A-8 DC003 Logic Symbol

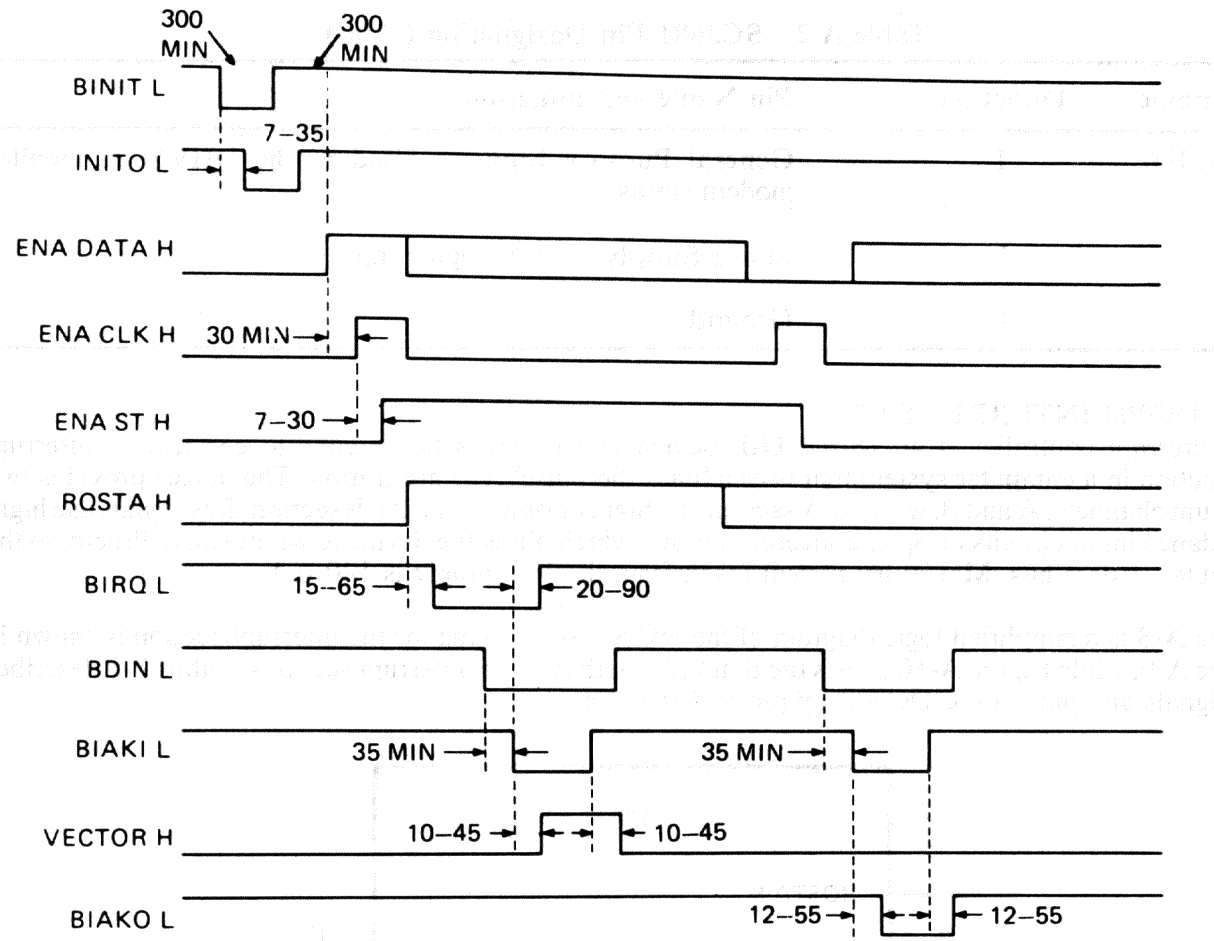
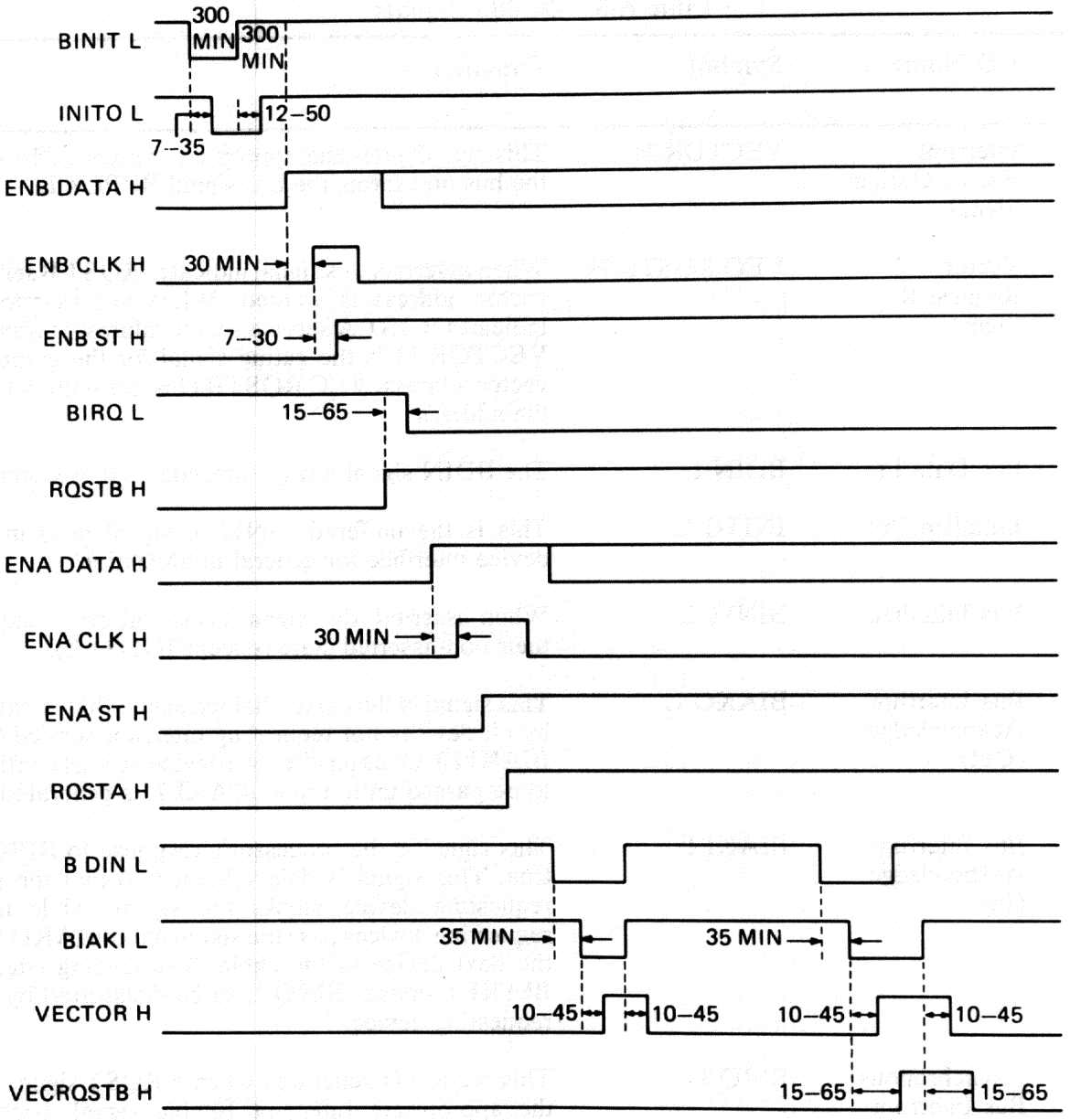


Figure A-9 DC003 A Section Timing



NOTE:
TIMES ARE IN NANOSECONDS.

Figure A-10 DC003 A and B Section Timing

Table A-3 DC003 Signals

Pin No.	I/O Name	Symbol	Function
1	Interrupt Vector Gating Signal	VECTOR H	This signal gates the appropriate vector address to the bus and forms the bus signal BRPLY L.
2	Vector Request B Signal	VEC RQSTB H	When asserted, this signal indicates RQST B service vector address is wanted. When not asserted it indicates RQST A service vector address is wanted. VECTOR H is the gating signal for the complete vector address; VEC RQSTB H is normally bit 2 of the address.
3	Bus Data In	BDIN L	The BDIN signal always precedes a BIAK signal.
4	Initialize Out	INITO L	This is the buffered BINIT L signal used in the device interface for general initialization.
5	Bus Initialize	BINIT L	When asserted, this signal brings all drive lines to their non-asserted state (except INITO L).
6	Bus Interrupt Acknowledge (Out)	BIAKO L	This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must continue to be passed until a new BIAKI L is generated.
7	Bus Interrupt Acknowledge (In)	BIAKI L	This signal is the processor's response to BIRQ L true. This signal is daisy-chained so that the first requesting device blocks the signal, while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be deasserted by the requesting device.
8	Asynchronous Bus Interrupt Request	BIRQ L	This request is generated when a RQST signal and the appropriate Interrupt Enable signal become valid. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal, or the removal of the appropriate interrupt enable, or by the removal of the appropriate request signal.
17 10	Device Interrupt Request Signal	RQSTA H RQSTB H	When asserted with the enable A/B flip-flop asserted, this signal causes BIRQ L to be asserted on the bus. This signal line normally stays asserted until the request is serviced.
16 11	Interrupt Enable Status	ENA ST H ENB ST H	This signal indicates the state of the interrupt enable A/B internal flip-flop which is controlled by the signal line ENA/B DATA H and the ENA/B CLK H clock line.

Table A-3 DC003 Signals (Cont)

Pin No.	I/O Name	Symbol	Function
15 12	Interrupt Enable Data	ENA DATA H ENB DATA H	The level on this line, in conjunction with the ENA/B CLK H signal, determines the state of the internal interrupt enable A flip-flop. The output of this flip-flop is monitored by the ENA/B ST H signal.
14 13	Interrupt Enable clock	ENA CLK H ENB CLK H	When asserted (on the positive edge), interrupt enable A/B flip-flop assumes the state of the ENA/B DATA H signal line.

A.5 DC004 PROTOCOL IC

The protocol chip is a 20-pin DIL device that functions as a register selector, providing the signals necessary to control data flow to and from up to four word registers (8 bytes). Bus signals can be directly attached to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed so that if close tolerance is not wanted, only an external 1 kilohm (+ or – 20%) resistor is needed. External RCs can be added to change the delay. Maximum current taken from the Vcc supply is 120 mA.

Figure A-11 is a simplified logic diagram of the DC004 IC. Signal timing in relation to different loads is shown in Figure A-12. Signal and pin definitions for the DC004 are shown in Table A-4.

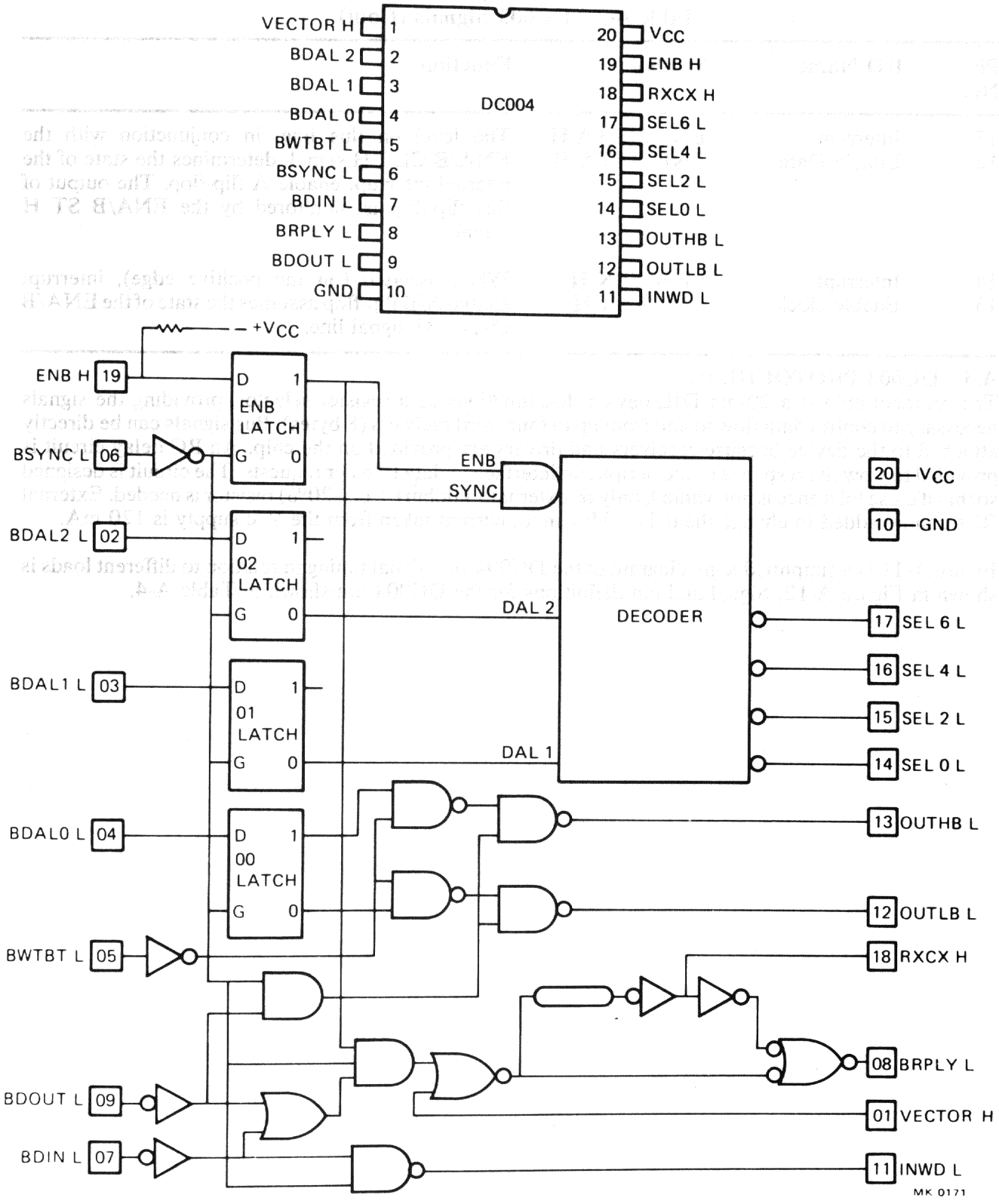
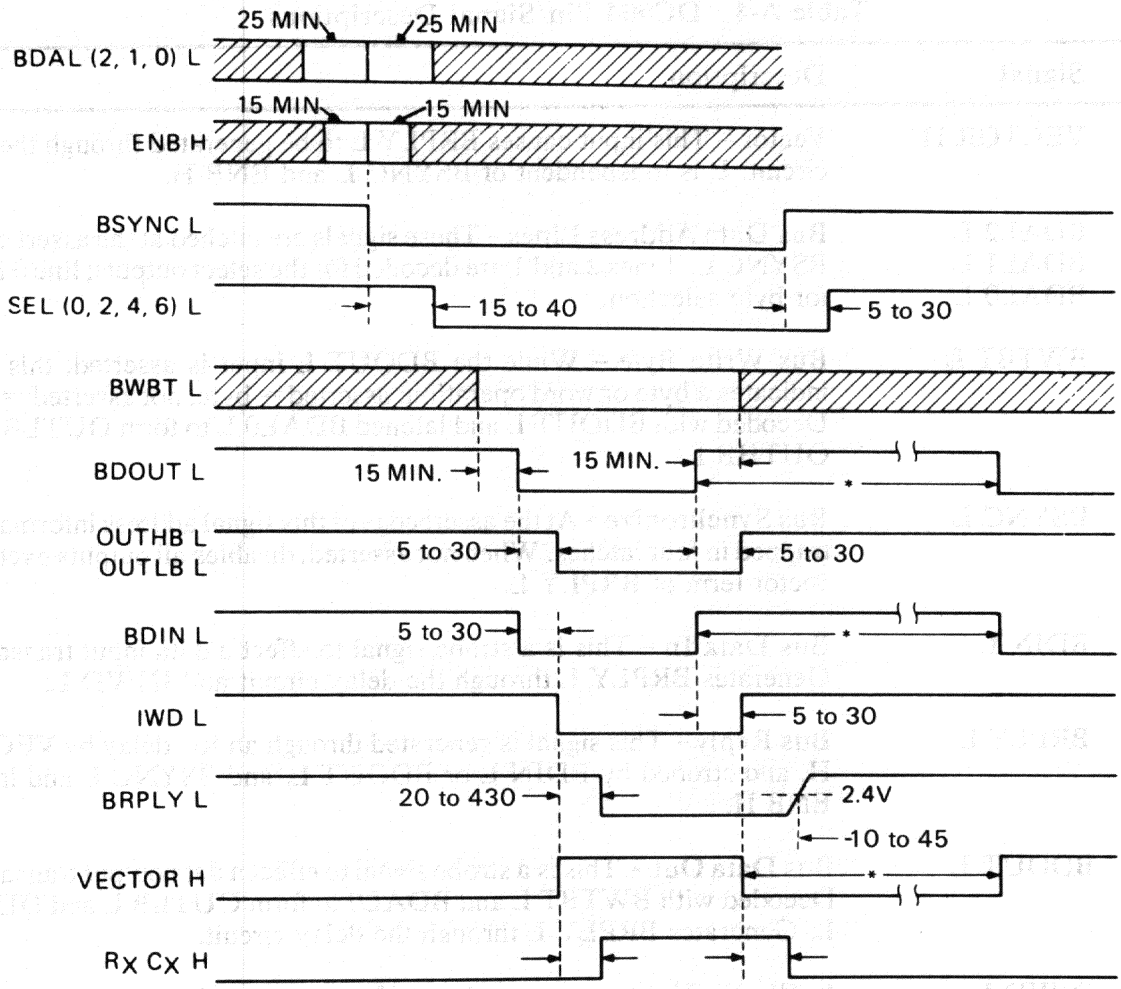


Figure A-11 DC004 Simplified Logic Diagram



*TIME REQUIRED TO DISCHARGE R_X C_X FROM ANY CONDITION ASSERTED = 150ns

NOTE:
TIMES ARE IN NANOSECONDS.

RD1346

Figure A-12 DC004 Timing Diagram

Table A-4 DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Vector – This input causes BRPLY L to be generated through the delay circuit. It is independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	Bus Data Address Lines – These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	Bus Write Byte – While the BDOUT L input is asserted, this signal indicates a byte or word operation: asserted = byte, not asserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	Bus Synchronize – At the assert edge of this signal address information is trapped in four latches. When not asserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	Bus Data In – This is a strobe signal to effect a data input transaction. Generates BRPLY L through the delay circuit and INWD L.
8	BRPLY L	Bus Reply – This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or BDOUT L, and BSYNC L and latched ENB H.
9	BDOUT L	Bus Data Out – This is a strobe signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWD L	In Word – Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUTLB L OUTHB L	Out Low Byte, Out High Byte – Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	Select Lines – One of these four signals is true as a function of BDAL2 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and, once asserted, are not deasserted until BSYNC L is deasserted.
18	RXCX	External Resistor Capacitor Node – This node is provided to vary the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to Vcc and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	Enable – This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

A.6 DC005 BUS TRANSCEIVER IC

The 4-bit transceiver is a 20-pin DIL low-power Schottky device for primary use in peripheral device interfaces. It functions as a bidirectional buffer between a data bus and peripheral device logic. In addition to the isolation function, the device also provides a comparison circuit for address selection, and a constant generator, useful for interrupt vector addresses. The bus I/O port provides high-impedance inputs and open-collector outputs to allow direct connection to a computer's data bus. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA tri-state drivers. Data on this port has the opposite polarity to the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs and to generate the signal MATCH. The MATCH output is open-collector, which allows the output of more than one transceiver to be wire-ANDed to form a combined address match signal. The address jumpers can also be put into a third logical state that disconnects that jumper from the address match, allowing for 'don't care' address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant, that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three operation states: receive data, transmit data, and disable.

Figure A-13 is a simplified logic diagram of the DC005 IC. Timing for the functions is shown in Figure A-14. Signal and pin definitions for the DC005 are given in Table A-5.

Table A-5 DC005 Pin/Signal Descriptions

Pin	Name	Function
12 11 9 8	BUS0 L BUS1 L BUS2 L BUS3 L	**Bus Data** – This set of four lines constitutes the bus side of the transceiver. Open-collector outputs; high-impedance inputs. Low = 1.
18 17 7 6	DAT0 H DAT1 H DAT2 H DAT3 H	**Peripheral Device Data** – These four tri-state lines carry the inverted received data from BUS (3:0) when the transceiver is in the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS (3:0). When in the disabled mode, these lines go open (high impedance). High = 1.
14 15 16	JV1 H JV2 H JV3 H	**Vector Jumpers** – These inputs, with internal pull-down resistors, directly drive BUS (3:1). A low or open on the jumper pin causes an open condition on the corresponding BUS pin if XMIT H is low. A high causes a 1 (low) to be transmitted on the BUS pin. Note that BUS0 L is not controlled by any jumper input.
13	MENB L	**Match Enable** – A low on this line enables the MATCH output. A high forces MATCH low, overriding the match circuit.
3	MATCH H	**Address Match** – When BUS (3:1) matches the state of JA (3:1) and MENB L is low, this output is open; otherwise, it is low.

Table A-5 DC005 Pin/Signal Descriptions (Cont)

Pin	Name	Function
1 2 19	JA1 L JA2 L JA3 L	**Address Jumpers** – A connection to ground on these inputs allows a match to occur with a 1 (low) on the corresponding BUS line. An open allows a match with a 0 (high). A connection to Vcc disconnects the corresponding address bit from the comparison.
5 4	XMIT H REC H	**Control Inputs** – These lines control the operation of the transceiver as follows. **REC XMIT** 0 0 DISABLE: BUS and DAT open 0 1 XMIT DATA: DAT to BUS 1 0 RECEIVE: BUS to DAT 1 1 RECEIVE: BUS to DAT To avoid tri-state overlap conditions an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode, and delays the enabling of tri-state drivers on the DAT lines. This action is independent of the DISABLE mode.

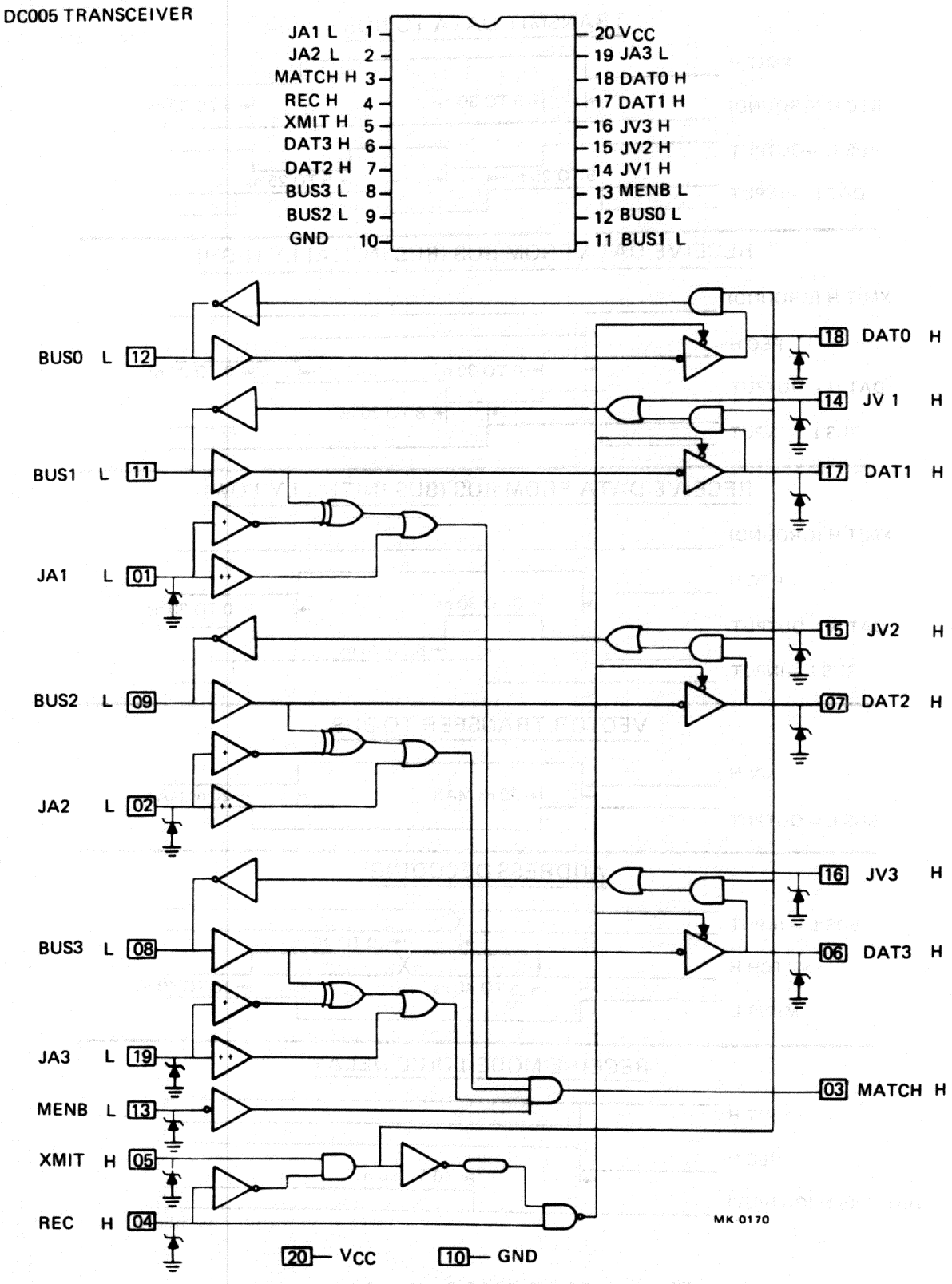


Figure A-13 DC005 Simplified Logic Diagram

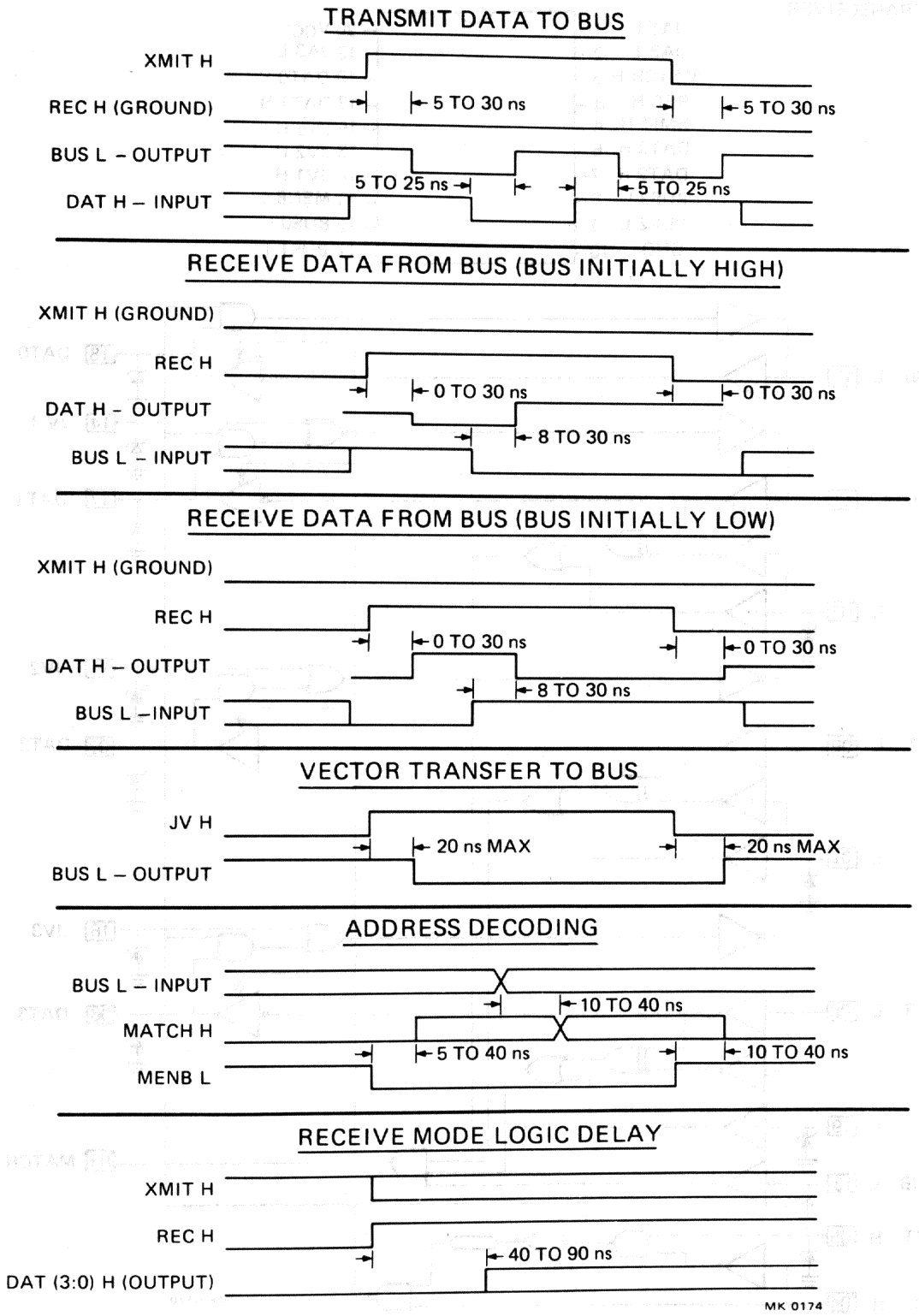


Figure A-14 DC005 Timing Diagram

A.7 DC010 DIRECT MEMORY ACCESS LOGIC

This DMA controller provides the logic to perform the handshaking operations needed to request and to gain control of the system bus. Once the DC010 becomes bus master it generates the signals needed to perform a DIN, DOUT, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up the bus.

Figure A-15 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are shown in Figure A-16, and the DC010 voltage waveforms are shown in Figure A-17. Table A-6 describes the signals and pins of the DC010 by pin and signal name. Figures A-18 and A-19 show the timing.

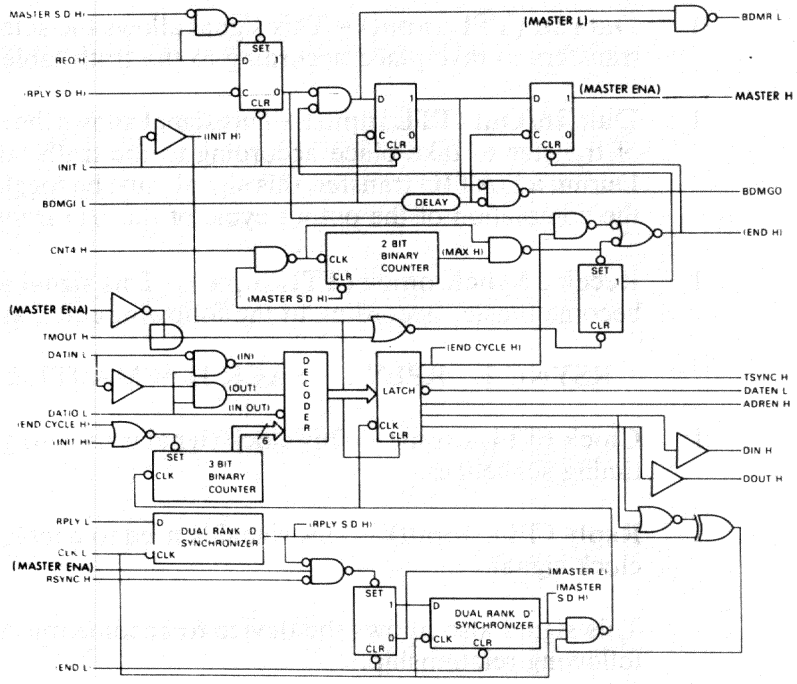


Figure A-15 DC010 Simplified Logic Diagram

Table A-6 DC010 Pin/Signal Descriptions

Pin	Signal	Group	Description
1	REQ H	1	**Request (TTL Inputs)** – A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L		**DMA Grant Input (High Impedance)** – A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise this signal is delayed and output as BDMGO.
16	CNT 4 H	1	**Count Four (TTL Output)** – A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open this pin will assume a high state.

Table A-6 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
14	TMOUT H	1	**Time-Out (TTL Input/Open Collector Output)** – This I/O pin is low while SACK H is high. It goes into high impedance when SACK H is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been deasserted because of the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	1	**Data In (TTL Input)** – This signal allows the selection of the type of transfers to take place according to the truth table (Figure A-16).
2	DATIO L	1	**Data In/Out (TTL Input)** – This signal allows the selection of the type of transfer to take place according to the truth table (Figure A-16). During a DATIO transfer, this signal must be toggled in order to allow the completion of the output cycle of the I/O transfer.
12	RSYNC L	1	**Receive Synchronize (TTL Input)** – This signal allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
17	CLK L	1	**Clock (TTL Input)** – This clock signal is used to generate all transfer timing sequences.
15	RPLY H	1	**Reply (TTL Input)** – This signal is used to enable or disable the free clock signal. This signal also allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
19	INIT L	1	**Initialize (TTL Input)** – This signal is used to initialize the chip to the state where REQ is needed to start a bus request transaction. When INIT is low, the following signals are deasserted: BDMR L, MASTER H, DATEN L, ADREN L, SYNC H, DIN H, DOUT H.
11	BDMR L	1	**DMA Request (Open Collector Output)** – A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	1	**Master (TTL Output)** – A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.
8	BDMGO L	1	**DMA Grant Output (Open Collector Output)** – This signal is the delayed version of BDMGI if no request is pending; otherwise it is not asserted. This output may be tied directly to the bus.

Table A-6 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Group	Description
7	TSYNC H	1	Transmit Synchronize (TTL Output) – This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	1	Data Enable (TTL Output) – This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	1	Address Enable (TTL Output) – This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	1	Data In (TTL Output) – This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	1	Data Out (TTL Output) – This signal is asserted to indicate that the bus master device has output valid data.

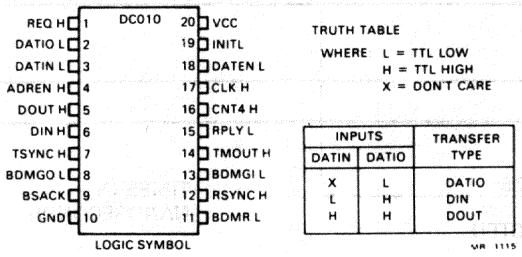


Figure A-16 DC010 Logic Symbol/Truth Table.

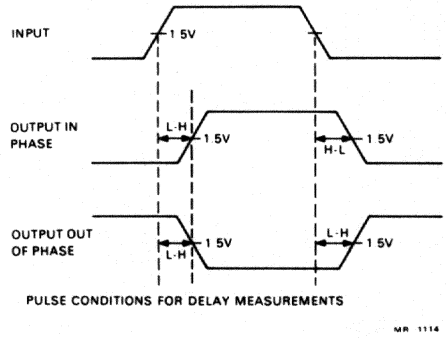


Figure A-17 DC010 Voltage Waveforms

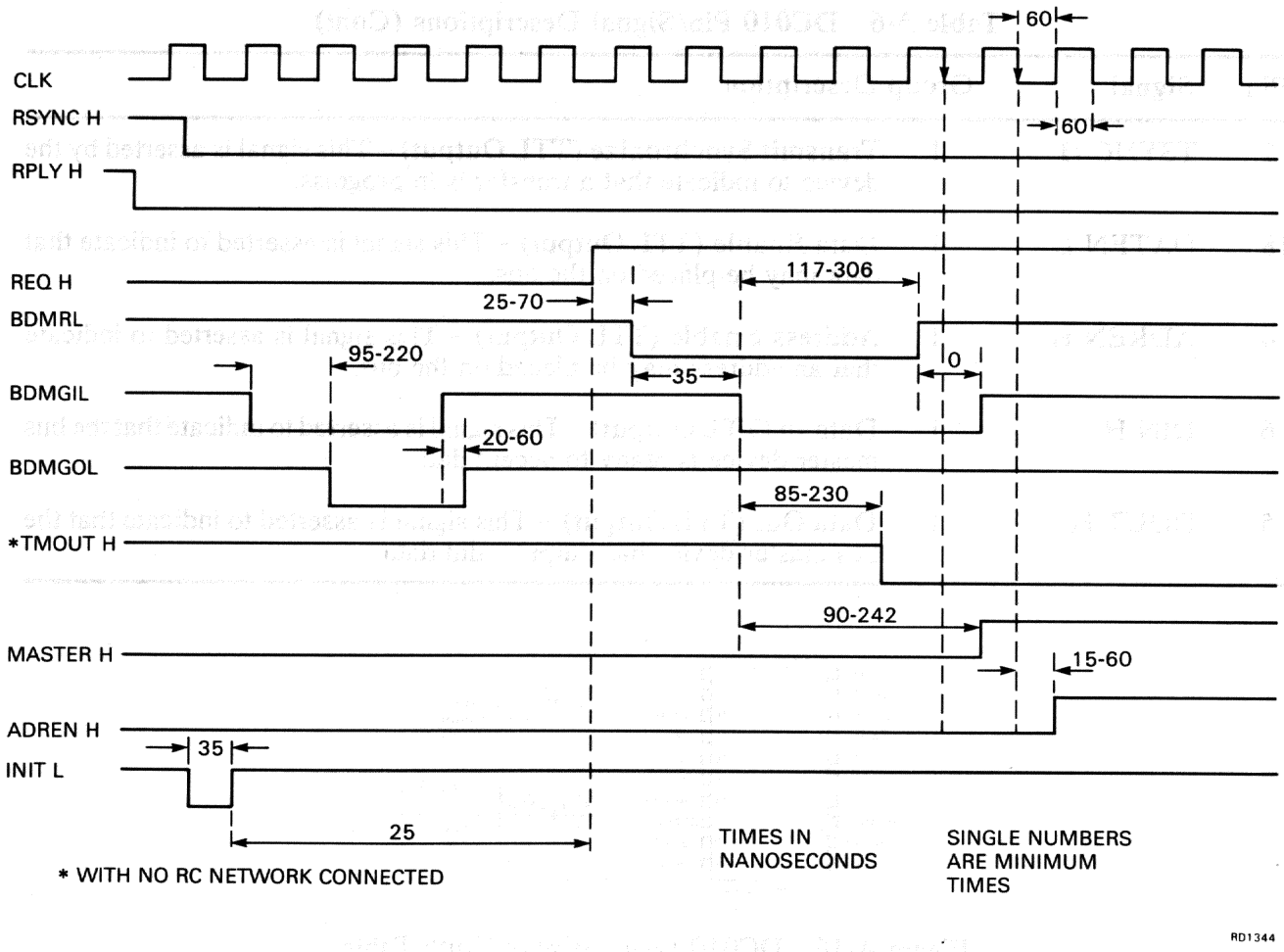


Figure A-18 DC010 Timing Diagram, DMA Request/Grant

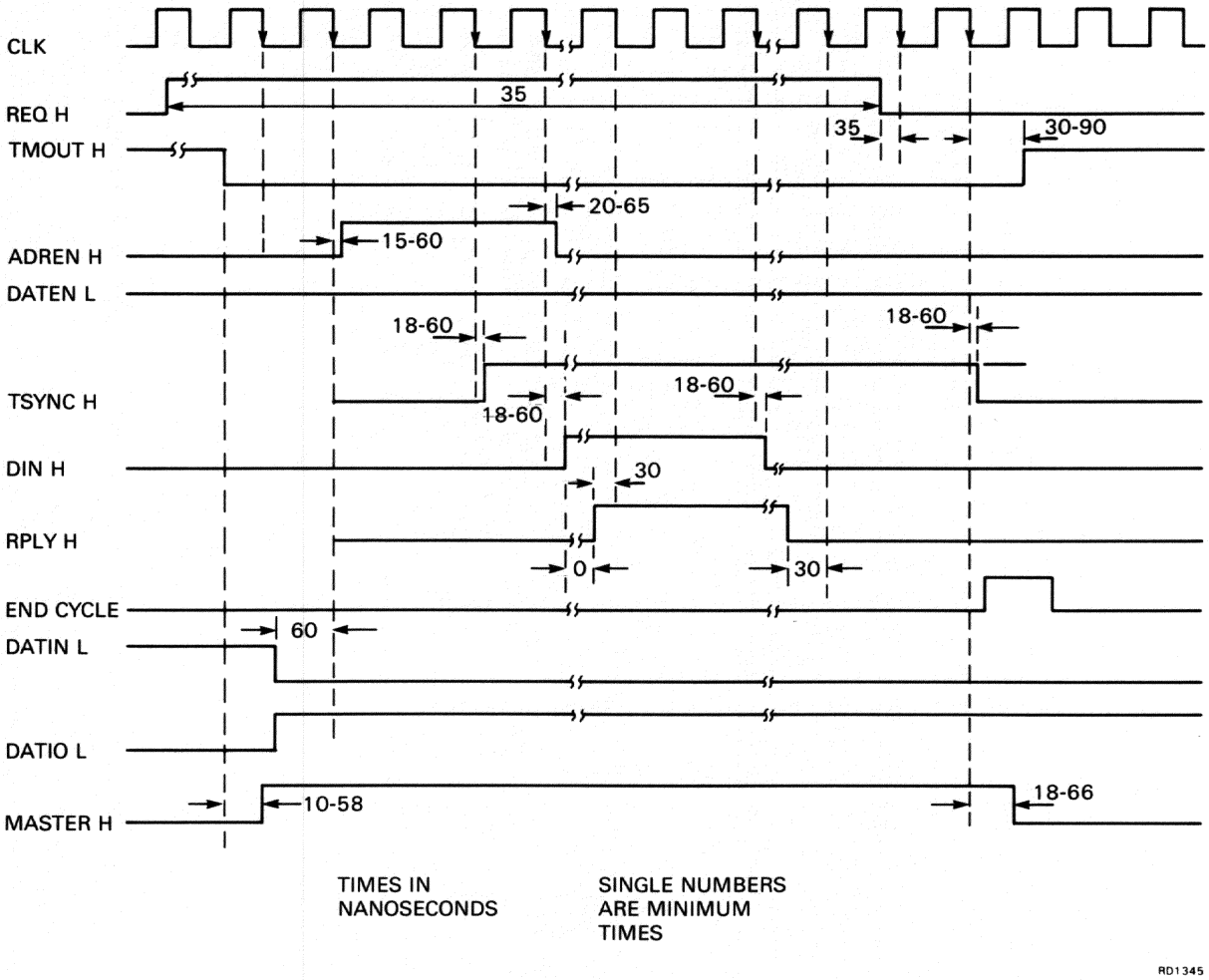


Figure A-19 DC010 Timing Diagram

APPENDIX B
MODEM CONTROL

B.1 SCOPE

This appendix contains information useful to both the programmer and the engineer. It defines control signals, describes typical modem control methods, and warns against likely network faults. A detailed example of auto-answer operation is included.

B.2 MODEM CONTROL

The DHV11 supports sufficient modem control to permit full-duplex operation over the public switched telephone network (PSTN) and over private telephone lines. Table B-1 lists the control leads supported by the DHV11 together with an explanation of their use and purpose. In this appendix, the terms MODEM and DATASET have the same meaning. They refer to the device which is used to modulate and demodulate the signals transmitted over the communications circuits.

The DHV11 modem control interface can be used in many applications. These include control of serial line printers, terminal cluster controllers, and industrial I/O equipment, in addition to the more usual applications in telephone networks. Use of the control leads described in Table B-1 is therefore completely application dependent, although there are international standards which telephone network applications should obey. There are no hardware interlocks between the modem control logic and the transmitter and receiver logic. Program control manages these actions as necessary.

A subset of the leads listed in Table B-1 could be used to establish a communications link using modems connected to the switched telephone network. Ring Indicator (RI), Data Terminal Ready (DTR), and Data Carrier Detected (DCD) are the absolute minimum requirements. In some countries Dataset Ready (DSR) is also needed. It is usually desirable, however, to implement modem control protocols which will operate over most telephone systems in the world. Also, some protection should be included to guard against network faults, particularly in applications such as dial-up time-sharing systems. Such faults include:

- Making a channel permanently busy (hung) because of a misdialed connection from a non-data station
- Connecting a new incoming call on an in-use channel. This fault might occur, for example, after a temporary carrier loss, if the host system assumed that the carrier was reasserted by the original caller.

Modem control with some protection against common faults, and which is compatible with the telephone networks in most geographic areas, can be implemented by using all the signals listed in Table B-1, in the way described by the CCITT V.24 recommendations. Section B.2.1 describes a method of implementing a full-duplex auto-answer communications link via modems over the PSTN. It is provided here only to show the operation and interaction of DHV11 modem control leads in a typical application.

Table B-1 Modem Control Leads

Name	RS-232-C	V.24	25-Pin	Definition
GND	AA	–	1	Protective ground. This provides a path between the modem and DHV11 for discharge of potentials such as static electricity.
GND	AB	102	7	Signal Ground. This is a reference level for the data and control signals used at the EIA interface.
TXD	BA	103	2	From DHV11 to modem. This signal contains the serial bit stream to be transmitted to the remote station.
RXD	BB	104	3	From modem to DHV11. This signal is the serial bit stream received by the modem from the remote station.
RTS	CA	105	4	From DHV11 to modem. Causes the modem's carrier to be placed on the line.
CTS	CB	106	5	From modem to DHV11. Indicates that the modem has successfully placed its carrier on the line and that data presented on circuit BA will be transmitted to the communication channel.
DSR	CC	107	6	From modem to DHV11. Indicates that the modem has completed all call establishment functions and is successfully connected to a communications channel.
DTR	CD	108/2	20	From DHV11 to modem. Indicates to the modem that the DHV11 is powered up and ready to answer an incoming call.
DCD	CF	109	8	From modem to DHV11. Indicates to the DHV11 that the remote station's carrier signal has been detected and is within appropriate limits.
RI	CE	125	22	From modem to DHV11. Indicates that a new incoming call is being received by the modem.

B.2.1 Example of Auto-Answer Modem Control for the PSTN

The system operator determines which DHV11 channels should be configured for either local or remote operation. Local operation implies control of data-leads only, while remote operation implies that modem control will be supported. The host software will assert DTR and RTS together with the Link Type bit in the LNCTRL register for all DHV11 channels configured for remote operation. DTR informs the modem that the DHV11 is powered up and ready to acknowledge control signals from the modem. RTS is asserted for the full-duplex mode of operation and causes the modem to place its carrier on the telephone line when the modem answers a call. Link Type (LNCTRL<8>) enables modem status information to be placed in the receive character FIFO where it will be handled by an interrupt service routine. Modem status changes are always reported in the STAT register regardless of the state of LNCTRL<8>. The modem is now prepared to auto-answer an incoming call.

Dialing the modem's number causes RI to be asserted at the EIA interface. This informs the DHV11 that a new call is being received. RI has to be in a stable state for at least 30 ms or else the change will not be reported by the DHV11. Since DTR is already asserted, the modem will auto-answer the incoming call and start its handshaking sequence with the calling station. The time needed to complete the handshaking sequence can be in the order of tens of seconds if fallback mode speed selection and satellite links are involved. The modem will assert DSR to indicate to the DHV11 that the call has been successfully answered and a connection established.

NOTE

On some older types of modem used on the PSTN, the opposite effect is also true. The RI signal may be very short, or it may not even occur if DTR is previously asserted. When this type of modem answers an incoming call it asserts DSR almost immediately and deasserts RI at the EIA interface. Programs must therefore expect RI or DSR or DCD as the first dataset status change received from the modem when establishing a connection.

As RTS was previously asserted, the modem's carrier will be placed on the line when DSR is asserted. When the modem has successfully placed its carrier on the line it will assert CTS which indicates to the DHV11 that it may start to transmit data. Should the incoming call be the result of a misdialed number then it is possible that a carrier signal would never be received. To guard against this, the host starts a timer when it detects RI or DSR. This is usually in the range of 15 to 40 seconds, within which time the carrier must be detected. When the modem detects the remote modem's carrier signal on the line, it will assert DCD which indicates to the DHV11 that data is valid on the RXD line.

The modem may now exchange data between the DHV11 and the calling station for as long as DCD, DSR, and CTS stay asserted. If any of these three signals disappear, or if RI should be detected during normal transmission, it would indicate a fault condition. A change of state of any of these signals would cause an interrupt via the receive FIFO.

The handling of the fault conditions now becomes country-specific as some telephone systems tolerate a transient carrier loss while others do not. In the USA it is usual to proceed with a call if carrier resumes within two seconds. In non-USA areas it is possible for telephone supervisory signals, such as dial-tone, to be misinterpreted by the modem as a resumption of carrier. In this case the host program would assume that the connection had been reestablished to the original caller and would cause a 'hung' channel. To prevent this, DTR should be deasserted immediately after the loss of DCD, CTS, or DSR to abort the connection. DTR should stay deasserted for at least two seconds, after which time a new call could be answered.

APPENDIX C
GLOSSARY OF TERMS

C.1 SCOPE

This appendix contains a glossary of terms used in this manual. The terms are in alphabetical order for easy reference.

C.2 GLOSSARY

asynchronous A method of serial transmission in which data is preceded by a start bit and followed by a stop bit. The receiver provides the intermediate timing to identify the data bits.

auto-answer A facility of a modem or terminal to automatically answer a call.

auto-flow Automatic flow control. A method by which the DHV11 controls the flow of data by means of special characters within the data stream.

backward channel A channel which transmits in the opposite direction to the usual data flow. Normally used for supervisory or control signals.

BAL Bus Address Line.

BDAL Bus Data and Address Line.

base address The address of the CSR.

BMP Background Monitor Program.

CCITT Comite Consultatif International de Telephonie et de Telegraphie. An international standards committee for telephone, telegraph, and data communications networks.

dataset See modem

DIL Dual-In-Line. The term describes ICs and components with two parallel rows of pins.

DMA Direct Memory Access. A method which allows a bus master to transfer data to and from system memory without using the host CPU.

DUART Dual Universal Asynchronous Receiver Transmitter. An IC used for transmission and reception of serial asynchronous data on two channels.

duplex A method of transmitting and receiving on the same channel at the same time.

EIA Electrical Industries of America. An American organisation with the same function as the CCITT.

EMC Electro-Magnetic Compatibility. The term denotes compliance with field-strength, susceptibility, and static discharge standards.

FCC Federal Communications Commission. An American organisation which regulates and licenses communications equipment.

FIFO First In First Out. The term describes a register or memory from which the oldest data is removed first.

floating address A CSR address assigned to an option which does not have a fixed address allocated. The address is dependent on other floating address devices connected to the bus.

floating vector An interrupt vector assigned to an option which does not have a fixed vector allocated. The vector is dependent on other floating vector devices connected to the bus.

FRU Field Replaceable Unit.

GO/NOGO A test or indicator which defines only an 'error' or 'no error' condition.

IC Integrated Circuit.

I/O Input/Output.

LSB Least Significant Bit.

LSI-11 bus Another name for the Q-bus.

microcomputer An IC which contains a microprocessor and peripheral circuitry such as memory, I/O ports, timers, and UARTs.

modem The word is a contraction of MOdulator DEModulator. A modem interfaces a terminal to a transmission line. A modem is sometimes called a dataset.

MSB Most Significant Bit.

multiplexer A circuit which connects a number of lines to one line.

null modem A cable which allows two terminals which use modem control signals to be connected together directly. Only possible over short distances.

PCB Printed Circuit Board.

protocol A set of rules which define the control and flow of data in a communications system.

PSTN Public Switched Telephone Network.

Q-bus A global term for a specific DIGITAL bus on which the address and data are multiplexed.

Q22, Q18 and Q16 Terms used to define 22-, 18-, and 16-bit address versions of Q-bus.

RAM Random Access Memory.

RFI Radio Frequency Interference.

ROM Read Only Memory.

SMPS Switch Mode Power Supply.

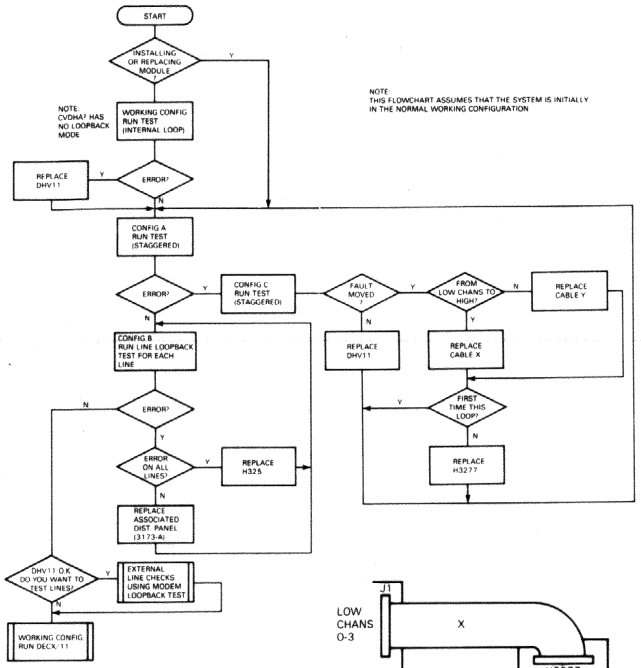
split-speed A facility of a data communications channel which can transmit and receive at different data rates at the same time.

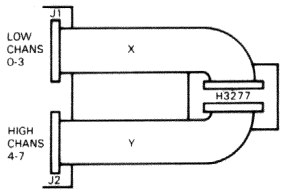
UART Universal Asynchronous Receiver Transmitter. An IC used for transmission and reception of serial asynchronous data on a channel.

X-OFF A control code (23_8) used to disable a transmitter. Special hardware or software is needed for this function.

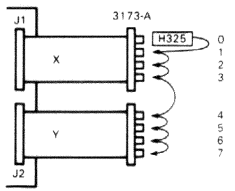
X-ON A control code (21_8) used to enable a transmitter which has been disabled by an X-OFF code.

TROUBLESHOOTING FLOWCHART

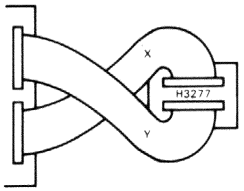




CONFIGURATION A



CONFIGURATION B



CONFIGURATION C

Basic Installation Procedure

1. Unpack and check the components of the option.
2. Check and, if necessary, set up device address and vector switches.
3. Install BC05L cables to J1 and J2.
4. Install module in its correct bus slot.
5. Check backplane voltages.
6. Connect other end of BC05L cables to distribution panels as in interconnection diagram.
7. Check out system and perform installation tests.
8. Check cable routing and replace any covers.

DIAGNOSTIC EXAMPLES

1. Error-free pass

```
R CVDHBA
CVDHBA.BIN

DRSC7
CVDHB-A-0
DHV-11 FUNCT TEST PART2
UNIT 1 IS DHV-11
RESTART ADDR: 147670

DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1

UNIT 0

CSR ADDRESS: (0) 160460 ? 160500
INTERRUPT VECTOR ADDRESS: (0) 300 ?_
ACTIVE LINE BIT MAP: (0) 377?_

TYPE OF LOOPBACK (1=INTERNAL, 2=STAGGERED,
                  3=25 PIN CONNECTOR, 4=MODEM): (0) 2 ?_

INTERRUPT BR LEVEL: (0) 4 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
NUMBER OF INDIVIDUAL DATA ERROR TO REPORT ON A LINE:  (D) 0 ?_

CVDHB EOP 1
    0 CUMULATIVE ERRORS

DR>EXIT
```

2. Test with wrong device address selected

```
R CVDHBA
CVDHBA.BIN
DRSC7
CVDHB-A-0
DHV-11 FUNCT TEST PART2
UNIT IS DHV-11
RESTART ADDR: 147670
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1

UNIT 0
CSR ADDRESS: (0) 160460 ? 160500
INTERRUPT VECTOR ADDRESS: (0) 377 ?_
ACTIVE LINE BIT MAP: (0) 377 ?_
TYPE OF LOOPBACK (1=INTERNAL, S=STAGGERED,
                  3=25PIN CONNECTOR, 4=MODEM): (0) 2 ?_
INTERRUPT BR LEVEL: (0) 4 ?_

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?_
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE (D) 0 ?_

CVDHB DVC FTL ERROR 00101 ON UNIT 00 TST 001 SUB 000 PC: 021354

DEVICE REGISTER ACCESS ERRORS
BUS TIME-OUT TRAP CAUSED BY READ ATTEMPT
BUS TIME-OUT TRAP CAUSED BY WRITE ATTEMPT
DHV MAY BE AT THE WRONG Q-BUS ADDRESS.

 UNIT    0 DROPPED FROM FURTHER TESTING

PASS ABORTED FOR THIS UNIT
CVDHB EOP  1
    1 CUMULATIVE ERRORS

DR>
```

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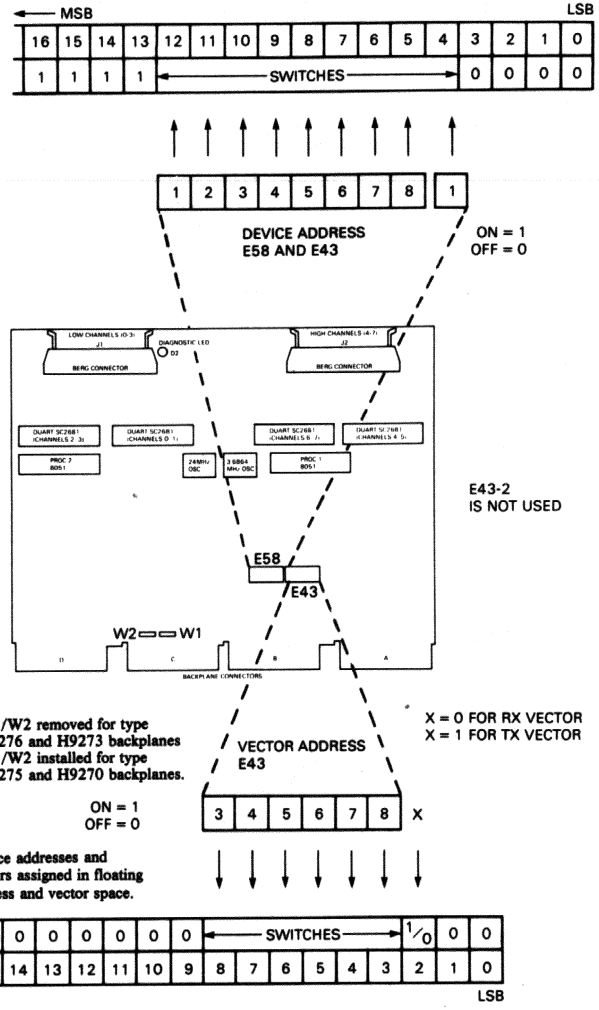
digital

EK-DHV11-MC

DHV11 MAINTENANCE CARD

JUMPER AND SWITCH LAYOUT



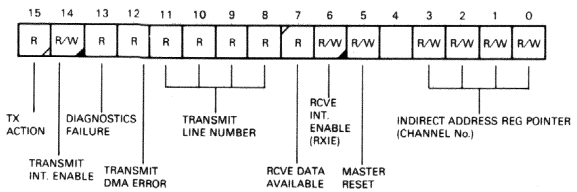
DIAGNOSTICS

PDP-11	**CVDHA?, CVDHB? and CVDHC? Functional Verification Test.**
System needs:	**Q-bus CPU, 32K memory, console terminal, DHV11 and XXDP+ load device with DRS.**
Prerequisites:	**All Q-bus diagnostics should run successfully.**

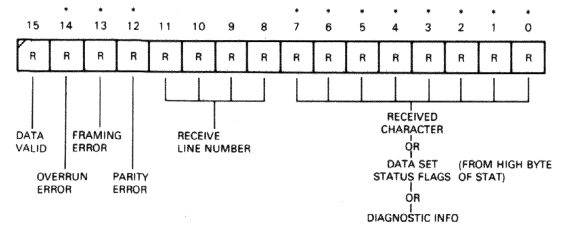
Error-free execution time: CVDHA? (15 s) CVDHB? (70 s) CVDHC? (4 min)

DHV11 REGISTERS

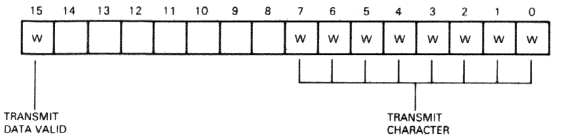
CSR (BASE)



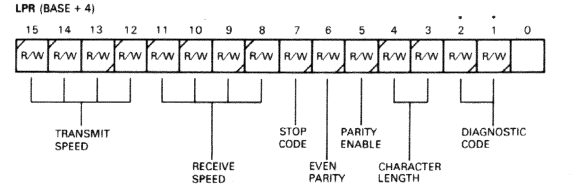
RBUF (READ BASE + 2)



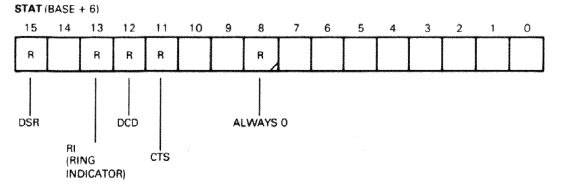
TXCHAR (WRITE BASE + 2)



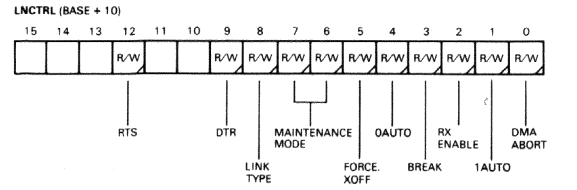
LPR (BASE + 4)



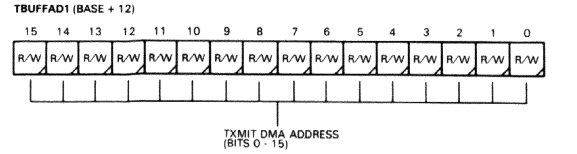
STAT (BASE + 6)



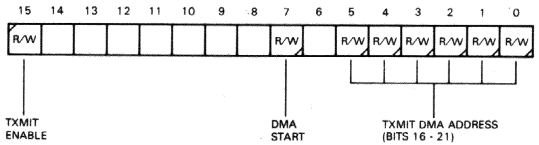
LNCTRL (BASE + 10)



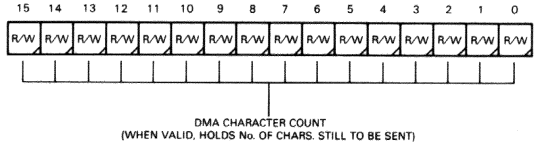
TBUFFAD1 (BASE + 12)



TBUFFAD2 (BASE + 14)



TBUFFCT (BASE + 16)



= CLEARED BY MASTER RESET

= SET BY MASTER RESET

= CLEARED BY BINIT, POWER-UP OR POWER-DOWN BUT NOT BY MASTER RESET

REGISTER CODES

LPR<15:12> and <11:8> Data Rate.

Code	Rate(bits/s)	Group
0000	50	A
0001	75	B
0010	110	A and B
0011	134.5	A and B
0100	150	B
0101	300	A and B
0110	600	A and B
0111	1200	A and B
1000	1800	B
1001	2000	B
1010	2400	A and B
1011	4800	A and B
1100	7200	A
1101	9600	A and B
1110	19200	A and B
1111	38400	A

LPR<4:3> Character Length

Code	Length
00	5 bits
01	6 bits
10	7 bits
11	8 bits

LPR<2:1> Diagnostics Code

Code	Meaning
00	Normal operation
01	Request for BMP report

Note: Code 305_8 = no error
All other BMP codes = error

LNCTRL<8> Link Type.

Code	Meaning
0	Data lines only
1	Full modem control

LNCTRL<7:6> Maintenance Mode

Code	Mode
00	Normal operation
01	Auto echo mode
10	Local loopback
11	Remote loopback

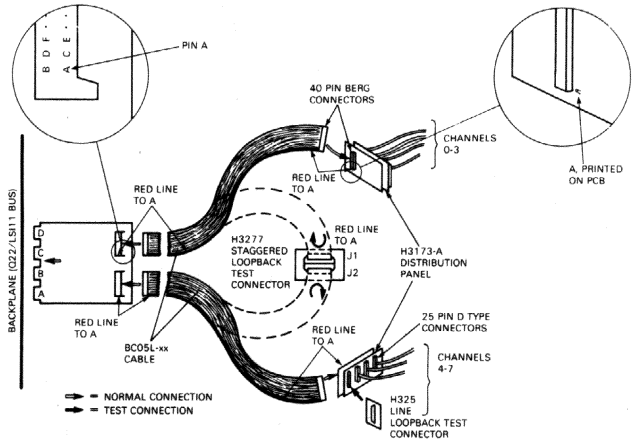
Self-Test Codes

Codes 201_8 or 203_8 = no error
Code Onnnnnn1 indicates ROM version nnnnnn.
Other codes = error (Refer to DHV11 Technical Manual EK-DHV11-TM)

Note

After the DHV11 is reset, CSR<3:0> may point to a non-existent channel. To access chanels 0 to 7, write channel number to CSR<3:0>.

INTERCONNECTION DIAGRAM



NOTE: BC05L-01 = 30.48 CM (12 INCHES)
BC05L-1K = 53.34 CM (21 INCHES)
BC05L-2F = 76.2 CM (30 INCHES)

FOUR STEPS TO RUN A SUPERVISOR DIAGNOSTIC

1. Enter the start command.

   When the prompt DR> is issued, type:

   STA/PASS:1/FLAGS:HOE<CR>

   The switches and flags are optional.

2. Answer the hardware parameter questions.

   The program prompts with:

   CHANGE HW?

   You must answer Y to this query if you want to change the hardware parameter tables. The program will then ask a number of hardware parameter questions in sequence. For example, the first question is:

   # UNITS?

   At this point, enter the number of units to be tested.

   NOTE

   Some versions of the diagnostic supervisor do not ask the CHANGE HW? question at the first start command. Instead they go straight into the hardware parameter question sequence.

The answers to the questions are used to build hardware parameter tables (P-tables) in memory. A series of questions is posed for each device to be tested. A hardware P-table is built for each device.

3. Answer the software parameter questions.

   When all the hardware P-tables are built the program responds with:

   CHANGE SW?

   If other than default parameters are wanted for the software, type Y. If the default parameters are wanted, type N.

   If you type Y, a series of software questions will be asked and the answers to these will be entered into the software P-table in memory. The software questions will be asked only once, regardless of the number of units to be tested.

4. Diagnostic execution

   After the software questions have been answered, the diagnostic starts to run.

   What happens next is determined by the switch options selected with the start command, or errors occurring during execution of the diagnostic.

DHV11 TECHNICAL MANUAL
EK-DHV11-TM-001

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